Fully-integrated inductive switched-mode DC-DC converters

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

SINGAPORE

**FULLY-INTEGRATED INDUCTIVE
SWITCHED-MODE DC-DC CONVERTERS**

SUN YIN

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

2020

**Fully-Integrated Inductive
Switched-Mode DC-DC Converters**

Sun Yin

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirements for the degree of
Doctor of Philosophy

2020

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarized materials, and has not been submitted for a higher degree to any other University or Institution.

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Sun Yin

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I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

24 March, 2020

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Date

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Prof. Joseph S. Chang

Authorship Attribution Statement

This thesis contains material from 2 papers submitted to the following peer-reviewed journals where I am the first author, and from a provisional patent where I am a co-inventor.

Chapter 3 is submitted as **Y. Sun**, V. Adrian, and J. S. Chang, “Modeling and Power Analysis of Fully-Integrated Switched-Mode DC-DC Converters with Bonding Wire Inductors,” *IEEE Transactions on Power Electronics*, 2020 (Reviewed and recommended for resubmission).

The contributions of the co-authors are as follows:

- I derived the analytical expressions, conducted the simulation and measurements, and prepared the manuscript drafts.
- Dr. Victor Adrian revised the manuscript.
- Prof. Joseph S. Chang provided the initial project direction, revised and proofread the manuscript.

Chapter 4 is submitted as **Y. Sun**, V. Adrian, J. S. Chang, K. Cui, and B. H. Gwee, “A Randomized Modulation Scheme to Mitigate Harmonics and Output Ripple Noise for Multi-Phase DC-DC Converters,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2020 (Reviewed and recommended for resubmission).

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- I derived the analytical expressions, conducted the simulations, and prepared the manuscript drafts.
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- Prof. Joseph S. Chang provided the initial project direction, revised and proofread the manuscript.
 - Dr. Cui Keer contributed to the analytical expressions.
 - Prof. Gwee Bah Hwee proofread the manuscript.

A small section of Chapter 3 was extracted from a provisional patent that is currently being filed by NTUitive and where I am a co-inventor.

24 March, 2020

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Summary

This Ph.D. research program pertains to single-phase (fully-integrated) and multi-phase (both fully-integrated and non-fully-integrated) inductive DC-DC converters. The general objectives are analytical investigations, proposal of a power optimization methodology, and a novel modulation scheme, and the ensuing designs of these DC-DC converters to improve one or more of the following attributes over the state-of-the-art: high power-efficiency, small form-factor, low input harmonics, and low output noise.

For the single-phase converter, the objectives include the modeling and power analysis for power-efficiency optimization, where the inductor is a bonding wire whose Q is moderate (ranging from 6-30), and a proposed power optimization methodology. The intended model and analysis are comprehensive where the ensuing proposed power-efficiency optimization accounts for both AC and DC power losses of the bonding wire inductor in a fully-integrated converter, and that can be applied to both continuous conduction mode and discontinuous conduction mode operations. Our model further encompasses analytical power loss expressions of the power transistors and their gate drivers. Our proposed model is verified with >90% accuracy through simulations and on the basis of physical measurements. We

provide applications of our model in three perspectives: bonding wire length, power losses and their ensuing optimization, and different CMOS processes. Our proposed model is useful as it provides valuable insights into the design of fully-integrated converters and the mechanisms for power-efficiency.

For the multi-phase converter, the objectives include the proposal of a randomized modulation scheme, and analysis and demonstration of its efficiency. The proposed scheme is denoted "Randomized Wrapped-Around Pulse Position Modulation scheme with Wrapped-Around Phase-Shifts (RWAPPM+WAPS)". To the best of our knowledge, this is the first-ever application of a randomized modulation scheme for a multi-phase converter. Our proposed scheme involves randomizing the pulse positions in the first phase to spread out the harmonic power, wrapping around the pulse shifts in other phases to reduce the overlapped pulses and hence mitigating the output noise, and if necessary, augmenting additional phases to further mitigate the output noise. We derive an analytical expression to predict the input current spectrum and show that our proposed RWAPPM+WAPS simultaneously mitigates both the input current harmonics and the output noise. For example, for a three-phase converter employing our proposed RWAPPM+WAPS, the peak input current spectral power and output noise ripple are simultaneously significantly reduced over the same converter employing a conventional randomized modulation scheme—by 3.6 dB (equivalent to $3.3\times$) and 200.3 mV (equivalent to

9.9×), respectively. Put simply, the proposed scheme is unique and advantageous as it mitigates both input harmonics and output noise for multi-phase converters.

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List of Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter
CCM	Continuous-Conduction Mode
CCM	Continuous Conduction Mode
CMOS	Complementary Metal-Oxide Semiconductor
COTS	Commercially-Off-The-Shelf
dB	Decibel
dBFS	Decibel with respect to Full Scale
DC	Direct Current
DC-DC	Direct-Current to Direct-Current
DCM	Discontinuous-Conduction Mode
DCM	Discontinuous Conduction Mode
DRAM	Dynamic Random-Access Memory
EEPROM	Electrically Erasable Programmable Read-only Memory
EMI	Electromagnetic Interference
ESR	Effective Series Resistance
HWADC	Hybrid Window ADC
IC	Integrated Circuits

List of Abbreviations

IoTs	Internet-of-Things
LFSR	Linear Feedback Shift Register
LNA	Low-Noise Amplifier
MIM	Metal-Insulator-Metal
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NMOS	n-channel Metal-Oxide Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PMOS	p-channel Metal-Oxide Semiconductor Field-Effect Transistor
PSiP	Power Supply in Package
PWM	Pulse Width Modulation
PwrSoC	Power Supply on Chip
RBW	Resolution Bandwidth
rms	root mean square
RWAPPM	Randomized Wrapped-Around Pulse Position Modulation
RWAPPM+WAPS	Wrapped-Around Pulse Position Modulation scheme with Wrapped-Around Phase-Shifts
SoC	System-on-Chip
SRAM	Static Random-Access Memory

Chapter 1

Introduction

1.1 Motivation

The global market for (ultra-)low-power portable electronic devices is gargantuan and growing rapidly. For example, the market for tablets and smartphones is estimated to reach more than 2.3 billion units by 2021, and the market for the Internet-of-Things (IoTs) is expected to grow to \$520 billion by 2021 [1], [2]. These devices are increasingly intelligent due to an increasing array of analog, digital and mixed-signal Integrated Circuits(ICs)/System-on-Chip (SoC), and sensors embodied therein.

Typically, voltage converters are employed therein to convert the battery voltage into different voltages for the various circuits in the ICs/SoCs and sensors. As these low-power devices are often constrained by the limited-energy battery and small form-factor, it is important that the voltage converters embodied therein similarly feature small IC area and with as few external passive components (or none at all) as possible for small overall form-factor, and feature high power-efficiency for a long

battery lifespan.

The power management of low-power devices with a power demand in the range of 5-500 mW, such as tablets, smartphones, and IoTs with WiFi connectivity, generally employ inductive switched-mode DC-DC converters (inductive converters) and low drop-out voltage regulators (LDOs). Inductive converters typically feature high power-efficiencies, where $\geq 80\%$ is common for commercially-off-the-shelf (COTS) converters. These converters, nonetheless, require off-chip passive filter components, i.e., inductors and capacitors, that are bulky and costly in terms of PCB area. On the other hand, linear voltage regulators, particularly capacitor-less LDOs, can be easily fully integrated on-chip. However, they can only perform step-down voltage conversions, and their power-efficiency is low when the drop out voltage is high, i.e., when the battery is fresh when its output voltage is higher.

Contemporary switched-mode DC-DC converters are designed to operate at increasingly high frequencies, ranging from tens of MHz to GHz [3]–[10]. The impetus for this trend is largely due to the reducing form-factor of the required passive components with the increasing operating frequency. Consequently, DC-DC converters may be fully physically-integrated where all their associated passive components are realized monolithically on-chip or integrated within the package encapsulating the converter IC. In view of the plethora of contemporary complex portable electronic devices, such fully-integrated converters offer smaller

form-factor, higher power density and lower cost advantages when compared to their conventional counterparts with bulky and typically more expensive off-chip/off-package components.

Based on the specific type of passive components, converters can be generally categorized into either capacitive or inductive converters. In general, inductive converters are preferred in practice because they typically feature lower sensitivity to load current variations, higher power-efficiency and higher power-density [3].

To delineate the challenges of designing and realizing a small form-factor inductive converter (with good power-efficiency), consider the block diagram of a conventional converter in Figure 1.1. The converter consists of a controller, power switches, and a passive filter. The controller controls the turning on and off of the power switches and generates digital-like width-modulated pulses. The passive filter embodies passive components to average the pulses from the power switches, thereby largely obtaining a DC output voltage. The controller takes the output voltage as feedback and adjusts the on and off timing of the power switches to ensure the output voltage is as desired.

These fully-integrated converters are often realized as part of a power management system, packaged as a Power Supply in Package (PSiP) [11], [12], or fabricated together with other systems as an IC with a Power Supply on Chip

Figure 1.1: Block diagram of a conventional buck DC-DC converter

(PwrSoC) [6]. In the somewhat expensive and complex PSiP approach, the ICs/SoCs and the passive filter components are placed on separate substrates that are subsequently joined via bumps. This allows the passive components to be realized using different technologies. Conversely, in the more common approach, the active circuits and the passive components are monolithically integrated, often within the SoC. In particular, the on-chip inductors realized using standard CMOS processes are of low quality, suffer from low inductance values (≤ 5 nH at 100 MHz switching-frequency), and require a fairly large die area. Of particular pertinence, compared to their external counterparts, these integrated passive components suffer from a low quality (Q) factor that severely compromises the overall power-efficiency of the converter. In short, these two approaches, especially the PwrSoC approach,

have limited applications to low cost yet high power-efficiency fully-integrated converters.

In view of the aforesaid fully-integrated inductive converters, it is desirable to employ a low-cost yet moderate or high quality-factor (Q) inductor in the switching frequency range—generally ≥ 50 MHz and ≤ 500 MHz in the literature [3]–[10]—of the fully-integrated converters. Compared to low Q (< 6) on-chip spiral metal inductors, bonding wire inductors—employing the parasitic inductance of bonding wires—typically feature moderately higher Q (ranging from 6 to 30) [13], [14], and depending on the geometry, higher inductance with relatively small variations ($< 5\%$) [15]. Further, as the latter is readily available in most packages, they are also often more cost-effective compared to other in-package inductors, such as inductors on magnetic substrate [11] or inductors on stacked chips [12].

Put simply, the bonding wire inductor is a good contender as the inductor for fully-integrated inductive converters. Largely for this reason, our work focuses on fully-integrated inductive buck converters (with bonding wire inductors) for ultra low-power and low-power portable applications, including sub-miniature IoTs where small form-factor and high power-efficiency are two critical design considerations.

Consider now, the losses in fully-integrated buck converter. The AC power loss of the integrated moderate- Q inductors can be considerable in fully-integrated

converters operating at high switching frequencies (≥ 50 MHz). This power loss should hence be accounted for the power analysis of the converter. Interestingly, this power loss is ignored in literature [16] largely because it is typically insignificant in conventional converters due to the employment of higher- Q external inductors and to the relatively lower switching frequencies (< 1 MHz). Further, because the inductance of integrated inductors is typically low (< 10 nH), fully-integrated converters are more likely to operate in the lower power-efficiency discontinuous-conduction mode (DCM) vis-à-vis the higher power-efficiency continuous-conduction mode (CCM). In DCM, the inductor current typically suffers from high current ripple [17] where the AC power loss of the integrated inductor (in DCM) is undesirably exacerbated. In short, reported power-loss models of the inductor in converters, are somewhat incomplete and insufficiently in-comprehensive.

At this juncture, this lack of a comprehensive model inadvertently leads to an incomplete optimization of fully-integrated high-frequency inductive converters (with bonding wire inductors) for high power-efficiency. Specifically, most reported models [16], [18] allows for the optimization of conventional converter designs that employ external high- Q inductors and that operate at moderately low switching frequencies (< 1 MHz), hence not entirely applicable to fully-integrated converters (with moderate- Q inductors and high switching frequencies). Other reported

models [3], [19] allow for an incomplete optimization of fully-integrated converter designs based on simplified inductor power loss models only for CCM, whereas fully-integrated converters may operate in both CCM and DCM.

From a power-efficiency optimization perspective, there is a need to comprehensively model and analyze the power loss mechanisms of fully-integrated converters embodying moderate- Q bonding wire inductors, with an emphasis on inductor AC loss, that can be applied to both CCM and DCM.

In terms of signal processing in converters—the modulation scheme in the controller in Figure 1.1—the converters generally employ Pulse Width Modulation (PWM) scheme. The modulation generates control signals that drive the on and off of the power switches depicted in Figure 1.1. The PWM scheme is a hardware-efficient algorithm that can be easily realized. However, because of the PWM, the frequent switching activities (on and off) of the power switches can render undesired strong harmonics at multiples of the switching-frequency [20], [21] and the power of the harmonics can be large and comparable to the output DC power of the converter. The strong harmonics are undesirable in two ways.

First, the harmonics can generate conducted electromagnetic interference (EMI) noise traveling through the power line [21], [22], causing interference to nearby electronic circuits. Second, the harmonics can generate radiated EMI noise when

traveling through the metal traces (akin to an antenna) at the output to circuits near the converter [23]. The harmonics are generally limited $\leq 5\%$ in a 'standard' power application of EN50160 [24]. Although the harmonics may be attenuated by adding passive EMI filters, it incurs increased cost and form-factor drawbacks [25].

To mitigate the harmonics, randomized modulation schemes are often employed in place of PWM. These schemes randomize one or more modulation parameters, such as the switching frequency [26]–[28], pulse position [29], [30], and the pulse width [31], to spread the power of the switching-frequency harmonics over the input current spectrum. The ensuing peak power of the harmonics can be desirably lower than the PWM.

Amongst the reported randomized modulation schemes, the Randomized Wrapped-Around Pulse Position Modulation scheme (RWAPPM) [30] features one of the simplest algorithm and high attenuation of the harmonic power in its output voltage. The RWAPPM achieves the high attenuation by means of adding a random delay before the pulse in each switching-period, but at the cost of exacerbated output noise due to the randomized delays [30].

To mitigate the output noise, converters [32]–[34] usually employ the multi-phase architecture vis-à-vis the single-phase architecture. This is because the multi-phase architecture offers worthwhile attributes, including reduced filter

capacitance, improved thermal performance and efficiency, and improved load transient performance [35].

A typical multi-phase DC-DC converter with N identical phases is depicted in Figure 1.2, where each phase comprises a pair of gate drivers, power transistors, gate drivers and a phase inductor. All N phases are connected in parallel and share the single output capacitor, C_{out} . The modulator generates the gate control signals to turn on and off the power transistors, creating output pulses (V_1 to V_N) in different phases (Phase 1 to Phase N), respectively.

Figure 1.2: Block diagram of an N -phase switched-mode DC-DC buck converter

The modulation of the multi-phase DC-DC converter is usually based on the

conventional PWM scheme [35], [36], where the output pulses of all the phases in a switching period have identical width, but are delayed in sequence by $2\pi/N$ phase shift after Phase 1 to Phase N . Nonetheless, we will show in detail later (Chapter 4) that the randomized modulation scheme, RWAPPM, is not entirely applicable to multi-phase converters. This is because the output pulses of each phase can negate the ripple noise cancellation advantage in the current of the output capacitor, i_C , as all phase currents, i_{ph} , now occur randomly (due to the randomized V_1 to V_N) and may not cancel each other out. Hence, although the input harmonics are mitigated, the output noise is undesirably exacerbated.

Put simply, there is a need for a cost- and form-factor-efficient method applicable to multi-phase converters to simultaneously mitigate the input current harmonics and the output noise.

In summary, the lack of a comprehensive model for power efficiency optimization of a single-phase fully-integrated converter and a randomized modulation scheme for low-harmonics low-noise of a multi-phase converter renders the strong motivations to comprehensively investigate the power loss mechanisms and to propose novel randomized modulation scheme for the aforesaid converters.

1.2 Objectives

The overall objectives of this Ph.D. research program pertain to single-phase and multi-phase inductive DC-DC converters. For the former, the objectives include the modeling and power analysis for power-efficiency optimization of a single-phase fully-integrated inductive DC-DC converter with a bonding wire inductor. The primary intention of these objectives is the derivation of a comprehensive model that accounts for both the AC and DC power losses of the bonding wire inductor, and its applicability to both CCM and DCM operations of the fully-integrated converter. For the latter, the objectives include the proposal and verification of our proposed randomized modulation scheme for a multi-phase (fully-integrated and non-fully-integrated) inductive DC-DC converter—to the best of our knowledge, a randomized modulation scheme has never been applied to a multi-phase converter. The primary intention of the proposed randomized modulation scheme is to efficiently and simultaneously mitigate both the input harmonics and output noise of a multi-phase converter.

For the single-phase converter, the specific objectives are to:

- (i) Derive a comprehensive model for optimizing the power efficiency of a single-phase fully-integrated inductive buck converter with a moderate- Q bonding wire inductor,

- (ii) Derive analytical expressions that model both the DC and AC power losses of the bonding wire inductor, applicable to both CCM and DCM operations of the fully-integrated converter, and power loss expressions of the power transistors and their gate drivers, and
- (iii) To design and realize a single-phase fully-integrated converter prototype and to verify the proposed model.

For the multi-phase converter, the specific objectives are to:

- (a) Propose a randomized modulation scheme applicable to multi-phase converters to simultaneously mitigate the input harmonics and output noise,
- (b) Derive an analytical model of the proposed modulation scheme that elucidates the non-linearities, including harmonics and the noise floor that are present in the input current, and can depict the mechanisms, i.e., identify the parameters that affect the said non-linearities,
- (c) Design a digital modulator design employing the proposed modulation scheme, and
- (d) Demonstrate the efficacy of the proposed modulation by means of simulations and measurements.

1.3 Contributions

The contributions made in this Ph.D. research program are congruous to the overall specific objectives outlined above.

For the single-phase converter, our contributions include:

- (i) A comprehensive model for optimizing the power efficiency of a single-phase fully-integrated inductive buck converter with a moderate- Q bonding wire inductor; see Chapter 3 later. Our model provides valuable insights into the design of fully-integrated converters and the mechanisms for power efficiency.
- (ii) The derivation of analytical expressions that include both the DC and the AC power losses of the bonding wire inductor, and the power loss of the power transistors and their gate drivers. Our expressions emphasize the considerable AC losses of the inductor that were previously ignored or inadvertently assumed to be negligible in reported works, and the power loss of the gate drivers that includes their readily determined design parameters.
- (iii) Simulations and measurements of a single-phase fully-integrated converter prototype with a bonding wire inductor in a CMOS 65nm IC process, depicted a good agreement ($>90\%$ accuracy) between the analytical (from our derived expressions), simulated (SPICE), and measured (from the prototype IC) power-efficiencies.

For the multi-phase converter, our contributions include:

- (a) Proposal of the Randomized Wrapped-Around Pulse Position Modulation scheme with Wrapped-Around Phase-Shifts (RWAPPM+WAPS) that can efficiently and simultaneously mitigate harmonics and output noise of multi-phase converters; see Chapter 4 later. We achieve this by randomizing the pulse positions to spread out the harmonic power, by wrapping around the pulse shifts in other phases to reduce the overlapped pulses, and if necessary, by adding additional phases to further mitigate the output noise.
- (b) A rigorous mathematical analysis of the proposed RWAPPM+WAPS, including the expressions of randomized input current, the DC power, the noise spectrum, and the power of switching-frequency harmonics. Our analytical expressions elucidate the non-linearities, including harmonics and the noise floor that are present in the input current, and can depict the mechanisms, i.e., identify the parameters that affect the said non-linearities. Our derived expressions provide valuable insights for designers as a tool in the early design cycle of the converter to explore the trade-offs between various parameters and to ascertain their effects on the spectrum.
- (c) A digital modulator design employing the proposed RWAPPM+WAPS for an N -phase converter. Our digital modulator design can be realized by using digital gates only, hence practically easy to implement and hardware-efficient.
- (d) A demonstration of the efficacy of the proposed modulation by means

of investigations on a two-phase and a three-phase converter employing our proposed RWAPPM+WAPS and our earlier proposed RWAPPM, respectively. The results show that for a three-phase converter employing our proposed RWAPPM+WAPS, its peak input current spectral power and output noise ripple are significantly reduced over the same converter employing RWAPPM—by 3.6 dB (equivalent to $3.3\times$) and 200.3 mV (equivalent to $9.9\times$), respectively.

1.4 Thesis Organization

The remainder of this thesis are organized in the following manner.

Chapter 2 reviews the different converter topologies, inductor integration technologies, power loss types and the conventional randomized modulation schemes. The emphasis of the review is on the limitations/trade-offs of these design techniques and control methodologies, and the inadequacy of reported state-of-art work to mitigate these limitations/trade-offs.

Chapter 3 presents the modeling and power analysis of fully-integrated switched-mode DC-DC converters with bonding wire inductors. Our proposed model includes analytical expressions that model both the DC and AC power losses of the embodied bonding wire inductor, and applies to both CCM and DCM operations.

In this chapter, the inductor power losses are first modeled, followed by the modeling of power transistor related power losses. Thereafter, the simulation and measurement results are presented. Finally, the applications of the proposed model are discussed, followed by the conclusions.

Chapter 4 presents our proposed randomized modulations scheme to mitigate harmonics and output ripple noise of multi-phase DC-DC converters. To the best of our knowledge, this is the first-ever a randomized modulation scheme applied to multi-phase converters that can efficiently and simultaneously mitigate the input current harmonics and the output noise. In this chapter, the proposed RWAPPM+WAPS is first introduced, followed by the rigorous analytics of the input current spectrum of the RWAPPM+WAPS. Thereafter, a digital modulator of the RWAPPM+WAPS is presented. Finally, the simulation results and benchmarking are presented, followed by the conclusions.

Chapter 5 draws the conclusions of this thesis and suggests recommendations for future work.

Chapter 2

Literature Review

In this chapter, we will provide a comprehensive review of different topologies of switched-mode DC-DC converters with an emphasis on inductive converters. Thereafter, we will review state-of-the-art inductor integration technologies, power loss types of the converters, and conventional randomized modulation schemes. Our literature review in this chapter serves as a preamble to our contributions delineated in the following Chapter 3 and 4.

This chapter is arranged in the following manner. Section 2.1 reviews the DC-DC buck converter topologies. Section 2.2 reviews inductor integration technologies. Section 2.3 presents the power loss mechanisms of the inductive buck converter, and Section 2.4 provides a review of conventional randomized modulation schemes. Section 2.5 draws the conclusions.

2.1 Overview of DC-DC Converter Topologies

As delineated in Chapter 1, a DC-DC converter is a critical sub-system in portable devices, where as a constituent of the power management unit, it converts the varying battery voltage to a stable output voltage with low noise. The key performance parameters of DC-DC converters include high power-efficiency and small form-factor. At this juncture, the design art of DC-DC converters is mature and they can be generally categorized into three topologies: linear voltage regulators, switched-capacitor (SC) converters, and inductive converters.

Linear voltage conversion is the most mature topology of DC-DC conversion methods; they are also known as LDO (Low Drop Out) where the difference between the output and input voltage is low, e.g., 50 mV difference. Linear voltage regulators can be fully integrated on-chip. However, they can only perform step-down voltage conversions and suffer from poor power-efficiencies particularly when the drop-out voltage is high. Nevertheless, their primary advantage is that their output is often very stable with very low noise and high power supply rejection ratio (PSRR). A comprehensive review of linear regulators may be found in numerous texts and articles, including [12]–[15].

In most general applications, converters are preferred over LDOs for their high power-efficiency. In applications where high stability and low noise are imperative,

a converter followed by an LDO is preferred—in these applications, the overall power-efficiency remains high if the output-input difference to the LDO is small. Compared to linear voltage regulators, converters suffer from large form-factor as they require bulky external passive components, which do not easily lend themselves to monolithic integration.

In the following sub-sections, we will review the two major switched-mode DC-DC converter topologies.

2.1.1 Switched-Capacitor Converter

The switched-capacitor (SC) converter, also known as the charge-pump voltage regulator, is a switched-mode inductor-less voltage conversion topology that utilizes capacitors as the energy storage elements. As a means to scale voltage as part of the DC-DC voltage conversion process, switches are used to transfer stored energy from one capacitor to another capacitor. The design-art of SC converters is mature [9], [37], [38]. Based on the output voltage, an SC converter can be the SC buck converter type where the output voltage is lower than the input, or the SC buck-boost converter type where the output voltage may be higher or lower than the input voltage.

A simplified SC buck converter schematic is depicted in Figure 2.1(a) [39]. It consists of four power switches ($S_1 - S_4$), and two capacitors (C_1, C_2) as the energy

storage elements.

Figure 2.1: SC buck converter: (a) simplified schematic, and (b) power-efficiency ($\eta_{sc-buck}$) plots against voltage conversion ratio

The switches are turned on and off periodically at switching-frequency f_{sw} .

The ideal output voltage, V_{out} , and the ideal power-efficiency, $\eta_{sc-buck}$, are given by [40]

$$V_{out} = k \cdot V_{in} = \frac{R_{load} f_{sw} C_1}{1 + 2R_{load} f_{sw} C_1} \cdot V_{in} \quad (2.1)$$

$$\eta_{sc-buck} = \frac{C_1 + 2(C_2 + C_1)k + 4C_2k^2}{2C_2 + 4C_1 - 4C_1k} \quad (2.2)$$

From Equation (2.1), the maximum V_{out} , that can be obtained is half of the input voltage. In other words, the voltage conversion ratio, k , cannot be >0.5 . The $\eta_{sc-buck}$ plots obtained using Equation (2.2) are depicted in Figure 2.1(b). The best power-efficiency curve is obtained when C_1 is significantly larger than C_2 , while the

worst power-efficiency curve is obtained when C_1 is significantly smaller than C_2 . The shaded area represents all other possible power-efficiency curves for different combinations of C_1 and C_2 values.

The disadvantages of the SC converters in practical implementations include two parts. First, the operation of the SC converters relies on periodically charging/discharging the capacitors through switches which are resistive due to their ‘on’ resistance, etc. Consequently, the power losses of an SC converter are typically high, leading to poor power-efficiency characteristics. Second, in order to maintain a minimum output voltage, a certain amount of charge has to be maintained across each energy storage capacitor. In varying load current conditions, a complex and high power-consuming control circuit is required [39], [41]–[43], further compromising the efficiency of the SC converter. In view of the disadvantages, the SC converters are typically implemented in applications that do not require tight voltage regulation [44].

2.1.2 Inductive Converter

Unlike the SC converters, an inductive converter utilizes a capacitor and an inductor as the energy storage elements. The design-art of the inductive converter is also mature [17] and a number of design/application variations have been reported

[45]–[49]. These designs include the buck converter, boost converter, inverting buck-boost converter, bridge converter, three-level buck converter, Watkins-Johnson converter, etc. In this Ph.D. program, we will focus on the buck converter for the purpose of our intended applications.

2.1.2.1 Single-Phase Inductive Buck Converter

Figure 2.2 depicts the simplified block diagram of a single-phase fully-integrated inductive synchronous buck converter. The converter comprises a controller, gate drivers, a high-side power transistor M_p and a low-side power transistor M_n , and an LC low-pass filter including an inductor, L , and an output capacitor, C_{out} . Power transistors, M_p and M_n , and the filter inductor L form the single phase of the converter.

Figure 2.2: Simplified block diagram of a single-phase inductive buck converter

During each switching period T , the controller controls the gate drivers to drive the power transistors on and off, delivering the stored from input V_{in} to output V_{out} via the inductor. The inductor stores energy during the charging phase and delivers the stored energy to the load during the discharging phase. The filter capacitor smooths V_{out} .

Depending on the load conditions, the inductive buck converter can operate in either a continuous conduction mode (CCM) or a discontinuous conduction mode (DCM). Figure 2.3(a) and 2.3(b) depict the ideal periodic current (i_L) waveforms of the inductor in the fully-integrated converter operating in CCM and DCM, respectively.

Figure 2.3: Ideal periodic inductor current i_L waveforms in (a) CCM and (b) DCM

The i_L comprises two components: DC component, I_{out} , and AC component (ripple current), Δi_L . It is well established [50] that the inductor current waveforms in CCM and DCM are different.

When the converter operates in CCM in Figure 2.3(a), the load condition is heavy (i.e., the output current, I_{out} , is large) and the inductor current, i_L , periodically ramps up for duration DT and down for D_1T , where $D + D_1 = 1$. The inductor current i_L is always above zero. During DT , M_p is on and M_n is off, and during D_1T , M_p is off and M_n is on.

On the other hand, when the converter operates in DCM in Figure 2.3(b), the load condition is light (i.e., I_{out} is small) and i_L periodically ramps up for duration DT , ramps down for D_1T , ramps to zero and remains at zero for $(1 - D - D_1)T$, where $D + D_1 < 1$. The power transistors, M_p and M_n , operate similarly as in CCM, but during $(1 - D - D_1)T$, both M_p and M_n are off.

2.1.2.2 Multi-Phase Inductive Buck Converter

The multi-phase architecture is generally employed in low-noise switched-mode DC-DC converters vis-à-vis the single-phase architecture. This is because the multi-phase architecture offers worthwhile attributes, including reduced filter capacitance, improved thermal performance and efficiency, and improved load

transient performance [35].

A typical multi-phase inductive DC-DC converter with N identical interleaved phases is depicted earlier in Figure 1.2. The modulation of the multi-phase DC-DC converter is usually based on the conventional PWM scheme [35], [36], where the output pulses of all the phases in a switching period have identical width, but are delayed in sequence by $2\pi/N$ phase shift after Phase 1 to Phase N . Figure 2.4 depicts the waveforms of a two-phase inductive buck converter employing PWM.

Figure 2.4: Waveforms of a two-phase converter employing PWM

The output pulses, V_2 of the power transistors in the second phase has a phase shift of π from V_1 . The ensuing inductor current in Phase 2, i_{ph_2} , is also shifted π from the inductor current in Phase 1, i_{ph_1} . i_{ph_1} and i_{ph_2} superpose at C_{out} , and due to the phase shift, these currents to a first-order cancel out each other. The resulting ripple of the capacitor current, i_C , is reduced, and thereby the output voltage ripple is also reduced.

2.1.3 Summary

This sub-section summaries the DC-DC converter topologies reviewed in Section 2.1. The process of charging and discharging of the inductor and the capacitor is ideally lossless. Unlike the SC converters, the power-efficiency of the inductive converters can in theory approach 100% regardless of the voltage conversion ratio and the output power [51]. Among the converter topologies, inductive voltage converters are the most widely used because they feature good output voltage regulation and high power-efficiency attributes. When compared to a single-phase architecture, inductive converters employing multi-phase architecture feature lower output noise. The primary drawback of inductive converters, however, is that they require inductors for energy storage and filtering, particularly in fully-integrated converters where the in-situ integration require high-quality filter inductors. This will now be reviewed.

2.2 Inductor Integration Technologies

Fully-integrated converters employ on-chip in-situ passive components while their non-fully-integrated converter counterparts employ external passive components. The passive components include resistors, capacitors, and inductors. Of these components, the integration of the inductor is the most challenging because in-situ inductors suffer from low Q factor, low inductance, high resistance and large area [16]. A number of techniques have been reported to realize in-situ inductors [17]–[27], including the inductor-on-silicon (IoS) approach where the inductor is realized on the same silicon of the converter, and the inductor-in-package (IiP) approach where the inductor is realized within the package of the converter.

As the inductor is a key component of the converter research in this Ph.D. program, we will now review the inductor integration technologies for these two approaches in this section. The on-chip inductors that will be discussed in Section 2.2.1 are the IoS approach. Hybrid inductors, inductors on stacked chips, inductors on magnetic substrates, inductors on printed circuit board (PCB) and bonding wires inductors, are IiP approaches and will be discussed in Section 2.2.2.

2.2.1 IoS Approach

2.2.1.1 On-Chip Inductors

On-chip inductors are realized by winding or spiraling available metal tracks in an IC. These inductors are monolithically integrated on the same die as the converter. As an example, Figure 2.5 depicts the microphotograph of a reported on-chip inductor for a monolithic converter [52].

Figure 2.5: An on-chip inductor for a monolithic converter [52]

The inductance and the parasitic resistance of the realized on-chip inductor in this reported example are 2 nH and 0.5 Ω , respectively. Other similar on-chip inductor designs have been reported, including [53], [54]. This design is popular for the integration due to the relatively simple structure and that no additional

processing is required. However, due to the high trace resistance and the high substrate-inter-layer capacitive coupling, the on-chip inductors generally suffer from low Q factors (<6) in the switching frequency range (≥ 50 MHz and ≤ 500 MHz) that most fully-integrated converters operate, and their performance is generally unacceptable for fully-integrated converters, but sometimes tolerated.

2.2.2 IiP Approach

2.2.2.1 Hybrid Inductors

The hybrid inductors can be integrated by fabricating the coils and the magnetic cores on the top of CMOS substrates using different materials and technologies. A reported [55] hybrid inductor is depicted in Figure 2.6, and consists of a magnetic core sandwiched between copper-based windings.

This fabricated inductor has dimensions of $5 \times 2 \times 0.25$ mm (width, length, thickness), and measures $1.25 \mu\text{H}$ at 1 MHz. As this technology requires additional processing steps, the overall fabrication is more complex than standard CMOS processes and consequently more expensive.

Figure 2.6: A hybrid inductor [55]

2.2.2.2 Inductors on Stacked Chips

The inductors can be realized in IC technology on a stacked chip with the converter. An example is depicted in Figure 2.7 [56].

The inductor is connected to the converter by flip-chipping the output filter chip on the converter chip using gold stud bumps and thermos compression bonding. The fabrication process used for the inductors can be different from the fabrication process of the active circuits to cut down the cost [57]. For example, the active circuits can be fabricated using an advanced 65nm IC process, while the inductor can be fabricated in another chip using a 180nm IC process at a lower cost. Implementing the inductor in an additional chip allows the use of thicker metal for the windings of the inductor as well as the deposition of ferromagnetic materials to increase the

Figure 2.7: Inductors realized on a stacked chip [56]

inductance and reduce the parasitic resistance. As a result of the integration of an additional chip and additional processing, the cost of integration is inevitably high.

2.2.2.3 Inductors on Magnetic Substrate

Instead of realizing on a chip, an inductor can be realized on a ferrite substrate [58], [59]. Figure 2.8 depicts the structure of a reported inductor [58] on a ferrite substrate integrated with the packaging of an IC chip.

The inductor utilizes a ferrite substrate as the magnetic core, where the substrate is the same size as the IC chip. The IC chip is directly bonded on the inductor using an ultrasonic flip-chip bonding method with a golden stud bump connection. The reported inductor has an inductance of $1.65 \mu\text{H}$ and 0.18Ω parasitic resistance at

Figure 2.8: An inductor integrated on magnetic substrate of packaging [58]

2 MHz. This integration technology takes advantage of the space available on the packaging substrate. However, it requires additional packaging processes and suffers from high fabrication cost.

2.2.2.4 Inductors on PCB

The inductors can also be fabricated in the PCB by patterning the copper layers on the PCB [60], [61], [62], [63]. Magnetic materials, e.g., ferrite polymer compounds (FPC), can be added to improve the quality of the inductors, as depicted in Figure 2.9.

Figure 2.9: Inductors realized on PCB [62]

The inductance of a reported inductor [62] is $95.7 \mu\text{H}$ at 450 kHz. In this approach, the PCB is utilized to fabricate inductors, requiring no additional processing of the converter IC fabrication. However, the performance of the inductors is limited due to the high interconnect resistance of the long traces [64].

2.2.2.5 Inductors on Bonding Wires

As conducting wires have parasitic inductance, the bonding wires for IC packaging can be used for realizing an integrated inductor [14], [65], [66]. A commonly configured Π -structure bonding wire inductor is depicted in Figure 2.10(a). The combined inductor is formed by the loop from V_x , or the output node of the power transistors, to a lead-frame, then to another lead-frame, and

Figure 2.10: A Π -structure bonding wire inductor (a) its physical implementation and (b) its simplified model

finally to the V_{out} feedback node. The two lead-frames are shorted together to form a loop of the bonding wires to further increase the parasitic inductance.

The electric characteristics of the bonding wire inductor are dependent on the physical implementation and geometry. Figure 2.10(b) depicts the simplified model of the Π -structure bonding wire inductor. The equivalent total inductance of the bonding wire inductor can be modeled as [67]

$$L_{\text{total}} = 2 \times (L_{\text{bond}} - M_{\text{bond}}) \quad (2.3)$$

$$L_{\text{bond}} = 2 \times l_{\text{seg}} \times \left[\ln \left(\frac{2l_{\text{seg}}}{r} \right) - 0.75 \right] \quad (2.4)$$

$$M_{\text{bond}} = 2 \times l_{\text{seg}} \times \left[\ln \left(\frac{2l_{\text{seg}}}{d} \right) - 1 + \frac{d}{l_{\text{seg}}} \right] \quad (2.5)$$

$$l = 2 \times l_{\text{seg}} \quad (2.6)$$

where

L_{bond} and M_{bond} are the self-inductance and mutual inductance in nH of the bonding wires, respectively,

l_{seg} is the length of the segmented bonding wires,

r is the radius of the bonding wire,

d is the spacing between the bonding wires, and

l is the total equivalent bonding wire length of the bonding wire inductor.

The bonding wire inductors have gained growing interest recently, especially for fully-integrated converters, due to their three salient advantages.

First, compared to low Q (<6) on-chip spiral metal inductors in Section 2.2.1.1,

bonding wire inductors typically feature moderately higher Q (ranging from 6 to 30) [13], [14], and depending on the geometry, higher inductance with relatively small variations ($<5\%$) [15]. For example, for the metric quad flat pack (MQFP) package, the inductance value of the packaging inductor therein can be 8-12 nH with $Q>8$ at 100 MHz [67], as depicted in Figure 2.11. This compares very favorably over 1.1 for an on-chip metal-track planar spiral inductor. This can translate to an advantageous average power-efficiency improvement of $>20\%$, when compared to a standard monolithically integrated CMOS DC-DC converter with an on-chip planar inductor [68].

Second, as bonding wires are readily available in most packages, bonding wire inductors are also often more cost-effective compared to other in-package inductors, such as inductors on stacked chips [12] in Section 2.2.2.2 or inductors on magnetic substrate [11] in Section 2.2.2.3.

Put simply, the bonding wire inductor is a good contender as the inductor for fully-integrated inductive converters, and hence the reason for its adoption in Chapter 3 (and in part for Chapter 4).

Figure 2.11: A spiral-shaped bonding wire inductor [67]

2.2.3 Summary

This sub-section summarizes the inductor integration technologies reviewed in Section 2.2. A general comparison between the IoS approach, the IiP approach is tabulated in Table 2.1. Of special interest, the bonding wire inductor, as one of the IiP approaches, is listed separately in the table for comparison.

The size of IoS inductors is generally smaller than that of IiP inductors. As IoS inductors are fabricated in batch on silicon wafers, the cost is generally lower than IiP

Table 2.1: Comparison of Inductor Integration Technologies

	IoS	IiP	Bonding Wire Inductor
Inductance	Small	Large	Moderate
Resistance	Large	Small	Moderate
Saturation current	Small	Large	Moderate
Core material options	Limited	Many	Usually Air
Output power	Small	Large	Moderate
Size	Small	Large	Small
Fabrication complexity	Simple	Complex	Simple
Cost	Low	High	Low

inductors. However, due to the limited conductor thickness of on-chip metal layers, the resistance of IoS inductors is generally high, and therefore, the Q is generally undesirably low. As most IiP inductors, on the other hand, require additional fabrication processing, the cost is generally high. In the case of the bonding wire inductor, it features higher Q than the IoS inductors due to the low resistance bonding wires, and much lower cost than the IiP inductors because no additional process is required, yet featuring small form-factor. Consequently, the bonding wire inductor is a good contender as the inductor for fully-integrated inductive switched-mode DC-DC converters. For these reasons, in this Ph.D. program, our research will target on a fully-integrated converter that will embody the moderate Q bonding wire inductor.

2.3 Inductive Converter Power Losses

The maximum power-efficiency of an inductive buck converter is ideally 100% [43]. However, in practice, due to the non-idealities present in the components of the converter, power losses occur and the ensuing power-efficiency is compromised. There are four types of power losses in a converter—conduction losses, switching losses, gate-drive losses, short-circuit losses and static losses. We will now review them in turn.

2.3.1 Conduction Losses

When current flows through non-ideal components, including the power switches and the on-chip inductor, conduction losses occur due to their equivalent series resistance (ESR) [18], [69]–[71]. On-chip capacitors usually have much smaller ESR compared to on-chip inductors, and for practical reasons, can thus be neglected in the converter designs. The conduction losses in PMOS, NMOS transistors and the inductor can be expressed, respectively, as follows

$$\begin{aligned}
 P_{p, \text{cond}} &= D \cdot i_{\text{rms}}^2 r_{p, \text{on}} \\
 P_{n, \text{cond}} &= (1 - D) \cdot i_{\text{rms}}^2 r_{n, \text{on}}, \text{ and} \\
 P_L &= P_{L, \text{dc}} + P_{L, \text{ac}}.
 \end{aligned} \tag{2.7}$$

where i_{rms} is the root-mean-square (rms) current, $r_{p, \text{on}}$ and $r_{n, \text{on}}$ are the respective conducting resistance of the PMOS and NMOS power transistor, and $P_{L, \text{dc}}$ and $P_{L, \text{ac}}$ are the DC power loss and AC power loss of the inductor, respectively. The total conduction loss, P_{cond} , of the converter is therefore

$$P_{\text{cond}} = P_{p, \text{cond}} + P_{n, \text{cond}} + P_L. \quad (2.8)$$

It is worth noting that conventional non-fully-integrated converters generally employ high- Q (>30) inductors and operate at low switching frequencies (<1 MHz). The ensuing inductor AC power loss, $P_{L, \text{AC}}$, is insignificant and therefore usually ignored in reported work [16], [18]. However, for fully-integrated converters operating at high switching frequencies (>50 MHz), due to the low or moderate Q (<30) of the integrated inductor, we will show later in Chapter 3 that $P_{L, \text{AC}}$ can be significant and hence should be accounted for in the power analysis.

Further, because the inductance of integrated inductors is typically low (<10 nH), fully-integrated converters are more likely to operate in the lower power-efficiency DCM vis-à-vis the higher power-efficiency CCM. In DCM, the inductor current typically suffers from high current ripple [17] where the AC power loss of the integrated inductor (in DCM) is undesirably exacerbated. Reported work [3], [19] simplified the modeling of inductor power loss only for CCM, whereas

fully-integrated converters may operate in both CCM and DCM.

In short, reported power-loss models of the inductor in converters are somewhat incomplete for fully-integrated converters, and the incomplete models may inadvertently lead to an incomplete optimization of fully-integrated high-frequency inductive converters (with bonding wire inductors) for high power-efficiency.

2.3.2 Switching Losses

The switching losses are due to the transistor on-and-off switching activities that charge and discharge the capacitive loads [18], [69]–[82], e.g., the gate of a power transistors and the next stage of inverters within its gate driver. As the equivalent capacitance of the power transistors and their gate drivers are large, the switching losses of the converter are dominated by the switching losses in the power transistors and their gate drivers therein [69]–[71], [75], [82].

The dominant switching losses of a power transistor and its gate driver can be estimated as [17]

$$P_{\text{sw}} = C_{\text{sw}} V_{\text{in}}^2 f_{\text{sw}} + C_{\text{driver}} V_{\text{swing}}^2 \cdot f_{\text{sw}}, \quad (2.9)$$

where C_{sw} and C_{driver} are the equivalent charging capacitance of the power transistor and its gate driver, respectively, and V_{swing} is the swing voltage of the gate driver.

Switched-mode DC-DC converters generally employ a tapered buffer structure [36] as the gate driver to drive the power transistor. Figure 2.12 depicts the structure of a tapered buffer.

Figure 2.12: Schematic of a tapered buffer

The tapered buffer structure comprises N stages of inverters where the channel width of each transistor in the inverter is a fixed multiple (tapering factor), F , larger than that of the preceding inverter. Generally, all the NMOS in the gate driver are sized at a constant ratio, β , over its PMOS counterpart such that each inverter stage has equal rise, fall, and delay times.

It is worth noting that the value of C_{driver} is dependent on the design parameters, i.e., N , F , and β , of the gate driver. In practice, the size of the power transistor is designed according to the required output power, i.e., a larger output power requires larger sized power transistors. To ensure sufficient drivability of the power transistors, gate drivers of larger N are required, and consequently, larger C_{drive} is

expected and more power will be dissipated in the gate drivers. In other words, C_{drive} is dependent on the design parameters (N , F , and β) and the size of the power transistors.

It is instructive to note that the analyses in reported work [83]–[85] either simply assumed that the power loss of the gate driver is a constant ratio of the power loss of the its driven power transistor [83], neglecting the design parameters of the gate driver, or empirically assumed a total gate charge value that has to be extracted from the datasheet [84], [85]. This shortcoming would mean that the reported ensuing modeled switching losses of the gate drivers may be inaccurately estimated, which may inadvertently lead to incomplete or poor optimization of the power-efficiency of the converter. We will delineate this shortcoming further in Chapter 3.

2.3.3 Short-Circuit Losses

During the rising and falling transitions of the PMOS and NMOS transistors, a short-circuit path [86] may exist for a short duration, t_s , and the ensuing short-circuit current, I_s , flows from the supply to the ground. These short-circuit loss can be generally expressed as

$$P_{\text{short}} = t_s V_{\text{in}} I_s. \quad (2.10)$$

The short-circuit losses can be significant, especially in converters employing large power transistors. However, the short-circuit losses can be significantly mitigated by established design techniques [87]–[91]. For example, by incorporating a dead-time controller to ensure that the power transistors are never turned on simultaneously, t_s can be significantly reduced to a negligible value. Put simply, by appropriate design, the short-circuit losses can be neglected in the power analysis. We will do this in our work in Chapter 3.

2.3.4 Static Losses

The CMOS transistors employed as switches in the circuits of a converter are not ideal switches. When these transistors are in the off state, there are leakage currents drawn due to the inversion charge that exists at the gate voltage is below the threshold voltage, and the reverse bias current in the source and drain diffusions. These leakage currents lead to the static losses that can be expressed as

$$P_{\text{stat}} = V_{\text{in}} I_{\text{stat}}, \quad (2.11)$$

where I_{stat} is the total equivalent leakage current of the converter.

As the static losses are generally small ($<1\%$) [17] when compared to the total power loss of a DC-DC converter, and that they can be further mitigated by design

techniques, e.g., power gating, the static losses can also be neglected from the power analysis. We will assume this in our work in Chapter 3.

2.3.5 Summary

This sub-section summarizes the power losses of a switched-mode converter reviewed in Section 2.3. The conduction losses (of the power transistors and the inductor) and the switching losses (of the power transistors and their gate drivers) are the major power losses of the converter. The short-circuit losses and the static losses can be greatly mitigated by established design techniques, and hence are usually neglected in power analysis. However, with concerns to the AC power losses of low to moderate Q integrated inductors employed in a fully-integrated converter for both CCM and DCM, reported models are somewhat oversimplified, and their applications to fully-integrated converters are hence incomplete. This lack of a comprehensive model may lead to inaccurate power-efficiency optimization for fully-integrated converters. This will be addressed in Chapter 3 as part of our research in this Ph.D. program.

2.4 Randomized Modulation Schemes

For a switched-mode DC-DC converter earlier depicted in Figure 1.1, the controller is a critical building block to obtain the desired output voltage level. The pulse density or widths of the output pulses from the controller are modulated according to the modulation scheme employed in the controller.

The PWM scheme [92]–[97] is the most commonly employed modulation scheme due to its algorithm simplicity and easy realization. For converters employing PWM, the power transistors switch at a constant switching frequency to generate the PWM pulses. Because of the constant switching frequency, undesirable strong harmonics power at multiples of the switching frequency will be generated. The randomized modulation schemes [26], [86], [98], [98]–[100], on the other hand, by randomizing one or more parameters of the PWM pulses, can efficiently mitigate the harmonics power by spreading the harmonic power over the whole spectrum.

In this section, we will first review five reported randomized modulation schemes in turn. Specifically, for each modulation scheme, we will present the waveforms of the modulated pulses and the analytical spectra expressions. Thereafter, using the expressions, we will plot the analytical spectra obtained to reveal the characteristics of the spread spectrum. This would allow us to critically compare the different modulation schemes and delineate the modulation scheme that

features the maximum peak spectra power mitigation.

2.4.1 Modulation Scheme 1: Randomized Pulse Position Modulation (RPPM)

The Randomized Pulse Position Modulation [98] is different from PWM by means of an added random delay, ε , at the beginning of each switching period so that the starting position of the pulse is randomly distributed in each switching period. Figure 2.13 depicts an example waveform of the modulated RPPM pulses.

Figure 2.13: Modulated RPPM pulses

Because of the random delay, ε , is limited within $T - \alpha$, where T is the switching period and α is the pulse width. As the switching period of RPPM is kept constant, the pulse width is constant during the operation of the converter.

The output voltage spectrum of the RPPM is [101]

$$S_{\text{RPPM}}(f) = W_{\text{RPPM}}(f) + P_{\text{RPPM}} + P_{\text{DC,RPPM}}, \quad (2.12)$$

The parameters are given as

$$W_{\text{RPPM}}(f) = \frac{H^2}{\tau} \mathcal{G}_{\text{RPPM}_1} (1 - \mathcal{G}_{\text{RPPM}_2}) \quad (2.13)$$

$$P_{\text{RPPM}} = \frac{H^2}{\tau^2} \mathcal{G}_{\text{RPPM}_1} \mathcal{G}_{\text{RPPM}_2} \sum_{q=-\infty}^{q=\infty} \delta\left(f - \frac{q}{\tau}\right) \quad (2.14)$$

$$P_{\text{DC,RPPM}} = D^2 H^2 \quad (2.15)$$

$$\mathcal{G}_{\text{RPPM}_1} = (\alpha \text{sinc}(\pi f D \tau))^2, \text{ and} \quad (2.16)$$

$$\mathcal{G}_{\text{RPPM}_2} = \frac{2}{\omega^2 (\varepsilon_2 - \varepsilon_1)^2} [1 - \cos(\omega (\varepsilon_2 - \varepsilon_1))]. \quad (2.17)$$

where H is the high-state level of the output pulses, τ is the constant switching period, and D is the duty cycle.

The $W_{\text{RPPM}}(f)$, P_{RPPM} , and $P_{\text{DC,RPPM}}$ are the continuous noise-spectrum, discrete harmonics, and the DC power, of the RPPM scheme, respectively. We will comment on the RPPM scheme in Section 2.4.6 later.

2.4.2 Modulation Scheme 2: Randomized Pulse Width Modulation (RPWM)

The Randomized Pulse Width Modulation Scheme (RPWM) [31] randomizes the pulse width in each switching cycle. Figure 2.14 depicts an example waveform of the modulated RPWM pulses.

Figure 2.14: Modulated RPWM pulses

In this modulation scheme, T is constant while the α is varied in each switching cycle. During the operation of the converter, the average pulse width is maintained to be the same as the equivalent pulse width in PWM.

The output voltage spectrum of the RPWM is [98], [101]:

$$S_{\text{RPWM}}(f) = W_{\text{RPWM}}(f) + P_{\text{RPWM}} + P_{\text{DC,RPWM}} \quad (2.18)$$

where

$$W_{\text{RPWM}}(f) = \left[\frac{H^2}{\tau} \left\{ \frac{2}{\omega^2} \mathcal{P}_1 - \mathcal{G}_{\text{RPWM}} \right\} \right]_{f \neq 0} \quad (2.19)$$

$$P_{\text{RPWM}} = \frac{H^2}{\tau^2} \mathcal{G}_{\text{RPWM}} \sum_{\substack{q=-\infty \\ q \neq 0}}^{q=\infty} \delta \left(f - \frac{q}{\tau} \right) \quad (2.20)$$

$$P_{\text{DC,RPWM}} = \left(\frac{\mathcal{A}_1 + \mathcal{A}_2}{2\tau} \right)^2 H^2 \quad (2.21)$$

$$\mathcal{G}_{\text{RPWM}} = \frac{2}{\omega^4 (\mathcal{A}_2 - \mathcal{A}_1)^2} \mathcal{P}_2 \quad (2.22)$$

$$\mathcal{P}_1 = 1 - \frac{1}{\omega} \left(\frac{1}{\mathcal{A}_2 - \mathcal{A}_1} \right) (\sin(\omega \mathcal{A}_2) - \sin(\omega \mathcal{A}_1)) \quad (2.23)$$

$$\mathcal{P}_2 = 1 - \omega (\mathcal{A}_2 - \mathcal{A}_1) (\sin(\omega \mathcal{A}_2) - \sin(\omega \mathcal{A}_1)) + \mathcal{P}_3 \quad (2.24)$$

$$\mathcal{P}_3 = \frac{\omega^2 (\mathcal{A}_2 - \mathcal{A}_1)^2}{2} - \cos(\omega (\mathcal{A}_2 - \mathcal{A}_1)) \quad (2.25)$$

$$\mathcal{A}_1 = [D - \min(D, 1 - D)]\tau \quad (2.26)$$

$$\mathcal{A}_2 = [D + \min(D, 1 - D)]\tau \quad (2.27)$$

The $W_{\text{RPWM}}(f)$, P_{RPWM} , and $P_{\text{DC,RPWM}}$ are the continuous noise-spectrum, discrete harmonics, and the DC power, of the RPWM scheme, respectively. We will comment on the RPWM scheme in Section 2.4.6 later.

2.4.3 Modulation Scheme 3: Randomized Carrier Frequency

Modulation with Variable Duty Cycle (RCFMVD)

The Randomized Carrier Frequency Modulation with Variable Duty Cycle (RCFMVD) randomizes the duty cycle by randomizing the switching period while keeping the pulse width constant. Figure 2.15 depicts an example waveform of the modulated RCFMVD pulses.

Figure 2.15: Modulated RCFMVD pulses

In this scheme, because of the randomized T , the duty cycle, $D = \alpha/T$, is different in each switching period. Nevertheless, the average duty cycle of RCFMVD is designed to be the same as the equivalent duty cycle in PWM.

The output voltage spectrum of the RCFMVD is [98], [101]:

$$S_{\text{RCFMVD}}(f) = W_{\text{RCFMVD}}(f) + P_{\text{DC,RCFMVD}} \quad (2.28)$$

where

$$W_{\text{RCFMVD}}(f) = \frac{2H^2}{T_a + T_b} \left[\mathcal{G}_{\text{VD1}} + 2 \operatorname{Re} \left(\frac{\mathcal{G}_{\text{VD2}} \mathcal{G}_{\text{VD3}}}{1 - \mathcal{G}_{\text{VD4}}} \right) \right] \quad (2.29)$$

$$P_{\text{DC,RCFMVD}} = D^2 H^2 \quad (2.30)$$

$$\mathcal{G}_{\text{VD0}} = \frac{2}{\omega^2} [1 - \cos(\omega\alpha)] \quad (2.31)$$

$$\mathcal{G}_{\text{VD1}} = \frac{1}{\omega^2 (T_2 - T_1)} \left(e^{i\omega T_2} - e^{i\omega T_1} \right) \left(e^{-i\omega\alpha} - 1 \right) \quad (2.32)$$

$$\mathcal{G}_{\text{VD2}} = \frac{i}{\omega} \left(1 - e^{i\omega\alpha} \right) \quad (2.33)$$

$$\mathcal{G}_{\text{VD3}} = \frac{i}{\omega (T_2 - T_1)} \left(e^{i\omega T_1} - e^{i\omega T_2} \right) \quad (2.34)$$

The $W_{\text{RCFMVD}}(f)$ and $P_{\text{DC,RCFMVD}}$ are the continuous noise-spectrum and the DC power of the RCFMVD scheme, respectively. We will comment on the RCFMVD scheme in Section 2.4.6 later.

2.4.4 Modulation Scheme 4: Randomized Carrier Frequency

Modulation with Fixed Duty Cycle (RCFMFD)

The Randomized Carrier Frequency Modulation with Fixed Duty Cycle (RCFMFD) [101] randomizes the switching period with a constant duty cycle. Figure 2.16 depicts an example waveform of the modulated RCFMFD pulses.

In this scheme, both T and α are randomized, and the randomizations of these

Figure 2.16: Modulated RCFMFD pulses

parameters are closely related so that the duty cycle, $D = \alpha/T$, is constant.

The output voltage spectrum of the RCFMFD is [98], [101]:

$$S_{\text{RCFMFD}}(f) = W_{\text{RCFMFD}}(f) + P_{\text{DC,RCFMFD}} \quad (2.35)$$

where

$$W_{\text{RCFMFD}}(f) = \frac{H^2}{(T_1 + T_2)/2} \left[\mathcal{G}_{\text{FD0}} + 2 \operatorname{Re} \left(\frac{\mathcal{G}_{\text{FD1}} \mathcal{G}_{\text{FD2}}}{1 - \mathcal{G}_{\text{FD3}}} \right) \right] \quad (2.36)$$

$$P_{\text{RCFMFD}} = D^2 H^2 \quad (2.37)$$

$$\mathcal{G}_{\text{FD0}} = \frac{2}{\omega^3 (T_2 - T_1)} \left[\omega (T_2 - T_1) - \frac{1}{D} (\sin(\omega D T_2) - \sin(\omega D T_1)) \right] \quad (2.38)$$

$$\mathcal{G}_{\text{FD1}} = \frac{1}{\omega^2 (T_2 - T_1)} \left[\frac{1}{(1 - D)} \left(e^{i\omega(1-D)T_2} - e^{i\omega(1-D)T_1} \right) - \left(e^{i\omega T_2} - e^{i\omega T_1} \right) \right] \quad (2.39)$$

$$\mathcal{G}_{\text{FD2}} = \frac{1}{\omega^2 (T_2 - T_1)} \left[\frac{1}{D} \left(e^{i\omega D T_1} - e^{i\omega D T_2} \right) + i\omega (T_2 - T_1) \right] \quad (2.40)$$

$$\mathcal{G}_{\text{FD3}} = \frac{i}{\omega (T_2 - T_1)} \left(e^{i\omega T_1} - e^{i\omega T_2} \right) \quad (2.41)$$

The $W_{\text{RCFMFD}}(f)$ and $P_{\text{DC,RCFMFD}}$ are the continuous noise-spectrum and the DC power of the RCFMFD scheme, respectively. We will comment on the RCFMFD scheme in Section 2.4.6 later.

2.4.5 Modulation Scheme 5: Randomized Wrapped-Around Pulse Position Modulation (RWAPPM)

Our earlier group's work, the Randomized Wrapped-Around Pulse Position Modulation (RWAPPM) [30], randomizes the starting delay, ε , of the pulse in each switching period. Figure 2.17 depicts an example waveform of the modulated RWAPPM pulses.

Figure 2.17: Modulated RWAPPM pulses

Similar to RPPM, RWAPPM randomized the pulse position while maintaining

the constant switching period, T . However, as opposed to RPPM, the maximum value of the random delay is extended to the full switching period, T . Consequently, when $\varepsilon > T - \alpha$, the pulse will overrun the current switching period. In this case, RWAPPM scheme wraps around the overrun portion of the pulse, and inserts the overrun portion at the beginning of the switching period, as depicted in Figure 2.17. When compared with RPPM, this wrapping around operation is the major difference. To facilitate the modeling of the RWAPPM pulses in the time domain, two new delays are employed, i.e., ψ and Δ , as depicted in Figure 2.17, instead of ε .

The output voltage spectrum of the RWAPPM is [30]:

$$S_{\text{RWAPPM}}(f) = W_{\text{RWAPPM}}(f) + P_{\text{RWAPPM}}(f) + P_{\text{DC,RWAPPM}} \quad (2.42)$$

where

$$W_{\text{RWAPPM}}(f) = \left[\frac{H^2}{\tau} G_{0A} \right]_{f \neq 0} \quad (2.43)$$

$$P_{\text{RWAPPM}} = \frac{H^2}{\tau^2} G_{0B} \sum_{\substack{q=-\infty \\ q \neq 0}}^{q=\infty} \delta \left(f - \frac{q}{\tau} \right) \quad (2.44)$$

$$P_{\text{DC,RWAPPM}} = D^2 H^2 \quad (2.45)$$

The parameters are

$$G_{0A} = G_{1A} (G_{1B} - G_{1C}) + G_{2A} (G_{2B} - G_{2C}) + G_{4A} (G_{4B} - G_{4C}) \quad (2.46)$$

$$G_{0B} = G_{1A} G_{1C} + G_{2A} G_{2C} + G_{3A} G_{3C} + G_{4A} G_{4C} \quad (2.47)$$

$$G_{1A} = (\alpha \operatorname{sinc}(\pi f \alpha))^2 \quad (2.48)$$

$$G_{1B} = 1 - D \quad (2.49)$$

$$G_{1C} = (D^2 - 2D + 1) \operatorname{sinc}^2(\pi f(\tau - \alpha)) \quad (2.50)$$

$$G_{2A} = ((\alpha - \tau) \operatorname{sinc}(\pi f(\alpha - \tau)))^2 \quad (2.51)$$

$$G_{2B} = G_{3C} = G_{4B} = D \quad (2.52)$$

$$G_{2C} = (D \operatorname{sinc}(\pi f \alpha))^2 \quad (2.53)$$

$$G_{3A} = 2 \operatorname{Re} [A_V(f) A_Z(-f) E \{e^{i\sigma\psi}\}] \quad (2.54)$$

$$+ 2 \operatorname{Re} [A_W(f) A_Z(-f) E \{e^{i\omega\psi}\} E \{e^{-i\omega\Delta}\}]$$

$$G_{4A} = ((\tau \operatorname{sinc}(\pi f \tau))^2 + 2 \operatorname{Re} [A_V(f) A_W(-f) E \{e^{i\omega\Delta}\}] \quad (2.55)$$

$$- 2 \operatorname{Re} [A_V(f) A_Z(-f) E \{e^{i\omega\psi}\}])$$

$$- 2 \operatorname{Re} [A_W(f) A_Z(-f) E \{e^{i\omega\psi}\} E \{e^{-i\omega\Delta}\}])$$

$$G_{4C} = D^2 \quad (2.56)$$

$$E \{e^{i\omega\psi}\} = \frac{1}{\omega(\tau - \alpha)} [\sin(\omega(\tau - \alpha)) - i(\cos(\omega(\tau - \alpha)) - 1)] \quad (2.57)$$

$$E \{e^{i\omega\Delta}\} = \frac{1}{\alpha\omega} [(\sin(\omega\tau) - \sin(\omega(\tau - \alpha))) \quad (2.58)$$

$$- i(\cos(\omega\tau) - \cos(\omega(\tau - \alpha)))]$$

$$E \{ e^{-i\omega\Delta} \} = \frac{1}{\alpha\omega} [(\sin(\omega\tau) - \sin(\omega(\tau - \alpha))) \quad (2.59)$$

$$+ i(\cos(\omega\tau) - \cos(\omega(\tau - \alpha)))]$$

$$A_Z(f) = \frac{1 - e^{-i\omega\alpha}}{i\omega} \quad (2.60)$$

$$A_V(f) = \frac{1 - e^{-i\omega\tau}}{i\omega} \quad (2.61)$$

$$A_W(f) = \frac{1 - e^{-i\omega(\alpha-\tau)}}{i\omega} \quad (2.62)$$

The $W_{\text{RWAPPM}}(f)$, $P_{\text{RWAPPM}}(f)$, and $P_{\text{DC,RWAPPM}}$ are the continuous noise-spectrum, discrete power of the harmonics, and the DC power, of the RCFMVD scheme, respectively. We will comment on the RWAPPM scheme later in Section 2.4.6.

2.4.6 Summary

This sub-section summarizes the properties of the randomized modulation schemes reviewed in Section 2.4. The properties of the reviewed randomized modulation schemes in Table 4.1. As the reviewed randomized modulation schemes are based on PWM, for the sake of completeness, the properties of PWM is also tabulated in Table 4.1. With the aforesaid, we will critically review these five randomized schemes.

Table 2.2: Comparison of Randomized Modulation Schemes

Modulation Scheme	α	T	ε	$D = \alpha/T$
PWM	Constant	Constant	Zero	Constant
RPPM	Constant	Constant	Randomized	Constant
RPWM	Randomized	Constant	Zero	Randomized
RCFMVD	Constant	Randomized	Zero	Randomized
RCFMFD	Randomized	Randomized	Zero	Constant
RWAPPM	Constant	Constant	Randomized	Constant

Of the five reviewed randomized modulation schemes, RPPM and RWAPPM randomize the starting delay, ε , which can be simply realized by digital gates. In this perspective, these schemes are advantageous over the increased complexity of switching period randomization and pulse width randomization in other three randomized modulation schemes (RPWM, RCFMVD, and RCFMFD). In other words, RPPM and RWAPPM feature the simplest realizations.

To investigate the spectrum power, the analytical spectrum expressed in Equations (2.12), (2.18), (2.28), (2.35), and (2.42) are plotted in Figure 2.18 based on a 120 kHz, 0.75 duty cycle single-phase converter [30]. The spectrum of PWM is also plotted for completeness and for cogent comparisons.

A perusal of Figure 2.18 depicts, as expected, that the randomized modulation

Figure 2.18: Spectra obtained analytically of various modulation schemes [30] (a) PWM, (b) RPPM, (c) RPWM, (d) RCFMVD, (e) RCFMFD, and (f) RWAPPM

scheme can efficiently spread the harmonics power (the discrete dots in PWM) over the whole spectrum (the continuous lines in Figure 2.18 (b)-(f)). As expected, the peak spectral power of PWM harmonics is the largest—0.4 dBFS, whereas the peak spectral power of the randomized modulation schemes is <0 dBFS. Of all the randomized modulation schemes, the peak spectral power of RWAPPM is the lowest, -26.6 dBFS (equivalent to 500× mitigation compared to PWM). In short, the RWAPPM scheme features one of the simplest realizations, yet low peak spectral power.

It is worthwhile to note that the randomized modulation schemes presented in the literature, including the five schemes reviewed, are generally employed only in single-phase converters. To the best of our knowledge, their application to multi-phase converters is unreported and we assert that this is the case because the randomization in each phase of the multi-phase converter may lead to numerous continuously overlapped pulses which will undesirably exacerbate the output noise.

We will propose and investigate the application of a randomized modulation scheme to a multi-phase converter in Chapter 4.

2.5 Conclusions

In this chapter, we have reviewed different topologies of switched-mode DC-DC buck converters. On the basis of our review, we have delineated that the inductive buck converter features better output regulation and higher power-efficiency attribute over the SC buck converter for varying load conditions. We have also delineated that the multi-phase inductive buck converter features reduced output noise than its single-phase counterpart.

In our review of inductor integrations technologies, we have compared the start-of-the-art IoS approaches and the IiP approaches. We have delineated the salient advantages of the bonding wire inductor in the IiP approaches, for the integration in a fully-integrated converter.

In our review of the power losses in an inductive buck converter, we have reviewed four different types of power losses, of which two are dominant—the conduction losses and the switching losses. We have ascertained the limitations of the power loss mechanisms in reported work, and delineated the need for a comprehensive model of power loss mechanisms that can be applied to fully-integrated converters. The lack of the comprehensive power loss model for a fully-integrated converter is partly the basis of our work in Chapter 3.

In our review of the modulation schemes, we have shown that the PWM has undesirable strong harmonic power whereas the randomized modulation schemes can efficiently spread the harmonic power over the frequency spectrum. Amongst all the randomized modulation schemes, the RWAPPM features one of the simplest realizations, yet low peak spectral power. Of particular note in our critical review, we have delineated that the randomized modulation schemes are generally applied to only single-phase converters and their application to multi-phase converters is unreported. This , in part, is the basis of our work in Chapter 4.

Chapter 3

Modeling and Power Analysis of Fully-Integrated Switched-Mode DC-DC Converters with Bonding Wire Inductors

3.1 Introduction

A large portion of this chapter is extracted from a paper submitted to the IEEE Transactions on Power Electronics [102] co-authored by the author of this thesis, and to a small part extracted from a provisional patent where the said author is a co-inventor.

As earlier delineated in Chapter 1 and Chapter 2, existing models in reported work are not comprehensive and do not completely apply to fully-integrated converters because they either ignore the inductor AC power loss, or they simplify the inductor power loss model only for CCM whereas fully-integrated converters may operate in both CCM and DCM.

In this chapter, we propose a comprehensive model for optimizing the power

efficiency of fully-integrated high-frequency converters with moderate- Q bonding wire inductors. Specifically, the proposed model extends reported models [3], [18], [19] for conventional inductive converters to now include our derived analytical expressions that depict the power losses of the bonding wire inductors; the considerable AC losses were previously ignored or inadvertently assumed to be negligible. Our derived analytical expressions model both the DC and the AC power losses, and is applicable to both the CCM and DCM operations. Our model further encompasses the power loss expressions of the power transistors and their gate drivers. Our derived analytical expressions of the gate drivers are more complete than reported expressions because our expressions include readily determined design parameters of the gate drivers vis-à-vis an empirical total gate charge value [85]. The application space of our proposed model is wide as it can be adapted for multi-objective optimizations [85], [103], e.g., Pareto optimization, convex optimizations, etc., of fully-integrated converters, and extend the optimization to both CCM and DCM operations. Put simply, the proposed model provides valuable insights into the design of fully-integrated converters and the mechanisms for power efficiency thereof.

The remainder of this chapter is organized as follows. Section 3.2 models the power losses of the bonding wire inductor of a fully-integrated converter. Section 3.3 presents the power losses and optimization of the power transistors and their gate

drivers. Section 3.4 presents the simulations and physical measurements. Section 3.5 discusses the applications of the proposed model. Finally, Section VI draws the conclusion.

3.2 Inductor Power Losses

In this section, we will first describe a fully-integrated inductive buck converter with a bonding wire inductor. Thereafter, we describe our proposed model, where unlike reported model [16], our model accounts for the moderate- Q of the bonding wire inductor and the high switching frequency (vis-à-vis high- Q external inductor and low switching frequency). Specifically, our model accounts for the inductor AC power loss in both CCM and DCM. Our derived Fourier Series expression of the inductor current in our model unambiguously identifies the DC and AC components, thereby providing a means to analyze the inductor DC and AC power losses in both CCM and DCM. Of specific interest, we show that the inductor AC power loss that is ignored [16] can be considerable and hence should be accounted for.

3.2.1 Inductor Current Analysis

Figure 3.1 depicts the simplified block diagram of a fully-integrated inductive synchronous buck converter. The converter comprises a controller, gate drivers, a

high-side power transistor M_p and a low-side power transistor M_n (where a PMOS and an NMOS, respectively, is used in this work), a bonding wire inductor (modeled as resistor $r_{L,esr}$ in series with ideal inductor L) and an on-chip capacitor (modeled as resistor $r_{C,esr}$ in series with ideal capacitor C). During each switching period T , the controller controls the gate drivers to drive the power transistors on and off, delivering current from input V_{in} to output V_{out} via the bonding wire inductor.

Figure 3.1: Simplified block diagram of a fully-integrated inductive buck converter

As depicted earlier in Figures 2.3(a) and 2.3(b), the ideal i_L comprises two components: DC component, I_{out} , and AC component (ripple current), Δi_L .

We model the inductor waveforms of CCM and DCM, and unify them in one

mathematical expression as

$$i_L(t) = \begin{cases} \frac{\Delta i_L \cdot t}{DT} + k, & \text{if } 0 < t \leq DT \\ \frac{-\Delta i_L(t - DT)}{D_1 T} + \Delta i_L + k, & \text{if } DT < t \leq (D + D_1)T \\ 0, & \text{if } (D + D_1)T < t \leq T \end{cases} \quad (3.1)$$

where k is

$$k = I_{\text{out}} - \frac{\Delta i_L(D + D_1)}{2}. \quad (3.2)$$

To unambiguously depict the DC and AC component of the inductor current, we expand Equation (3.1) into a Fourier series expression as:

$$\begin{aligned} i_L(t) &= I_{\text{out}} + \sum_{n=1}^{\infty} \left(a_n \cos \frac{2\pi n t}{T} + b_n \sin \frac{2\pi n t}{T} \right) \\ &= I_{\text{out}} + \sum_{n=1}^{\infty} I_{\text{ac},n} \cos \left(\frac{2\pi n t}{T} + \phi_n \right), \end{aligned} \quad (3.3)$$

where I_{out} is the DC value of the inductor current, $I_{\text{ac},n}$ and ϕ_n are the amplitude and phase of the n^{th} harmonic, respectively. $I_{\text{ac},n}$ and ϕ_n are obtained as follows

$$\begin{aligned}
I_{ac,n} &= \Delta i_L \sqrt{a_n^2 + b_n^2}, & \phi_n &= -\arctan(b_n/a_n), \\
a_n &= \frac{z_1 - z_2 + z_3}{2\pi^2 n^2 D D_1}, & b_n &= \frac{z_4 - z_5 + z_6}{2\pi^2 n^2 D D_1}, \\
z_1 &= D_1(\cos 2\pi n D - 1), & z_2 &= D \cos 2\pi n(D + D_1), \\
z_3 &= D \cos 2\pi n D, & z_4 &= D_1 \sin 2\pi n D, \\
z_5 &= D \sin 2\pi n(D + D_1), & z_6 &= D \sin 2\pi n D,
\end{aligned} \tag{3.4}$$

and D_1 is obtained as

$$D_1 = \left(\frac{2I_{out}}{\Delta i_L} - D \right) \hat{H}(\Delta i_L - 2I_{out}) + (1 - D) \hat{H}(2I_{out} - \Delta i_L), \tag{3.5}$$

where H is the Heaviside step function defined as

$$\hat{H}(x) = \begin{cases} 0, & \text{if } x < 0, \\ 1, & \text{if } x \geq 0. \end{cases} \tag{3.6}$$

In Equation (3.3), I_{out} is the fundamental (DC value, see Figure 2.3) and constitutes to the DC power loss of the inductor. The second term in Equation (3.3) is the harmonics, i.e., the AC value, and constitutes to the AC power loss of the inductor.

Our derived inductor current Fourier series in expression Equation (3.3) generally matches the ideal inductor current waveforms depicted in Figure 2.3.

Figure 3.2: Validation of inductor waveforms obtained using (3) at $f = 100$ MHz, $D = 0.4$ and $\Delta i_L = 50$ mA where $I_{out} = 200$ mA in CCM and $I_{out} = 20$ mA in DCM

For example, using Equation (3.3) and Equation (3.4), for a converter operating at $f = 100$ MHz, $D = 0.4$ and $\Delta i_L = 50$ mA, we plot in Figure 3.2 the waveforms of the modeled inductor current in a converter operating in CCM and DCM. In CCM where $I_{out} = 200$ mA, the inductor current waveform matches the waveform in Figure 2.3(a). On the other hand, in DCM where $I_{out} = 20$ mA, the inductor current waveform matches the waveform in Figure 2.3(b).

We will now utilize our derived unified CCM and DCM Fourier series inductor current expression in Equations (3.3) and (3.4) for the power analysis.

3.2.2 Bonding wire Inductor Power Losses

The power loss of an inductor generally includes core loss, DC loss, and AC loss. In the case of the bonding wire inductor having air as its core (instead of magnetic materials [13]), it does not suffer from core losses [104].

The DC loss occurs when DC current flows through the bonding wire inductor due to the DC resistance of its conductor. The DC resistance [105] is given as

$$r_{dc} = \frac{\rho l}{\pi r^2}, \quad (3.7)$$

where ρ , l and r are the resistivity, total length, and the radius of the bonding wire, respectively. The ensuing DC loss of the inductor is

$$P_{L,dc} = r_{dc} I_{out}^2 = \frac{\rho l I_{out}^2}{\pi r^2}. \quad (3.8)$$

The AC loss, on the other hand, is due to the skin effect (Figure 3.3) of the inductor windings when high-frequency AC current flows. The AC current flows mainly in the "skin" of the conductor, whose skin depth [105] is

$$\delta = \sqrt{\frac{\rho}{\pi \mu f_{sin}}}, \quad (3.9)$$

Figure 3.3: Skin effect of a round conductor when high-frequency AC current flows

where $f_{\sin}$ and μ are the frequency of a sinusoidal current flowing in the inductor and the permeability of the conductor material, respectively.

When $f_{\sin}$ falls below a certain value which is dependent on the property of the conductor, the skin depth is deeper than the conductor radius. In this situation, the skin effect is negligible and the ensuing AC resistance is the same as the DC resistance. However, when $f_{\sin}$ is higher than the said certain value, the skin effect tends to concentrate the current on the surface, thereby increasing the AC resistance. In this situation, $\delta < r$ and the AC resistance is given by [105]

$$r_{ac} = \frac{\rho \cdot l}{\pi r^2 - \pi(r - \delta)^2}. \quad (3.10)$$

As the inductor current of the converter is non-sinusoidal (see Figure 2.3), we will use the obtained Fourier series expression with sinusoidal harmonics in

Equation (3.3) to derive the AC resistance due to the skin effect. By combining Equations (3.7), (3.9) and (3.10), we derive the AC resistance for the n^{th} harmonic of the inductor current as

$$r_{ac,n} = \frac{\rho l}{\pi r^2} \cdot \hat{H}\left(\frac{\rho}{n\pi\mu r^2} - f_{sw}\right) + \frac{\rho l \mu \cdot n f_{sw}}{2r\sqrt{\pi\mu\rho \cdot n f_{sw} - \rho}} \cdot \hat{H}\left(f_{sw} - \frac{\rho}{n\pi\mu r^2}\right), \quad (3.11)$$

where f_{sw} and l are the switching frequency of the converter and the total length of the bonding wire used in the inductor, respectively.

By means of Equation (3.11), the AC loss of the bonding wire inductor can be more comprehensively modeled, in the sense that the specificities of the conductor bonding wire are now accounted for, i.e.,

$$P_{L,ac} = \sum_{n=1}^{\infty} r_{ac,n} \cdot I_{ac,n}^2, \quad (3.12)$$

where $I_{ac,n}$ and $r_{ac,n}$ are the amplitude of the n^{th} harmonic in Equation (3.4) and the inductor AC resistance at the n^{th} harmonic defined in Equation (3.11), respectively.

Finally, by combining Equations (3.12) and (3.8), we derive the total power loss of the bonding wire inductor including the DC power loss and the AC power

loss due to the skin effect for both CCM and DCM as

$$\begin{aligned}
 P_L &= P_{L,\text{dc}} + P_{L,\text{ac}} \\
 &= \frac{\rho l}{\pi r^2} \cdot I_{\text{out}}^2 + \sum_{n=1}^{\infty} r_{\text{ac},n} \cdot I_{\text{ac},n}^2.
 \end{aligned} \tag{3.13}$$

It is worthwhile reiterating that the AC loss of the inductor in a converter is typically ignored in reported work [16], particularly when compared to the DC loss. We will now depict that the AC loss should not be ignored for the bonding wire inductor in a fully-integrated converter. We first define the ratio of inductor AC power loss over its DC power loss, P_{ratio} , as

$$P_{\text{ratio}} = \frac{P_{L,\text{ac}}}{P_{L,\text{dc}}} = \frac{\pi r^2}{\rho l} \cdot \sum_{n=1}^{\infty} r_{\text{ac},n} (a_n^2 + b_n^2) (\Delta i_{\text{norm}})^2, \tag{3.14}$$

where a_n and b_n are defined in Equation (3.4), and Δi_{norm} is the normalized inductor current ripple defined by

$$\Delta i_{\text{norm}} = \frac{\Delta i_L}{I_{\text{out}}}. \tag{3.15}$$

Using Equation (3.14) and the parameters of the bonding wire inductor employed in our fully-integrated converter (see Section 3.4 later), we plot in Figure 3.4 a contour map of P_{ratio} as a function of Δi_{norm} and f_{sw} . The contour map includes P_{ratio} for both CCM ($\Delta i_{\text{norm}} < 2$) and DCM ($\Delta i_{\text{norm}} > 2$). As the inductor DC power

loss in Equation (3.8) is not a function of f_{sw} and Δi_{norm} , $P_{L,dc}$ remains constant in this figure, therefore a higher P_{ratio} indicates a higher $P_{L,ac}$.

Figure 3.4: Contour map AC/DC power loss ratio (P_{ratio}) of the bonding wire inductor on the plane of f_{sw} versus Δi_{norm}

We note two observations. First, as expected, for a given Δi_{norm} , $P_{L,ac}$ relative to $P_{L,dc}$ increases with switching frequency. This means that the fully-integrated converter (with bonding wire inductors) operating at high switching frequencies would suffer from higher $P_{L,ac}$ compared to the same converter operating at lower switching frequencies. As a case in point, for a converter operating at $\Delta i_{norm} = 2$

in Figure 3.4, $P_{L,ac}$ is $3\times$ of $P_{L,dc}$ when $f_{sw} = 50$ MHz compared to the case where $f_{sw} = 500$ MHz. Particularly, this means that to reduce $P_{L,ac}$, a low f_{sw} is required but at the cost of compromising the form-factor.

Second, for a given f_{sw} , $P_{L,ac}$ increases significantly with Δi_{norm} . Of specific interest, when $\Delta i_{norm} > 2$ where the converter operates in DCM, $P_{L,ac}$ can be significant compared to the case when $\Delta i_{norm} < 2$, where the converter operates in CCM. As a case in point, for the converter operating at 100 MHz, $P_{L,ac}$ is $20\times$ of $P_{L,dc}$ when $\Delta i_{norm} = 3.5$ compared to the case where $\Delta i_{norm} = 0.7$. Particularly, this means that to reduce $P_{L,ac}$, a small Δi_{norm} is required but at the cost of long bonding wires that may not be practical to be realized in the package.

From the last two aforesaid observations, it is obvious that low power loss of the inductor is obtained when both f_{sw} and Δi_{norm} are simultaneously low. However, for fully-integrated converters, these conditions are largely unattainable because a large L is required—the inductance of the bonding wire is a small L , e.g., ~ 10 nH for 16 mm-length bonding wire. Put simply, in the broad perspective for the design of fully-integrated converters, the power loss of the bonding wire inductor, as one of several trade-offs of the converter design, should be optimized with other design parameters, including the length of the bonding wire and the load current.

3.3 Power Transistor Related Power Losses

In this section, we will model and analyze the power losses due to the power transistors in fully-integrated buck converters. The intention is the derivation of the optimized power loss of the power transistors and their gate drivers.

A general expression [69] for the power loss of a single transistor including the conduction loss and the switching loss is

$$\begin{aligned} P_M &= P_{M, \text{conduction}} + P_{M, \text{switching}} \\ &= \frac{r_{\text{on}0}}{W} i_{\text{rms}}^2 + W f_{\text{sw}} (C_{\text{g}0} V_{\text{g}}^2 + C_{\text{oss}0} V_{\text{in}}^2), \end{aligned} \quad (3.16)$$

where

$P_{M, \text{conduction}}$, $P_{M, \text{switching}}$, W , and V_{g} are the conduction loss, the switching loss, the width, and the gate voltage swing of the power transistor, respectively,

$r_{\text{on}0}$ is the unit width conducting resistance of the power transistor,

$C_{\text{g}0}$, and $C_{\text{oss}0}$ are the equivalent gate capacitance, and output capacitance per unit width of the power transistor, respectively, and

i_{rms} is the root-mean-square of conducting current of the power transistor.

Note that as $r_{\text{on}0}$ and $C_{\text{g}0}$ can be different for PMOS and NMOS, we will

denote in our analysis, $r_{\text{on0,pmos}}$, $C_{\text{g0,pmos}}$ and $r_{\text{on0,nmos}}$, $C_{\text{g0,nmos}}$ as the conductance resistance and equivalent gate capacitance per unit width for PMOS and NMOS, respectively. In our analysis, for sake of simplicity, we assume the power transistors and the transistors in their gate drivers are of the same type—the PMOS used for power transistors and gate drivers have the same $r_{\text{on0,pmos}}$ and $C_{\text{g0,pmos}}$, and similarly, the NMOS used for power transistors and gate drivers have the same $r_{\text{on0,nmos}}$ and $C_{\text{g0,nmos}}$.

Figure 3.5: Schematic of a power transistor and its gate driver

As for gate drivers, they generally employ a tapered buffer structure [36] as depicted in Figure 3.5. This structure comprises N stages of inverters where the channel width of each transistor in the inverter is a fixed multiple (tapering factor), F , larger than that of the preceding inverter. All the NMOS in the gate driver are sized at a constant ratio, β , over its PMOS counterpart such that each inverter stage

has equal rise, fall, and delay times.

During operation, the output current of each inverter stage charges and discharges the equivalent gate capacitor of the inverter in the following stage, leading to switching losses. Because the switching loss of the gate driver is dominant [69] when the gate driver operates at high switching frequencies (> 1 MHz), the conduction loss of the gate driver will be assumed to be negligible in our analysis.

The number of stages, N , is an integer expressed by:

$$N = \left\lceil \log_F \frac{WC_{g0}}{W_{\min}C_{g0,\text{pmos}} + W_{\min}\beta C_{g0,\text{nmos}}} \right\rceil, \quad (3.17)$$

where W and C_{g0} are the width and the gate capacitance per unit width of the power transistor, respectively.

From Equation (3.17), $W_{\min}$ can be expressed as:

$$W_{\min} = \frac{W}{F^N} \cdot \frac{C_{g0}}{C_{g0,\text{pmos}} + \beta C_{g0,\text{nmos}}}. \quad (3.18)$$

Summing up the switching loss of each transistor in the gate driver depicted in Figure 3.5, the composite power loss of the gate driver can be derived as

$$\begin{aligned}
P_{\text{driver}} = & \frac{F^N - 1}{F - 1} W_{\min} (C_{g0,\text{pmos}} + C_{\text{oss0},\text{pmos}}) V_g^2 f_{\text{sw}} \\
& + \frac{F^N - 1}{F - 1} W_{\min} \beta (C_{g0,\text{nmos}} + C_{\text{oss0},\text{nmos}}) V_g^2 f_{\text{sw}}
\end{aligned} \tag{3.19}$$

By resolving F^N from Equation (3.18), then substituting F^N and $W_{\min}$ to Equation (3.19), we obtain the total power loss of the gate driver as a function of W and F :

$$P_{\text{driver}} = p_1 C_{g0} V_g^2 f_{\text{sw}} \cdot W - \frac{p_1 V_g^2 f_{\text{sw}} W_{\min}}{C_{g0,\text{pmos}} + \beta C_{g0,\text{nmos}}}, \tag{3.20}$$

where p_1 is defined as

$$p_1 = \frac{1}{F - 1} \cdot \left(1 + \frac{C_{\text{oss0},\text{pmos}} + \beta C_{\text{oss0},\text{nmos}}}{C_{g0,\text{pmos}} + \beta C_{g0,\text{nmos}}} \right). \tag{3.21}$$

Note that our analytical expression of the gate driver power loss in Equation (3.20) includes the design parameters of the gate driver that are dependent on the size of the power transistor.

The total power transistor loss, $P_{M,\text{tot}}$ is a combination Equations (3.16) and

(3.19), and can be expressed as:

$$\begin{aligned}
 P_{M,\text{tot}} &= P_M + P_{\text{driver}} \\
 &= \frac{r_{\text{on0}} i_{\text{rms}}^2}{W} + W f_{\text{sw}} (C_{\text{g0}} V_{\text{g}}^2 + C_{\text{oss0}} V_{\text{in}}^2 + p_1 C_{\text{g0}} V_{\text{g}}^2) \\
 &\quad - \frac{p_1 C_{\text{g0}} V_{\text{g}}^2 f_{\text{sw}}}{C_{\text{g0,pmos}} + \beta C_{\text{g0,nmos}}} W_{\text{min}}.
 \end{aligned} \tag{3.22}$$

To minimize $P_{M,\text{tot}}$, Equation (3.22) is differentiated with respect to W and equated to zero. The result is the optimum width of the power transistor, and is given by

$$W_{\text{opt}} = \sqrt{\frac{r_{\text{on0}} i_{\text{rms}}^2}{f_{\text{sw}} (C_{\text{g0}} V_{\text{g}}^2 + C_{\text{oss0}} V_{\text{in}}^2 + p_1 C_{\text{g0}} V_{\text{g}}^2)}}. \tag{3.23}$$

The optimum power loss of a power transistor (M_p or M_n) can be therefore derived as

$$P_{M,\text{opt}} = 2i_{\text{rms}} \sqrt{r_{\text{on0}} f_{\text{sw}} (C_{\text{g0}} V_{\text{g}}^2 + C_{\text{oss0}} V_{\text{in}}^2 + p_1 C_{\text{g0}} V_{\text{g}}^2)}. \tag{3.24}$$

To model the power loss of each power transistor for both CCM and DCM, we derive the expressions of the rms currents in M_p and M_n from [17] as

$$\begin{aligned}
 i_{\text{rms},p} &= \sqrt{D} \cdot p_2, \quad \text{and} \\
 i_{\text{rms},n} &= \sqrt{D_1} \cdot p_2,
 \end{aligned} \tag{3.25}$$

respectively, where p_2 is defined as

$$p_2 = \sqrt{(I_{\text{out}}^2 + \Delta i_L^2/12)} \cdot \hat{H}(2I_{\text{out}} - \Delta i_L) + \sqrt{(\Delta i_L^2/3)} \cdot \hat{H}(\Delta i_L - 2I_{\text{out}}). \quad (3.26)$$

Finally, based on W_{opt} of the converter power transistors M_p and M_n defined in Equation (3.23), and the rms currents in Equation (3.26), we derive the total loss, including the conduction loss, switching loss and the gate driver loss of the optimized M_p and M_n , for both CCM or DCM as

$$P_{\text{transistors,tot}} = 2p_2 \sqrt{p_3 f_{\text{sw}} D r_{\text{on0,pmos}}} + 2p_2 \sqrt{p_4 f_{\text{sw}} D_1 r_{\text{on0,nmos}}}, \quad (3.27)$$

where p_1 and p_2 are defined in Equations (3.21) and (3.26), respectively, and p_3, p_4 are defined as

$$p_3 = C_{\text{g0,pmos}} V_g^2 + C_{\text{oss0,pmos}} V_{\text{in}}^2 + p_1 C_{\text{g0,pmos}} V_g^2, \quad (3.28)$$

$$p_4 = C_{\text{g0,nmos}} V_g^2 + C_{\text{oss0,nmos}} V_{\text{in}}^2 + p_1 C_{\text{g0,nmos}} V_g^2.$$

It is worth noting that our derived optimized power loss model in Equation (3.27) embodies the power losses of both the power transistor and their gate drivers for both CCM and DCM. Unlike reported models [85], [106] that require the total gate charge value, which needs to be extracted from the datasheet (or measured), our

derived power loss model of the gate driver is based on the design parameters, which can be conveniently estimated from the process parameters. Our derived power transistor loss model is particularly meaningful for multi-objective optimizations, such as Pareto optimization, Convex optimization, etc., that need to evaluate various different converter designs with different design parameters.

3.4 Simulation Results and Experimental Verification

We will now apply our derived model to analyze the design of a prototype converter in a CMOS 65nm IC process with a bonding wire inductor. The micrograph of the power transistors and the gate drivers of the converter is depicted in Figure 3.6. The process parameters and the (range of) design specifications are tabulated in Table 3.1.

To demonstrate the good accuracy provided by our proposed analytical model, comparisons of analytical (from the derived expressions), simulated (SPICE), and measured (from the prototype IC) power-efficiencies are depicted in Figure 3.7.

The power-efficiencies are simulated and measured over a range of load currents from 80 mA to 500 mA at 200 MHz switching frequency. In general, there is good agreement between the said curves, thereby verifying the derived analytical model.

Figure 3.6: Micrograph of the bonding wire inductor, power transistors, and the gate drives of the prototype converter IC

For completeness, the minor difference between the plots is largely due to losses that are not modeled in our analytical model, i.e., the parasitic capacitance and resistance of the routing traces in the IC layout and the PCB. As expected, in view of this, the highest divergence between the plots is at the highest output current.

3.5 Applications of the Proposed Model

We will now present and discuss the applications of our proposed model using the same process parameters and the same design specifications tabulated in Table 3.1. For illustration and sake of brevity, the converter is designed for a single output, $I_{\text{out}} = 500 \text{ mA}$; fully-integrated converters with bonding wire inductors

Table 3.1: Process Parameters and Design Specifications

Parameter	Value	Parameter	Value
μ	$4\pi \times 10^{-7}$ H/m	ρ	$2.44 \times 10^{-8} \Omega \cdot \text{m}$
r	25×10^{-6} m	$r_{\text{on0,pmos}}$	$9.46 \times 10^{-3} \Omega \cdot \text{m}$
l	0.1 to 30 mm	$r_{\text{on0,nmos}}$	$5.91 \times 10^{-3} \Omega \cdot \text{m}$
$C_{\text{g0,pmos}}$	2.06×10^{-9} F/m	$C_{\text{g0,nmos}}$	2.63×10^{-9} F/m
W_{min}	$0.66 \mu\text{m}$	F	2.9
V_{in}	3.3 V	V_{out}	1.65 V
V_{g}	3.3 V	I_{out}	500 mA
f_{sw}	50 to 500 MHz	Δi_{norm}	0.1 to 4

with other loads may be similarly designed. By employing respective inductance models, bonding wire inductors of different shapes [65], [107] can be fitted into our proposed power loss model and evaluated. For sake of simplicity, the commonly employed Π -shaped bonding wire inductor (see Figure 2.10) is assumed and the inductance model based on Equation (2.6) is evaluated in the following analysis. For completeness, the estimated L and Q of the bonding wire inductor employed in the prototype IC are ~ 3.7 nH and 14.9 at 200 MHz, respectively.

Our proposed model can be used to explore the maximum power-efficiency and the required bonding wire length of fully-integrated converters with bonding

Figure 3.7: Comparison of the analytical, simulated, and measured power-efficiencies of the prototype converter

wire inductors. Figure 3.8 and Figure 3.9 depict the contour map of the maximum power-efficiencies and the required bonding wire inductor lengths, respectively, for different possible optimized converters operating at various f_{sw} and Δi_{norm} .

Consider first, in the perspective of the bonding wire length, it can be observed that fully-integrated converters (with a bonding wire inductor) generally feature high power-efficiencies at low f_{sw} and small Δi_{norm} . However, the cost is the employment of longer bonding wire inductors (for larger inductance), which may be impractical for integration. For example, for fully-integrated converters operating at 50 MHz

Figure 3.8: Contour map of the maximum power-efficiencies on the plane of f_{sw} versus Δi_{norm}

Figure 3.9: Contour map of the required bonding wire length l (mm) on the plane of f_{sw} versus Δi_{norm}

and with Δi_{norm} of 0.4, the optimized bonding wire is an impractical 70 mm.

Consider second, in the perspective of the power losses and their ensuing optimization, Figures 3.10, 3.11 and 3.12 depict the comparison of the analytical power loss breakdown of various optimized fully-integrated converters with bonding wire inductors operating at various f_{sw} and Δi_{norm} , respectively. We note two observations.

First, $P_{L,\text{ac}}$, as expected, increases with both f_{sw} and Δi_{norm} , and is considerable when Δi_{norm} is large (>2 , i.e., in DCM). For example, as depicted in Figure 3.12, for converters operating at 500 MHz and $\Delta i_{\text{norm}} = 3$, $P_{L,\text{ac}}$ is a considerable $> 8\%$. Practically, in order to reduce the inductor power loss, it is desired to operate the converter at low f_{sw} and small Δi_{norm} .

Second, the power transistor related power losses, including P_{driver} , $P_{\text{M,switching}}$, and $P_{\text{M,conduction}}$, are the major power losses. This is largely because the thick-oxide power transistors of the 65nm process have relatively high conducting resistance and high parasitic capacitance. To further reduce the power transistor related losses, IC processes featuring low conducting resistance and low parasitic capacitance power transistors, e.g., CMOS with BCD transistors or III-V devices such as GaN, InGaAs,

Figure 3.10: Power loss breakdown of optimized converters operating at various f_{sw} and with $\Delta i_{\text{norm}} = 1$

Figure 3.11: Power loss breakdown of optimized converters operating at various f_{sw} and with $\Delta i_{\text{norm}} = 2$

Figure 3.12: Power loss breakdown of optimized converters operating at various f_{sw} and with $\Delta i_{norm} = 3$

etc., should be considered.

Consider third, in the perspective of different IC processes for implementing fully-integrated converters with bonding wire inductors, Figure 3.13 depicts the comparison of the maximum power-efficiency achievable using 3.3 V thick-oxide transistors in two IC processes: CMOS 65 nm and CMOS 180 nm. This plot is obtained from our analytical model. The plot depicts that the fully-integrated converters implemented in the 180 nm process using 3.3 V transistors feature higher power-efficiencies than those of the same design but implemented in the 65 nm process—the former is therefore preferred for the implementation of fully-integrated converters. To illustrate, from Figure 3.13, a fully-integrated converter design with

Figure 3.13: Contour map of the maximum power-efficiencies on the plane of f_{sw} versus Δi_{norm} evaluated using CMOS 65 nm and 180 nm processes

a bonding wire inductor operating at 50 MHz with $\Delta i_{norm}=1$ if implemented in the 180 nm process will feature the highest power-efficiency of 80%, whereas the same design, if implemented in the 65 nm process, will only feature the highest power-efficiency of 76%—a 4% reduction.

In short, our derived analytical model provides meaningful insights for the design of fully-integrated DC-DC converters with bonding wire inductors.

3.6 Conclusion

In this chapter, we have proposed a comprehensive analytical model for moderate- Q bonding wire inductors, power transistors, and gate drivers of fully-integrated converters has been proposed to facilitate the optimization of power-efficiency. The proposed model considers both the DC and AC power losses of the embodied bonding wire inductor, and is applicable to both CCM and DCM operations. The AC power loss of the inductor is shown to be considerable for fully-integrated converters, particularly in DCM operations. The applications of our proposed model are provided in three perspectives—bonding wire length, power losses and their ensuing optimization, and different CMOS processes. The proposed model provides valuable insights into the design of fully-integrated converters with moderate- Q bonding wire inductors.

Chapter 4

A Randomized Modulation Scheme to Mitigate Harmonics and Output Noise for Multi-Phase DC-DC Converters

4.1 Introduction

A large portion of this chapter is extracted from a paper submitted to the IEEE Transactions on Circuits and Systems I: Regular Papers [108] co-authored by the author of this thesis.

As earlier delineated in Chapter 1, there is a need for a cost- and form-factor-efficient method applicable to multi-phase converters to simultaneously mitigate the input current harmonics and the output noise.

In this chapter, we propose a randomized modulation scheme—denoted as the ‘Randomized Wrapped-Around Pulse Position Modulation scheme with Wrapped-Around Phase-Shifts (RWAPPM+WAPS)’—for multi-phase switched-mode DC-DC converters. This application of a randomized modulation

scheme is, arguably the first-ever, application of a randomized modulation scheme to multi-phase converters. The intention of the proposed RWAPPM+WAPS is to simultaneously mitigate *both* the input current harmonics and the output noise—to the best of our knowledge, our proposed RWAPPM+WAPS is the only modulation scheme to-date that can simultaneously mitigate both the input current harmonics and the output noise without the employment of external EMI filters. We achieve this by three means. First, by randomizing the pulse positions in the first phase to spread out the harmonic power, the input current harmonics are mitigated. Second, by wrapping around the pulse shifts in other phases to reduce the overlapped pulses, the output noise is mitigated. Third, by adding additional phases, the output noise is further mitigated.

In this chapter, we provide a rigorous mathematical analysis of the input current spectrum of RWAPPM+WAPS. We derive an analytical expression for the input current spectrum and the analytical expression is useful for two purposes. First, it elucidates the non-linearities, including harmonics and noise floor that are present in the input current. Second, it depicts the mechanisms, i.e., identifies the parameters that affect the said non-linearities. This is particularly useful for designers as a tool in the early design cycle of the converter to explore the trade-offs between various parameters and to ascertain their effects on the spectrum. We also provide a digital modulator design to generate the RWAPPM+WAPS pulses. In short, the proposed

RWAPPM+WAPS is a hardware-efficient method to efficiently and simultaneously mitigate the input current harmonics and the output noise to realize low-harmonic low-noise multi-phase converters.

The remainder of this chapter is organized as follows. Section 4.2 details the operation of the RWAPPM+WAPS. Section 4.3 presents the derivation for the input current spectrum of the RWAPPM+WAPS for a general N -phase converter. Section 4.4 describes the proposed digital modulator design. Section 4.5 presents the simulations performed to verify the derived expression, and the comparison on the performance of the RWAPPM+WAPS against a conventional randomized modulation scheme and multi-phase PWM. Section 4.6 concludes this chapter.

4.2 The Randomized Wrapped-Around Pulse Position

Modulation Scheme with Wrapped-Around Phase-Shifts (RWAPPM+WAPS)

Conventional randomized modulation schemes that randomize pulses to spread the power over the whole spectrum are generally applied to single-phase converters. Their applications to multi-phase converters are largely inapplicable and hence unreported because the randomized pulses in each phase may overlap each other, thereby undesirably exacerbating the noise at the output.

In this section, we will apply our previously proposed RWAPPM[8], which was previously applied only to a single-phase converter, to a multi-phase converter—the RWAPPM is employed herein because it features one of the simplest realizations, yet featuring low peak spectral power and low noise. Of specific interest, we will show that RWAPPM mitigates the input harmonics in a multi-phase converter but at the cost of exacerbated output noise. To reduce the exacerbated output noise penalty in the multi-phase converter, we propose a new modulation scheme, denoted as RWAPPM+WAPS, embodying two parts: RWAPPM that randomizes the pulses in the first phase, and WAPS that wraps around the randomized pulses in the rest of the phases to reduce the pulse overlapping. Put simply, the proposed RWAPPM+WAPS mitigates both the input harmonics and the output noise in multi-phase converters.

For the sake of illustration without loss of generality, to describe the modulation schemes, we will use a two-phase converter, where $N = 2$ in Figure 1.2 depicted earlier in Chapter 1; we will describe in Section 4.5 our extension to a general N -phase converter. We will now describe the operation of the two-phase converter using our earlier proposed RWAPPM, and thereafter, using WAP—our proposed RWAPPM+WAP.

4.2.1 RWAPPM for Two-Phase Converters

Figure 4.1 depicts the operation waveforms of a two-phase converter employing RWAPPM. For Phase 1 in the k^{th} switching-cycle, T_k , RWAPPM generates the output pulse, V_1 , with pulse width, α , and a random delay, ε_{1k} . The random delay serves to vary/modulate the equivalent switching-frequency, thereby spreading the power of the switching-frequency harmonics over the current spectrum and ensuigly mitigates the harmonics in the current spectrum.

Figure 4.1: Waveforms of a two-phase converter employing RWAPPM (a) two cases of V_1 , and (b) exacerbated output noises

The value of ε_{1k} is generally limited to the range $[0, T]$, where T is the switching-period. Depending on the value of ε_{1k} , two different pulses of V_1 in T_k can be generated. First, when ε_{1k} is small ($\varepsilon_{1k} \leq T - \alpha$), as depicted as Case 1 of V_1 in T_k in Figure 4.1(a), the generated pulse is within T_k and only one pulse is generated during T_k . Second, when $\varepsilon_{1(k+1)}$ is large ($\varepsilon_{1(k+1)} > T - \alpha$), as depicted as Case 2 of V_1 in the next switching-cycle, T_{k+1} , in Figure 4.1(a), a part of the pulse will undesirably overrun T_{k+2} . The overrun portion of the pulse is then shifted (wrapped around) to the beginning of the current T_{k+1} , and two pulses are generated during T_{k+1} .

V_1 in Figure 4.1(a) is the combination of pulses of Case 1 and Case 2. The output pulses of Phase 2, V_2 , are delayed in sequence by $T/2$ with reference to V_1 , as depicted in Figure 4.1(b). The ripple noise in each phase of the two-phase converter, in general, can to a first-order cancel each other out. However, because ε_{1k} is random for each T_k , the pulse overlapping among all phases can occur frequently. Figures 4.1(a) and 4.1(b) illustrate a scenario where the randomization of the pulses undesirably exacerbates the output noise. The overlapping pulses of V_1 and V_2 , as depicted in the hatched area in Figure 4.1(b), cause the phase currents, i_{ph_1} and i_{ph_2} , to rise. These phase currents superpose into i_C , causing increased current ripples, thereby exacerbating the output noise. Put simply, the RWAPPM, while applicable to single-phase converters [8], it is not entirely applicable to low-harmonics low-noise

multi-phase converters.

4.2.2 WAPS for Two-Phase Converters

To mitigate the aforesaid output noise, we propose to augment WAPS to the RWAPPM—denoted as RWAPPM+WAPS. In RWAPPM+WAPS, other than generating V_1 in Phase 1 with randomized ε_{1k} using the RWAPPM, as described earlier, RWAPPM+WAPS wraps around the pulse shifts in other phases to reduce overlapped pulses.

In WAPS, the V_1 pulse generated by RWAPPM previously, is delayed with a phase shift of $T/2$ in a switching-cycle T_k . This is depicted as the temporary pulse of Phase 2, $\hat{V}_2$, in Figure 4.2. The total delay of $\hat{V}_2$, ε_{2k} , in T_k is hence

$$\varepsilon_{2k} = \varepsilon_{1k} + \frac{T}{2} \quad (4.1)$$

Depending on the value of ε_{2k} , two different pulses of V_2 may be generated by WAPS, as depicted in Figure 4.2. First, if the pulse of $\hat{V}_2$ is within T_k , where $\varepsilon_{2k} \leq T - \alpha$, the pulse of V_2 is generated as $\hat{V}_2$. Second, if the pulse of $\hat{V}_2$ overruns T_k , where $\varepsilon_{2k} > T - \alpha$, the overrun part of the pulse is moved to the beginning of T_k .

Figure 4.2: A scenario of a two-phase converter employing RWAPPM+WAPS that mitigates the output noise

It can be observed that the overlapped pulses between V_1 and V_2 generated by RWAPPM in Phase 1 and WAPS in Phase 2, respectively, have been significantly reduced in Figure 4.2. The ensuing phase currents, i_{ph_1} and i_{ph_2} , can significantly cancel, to a first-order, each other out in i_C . Put simply, the proposed RWAPPM+WAPS reduces the output noise of the RWAPPM when applied to multi-phase converters—the ripple noise at i_C in Figure 4.2 is largely mitigated, whereas the current ripple at i_C in Figure 4.1(b) is largely unmitigated.

4.3 Input Current Spectrum of the RWAPPM+WAPS

We will now derive the analytical expression for the spectrum of the input current, i_{in} , for an N -phase converter in Figure 1.2 employing the proposed RWAPPM+WAPS. This expression depicts the mechanisms of the non-linearities and will be used later to explore the trade-offs. The time-domain expression of i_{in} is first obtained by summing the input phase currents (i_1 to i_N) of all phases. Subsequently, the time-domain expression is transformed to the frequency-domain expression to obtain the spectrum of i_{in} .

In Figure 4.2, we define ϕ_{nk} as the total phase-shift for the output pulse of phase n at the k^{th} switching period, T_k . We obtain ϕ_{nk} by summing ε_{1k} and the phase-shift $((n-1)/N \cdot T)$. The ensuing possible values of ϕ_{nk} are

$$\phi_{nk} = \begin{cases} \varepsilon_{1k} + \frac{n-1}{N} \cdot T, & \text{for } \varepsilon_{1k} < T - \frac{n-1}{N} \cdot T \\ \varepsilon_{1k} + \frac{n-1}{N} \cdot T - T, & \text{for } \varepsilon_{1k} \geq T - \frac{n-1}{N} \cdot T \end{cases} \quad (4.2)$$

Depending on the value of ϕ_{nk} , there are two possible cases for V_n and i_n , as depicted in Figures 4.3(a) and 4.3(b), respectively.

We define $\mathcal{X}_{nk}$ as the Bernoulli probability of Case A and B to occur in the

Figure 4.3: Two possible cases for (a) V_n and (b) i_n of phase n in a multi-phase converter employing the proposed RWAPPM+WAPS

output pulse of phase n at T_k , and is given by

$$\mathcal{X}_{nk} = \begin{cases} 0, & \text{Case A} \\ 1, & \text{Case B} \end{cases} \quad (4.3)$$

We will now derive the expression for i_n of phase n . We note that i_n is a function of time and ϕ_{nk} , and it comprises the following two current segments for Case A and Case B as

$$i_n(t; \phi_{nk}) = \begin{cases} i_{An}, & \text{for Case A} \\ i_{Bn} + i_{Cn}, & \text{for Case B} \end{cases} \quad (4.4)$$

where i_{An} is the non-zero segment of i_n in Case A, i_{Bn} and i_{Cn} are the first and the

second non-zero segment of i_n in Case B, respectively, as depicted in Figure 4.3(b).

It can be observed from Figure 4(b) that i_{An} , i_{Bn} , and i_{Cn} can be decomposed into a rectangular waveform and a ramp-up triangle waveform with the slope, k_{slope} , given as

$$k_{\text{slope}} = \frac{V_{\text{in}} - V_{\text{out}}}{L}. \quad (4.5)$$

Consequently, the analytical expressions of i_{An} , i_{Bn} , and i_{Cn} can be derived using the methodology described in our earlier work [4] as

$$\begin{aligned} i_{An}(t; \phi_{nk}) = & p_1 \cdot V_{An} \\ & + k_{\text{slope}} \cdot \left[\int_{-\infty}^t V_{An} dt - \alpha \cdot \hat{H}(t - \alpha - \phi_{nk}) \right] \end{aligned} \quad (4.6)$$

$$\begin{aligned} i_{Bn}(t, \phi_{nk}) = & p_2 \cdot V_{Bn} + k_{\text{slope}} \cdot \\ & \left[\int_{-\infty}^t V_{Bn} dt - (\phi_{nk} + \alpha - T) \cdot \hat{H}(t - \phi_{nk} - \alpha + T) \right] \end{aligned} \quad (4.7)$$

$$\begin{aligned} i_{Cn}(t; \phi_{nk}) = & p_3 \cdot V_{Cn} \\ & + k_{\text{slope}} \cdot \left[\int_{-\infty}^t V_{Cn} dt - (T - \phi_{nk}) \cdot \hat{H}(t - T) \right] \end{aligned} \quad (4.8)$$

where

I_{out} is the nominal total output current of the converter,

V_{in} is the input voltage,

V_{out} is the output voltage,

L is the inductance of the phase inductor in each phase,

α is the pulse width in each switching-period,

$\hat{H}(x)$ is the Heaviside step function,

V_{An} , V_{Bn} , and V_{Cn} are the rectangular voltage waveforms depicted in Figure 4(a)

with an unit amplitude that can be obtained from [30] as

$$V_{An} = \int_{-\infty}^{\infty} \frac{1 - e^{-j2\pi\alpha f}}{j2\pi f} e^{-j2\pi f(kT + \phi_{nk}) + j2\pi f t} df \quad (4.9)$$

$$V_{Bn} = \int_{-\infty}^{\infty} \frac{1 - e^{-j2\pi f(\phi_{nk} + \alpha - T)}}{j2\pi f} e^{-j2\pi f kT + j2\pi f t} df \quad (4.10)$$

$$V_{Cn} = \int_{-\infty}^{\infty} \frac{1 - e^{-j2\pi f(T - \phi_k)}}{j2\pi f} e^{-j2\pi f(kT + \phi_x) + j2\pi f t} df \quad (4.11)$$

and p_1 , p_2 , and p_3 are given as

$$p_1 = \frac{I_{\text{out}}}{N} - k_{\text{slope}} \phi_{nk} \quad (4.12)$$

$$p_2 = \frac{I_{\text{out}}}{N} \quad (4.13)$$

$$p_3 = \frac{I_{\text{out}}}{N} + \frac{V_{\text{in}}}{L} \cdot (\phi_{nk} + \alpha - T) - \frac{V_{\text{out}}}{L} \cdot \phi_{nk} \quad (4.14)$$

As both Case A and Case B of i_n depicted in Figure 4.3 can appear in each phase during T_k , there are 2^N possible combinations of i_n for an N -phase converter employing the proposed RWAPPM+WAPS. The general time-domain expression of i_{in} can be derived as

$$i_{\text{in}}(t - kT; \phi_{nk}) = \sum_{2^N \text{ terms}} \left(\left(\prod_{n=1}^N \lambda_n \right) \cdot \left(\sum_{n=1}^N i_n(t; \phi_{nk}) \right) \right) \quad (4.15)$$

where λ_n denotes the occurrence of either Case A ($\lambda_n = 1 - \mathcal{X}_n$) or Case B ($\lambda_n = \mathcal{X}_n$) in phase n , and i_n is defined in (4).

The input current spectrum, $S(f)$, can be obtained by substituting the Fourier Transform of i_{in} , $I_{\text{in}}(f)$, into the general randomized modulation scheme power spectrum equation in [6]. $S(f)$ is described by

$$S(f) = P_{\text{DC}} + W(f) + P(f) \quad (4.16)$$

In (4.16), P_{DC} , $W(f)$, and $P(f)$ are the DC power, noise spectrum, and the power of the switching-frequency harmonics, respectively, and their expressions are given by

$$P_{\text{DC}} = \left(\frac{\alpha I_{\text{out}}}{T} \right)^2 \quad (4.17)$$

$$\begin{aligned} W(f) = & \frac{1}{T} \cdot \sum_{2^N} \left[E \left\{ \prod_{n=1}^N \lambda_n \right\} \right. \\ & \cdot E \left\{ \sum_{n=1}^N (I_n(f)) \cdot \sum_{n=1}^N (I_n^*(f)) \right\} - \left(\prod_{n=1}^N E \{ \lambda_n \} \right) \\ & \left. \cdot E \left\{ \sum_{n=1}^N (I_n(f)) \right\} \cdot E \left\{ \sum_{n=1}^N (I_n^*(f)) \right\} \right] \end{aligned} \quad (4.18)$$

$$\begin{aligned} P(f) = & \frac{1}{T^2} \cdot \sum_{2^N} \left[\left(\prod_{n=1}^N E \{ \lambda_n \} \right) \cdot E \left\{ \sum_{n=1}^N (I_n(f)) \right\} \right. \\ & \left. \cdot E \left\{ \sum_{n=1}^N (I_n^*(f)) \right\} \right] \cdot \sum_{q=-\infty, q \neq 0}^{q=\infty} \hat{H} \left(f - \frac{q}{T} \right) \end{aligned} \quad (4.19)$$

where the operator $*$ denotes a conjugate operation, and $E \{ \cdot \}$ denotes the expectation (statistical average) operation.

The $W(f)$ and $P(f)$ in (18) and (19) delineate the presence of noise and harmonics, respectively, in the input current of the multi-phase converter employing RWAPPM+WAPS, and the parameters that affect the magnitude of the noise and the harmonics. These derived expressions are useful and insightful as they provide an

analytical means to estimate the spectrum of a converter design without resorting to time-consuming circuit simulations and measurements—see Section V later. As the mechanisms of noise and harmonics are depicted therein, these equations also provide a useful means for trading off between the different parameters.

4.4 Proposed RWAPPM+WAPS Digital Modulator

In this section, we will first describe the extension of the proposed RWAPPM+WAPS modulation scheme, depicted earlier in Section II for a two-phase convert, to a general N -phase converter. Thereafter, we will propose a digital modulator design that implements the proposed RWAPPM+WAPS. The digital modulator design will be used in Section V for a two-phase converter and a three-phase converter design employing RWAPPM+WAPS.

4.4.1 RWAPPM+WAPS for N -Phase Converters

Figure 4.4 depicts our suggested procedure to setup the proposed RWAPPM+WAPS for an N -phase converter. In Box 1, the inputs are the number of phases N , the switching-period T , and the pulse width α . With these inputs for Phase 1, the RWAPPM is thereafter applied in Boxes 2-5, and in the subsequent Phase 2 - N , WAPS is applied.

Figure 4.4: Suggested procedure to setup the proposed RWAPPM+WAPS for an N -phase converter

For Phase 1, ε_{1k} is generated first in Boxes 2-4 in Figure 4.4. Depending on the value of ε_{1k} , the pulse of V_{1k} can be delayed by ε_{1k} (Case A in Figure 4.3), or delayed and wrapped around the overrun portion $\varepsilon_{1k} + \alpha - T$ (Case B in Figure 4.3).

For the next phase in Box 6 in Figure 4.4, where $n = n + 1$, the phase shift, ϕ_{nk} , is determined based on ε_{1k} . Depending on the value of ϕ_{nk} , V_{2k} can be shifted with a phase shift of ϕ_{nk} with reference to V_{1k} , or wrapped around V_{1k} with a new phase shift value $\phi_{nk} = \phi_{nk} - T$, as depicted earlier in Figure 4.2. This WAPS procedure in Boxes 6-11 will be repeated for the remaining phases to generate the pulses in each phase.

When all the pulses in every phase of the N -phase converter have been generated for T_k , the RWAPPM+WAPS will modulate the pulses in the next switching-cycle T_{k+1} , and the entire process is repeated.

4.4.2 Digital Modulator for N -Phase Converters

We will now describe our proposed digital modulator embodying the proposed RWAPPM+WAPS for the N -phase converter. Figure 4.5 depicts the block diagram of the proposed digital modulator.

Figure 4.5: Block diagram of the proposed digital modulator implementing RWAPP+WAPS for an N -phase converter

The proposed modulator consists of three main blocks described as follows:

1) ε_{1k} *Generator*: The ε_{1k} generator performs the operations of Boxes 2 in Figure 4.4 to generate a pseudo-random delay for Phase 1 in the N -phase converter. The linear feedback shift register(LFSR) [109] method is generally employed to realize the ε_{1k} generator because it is hardware-efficient, where only M shift registers and several XOR gates are required to generate the $2^M - 1$ different random values. The resolution of the ε_{1k} generator based on the LFSR method can be easily reconfigured by adding additional or removing existing shift registers, depending on the specifications of the converter.

2) ϕ_{nk} *Generator*: The ϕ_{nk} generator performs the operations from Stage 3 to Stage 9 in Figure 4.4 to generate the phase shifts, ϕ_{1k} to ϕ_{Nk} , in each phase based on the proposed RWAPP+WAPS. Note that for a multi-phase converter, ε_{1k} is

directly used as ϕ_{1k} .

3) *Pulse Generator*: The pulse generator performs the operations of Stage 10 in Figure 4.4 to generate the pulses, V_1 to V_N , with pulse width, α . The pulse generator is a counter-based structure that delays the pulse according to the value of ϕ_{nk} in each phase. Based on ϕ_{nk} , the generated pulse is either Case A or Case B, as depicted in Figure 4.3.

The proposed modulator can be realized by using digital gates only and hence is easy to implement and hardware-efficient. We will employ the proposed digital modulator later in a two-phase and a three-phase converter as design examples to simulate and verify our proposed RWAPPM+WAPS.

4.5 Simulation and Measurement Results

We will now employ our proposed digital modulator in a two-phase and a three-phase prototype converter. To verify our derived analytical expression in Equation (4.16), we compare the input current spectra predicted by the expression in Equation (4.16) against those obtained from simulations and measurements of these converters. For benchmarking of spread-spectrum modulation schemes for multi-phase converters, we will compare our proposed RWAPPM+WAPS against RWAPPM to show that our proposed RWAPPM+WAPS can efficiently and

(a)

(b)

Figure 4.6: Analytical, simulated and measured input current spectra of (a) a two-phase converter employing RWAPPM+WAPS, (b) a three-phase converter employing RWAPPM+WAPS

(a)

(b)

Figure 4.7: Simulated input current spectra of (a) a two-phase converter employing RWAPPM, and (b) a three-phase converter employing RWAPPM.

simultaneously mitigate the input current harmonics and the output noise.

The two- and three-phase converters are designed to operate with $V_{in} = 3.3$ V, $V_{out} = 2.5$ V, average $f_{sw} = 100$ kHz, $\alpha = 7.5$ μ s (equivalent to a duty cycle of 0.75), and $I_{out} = 200$ mA. The inductor, L , for each phase is 103 μ H and the single output capacitor, C_{out} , is 13 μ F. The pulses in Phase 1 of the two-phase converter are generated with randomized ε_{1k} values. For fair comparison, the generated ε_{1k} values will also be employed to generate the pulses in Phase 1 of the three-phase converter. Both converters are designed to operate in an open-loop configuration to depict the real advantages of the proposed RWAPPM+WAPS, i.e., avoiding the interferential compensation in closed-loop that may otherwise mask the advantages. The prototype converters employ Si3585DV N- and P- channel MOSFET as the power transistors, and the measurements are performed using the same test conditions.

Consider first the verification of the analytical expression in Equation (16) to predict the input current spectrum. Figures 4.6(a) and 4.6(b) depict the input current spectra obtained analytically from Equation (16), simulations (SPICE), and measurements for the two- and the three-phase converters, respectively, both employing RWAPPM+WAPS. The power along the ordinate is depicted in dB with respect to full scale (dBFS) with a resolution bandwidth (RBW) of 200 Hz along the abscissa. For the sake of illustration, the input current spectrum is shown up to 800 kHz, i.e., $8\times$ of the average f_{sw} . A perusal of Figures 4.6(a) and 4.6(b)

depicts that, in general, for both the two- and three-phase converters employing our proposed RWAPPM+WAPS, all spectra obtained by measurements, simulations, and analytical results agree well, thereby verifying the derived analytical expression (16).

Consider now the benchmarking of RWAPPM+WAPS against RWAPPM for the two-phase converter and the three-phase converters. Figures 4.7(a) and 4.7(b) depict the simulation results of the two- and three-phase converters based on the same operating conditions but employing RWAPPM. From the perusal of Figures 4.6 and 4.7, we make the following observations.

The peak spectral power of the two-phase converters employing RWAPPM+WAPS in Figure 4.6(a) and RWAPPM in Figure 4.7(a) is approximately the same, ~ -28 dBFS. This is expected because the pulses in the first phase of the two converters are randomized employing the same RWAPPM method. However, the peak spectral power of the three-phase converter employing RWAPPM+WAPS (Figure 4.6(b)) markedly mitigated over that for RWAPPM (Figure 4.7(b))— -35.5 dBFS versus -31.9 dBFS, respectively. This marked improvement is also expected because the wrapped-around randomized pulses in the third phase will further spread the power of the harmonics over the whole current spectrum. Consequently, for a converter with an even higher number of phases, the peak spectral power would be further mitigated.

From a practical perspective, there are two considerations for the number of phases employed in a multi-phase converter. First, augmenting additional phases will need more components, e.g., inductors and power transistors, which leads to increased cost. Second, augmenting additional phases renders challenges with phase management, which leads to the increased modulator design complexity. At this juncture, multi-phase converters are generally designed with a maximum of three phases.

Consider now the mitigation of the output noise. Figures 4.8(a) - (b) and Figures 4.9(a) - (b) respectively depict the measured output voltage spectrum of the two- and the three-phase converters employing the spread-spectrum modulation schemes—the proposed RWAPPM+WAPS and the conventional RWAPPM. Similarly, for the sake of illustration, the output voltage spectrum are depicted up to 800 kHz. The output root-mean-square (rms) noise are calculated from the measured output voltage spectrum in Figures 4.8(a) - (b) and Figures 4.9(a) - (b) and are tabulated in Table 4.1. We make three observations.

First, the output rms noise is efficiently mitigated by our proposed RWAPPM+WAPS. For the two-phase converters, the output rms noise of the converter employing the proposed RWAPPM+WAPS and the conventional RWAPPM are 47.3 mV and 74.3 mV, respectively. Similarly, for the three-phase

(a)

(b)

Figure 4.8: Measured output voltage spectra of (a) a two-phase converter employing RWAPPM+WAPS, and (b) a three-phase converter employing RWAPPM+WAPS.

(a)

(b)

Figure 4.9: Measured output voltage spectra of (a) a two-phase converter employing RWAPPM, and (b) a three-phase converter employing RWAPPM.

Table 4.1: Output rms Noise for Two- and Three-Phase Converters Employing RWAPPM+WAPS and RWAPPM

Output rms Noise (mV)	Two-Phase	Three-Phase
RWAPPM+WAPS	47.3	39.3
RWAPPM	74.3	82.6

converters, the output rms noise of the converter employing the proposed RWAPPM+WAPS and the conventional RWAPPM are 39.3 mV and 82.6 mV, respectively. In short, our proposed RWAPPM+WAPS can efficiently mitigate the output noise in a multi-phase converter, i.e., the output rms noise of our proposed RWAPPM+WAPS is significantly lower than conventional RWAPPM, by $1.6\times$ (27 mV) and $2.4\times$ (43.3 mV), for two- and three-phase converters, respectively.

Second, the output noise of converters employing our proposed RWAPPM+WAPS is further mitigated when a phase is augmented. Specifically, the output rms noise of the two- and three-phase converters are 47.3 mV and 39.3 mV, respectively, i.e., the output rms noise is further mitigated by 8 mV from two-phase to three-phase. As delineated earlier, the mechanism for the lower output noise of RWAPPM+WAPS with additional phases is that the number of overlapped pulses in all phases is reduced (due to the WAPS). Nevertheless, from a practical

perspective, due to cost and modulator complexity concerns, the maximum number of phases of practical converters is generally limited to three phases.

Third, contrary to the aforesaid two, the output rms noise is exacerbated in converters employing the conventional RWAPPM when phases are augmented. Specifically, the output rms noise of the two-phase converter employing RWAPPM is 74.3 mV, and increases to 82.6 mV for the three-phase converter, i.e., 8.3 mV worse. This increased output rms noise is expected, as explained earlier, because the randomized pulses in each phase may continuously overlap, thereby exacerbating the output noise. Put simply, the conventional RWAPPM scheme, unlike the proposed RWAPPM+WAPS, is not appropriate for multi-phase converters.

For completeness, consider now the input current power spectrum and the output rms noise for the two- and three-phase converters employing PWM. These are respectively depicted in Figures 4.10 and 4.11, respectively. The calculated output rms noise from Figure 4.11(a) and Figure 4.11(b) are 23.4 mV and 15.8 mV for the two- and three-phase converters employing PWM, respectively. We make the following observations for converters employing PWM and that employ RWAPPM and RWAPPM+WAPS.

First, as explained earlier, the input current power spectrum for multi-phase converters employing PWM is significantly higher than that for the same employing

Figure 4.10: Measured input current spectra of a (a) two-phase converter employing PWM, and (b) three-phase converter employing PWM.

(a)

(b)

Figure 4.11: Measured output voltage spectra of a
(a) two-phase converter employing PWM, and (b) three-phase converter employing PWM.

spread-spectrum modulation schemes. Specifically, the peak input current spectral power for a two-phase and a three-phase converter employing PWM are -10.5 dBFS and -16.6 dBFS, respectively. These compare rather poorly against -28.3 dBFS and -31.9 dBFS of the two- and three-phase RWAPPM, respectively, and against -28.4 dBFS and -35.5 dBFS of the two- and three-phase RWAPPM+WAPS, respectively. The maximum peak spectral power difference between the converter employing PWM and the proposed RWAPPM+WAPS is a very significant 18.9 dB (35.5 dBFS $- 16.6$ dBFS), or $100\times$ larger.

Second, further to the said first, the peak spectral power of the input current of converters employing PWM reduces with an increasing number of phases. This is similar to the reduction of the input current peak spectral power with additional phases in converters employing spread-spectrum modulation scheme. Specifically, the peak input current spectral power for a three-phase converter employing PWM are -16.6 dBFS, i.e., 6.1 dBFS lower than that of a two-phase converter.

Third, a perusal of Figures 4.6 - 4.11 depicts that the markedly improved input current spectrum of the multi-phase converters employing spread-spectrum modulation schemes over that of the PWM is at the cost of output rms noise. The output rms noise for a two-phase converter employing the PWM, RWAPPM, and RWAPPM+WAPS are 23.4 mV, 74.3 mV, and 47.3 mV, respectively. For a three-phase converter, the output rms noise are 15.8 mV, 82.6 mV, and 39.3

mV, respectively. The mechanism for this is, as explained earlier, the uniformly distributed PWM pulses have the least overlapping in all phases. However, as expected, the peak output noise harmonics of converters employing PWM is the largest of the three (due to the large input current harmonics), i.e., -35 dbFS for a two-phase converter and -40 dbFS for a three-phase converter. Put simply, although the multi-phase converter employing the PWM expectedly features the lowest output rms noise, it suffers from severe input current harmonics and output noise harmonics.

4.6 Conclusions

We have proposed a randomized modulation scheme, denoted as RWAPPM+WAPS, for multi-phase switched-mode DC-DC converters—arguably the first application of a randomized modulation scheme in multi-phase converters. Our proposed RWAPPM+WAPS can efficiently and simultaneously mitigate the input current harmonics and the output noise over other randomized modulation schemes. We have also provided a rigorous mathematical analysis of the input current spectrum of RWAPPM+WAPS, including the derivation of an analytical expression to predict the input current spectrum. By means of converter designs employing our proposed modulation scheme and the RWAPPM, and by simulations and measurements, we have verified our derived expression and the significant reduction in the input current harmonics and the output noise.

Chapter 5

Conclusions and Recommendations

This chapter draws the conclusions of the work reported in this Ph.D. research program and delineates recommendations for future work.

5.1 Conclusions

The overall objectives of this Ph.D. research program pertained to single-phase and multi-phase inductive DC-DC converters.

For the former, the objectives included the modeling and power analysis for power-efficiency optimization of a single-phase fully-integrated inductive DC-DC converter with a bonding wire inductor. The primary intention of these objectives was a comprehensive model that accounted for both the AC and DC power losses of the bonding wire inductor, and its applicability to both CCM and DCM operations of the fully-integrated converter.

For the latter, the objectives included the proposal and verification of a randomized modulation scheme for a multi-phase (fully-integrated and

non-fully-integrated) inductive DC-DC converter—of particular note, to the best of our knowledge, this would be the first-ever application of a randomized modulation scheme for a multi-phase converter. The primary intention of the proposed randomized modulation scheme is to efficiently and simultaneously mitigate both the input harmonics and output noise of a multi-phase converter.

The conclusions of the research work presented in this thesis are as follows.

In Chapter 1, the motivation, objectives, and contributions of this Ph.D. program have been presented in this thesis.

In Chapter 2, different converter topologies, inductor integration technologies, converter power loss types, and conventional randomized modulation schemes have been reviewed.

In Chapter 3, a comprehensive model for optimizing the power efficiency of a single-phase fully-integrated inductive buck converter with a moderate- Q bonding wire inductor has been proposed. We have derived analytical expressions that include both the DC and AC power losses of the bonding wire inductor, and the power loss of the power transistors and their gate drivers. Our derived expressions emphasized the AC power loss of the inductor that was previously ignored or inadvertently assumed to be negligible in reported works, and the power loss of the gate drivers accounted for their readily determined design parameters. We have shown that the AC power

loss of the inductor can be considerable for fully-integrated converters.

We have verified our model by means of simulations and measurements of a prototype fully-integrated inductive buck converter fabricated in a 65nm CMOS process. We have provided applications of our proposed model in three-perspectives—bonding wire length, power losses and their ensuing optimization, and different CMOS processes. We have delineated the valuable insights provided by our proposed model into the design of fully-integrated converters with moderate- Q bonding wire inductors.

In Chapter 4, a randomized modulation scheme for multi-phase switched-mode DC-DC converters, denoted as RWAPPM+WAPS, has been proposed. The proposed RWAPPM+WAPS has been shown to efficiently and simultaneously mitigate the input current harmonics and the output noise in a multi-phase converter over other randomized modulation schemes. We have provided a rigorous mathematical analysis of our proposed RWAPPM+WAPS, including the expressions of randomized input current, the DC power, the noise spectrum, and the power of switching-frequency harmonics. We have shown that our analytical expressions elucidated the non-linearities, including harmonics and the noise floor that are present in the input current, and can depict the mechanisms, i.e., identify the parameters that affect the said non-linearities. Of particular note, we have proposed a digital modulator employing our proposed RWAPPM+WAPS. The proposed digital

modulator has been shown to be easily implemented by using only digital gates, and hardware-efficient.

We have provided a demonstration of the efficacy of the proposed modulation by means of investigations on a two-phase and a three-phase converter employing our proposed RWAPPM+WAPS and RWAPPM, respectively. The efficacy of a three-phase converter employing our proposed RWAPPM+WAPS has been shown. Particularly, its peak input current spectral power and output noise ripple were significantly reduced over the same converter employing RWAPPM—by 3.6 dB (equivalent to $3.3\times$) and 200.3 mV (equivalent to $9.9\times$), respectively.

Chapter 5 herein draws the conclusions of this thesis and suggests recommendations for future work.

5.2 Recommendations for Future Work

On the basis of the literature review and the research work in this research program, the following future work is recommended:

- (i) The investigation into the application of advanced III-V fabrication technology for power transistors, e.g., the SMART-LEES (III/V-on-CMOS) process, including a critical appraisal of their merits and limitations, particularly in

view of power-efficiency and switching frequency

As depicted in Chapter 3, the power transistor is one of the major power loss contributors in the fully-integrated converter. In the context of the fully-integrated converter where the switching frequency is much higher (at least 10 $\times$) than conventional converters, III-V technologies with their lower switching-losses can possibly be used to realize the power transistors of the fully-integrated converter. In particular, we propose further investigations into the LEES-SMART III/V-on-CMOS technology for its application in fully-integrated converter designs.

- (ii) The investigation into the closed-loop multi-phase converter employing our proposed RWAPPM+WAPS

Chapter 4 has demonstrated our proposed RWAPPM+WAPS in an open-loop configuration to depict the real advantages, i.e., avoiding the interferential compensation in closed-loop that may otherwise mask the advantages. However, in view of practical implementations, converters are usually designed in a closed-loop configuration to regulate the output. We hence recommend an investigation into a closed-loop converter employing our proposed RWAPPM+WAPS, and analysis on the performance of RWAPPM+WAPS in the closed-loop multi-phase converter.

- (iii) The investigation into the modeling, power analysis, and power efficiency optimization for multi-phase fully-integrated converters employing our proposed RWAPPM+WAPS

In Chapter 4, the proposed RWAPPM+WAPS modulation scheme was shown to be attractive and can be applied to fully-integrated converters. However, as multiple inductors will be employed in the multi-phase inductor, the power loss mechanisms and power efficiency optimization of a multi-phase fully-integrated converter employing RWAPPM+WAPS can be significantly different from that of a single-phase converter employing conventional PWM. In view of this, we recommend an investigation into the modeling, power analysis, and power efficiency optimization for multi-phase fully-integrated converters employing our proposed RWAPPM+WAP.

List of Publications

Patent Publication

- [1] J. S. Chang, **Y. Sun**, and V. Adrian, “An Inductor Apparatus for DC-DC Converters,” NTU Technology Disclosure No. 2019-349, Filed Provisional Patent in Singapore

Journal Publications

- [1] **Y. Sun**, V. Adrian, and J. S. Chang, “Modeling and Power Analysis of Fully-Integrated Switched-Mode DC-DC Converters,” in *IEEE Transactions on Circuits and Systems–I: Regular Papers*, 2020 (In Review).
- [2] **Y. Sun**, V. Adrian, J. S. Chang, K. E. Cui and B. H. Gwee, “A Randomized Modulation Scheme to Mitigate Harmonics and Output Ripple Noise for Multi-Phase DC-DC Converters,” in *IEEE Transactions on Circuits and Systems–I: Regular Papers*, 2020 (In Review).

Conference Publications

- [1] **Y. Sun**, V. Adrian, and J. S. Chang, “Power-Loss and Design Space Analysis for Fully-Integrated DC-DC Converters,” in *IEEE International Symposium on Circuits and Systems (ISCAS)*, 2018.08
- [2] **Y. Sun**, V. Adrian, T. Ge and J. S. Chang, “A Circuit for Reducing the Reverse Current in DCM DC-DC Converters,” in *IEEE 23rd International Conference on Digital Signal Processing (DSP)*, 2018.
- [3] K. E. Cui, V. Adrian, **Y. Sun**, B. H. Gwee, and J. S. Chang, “A low-harmonics low-noise randomized modulation scheme for multi-phase DC-DC converters,” in *2017 IEEE International New Circuits and Systems (NEWCAS)*, 2017.
- [4] **Y. Sun**, V. Adrian, and J. S. Chang, “A novel high-rate hybrid window ADC design for monolithic digitally-controlled DC-DC converters,” in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017.
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