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**CHARACTERIZATION OF NEGATIVE BIAS
TEMPERATURE INSTABILITY IN ULTRA-THIN
OXYNITRIDE GATE P-MOSFETS**

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SUMMARY

Negative Bias Temperature Instability (NBTI) is a critical reliability issue of metal-oxide-semiconductor field effect transistors (MOSFETs) due to imperfections located at the oxide-semiconductor interface. However, several problems on NBTI remain unclear or controversial, such as the mechanisms controlling NBTI; physical characteristics of NBTI-induced interfacial imperfections, etc. Therefore, the target of this project is to investigate these significant problems.

According to the conventional Reaction-Diffusion model, interface traps are generated at the Si-SiO₂ interface, due to the dissociation of Si-H bonds during NBTI stressing. Interface traps were believed to be the only interfacial imperfections that cause NBTI-induced degradation. In this project, however, it is found that deep-level oxide charges with distinct physical origins play a significant role in the NBTI problem. These deep-level trapped charges are located in the oxide near the Si-SiO₂ interface, but of high energy states beyond the electron tunneling energy window and the charge pumping current measurement capability. Therefore, they contribute to an important portion of threshold voltage shift during NBTI stressing, and remain charged after the stress is terminated. Furthermore, more nitrogen in the gate oxide enhances the generation of deep-level hole traps and results in severer threshold voltage shift.

Besides, activation energy of NBTI-induced degradation was studied. Contrary to the single activation energy of the conventional SiO₂ gate p-MOSFET, two distinct activation energies were obtained on ultra-thin oxynitride gate p-MOSFETs. One of the activation energy coincides with that obtained from conventional SiO₂ gate p-MOSFET; while the other activation energy is much smaller, representing a thermally-insensitive mechanism. Compared to the conventional mechanism, the thermally-insensitive mechanism is less dependent on temperature and stress time, but more sensitive to nitrogen in the gate oxide. With more nitrogen in the gate oxide, degradation due to the thermally-insensitive mechanism is significantly increased. This novel nitrogen-related thermally-insensitive NBTI mechanism superposes on the conventional mechanism, leading to severer degradation of oxynitride p-MOSFETs.

NBTI-induced degradation under ac stress was studied. Threshold voltage shift was observed to have inverse dependence on the gate frequency. Furthermore, more nitrogen in the gate oxide leads to weaker frequency dependence of NBTI-induced degradation. The weaker frequency dependence was believed to be due to the significant role of deep-level hole traps. The strategic energy states of nitrogen-related deep-level hole traps ensure that they remain charged albeit the alternative change of the gate stress polarity. NBTI-induced degradation due to deep-level hole traps remains important under ac stress.

In this project, impacts of temperature, NBTI stress time, nitridation conditions in the

gate oxide, and ac stress frequency on NBTI were investigated. A novel nitrogen-related thermally-insensitive mechanism was revealed to superpose on the conventional mechanism, and lead to severer NBTI-induced degradation of nano-scale oxynitride gate p-MOFETs. In addition to interface traps, nitrogen-related deep-level hole traps with distinct physical origin were found to play a significant role during dc and ac NBTI stressing. These new observations on ultra-thin oxynitride gate p-MOSFETs supplement the conventional NBTI model, and provide a more comprehensive understanding of NBTI mechanisms.

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Chapter 1 Introduction

1.1 Introduction to MOSFET

The invention and application of semiconductor-based microchip is one of the most important technological progresses in 20th century. Semiconductor-based microchips operate as the "brains" of a wide spectrum of man-made machines, ranging from sophisticated spacecrafts, ultra-fast data-crunching computers to life-saving medical instrumentation and electronic gadgets. It was the stable operation of these machines that changed the industry based society into information and knowledge based society. The drive force of microchips is the metal-oxide-semiconductor field-effect-transistor (MOSFET), which is a switch controlled by the voltage supply on the gate electrode. Millions of MOSFETs combine and co-function with other components as an integrated circuit. The terminology of MOSFET was first utilized for old-generation transistors using metal as the gate, SiO₂ as the gate dielectric, and silicon as the substrate. For state-of-the-art transistors, metal gate is replaced by p⁺-poly silicon gate, especially for high-density fabrication, as poly-silicon gate is more compatible with the gate oxide than metal gate. And the gate oxide is not always pure SiO₂; in some applications nitrogen is added for better transistor performance; in some applications other materials with higher dielectric constant could replace SiO₂ as well. However, the terminology of MOSEFT is still utilized nowadays. During the past 50 years, the performance of semiconductor products has been continuously improved by scaling

down the dimensions of MOSFETs. The smaller the linear dimension of MOSFETs is scaled, the higher packing density, the higher speed, and the lower power dissipation an IC could achieve. Therefore, semiconductor products such as computers could offer superior performance, dramatically reduced cost and reduced physical size. A widely accepted description of the evolution of MOSFET technology is Moore's law. According to this principle proposed by G. E. Moore in 1965, the number of components per chip would double each year for the following 10 years, and the double in the component density would require ~ 2 years subsequently [1,2]. Along with such an aggressive scaling down of integrated circuits is the reduction in the fabrication cost. In the past 50 years, MOSFET technology has been advanced to 45 nm generation and further miniaturization of integrated circuit is still in progress.

1.2 Critical Issues in the Scaling Down of MOSFET

If the scaling down of MOSFET dimensions is achieved by a ratio of α (<1), with proper adjustment of supply voltage ($\times\alpha$) and doping conditions ($/\alpha$), the electric field in the MOSFETs will remain invariant ideally. Thus the circuit speed will be improved by a factor of α , and the circuit density will be increased by α^2 [3]. However, the operation temperature of MOSFETs is not scaled down together with the dimensions, thus the off current would be degraded. Consequently the threshold voltage would be higher, and the power density would increase over time as well. On the other hand, to ensure the performance of MOSFETs in higher density, the supply voltage could not be scaled as much as linear dimensions [3]. Thus the electric field in

operation becomes larger, leading to severer failure mechanism or reliability issues. The critical front-end issues with the scaling down of MOSFET are briefed as follows.

1.2.1. Short Channel Effect

Short Channel Effect (SCE) takes place when the effective channel length of a MOSFET is comparable to the source (or drain) junction depletion width. The electric field distribution in the channel becomes two-dimensional. One of the SCE models is charge sharing model. In this case, the fraction of charge in the channel region controlled by the gate decreases as the channel length decreases. Fig. 1.1 shows the charge sharing condition in this model.

Fig. 1.1 Charge sharing in the short channel threshold voltage model [4].

Assuming the lateral diffusion distance under the gate is the same as the vertical diffusion distance, only the charge in the trapezoidal region under the gate is controlled by the gate. Thus threshold voltage V_{th} will be shifted by ΔV_{th} [4].

$$\Delta V_{th} = -\frac{qN_a W_{dm}}{2C_{ox}} \cdot \frac{L - L'}{L} \quad (1.2.1-1)$$

N_a in Eq. 1.2.1-1 is the doping concentration in the substrate; q is electron charge; W_{dm} is the space charge width; and C_{ox} is the capacitance of the gate oxide per unit

area. Another SCE model named drain-induced barrier lowering (DIBL) interpret SCE from a different view. If the channel length is very small, the distance between the source and drain is too short. The drain bias reduces the peak value of the energy barrier in the channel, thus leading to increased leakage current into the channel and reduced threshold voltage. Retrograde doping profile in the channel and halo implants may be utilized to improve short channel effect [5].

1.2.2. Hot Carrier Injection

Hot Carrier Injection (HCI) happens as the voltage supply scaling down becomes more and more difficult to achieve certain circuit operation margin. When the voltage applied on the drain and gate is less scaled down than the channel length, the lateral electric field and the vertical electric field near the drain is increased. Thus carriers traveling from the source to the drain could gain sufficient energy to cause impact ionization which generates electron-hole pairs. The carriers with enough energy could be injected into the gate dielectric and get trapped by interface states and oxide traps, leading to threshold voltage shift, transconductance degradation and drain current degradation [6, 7]. HCI-induced degradation is severer in *n*-type MOSFET than *p*-type MOSFET, since the carriers for nMOSFET are electrons with higher mobility and lower energy barrier than holes in pMOSFET. Drain engineering such as introducing a graded-drain structure near the drain junction, with a space-charge transition region with lower doping concentration than the drain, is utilized to alleviate HCI-induced degradation [6, 7]. The profile of lateral electric field in the

channel could be improved by reducing the peak electric field near the drain junction. As interface states near the SiO_2/Si interface and oxide traps in the gate oxide are believed to be responsible for HCI, gate oxide engineering such as thermal nitridation and fluorine implantation have been used as well to reduce HCI-induced degradation [7]. HCI was the major reliability issue in older generation technologies, but another reliability issue NBTI becomes more and more significant in limiting the lifetime of new generation CMOS circuit, which will be discussed in later sections.

1.2.3. Gate dielectric reliability issues

As the channel length/width of MOSFETs is shrinking, the oxide thickness is required to scale down proportionally to guarantee the gate control over the channel. The gate oxide for new generation technology is scaled down to less than 2nm, which is composed by only a few atomic layers. For such ultra-thin gate oxide, quantum tunneling take places and the leakage current increases exponentially as the oxide thickness is reduced [8]. Higher leakage current leads to undesirable power consumption and time dependent gate dielectric breakdown. Adding nitrogen into SiO_2 or replacing SiO_2 with other materials with higher dielectric constant is a solution to the leakage current related reliability issues. These materials ensures a physical gate dielectric thickness large enough to block leakage current, meanwhile exhibit a small electrical oxide thickness (EOT) to retain good gate control [9].

In addition to leakage current, boron penetration is another reliability issue that arises

with oxide thickness scaling down. In advanced CMOS fabrication process, a *p*-type poly-silicon gate electrode containing boron replaces *n*-type gate electrode, to make a surface-channel *p*-MOSFET instead of a buried-channel *p*-MOSFET due to reduced short channel effect and better turn-off characteristics of surface channel *p*-MOSFET [10]. With the scaling down of gate oxide thickness, boron in the gate electrode can easily diffuse into the substrate through the gate oxide, and shifts threshold voltage [11]. Experiential solution to boron penetration is incorporating nitrogen into gate oxide [12]. However, nitrogen incorporation in the gate oxide leads to worse NBTI-induced degradation. Furthermore, how nitrogen behaves in preventing boron penetration is not well-understood yet.

1.2.4. Negative Bias Temperature Instability (NBTI),

As mentioned in the last few sections, it is not HCI but NBTI that limits the lifetime of new generation CMOS circuits. Furthermore, the incorporation of nitrogen initially utilized to prevent boron penetration leads to worse NBTI-induced degradation. Negative Bias Temperature Instability (NBTI) refers to the degradation of *p*-type metal-oxide-semiconductor field-effect transistor (MOSFET) performance due to the accumulation of positive trapped charges along the SiO₂-Si interface under negative gate bias at elevated temperature. Fig. 1.2 illustrates the NBTI stressing of a *p*-MOSFET. A negative voltage bias is applied on the gate with the other terminals grounded. Under such a gate stress at elevated temperature (75~125°C), more and more interface traps and positive charges are generated near the SiO₂-Si interface and

in the SiO₂.

Fig. 1.2 Schematic diagram of *p*-type MOSFET under NBTI stressing. × denotes interface traps. + denotes positive trapped charge in the gate oxide near the Si-SiO₂ interface.

Fig. 1.3 Degradation of drain current after 70000s NBTI stress. Gate bias is -2.6V; stress temperature is 398K. Compared to the drain current of the fresh device, drain current after NBTI stress is decreased.

Along with NBTI stress, the p-MOSFET suffers from smaller drive current I_{dsat} , higher threshold voltage $|V_{\text{th}}|$, and smaller carrier mobility μ , etc. Fig. 1.3 shows the

drain current I_d versus drain voltage V_d characteristics before and after NBTI stress. After 70000s NBTI stress, about 5% reduction in the saturation drain current is observed.

Besides drain current degradation, threshold voltage of the p-MOSFET is also increased in magnitude. As shown in Fig. 1.4, the gate bias (V_g) is swept from 0V to -1V, meanwhile drain current (I_d) is measured. After 70000s NBTI stress, the I_d - V_g curve is shifted to the right side, i.e., a shift towards negative V_g is observed. As shown by the offset in Fig. 1.4, a shift of $\sim 30\text{mV}$ in the threshold voltage is observed after 70000s stress.

Fig. 1.4 Shift of the drain current versus gate voltage curve following NBTI stress. Stress conditions are the same as in Fig. 1.3. Significant shift in threshold voltage is shown by the arrows.

Contrast to hot carrier injection, NBTI-induced degradation in the performance of n-type MOSFET is not as significant as in p-type MOSFET [13]. However, the introduction of Complementary MOS (CMOS) invertors made p-MOSFETs as

important as nMOSFETs for IC design. Degradation in the drive current of pMOSFETs due to NBTI will finally lead to the speed reduction of CMOS circuits. And NBTI-induced degradation of p-MOSFETs limits the lifetime of CMOS invertors rather than HCI-induced degradation of n-MOSFETs, especially for new generation ultra-thin gate devices [14]. As the focus of this thesis, more detailed review and studies on NBTI will be provided in later sections.

1.3 Back Ground of Negative Bias Temperature Instability

1.3.1. A Brief of Historical NBTI Theories

NBTI was reported as early as 1966. Generation of positive charges was observed in the oxide near the Si-SiO₂ interface, with a negative bias on the Al electrode on the gate [15, 16]. Goetzberger *et al.* observed constant flatband voltage during negative gate bias stress, thus proposed a model attributing the charge generation to space charge limited emission of positive ions from the silicon into the gate oxide [16]. But later in 1973, logarithmic time dependence was reported by the same group [17]. Equal generation of positive oxide charges and interface traps was observed by Deal *et al.* in 1967 [18]. In addition, they reported that the density of positive charges in the oxide near the SiO₂-Si interface during negative gate bias stressing is independent of either gate oxide thickness or applied voltage, but proportional to oxide electric field and initial positive oxide charge density. Based on their experimental results and analysis, Deal's group explained the generation of positive charges in the oxide near the SiO₂-Si interface as related to the excess silicon ions in the gate oxide, very near

to the SiO_2 -Si interface [18]. Although some of the experimental observations from these groups were reproduced by later researches, their attempts to model NBT-induced positive surface charges were not well supported by experimental evidences.

Fig. 1.5 Energy diagram of the oxide charge centers. V_{FB} is the flatband voltage and V_b is the negative bias voltage applied to the gate of the MOS device. (a) Flat band condition: The centers are neutral and the ground states of the centers lie below the top of the valence band of the silicon. The centers have excited states, $E_A \approx 1.3$ eV. (b) Charging of the centers: The negative bias voltage causes a number of ground states to be raised above the Fermi level. These active centers become positively charged by the thermal emission of electrons to the excited states, from which the electrons tunnel to the silicon. [Data after Ref. [19]]

Breed proposed a thermally assisted electron tunneling model in 1975 to explain the generation of positive charges in the gate oxide [19]. As shown in Fig. 1.5, neutral “centers” are distributed throughout the oxide near the interface. At flat band

condition (Fig. 1.5(a)), the ground states of these centers lie below the valence band of the silicon substrate, while the excited states are ~ 1.3 eV above. Under a negative gate bias (Fig. 1.5(b)), part of these ground states are raised above the Fermi level. Electrons in the ground states can be thermally emitted into the excited states, from which the electrons tunnel into the conduction band of the silicon substrate, resulting in the formation of positively charged centers in the oxide. The contribution from interface traps was not included in this model. The time and temperature dependence of oxide charging was explained as follows: The charging rate is determined by the occupation probability of the excited states by electrons, which is temperature dependent. Another factor controlling the charging rate is the tunneling probability of electrons from the excited states in the oxide into the silicon substrate, which results in a logarithmic time dependence of positive oxide trapped charge generation.

These pioneer research work on NBTI-induced degradation of p-MOSFETs reported the shift of physical parameters during NBTI stressing, such as change of flat band voltage, generation of positive charges at SiO_2 -Si interface and in the oxide near the interface, etc. Besides, influence from oxide electric field, applied gate bias, oxide thickness, and fabrication process were investigated. But no detailed model was established which well explains the chemical/physical mechanisms leading to the generation of positive charges.

1.3.2. Reaction-Diffusion Model

1.3.2-1. Classical Reaction-Diffusion Model

In 1977, Jeppson and Svensson proposed a systematic explanation for NBTI [20]. A two-phase reaction-diffusion (R-D) model was established. Since then, the R-D model became the most popular model for NBTI, although some modifications by later researchers were necessary to make it applicable for state-of-the-art p-MOSFETs.

Al-oxide-Si MOSFETs were stressed at varying oxide electric field and temperature. After a certain period of NBTI stress, the gate bias was removed and the temperature cooled down to room temperature. Interface trapped charge density (N_{it}) was monitored using capacitance voltage (C-V) technique. On the other hand, oxide trapped charge density (N_{ot}) was calculated from mid-gap voltage shift [20]. During NBT stressing, equal generation of interface trapped charge and oxide trapped charge was observed independent of oxide electric field and temperature. After stress at high temperature (125°C), the density of stress-induced interface trapped charge, ΔN_{it} was observed to exhibit a power-law dependence on stress time, i.e., $\Delta N_{it} \propto t^n$, $n \sim 0.25$. At room temperature the $t^{1/4}$ dependence is valid for low oxide field; for oxide field larger than 6.3 MV/cm the formation of N_{it} becomes proportional to stress time.

Based on the experimental observations above, a two-phase Reaction-Diffusion model is proposed for NBTI-induced charge generation [20]:

Phase A (Eq. 1.3.2-1a): Interface trap precursors are dissociated via certain chemical reaction, forming interface traps at the SiO₂-Si interface and oxide trapped charge in the SiO₂ near the interface. The species X and e^- are other resultants. Phase B (Eq. 1.3.2-1b): The species X diffuse from the SiO₂-Si interface towards SiO₂ bulk. This two-phase process agrees well with the observation that equal numbers of interface traps and oxide trapped charge are generated. The recovery of NBTI-induced device degradation is also taken into account by the model. When the species X diffuse back to the interface, the reverse reaction relaxes part of generated N_{it} and N_{ot} , i.e., both reactions shown by Eq. 1.3.2-1a and Eq. 1.3.2-1b take place towards left side.

Therefore, the generation rate of N_{it} may be expressed as follows [20]:

$$\frac{\partial N_{\text{it}}}{\partial t} = \underbrace{A(N_{\text{D}} - N_{\text{it}})}_{\text{Generation}} - \underbrace{BN_{\text{it}}C_{\text{Xi}}}_{\text{Relaxation}} \quad (1.3.2-2)$$

The first term of Eq. 1.3.2-2 denotes the generation of N_{it} ; while the second term denotes the recovery of N_{it} by back diffusion of the species X . In Eq. 1.3.2-2, N_{D} is the initial concentration of interface defects; C_{Xi} is the concentration of the species X at the interface; and A and B are field-dependent rate constants.

If this two-phase R-D process is diffusion limited rather than reaction-rate limited, the generation rate of N_{it} is controlled by the diffusion of X away from the interface [20]:

$$\frac{\partial N_{it}}{\partial t} = -D \frac{\partial C_X}{\partial z} \quad (1.3.2-3)$$

Where D is the diffusion constant of X and $\partial C_X / \partial z$ is the concentration gradient of X in the oxide at a distance of z from the interface. The diffusion front of the species X moves as $\sqrt{Dt}$, and the diffusion flux is given by [60]:

$$D \frac{\partial C_X}{\partial z} = D \frac{C_X^{(0)}}{\sqrt{Dt}} \quad (1.3.2-4)$$

Where $C_X^{(0)}$ is the concentration of X at the SiO_2 -Si interface. From Eq. 1.3.2-3 and Eq. 1.3.2-4, $C_X^{(0)}$ may be solved as:

$$C_X^{(0)} = \sqrt{\frac{t}{D}} \frac{\partial N_{it}}{\partial t} \quad (1.3.2-5)$$

Assuming the net trap generation is slow and negligible compared to the large diffusion and back-diffusion fluxes, from Eq. 1.2.1-2, $A(N_D - N_{it}) = BN_{it}C_X^{(0)}$. Solving this equation together with Eq. 1.3.2-5, with the assumption that the reaction in Phase A is far from saturation, i.e., $N_{it} \ll N_D$, the density of interface trapped charge is given as follows:

$$N_{it} \sim \sqrt{\frac{AN_D}{B}} (Dt)^{1/4} \quad (1.3.2-6)$$

Therefore, the observed $t^{1/4}$ behavior of N_{it} indicates the generation of interface trapped charge is diffusion controlled. A specific chemical reaction based on R-D model is provided by Jeppson and Svensson as well to describe NBTI-induced charge generation [20]:

As shown in Fig. 1.6, when the trap precursor (Si-H) is dissociated, the hydrogen

weakly bonded to the Si atom is released and reacts with SiO_2 , and forms Si-OH group, leaving a trivalent $\equiv\text{Si}\cdot$ (N_{it}) at the Si/SiO₂ interface and a positive charged $\equiv\text{Si}^+$ in the oxide. When hydrogen species (i.e., $\equiv\text{Si-OH}$) diffuse away from the interface, reaction moves towards the right side and more interface trapped charge is generated.

Fig. 1.6 Schematic two-dimensional representation of the Si-SiO₂ interface, showing (a) the $\equiv\text{Si-H}$ trap precursor, (b) the trap precursor may be electrically activated during negative bias stress to form an interface trapped charge (N_{it}). Released hydrogen species reacts with SiO_2 and forms an oxide trapped charge (N_{ot}), and a hydroxyl group, and (c) the hydroxyl may diffuse in the oxide. [Data after Ref. [20]]

Although not proved to be the very mechanism behind NBTI yet, this reaction well explained the equal generation of N_{it} and N_{ot} , and the $t^{0.25}$ time dependence. Most of later NBTI theories were improved versions of this hypothesis. However, a latent assumption in this model is that N_{ot} and N_{it} are of the same origin, and the relaxation rate of N_{ot} is also equal to that of N_{it} , which might not be the case.

1.3.2-2. Refined R-D model by Ogawa *et al.*

In the conventional R-D model proposed by Jeppson and Svensson [20], to simply the boundary conditions, the oxide thickness of the MOSFET examined was assumed to be infinite, so that the effect of gate electrode/SiO₂ interface on hydrogen diffusion could be ignored. However, this assumption is no longer applicable for the ultra-thin gate oxide transistors in modern technology. In 1995, Ogawa *et al.* refined the R-D model by taking the effect of a finite oxide thickness into account [21]. Assuming the gate electrode as an “absorbing” wall for the diffusing species, i.e. the concentration of X_{Si} is zero, at the gate/oxide interface, a quantitative description was given for the generation of interface traps [21, 22]:

$$\Delta N_{it}(t) = (D_0)^{1/4} R' t^{1/4} \exp(-E_a^D / 4kT) / t_{ox} \quad (1.3.2-8)$$

where D_0 is diffusion coefficient factor, R' is a constant dependent on the ratio of generation rate to the recovery rate of the reaction. E_a^D is activation energy of the diffusion process, and t_{ox} is thickness of oxide. This quantitative description derived from mathematical calculation and physical simulation is consistent with the experimental results [21], in terms of time dependence, temperature dependence, and the influence from oxide thickness. But the dependence on electric field is not included in Eq. 1.3.2-8. A more complete equation is expressed by [21]

$$\Delta N_{it}(E_{ox}, t_{ox}, T, t) = B E_{ox}^{3/2} t^{1/4} \exp(-E_a^{exp} / kT) / t_{ox} \quad (1.3.2-9)$$

where B is an independent constant and E_a^{exp} is experimental activation energy value. Combined with Equation (1.3.2-8), the value of E_a^{exp} should be a quarter of E_a^D . The electric field dependence was attributed to the nature of the electrochemical reaction

shown in Equations (1.3.2-1a) and (1.3.2-1b). The inverse proportionality of ΔN_{it} on the oxide thickness highlights the impact of gate oxide scaling on NBTI. It shows that with the scaling down of MOSFETs, more interface traps will be generated during operation, and NBTI degradation will become more severe in ultra-thin gate oxide transistors. As for possible diffusion species, atomic hydrogen (H^0) [23, 24], molecular hydrogen (H_2) [22, 25-28], proton (H^+) [29-32], and hydronium (H_3O^+) [33, 34] have been proposed to be possible candidates. In Jeppson and Svensson model, hydroxyl (OH group) was believed to be the diffusion species [20]. All the proposed choices were supported by individual experimental results, analysis and derivation. In Ogawa's model, after ruling out other possibilities, molecular hydrogen (H_2) was proposed to be the diffusion species limiting the NBTI reaction rate [21, 22].

Although the details of the trap generation process are still not clear and the actual diffusion species have not been identified till today, the diffusion-controlled chemical reaction model well explains the time and temperature dependence, as well as the oxide thickness dependence of NBTI degradation.

1.3.3. Revival of NBTI Investigation

Before 1999, research on NBTI of *p*-type MOSFET was sporadic and was mainly a subject of academia. It was not paid much attention in industry, as there was a more severe instability problem due to HCI. To achieve high current drive and low power operation, the gate oxide thickness has been reduced aggressively, from 95 nm in the

1970's to the current 2 nm or thinner. But to maintain circuit operation margin, the supply voltage could not be scaled down proportionally. Thus the oxide electric field is increasing along with the scaling down of MOSFETs, leading to severer NBTI-induced degradation on p-MOSFET. On the other hand, as MOS devices are scaled down, a surface channel p-type MOSFET replaces the buried-channel device to alleviate the short channel effect (SCE) [35]. Boron used for p^+ -gate doping during the fabrication of surface PMOS devices could diffuse and penetrate through the gate oxide into the channel. The penetrated boron may shift flat-band voltage and generate defects in the gate oxide. Therefore, nitrogen was introduced into the gate oxide to reduce boron penetration and reduce leakage current.

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Fig. 1.7 The transition of lifetime limitation mechanisms as a function of gate oxide thickness. When the thickness of the gate oxide is reduced to be less than 3.5 nm (after 1999), degradation due to NBTI begins to limit the device lifetime.

In 1999, Kimizuka et al. [14] reported severer degradation of ultra-thin oxynitride gate p-MOSFETs subjected to NBT stress. The authors further showed that with further scaling of the gate oxide, the lifetime due to NBTI would become shorter than

that due to HCI (Fig. 1.7). This report attracted a lot of attention on NBTI in the following years.

Although severer NBTI-induced degradation was observed on ultra-thin oxynitride gate p-MOSFETs, R-D model was reported by some researchers to be still valid on new generation devices [32, 36, 59]. In addition to the power-law time dependence of NBTI-induced threshold voltage shift ΔV_{th} under static negative gate bias, the recovery of ΔV_{th} after the gate stress is removed is also observed experimentally.

Fig. 1.8 Time evolution of threshold voltage shift of a PMOS during NBTI stress. The degradation rate is small initially but breaks off and increases at longer time. The break time and post-break slope are insensitive to oxide field (gate voltage), suggesting the long-time enhancement is not a bulk-trap activated process. Such enhancement is anticipated by the R–D model. Absence of field acceleration of the breakpoint suggests neutral diffusion species. [Data after Ref. [36]]

Fig. 1.8 illustrates the power-law time dependence of measured threshold voltage shift on ultra-thin gate dielectric p-MOSFET during NBT stress. Fig. 1.9 plots ΔV_{th}

under negative gate bias (stress period) and without gate stress (relaxation period). Measured data could be well fit by the simulation results based on R-D model. Part of NBTI-induced ΔV_{th} is recovered after the gate stress is removed.

Fig. 1.9 The R-D model is solved numerically for two cycles of interrupted stress (stress 1000 s, relaxation 1000 s). The simulation results (continuous line) agree well with measured data (symbols). Each 1000 s segment is characterized by a fast phase (first few seconds) followed by a slower phase of interface-trap generation, which relate to reaction-limited and diffusion-limited regimes, respectively. [Data after Ref. [36]]

1.3.4. Recent Progresses in NBTI Study

1.3.4-1. Nitrogen Effect on Trap Generation

As mentioned in the last section, the revival of NBTI study accompanies the introduction of nitrogen into the gate dielectrics of p-MOSFET to inhibit boron

penetration. Since then, lots of experiments and simulations were carried out to investigate how nitrogen behaves in the NBTI problems.

Fig. 1.10 Temperature dependence of ΔV_{th} for pMOSFETs having SiON and SiO₂ film. The oxide thickness is 2.3 nm. It is found that NBTI degradation of SiON is more remarkable than that of SiO₂, and the activation energy of ΔV_{th} for SiON ($E_a \sim 0.1$ eV) is lower than that for SiO₂ ($E_a \sim 0.2$ eV). [Data after Ref. [37]]

Mitani *et al.* [37] compared the NBTI-induced degradation of p-MOSFET with SiO₂ gate and oxynitride gate. They found the activation energy of ΔV_{th} is smaller for SiON gate PMOS than SiO₂ gate PMOS, as shown in Fig. 1.10. As very small leakage current is monitored, the interface traps and positive fixed charge were reported to be generated by “cold” holes. According to the explanation given by Mitani *et al.*, Si-H bond breaking dominates the NBTI degradation of SiO₂ gate devices, as shown in Fig. 1.11(a). On the other hand, after absorbing electrons from Si dangling bond, twofold coordinated nitrogen are formed at the SiO₂-Si interface of SiON gate devices. When holes are trapped here, interface traps and positive charges are formed, as shown in Fig. 1.11(b).

Fig. 1.11 Schematic diagram for mechanism of NBT degradation. It is inferred that two kinds of origins contribute to NBT degradation. One is the hydrogen-related process such as Si-H bond-breaking (a). The other is hydrogen-unrelated structure such as twofold coordinated N contributes to NBT degradation (b). [Data after Ref. [37]]

Fig. 1.12 Activation energy of both the interface trapped charge and oxide trapped charge (so called fixed charge trapping in the picture) for devices with nitrogen concentration ranging in 0~8 at.%. [Data after Ref. [38]]

Tan *et al.* studied the generation of interface traps and oxide trapped charge in p-MOSFETs with different nitrogen concentrations in the gate oxide, and formulated a quantitative relationship between nitrogen concentration and activation energy [38].

As shown in Fig. 1.12, the more nitrogen in the gate dielectric, the smaller the activation energy becomes. Tan *et al.* interpreted the influence of nitrogen based on the R-D model. Eqs. 1.3.4-1, 1.3.4-2, and 1.3.4-3 are the electrochemical reactions proposed to describe the generation of interface traps and oxide trapped charge [38]. The incorporation of nitrogen enhances the trapping of the dissociated hydrogen species at the SiON-Si interface. Furthermore, the nitrogen at the SiON-Si interface acts as a diffusion barrier against the diffusion of hydrogen species from SiON bulk to the interface. These effects reduce the concentration of hydrogen species at the SiON-Si interface, thus increase the reaction rates of the forward direction reactions expressed by Eqs. 1.3.4-1 and 1.3.4-2. Therefore, the generation of interface traps and oxide trapped charge is enhanced.

Besides the impact on activation energy, nitrogen was reported to increase the density of trap precursors Si-H at the SiO₂-Si interface. Such an increase of trap precursor density was attributed to more significant interfacial strain due to the presence of nitrogen [39]. On the other hand, a larger threshold voltage shift was observed for nitrated oxide devices as compared to pure oxide devices, with the same amount of interface traps. This observation led to the conclusion that nitrogen-related hole traps were generated near the interface [37, 40]. Calculation of reaction energy E_R of hole trapping and subsequent hydrogen dissociation reactions indicates that

nitrogen-related centers have a lower reaction energy than oxygen-related centers [41]. Hence, a nitrided oxide has more hole trapping sites than a pure oxide. Tan *et al.* also reported that E_R of hydrogen ion trapping reaction with nitrogen-related centers is lower than the reaction involving oxygen-related centers [42].

In addition to the quantity, the profile of nitrogen in the oxide also influences the degradation of the p-MOSFET. Tan *et al.* [43] compared the degradation of decoupled plasma-nitrided oxide (DPNO) and rapid thermal nitrided oxide (RTNO); These two types of gate dielectrics have a comparable peak nitrogen concentration of 3 at.% but with different nitrogen profiles. DPNO device has a peak nitrogen concentration near the gate-SiO₂ interface; while RTNO device has a peak nitrogen concentration near the SiO₂-Si interface. It was found that DPNO devices exhibited a higher activation energy and generated less surface charges, compared to RTNO devices. The effect of nitrogen profile on NBTI was also observed by Sasaki *et al.* [44]. In their experiments, NO-First annealing process is compared to NO-Last annealing process. An NO-first annealing process results in a nitrogen concentration peak near the gate electrode, while an NO-last annealing process produces a nitrogen concentration peak near the oxide-substrate interface. The NO-first process exhibited more resistance to NBTI as well as better suppression of gate leakage current and boron penetration. Therefore, it was suggested that the process should be optimized to keep the nitrogen away from the SiO₂-Si interface. Increased NBTI degradation of nitrided oxide devices was repeatedly observed, however, the exact mechanism is yet

to be clarified.

1.3.4-2. Deviation from R-D model

According to the R-D model established on the conventional SiO₂ gate p-MOSFET, Si-H bonds are broken, forming silicon dangling bonds and hydrogen species: [21]

where Y is the reactant, widely believed to be hole. X is resultant hydrogen species, which could be H⁰ atoms, or H⁺, H₂, etc. NBTI-induced threshold voltage shift ΔV_{th} can be expressed as follows:

$$|\Delta V_{th}|(T, t) = A \exp(-E_a / kT) t^n \quad (1.3.4-5)$$

where A is a constant depending on the trap precursor density, electric field, etc. The value of E_a and n are determined by the exact chemical and physical reactions leading to NBTI degradation. The nature of hydrogen species is significant in controlling the value of n and E_a , and the prediction of device lifetime. From simulation results based on R-D model, charged species like H⁺ should produce $\Delta V_{th} \sim t^{0.5}$ time dependence [22]. Thus X is believed to be neutral hydrogen species as $t^{0.25}$ is more often observed. Chakravarthi *et al.* [45] conducted simulation on various chemical reactions and summarized the power-law exponent values in Table I.

However, deviation of electrical characteristics of NBTI-induced degradation of state-of-the-art ultra-thin oxynitride gate p-MOSFETs are observed to deviate from

those reported in the past for the conventional pure SiO₂ gate p-MOSFETs. For instance, the power-law exponent n , varies over a range of 0.08~0.3 [46-50], depending on test device and measurement method. Such dispersion in the power-law exponent challenges the classical R-D model. New NBTI models were proposed to fit ultra-thin oxynitride gate p-MOSFETs.

Table I. Effect of different species on fractional time dependence of NBTI evolution for a diffusion limited system. [45]

Model	Reaction	Mobile Species	Slope
I	$\text{SiH} + \text{h}^+ \rightleftharpoons \text{Si}^+ + \text{H}^0$	H^0	0.25
II	$\text{SiH} + \text{h}^+ \rightleftharpoons \text{Si}^+ + 0.5\text{H}_2^0$	H_2	0.165
III	Models I and II	H^0, H_2	0.165–0.25
IV	$\text{SiH} + 2\text{h}^+ \rightleftharpoons \text{Si}^+ + \text{H}^+$	H^+	0.25–0.5
V	Models I, II and III	$\text{H}^0, \text{H}^+, \text{H}_2$	0.165–0.5
VI	Model I and trapping of H	H^0	> 0.25
VII	Model I and release of H	H^0	< 0.25
VIII	Model II and trapping of H ₂	H_2^0	> 0.165
IX	Model II and release of H ₂	H_2^0	< 0.165

Fig. 1.13 NBTI exponent b as a function of temperature T . [Data after Ref. [49]]

In addition to the observation that test device and measurement method affect the power-law exponent value, temperature is also reported to play a role. Non-Arrhenius

behavior of the exponent, i.e., n increases with temperature, was observed by Alam *et al.* [36], Kaczer *et al.* [49] and Huard *et al.* [51].

Conventional R-D model contains two phases: Reaction and diffusion phase. The reaction phase in the conventional R-D model was retained in this dispersive transport model. But the distinction in the dispersive transport model is that the transportation behavior of particles in disordered structures, such as amorphous SiO₂, is not Gaussian, but dispersive [52]. Thus, the effect on the transport process from the energy distribution of hydrogen traps is considered in this model. With the presumptions that the energy distribution of hydrogen traps is larger than kT , k is Boltzmann's constant, T is temperature; and hydrogen traps with deep energy states are not fully filled, NBTI degradation due to dispersive transport of hydrogen is expressed as follows [49]:

$$|\Delta V_{th}| = At^b, \text{ where } b = \frac{kT}{4E_0} \quad (1.3.4-6)$$

Similar to the conventional R-D model, the dispersive transport model predicts a power-law time dependence for $|\Delta V_{th}|$. But the exponent b contains factors such as temperature T and the density of states of hydrogen E_0 . Therefore, the exponent should increase, as temperature increases. It could also change from device to device, due to the difference in the energy distribution of hydrogen traps. This dispersive transport model well explains the controversy in the value of the power-law exponent.

1.3.4-3. Recovery behavior of NBTI-induced degradation

P-MOSFETs operating under negative gate voltage at high temperature tend to degrade with stress time due to the accumulation of interface traps and oxide trapped positive charge. However, p-MOSFETs in circuit operation do not always work under a static gate biasing condition. During the operation of a p-MOSFET in a CMOS inverter, the applied gate voltage is switching between “high” and “low” voltages, while the drain voltage is alternating between “low” and “high” voltages correspondingly. Similar dynamic modes are also observed when *p*-type MOSFETs function as part of DRAM, SRAM, sense amplifier, etc. Therefore, the performance of p-MOSFETs under dynamic stress received a lot of attention in recent years. Fig. 1.14 illustrates the recovery of threshold voltage shift and interface traps after changing the gate bias from negative to positive. A significant portion of $|\Delta V_{th}|$ is relaxed under a positive gate bias. Almost complete recovery of NBTI degradation at low temperature was observed by Rangan *et al.* [53].

Fig. 1.14 Relative shift for (a) $|\Delta V_{th}|$ and (b) ΔN_{it} versus stress time under a negative and positive gate voltage [51, 54].

Compared to the significant recovery of $|\Delta V_{th}|$, negligible recovery of interface traps was observed. Thus, recovery of oxide trapped charge was believed to play a more important role than interface traps. From the experiment conducted by Denias *et al.*, only oxide trapped charge decreases during recovery, while interface trap density has no significant change [55]. A slight decrease of N_{it} is also reported by Lee *et al.* [56]. Lin *et al.* also indicate that the re-passivation of interface traps has small contribution to the recovery of threshold voltage shift, while the de-trapping of trapped holes during the relaxation period is the main reason of the recovery [57]. Huard *et al.* [51] also concluded that the recovery of threshold voltage shift is primarily due to detrapping of holes captured by the nitrogen-related centers in the oxide, but not due to the re-passivation of interface traps.

Fig. 1.15 (a) N_{it} generation: Si-H bond breaking at the interface and hydrogen diffusion towards the gate electrode during negative gate bias stressing. (b) N_{it} passivation: hydrogen moves back to the interface and passivates the Si dangling bonds during positive gate bias. X stands for hydrogen species. [Data after Ref. [59]]

Similar to the controversy in NBTI mechanism under static stress, contradicting observations and theories were reported for the recovery of NBTI degradation. Chen

et al. observed the recovery behavior of NBTI-induced degradation on p-MOSFET [59]. They interpreted the recovery process as a diffusion-controlled mechanism based on an observed $t^{0.25}$ time dependence. Under a negative gate bias stress, the holes from the induced inversion layer react with Si-H bonds, and form interface traps (Si dangling bonds). The resultant hydrogen species, denoted as X in Fig. 1.15, diffuse/drift to the gate electrode. When the bias is reversed to positive, as shown in Fig. 1.15 (b), the channel inversion layer disappears. X moves back to the Si-SiO₂ interface under the influence of positive gate voltage, and passivates the Si dangling bonds, resulting in N_{it} recovery [59].

In this model, the contribution of oxide trapped charge to the threshold voltage shift was assumed to be negligible, due to the ease of detrapping by tunneling electrons. Therefore, the recovery of threshold voltage shift was mainly attributed to the re-passivation of interface traps. This model was supported by the numerical solution to the R-D model by Alam [60] and the experimental results of Tsujikawa *et al.* [61]. Rangan *et al* [53] used charge pumping measurement to monitor the generation of interface traps and monitored drain current in the linear region I_{dlin} to evaluate NBTI degradation. The similarity in the behavior of I_{cp} and I_{dlin} recovery leads to the conclusion that only the passivation or annihilation of interface traps is responsible for recovery, and the diffusion species was believed to be neutral hydrogen [53].

1.3.4-4 Discussions on NBTI Characterization Method

I. Challenges to Conventional DC Characterization Method

Conventional NBTI characterization method applies a stress on the gate, and interrupts the stress to measure the drain current, threshold voltage, interface trap density, or other parameters. During the measurement, normally a full I_d - V_g sweep is carried out. Threshold voltage V_{th} is later extracted from the I_d - V_g characteristics, using either maximum g_m method or constant-drain-current method [62]. In some applications, charge pumping current measurement [62] or DCIV measurement [63] is also carried out to monitor the generation of interface traps. I_d - V_d characteristics were measured to monitor the degradation of carrier mobility μ . NBTI stressing is resumed after the measurements.

Fig. 1.16 As measurement time t_m increases, threshold voltage shift ΔV_{th} is underestimated, and the power-law exponent is increased. [Data after Ref. [50]]

But the delay caused by the measurements between neighboring NBTI stressing periods was reported to result in fast recovery of NBTI-induced degradation, leading

to underestimation of the degradation rate [50-51, 64]. As shown in Fig. 1.16, threshold voltage shift ΔV_{th} was observed to be underestimated with long measurement time. The power-law exponent of ΔV_{th} increases while the measurement delay increases. Therefore, the accuracy of the conventional DC characterization method was challenged, as it takes 1~30s to finish the measurements.

II. Review on Fast Characterization Methods

To reduce the post-stress recovery of NBTI-induced degradation, time-critical measurement methods with shorter delay were developed. Denais *et al.* [65] proposed on-the-fly characterization (OTF) method. This methodology characterizes NBTI degradation almost without inherent recovery since the gate bias remains close to stress voltage during the measurement.

Fig. 1.17 Schematic of the on-the-fly measurement methodology. Linear drain current shifts as well as the associated transconductance g_m variations can be monitored. [Data after Ref. [51]]

As shown in Fig. 1.17, characterization of degradation is carried out by superimposing small gate bias pulses on the gate stress voltage. Meanwhile the evolution of the currents is monitored. Using the OTF technique, linear drain current I_{dlin} , threshold voltage shift $|\Delta V_{\text{th}}|$ and transconductance g_m can be obtained. Although theoretically no inherent recovery of NBTI-induced degradation happens during the measurement, the OTF method has drawback in the extraction of threshold voltage, which will be addressed in the next chapter.

In another fast switching method [66], the gate bias is lowered briefly from the stress voltage to a measurement voltage which is near V_{th} . The drain current is measured simultaneously. Threshold voltage shift can be calculated from the change in the drain current before and during measurement. Compared to the OTF method, the advantage of the fast switching method is that the mobility degradation is taken into account as well. But as the gate bias is lowered to near V_{th} during measurements, recovery is inevitable although the measurement time is shorter ($\sim 0.2\text{s}$) than the conventional DC method. Advantages and drawbacks of the fast switching method will be addressed in details in the next chapter.

Krishnan *et al.* [46] compared the interface trap density N_{it} measured by the conventional DC method ($\sim 1\text{s}$ delay) and N_{it} measured by the OTF method (no delay). As shown in Fig. 1.18, compared to the conventional method with longer measurement delay, the OTF technique monitors more interface traps generated

during NBTI stressing. In addition, the power-law exponent is also increased to 0.19 if the measurement delay is shortened to zero.

Fig. 1.18 Interface trap density N_{it} vs. stress time measured with ~ 1 s delay ($\circ$) and without any delay ($\bullet$), showing that the delay between stress and measurement results in a large increase in slope. [Data after Ref. [46]]

Mahapatra *et al.* [67] utilized the OTF I_{dlin} measurement method to characterize NBTI-induced threshold voltage shift $|\Delta V_{th}|$ on plasma nitrided gate oxide p-MOSFET. The power-law exponent n of $|\Delta V_{th}|$ is observed to be ~ 0.14 . The simulation results based on the R-D model indicates $n \sim 1/6$ for molecular H_2 diffusion process; and $n \sim 1/4$ for atomic H_0 diffusion process [45]. Thus the observed $n \sim 0.14$ using the OTF method is believed to result from the diffusion of H_2 away from SiO_2 -Si interface. This conclusion challenges the long-term belief that it is H_0 diffusion that controls the R-D model and leads to NBTI degradation. However, $n \sim 1/6$ is not the extreme exponent value obtained by fast measurement technique. Smaller power-law exponent $n < 0.1$ is observed by Shen *et al.* [50] and Reisinger *et al.* [64], which could not be reconciled by the R-D model.

1.4 Motivation of This Thesis

The previous sections provided an overview of reliability issues concerning aggressively scaled MOSFETs, and recent developments in the study of NBTI-induced degradation in *p*-type MOSFETs. Research on NBTI-induced degradation of p-MOSFETs mainly focused on three main aspects: (1) The physical origins that lead to the increased NBTI-induced degradation of ultra-thin oxynitride gate p-MOSFETs; (2) The interpretation of the power-law exponent n extracted from the time evolutions of threshold voltage shift and NBTI-generated interface traps; (3) The recovery mechanism of NBTI-induced degradation of p-MOSFET when the negative gate stress is removed or replaced by a positive gate stress.

Compared to the conventional p-MOSFETs having pure SiO₂ gate dielectric, NBTI-induced degradation was observed to be increased significantly in ultra-thin oxynitride gate p-MOSFETs [14]. The activation energy of NBTI-induced threshold voltage shift E_a was also reduced for oxynitride gate devices [37, 38]. Both the density and the profile of nitrogen inside the gate oxide were reported to affect the degradation conditions [38, 43]. On the other hand, reaction energy E_R was utilized as a parameter to study the different degradation behaviors between conventional SiO₂ gate p-MOSFETs and oxynitride gate devices. Smaller E_R was obtained for the reaction of hole trapping in nitrogen-related centers and subsequent hydrogen dissociation reaction [41, 42], indicating nitrogen-related interface traps are more stable than oxygen-related ones. However, no direct evidence is available to link the

severer degradation and smaller activation energy of oxynitride gate p-MOSFET with specific reactions. How nitrogen behaves to enhance the generation of interface traps and oxide trapped charge remains unclarified. Therefore, it is essential to further investigate the physical mechanisms behind the increased NBTI-induced degradation of p-MOSFET having ultra-thin oxynitride gate and the impact of nitrogen on the mechanisms.

Time evolution of NBTI-induced threshold voltage shift or interface trap density is another research focus, as accurate extrapolation of the lifetime of p-MOSFET is critical to qualify CMOS circuits. Power-law time dependence of NBTI-induced degradation was observed on both conventional SiO₂ gate p-MOSFETs and oxynitride gate p-MOSFETs. But recently the power-law exponent n was observed to vary depending on test device, stress temperature and measurement methods. The classical R-D model fails to offer a complete explanation for the variety of the power-law exponent. Moreover, the presumption of the R-D model is the diffusion of neutral hydrogen species. But the observation of polarity dependent $|\Delta V_{th}|$ recovery cannot be explained by the reverse-direction diffusion of neutral species. This motivated a growing effort to examine the factors that influence the time-evolution of NBTI-induced degradation. Physical mechanisms that lead to the variety of the power-law exponent n will be addressed in this thesis.

Post-stress recovery of NBTI-induced degradation became more and more significant

as it must be taken into account to obtain accurate anticipation of the lifetime of p-MOSFETs, especially when p-MOSFET operates at dynamic modes. It also inspired great challenge to conventional DC characterization method with long measurement delay. Hole detrapping and reverse R-D model were proposed separately to explain the recovery process of NBTI-generated interface traps [51, 60]. Such controversy requires further study of the degradation behavior of p-MOSFET during dynamic gate stress, and the physical mechanisms that cause the recovery of NBTI-induced degradation.

1.5 Organization and Original Contributions of the Thesis

The work described in this thesis will focus on several aspects of NBTI-induced degradation in ultra-thin oxynitride gate p-MOSFETs, including the temperature dependence, time evolution, and impact of nitrogen on NBTI-induced degradation, etc. The objective is to gain a fundamental understanding of the NBTI-induced degradation mechanisms as well as the recovery mechanisms when the p-MOSFET operates at dynamic modes.

This thesis is organized into seven chapters. Chapter two elucidates the NBTI stress conditions and characterization methods used in this work. Detailed bias conditions applied on the terminals of p-MOSFETs are presented. Potential errors in the characterization methods will be analyzed and corrected correspondingly. Chapter three presents a study of NBTI-induced threshold voltage shift and examined the role

of interface traps during NBT stressing. In addition to interface traps, deep-level positive trapped charge is observed to be generated as well. Moreover, the deep-level positive charge plays a significant role in the degradation of p-MOSFETs due to the strategic energy states beyond the conduction band of Si substrate. Chapter four studies the temperature dependence of NBTI-induced degradation, in terms of threshold voltage shift $|\Delta V_{th}|$ and interface trap density N_{it} . It is found that two distinct mechanisms are responsible for the NBTI-induced degradation of ultra-thin oxynitride gate p-MOSFETs. A temperature-insensitive mechanism is superposing on the temperature-sensitive mechanism which is also observed in conventional SiO_2 gate devices. Furthermore, nitrogen in the gate oxide enhances the temperature-insensitive mechanism, indicating the temperature-insensitive mechanism is related to the incorporated nitrogen in the gate oxide. The time dependence of the two NBTI mechanisms controlling NBTI degradation of oxynitride gate p-MOSFET is investigated in chapter five. The temperature-insensitive mechanism shows a weaker time dependence than the temperature-sensitive mechanism. Based on the thermal characteristics and the time-evolution behavior, the novel temperature-insensitive mechanism is linked to nitrogen-related hole trapping mechanism. Frequency dependence of NBTI-induced threshold voltage shift of the p-MOSFET subjected to unipolar ac stress is studied in Chapter six. The impacts of nitrogen concentration and profile on the frequency dependence are investigated. Weaker frequency dependence is observed for the threshold voltage shift of the p-MOSFET with more nitrogen in the gate oxide, regardless of the nitrogen profile, indicating more deep-level hole trapping

occurs in the p-MOSFET of larger oxide nitrogen concentration. The generation and recovery behaviors of NBTI-induced charges during unipolar stressing are analyzed as well. The last chapter concludes the thesis and provides some recommendations for future study.

Chapter 2 Methodology

Through out this work, DC I_d - V_g characterization method was employed to measure the threshold voltage of fresh p-MOSFET and after certain period of NBTI stressing. Charge pumping (CP) current measurement was carried out after DC I_d - V_g measurement to measure interface trap density. After finishing the measurements, NBTI stress is resumed until the next time of measurement. The equivalent oxide thickness and stress electrical field was extracted using the C-V simulator from North Carolina State University, to ensure that stress electrical field is low enough to avoid large amount of hot-hole injection into the gate oxide, and the monitored degradation is mainly due to NBTI stress [74]. Fig. 2.1 illustrates the gate bias during NBTI stressing and measurement.

Fig. 2.1 Schematic diagram showing the gate bias during NBTI stressing and periodic drain current vs. gate voltage sweep (I_d - V_g) and charge pumping current measurement.

2.1 Charge Pumping Current Method

2.1.1. Introduction of Charge Pumping Current Method

CP current measurement is carried out to monitor the amount of stress-induced interface traps. Fig. 2.2 illustrates the basic experimental setup for CP current measurement. A 1MHz voltage pulse with a rise/fall time gradient of 20ns/V is applied on the gate, while the source and drain terminals are grounded. CP current is measured at the substrate. When the gate voltage is negative, the p-MOSFET is biased in inversion condition, as shown in Fig. 2.3 (a). All the interface traps are occupied by holes from the channel. But when the gate voltage is switched to positive, the transistor is now biased in the accumulation regime, as shown in Fig. 2.3 (d). Electrons occupy all the interface traps. Although the transition time between inversion and accumulation is very short, important processes take place during this short period.

Fig. 2.2 Basic experimental setup for charge pumping measurements.

When the gate voltage switches from a negative to a positive value, holes at the surface of the channel drift to the source and drain. In addition, holes captured by the interface traps near the valence band are thermally emitted into the valence band, and also drift to the source and drain, as shown in Fig. 2.3 (b). But those holes trapped in deeper states do not have sufficient time to be emitted and remain captured in the traps. When the electron barrier is further reduced as gate voltage increases, electrons flow to the surface where some are captured by the interface traps and recombined with the trapped holes, as shown in Fig. 2.3 (c).

Such recombination also occurs when the gate voltage is switched from positive to negative: holes drifting from the source and drain are captured at the substrate surface, and recombine with electrons not able to return to the substrate but trapped in the interface traps. As a consequence, the amount of electrons returning to the substrate is always smaller than those flowing into the surface channel, resulting in a DC charge pumping current which can be measured at the substrate.

The change of charge pumping current is directly proportional to the density of generated interface trap (ΔN_{it}), transistor gate area (A_G), and frequency of the gate pulse (f_{cp}) [68]:

$$\Delta I_{cp} = q A_G f_{cp} \Delta N_{it} \quad (2.1-1)$$

Fig. 2.3 Energy band diagrams for different stress cycles during charge pumping measurements. Filled circles stand for electrons, and open circles stand for holes. The short horizontal lines show interface traps distributed along the interface. [Data after Ref. [62]]

2.1.2. Correction of Leakage Current

CP current method was proposed to be an effective characterization technique to monitor interface trap density at the SiO₂-Si interface of MOSFETs [68]. But with the shrinking of device dimensions, the gate oxide thickness becomes thinner and thinner. The p-MOSFETs tested in this work has ultra-thin gate dielectric (≤ 2 nm), significant

direct tunneling takes place through the gate oxide. As discussed in last section, CP technique measures the DC current I_{it} due to recombination of holes and electrons at the interface traps when the gate bias switches between inversion and accumulation. If tunneling occurs during the CP current measurement, in addition to the interface trap component I_{it} , the measured current I_{cp} consists of a parasitic leakage current I_{lk} due to the direct tunneling through the gate oxide. The existence of direct tunneling gate leakage causes important errors in the measurements of the interface traps, if the leakage current I_{lk} is of comparable order as I_{it} . Thus correction of errors due to direct tunneling gate leakage is essential to ensure the accuracy of the CP technique.

As reported by Masson *et al.* [69], CP current measured at low frequency (~ 1 kHz) is comparable to calculated gate leakage current, i.e., I_{it} is reduced to a negligible value at low frequency. Thus substrate current measured by CP technique at low frequency is considered as the leakage current. Therefore, the influence of gate leakage current on the measured CP current measurements was compensated by subtracting measured substrate current at low frequency (10 kHz) from I_{cp} measured at high frequency (1 MHz). Fig. 2.4 illustrates how the charge pumping measurement result was used to determine interface trap density in this thesis. Source and drain terminals of p-type MOSFET were grounded, and AC pulse was applied on the gate, substrate current was measured as I_{cp} , as shown in Fig. 2.2. Constant gate top CP technique was used in this thesis, i.e. the top voltage of the AC pulse applied on the gate is at 1V; while the base voltage of the AC pulse is reduced from 0.7V to -1V during CP measurement [103,

104]. I_{cp} measured when 1MHz AC pulse was applied on the gate is I_{it} . And I_{cp} measured when 10kHz AC pulse was applied on the gate is I_{lk} . The net CP current ($I_{it} - I_{lk}$) corresponds to the interface trap density measured at a frequency of 1 MHz in Eqn. 2.1-1 without the influence of gate leakage current. Eq. 2.1-1 is written as Eq. 2.1.2-1:

$$\Delta(I_{it} - I_{lk}) = qA_G f_{cp} \Delta N_{it} \quad (2.1.2-1)$$

Fig. 2.4 Schematic diagram showing the corrected charge pumping current obtained by subtracting the gate leakage current (triangles) from the measured charge pumping current (open squares). Gate leakage current is measured at 10 kHz. Charge pumping current is measured at 1 MHz. Resultant net charge pumping current (solid squares) is due to interface traps. Constant gate top method is used in the CP technique. The top voltage of gate bias is fixed at 1V; while the bottom voltage is changing from 0.7V to -1V.

As shown in Fig. 2.4, I_{cp} saturates when V_{gb} is lower than -0.5. Thus I_{it} and I_{lk} at $V_{gb} = -0.9V$ were extracted to calculate ΔN_{it} . Take a p-type MOSFET with 20 μm channel width and 0.18 μm channel length as an example, $A_G = 3.6 \mu m^2$. Before NBTI stress, $I_{it}@ (V_{gb} = -0.9V)$ is -238.57 pA, $I_{lk}@ (V_{gb} = -0.9V)$ is -4.34 pA. After 70000s

stress, $I_{it}@ (V_{gB} = -0.9V)$ is -325.06 pA, $I_{lk}@ (V_{gB} = -0.9V)$ is -12.93 pA (CP results not shown in Fig. 2.4). Thus $\Delta(I_{it} - I_{lk})$ is -77.9 pA. f_{cp} is 1MHz and q is electron charge. Based on Eq. 2.1.2-1, $\Delta N_{it} = \Delta(I_{it} - I_{lk}) / (qA_G f_{cp}) = 1.3 \times 10^{10} \text{ cm}^{-2}$.

2.1.3. Limitations of Charge Pumping Current Method

CP current technique was utilized to monitor interface trap density and assist in data analysis in this work. Thus limitations of this method will be addressed in this section. One of the factors affecting the accuracy of the CP technique is temperature. The basic assumption of the CP technique is that carriers trapped in the interface traps do not have enough time to respond to the gate bias switching. Holes trapped at the interface cannot be emitted and thus recombine with electrons from the substrate when the gate bias is switched from negative to positive. Similar process happens when the gate bias is switched from positive to negative. The net loss of electrons results in a substrate current, which is measured by the CP technique. The emission process of trapped carriers is strongly dependent on the temperature [68]. At higher temperature, the holes and electrons are emitted more readily. Therefore, the CP current measured at higher temperature cannot monitor all the interface traps.

Another problem with the CP technique is that only a limited portion of the Si bandgap can be probed; i.e. only interface traps distributed within certain energy range ΔE_{cp} can be monitored by the CP current method. The effective energy range ΔE_{cp} is limited by thermal emission of electrons to (from) the conduction (valence)

band edge during gate pulse transition. In accordance to [68], ΔE_{cp} may be expressed as

$$\Delta E_{CP} = -2kT \ln \left[n_i \cdot v_{th} \cdot \sqrt{\sigma_n \sigma_p} \cdot \left(\frac{V_{FB}^{CP} - V_t^{CP}}{\Delta V_G} \right) \cdot t_{rf} \right] \quad (2.1.3-1)$$

where k is Boltzman constant, n_i is intrinsic carrier concentration, v_{th} ($\sim 10^7$ cm/s) is thermal velocity, V_{FB}^{CP} (~ 0.8 V) and V_t^{CP} (~ -0.2 V) are respectively the CP flat band and threshold voltages, ΔV_g ($= 2$ V) is amplitude of the gate pulse, t_{rf} ($= 40$ ns) is gate pulse transition time, σ_n (σ_p) is electron (hole) capture cross-section, and T is temperature in Kelvin. At $T = 373$ K (100°C), $n_i \sim 1.4 \times 10^{12} \text{ cm}^{-3}$. Assuming $\sqrt{\sigma_n \sigma_p} \sim 10^{-14} - 10^{-15} \text{ cm}^{-2}$ [70], ΔE_{CP} is estimated to range from 0.37–0.52 eV, which corresponds to 33–45% of the Si bandgap ($E_g = 1.12$ eV). It should be mentioned that precise determination of ΔE_{CP} is generally not possible, since σ_n and σ_p and their associated temperature dependence are unknown.

As CP current measurement was carried out after DC I_d - V_g measurement, Yang *et al.* [70] argued that passivation of interface traps occurs during subsequent CP measurement. Since the gate bias was switched between -1V and 1V during CP current measurement, the positive gate bias might lead to further recovery of NBTI degradation. In summary, influences from temperature, measurement sequence and the theoretical limitation of the CP technique lead to errors in the measurement of interface trap density. Despite the limitations of the CP method, it is still the most valid to monitor the generation of interface traps in small-dimension p-MOSFETs during NBTI stressing. Parallel comparison will be made in the next few chapters to

ensure the analysis not affected by the errors in the CP measurement.

2.2 Threshold Voltage Measurement

2.2.1. DC I_d - V_g Characterization Method

In this project, DC I_d - V_g measurement was used to monitor NBTI-induced threshold voltage shift. Before NBTI stressing and after certain period of NBTI stressing, I_d - V_g sweeping was carried out. During I_d - V_g sweeping, the drain bias is -0.1V, the gate bias V_g sweeps from 0V to -1.2V, meanwhile the drain current was measured. Identical I_d - V_g measurement setup is utilized in the following chapters, if not specified. Fig. 2.5(a) illustrates the I_d - V_g characteristics before and after NBTI stressing (I_d - V_g curve beyond -1V not shown).

Fig. 2.5 I_d vs. V_g characteristics of p-MOSFET before and after 70000s NBTI stress. Gate stress voltage is -2.6V during NBTI stressing, temperature is 398K. V_d is -0.1V during I_d - V_g measurement. (a) Constant drain-current method is used to extract threshold voltage. 26 mV shift in threshold voltage is shown by the arrows. (b) Maximum g_m method is used to extract threshold voltage. 24 mV shift is resulted.

Constant drain-current method was used in this project to obtain threshold voltage, i.e.

the gate voltage at a specified threshold drain current, I_{th} , is taken to be the threshold

voltage. In Fig. 2.5 (a), I_{th} is 20 μA , as the channel width/length of the p-MOSFET tested is 20/0.18 μm . In the subsequent chapters, I_{th} will be determined by the dimensions of p-MOSFETs. At $I_{th} = 20 \mu A$, a 26 mV threshold voltage shift is observed in Fig. 2.5 (a), shown by the arrows. As a comparison, extracting threshold voltage shift using maximum g_m method was shown in Fig 2.5 (b). 24 mV V_{th} shift is resulted, very close to the result obtained by constant drain current method.

The stress temperature used in Fig. 2.5 is 398K. As NBTI-induced degradation at various temperatures was studied in this work, the influence of temperature on initial threshold voltage V_{th0} is addressed here. Eqn. 2.2-1 shows the expression of threshold voltage V_{th} of p-MOSFET, without taking stress-induced interface traps or other charges into account.

$$V_{th} = V_{FB} - 2\phi_F - \frac{\sqrt{4q\epsilon_{Si}\epsilon_0\phi_F}}{C_{ox}} \quad (2.2-1)$$

$$\phi_F = \frac{kT}{q} \ln \left(\frac{N_A}{n_i} \right) \quad (2.2-2)$$

where V_{FB} is flat band voltage; ϕ_F is Fermi potential; ϵ_{Si} is the dielectric constant of Si; ϵ_0 is the permittivity of free space; C_{ox} is the oxide capacitance. The expression of ϕ_F is shown in Eqn. 2.2-2, where k is Boltzman's constant; N_A is acceptor doping density; n_i is intrinsic carrier density.

Therefore, as temperature increases, initial V_{th} on fresh p-MOSFET decreases, as shown in Fig. 2.6. Thus the calculation of threshold voltage shift must be based on

V_{th0} at the stress temperature.

Fig. 2.6 Initial threshold voltage V_{th0} on p-MOSFET as a function of temperature. Constant drain current method is used to extract V_{th0} .

2.2.2. Problems with Fast Switching Method

As discussed in section 1.3.4, fast characterization methods of V_{th} were developed to reduce post-stress recovery of $|\Delta V_{th}|$, such as fast switching method, etc. Thus $|\Delta V_{th}|$ on p-MOSFETs after NBTI stressing using different characterization methods were compared subsequently. Fig. 2.7 (a) compares $|\Delta V_{th}|$ obtained using the conventional DC I_d - V_g method (■) with that obtained using fast switching method (▲). During the conventional DC measurement, V_g sweeps from 0 to -1V, meanwhile I_d is measured. Constant drain current method ($I_{th}=10pA$) is used to extract V_{th} from the I_d - V_g characteristics.

Fig. 2.7 (a) Comparison of the time dependence of threshold voltage shift $|\Delta V_{th}|$ on p-MOSFET, using different characterization methods. ■ denotes $|\Delta V_{th}|$ measured using conventional DC I_d - V_g method; ▲ denotes $|\Delta V_{th}|$ measured using fast switching method. NBTI gate stress voltage in both cases is -2.6V . During the conventional DC measurement, V_g sweeps from 0 to -1V , I_d is measured. (b) Gate voltage waveform using fast switching method. At the end of NBTI stressing, drain current I_{ds} is measured at stress gate voltage. then V_g is lowered to -0.5V to measure drain current I_{dm} .

Gate voltage supply using fast switching method is shown in Fig. 2.7(b). Gate voltage is at -2.6V for a short period in the beginning. Without changing gate voltage, drain current I_{ds1} is measured. After that, V_g is lowered to -0.5V to measure drain current I_{dm1} . Then V_g is changed to -2.6V and kept constant during NBTI stressing. At the end of NBTI stress interval, drain current at -2.6V is measured as I_{ds2} . Then V_g is lowered to -0.5V to measure drain current I_{dm2} . Assuming transconductance g_m is constant with stress time, $|\Delta V_{th}|$ induced by NBTI stressing between the first time of measurement and the second time can be calculated from the change of drain current at -0.5V , as shown in Eqn. 2.2-3. Similarly, $|\Delta V_{th}|$ between the second and the third time of measurement can be calculated by Eqn. 2.2-4. Sum of $|\Delta V_{th}|$ between neighboring measurements results in total $|\Delta V_{th}|$ after certain period of NBTI stressing. Clearly

shown in Fig. 2.7(a), compared to data measured by the conventional DC method, $|\Delta V_{th}|$ measured by the fast switching method is larger. And the power-law exponent is also smaller.

$$|\Delta V_{th}|_1 = \frac{I_{dm2} - I_{dm1}}{g_m} \quad (2.2-3)$$

$$|\Delta V_{th}|_2 = \frac{I_{dm3} - I_{dm2}}{g_m} \quad (2.2-4)$$

However, the basic presumption of the fast switching method is the constant g_m during NBTI stressing, which is not true.

Fig. 2.8 Time evolution of transconductance g_m of p-MOSFET during NBTI stressing. g_m is extracted at $V_g = -0.5V$ from I_d - V_g characteristics. Stress condition is the same as in Fig. 2.7.

Fig. 2.8 illustrates the degradation of g_m along with NBTI stressing. Here g_m is extracted from I_d - V_g characteristics at $V_g = -0.5V$. Another problem with the fast switching method is that V_{th} obtained is controlled by the measurement gate bias $V_{g, meas}$. One set of fast switching measurement with various $V_{g, meas}$ values were

conducted. As shown in Fig. 2.9, as $|V_{g, \text{ meas}}|$ increases from 0.4V to 1V, significant increase in the measured $|\Delta V_{\text{ th}}|$ is observed. Therefore, fast switching measurement result is very sensitive to the selection of $V_{g, \text{ meas}}$.

Fig. 2.9 Threshold voltage shift $|\Delta V_{\text{ th}}|$ measured using fast switching method, as a function of measurement gate bias $V_{g, \text{ meas}}$. As $V_{g, \text{ meas}}$ decreases from -0.4V to -1V, significant increase in the measured $|\Delta V_{\text{ th}}|$ is observed. [Data after Ref. [72]]

Fast switching method contains unsolved theoretical problem, i.e. the presumption of constant transconductance is not correct. Furthermore, the result obtained by fast switching method is very sensitive to the selection of the gate bias during measurement. Therefore, conventional DC I_d - V_g characterization technique was used in this work to monitor NBTI-induced threshold voltage shift. As will be shown in the next few chapters, parallel experiments were carried out to reduce the errors induced by post-stress recovery.

Chapter 3 Role of Oxide Trapped Charge

3.1 Introduction

Negative bias temperature instability (NBTI) of p-type MOSFETs is due to the generation of positive charges along the Si/SiO₂ interface under negative stress at elevated temperature. Continuous effort was made in the investigation of the physical origins and generation mechanisms of these positive charges. Generation of interface traps by the breaking of Si-H bonds is generally believed to be one of the NBTI mechanisms [20-21]. But whether interface traps are the only defects leading to NBTI degradation is controversial. Other possibility such as oxide trapped charges was not believed to exist or only play a negligible role [73]. In this chapter, apart from interface traps, other positive charges which cannot be monitored by charge pumping current measurement are shown to be generated as well during NBTI stressing. Moreover, this part of charges which are not believed to be present in pMOSFETs with ultra-thin gate dielectrics is observed to play a significant role in the degradation of threshold voltage.

3.2 Experimental Setup

The test devices used in this chapter are p-MOSFETs with p⁺-polysilicon gate electrode. Some devices have gate dielectric fabricated via rapid thermal nitridation (RTN). The gate oxide of RTN1 devices is formed by dry oxidation, followed by N₂O annealing, producing ~ 1 at.% nitrogen concentration ([N]) at the Si/SiO₂ interface.

The equivalent oxide thickness (EOT) of RTN1 p-MOSFET is ~ 20 Å, while the channel width is $20\text{ }\mu\text{m}$, and channel length is $0.18\text{ }\mu\text{m}$. In addition to RTN1 devices, a set of RTN p-MOSFETs (RTN2) with different nitrogen concentration were tested. The gate dielectric (EOT = 17 Å) was first formed by rapid thermal dry oxidation and then subjected to different NO annealing conditions, which yields a nitrogen concentration in the range of 1-4 at.% near the Si-SiO₂ interface. RTN2 devices have $10\mu\text{m}/120\text{nm}$ channel width/length respectively. Besides, p-MOSFETs with gate dielectric fabricated via decoupled plasma nitridation (DPN) were tested as well. The gate dielectric of DPN devices is fabricated by exposing an *in-situ* steam generated base oxide, of thickness 13 Å, to remote nitrogen plasma of varying power and duration. The EOT of the DPN p-MOSFET is 15 Å, while the channel width is $10\text{ }\mu\text{m}$, and channel length is $0.1\text{ }\mu\text{m}$. The last category of p-MOSFET has a silicon nitride/SiO_x gate stack, and is a split of the RTN1 p-MOSFET. An optimized chemical vapor deposition process followed by *in-situ* H₂/O₂ annealing yielded a SiN gate p-MOSFET whose electrical performance is comparable to that of the RTN1 p-MOSFET. A negative bias of -2.6V (-2.1V for DPN p-MOSFET) is applied on the gate during static NBTI stressing, with other terminals grounded. NBTI stress was periodically interrupted and the drain current vs. gate voltage (I_d - V_g) characteristics are measured. Charge pumping (CP) current measurement was carried out after each I_d - V_g measurement. During NBTI stressing and measurement intervals, temperature is kept at 373K , if not separately elaborated. The gate bias during NBTI stress and measurement are shown in Fig. 2.1. I_d - V_g and CP measurements take $\sim 20\text{s}$ to finish.

Besides static NBTI stress, dynamic NBTI stress was also conducted in this chapter to assist in the data analysis. Under dynamic stress, the gate bias was switched between stress voltage (V_g^s) and relaxation voltage (V_g^r). A trapezoidal voltage pulse with 50% duty cycle, as shown in Fig. 3.1 was applied on the gate. During unipolar stressing, relaxation voltage V_g^r was set to 0, while during bipolar stressing, V_g^r was positive. The stress voltage V_g^s during dynamic stressing was kept the same as that during static stressing for comparison.

Fig. 3.1 A trapezoidal voltage pulse switching between stress voltage V_g^s and relaxation voltage V_g^r was applied on the gate during dynamic NBTI stressing. The rise/fall time is 50ns.

3.3 Role of Interface Traps

To study the role of interface traps on NBTI degradation, a negative bias of -2.6V is applied on the gate of pMOSFET with RTN gate oxide, which produced an oxide electric field $E_{ox} < 8\text{MV/cm}$. This level of oxide electric field is common for state-of-the-art ultrathin gate dielectrics. It is also low enough to avoid large amount of hot-hole injection into the gate oxide, ensuring the monitored degradation is mainly due to NBTI stress [74]. The solid squares in Fig. 3.2 illustrate the time dependence of threshold voltage shift $|\Delta V_{th}|$ of RTN p-MOSFET. A power-law time dependence, i.e.

$|\Delta V_{th}| \propto t^n$ is evident.

Fig. 3.2 Threshold voltage shift during static negative bias stressing (solid squares), as a function of stress time. Stress-induced interface trap density (solid triangles), calculated from the increase in charge pumping current, is also shown for comparison.

$$\Delta N_{it} = \frac{\Delta I_{cp}}{q f_{cp} A_G} \quad (3.3-1)$$

Based on Eq. 3.3-1, the density of stress-induced interface traps ΔN_{it} is calculated from the charge pumping current measurement results, and plotted as a function of stress time, as shown by the solid triangles in Fig. 3.2. The symbol q in Eq. 3.3-1 is electron charge, f_{cp} is the frequency used in charge pumping current measurement, and A_G is the area of gate dielectric (the product of channel width and length). A similar power-law time dependence of ΔN_{it} is observed, but the exponent for ΔN_{it} is ~ 0.3 , which is larger than the exponent extracted from the $|\Delta V_{th}|$ vs. stress time plot.

To further investigate the role of interface traps, $|\Delta V_{th}|$ during NBTI stressing is plotted versus ΔN_{it} in Fig. 3.3, as shown by the solid squares.

Fig. 3.3 Threshold voltage shift versus interface trap density for the RTN pMOSFET subjected to static stress. Gate stress voltage is -2.6V. Total stress time is 30000s. Solid squares denote measured $|\Delta V_{th}|$ vs. ΔN_{it} correlation. The straight line is the theoretical $|\Delta V_{th}|_{IT}$ vs. ΔN_{it} correlation, assuming donor-like interface traps to be the only defects leading to NBTI degradation: $|\Delta V_{th}|_{IT} = q\Delta N_{it}/C_{ox}$.

If no charges other than interface traps contribute to NBTI degradation, the expected threshold voltage shift $|\Delta V_{th}|$ should follow the expression:

$$|\Delta V_{th}|_{IT} = \frac{q\Delta N_{it}}{C_{ox}} \quad (3.3-2)$$

where q is electron charge, C_{ox} is oxide capacitance per unit area. The straight line in Fig 3.3 plots $|\Delta V_{th}|_{IT}$ as a function of ΔN_{it} , assuming donor-like interface traps to be the only defect leading to NBTI. The large difference between the measured $|\Delta V_{th}|$ and $|\Delta V_{th}|_{IT}$ for a given ΔN_{it} , challenges the assumption that no other charges exist apart

from the donor-like interface traps. There should be a significant portion of positive charges near the Si/SiO₂ interface, which affect threshold voltage shift but could not be monitored by charge pumping current measurement, possibly due to different physical location and/or energy distribution from the interface traps, or other distinct chemical characteristics. This portion of positive charge was previously regarded as oxide trapped charge (N_{ot}), based on the understanding that their physical location is in the gate oxide near the interface [75]. But along with the scaling down of the MOSFET channel length, the physical oxide thickness is reduced to less than 2nm. Thus, the existence of oxide trapped charge in devices with ultra-thin direct tunneling gate dielectric falls into dispute. As will be discussed in latter chapters, positive charges are trapped at higher energy states beyond electron tunneling window. For the convenience of later discussion, this portion of positive charge will be named N_{pc} , to distinguish it from the interface traps. Their physical location and other characteristics will be investigated in the later chapters. However, the conclusion above was based on the assumption that the CP technique measures all the NBTI-induced interface traps. The errors in measured ΔN_{it} due to the limitations of the CP current method must be addressed.

3.4 Discussion on CP Current Measurement Results

As discussed in section 2.1.3, the CP current measurement method could not monitor all of the stress-induced ΔN_{it} . As shown in Fig. 3.4, if underestimation of ΔN_{it} occurs during CP current measurement, i.e., ΔN_{it1} shifts to a smaller value ΔN_{it2} , for a given

$|\Delta V_{th}|$ measured from the preceding DC I-V method. As a consequence, the $|\Delta V_{th}|$ vs. ΔN_{it} plot will be shifted from curve A to curve B.

Fig. 3.4 Effect of the underestimation of ΔN_{it} on the ΔV_{th} vs. ΔN_{it} curve. Underestimation of ΔN_{it} results in curve A shifting towards curve B.

The difference between Curve B and Curve A at a given ΔN_{it} will be regarded as the contribution from other charges than interface traps. The vertical arrows in Fig. 3.4 illustrate the “apparent” ΔN_{ipc} due to underestimation of ΔN_{it} using the CP technique. Thus whether the difference between measured $|\Delta V_{th}|$ and $|\Delta V_{th}|_{IT}$ in Fig. 3.3 is resulted from errors in ΔN_{it} , or due to the existence of other charges will be studied subsequently.

As CP current measurement was carried out after DC I_d - V_g measurement, Yang *et al.* [70] argued that passivation of interface traps occurs during subsequent CP measurement. Therefore, ΔN_{it}^{ss} calculated from Subthreshold Swing (S), will be compared with ΔN_{it}^{cp} measured using the CP current method in this section. As S is extracted from the subthreshold portion of I_d - V_g curve, ΔN_{it}^{ss} should not suffer from

the passivation which may occur during the CP current measurement. Analysis consistently reveals stress induced generation of deep-level positive trap states in the upper half of the Si bandgap, as well as near and above the E_C of Si.

Fig. 3.5 Drain current of p-type MOSFET with gate nitrided oxide fabricated via decoupled plasma nitridation process, as a function of gate voltage.

Fig. 3.5 plots drain current I_d in log scale versus gate voltage V_g of a p-MOSFET with decoupled plasma nitrided gate oxide (DPN). Open squares denote the I_d - V_g curve before NBTI stress, and solid squares denote the curve after stress. Compared to the fresh curve, the I_d - V_g curve after NBTI stress is shifted to the negative gate bias direction, leading to a higher off current and a larger threshold voltage. Besides, the subthreshold swing S is also increased due to the generation of interface traps. Assuming a trap-free SiO_2 -Si interface, S may be expressed as

$$S = \ln 10 \frac{kT}{q} \left(1 + \frac{C_d}{C_{ox}} \right) \quad (3.4.1-1)$$

where k is Boltzman's constant; T is temperature; C_d is capacitance of depletion region; C_{ox} is oxide capacitance.

Fig. 3.6 Schematic energy band diagram of the p^+ -poly/SiON/n-Si structure in the subthreshold regime: The shaded region shows the energy range ($\sim 0.33\text{eV}$) probed by the subthreshold swing method.

Fig. 3.6 illustrates the portion of the Si bandgap probed by the subthreshold swing method.

In the subthreshold (depletion) regime, the Si surface band bending ψ_s at a given V_g may be expressed as

$$V_g - V_{FB} = \psi_s - \frac{\sqrt{2\epsilon_s\epsilon_o q N_D \psi_s}}{C_{ox}} + V_{poly} \quad (3.4.1-2)$$

where ϵ_s ($= 11.8$) is relative permittivity of Si, ϵ_o is permittivity of free-space, N_D is doping concentration of the n-Si substrate, V_{poly} (~ 0 in the subthreshold regime) is polysilicon depletion voltage, and V_{FB} is flat band voltage. In a fresh device with a low interface state density, V_{FB} may be assumed to be independent of ψ_s . The second term on the left-hand side of (2) denotes voltage drop across the gate oxide layer V_{ox} . For an ultra-thin gate oxide

(EOT = 1.5 nm), $C_{ox} \sim 2.3 \times 10^{-6}$ F/cm². For N_D on the order of 10^{17} cm⁻³, $V_{ox} \sim 60$ mV at $\psi_s = 0.6$ V. This first-order analysis implies that in an ultra-thin gate MOSFET, the change in Si surface band bending $\Delta\psi_s$ follows closely the change in the gate voltage ΔV_g in the subthreshold regime (i.e. $\Delta\psi_s \sim \Delta V_g$), as the voltage drop across the ultra-thin gate oxide is small. Hence, by extracting the subthreshold swing over a given V_g range, say $|\Delta V_g| = 0.4$ V (Fig. 3.6), one could ascertain that ~ 0.33 - 0.34 eV of the Si bandgap is probed.

With generation of interface traps and oxide trapped charge after NBTI stress, the flat band voltage of the p-MOSFET is changed. As a consequence, the same $|\Delta V_g|$ of 0.4 V would now correspond to a different ΔE_{ss} . But this problem can be overcome by the fact that in the subthreshold regime, I_d is a unique function of ψ_s ; in particular, $I_d \propto \exp(\psi_s)/\sqrt{\psi_s}$ [105]. Hence, by extracting the change in the subthreshold swing ΔS from a pre-defined fixed I_d range, e.g. 10^{-9} to 10^{-5} A which corresponds to the initial $|\Delta V_g|$ of 0.4 V (Fig 3.6), one would essentially be assured that approximately the same energy range of the Si bandgap is probed.

With the generation interface states, the subthreshold swing will be degraded as the capacitance associated with the interface traps C_{it} is in parallel with C_d . The resultant increase of subthreshold swing ΔS may be expressed as

$$\Delta S = \ln 10 \cdot \frac{kT}{q} \cdot \frac{C_{it}}{C_{ox}} \quad (3.4.1-2)$$

$$C_{it} = \frac{q \Delta N_{it}}{\Delta E_{ss}} \quad (3.4.1-3)$$

where ΔE_{ss} is the effective energy range probed by the subthreshold swing method. As shown in Eqn. 3.4.1-3, C_{it} is proportional to the stress-induced interface trap density ΔN_{it} . Thus from the shift of subthreshold swing, the density of interface traps generated during NBTI stress is calculated as ΔN_{it}^{ss} :

$$\Delta N_{it}^{ss} = \frac{\Delta E_{ss} C_{ox}}{\ln 10 kT} \Delta S \quad (3.4.1-5)$$

Fig. 3.7 Comparison of stress-induced interface trap density calculated from charge pumping measurement result (ΔN_{it}^{CP}) and subthreshold swing (ΔN_{it}^{ss}) to the effective positive trapped charge density extracted from threshold voltage shift (ΔN_{pt}), as a function of stress time. DPN device was stressed at -2.1V at 373K.

Fig. 3.7 plots ΔN_{it}^{ss} calculated from ΔS (open squares), as a function of stress time.

The interface trap density monitored by charge pumping measurement ΔN_{it}^{CP} is also included for comparison (solid squares). The solid triangles show effective positive trapped charge density ΔN_{pt} directly calculated via Eqn. 3.4.1-6.

$$|\Delta V_{th}| = \frac{q \Delta N_{pt}}{C_{ox}} \quad (3.4.1-6)$$

The large difference between ΔN_{pt} and ΔN_{it}^{CP} recalls Fig. 3.3. The difference between

the measured $|\Delta V_{th}|$ and $|\Delta V_{th}|_{IT}$ in Fig. 3.3 was attributed to the passivation of interface traps during the CP current measurement after I_d - V_g sweep [70].

However, negligible difference between ΔN_{it}^{ss} and ΔN_{it}^{cp} is observed in Fig. 3.7. As ΔN_{it}^{ss} is calculated from I_d - V_g sweep results, the good agreement between ΔN_{it}^{ss} and ΔN_{it}^{cp} indicates conforms to the general notion that both the CP and the subthreshold swing methods measure ΔN_{it} within a similar portion of the Si bandgap. A subtle point that should be highlighted is that the CP current measurement involves switching the gate bias from a negative voltage to a positive voltage. However, no change in gate polarity is involved in the preceding I_d - V_g measurement. The similar ΔN_{it}^{ss} and ΔN_{it}^{cp} thus imply no significant relaxation of ΔN_{it} occurs during the CP current measurement. The difference between the measured $|\Delta V_{th}|$ and $|\Delta V_{th}|_{IT}$ in Fig. 3.3 is not due to errors in ΔN_{it}^{cp} . Generally, I_d - V_g measurement of a p-MOSFET mostly probes the lower half and a limited portion of the upper half of the Si bandgap. In a direct tunneling gate p-MOSFET, a greater ΔN_{pt} would imply the existence of positive trap states (in the oxide bulk or at the Si/SiO₂ interface) at energy levels above the measurement window of the subthreshold swing method, i.e. high-energy-state positive charge ΔN_{pc} which cannot be measured by the subthreshold swing and the CP methods is generated during NBTI stressing.

3.5 Presence of Oxide Trapped Charge

As discussed in last few sections, high-energy-state positive charges ΔN_{pc} are

indicated to be generated in addition to interface traps during NBTI stressing. To further study the physical characteristics of ΔN_{pc} , the recovery behavior of NBTI-induced degradation during dynamic stressing was investigated. Furthermore, the analysis on dynamic stress induced degradation serves as a reinspection of the conclusion that no significant relaxation of ΔN_{it} occurs during the CP current measurement.

The basic concept is illustrated in Fig. 3.8. Besides static stress, bipolar ac gate stress was also employed. In both cases, the post-stress measurement sequence was kept the same, i.e. DC I_d - V_g sweep first, followed by I_{cp} measurement. For bipolar stress, a 100-kHz trapezoidal voltage pulse switching between V_g^s (equal to that of static stress) and a positive gate relaxation voltage V_g^r ($= +1.5$ V) was applied to the gate. The pulse transition time was 40 ns and the duty cycle was 50 %. V_g^r was chosen to be greater than the positive gate voltage (+1 V) used in I_{cp} measurement.

An important advantage of this approach is that the alternative positive gate cycles provide for “on-the-fly” recovery of oxide trapped charge induced by the preceding stress cycle. Under bipolar stress, the p-MOSFET was subjected to a positive gate bias larger than that used for I_{cp} measurement, and for a net recovery period which was as long as the net stress period. This net recovery period is much longer than the time taken for I_{cp} measurement (< 1 s). Hence, if ΔN_{it} passivation is indeed enhanced by a positive gate bias, one would expect ΔN_{it} of bipolar stress to be significantly

lower than that of the static stress. The $|\Delta V_{th}|$ and ΔN_{it}^{CP} data of the static and bipolar stress may then be compared at equivalent stress time to verify the hypothesis.

(a) Static Stress

(b) Bipolar Stress

(c) $|\Delta V_{th}|$ and ΔN_{it}^{CP}

Fig. 3.8 Using bipolar ac stress to investigate the extent of $|\Delta V_{th}|$ and ΔN_{it}^{CP} relaxation under positive gate biasing. The alternate positive gate cycles induce “on-the-fly” relaxation of oxide trapped charge generated by the preceding stress cycle. As a consequence, the threshold voltage V_{th} shift under bipolar stress is lower than that of the static stress (arrow 1). A gate relaxation voltage V_g^r ($> +1$ V) more positive than used by the charge pumping (CP) method was chosen. Since the net recovery time (t_o) is generally much longer than that encountered during CP current measurement, one would also expect a much lower ΔN_{it} for a net equivalent stress period $2t_o$, if stress induced interface states are indeed passivated by the alternate positive gate cycles. Arrow 2 and 3 show possible passivation of stress induced interface states by the CP method, resulting in an underestimation of ΔN_{it} .

The above prediction is, however, not borne out by Fig. 3.9. P-MOSFETs of gate dielectrics fabricated via different technologies were stressed under static and bipolar stress. As shown in Fig. 3.9(a), a significant reduction in $|\Delta V_{th}|$ is evident under bipolar stress (open squares), indicating that part of the oxide trapped charge generated during the stress cycle are indeed annealed during the recovery cycle. However, ΔN_{it}^{CP} of bipolar stress is comparable to that of the static stress for the entire period investigated. Similar observations are evident for p-MOSFETs having different gate dielectrics, shown in Fig. 3.9(b)-(d). It should be noted that $|\Delta V_{th}|$ is extracted from a DC I_d - V_g measurement performed before I_{cp} measurement. A much smaller $|\Delta V_{th}|$ but comparable ΔN_{it}^{CP} of bipolar stress unambiguously show that stress induced interface traps (at least those within the energy range probed by the CP method) are not responsible for the much greater recovery of $|\Delta V_{th}|$. The result thus conforms to the notion that the greater $|\Delta V_{th}|$ recovery observed under bipolar stress is due to the detrapping of oxide trapped charge [51, 55, 61, 76].

Observation of a similar ΔN_{it}^{CP} for both static and bipolar stress in Fig. 3.9, however, does not completely rule out the possibility that substantial relaxation of ΔN_{it} occurs during I_{cp} measurement. Ascertaining that measurement induced passivation of ΔN_{it} does not happen is crucial. If it does, a greater slope of the $|\Delta V_{th}|$ - ΔN_{it}^{CP} curve would result, overestimating the impact of ΔN_{pc} . Zhu *et al.* [77, 78] has shown that interface trap generation is increased under bipolar stress, especially for gate pulses of short transition time. Thus, it may be argued that the actual ΔN_{it} of bipolar stress is higher, but because of measurement induced

passivation, the resultant ΔN_{it}^{CP} appears to be nearly the same as that of static stress.

Fig. 3.9 Comparison of stress induced threshold voltage shift $|\Delta V_{th}|$ and interface state generation ΔN_{it}^{CP} (measured by CP method) for static and bipolar ac negative-bias temperature stress. Bipolar ac stress was carried out using a 100-kHz trapezoidal voltage pulse with 40-ns transition time. Arrow 1 denotes a reduction in $|\Delta V_{th}|$ under bipolar stress, but no decrease is observed for ΔN_{it}^{CP} . The p-MOSFETs have nitrided gate dielectrics fabricated using different technologies. Measurement sequence: DC I_d - V_g followed by CP current measurement.

To investigate whether passivation of ΔN_{it} occurs during positive gate biasing, ΔN_{it} is measured by the subthreshold swing method, instead of the CP method. The main advantages of the subthreshold swing method are: (1) No change in gate polarity during measurement, and (2) subthreshold swing degradation is derived from the same segment of the DC I_d - V_g curve used for extracting $|\Delta V_{th}|$. Hence, issues associated with the CP method are avoided altogether. Fig. 3.10 compares the $|\Delta V_{th}|$ and ΔN_{it}^{SS} data of DPN p-MOSFETs subjected to static and bipolar stress. As expected, $|\Delta V_{th}|$ is reduced under bipolar stress. But comparable ΔN_{it}^{SS} are again apparent in both cases. This result clearly indicates no

significant relaxation of interface states under positive gate biasing. Thus, I_{cp} can reliably measure ΔN_{it} , albeit within only a portion of the Si bandgap.

Fig. 3.10 Threshold voltage shift $|\Delta V_{th}|$ and increase in interface trap density ΔN_{it}^{SS} extracted from subthreshold swing degradation, under static and bipolar ac stress. $|\Delta V_{th}|$ is decreased under bipolar stress, but no decrease is observed for ΔN_{it}^{SS} .

Fig. 3.11 Threshold voltage shift $|\Delta V_{th}|$ under bipolar stress (open triangles), versus interface trap density ΔN_{it} . Also shown in the plot under static stress (solid squares) and $|\Delta V_{th}|_{IT}$ only counting ΔN_{it} .

As shown by the open triangles in Fig. 3.11, the threshold voltage shift $|\Delta V_{th}|$ under bipolar stress is plotted versus ΔN_{it} . The plot for static stress (solid squares) is included for comparison. Stress voltage in both cases was -3V, while the relaxation voltage V_g^r for bipolar stress was 2V. An important indication in Fig. 3.11 is that the slope of $|\Delta V_{th}|$ vs. ΔN_{it} plot reflects the contribution from ΔN_{pc} , relative to that from ΔN_{it} . A larger slope means larger $|\Delta V_{th}|$ at a given ΔN_{it} , indicating more contribution from ΔN_{pc} . To further study the recovery behaviors of ΔN_{it} and ΔN_{pc} during bipolar stress, a set of bipolar stress with relaxation voltage V_g^r ranging from 0.5V to 2.5V was carried out. Clearly shown in Fig. 3.12(a), as V_g^r is increasing from 0.5V ($\blacktriangle$) to 2.5V ($\blacktriangledown$), the slope of $|\Delta V_{th}|$ vs. ΔN_{it} plot keeps decreasing. On the other hand, ΔN_{it} after equivalent stress time is observed to increase when V_g^r is increasing. The stress-induced interface trap density and threshold voltage shift after 70000s of bipolar stress is plotted as a function of relaxation voltage in Fig. 3.12(b). $|\Delta V_{th}|$ and ΔN_{it} after 70000s unipolar stress ($V_g^r = 0V$) are included as well. Both $|\Delta V_{th}|$ and ΔN_{it} show a decrease-first-then-increase tendency as V_g^r is changed from 0V to 2.5V, but with different transition point.

Combining the two figures, when V_g^r is increasing from 0V to 0.5V, more ΔN_{pc} and ΔN_{it} are recovered, leading to the reduction of $|\Delta V_{th}|$. But beyond 0.5V, the increase of V_g^r leads to more generation of ΔN_{it} , but as more ΔN_{pc} continues being recovered, reduction in $|\Delta V_{th}|$ is observed. Later when V_g^r is further increased beyond 1V, the generation of ΔN_{it} dominates over the recovery of ΔN_{pc} , thus causing $|\Delta V_{th}|$ to increase

with V_g^r .

Fig 3.12 (a) Threshold voltage shift $|\Delta V_{th}|$ under bipolar stress versus interface trap density ΔN_{it} . Various relaxation voltage values are selected. Results under static stress (solid squares) and unipolar stress (open squares) are included for comparison. The straight line is the $|\Delta V_{th}|_{IT}$ vs. ΔN_{it} correlation, assuming donor-like interface traps to be the only defects leading to NBTI degradation: $|\Delta V_{th}|_{IT} = q\Delta N_{it}/C_{ox}$. (b) $|\Delta V_{th}|$ and ΔN_{it} after 70000s bipolar and unipolar stress, as a function of relaxation voltage.

However, the progressive reduction in the slope of the $|\Delta V_{th}|$ vs. ΔN_{it} plot indicates continuous recovery of ΔN_{pc} . The extreme case is when V_g^r is large enough to eliminate all the recoverable interfacial positive charge and $|\Delta V_{th}|$ is purely due to the accumulation of interface traps, i.e., $|\Delta V_{th}|_{IT} = q\Delta N_{it}/C_{ox}$, as shown by the straight line in Fig. 3.12(a). The negligible difference between the plots at $V_g^r = 1.5V$ and $2.5V$ indicates no more recovery of ΔN_{pc} occurs when $V_g^r > 2.5V$. The remaining difference between the curve for bipolar stress with $V_g^r = 2.5V$ and the straight line might be due to the underestimation of ΔN_{it} by the CP current measurement as discussed in sections 2.1.3 and 3.4. Another possibility is that certain portion of high-energy-state positive charge are “pinned” by the SiO₂-Si conduction offset and is anti-recovery (N_{pc}^{AR}), i.e., $|\Delta V_{th}| = q\Delta N_{it}/C_{ox} + q\Delta N_{pc}^{AR}/C_{ox}$. The hypothesis of high-energy-state positive charge trapped in the oxide will be discussed in the following section.

3.6 Deep-level Hole Traps

As discussed in the last few chapters, besides the interface traps, positive oxide trapped charge is also generated during the NBTI stressing. These positive oxide charges cannot be measured either by the subthreshold swing or the CP method, but result in significant threshold voltage shift. In view of the ultra-thin gate oxide thickness, the stability of the positive oxide charge under DC measurement implies that their energy states are situated outside the energy window of direct electron tunneling. Fig. 3.13 shows a schematic illustration of the energy states of positive oxide charges.

During stressing (Fig. 3.13(a)), the negative gate bias induces the generation of positive oxide charge and interface traps situated above the Si conduction band edge E_C [82, 83], in addition to those situated in the Si bandgap. A possible mechanism is the field- and thermal-assisted dissociation of oxide defect precursors (such as overcoordinated oxygen [84, 102]/nitrogen [85], strained Si-Si bonds, Si-H bonds etc. near the Si-SiO₂ interface). The subsequent loss of electronic charge to the conduction band of the n-Si substrate leaves behind positively charged hole-trap states above E_C .

Fig. 3.13 (a) Schematic energy band diagram illustrating the generation of deep-level hole traps (energy states above the n-Si substrate conduction band edge E_C) by negative-bias temperature stressing. Energy distribution of stress induced hole traps is denoted by the shaded region. A possible hole-trap generation mechanism involves field- and thermal-assisted dissociation of oxide defect precursors and subsequent loss of electronic charge to the conduction band of the n-Si substrate. (b) Shallower hole traps (i.e. those below E_C) are instantaneously discharged by electron tunneling in from the n-Si substrate upon termination of stress; deep-level hole traps, however, do not relax. (c) A positive gate bias lowers the hole-trap states, causing more relaxation but some fraction may still remain since their energy states are pinned by the Si-SiO₂ conduction band offset.

When the gate voltage is returned to zero (Fig. 3.13(b)), shallow hole-trap states (i.e. those below E_C) would spontaneously discharge by electronic charge exchange with the n-Si and oxide valence band, resulting in a fast-recovery transient [65, 70]. Positive charge of energy states above E_C , however, would not instantaneously discharge, and could be probed by post-stress DC I - V measurement. The situation in Fig. 3.13(b) was supported by the recovery of $|\Delta V_{th}|$ under unipolar ac stress (open squares in Fig. 3.12(a)). In the unipolar ac stress experiment, the relaxation gate voltage was at 0V, and the stress gate voltage was maintained at -3V. In the initial stage, $|\Delta V_{th}|$, for a given ΔN_{it} , is nearly the same as that of static stress, implying the generation of deep-level hole traps which remain stable even when the gate switches to 0 V or when the stress is interrupted. In the later stage, $|\Delta V_{th}|$ lies in between that of the static and bipolar stresses. This is due to the “partial” discharge of the positive oxide charges. Since the zero gate voltage could only lower a limited number of the deep-level hole traps below E_C , compared to bipolar ac stresses, a greater amount of positive oxide charges remain undischarged under unipolar ac stress.

Application of a positive gate voltage (Fig. 3.13(c)) (e.g. during I_{cp} measurement or bipolar stress) “lowers” these trap states below E_C , and induces a fast $|\Delta V_{th}|$ recovery transient [47, 51, 81, 86]. Larger V_g^+ further lowers the energy states of oxide charges, thus leading to more recovery of oxide charges and smaller $|\Delta V_{th}|$, as shown in Fig. 3.12(a). But a certain fraction of the hole-trap states are “pinned” by the Si-SiO₂ conduction band offset, and thus may not readily discharge even under a positive gate

voltage. In view of their very long relaxation time constant, these “permanently” positive defect states may be responsible for the slightly higher $|\Delta V_{th}|$ of bipolar stress as compared to $|\Delta V_{th}|_{IT}$ (Fig. 3.12(a)).

3.7 Impact of Nitrogen on Deep-Level Hole Traps

Deep-level hole trapped positive charge were proposed to be present in the last few sections. To study the origins of deep-level hole traps, impact of nitrogen was studied. Fig. 3.14 shows the $|\Delta V_{th}|-\Delta N_{it}$ characteristics of RTN2 p-MOSFETs subjected to unipolar ac stress. P-MOSFETs with different nitrogen concentration at the Si-SiO₂ interface, ranging from 1.3 at. % to 4.1 at. %, were stressed and compared. The measured $|\Delta V_{th}|$ is larger than $|\Delta V_{th}|_{IT}$ (dashed line), implying presence of positive oxide charges at deep energy levels.

In addition, two other salient features should be highlighted. First, the $|\Delta V_{th}|$ (at a given ΔN_{it}) of p-MOSFETs whose gate oxides have a higher Si-SiO₂ interfacial nitrogen concentration exhibits a larger increase in the initial stage. This implies greater generation of positive oxide charges. In the later stage, partial relaxation of positive oxide charges causes the slope of $|\Delta V_{th}|$ vs. ΔN_{it} curves to decrease and deviate from that of the initial stage. Second, more positive oxide charges are locked into p-MOSFETs whose gate oxides have higher interfacial nitrogen concentration. This implies that the density of deep-level trap precursors in heavily nitrated gate oxide is higher, thus rendering the p-MOSFET more resistant to recovery. In

oxynitrides with increased nitrogen content, severe interfacial bonding constraint is expected to arise from the high average coordination number of Si_3N_4 [87], leading to a more defective Si-SiO₂ interface. Hence, the deep-level hole traps may include a substantial portion of nitrogen-related defects [88, 89].

Fig. 3.14 Threshold voltage shift $|\Delta V_{th}|$ versus stress-induced interface trap density ΔN_{it} of RTN2 p-MOSFETs. RTN2 p-MOSFETs with different nitrogen concentration near the Si-SiO₂ interface were subjected to unipolar ac stress. A 50%-duty-cycle 100-kHz rectangular voltage pulse was applied on the gate, with $V_g^s = -2.6\text{V}$, and $V_g^r = 0\text{V}$. The dashed line is the $|\Delta V_{th}|_{IT}$ vs. ΔN_{it} correlation, assuming donor-like interface traps to be the only defects leading to NBTI degradation: $|\Delta V_{th}|_{IT} = q\Delta N_{it}/C_{ox}$.

Fig. 3.15 shows the schematic diagram illustrating the deep-level hole trapping process. Under NBTI stress, nitrogen-related defect precursors near the Si-SiO₂ interface may lose electrons by tunneling from gate oxide to the conduction band of Si substrate, leaving behind holes trapped in the gate oxide. Since these trapped holes have deep-level energy states outside of the electron tunneling window (Fig. 3.13 (b)-(c)), they may remain positively charged when the negative voltage stress is

removed or replaced by positive voltage stress.

Fig. 3.15 Schematic bandgap diagram illustrating the process of deep-level hole trapping. Nitrogen-related trap precursor of deep-level energy state loses electron to the conduction band of Si substrate, leaving behind a hole trapped in the deep-level trap state.

3.8 Summary

NBTI-induced threshold voltage shift and interface trap generation was studied. An objective analysis of DC I_d - V_g characteristics and charge pumping current change during NBTI stressing was carried out. In addition to interface traps in the lower-half of the Si bandgap, positive trapped charges are found in the upper half and above the conduction band of Si. Furthermore, the density of interface traps is almost unchanged by replacing static stress with bipolar stress, while the high-energy-state positive trapped charge is significantly decreased. The distinct relaxation behavior under bipolar stress indicates the high-energy-state positive trapped charges are of different

origin from interface traps. Furthermore, more high-energy-state positive oxide charges were generated in p-MOSFETs with more nitrogen in the gate oxide. Therefore, a deep-level hole trapping mechanism was proposed to generate oxide trapped positive charges. Those oxide trapped charge of energy states beyond electron tunneling window may remain undischarged under positive gate stress or during the relaxation cycle of bipolar ac stress.

Chapter 4 Temperature Dependence of NBTI

4.1 Introduction

Negative bias temperature instability (NBTI) is known to be a temperature-accelerated process, i.e. degradation in the performance of the p-MOSFET is significantly aggravated when the device is stressed at elevated temperature [20-21, 54]. In the conventional R-D model, NBTI is proposed to occur via a two-phase process: In an initial phase A, Si-H bonds located at the SiO₂-Si interface are broken via a chemical reaction. In a subsequent phase B, the liberated hydrogen species diffuse away from the SiO₂-Si interface, leaving behind dangling Si bonds, which act as interface traps [20]. Phase A could happen fast, but it is the slower phase B which controls the final generation rate of the interface traps, as hydrogen species at the SiO₂-Si interface could repassivate the dangling Si bonds. In the past, the temperature dependence of NBTI was explained by a thermally sensitive diffusion process of hydrogen species in phase B, which controls the reaction rate of the R-D process [21]. The generation rate of interface traps may be expressed as [21]

$$\frac{\partial N_{it}(t)}{\partial t} = G[N_D - N_{it}(t)] - S[N_{it}(t)]^{1/a} [C_{Xi}(t)]^{1/b} \quad (4.1-1)$$

where $N_{it}(t)$ is the concentration of interface traps (Si dangling bonds); N_D is the initial density of interface trap precursors (Si-H bonds); $C_{Xi}(t)$ is the concentration of diffusing hydrogen species X arising from the dissociation of Si-H bonds; G and S are

electric field dependent rate constants; a and b are related to the reaction coefficients [21]. Phase B is a thermally activated process, and the diffusion coefficient D_X of hydrogen species X may be expressed as follows:

$$D_X = D_0 \exp(-E_{aD} / kT) \quad (4.1-2)$$

where k is Boltzman's constant; T is temperature; D_0 is the constant, depending on the characteristics of the diffusing species and the transport mechanism. For instance, for H_2 diffusion in silicon dioxide, $D_0=5.64 \times 10^{-4}$ cm/s [90]. The diffusion of atomic hydrogen at Si surface has $D_0=10^{-3}$ cm/s [94]. E_{aD} is the activation energy required to trigger the diffusion process; for H_2 in SiO_2 , $E_{aD}=0.45$ eV [90]. For neutral species diffusing in an infinitely thick SiO_2 , ΔN_{it} may be derived from Eq. 4.1-1 and expressed as (Section 1.3.2)

$$\Delta N_{it} \propto (D_X)^{\frac{1}{4}} \quad (4.1-3)$$

For neutral species diffusing in SiO_2 of a finite thickness, ΔN_{it} may be expressed as [22]

$$\Delta N_{it}(t) = \frac{D_X}{t_{ox}} \int_0^t d\tau C_{Xi}(t-\tau) \left\{ 1 + 2 \sum_{n=1}^{\infty} \exp\left(-\frac{n^2 \pi^2 D_X t}{t_{ox}^2}\right) \right\} \quad (4.1-4)$$

For the transport of charged species, ΔN_{it} may be expressed as [22]

$$\Delta N_{it} \propto (D_X)^{\frac{3}{4}} \quad (4.1-5)$$

Assuming interface traps are the only defects responsible for NBTI degradation of the p-MOSFET, threshold voltage shift $|\Delta V_{th}|$ is expressed as

$$|\Delta V_{th}| = \frac{q \Delta N_{it}}{C_{ox}} = A \exp(-E_a / kT) \quad (4.1-6)$$

where A is a constant including factors such as stress time, electric field, etc; E_a is

related to the activation energy of the diffusion process of X . E_a is equal to $1/4$ of E_{aD} for neutral species diffusing in an infinitely thick SiO_2 ; while E_a equals to $3/4$ of E_{aD} for charged species diffusing in thin SiO_2 . Regardless of the dependence of ΔN_{it} on the diffusion coefficient D_x , as long as a unique diffusion process is controlling NBTI, there should be a single E_a .

As stated in Chapter 3, in addition to interface traps (ΔN_{it}), high-energy-state positive charges (ΔN_{pc}) are generated near the SiO_2 -Si interface during NBTI stressing. Thus, threshold voltage shift ($|\Delta V_{th}|$) of the p-MOSFET should be expressed as Eq. 4.1-7, where C_{ox} is the gate oxide capacitance per unit area.

$$|\Delta V_{th}| = \frac{q(\Delta N_{it} + \Delta N_{ipc})}{C_{ox}} \quad (4.1-7)$$

In Chapter 3, high-energy-state positive charge (ΔN_{ipc}) which is not monitored by the CP current measurement is shown to be responsible for a significant part of threshold voltage shift. Furthermore, different from ΔN_{it} , ΔN_{pc} can be further recovered when the unipolar stress is relaxed by bipolar stress, indicating distinct recovery behaviors of these two types of charges. Activation energy (E_a) is the signature of a thermally activated reaction/process. Different mechanisms may have similar E_a , but a single mechanism should not exhibit more than one E_a . Thus activation energy is an effective chemical parameter to investigate the mechanism behind observed electrical parameters. Therefore, activation energy of NBTI degradation is studied in this chapter. If only one physical mechanism is responsible for the threshold voltage shift, a single activation energy should be obtained. Single E_a of NBTI-induced $|\Delta V_{th}|$ was

observed on p-MOSFETs, and the value was observed to be smaller on oxynitride gate p-MOSFETs relative to SiO₂ gate devices. [37, 38] However, the mechanism producing the observed E_a value and the relationship between nitrogen and the reduced E_a are unclear. In this chapter, temperature dependence of NBTI-induced degradation on oxynitrided gate p-MOSFETs is investigated. Two distinct activation energy values are observed, indicating at least two mechanisms are responsible for NBTI of oxynitrided gate p-MOSFET.

4.2 Sample Selection and Experimental Setup

Four sets of p⁺ polysilicon gate p-MOSFETs with gate dielectrics fabricated via different techniques were tested in this chapter. Device A (SiON) has $\sim 21.6\text{\AA}$ oxynitride gate dielectric, fabricated via dry oxidation and N₂O annealing at 950°C. The nitrogen concentration [N] is ~ 1 at. % at the Si-SiO₂ interface. Device B (SiN) is a split of Device A and has a Si₃N₄-SiO_x gate stack. The nitride layer was deposited via chemical vapor deposition using an optimized SiH₄/NH₃ ratio, which suppressed formation of a Si rich film. *In-situ* H₂-O₂ annealing yields a $\sim 9\text{\AA}$ SiO_x interfacial layer and a resultant $\sim 19\text{\AA}$ nitride layer, giving an equivalent oxide thickness of $\sim 22.2\text{\AA}$. Device A and B have drawn channel length and width of 0.18 and 20 μm respectively. Besides, two types of p-MOSFETs with decoupled-plasma nitrided (DPN) gate dielectric were also tested. The gate dielectric of DPN devices was fabricated by exposing an *in-situ* steam generated base oxide, of thickness 13 $\text{\AA}$, to remote nitrogen plasma of varying power and duration. The resultant nitrogen profile in the gate oxide has a

peak located near the gate-SiO₂ interface and decreasing towards the SiO₂-Si interface. [N] ~6.3 at. % at the gate-SiO₂ interface was achieved for Device DPN1; while [N] ~13 at. % at the gate-SiO₂ interface was achieved for Device DPN2. EOT of the DPN p-MOSFET is 15 Å.

Fig. 4.1 Schematic diagram of the gate dielectric structure in Device A, Device B and DPN device. Device A has a ~21.6 Å oxynitride gate dielectric, with [N]~1at. % at the SiO₂-Si interface. Device B has a stacked gate dielectric, composed of a 19 Å Si₃N₄ layer and a 9 Å SiO_x layer. The nitrogen concentration of the DPN device peaks at the gate-SiO₂ interface, decreasing towards the SiO₂-Si interface. EOT of DPN devices is 15 Å.

NBTI degradation under static gate stress and dynamic gate stress are studied in this chapter. The stress conditions and measurement sequences were the same as those stated in Section 3.2 of Chapter 3. NBTI degradation was studied over a wide temperature range of 350K. Parallel tests were conducted at different temperature. Tested device was at certain temperature during stressing and measurement, in the range of 193K to 533K. Temperature variation was achieved by a miniature heater/refrigerator platen, with excellent long-term control of ±0.1K. According to the

Joule-Thomson effect, expansion of a gas at constant enthalpy causes cooling, if the initial temperature is below the Joule-Thomson inversion temperature. The Joule-Thomson inversion temperature of nitrogen is 621K (348°C), thus compressed nitrogen is used as the coolant, meanwhile electrical heating is activated to balance the temperature and keep the fluctuation within ± 0.1 K.

4.3 Non-Arrhenius Behavior of NBTI-Induced Threshold Voltage Shift

As shown in Fig. 4.2, static negative gate bias at -2.6V is applied on identical p-type MOSFETs, but at different temperatures. A power-law time dependence is observed at all temperatures, consistent with the results in Chapter 3. In addition, as temperature is increased over a wide range, threshold voltage shift at identical stress time is increased as well.

Fig. 4.2 Threshold voltage shift of p-MOSFETs stressed at different temperature, as a function of stress time.

As expressed by Eq. 4.3-1, threshold voltage shift $|\Delta V_{th}|$ is inversely exponentially dependent on stress temperature:

$$|\Delta V_{th}| = A \exp(-E_a / kT) \quad (4.3-1)$$

Thus, by plotting $|\Delta V_{th}|$ after certain period of NBTI stress as a function of $1/kT$, i.e., the Arrhenius plot; activation energy can be calculated from the slope.

Fig. 4.3 Arrhenius plot of threshold voltage shift on pMOSFETs with oxynitride gate dielectric. Stress condition is: $V_g = -2.6V$, $V_s = V_d = V_{sub} = 0$. Temperature ranges from $-80^\circ C$ to $260^\circ C$. Two activation energy (E_a) values are extracted from the two-slope plot.

Fig. 4.3 shows the Arrhenius plot of Device A, for a temperature range of 350 K. The devices were stressed for 50000s. A long stress period is necessary to ensure sufficient degradation at the lowest stress temperature (193 K) so that uncertainty in measuring small V_{th} shift (< 1 mV) may be avoided. Several salient features should be noted. In the low-temperature regime (≤ 303 K), device degradation is relatively independent of the stress temperature. The extracted activation energy E_a^L (from a best-fit of data points collected at temperatures below $25^\circ C$) is only ~ 0.037 eV. Deviation from this E_a is apparent as the stress temperature increases, implying that a second

temperature-sensitive mechanism begins to dominate. The extracted E_a^H in the high-temperature regime is ~ 0.14 eV (excluding data points in the “knee” region between 25°C and 75°C). The result thus implies the coexistence of 2 distinct degradation mechanisms.

Based on the R-D model, the activation energy of threshold voltage shift should be a single value in the range of $0.1\sim 0.3\text{eV}$ [20-21, 58, 98]. But two activation energies are extracted from Fig. 4.3, $E_a^L \sim 0.037$ eV is smaller than the values in the literature; while $E_a^H \sim 0.14$ eV is comparable to that observed by Mitani *et al.* [37] and Tan *et al.* [38]. The $E_a^H \sim 0.14$ eV was extracted in the temperature range above 75°C . And the E_a reported by Mitani *et al.* [37] and Tan *et al.* [38] was obtained at a similar temperature range ($>75^\circ\text{C}$). The limited temperature range used in the literature may explain the single E_a .

Since activation energy is a signature of a chemical/physical mechanism, the observation of two activation energies implies that there should be more than one mechanism responsible for the threshold voltage shift. Furthermore, the activation energy value for the low-temperature region E_a^L is $\sim 0.037\text{eV}$. Such a small number suggests at this low-temperature region, $|\Delta V_{th}|$ is almost independent of temperature. As discussed in Section 4.1, the diffusion of hydrogen species in SiO_2 is a thermally activated process. Besides, the activation energy for the diffusion of hydrogen species was reported to be larger than E_a^L . Hence, the results clearly show that it should be another temperature-insensitive mechanism/process responsible for the V_{th}

degradation at low temperature regime. Another important indication in Fig. 4.3 is that a significant portion of V_{th} degradation results from the temperature-insensitive mechanism. In the operation temperature range of CMOS circuits (75°C~125°C), $|V_{th}|$ extrapolated from the low temperature regime data accounts for a fraction of 45%~70% of the measured V_{th} degradation.

4.4 Coexistence of Two Mechanisms

In the last section, it is shown that two distinct activation energies may be extracted from the Arrhenius plot for the threshold voltage shift of Device A. The small activation energy for the low temperature regime strongly implies that a temperature-insensitive mechanism is determining a substantial portion of the threshold voltage shift. On the other hand, when temperature increases beyond 75°C, the activation energy is increased to a higher value of $\sim 0.14\text{eV}$. This indicates that another mechanism, which is more sensitive to temperature change, begins to dominate over the temperature-insensitive mechanism. For the convenience of later discussion, the temperature-insensitive mechanism will be named as TINS mechanism; and the temperature-sensitive mechanism will be named as TS mechanism. It is probably that the TINS is superposing to the TS mechanism, resulting the measured threshold voltage shift.

To verify the possibility of the coexistence of two mechanisms with different activation energies, a mathematical modeling is conducted to study the behavior of

threshold voltage shift with regard to the relative contributions of the TINS and TS mechanisms. As shown in Fig. 4.4, the dotted line denotes threshold voltage shift caused by the TINS mechanism as a function of temperature: $|\Delta V_{th}|^{TINS} = A \exp(-0.037 \text{ eV}/kT)$. The activation energy extracted from Fig. 4.3, $E_a^L = 0.037 \text{ eV}$ is used here; and A is the constant including other factors such as electric field, stress time, trap precursor density, etc.

Fig. 4.4 A mathematic modeling exercise showing a non-Arrhenius behavior of $|\Delta V_{th}|$, arising from the superposition of two physical processes/mechanisms having different activation energies; $|\Delta V_{th}|^{TINS} = A \exp(-0.037 \text{ eV}/kT)$; $|\Delta V_{th}|^{TS} = B \exp(-0.3 \text{ eV}/kT)$; $|\Delta V_{th}|^{total} = |\Delta V_{th}|^{TINS} + |\Delta V_{th}|^{TS}$.

The threshold voltage shift due to the TS mechanism used the expression $|\Delta V_{th}|^{TS} = B \exp(-0.3 \text{ eV}/kT)$, as shown by the dash-dot line in Fig. 4.4. B is a constant. Here 0.3 eV is used as it is the value reported by Jeppson and Svensson [20] for the R-D model. As the purpose of this mathematical modeling is to study the possibility of the coexistence of two mechanisms and their relative contributions, the value of A and B

is also arbitrarily selected, and resultant threshold voltage shift is in arbitrary unit. As will be discussed in later chapters, the value of A and B will change with other factors and they in turn determine the relative contributions from the TINS and TS mechanisms at a given temperature.

The solid curve shows the sum of $|\Delta V_{th}|^{TINS}$ and $|\Delta V_{th}|^{TS}$. At relatively low temperature, $|\Delta V_{th}|^{TS}$ (dash dot line) is negligible, thus the total $|\Delta V_{th}|$ is dominated by $|\Delta V_{th}|^{TINS}$, and the E_a of total $|\Delta V_{th}|$ is determined by the E_a of $|\Delta V_{th}|^{TINS}$ (dotted line). When the temperature is higher, the TS mechanism begins competing with the TINS mechanism and contributing more to the total threshold voltage shift. Thus, the solid curve bends upwards and approaches the dash dot line which denotes $|\Delta V_{th}|^{TS}$. At very high temperature, the total $|\Delta V_{th}|$ is dominated by $|\Delta V_{th}|^{TS}$ and the E_a becomes almost the same as that of $|\Delta V_{th}|^{TS}$. Such behaviors of the solid curve are identical to the $|\Delta V_{th}|$ vs. $1/kT$ plot in Fig. 4.3, providing a strong support for a coexistence of two mechanisms behind NBTI degradation of the oxynitride gate p-MOSFET..

25~150°C is the common temperature range studied in the literature, which might be the reason why the TINS mechanism was not discovered before. If only the portion of the solid curve within this temperature range is considered, an “apparent” $E_a^A \sim 0.16$ eV would be obtained, which is smaller than 0.3eV and larger than 0.037eV. The relative contribution of $|\Delta V_{th}|^{TINS}$ changes the apparent activation energy, which is shown by the bending part of the solid curve in Fig. 4.4. An increase in $|\Delta V_{th}|^{TINS}$

decreases the apparent activation energy, which might explain the reduction and the spread in activation energy reported for oxynitride p-MOSFETs in the literature.

4.5 Delineating the $|\Delta V_{th}|$ Due To the Two Mechanisms

From the mathematical modeling result presented in the last section, it is probable that two mechanisms coexist and simultaneously contribute to the NBTI-induced threshold voltage shift. Thus, in this section, attempts aiming at separating the two mechanisms will be made. Assuming the TINS mechanism dominates $|\Delta V_{th}|$ in the low temperature regime; and the physical process governing the TINS mechanism does not change with temperature, i.e. E_a for the TINS mechanism is a constant independent of temperature, $|\Delta V_{th}|^{TINS}$ at higher temperature may be estimated, by extrapolating the low temperature regime curve to the high temperature regime.

Fig. 4.5 Arrhenius plot for threshold voltage shift $|\Delta V_{th}|$ of Device A, stressed at -2.6V gate bias for 50000s. Measured $|\Delta V_{th}|$ is denoted by open squares; solid square shows $|\Delta V_{th}|^{TINS}$ due to TINS mechanism by extrapolating from the $|\Delta V_{th}|$ results at low temperatures; $|\Delta V_{th}|^{TS}$ (solid triangles) is obtained by subtracting $|\Delta V_{th}|^{TINS}$ (solid squares) from the measured $|\Delta V_{th}|$ (open squares).

The solid squares in Fig. 4.5 are the anticipated $|\Delta V_{th}|^{TINS}$ at high temperature, extrapolated based on the experimental data obtained for the low temperature regime. The open squares denote the measured $|\Delta V_{th}|$ at different temperatures. After subtracting $|\Delta V_{th}|^{TINS}$ (solid squares) from the measured $|\Delta V_{th}|$ (open squares), the resultant $|\Delta V_{th}|^{TS}$ is shown by solid triangles. The $|\Delta V_{th}|^{TS}$ data are observed to fall on one single straight line. The $|\Delta V_{th}|^{TS}$ data obey the Arrhenius law, indicating that a single physical mechanism is responsible for $|\Delta V_{th}|^{TS}$. The activation energy extracted from the $|\Delta V_{th}|^{TS}$ data is $\sim 0.23\text{eV}$. This value is much larger than E_a^{TINS} (0.037eV), and is in the range of $0.18\sim 0.3\text{eV}$ reported for the $|\Delta V_{th}|$ of SiO_2 gate p-MOSFETs in the past [20-21, 58, 98]. The results therefore strongly implies that NBTI of the ultra-thin oxynitride gate p-MOSFET is a result of the superposition of two different physical mechanisms. One of them is relatively independent of temperature and has a small activation energy $E_a^{TINS} \sim 0.037\text{eV}$; while the other one exhibits a stronger dependence on temperature and has a much larger activation energy $E_a^{TS} \sim 0.23\text{ eV}$. Since E_a^{TS} falls in the range of activation energy predicted by the R-D model, the temperature-sensitive mechanism is probably linked to the diffusion of hydrogen species.

The temperature dependence of $|\Delta V_{th}|$ for the DPN devices was studied as well. Fig. 4.6 shows the Arrhenius plot for $|\Delta V_{th}|$ of Device DPN1 with $[\text{N}] \sim 6.3\text{ at. \%}$ at the gate- SiO_2 interface. By a similar way as illustrated in Fig. 4.5, two coexistent NBTI mechanisms were observed. The threshold voltage shift due to the TINS mechanism

dominates at the low temperature regime; while the TS mechanism starts competing with the TINS mechanism as temperature increases. The coexistence of two NBTI mechanisms with distinct activation energies on p-MOSFETs with different gate dielectric fabrication techniques indicates that NBTI-induced $|\Delta V_{th}|$ of ultra-thin oxynitride p-MOSFET may not be solely modeled by the R-D model. The temperature-insensitive mechanism was present in oxynitride p-MOSFETs, regardless of the nitrogen profile in the gate oxide. Furthermore, the TINS mechanism induced $|\Delta V_{th}|$ (solid squares) plays a significant role within 75~125°C, which is the normal operation temperature range of CMOS circuits.

Fig. 4.6 Arrhenius plot for threshold voltage shift $|\Delta V_{th}|$ of Device DPN1, stressed at -2V gate bias for 50000s. Measured $|\Delta V_{th}|$ is denoted by open squares; solid square shows $|\Delta V_{th}|^{TINS}$ due to TINS mechanism by extrapolating from the measured $|\Delta V_{th}|$ results at low temperatures; $|\Delta V_{th}|^{TS}$ (solid triangles) is obtained by subtracting $|\Delta V_{th}|^{TINS}$ (solid squares) from the measured $|\Delta V_{th}|$ (open squares).

4.6 Temperature Dependence of Interface Trap Generation

In the last few sections, two mechanisms of very different temperature dependence are observed to result in the threshold voltage shift of p-MOSFETs with oxynitride gate dielectrics. In this section, the temperature dependence of interface trap generation will be studied as well. Fig. 4.7 plots the time dependence of stress-induced interface trap density (ΔN_{it}) monitored by the charge pumping current method, as a function of temperature. Power-law time dependence is observed for all temperatures, and as temperature increases from -80°C to 160°C , more interface traps are generated for a given stress time.

Fig. 4.7 Time dependence of stress-induced interface trap density ΔN_{it} of Device A, as a function of temperature. Negative bias at -2.6V is applied on the gate, with other terminals grounded.

To study the activation energy of interface trap generation, interface trap density ΔN_{it} after 50000s static stress is plotted as a function of $1/kT$ in Fig. 4.8. Similar to the $|\Delta V_{th}|$ data presented in the last section, a non-Arrhenius behavior is evident. The

results imply that more than one physical mechanism is responsible for interface trap generation during NBTI stressing. The activation energy for the temperature-insensitive (TINS) mechanism is $\sim 0.032\text{eV}$, very close to the activation energy for the TINS mechanism (0.037eV) extracted from the Arrhenius plot for $|\Delta V_{\text{th}}|$ (Fig. 4.5). By extrapolating from the data measured at low temperature, $\Delta N_{\text{it}}^{\text{TINS}}$ generated by the TINS mechanism at high temperature may be estimated and are denoted by the solid squares. $\Delta N_{\text{it}}^{\text{TS}}$, the component of $\Delta N_{\text{it}}^{\text{total}}$ generated by the temperature-sensitive mechanism (solid triangles) is obtained by subtracting $\Delta N_{\text{it}}^{\text{TINS}}$ (solid squares) from the measured $\Delta N_{\text{it}}^{\text{total}}$ (open squares). The activation energy for $\Delta N_{\text{it}}^{\text{TS}}$, E_a^{TS} is $\sim 0.26\text{eV}$, which is almost the same as the E_a^{TS} for $|\Delta V_{\text{th}}|^{\text{TS}}$ in Fig. 4.5.

Fig. 4.8 Arrhenius plot for stress-induced interface trap density ΔN_{it} of Device A, showing the coexistence of two different mechanisms responsible for the interface trap generation. Open squares denote $\Delta N_{\text{it}}^{\text{total}}$ measured by the charge pumping method. Solid squares denote $\Delta N_{\text{it}}^{\text{TINS}}$ extrapolated from the low temperature data; solid triangles denote $\Delta N_{\text{it}}^{\text{TS}} = \Delta N_{\text{it}}^{\text{total}} - \Delta N_{\text{it}}^{\text{TINS}}$.

Similar observations are also evident for DPN p-MOSFETs. ΔN_{it} components due to the TINS and TS mechanisms are separated as shown in Fig. 4.9. Thus, the TINS mechanism induced interface traps are also present in p-MOSFETs fabricated via DPN process. The small activation energy obtained from the low temperature regime indicates the TINS mechanism is a distinct physical process from the hydrogen diffusion process as described by the R-D model. The TINS mechanism should be a quasi-temperature-independent process, for instance, tunneling process. Further investigation of the TINS and TS mechanisms will be provided subsequently.

Fig. 4.9 Arrhenius plot for stress-induced interface trap density ΔN_{it} of DPN Device of [N] $\sim$ 13 at. %, showing the coexistence of two different mechanisms responsible for the interface trap generation. Open squares denote ΔN_{it}^{total} . Solid squares denote ΔN_{it}^{TINS} ; solid triangles denote $\Delta N_{it}^{TS} = \Delta N_{it}^{total} - \Delta N_{it}^{TINS}$.

4.7 Impact of Nitrogen on the Two NBTI Mechanisms

The possible coexistence of two distinct NBTI mechanisms with different activation energies were discussed in the last few sections. Since the activation energy for the TS

mechanism, E_a^{TS} is $\sim 0.23\text{eV}$, which falls in the range predicted by the R-D model, this temperature-sensitive mechanism is probably related to the diffusion of neutral hydrogen species. On the other hand, the temperature-insensitive mechanism needs more study to understand the exact trap generation process. Since the recent revival of interest on NBTI is primarily due to the severe degradation of p-MOSFETs employing nitrated gate oxide, the influence of nitrogen on the two mechanisms will be investigated in this section.

4.7.1. Impact of Nitrogen Concentration in the Gate Dielectric

Fig. 4.10 compares the Arrhenius plots for the threshold voltage shift of two types of p-MOSFETs with different nitrogen concentration in the gate dielectric. The open circles denote the $|\Delta V_{th}|$ vs. $1/kT$ curve for Device A, i.e., p-MOSFETs with oxynitride gate dielectric, stressed at -2.6V for 50000s . As discussed in the previous sections, $|\Delta V_{th}|$ is decomposed into $|\Delta V_{th}|^{TINS}$ and $|\Delta V_{th}|^{TS}$, the respective ΔV_{th} shift contributed by the TINS and TS mechanisms. The solid circles show that $|\Delta V_{th}|^{TS}$ exhibited an Arrhenius behavior, with activation energy $\sim 0.23\text{eV}$. To investigate the impact of nitrogen on the temperature dependence of $|\Delta V_{th}|$, the Arrhenius plot for $|\Delta V_{th}|$ of p-MOSFETs with thick pure SiO_2 gate dielectric was shown by the open triangles. Since contamination of nitrogen is inevitable during some fabrication steps for the state-of-the-art p-MOSFET, the pure SiO_2 gate p-MOSFET was from an earlier $0.6\text{-}\mu\text{m}$ CMOS technology, and the gate oxide is 12nm partial wet SiO_2 . The gate stress voltage for the SiO_2 gate p-MOSFET was adjusted to yield an oxide field

comparable to that of Device A.

As shown by the open triangles in Fig. 4.10, NBTI-induced $|\Delta V_{th}|$ of the SiO₂ gate p-MOSFET obeys the Arrhenius law. An activation energy, $E_a=0.27\text{eV}$, is extracted from the plot. The E_a agrees very well with the activation energy for the TS mechanism of Device A (solid circles).

Fig. 4.10 Threshold voltage shift $|\Delta V_{th}|$ of Device A, stressed at -2.6V for 50000s, as a function of $1/kT$ (open circles). Solid circles denote $|\Delta V_{th}|^{TS}$, the component of $|\Delta V_{th}|$ contributed by the TS mechanism. Also shown for comparison is the Arrhenius plot for the $|\Delta V_{th}|$ of a 12nm SiO₂ gate pMOSFET, stressed at comparable oxide field.

Such a good agreement indicates that the NBTI degradation of the nitrated gate p-MOSFET is a consequence of the superposition of a new degradation mechanism on the conventional mechanism reported for the pure SiO₂ gate p-MOSFET. In other words, the TS mechanism which exists in state-of-the-art ultra-thin oxynitride gate p-MOSFETs may have the same nature as that present in the SiO₂ gate p-MOSFET. The good agreement between the activation energies, which fall in the range of

0.18-0.3 eV as predicted by the R-D model, provides further support to the earlier claim that the TS mechanism is linked to the diffusion of neutral hydrogen species. The results also clearly show that increased degradation of the oxynitride gate p-MOSFET is due in a large part to the introduction of a new mechanism which is relatively independent of temperature. As shown in Fig. 4.10, the new mechanism is responsible for a substantial fraction of the $|\Delta V_{th}|$ at normal temperature range (75~125°C). Absence of the TINS mechanism in the SiO₂ gate p-MOSFET suggests that it is linked to the presence of nitrogen in the gate dielectric.

Fig. 4.11 Arrhenius plots for NBTI-induced threshold voltage shift $|\Delta V_{th}|$ of Device A and B. The stress conditions are as given in Fig. 5.8. The circles denote $|\Delta V_{th}|$ due to the TS mechanism in Device A and B.

Further investigation on the nitrogen effect was carried out by stressing p-MOSFETs with different nitrogen concentration in the gate dielectric. Extreme scenario of a Si₃N₄-SiO_x gate stack (Device B) was investigated. Both Device A and Device B were stressed at identical oxide field for 50000s. As shown in Fig. 4.11, $|\Delta V_{th}|$ of Device B is much larger than that of Device A, indicating that more nitrogen in the gate

dielectric worsens NBTI degradation [79].

As in the case of Device A, a non-Arrhenius behavior is clearly apparent for the $|\Delta V_{th}|$ of Device B. Adopting the same analysis as applied on Device A, the activation energy for the TINS mechanism is 0.019eV. This value is smaller than the E_a^{TINS} for Device A. The observation implies that increased nitrogen concentration in the gate dielectric further weakens the temperature dependence of the TINS mechanism. As discussed in section 3.7 of chapter 3, more nitrogen in the gate dielectric of p-MOSFETs enhances the generation of deep-level hole traps, which are relatively immune to fast recovery after the stress is terminated. Thus, larger V_{th} shift is monitored in Device B.

$|\Delta V_{th}|$ due to the TS mechanism are denoted by the circles in Fig. 4.11. Although the $|\Delta V_{th}|^{TS}$ of Device B (open circles) is also increased compared to Device A (solid circles), the increment is marginal, in contrast to the much more significant relative increase in $|\Delta V_{th}|^{TINS}$. These results indicate the increased $|\Delta V_{th}|$ of Device B is mainly due to the enhancement of the TINS mechanism. Heavier nitridation of the gate dielectric increases $|\Delta V_{th}|^{TINS}$ significantly, but has little impact on $|\Delta V_{th}|^{TS}$. The TS mechanism, which controls the NBTI degradation of conventional SiO₂ gate p-MOSFETs, is not altered by the nitridation of gate dielectrics. Inverse dependence of activation energy on nitrogen concentration in the gate dielectric was also observed by other groups [37, 38]. First-principle calculation of reaction energy showed

nitrogen-related R-D reactions may have smaller reaction energy, i.e., nitrogen makes the R-D process more easily occur [80]. However, the change of obtained activation energy should reflect variation in the physical mechanisms behind, not the possibility for a reaction to happen. The latter one may be studied through reaction energy calculation. But the change of activation energy cannot be explained through reaction energy calculation results. In this project, we focus on activation energy and the mechanisms behind activation energy. Based on the discussions above, nitrogen does not alter the activation energy of the TS mechanism, i.e., the nature of the classic NBTI mechanism is not changed by the presence of nitrogen.

Since it is not observed on SiO₂ gate devices, the temperature-insensitive mechanism should be related to the nitrogen introduced into the dielectrics for new-generation MOSFETs. Furthermore, Device B exhibited $\sim 10\times$ lower direct tunneling leakage current due to a larger physical dielectric thickness [81]. But larger NBTI-induced $|\Delta V_{th}|$ is observed on Device B. Thus the worsened degradation of Device B, especially in the low-temperature regime, is not due predominantly to direct tunneling current. The increased $|\Delta V_{th}|$ of Device B should be due to enhancement of the nitrogen-related TINS mechanism. Considering the activation energy is quite small ($\sim 0.019\text{eV}$), the TINS mechanism may be nitrogen-related trapping mechanism occurring in the gate oxide near the Si-SiO₂ interface. Holes from the substrate get trapped by the nitrogen-related defect precursors and result in negative V_{th} shift.

Fig. 4.12 shows the generation of interface traps in Device B during NBTI stress monitored via the charge pumping method and the results compared to those of Device A. Two distinct activation energies corresponding to two different degradation mechanisms are also evident.

Fig. 4.12 Arrhenius plots for NBTI-induced interface trap generation (ΔN_{it}) in Device A and B. Interface trap generation is measured by charge pumping current method. The circles denote ΔN_{it} generated via the TS mechanism. Also shown for comparison is the Arrhenius plot of the SiO_2 gate device.

Compared to Device A (solid squares), greater interface trap generation in Device B is apparent (open squares). The portion of ΔN_{it} generated by the TS mechanism (circles) exhibits an activation energy of $\sim 0.25\text{eV}$, which agrees very well with that of the SiO_2 gate p-MOSFET (triangles). Thus this portion of ΔN_{it} may be generated by the classic NBTI mechanism. On the other hand, an activation energy of $\sim 0.03\text{eV}$ was obtained from the Arrhenius plots of Device A and B in the low-temperature regime. Such a small activation energy indicates nitrogen introduces a new interface trap generation mechanism, which is distinct from the classic NBTI mechanism and is

temperature-insensitive. As shown by the low-temperature regimes of Device B, the portion of ΔN_{it} generated by the TINS mechanism is significantly increased compared to that of Device A. In contrary, the negligible difference between the Arrhenius plots of ΔN_{it} generated by the TS mechanism indicates nitrogen has almost no impact on the classic NBTI mechanism.

4.7.2. Impact of Nitrogen Profile in the Gate Dielectric

In the last section, impact of nitrogen concentration on NBTI mechanisms was discussed. The p-MOSFETs tested in the last section have peak nitrogen concentration near the Si-SiO₂ interface and reduced concentration towards the gate. To further study the role of nitrogen in the NBTI problems, DPN p-MOSFETs with nitrogen concentration peaking at the gate-SiO₂ interface were tested in this section. Fig. 4.13 shows the interface trap density as a function of $(kT)^{-1}$ of DPN p-MOSFETs with different nitrogen concentration at the gate-SiO₂ interface. Similar to the conclusion obtained in the last section, for DPN p-MOSFETs, more interface traps were monitored on the p-MOSFET with more nitrogen in the gate oxide (13 at. % [N]). Besides, the two NBTI mechanisms observed on Device A and B are also present in DPN p-MOSFETs. The nitrogen-introduced TINS mechanism generated a significant portion of ΔN_{it} (solid triangles), and this component of generated by the TINS mechanism is obviously increased in the p-MOSFETs of 13 at.% [N]. In contrary, enhancement of the TS mechanism is negligible.

Fig. 4.13 Arrhenius plots of interface trap density ΔN_{it} (extracted from charge pumping method) of DPN p-MOSFETs. Solid triangles and open squares denote measured data. Open triangles and solid squares denote the component due to the TS mechanism. Data of SiO_2 gate p-MOSFET are included for comparison (open circles).

Fig. 4.14 Arrhenius plots of threshold voltage shift $|\Delta V_{th}|$ of DPN p-MOSFETs with different nitrogen concentration [N] at the gate- SiO_2 interface. Solid squares and solid triangles denote measured $|\Delta V_{th}|$. Open squares and open triangle denote the component due to the TS mechanism. Data of SiO_2 gate p-MOSFET are included for comparison (open circles).

Threshold voltage shift of DPN p-MOSFETs with different nitrogen concentration was measured as well. As shown in Fig. 4.14, the components due to the two NBTI mechanisms were separated and compared. $|\Delta V_{th}|$ due to the TINS mechanism is significantly increased for the p-MOSFETs of 13 at.% [N] (solid triangles in the low-temperature regime). This is consistent with that observed on p-MOSFETs with nitrogen concentration peaking at the Si-SiO₂ interface. A different feature in Fig. 4.14 is the behavior of $|\Delta V_{th}|$ due to the TS mechanism. For p-MOSFETs with nitrogen concentration peaking at the Si-SiO₂ interface, nitrogen concentration has almost no impact on $|\Delta V_{th}|$ due to the TS mechanism, i.e. negligible increase of $|\Delta V_{th}|^{TS}$ was observed as [N] at the Si-SiO₂ interface increases. But for DPN p-MOSFETs with nitrogen concentration peaking at gate-SiO₂ interface, increase of $|\Delta V_{th}|^{TS}$ is obvious. Nevertheless, the enhancement of the TS mechanism is not as much as that of the TINS mechanism.

Therefore, regardless of the nitrogen profile in the gate dielectric, two NBTI mechanisms are present in ultrathin oxynitride gate p-MOSFETs. One of them is the classic hydrogen-diffusion mechanism observed on conventional SiO₂ p-MOSFET. The new mechanism is nitrogen-introduced temperature-insensitive mechanism, which is not present in SiO₂ p-MOSFETs and has positive correlation with nitrogen concentration in the gate dielectric.

4.8 Behavior of the Two Mechanisms under Dynamic Stress

In the last few sections, it was shown that two mechanisms with different temperature

dependence are responsible for the NBTI of ultra-thin oxynitride gate p-MOSFETs. One of them is the temperature-insensitive (TINS) mechanism, with an $E_a^{\text{TINS}} \sim 0.037\text{eV}$. The other is the temperature-sensitive (TS) mechanism, with a larger E_a^{TS} in the range of $0.23 \sim 0.25\text{eV}$. To further investigate the nature of the two mechanisms, the NBTI degradation under dynamic stress is studied in this section.

Fig. 4.15 Comparison on the Arrhenius plots of threshold voltage shift under static NBTI stress versus unipolar NBTI stress. -2.6V gate bias is applied under static stress for 25000s ; while for unipolar stress, gate voltage is switched between -2.6V and 0V for 50000s (50% duty cycle), at 100k Hz frequency.

Fig 4.15 compares the Arrhenius plots for $|\Delta V_{\text{th}}|$ subjected to different NBTI stress modes. Open squares denote $|\Delta V_{\text{th}}|^{\text{total}}$ measured under static stress, as a function of $1/kT$. For static stress, -2.6V was applied on the gate for 25000s , with other terminals grounded. For unipolar stress, the gate bias is switching between -2.6V and 0V , with other terminals grounded. As a 50% duty cycle is employed at unipolar stress, to keep the accumulative stress time identical, the clock time for unipolar stress is twice of the clock time for static stress, i.e., 50000s unipolar stress is applied. $|\Delta V_{\text{th}}|$ due to the two

NBTI mechanisms are separated. $|\Delta V_{th}|^{TINS}$ caused by TINS mechanism is shown by the solid line; and $|\Delta V_{th}|^{TS}$ caused by TS mechanism is shown by the solid squares. The activation energy for the TINS mechanism is $\sim 0.036\text{eV}$; while the activation energy for the TS mechanism is $\sim 0.25\text{eV}$. Both are quite close to the values extracted from the data after 50000s static stress (Fig. 4.5).

The threshold voltage shift measured under unipolar stress is denoted by the open circles in Fig. 4.15, as a function of $1/kT$. The difference between the open squares and open circles indicates part of $|\Delta V_{th}|$ was recovered during unipolar stress. Although the cumulative stress time is identical in the two stress modes, the 50% recovery time under unipolar stress results in a partial recovery of $|\Delta V_{th}|$. A non-Arrhenius behavior is also evident under unipolar stress. $|\Delta V_{th}|^{TINS}$ due to the TINS mechanism under unipolar stress is shown by the dashed line; while $|\Delta V_{th}|^{TS}$ due to the TS mechanism shown by the solid circles. As shown in Fig. 4.15, both $|\Delta V_{th}|$ due to TINS mechanism (dashed line) and TS mechanism (solid circles) are reduced under unipolar stress, indicating NBTI degradation caused by both mechanisms could be partially recovered after the negative gate bias is removed.

In addition to unipolar stress, bipolar stress was also carried out to study the recovery behavior of the two mechanisms. Fig. 4.16 compares the Arrhenius plots for $|\Delta V_{th}|$ subjected to bipolar stress and unipolar stress. The bipolar NBTI stress conditions were the same as those of unipolar stress, except that the gate bias was switched

between -2.6V and 1.5V. The solid circles in Fig. 4.16 denote measured $|\Delta V_{th}|^{total}$ under unipolar stress; while the solid triangles denote measured $|\Delta V_{th}|^{total}$ under bipolar stress.

Fig. 4.16 Comparison on the Arrhenius plots of threshold voltage shift under bipolar NBTI stress versus unipolar NBTI stress. Under unipolar stress, gate bias is switched between -2.6V and 0V for 50000s (50% duty cycle), at 100k Hz frequency. Under bipolar stress, gate bias is switched between -2.6V and 1.5V for 50000s (50% duty cycle), at 100k Hz frequency.

A reduction in $|\Delta V_{th}|^{total}$ for bipolar stress is observed at low temperature, but at higher temperature, the two $|\Delta V_{th}|$ vs. $(kT)^{-1}$ curves tend to merge, indicating comparable $|\Delta V_{th}|$ for both bipolar and unipolar stress. Total $|\Delta V_{th}|$ under the two stress modes are separated into two parts: one part due to TINS mechanism and the other part due to TS mechanism. $|\Delta V_{th}|^{TINS}$ due to TINS mechanism under unipolar stress is shown by the dashed line, while $|\Delta V_{th}|^{TINS}$ due to TINS mechanism under bipolar stress is shown by the solid line. Obviously, compared to unipolar stress, $|\Delta V_{th}|^{TINS}$ is smaller under bipolar stress, i.e. $|\Delta V_{th}|$ due to the TINS mechanism is further recovered under

bipolar stress. On the other hand, $|\Delta V_{th}|^{TS}$ due to TS mechanism under unipolar stress is shown by the open circles; while $|\Delta V_{th}|^{TS}$ due to TS mechanism under bipolar stress is shown by the open triangles. Almost no difference is observable between $|\Delta V_{th}|^{TS}$ under unipolar and bipolar stress, indicating further recovery in $|\Delta V_{th}|^{TS}$ under bipolar stress is negligible.

In summary, compared to static stress, threshold voltage shift $|\Delta V_{th}|$ is partially recovered under dynamic stress. Under unipolar stress with gate bias switching between -2.6V and 0V, both TINS mechanism induced $|\Delta V_{th}|$ and TS mechanism induced $|\Delta V_{th}|$ could be recovered. On the other hand, compared to unipolar stress, $|\Delta V_{th}|$ due to the TS mechanism is almost not changed under bipolar stress (gate bias switching between -2.6V and 1.5V). Only TINS mechanism induced $|\Delta V_{th}|$ is further recovered under bipolar stress.

4.9 Summary

By studying the temperature dependence of the NBTI-induced degradation of p-MOSFETs with oxynitride gate dielectric, two different mechanisms are shown to be responsible for the threshold voltage shift. One of the mechanisms is temperature-insensitive (TINS) with $E_a \sim 0.037\text{eV}$. This mechanism dominates the $|\Delta V_{th}|$ at low temperature (below 25°C). At high temperatures, although the contribution to NBTI degradation from the TINS mechanism is still present, another temperature-sensitive (TS) mechanism ($E_a \sim 0.23\text{eV}$) becomes important and begins

to dominate $|\Delta V_{th}|$. As temperature is increased, threshold voltage shift due to TS mechanism, $|\Delta V_{th}|^{TS}$ is significantly increased. In addition to threshold voltage shift, the temperature dependence of stress induced interface trap density ΔN_{it} is studied. Similar to the observation on $|\Delta V_{th}|$, ΔN_{it} is shown to result from two mechanisms. At low temperature, ΔN_{it} is mainly generated by the TINS mechanism; while at high temperatures, both TINS and TS mechanisms contribute to ΔN_{it} . As temperature increases, more ΔN_{it} is generated by the TS mechanism.

The influence of nitrogen in the gate dielectric on NBTI-induced degradation is also studied. The TINS mechanism has close correlation with nitrogen concentration, and is significantly enhanced by more nitrogen in the gate dielectrics. Thus the TINS mechanism should be nitrogen-introduced hole trapping mechanism present in ultra-thin oxynitride p-MOSFETs. In contrary, the impact of nitrogen on TS mechanism is not as important as TINS mechanism. The TS mechanism was observed to have similar thermal characteristics with the classic hydrogen-diffusion mechanism.

In addition to static NBTI stress, dynamic stress modes including unipolar stress and bipolar stress were investigated as well. Compared to static stress, both $|\Delta V_{th}|^{TINS}$ and $|\Delta V_{th}|^{TS}$ are partially recovered under unipolar stress. Comparing bipolar to unipolar stress, further $|\Delta V_{th}|$ recovery is shown to be mainly due to the recovery of $|\Delta V_{th}|^{TINS}$, while no decrease can be observed for $|\Delta V_{th}|^{TS}$.

Chapter 5 Time Dependence of NBTI

5.1 Introduction

NBTI is a critical reliability issue of p-MOSFETs, as the interfacial imperfections accumulates along with NBTI stressing. As stress time is increased, threshold voltage shift becomes severer and the drive current channel is more difficult to be formed. The fatal result is that the threshold voltage of the p-MOSFET is too large for normal operation. Clear description of the time dependence of NBTI-induced degradation is critical for the estimation of p-MOSFET's lifetime. Therefore, the time evolution of NBTI-induced degradation has been one of the most important research topics. Besides, the time dependence of NBTI-induced degradation also assists the investigation of NBTI mechanisms. Impact of nitrogen on NBTI problems was studied through the temperature dependence of threshold voltage shift and interface trap generation in the last chapter. In this chapter, role of nitrogen in NBTI problems will be further studied through the time dependence of NBTI-induced degradation.

Throughout the history of NBTI problems, power-law time dependence is repeatedly observed for $|\Delta V_{th}|$, as expressed by $|\Delta V_{th}|(t) = At^n$. The accurate determination of n guarantees the anticipation of the time evolution of V_{th} shift along with the stressing. Therefore, the lifetime of p-MOSFET can be obtained with the constants A and n known. Furthermore, the value of n reflects the degradation process of V_{th} . It was an

important parameter in the study of NBTI problems. However, controversy in the value of n exists among different research groups [20, 45, 58]. According to the conventional R-D model, the rate of NBTI-induced degradation of V_{th} or generation of interface traps is controlled by the diffusion of hydrogen species away from the Si-SiO₂ interface. Thus, the time evolution of $|\Delta V_{th}|$ is significantly affected by the hydrogen species and the structure of gate dielectric. The value of n was reported to be 0.25 for the diffusion of neutral hydrogen atoms in pure SiO₂ [21, 45]. As for hydrogen molecules to diffuse in pure SiO₂, n was shown to be $\sim 1/6$ based on simulation [45]. Since most of the n values in earlier research results were ~ 0.25 , neutral hydrogen atoms were believed to be the diffusion species for a long time. But Mahapatra *et al.* employed fast switching measurement method and yielded an $n \sim 0.13$ [67]. Based on their observation, the diffusion of hydrogen molecules was proposed to be the NBTI mechanism. The earlier theories based on $n \sim 0.25$ and neutral hydrogen atom diffusion process were challenged due to the possible fast recovery during measurement period. For the transportation of protons in SiO₂, n was reported to increase from 0.25 to 0.5 along with stress time [45]. Most of the researchers employed simulation results as the basis for argument on the type to hydrogen species. However, n values smaller than 0.1 was observed by fast measurement methods [50, 64]. Thus, there is controversy in the nature of diffusion species as different n values were observed.

Besides the variation of n value using different characterization methods, another phenomenon is the dependence of n on gate materials of p-MOSFETs. Compared to the conventional pure SiO₂ gate p-MOSFET, those p-MOSFETs with nitrogen introduced into the gate dielectric exhibited smaller n [37, 49]. Based on the conclusion of last chapter, two mechanisms with different temperature dependence coexistent are responsible for NBTI degradation. In this chapter, the time dependence of the two NBTI mechanisms was studied. The nitrogen-related TINS mechanism is characterized by $t^{0.1}$ time dependence. And the classic TS mechanism related to hydrogen diffusion is characterized by $t^{0.25}$. Furthermore, the roles of the two mechanisms in the reduction in the value of n were investigated. The more significant role of the TS mechanism at higher temperature causes the exponent n of the overall degradation to increase with stress temperature.

5.2 Experimental Setup

Three sets of p⁺ polysilicon gate p-type MOSFETs were tested in this chapter. Device A has nitrogen concentration [N] ~ 1 at.% at the Si/SiO₂ interface. Device B has a Si₃N₄-SiO_x gate stack. Device A has ~ 21.6Å oxynitride gate dielectric. The EOT of Device B is ~ 22.2Å. The devices have drawn channel length and width of 0.18 and 20 μm respectively. Pure SiO₂ gate p-MOSFET from an earlier 0.6-μm CMOS technology was also tested for comparison. The gate oxide is 12nm partial wet SiO₂.

NBTI degradation under static negative gate stress and dynamic gate stress are studied in this chapter, with similar stress condition as stated in Section 4.2 of Chapter 4. A computer-controlled stress-measurement sequence kept the measurement time delay (~ 20 s) constant. This DC method only probes the slow-recovery defects; the transience effect of fast trapping/detrapping is not included here. Since measurement delay was reported to affect the exponent n [45, 91], the purpose of the analysis in this chapter is neither to find the exact n value nor to extrapolate the lifetime of devices. It aims to provide a physical explanation for the reduce value of exponent n for modern oxynitride gate p-MOSFETs.

5.3 Non-Arrhenius Behavior of Time Dependence

As mentioned in the introduction, a power-law time dependence was repeatedly observed for NBTI-induced V_{th} shift, i.e. $|\Delta V_{th}| = At^n$. Fig. 5.1(a) shows such a time dependence of the threshold voltage shift of Device B. Although same power-law time dependence is observed for all temperatures, the slope is increased at higher temperature. The exponent n is increased from 0.095 to 0.158, when the temperature is increased from 183K to 513K. As discussed in section 1.3.4-4, fast recovery may occur during the measurement delay, and the exponent n may increase due to the underestimation of NBTI-induced degradation [50, 67]. However, the measurement time at all temperatures in Fig. 5.1 is identical. Furthermore, slower recovery of NBTI-induced degradation was observed at higher temperature [53, 73].

Fig. 5.1 (a) Threshold voltage shift $|\Delta V_{th}|$ of Device B as a function of stress time. Gate bias at -2.6V is applied for 70000s at different temperatures from 183K to 513K. Symbol denotes experimental result and lines are power-law fits. (b) The exponent of the power-law fit of $|\Delta V_{th}|$ vs. time plots, as a function of stress temperature.

To address the influence of measurement time on the spread in the exponent n , conventional SiO₂ gate p-MOSFET was stressed at different temperatures. As shown in Fig. 5.2, for all temperatures, $|\Delta V_{th}|$ shows a power-law time dependence with a constant exponent $n \sim 0.27$. Thus the measurement delay induced fast recovery does not cause the exponent n of TS mechanism to change with temperature. The spread in

the exponent n shown in Fig. 5.1(a) should be due to other reasons.

Fig. 5.2 Time dependence of threshold voltage shift $|\Delta V_{th}|$ on conventional pMOSFETs with SiO₂ gate dielectric, at different temperatures.

Classical R-D model proposed the diffusion of neutral hydrogen species to explain the observation that $n = 0.25$, independent of stress temperature [20, 22, 60]. The non-Arrhenius behavior is beyond the prediction of R-D model. Recently, an improved dispersive transport model was proposed to address the change of n value with stress temperature [49]. In this model, deviation of the exponent n from the classical 0.25 value was explained in terms of the density of defects in the gate dielectric. These defects are believed to disrupt the movement of hydrogen species in the oxide network, through random capture and release events. As temperature increases, the gradual transition from dispersive transport to classical diffusion was believed to be responsible for the increase of the exponent n from ~ 0.15 to 0.25 [49]. According to the dispersive transport model, the exponent n should exhibit a linear dependence on temperature [49]. However, as shown in Fig. 5.1(b), the variation in

exponent n in our case occurs over a narrower temperature range. The exponent n is approximately proportional to temperature in the range 300-450K (open squares in region II). For stress temperatures outside the 300-450K range, the exponent n is observed to remain approximately constant at ~ 0.11 in the low temperature regime (below 300K); and ~ 0.16 in the high temperature regime (above 450K). Therefore, the dispersive transport model cannot be employed to explain all these observations. A closer study of the mechanism responsible for NBTI degradation is required.

5.4 Time Dependence of the TS and TINS Mechanisms

As shown in Fig. 5.2, the exponent n of $|\Delta V_{th}|$ on conventional SiO₂ devices at different temperatures is ~ 0.27 , indicating the exponent for TS mechanism is independent of temperature, in contrast to the non-Arrhenius behavior of the exponent in Fig. 5.1. From the experimental results and analysis in chapter 5, it is shown that the temperature-sensitive (TS) mechanism is present on SiO₂ gate p-MOSFET. And the temperature-insensitive (TINS) mechanism superposes on the TS mechanism and results in severer NBTI-induced degradation of oxynitrided gate p-MOSFETs. The exponent n of the TS mechanism (~ 0.27) is much larger than the exponent in Fig. 5.1, indicating the superposition of the TINS mechanism on the TS mechanism causes the exponent n of Device B to decrease. Attempts to separate the two mechanisms and study their time dependence will be conducted subsequently.

Taking both the time and temperature dependence into account, NBTI-induced threshold voltage shift of the p-MOSFET may be expressed as

$$|\Delta V_{th}|(T, t) = C \exp\left(-\frac{E_a}{kT}\right) t^n \quad (5.4-1)$$

where C is a constant including factors such as oxide electric field and trap precursor density, etc. For a given stress condition, i.e. constant V_g^s is applied, C is approximately constant for different temperature and stress time. For a single degradation mechanism, for instance, the TINS mechanism, the corresponding threshold voltage shift may be expressed as

$$|\Delta V_{th}|^{TINS}(T, t) = C_1 \exp\left(-\frac{E_a^{TINS}}{kT}\right) t^n \quad (5.4-2)$$

Assuming that the TINS mechanism has unique time dependence, i.e. n is constant at all temperatures (which may be verified by the constant value in region I of Fig. 5.1(b)), $|\Delta V_{th}|^{TINS}$ at different temperature T_1 and T_2 are given by

$$|\Delta V_{th}|_{T_1}^{TINS}(t) = C_1 \exp\left(-\frac{E_a^{TINS}}{kT_1}\right) t^n \quad (5.4-3)$$

$$|\Delta V_{th}|_{T_2}^{TINS}(t) = C_1 \exp\left(-\frac{E_a^{TINS}}{kT_2}\right) t^n \quad (5.4-4)$$

Thus, from the $|\Delta V_{th}|^{TINS}$ after a certain stress period at a lower temperature T_1 in region I of Fig. 5.1, the $|\Delta V_{th}|^{TINS}$ after the same stress period at T_2 can be extrapolated by

$$|\Delta V_{th}|_{T_2}^{TINS} = \exp\left(\frac{E_a^{TINS}}{kT_1} - \frac{E_a^{TINS}}{kT_2}\right) |\Delta V_{th}|_{T_1}^{TINS} \quad (5.4-5)$$

For a given stress time, a plot of $|\Delta V_{th}|$ vs. $(kT)^{-1}$ is generated, as shown by the open squares in Fig. 5.3. $|\Delta V_{th}|^{TINS}$ at high temperature is estimated by extrapolating from

the low temperature data (according to Eq. 5.4-5), as shown by the solid triangles in Fig. 5.3. $|\Delta V_{th}|^{TS}$ is obtained by subtracting $|\Delta V_{th}|^{TINS}$ from $|\Delta V_{th}|^{total}$. Thus, $|\Delta V_{th}|^{TINS}$ at a given stress time at all stress temperatures is known. In the same way, $|\Delta V_{th}|^{TINS}$ at a given stress temperature can be obtained, as a function of stress time.

Fig. 5.3 Threshold voltage shift $|\Delta V_{th}|$ vs $(kT)^{-1}$ plot of Device B (open squares). The $|\Delta V_{th}|^{total}$ of Device B could be separated into the $|\Delta V_{th}|^{TINS}$ (solid triangles) and $|\Delta V_{th}|^{TS}$ (solid squares), the components of $|\Delta V_{th}|$ induced by the TINS and TS mechanism respectively.

The open triangles in Fig. 5.4 denote $|\Delta V_{th}|^{TINS}$ at 453K, as a function of stress time. By subtracting $|\Delta V_{th}|^{TINS}$ from measured $|\Delta V_{th}|$, which is denoted by the solid squares, $|\Delta V_{th}|^{TS}$ due to the TS mechanism are obtained, as denoted by the circles in Fig. 5.4. A power-law time dependence is observed for the TS mechanism induced $|\Delta V_{th}|$, with exponent $n \sim 0.258$, which agrees very well to the exponent obtained for p-MOSFET with SiO₂ gate dielectric (Fig. 5.2) [20-22].

Fig. 5.4 Threshold voltage shift $|\Delta V_{th}|$ of Device B stressed at -2.6V at 453K, as a function of stress time (solid squares). The triangles denote $|\Delta V_{th}|^{TINS}$ due to the TINS mechanism by extrapolating from low temperature data; while the circles denote $|\Delta V_{th}|^{TS}$ due to the TS mechanism by subtracting $|\Delta V_{th}|^{TINS}$ from $|\Delta V_{th}|^{total}$.

Fig. 5.5 Threshold voltage shift due to the TS mechanism as a function of time for different temperatures. Solid lines are power-law fits with exponent $n \sim 0.25$, independent of temperature.

In a similar way, $|\Delta V_{th}|^{TS}$ at different temperatures are extracted and plotted as a function of stress time in Fig. 5.5. As temperature is increased from 338K to 493K, $|\Delta V_{th}|^{TS}$ is correspondingly increased. More importantly, $|\Delta V_{th}|^{TS}$ exhibits power-law

time dependence, with an almost constant exponent of ~ 0.25 . This result implies that $|\Delta V_{th}|^{TS}$ due to the TS mechanism also has unique time dependence, independent of temperature. The slight deviation from the fitting line at longer stress time at 493K might indicate the onset of saturation of $|\Delta V_{th}|^{TS}$.

Therefore, in addition to the distinct temperature dependence (Fig. 5.3), the two NBTI degradation mechanisms have different time dependence as well. The TINS mechanism, which dominates $|\Delta V_{th}|$ at low temperatures, has a relatively weak time dependence with exponent $n \sim 0.1$, as shown in Region I of Fig. 5.1(b). Threshold voltage shift due to the TINS mechanism may be expressed as Eq. 5.4-6; the activation energy $\sim 0.019\text{eV}$ is extracted from Fig. 4.11. On the other hand, the TS mechanism, which coexists with the TINS mechanism at high temperatures, has a stronger time dependence with exponent $n \sim 0.25$ as shown in Fig. 5.5. This part of threshold voltage shift may be expressed as Eq. 5.4-7; the activation energy $\sim 0.23\text{eV}$ is extracted from Fig. 4.11.

$$|\Delta V_{th}|^{TINS}(T, t) = C_1 \exp\left(-\frac{0.019\text{eV}}{kT}\right) t^{0.11} \quad (5.4-6)$$

$$|\Delta V_{th}|^{TS}(T, t) = C_2 \exp\left(-\frac{0.23\text{eV}}{kT}\right) t^{0.25} \quad (5.4-7)$$

As discussed in section 3.6 and 3.7 of Chapter 3, nitrogen may introduce defect precursors in the gate oxide near the Si-SiO₂ interface. These defect precursors may get positively charged by losing electrons towards the conduction band of Si substrate (Fig. 3.15). A weak time dependence of $|\Delta V_{th}|$ due to the TINS mechanism is observed in this section, indicating the TINS mechanism may be a rapid tunneling process

almost independent of temperature and stress time. In chapter 3, it is found that part of interface traps are generated by the TINS mechanism. This can be explained by the energy distribution of nitrogen-introduced defect precursors. If the energy state of the defect precursor is high enough, i.e. beyond the conduction band of the substrate (Fig. 3.13), they can remain discharged even after the gate stress is terminated. This part of traps are named as deep-level hole traps in Chapter 3. Else if the energy state of the defect precursor is within the probe energy range of the CP current measurement, it may get charged and discharged during the CP current measurement, thus contributing to the measured ΔN_{it} .

5.5 Modeling of the Time Dependence of the TS and TINS Mechanisms

Based on the analysis in the last section, NBTI-induced $|\Delta V_{th}|$ of the oxynitrided gate p-MOSFET is the sum of $|\Delta V_{th}|^{TINS}$ and $|\Delta V_{th}|^{TS}$:

$$|\Delta V_{th}|^{total} = C_1 \exp\left(-\frac{0.019eV}{kT}\right)t^{0.11} + C_2 \exp\left(-\frac{0.23eV}{kT}\right)t^{0.25} \quad (5.5-1)$$

Fig. 5.6 shows the modeling results based on Eq. 5.5-1. Fig. 5.6(a) shows the time dependence of $|\Delta V_{th}|^{total}$ for the case of a constant $|\Delta V_{th}|^{TS}$ and a gradually increasing $|\Delta V_{th}|^{TINS}$. The circles in Fig. 5.6(a) denote $|\Delta V_{th}|^{TINS}$; while the solid squares denote $|\Delta V_{th}|^{total}$. From Case 1 to Case 3, $|\Delta V_{th}|^{TINS}$ is increasing by adjusting the value of C_1 . The value of C_1 and C_2 are listed in the inset. The resultant $|\Delta V_{th}|^{total}$ exhibits a gradually smaller exponent (lower slope). This indicates that for a given $|\Delta V_{th}|^{TS}$, an increase in $|\Delta V_{th}|^{TINS}$ will result in a reduction in the power-law exponent of $|\Delta V_{th}|^{total}$,

i.e. n will become closer to 0.1. This modeling result is consistent with Fig. 5.1(b), the exponent of $|\Delta V_{th}|^{total}$ in region I is ~ 0.1 , independent of temperature, as TINS mechanism dominates $|\Delta V_{th}|$ in this regime, like case 3 of Fig. 5.6(a).

Fig. 5.6 (a) Modeling the time dependence of $|\Delta V_{th}|$ for the case of a constant $|\Delta V_{th}|^{TS}$: The circles denote the $|\Delta V_{th}|^{TINS}$; and the solid squares denote the total threshold voltage shift, which is the sum of $|\Delta V_{th}|^{TS}$ and $|\Delta V_{th}|^{TINS}$. $|\Delta V_{th}|^{TINS}$ is increased from case 1 to 3. (b) Simulating the time dependence of $|\Delta V_{th}|$ for the case of a constant $|\Delta V_{th}|^{TINS}$: The open triangles denote $|\Delta V_{th}|^{TS}$; and the solid squares denote the total threshold voltage shift. $|\Delta V_{th}|^{TS}$ is increased from case 1 to 3.

Fig. 5.6(b) depicts the change in the time dependence of $|\Delta V_{th}|^{total}$ for the case of a constant $|\Delta V_{th}|^{TINS}$, and a gradually increasing $|\Delta V_{th}|^{TS}$. The open triangles in Fig. 5.6(b) denote $|\Delta V_{th}|^{TS}$; while the solid squares denote $|\Delta V_{th}|^{total}$. From Case 1 to Case 3, $|\Delta V_{th}|_{TS}$ is increased by adjusting the value of C_2 . The value of C_1 and C_2 are listed in the inset of Fig. 5.6(b). The resultant $|\Delta V_{th}|^{total}$ exhibits a progressively larger exponent (higher slope). The result indicates that for a constant $|\Delta V_{th}|^{TINS}$, a greater contribution from $|\Delta V_{th}|^{TS}$ will result in an increase in the exponent of $|\Delta V_{th}|^{total}$ (closer to 0.25). This trend is consistent with region II of Fig. 5.1(b). In this region, as temperature increases, $|\Delta V_{th}|$ due to the TS mechanism begins to dominate, thus the time dependence of $|\Delta V_{th}|^{total}$ approaches that of the TS mechanism. The increase in the exponent value in region III of Fig. 5.1(b) is not as obvious as region II. This might be due to the onset of saturation in the TS mechanism, as observed in Fig. 5.5.

Table II. NBTI mechanisms at different temperatures

Phase	T	n	Mechanisms
I	< 300K	~ 0.11	TINS mechanism dominating
II	300K $\sim$ 450K	$\propto T$	TINS & TS mechanisms coexistent, TS mechanism starts dominating as temperature increases
III	> 450K	~ 0.16	TS mechanism dominating

In summary, the modeling results and analysis above validate the relative role of the TINS mechanism and TS mechanism determining the time dependence of the overall $|\Delta V_{th}|$. In addition to a weak temperature dependence, the TINS mechanism has a rather weak time dependence as well. At low temperature, when the TINS mechanism is responsible for most of the V_{th} shift, the observed time dependence of $|\Delta V_{th}|$ is

weaker. At high temperature, as the TS mechanism gradually dominates $|\Delta V_{th}|$, the threshold voltage shift will exhibit a stronger time dependence. Therefore, the time dependence of NBTI-induced threshold voltage shift may change with temperature. Table II summarizes the NBTI mechanisms at different temperature ranges.

5.6 Nitrogen Effect on the Time Dependence

As discussed in section 4.7, nitrogen has significant role in NBTI degradation. The result shows that nitrogen is responsible for the TINS mechanism, which results in an increased $|\Delta V_{th}|$ of p-MOSFETs with oxynitride gate dielectric. The effect of nitrogen on the time dependence of NBTI degradation will be studied in this section, to further elucidate the role of nitrogen in NBTI degradation. NBTI degradation of Device B is studied in the last few sections, thus the degradation behavior of Device A, which has a lesser nitrogen content in the gate dielectric, is examined in this section. Fig. 5.7 plots the threshold voltage shift of Device A, stressed at $V_g^s = -2.6V$, as a function of stress time. At all temperatures, a power-law dependence on stress time is observed. Similar to Device B (Fig. 5.1(a)), a larger exponent is evident at higher temperature.

To study the effect of nitrogen concentration in the gate dielectrics, both Device A and B with identical EOT are stressed at identical oxide field for the same period. The time evolution of threshold voltage shift on Device A and B are compared in Fig. 5.8. As shown in Fig. 5.8, compared to Device B which has more nitrogen in the gate dielectric, a lesser shift in the threshold voltage is observed on Device A. More

importantly, the power-law exponent n , which reflects the degradation rate, is also smaller for Device B. This trend is more clearly illustrated in Fig. 5.9.

Fig. 5.7 Threshold voltage shift $|\Delta V_{th}|$ as a function of stress time, at different temperatures, for Device A. Symbol denotes experimental result and lines are power-law fits.

Fig. 5.8 The time dependence of NBTI induced threshold voltage shift of Device A and B. Identical stress condition was applied to both devices.

Fig. 5.9 Exponent of the power-law fit of the $|\Delta V_{th}|$ vs. time plot, as a function of temperature. Squares denote the exponent for Device A; triangles denote the exponent for Device B.

As shown in Fig. 5.9, the exponent n for Device B is consistently smaller than Device A, over the wide range of temperature studied. From the analysis presented in last section, the observed exponent is determined by the relative dominance of the TINS and TS mechanism. With a greater contribution from the TINS mechanism, which intrinsically has a weaker time dependence ($n \sim 0.1$), the ultimate exponent of $|\Delta V_{th}|^{\text{total}}$ will be resulted. Therefore, the smaller n value for Device B implies that the NBTI-induced degradation of Device B is mainly due to the TINS mechanism. This conclusion is consistent with the conclusion derived in section 4.7. As shown in section 4.7 (Fig. 4.11), a larger concentration of nitrogen in the gate dielectric increases $|\Delta V_{th}|$ due to the TINS mechanism in Device B. Therefore, the overall degradation of Device B exhibits a much weaker time dependence. A interesting feature of Fig. 5.9 is that the exponent n at higher temperature is larger than 0.25. This indicates the exponent may become larger than the real value, due to the

measurement delay induced fast recovery [50, 67]. However, the important information of Fig. 5.9 is not the values of exponent, but the smaller n of Device B. Since the measurement delay for the two devices is identical, the different exponent values between Device A and B should not be due to the measurement induced recovery.

5.7 Summary

The time dependence of NBTI-induced threshold voltage shift is studied in this chapter, as a function of temperature. Although the $|\Delta V_{th}|$ at all temperatures could be fitted to a power-law time dependence, non-Arrhenius behavior of the exponent n is observed, i.e. the exponent increases as temperature increases. To address such a non-Arrhenius behavior, the threshold voltage shift was separated into two components: one part is induced by a temperature-insensitive mechanism and the other part is induced by a temperature-sensitive mechanism, on the basis of the insight derived from the detailed temperature dependence study of $|\Delta V_{th}|$ presented in Chapter 4. The threshold voltage shift due to the TINS mechanism exhibits a power-law dependence on stress time, with a small exponent of ~ 0.1 . On the other hand, $|\Delta V_{th}|$ induced by the TS mechanism exhibits a larger exponent of ~ 0.25 . The non-Arrhenius behavior of the overall exponent of $|\Delta V_{th}|$ was found to result from the relative dominance of the TINS and TS mechanism. As temperature decreases, the relative dominance of the TINS mechanism over the TS mechanism will result in a weaker time dependence of the overall threshold voltage shift (closer to 0.1), and vice

versa. Furthermore, a comparison between Device A and B in terms of the time dependence of $|\Delta V_{th}|$ also validates the claim that the TINS mechanism is related to nitrogen in the gate dielectric. The study unambiguously shows that for state-of-the-art oxynitride gate p-MOSFETs, increased generation of nitrogen-introduced hole traps plays an important role in the time dependence of the NBTI induced threshold voltage shift.

Chapter 6 Frequency Dependence of

Dynamic NBTI

6.1 Introduction

During static NBTI stressing, due to the generation of interfacial imperfections, threshold voltage and drive current of p-MOSFETs degrades with stress time. However, it has been shown that the threshold voltage shift caused by static NBTI stress is substantially reduced when the stress is terminated [51, 53]. Since ac gate stress on p-MOSFET is more frequently encountered during industry operation, the recovery of NBTI-induced degradation has important indication. Ignoring the recovery effects may induce significant underestimation of the lifetime of p-MOSFETs [47]. Under ac stress, the gate bias is switched between stress voltage ($V_g^s < 0$) and relaxation voltage ($V_g^r \geq 0$). It was observed less degradation of p-MOSFET and the CMOS circuit was resulted due to the recovery of NBTI degradation during the relaxation cycles [47]. Therefore, theories based on static NBTI experimental results must be adjusted and take recovery into account for ac stress.

Recovery of threshold voltage shift triggers keen interest in the behaviors of NBTI-induced degradation under dynamic NBTI, which has a direct impact on circuit reliability. Zhu *et al* [77] reported that the ac pulse waveform affects stress-induced

interface trap density. Rising time (t_r) for the gate bias to switch from V_g^s to V_g^r has more significant impact on interface trap generation than the falling time (t_f). The longer t_f results in the less interface traps generated [77]. Frequency dependence of NBTI-induced degradation under dynamic stress was also studied widely. However, controversy exists in this topic. Weak or no dependence on frequency was reported for dynamic NBTI induced threshold voltage shift [92, 93]. This observation was ascribed to the intrinsic symmetry of the stress and relaxation phases under the framework of the R-D model [60]. As discussed in the last few chapters, some conclusions based on the R-D model were found to be not applicable for modern ultra-thin oxynitride gate p-MOSFETs. The R-D model does not take into account the role of nitrogen in the gate dielectric. In contrast to the conclusion based on the R-D model, less threshold voltage degradation and longer lifetime for oxynitride p-MOSFETs were reported when the gate frequency is increased [94].

As discussed in the pervious two chapters, a distinct nitrogen-driven NBTI mechanism is present on oxynitride gate p-MOSFETs. Thus, it is crucial to understand the effect of nitrogen on dynamic NBTI induced threshold voltage shift. In this chapter, it is shown that the threshold voltage shift arising from dynamic NBTI may be described by an inverse frequency power-law, i.e. $|\Delta V_{th}| \propto f^{-\gamma}$, for the frequency range investigated. For p-MOSFETs whose gate dielectric contains a higher nitrogen concentration, dynamic NBTI induced $|\Delta V_{th}|$ is not only increased, it also exhibits a much weaker dependence on gate frequency. The resultant greater lock-in of $|\Delta V_{th}|$ at

high frequency has serious implication on circuit-level reliability. It is shown that this greater lock-in of $|\Delta V_{th}|$ at high frequency is mainly due to an increased generation of recovery-resistant deep-level hole traps in heavily nitrided gate p-MOSFETs.

6.2 Experimental Setup

P⁺ polysilicon gate p-MOSFETs with decoupled-plasma nitrided (DPN) and rapid thermal nitrided (RTN) SiO₂ gate dielectric were tested. For the DPN p-MOSFETs, nitrogen was incorporated mainly at the gate-SiO₂ interface. The peak nitrogen concentration [N] at the gate-SiO₂ interface was varied by controlling the exposure time to nitrogen plasma. DPN p-MOSFETs of [N] ranging from 6.3 at. % to 13 at. % were tested. For the RTN p-MOSFETs, [N] is situated closer to the Si-SiO₂ interface. RTN p-MOSFETs of [N] ranging from 1.1 at. % to 4.2 at. % were tested. The EOT of the DPN p-MOSFET is 15 Å, and the drawn channel width and length are 10 and 0.1 μm respectively. The EOT of the RTN p-MOSFET is 20 Å, and the drawn channel width and length are 10 and 0.12 μm respectively.

Unipolar ac stress was performed at 373K using a trapezoidal gate voltage pulse (50 ns transition time; 50% duty cycle) with frequency ranging from 1 – 10⁶ Hz. The gate voltage for the stress cycle V_g^s was –2V for the DPN p-MOSFET, and the V_g^s was –2.6V for the RTN p-MOSFET. The gate voltage for the relaxation cycle V_g^r was 0 V for both types. The stress was periodically interrupted for ~ 15 s for DC I_d - V_g measurement, followed by charge pumping current measurement. V_{th} was extracted

via the constant drain current (I_d) method. A trapezoidal gate pulse switching between 1 and -0.9 V was applied during CP measurement. Because fast-recovery already occurs during the relaxation cycle of AC stress, subsequent recovery occurs much more slowly over an extended period. Hence, the periodic stress interruption did not severely underestimate $|\Delta V_{th}|$. To verify that negligible slow recovery occurs during the DC measurement, parallel experimental using fast switching (FS) measurement following identical ac stress was conducted.

Fig. 6.1 Gate waveform of unipolar ac stress and fast switching characterization. During fast switching measurement interval, gate voltage is lowered to $V_{g, measB}$, then a pulse is superposed onto gate voltage supply to further lower gate voltage to $V_{g, measT}$, after measurement is finished, the gate voltage is brought back to V_g^s . Drain current is measured twice during measurement interval, at $V_{g, measB}$ and $V_{g, measT}$ respectively. Fast switching measurement takes ~ 100 ms.

Fig. 6.1 illustrates the gate voltage waveform during unipolar ac stress and following FS measurement. During stress and measurement, $V_d = -50$ mV; source and substrate terminals are grounded. During the stress period, $V_g^s = -2.6$ V and $V_g^s = 0$. During the FS measurement, gate voltage is lowered to $V_{g, measB}$ (-0.6 V) to measure drain current I_{dB} , then gate voltage is further lowered to $V_{g, measT}$ (-0.5 V) to measure drain current

I_{dT} . After FS measurement is finished, gate voltage is changed to V_g^s to continue stressing. Transconductance g_m can be calculated by

$$g_m = \frac{I_{dB} - I_{dT}}{V_{g, measB} - V_{g, measT}} \quad (6.2-1)$$

Since the drain voltage is -50 mV, the p-MOSFET is working at linear region during the FS measurement. Drain current is thus given by

$$I_d = \mu C_{ox} V_d \frac{W}{L} \left(V_g - V_{th} - \frac{V_d}{2} \right) \quad (6.2-2)$$

Since identical $V_{g, measB}$ is applied at two neighboring measurement intervals, the relationship between $I_{d, meas}$ and V_{th} shift can be derived from Eq. 6.2-2 and expressed by

$$\frac{\partial I_{d, meas}}{\partial V_{th}} = -\mu C_{ox} V_d \frac{W}{L} \quad (6.2-3)$$

If the stress time between neighboring FS measurement intervals is kept short enough, V_{th} shift during this stress period may be assumed negligible compared to V_{th} , i.e. $\Delta V_{th} \ll V_{th}$. Thus, it can be derived from Eq. 6.2-2 that

$$g_m = \frac{\partial I_d}{\partial V_g} = \mu C_{ox} V_d \frac{W}{L} \quad (6.2-4)$$

By combining Eq. 6.2-3 and 6.2-4, V_{th} shift during each stress period can be expressed by

$$\partial V_{th} = -\frac{\partial I_{d, meas}}{g_m} \quad (6.2-5)$$

Therefore, by combining Eq. 6.2-1 and 6.2-5, the overall V_{th} shift after certain period of ac stress can be expressed by

$$|\Delta V_{th}(t)| = \sum_{n=1}^m \left(\frac{I_{d,meas}(n) - I_{d,meas}(n-1)}{I_{dB}(n-1) - I_{dT}(n-1)} (V_{g,measB} - V_{g,measT}) \right) \quad (6.2-6)$$

where m is the number of measurement intervals.

Fig. 6.2 Threshold voltage shift of RTN nitrided gate p-MOSFET ([N] ~ 4.2 at. %) obtained by different measurement methods, as a function of stress time. Unipolar ac stress at 1M Hz was applied on the gate: $V_g^s = -2.6V$; $V_g^r = 0V$; duty cycle = 50%; rising/falling time = 50 ns. (■) denotes $|\Delta V_{th}|$ measured by fast switching (FS) method. (□) denotes $|\Delta V_{th}|$ extracted by constant drain current method from the subthreshold region of DC I_d - V_g curve. (Δ) denotes $|\Delta V_{th}|$ extracted at $V_g = -0.6V$ from DC I_d - V_g data.

As shown in Fig. 6.2, $|\Delta V_{th}|$ measured by DC I_d - V_g method (Δ and □) is compared to that measured by fast switching (FS) method. Open squares denotes $|\Delta V_{th}|$ extracted from the subthreshold region of I_d - V_g characteristics, using constant drain current method as discussed in section 2.2.1 of chapter 2. The significant difference between $|\Delta V_{th}|$ extracted at subthreshold region and that measured by FS method might lead people to believe DC method severely underestimates $|\Delta V_{th}|$. However, if comparing $|\Delta V_{th}|$ measured by FS method to that extracted from the linear region ($V_g = -0.6V$) of I_d - V_g characteristics (■ vs. Δ), negligible difference is observed. Therefore, the $|\Delta V_{th}|$

at the same operation regime of p-MOSFETs after ac stress is similar by using DC measurement or FS measurement. The “underestimation” of $|\Delta V_{th}|$ by constant drain current method is due to the non-parallel shift of I_d - V_g curves before and after stress (Fig. 6.3). $|\Delta V_{th}|$ measured by the conventional DC method reflects the V_{th} shift in the subthreshold region; while the FS method gives the shift in the linear region. In this chapter, results from DC method will be used since no significant slow recovery of $|\Delta V_{th}|$ occurs after unipolar ac stress.

Fig. 6.3 I_d - V_g characteristics of RTN gate p-MOSFETs of $[N] \sim 4.2$ at. % before and after unipolar ac stress. Stress condition is the same as in Fig. 6.2. Shift of gate voltage at a given drain current increases as $|V_g|$ increases. The inset shows the subthreshold region and part of linear region of the I_d - V_g curve.

6.3 Frequency Dependence of Threshold Voltage Shift

During the relaxation cycle of unipolar ac stress, the gate voltage is switched to 0.

Part of $|\Delta V_{th}|$ can be recovered due to the termination of negative gate stress [93].

During the next stress cycle, further generation of interfacial imperfections will cause $|\Delta V_{th}|$ to increase again. However, compared to static stress, the overall $|\Delta V_{th}|$ after identical period of unipolar ac stress is smaller [95]. This is clearly shown in Fig. 6.4.

Fig. 6.4 Threshold voltage shift of RTN p-MOSFET of $[N] \sim 1.1$ at. % subjected to static NBTI stress and unipolar stress, as a function of stress time. For static stress, $V_g = -2.6V$. For unipolar stress, stress cycle: $V_g^s = -2.6V$; relaxation cycle: $V_g^r = 0$; pulse transition time: 50 ns; duty cycle: 50%.

Unipolar ac stress was applied on the RTN p-MOSFET of $[N] \sim 1.2$ at. % for 50000s (clock time), at various frequencies. $|\Delta V_{th}|$ subjected to static stress (circles) for 25000s was included as well for comparison. As shown in Fig. 6.4, less $|\Delta V_{th}|$ was observed for unipolar stress, due to the recovery during relaxation periods. The recovery of NBTI-induced $|\Delta V_{th}|$ was claimed due to the back diffusion of hydrogen species and subsequent passivation of Si dangling bonds [59, 60]. As a consequence of symmetric diffusion and back-diffusion of hydrogen species, $|\Delta V_{th}|$ after certain period of ac stress should be constant, independent of stress frequency [60].

However as shown in Fig. 6.4, as stress frequency is increased from 1 Hz (solid squares) to 1M Hz (solid triangles), less $|\Delta V_{th}|$ is monitored at a given clock time. This trend is more clearly shown in Fig. 6.5, where $|\Delta V_{th}|$ after 50000s unipolar ac stress is plotted as a function of stress frequency. An inverse power-law dependence is evident: $|\Delta V_{th}| \sim f^{-\gamma}$, with $\gamma \sim 0.045$.

Fig. 6.5 Unipolar ac stress induced threshold voltage shift, after 50000s ac stress time, of RTN gate p-MOSFET of $[N] \sim 1.1$ at. %, as a function of frequency. Stress condition is the same as in Fig. 6.4.

Similarly, an inverse power-law frequency dependence is also observed for p-MOSFETs with DPN gate dielectric. The solid squares in Fig. 6.6 denote $|\Delta V_{th}|$ of DPN p-MOSFET ($[N] \sim 6.3$ at. %) after 50000s unipolar ac stress, as a function of stress frequency. $|\Delta V_{th}| \sim f^{-\gamma}$ is obtained, with $\gamma \sim 0.015$. Furthermore, the frequency dependence of $|\Delta V_{th}|$ after 1000s unipolar ac stress (open triangles) and $|\Delta V_{th}|$ after 30000s unipolar ac stress (open squares) are also included. Constant $\gamma \sim 0.015$ is obtained, regardless of stress time.

Fig. 6.6 Frequency dependence of the $|\Delta V_{th}|$ of DPN p-MOSFET of $[N] \sim 6.3$ at. % subjected to unipolar ac stress, as a function of stress time. $V_g^s = -2V$; $V_g^r = 0$; duty cycle: 50%. Constant γ is observed at different stress time.

6.4 Impact of Nitrogen on Unipolar NBTI

According to the simulation based on the conventional R-D model, the transport of hydrogen species during ac NBTI stress should result in no frequency dependence of $|\Delta V_{th}|$ [60]. However, an inverse power-law frequency dependence was observed for oxynitrided gate p-MOSFETs. As discussed in the last few chapters, nitrogen introduces a novel temperature-insensitive NBTI mechanism to modern nano-scale p-MOSFETs. The observed frequency dependence may be related to nitrogen in the gate dielectrics. Thus, impact of nitrogen in the gate dielectrics on the frequency dependence of $|\Delta V_{th}|$ was investigated.

Identical unipolar ac stress was applied on DPN nitrided gate p-MOSFETs with

different $[N]$ at the gate-SiO₂ interface. Fig. 6.7 shows $|\Delta V_{th}|$ of DPN gate p-MOSFETs after 50000s unipolar stress, as a function of frequency. Larger $|\Delta V_{th}|$ is resulted for the p-MOSFET of $[N] \sim 13$ at. %. Furthermore, inverse power-law frequency dependence, i.e. $|\Delta V_{th}| \sim f^{-\gamma}$, is evident for both types of DPN gate p-MOSFET of $[N] \sim 6.3$ at. % and 13 at. %. However, the p-MOSFET with a higher $[N]$ exhibits a smaller exponent γ . The exponent γ of 13 at. % RTN gate p-MOSFET is ~ 3 times smaller than that of the 6.3 at. % device. The resultant greater relative increase in $|\Delta V_{th}|$ of the 13 at. % RTN p-MOSFET at high frequency has serious implication for circuit-level reliability.

Fig. 6.7 Unipolar NBTI induced threshold voltage shift, after 50000s ac stress time, of p-MOSFETs having DPN nitrided gate dielectric, as a function of frequency. Stress cycle: $V_g^s = -2V$; relaxation cycle: $V_g^r = 0$; pulse transition time: 50 ns; duty cycle: 50%.

A recent work [96] suggested that the profile of nitrogen in the gate oxide could affect post-stress $|\Delta V_{th}|$ recovery. In the framework of the R-D model, it was proposed that

nitrogen at the gate-SiO₂ interface trapped hydrogen species released from the dissociation of Si-H bonds. Thus the back diffusion of hydrogen species was inhibited and the passivation of Si-SiO₂ interface traps during relaxation was limited. This implies that $|\Delta V_{th}|$ recovery may be suppressed for the 13 at. % DPN p-MOSFET. As a result, the frequency dependence of $|\Delta V_{th}|$ is reduced for 13 at. % DPN p-MOSFET. To address the possible influence of nitrogen profile, the same unipolar ac stress was carried out on the RTN p-MOSFET. The dependence of $|\Delta V_{th}|$ on the stress frequency is depicted in Fig. 6.8.

Fig. 6.8 Unipolar NBTI induced threshold voltage shift, after 50000s ac stress time, of p-MOSFETs having RTN nitrided gate dielectric, as a function of frequency. Stress cycle: $V_g^s = -2.6V$; relaxation cycle: $V_g^r = 0$; pulse transition time: 50 ns; duty cycle: 50%.

A similar reduction in the exponent γ is evident for the 4.2 at. % RTN p-MOSFET, as compared to that of the 1.1 at. % RTN p-MOSFET. This observation implies that nitrogen profile is not the key factor determining the reduced frequency dependence

of $|\Delta V_{th}|$ of the 13 at. % DPN p-MOSFET. Nevertheless, the results clearly show that the frequency dependence of unipolar NBTI induced $|\Delta V_{th}|$ generally becomes weaker for more heavily nitrided gate p-MOSFETs.

Fig. 6.9 more clearly illustrates the impact of nitrogen concentration on the recovery of $|\Delta V_{th}|$. The $|\Delta V_{th}|$ after 50000s unipolar ac stress ($|\Delta V_{th}|_{AC}$) was divided by the $|\Delta V_{th}|$ after 25000s static stress ($|\Delta V_{th}|_{DC}$). Resultant fraction $\alpha = |\Delta V_{th}|_{AC}/|\Delta V_{th}|_{DC}$ was plotted as a function of gate stress frequency in Fig. 6.9. For more heavily nitrided devices, either DPN gate p-MOSFETs or RTN gate p-MOSFETs, a larger fraction of $|\Delta V_{th}|$ remains unrecovered at high frequency ac stress. Therefore, nitrogen seems to lock-in more $|\Delta V_{th}|$ in more heavily nitride p-MOSFETs at high frequencies.

Fig. 6.9 Fraction of threshold voltage shift after 50000s unipolar ac stress $|\Delta V_{th}|_{AC}$, divided by threshold voltage shift after 25000s static stress $|\Delta V_{th}|_{DC}$, α , i.e. $\alpha = |\Delta V_{th}|_{AC}/|\Delta V_{th}|_{DC}$. Unipolar stress conditions are the same as in Fig. 6.7 and 6.8. Stress voltage of static stress is the same as that of unipolar stress.

6.5 Role of Deep-Level Hole Traps

As discussed in the last section, after identical period of unipolar ac stress, more $|\Delta V_{th}|$ remains unrecovered at high frequency ac stress for p-MOSFETs having more heavily nitrated gate dielectrics. This phenomenon coincides with the previous observation that nitrogen introduces deep-level interfacial imperfections, which are relatively resistant to post-stress recovery. Thus, the role of deep-level hole traps during dynamic NBTI stress was investigated.

Fig. 6.10 Threshold voltage shift versus NBTI induced interface trap density ΔN_{it}^{cp} correlations. Unipolar stress conditions: $V_g^s = -2.6\text{V}$; $V_g^r = 0$. Bipolar stress conditions: $V_g^s = -2.6\text{V}$; $V_g^r = 1.5\text{V}$ (2.5V) for the 1.1 at. % (4.2 at. %) RTN gate p-MOSFET. Gate stress frequency = 1M Hz; total stress time: 50000s.

As discussed in section 3.5 of Chapter 3, the extent of deep-level hole trap generation may be investigated through comparing the $|\Delta V_{th}|$ vs. ΔN_{it}^{cp} correlation plot of unipolar ac stress to that of the static or bipolar ac stress. Fig. 6.10 shows the $|\Delta V_{th}|$ vs. ΔN_{it} correlations of unipolar and bipolar ac stress. Under bipolar stress, the positive gate

voltage lowers the energy states of deep-level hole traps below the conduction band of Si during the relaxation cycle, resulting in them being compensated by the tunneling electrons (Fig. 3.13 (c)). The resultant $|\Delta V_{th}|$ is due mainly to the interface traps, i.e. $|\Delta V_{th}| \sim |\Delta V_{th}|_{IT} = q\Delta N_{it}^{cp}/C_{ox}$ for bipolar stress. Since the EOT for RTN p-MOSFETs is constant, the $|\Delta V_{th}|$ vs. ΔN_{it}^{cp} plots for the 1.1 at. % and 4.2 at. % RTN p-MOSFETs fall on the same curve. $|\Delta V_{th}|$ of bipolar stress is larger than the theoretical value because at the given temperature (373K), the CP method only probes $\sim 33\text{-}45\%$ of the Si bandgap (section 3.4). Donor-like interface traps of energy states in the upper half of the Si bandgap are not probed by the CP method, but they contribute to $|\Delta V_{th}|$ (section 3.4). For a given ΔN_{it}^{cp} , the difference between $|\Delta V_{th}|$ of unipolar and bipolar stress indicates the extent of deep-level hole trap generation. As shown in Fig. 6.10, besides a greater generation of interface traps, increased deep-level hole trapping is evident in the 4.2 at. % RTN p-MOSFET. Thus, more deep-level hole traps remain charged when the 4.2 at. % RTN p-MOSFET is subjected to 1M Hz unipolar ac stress, which explains the larger difference at high frequency between 1.1 at. % and 4.2 at. % RTN p-MOSFETs in Fig. 6.8.

In Fig. 6.11, the component of $|\Delta V_{th}|$ due to interface traps $|\Delta V_{th}|_{IT}$, and the component due to deep-level hole traps $|\Delta V_{th}|_{DLHT}$ ($= |\Delta V_{th}| - |\Delta V_{th}|_{IT}$), are separated. The frequency dependence of the two components are examined. For the 4.2 at. % RTN p-MOSFET, $|\Delta V_{th}|_{DLHT}$ is $\sim 2.5\times$ larger than that of the 1.1 at. % device, while $|\Delta V_{th}|_{IT}$ is $\sim 1.5\times$ larger. A substantial contribution to the increased $|\Delta V_{th}|$ of the 4.2 at. % RTN p-MOSFET thus stems

from an increased generation of deep-level hole traps. The nearly parallel lines in Fig. 6.11 imply that increased $[N]$ in the gate dielectrics does not significantly affect the intrinsic frequency dependence of $|\Delta V_{th}|_{DLHT}$ and $|\Delta V_{th}|_{IT}$. Thus, the above observations suggest the reduced frequency dependence of the overall $|\Delta V_{th}|$ observed in Fig. 6.7 and 6.8 is not a consequence of a fundamental change in the trap generation mechanism. It is mainly due to an increased generation of recovery-resistant deep-level hole traps in the more heavily nitride p-MOSFET.

Fig. 6.11 (a) Threshold voltage shift due to deep-level hole traps, $|\Delta V_{th}|_{DLHT}$ ($= |\Delta V_{th}| - |\Delta V_{th}|_{IT}$) as a function of frequency. (b) Threshold voltage shift due mainly to interface traps, $|\Delta V_{th}|_{IT}$. $T = 373K$.

As proposed in section 3.6, deep-level hole traps are generated via electron tunneling from nitrogen-related trap precursors to the conduction band of Si substrate.

According to the tunneling front model [97], the electron tunneling time constant for an electron to tunnel from a neutral trap precursor situated at a distance x from the Si-SiO₂ interface to the Si conduction band is expressed by

$$t = t_0 \exp(2\beta x) \quad (6.5-1)$$

where $\beta = \sqrt{\frac{2m_t^*}{\hbar^2} E_t}$ when no gate bias is applied; t_0 (on the order of 10^{-13} s) is related to the fundamental transition rate of electrons to the closest traps at the interface; m_t^* is the tunneling effective mass; E_t is the barrier height, i.e. the hole trap energy state with respect to the top of the SiO₂ valence band. For electrons facing a tunneling barrier ~ 3 eV, β is found to be $\sim 5.62 \text{ nm}^{-1}$. Thus for $x=0.5 \text{ nm}$, t is found to be in the order of 10^{-11} s. This first order calculation implies that generation of deep-level hole traps may occur spontaneously during the negative stress cycle even at a very high gate frequency. The trap energy states are situated above the conduction band of Si, i.e. outside the window of direct electron tunneling between Si and gate. Once generated, they do not readily relax so long as the gate voltage is maintained at zero or in the negative regime.

6.6 Summary

Dynamic NBTI of the ultra-thin oxynitride gate p-MOSFET is investigated. Inverse power-law frequency dependence of NBTI-induced threshold voltage shift was observed for oxynitride gate p-MOSFETs subjected to unipolar ac stress, i.e. less threshold voltage shift was monitored for unipolar stress at higher gate frequency. Furthermore, increased nitrogen concentration in the gate dielectrics is shown to result

in a much weaker dependence of threshold voltage shift on the gate frequency. Evidence shows that the generation of recovery-resistant deep-level hole traps is increased in a heavily nitrated p-MOSFET. As a consequence, larger threshold voltage shift was caused for more heavily nitrated p-MOSFETs. The fast generation process and stagedic energy states make the contribution from deep-level hole traps become more important at high gate frequency. The significant role of deep-level hole traps during dynamic NBTI has important indication for high frequency circuit level reliability.

Chapter 7 Conclusion

7.1 Conclusion

A detailed study of negative bias temperature instability (NBTI) induced degradation of ultra-thin oxynitride gate p-MOSFETs was presented in this thesis. The focus is on the physical mechanisms of NBTI and the impacts of gate material and stress conditions on NBTI. This research provided a more comprehensive understanding of NBTI stress induced interfacial imperfections and degradation mechanisms of modern ultra-thin oxynitride gate p-MOSFETs. A consistent deep-level hole trapping model for NBTI was presented. A novel nitrogen-related temperature-insensitive NBTI mechanism was revealed to superpose on the classic NBTI mechanism responsible for the degradation of conventional SiO₂ gate p-MOSFETs, thus resulting in severer degradation of oxynitride gate p-MOSFETs. Besides, the significant role of nitrogen in static and dynamic NBTI was studied and presented in this thesis.

From an objective and systematic analysis of DC I_d - V_g data, it is revealed that besides the interface traps of energy states in the lower-half of the Si bandgap, trap states are found in the upper half and above the E_C of Si. These trap states in the upper half and beyond E_C (i.e. deep-level hole traps) manifest themselves as positive oxide trapped charge since they are outside the window of direct electron tunneling. The strategic energy states ensures deep-level hole traps exhibit significant role in static and

dynamic NBTI stressing. Furthermore, distinct relaxation characteristics under positive gate biasing suggest a fundamental difference in the origins of interface traps and deep-level hole traps. When the p-MOSFET is subjected to positive gate bias, density of interface traps is relatively unchanged but that of deep-level hole traps is significantly decreased. The characteristics of deep-level hole traps imply that these trap states arise from the trapping of holes.

A non-Arrhenius behavior of NBTI induced threshold voltage shift further suggests the presence of more than one defect generation mechanism. A novel temperature-insensitive NBTI mechanism of $E_a \sim 0.02$ eV was observed to superpose on the classic temperature-sensitive hydrogen diffusion mechanism of $E_a \sim 0.25$ eV, resulting in severer degradation of oxynitride gate p-MOSFETs. Deep-level hole traps and part of interface traps may be generated via this temperature-insensitive mechanism. Since significant enhancement of the temperature-insensitive mechanism was monitored in more heavily nitrided p-MOSFETs, it is linked to nitrogen-related hole trapping process. Time evolution of the temperature-insensitive mechanism was studied subsequently. In contrast to the gradual accumulation of interface traps generated by the classic NBTI mechanism ($\sim t^{0.25}$), degradation due to the temperature-insensitive mechanism exhibits much weaker time dependence ($\sim t^{0.1}$), which may result from the spontaneous generation of positive trap charge via electron tunneling under negative oxide field. Portion of the temperature-insensitive mechanism induced degradation is recovered under dynamic stress. However, the

remaining component yet provides comparable contribution to that of the classic NBTI mechanism.

Dynamic NBTI of ultra-thin oxynitride gate p-MOSFET is investigated, as unipolar ac stress induced degradation has direct impact on circuit-level reliability. Inverse power-law frequency dependence implies less NBTI induced threshold voltage shift may be resulted at high frequency ac stress. However, increased nitrogen concentration in the gate dielectrics results in a much weaker dependence of threshold voltage shift on the gate frequency. This phenomenon was due to an increased generation of recovery-resistant deep-level hole traps in a heavily nitrated p-MOSFETs. Nitrogen-related trap precursors lock-in more deep-level positive trap charge, leading to larger threshold voltage shift of heavily nitrated p-MOSFETs at high frequency.

7.2 Recommendations for Future Work

Negative bias temperature instability was one of the most critical reliability issues for CMOS circuits, especially for new generation p-MOSFETs with channel length smaller than 150 nm. As presented in this thesis, a novel temperature-insensitive hole trapping mechanism is introduced by nitrogen incorporated into the gate dielectrics and results in severer NBTI induced degradation of oxynitride gate p-MOSFETs. But the origin of nitrogen-related trap precursors is not very clear. More indepth physical/chemical experiments would make the theory more complete. Deep-level

hole trap of high energy state beyond the conduction band of Si plays a significant role in NBTI problems. Besides oxynitride gate dielectrics, other types of high-k dielectrics such as $H_fO_xN_y$ etc. are widely investigated recently. These gate dielectric candidates nowadays still in experimental stage may become the new generation gate materials one day. It is necessary to extend the studies presented in this thesis to these new materials. Since defect precursors of energy states beyond the conduction band of Si were reported for high-k materials [99], the contribution from deep-level hole traps may remain important.

Deep-level hole trapping theory was proposed in the thesis and lots of experimental results were provided to support this theory. However, direct evidence is yet required to make the generation process of deep-level hole traps clearer. A possible solution is atomic level simulation of the transformation from nitrogen-related trap precursor to positive trap charge. Since the chemical and physical background to do such simulation is not ready yet, this task may be suggested for future researchers.

Weaker dependence of NBTI-induced threshold voltage shift on gate stress frequency was reported for devices with more nitrogen in the gate dielectric. However, the origin of the inverse power-law dependence is not clear, although the observation is consistent with deep-level hole trapping theory. A study of the time dependence of NBTI-induced threshold voltage shift during the stress period at AC NBTI stress and the time dependence of post-stress recovery of threshold voltage shift may explain the

observed frequency dependence. Due to the limited equipment capability, this study was not done in this project, but it is recommended as future work.

The channel length of the p-MOSFETs tested in this thesis is in the range of 100nm ~ 130 nm. But new generation of p-MOSFETs have further smaller dimensions below 65 nm. As the devices further scales down, secondary effects such as physical stress applied on the channel occur due to the drain/source terminal engineering [100] or the employment of etch stop layer during fabrication [101]. These secondary effects may invite new problems or mechanisms to NBTI induced degradation. It is of interest to perform further study about these potential new issues and complementary current understanding of NBTI problems.

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