Multi-objective optimization for smaller, efficient and better performed design of buck-boost converters

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Multi-objective Optimization for Smaller, Efficient and Better Performed Design of Buck-boost Converters

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Master of Engineering

2021

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

03/01/2021
Date

Huang Xianmiao *Huang Xianmiao*

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

01/01/2021
Date

Hung Dinh Nguyen

A handwritten signature in blue ink, consisting of a stylized 'H' followed by a cursive 'D' and 'N'.

Authorship Attribution Statement

This thesis contains material from one paper(s) published in the following peer-reviewed journal(s) / from papers accepted at conferences in which I am listed as an author.

Chapter 1, chapter 2, chapter 3 and chapter 4 in part 2 is published as X. Huang, X. Zhang, and X. Li, "Multi-objective Optimization for Smaller, Efficient and Better Performed Design of Buck-boost Converters," in *2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2020, vol. 7, no. 2, pp. 266–269, doi: 10.1109/pedg48541.2020.9244342.

The contributions of the co-authors are as follows:

- Prof X. Zhang provided the initial project direction and allocated different roles of co-authors.
- I co-worked with Dr. X. Li to solve the problems in the NSGA-II programming code. And I co-analyzed OPAL-RT results with him.
- I carried out the preparation of three objectives in the early stage and modified the programming to get the Pareto frontier.
- I analyzed the results from NSGA-II and dealt with the figures for analysis.
- All the simulation results, including case analysis, was conducted by me in the Clean Energy Research Lab, Nanyang Technological University.

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Date

Huang Xianmiao

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Summary

Converters are essential components in DC-DC transformation and each objective of a converter plays an important role in the transformation. However, in most cases, improving one objective means sacrifices the others. As a result, the overall performance of the converters is not satisfied. The thesis proposes a method to optimized volume, efficiency, and cut-off frequency of LC-filter in buck-boost converter with full consideration of keeping three objectives on optimal conditions compared to the existed method. The Multi-objective optimization is for building a more portable, highly efficient, and better performance converter. For avoiding the interference of improving each objective and for obtaining optimal solutions with a fast process and better convergence, the author applies Non-dominated Sorting Genetic Algorithm-II to generate a Pareto frontier which could provide researchers a visualized figure to select the cases based on their demands. The multi-objective optimization results are compared with single-objective optimization results to verify the feasibility of the project.

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Chapter 1. Introduction

1.1 Motivation

Though single criteria of the converters have been improved by efforts of researchers, it met many difficulties to transfer novel converter models to industry productivity. The overall performance of converters has not seen significant improvement because, in many cases, improving one criterion means sacrificing the others. For instance, to controlling the ripples, inductance, and capacitance with a big value are likely to be taken, which means the volume of the LC-filter has to be increased. In this example, improving the filtering performance means sacrificing the portability of the converters. As a result, multi-objective optimization is applied in the author's research for considering all the objectives at the same time. The motivation is to take three criteria into account to design converters with outstanding overall performance.

1.2 Objectives

The major objective is to get the set of multi-objective solutions, the Pareto frontier with three criteria. By this frontier, the designers could select the optimal solutions by their demands and the author also could obtain the single-objective optimization solutions to do the analysis in the following parts.

In recent years, researchers have focused on the multi-objective optimization of Power Electronics[1][2]. However, not enough works have been done yet in this area. There are two important parts of the multi-objective optimization when researchers plan to start the study. The first section is figuring out the objectives supposed to be optimized. In the thesis, the author optimizes three objectives which are the volume of LC-filter, efficiency, and cut-off frequency for designing smaller, more efficient, and better performed buck-boost converters[3]. For converters designs, smaller and efficient means more portable and energy saving while applying in home appliances. Moreover, a low cut-off frequency is also important for the converter to control the ripples. The second part is to select the algorithm based on their different features to start the optimization. In traditional designs, multi-objective evolutionary algorithms using a non-dominated sorting and sharing parameters usually be applied, which always be criticized with computational complexity, non-elitism approach, and acquiring specific sharing parameters. However, the author applied a fast and elitist non-dominated sorting

genetic algorithm that can apply an all-around spread of solutions, lesser computational complexity and better convergence near the true Pareto-optimal frontier[4].

1.3 The major contribution of the Thesis

The Pareto frontier in the thesis shows different improving directions compared with conventional design while reflecting the trade-off relationships of different criteria. Two types of Pareto frontiers will be generated in the following parts. The first one is the curve with three dimensions and each dimension represents one objective. In this figure, the users could obtain the overall spread of optimal designs of the converters. The second type of Pareto frontiers is three two-dimension figures. The direct contribution is that the Pareto figures could provide users more visualized relations between two objectives. Under this circumstance, the users can select the optimal solutions based on their productive demands by this visualized and better converged Pareto frontier.

Moreover, another contribution is that the comparison between the results of single-objective optimization and multi-objective optimization will be made. By this analysis, the designers have more choice to select the solutions based on their demands.

1.4 Organization of the Thesis

The thesis will be divided into three major parts which are the introduction, actual work is done, and conclusion and recommendations. The introduction, including four chapters which are motivation, objective, the major contribution of the thesis, and organization of the Thesis. The second part is divided into five chapters, including a literature survey, a preliminary of the proposed three objectives supported for multi-objective optimization, select qualified cases by Pareto frontier, experimental results, and results comparisons with single-objective optimization. Literature survey presents the background of power electronics including the classification of four types of power electronics, power electronic applications as well as the improvement made by the researchers. The second chapter could be understood as the preparation of multi-objective optimization. The author conducts equations of LC-filter's volume, total power loss in the buck-boost circuit as well as cut-off frequency by buck-boost equivalent circuit analyzing and mathematical derivation. Additionally, all those objectives are expressed by two variables which are inductance and capacitance for LC-

filter design. The next chapter presents the procedures of a non-dominated sorting genetic algorithm as well as the figure of optimal solutions, the Pareto frontier. The author selects three cases showing different improving directions of the conventional method and the trade-off relationships of different criteria. Chapter 4 is about the experimental results of those three cases to verify the accuracy of the optimization applied by a non-dominated sorting genetic algorithm and the feasibility of this buck-boost design. The last chapter is about the comparison between the multi-objective results and single-objective results. In the end, the conclusion and recommendation are to summarize the thesis, figure out the weakness, and then draw up a plan to move this project forward.

Chapter 2. Actual Work Done

2.1 Literature survey

With power electronic devices widely used in many fields, from grid integration of clean energy sources to phone chargers, they have already played important roles in modern human lives. Power electronic converters, the essential components in power electronic devices, are used to convert input voltage and frequency to output voltage and frequency. There are four types of power electronic converters differed from their functions, which are DC-AC inverters, AC-DC rectifiers, AC-AC converters, and DC-DC converters.

DC-AC inverters could provide AC power supply by converting DC voltage, which is widely applied in industries. For example, a 6-switched 3-level inverter is preferred to use in the micro-hybrid system for smart grid integration[5] and the pulse-width-modulated voltage-source inverters are applied for voltage regulation[6]. Meanwhile, inverters are usually combined with an AC-DC rectifier to supply uninterruptible power for protecting critical loads and handling disturbances in hospitals, data centers, and water fabs[7]-[8]. In this case, the AC-DC rectifiers are applied for converting AC power from power systems to DC power which will act as the input of the DC-AC inverters. DC-AC rectifiers are also commonly applied in industries, especially in consumer electronics and home appliances. In those cases, rectifiers are usually combined with buck converters which could step down the voltage outputted by rectifiers for charging consumers' electronics[9]. Typically, Rectifiers could be divided into passive rectifiers which are using diodes and active rectifiers built with semiconductor devices. The latter is controllable but more expensive. Furthermore, the third type of power electronic converters is AC-AC converters consist of cyclo-converters and matrix converters which are commonly used for wind power generation[10].

DC-DC converters are as important as others. Based on different features, converters are divided into many types, for example, buck converters for stepping down voltage[11], boost converters for stepping up[12]. Switched-mode electronic method is mostly used to implement DC-DC converters for compact size and less power loss. When applied in industries, many features are desired to value DC-DC converters such as regulated output, electrical isolation, multiple outputs, high efficiency, and compact design. Many researchers focus on how to improve the performance of converters in

those areas. For example, In[13], a high step-up switched-capacitor converter is proposed for regulated output voltage; In[14], The researchers provided a high-efficiency-isolated single-input multiple-output bidirectional converter for power storage system; In[15], for interfacing storage in a range of applications, the researchers proposed a novel bidirectional DC-DC converters with high voltage gain and high efficiency; In[16], novel power inductor embedded in silicon was applied to minimize the volume of the converter.

Countless criteria could be set as objectives in the optimization. However, improving one criterion means sacrificing the others. Under this circumstance, it's necessary to put multi-objective optimization into converter optimization. Some paper have already applied it, for instance, the researchers optimize efficiency, reliability, and cost-saving of the converter together in[17]. Similarly, cut-off frequency, lifetime of the capacitor, and total volume of the LC filter were set to be the objectives in the experiment[18]. By applying multi-objective optimization, researchers are able to obtain the designs of converters with overall improvements.

Multi-objective optimization is combined with the development of programming methods. An overview of genetic algorithm was published in1993[19] and it was also in 1990's, particle swarm optimization, genetic algorithm and simulated annealing have been applied in MATLAB. Particle swarm optimization and genetic algorithm are two typical programming methods in objectives optimization. The major difference between these two algorithms is the different optimized mechanisms. In particle swarm optimization, each particle is guided by the local-best position in the searching space. An advanced particle swarm optimization which could be used in many-objective optimization has been proposed in [20]. However, each candidate is sorted and selected as natural selection in genetic algorithm. Moreover, many other kinds of algorithms were applied in power electronics optimization. As an example, multi-level DC-DC converters have been optimized by geometric programming for using fast, powerful solvers that guarantee global optimality of solutions in[21]; The immune algorithm has been applied in[22]. In general, the practicality of an algorithm could be measured in two major aspects, which are computational complexity and time to get satisfied convergence.

2.2 Preliminary of the proposed three objectives supported for multi-

objective optimization

2.2.1 Express three objectives by inductance and capacitance

Buck-boost converter is the object be optimized in this research. Compared with buck converters and boost converters, buck-boost converters can either step up or step down the input voltage by controlling duty circles, which is more flexible for use. Buck-boost converters could work in three conditions that differs from the minimum value of inductor current, which are continuous conductor mode (CCM), boundary conductor mode (BCM), and discontinues conductor mode (DCM). Because in general, the current ripples are supposed to be controlled below 30% of the average inductor current to reduce the current stress to the inductor and semiconductor devices, the author operates a CCM buck-boost converter in this project.

In the author's project, the volume of LC-filters, efficiency, and cut-off frequency are the three objectives. The goal of this part is to express those objectives by only two variables, inductance, and capacitance. In this way, each pair of inductance and capacitance represents a unique match of three objectives. Moreover, inductance and capacitance also act as variables of the non-dominated sorting algorithm which finally generate the Pareto frontier with three objectives as criteria. For achieving that, the author has to input the prepared equations of three objectives as subfiles in programming.

2.2.2 Volume calculation of LC-filter

The first object is the volume of LC-filter and in this part. LC-filter built up by an inductor and capacitor is for picking out a signal with particular frequency from a more complex signal by filtering unwanted disturbances.

Due to the filtering ability, LC-filters are generally divided into four types, low-pass filter, high-pass filter, bandpass filter, and band-stop filter. In mathematical calculation, it usually treated as an idealized model since it assumes there is no dissipation energy due to resistance. However, in this project, the resistance of the inductor and capacitor cannot be ignored because power loss is one of the objectives to be optimized and efficiency is a key factor in industrialized productivity.

The volume of LC-filter directly determines the compact design of the whole converter. Converters are usually applied to build home appliances where portability is a key

advantage to attracting consumers. Under this circumstance, smaller LC-filters are demanded.

Fig. 1 Basic LC-filter.

In this report, the volume of LC-filter is treated as a combination of inductor volume of capacitor volume in the equation below.

$$V = V_L + V_C \quad (1)$$

The volumes of capacitor and inductor are expressed in formula (2) and formula (3), and graphically shown in Fig.2 below. Although the length of the capacitor is not always constant, it still gives the insight of linearity.

Fig. 2 Capacitor and Inductor.

$$V_C = \left(\frac{D}{2}\right)^2 \cdot \pi \cdot h \quad (2)$$

$$V_L = \left(\frac{OD^2 - ID^2}{4}\right) \cdot \pi \cdot H \quad (3)$$

In this report, the author applies Aluminum Electrolytic Capacitors (Radial Lead Type). Through the parameters provided in 50V working condition, the relationship between capacitor volume and capacitance is obtained in formula (4) by generating a linear fitting curve.

$$V_C = 5.035e^{-3}C + 1.533e^{-7} \quad (4)$$

MCAP series inductor is used in this project. As for the toroidal inductor graphically shown in the Fig. 2, the author obtains the linear relationship between inductor volume and inductance shown in formula (5):

$$V_L = 3.892e^{-2}L + 2.643e^{-7} \quad (5)$$

The relationship between the volume of LC-filter and two variables has been acquired in this part. Moreover, the parameters of Aluminum Electrolytic Capacitors and MCAP Series Inductor could also be used to generate the relationship between the inductor resistance and the inductance, capacitor resistance, and the capacitance, which could not be ignored in this project. Moreover, the inductor resistance, R_L , and capacitor resistance R_C are brought into the calculation of total power loss of the buck-boost converter.

2.2.3 Efficiency calculation

The second objective is efficiency which means low power loss. Power loss is easy to be ignored when converters are treated as idealized models. However, to realize the power loss of a synchronous converter and to improve efficiency is important for designers. It is an essential part to be minimized while applying in industries as more power loss means consuming more electricity.

There are many types of power loss while operating buck-boost converters including conduction loss, driving loss, copper loss, switching loss, capacitor loss, and core loss. Conduction loss, copper loss, and capacitor loss are the power lost by the resistance of semiconductors, inductor, and capacitor. In this report, semiconductors are a MOSFET and a diode. Obtaining those three types of power loss acquires buck-boost equivalent circuit analysing and mathematical derivation. Driving loss and switching loss related to the internal structure of MOSFET and diode. Additionally, core loss is subjected to the changing magnetic field in the inductor, dissipated as heat and sometimes as noise.

In this part, the author manages to obtain the equation of the total power loss by acquiring each type of loss. Moreover, the power losses are expressed by two variables, inductance, and capacitance as well for the following optimization.

(A) Conduction loss

Conduction loss is related to the current flowing through the resistance of semiconductors. Fig. 3 is the equivalent circuit of the buck-boost converter and i_T as well as i_D flow through MOSFET and diode respectively. It is clear that the key to calculate conduction loss is to analyse the state of i_T and i_L . In continuous conduction mode, the current state of i_T and i_L are presented below.

Fig. 3 Equivalent circuit of the buck-boost converter.

Fig. 4 Conduction current of MOSFET and Diode.

As shown in Fig.4, i_T and i_D conduct complementary in a whole period. Moreover, from the basic buck-boost circuit analyzing, the slopes of i_T and i_D are presented in this figure. Meanwhile, i_L is the combination of i_T and i_D in a whole period. Based on the basic buck-boost analysis, the author obtains the relationship of the averaged inductor current, input current and output current presented in formula (6) below, which is the key to derive the mathematical expression of i_T and i_D .

$$I_L = I_{in} + I_o \quad (6)$$

And then, the conduction loss could be calculated as:

$$P_{on} = \frac{1}{T} \left(\int_0^{DT} i_T^2 \cdot R_{on} dt + \int_{DT}^T i_D^2 \cdot R_{diode} dt \right) \quad (7)$$

The final mathematical expression of conduction power loss with two variables is obtained below in formula (8).

$$P_{on} = \left[\frac{DI_o^2}{(1-D)^2} + \frac{D(1-D)^2 V_o^2}{12L^2 f^2} \right] \cdot R_{on} + \left[\frac{I_o^2}{1-D} - \frac{(1-D)^3 V_o^2}{12L^2 f^2} \right] \cdot R_{diode} \quad (8)$$

D is the duty circle.

R_{on} is MOSFET resistance.

R_{diode} is diode resistance which is assigned a small value. The whole conduction loss takes a very low percentage of the total power loss. Under this circumstance, the calculation of conduction loss is simplified and the threshold voltage of the diode is ignored in this report.

(B) Copper loss

Copper loss is caused by the thermal effect of the inductor resistance. In general, the inductor is regarded as an idealized model without power loss. However, inductor resistance is supposed to be considered in the total power loss in buck-boost optimization.

The first step is to understand the state of the inductor current. Through analysing buck-boost equivalent circuit in Fig.5, the inductor current waveform is presented below.

Fig. 5 Conduction current of the inductor.

The next step is to obtain the inductor resistance. Inductor resistance is not regarded as a constant in this project. The author needs the inductor resistance formula expressed by inductance which is one of the variables in optimization. Data is

gathered from the MCAP series inductor. From the relationship between those single spots of inductance and resistance, the author obtained the formula of inductor resistance by fitting the linear curve. The equation is provided in formula (9).

$$R_L = 102.4L + 0.023 \quad (9)$$

The final step is to derivate the formula of copper loss.

$$P_{Cu} = \left[\int_0^{DT} i_L^2 dt + \int_{DT}^T i_L^2 dt \right] \cdot \frac{R_L}{T} \quad (10)$$

The final expression of copper loss is obtained in formula (11) below.

$$P_{Cu} = \left[\frac{I_o^2}{(1-D)^2} + \frac{(1-D)^2 V_o^2}{12L^2 f^2} \right] \cdot R_L \quad (11)$$

R_L is inductor resistance.

(C) Capacitor loss

Capacitor loss is resulted by the thermal effect of capacitor resistance. Capacitor resistance is usually ignored in calculation as well. But it plays an important role in total power loss. If capacitor loss is not counted, the researchers may encounter nonnegligible err in the programming analysing.

For obtaining capacitor loss, the author needs to figure out which current flows through capacitor resistance based on the timing in one period.

From Fig. 3, while MOSFET is conducting, the current generated by input voltage cannot supply the capacitor and the output. In this period, the remaining charge of the capacitor supplies the output, and i_C is in the positive direction from Fig. 3. However, the inductor current cannot step up or step down immediately while the MOSFET is switched off. When the MOSFET is in off-state, the input voltage cannot supply the buck-boost circuit. But the inductor current remains flowing in a dropping state as shown in Fig. to supply the capacitor and the output.

The state of current flowing through the capacitor resistance is provided below in Fig.6.

Fig. 6 Conduction current of the capacitor.

The next step is to obtain the formula of capacitor resistance expressed by capacitance. For gathering data from Aluminum Electrolytic Capacitors (Radial Lead Type), the author acquires the relationship between resistance and capacitance, which is provided below.

$$R_c = \frac{\tan \delta}{2\pi fC} \quad (12)$$

$\tan \delta$ is the parameter depending on the voltage putting on the capacitor. In this report, the output voltage is 50V and the corresponding $\tan \delta$ is 0.1.

The final step is to derivate the formula of Capacitor loss.

$$P_c = \frac{R_c}{T} \left(I_o^2 \cdot DT + \int_{DT}^T i_c^2 dt \right) \quad (13)$$

The final equation of capacitor loss is presented in formula (14) below.

$$P_c = \left[\frac{(2-D)I_o^2}{(1-D)} + \frac{(1-D)^3 V_o^2}{12L^2 f^2} \right] \cdot R_c \quad (14)$$

R_c is the capacitor resistance.

(D) Switching loss

Switching loss is caused by switching on and off of the MOSFET. In this project, the switching frequency is 10^4 Hz means that the MOSFET switches on and off 10^4 in one second. Under this circumstance, switching loss cannot be ignored.

For achieving the formula of switching loss, the first step is to understand the conducting features of MOSFET. From Fig.7, the switching on procedure of

MOSFET is provided and in this report, the author assumes the switching off procedure is the reversion of the switching on procedure.

Fig. 7 Switching on period of MOSFET.

The next step is to analyze switching on period. At the switching moment, the volume of V_{DS} is the sum of V_{in} and V_o . I_{DS} is the minimum value of I_L . As a result, the switching-on loss could be expressed by formula (15).

$$P_{switchingon} = \frac{f \cdot (V_{in} + V_o) \cdot (t_{ri} + t_{dv}) \cdot I_{Lmin}}{2} \quad (15)$$

The switching off period is similar with switching on period with V_{DS} equals to the sum of input and output voltage. However, I_{DS} the maximum value of I_L in this turn. The switching-off loss is expressed by formula (16) below.

$$P_{switchingoff} = \frac{f \cdot (V_{in} + V_o) \cdot (t_{di} + t_{rv}) \cdot I_{Lmax}}{2} \quad (16)$$

The total switching loss is the sum of the switching-on loss and switching-off loss, which is presented below in formula (17).

$$P_{switching} = \frac{1}{2} (V_{in} + V_o) [I_{Lmin} \cdot (t_{ri} + t_{dv}) + I_{Lmax} \cdot (t_{rv} + t_{di})] \cdot f \quad (17)$$

t_{ri} is the period while the current is rising.

t_{di} is the period while the current is dropping.

t_{dv} is the period while the voltage is dropping.

t_{rv} is the period while the voltage is rising.

(E) Driving loss

Driving loss is the power consumed while the gate driver of the MOSFET charging

the total semiconductor structure. The gate driver loss is usually straightforward given by the datasheet of the MOSFET.

The formula for driving loss is given below in (18).

$$P_{dr} = Q_G V_{gs} f \quad (18)$$

In the author's project, Q_G is set as $8e^{-9}C$ and V_{gs} is 5V.

(F) Core loss

Inductor core losses are major caused by an alternating magnetic field in the core material dissipated by heat sometimes by noise.

Inductor core loss takes up a big part of total power loss, and as a result, the prediction of accurate inductor core loss is important for buck-boost design.

Applying models based on Steinmetz's model is the most popular method to predict core losses. However, this method shows limitations while applying in small components. Under this circumstance, the author uses a novel method which is suitable for predicting inductor core loss in buck-boost converters[23].

The formula of core loss is presented below in (19).

$$P_{fe} = k_i \cdot (\nabla B \cdot 10^{-4})^\beta \cdot f^\alpha \cdot \left[D^{(1-\alpha)} + (1-D)^{(1-\alpha)} \right] \cdot V_e \cdot 10^{-3} \quad (19)$$

In formula (19), k_i , α , and β are the parameters of Steinmetz's equations; ∇B is the magnetic fluctuation; V_e is the equivalent cross-sectional area of the magnetic field.

(G) Total power loss

Total power loss is the sum of conduction loss, copper loss, capacitor loss, switching loss, driving loss, and core loss as shown in (20).

$$P_{total} = P_{on} + P_{dr} + P_{Cu} + P_{switching} + P_C + P_{fe} \quad (20)$$

2.2.4 Cut-off frequency

Switched-mode power supplies are widely used in power electronics and like other power supplies, an SMPS is to transfer power from a DC or AC source to DC loads. Unlike a linear power supply, the pass transistor of a switched-mode supply continually

switches between low-dissipation, full-on and full-off states, and spends very little time in the high dissipation transitions, which minimizes wasted energy. The main advantage of the switching power supply is higher efficiency than linear regulators. Moreover, smaller size, lower noise, and lighter weight are reasons why it so popular nowadays as well. However. The generation of high-amplitude, high frequency energy, and harmonics are supposed to be eliminated by researchers.

The ability to filter the harmonics is described as cut-off frequency which is the third objective in this project. In electrical engineering, the cut-off frequency is a boundary in a system's frequency response where energy flowing through the system begins to reduce rather than passing through. Cut-off frequency applies as an edge in lowpass, highpass, bandpass, or band-stop filters.

The formula of cut-off frequency is presented in (21) below.

$$f_c = \frac{1}{2\pi\sqrt{LC}} \quad (21)$$

It clearly shows that the value of cut-off frequency is directly determined by inductance and capacitance. However, the principle to optimize cut-off frequency is not clearly shown in formula (19). The key point is to figure out the optimizing direction of the cut-off frequency.

The next step is to derivate the formula of voltage ripple and current ripple expressed by inductance and capacitance of this buck-boost converter.

$$\frac{\Delta V_o}{V_o} = \frac{I_o DT_s + I_{in} C \cdot R_c}{CV_o} = \frac{IDT_s}{CV_o} + \frac{I_{in} R_c}{V_o} \quad (22)$$

$$\frac{\Delta I_L}{I_L} = \frac{V_{in} DT_s}{L(I_{in} + I_o)} \quad (23)$$

As shown in formula (22) and (23), it's obvious that capacitance and inductance appear only in the denominator. Under this circumstance, for eliminating harmonic ripples, the value of the inductance and capacitance are supposed to be as big as possible which means the author demands smaller cut-off frequency in the optimization.

Based on formula (22), the capacitor resistance is a variable for determining the voltage ripple in output. However, as having tiny resistance comparing with load, the capacitor resistance exerts a small impact on filterability, which could be ignored.

2.2.5 The requirements of voltage ripple and current ripple

For selecting optimal pairs of inductors and capacitors, the requirements of low power loss, compact volume, and small cut-off frequency are not enough. Limitation of voltage and current ripple must be considered to regulate the value of inductance and capacitance as well.

In general, the selection of inductor and capacitor are supposed to satisfy the principle that voltage ripple is better to below 10% and current ripple should below 50%. The requirement is presented in formula (24) and (25).

$$\frac{\Delta V_o}{V_o} = \frac{I_o D T_s + I_{in} C \cdot R_C}{C V_o} \leq 10\% \quad (24)$$

$$\frac{\Delta I_L}{I_L} = \frac{V_{in} D T_s}{L(I_{in} + I_o)} \leq 50\% \quad (25)$$

The ripple constraints are peak to peak ripple and this requirement doesn't reach full potential as the initial inductance and capacitance selecting range in the algorithm program are far smaller than the requirement in (24) and (25).

2.3 Select qualified cases by the Pareto frontier

2.3.1 Introduction of the Non-dominated Sorting Genetic Algorithm

(A) Pareto frontier

Pareto efficiency or Pareto optimality is a situation where no individual or preference criterion can be better off without making at least one individual or preference criterion worse off. The concept is named from Vilfredo Pareto, an Italian engineer and economist. The concept of Pareto optimality was initially used in studies of economic efficiency and income distribution.

The Pareto frontier is the set of all Pareto efficient allocations shown on the graph. The Pareto frontier is also known as Pareto front and Pareto set. Finding Pareto frontiers is particularly useful in engineering. By presenting all the potentially optimal solutions graphically, designers could focus on the tradeoffs within a constrained set of parameters, rather than considering a full range of solutions.

In this report, the author is supposed to get the Pareto frontier in a graph with three

criteria acted as three axes, the volume of LC-filter, total power loss, and cut-off frequency. Each Pareto optimality in the Pareto front means a steady state of optimization that they couldn't get better from changing the allocation.

The standard to judge whether an optimized solution has already become the best is the level of non-domination, called rank in this report. When all the population (the size of the population determined by the demanded optimal cases) are sorted in the first non-domination level or the iteration has reached the maximum number set in the program initially, a Pareto frontier has been generated. Based on all the optimal cases in the Pareto frontier, the designers could select the solutions visualized by their own demands.

(B) Criticism of NSGA

The presence of multi-objective problems delivered the demands to obtain a set of optimal solutions instead of the best solution. This is because improving one criterion usually means sacrifices the others. In other words, the best solution doesn't exist in the most multi-objective problems.

The main feature of optimal solutions is that each optimal solution cannot be regarded to be better than the others without any further information. The optimal set is expected to provide designers as many Pareto-optimal solutions as possible. Classical optimization method suggests converting multi-objective problems into several single-objective problems by optimizing one single criterion at a time. However, it dramatically increases the computational complexity and useless calculation in the optimized procedure.

Fig. 8 Pareto frontier with two objectives.

Many types of multi-objective evolutionary algorithms (MOEAs) came to world for finding multi-objective Pareto solutions in one single optimization attempt. The non-dominated sorting genetic algorithm (NSGA) is one typical evolutionary algorithm invented in that period. Over the years, three main criticisms of the NSGA have been proposed.

The first disadvantage is the high computational complexity in non-dominated sorting. The computational complexity of the currently used NSGA is $O(MN^3)$, where M is the objective number and N is the population size set in programming. The computational complexity will dramatically increase with a larger population size, which restricts the optimized ability of NSGA.

The second criticism is the lack of elitism. Elitism is the one fittest candidate or few candidates in the fittest non-dominated level which are directly copied into next generation for preventing the loss of qualified candidates once they have been found. This can sometimes lay a dramatic impact by ensuring the genetic algorithm will not waste time to re-discover previously discarded partial solutions[24].

The third criticism is requiring the sharing parameter σ_{share} . This parameter is related to the distance metric chosen to calculate the proximity measure between two population candidates for deciding which candidate could move to the next generation. However, the performance of maintaining the diversity of solutions relays largely on the chosen value of σ_{share} . Moreover, with the method of using sharing parameter, each candidate has to compare with the rest population, which largely increases computational complexity.

(C) Improvement of Non-dominated Sorting Genetic Algorithm-II

Computational complexity in non-dominated sorting genetic algorithm-II is simplified compared with NSGA. It's clearly shown in the description of the procedure for sorting a population into different non-domination levels.

In traditional NSGA, each candidate is supposed to be compared with every other candidate in the population to find if it is dominated. $O(MN)$ comparisons are required for each candidate in sorting it into one non-dominated level, where M is the number of objectives and N is the population size. Then this algorithm keeps finding all the members of the first non-dominated levels by comparing each candidate with the others.

It takes $O(MN^2)$ rounds comparisons to clarify the first non-dominated level. When the worst case happens that each non-dominated level only obtains one candidate, $O(MN^3)$ computations are required.

However, in NSGA-II, two entities are supposed to be calculated at first, which are n_p and S_p [4]. n_p is the number of candidates that dominate the candidate p and S_p is a set of candidates dominated by candidate p . The candidates with n_p equal to zero are sorted into the first non-dominated front. Then for each candidate in the first non-dominated sorting level, the sets of S_p are visited. In the next step, n_p of each candidate q in set S_p is reduced count by 1. After doing so, if for any candidate q , the n_p comes to zero, they are put in a list Q . All the candidates in Q are sorted into the second non-dominated level. Then, the above procedure is done with the S_p of each candidate in the second non-dominated level. This process continues until all the candidates have been assigned a non-dominated sorting level. Thus, each candidate will be operated at most $N-1$ times before it is ranked in one non-dominated sorting level. Once the candidate is put into one level, it will never be visited again. Because there are at most $N-1$ candidates waiting to be assigned initially, the total computational complexity of the NSGA-II procedure is $O(MN^2)$.

An all-around spread of Pareto optimality is also desired in multi-objective optimization because if the optimal solutions are concentrated spread in one area, some important information cannot be shown in the final optimal cases. For example, if the author sets 1500 candidates in the population, 1500 optimal solutions will be generated at the end. However, 1500 optimal solutions are not all the optimal cases and if most of the optimal solutions are located in one area in the graph, for example, in the small-volume-area, the designers have trouble to get enough solutions with high efficiency or low cut-off frequency. As a result, maintaining the diversity of optimal solutions is very important.

In the proposed NSGA-II, the sharing parameter is replaced by a crowding-comparison approach which could eliminate the problems of highly dependent on initial parameters and computational complexity. The crowding-distance method requires users to build a density-estimation metric and a crowded-comparison operator, instead of defining initial parameters.

An important concept, the crowding distance, has been introduced in NSGA-II. The crowding distance of the i^{th} candidate is shown in the Fig. 9.

Fig. 9 Crowding distance calculation.

As shown in Fig. 9, the crowding distance of candidate i (marked with a red circle) is dependent on the distance of its two nearest neighbors (marked with the yellow circles). The crowding distance is the average side length of the cuboid (shown in the dashed square) and it could serve as an estimate of the perimeter of the cuboid. For protecting the diversity of the optimal solutions, the candidates in lesser crowded areas which mean the candidates are assigned with larger crowding distance are preferred.

The crowding distance theory is worked when the algorithm needs to select a couple of solutions when they are in the same non-dominated level. For instance, 1497 candidates of 1500 have been sorted into the upper non-dominated level, and there are 10 candidates in the next level. 3 candidates with smaller crowding distance are selected to build the next generation with the other 1497 candidates. This procedure is shown in Fig. 10.

(D) The procedures of NSGA-II

(a) Initial setting of NSGA-II

Before operating the multi-objective optimization, the designers are supposed to set all the initial parameters of the programming. In this NSGA-II programming, the initial parameters are presented in Tab. 1 below.

In Tab. 1, M is the number of objectives of this project, which are volume, total power loss, and cut-off frequency. N is the number of candidates in one generation.

Fig. 10 Sorting procedure of NSGA-II

Tab. 1 Initial setting of NSGA-II

M	N	V	NO_RUN
3	1500	2	1
ETAC	ETAM	GEN_MAX	PM
20	20	45	0.5

NO_RUN represents the number of runs of the whole programming which are supposed to be distinguished from GEN_MAX, the maximum number of generations. Even if the candidates haven't reached the standard of optimal solutions, the algorithm will stop after iterating 45 times. V is the number of variables in this programming which are inductance and capacitance. ETAC and ETAM are the distribution index of crossover and mutation respectively. The last parameter is PM, the mutation probability, set as 0.5 in the beginning and it will drop to 0.05 at the end of optimization. The reason why I apply a large value at first is that a large mutation probability could create a population with all-around diversity. The mutation probability drops with iterations, the chosen population will be more stable which benefits the uniformity of the Pareto frontier.

Tab. 2 Parameters related to the buck-boost converter circuit

V_o (V)	V_{in} (V)	I_o (A)	X_L	X_U
50	50	2	$[400e^{-6}, 10e^{-6}]$	$[4000e^{-6}, 1500e^{-6}]$

Tab. 2 presents the initial parameters related to the buck-boost converter circuit set in the programming. V_o , V_{in} and I_o are the output voltage, input voltage and output current expected in the buck-boost converter. Setting these parameters is for objectives calculations in the algorithm. Besides, X_L is the lower boundary of the inductance and capacitance respectively. X_U is the upper boundary of them in the same way.

(b) Population Initialization

Initially, N pairs of L and C are selected randomly based on the limitation factors as the parent population P_0 . The values of L and C in the algorithm are represented by binary numbers, 0 and 1. In this way, L and C of each candidate act as the chromosome full genes. After obtaining the first generation P_0 , each candidate in P_0 is assigned to a non-dominated sorting level. Then, based on the selection of elitism, crossover, and mutation, an off-spring population is generated from P_0 of size N .

The crossover procedure is provided in Fig. 11. Two candidates in the parent population are selected based on the crossover probability set at the beginning. During the procedure, each chromosome is assigned with a crossover point where two chromosomes exchange their genes[19]. The whole crossover procedure is provided in Fig. 11.

Fig. 11 Crossover procedure

Mutation is applied to candidates of the offspring after crossover procedure. Each gene in the chromosomes is alerted with a small probability of mutation. Fig. 12 shows that the third, fourth, and fifth genes of the chromosome being mutated.

The traditional view is that crossover is more important than mutation for rapidly exploring a search space. Instead, mutation only provides a small amount of random search to ensure that no gene in the optimization remains in a steady state[25]. Both

crossover and mutation have the same purpose for exploring the diversity of candidates.

Fig. 12 Mutation procedure

After the crossover and mutation procedure, an off-spring generation with N candidates has been generated. Then, it is combined with the initial parent generation to form a new population with $2N$ candidates.

(c) Non-dominated Sorting procedures

The population with $2N$ candidates is put into a non-dominated sorting procedure. At first, each candidate is assigned to a non-dominated sorting level. As shown on Fig. 10, all the candidates in the first lower levels are selected if the numbers of candidates in those levels cannot reach 1500. When the candidates in the next level cannot be all selected, the crowding distance operator works. Those candidates with smaller crowding distances are selected to go through the next step. Since then, a new generation with N candidates is formed to iterate.

(d) The iteration of NSGA-II

It's assumed that the iteration has gone through t times and the new generation is P_t which means the t^{th} parent generation. O_t is generated from P_t by copying elitism, crossover, and mutation with other N candidates. P_t and O_t are combined as a population with $2N$ candidates. By operating non-dominated sorting and crowding distance selecting, $(t+1)^{\text{th}}$ has been formed, represented by P_{t+1} .

The iteration will end until the candidates satisfy the constraints or the number of

iterations has reached the maximum number set by the users.

Fig. 13 Procedures of NSGA-II

(e) Generate the Pareto frontier

When it reaches the stop criterion, the designers could obtain the Pareto frontiers and select optimal solutions by their demands.

2.3.2 Select qualified cases by the Pareto frontier

(A) The Pareto frontier

The author generates the Pareto frontier by operating the NSGA-II algorithm and the Pareto frontier in three dimensions is shown in Fig. 14.

Fig. 14 The Pareto frontier in three dimensions

(B) Three selected cases

Three optimal cases are selected shown in Fig.14 to compared with the traditional design. In this part, the author analyses the comparisons between those four cases.

For a detailed view of the improvement trade-off, the Pareto frontier provided in Fig. 14 is divided into three graphs with two dimensions in Fig. 15.

For the sake of clarity, case 1 is not one of the optimal solutions as it is not appearing on the Pareto frontier. Instead of that, case 1 is the traditional design which satisfies the constraints of formula (24) and (23). The other three cases are the optimal solutions selected by three different rules.

(a) Case 2: minimizing volume and cut-off frequency while maintaining the same efficiency

As shown in the first graph in Fig. 15 and Tab. 3, case 2 is aimed to maintain the same efficiency with traditional design (case 1) while minimizing the volume and cut-off frequency. The improvement is shown in the purple line in Fig. 15. If this case is preferred, the designers need to select the LC value pair based on the principle discussed above.

(b) Case 3: minimizing the efficiency and volume while keeping the same cut-off frequency

In case 3, the optimized objectives are efficiency and cut-off frequency. The volume is maintained compared with case 1 and the improvement is visualized by the orange line in Fig. 15. If the designers only focus on an efficient and high-performed buck-boost converter, case 3 could be a great selection.

(c) Case 4: minimizing volume and maintaining the cut-off frequency while sacrificing efficiency

The optimized pattern is a little difference in case 4 compared with case 2 and case 3.

In case 4, the author has to sacrifice the efficiency in order to improve the overall design. Case 4 represents another optimized direction of obtaining a compact buck-boost converter while keeping the same cut-off frequency. The LC pair of this optimal solution is given in Tab. 3.

However, before putting the selected LC pairs into productive uses, the designers also need to calculate the voltage and current ripples based on the value of selected LC pairs to avoid unacceptable ripples.

Fig. 15 The Pareto frontier in three Graphs

2.4 Experimental results

2.4.1 Simulink results

Tab. 3 Data of four cases

Case	Volume (m ³)	Power Loss (W)	Cut-off Frequency (Hz)	Inductanc e (H)	Capacitance (F)
1	4.92e-5	6.122	991.8169	1.25e-3	2.06e-5
2	2.91e-5	6.116	4.00e2	7.09e-4	2.24e-4
3	4.92e-5	5.246	1.98e2	1.20e-3	6.00e-4
4	1.63e-5	8.375	9.90e2	4.00e-4	6.42e-5

The structure of the buck-boost converter in Simulink is provided in Fig. 16. Four scopes respectively provide the views of the input power, input voltage and current, output power, output current, and voltage. In this part, the author mainly compares the power loss between input power and output power of the three optimal cases. For the sake of clarity, core loss is not counted in this part.

Fig. 16 The structure of the buck-boost circuit in Simulink

(A) Efficiency in case 2

The inductance and capacitance in case 2 are $7.09 \times 10^{-4} \text{H}$ and $2.24 \times 10^{-4} \text{F}$ respectively. Based on the value of inductance and capacitance, the author obtains the inductor resistance and capacitor resistance which are 0.0956Ω and $7.10 \times 10^{-3} \Omega$ by formula (9) and (12). All those four values are inputted into the Simulink circuit. The value of input power and output power are provided by the measurements of input and output power in Fig. 18 and Fig. 20.

(B) Efficiency in case 3

The values of inductance and capacitance in case 3 are $1.20 \times 10^{-3} \text{H}$ and $6.00 \times 10^{-4} \text{F}$ respectively. And calculating by formula (9) and (12), the author obtains the values of

Fig. 17 The input power of case 2

Cursor Measurements			
Settings			
Measurements			
	Time	Value	
1	0.070	9.892e+01	
2	0.080	9.898e+01	
ΔT	9.797 ms	ΔY	5.532e-02
$1 / \Delta T$		102.074 Hz	
$\Delta Y / \Delta T$		5.647 (/s)	

Fig. 18 Input power measurements of case 2

inductance and capacitance which are 0.146Ω and $2.70e^{-3}\Omega$. The plot of input power and output power are provided in Fig. 22 and Fig. 23 below. The author also could obtain the power loss by comparing the values in Fig.21 and Fig.24.

The values of inductance and capacitance in case 3 are $1.20e^{-3}H$ and $6.00e^{-4}F$ respectively. Calculating by formula (9) and (12), the author obtains the values of inductance and capacitance which are 0.146Ω and $2.70e^{-3}\Omega$. The plot of input power and output power are provided in Fig. 22 and Fig. 23 below. The author also could obtain the power loss by comparing the values in Fig.21 and Fig.24.

Fig. 19 The output power of case 2

Cursor Measurements			
Settings			
Measurements			
	Time	Value	
1	0.070	9.711e+01	
2	0.080	9.707e+01	
ΔT	10.109 ms	ΔY	4.309e-02
$1 / \Delta T$		98.918 Hz	
$\Delta Y / \Delta T$		4.262 (/s)	

Fig. 20 Output power measurements of case 2

Cursor Measurements			
Settings			
Measurements			
	Time	Value	
1	0.070	9.823e+01	
2	0.080	9.828e+01	
ΔT	9.953 ms	ΔY	4.572e-02
$1 / \Delta T$		100.471 Hz	
$\Delta Y / \Delta T$		4.594 (/s)	

Fig. 21 Input power measurements of case 3

Fig. 22 The input power of case 3

Fig. 23 The output power of case 3

Cursor Measurements			
Settings			
Measurements			
	Time	Value	
1	0.070	9.570e+01	
2	0.080	9.570e+01	
ΔT	9.953 ms	ΔY	6.844e-03
$1 / \Delta T$		100.471 Hz	
$\Delta Y / \Delta T$		687.665 (/ks)	

Fig. 24 Output power measurements of case 3

(C) Efficiency in case 4

The value of inductance and capacitance are $4.00\text{e-}^4\text{H}$ and $6.42\text{e-}^5\text{F}$ respectively. And the corresponding inductor resistance and capacitor resistance are $6.40\text{e-}^2\Omega$ and $2.48\text{e-}^2\Omega$. The plots of input power and output power are presented in Fig. 25 and Fig. 27 below. The power loss in case 4 could be calculated by comparing Fig. 26 and Fig. 28.

Fig. 25 The input power of case 4

Cursor Measurements			
Settings			
Measurements			
	Time	Value	
1	0.070	9.833e+01	
2	0.080	9.876e+01	
ΔT	10.005 ms	ΔY	4.271e-01
$1 / \Delta T$		99.948 Hz	
$\Delta Y / \Delta T$		42.688 (/s)	

Fig. 26 Input power measurements of case 4

2.4.1 The OPAL-RT results

The OPAL-RT experiment is operated to verify the ripples of input voltage, output voltage, inductor current, and capacitor current. In this experiment, the author uses the OP5650.

Fig. 27 The output power of case 4

Cursor Measurements			
Settings			
Measurements			
	Time	Value	
1	0.070	9.694e+01	
2	0.080	9.710e+01	
ΔT	9.849 ms	ΔY	1.605e-01
$1 / \Delta T$		101.534 Hz	
$\Delta Y / \Delta T$		16.298 (/s)	

Fig. 28 Output power measurements of case 4

As shown in Fig. (23)-(25), the input voltages of the three cases keep at 50V and the output voltages maintain at -50V. Output voltages are in minus value because the author reverses the output connectors of the buck-boost circuit in OPAL-RT.

In case 2, the inductor ripples fluctuate between 3A-6A in a blue polyline. The capacitor ripples fluctuate from -4A to reach a short plateau period of 2A which is because the capacitor needs to supply output current for output during the MOSFET is off.

In case 3, the inductor current flows between 3A to 5A due to the on and off of the MOSFET. While the capacitor current starts from -4A to 2A in the whole period.

Fig. 29 View of case 2 in OPAL-RT

Fig. 30 View of case 3 in OPAL-RT

However, in case 4, the unit of the inductor current is changed to 10 (A/div). The inductor current, from 2A to 8A, is much higher than it in case 2 and case 3. Meanwhile, the capacitor current is also much higher than before, from -5A to 2A.

The ripples of those four criteria in OPAL-RT are matched with the simulated results in Simulink.

Fig. 31 View of case 4 in OPAL-RT

2.5 Results comparison with single-objective optimization

2.5.1 Introduction of single-objective optimization

Single-objective optimization is a kind of optimization contrast to multi-objective optimization. The major difference is single-objective optimization only cares about one criterion and to some extent, the solutions of single objective optimization are special cases in the solution set of multi-objective optimization. Single-objective optimization's goal is to find a best optimal case only based on one objective. Single-objective optimization is commonly used by researchers for obtaining solutions with stronger target orientation. However, for considering the incompleteness of the results of single-objective optimization, it is gradually replaced by other kind of optimization, such as multi-objective optimization and many-objective optimization[26].

Single-objective optimization could exert effects on the optimization results in many ways. Single-objective optimization usually applied with multi-objective optimization[27]. For instance, applying single-objective optimization at first and using the solutions of single-objective optimization as an candidate in Multi-objective optimization could improve the searching ability in NSGA-II[28]. Moreover, single-objective optimization could also act as the basis of the optimization, and researchers may make some improvements based on it. As an example, an improved single-objective optimization was applied to solving many-objective optimization problems of

antenna arrays in[29].

2.5.2 Results of single-objective optimization

In the thesis, the multi-objective optimization generates a pareto frontier which is the set of all optimal solutions considering three criteria including volume, efficiency and cut-off frequency. For obtaining single-objective results, the author considers three objectives respectively. Under this circumstance, there solutions are the cases with smallest cut-off frequency, smallest volume and best efficiency in turn which are case 5, case 6 and case 7. Each single-objective solution appears at the end points of the Pareto frontier.

Based on the constraints between these three objectives, the solutions with best efficiency and smallest cut-off frequency are the same. In this way three single-objective solutions could be compressed into two.

Three comparisons are made in the following parts, which are case 5 versus case 2, case 6 versus case 1 and case 7 versus case 3.

(A) Case 5 versus case 2

Case 5 is the solution with smallest cut-off frequency and case 2 minimizes volume and cut-off frequency while maintaining the efficiency with the traditional design. The pareto frontier is given in Fig. 32 and Fig.33. The yellow spots are case 2 and the purple spots represents case 5 in the pareto frontier. The improving direction and visualized data comparison is provided in Fig.33 and Fig. 34.

As shown in the figures, the efficiency and cut-off frequency of case 5 are only 84.6% and 25.2% of case 2 respectively. However, the designers have to sacrifice the volume from $2.91\text{e}^{-5}\text{m}^3$ to $6.16\text{e}^{-5}\text{m}^3$ for obtaining a LC-filter with smaller volume and ripples. In general, case 5 is a acceptable choice for designers who treat smaller ripples as the most important criterion and do not mind to sacrifices the compactness for achieving it.

Fig. 32 The Pareto frontier of solution with smallest cut-off frequency

Fig. 33 The Pareto frontier 2 of solution with smallest cut-off frequency

(B) Case 6 versus case 1

Case 6 is the solution with most compact design selected by single-objective optimization. In this part, the comparison is not made between single-objective optimization and multi-objective optimization. However, case 1 is the traditional design which meets the constraints requirements in formula (24) and (25). The comparison is

to qualify the improvement of single-objective optimization contrast to the traditional design.

Fig. 34 Case 5 versus case 2

Fig. 35 The Pareto frontier of the solution with the smallest volume

As shown in Fig. 35 and Fig. 36, the red spots are case 1 and the grey spots represents case 6. The grey lines mark out the changing direction from case 1 to case 6. Case 6 is selected by single objective optimization with one criterion, volume. As a result, the volume decreases 67% from traditional design to case 6 as shown in Fig.37. However, the cut-off frequency nearly remains the same value, while at the same time the power

loss is increased by 37%. Therefore, case 6 is a design extremely focused on improving the compactness.

Fig. 36 The Pareto frontier 2 of the solution with the smallest volume

Fig. 37 Case 6 versus case 1

(C) Case 7 versus case 3

Case 7 is focus on obtain the highest efficiency which means the smallest power loss. This is the third case selected by single-objective optimization. Because of the relation constraints between cut-off frequency, volume and efficiency, the case with smallest cut-off frequency and the case with the highest efficiency could be regarded as the same case as shown in Fig. 38 and Fig. 39. This part is to make a comparison between case 7

and case 3, the case with an optimized efficiency and volume compared to traditional design.

Fig. 38 The Pareto frontier of the solution with the highest efficiency

Fig. 39 The Pareto frontier 2 of the solution with the highest efficiency

Fig. 40 Case 7 versus case 3

Brown spots represents case 7 and blue spots represents case 3. The location of case 7 is close to case 3 in Fig.38 and Fig.39 and the brown lines mark out the changing direction from case 7 to case 3. Fig. 40 also shows slight improvements and fall backs from case 3 to case 7 in a more visualized way. Although the purpose of case 7 is to optimize the efficiency, no space for improvement in efficiency with the power loss only decreasing 1.1% from case 3 to case 7. However, for slightly improving the efficiency, the volume of LC-filter design is not as compact as case 3. Fortunately, the third criterion, cut-off frequency, drops nearly a half in case 7 which means smaller ripples could be expected in this design.

(D) Case 8 versus case 3

Cases selected by Single-objective optimization have been compared with multi-objective cases in the former three parts. In part (D), case 8 is a traditional optimized solution based on case 3. Case 8 maintains the volume with case 3 and optimizes cut-off frequency at the same time. However, for obtaining smaller ripples, the designers have to sacrifice efficiency.

The pink spots represent case 8 and the blue spots are locations of case 3 in the Pareto frontier. From the pink line in Fig. 41, the power loss is increase dramatically from case 3 to case 8, which means the designers have to sacrifice efficiency in a large scale. However, the performance of other criteria could not be clearly measured by a three-dimension plot. Fig. 42 provide us three two-dimension plot to analyse the changing direction of three criteria from case 3 to case 8.

The point of case 8 is to optimize cut-off frequency based on an optimal case. As shown in Fig. 43, the cut-off frequency of case 8 is nearly a half compared with case 3. However, the cost for smaller ripples is that nearly 60% energy will be wasted in case 8.

Fig. 41 The Pareto frontier of case 8

Fig. 42 The Pareto frontier 2 of case 8

Fig. 43 Case 8 versus case 3

(E) Summary

From the comparisons between single-objective optimization and multi-objective optimization, it's clearly that the single-objective solution is the boundary case in the Pareto frontier of multi-objective optimization. Only if the designers demand converter product with extreme performance in one criterion, the single-objective optimization is seldom applied in converter optimization. Obviously, multi-objective optimization could help researchers to obtain the optimal and balanced design of buck-boost converters.

N. Conclusion and Recommendations

N.1 Conclusion

Optimization of power electronics is a popular topic in recent years and many methods have been applied such as introducing topology in buck converter [30] and presenting dual operating modes control technology for fast-transient response [31]. Many researchers also focus on multi-objective optimization and make achievements in that area. However, not enough works have been done with an advanced genetic algorithm, NSGA-II, which could lay different influences on the final optimal solutions in buck-boost converter design. Moreover, not enough analysis has been provided by researchers to compare the overall performance between multi-objective design and single-objective design. Under this circumstance, this thesis applies NSGA-II to optimize buck-boost converters in three criteria and provides the comparisons between the multi-objective results and single-objective results. The Non-dominated Sorting Genetic Algorithm-II applies elitism theory which could sort the best candidate to the next iteration directly. Most of algorithms are lack of elitism, therefore they need to rediscover qualified candidate in the next generation which is time-consuming. Moreover, the sorting parameters are replaced by crowding distance theory in NSGA-II, which could stabilize the sorting results. And the computational complexity to get the Pareto set of three objectives is also simplified. Based on the set of optimal solutions, the designers could select the cases in their demands. Three multi-objective cases are selected by the author and those cases are analyzed by comparing with single-objective solutions. The analysis of the results presents designers with a clear view to select the cases.

This thesis is divided into three major parts. The first part is the introduction of different types of power electronics and recent researchers about DC-DC converters. The second part is the main part of the thesis, the actual work done. The main part of the thesis could be divided into two sections logically. The first section presents an NSGA-II based multi-objective optimization for an efficient, compact, and well-performed buck-boost converter. And the second section briefly introduces single-objective optimization and compares the results from single-objective optimization to single-objective optimization. Five chapters are in this part, which is, literature survey, the preliminary of the proposed three objectives supported by optimization, select qualified cases by Pareto-frontier, experimental results, and results comparisons with single-objective optimization.

Literature survey is to introduce the works that have been done by researchers in recent years. The second chapter shows the preparation of three objectives which are efficiency, volume, and cut-off frequency. The next chapter is named select qualified cases by Pareto frontier. At first, the improvements of NSGA-II compared with the traditional evolutionary algorithms are introduced. Then, the author describes the procedures of a non-dominated sorting procedure and crowding distance operator. After generating the Pareto frontier, three optimal solutions are selected to compare with the traditional designs. The fourth part is experimental results from Simulink and OPAL-RT. And in the final chapter in part two, the author compares the result between single-objective optimization and multi-objective optimization for analysing the advantages and fallbacks of multi-objective optimization comprehensively. The final part is the conclusion and recommendation.

In general, this thesis not only provides designers a Pareto frontier for selecting the cases based on their demands, but also presents them a comprehensive view of the features in different types of solutions.

N.2 Recommendations and future work

A hardware experiment could be conducted in the next step. Case 2, case 3, and case 4 should be achieved by hardware experiments to verify the accuracy of the results. Some problems need to be solved such as how to connect inductor and capacitor to minimize the errors of volume because of the incomplete utilization of the LC-filter space. Once the errors of the results could be controlled into an acceptable range, the achievement could be popularized into grid architecture and industrial production.

Author's Publications

- [1] X. Huang, X. Zhang, and X. Li, "Multi-objective Optimization for Smaller, Efficient and Better Performed Design of Buck-boost Converters," in *2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2020, vol. 7, no. 2, pp. 266–269, doi: 10.1109/pedg48541.2020.9244342.

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