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Investigation of interface properties of h-BN and AlN on AlGaN/GaN heterostructures

Matthew David Whiteside

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2020

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

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Prof. Ng Geok Ing

Authorship Attribution Statement

This thesis contains material from 5 paper(s) published in the following peer-reviewed journal(s) / from papers accepted at conferences in which I am listed as an author.

Chapter 3 is published as: **M. Whiteside**, S. Arulkumaran, S. S. Chng, M. Shakerzadeh, E. H. T. Teo, and G. I. Ng, “On the recovery of 2DEG properties in vertically-ordered h-BN deposited AlGaIn/GaN heterostructures on Si substrate,” Appl. Phys. Express, pp. 0–6, 2020, doi: 10.35848/1882-0786/ab92ee.

The contributions of the co-authors are as follows:

- A/Prof E. H. T. Teo provided the initial project idea and edited the manuscript drafts.
- I prepared the manuscript drafts. The manuscript was revised by Prof. G. I. Ng and Dr. S. Arulkumaran
- I co-designed the study with Prof G. I. Ng and Dr. S. Arulkumaran and performed all the laboratory work, fabrication, measurements and analysis.
- S. S. Chng and M. Shakerzadeh aided in the optimization of the h-BN film deposition.

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The contributions of the co-authors are as follows:

- I co-designed the study with Prof G. I. Ng and Dr. S. Arulkumaran and performed all the laboratory work, fabrication, measurements and analysis.
- K. Ranjan and A. Sandupatla assisted in the result analysis.
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Abstract

AlGaIn/GaN based high electron mobility transistors (HEMTs) are excellent for high-frequency and high-power applications such as DC-DC converters, cellular base stations, radar and wireless communication systems. This is due to its excellent intrinsic material properties such as a wide band gap, high critical electric field, and high electron saturation velocity in the two-dimensional electron gas (2DEG) channel. However, in spite of these advantages, there remain issues to be solved. Two such issues are current collapse and the self-heating effect. Current collapse is due to the trapping of electrons during device operation. These traps are typically found on the surface of the HEMT structure and/or distributed within AlGaIn barrier and/or GaN buffer region. While the traps within the AlGaIn barrier and GaN buffer regions are formed during the growth of the device structure, the traps at the HEMT surface can be reduced using various passivation schemes. Si_3N_4 is the most widely used passivation layer for suppressing the current collapse. However, its poor thermal conductivity ($10 \text{ WK}^{-1}\text{m}^{-1}$) prevents suppression of self-heating of the device. Ideally, a passivation layer used on GaN HEMT will suppress both the current collapse and reduce the self-heating inherent in these devices. Therefore, materials with high thermal conductivity such as hexagonal boron nitride (h-BN) ($\sim 400 \text{ Wm}^{-1}\text{K}^{-1}$) and AlN ($\sim 285 \text{ WK}^{-1}\text{m}^{-1}$) would be more useful for heat extraction compared to Si_3N_4 . However, the typical

deposition methods for both these materials either require high temperature such as metal organic chemical vapor deposition (MOCVD) or deposit at very slow rates such as plasma enhanced atomic layer deposition (PEALD). Therefore, alternative methods of depositing these materials, and the investigation of the effects of the deposition method on the interface and thermal properties is required.

In this thesis, the main objectives are to analyze the interface properties of h-BN and AlN on GaN. This involved the analysis of novel deposition methods of h-BN and AlN on GaN HEMT. An investigation of interface traps was performed for each material.

The major contributions of this thesis are summarized below:

- 1) Vertically ordered h-BN films were successfully sputtered on AlGaIn/GaN heterostructure (HS) using High Power Impulse Magnetron Sputtering (HiPIMS) at room temperature. The deposition process was optimized to produce h-BN with vertical ordering along the (0002) plane, which was confirmed using high-resolution transmission electron microscopy. After the h-BN deposition, degradation of 2DEG properties was observed in AlGaIn/GaN HS. Full recovery of 2DEG mobility, along with an improvement in sheet resistance and an increase in sheet carrier concentration was obtained after rapid thermal annealing at 500 °C for 300s in a N₂ atmosphere, which is found to be due to the reduction of sputtering related structural damage.
- 2) AlGaIn/GaN metal-insulator-semiconductor (MIS) diodes using HiPIMS deposited vertically ordered h-BN at room temperature as

a dielectric have been demonstrated for the first time. The MIS-diodes exhibited 2 orders of magnitude lower gate leakage current compared to conventional Schottky diodes. The interface state density (D_{it}) was extracted using the frequency dependent parallel conductance method, with an estimated minimum value of $8.5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at 0.25 eV below the conduction band. However, despite the relatively low D_{it} , the nano-crystalline structure of the deposited h-BN film showed poor current collapse prevention due to remaining structural damage caused during the HiPIMS deposition.

- 3) AlGaIn/GaN MIS-diodes were fabricated using low temperature epitaxy (LTE) grown single-crystalline AlIn at 200 °C, a technique combining both physical vapor deposition and chemical vapor deposition. This was the first time LTE grown AlIn film was successfully used as the passivation layer for GaN MIS-diodes. The D_{it} characteristics of the MIS-diodes were investigated using the frequency dependent parallel conductance method. Initial results showed a minimum D_{it} value of $2.6 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$.
- 4) The deposition method of AlIn by LTE was further optimized to reduce surface damage during the deposition. This process optimization led to ~ 3.8 times improvement in D_{it} compared to the previous values prior to process optimization. Two distinct interface trapping regions were observed namely fast and slow traps. The fast interface traps had D_{it} as low as $6.7 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ while the slow interface traps D_{it} were as low as $6.8 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. The fast

traps are located within the energy interval of 0.24 to 0.30 eV below the conduction band while the slow traps are located 0.44 to 0.56 eV below the conduction band. The observed fast traps were associated with the AlGaN/GaN interface, while the observed slow traps may have formed at AlN/GaN interface during the deposition of AlN by LTE. The reported low D_{it} values were in between values reported by in-situ MOCVD AlN and PEALD AlN. Post gate annealing effects of AlGaN/GaN MISHEMT were also examined. The 400 °C annealed MISHEMT exhibited an increase of 15% in maximum extrinsic transconductance (g_{mmax}) and an order of magnitude reduction in reverse gate leakage, while maintaining high suppression (93-95%) of current collapse. The reduction of gate leakage current is attributed to the reduction of fast (13%) and slow (25%) interface states after post gate annealing at 400 °C. This study demonstrates that LTE grown AlN can be used as an alternative method to achieve reasonably low D_{it} values at low temperature which is compatible to mainstream wafer processing.

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List of Acronyms

BN	Boron Nitride
GaN	Gallium Nitride
AlN	Aluminum Nitride
HEMT	high-electron mobility transistors
FOM	Figure of Merit
BFOM	Baliga's Figure of Merit
JFOM	Johnson's Figure of Merit
GaAs	Gallium Arsenide
SiC	Silicon Carbide
R_{on}	On resistance
V_{br}	Breakdown voltage
Al₂O₃	Aluminum Oxide
2DEG	Two-dimensional electron gas
AlGaN	Aluminum Gallium Nitride
MOCVD	Metal organic chemical vapor deposition
PEALD	Plasma enhanced atomic layer deposition
HS	Heterostructure
MIS	Metal-insulator-semiconductor
D_{it}	Interface state density
LTE	Low temperature epitaxy
g_m	Extrinsic transconductance
SiN	Silicon Nitride
HfO₂	Hafnium Oxide
ZrO₂	Zirconium Oxide
MISHEMT	Metal-insulator-semiconductor high-electron mobility transistors
HiPIMS	High impulse power magnetron sputtering
VO	Vertically Ordered
W_g	Gate width
L_g	Gate Length
L_{sg}	Source-gate Spacing
L_{gd}	Gate-drain spacing
V_{DS}	Drain-source voltage

V_G	Gate voltage
I_D	Drain current
I-V	Current-voltage
C-V	Capacitance-voltage
P_{max}	Maximum output power
2D-VRH	Two-dimensional variable-range hopping
CVD	Chemical vapor deposition
AFM	Atomic force microscope
FTIR	Fourier-transform infrared spectroscopy
HRTEM	High Resolution transmission electron microscopy
DCMS	Direct current magnetron sputtering
LaB₆	Lanthanum hexaboride
FFT	Fast Fourier transform
SAED	Selected area electron diffraction
EDX	Electron-dispersive X-ray spectroscopy
k_s	Substrate thermal conductivity
k_f	Thin film thermal conductivity
rms	Root mean squared
PECVD	Plasma enhanced chemical vapor deposition
R_{sh}	Sheet resistance
TLM	Transmission line method
G-F	Conductance-frequency
τ_{it}	Trap time constant
G_p	Parallel conductance
E_T	Trap state energy below the conduction band
PVD	Physical vapor deposition
n_s	Carrier concentration
μ_n	Hall mobility
V_{th}	Threshold Voltage

1. Introduction

1.1 AlGaN/GaN HEMT Technology Overview

In recent years, Gallium Nitride (GaN) based high-electron mobility transistors (HEMT) have demonstrated excellent high-frequency, high-temperature and high-power performance. Table 1.1 gives a detailed comparison between the material properties of GaN, Si, GaAs, and 4H-SiC [1]. Owing to GaN's excellent material properties, such as large breakdown field (3.3 MV/cm) and wide band gap (3.40 eV), it is a suitable material for high voltage devices such as Schottky barrier diodes and HEMTs. Additionally, the high electron mobility (900-2000 cm²/V.s) and saturation drift velocity (1.5×10^7 cm/s) allows for the HEMT to operate at high frequencies and high current densities. To aid in the comparison between materials, figure-of-merits (FOM) such as Johnson's FOM (JFOM) [2] and Baliga's FOM (BFOM) [3] are typically used. These FOMs allow for a rough quantitative estimation of the materials relative strengths to be determined with respect to specific device applications. The JFOM is an estimation of the materials performance in high-frequency applications, while the BFOM is used to describe how well a semiconductor conducts in the on-state for low-frequency applications. In both cases, GaN exhibits much higher FOMs compared to Si and GaAs devices. A summary of the advantages GaN has over Si and GaAs can be seen in Fig. 1.1 [4].

Figure 1.2 shows a comparison of power versus frequency between Si,

Figure 1-1 - Merits of GaN vs Si and GaAs. [4]

Table 1-1 – Material properties of GaN compared to other typically used semiconductor materials.

Material	Si	GaAs	4H-SiC	GaN
Bandgap E_g (eV)	1.12	1.42	3.26	3.40
Dielectric Constant ϵ_s	11.8	12.9	10.0	9.0
Electron Mobility μ_n (cm ² /V.s)	1350	8500	700	900-2000
Breakdown Field E_c (10 ⁶ V/cm)	0.3	0.4	3	3.3
Saturation velocity of electrons (holes) $v_s(v_p)$ (10 ⁷ cm/s)	1.0 (1.0)	1.3 (2.1)	2.0 (2.0)	1.5 (2.1)
Thermal Conductivity κ (W/m.K)	150	54	450	130-200
Johnson's FOM	1	7.1	180	760
Baliga's FOM	1	15.6	130	650

SiC and GaN [5]. The high operating frequency capability of GaN HEMT makes it an excellent candidate for applications such as radar technology and high switching power supplies for data centers.

Additionally, GaN is ideal for satellite communications due to its resistance to ionizing radiation. By utilizing the high electron mobility of GaN, it is possible for enhanced power amplification in satellite frequency bands for satellite communication uplinks [6]. Typically, GaAs is currently used for these satellite applications; however satellite components based on GaAs devices are larger, heavier and have a lower output power compared to GaN.

In addition to switching applications, there is also an increasing demand for GaN power devices. For these applications, it is desirable for the

Figure 1-2 – Power vs frequency plot showing applications for GaN vs Si and SiC. [5]

device to have negligible on-resistance while maintaining near infinite off-resistance. Therefore, the on-resistance (R_{on}) and breakdown voltage (V_{br}) are the two most important requirements for high-power switching devices. Figure 1.3 shows the theoretical limit of V_{br} vs R_{on} for Si, 4-H SiC, bulk GaN and AlGaIn/GaN HEMT. The performance advantage in the specific resistance of the AlGaIn/GaN HEMT structure decreases at low voltages due to the impact of the contact resistances, which has not been taken into account in the vertical structures (Si, 4H-SiC, and Bulk GaN). While current devices are yet to reach the theoretical limit of GaN, significant advancements have been made over the years. Y. Uemoto et al have managed to fabricate devices with a V_{br} of 10400 V ($R_{on} \sim 186 \text{ m}\Omega\cdot\text{cm}^2$) using poly-AlN passivation, field plates and deep via-holes

Figure 1-3 – Specific on-resistance as a function of breakdown voltage.

through sapphire [7]. While M. Inada et al have succeeded in achieving a low R_{on} of $0.09 \text{ m}\Omega\cdot\text{cm}^2$ ($V_{br} \sim 35\text{V}$) by reducing the source-drain spacing to $2.2 \text{ }\mu\text{m}$ [8].

1.2 AlGaN/GaN MISHEMT Technology

Although AlGaN/GaN based high-electron-mobility transistors (HEMTs) have demonstrated excellent high-frequency and high-power performance owing to their excellent material properties, they are still facing several issues. Two of the major limiting factors that conventional GaN HEMTs with Schottky metal gates suffer from are high gate-leakage current and current collapse [9]. The high gate-leakage occurs due to the Schottky metal contact, while current collapse is caused by charge trapping at the surface states present on the GaN surface as well as bulk traps within the AlGaN/GaN heterostructure. The high forward gate current under forward bias is attributed to thermionic emission, thermionic field emission and other trap induced mechanisms. This affects the gate-channel capacitance, resulting in an alternative leakage path thus limiting the maximum drain current (I_{dmax}). While under reverse bias, the leakage current is mainly defect-state based, taking place via trap assisted tunneling or emission. A high reverse leakage current can lead to premature breakdown and reducing the reliability of the device. To solve these issues, the introduction of a gate dielectric can be used, as seen in Fig 1.4. By inserting a gate dielectric between the gate and AlGaN/GaN, a significantly larger potential barrier is created. This will effectively

Figure 1-4 – Energy band diagram of an AlGaN/GaN MISHEMT

suppress the leakage current to the Schottky gate while maintaining a large gate voltage swing. The gate dielectric can also act as a surface passivation layer thus reducing surface leakage and current collapse present in GaN HEMT. For these purposes, various materials such as SiN[10], Al₂O₃[11], [12], HfO₂[13] or ZrO₂[14] have been used as both a passivation layer and gate dielectrics.

1.3 Motivation

While AlGaN/GaN MISHEMTs have their advantages compared to HEMT, they also suffer from some of the same disadvantages. One of the main ones is self-heating. Self-heating occurs at high-bias conditions,

where a large electric field is generated at the gate edge of the gate-drain region. This in turn generates a large amount of heat in the channel region, causing an increase in phonon scattering, thereby reducing the drain current of the device. Therefore, to reduce this self-heating effect a high thermal conductivity gate dielectric and passivation layer is desirable. While typical materials used as a gate dielectric for AlGaIn/GaN MISHEMT have their own advantages and disadvantages, they are mainly oxide based with a low thermal conductivity. For example, Al_2O_3 has a large bandgap and good thermal stability, but exhibits low thermal conductivity of $\sim 35 \text{ W/mK}$. Therefore, in this thesis gate dielectrics with high thermal conductivity are explored. The two chosen materials are h-BN and AlN, which have thermal conductivities of $\sim 400 \text{ W/mK}$ and $\sim 200 \text{ W/mK}$ respectively.

When only considering using a material as a gate dielectric, it is acceptable to have a low deposition rate, which for example can be as low as 0.12 nm/cycle for ZrO_2 [15]. However, when considering using the film as a passivation layer, a faster deposition rate is required. Additionally, a low temperature is ideal for increased compatibility with current semiconductor manufacturing requirements. Therefore, in this thesis, two novel deposition methods are used for the deposition of these films to achieve a low deposition temperature and high deposition rate. The deposition methods used are high impulse power magnetron sputtering (HiPIMS) for h-BN and low-temperature epitaxy (LTE) for AlN. As these methods have not been previously reported for depositing the gate dielectric for AlGaIn/GaN MISHEMT, the study of their interface

quality is of the utmost importance to ensure good MISHEMT performance. In general, the process conditions during device fabrication have great influence on interfacial properties. Therefore, in this thesis a detailed investigation of h-BN and AlN gate dielectrics deposited on AlGaIn/GaN based semiconductors is carried out.

1.4 Organization of Thesis

This thesis mainly focuses on the trapping mechanisms and device characteristics of using h-BN and AlN as gate dielectrics in AlGaIn/GaN MISHEMT.

In chapter 2, a general explanation of AlGaIn/GaN MISHEMT principles and device structure is given. This chapter also discusses the trapping mechanisms and issues caused by traps in AlGaIn/GaN MISHEMT. An overview of the characterization techniques used in evaluating the trapping effects is also explained.

Chapter 3 describes the HiPIMS deposition technique used to grow vertically ordered (VO) h-BN. A detailed analysis of the h-BN film is performed, as well as the method used to achieve vertical ordering. An examination of the Hall properties is undertaken, with an annealing scheme as well as the insertion of a SiN buffer layer proposed to recover from any deposition related damage caused.

Chapter 4 investigates using VO h-BN as a gate dielectric in AlGaIn/GaN MISHEMT. The DC performance of the devices is analyzed and compared to conventional GaN HEMT. Furthermore, an investigation of

dielectric interface trapping characteristics using the AC conductance method is presented. Finally, using VO h-BN as a passivation layer on GaN HEMT as a means of reducing the self-heating effect is reported.

Chapter 5 details the film analysis of LTE-AlN thin films. The DC performance of LTE-AlN MISHEMT is analyzed. An annealing scheme is devised to improve device performance. The AlN/GaN interface is investigated using the AC conductance method.

In chapter 6, the results of this thesis are summarized. Additionally, future work and recommendations related to this work are also given.

2. AlGaN/GaN HEMTs, MISHEMTs and Trapping Mechanisms

2.1 Principles of AlGaN/GaN Heterostructure

AlGaN/GaN is a group III-Nitride based heterostructure that consists of two different materials, a smaller bandgap GaN buffer layer topped with a wider bandgap ternary alloy barrier layer (AlGaN). At the junction where these two materials with different bandgaps meet, a triangular quantum well is formed due to the conduction band offset. A 2DEG is then generated within the confinement of the electrons in the quantum well.

For conventional III-V semiconductors such as GaAs, the wider bandgap barrier layer is the main source of carriers for the 2DEG channel. As the electrons are isolated from the ionized donors and confined to the quantum well due to the potential barrier at the heterojunction, there is a reduction in the scattering effect. This allows for a high mobility and carrier density to be obtained, enabling HEMTs to be used for high-power and high-frequency applications [16]. However, for GaN-HEMT the origin of the 2DEG formation is due to spontaneous and piezoelectric polarizations effects [17]. This polarization effect can be ~5 times stronger than that seen in other HEMT structures such as GaAs [18], enabling the formation of a conductive high-density 2DEG even without intentional doping in the barrier layer [19]. The formation of the 2DEG in AlGaN/GaN heterostructure can be seen in Fig. 2.1.

When taking spontaneous polarization into account, the direction of the polarization field relies on the crystal structure. For GaN and its related

ternary allows, there are 3 different crystal structures: i) Wurtzite, ii) Zinc blende and iii) Rock salt [20]. Out of these structures, wurtzite is the most thermodynamically stable, and most AlGaIn/GaN based semiconductor technology is based on this structure. The wurtzite structure consists of alternating Ga and N atoms covalently bonded in a tetrahedral, so each atom is bonded to 4 atoms of the alternative type. This leads to the crystal having a Ga-face when in (0001) orientation, and a N-face in (000 $\bar{1}$) as seen in Fig.2.2. There are several notable differences between the Ga-face and N-face surfaces for GaN [18]. The most notable differences include surface morphology and electron transport properties. N-face GaN has the advantage of being able to be wet etched, however this also causes a rough surface morphology. Ga-face GaN can only be etched by using plasma etching methods, however it typically has a smoother

Figure 2-1 – Energy band diagram of GaN and AlGaIn before and after Fermi level alignment.

surface. There is also a difference in background carrier concentration, with the Ga-face's lower concentration being advantageous for device isolation. The Ga-face also offers enhanced electron transport properties, making it the preferred face for GaN based devices [21].

The piezoelectric polarization in GaN comes about from the thin AlGaN barrier layer deposited on the GaN channel to form the heterostructure. This strain is due to the lattice mismatch between the GaN and AlGaN layer, causing a deformation of the crystal lattice and generating piezoelectric polarization.

Due to the differences in spontaneous and piezoelectric polarization between the GaN channel and AlGaN barrier layer, positive charges are

Figure 2-2 – GaN Wurtzite crystal structure showing the (a) Ga-face and (b) the N-face.

formed at the interface. These charges attract electrons and lead to the accumulation at the interface forming the 2DEG channel. By increasing the Al-content in the AlGaN layer, the piezoelectric polarization will increase. This allows for the carrier concentration to be adjusted to the desired application, as seen in Fig 2.3 [22].

Figure 2-3 – Sheet carrier concentration of the 2DEG confined at a Ga-face GaN/AlGaN/GaN for different thickness of the AlGaN barrier [21].

2.2 Principles of MISHEMT

As with other transistors, the operating principle of AlGaN/GaN HEMT and MISHEMT is the modulation of channel by the gate. A cross-sectional schematic of a typical AlGaN/GaN MISHEMT can be seen in Fig. 2.4. A conventional GaN-based MISHEMT is a three terminal device consisting of source, gate, and drain electrodes. The devices geometric parameters consist of the gate width (W_g), gate length (L_g), source-gate spacing (L_{sg}) and gate-drain spacing (L_{gd}). As discussed previously, the polarization effects of the AlGaN/GaN heterostructure gives rise to a 2DEG channel at the interface. The source and drain are ohmic contacts with a low contact resistance which is highly conductive to the electrons in the 2DEG channel. Electrons are supplied from the source and flow to the drain contact when a positive bias is applied to the drain contact (V_{DS}). The gate electrode metal is chosen such that it forms a Schottky contact, for the devices in this work it is a Ni contact. By applying a voltage to the gate (V_G), the position of the Fermi level relative to the conduction band under the gate can be modulated, thus controlling the amount of electrons

Figure 2-4 – Cross-sectional schematic of a) a typical AlGaN/GaN MISHEMT and b) a typical AlGaN/GaN MIS-diode

flowing in the channel. In this work, the AlGaIn/GaN MISHEMT is in depletion mode, or normally-ON transistors. This means that a current can flow with a zero-gate bias. By applying a negative gate bias below the threshold voltage, the relative positions of the conduction band and Fermi level are such that the 2DEG channel is fully depleted of carriers and the device is turned off.

The two main parameters used to characterize the operation of AlGaIn/GaN MISHEMT are the saturation current I_{DS} and the transconductance g_m . The typical DC output and transfer characteristics of an AlGaIn/GaN MISHEMT are shown in Fig 2.5. Using the output curves in Fig 2.5(a), the maximum saturation current (I_{Dmax}) can be obtained. The on-resistance can be estimated from the linear region (low V_{DS}) of curve at $V_G = 0$ V. In the saturation region, ideally I_D would remain quasi-independent of V_{DS} . However, deviation from the ideal can occur mainly due to self-heating.

Figure 2-5 – Typical DC I-V (a) output and (b) transfer characteristics for AlGaIn/GaN MISHEMT.

The g_m of the device is an important indicator for microwave applications, as it describes the response in I_{DS} to a change in V_G as defined by [23]:

$$g_m = \left. \frac{\partial I_{DS}}{\partial V_{GS}} \right|_{V_{GS} = \text{constant}} \quad (2.1)$$

The g_m has a strong relationship with device gains and high-frequency properties. The maximum value of g_m is defined as g_{mmax} and is a key parameter to deciding the cut-off frequency of the device. Figure 2.5(b) shows the typical g_m for a AlGaIn/GaN MISHEMT.

2.3 Influence of Interfacial Traps on MISHEMT

There are several proposed trapping mechanisms in GaN HEMT to explain the device degradation. The difference comes from the location of the electron traps, such as surface traps, dielectric traps, hetero-interface traps, barrier traps and buffer traps. These can be further split into two broad classifications: i) surface traps present near the surface of the heterostructure, and ii) bulk traps present within the heterostructure.

One of the major causes for surface trapping effects is considered to be the “surface states” [24]. The surface state model implies that there is a positive sheet charge on the heterostructure surface in order for the 2DEG to be present in the AlGaIn/GaN interface. Other traps on the surface include surface point-defects, dangling bonds, and/or impurities on the surface. These traps typically originate during the GaN crystal growth or in various device fabrication processes such as metal evaporation or plasma damage during etching. The presence of traps at the surface of a semiconductor have significant impact on the device’s performance and operation. In GaN-based HEMT and MISHEMT, the surface traps will

cause significant current collapse[25]–[28] and surface leakage[29]–[31]. Bulk traps are typically referred to any trap that is within or below the AlGa_N barrier and are typically formed during the crystal growth. There are various reasons for bulk traps to form, such as dislocations caused by lattice mismatch between the GaN and the substrate. Another cause is point defects caused by Ga and N vacancies. There are also several common impurities found in GaN during the MOCVD growth which act as un-intentional dopants, such as Fe, Si, C, H, and O. Under high electric fields, electrons in the 2DEG may get injected into traps within the heterostructure. These trapped electrons produce a negative charge which depletes the 2DEG, resulting in drain current dispersion.

The energy level can be used to classify the corresponding trap. When the energy level of a trap is close to either the conduction or valence band, it is called a shallow-level trap. These traps are typically responsible for parasitic doping effects. When the trap energy level is deep within the bandgap, it is called a deep-level trap. Deep-level traps are mainly responsible for charge trapping and/or non-radiative recombination. Figure 2.6 shows the trapping locations within the bandgap. Deep-level traps localized in the upper half of the bandgap have a higher probability to capture electrons and emit them to the conduction band. These deep-level traps have a variety of origins and can depend on the fabrication

Figure 2-6 – Trapping levels within the bandgap of a semiconductor, showing shallow and deep-level traps.

Table 2-1 - Physical origin of traps with the trap energy below conduction band in GaN-based devices [137], [138].

Physical Origin	Trap Energy (eV)	Ref
C/O/H Impurities	0.44, 0.45 0.58	[137], [139]
VGa+Oxygen complex	0.58, 0.65	[137]
Nitrogen Interstitials	0.73	[137]
Fe dopant	0.57, 0.72	[140], [141]
Nitrogen vacancies	0.27	[142]
Possible AlGaN surface	0.34	[143]
Gallium vacancies	0.8	[144]
GaN native defects	0.62, 0.65	[139], [145]
Nitrogen Anti-sites	0.51, 0.55, 0.69	[146]

conditions. Some examples include defect, dislocations, or impurities in the crystal structure as seen in table 2.1. These traps can be further categorized into two main types, namely acceptor-like and donor-like traps. Acceptor-like traps have a net neutral charge when empty, however when occupied by an electron the trap has a net negative charge. However, donor-like traps have a net neutral charge when occupied by an electron and have a net positive charge once the electron is donated and the trap is occupied by a hole.

2.3.1 Current Collapse

When electrons are trapped, there is a resultant reduction of sheet-carrier density in the 2DEG channel in order to conserve charge neutrality. This leads to a corresponding reduction in the drain current density. This phenomenon is generally referred to as current collapse [26], [32]. Current collapse is best defined as the discrepancy between the drain current in DC and pulse measurements of I-V curves. The main parameters used in the characterization are the “gate-lag” and “drain-lag” quiescent bias (q-bias) conditions [26]. The gate-lag is defined by the transient response of the drain current to an applied gate voltage while the drain voltage remains constant. Conversely, drain-lag is the transient response of the drain current to an applied drain voltage while the gate voltage remains constant. The I_D - V_D characteristics seen in Fig. 2.7 shows the effect of current-collapse on the output power of GaN HEMT [33]. By observing the pulse curve (dashed) in Fig.2.7, there is a clear increase in dynamic R_{on} , as well and in increase in knee voltage and a decrease in maximum

drain current (I_{dmax}). Furthermore, this leads to a decrease in maximum output power (P_{max}) which is given by:

$$P_{max} = \frac{\Delta V_D \times \Delta I_D}{8} \quad (2.2)$$

where ΔV_D is the maximum voltage swing and ΔI_D is the maximum current swing. Current collapse is caused in GaN HEMTs when they are biased under a high V_{DS} off-state condition. This causes a high electric field to exist on the side of the Schottky gate close to the drain. The high electric field induces an injection of electrons from the gate to surface traps [27], [34]. As these electrons are trapped, the channel below is subsequently

Figure 2.7 – I_d - V_d characterization of GaN HEMT before (solid lines) and after (dashed lines) current collapse. The shaded boxes correspond to the approximate maximum attainable output-power of the device before and after current collapse [33].

depleted. Once the GaN HEMT is switched on, the trapped electrons are emitted from the traps and increase the current in the channel. However, the emission time of these traps is highly dependent on their location within the bandgap, with deeper traps being considerably slower than shallow traps. This in turn leads to a slow recovery of the current during a pulse on-state. As the pulse is not of sufficient length to fully recover the device, there is a resultant higher dynamic R_{on} and a lower I_{Dmax} , as depicted in Fig. 2.7.

2.3.2 Surface Leakage

While GaN HEMTs suffer from vertical gate leakage through one-dimensional transport at the Schottky gate interface, there is also an issue with surface leakage. Surface leakage is caused by the lateral injection of electrons to the GaN surface through the edge of the gate, and can cause instability in device operation [35], [36]. One possible mechanism for surface leakage current is two-dimensional variable-range hopping (2D-VRH) assisted by a high-density of states at the GaN surface. This mechanism is caused by the high electric field at the gate metal edge causing a lateral injection of electrons via tunneling to the GaN surface states. These laterally injected electrons then propagate towards the drain electrode through 2D-VRH, generating a surface leakage current.

2.4 Calculating interface traps using the AC conductance method

There are several methods for calculating the density of interface states (D_{it}), such as the combined high-low frequency capacitance (Castagné–Vapaille) method [37], the Terman method [38], [39], and the AC conductance method [40]–[42]. Each method has its own advantages and limitations. For example, the high-low frequency method is the fastest and simplest method to extract the D_{it} , as it uses a comparison between a CV curve measured at 100 Hz and one measured at 1 MHz. However, as the 100 Hz and 1 MHz CV curves are not true low and high frequency curves the D_{it} is typically underestimated using this method. This is because traps close to the band edge respond to the CV signal first, causing the AC contribution of interface traps to stretch-out of the measured curve. The D_{it} will consequently be underestimated due to the increase in slope of the measured CV curve [43]. For the Terman method, the measured CV data is compared to a theoretically ideal CV curve, and the D_{it} is extracted from the differences between the two curves. The accuracy of this method is heavily dependent on the two input parameters needed to calculate the ideal CV curve, the dopant concentration and oxide capacitance. For example, a dopant concentration 30% lower than its actual value will result in a D_{it} underestimated by 3 times [43].

In this thesis, the AC conductance method was chosen as it uses the conductance, which represents a loss in the device due to the capture and emission of carriers at the interface, to calculate the interface trap

density. This method analyzes the loss which is caused by the change in trap level charge states [44]. As this method is sensitive to the charge state levels, it is a useful method to investigate the interface trap density in the depletion and weak inversion layer [45]. However, this method has a limitation in that if the interface capacitance is significantly larger than the oxide capacitance then the D_{it} will be underestimated. Therefore, this method is sensitive to an accurate measurement of the oxide capacitance.

A MIS-diode with typical AlGaIn/GaN heterostructure can be drawn as a

Figure 2-8 - The schematic and equivalent circuit of a MIS diode: (a) the top view of a typical circular MIS diode; (b) the equivalent circuit element distribution; (c) the equivalent circuit topology [33].

schematic with its equivalent circuit, as shown in Fig. 2.8 [33]. While Fig. 2.8 (a) shows a top view, and (b) shows its cross-section and equivalent circuit element distribution, the equivalent circuit topology shown in (c) is used for further analysis. In Fig. 2.8(c), the resistance R_s is the series resistance from the ohmic contact to the channel below gate through the access region between the source and gate electrodes. The resistance R_t is the resistance associated with the gate leakage current through the gate to the channel. The capacitance C_{IN} is the capacitance of the gate insulator. The capacitance C_b represents the capacitance of the barrier layer (including the GaN cap layer). The capacitance C_d represents the capacitance associated with the channel depletion region. The series C_{it} and R_{it} describes the capacitance and resistance effects of the traps located at the interface between the gate insulator and semiconductor

Figure 2-9 - (a) Simplified circuit of Fig. 2.8(c) using the stated assumptions, (b) simplified circuit of a conventional Schottky diode and (c) measured circuit seen by C-V measurements [33].

materials. These traps have an associated time constant of $\tau_{it} = R_{it} \times C_{it}$. Several assumptions can be made to simplify this equivalent circuit. If the gate leakage current is negligible, then the value of R_t will be extremely large. Also, if the gate bias is oscillating at a very high frequency significantly faster than the time constant τ_{it} , then the effect of R_{it} and C_{it} can be ignored. Finally, if the device is working in the accumulation region then C_d is not plausible. Using these assumptions, the circuit seen in Fig.2.8(c) can be simplified to Fig.2.9(a). Similarly, the conventional Schottky diode can be simplified to Fig.2.9(b). The actual circuit measured through C-V measurements can be assumed to be that seen in Fig. 2.9(c). In Fig. 2.9(c) the C_m and G_m are the values of capacitance and conductance measured during the C-V measurements. The series resistance R_s can be calculated by biasing the diode in the accumulation region and using the equation:

$$R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2} \quad (2.3)$$

The effect of R_s on the measured capacitance and conductance can thus be

given by:

$$C'_m = \frac{C_m}{(1 - G_m R_s)^2 + (\omega C_m R_s)^2} \quad (2.4)$$

$$G'_m = \frac{\omega^2 R_s C_m C'_m - G_m}{R_s G_m - 1} \quad (2.5)$$

For the conventional Schottky (SB) diode, $C'_m = C_{HEMT} = C_b$ and for MIS-diodes $C'_m = C_{MISHEMT}$, where:

$$\frac{1}{C_{MISHEMT}} = \frac{1}{C_{IN}} + \frac{1}{C_b} \quad (2.6)$$

C_{IN} can then be extracted from the measured overall capacitance for the corresponding MIS diode ($C_{MISHEMT}$) and conventional Schottky diode (C_{HEMT}):

$$C_{IN} = \frac{1}{\left(\frac{1}{C_{MISHEMT}} - \frac{1}{C_{HEMT}}\right)} \quad (2.7)$$

By extracting R_S and C_{IN} from the measurements, these can be subtracted from Fig. 2.8(c) and the dashed frame in Fig. 2.10(a) can be de-embedded. The capacitances C_b and C_d can be combined into C_d' , and a Thevenin transformation can be used on Fig. 2.10(b) to describe 2.10(c). By measuring the equivalent parallel conductance G_p of the MIS-diode as a function of bias voltage and frequency, the trap density can be estimated.

G_p can be described in two ways, by assuming a continuum of trap energy levels [41], [46], [47], and by assuming a discontinuity of trap energy levels [44], [48], [49]

Figure 2-10 - (a) Simplified circuit of Fig. 2.8(c), (b) simplified equivalent circuit of a MIS diode and (c) further simplified for interface density calculations by the AC conductance method [33].

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln(1 + \omega^2\tau_{it}^2) \quad (\text{continuum}) \quad (2.8)$$

$$\frac{G_p}{\omega} = \frac{q\omega D_{its}\tau_{it}}{1 + \omega^2\tau_{it}^2} \quad (\text{discontinuity}) \quad (2.9)$$

where ω is the radial frequency ($\omega=2\pi f$), D_{it} is the interface trap density and τ_{it} is the trap time constant.

However, the G_p used in equations 2.8 and 2.9 are based on the parallel C_p - G_p equivalent circuit in Fig. 2.10(c), which ignores the gate insulator capacitance C_{IN} . A circuit comparison between Fig. 2.9(c) and Fig. 2.10(c) while taking into account the effect R_S has on the circuit gives G_p as

$$\frac{G_p}{\omega} = \frac{\omega G_m' C_{IN}^2}{G_m'^2 + \omega(C_{IN} - C_m')^2} \quad (2.10)$$

Equation 2.10 allows for an accurate plotting of G_p from the measured G_m and C_m . This curve can then be line fitted using equations 2.8 or 2.9 depending on the trap continuity to estimate the D_{it} of the system.

3. Vertically Orientated Hexagonal Boron Nitride Deposition and Characterization

3.1 Introduction

Recently, the development of two-dimensional (2D) materials with high-thermal conductivity have been explored to provide new ways for thermal management in high-power transistors [50]. This is required because amorphous SiN, the conventional passivation material for GaN based devices, has a low thermal conductivity ($\sim 1 \text{ Wm}^{-1}\text{K}^{-1}$) [51] and is consequently not effective in reducing the self-heating from the device when it is operating at high voltages. The self-heating effect appears at high bias conditions when the temperature rises due to the generation of Joule heat which reduces the drain current [52]. This heat can be partially mitigated by using a 2D material such as hexagonal boron nitride (h-BN). h-BN has a layered structure similar to graphene with a relatively high in-plane thermal conductivity ($\sim 400 \text{ Wm}^{-1}\text{K}^{-1}$) [53] as well as an excellent electrically resistive nature with chemical stability. A summary of h-BN material properties can be seen in Table 3.1 [54]–[57].

Researchers have transferred few monolayers of h-BN which was grown using chemical vapor deposition (CVD) at high temperatures ($\sim 1000^\circ\text{C}$)

Table 3-1 – Material properties for h-BN.

Bond Length (nm)	0.145 $\parallel$; 0.334 $\perp$ [54]
Thermal Conductivity	400 $\parallel$; 0.30 $\perp$ [54]
Bandgap (eV)	5.97 [55]
Dielectric Permittivity	6.93 $\parallel$ [56]; 2.87 $\perp$ [57]
Breakdown electric field (MV/cm)	3 $\parallel$ 12 $\perp$ [54]

[58], [59]. However, high temperature depositions and transfer techniques are undesirable for large-scale and high yield manufacturing. Other methods such as pulsed lasers [60], ion beams [61], or magnetron sputtering [62], [63] have also shown promising results on the deposition of h-BN films. This is largely due to physical vapor deposition techniques allowing for thick films to be deposited, as well as being adaptable for large-scale manufacturing. To assist with better thermal management to extract heat away from the hotspots formed in the gate-drain region of the transistor, a high thermal conductivity along the vertical plane relative to the substrate is required. As h-BN has an anisotropic nature, thermal conductivity along the plane of the layer (in-plane) is much higher than that between planes (out-of-plane). The anisotropic nature is due to the stacked layer nature of h-BN. When heat is conducting along the layer, the thermal conductivity is significantly higher than between the layers due to the continuous crystalline structure. Hence the vertical ordering of h-BN relative to the substrate is desired for the extraction of heat from the device channel (see Fig. 3.1(b)). However, the previously reported techniques are mainly horizontally ordered relative to the plane of the substrate. Recently Cometto et al achieved vertically ordered h-BN on Si substrates using a high-power impulse magnetron sputtering (HiPIMS) system [64]. This method allows the deposition of considerably thick films at room-temperature. Room temperature h-BN deposition has an added advantage of being compatible with lift-off using conventional lithography process.

In this chapter, the successful deposition of vertically ordered h-BN films

on AlGaIn/GaN heterostructures (HS) using HiPIMS is demonstrated. In addition, characterization using Fourier-transform infrared spectroscopy (FTIR), atomic force microscope (AFM), and transmission electron microscopy (TEM) were used to examine the deposited h-BN. Hall measurements were also carried out to study the two-dimensional electron gas (2DEG) properties of the AlGaIn/GaN HSs and the effect of annealing was investigated.

3.2 High Power Impulse Magnetron Sputtering (HiPIMS)

High Power Impulse Magnetron Sputtering is a physical vapor deposition method invented in 1999 by Kouznetsov et al [65]. HiPIMS is based on direct current magnetron sputtering (DCMS), and it relies on extremely high peak power densities to increase the ionization rate and energy of the target species to improve film density. DCMS working principles involve a large negative voltage (200-1000 V) applied to the cathode (deposition target). The high voltage induces a glow discharge in a gas (usually argon) to ionize it and produce a plasma. As the gas molecules become positively charged, they accelerate towards the negatively charged target causing a sputtering effect. A magnetron which produces a powerful magnetic field is used to trap the ionized species and confine them to the vicinity of the target. This increases the sputtering yield and ionization rate of the target due to electron secondary collisions with the sputtered atoms. Depending on the energy of the ionized atoms, they will either get trapped by the magnetron and re-sputter the target or escape

Table 3-2 - Comparison table between HiPIMS and DC Magnetron Sputtering

Parameter	HiPIMS	DC Magnetron
Working Pressure [Torr]	$10^{-4} - 10^{-2}$	$10^{-4} - 10^{-2}$
Cathode Current Density [A/cm^2]	$J_{\text{MAX}} \leq 10$	$J_{\text{MAX}} \leq 0.1$
Discharge Voltage [kV]	0.5 – 1.5	0.3 – 0.6
Plasma Density [cm^{-3}]	$\leq 10^{13}$	$\leq 10^{11}$
Cathode Power Density [kW/cm^2]	1 – 3	< 0.1
Ionization Fraction	30% – 90%	< 1%

the magnetic field and contribute to the deposition of a thin film on the substrate.

HiPIMS uses the same basic operating principles as DCMS, with the distinction coming from the inclusion of pulsing the sputtering targets voltage to produce an on/off ratio. When pulsing the voltage, current densities up to 2 orders of magnitude higher can be achieved. This is done by having a duty cycle typically below 5%. By pulsing high currents for a few tens of microseconds, high energy densities can be achieved. High energy density of several hundred watts per square centimeter enables the formation of a very high-density plasma with an increased ionization rate compared to DC sputtering. Table 3.2 shows a comparison between typical HiPIMS and DCMS parameters.

HiPIMS growth of metals and plasma studies are well covered in the literatures, with the current work being focused on the growth of dense metal oxides or metal nitrides. However, reports on the growth of ceramic materials with the exception of carbon are rare. In particular, the growth of BN with HiPIMS has only recently being examined [64], [66]. Using

HiPIMS as a method for depositing h-BN allows for thick vertically ordered h-BN film to be deposited at room temperature. This is a significant advantage over other deposition methods such as CVD which require high temperatures, or magnetron sputtering which does not produce vertically ordered films. As it is a room temperature deposition, it is more compatible with current GaN HEMT manufacturing process.

3.3 Experimental Setup

In this chapter, AlGaIn/GaN HSs were grown by metalorganic chemical vapor deposition (MOCVD) on 4-inch Si (111) substrates [67]. It consists of i-GaN (2 nm) cap layer, i-Al_{0.27}Ga_{0.73}N (18 nm) barrier layer, i-GaN (800 nm) buffer layer and transition layer (1400 nm). The high resistivity Si substrate (HR-Si) has a resistivity >6,000 $\Omega\cdot\text{cm}$. A schematic of the HS can be seen in Fig. 3.1. For Hall samples preparation, ohmic contacts consisting of Ti/Al/Ni/Au (20/120/40/50 nm) were deposited on 13 mm squares by e-beam deposition, followed by rapid thermal annealing at 775 °C for 30 s in an N₂ atmosphere. The as-grown AlGaIn/GaN HSs exhibited a room temperature sheet resistance (R_{sh}) of 467 $\Omega/\square$, a Hall mobility (μ_H) of 1430 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and a sheet carrier concentration (n_s) of $9.37 \times 10^{12} \text{ cm}^{-2}$. The h-BN films were deposited using a HiPIMS system at room temperature with a thickness of ~400 nm. Previously, Cometto et al have shown that the high ion energy during a HiPIMS deposition is the leading cause for the vertical ordering of h-BN on Si [64]. Therefore, to achieve vertical ordering of the h-BN film on GaN, the deposition conditions were optimized as described in chapter 3.4. Typical deposition conditions are

as follows: a pulse rate of 8000 Hz and a pulse width of 25 μ s, with a duty cycle of 20%. The base pressure used in the chamber is 3×10^{-4} Pa and a process pressure of 4×10^{-1} Pa. Ideally, a pure boron target would be used; however, boron is electrically insulative at room temperature and requires to be heated up to >500 °C before it starts being conductive. Hence, a 3-inch diameter lanthanum hexaboride (LaB_6) target was used

Figure 3-1 – (a) Schematic cross-sectional diagram of AlGaN/GaN HS with VO h-BN on Si substrate. (b) Vertical ordering of the h-BN relative to the surface.

Table 3-3 - Optimized deposition conditions to achieve vertically-ordered h-BN on AlGaIn/GaN HS.

Parameter	Deposition Conditions for vertically-ordered h-BN
Target [3-inch diameter]	LaB ₆
Ar/N ₂ Flow Rate [sccm]	30/10
Base Pressure [Pa]	3×10 ⁻⁴
Process Pressure [Pa]	4×10 ⁻¹
Average Power [W]	280
Pulse Voltage [V]	350
Pulse Frequency [kHz] / Width [μs]	8 / 25
Peak Pulse Intensity [A]	22
Power Density [Wcm ⁻²]	30
Thickness [nm]	300
Substrate Temperature [°C]	24 - 48

instead as it does not require high temperature and is also able to produce plasma with very high boron content and high ionization rate. While using a LaB₆ target there is a possibility of La incorporation in the deposited h-BN film. This is further analyzed in chapter 3.4.3. Typically, h-BN deposition using the LaB₆ target was reactively sputtered in a gas mixture of N₂ (25%) /Ar (75%). The pulse voltage was ~350 V with an average power of 280 W and a peak power density of ~30 W cm⁻². A summary of typical deposition conditions can be seen in Table 3-3. Figure 3.2 shows the HiPIMS setup used for all depositions.

Figure 3-2 – HiPIMS setup used for the deposition of h-BN films.

3.4 Vertically aligned h-BN on AlGaN/GaN heterostructure

Physical and Structural analysis

After deposition of the h-BN films, characterization using Fourier-transform infrared spectroscopy (FTIR), atomic force microscope (AFM), and transmission electron microscopy (TEM) were used to examine the deposited h-BN. Hall measurements were also carried out to study the two-dimensional electron gas (2DEG) properties of the AlGaN/GaN HSs and the effect of annealing was investigated.

3.4.1 FTIR

The deposited h-BN film ordering was characterized using FTIR. FTIR has been widely used to characterize BN thin films [62]–[64], [68]. From the measured data, the observed peaks give the vibration modes in the BN crystalline structure and can be used to verify the formation of hexagonal structure. This technique has also been used to determine the ordering of the hexagonal phase of the BN films [62]–[64], [68]. In the characterization of BN films, the three main peaks to examine are at 1080 cm^{-1} (cubic-BN mode), 780 cm^{-1} (out-of-plane B-N-B bending mode absorption peak) and the 1380 cm^{-1} (in-plane B-N stretch mode) as seen in Fig 3.3 (a-c) [64], [69]. For a vertically ordered film, there is an enhanced response peak at 780 cm^{-1} relative to the 1380 cm^{-1} peak as well as a “derivative-like” response at 1600 cm^{-1} [70]. In this study, the film orientation was initially determined by computing the ratio of the in-plane and out-of-plane peaks. Each spectrum shows the characteristic of h-BN, with a broad peak at 1380 cm^{-1} and an additional peak centered at 780

cm⁻¹. The absence of a peak at 1080 cm⁻¹ indicates that there is no presence of cubic BN phase in the deposited films. The peak at 600 cm⁻¹ is referring to the GaN-on-Si substrate. Each spectrum was normalized between 0 and 1 for all values between 400 cm⁻¹ and 2000 cm⁻¹. The minimum transmission peak reaches 0 around the 1380 cm⁻¹ peak, allowing the peak intensity ratio $R_{780/1380}$ to be written as:

$$R_{780/1380} = \frac{1-I_{780}}{1-I_{1380}} = \frac{1-I_{780}}{1}$$

(3.1)

Figure 3.3 shows the FTIR spectrum for the h-BN samples grown using input currents ranging from 200 mA to 800 mA. Using equation 3.1, the peak intensity ratio for the different input current was calculated as 0.59, 0.70, 0.69 for 200 mA, 600 mA and 800 mA respectively. As the 780 cm⁻¹ peak is absent in the FTIR curve with a 400 mA input current, the ratio was not able to be calculated. A higher peak ratio is an indication of enhanced vertical ordering of the h-BN film. Therefore, at higher input currents the films are more vertically ordered. At an input current of 400 mA, there is no visible presence of corresponding 780 cm⁻¹ peak which indicates that this film is horizontally ordered. This could be explained by the increasing compressive stress on the films as the input current increases because a high compressive stress is required for vertically ordered h-BN growth [64]. There were no successful growths at input currents higher than 800 mA, as these films delaminated due to excessive stress in the deposited h-BN films. Since a highly vertically ordered film is desirable to extract heat away from the channel of a device, the growth

conditions associated with the 800 mA spectrum were considered optimal for this work. Both 600 mA and 800 mA deposited samples exhibited vertically ordered h-BN films on AlGaIn/GaN HS with nearly identical peak intensity ratios, which is desirable to extract the heat from the device. In this work, the 800 mA samples were selected for further characterization

Figure 3-3 - Structure and IR active phonon modes of h-BN. (a) The h-BN crystal. (b) The IR-active in-plane phonon mode. (c) The out-of-plane IR-phonon mode. [69]. (d) FTIR spectra of HiPIMS deposited h-BN on AlGaIn/GaN HS using input currents ranging from 200 to 800 mA. Inset: Schematic diagram of vertically ordered h-BN on the substrate.

and analysis due to the increased deposition rate without compromising the film quality. Further parameters were analyzed the same way including gas ratio, deposition temperature and voltage bias, with the corresponding peak ratios seen in Fig. 3.4. For each deposition, the conditions remained constant except for the parameter being examined. When changing the N₂/Ar gas ratio, it can be seen that by increasing the nitrogen ratio from 25% to 75%, there is a decrease in the peak ratio from 0.72 to 0.4. This decrease in peak ratio likely comes from a decrease in plasma density, as Ar is gas species responsible for sputtering in HiPIMS. As the plasma density decreases, the average ion energy also decreases. Since vertically ordered h-BN requires high ion energy to achieve vertical ordering, a reduction in ion energy would cause a decrease in vertical peak ratio. Figure 3.4(b) shows the FTIR peak ratio plotted against the negative substrate bias. As the substrate bias increases, there is a downward trend in the peak ratio. A similar trend can be seen in Figure 3.4(c), where an increase in temperature causes a decrease in peak ratio. As the peak ratio is proportional to the induced stress in the film [64], this indicates that by increasing the ion energy there is a decrease in stress in the BN film. The stress in the BN film can be approximated by the following equation [64], [71]

$$\sigma \propto \frac{1}{kE^5}$$

(3.2)

where E is the ion energy, $k = 0.016\rho E_0^{-5/3}$, ρ and E_0 are parameters

Figure 3-4 – Peak ratios for (a) N₂ gas percentages, (b) voltage bias, and (c) deposition temperature.

related to the material properties. As HiPIMS is a high energy process, increasing the ion energy actually decreases the film stress. A lower stress arises when high energy ions impact the film with too much energy causing a re-sputtering effect. This either rips ions away from the film structure or displaces the atoms in a way that causes the crystal structure to relax. Therefore, by increasing the ion energy through either voltage bias or temperature, there is a reduction in film stress and thus a reduction in peak ratio. A similar effect was shown by Cometto et al. for h-BN

Figure 3-5 - Curve plotted from the stress curve formula given by McKenzie et al. showing the compressive stress depending on the ion energy for carbon. Assuming a similar curve distribution for boron nitride, the current results are located at the high ion energy portion as shown in the inset, displaying the computed compressive stress for ordered h-BN films grown at room temperature [64].

Figure 3-6 - FTIR spectra of HiPIMS deposited h-BN on AlGaIn/GaN HS using optimized deposition conditions, with a 780/1380 peak ratio of 0.90.

deposited on Si, as seen in Fig. 3.5 [64]. After optimization, an FTIR spectra of the film can be seen in Fig. 3.6. The peak intensity ratio $R_{780/1380}$ of the film was measured to be 0.90, indicating high vertical ordering was achieved.

3.4.2 Transmission Electron Microscopy of h-BN

HRTEM was used to verify if the optimized deposited h-BN was vertically ordered. The presence of ordered h-BN film was also found in the HRTEM image (see Fig. 3.7(a)). From the observation of the distinct basal planes, the formation of the planes is highly oriented and homogeneous across the entire film. The fast Fourier transform (FFT) of the ordered BN film

exhibits the characteristic pattern of a polycrystalline film, predominantly oriented with the (0002) plane perpendicular to the substrate. However, the presence of some rings in the FFT (see Fig. 3.7(c) inset) indicates

Figure 3-7 - (a) Cross-sectional HRTEM images of h-BN on AlGaIn/GaN HS. (b) SAED of the sample showing an interplanar spacing of 0.342 nm along the (0002) plane. (c) Cross-sectional HRTEM image of the BN film away from the interface region as deposited and (d) Cross-sectional HRTEM image of h-BN after annealing at 500 °C for 300 s. Arcs seen in the FFT of the TEM indicates majority normal alignment.

there is also presence of some turbostratic phases in the film. Turbostratic is used to describe a crystal structure where the basal planes have slipped out of alignment. The ordered h-BN was also further verified by doing the selected area electron diffraction (SAED) on the deposited h-BN film, as shown in figure 3.7(b). This shows (0002) plane orientation with an interplanar spacing of 0.342 nm which is typical for the deposited ordered h-BN film [72]–[74]. An interplanar spacing of 0.342 nm indicates that the h-BN is turbostratic along the vertical plane relative to the GaN substrate, which is consistent with the rings seen in the FFT of the HRTEM image.

3.4.3 Electron Dispersive X-ray spectroscopy

A qualitative elemental analysis (B, N and La) was also carried out on the deposited h-BN using electron-dispersive X-ray spectroscopy (EDX) profiling (see Fig. 3.8). The presence of La was observed throughout the deposited h-BN film on AlGaIn/GaN HS with the average atomic percentages of B:N:O:La = 49:39:9:3. This shows that there is a higher percentage of B-content compared to that of N-content, with a ratio of B:N of 1.23:1. La is uniformly distributed throughout the deposited h-BN. It is likely that the presence of O in the structure is replacing nitrogen, as the ratio between B:O+N is ~1:1. After annealing at 500 °C for 300 s (for reasons related to the electrical performance, see chapter 3.5), the average atomic percentages of the film changes to B:N:O:La = 50:41:7:2. There is a noticeable reduction in O in the film with a corresponding increase in N. There is also a significant decrease in B in the AlGaIn layer,

Figure 3-8 - EDX results of h-BN deposited on AlGaIn/GaN HS at the h-BN/AlGaIn/GaN interfaces and their corresponding SEM line scan image for (a) as deposited and (b) annealed at 500 °C for 300 s.

as well as a sharper boundary at the h-BN:GaN interface. The difference in the La:B stoichiometry from the target (1:6) compared to the film (1:18) is due to the difference in ionization energy between B and La [64]. Though there is a presence of La in the deposited BN, the measured

resistivity of the film was $> 10^{12} \Omega\text{cm}$ using 4-point probe measurement technique, indicating that the deposited h-BN has a highly insulating nature.

3.4.4 Thermal Conductivity by 3ω

The 3ω method was first developed by Cahill and Pohl to measure the thermal conductivity of amorphous solids in 1987 [75], and has since been extended for the thermal characterization of thin films [76]. This method uses a narrow metal wire deposited on the thin film. An AC current at frequency ω is applied to the metal wire, which causes a temperature wave at a frequency of 2ω to diffuse into the sample due to the Joule heating effect. The generated heat causes the resistance in the wire to oscillate at a frequency 2ω , as the metals resistivity increases linearly with temperature. This change in resistance causes the voltage drop across the wire to oscillate at frequency 3ω . The voltage oscillations can then be used to determine the thermal properties of the sample.

A one-dimensional (1D) heat conduction model is usually used to analyze the heat flow across the system. To ensure that the 1D heat conduction model is valid, the following conditions must be satisfied:

- 1) the thermal conductivity of the substrate (k_s) should be much larger than the thermal conductivity of the films (k_f).
- 2) the metal wire width ($2b$) should be much larger than the film thickness (d_f).

- 3) the film anisotropy should be small to minimize the heat spreading effects inside the film.
- 4) the metal wire width ($2b$) should be smaller than the thermal penetration depth ($1/q$) to make sure the line source approximation is valid.

Assuming the specified conditions are satisfied, the thermal properties of the thin film can be calculated using the differential method [77], [78]. In this method, the thin film is treated as a simple thermal resistor which adds a frequency-independent temperature oscillation to the film-on-substrate system. This method requires two measurements to be performed, one on the substrate and one on the film-on-substrate system. The temperature rise of the system can be written as:

$$k_f = \frac{d_f}{2} \left(\frac{b l T_{r+f}}{P} + \frac{b l T_r}{P} \right)^{-1} \quad (3.3)$$

where T_r is the temperature rise of the reference, T_f is the temperature rise of the film, P is the input power, d_f is the film thickness, b is the wire width, l is the wire length, and k_f is the thermal conductivity of the film.

To facilitate the 3ω measurements, a Ti/Au (20/100 nm) wire pattern 1 mm long by 10 μm wide was deposited on top of a AlGaIn/GaN on Si reference sample and a BN/AlGaIn/GaN on Si sample. The sample was then attached to a 16-pin integrated circuit package using silver paste, and electrical connections were achieved using a gold wire bonding process. The patterns were measured to have a resistance of 32-36 Ω at room temperature. Figure 3.9 shows the temperature oscillation as a function of frequency for the BN film on the AlGaIn/GaN on Si substrate.

Figure 3-9 – The real part of the temperature oscillation for optimized h-BN on GaN HS.

Figure 3-10 – Thermal conductivity of polycrystalline h-BN sheets as a function of grain size at 300 K, 600 K and 900 K. Data points represent molecular dynamics results. Dashed lines are the finite element predictions for the thermal conductivity of polycrystalline h-BN films with larger grain sizes. [81]

Using equation 3.3, the thermal conductivity of the film was calculated to be 9.52 W/mK. For comparison, a 120 nm SiN on GaN sample deposited via PECVD was also fabricated and measured using the same method. The SiN sample was measured at 0.35 W/mK. The measured BN films thermal conductivity is significantly lower than that of bulk h-BN (400 W/mK) or few layer h-BN (300 W/mK for 11 layers [79], 751 W/mK for 1 layer [80]). The lower thermal conductivity is likely due to the nano-crystalline structure of the film [81], as described in chapter 3.4.2. This nano-crystalline structure creates significant thermal boundaries in the film, reducing its thermal conductivity as seen in Fig 3.10. The grain boundary resistance plays a significant role in the reduction in film thermal conductivity. With reduced grain size, the thermal conductivity of the film decreases significantly due to phonon-defect scattering [81]. However, compared to the conventional SiN sample used for current GaN HEMT passivation, the HiPIMS deposited BN film has ~27 times higher thermal conductivity, making it a promising replacement for SiN as a thermal reduction layer on GaN HEMT devices.

3.4.5 Atomic Force Microscopy

For the purpose of examining the surface morphology of the h-BN films, AFM scanning was carried out. The AFM scanning was executed on a 13 mm square sample of optimized h-BN on AlGaIn/GaN HS. The scan area was a 5×5 μm square for all samples. Figure 3.10 shows the AFM images of (a) as grown AlGaIn/GaN, (b) h-BN and (c) annealed h-BN deposited

Figure 3-11 – AFM images of (a) as grown AlGaIn/GaN HS, (b) h-BN deposited on AlGaIn/GaN HS, and (c) annealed h-BN deposited on AlGaIn/GaN HS at 450 °C for 300 s.

on AlGaIn/GaN HS at 450 °C for 300 s. It can be seen from Figure 3.10(b) that the morphology of the h-BN film tends to follow the surface features of as grown AlGaIn/GaN HS. The root mean square surface (rms) roughness of the as grown AlGaIn/GaN HS surface, after h-BN deposited AlGaIn/GaN HS and after annealing of h-BN deposited AlGaIn/GaN HS were measured as 0.535 nm, 0.427 nm, and 0.376 nm respectively. This indicates that the deposited h-BN films are relatively smooth without any noticeable anomalies. The annealed h-BN film at 450 °C for 300 s exhibited slightly lower rms roughness values than the as-deposited h-BN film, although the minimal difference in surface morphology was observed (see figure 3.10(c)).

3.5 Hall Measurements of h-BN on AlGaIn/GaN (Hall)

Hall measurements were performed at room temperature to see the effects of the h-BN deposition on the 2DEG properties. Figure 3.12 shows the normalized sheet resistance and Hall mobility of AlGaIn/GaN HSs

versus the different conditions (before h-BN deposition, after h-BN, and with the insertion of a SiN buffer layer). After depositing 300 nm of h-BN deposition on the AlGaIn/GaN HS, there is a 64.5 % increase in sheet resistance (from 467 $\Omega/\square$ to 768 $\Omega/\square$). This is attributed to the plasma damage to the 2DEG channel during the sputtering process [82]. There is also a corresponding decrease of 67 % in the 2DEG. During the h-BN deposition, B is incorporated into the AlGaIn barrier region as shown in chapter 3.4.3. Penetration into the heterostructure causes significant deterioration of the 2DEG mobility due to scattering as well as increasing leakage current via trap assisted tunneling [83]. The sputtering related damage during the deposition of the h-BN on AlGaIn/GaN HS has been recovered by a post deposition annealing process (see chapter 3.5).

In order to verify the influence of structural damage to the AlGaIn barrier, the AlGaIn barrier covered with a protective film of 20 nm of SiN by plasma enhanced chemical vapor deposition (PECVD) at 300 °C before the deposition of h-BN by HiPIMS. After the SiN deposition, there was a 9.1 % reduction in sheet resistance and a 7 % decrease in μ_H compared to a control GaN sample with a room temperature sheet resistance (R_{sh}) of 467 $\Omega/\square$, a Hall mobility (μ_H) of 1430 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and a sheet carrier concentration (n_s) of $9.37 \times 10^{12} \text{ cm}^{-2}$. This can be explained by the surface screening effect [84], [85]. No significant change in R_{sh} or μ_H was seen after h-BN deposition on the SiN protected AlGaIn/GaN HS. This confirms that the SiN is effectively preventing the sputtering related structural damage (see Fig. 3.12). However, as SiN has a low thermal conductivity,

Figure 3-12 - Normalized sheet resistance (R_{sh}) and 2DEG mobility (μ_H) of AlGaIn/GaN HSs versus the different deposition conditions (Control, after SiN, after h-BN/SiN, after h-BN deposition)

this solution will introduce an additional thermal boundary resistance to the passivation scheme thus limiting the extraction of self-heat from the device.

3.5.1 Effects of Post-annealing of h-BN on AlGaIn/GaN (Hall)

As the low thermal conductivity of SiN has a detrimental effect on the total thermal conductivity of the passivation film, an annealing scheme was developed to help recover the 2DEG properties of the deposited h-BN sample on AlGaIn/GaN HS. The post-deposition annealing was

performed by rapid thermal annealing. The sheet resistance and Hall mobility gradually improved with the increase of post deposition annealing temperature (350 °C to 500 °C) as seen in Fig. 3.13. At 500 °C post-deposition annealing, about an 11% improvement in R_{sh} and 2% improvement in μ_H was observed compared to the sample without h-BN. Additionally, an increase of 10% in sheet carrier concentration was observed after annealing at 500 °C. The recovery may be due to the removal of sputtering induced structural damage as annealing has been shown to restore 2DEG properties [86], [87]. Higher temperature and longer annealing schemes showed a decrease in 2DEG properties. Therefore, there is a limit on the maximum annealing

Figure 3-13 - Normalized sheet resistance (R_{sh}) and 2DEG mobility (μ_H) of AlGaN/GaN HSs versus the different deposition conditions (Control, after SiN, after h-BN/SiN, after h-BN deposition and after post-deposition annealing temperatures). For post-deposition annealing, each of the samples were subjected for 300 s at the respective temperatures.

temperature and time at 500 °C for 300 s for maximum effectiveness.

These results show that it is feasible to maintain the 2DEG mobility of AlGaIn/GaN HS by the deposition of h-BN followed by post-deposition annealing without the insertion of SiN interlayer.

To verify that there was no change in h-BN properties after annealing, FTIR was performed before and after annealing (see Fig. 3.14). After annealing at 500 °C for 300 s there is no significant change to the peak intensity ratio $R_{780/1380}$, which was measured at 0.90 and 0.91 for before and after annealing respectively. This indicates that there is no structural change in the h-BN after annealing, which corresponds with the HRTEM measurements seen in chapter 3.4.2

Figure 3-14 – FTIR spectra of HiPIMS deposited h-BN on AlGaIn/GaN HS using optimized deposition conditions before and after annealing at 500 °C for 300 s.

3.6 Conclusion

Vertically ordered h-BN has been realized on AlGaIn/GaN HSs at room temperature and its passivation effects were also studied. The HiPIMS deposition conditions were optimized to achieve vertically ordered h-BN along the (0002) plane, which was confirmed by FTIR and HRTEM. AFM scans confirmed a low surface roughness of 0.535 nm, which was not affected by rapid thermal annealing up to 500 °C. After h-BN deposition, the 2DEG properties of the AlGaIn/GaN HS were degraded. The degradation was due to sputtering related damage during the deposition of h-BN by HiPIMS. This damage was shown to be prevented by the insertion of a 20 nm SiN layer. However, as SiN has a low thermal conductivity, this method is not ideal for device passivation. Post deposition annealing at 500 °C for 300 s helped to recover the 2DEG mobility completely, along with an improvement in sheet resistance and an increase in sheet carrier concentration by the removal of sputtering related structural damage. These results indicate that vertically ordered h-BN deposited at low temperature using HiPIMS could also be a promising material for the surface passivation of AlGaIn/GaN HEMT.

4. GaN MISHEMT using h-BN

4.1 Introduction

Conventional GaN HEMTs with Schottky metal gates suffer from high gate leakage current [9], [88]. The adoption of a gate insulator in metal–insulator–semiconductor HEMT (MISHEMT) has been shown to be very effective for reducing the gate leakage current in comparison with its conventional Schottky-gate counterpart. In particular, high-dielectric constant (high-k) oxide materials, such as Al_2O_3 , [11][12] HfO_2 [13] or ZrO_2 [14] have been investigated as gate insulators for MISHEMTs.

As described in Chapter 3, we have achieved vertically-ordered h-BN on AlGaIn/GaN grown on Si substrates at room temperature using a high-power impulse magnetron sputtering (HiPIMS) system [89] as a passivation layer. This method allows the deposition of considerably thick h-BN ($\sim 1 \mu\text{m}$) on AlGaIn/GaN HEMT structure at room temperature which can help to dissipate the heat from the hot spot of the transistor (gate-drain region). Room temperature h-BN deposition has an added advantage of not affecting any other subsequent fabrication processes. Through the post deposition annealing at 500°C for 300 s, we have recovered the 2DEG properties of AlGaIn/GaN HEMTs after the passivation of 300-nm thick vertically ordered (VO) h-BN as described in chapter 3.

The quality of interface between gate insulator and the semiconductor wafer is crucial for the AlGaIn/GaN MISHEMTs to achieve excellent and reliable performance. For example, in switching applications it is important

to investigate the interface traps as they could degrade device switching properties through charging and discharging [90]. Although researchers have realized MISHEMTs with h-BN,[91]–[93] no interface properties have so far been reported for VO h-BN on AlGaN/GaN heterostructures. Many characterization techniques have been developed to evaluate the interfacial quality. However, the most commonly used technique is capacitance-voltage (C-V) measurements due to its simplicity and reliability to evaluate the interfacial quality both qualitatively and quantitatively.

4.2 Device Fabrication

For this study, 4" diameter AlGaN/GaN HEMT on Si wafer was diced into 1/2" squares for the device fabrication. The AlGaN/GaN HEMTs devices were fabricated using standard GaN HEMT processing techniques. The fabrication processes consist of the following steps, as shown in Fig. 4.1:

- I. Mesa Isolation
- II. Ohmic contact formation (Source and Drain contact)
- III. h-BN deposition (for MISHEMT)
- IV. Schottky Gate contact formation
- V. Metal pad thickening
- VI. Surface passivation (for HEMT)

Figure 4-1 – Fabrication flow for a typical VO-hBN MISHEMT on AlGaIn/GaN on Si.

Mesa Isolation

It is necessary to electrically isolate two adjacent active devices to prevent leakage current between them. The device fabrication was started with the mesa isolation process. The etching of GaN/AlGaIn/GaN layer (~150 nm) was done by dry etching process using Inductive coupled plasma (ICP) system with an Ar/Cl₂/BCl₃ gas mixture. The GaN layer etching depth was much deeper than that of the 2DEG depth (~20 nm). The isolation current between the mesa region was obtained around 10⁻⁶ A/mm at +20 V which was measured after the ohmic contact formation.

Ohmic Contact

After optical lithography, samples were treated in 10% HCl:H₂O solution to remove the native oxide from the ohmic metal region. The ohmic contact was formed by e-beam deposition. The ohmic metal stack was

Ti/Al/Ni/Au (20/120/45/50 nm) followed by rapid thermal annealing at 825 °C for 30 s in a N₂ atmosphere. The annealing allows for low resistance ohmic contacts for the source and drain to achieve high drain current as well as low on-resistance in the device.

After annealing, the contact resistance was measured via the transmission line method (TLM). A linear TLM pattern with a series of ohmic metal pads was fabricated on an isolation mesa of AlGaIn/GaN heterostructure. The total resistance R_{tot} between 2 pads in the pattern can be calculated as [44]:

$$R_{tot} = 2 \frac{R_C}{W} + R_{sh} \frac{L}{W} \quad (4.1)$$

where R_C is the ohmic contact resistance, R_{sh} is the sheet resistance of the AlGaIn/GaN heterostructure between the two pads, L is the gap spacing and W is the pad width. As R_{tot} is proportional to the gap spacing, by plotting R_{tot} as a function of L the values of R_C and R_{sh} can be extracted. For this work, the ohmic contact resistance R_C was measured to be ~0.4 Ω.mm.

Gate Contact

Gate contact is the Schottky contact with the top GaN layer in GaN HEMTs. This is achieved by using metals with high work function. Thus, in order to achieve low gate leakage currents and high breakdown voltages, gate contact with high Schottky barrier height is required. In this work, Ni/Au (50/200 nm) gate metallization was formed using conventional lithography and e-beam evaporation followed by a lift-off process.

Interconnect Metallization

Finally, thick Ti/Au (50/1000 nm) was formed in order to withstand high current density that flows through the source and drain electrode. This Ti/Au (50/400 nm) metallization helps to protect the device from metal punch through during high voltage DC measurements.

h-BN Deposition

In this work, for MISHEMT fabrication, h-BN (~ 22 nm) was used as the gate dielectric and was deposited after the ohmic metal contact annealing and before the gate metal deposition. This thickness was confirmed using an TEM scan as seen in Fig 4.2. In order to carry out the thermal measurements, HEMT devices were also fabricated with ~300 nm h-BN

Figure 4-2 – TEM image of the h-BN dielectric under a MIS-diode.

deposited after the Schottky gate metal contact formation. The h-BN deposition and subsequent annealing was performed as described in Chapter 3.

4.3 MIS-diode Measurements

For the h-BN MIS-diodes, the gate choice was Ni/Au to be comparable to conventional HEMT fabrication. As this gate scheme has previously been shown to suffer from degradation after high temperature annealing [94], the devices were annealed at 450 °C for 300 s in an N₂ atmosphere. An energy band diagram of the VO h-BN MIS-diode was simulated as seen in Fig. 4.3. The Ni/h-BN interface was fixed at 0.66 eV, as determined from the IV curves present in this chapter. The following material constants were used: energy gap = 5.97 eV [95], conduction band offset to GaN = 1.95 eV [93], [95], dielectric constant = 5.39 (see chapter 4.3.2),

Figure 4-3 – Energy band diagram of the VO h-BN/GaN interface.

electron effective mass = 0.26 [96], hole effective mass = 0.47 [96], polarization = no, absorption coefficient = 1700 cm^{-1} [97], [98].

4.3.1 IV Characteristics

Current-voltage (I-V) measurements were carried out at room temperature on $200\mu\text{m}$ diameter diodes using an Agilent B1505A power device analyzer for both conventional Schottky and a h-BN MIS-diode. The results can be seen in Fig. 4.4. The h-BN MIS-diodes exhibited approximately two orders lower reverse leakage current ($2.75 \times 10^{-3}\text{ mA/cm}^2$) compared to the conventional Schottky diode ($6.03 \times 10^{-1}\text{ mA/cm}^2$). The reduction in reverse leakage current is due to the insertion of the h-BN, which increases the effective barrier height of the MIS-diode. There is also a corresponding decrease in forward gate current at +2 V compared to conventional Schottky devices. The higher gate bias voltage required for the MIS-diodes to get the same forward current as the conventional Schottky diode allows for high input voltages to be applied to the gate during device operation.

At low voltages, there is an increase current flow for the MIS-diodes compared to the Schottky diodes. This is attributed to an increase in the buffer leakage after the h-BN deposition. To verify this, the buffer leakage was measured between two pads spaced $10\text{ }\mu\text{m}$ apart with a mesa-etched region in between. The resultant current can be seen in Fig. 4.5. It can be observed that there is ~2 orders of magnitude higher buffer leakage at low voltages after h-BN passivation, increasing to ~3.5 orders

Figure 4-4 - Two terminal gate leakage current of Schottky-gate diode and BN MIS-diode as a function of voltage.

Figure 4-5 - Two terminal buffer leakage current for $10 \mu\text{m}$ spacing for unpassivated and with h-BN passivation.

at 20 V. This indicates that there is an introduction of a leakage path along the h-BN/GaN interface.

4.3.2 CV Characteristics

Standard capacitance-voltage (C-V) measurements were carried out at room temperature on 200 μm diameter diodes using an Agilent B1505A power device analyzer for both conventional Schottky and h-BN MIS-diode with. Figure 4.6 shows the typical C-V characteristics of VO h-BN MIS-diode and conventional Schottky diode at 1 MHz. Zero-bias capacitances of 373 nF/cm² and 136 nF/cm² were observed for 200 μm conventional diode and MIS-diode respectively. The negative threshold shift seen in the MIS-diode is associated with the large increase in thickness due to h-BN insertion.

Using the measured capacitance of at 1 MHz, the effective dielectric permittivity (ϵ_{BN}) of the deposited VO h-BN is estimated using the equation (4.2),

$$\epsilon_{BN} = \frac{d_{BN}}{A \left(\frac{1}{C_{MISdiode}} - \frac{1}{C_{HEMT}} \right)} \quad (4.2)$$

where, d_{BN} is the thickness the VO h-BN layer, A is the diode area and $C_{MISdiode}$ and C_{Diode} are the capacitances of MIS-diode and conventional Schottky diode, respectively. At zero-bias, the measured capacitances of 200 μm diameter conventional Schottky diode and MIS-diode was 373 nF/cm² and 136 nF/cm², respectively. From this, the estimated ϵ_{BN} is ~5.39. This is lower than the reported value for in-plane h-BN of 6.93 [57]. The lower effective dielectric constant is due to the fact that throughout

Figure 4-6 - C-V characteristics of Schottky and h-BN/AlGaIn/GaN MIS-diodes at 1 MHz.

the h-BN layer there are sections of h-BN that are not perpendicular to the substrate, especially closer to the h-BN/GaN interface. At any angle other than 90° to the substrate, the dielectric constant of the h-BN will decrease until it reaches that of horizontally ordered BN ($\epsilon_{BNhorizontal} = 2.87$) at 0° [56]. Due to the presence of variously angled VO h-BN in the deposited AlGaIn/GaN HEMT sample, the overall effective dielectric permittivity of the deposited VO h-BN layer is lower than that of purely in-plane h-BN.

4.4 Interface quality characterization via AC conductance method

The quality of interface between gate insulator and the GaN cap layer is crucial for the AlGaIn/GaN MISHEMTs to achieve excellent and reliable performance. For example, in switching applications it is important to

investigate the interface traps as they could degrade device switching properties through the charging and discharging phenomenon [90]. Many characterization techniques have been developed to evaluate the interfacial quality. However, the most commonly used technique is conductance-frequency (G-F) measurements due to its simplicity and reliability to evaluate the interfacial quality both qualitatively and quantitatively, as described in chapter 2.3.2.

Frequency-dependent conductance measurements were performed at selected biases to estimate the density of interface states (D_{it}) and trap time constant (τ_{it}) at the VO h-BN/GaN interface [44]. The frequency was varied from 1 kHz to 5 MHz over a voltage range from -5.6 V to -4.8 V. The resultant parallel conductance G_p/ω versus ω for the same V_G ranges can be seen in Fig. 4.7. The peaks in a G_p/ω versus ω are representations of the types of traps, and in this case, there are two peaks

Figure 4-7 - G_p/ω versus radial frequency plot for different gate voltages post gate annealed MIS diodes (-5.6 V to -4.8 V, step = 0.2 V).

present. These peaks correspondingly indicate the presence of both low frequency and high frequency traps. Assuming a discontinuity of trap levels for both the fast and slow traps as described in [44], [48], [49], [99], G_p described in equation 2.8 can be expressed as

$$\frac{G_p}{\omega} = \frac{q\omega D_{its}\tau_s}{1+\omega^2\tau_s^2} + \frac{q\omega D_{itf}\tau_f}{1+\omega^2\tau_f^2} \quad (4.3)$$

where ω is the radial frequency, D_{its} and D_{itf} are the interface trap densities while τ_s and τ_f are the trap time constants for slow and fast traps respectively. Using equation 4.3 as a fitting curve for the measured data in Fig. 4.7, the D_{it} and τ were extracted for both the slow and fast traps. Typically, fast and slow traps are defined by their time constants, with fast traps having a time constant $<10 \mu s$, while slow traps have a time constant above that. The extracted time constants for fast traps were between 1.65 to $6.07 \mu s$, while the slow traps have a time constant of $39.5 \mu s$ to $44.1 \mu s$. Using the trap time constants, the corresponding interface state energy can be estimated using equation (4.3) [44]:

$$E_T = -kT \ln(\tau_T \sigma_T v_t N_C) \quad (4.4)$$

where σ_T is the capture cross-section ($3.4 \times 10^{-15} \text{ cm}^2$), v_t is the thermal velocity of electrons ($2.6 \times 10^7 \text{ cm s}^{-1}$), T is the temperature, N_C is the effective density of states at the conduction band in GaN ($4.3 \times 10^{14} \times T^{3/2} \text{ cm}^{-3}$), and E_T is the trap state energy below the conduction band [45]. These time constants correspond to estimated interface state energy levels located at a depth ($E_C - E_T$) of 0.33 eV to 0.36 eV for fast traps and 0.407 eV to 0.410 eV for slow traps.

The distribution of interface trap states as a function of relative trap energy

level is shown in Fig. 4.8. The fast traps had an estimated D_{it} in the range of 1.2 to $1.8 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ while the slow traps estimated D_{it} was in the range of 2.6 to $3.4 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$. The fast traps are generally seen in HEMT and are associated with the AlGaIn/GaN hetero-interface, and are in a similar range for both pre and post annealed diodes [100]. The presence of slow traps can be associated with the VO h-BN/GaN interface. The D_{it} for the slow traps related to the BN/GaN interface is comparable to the h-BN/GaN interface trap density reported elsewhere ($\sim 2 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ at $E_C - E_T$ of 0.4 eV) using the PLS technique [101] on MW-PECVD deposited h-BN [91].

Figure 4-8 - Distribution of interface state density of MIS-diodes with VO h-BN as the dielectric for annealed MIS-diode. Inset is an expanded view of the slow traps.

4.5 Electrical Characteristics

The electrical properties of the MIS-HEMT were characterized in comparison with conventional HEMT, as seen in Fig. 4.9. The DC output current-voltage characteristics (I_D - V_D) with varied gate voltages can be seen in Fig. 4.9(a), with typical pinch-off featured. The VO h-BN MISHEMT showed a maximum drain current (I_{Dmax}) of 685 mA/mm at a gate bias of +4 V and a maximum extrinsic transconductance (g_{mmax}) of 93 mS/mm under a drain bias of 6 V. The enhanced response at a gate voltage of +2 V compared to the conventional HEMT is due to the surface passivation effects (increase in sheet carrier density) and the occurrence of low interface state density ($2.6 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$) at VO h-BN/GaN interface. This is a significant improvement over values reported for MW-PECVD ($\sim 460 \text{ mA/mm}$ [91]) at gate voltage of +4 V. The increase of sheet carrier density in AlGaIn/GaN HEMT structure after VO h-BN passivation ($7.29 \times 10^{12} \text{ cm}^{-2}$ to $1.10 \times 10^{13} \text{ cm}^{-2}$) was also confirmed by Hall measurements. Other passivation schemes (for example SiN) have also shown an increase in sheet carrier density after passivation [85], [102]. The threshold voltage (V_{th}) can be extracted by extrapolating the curve to the zero drain current in the plot of $(I_{Dsat})^{0.5}$ versus V_{GS} . Under a drain voltage of 6 V, the V_{th} for conventional HEMT is about -3.4 V. A negative V_{th} shift to -5.8 V was calculated for the VO h-BN MISHEMT, which is attributed to the increase of thickness due to the h-BN insertion.

Figure 4-9 - (a) DC I_D - V_D and (b) transfer characteristics ($V_D = 6V$) h-BN/AIGaN/GaN MISHEMT and conventional HEMT.

4.6 DC HEMT Characterization and Self Heating Analysis

DC characterization was performed at room temperature on two HEMT samples, one passivated with 300 nm VO h-BN and one with 120 nm conventional SiN passivation by PECVD. Figure 4.10 shows the combined plot of DC I_D - V_D of both the VO h-BN and SiN passivated HEMTS. The VO h-BN sample was annealed at 450 °C for 300 s to recover the 2DEG properties as described in chapter 3.5. The SiN passivated HEMT was measured up to 20 V while the VO h-BN device was measured up to 40 V, starting with a gate bias voltage of $V_G = +1$ V to avoid on-state device breakdown. The SiN passivated devices were measured up to 20 V because the devices suffered catastrophic burn out when they were measured at 40V, possibly due to larger heat retention in the channel. The SiN passivated HEMT exhibited a maximum drain current density (I_{Dmax}) of 704 mA/mm, while the VO h-BN device showed an I_{Dmax} of 421 mA/mm before annealing and 586 mA/mm after annealing. A summary of the DC performance of the passivated HEMT can be seen in table 4.1. As shown in Fig. 4.10(a), the SiN passivated HEMT shows a larger I_D reduction rate at $V_G = +1$ V compared to the annealed VO h-BN sample. A reduction rate of 14.9 mA/mm.V was calculated for the SiN passivated HEMT while a rate of 6.6 mA/mm.V was calculated for the VO h-BN passivated HEMT. By normalizing the $V_G = +1$ V as seen in Fig. 4.10(b), it can be seen that at a V_{DS} of +20 V, there is a 32% drop in current for the SiN passivated HEMT while only a 14% drop for the VO h-BN HEMT. This corresponds to a maximum dissipated power density (P_D

Figure 4-10 - (a) DC I_D - V_D and (b) normalized I_D - V_D curve for $V_G = 1V$ for SiN, VO h-BN, and annealed VO h-BN passivated HEMT.

$= V_D \times I_D$) of 9.6 W/mm for SiN passivated HEMT compared to 10.1 W/mm at $V_D = 20$ V and 15.8 W/mm at $V_D = 40$ V for VO h-BN passivated HEMT. The increase in maximum power for the VO h-BN devices could be attributed to a lower increase in channel temperature compared to SiN passivated devices, likely due to the higher thermal conductivity of the VO h-BN passivation film as described in chapter 3.4.3.

Figure 4-11 - Transfer characteristics of SiN, VO h-BN, and annealed VO h-BN passivated HEMT.

Table 4-1 – Summary of BN HEMT DC performance.

Device Passivation	I_{dmax} (mA/mm)	g_{mmax} (mS/mm)
SiN	704	141
VO h-BN As Deposited	421	118
VO h-BN RTA 450 °C	586	156

The measured I_D - V_G curves for $V_{DS} = 6V$ can be seen in figure 4.11. The HEMT extrinsic transconductances (g_{mmax}) measured were 141 mS/mm, 118 mS/mm, and 156 mS/mm for the SiN passivated HEMT, the VO h-BN passivated HEMT and the annealed VO h-BN passivated HEMT respectively. The decrease in g_{mmax} after the VO h-BN can be attributed to a decrease in 2DEG properties as described in chapter 3.5. Conversely, the increase in g_{mmax} after annealing is caused by an increase in carrier concentration. These properties indicate that the VO h-BN is providing an improved effect on the self-heating of the AlGaIn/GaN HEMT.

4.7 Conclusion

In conclusion, a quantitative investigation of the density of interface states and DC performance was carried out on VO h-BN/AlGaIn/GaN MISHEMT. Furthermore, the self-heating effect on DC performance of VO h-BN passivated HEMT was examined. About two order of magnitude lower reverse gate leakage current was observed in the fabricated MIS-diodes when compared with the conventional Schottky diodes. Two distinct interface trapping regions were observed. The fast traps had an estimated D_{it} in the range of 1.2 to $1.8 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ while the slow traps estimated D_{it} was in the range of 2.6 to $3.4 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$. The estimated interface state energy levels were located at a depth ($E_C - E_T$) from 0.33 eV to 0.36 eV for fast traps and 0.407 eV to 0.410 eV for slow traps. These results are comparable to D_{it} results for MW-PECVD h-BN. An enhanced output current (685 mA/mm) was obtained after the insertion of h-BN, which is

attributed to the low-density of defects in VO h-BN. These studies indicate that VO-BN can also be used as a potential dielectric in AlGaIn/GaN MISHEMT. The VO h-BN passivated HEMT showed a ~2.3× lower rate of I_{Dreduc} compared to conventional SiN passivation. This was due to the higher thermal conductivity of the VO h-BN lowering the channel temperature during device operation.

5. GaN MISHEMT using AlN

In previous chapters, a detailed analysis of h-BN as a gate dielectric for AlGaN/GaN Metal-Insulator-Semiconductor (MISHEMT) has been presented. However, h-BN has limitations in the improvement it offers as a gate dielectric, largely due to the deposition method. An alternative material is AlN which is deposited by low temperature epitaxy (LTE) which will be presented in this chapter. LTE allows for low temperature depositions (200 °C) while maintaining single crystalline properties required for low interface trap density. In this chapter, a systematic investigation of the DC performance as well as interface trap characteristics in LTE-AlN/AlGaN/GaN MISHEMTs on silicon was carried out. DC transfer characterization was carried out to determine LTE-AlN MISHEMT performance. Conductance-Frequency (G-f) measurement techniques were used to estimate the trap densities which were carried out, before and after post-gate annealing.

5.1 Introduction

Among non-oxide insulators, AlN is an attractive high-k dielectric material for III–N MISHEMTs due to its high breakdown field and high dielectric constant[103], [104]. In addition, AlN is of interest due to its high thermal conductivity ($200 \text{ WK}^{-1}\text{m}^{-1}$), which makes it suitable for use as a passivation layer to suppress the self-heating [52]. AlN has also been reported to help reduce current collapse [105]. There are two main methods used for the deposition of AlN namely metal-organic chemical vapor deposition (MOCVD) [106] and plasma-enhanced atomic layer

deposition (PEALD) [47], [100]. However, the growth temperature of MOCVD ($>600\text{ }^{\circ}\text{C}$) is not desirable for the fabrication of AlGaN/GaN HEMTs. Also, the use of a lower growth temperature has the advantage of preventing tensile strain-induced cracking of AlN layer in AlN based MIS-HEMTs [107], [108]. PEALD is a different approach to grow AlN films which can form a better interface with GaN at $350\text{ }^{\circ}\text{C}$ but with a low deposition rate [109]. Recently, Dikme et al. [110] realized thick single crystalline AlN layers on Si and sapphire substrates at $200\text{ }^{\circ}\text{C}$ using a novel technique called low-temperature epitaxy (LTE). In this technique, AlN is deposited as a combination of physical vapor deposition (PVD) and chemical vapor deposition (CVD). LTE also allows for thick ($\sim 1\text{ }\mu\text{m}$) crystalline films to be grown at low-temperatures which is compatible with III-V device processing. However, before LTE-AlN can be used as a passivation layer to reduce self-heating, the LTE-AlN/GaN interface must be quantified. In this chapter, material analysis of the LTE-AlN on AlGaN/GaN on Si is undertaken, followed by AlN MISHEMT fabrication. Finally, the current collapse of as-deposited and annealed devices are correlated to their interface states.

5.2 Low-temperature Epitaxy Aluminum Nitride

The LTE deposition of AlN was achieved through the collaboration with Dr. Y Dikme from AIXaTECH GmbH in Germany. The single crystalline AlN used in this work was grown by LTE at $200\text{ }^{\circ}\text{C}$ for a thickness of $\sim 8\text{ nm}$. To grow single crystalline AlN, a high surface mobility of the Al- and N- atoms are required. Standard growth methods use a high temperature

deposition process to achieve this surface mobility. However, in our LTE deposition, the surface mobility of Al- and N- atoms were enhanced by a combination of two different plasma sources. This helped to achieve sufficient surface mobility of Al- and N- atoms for the growth of single crystalline AlN at around 200 °C. Optimization of the LTE-AlN deposition was undertaken to improve the interface quality, as discussed in Chapter 5.5. Initial LTE AlN depositions used the same plasma power to deposit the entire thickness of the AlN. However, this turned out to have a poor quality at the interface. After optimization to improve the interface quality, the deposition steps are as follows. First, the sample was cleaned with a weak Ar/H₂ plasma to remove the native oxide. Next, an initial AlN layer was grown using nitrogen rich conditions. The AlN seeding layer (~0.5 nm) was grown at a sufficiently low plasma power to prevent damage of the GaN surface. This thin layer was then annealed in a nitrogen plasma to improve the AlN seed layer quality and to ensure that it continues the GaN lattice structure. The remaining AlN was then grown at a higher plasma power to the desired thickness of ~8 nm.

5.2.1 TEM/SEM analysis of AlN on AlGaIn/GaN

For the purpose of examining the surface morphology of the LTE-AlN films, scanning electron microscopy (SEM) was carried out on the surface of a sample with 1000 nm thick AlN film. From figure 5.1, it can be seen that there are clear triangular grain boundaries and voids in the crystal structure. This is indicative of preferential columnar growth. To verify if the entire film is columnar, high resolution transmission electron microscopy

(HRTEM) was performed on a ~ 8 nm sample, as seen in Fig. 5.1(b). The digital diffraction pattern obtained by fast Fourier transform (FFT) of AlN layer (as seen in Fig.5.1(c)) reveals a high-quality single crystal of hexagonal AlN with [0001] orientation perpendicular to the substrate

Figure 5-1 – (a) Surface SEM image of 1000 nm LTE-AlN/AlGaN/GaN, (b) Cross-sectional HRTEM image of the Ni/AlN/GaN interface. (c) Digital diffraction pattern of AlN layer obtained by FFT.

surface, indicating this technique can produce single crystalline AlN at low thicknesses. Therefore, the enhanced growth rate associated with thick layers is responsible for the columnar growth seen in the 1000 nm AlN sample. This indicates that there is a trade-off between film crystallinity and deposition rate, as the first ~10 nm is grown significantly slower to ensure that a quality interface is formed with the underlying GaN layer.

5.2.2 EDX analysis of AlN on AlGaN/GaN

A qualitative elemental analysis (Al, Ni, N, O, and Ga) was carried out on the deposited LTE-AlN film on GaN using electron-dispersive X-ray spectroscopy (EDX) profiling before and after annealing at 400 °C (see Fig. 5.2). In both profiles, there is a constant 18-20% O content throughout all layers. As this is constant regardless of which layer is being measured, it is highly unlikely that this is a true representation of the O content in the film and is most likely associated with surface contamination after the focused ion-beam cut. The exception to the constant O content is at the Ni/AlN boundary. At this interface, the O content reaches 39% and 38% for the unannealed and annealed samples respectively. This indicates that the surface of the AlN suffered from oxidation before the Ni gate was deposited. The long time between the AlN deposition and the gate deposition is a contributing factor to this oxidation. This also indicates that there may be a need to do a surface treatment before the Ni gate deposition. To verify the accuracy of the measurements, the Al content in the AlGaN layer was examined. The AlN content was 16% for both before and after annealing.

Figure 5-2 – EDX results of LTE-AlN deposited on AlGaN/GaN at the LTE-AlN/GaN/AlGaN interfaces for (a) as received (b) after annealing at 400 C for 300 s

Assuming perfect stoichiometry with no contamination, for the barrier layer consisting of $i\text{-Al}_{0.27}\text{Ga}_{0.73}\text{N}$ an Al content of 14% is expected. Therefore, there is up to 2 % error in the accuracy of the measurements. The average atomic ratio of Al:N for the LTE-AIN film were 1:0.61 and 1:0.72 for before and after annealing respectively. This indicates that the as-deposited AIN film tends to lack nitrogen, some nitrogen vacancies exist in the film, and annealing in a nitrogen atmosphere can effectively promote nitridation of the AIN film.

5.2.3 AFM analysis of AIN on AlGaN/GaN

For the purpose of examining the surface morphology of the LTE-AIN films, AFM scanning was carried out. The AFM scanning was executed on a 13 mm square sample of LTE-AIN on AlGaN/GaN HS. The AlGaN/GaN HS is similar to that shown in Chapter 3.3 (see Fig. 3.1). The scan area was a $5\times 5\text{ }\mu\text{m}$ square. Figure 5.3 shows the AFM images of LTE-AIN deposited on AlGaN/GaN HS. It can be seen that the morphology of the LTE-AIN film tends to follow the surface features of as grown AlGaN/GaN HS. The root mean square surface (rms) roughness of the LTE-AIN film on AlGaN/GaN HS was measured as 0.401 nm. Unlike with the 1000 nm film SEM image seen in chapter 5.2.1, there is no triangular AIN growths seen. This indicates that the surface morphology changes with a thick film size, and such triangular growth doesn't happen with thin films.

Figure 5-3 – AFM images of 10 nm as grown LTE-AlN on AlGaIn/GaN.

5.2.4 3ω analysis of AlN on AlGaIn/GaN

The 3ω method was used to characterize the thermal conductivity of LTE-AlN films. A detailed description of how the 3ω method works can be found in chapter 3.4.3. To facilitate the 3ω measurements, a Ti/Au (20/100 nm) wire pattern 1 mm long by 10 μm wide was deposited on top of a GaN reference sample and an LTE-AlN/GaN sample. The sample was then attached to a 16-pin integrated circuit package using silver paste, and electrical connections were achieved using a gold wire bonding process. The patterns were measured to have a resistance of

30-33 Ω at room temperature. Figure 5.4 shows the temperature oscillation as a function of frequency for the LTE-AIN film on the GaN substrate. Using equation 5.1,

$$k_f = \frac{d_f}{2} \left(\frac{blT_{r+f}}{P} + \frac{blT_r}{P} \right)^{-1} \quad (5.1)$$

where T_r is the temperature rise of the reference, T_f is the temperature rise of the film, P is the input power, d_f is the film thickness, b is the wire width, l is the wire length, and k_f is the thermal conductivity of the film, the thermal conductivity of the film was calculated to be 24.07 W/mK. For comparison, a 120 nm SiN sample was measured at 0.35 W/mK.

The measured LTE-AIN films thermal conductivity is significantly lower than that of bulk AIN (280 W/mK). While the measured AIN film has a

Figure 5-4 – The real part of the temperature oscillation for 1000 nm LTE-AIN on GaN HS.

lower thermal conductivity than that of bulk, this is to be expected. There are two main reasons for a reduction in thermal conductivity namely point defects and phonon scattering [111]. In AlN, C and O atoms typically substitute for N atoms, while Si substitutes for Al [112], which cause point defects.

Xu et al [111] showed that for the accumulated thermal conductivity, phonons with mean free paths larger than 0.3 μm (or 7 μm) contribute to 50% (or 10%) of heat conduction at room temperature. This implies that AlN thin films and devices with sub-micron features will exhibit strongly reduced effective thermal conductivity compared to the bulk value, even in the absence of point defects. This effect is so strong that for defect free samples, a 10 nm AlN film is expected to have a thermal conductivity of 25 W/mK while a 100 nm film is 110 W/mK (see Fig. 5.5(a)).

While the measured thermal conductivity of this sample is much lower than expected for a defect free sample, it is within the expected range for thermal conductivity for AlN films [113]–[122][123], as shown in Fig. 5.5(b). The reduction could be due to the deviation from typical stoichiometry as discussed in chapter 5.2.2, or due to the triangular structures present on the surface of the thick AlN layer as discussed in chapter 5.2.1. However, compared to the conventional SiN sample used for current GaN HEMT passivation, the LTE deposited AlN film has ~69 times higher thermal conductivity, making it a promising replacement for SiN as a thermal reduction layer on GaN HEMT devices.

Figure 5-5 – (a) Expected temperature dependence of thermal conductivity for different film thicknesses, for defect-free AlN films. Thinner films have weaker temperature dependence, due to the predominance of boundary scattering. (b) Thermal conductivity of AlN vs. sample thickness, at room temperature [111]. Solid lines are the theoretical calculation using different AlN defect densities. Diamond symbols are single crystal samples measured by Slack et al. [113] (in purple), and Rounds et al. [114]. Square symbols are a polycrystalline bulk sample [123] (in green) and various polycrystalline films (grey: Kuo et al. [116], purple: Duquenne et al. [115], black: Zhao et al. [117], red: Choi et al. [118], blue: Yalon et al. [119], yellow: Jacquot et al. [120], green: Bian et al. [121]. White round symbols correspond to amorphous thin films by Zhao et al. [107] and Gaskins et al. [122]

5.2.5 Hall Characterization of AlN on AlGaIn/GaN

Hall measurements were performed at room temperature to see the effects of the LTE-AlN deposition on the 2DEG properties. [67]. Ohmic contacts consisting of Ti/Al/Ni/Au (20/120/40/50 nm) were deposited on 13 mm squares by e-beam deposition, followed by rapid thermal annealing at 775 °C for 30 s in an N₂ atmosphere. After the LTE deposition of 400 nm of AlN on the AlGaIn/GaN HS, there is a 11.5 % reduction in sheet resistance (from 591 $\Omega/\square$ to 523 $\Omega/\square$). There is also an increase in sheet carrier concentration of 34.6 % (from 7.35 to 9.89 $\times 10^{12}$ cm⁻²) and a 16.0 % reduction in mobility (from 1440 to 1210 cm²V⁻¹s⁻¹). This can be explained by the surface screening effect [84], [85]. The sample was subjected to rapid thermal annealing at 400 °C and 450 °C for 300 s to determine the effect of annealing on the LTE-AlN film. After annealing, there was a negligible change in sheet resistance, but a 10 % increase in mobility and an 8.8% decrease in sheet carrier concentration. A summary of the LTE-AlN Hall characteristics can be seen in Table 5.1. One possible reason for the change in 2DEG characteristics after annealing is due to a reduction of interface states [124]. A reduction in interface states reduces the Coulomb scattering from the dielectric layer [125], thus enhancing the mobility.

Table 5-1– 2DEG properties of AlGaIn/GaN with and without AlN and its post deposition annealing at 400 °C and 450 °C for 300 s in N₂.

2DEG Parameters	AlGaIn/GaN HEMT structure			
	Without LTE-AlN	With LTE-AlN		
		As-dep.	Annealing temperature (°C)	
			400	450
Sheet Resistance ($\Omega/\square$)	591	523	520	512
Hall Mobility ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)	1440	1210	1330	1360
Sheet Carrier Concentration ($\times 10^{12} \text{ cm}^{-2}$)	7.35	9.89	9.02	8.76

5.3 Device Fabrication – MIS-diode and MISHEMT

The AlGaIn/GaN HEMT structure on Si substrate was grown by MOCVD technique. It exhibited room temperature sheet resistance of 591 $\Omega/\square$, a Hall mobility of 1440 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and a sheet concentration of $7.35 \times 10^{12} \text{ cm}^{-2}$ [126]. The device fabrication process started with mesa isolation by reactive ion etching (RIE) using a Cl_2/BCl_3 mixture. The ohmic contacts consisting of Ti/Al/Ni/Au (20/120/40/50 nm) were deposited followed by rapid thermal annealing at 825 °C for 30 s in an N₂ atmosphere. Transmission line measurements showed a contact resistance of 0.4 $\Omega.\text{mm}$. An 8 nm thick AlN gate dielectric was deposited by LTE at 200 °C. The gate metal contact is formed by E-beam evaporation. In this case, the Ni/Au (50/200 nm) gate metallization was formed using conventional lithography and e-beam evaporation followed by a lift-off process. After initial measurements, the devices were annealed at 400 °C for 300 s in a N₂ atmosphere. 400 °C was chosen as the 2DEG properties showed

minimal change between annealing at 400 °C and 450 °C (~2%, as seen in Table 5.1), and higher temperatures have been shown to cause degradation of Ni/Au gates [94], [127]. The optical microscope image of fabricated AlGaN/GaN MIS-Diode and MIS-HEMTs cross-section are shown in Fig. 6(a). The cross-sectional TEM image of fabricated

Figure 5-6 - (a) Optical image of AlN MIS-diode with its corresponding schematic cross-section, where the dotted line indicates the TEM location, (b) cross-sectional STEM image of the Gate region. (c) A simulated energy band diagram of under the gate.

AlGaIn/GaN MIS-HEMT shows the LTE-AlN thickness ~ 8.5 nm (See Fig. 6(b)).

5.4 Electrical characteristics of unpassivated AlGaIn/GaN MISHEMT

The DC characterization was conducted on MISHEMTs ($L_g/L_{sg}/L_{gd}/W_g = 2/2/2/(2 \times 100) \mu\text{m}$) at room temperature using Cascade Microtech summit 11000M Tesla probe station integrated with B1505A Power Device Analyzer/Curve Tracer. Figure 5.7 shows (a) the capacitance-voltage (C-V) and (b) gate leakage current (I_{leak}) characteristics of Schottky diode (MS-diode), LTE-AlN MIS-diode with and without post-gate annealing. At zero-bias, the capacitance density of 373 nF/cm^2 and 302 nF/cm^2 for $200 \mu\text{m}$ diameter conventional Schottky diode and MIS-diode were obtained, respectively. After annealing, there is no significant change in capacitance density at 0 V. Using the C-V curves, the deposited dielectric layer thickness was determined to be ~8.5 nm by using equation (5.2),

$$d_{\text{AlN}} = \frac{\epsilon_{\text{AlN}} d_{2\text{DEG}}}{\epsilon_{\text{AlGaIn}}} \left(\frac{C_{\text{MIS-Diode}}}{C_{\text{Diode}}} - 1 \right) \quad (5.2)$$

where ϵ_{AlN} and ϵ_{AlGaIn} are the dielectric permittivity of AlN (9.14) and AlGaIn layer (9.0), respectively.[128], [129] The grown AlN thickness by LTE was also confirmed by transmission electron microscopy (TEM) in chapter 5.2.1.

With reference to Schottky diode, the LTE-AlN MIS-diode exhibited 2 orders of magnitude lower I_{leak} at -20 V (Fig. 5.7(b)). After post-gate

Figure 5-7 - (a) C-V characteristics and (b) two terminal I_{gleak} - V_G (200 μ m diameter diodes) for Ni/AlGaIn/GaN Schottky diode, as-deposited LTE-AlIn/AlGaIn/GaN MIS-diode and post-gate annealed MIS-diode at 400 °C.

annealing at 400 °C, MIS-diodes exhibited about an order of magnitude further reduction in $I_{g\text{leak}}$. The V_{on} for the devices were measured at 1.3 V, 5.2 V, and 5.6 V for the Schottky diode, unannealed MIS-diode and annealed MIS-diode respectively. From this it is clear that the interface properties of LTE-AIN on GaN/AlGaN has been improved after 400 °C annealing [130].

Figure 5.8 shows (a) current-voltage ($I_{\text{DS}}-V_{\text{DS}}$) and (b) transfer characteristics of LTE-AIN/AlGaN/GaN MISHEMTs without and with post-gate annealing at 400 °C. The as-deposited AIN MISHEMT showed a maximum drain current (I_{Dmax}) of 708 mA/mm at a gate bias of 4 V and a maximum extrinsic transconductance (g_{mmax}) of 129 mS/mm. After annealing, MISHEMT exhibited I_{Dmax} of 684 mA/mm at a gate bias of 4 V and g_{mmax} of 148 mS/mm. The decrease in I_{Dmax} after annealing originates from a change in 2DEG carrier concentration (n_s), as $I_D \propto n_s$. As shown in Table 5.1, after annealing at 400 °C, n_s was found to decrease by 9 % (from $9.89 \times 10^{12} \text{ cm}^{-2}$ to $9.02 \times 10^{12} \text{ cm}^{-2}$) which results in the 9 % reduction in I_{Dmax} . Similarly, the 15 % improvement of g_{mmax} after post-gate annealing is attributed to an increase in electron mobility as well as a reduction of interface states [124]. This is attributed to a reduction in Coulomb scattering from the dielectric layer near the AlGaN/GaN interface [125]. The enhanced mobility was confirmed by Hall measurements, which shows ~10 % improvement (from $1210 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ to $1330 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) in 2DEG Hall mobility (μ_n), as seen in Table 5.1. From the figure 5.8(b), it is clear that AIN MISHEMT exhibited an order of magnitude improvement in the device $I_{\text{ON}}/I_{\text{OFF}}$ ratio after the post-gate

Figure 5-8 - (a) DC I_{DS} - V_{DS} and (b) transfer characteristics as-deposited LTE AlN/AlGaIn/GaN MISHEMT and post-gate annealed MISHEMT at 400 °C.

annealing at 400 °C, which is due to the reduction of drain current at OFF-state. This is possibly caused by a reduction of traps at the AlN/GaN interface reducing the available leakage current conduction paths. The threshold voltages (V_{th}) of the devices were measured as -3.95 V, and -3.8 V for as-deposited MISHEMT and post-gate annealed MISHEMT at 400 °C, respectively. V_{th} can be expressed as

$$V_{th} = V_{th0} - \frac{Q_{it}}{C_{AlN}}$$

(5.3)

where V_{th0} is the threshold voltages without any interface states, Q_{it} is the interface-trapped charge density and C_{AlN} is the capacitance of the AlN layer. After annealing at 400 °C there is a minimal positive shift in threshold voltage which could be caused by a slight reduction of interface traps at LTE-AlN/GaN interface. This is verified by the frequency-dependent conductance measurements which will be discussed in section 5.5.2. A similar occurrence was also reported after post-gate annealing by Zhou et al. for Al_2O_3 and Shih et al. for HfO_2 [13], [124]. In these cases, it was postulated that the positive V_{th} shift was caused by a reduction in positively charged traps and interface traps or positive fixed/mobile charges and was confirmed by a reduction in calculated interface states after annealing.

Figure 5.9 shows pulsed I_D - V_D characteristics of (a) as-deposited MISHEMTs with LTE-AlN, and (b) MISHEMTs with post-gate annealing at 400 °C. The devices were subjected to the pulse width/period of 100 μ s/10ms and quiescent biases of (V_{GS0} , V_{DS0}) = (0,0) and (-6, 20) V were

Figure 5-9 - Pulsed I_{DS} - V_{DS} characteristics at quiescent bias points of $(V_{GS0}, V_{DS0}) = (0,0), (-6, 20)$ for (a) LTE-AIN MISHEMTs and (b) 400 °C annealed MISHEMTs. (c) Normalized I_D with I_{Dmax} for as-deposited LTE AIN/AlGaIn/GaN MISEMT and post-gate annealed MISHEMT at 400 °C vs the quiescent bias points $(V_{GS0}, V_{DS0}) = (0,0), (-6, 0), (-6, 20)$ V.

Table 5-2 - Summary of AIN MISHEMT performance before and after annealing.

Device	I_{gleak} (mA/cm ²)	I_{dmax} (mA/mm)	g_{mmax} (mS/mm)	D_{it} (cm ⁻² eV ⁻¹)	I_d/I_{dmax} (-6,0)	I_d/I_{dmax} (-6,20)
As-deposited	8.9×10^{-6}	708	129	2.6×10^{12}	0.92	0.91
RTA 400 °C	1.1×10^{-6}	684	148	6.8×10^{11}	0.99	0.94

used for this pulsed I-V measurements. The as-deposited LTE-AIN MISHEMT exhibited the I_D/I_{Dmax} ratio of 0.91 for both quiescent biases (V_{GS0}, V_{DS0}) = (0,0) and (-6, 20). This indicates that the devices exhibited around 9% drain current (I_D) collapse. After annealing at 400 °C the I_D/I_{Dmax} ratio of MISHEMT increases to 0.94. This indicates that about 3% I_D collapse suppressed after post-gate annealing at 400 °C. The improvement in current collapse in 400 °C annealed MISHEMT is possibly due to the reduction of interface traps at the AIN/GaN interface. The static on resistance was extracted to be 0.59, 0.68, and 0.61 mΩ/cm² for as grown, 400 °C annealed and 450 °C annealed respectively while the dynamic on resistance was calculated as 0.38, 2.09, 1.17 mΩ/cm² for as grown, 400 °C annealed and 450 °C annealed respectively. A summary of the AIN MISHEMT device performance can be seen in table 5.2

5.5 Interface measurements

5.5.1 Interface state density of as-deposited LTE-AIN

Films

Frequency-dependent conductance measurements were performed at selected biases to estimate the density of interface states (D_{it}) and trap time constant (τ_{it}) at the AIN/GaN interface [44]. A detailed analysis for the Frequency-dependent conductance method can be found in chapter 2.4. For the optimized LTE-AIN deposition, the frequency was varied from 1 kHz to 5 MHz over the gate voltage (V_G) range of -4.2 V to -3.4 V. Figure 5.10 shows the parallel conductance (G_p) G_p/ω versus ω for the same V_G

range. The two peak regions in the G_p/ω plots correspondingly indicate the presence of both low frequency slow traps and high frequency fast traps. Assuming a continuum of trap energy levels, G_p can be expressed as

$$\frac{G_p}{\omega} = qD_{its} \left(\frac{\ln(1+\omega^2\tau_s^2)}{2\omega\tau_s} \right) + qD_{itf} \left(\frac{\ln(1+\omega^2\tau_f^2)}{2\omega\tau_f} \right) \quad (5.4)$$

where ω is the radial frequency, D_{its} and D_{itf} are the interface trap density while τ_s and τ_f are the trap time constants for slow and fast traps respectively. In Fig. 5.10, the trap densities and time constants were extracted from the fitted curves using Eq. 2. As the corresponding peaks for the slow traps occur at much lower than the measurable frequencies, the interface trap density and trap time constant were estimated from the

Figure 5-10 – G_p/ω versus radial frequency plot for different gate voltages of LTE-AIN MIS-diode for the optimized LTE-AIN deposition (solid lines are fitting curves).

fitting parameters. Similar extraction of parameters has also been reported [41], [42]. Typically, fast and slow traps are defined by their time constants, with fast traps having a time constant $<100 \mu\text{s}$, while slow traps have a time constant above that. The extracted time constants for fast traps were between 53 to 654 ns, while the slow traps have a time constant of 437 μs to 3 ms. The trap time constants are only used in the extraction of the trap state energies. A similar range of AlN interface state time constants have also been reported elsewhere [8,11]. The trap state energy was estimated using the expression [16]. The trap state energy was estimated using equation 5.5 [44]

$$E_T = -kT \ln(\tau_T \sigma_T v_t N_C) \quad (5.5)$$

where σ_T is the capture cross-section ($3.4 \times 10^{-15} \text{ cm}^2$), v_t is the thermal velocity of electrons ($2.6 \times 10^7 \text{ cm s}^{-1}$), T is the temperature, N_C is the effective density of states at the conduction band in GaN ($4.3 \times 10^{14} \times T^{3/2} \text{ cm}^{-3}$), and E_T is the trap state energy below the conduction band [45]. The extracted traps energy levels were located at a depth ($E_C - E_T$) from 0.24 to 0.56 eV. The estimated D_{it} for both the slow and fast traps after LTE-AlN optimization are shown in Fig.5.11. The fast traps had an estimated D_{it} in the range of 6.7 to $8.2 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ within the energy interval of 0.24 to 0.30 eV below the conduction band, while the slow trap D_{it} was in the range of 6.8 to $78.8 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ with depth 0.44 to 0.56 eV below the conduction band.

A similar analysis was performed on a sample before the LTE deposition optimization. Before the LTE optimization, the fast traps had an estimated D_{it} in the range of 5.9 to $9.4 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ within the energy interval of

Figure 5-11 –Distribution of interface state density of as-deposited LTE-AIN MIS-diodes before and after AIN deposition optimization

0.26 to 0.30 eV below the conduction band, while the slow trap D_{it} was in the range of $9.6 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$ to $1.8 \times 10^{14} \text{ cm}^{-2}\text{eV}^{-1}$ with depth 0.44 to 0.57 eV below the conduction band. After optimization, the D_{it} is reduced by ~1.1 orders of magnitude. This improvement was achieved by optimization of the LTE conditions as mentioned earlier. The fast traps are generally seen in HEMT and are associated with the AlGaIn/GaN hetero-interface [100]. This is confirmed by the fact that the LTE-AIN optimization process had negligible effect on the fast traps. The presence of slow traps can be associated with the LTE grown AIN/GaN interface. As the energy of the traps is relative to the Fermi level in the semiconductor, variation of trap energy with voltage can be observed. Variations in time constants with voltage can be used to determine the

uniformity of trap states throughout the AlGaN/GaN and AlN/GaN interfaces. If there is an exponential dependence between the two, then there is uniformity in traps throughout the interface. This can be seen as a horizontal line in Fig.5.11. Such a horizontal line is present for the fast traps, signifying a uniform distribution of fast traps. However, for the slow traps there is no such exponential dependence. This indicates that the interface states in the AlN layer are not uniformly distributed [45]. A comparison between the minimum D_{it} values obtained in this study and the values using PEALD AlN [47], [100] and in-situ MOCVD AlN [106], [131] can be seen in Table 5.3. The measured minimum D_{it} value of LTE-AlN on GaN/AlGaN/GaN is in between the D_{it} values reported using PEALD (3.1×10^{11} to $3 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$).

5.5.2 Interface state density of annealed LTE-AlN Films

In order to quantify the effect of annealing on the interface states at the LTE-AlN/GaN interface, frequency-dependent conductance measurements were performed at selected biases to estimate the density of interface states (D_{it}) and trap time constant (τ_{it}). The frequency was varied from 1 kHz to 5 MHz over a wide range of gate voltages (V_G). Figure 5.12(a) shows the typical G_p/ω versus ω graph of LTE-AlN st-gate annealed at 400 °C measured at different V_G values between -4.1 V to -3.5 V. The two peak regions in the G_p/ω plots correspondingly indicate the presence of both low frequency slow traps and high frequency fast traps. The D_{it} calculations were performed using the conductance-frequency method, which is widely used for interface calculations [40]–

[42]. The estimated D_{it} for the slow traps are shown in Fig. 5.12(b) for the as-deposited LTE-AlN MIS-diode, as well as the MIS-diodes with post-gate annealing at 400 °C. The minimum D_{it} for the slow traps associated with the LTE-AlN/GaN interface were estimated as $7.6 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ and $5.0 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ for the as-deposited MIS-diode and MIS-diode with post-gate annealing at 400 °C, respectively. With reference to as-deposited MIS-diode, a reduction of D_{it} (24%) was observed in the MIS-diode after post-gate annealing at 400 °C. This reduction of interface traps can be associated with the suppression of I_D collapse. Annealing up to 400 °C helps to reduce the slow deep level traps thus reducing the remote Coulomb scattering from the AlN layer [132].

Table 5-3 - Benchmarking of extracted D_{it} values from AlN/GaN MIS diodes with other deposition technique.

Deposition Method	Thickness (nm)	Dep Temp (°C)	D_{it} ($\text{cm}^{-2} \text{ eV}^{-1}$)
PEALD	3	300	3×10^{12} [100]
PEALD	20	300	3.1×10^{11} [105]
In-situ MOCVD	11	1120	4.5×10^{12} [131]
In-situ MOCVD	5	600	1.1×10^{11} [106]
LTE Before optimization	6	200	2.6×10^{12} [40]
LTE After optimization	8.5	200	6.8×10^{11} [89]

Figure 5-12 – (a) Gp/ω versus radial frequency plot for different gate voltages of post-gate annealed LTE-AIN MIS-diode at 400 °C (solid lines are fitting curves). (b) Distribution of interface state density as a function of the gate voltage of as-deposited LTE-AIN MIS-diodes and post-gate annealed MIS-diodes at 400 °C.

5.6 Conclusion

In summary, the interface trap characteristics of LTE grown AlN on GaN/AlGaIn/GaN MIS-diodes were investigated using the parallel conductance method. The MIS-diode showed two orders of magnitude lower reverse leakage current at -20 V and five orders of magnitude lower forward current at +2 V as compared to the conventional Schottky diode. After post-gate annealing at 400 °C, about 15% of increase in g_{mmax} and an order of magnitude reduction of gate leakage was observed in LTE-AlN MISHEMT. About a 3% improvement of I_D collapse suppression was also observed after post-gate annealing at 400 °C. The fast traps were associated with the AlGaIn/GaN interface, and had an estimated minimum D_{it} of $6.7 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ while the slow traps were associated with the AlN/GaN interface and had a minimum of $6.8 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$. The fast traps were located within the energy interval of 0.24 to 0.30 eV below the conduction band while the slow traps were located 0.44 to 0.56 eV below the conduction band. After annealing there is a reduction of fast traps by 13% as well as the reduction of slow traps by 25%. These results warrant that LTE grown AlN can be used as an alternative method to achieve reasonably low D_{it} values at low temperature which is compatible for mainstream wafer processing.

6. Conclusions and recommendations for future work

6.1 Conclusions

AlGaIn/GaN based high-electron-mobility transistors (HEMTs) have demonstrated excellent high-frequency and high-power performance owing to their excellent material properties, such as large breakdown field, wide band gap and high electron mobility. [133]–[136] However, some of the major limiting factors that conventional GaN HEMTs with Schottky metal gates suffer from are a high gate leakage current, self-heating, and current collapse.[9] To help solve these issues, various gate dielectrics such as SiN[10], Al₂O₃[11], [12], HfO₂[13] or ZrO₂[14] have been used as both a passivation layer and gate dielectrics. However, while these materials help with solving the current collapse and gate leakage issues, their thermal conductivities are too low to help improve the self-heating issue faced by GaN based devices. To that end, in this thesis two high thermal conductivity materials using low temperature novel deposition methods have been investigated, namely h-BN via high power impulse magnetron sputtering (HiPIMS) and AlN via low temperature epitaxy (LTE).

Vertically ordered (VO) h-BN has been realized on AlGaIn/GaN Heterostructure (HS) at room temperature and its passivation effects were also studied. The HiPIMS deposition conditions were optimized to achieve vertically ordered h-BN along the (0002) plane. This was confirmed by FTIR and HRTEM. The surface roughness was examined using an AFM

scan to be 0.535 nm, which was not affected by rapid thermal annealing up to 500 °C. After h-BN deposition, the 2DEG properties of the AlGaIn/GaN HS were found to be degraded. The degradation was due to sputtering related damage during the deposition of h-BN by HiPIMS. This damage was shown to be prevented by the insertion of a 20 nm SiN layer, as well as by post-deposition annealing. These results indicate that vertically ordered h-BN deposited at low temperature using HiPIMS could also be a promising material for the surface passivation of AlGaIn/GaN HEMT.

VO h-BN was used as a gate dielectric for AlGaIn/GaN MISHEMT. Furthermore, the self-heating effect on DC performance of VO h-BN passivated HEMT was examined. About two order of magnitude lower reverse gate leakage current was observed in the fabricated MIS-diodes when compared with the conventional Schottky diodes. Two distinct interface trapping regions were observed, fast traps and slow traps. The fast traps were associated with the AlGaIn/GaN interface while the slow traps were from the h-BN/GaN interface. The estimated value for the slow traps density of interface states (D_{it}) was in the range of 2.6 to $3.4 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. The estimated interface state energy levels were located at a depth ($E_C - E_T$) from 0.407 eV to 0.410 eV for the slow traps. These results are comparable to D_{it} results for MW-PECVD h-BN. An enhanced output current (685 mA/mm) was obtained after the insertion of h-BN, which is attributed to the low-density of defects in VO h-BN. These studies indicate that VO-BN can also be used as a potential gate dielectric in AlGaIn/GaN MISHEMT. The VO h-BN passivated HEMT showed a ~2.3 times lower

rate of I_{Dreduc} compared to conventional SiN passivation. This was due to the higher thermal conductivity of the VO h-BN lowering the channel temperature during device operation.

LTE grown AlN was also used as a gate dielectric on GaN/AlGaIn/GaN MIS-diodes and MISHEMT. The MIS-diode showed two orders of magnitude lower reverse leakage current at -20 V and five orders of magnitude lower forward current at +2 V as compared to the conventional Schottky diode. After post-gate annealing at 400 °C, about 15% of increase in g_{mmax} and an order of magnitude reduction of gate leakage was observed in LTE-AlN MISHEMT. There was about a 3% improvement of I_D collapse suppression after post-gate annealing at 400 °C. The fast traps were associated with the AlGaIn/GaN interface while the slow traps were associated with the AlN/GaN interface and had a minimum of $6.8 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. The slow traps were located 0.44 to 0.56 eV below the conduction band. After annealing there was a reduction of slow traps by 25%. These results warrant that LTE grown AlN can be used as an alternative method to achieve reasonably low D_{it} values at low temperature which is compatible for mainstream wafer processing.

6.2 Key contributions of this work

In this thesis, VO h-BN and AlN dielectrics materials with high thermal conductivity have been studied for MISHEMT applications for the first time. The key contributions of this thesis are:

- Successful development and optimization of VO h-BN deposition technique using high power impulse magnetron sputtering

(HiPIMS) at room temperature has been realized for the first time on AlGaIn/GaN HSs. This deposition technique which is achieved at room temperature is attractive as it is compatible to mainstream silicon manufacturing process.

- Post deposition annealing scheme was developed to recover the 2DEG mobility completely, along with an improvement in sheet resistance and an increase in sheet carrier concentration by the removal of sputtering related structural damage.
- Quantitative investigation of the density of interface states and DC performance was carried out on VO h-BN/AlGaIn/GaN MISHEMT. The measured interface trap density of $2.6 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ is comparable with benchmarked h-BN deposited by MW-PECVD. Furthermore, the self-heating effect on DC performance of VO h-BN passivated HEMT was examined. The VO h-BN passivated HEMT showed an improvement to self-heating compared to conventional SiN passivation.
- LTE grown AlN at low temperature (200°C) was used as a gate dielectric for AlGaIn/GaN MISHEMT for the first time. The fabricated MISHEMTs showed improved device performance such as reduction in gate leakage current and suppression of current collapse. A post-gate annealing scheme was devised which improved the transconductance by 15 % and reduced the gate leakage by 1 order of magnitude.
- Detailed analysis of the AlN/GaN interface properties were carried out using the AC conductance-frequency method. It was

determined that there are two distinct trapping regions: (i) the fast traps were associated with the AlGa_N/Ga_N heterointerface and (ii) the slow traps were associated with the Al_N/Ga_N interface. A post gate annealing scheme was developed to reduce the density of traps at the Al_N/Ga_N interface by 25%. This low interface trap density was comparable to MOCVD and PEALD deposited Al_N.

6.3 Recommendations for future work

In this thesis, an investigation into using low temperature deposited high thermal conductivity gate dielectrics was undertaken. While several promising results were discussed, there is still room for further improvement, namely:

- Although it was shown to be possible to deposit VO h-BN by HiPIMS at room temperature, further optimizations may be undertaken. By replacing the LaB₆ target with a pure B target, it might be possible to achieve h-BN films without the incorporation of La. Additionally, using an ion gun in addition to the regular HiPIMS system would increase the traction rate of single nitrogen atoms in the plasma. This could produce denser material phases, possibly improving the thermal conductivity of the film.
- Using implantation instead of mesa etching for the h-BN gate dielectric devices may lead to improved leakage performance. It was observed that after the h-BN deposition the buffer leakage increased by ~3 orders of magnitude, indicating the deposition process introduced new leakage paths. This also places a limit on

the leakage improvement. By using implantation, this may be reduced.

- Pre-surface treatments such as a plasma pre-treatment or sulphur passivation to remove or passivate the native oxide layer to the sample before h-BN or AlN deposition may also improve interface quality.
- Further investigation into the reduction of self-heating achieved using these low temperature high thermal conductivity materials is required. As both of these materials and deposition methods allow for thick growths, the advantage of applying a thick passivation layer ($\sim 1\mu\text{m}$) may prove to be useful in preventing self-heating.

7. Publication List

Journal Publications:

- **M. Whiteside**, S. Arulkumaran, S. S. Chng, M. Shakerzadeh, E. H. T. Teo, and G. I. Ng, "On the recovery of 2DEG properties in vertically-ordered h-BN deposited AlGa_N/Ga_N heterostructures on Si substrate," *Appl. Phys. Express*, pp. 0–6, 2020, doi: 10.35848/1882-0786/ab92ee.
- **M. Whiteside**, S. Arulkumaran, Y. Dikme, A. Sandupatla, and G. I. Ng, "Improved Interface State Density by Low Temperature Epitaxy Grown AlN for AlGa_N/Ga_N Metal-Insulator-Semiconductor Diodes," *Mater. Sci. Eng. B Solid-State Mater. Adv. Technol.*, 262, 114707, 2020 doi: 10.1016/j.mseb.2020.114707.
- **M. Whiteside**, S. Arulkumaran, Y. Dikme, A. Sandupatla, and G. I. Ng, "Post gate annealing effects on AlGa_N/Ga_N MISHEMT with Low-Temperature Epitaxy grown AlN on Si substrate," *Electronics*, 9, 1858, 2020, doi: 10.3390/electronics9111858.
- **M. Whiteside**, S. Arulkumaran and G. I. Ng, "Demonstration of Vertically-Ordered h-BN/AlGa_N/Ga_N Metal-Insulator-Semiconductor High-Electron-Mobility Transistors on Si substrate," *Mater. Sci. Eng. B Solid-State Mater. Adv. Technol.*, 270, 115224, 2021, doi: 10.1016/j.mseb.2021.115224.
- S. S. Chng, M. Zhu, Z. Du, X. Z. Wang, **M. Whiteside**, Z. K. Ng, M. Shakerzadeh, S. H. Tsang, E. H. T. Teo, "Dielectric dispersion and

superior thermal characteristics in isotope-enriched hexagonal boron nitride thin films: evaluation as thermally self-dissipating dielectrics for GaN transistor," *J. Mat. Chem. C*, 28, 2020.

Conference Publications:

- **M. Whiteside**, G. I. Ng, S. Arulkumaran, K. Ranjan, and Y. Dikme, "Low Temperature Epitaxy grown AlN Metal-Insulator-Semiconductor Diodes on AlGaIn/GaN HEMT structure," in *2019 Electron Devices Technology and Manufacturing Conference, EDTM 2019*, 2019, pp. 103–105, doi: 10.1109/EDTM.2019.8731261.
- Z. L. Ngoh, F. N. Leong, R. Y. Tay, **M. Whiteside**, S.S. Chng, J. J. Yu, S. H. Tsang, D. Tan, G. I. Ng, E. H. T. Teo, "Boron Nitride Coated Three-Dimensional Graphene as an Electrically Insulating Electromagnetic Interference Shield," *IMWS-AMP 2019 - 2019 IEEE MTT-S Int. Microw. Work. Ser. Adv. Mater. Process. RF THz Appl.*, pp. 127–129, 2019, doi: 10.1109/IMWS-AMP.2019.8880119.

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