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Growth and Fabrication of Carbon-Based Three-Dimensional Heterostructure in Through-Silicon Vias (TSVs) for 3D Interconnects

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Abstract

Carbon nanomaterials such as graphene and carbon nanotubes (CNTs) have recently received much attention as potential materials proposed for integration in the future semiconductor technologies because of the advantageous properties particularly in thermal and electrical conductivities. Among them, three-dimensional (3D) pillared CNT-graphene nanostructures are especially attractive due to the desirable out-of-plane and in-plane properties. In this work, a growth and fabrication process flow of CNT-graphene heterostructure as filler of TSV for 3D interconnects was designed and explored. First, experiments for the fabrication of top wafer with unfilled TSV of various diameters (5-50 μm) and bottom wafer with patterned graphene electrodes and catalyst deposition were completed successfully. Next, top TSV wafer and bottom graphene wafer were bonded and manually ground followed by wet and dry etching to completely remove the handling wafer and buried oxide, exposing the underlying TSV. CNT growth was conducted for both within TSV and free standing on the graphene. Compared to the free-standing growth with sufficient length ($\sim 334\mu\text{m}$) and high density ($\sim 10^{11} \text{ cm}^{-2}$ estimated), few via holes have CNTs grown and none was completely filled by CNTs. The inhibited growth of CNTs within unfilled TSV can possibly be attributed to several process-engineering steps involved in wafer-bonding, grinding and wet/dry etching. Further modification and optimization of the process steps need to be done in order to attain higher CNT fillings within the unfilled TSV.

Introduction

In the recent two decades, owing to the excellent electrical [1, 2], mechanical [3, 4] and thermal [5, 6] properties, carbon nanomaterials such as graphene and carbon nanotubes (CNTs) are emerging rapidly as potential materials proposed for a wide range of applications in the future semiconductor technologies. Among them, hybrid carbon nanostructures, for example, pillared CNT-graphene nanostructures are especially attractive [7]. Benefiting from a combination of one-dimensional (1D) nanotubes and two-dimensional (2D) graphene, three-dimensional (3D) CNT-graphene heterostructure can possess desirable out-of-plane properties [8–10] while maintaining in-plane properties, attracting numerous innovative applications including new efficient electrodes for fuel cells [11], nano-porous structures for hydrogen storage [12] and supercapacitors [13], tailored orthogonal thermal transport materials [14] and building blocks for nano/microscale integrated devices [15,16].

To date, many attempts for the fabrication of CNT-graphene hybrid materials [17-20] have been done successfully. For instance, Lee et al [20] reported the fabrication and characterization of a hybrid system with

vertical CNTs grown on reduced graphene films composed of overlapping and reduced graphene oxide platelets, which was found to have ohmic electrical contacts throughout all junctions of CNT/metal-catalyst/graphene-film. Subsequently, Zhu et al [21] developed a method to grow single-wall carbon nanotubes (SWCNTs) on the graphene seamlessly, also showing that an ohmic contact formed between the as-grown CNTs and graphene. In their reports, the covalent transformation of sp^2 carbon between the planar graphene and the vertical-aligned SWCNTs was clearly observed at the atomic resolution level by scanning transmission electron microscopy (STEM) [21]. Recently, Ghosh et al [22] developed a process flow for growth of multi-wall carbon nanotubes (MWCNTs) on top of semi-metallic few-layer graphene (FLG) and measured that the FLG/CNT contact resistance (5.8 k Ω) of a single CNT was about 6 times smaller than the Cu/CNT contact resistance (35.15 k Ω) under comparable growth and measurement conditions. The good electrical property of the CNT-graphene heterostructure towards three dimensions suggests that it can possibly have a potential application in 3D interconnects.

In this work, a growth and fabrication process flow was designed and explored for the possibility of replacing both conventional metals in through-silicon vias (TSVs) and horizontal metals at back-end-of-line (BEOL) in 3D IC by the CNT-graphene heterostructures. The advantages include: 1) less thermal mismatch stress in TSV compared with the conventional metal due to the low coefficient of thermal expansion (CTE) of CNTs compared with that of metal [23]; 2) assisting heat dissipation with the high thermal conductivity of CNTs and graphene [23]; and possibly 3) lower contacting resistance of the CNT/graphene interface than that of the CNT/metal interface [22].

Experimental

Generally, the designed growth and fabrication process flow mainly contains three parts: 1) top wafer with TSV etching, 2) bottom wafer with graphene patterning and catalyst deposition and 3) process steps after top and bottom wafers bonded as shown in Fig. 1.

Process flow for the fabrication of TSVs starts with a bulk, 6" diameter silicon-on-insulator (SOI) wafer. The thickness of device layer, buried oxide layer and supportive handling wafer of the SOI is 20, 1 and 600 μm , respectively. Channel area, designed to leave a space for graphene and catalyst, was patterned on the device layer of SOI first. Standard lithographic techniques of spin-coating (S1813 positive photoresist), exposure (Karl Suss MA-6, Double Side Aligner) and standard developer were used for the patterning. Reactive-ion-etching (RIE) system (Oxford Plasmalab-80) was used to etch a depth of 50nm Si for the channel area. After that, the desired diameters of via holes were patterned using same

standard lithographic method. The designed diameters vary from 5-50 μm . Deep-Reactive-Ion-etching (DRIE) system (SAMCO's RIE-800iPB) was used to form 20 μm deep TSV through the device layer till the buried oxide stop, via the widely-used BOSCH process. After removing the photoresist hard-mask, the full wafer was sent into the furnace for thermal oxidation in order to form an oxide layer ($\sim 100\text{nm}$) on the sidewall of TSV for electrical insulation. The full wafer was then diced into small dies with 10mm x 10mm dimension. Fig. 2 shows the SEM images of the fabricated TSV with diameter 7, 14 and 48 μm . As shown in the SEM images, the sidewalls of vias were straight and did not show much over-etching at via bottom.

Fig. 1. Schematic illustration of the process flow

Fig. 2. SEM images of the cross-section of TSVs with a) 7, b) 14 and c) 48 μm diameters (depths are all 20 μm)

Original graphene wafer used in this work is purchased commercial 4" diameter silicon wafer (with SiO_2 550nm) with 7cm $\times$ 7cm single-layer graphene transferred on the top. The full wafer was manually cleaved into small dies with 12mm $\times$ 12mm dimension before processing. The quality of original graphene wafers was carefully examined by optical and Raman microscopy (Raman system: Witec Alpha 300R) before lithography (Fig. 3). Standard lithography process of spin-coating (AZ5214 positive photoresist), exposure (MJB4 Karl SUSS Mask Aligner) and developer were used for patterning graphene as the bottom electrodes. O_2 plasma etching (1 min, 60 W, 20 sccm oxygen flow) was carried out in the RIE system (Oxford Plasmalab-80) to etch off uncovered graphene area. The recipe of O_2 plasma etching was optimized for a complete clean of graphene but no over-etching off the underlying SiO_2 .

After graphene patterning, buffer/catalyst layer was deposited on the graphene electrodes using lift-off process. Negative photoresist (ma-N 1440) was used to pattern the area for buffer/catalyst layer deposition. 8 nm of Al, 2 nm of Al_2O_3 , and 1.1 nm of Fe were sequentially deposited inside e-beam evaporator at nominal vacuum of 5×10^{-6} mbar at low temperature ($< 80^\circ\text{C}$). Deposition speed was set as around 0.1~0.2 $\text{\AA}/\text{sec}$. Thin Al/ Al_2O_3 layer, i.e. the buffer layer, acts as an anti-diffusion barrier for the catalyst Fe during the high temperature process of CNT growth.

Fig. 3. Raman spectra images of the graphene before and after lithography process

Fig. 4. Optical images with 20x (left) and 50x (right) after graphene patterning and catalyst deposition: long strips are patterned graphene electrodes and round circles are deposited catalyst/buffer layers

Results and Discussion

Fig. 4 shows the optical images after graphene patterning and catalyst deposition. No serious cracks/peeling-off of the graphene was observed after lithography process. The quality of graphene was also checked by Raman microscopy after lithography process, which shows no significant increase of I_D ($\sim 1350\text{cm}^{-1}$)/ I_G ($\sim 1580\text{cm}^{-1}$) peak ratio, i.e. no severe graphene degrades (Fig. 3).

The two wafers, top TSV die and bottom graphene die, are then bonded face-to-face in a die-to-die bonder (FINEPLACER® matrix) with top-side alignment marks at room temperature by fusion bonding approach. Ar plasma (100W, 10s) was used as the activation of bonding process. Two dies were successfully bonded with good bonding strength. In order to expose the underlying TSV for CNT growth, the handling wafer and buried oxide layer of the top SOI needs to be removed. However, removing the handling wafer is a challenge because it is too thick ($\sim 600\mu\text{m}$). Grinding is usually used in the wafer processing to thinning down the thickness of full wafer. But for small die (10mm x 10mm) grinding, as there would be very little holding power on the die during the grinding process, risk of the die dislodging, damaged/missing during the process is high. On the other hand, KOH wet etching is an alternative method for the handling wafer removal. But the practical etching rate is very slow: etching rate of Si in 20% KOH solution at 80°C is $\sim 60\mu\text{m}/\text{hour}$, which means that it will take ~ 10 hours to etch-off all the $600\mu\text{m}$ thickness.

A trial process was done to remove the handling wafer by manually grinding $\sim 400\mu\text{m}$ depth using sand paper (Grid 280), following a long-time wet etching (3-4 hours, 80°C 20% KOH solution) to etch off the left $\sim 200\mu\text{m}$ Si. After that, the exposed buried oxide was removed by RIE. From the optical images (Fig. 5) after buried oxide removal, it can be seen that there are some color changes in via holes at different portions of the die. For example, TSVs at the ‘top left’ and ‘bottom left’ regions are green (i.e. the color of original 550nm SiO_2) while it turns to purple (i.e. $\sim 450\text{nm}$ SiO_2) at the ‘top right’ region. It is because manually grinding was not even for the whole surface area of the die. The remaining Si thickness at the ‘top right’ region was thinner than that at the ‘top left’ or ‘bottom left’ region. Due to the uneven Si thickness after grinding, the remaining Si at the ‘top right’ region was completely etched-off and the underlying buried oxide was started to be over-etched during the wet etching process while the solution was still etching the remaining Si at the ‘top left’ and ‘bottom left’ regions. Thus, the exposed buried oxide has thinner thickness at the ‘top right’ region compared with ‘top left’ and ‘bottom left’ regions. Eventually, when RIE was applied to remove the buried oxide for via holes open, the ‘top right’ region was over-etched down to the bottom oxide layer of bonded wafer, resulting in the color changes of TSVs.

After via holes opened, the whole die was sent into the Axitron Black Magic (BM) System for a growth of vertical-aligned multi-wall carbon nanotubes (MWCNTs) under the thermal CVD (TCVD) mode with hydrogen (H_2) and acetylene (C_2H_2) gas flows. Pre-growth and CNT growth were set at $600/700^\circ\text{C}$ with 30sec/30min, respectively. C_2H_2 and H_2 gas flows during the CNT growth were set as 200/600 sccm respectively. On the other hand, another piece of bottom die

after the process of graphene patterning and catalyst deposition (as shown in Fig. 4) was used for the free-stranding CNT growth as a comparison. The CNT growth conditions were set as the same except for the growth time reduced to 5min.

Fig. 5. Optical images after the handling wafer and buried oxide removal: exposed TSVs at a) top left, b) top right, c) bottom left and d) bottom right region of the die

Fig. 6. a) SEM images of free-standing pillared CNTs grown on the graphene; b) Raman spectra images of the CNTs as-grown

Fig. 6 is the SEM and Raman images of free-standing CNT pillars grown on the graphene, which show the vertically aligned CNTs with sufficient length ($\sim 334\mu\text{m}$) and high density ($\sim 10^{11}\text{ cm}^{-2}$ estimated). Fig. 7 shows the TEM images of a single CNT with multi-walls more than 20. However, despite that the growth time was six times longer than that for free-standing CNTs, CNT growth was inhibited and severely affected within the unfilled TSV ($20\mu\text{m}$ diameter) as shown in Fig. 8. This drastic reduction in growth of CNTs can probably be attributed to the process-engineering steps involved in wafer-bonding, grinding and wet/dry etching. 1) Ar plasma activation of the bonding process and over etching of the buried oxide by RIE can possibly etch off the thin layer of catalyst, which leads to a shorter or none growth of CNTs. 2) Bonding and grinding process can possibly shift the top TSV die resulting in a large misalignment between via holes and patterned bottom catalyst (Fig. 8 b and c), leading to the partially filling of CNTs in TSV. 3) Long time over-etching of the buried oxide by KOH solution can damage or spreading the catalyst particles on sidewall or on the top surface of TSVs, leading to the scattered CNT growth (Fig. 8 c and d). Hence, it is reasonable that the CNT growth was quite restricted within the TSV after these process-engineering steps.

Fig. 7. TEM images of a single CNT (as-grown) with multi-walls

Fig. 8. SEM images for CNT growth within TSV: a) 3 out of 6 via holes have CNTs grown but none was completely filled by CNTs; b) a shift of top die leading to the partially filling of CNTs in the via, inserted figure is a Raman image of CNTs as-grown; the scattered CNT grown on c) sidewall and d) top surface of TSV

Conclusion

In this work, a growth and fabrication process flow of CNT-graphene heterostructure as filler of TSV for 3D interconnects was designed and explored. Compared to the free-standing growth of CNTs on the graphene, CNT growth within the unfilled TSV was very few owing to the process-engineering steps involved in wafer-bonding, grinding and wet/dry etching. Hence, process steps of TSV fabrication and conditions for CNT growth need to be modified and optimized in order to attain higher CNT fillings within the unfilled TSV.

Acknowledgments

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