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Effect of Capacitor Voltage Ripples on Submodule Active Power Control Limits of Cascaded Multilevel Converters

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Abstract—In the operation of cascaded H-bridge (CHB) converters and modular multilevel converters (MMCs) with energy storage or renewable power resources, unbalanced active power distribution among the submodules (SMs) is unavoidable. Depending on the operating conditions, there are certain upper and lower limits on the active power that can be processed by a single SM or a subset of SMs. The control system needs to restrict the SM power references to these limits, hence, accurate knowledge of the power limits is important. In existing methods to derive the power limits, the SM capacitor voltages are assumed to have negligible ripples, whereas in practice the ripples can be considerable. This paper analyzes the effect of capacitor voltage ripples on the SM active power control limits and highlights the importance of considering the ripple effect. A methodology is proposed to accurately incorporate capacitor voltage ripples in the derivation of SM active power control limits. Simulation and experimental results are provided to evaluate the effectiveness of the proposed methodology.

Index Terms—Active power control limits, cascaded H-bridge, capacitor voltage ripple, hybrid integration of energy sources, modular multilevel converter.

I. INTRODUCTION

Cascaded H-bridge (CHB) converters and modular multilevel converters (MMCs) are popular choices to connect renewable energy resources and energy storage systems to the power system [1]–[3]. Compared to the conventional two-level converter, these two converters provide evident advantages, such as modularity, excellent harmonic performance, low switching frequency, etc. [4].

Fig. 1(a) depicts the circuit representation of a phase of the CHB converter with N submodules (SMs). Fig. 1(b) depicts

Fig. 1. Circuit diagrams of the converters: (a) CHB converter and (b) MMC.

the circuit representation of a phase of the MMC, which consists of two arms and each arm has N SMs. Renewable power resources and energy storage systems are connected to the SMs, which enable the SMs to process active power. The control system allocates the active power reference to each SM with consideration of the integrated energy sources to achieve certain control objectives. For example, in a converter integrated with batteries, the SM power references are determined based on the states of charge (SoC) and states of health (SoH) of batteries [5], [6]. Another example is a converter integrated with photovoltaic (PV) panels, where the active power generation from each SM is affected by the irradiance and temperatures of the PV strings [7]. Therefore, the active power distribution can be unbalanced among the SMs.

The unbalanced active power distribution is especially important in systems with hybrid energy sources, where different SMs are integrated with different types of energy sources [8], [9]. A typical example is the use of second-life batteries in energy storage applications to reduce cost, where the batteries can have different power ratings, energy capacities and chemistries [10]. There is also the possibility of partial integration of batteries, which means batteries are added to some SMs instead of all the SMs [11], [12]. This hybrid/partial integration makes the active power distribution among the SMs highly unbalanced [13].

Depending on the operating condition (SM capacitor voltage reference, output voltage and current reference of the converter), every subset of SMs have upper and lower limits on how much active power it can process [14]. These limits are defined as the SM active power control limits (APCLs). When the system operates close to the boundaries, accurate knowledge of the APCLs becomes imperative for the control system. If the provided limits to the control system are beyond the actual APCLs, then the controller may allocate power

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Fig. 2. Circuit diagram of an SM with the IAI between its batteries and capacitors.

references to some SMs that are beyond the actual limits, which means those SMs will not be able to track the references and the converter operation can become unstable. On the other hand, setting the APCLs too low will result in suboptimal operation of the system. Take a SM integrated with PV panels as an example. The PV power generation should be limited to the maximum APCL of this SM. Hence, if the calculated APCL is lower than the actual value, this SM will fail to extract the maximum power from the PV panels by unnecessarily curtailing the power to an incorrect limit. Therefore, it is important to derive the SM APCLs accurately.

A graphical method is proposed to derive the SM APCLs for CHB converters in [15], which is further developed as an analytical method in [16]. However, this research only investigates CHB converters with two SMs per phase. In [17], the authors investigated the APCLs of a single SM in the MMC. However, the APCL of a subset with multiple SMs are not analyzed, which is an important drawback as the APCLs of n SMs are not necessarily equal to n times the APCLs of one SM [18]. An analytical method is proposed in [14] to derive the APCLs of an arbitrary number of SMs in the MMC, which can be extended to the CHB converter.

A common limitation of all the mentioned studies is that the SM capacitor voltage ripples (CVRs) are assumed negligible in the analysis. However, the ripples can be large in practice. For example, in Fig. 2, an indirect active interface (IAI, i.e. a boost converter in this figure) is implemented between the capacitor and batteries to suppress the battery current ripples and regulate the average capacitor voltage [19]. In this case, the energy oscillation is burdened by the capacitor and thus, depending on the capacitance, the CVRs can be large [20]. Albeit, there is uncertainty on how much difference can be caused on the SM APCLs by the CVRs. To fill this gap, the main contributions of this paper are as follows: 1) investigating the effect of CVRs on the SMs APCLs and demonstrating its significance, and 2) proposing a methodology to incorporate the CVRs in the derivation of SM APCLs.

The rest of this paper is organized as follows. Section II introduces the operation principles of the converter and the derivation of SM APCLs, where negligible capacitor voltage ripples are assumed. Section III proposes a method to incorporate the CVRs in the derivation of SM APCLs. Simulation and experimental results are provided in Sections IV and V respectively, to verify the proposed analysis. Finally, Section VI summarizes this paper.

Fig. 3. Control scheme of an MMC integrated with batteries.

II. OPERATION PRINCIPLES OF THE CONVERTER

This section first introduces the control scheme of an MMC integrated with battery energy storage, where the knowledge of SM APCLs is needed. The conventional approach to derive the SM APCLs is also introduced, where CVRs are assumed negligible. Though the provided introduction only focuses on one arm of the MMC with N SMs, a similar analysis can be applied to the CHB converter. This is because they have similar topologies and operating principles in the sense they both synthesize a certain voltage waveform using a series connection of SMs while being subjected to a certain current waveform.

A. Control Scheme

Fig. 3 depicts the control scheme for an MMC integrated with battery energy storage [19]. In the arm current controller, the arm current reference (i_{arm}^*) is decided according to the dc-side power reference (P_{dc}^*), dc-side voltage (V_{dc}), ac-side power references and voltage ($\bar{P}_{ac}^*$, Q_{ac}^* and v_o) of the MMC. The output of the current controller block is the arm voltage reference [21].

In the SM power reference controller, the power reference for each SM is normally decided according to the SoC and SoH of batteries, where $\bar{P}_{SMi}^*$ represents the active power reference of the i th SM [5], [6]. The desired unbalanced power references can become unviable, which means they cannot be tracked by the corresponding SMs. To ensure the viability of the power references, a viability check and modification block is used, where the knowledge of the SM APCLs is required as an input [14]. If and only if the power references of all the subsets of SMs are within the corresponding APCLs, the power references are viable and can be allocated to the corresponding SMs. Otherwise, the SM power references need to be modified. Details of the viability check and modification are reported in [14]. The derivation of SM APCLs is introduced in Subsection II-B.

In the SM power controller, a moving average filter (MAF) calculates the average power of each SM (P_{SMi}), which is then compared to the reference ($\bar{P}_{SMi}^*$) to derive the error (ΔP_{SMi}). According to the error, a sorting algorithm is used to distribute the output voltage reference for each SM

(v_{SMi}^*), which regulates the active power of each SM to its reference and simultaneously synthesizes the output voltage of the converter arm [14].

The SM capacitor voltage controller regulates the SM average capacitor voltage ($\bar{v}_{Ci}$) to the reference (V_C) through the battery current reference (i_{Bi}^*). For a faster response, a feedforward component ($I_{Bi}^* = \bar{P}_{SMi}/v_{Bi}$, where v_{Bi} is the battery voltage) is added to the output of the PI-based capacitor voltage controller Δi_{Bi}^* ($i_{Bi}^* = I_{Bi}^* + \Delta i_{Bi}^*$) [19]. Then, in the battery current controller, the battery current of each SM is regulated to its reference.

The controllers in Fig. 3 can also be applied to the CHB converter, except the arm current controller. In the CHB converter, the output current reference (i_{arm}^*) and voltage reference (v_{arm}^*) are decided based on the ac-side power and voltage ($\bar{P}_{ac}^*$, Q_{ac} and v_o) [13].

B. Active Power Control Limits with Negligible Capacitor Voltage Ripples

The average active power of one SM is calculated as:

$$\bar{P}_{SMi} = \frac{1}{T} \int_{t_0}^{t_0+T} v_{SMi}(t) i_{arm}(t) dt, \quad (1)$$

where T represents the fundamental voltage period and v_{SMi} is the instantaneous output voltage of the i th SM, respectively. To achieve the maximum power, the ac-side output voltage of an SM should be maximum when the arm current is positive, and minimum when the arm current is negative. This can be generalized to an arbitrary combination of n SMs, where $n \in [1, N]$. Hence, the maximum APCL of a combination with n SMs can be derived as:

$$\bar{P}_{max}^n = \frac{1}{T} \int_{t_0}^{t_0+T} v_{max}^n(t) i_{arm}(t) dt, \quad (2)$$

$$v_{max}^n(t) = \begin{cases} v_{max}^n(t) & \text{if } i_{arm}(t) \geq 0; \\ v_{min}^n(t) & \text{if } i_{arm}(t) < 0, \end{cases}$$

where $\bar{P}_{max}^n$ represents the maximum active power of n SMs. v_{max}^n and v_{min}^n represent the maximum and minimum allowed output voltage of n SMs, respectively. Similarly, the minimum APCL of n SMs can be derived as:

$$\bar{P}_{min}^n = \frac{1}{T} \int_{t_0}^{t_0+T} v_{min}^n(t) i_{arm}(t) dt, \quad (3)$$

$$v_{min}^n(t) = \begin{cases} v_{min}^n(t) & \text{if } i_{arm}(t) \geq 0; \\ v_{max}^n(t) & \text{if } i_{arm}(t) < 0. \end{cases}$$

The maximum and minimum output voltages of unipolar SMs, which means the output voltage can be either zero or positive, are derived in [14]:

$$v_{max}^n(t) = \min[nV_C, v_{arm}^*(t)], \quad (4)$$

$$v_{min}^n(t) = \max[0, v_{arm}^*(t) - (N - n)V_C], \quad (5)$$

where V_C represents the capacitor voltage of one SM and v_{arm}^* represents the arm voltage reference. Extending to bipolar

SMs, whose output voltage can be negative as well, (4) and (5) are rewritten as:

$$v_{max}^n(t) = \min[nV_C, v_{arm}^*(t) + (N - n)V_C], \quad (6)$$

$$v_{min}^n(t) = \max[-nV_C, v_{arm}^*(t) - (N - n)V_C]. \quad (7)$$

This conventional analysis assumes constant capacitor voltages, i.e. capacitor voltages with negligible ripples. However, the CVRs can be notable in practice and neglecting their effect can cause significant errors in the derivation of APCLs. This is a major limitation of the conventional analysis, which this paper overcomes as explained in Section III.

III. ACTIVE POWER CONTROL LIMITS WITH CONSIDERING CAPACITOR VOLTAGE RIPPLES

This section proposes a method to incorporate the CVRs in the derivation of the SM APCLs. The proposed analysis considers one arm of the MMC with N SMs, but it can be readily applied to the CHB converter as they have similar topologies and operational principles (they both synthesize a certain voltage waveform using a series connection of SMs while being subjected to a certain current waveform).

A. Modeling of Capacitor Voltage Ripples

If the time-variant capacitor voltages of the SMs are known, their APCLs can be derived from (2)-(7). Although the arm current is common for all the SMs in one arm, the corresponding power references and the output voltage references of each SM can be different, which makes the SM capacitor voltages unequal. Nevertheless, to derive the APCLs of an arbitrary subset of n SMs, only the sum of the capacitor voltages of the n SMs in this subset and the capacitor voltage sum of the remaining $N - n$ SMs are needed. Thus, this subset of the n SMs and the subset of the remaining $N - n$ SMs can be considered as a clustered SM, respectively. The capacitor voltage of such a clustered SM, $v_C^n(t)$, is equal to the sum of the capacitor voltages of all the SMs within the cluster. The capacitor voltage reference of this clustered SM is nV_C , its capacitance is C/n (C represents the capacitance of a single SM), and its power reference is equal to the sum of power references of all the SMs in the cluster.

The CVR of this clustered SM depends on its power reference and output voltage reference. When the SM is charged with the maximum power, the power reference is the maximum APCL while the output voltage reference is $v_{max}^n(t)$ in (2). When the SM is charged with the minimum power, the power reference is the minimum APCL while the output voltage reference is $v_{min}^n(t)$ in (3). According to the relationship between the capacitor current and voltage, the capacitor voltage of this clustered SM is expressed as:

$$v_C^n(t) = \frac{\int_0^t i_C(t) dt}{C/n} + v_C^n(0), \quad (8)$$

where $i_C(t)$ represents the charging current into this clustered capacitor, and $v_C^n(0)$ represents the initial value of the capacitor voltage. As depicted in Fig. (2), the current $i_C(t)$ can be expressed as:

$$i_C(t) = i_{SM}(t) + i_{BC}(t), \quad (9)$$

where $i_{SM}(t)$ is the charging current from the ac side of the SM and $i_{BC}(t)$ is the charging current from the integrated energy sources.

The current from the ac-side can be expressed as:

$$i_{SM}(t) = \frac{v^{n*}(t)}{v_C^n(t)} i_{arm}(t), \quad (10)$$

where $v^{n*}(t)$ represents the output voltage reference of this clustered SM. The current from the integrated energy source is affected by the average power of this SM. Assuming the integrated energy sources are providing a constant power (such as batteries with the IAI in Fig. 2), to maintain the average capacitor voltage, the current is regulated as:

$$i_{BC}(t) = \frac{\bar{P}_{SM}^n}{nV_C}, \quad (11)$$

where $\bar{P}_{SM}^n$ represents the average power of the clustered SM and is equal to its power reference in the steady state, i.e. the maximum/minimum APCL. Though the model of $i_{BC}(t)$ in (11) returns a dc value, without loss of generality of the following analysis, the model can change according to different control objectives.

As can be concluded from (8)-(11), to derive the APCLs of a subset with n SMs in one arm, the sum of their capacitor voltages is required. However, to derive the sum of the capacitor voltages, the initial capacitor voltages and the power references, i.e. the APCLs, are required. Therefore, it is challenging to derive the APCLs and the capacitor voltages of the SMs because they affect each other. To overcome this challenge, a numerical method is used to calculate the capacitor voltages and APCLs iteratively as explained in Subsection B.

B. Iterative Active Power Control Limits Calculation Considering Capacitor Voltage Ripples

This subsection proposes a method to incorporate the CVRs in the derivation of APCLs. The analysis focuses on the derivation of the maximum APCL of a subset with n SMs ($n \in [1, N]$), but it can be readily applied to derive the minimum APCL of SMs without loss of generality. In the following analysis, all the estimated quantities are distinguished from the real ones with the hat sing " $\hat{\cdot}$ ". For example, the estimated sum of capacitor voltages of the n SMs is denoted as $\hat{v}_C^n(t)$, while the true value is $v_C^n(t)$.

The value of $\hat{v}_C^n(t)$ at any time step can be derived by rewriting (8) in a discretized form:

$$\hat{v}_C^n(kT_d + T_d) = \frac{\hat{i}_C^n(kT_d)T_d}{C/n} + \hat{v}_C^n(kT_d), \quad (12)$$

Fig. 4. Proposed method to derive SM APCLs with considering CVRs.

where T_d represents the sampling period and k represents the sampling instance. According to (9), (10) and (11), the estimated charging current, $\hat{i}_C^n(t)$, is expressed as:

$$\hat{i}_C^n(kT_d) = \frac{v^{n*}(kT_d)}{\hat{v}_C^n(kT_d)} i_{arm}(kT_d) + \frac{\hat{P}_{max}^n}{nV_C}, \quad (13)$$

where $\hat{P}_{max}^n$ represents the estimated maximum APCL.

According to (8), the average of $\hat{v}_C^n(t)$ in a fundamental cycle, represented as $\hat{v}_{C-ave}^n$, is derived as:

$$\hat{v}_{C-ave}^n = \frac{1}{T} \int_0^T \hat{v}_C^n(t) dt = \hat{v}_C^n(0) + \frac{1}{T} \int_0^T \left(\frac{\int_0^t \hat{i}_C^n dt}{C/n} \right) dt, \quad (14)$$

where $\hat{v}_C^n(0)$ is the estimated initial capacitor voltage. In other words, $\hat{v}_{C-ave}^n$ is a function of $\hat{v}_C^n(0)$, represented as $\hat{v}_{C-ave}^n(\hat{v}_C^n(0))$. If the estimated $\hat{v}_C^n(t)$ is equal to the true value $v_C^n(t)$ at each time step, its average value ($\hat{v}_{C-ave}^n$) should be equal to nV_C , the average of $v_C^n(t)$. Thus, defining a function:

$$f(\hat{v}_C^n(0)) = \hat{v}_{C-ave}^n(\hat{v}_C^n(0)) - nV_C, \quad (15)$$

the value of $f(\hat{v}_C^n(0))$ is zero if $\hat{v}_C^n(t)$ equals the true voltage $v_C^n(t)$. When $f(\hat{v}_C^n(0))$ is not zero, this value indicates how to update the estimated values. According to Newton's Method [22], the estimated $\hat{v}_C^n(0)$ can be updated as:

$$\hat{v}_{C-(K+1)}^n(0) = \hat{v}_{C-K}^n(0) - \frac{f(\hat{v}_{C-K}^n(0))}{f'(\hat{v}_{C-K}^n(0))}, \quad (16)$$

where $\hat{v}_{C-K}^n(0)$ is the estimate of $v_C^n(0)$ after K iterations, while $f'(\hat{v}_{C-K}^n(0))$ represents the derivative of the function $f(\hat{v}_{C-K}^n(0))$. According to (15), $f'(\hat{v}_{C-K}^n(0))$ is derived to be:

$$f'(\hat{v}_{C-K}^n(0)) = \frac{\partial \hat{v}_{C-ave}^n}{\partial \hat{v}_{C-K}^n(0)}. \quad (17)$$

Hence, assuming a minor increment ε to $\hat{v}_{C-K}^n(0)$, $f'(\hat{v}_{C-K}^n(0))$ can be calculated as:

$$f'(\hat{v}_{C-K}^n(0)) = \frac{\hat{v}_{C-ave}^n(\hat{v}_{C-K}^n(0) + \varepsilon) - \hat{v}_{C-ave}^n(\hat{v}_{C-K}^n(0))}{\varepsilon}. \quad (18)$$

TABLE I
PARAMETERS OF THE SYSTEMS

Parameter	Simulated MMC	Experimental CHB Converter
Number of SMs per arm, N	5	2
Capacitor voltage reference, V_C	3 kV	60 V
Battery voltage, V_B	2.4 kV	50 V
SM capacitance, C	5 mF	10 mF
Nominal output current (Peak), i_o	1.2 kA	20 A
Nominal output voltage, v_o	6.6 kV	110 V

A similar analysis is applied to estimate the capacitor voltages summation of the remaining $N - n$ SMs, represented as $\hat{v}_C^{N-n}(t)$. Its estimated initial value and the average are represented as $\hat{v}_C^{N-n}(0)$ and $\hat{v}_{C-ave}^{N-n}$, respectively. The value of $\hat{v}_C^{N-n}(0)$ can be updated with the same method of updating $\hat{v}_C^n(0)$.

After $\hat{v}_C^n(0)$ and $\hat{v}_C^{N-n}(0)$ are updated, the estimated values of $\hat{v}_C^n(t)$ and $\hat{v}_C^{N-n}(t)$ are calculated from (12). Afterwards, the estimated $\hat{P}_{max}^n$ is updated using (2)-(7), where nV_C and $(N - n)V_C$ are replaced with $\hat{v}_C^n(t)$ and $\hat{v}_C^{N-n}(t)$, respectively. The iteration process continues until the estimated values of the voltages and the APCLs converge to the true values. If the estimated voltages ($\hat{v}_C^n(t)$ and $\hat{v}_C^{N-n}(t)$) are close to the true values, then:

$$\hat{v}_C^n(T) \simeq \hat{v}_C^n(0), \hat{v}_{C-ave}^n \simeq nV_C; \quad (19)$$

$$\hat{v}_C^{N-n}(T) \simeq \hat{v}_C^{N-n}(0), \hat{v}_{C-ave}^{N-n} \simeq (N - n)V_C. \quad (20)$$

If $\hat{v}_C^n(t)$ and $\hat{v}_C^{N-n}(t)$ are close to the true values, the estimated $\hat{P}_{max}^n$ is also close to its true value.

The complete process of the proposed numerical method is displayed in Fig. 4. The initial estimated values of $\hat{v}_C^n(0)$ and $\hat{v}_C^{N-n}(0)$ can be chosen as nV_C and $(N - n)V_C$, while the initial $\hat{P}_{max}^n$ is the calculated value of $\bar{P}_{max}^n$ in (2) with the assumption of negligible CVRs. The proposed method applies to both the MMC and CHB converter. Moreover, since no constraint is imposed on the arm voltage/current in the analysis, the proposed method is generic, i.e., it is applicable irrespective of the control methodology and presence of any circulating current or common-mode voltage. In practice, the SM capacitance can have deviation, which affects the estimation of CVRs. This challenge can be overcome with available capacitance condition monitoring methods [23].

C. Effect of the Capacitor Voltage Ripples

To investigate the effect of the CVRs on the SM APCLs, the maximum SM APCLs of an MMC with bipolar SMs are studied. Parameters of the studied system are provided in Table I. The circulating current is zero and the ac-side output current of the converter is 1200 A (peak).

With the proposed method, the derived maximum APCLs of one SM on various operating points are provided in Fig. 5(a), where the CVRs are considered. The modulation index (m_a) varies between $[0.2, 1]$ and the phase shift (φ) between the output voltage and current of the MMC varies

Fig. 5. Derived results for one SM in the studied MMC under various operating points: (a) Derived maximum APCLs with considering CVRs, (b) amplitudes of CVRs, and (c) difference between the APCLs with and without considering the CVRs.

between $[0^\circ, 180^\circ]$. When m_a decreases, the maximum APCL increases. This is because when m_a decreases, the arm voltage requirement becomes lower, which provides higher flexibility for operating the SMs. When φ increases from 0 to 180° , the maximum APCL increases because the MMC changes from injecting active power to absorbing power from the ac-side.

Fig. 5(b) displays the amplitude of the CVR on the SM when it is charged with the maximum APCL. The ripple is normalized to the reference capacitor voltage (3 kV). Fig. 5(c) displays the difference between the derived maximum APCLs with and without considering the CVRs, which depicts the effect of the CVRs on the maximum APCLs. Representing the derived maximum APCL as $\bar{P}_{max}$ when CVRs are considered and the APCL as $\tilde{P}_{max}$ when the CVRs are ignored, the difference of these two values is normalized in Fig. 5(c) as:

$$\Delta \bar{P}_{max} = \left| \frac{\bar{P}_{max} - \tilde{P}_{max}}{\bar{P}_{max}} \right| \times 100\%. \quad (21)$$

According to Figs. 5(b) and (c), the effect of CVRs is highly

dependent on the phase shift (φ) between the MMC output voltage and current. When φ is close to 0, regardless of the modulation index and the amplitude of CVRs, the effect on the APCL is negligible (around 1% or less). However, when φ is close to 45° , the effect is considerable. For example, when $m_a = 1$ and $\varphi = 0$, the CVR amplitude is 9.47% but only changes the APCL by 1.03%. However, when $m_a = 1$ and $\varphi = 45^\circ$, the CVR amplitude is 9.19% and changes the APCL by 9.34%. In other words, the CVRs can have a considerable effect on the SM APCLs and should not be ignored.

Therefore, to accurately derive SM APCLs, the proposed method in Fig. 4 should be applied if the capacitor voltages contain notable ripples. In practice, if the control processing power is limited and the APCLs are calculated online, while the viability check is ongoing, the active power requirement of the converter can be evenly distributed among the SMs to ensure the viability of the power distribution. As the SM APCLs are decided by the operating point of the converter and not affected by the SM power references, the APCLs only need to be calculated and updated when the operating point changes. The APCLs can also be precalculated and stored in a look-up table for faster response.

IV. SIMULATION RESULTS

To verify the proposed analysis, simulation results are obtained on the MMC analyzed in Subsection III (parameters are given in Table I). Batteries are integrated into each SM with boost converters as in Fig. 2. The implemented control scheme is similar to the one in Fig. 3 except for the SM power references controller. In this paper, to verify the derived SM APCLs, the SM power references are manually decided and allowed to become unviable. When the power reference of one SM (or a subset of multiple SMs) exceeds its maximum APCL, the corresponding measured power will be saturated at the limit, which should be equal to the derived value if the proposed analysis is valid.

Simulation results displayed on Fig. 6 are obtained with $m_a = 0.9$ and $\varphi = 45^\circ$. The upper arm is discharging with 1.43 MW. Hereinafter in this section, the power values are all normalized to 1.43 MW. According to Fig. 5, the derived maximum APCL of one SM is 40.49% when CVRs are considered. Ignoring the CVRs, the derived maximum APCL becomes 43.73%. The relative difference between these two limits is around 8%.

Fig. 6(a) displays the power reference and average measured power of each SM during the simulation. As observed, before $t = 0.6$ s, even though the active power distribution among the SMs is highly unbalanced, the SMs can still track their corresponding reference power because the references do not exceed the APCLs. From $t = 0.6$ s to $t = 1.0$ s, the power reference of the first SM ($\bar{P}_{SM1}^* = 43\%$) is higher than the derived maximum APCL (40.49%) when CVRs are considered. Thus, this power reference is unviable and the measured power saturates at the derived limit. However, if the CVRs are ignored, the derived limit is 43.73% and this power reference will be considered as viable, which is incorrect. After

$t = 1.0$ s, the measured power of the first SM is not saturated at the derived APCL because the SM capacitor voltages have diverged, as displayed in Fig. 6(c). The capacitor voltages affect the SM APCLs.

In Fig. 6(b), $\bar{P}^{n*}$ and $\bar{P}^n$ represent the power reference and the measured power of a subset with n SMs (from the first SM to the n th SM), respectively. The corresponding maximum APCL is derived as $\bar{P}_{max}^n$ with the proposed method. As observed, before $t = 0.6$ s, each subset can track its power reference as the references do not exceed the limits. From $t = 0.6$ s to $t = 1.0$ s, when the references exceed the limits, the measured powers saturate at the corresponding derived limits. Results displayed in Figs. 6(a) and (b) verify the effectiveness of the derived SM APCLs using the proposed method. As can be seen, the proposed method provides accurate APCLs prediction because of the consideration of CVRs.

Figs. 6(c) and (d) depicts the measured capacitor voltage and battery current of each SM, respectively. Before $t = 0.6$ s, when each SM tracks its power reference, the capacitor voltages are balanced and battery currents are regulated. From $t = 0.6$ s to $t = 1.0$ s, even though the power references slightly exceed the APCLs, the capacitor voltage controller still regulates the voltages and battery currents. However, after $t = 1.0$ s, because the power references further exceed the APCLs, the SM capacitor voltages diverge. Moreover, since the capacitor voltages of the first and second SMs drop lower than the battery voltage in some intervals, the boost converter cannot regulate the battery current in those intervals. Consequently, pulses appear in the battery currents of these SMs, which deteriorate the health of the integrated batteries. This specific case demonstrates the importance of the power distribution viability, which requires the knowledge of SM APCLs.

Fig. 6(e) depicts the measured capacitor voltage of the first SM when it is charged with the maximum power and its estimate ($\hat{v}_C^1$) with the proposed method. The estimated voltage is close to the measured one, which verifies the effectiveness of the capacitor voltage estimation in the proposed method.

V. EXPERIMENTAL RESULTS

Experimental results are obtained on a CHB converter that is built with Imperix PEH 2015 full-bridge power modules. Parameters of the setup are given in Table I and a picture is provided in Fig. 7. Three RS 537-5488 lead-acid batteries are connected in series to the dc-side of each SM through a boost converter. Results are obtained with two fundamental frequencies of the converter output voltage (20Hz and 50Hz).

A. 20Hz Case

In this case, a $2.4\text{-}\Omega$ resistor, 6.1-mH inductor and 1.2-mF capacitor are connected in series to the output of the CHB converter as a load. The modulation index is 0.9. Considering the CVRs, the maximum APCL of one SM is derived to be 43.1%. However, if CVRs are ignored, the APCL is derived to be 45.5%. The relative difference is around 5%. Results are provided in Fig. 8.

Fig. 6. Simulation results of the MMC: (a) Power references and average measured powers of the SMs, (b) power references and average measured powers of clustered SMs, (c) SM capacitor voltages, (d) battery currents, and (e) measured capacitor voltage of the first SM and its estimated value when charging with the maximum power.

Fig. 7. Photo of the experimental setup.

Fig. 8. Experimental results with 20Hz fundamental frequency: (a) Power reference and measured power of each SM, and (b) measured and estimated capacitor voltages.

Fig. 8(a) displays the SM powers. Before $t = 2.4$ s, the power references are viable and each SM tracks its reference. At $t = 2.4$ s, the power reference of the first SM (45%) is higher than the maximum APCL (43.1% when considering CVRs), which means the reference is unviable. As observed, this SM cannot track the reference and saturates at the derived APCL. However, if CVRs are ignored in the derivation of APCL, the power references will be considered viable, which is incorrect. This specific case emphasizes the importance of the proposed method that considers CVRs. After $t = 4.2$ s, the power references are unviable even if CVRs are not considered. Consequently, the SM powers are saturated at the derived APCLs with consideration of CVRs. The obtained results verify the accuracy of derived SM APCLs using the proposed method.

Fig. 8(b) depicts the measured capacitor voltages of the two SMs in one fundamental cycle and the corresponding estimates. As observed, the estimated voltages are close to the measured ones, which verifies the validity of the proposed method.

B. 50Hz Case

In this case, a 5.4- Ω resistor and 5-mH inductor are connected in series to the output of the CHB converter as a

Fig. 9. Experimental results with 50Hz fundamental frequency: (a) Measured powers and references of each SM, (b) measured and estimated capacitor voltages when $m_a = 0.9$, and (c) measured and estimated capacitor voltages when $m_a = 0.8$.

load. two modulation indices ($m_a = 0.9$ and $m_a = 0.8$) are investigated. Considering the CVRs, the maximum APCL of one SM is derived to be -26.55% when $m_a = 0.9$ and -17.34% when $m_a = 0.8$. Results are provided in Fig. 9.

Fig. 9(a) displays the power references and measured powers of the SMs. When the power references exceed the derived limits, the SM powers are saturated at the corresponding limits. Figs. 9(b) and (c) depict the measured and estimated capacitor voltages of the two SMs when $m_a = 0.9$ and $m_a = 0.8$, respectively. In both conditions, the estimated voltages are close to the measured ones.

VI. CONCLUSION

This paper has investigated the effect of CVRs on the SM APCLs for the MMC and CHB converter. It is revealed that, depending on the phase shift between the converter output voltage and current, the CVR can have a considerable effect on the SM APCLs (around 9% CVRs can change the SM APCLs by more than 9%). Moreover, a methodology is proposed to incorporate the CVRs in the derivation of SM APCLs, which provides more accurate results than the conventional method that ignores the CVRs. Simulation and experimental results

obtained on both the MMC and CHB converter verified the validity of the proposed analysis.

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