Development of resistive random access memory for next-generation embedded non-volatile memory application

Sun, Jianxun

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Development of Resistive Random Access Memory for Next-generation Embedded Non-volatile Memory Application

Sun Jianxun

School of Electrical & Electronic Engineering

**A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy**

2020

Statement of Originality

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Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

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Chen Tupei

Authorship Attribution Statement

This thesis contains material from 3 papers published in the following peer-reviewed journals in which I am listed as the first author.

Chapter 4 is published as J. Sun, J. B. Tan, and T. Chen, “Investigation of Electrical Noise Signal Triggered Resistive Switching and Its Implications,” IEEE Transactions on Electron Devices, 2020. DOI: 10.1109/TED.2020.3014841

The contributions of the co-authors are as follows:

- I conducted the experiments and wrote the manuscript.
- Dr. Tan edited the manuscript.
- Prof. Chen provided the initial project direction and feedback on the data analysis.

Chapter 5 is published as J. Sun, Y. B. Li, Y. Ye, J. Zhang, G. Y. Chong, J. B. Tan, Z. Liu and T. Chen, “3-D Geometric Engineering of the Double Wedge-like Electrodes for Filament-type RRAM Device Performance Improvement,” IEEE Access, vol. 8, pp. 4924-4934, 2019. DOI: 10.1109/ACCESS.2019.2962869

The contributions of the co-authors are as follows:

- I carried out the experiments and wrote the manuscript.
- Mr Li contributed partially to SEM imaging.
- Dr. Ye contributed partially to the modelling of the device.
- Dr. Zhang provided feedback on the explanation of the physic mechanism.
- Dr. Chong contributed partially to the fabrication of the device.

- Dr. Tan revised the manuscript.
- Prof. Liu gave suggestions on the design of experiments.
- Prof. Chen provided the initial project direction and evaluated on the measurement data.

Chapter 6 is published as J. Sun, J. B. Tan, and T. Chen, “HfO_x-based RRAM Device with Sandwich-like Electrode for Thermal Budget Requirement,” IEEE Transactions on Electron Devices, 2020. DOI: 10.1109/TED.2020.3014846

The contributions of the co-authors are as follows:

- I performed the experiments and wrote the manuscript.
- Dr. Tan amended the manuscript.
- Prof. Chen provided the initial project direction and guided me on the failure analysis.

15-09-20

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Date

.....
Sun Jianxun

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Summary

Resistive random access memory (RRAM) is a promising candidate for the next-generation non-volatile memory owing to its simple structure, fast read/write speed, low power consumption, high memory density, and complementary metal oxide semiconductor (CMOS) compatibility. However, many challenges such as high forming voltage, switching variation, thermal stability, and reliability degradation have hindered the high volume production of RRAM devices. In this work, engineering approaches from different perspectives have been implemented to improve the performance of the RRAM devices. To have a better picture of the work done, two terms “macro” and “micro” are introduced. The term “macro” refers to the work carried out at the device operation level such as forming, set, and reset, while the term “micro” refers to the work conducted at the device fabrication level like structural modification and interfacial engineering.

Prior works have been accomplished at the “macro” level to achieve multi-level cell (MLC) operation. It is well known that the MLC can be obtained through tuning of the DC operation parameters like set compliance current (CC) and reset stop voltage (SV). Since the larger the resistance window, the more levels could be accommodated, it is important to know the boundaries of the DC parameters. However, the method of finding the boundaries has not been documented. In this thesis, the progressive analysis of the resistive switching I - V characteristics has been adopted to explore the upper and lower bounds of the DC parameters. The significant changes of the I - V curves have been observed when the DC parameters are out of the ranges. It is also found that the conventional way of doing MLC operation by varying one parameter while fixing the

other one would lead to the drifting of resistances. Hence, the concept of dynamic boundaries has been proposed after taking the evolution of the filament into account. Experimental results show that the drifting has been mitigated by slightly reducing the reset SV.

As the forming voltage of the RRAM devices is usually higher than the operation voltages, it becomes a hurdle for the low voltage CMOS circuits. Pulse engineering (“macro” level) is a known method to reduce the forming voltage. Unfortunately, the demonstrated reduction percentage is only 10%. It is found that the voltage amplitude of the noise signal which triggers the forming process is much lower than the unipolar pulse height. Since the noise signal is generated by switching the halogen lamp, the light factor has been investigated. Based on the results of the “dark test”, it is highly speculated that the reduction of the forming voltage is attributed to the facilitation effect of the negative voltage. A novel bipolar pulse writing scheme is proposed to verify the above hypothesis. Experimental results show that the reduction percentage of the forming voltage is more than 30%, which is much higher than the reported value. Besides, the variability of the forming voltage also gets improved by more than 50%. On the contrary, the inhibition effect of the negative voltage is observed for the set process, which implies that the role of the negative voltage varies with the state of the device.

The resistive switching variability and reliability degradation are the two major roadblocks for the development of RRAM devices. Electrode structure engineering (“micro” level) is known to be effective for the improvement of the above two

performance metrics. Nonetheless, instead of two electrodes, only one of the electrodes is structurally modified based on the prior works. Here, to attain better filaments confinement, both electrodes of the RRAM devices are engineered. The unique geometric parameters such as electrode angle (EA), electrode spacing (ES), and electrode trench depth (ETD) associated with the double wedge-like electrodes are examined. Apart from the resistive switching uniformity, the reliability performance is significantly improved for the device with small EA, narrow ES, and deep ETD owing to the electric field confinement and enhancement.

The thermal budget of the standard integrated circuits (IC) manufacturing process is one of the key considerations even in the design stage of the RRAM devices. Nevertheless, such an important criterion seems to be overlooked by many of the research works. The duration of the thermal stability test reported has been less than or equal to one hour, which is not sufficient for the modern IC fabrication process. In this study, the thermal budget test is carried out by subjecting the RRAM devices to post-metalization annealing (PMA) at 400°C for more than 3 hrs. With the proper engineering of the oxidation reaction at the top metal/metal oxide interface (“micro” level), a device with the sandwich-like (TiN/Ti/TiN) top electrode exhibits better performance in thermal stability, forming, switching uniformity, and endurance when compared to other devices with a single layer (TiN) or bi-layer (TiN/Ti) top electrode.

It is common knowledge that noble metals such as Pt, Au, Ir, and Ru are quite costly and hard to etch for the semiconductor industry. Despite that, these materials are widely used

to form the electrodes of RRAM devices due to the chemical inertness. Good resistive switching has been demonstrated for the device with Pt bottom electrode (BE) in chapter 6. However, the degradation of switching uniformity is observed when Pt is replaced by TiN, which is a conventional fab material. The oxygen plasma treatment (OPT) has been implemented to passivate the TiN surface before the deposition of switching material. The switching uniformity and resistance window are improved at the expense of increased forming voltage possibly due to the reduction of defects at the bottom metal/metal oxide interface (“micro” level). RRAM cells with moderate OPT have been successfully integrated with thin film transistors (TFT) at the mini array level to demonstrate the possibility of practical application in the field of large-area electronics (LAE).

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List of Abbreviations

AFM	Atomic force microscope
ALD	Atomic layer deposition
BEOL	Back-end-of-line
BL	Bit line
BE	Bottom electrode
BGTC	Bottom-gate-top-contact
CD	Critical dimension
CMOS	Complementary metal oxide semiconductor
CRS	Complementary resistive switching
CC	Compliance current
CAFM	Conductive atomic force microscopy
CBRAM	Conductive bridging random access memory
CF	Conductive filaments
DI	De-ionized
DUT	Device under test
DHF	Diluted hydrofluoric acid
DRAM	Dynamic random access memory
EA	Electrode angle
ETD	Electrode trench depth
ES	Electrodes spacing
EUV	Extreme ultraviolet
FN	Fowler–Nordheim
HRS	High resistance states
HRTEM	High-resolution transmission electron microscopy
IGZO	Indium-gallium-zinc-oxide

IC	Integrated circuits
IL	Interfacial layer
IPA	Isopropyl alcohol
LAE	Large-area electronics
LRS	Low resistance states
OxRAM	Oxide random access memory
MIM	Metal-insulator-metal
MLC	Multi-level cell
1T1R	One-transistor-one-resistor
OPT	Oxygen plasma treatment
PL	Passivation layer
PF	Poole-Frenkel
PCRAM	Phase change random access memory
PVD	Physical vapor deposition
PECVD	Plasma-enhanced chemical vapor deposition
PMA	Post-metallization annealing
RTP	Rapid thermal processing
RIE	Reactive ion etching
RRAM	Resistive random access memory
SEM	Scanning electron microscope
SCS	Semiconductor characterization system
SDA	Semiconductor device analyzer
SL	Source line
SCLC	Space-charge-limited current
STT-MRAM	Spin-transfer torque magnetoresistive random access memory
SRAM	Static random access memory
SV	Stop voltage

SPM	Sulfuric peroxide mixture
TFT	Thin film transistors
TE	Top electrode
UV	Ultraviolet
VRRAM	Vertical resistive random access memory
WL	Word line
XPS	X-ray photoelectron spectroscopy
XRR	X-ray reflectometry

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In this chapter, working principles and development challenges of the mainstream memories are briefly introduced. For comparison, the different types of emerging memories are illustrated. Resistive random access memory (RRAM) as a potential candidature to replace flash memory is the focus of this work. The motivation, objectives, and scope of research are presented. The major contributions and organization of the thesis are described.

1.1 Background

Currently, flash memory is the mainstream technology for non-volatile memory applications such as code and data storage in mobile and embedded devices. It has a transistor-like structure where charges can be electrically stored in the floating gate (polysilicon) or nitride layer by hot carrier injection or Fowler–Nordheim (FN) tunneling, depending on the types of flash memories. Similarly, the stored charges can be electrically erased by hot hole injection or FN tunneling. With the ever-growing demand in memory density, the planar flash memory is reaching the limit of scaling due to fundamental issues such as random doping fluctuations [1], random telegraph noise [2], and electron injection statistics [3]. As a result, the distribution margin of the threshold voltage has been significantly reduced. Fortunately, the design of vertical flash has been proposed to overcome the bottleneck of planar technology. The array architectures of the 3-D flash can be classified into two categories, namely the stacked NAND and vertical NAND. Their schematics are shown in Fig. 1(a) and (b), respectively. The major difference between these two architectures is the orientation of the transistor channel. For the stacked flash, the channel is horizontal (X-axis), which is the same as that of the planar flash. However, the channel of the vertical flash is along the Z-axis, which is perpendicular to the substrate. Although many efforts have been made in

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research and development, the 3-D flash still facing the following challenges. (1) The cell size is large due to the high aspect ratio of the vertical channel. (2) The word line staircase is bulky owing to a high number of stacked cells. (3) The periphery circuit is area consuming. (4) The wafer throughput is low since the integration process is complex. (5) The cost of process development is huge.

FIG. 1. (a) Schematic of two-layer stacked NAND flash. (b) Schematic of vertical NAND flash. Figures are taken from [4].

With the scaling and 3-D technologies, more memory cells can be integrated without increasing the chip size. The multi-level cell (MLC) technology is an alternative approach to improve storage capacity. Instead of one bit per cell, multiple bits can be stored in a single device. The relationship between the number of levels (N) and the number of bits (n) can be described by a simple equation of $N=2^n$. The MLC operation can be realized in flash memory. The schematics of the MLC flash memory array and the cross-sectional view of a single cell are shown in Fig. 2(a) and (b), respectively. Each cell has four storage nodes due to the sharing of the gates and sources of two transistors through the recessed channel. Four bits per cell can be obtained by varying bias

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conditions. Considering the complexity of the peripheral circuit, the bits density is three times higher than that of the conventional NOR flash [5]. However, the aforementioned fundamental issues such as random doping fluctuations, random telegraph noise and electron injection statistics can become aggravated for the MLC flash memory. As a result, the MLC devices are more prone to reliability failures.

FIG. 2. (a) Schematic of the MLC flash memory array. (b) Schematic of the cross-sectional view of a single device. Figures are taken from [5].

Emerging memories such as spin-transfer torque magnetoresistive random access memory (STT-MRAM), phase change random access memory (PCRAM), and resistive random access memory (RRAM) have drawn much attention due to the non-charge based memory effects. They are similar in terms of the two-terminal sandwich-like device structure, non-volatile storage nature, and resistive switching operation. The transition between the high resistance states (HRS) and low resistance states (LRS) can be triggered by the external electrical signals. The HRS is corresponding to bit 0 (off state) and the LRS is corresponding to bit 1 (on state). The switching mechanisms of emerging memories are different. For STT-MRAM, the memory stack as shown

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in Fig. 3(a) consists of a tunneling layer and two ferromagnetic layers. The spin configuration of the top free layer can be changed from parallel (LRS) to anti-parallel (HRS) with respect to that of the bottom pinned layer and vice versa [6]. For PCRAM, the memory cell as shown in Fig. 3(b) comprises a chalcogenide layer and two electrodes. The phase of the chalcogenide layer can be varied from crystalline (LRS) to amorphous (HRS) and vice versa [7]. The device structures of the oxide random access memory (OxRAM) and conductive bridging random access memory (CBRAM) are shown in Fig. 3(c) and (d), respectively. Both types of RRAM devices can switch from the HRS to LRS by forming the conductive filaments (CF) between the top and bottom electrodes, and the reversed switching (LRS→HRS) can be achieved via rupturing the CF [8]. The major difference between the two devices is the chemical constitution of the CF. The CF of OxRAM is made of oxygen vacancies which are generated in the dielectric layer, whereas the CF of CBRAM is built by metal atoms that are injected from the electrode layer.

FIG. 3. Schematics of the structures of emerging memories: (a) MRAM, (b) PCRAM, (c) OxRAM, and (d) CBRAM. Figures are taken from [9].

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1.2 Motivation

Due to the trade-offs in memory device engineering, it is hard for one type of memory to meet all the performance requirements such as fast read/write speed, low operation voltage, low power consumption, long data retention time, stable cycling endurance, and multi-bit storage. [Table I](#) compares the main characteristics of mainstream memories and emerging memories.

	Mainstream Memories				Emerging Memories		
	SRAM	DRAM	FLASH		STT-MRAM	PCRAM	RRAM
			NOR	NAND			
Cell Area	$>100F^2$	$6F^2$	$10F^2$	$<4F^2$ (3D)	$6\sim 20F^2$	$4\sim 20F^2$	$<4F^2$ if 3D
Multi-bit	1	1	2	3	1	2	2
Voltage	$<1V$	$<1V$	$>10V$	$>10V$	$<2V$	$<3V$	$<3V$
Read Time	$\sim 1ns$	$\sim 10ns$	$\sim 50ns$	$\sim 10\mu s$	$<10ns$	$<10ns$	$<10ns$
Write Time	$\sim 1ns$	$\sim 10ns$	$10\mu s\sim 1ms$	$100\mu s\sim 1ms$	$<5ns$	$\sim 50ns$	$<10ns$
Retention	N/A	$\sim 64ms$	$>10y$	$>10y$	$>10y$	$>10y$	$>10y$
Endurance	$>1E16$	$>1E16$	$>1E5$	$>1E4$	$>1E15$	$>1E9$	$>1E6\sim 1E12$
Write Energy (J/bit)	$\sim fJ$	$\sim 10fJ$	$100pJ$	$\sim 10fJ$	$\sim 0.1pJ$	$\sim 10pJ$	$\sim 0.1pJ$
F: feature size of the lithography, and the energy estimation is on the cell-level (not the array-level)							

TABLE I. Comparison of the main characteristics of mainstream memories and emerging memories. The figure is taken from [10].

Based on the data shown in [Table I](#), RRAM is a promising candidate to replace flash memory for code and data storage due to low operation voltage, fast read/write speed, and stable cycling endurance [11]. In addition, RRAM has lower power consumption as compared to PCRAM and simpler device structure as compared to MRAM [12], which make it more suitable for embedded memory application with low cost and high energy efficiency. Notably, the crossbar RRAM

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architecture [13] and the multi-bit storage [14] can improve the memory capacity tremendously. As a result, RRAM also shows the potential application in the area of neuromorphic computing.

1.3 Objectives and Scope of Research

Although RRAM technology looks promising from various perspectives, the semiconductor industries still have to overcome certain challenges to achieve volume production of RRAM devices. Some of the critical issues are listed below:

- (1) The forming process is a hurdle for the low-voltage complementary metal oxide semiconductor (CMOS) circuits since the forming voltage is higher than the operation (set/reset) voltages.
- (2) The variation of resistance which is caused by the stochastic resistive switching results in a low sense margin.
- (3) Certain types of RRAM devices are not able to meet the thermal budget requirement of semiconductor foundries.
- (4) The stress-induced interfacial reaction leads to the degradation of device reliability.
- (5) Noble metals which have been widely used as the electrodes of RRAM devices are not compatible with the CMOS process due to high etch resistance.

The main objective of this thesis is to provide possible solutions to the above problems by engineering the program/erase signals, materials, structure, and interfaces of RRAM devices.

The scope of this research covers the performance improvement of both types of filamentary RRAM devices, specifically, the Ag-based CBRAM and HfO_x-based OxRAM. Notably, the

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switching uniformity and reliability are heavily studied. The non-filamentary RRAM device, crossbar array, and analog switching are not the focus of this thesis.

1.4 Major Contributions of the Thesis

The major contributions of the thesis are listed below:

(1) The operation boundaries of the DC parameters such as set compliance current (CC) and reset stop voltage (SV) are determined through the progressive analysis of the I - V characteristics. To obtain stable MLC operation, the boundary conditions need to be fine-tuned according to the evolution of the filament.

(2) Inspired by the electrical noise signals, a novel bipolar pulse writing scheme is proposed to reduce the forming voltage and variability. Experimental data shows that the average and standard deviation of the pulse heights are reduced by more than 30% and 50%, respectively.

(3) A novel device structure with double wedge-like electrodes is designed to improve resistive switching uniformity and reliability. Results show that the device performance is strongly dependent on the geometric parameters such as electrode angle (EA), electrode spacing (ES), and electrode trench depth (ETD) thanks to the electric field confinement and enhancement.

(4) With proper engineering of the oxidation reaction at the metal/metal oxide interface, a device with the sandwich-like (TiN/Ti/TiN) top electrode exhibits better performance in thermal stability, forming, switching uniformity, and endurance when compared to other devices with a single layer (TiN) or bi-layer (TiN/Ti) top electrode.

(5) The switching uniformity and resistance window are enhanced through the oxygen plasma treatment (OPT) of the bottom TiN electrode, whereas the DC forming voltage increases with the

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processing time. RRAM devices with moderate treatment are integrated with thin film transistors (TFT) to form a 64-bit one-transistor-one-resistor (1T1R) array, and the basic functions are successfully demonstrated.

1.5 Organization of the Thesis

The chapters of the thesis are organized as follows:

In Chapter 1, the mainstream memories and emerging memories are briefly introduced. By comparing the performance of various types of non-volatile memories, RRAM is chosen as a potential candidature to replace flash memory. The objectives, scope, and major contributions of the research are illustrated concisely to give a preview of the thesis.

In Chapter 2, literature reviews on the topics of development roadmap, device structure, array architecture, resistive switching (process, mode, and mechanism), current conduction, performance metrics, and multi-bit storage of RRAM devices are presented.

In Chapter 3, two important DC operation parameters namely set CC and reset SV are examined. The operation boundaries of the DC parameters are determined by progressive analysis of the I - V characteristics. For MLC operation, boundary conditions need to be adjusted based on the evolution of the filament to achieve stable resistive switching.

In Chapter 4, the electrical noise signal triggered resistive switching is explored. Although noise is often undesirable, the voltage amplitude of the noise signal is much lower than the unipolar pulse height owing to the facilitation effect of the negative voltage. As a result, a novel bipolar pulse writing scheme is proposed to reduce the forming voltage and variability.

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In Chapter 5, a novel device structure with the double wedge-like electrodes is fabricated. The effects of EA, ES, and ETD on device performance are studied. Good switching uniformity and reliability have been demonstrated in device with 90° EA, 440 nm ES, and 90 nm ETD.

In Chapter 6, the effects of the thermal budget on device performance have been investigated. A device with the sandwich-like (TiN/Ti/TiN) top electrode is engineered to achieve good performance in thermal stability, forming, switching uniformity, and endurance.

In Chapter 7, the effects of the oxygen plasma treatment (OPT) on the TiN bottom electrode (BE) are discussed. The switching uniformity and resistance window are improved via the BE passivation process. RRAM devices with moderate treatment are integrated with thin film transistors (TFT) to form a 64-bit one-transistor-one-resistor (1T1R) array, and the basic functions have been successfully demonstrated.

In Chapter 8, the research works carried out in this thesis are summarized, and some future works are recommended.

Chapter 2 Literature Review

Literature reviews on the topics of development roadmap, device structure, array architecture, resistive switching (process, mode, and mechanism), current conduction, performance metrics, and multi-bit storage of the resistive random access memory (RRAM) are presented. The tools used for the fabrication and characterization of RRAM devices are listed.

2.1 Introduction to RRAM

The discovery of the resistive switching phenomenon can be traced back to the 1960s. The negative resistance and high current densities have been observed in metal oxide films when a large voltage is applied [15]. However, RRAM technology has not been developed until 30 years later due to the instability of resistive switching and the successful demonstration of silicon-based memories. The resistive switching of perovskite oxides such as PrCaMnO_3 [16], SrZrO_3 [17], and SrTiO_3 [18] with a hysteresis of I - V characteristic was reported between the late 1990s and early 2000s. The following three major events put RRAM again in the picture. (1) In 2004, the NiO-based RRAM device with good performance was successfully integrated with 0.18 μm complementary metal oxide semiconductor (CMOS) technology by Samsung for the first time [19]. (2) In 2008, the theoretical concept of memristor (a fourth fundamental element) was applied to RRAM by HP labs, which has triggered numerous research works in the electronics world [20]. (3) In 2008, the first RRAM cell with fully CMOS compatible materials was integrated with 0.18 μm CMOS technology by ITRI [21]. Since then, RRAM technology has been booming due to the simple device structure and CMOS compatibility. Tens of metal oxides such as NiO [22], TiO [23], CuO [24], ZrO [25], ZnO [26], AlO [27], TaO [28], HfO [29], etc., have been demonstrated with resistive switching behavior. [Table II](#) gives a brief summary of the materials that have been used

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of via is shown in Fig. 4(c). In Fig. 4(d), the top electrode (TE) and the switching layer are sitting on a concave structure. Device scaling can still be achieved by reducing the open area of the concave structure, even though the BE could be a piece of wide metal. Fig. 4(e) shows a MIM stack formed at the cross point of two perpendicular metal lines.

FIG. 4. The various designs of RRAM stacks: (a) a typical MIM stack embedded between two vias, (b) a MIM stack with blanket oxide as a switching layer and via as BE, (c) a MIM stack with a switching layer formed by oxidation of via, (d) a MIM stack with concave structure, and (e) a MIM stack with crossbar design. Figures are taken from [30].

The RRAM array architectures can be classified into four types namely one-transistor-one-resistor (1T1R), crossbar, one-transistor-N-resistor (1TNR), and vertical RRAM (VRRAM). The schematic of the 1T1R is shown in Fig. 5. Each RRAM cell is collected in series with a transistor which serves as a selector and current limiter. To access the information stored in the RRAM device, the transistor has to be turned on first by applying a bias to the word line (WL) before the current can flow from the bit line (BL) to the source line (SL) and vice versa. The current can be

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unidirectional or bi-directional depends on the switching mode (to be discussed in the following section) of the RRAM device.

FIG. 5. Schematic of the 1T1R array architecture. The figure is taken from [10].

As the 1T1R array architecture provides good cell to cell isolation, it reduces the probability of cross-talk. It is not preferred for the data storage applications due to the relatively large effective cell area of $12F^2$ (F is the feature size of lithography) when compared to that ($4F^2$) of the crossbar array architecture which is shown in Fig. 6(a). The WL and BL of the crossbar array are perpendicular to each other with RRAM devices and selectors placed at the cross points. The driving transistors (not shown here) are located at the periphery of the array. As shown in Fig. 6(b), the selectors are inserted to minimize the undesired sneak path current that could flow through the unselected neighbor cells.

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FIG. 6. (a) Schematic of the crossbar array architecture. (b) Demonstration of the sneak path current. Figures are taken from [10].

1TNR hybrid array architecture is proposed to tackle the problems of the large cell size of the 1T1R and sneak path current of the crossbar at the same time. The schematics of the 1T4R and 1T8R sub-arrays are shown in Fig. 7. A single transistor is shared by several RRAM cells with individual BL and common WL. As the leakage current is well controlled within the sub-array, it is independent of the size of the full array. The effective cell size of the 1T4R is $4F^2$ which is comparable to that of the crossbar [31]. With memory stacking technology, the effective cell size can be further scaled to $2.5F^2$ by adopting the 1T8R design [31].

FIG. 7. Schematics of the 1T4R (left) and 1T8R (right) sub-arrays. The figure is taken from [31].

Likewise, the crossbar array architecture is also suitable for 3-D stacking to improve memory density. A two-layer stacked crossbar array with shared BL has been demonstrated. For example, Panasonic reported an 8 Mb TaO_x-based RRAM prototype [32] and Sandisk/Toshiba reported a 32 Gb RRAM prototype [13]. The schematic of the 3-D stacked crossbar array is shown in Fig. 8(a). Due to the increase in the number of critical mask layers and the cost of the lithography process, the integration becomes more and more challenging when the number of stacked layers goes up [33]. As shown in Fig. 8(b), VRRAM is proposed to address the above issues. Similar to the formation of a vertical channel in VNAND, the electrode of RRAM is oriented vertically. The schematic of the cross-sectional view of the VRRAM is shown in Fig. 8(c). The via is filled with the switching material followed by the vertical electrode. The deposition of multiple layers of horizontal electrodes and isolation layers can be processed at one time [34]. The effective cell area can be easily scaled by controlling the thickness of the horizontal electrode since the resistive switching occurs at the sidewall of the via. As the selector with additional electrode is hard to be

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formed at the sidewall, RRAM devices with self-selective function are required to reduce the leakage current.

FIG. 8. (a) Schematic of the 3-D stacked crossbar array [35]. (b) Schematic of the 3-D VRRAM [35]. (c) Schematic of the cross-sectional view of the 3-D VRRAM. Figures are taken from [10].

2.1.2 Resistive Switching Process and Modes

In general, the resistive switching process of metal oxide RRAM devices includes three steps namely forming, reset, and set. The forming process is also considered as the first set process since both steps change the device from the high resistance state (HRS) to the low resistance state (LRS). The pristine state of the RRAM device is almost non-conductive as fewer defects exist in the metal oxide. A large forming voltage is required to induce a strong electric field which can generate a sufficient number of defects by knocking out the oxygen atoms from the lattice [8]. This initialization process can be interpreted as a soft breakdown of the dielectric [36]. To prevent the device from hard breakdown, current compliance is required. The forming voltage can be controlled by engineering the dielectric film thickness [21] and the number of defects in the film [37]. As the negatively charged oxygen ions are driven towards the anode by the electric field, the

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positively charged oxygen vacancies form the conductive filaments (CF). The localized CF has been observed in various types of metal oxides by using conductive atomic force microscopy (CAFM) [38, 39] and high-resolution transmission electron microscopy (HRTEM) [40]. Noted that the forming process is only conducted once. The subsequent reset process converts the device from the LRS back to HRS. The R_{HRS} is smaller than the resistance of the pristine state due to partial rupturing of the CF. The reset process can be understood as the recombination process between the oxygen ions and vacancies. As a result, a resistive gap between the electrode and the virtual electrode (the remaining portion of the CF) is formed. The following set process moves the oxygen ions back to the anode, and the LRS is achieved again due to recovery of the CF. The set voltage is smaller than the forming voltage since fewer oxygen ions are involved in the set process. Multiple time programming can be realized by repeating the set and reset cycle. Fig. 9 schematically illustrates the resistive switching process.

FIG. 9. Schematic of the resistive switching process of metal oxide RRAM. The figure is taken from [41].

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The resistive switching modes can be divided into two groups namely unipolar and bipolar. For unipolar switching, as shown in Fig. 10(a), the threshold voltages which trigger the set and reset process are at the same polarity. However, the threshold voltages which activate the set and reset process of the bipolar switching are at different polarities as shown in Fig. 10(b). The resistive switching mode is determined by both the metal oxide material and oxide/electrode interfaces [8]. As a rule of thumb, the unipolar mode is often observed in the memory stack with noble metals such as Pt, Au, and Ru as both the TE and BE, whereas the bipolar mode is usually discovered in the memory stack with oxidizable metals such as Ti, Ta, and TiN as one or both of the electrodes. Since unipolar devices exhibit poor device uniformity and cycling endurance [42], bipolar devices become the focus of research.

FIG. 10. (a) I - V curves of unipolar switching. (b) I - V curves of bipolar switching. Figures are taken from [8].

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2.1.3 Resistive Switching Mechanisms

The 1D filament model and 2D interface model can be used to describe the resistive switching mechanisms of various types of RRAM devices. For the filament-type RRAM device, the R_{HRS}/R_{LRS} is almost independent of the effective cell area since the diameter of the localized filaments is in the order of nanometers [43]. This statement is true only if the device size is much larger than the size of the filaments. The 1D filament model can be further divided into three sub-models: (1) thermochemical fuse/anti-fuse model, (2) oxygen vacancy migration model, and (3) electrochemical metallization model.

For the thermochemical fuse/anti-fuse model, the formation and rupture of the filaments are mainly triggered by the current-induced Joule heating, which is similar to the function of a fuse. The fuse blows if the current passing through it exceeds a certain limit. The local temperature along the filaments can rise to about 600 K during the reset process [44, 45]. The schematic illustration of the thermochemical effect is shown in Fig. 11. Such an effect usually results in unipolar resistive switching. The set state and reset state are corresponding to the fuse and anti-fuse, respectively. During the set process, the oxygen vacancies that form the filaments are generated by breaking the metal-oxygen bonds under the high electric field. During the reset process, the surrounding oxygen atoms recombine with the oxygen vacancies through a heat-accelerated diffusion process, which thermally dissolves the filaments.

FIG. 11. Schematic of the thermochemical fuse/anti-fuse model. The figure is taken from [46].

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For the oxygen vacancy migration model as shown in Fig. 12, the TE can function as an oxygen reservoir to facilitate the formation and rupture of the CF. An additional buffer layer can be inserted between the electrode and metal oxide for cycling endurance improvement [21]. The migration of oxygen vacancies is mainly driven by the electric field. As compared to the diffusion process, the drift process is more directional, thus it is beneficial for the control of the filaments. In the set process (formation of the filaments), the oxygen vacancies drift from anode (TE) to cathode (BE), whereas the direction of migration is reversed in the reset process (rupturing of the filaments). This model is widely used to explain the switching mechanisms of bipolar RRAM devices.

FIG. 12. Schematic of the oxygen vacancy migration model. The figure is taken from [47].

For the electrochemical metallization model, instead of oxygen vacancies, the particles under migration are metal atoms such as Ag [48] and Cu [49]. These two metals are the most frequently reported anode materials for conductive bridging random access memory (CBRAM) due to high mobility. The I - V curve and schematics of the electrochemical metallization model of the Ag-based CBRAM are shown in Fig. 13. In the set process, the Ag atoms are oxidized and become Ag ions. These ions are injected into the solid electrolyte (GeSe) and subsequently reduced back

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to Ag atoms at the cathode. The accumulation of the Ag atoms forms a conductive path between the electrodes. In the reset process, the Ag atoms which constitute the filaments are converted to Ag ions. The filaments are ruptured due to the withdrawal of the Ag ions.

FIG. 13. *I-V* curve and schematics of the electrochemical metallization model of the Ag-based CBRAM. The figure is taken from [50].

The growth of filaments can be mathematically modeled by the following rate equation [51].

$$\frac{d\phi}{dt} = A \exp\left(-\frac{E_a}{KT}\right) \quad (1)$$

Where ϕ is the effective diameter of the filaments, A is a constant, E_a is the energy barrier for ion migration, T is the local temperature along the filaments. The growth of filaments is directly controlled by the energy barrier and local temperature. The E_a is governed by the following equation [51].

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$$E_a = E_{a0} - \alpha qV \quad (2)$$

Where E_{a0} is the energy barrier of ion migration at zero voltage, α is a constant, q is the electron charge, V is the applied voltage. The higher the applied voltage, the lower the barrier. The temperature T in equation (1) can be estimated by the following equation [51].

$$T = T_0 + \frac{R_{th}}{R} V^2 \quad (3)$$

Where T_0 is the room temperature, R_{th} is the effective thermal resistance, R is the resistance, V is the applied voltage. For $V=1$ V and the device is at LRS state, the R_{th}/R ratio is around 434 K/V² [52]. The calculated temperature along the filaments is more than 450 °C which suggests the significance of the Joule heating effect. Once the diameter of filaments is obtained, the device resistance can be calculated by the following equation [53].

$$R = \frac{4\rho t_{ox}}{\pi\phi^2} \quad (4)$$

Where ρ is the resistivity of the filaments, t_{ox} is the thickness of the metal oxide layer. For a given circuit, the above equations can be used to simulate the electrical behavior of the RRAM device.

Unlike the filament-type RRAM device, the R_{HRS}/R_{LRS} of the interface-type RRAM device is dependent on the effective switching area. The 2D interface model can be classified into two sub-models namely Schottky barrier height modulation and depletion width modulation. As the RRAM stack consists of metal and insulator, the Schottky barrier is formed at the metal/metal oxide interface. Fig. 14 illustrates the barrier height modulation caused by the redox reaction at the interface. When oxygen ions migrate from the bulk to the interface during the reset process, the bandgap of the interface material is enlarged owing to the oxidation reaction. As a result, the

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Schottky barrier height between the electrode and the interface layer is increased. The current is weakened as the electrons need more energy to overcome the barrier. Thus, HRS is achieved. On the contrary, when oxygen ions move away from the interface layer during the set process, the bandgap of the interface material is lowered. Hence, the Schottky barrier height is decreased and LRS is obtained.

FIG. 14. Schottky barrier height modulation. The figure is taken from [54].

Fig. 15 illustrates the depletion width modulation caused by the charging effect at the interface. When oxygen vacancies move away from the interface during the set process, the depletion of the positive charges raises up the Fermi level and narrows the depletion width. The current is enhanced due to the electron tunneling. Conversely, when oxygen vacancies move towards the interface during the reset process, the accumulation of the positive charges lowers down the Fermi level and widens the depletion width. The current is weakened as the electron tunneling is suppressed.

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FIG. 15. Depletion barrier width modulation. The figure is taken from [55].

2.1.4 Current Conduction Mechanisms

For filament-type RRAM devices, the current conduction mechanism of the LRS is simply ohmic conduction governed by the Ohms law. However, the current conduction mechanisms of the HRS are quite diverse. The schematic of the possible electron conduction paths from cathode to anode is shown in Fig. 16. Path No.1 indicates Schottky emission. The electrons activated by the thermal energy can overcome the Schottky barrier and get injected into the conduction band of the dielectric. Path No.2 indicates the Fowler–Nordheim (FN) tunneling. The electrons under the high electric field can tunnel from the cathode to the conduction band of the dielectric. Path No.3 indicates direct tunneling. The electrons can directly tunnel from the cathode to the anode if the dielectric layer is thin enough. The rest of the paths are under the group of trap-assisted tunneling which includes path No.4 (electrons tunnel from the cathode to trap), path No.5 (electrons emit from trap to the conduction band), path No.6 (electrons tunnel from trap to the conduction band), path No.7 (electrons hop from trap to trap), and path No.8 (electrons tunnel from trap to the anode). Among all, the following three conduction mechanisms such as the Schottky emission ($\log(I) \sim V^{1/2}$) [56], Poole-Frenkel (PF) emission (path No.5) ($\log(I/V) \sim V^{1/2}$) [57], and space charge limited current (SCLC) ($I \sim V$ & $I \sim V^2$) [58] are commonly used to describe the current conduction of the HRS.

FIG. 16. Schematic of the possible electron conduction paths through an RRAM stack. The figure is taken from [59].

2.1.5 Device Performance Metrics

The major performance metrics of the filamentary RRAM devices include variability and reliability. From the industry point of view, the variability hinders large-scale manufacturing. Both the set/reset voltages and R_{HRS}/R_{LRS} vary significantly with time (cycle to cycle) and space (device to device). The spatial variations can be improved via the precise control of the device fabrication process, whereas the temporal variations are hard to be minimized due to the stochastic generation and migration of the oxygen vacancies/metal ions [60]. Usually, the variation of the R_{HRS} is worse than that of the R_{LRS} as the current conduction mechanisms are different. The variation of the R_{LRS} is caused by the change of the diameter of filaments, whereas the variation of the R_{HRS} is caused by the change of the distance of the resistive gap. A small change in the gap distance can result in a big change in the tunneling current due to the amplification effect of the exponential term. Many engineering works have been done to improve the switching uniformity of the oxide-based RRAM

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devices. Four ways of device engineering are listed here for detailed illustration. The first method is to embed the buffer layers at the electrode/oxide interface. A thin Al buffer layer is inserted between the TiN electrode and HfO_x switching layer to improve the distribution of set voltage and resistance [61]. The second approach is to dope the bulk oxide with nanoparticles. Ti atoms are implanted into the ZrO_x to confine the filaments through local electric field enhancement [62]. The third means is to modify the shape of the electrode. A tip electrode is fabricated by reactive ion etching (RIE) process to concentrate the filaments through the electric field confinement [63]. The fourth method is to scale the cell area. The cell size of $\text{ZrO}_x/\text{HfO}_x$ bilayer RRAM is reduced to 50 nm to eliminate the formation of undesired filaments and improve both the temporal and spatial uniformity [64]. Noted that the third and fourth methods can be applied to CBRAM as well. Other than device engineering, the verification programming technique can also be implemented to narrow the distribution of resistance [65].

The reliability performance includes cycling endurance and data retention. Endurance refers to the number of cycles that the device can be programmed/erased before the resistance window collapses. A typical endurance plot is shown in [Fig. 17\(a\)](#). Due to the stress caused by consecutive switching, the resistance window might shrink gradually or close abruptly with set/reset failure. A set failure occurs when the set voltage is too weak to convert the device from the HRS to LRS. In other words, the resistance is stuck at the HRS. A reset failure occurs when the resistance is stuck at the LRS due to the weak reset voltage. For the filament-type RRAM device, the unbalanced migration of charged particles (oxygen vacancies/metal ions) during the set and reset cycles is the root cause of the endurance failure. Three types of endurance failure mechanisms of the oxide-based RRAM devices namely (1) interfacial oxidation reaction, (2) generation of extra vacancies and (3) depletion of oxygen ions have been discussed in [66]. The balanced set/reset voltage has

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to be determined to achieve optimal endurance [67]. The highest ever reported endurance is 10^{12} cycles [28].

Data retention refers to the time duration of a memory bit to retain its data state (R_{HRS}/R_{LRS}). The typical requirement for the data retention of non-volatile memory is at least 10 years ($\sim 3 \times 10^8$ s) at 85 °C. Fig. 17(b) shows an example of the data retention plot. There are three different techniques for data retention measurement. For the first method, the device is stressed at the elevated temperature, and a small voltage pulse is applied at certain time intervals (e.g., 1 s) for reading. The evolution line of resistance is extrapolated to the ten-year point. It is worth pointing out that the voltage stress exerted by the read pulse could disturb the resistance state. To minimize the stress, the device is heated at high temperature for extended intervals (e.g., 24 hrs) and the resistance is read out after the cooling. Although the above two approaches are quite simple, they cannot guarantee that the resistance state can sustain after the test period as the resistance window could collapse abruptly rather than gradually [68]. A more rigorous method called temperature-accelerated testing is proposed. The devices are stressed at different high temperatures, and the time-to-failure at each temperature is recorded. The Arrhenius plot can be used to extract the activation energy, and the time-to-failure at the operation temperature can be extrapolated. Noted that the third method is destructive and more expensive when compared to the first two methods.

FIG. 17. (a) Cycling endurance plot. (b) Data retention plot. Figures are taken from [19].

2.1.6 Multi-bit Storage

The multi-level cell (MLC) operation or multi-bit operation is an alternative approach to increase the bits density since each cell can store more than one bit. The WO_x-based RRAM device demonstrated in [69] has the highest number of levels (8 levels) reported so far. Typically, there are three different ways of obtaining multi-bit storage. The first approach is to tune the set compliance current (CC) and reset stop voltage (SV) as shown in Fig. 18. The R_{LRS} can be varied by adjusting the set CC possibly due to the modulation of the diameter of filaments [21]. The higher the CC, the larger the diameter of filaments, and the lower the R_{LRS}. The R_{HRS} can be changed by varying the reset SV possibly due to the modulation of the gap distance [21]. The larger the reset SV, the wider the gap distance, and the higher the R_{HRS}. This method is time consuming due to the sweep of the voltage.

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FIG. 18. MLC operation: (a) R_{HRS} is changed by varying the reset SV, and (b) R_{LRS} is changed by varying the set CC. Figures are taken from [21].

The second technique is to tune the pulse width and amplitude. Fast resistive switching can be realized owing to the short pulse width. The R_{HRS} can be increased by either exponentially increasing the pulse width (Fig. 19(a)) or linearly increasing the pulse amplitude (Fig. 19(b)) [70]. The tuning of pulse amplitude is more energy-efficient as compared to the pulse width adjustment based on the transient current response [70].

FIG. 19. MLC operation: (a) R_{HRS} is changed by varying the pulse width, and (b) R_{HRS} is changed by varying the pulse amplitude. Figures are taken from [70].

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The third approach is to tune the light intensity or wavelength. As shown in Fig. 20, the set process is triggered by the visible light pulse, and the reset process is activated by the voltage pulse. During the set process, the light generated electrons move away from the oxide/metal interface under the built-in electric field. The depletion width of the Schottky barrier is reduced, thus the thin Schottky barrier results in the LRS. Conversely, the electrons driven by the reset pulse move back to the interface and the trapped electrons recover the Schottky barrier. As a result, the HRS is restored. As the number of excited electrons is proportional to the light intensity and wavelength, the LRS can be varied. Fig. 20(a) and (b) show the variation of R_{LRS} by controlling the light intensity and wavelength, respectively.

FIG. 20. MLC operation: (a) R_{LRS} is changed by varying the light intensity, and (b) R_{LRS} is changed by varying the wavelength. Figures are taken from [71].

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2.2 Fabrication of RRAM Devices

In this thesis, all RRAM devices are fabricated in Nanyang NanoFabrication Centre (N2FC). The device fabrication process includes wet clean, wet oxidation, physical vapor deposition (PVD), atomic layer deposition (ALD), lithography, reactive ion etching (RIE), plasma-enhanced chemical vapor deposition (PECVD), lift-off, rapid thermal processing (RTP), post-metallization annealing (PMA), and oxygen plasma treatment (OPT). The photos of various types of tools are shown in [Fig. 21](#). A brief description of each process is given below.

Wet clean: the wafer is cleaned by using the sulfuric peroxide mixture (SPM) solution at 80 °C to remove the organic particles, followed by the diluted hydrofluoric acid (DHF) dip to remove the native oxide. After that, the wafer is spin-dried.

Wet oxidation: the wafer is loaded into the center position of the horizontal oxidation furnace filled with hydrogen and oxygen gas mixture to grow a 550-nm-thick SiO₂ layer at 1000 °C for electrical isolation.

PVD: the PVD process includes sputtering and electron-beam evaporation. Most of the conducting materials such as Ti, TiN, Al, and Pt are deposited by sputtering. Metal oxide such as indium-gallium-zinc-oxide (IGZO) is also deposited by sputtering. The thickness of the film can be varied by tuning the power, gas flow, and deposition time. For electron-beam evaporation, the deposition rate is controlled by the beam current. Ag is deposited by electron-beam evaporation at a slow rate of ~0.1 nm/s to improve the film adhesion.

ALD: most of the dielectrics such as HfO₂, Al₂O₃, and ZrO₂ are deposited by ALD at 250 °C. It is a self-limited sequential deposition with a slow rate and good uniformity. For example, two

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precursors namely water (H_2O) vapor and metal-organic ($\text{C}_8\text{H}_{24}\text{N}_4\text{Hf}$) vapor are introduced alternately to form HfO_2 . The thickness of the film is controlled by the number of pulse cycles. Each cycle gives a thickness of 1.2 to 1.6 Å.

Lithography: the basic steps of the negative lithography process include (1) pre-bake, (2) spin coating, (3) soft bake, (4) first exposure, (5) reversal bake, (6) flood exposure, (7) develop, and (8) hard bake. The resolution ($\sim 2\text{ }\mu\text{m}$) is limited by the wavelength (365 nm, i-line) of the ultraviolet (UV) light.

RIE: the etch rate, selectivity and etch profile are the three important metrics of the etch process. The optimization of the etch rate is essential since a fast etch rate may cause too much over etch and a slow etch rate leads to low throughput. Selectivity is the ratio of two etch rates: the etch rate of the layer to be removed and the etch rate of the layer to be protected. To keep the mask layer thin, high selectivity is preferred. A smooth etch profile with a steep sidewall is required to maintain the critical dimension (CD).

PECVD: SiO_2 as a common BEOL isolation layer is deposited by PECVD with SiH_4 and N_2O as precursors at 300 °C due to the requirement of thermal budget. The film deposited by PECVD is more conformal than the film deposited by PVD. Amorphous silicon (a-Si) as the solid electrolyte of CBRAM is deposited by PECVD as well.

Lift-off: in research labs, lift-off together with negative lithography is widely used for patterning as it is an etch-free process. An organic solvent like acetone is used to dissolve the photoresist (sacrificial material) and lift-off the target material on the top. Patterns are formed only in the regions where the target material makes direct contact with the substrate.

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RTP: good contact with minimum inter-diffusion can be achieved by fast annealing the sample at a temperature ramp rate of ~ 20 °C/s. The Ag-based CBRAM device is annealed in the RTP chamber at 400 °C for 600 s to form intimate contact between the electrodes and solid electrolyte.

PMA: similar to the wet oxidation, the sample is loaded into the center position of the horizontal alloy furnace filled with nitrogen gas to perform the PMA. The HfO₂-based RRAM device is annealed at 400 °C for 3 hrs to study the effect of thermal budget.

OPT: oxygen plasma is often used to strip the photoresist after the etch process. It also can be used for device engineering. The surface of TiN is passivated by using OPT with a power of 800 W and an oxygen flow of 800 ml/min to improve resistive switching uniformity.

(a)

(b)

(c)

(d)

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FIG. 21. Photos of various types of fabrication tools: (a) oxidation furnace, (b) sputter, (c) electron-beam evaporator, (d) ALD, (e) exposure tool, (f) RIE, (g) PECVD, and (h) RTP.

2.3 Characterization of RRAM Devices

For characterization of materials, the 4-point probe is used to measure the conductivity of the metal film, the surface profiler is used to measure the step height, the ellipsometry is used to measure the thickness of dielectric on the silicon substrate, the spectrophotometer is used to measure the film transmittance, the high-resolution transmission electron microscopy (HRTEM) is used to observe the cross-section of a sample, the X-ray photoelectron spectroscopy (XPS) is used to analyze the composition of a material, the scanning electron microscope (SEM) is used to inspect the surface of a sample, and the X-ray reflectometry (XRR) is used to measure the thickness of film on the metal substrate. Fig. 22 shows photos of various types of characterization tools.

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FIG. 22. Photos of various types of characterization tools: (a) 4-point probe, (b) surface profiler, (c) ellipsometry, (d) spectrophotometer, (e) HRTEM, (f) XPS, (g) SEM, and (h) XRR.

For electrical characterization, the Keithley 4200 semiconductor characterization system (SCS) is used to study DC behaviors of the RRAM device. The Agilent B1500A semiconductor device analyzer (SDA) is used to investigate AC responses such as pulse forming and endurance of the RRAM device. The Cascade CM300xi probe station is used to set up the connections between the tester and device. Fig. 23 shows photos of electrical characterization tools.

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(a)

(b)

(c)

FIG. 23. Photos of electrical characterization tools: (a) Keithley 4200 SCS, (b) Agilent B1500A SDA, and (c) Cascade CM300xi probe station.

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Two important DC parameters of resistive random access memory (RRAM) namely set compliance current (CC) and reset stop voltage (SV) are investigated. To achieve stable multi-level cell (MLC) operation, the boundaries of the DC parameters are determined. Unbalanced resistive switching such as over set and over reset can be observed via the I - V curves if the parameters are out of the ranges. A total of five resistance states have been obtained by varying the set CC while fixing the reset SV. The drifting of the high resistance state (HRS) resistances that occurred at low set CC can be retarded by slightly reducing the magnitude of the reset SV. This implies that the operation boundaries are dynamic and strongly correlated to the evolution of filament.

3.1 Introduction

It is well known that the multi-level cell (MLC) operation is an alternative way of improving the bits density of resistive random access memory (RRAM). As compared to the approaches of device scaling and 3D integration, the MLC operation seems to be easier since the engineering work is carried out at the circuit level instead of the device level. Many research works [72-77] have demonstrated the MLC operation by tuning the program/erase signals (DC/pulse). In the case of DC operation, multiple high resistance states (HRS) and low resistance states (LRS) can be achieved by varying the reset stop voltage (SV) and set compliance current (CC), respectively. Noted that when one parameter is changing, the other parameter is fixed. Since the number of states is limited by the resistance window, the operation boundaries need to be determined to

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maximize the sense margin. Little work has documented the method of finding the DC operation boundaries. In this work, the progressive analysis of the resistive switching I - V curves is used to define the upper and lower bounds of the DC parameters. The significant changes in the I - V characteristics can be observed if the parameters are out of the ranges. It is noticed that the R_{HRS} becomes unstable when low set CC is used. As switching variability is another factor that controls the number of states for a given resistance window, the magnitude of the reset SV is slightly reduced to mitigate the drifting of the R_{HRS} . A different concept of dynamic boundaries is proposed after taking the evolution of the filament into account.

3.2 Experiment

The cross-sectional view of the RRAM device is shown in Fig. 24. Pt bottom electrode (~50 nm) is deposited by the DC magnetron sputter on the SiO_2/Si substrate. HfO_2 switching dielectric (~11.26 nm) is formed by the atomic layer deposition (ALD) at 250 °C. The deposited HfO_2 is oxygen-rich with 2.14 oxygen (O 1s) to hafnium (Hf 4f) ratio based on the analysis of the elements conducted by the Thermo Scientific ESCALAB 250Xi X-ray Photoelectron Spectrometer (XPS). TiN top electrode (~60 nm) is deposited by the same sputter tool and the circular pattern with a size of 200 μm is achieved by the UV lithography and lift-off process. The measured sheet resistance (R_s) of TiN is around 13.11 Ω/sq . The electrical measurements are carried out by the Keithley 4200 semiconductor characterization system (SCS). The signals are applied through probe 1 while probe 2 is always grounded.

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FIG. 24. Schematic of the cross-sectional view of the RRAM device.

3.3 Results and Discussion

3.3.1 Pt/HfO₂/TiN RRAM Device Performance

The DC forming, reset, and set processes were investigated first to check the basic functionalities of the fabricated device. As the resistance of the pristine state of the device is usually quite high, around G Ω , a forming process is required to initialize the resistive switching. As shown in Fig. 25(a), the forming was carried out by sweeping the DC voltage from 0 V to 10 V with 10 μ A CC. A forming voltage (V_{form}) of 5.3 V was extracted at the point where the current first reached the compliance level. The discharging current observed from 0 V to $\sim$ 1.5 V was caused by the previous voltage sweep with stop voltage less than the forming voltage. A small read bias (0.1 V) was applied after the forming to validate the change of the resistance state. In this case, the resistance right after the forming is 190.77 Ω which suggests a huge transition of the resistance from high to low. It is noteworthy that a small CC would lead to volatile threshold switching [78]. Although the

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surge of the current was also observed in threshold switching, it did not guarantee that the filaments were successfully formed. On the other hand, a large CC would cause a hard breakdown of the device. Thus, the selection of the forming CC is an important step for the subsequent switching process. Based on the bipolar switching characteristic of the HfO₂-based RRAM device, a negative voltage is required to rupture the filaments. As shown in Fig. 25(b) blue curve, the reset process was performed by sweeping the DC voltage from 0 V to -2 V and back to 0 V without the CC. The maximum reset current (4.93 mA) is closed to the set CC (5 mA) due to the filaments-based switching mechanism [79]. The DC reset voltage (-0.8 V) was extracted at the point where the current reached the maximum value. The reset SV (-2 V) is an important parameter for the DC multi-bit operation since the resistance of the device increases with the magnitude of the SV. However, if the magnitude of the reset SV is too large, a hard breakdown or over reset of the device may occur. The gradual reduction of the current is attributed to the diffusion of the oxygen ions generated by the forming process [80]. As compared to the abrupt reset (a sudden drop of the current), the gradual reset would result in stable switching with a relatively small resistance window. The set process as shown in Fig. 25(b) red curve was conducted by sweeping the DC voltage from 0 V to 2 V and back to 0 V with 5 mA CC. Similar to the forming voltage, the set voltage (1.2 V) was extracted at the point where the current first reached the compliance level. Unlike the smooth I - V curve of reset, the sudden increase of the current was noticed owing to the formation of conductive filaments. The filaments are made of clusters of oxygen vacancies, and the quick generation of the oxygen vacancies is caused by the thermally driven positive feedback [81]. When more oxygen vacancies are created, the leakage current increases. This leads to an increase in the local temperature, which further assists the generation of oxygen vacancies. It is worth pointing out that instead of an abrupt set, the gradual set is preferred for the application of

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neuromorphic computing due to the linear modulation of the resistance [82]. However, a trade-off between the resistance window and the linearity hinders the development of RRAM-based artificial synapse. The set CC is another critical parameter for the DC multi-bit operation since the conductance of the device increases with the CC. Nevertheless, if the set CC is too high, it would result in hard breakdown or over set of the device.

FIG. 25. (a) *I-V* curve of DC forming. (b) *I-V* characteristics of bipolar resistive switching.

After examining the fundamental resistive switching process, the next step is to study the reliability of the RRAM device. DC endurance was conducted for 40 cycles to investigate the variation of the resistance and switching voltages. Fig. 26(a) shows the extracted R_{HRS} and R_{LRS} , and it is clear that the R_{LRS} is more stable than the R_{HRS} . From the statistics point of view, the resistance window (23.41) was calculated as the ratio between the minimum R_{HRS} and the maximum R_{LRS} . Fig. 26(b) shows the extracted set and reset voltages, and it is obvious that the reset voltage is more uniform than the set voltage. The average set voltage is 0.88 V with a standard deviation of 0.048 V and

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the average reset voltage is -0.69 V with a standard deviation of 0.016 V. Since the activation energy of the Hf-O bond breaking (2.9 eV) is higher than that of the oxygen ion/vacancy recombination (0.2 eV), the set voltage is larger than the magnitude of the reset voltage [81]. The variation of the set voltages is corresponding to the fluctuation of the R_{HRS} .

FIG. 26. DC cycling endurance: (a) Extracted R_{HRS} and R_{LRS} , and (b) Extracted set and reset voltages.

Besides endurance, another key index of reliability is data retention, which is used to evaluate the nonvolatility of the memory states. The data retention test was conducted at room temperature. A small read bias (0.1 V) with programmed intervals was applied to monitor the resistance states of the device. To minimize the read error, the average value of 10 sampling points was calculated for each reading. As shown in Fig. 27, both the R_{HRS} and R_{LRS} can sustain up to 10^5 s without any drift.

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FIG. 27. Data retention plot of the R_{HRS} and the R_{LRS} .

3.3.2 Determination of the DC Operation Boundaries

It is known that the R_{LRS} can be decreased by increasing the set CC and the R_{HRS} can be increased by increasing the magnitude of the reset SV. However, for stable resistive switching, both the set CC and the magnitude of the reset SV cannot be too large. The optimum ranges of the above parameters are worked out to achieve the balanced set/reset process. The word “balance” implies that there is no over set/reset during the resistive switching [67].

The maximum magnitude of the reset SV was investigated first. The same forming process was performed on each device to achieve stable R_{LRS} , then the reset processes with increased magnitudes of SV were conducted as shown in Fig. 28. The R_{HRS} is 3793.83 Ω , 5910.93 Ω , and 6563.58 Ω for -2 V, -2.2 V, and -2.4 V reset SV, respectively. Indeed, the R_{HRS} increases with the magnitude of the reset SV due to the widening of the electron tunneling gap. The shape of the I - V

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curve (colored in red) is different from others due to the appearance of surge current at the vicinity of the SV (-2.5 V). The lowering of the R_{HRS} (4330.62 Ω) was attributed to the over migration of the oxygen ions under high voltage. For the reset process with -2 V SV, the oxygen ions moved towards the bottom electrode under the electric field and recombined with the oxygen vacancies. Thus, an HRS was achieved owing to the rupturing of the filaments. Whereas for the reset process with -2.5 V SV, the enhanced electric field resulted in the rebuilding of the filaments due to rebreaking of the metal-oxygen bonds that were formed during the recombination. Hence, the R_{HRS} was reduced. To avoid the over reset, the magnitude of the reset SV should be less than 2.5 V. After considering the variations and power consumption, the maximum magnitude of the reset SV was set to 2 V.

FIG. 28. DC reset I - V curves with increased magnitudes of SV.

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After finding the maximum magnitude of the reset SV, the next step is to determine the maximum set CC. The bias conditions of reset were fixed to obtain uniform R_{HRS} . Fig. 29(a) shows the zoomed-in views of the set I - V curves with 5 mA and 20 mA CC. The I - V curve (colored in green) with 5 mA CC shows the typical set process with an abrupt transition of current. The I - V curve (colored in magenta) with 20 mA CC shows the two-stage transition. The first stage is abrupt whereas the second stage is gradual. Such characteristic was also observed for the I - V curve (colored in blue) with 10 mA CC as shown in Fig. 29(b). The second stage suggests the formation of the interfacial layer due to current-induced Joule heating [66]. The interfacial layer behaves as a series resistor, which limits the rise of the current [83]. The R_{LRS} is 163.31 Ω , 108.76 Ω , and 76.93 Ω for 5 mA, 10 mA, and 20 mA CC, respectively. The reduction of the R_{LRS} is caused by the widening of the diameter of the filaments. The shape of the I - V curve (colored in red) was significantly changed when CC was more than 20 mA. The increase of R_{LRS} (450.89 Ω) was attributed to the over migration of the oxygen ions. For the set process with 5 mA CC, the connection between the residual filaments and the bottom electrode was re-built by driving the oxygen ions towards the top electrode. Whereas for the set process with 30 mA CC, the oxygen ions were overdriven and recombined with the oxygen vacancies near the top electrode. As a result, the size of the filaments was shrunk, which led to an increase in R_{LRS} . The over set process is similar to the complementary resistive switching (CRS) process as shown in Fig. 30. From left to right, the status of filaments changes from rupture to formation then back to rupture, and the corresponding resistance state changes from HRS to LRS then back to HRS. On the other hand, the increase of the CC would facilitate the dissolution of the filaments due to the thermally-assisted recombination process. The set process with high CC would lead to unstable resistive switching

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due to unbalanced migration of oxygen ions. The maximum CC was selected to be 5 mA based on the single-stage transition of current.

FIG. 29. (a) The zoomed-in views of the set I - V curves with CC of 5 mA and 20 mA. (b) DC set I - V curves with increased CC.

FIG. 30. Schematic of the modulation of filaments under complementary resistive switching. The figure is taken from [42].

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To verify the deterioration effect of the high CC, the DC endurance test was conducted by using 8 mA set CC and -2 V reset SV. Fig. 31(a) shows the initial and final set I - V curves extracted from 20 DC cycles. Noted that the abovementioned two-stage transition of current was also observed for the 1st set process (colored in green). The 20th I - V curve (colored in blue) indicated the set failure since the current during the backward sweep (2 V $\rightarrow$ 0 V) was lower than the current during the forward sweep (0 V $\rightarrow$ 2 V). The lowering of the R_{HRS} and the rising of the R_{LRS} can be clearly shown in Fig. 31(b). The shrinkage of the resistance window was caused by the heat-induced oxidation reaction at the top electrode/dielectric interface [66]. The formation of the barrier layer (TiON) with high oxygen content could restrict the migration of the oxygen ions during the set and reset process. For comparison, the I - V curves of the 1st and 40th DC set process with 5 mA CC are shown in Fig. 32(a). The well-overlapped I - V curves implied the balanced resistive switching. Likewise, the DC endurance with 5 mA set CC and -2 V reset SV is shown in Fig. 32(b). No degradation of the resistance window was observed.

FIG. 31. (a) The 1st and 20th DC set I - V curves with CC of 8 mA. (b) 20 DC cycles with set CC of 8 mA and reset SV of -2 V.

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FIG. 32. (a) The 1st and 40th DC set *I-V* curves with CC of 5 mA. (b) 40 DC cycles with set CC of 5 mA and reset SV of -2 V.

After determining the upper limit of the set CC, the same methodology can be implemented to find the lower limit. Fig. 33(a) shows the DC set *I-V* curves with reduced CC. For the set process with 0.3 mA CC, there was no abrupt transition of current and the resistance window was less than 2. The set failure was observed if the CC was further reduced to 0.2 mA and below. As shown in Fig. 33(b), the current during the backward sweep was smaller than the current during the forward sweep owing to the insufficient energy applied. The set process involves two competing events, drift and diffusion. The drift of the oxygen ions towards the top electrode is driven by the electric field and it leads to the generation of oxygen vacancies. The diffusion of the oxygen ions towards the bottom electrode is triggered by the heat and concentration gradient and it results in the recombination of ions and vacancies. At low set CC, the recombination process could become more dominant as compared to the generation process since the activation energy of the generation process is much higher than that of the recombination process. As a result, the dissolution of

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filaments surpassed the formation of filaments. The minimum CC was set to 0.3 mA to make sure there was no occurrence of the set failure.

FIG. 33. (a) DC set I - V curves with reduced CC. (b) DC I - V curves with set failures.

Again, the same approach was used to find the minimum magnitude of the reset SV. Fig. 34(a) shows the DC reset I - V curves with reduced magnitudes of SV. For the reset process with -0.8 V SV, the resistance window was less than 2. The reset failure occurred when the SV was -0.7 V. As shown in Fig. 34(b), the current during the forward sweep overlapped with the current during the backward sweep. The applied energy was too weak to induce a change of resistance. To avoid the reset failure, the minimum magnitude of SV was set to 0.8 V.

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FIG. 34. (a) DC reset I - V curves with reduced magnitudes of SV. (b) DC I - V curve with reset failure.

3.3.3 Multi-bit Storage

With the ranges of the DC parameters determined, the multi-bit operation can be achieved via tuning the set CC while fixing the reset SV. Here, we demonstrated a total of five resistance states based on a pre-defined resistance window (~ 2) of adjacent states. In other words, the minimum resistance of state X is almost twice the maximum resistance of state X-1. Fig. 35(a) shows the DC endurance of each resistance state. State 5 is the HRS and the resistance were extracted from the reset process with -2 V SV. State 4 to state 1 are LRS and the resistance were extracted from the set process with 0.5 mA, 1 mA, 3 mA, and 5 mA CC, respectively. The data retention test of each resistance state as shown in Fig. 35(b) was also conducted at room temperature. For both reliability tests, there was no overlapping of the resistance among all the states.

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FIG. 35. (a) DC cycling endurance of each resistance state. (b) Data retention of each resistance state.

In Section 3.3.2, the R_{HRS} was enlarged by increasing the magnitude of the reset SV while the set CC was fixed. During the study of the multi-bit operation, it was noticed that the R_{HRS} could also be increased by reducing the set CC while the reset SV was fixed. Fig. 36(a) shows the effect of the set CC on the resistance of state 5. As a lower set CC (0.5 mA) would lead to the formation of weaker filaments, they were more prone to be ruptured during the reset process. To mitigate the drifting of the R_{HRS} , the magnitude of the reset SV should be reduced accordingly. Fig. 36(b) shows the maintenance of the resistance of state 5 after adjusting the reset SV from -2 V to -1.8 V. The evolution of the filament should be taken into consideration during the MLC operation. Instead of tuning one parameter while fixing the other one, both parameters should be engineered simultaneously. Besides the drifting of the initial resistance, the upward drifting of R_{HRS} with cycles might be caused by the enhanced recombination process. With consecutive switching, the accumulation of the Joule heating leads to the increase of the local temperature, which facilitates

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the recombination of ions and vacancies. As compared to the case of 0.5 mA set CC, the rate of upward drifting is slower for the case of 5 mA set CC, possibly due to the formation of stronger filament. With the reduced reset SV, the rate of upward drifting gets attenuated as well.

FIG. 36. (a) Effect of the set CC on the resistance of state 5. (b) Maintenance of the resistance of state 5 after adjusting the reset SV from -2 V to -1.8 V.

3.4 Conclusion

To maximize the resistance window, the operation boundaries of the DC parameters have been determined through the progressive analysis of the resistive switching I - V curves. The obvious changes of the I - V characteristics during the engineering of the DC parameters make the above process intuitive. For MLC operation, the pre-determined boundaries might not be suitable for all the resistance states due to the evolution of filament. Thus, the magnitude of the reset SV is slightly adjusted to mitigate the drifting of the R_{HRS} .

Chapter 4 Reduction of Pulse Forming Voltage via Signal Engineering

The electrical noise signal triggered switching of resistive random access memory (RRAM) device is investigated. As noise is also generated when powering up the light source, such a phenomenon can be easily mistaken as a light-activated event. Thus, it is necessary to conduct a “dark test” on the light related experimental work to make a correct judgement of the observation. Although noise is often undesirable, we show that the voltage amplitude of the noise signal which triggers the forming process is much lower than the unipolar pulse height owing to the facilitation effect of the negative voltage. As a result, we propose a novel bipolar pulse writing scheme to reduce the forming voltage and variability. Conversely, the reverse effect is demonstrated for the set process, as the role of the negative voltage changes with the state of the device. This study provides a guideline for the design and optimization of the operation signals of RRAM devices.

4.1 Introduction

RRAM as one of the emerging non-volatile memories has become a research hotspot in brain-inspired neuromorphic computing area [84], [85] owing to its fast read/write speed, low power consumption, excellent scalability, and complementary metal oxide semiconductor (CMOS) process compatibility [8, 30, 86]. However, the relatively high forming voltage of the RRAM device is a hurdle for the CMOS circuit due to the low voltage constraint although such operation is only required to be carried out once. Many approaches have been implemented to reduce the forming voltage or even make the device forming free such as film thickness scaling [87], film stoichiometry tuning [88], additional film insertion [89], CMOS process treatment [90], cell

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structure engineering [91], and pulse signals design [92]. Among these techniques, the engineering of the pulse signals conducted at the circuit level seems to be easier and more versatile when compared to other means applied at the device level. Despite that, the reduction of the forming voltage by using the bipolar pulse [92] is not significant as the pulse signal has not been fully optimized, and the effects of the negative voltage have not been investigated for the set operation.

In this work, we investigate the electrical noise signal triggered resistive switching and explore the implications through experimental study. During the electrical characterization of RRAM devices, we find that the noise signal can be generated when turning on the light source, and the signal can be coupled into the device under test (DUT) through the ground loop. The noise triggered resistive switching can be easily mistaken as a light-activated event. Therefore, it is necessary to perform a “dark test” to make a correct judgement on the observation. In particular, the light effect can be ruled out if the resistive switching occurs under the dark condition. Although noise is often undesirable, we notice an interesting fact that the voltage amplitude of the noise signal which drives the forming process is much lower than the unipolar pulse height. By studying the waveform of the noise signal, we speculate that the lowering of the forming voltage could be attributed to the facilitation effect of the negative voltage. To validate our assumption, a novel bipolar pulse writing scheme is proposed, and the reduction of the forming voltage and variability is observed for four different types of RRAM devices. On the contrary, the inhibition effect of the negative voltage is demonstrated for the set process, which implies that the role of the negative voltage varies with the state of the device.

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4.2 Experiment

The noise triggered resistive switching phenomenon was first found on device A with Pt/HfO₂/TiN structure. The Pt (~50 nm) bottom electrode was sputtered on the Ti/SiO₂/Si substrate, followed by the atomic layer deposition (ALD) of 5.90-nm-thick HfO₂ dielectric layer at 250 °C. The TiN (~120 nm) top electrode was sputtered at room temperature and the circular pattern with a size of 100 μm was achieved by the UV lithography and lift-off process. A 5.57-nm-thick dielectric of device B (Pt/ZrO₂/TiN) and a 5.34-nm-thick dielectric of device C (Pt/Al₂O₃/TiN) was deposited by the ALD process as well. For device D (TiN/HfO₂/TiN), everything is the same as device A except the bottom electrode. The 3-D schematics of the four devices are shown in the inset of Fig. 41(a)-(d), respectively. The electrical tests were conducted by the Agilent B1500A semiconductor device analyzer (SDA) with the Cascade CM300xi probe station. The voltage signals were applied to the top electrode while the bottom electrode was always grounded. The waveforms of electrical noise signals were captured by the Tektronix TD3052 two-channel color digital phosphor oscilloscope.

4.3 Results and Discussion

4.3.1 Discovery of the Noise-induced Resistive Switching

Device A was connected to the SDA through probing. Since the probe station is light-tight, the device gets disturbed only when the light source (EKE 21V 150 W halogen lamp) of the microscope is turned on. A potentiometer knob is used to control both the on/off and light intensity of the lamp. A light guide is connected between the light source and microscope. The leakage current of the device was sensed by applying a small DC bias (0.1 V) with a long duration (>10 s)

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in sampling mode. As shown in Fig. 37(a), a huge change in leakage current was detected when the lamp was turned on at about 7.6 s. After that, the current remained unchanged regardless of the switching of the lamp possibly due to the formation of stable filaments. The transition from a virgin state to a low resistance state (LRS) is defined as a forming process. The LRS can be reset back to a high resistance state (HRS) by applying a negative voltage sweep from 0 V to -2 V. A set process (HRS→LRS) as shown in the inset of Fig. 37(a) was captured when the lamp was turned on again. The above forming and set process could be activated by just switching on the lamp without applying the DC bias (0.1 V) concurrently. The impact of the DC bias could be ignored since the low resistance values after the forming/set process with/without the DC bias were quite comparable. Besides, we carried out the same tests on other devices with different HfO₂ thicknesses. For devices with 10.13-, 15.03-, and 18.93-nm-thick HfO₂, the forming process could not be triggered by turning on the lamp. However, after the DC forming (positive voltage sweep with 10 μ A current compliance) as shown in Fig. 37(b) and reset process, the set process could be stimulated by switching on the lamp.

(a)

(b)

FIG. 37. (a) Noise triggered forming process detected by the SDA. The inset shows the noise triggered set process. (b) DC forming process of device A with different HfO₂ thicknesses.

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A hypothesis of light-driven resistive switching was proposed initially since similar phenomena [71, 93-97] have been reported. During the verification, our measurement results as shown in Fig. 38 such as the low transmittance of TiN, device size-, light power-, and wavelength-independent resistive switching contradicted the hypothesis. For the transmittance measurement, the TiN was deposited on the quartz substrate first. Then, the transmittance of the quartz substrate was measured, followed by the measurement of TiN on the quartz sample. The maximum transmittance of TiN was calculated to be ~1.7% at the wavelength of 504 nm, and our result was consistent with the prior work [98]. The effects of device size, lamp power, and wavelength on resistive switching were studied via the control variable method. For instance, full-spectrum emission and 3.5 mW lamp power were used for the investigation of the cell size effect. Likewise, full-spectrum emission and 100 μm device size were used for the examination of the lamp power effect. Similarly, 100 μm device size and 3.5 mW lamp power were used for the exploration of the wavelength effect. Noted that the power of monochromatic light varies with the wavelength, although the lamp power is fixed. The stable R_{LRS} suggests that there is no strong correlation between the set process and light exposure for the given ranges of parameters. In view of the phenomena unlikely caused by light, the electrical noise signals generated during powering up the electrical appliances were thought to be responsible for these events. To eliminate light interference, a simple “dark test” was conducted. The light guide was detached and covered at the lamp side. The same resistive switching of the device was observed when the lamp was turned on and the low resistance values after the forming/set process with/without the light exposure were almost the same. As the light factor was ruled out, we confirmed that the energy required to induce the resistive switching was from the electrical noise signal.

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FIG. 38. (a) The transmittance of 120 nm TiN measured by PerkinElmer LAMBDA 950 UV/Vis/NIR Spectrophotometer. (b)-(d) show the independence of the R_{HRS} and R_{LRS} on cell size, lamp power, and wavelength, respectively. The lamp power was measured by the THORLAB PM100 power meter with S130A slim sensor. The single wavelength was selected by the TMc 300 Monochromator. The HRS was achieved by DC reset and the LRS was achieved by turning on the lamp.

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As shown in Fig. 39(a), the full waveform of the noise signal was captured by an oscilloscope with the time scale set to microseconds. The noise signal is composed of many irregular pulses with random peaks. The maximum and minimum peak values in the starting region (highlighted in yellow) of the waveform are 1.56 V and -1.60 V, respectively. After a few microseconds, the signal gets attenuated significantly. The relatively long transition time as shown in Fig. 37(a) was attributed to the system delay in SDA. To have a zoomed-in view of the starting region, the time scale of an oscilloscope was adjusted to nanoseconds. The partial waveform of another noise signal is shown in Fig. 39(b). The maximum and minimum peak values are 1.64 V and -1.66 V, respectively. The slight variation of the peak values was caused by the minor change of the knob position after each turning. The pulse width of individual peak varies from several nanoseconds to tens of nanoseconds. We found that the maximum and minimum peak values were independent of the resistance state and dielectric thickness of the device. For the device with a thicker dielectric (≥ 10 nm), the noise signal was not sufficient to trigger the forming process as a higher forming voltage was required. Since the set voltage is independent of the dielectric thickness [99], the noise triggered set process was still observed.

FIG. 39. (a) The full waveform of the noise signal captured by an oscilloscope. (b) The partial waveform of the noise signal.

4.3.2 Facilitation Effect of Negative Voltage

As the noise signals are often undesirable and are not suitable for practical applications, the commonly used unipolar pulse (Type I) as shown in Fig. 40 is preferred. For all types of pulses used in this study, the rise/fall time, pulse width, and duty cycle were set to 10 ns, 500 ns, and 50%, respectively. Based on the bipolar resistive switching behavior of device A, a positive voltage is required for the forming and set operations to form the filaments whereas a negative voltage is needed for the reset operation to rupture the filaments. The pulse forming voltages of 15 samples were collected and the mean and standard deviation are 3.62 V and 0.21 V, respectively. A significant reduction of the forming voltage was realized when we compared the unipolar pulse height with the maximum peak value of the noise signal. As prior work [92] has reported the reduction of the forming voltage through the engineering of bipolar pulse, we speculated that the strong negative peaks that appeared in the noise signal could effectively facilitate the forming

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process. To validate our assumption, we designed a novel bipolar pulse (Type II) with negative starting voltage (highlighted by the red dotted circle) and uniform amplitude as shown in Fig. 40. The bipolar pulse forming was conducted on 15 samples as well. Since the maximum voltage drop across the device is the positive peak voltage instead of the peak-to-peak voltage, the mean (2.27 V) and standard deviation (0.08 V) were calculated based on the positive peak values. The box plots of the unipolar and bipolar pulse heights are shown in Fig. 41(a). A significant improvement in both the mean and standard deviation was achieved by using the bipolar pulse. Three more devices with different film stacks were fabricated to further verify our hypothesis. As expected, the noise triggered resistive switching was demonstrated for all devices. Furthermore, the bipolar pulses-induced lowering of the forming voltage and variability are also illustrated in Fig. 41(b)-(d).

FIG. 40. Three different types of pulses studied in this work.

FIG. 41. (a)-(d) Box plots of the unipolar and bipolar pulse heights for devices A, B, C, and D, respectively. The inset shows the 3-D schematic of the RRAM device.

Table III summarises the means (μ) and standard deviations (σ) of unipolar and bipolar pulse heights. The reduction percentages of means and standard deviations are quite consistent for all devices. Based on the results from device A, B, and C, it seemed that the bipolar pulse approach could be applied to metal oxide-based RRAM devices with different dielectric materials and asymmetric electrodes to reduce the forming voltage, and such method might also work for devices

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with symmetric electrodes according to the data from device D. To our best knowledge, the pulse forming voltages of the four types of devices are reported for the first time. When compared to the 10% improvement demonstrated in prior work [92], we achieved a much higher percentage of reduction of the pulse forming voltage. Since the device (TiN/HfO₂/Ti) reported in prior work [92] was different from our devices, a device (Pt/HfO₂/TiN) from prior work [100] with similar stack information when compared to our device A was chosen as the reference. The DC forming voltage of the reference device with 5-nm-thick HfO₂ and a size of 400 μm is around 3.5 V which is comparable to the unipolar pulse forming voltage of device A (3.62 V). Although device A has a thicker HfO₂ (5.90 nm) and smaller device size (100 μm), a much lower bipolar pulse forming voltage of 2.27 V was obtained. For other types of devices, it is quite hard to make a direct comparison with the prior works [101-103] since the bipolar pulse is not the only contributor to the reduction of the forming voltage.

Device	Unipolar pulse		Bipolar pulse		Reduction	
Type	(V)		(V)		(%)	
	μ	σ	μ	σ	μ	σ
A	3.62	0.21	2.27	0.08	37.4	61.3
B	2.90	0.27	1.78	0.09	38.6	67.8
C	3.78	0.26	2.33	0.09	38.4	65.6
D	2.59	0.21	1.72	0.09	33.7	58.7

TABLE III. Summary of the means (μ) and standard deviations (σ).

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The forming process can be regarded as a soft breakdown of the dielectric. For metal oxide-based RRAM devices, conductive filaments which are made of oxygen vacancies are formed after the forming due to the breaking of the metal-oxygen bonds and migration of the oxygen ions. The generation of oxygen vacancies is controlled by both the electric field and temperature. The higher the electric field and temperature, the lower the activation energy for oxygen dissociation [81]. To understand the mechanism behind the negative voltage effect phenomenon, the energy band diagrams of pristine devices were plotted as shown in Fig. 42. The work functions of Pt and TiN, the electron affinities, and bandgaps of HfO_2 , ZrO_2 , and Al_2O_3 were extracted from literature [104-108]. For device A, B, and C, the barrier height at the top metal/metal oxide interface is much smaller than that at the bottom interface due to the work function difference between Pt and TiN. It is well known that the lower the conduction band offset, the easier the electron transport. Thus, more electrons could be injected from the TiN under the negative bias when compared to the case of positive bias. With more electrons injected, the phonons generated during the transport of electrons through initial defects increase the local temperature and reduce the energy barrier for breaking of the chemical bonds [109]. In other words, a lower electric field is required to relocate the oxygen ions. Since the negative starting voltage could facilitate the activation process more effectively when compared to the positive voltage, the bipolar pulse height can be reduced. We also tried to use the negative unipolar pulse to trigger the initialization process of device A. Although the magnitudes of the negative unipolar pulses were smaller than the positive ones, devices were unable to be switched back to the HRS due to the hard breakdown. Thus, such a pulse writing scheme was not adopted. The intra-variation of the forming voltages could be attributed to the stochastic formation of initial defects in the metal oxide. Owing to the strong facilitation effect of the negative voltage, it allows more room for variation of the defects. Hence, the standard

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deviation gets improved as well. The inter-variation of the forming voltages among device A, B, and C was mainly caused by the different thicknesses and chemical bond energies of the dielectric materials and different barrier heights at the metal/metal-oxide interfaces.

FIG. 42. (a)-(d) Schematic energy band diagrams of pristine devices. The bottom barrier height of device D is not given as the exact value has not been reported by prior work. (TE: top electrode, BE: bottom electrode, E_F : Fermi level, E_{CBM} : conduction band minimum, E_{VBM} : valence band maximum, Φ_{eb} : bottom barrier height, Φ_{et} : top barrier height, E_g : energy bandgap.)

Although both electrodes of device D are the same, the barrier heights at the interfaces might not be symmetric due to the barrier modulation which is caused by the process-induced interfacial layer (IL) [107], [110]. We ignore the bottom ILs for the as-fabricated device A, B, and C owing

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to the chemical inertness of Pt, and the top ILs of all devices can also be neglected due to the inactiveness of TiN at room temperature. Take note that the switching-induced ILs could be formed at the top interfaces after the forming process as a result of the redox reaction. The formation of bottom IL (TiON) of device D was attributed to the oxygen scavenging ability of TiN and the oxidation effect of water vapor at elevated temperature [111]. Since the bottom IL is dominant, the barrier height at the top interface is lower than that at the bottom interface [110]. The energy band diagram as shown in Fig. 42(d) was drawn based on the bandgap of TiON and valence band offset between TiN and TiON reported in the literature [112]. Although the difference between the two barrier heights of device D is smaller than that of other devices, the significant lowering of the bipolar pulse height reveals the stability of the negative voltage effect. The unipolar pulse height of device D is smaller than that of device A due to the lower barrier height at the bottom interface and IL-induced generation of oxygen vacancies in the HfO₂ layer. It is worth noting that the resistance of the devices after the bipolar pulse forming are less than 100 Ω . The filaments are so strong that the negative pulse (2nd half of the bipolar pulse) is insufficient to trigger the reset process.

To further validate the hypothesis of energy band offset at the metal/oxide interface, the DC sweep test has been conducted for all types of devices. Results, as shown in Fig. 43, indicate good consistency in terms of more current has been observed in the negative voltage regime than in the positive one due to the difference of energy barriers at both interfaces. To avoid the intra device variation, the leakage currents under both voltage regimes were measured for the same device of each type by keeping the magnitude of the stop voltage below the forming voltage. The leakage current was extracted at ± 2 V for device A and C and ± 1.5 V for device B and D due to the inter-

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device variation. The DC sweep was carried out five times for both voltage regimes to ensure the accuracy of the results.

FIG. 43. (a)-(d) Box plots of the leakage current extracted during the positive and negative voltage sweep for devices A, B, C, and D, respectively.

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4.3.3 Inhibition Effect of Negative Voltage

To verify the success of bipolar pulse forming and examine the operation polarity, the DC I - V characteristics of all devices were measured as shown in Fig. 44. The set processes were carried out by sweeping the voltage from 0 to 1 V with different compliance currents. Noted that the compliance current was optimized for each type of device to obtain stable resistive switching with a similar resistance window. The reset process was conducted by sweeping the voltage from 0 to -1 V. All devices exhibit bipolar resistive switching behavior with the same operation polarity. The variations on the I - V curves were possibly attributed to the difference in terms of dielectric and electrode materials. The reliability performance after the bipolar pulse forming was also examined by conducting the DC endurance and high-temperature data retention tests on device A. As shown in Fig. 45, no degradation of the resistance window was observed for the given test cycles and period. We further investigated the negative voltage effect on the set process. Again, device A was studied first. To keep the device at a stable HRS, the DC reset was used after each pulse set. The set voltage was determined by applying the unipolar pulse. For the R_{HRS} of $\sim 3\text{ K}\Omega$, a 0.6 V is required to achieve the R_{LRS} of $\sim 200\text{ }\Omega$. After that, the bipolar pulses with voltage amplitudes varied from 0.1 V to 0.6 V were tested. However, there was no setting of the device after applying the bipolar pulses. This phenomenon implies that the negative voltage could inhibit the set process.

FIG. 44. (a)-(d) Typical I - V characteristic of each device after the bipolar pulse forming. All devices show bipolar resistive switching behavior with the same operation polarity. (CC, compliance current; SV, stop voltage.)

FIG. 45. (a) DC cycling endurance of device A after the bipolar pulse forming. (CC, compliance current; SV, stop voltage.) (b) High-temperature data retention test of device A.

The nonuniform bipolar pulse (Type III) as shown in Fig. 40 was engineered to examine the negative voltage effect. The positive peak voltage of the nonuniform bipolar pulse was fixed at 0.6 V and the negative starting voltage was varied from -0.1 V to -0.7 V. Fig. 46(a) shows the correlation between the resistance after the set operations and the negative peak voltages. The shaded areas indicate the states of the device. The set process was not affected by the negative voltage if its magnitude is less than or equal to 0.3 V. The disturbance to the set process was noticed when the magnitude of the negative voltage is greater than 0.3 V. The intermediate LRS1 and LRS2 imply the retarded set operations and the HRS suggests the counteraction of the positive and negative voltage effects. When the negative peak voltage reached -0.7 V, the set process was converted to the reset process since the resistance became larger than the R_{HRS} . The inhibition effect of the negative voltage is determined by the state of the device. Due to the tremendous increase in the leakage current after the forming process, the energy supplied by the negative

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voltage is much higher than the energy required for the activation process. Thus, the extra energy could be utilized to drive the oxygen ions towards the bottom electrode. The drift direction of the oxygen ions under the negative bias is opposite to that under the positive bias. Hence, the reset process is competing against the set process when a bipolar pulse is applied. The inhibition effect of the negative voltage was not observed for the noise triggered set process possibly due to a much higher R_{HRS} of $\sim 500\text{ K}\Omega$ and a much larger positive peak voltage of $\sim 1.6\text{ V}$.

The same methodology has been implemented on other devices and the results were consistent. When compared to device A and B, a slightly higher set voltage of 0.7 V was found for the device C and D. Thus, the negative peak voltage was evaluated until -0.8 V as shown in Fig. 46(b) to capture the transition from set to reset. All devices have demonstrated the inhibition effect of the negative voltages according to the trends of resistance as shown in Fig. 46.

FIG. 46. The correlation between the resistance after the set operation and the negative peak voltages of the nonuniform bipolar pulses: (a) data collected from devices A and B, and (b) data collected from devices C and D.

4.4 Conclusion

In summary, the phenomenon of noise triggered resistive switching was investigated and three important implications were explored. First, a “dark test” was proposed for the light related experimental works to examine if the resistive switching was activated by the undesirable electrical noise signal. Second, inspired by the unique waveform of the noise signal, a novel bipolar pulse writing scheme was designed to reduce the forming voltage and variability owing to the facilitation effect of the negative voltage. Last but not least, the negative voltage could inhibit the formation of filaments during the set process due to the leaky state of the device. Thus, our work provides a guideline for the design and optimization of the operation signals of RRAM devices.

Chapter 5 Reliability Improvement Through Device Structure Engineering

The resistive switching variability and reliability degradation are the two major challenges that hinder the high-volume production of the resistive random access memory (RRAM) devices. In this work, a 3-D electrode structure engineering method is proposed. The geometric parameters defined as electrode angle (EA), electrodes spacing (ES) and electrode trench depth (ETD) associated with the double wedge-like electrodes of the filament-type RRAM devices are studied for the first time. Our experimental results show that apart from the resistive switching uniformity, the reliability performance such as cycling endurance and data retention is significantly improved for the device with small EA (90°), narrow ES (440 nm) and deep ETD (90 nm) owing to the electric field confinement and enhancement. Thus, this new approach can be served as a guideline for the design and optimization of filament-type RRAM devices.

5.1 Introduction

The fourth fundamental two-terminal circuit element named memristor has been found by Hewlett Packard labs more than one decade ago [20]. Up to now, a wide range of applications such as non-volatile memory [113], in-memory computing [114], artificial neural network [115, 116], and chaotic system [117] have been demonstrated by using memristor. RRAM as one type of memristor has drawn much attention due to its fast read/write speed, low power consumption, simple metal-insulator-metal (MIM) device structure, and complementary metal oxide semiconductor (CMOS) compatibility [118-120]. However, the resistive switching variability which is caused by the inherently stochastic nature of the generation and migration of defects [60]

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seems to be the fundamental issue of RRAM devices despite various techniques [61, 63, 121-128] have been implemented. Among which the electrode structure engineering through the reactive ion etching (RIE) process can be widely adopted by the CMOS foundries to enhance the performance of the filament-type RRAM devices [63, 124]. The electrode structure-induced filaments confinement provides good filaments control [63] without embedding additional materials into the RRAM stacks [61, 121] and scales the effective switching area to several nanometers in diameter [124] without using the expensive extreme ultraviolet (EUV) lithography process. To date, prior works [63, 123-128] have shown improvement by engineering the structure of a single electrode. The filaments confinement can only be achieved near the engineered electrode. Devices with both structurally modified electrodes have not been demonstrated. Therefore, the effects of the variation of the electrode geometric parameters on device performance have not been investigated as well. Furthermore, the filaments confinement which has been mostly explained by the models and simulation results has yet to be proven by the microscopic images.

The Ag-based RRAM devices with planar double wedge-like electrodes were designed and fabricated in this work. The combination of one flat electrode with one wedge-like electrode was not studied here as many research works have been done with similar comparison and the conclusions have been consistent with better performance being achieved using non-flat type electrodes. Thus, the engineering of the electrode geometric parameters of both electrodes was the key focus here. The 3-D schematics of the fabricated device and the planar double wedge-like electrodes with three geometric parameters are shown in [Fig. 47\(a\)](#). Electrode angle (EA) is defined as the vertex angle of the isosceles triangle within the XY plane, and it can be varied by changing the photomask patterns (isosceles triangles) with different vertex angles. Electrodes spacing (ES) in the Y direction is the minimum distance between two wedge-like electrodes, which

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can be adjusted by fine-tuning the photolithography alignment process. Electrode trench depth (ETD) is equivalent to the thickness of the electrode along the Z direction and it can be modified by changing the duration of the etch process. The improvement of the device performance including resistive switching uniformity, cycling endurance, and data retention was achieved by appropriate engineering of the above electrode geometric parameters. It is noteworthy that both wedge-like electrodes are placed side by side with the tip to tip orientation for the ease of device fabrication and Ag filaments observation [78, 129] when compared to the vertical one which is shown in [Fig. 47\(b\)](#). The main objective of this work is to demonstrate and validate the feasibility of the proposed 3-D electrode structure engineering method by comparing the performance of devices with different sets of electrode geometric parameters. The data presented here serve as important references for the future development of the filament-type RRAM device with the vertical configuration for high-density memory application.

FIG. 47. (a) 3-D schematics of the fabricated RRAM device and the planar double wedge-like electrodes with three geometric parameters. (b) 3-D schematic of the vertical double wedge-like electrodes.

5.2 Experiment

The Ag/a-Si/TiN RRAM device was fabricated with the following process steps. First, a 550 nm SiO₂ isolation layer was grown on the silicon substrate by the wet oxidation process. Then, a 300 nm a-Si layer which served as the solid electrolyte was deposited by the plasma-enhanced chemical vapor deposition (PECVD) at 300 °C. The inert electrode pattern was transferred to the sample through the i-line UV photolithography process followed by the reactive ion etching (RIE) with Cl₂ gas. The inert electrode trench was filled by TiN during DC magnetron sputtering of Ti target in the N₂ environment. The subsequent lift-off process ensured only the defined electrode area was covered by TiN. Similar lithography, RIE and lift-off processes were used to pattern the Ag active electrode. The electron beam evaporation was used to deposit Ag due to the lower deposition rate when compared to that of the sputtering process. A good Ag to a-Si adhesion can be achieved with the low deposition rate. At last, the device was N₂ annealed by the Rapid Thermal Processing (RTP) at 400 °C for 600 s. The schematic of the cross-sectional view of the device after each fabrication process is shown in [Fig. 48](#). All electrical tests were conducted by using the Keithley 4200 semiconductor characterization system. The double wedge-like electrodes and the distribution of the Ag filaments were observed by the Scanning Electron Microscopy (SEM).

FIG. 48. Schematic of the cross-sectional view of the device after each fabrication process.

5.3 Results and Discussion

5.3.1 Effects of Electrode Angle (EA)

Research on the electrode geometric parameters was systematically carried out. First, EA parameter was examined. A total of five EA namely 150°, 120°, 90°, 60°, and 30° were designed. With fixed ETD (20 nm) and photomask pattern defined ES (2 μm), the actual ES measured by the SEM for different EA (not shown here) indicated that the devices with EA less than 90° suffered from serious electrode corner shrinkage issue due to pattern dependent optical proximity effects [130]. In other words, ES gets larger for smaller EA. To exclude the ES variation, only the EA of 150°, 120°, and 90° with almost the same ES (2.6 μm) as shown in Fig. 49(a) were used in this experiment. As the device dimensions are limited by the resolution of the i-line UV mask aligner, advanced lithography techniques are required for future study of the effects of the small

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EA ($<90^\circ$). The inset of Fig. 49(b) shows the forming process, which was conducted on the device with 120° EA by applying a small constant voltage (1 V) to the Ag anode for 5000 s while the TiN cathode was grounded. The cell resistance decreased from the initial high resistance ($\sim 10^{11} \Omega$) to the final low resistance ($\sim 200 \Omega$) with a stepwise profile owing to the gradual growth of the Ag filaments [131]. The saturation of resistance after 2500 s indicated the cease of filaments growth, which was attributed to the reduction of the voltage drop across the solid electrolyte. As shown in Fig. 49(b), typical bipolar resistive switching behavior was observed with the set process (the increase of conductance) that occurred in the positive DC sweep ($0 \text{ V} \rightarrow 2 \text{ V}$) and reset process (the decrease of conductance) occurred in the negative DC sweep ($0 \text{ V} \rightarrow -1.5 \text{ V}$). The formation and dissolution of the Ag filaments were responsible for the resistive switching from high resistance state (HRS) to low resistance state (LRS) and vice versa, respectively [132]. The resistance window (the ratio of HRS resistance to LRS resistance) read at 0.1 V was about one order.

FIG. 49. (a) SEM image of the Ag/a-Si/TiN device with EA= 120° , ES= $2.6 \mu\text{m}$, and ETD= 20 nm before the forming process. (b) Bipolar I - V characteristics of the Ag/a-Si/TiN device after the forming process. The inset shows the forming process with a constant voltage of 1 V.

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The same test conditions of forming, set, and reset were used to characterize the other devices with different electrode parameters. 200 consecutive DC sweep cycles were conducted on the aforementioned three devices immediately after the forming process to study the resistive switching uniformity. An obvious trend towards stable resistive switching was noticed by comparing the I - V characteristics of the devices with different EA for 50 cycles as shown in Fig. 50(a)-(c). The instability of the resistive switching which was described as the abrupt current drop during the reset process as shown in Fig. 50(d) was significantly reduced through shrinkage of the EA. Since the event of the abrupt reset was random, the cumulative probability versus resistance plot was used to illustrate the changes. For striking comparison, only the worse and the best data are shown in Fig. 51. For the device with 150° EA, the extremely high resistance ($>10^8 \Omega$) which were caused by the abrupt reset were highlighted by yellow. The percentage was calculated to be 59% whereas the occurrence probability of the extremely high resistance was 0% for the device with 90° EA (the average value of the HRS resistance was $\sim 2.8 \text{ K}\Omega$).

FIG. 50. (a)-(c) I - V characteristics of the devices with 150° , 120° , and 90° EA, respectively for 50 DC sweep cycles. (d) I - V characteristics of the device with 150° EA for one DC sweep cycle randomly picked from the 50 cycles.

FIG. 51. The statistical distribution of the R_{HRS} and R_{LRS} for 200 DC sweep cycles for two devices with different EA.

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It was assumed that different EA led to different resistive switching mechanisms. To verify the assumption, SEM was used to directly observe the distribution of the filaments. Interestingly, a clear tendency of narrowing of the Ag filaments distribution along the X direction was captured right after the cycling operation for the above three devices. As shown in Fig. 52, with the same magnification (x2420), the distribution of the Ag filaments (indicated by the red bidirectional arrow) in the device with 150° EA was much broader than that of the device with 90° EA, which implied that smaller EA could provide better filaments confinement, thus better filaments control and switching uniformity. To theoretically explain the phenomenon, we referred to the electric field simulation works done by other groups [63, 124] the strongest electric field along the Y direction should be allocated at the tip region of the double wedge-like electrodes and the electric field strength gradually get weakened in the surrounding area according to the contour of the electrode. The decreasing rate of the electric field strength is inversely proportional to the EA. For a given voltage bias, the coverage of the electric field which could drive the Ag ions was much smaller in the device with a smaller EA. Therefore, electric field confinement could be achieved by reducing the EA. In the meantime, a smaller EA associated with a smaller electrode tip radius also gave rise to the enhancement of the electric field [133].

(a)

(b)

FIG. 52. SEM images of the distribution of the Ag filaments right after the cycling operation: (a) device with 150° EA, and (b) device with 90° EA.

To explain the huge difference between the R_{HRS} of the two devices, two resistive switching models as shown in Fig. 53 were proposed. For the device with 150° EA, multiple filaments with low Ag atom density were formed after the set process due to distributed and weak electric field. Rupture of the filaments was more likely to be the resistive switching mechanism during the reset process. However, the filaments formed in the device with 90° EA were concentrated and dense owing to the confined and strong electric field. The increasing of the Ag atom concentration in the filaments should be the resistive switching mechanism for the set process, and vice versa for the reset process. We also studied the effect of EA variation on device reliability such as data retention due to instability of the Ag filaments [48]. The same set of devices was tested at room temperature with the application of 0.1 V read voltage for 1000 s. However, the effect of EA variation on data retention was insignificant based on the test results (not shown here). A plausible explanation was given in the following section.

FIG. 53. The proposed resistive switching models for two devices (top view) with different EA.

5.3.2 Effects of Electrode Spacing (ES)

Next, the ES parameter was investigated. A 440 nm ES as shown in Fig. 54(a) was obtained by fine-tuning the UV lithography alignment process. Both EA and ETD were fixed at 120° and 20 nm, respectively. The forming process was found to be much faster in the device with shorter ES. As shown in the inset of Fig. 54(b), the forming process took about 100 s to change the device's resistance from the initial state of ~800 K Ω to the LRS of ~300 Ω . The acceleration of the forming process was caused by the shortening of the Ag migration path and the enhancement of the electric

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field. Furthermore, the set sweep ($0\text{ V} \rightarrow 2\text{ V} \rightarrow 0\text{ V}$) current-voltage curve as shown in Fig. 54(b) was smoother than that of Fig. 49(b), which indicated the formation of more stable Ag filaments.

FIG. 54. (a) SEM image of the Ag/a-Si/TiN device with $EA=120^\circ$, $ES=440\text{ nm}$, and $ETD=20\text{ nm}$ before the forming process. (b) Bipolar I - V characteristics of the Ag/a-Si/TiN device after the forming process. The inset shows the forming process with a constant voltage of 1 V .

To investigate the current conduction mechanism, the set sweep current-voltage curve was replotted in a log-log scale with linear fittings as shown in Fig. 55. Ohmic conduction with the slope of ~ 1 was demonstrated in the LRS curve. However, the HRS curve was divided into three different segments. In the low-voltage region, Ohmic transport with the slope of ~ 1 was observed whereas the slope increased to ~ 2 and further rose to ~ 3 in the high-voltage region, which showed good agreements with the space-charge-limited current (SCLC) conduction mechanism [134].

FIG. 55. Logarithmic I - V plot of the Ag/a-Si/TiN device. The linear fittings show good agreement with the space-charge-limited current (SCLC) conduction mechanism.

The stability of the Ag filaments was further verified by the data retention tests as shown in Fig. 56. When compared to the device with 440 nm ES, both HRS and LRS resistance of the device with 2.6 μm ES were increasing, which led to the shrinkage of the resistance window from ~ 11 to ~ 2 . The drifting of the resistance suggested the dissolution of the Ag filaments and the dissolution rate was highly dependent on the width of the filaments [135]. To acquire better data retention, wider filaments width was required. For this case (planar device), the length of the filaments was along the Y direction and the width of the filaments was along the Z direction. A model as shown in Fig. 57 was proposed to illustrate the improvement of data retention. It was worth noting that the actual angle formed between the trench base and the trench sidewall was not 90° due to the lateral etching effect. The electric field became weak as it went deep along the Z direction because of the slanted sidewall profile. Since the stronger electric field was induced in a device with

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narrower ES, Ag atoms located below the electrode surface could participate in the process of filaments formation, which resulted in filaments with a wider diameter. In the previous section, although the electric field was enhanced by reducing the EA, the electric field strength might not be sufficient to drive the Ag atoms beneath the surface as the bulk migration was more resistive than the surface migration. It is speculated that the small EA ($<90^\circ$) could further improve both the switching uniformity and data retention.

FIG. 56. Data retention tests performed at room temperature for 1000 s: (a) device with 2.6 μm ES, and (b) device with 440 nm ES.

FIG. 57. The proposed model for the formation of stable filaments in the device (cross-sectional view) with shorter ES.

Similarly, the resistive switching uniformity test was carried out for the two devices. As shown in [Fig. 58](#), the occurrence probability of the extremely high resistance was reduced from 6.5% to 0% by narrowing the ES from $2.6\mu\text{m}$ to 440 nm. Once again, the improved resistive switching uniformity was attributed to the confined distribution of the Ag filaments as shown in [Fig. 59](#). The relatively dark rectangle that appeared in [Fig. 59\(b\)](#) was caused by the enhanced electron charging effect during the focus tuning process within a small rectangular area which was defined by the SEM user, and the distribution of the filaments was not affected by the electron irradiation. The rapid formation of the Ag filaments in the center of the device with short ES eliminated the growth of the surrounding filaments due to the reduction of the voltage drop across the solid electrolyte. The reliability data of the submicron-scale device with Ag electrode and a-Si solid electrolyte [136,

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137] were demonstrated. However, the device performance was limited by the ES, which was limited by the resolution of the i-line UV mask aligner. Based on the promising data shown by other references in [138-140], the vertical cell configuration could provide an easy way to achieve nanometer-scale ES with better results.

FIG. 58. The statistical distribution of the R_{HRS} and R_{LRS} for 200 DC sweep cycles for two devices with different ES.

FIG. 59. SEM images of the distribution of the Ag filaments right after the cycling operation: (a) device with 2.6 μm ES, and (b) device with 440 nm ES.

5.3.3 Effects of Electrode Trench Depth (ETD)

Finally, the ETD parameter was studied. A total of three ETD of 20 nm, 50 nm, and 90 nm were attained through tuning the a-Si RIE etching time. As lateral etching was inevitable, the ES parameter also played a part in the course of ETD engineering. SEM measurements (not shown here) indicated that ES decreased from 2.6 μm to 1.9 μm and then 1.3 μm with increasing ETD from 20 nm to 50 nm and then 90 nm, respectively. EA was fixed at 150°. A trend towards better resistive switching uniformity and data retention was observed. To avoid showing duplication, data collected from the device with 20 nm ETD is not shown here. The plot of cumulative probability versus resistance for two devices with different ETD is shown in Fig. 60. The occurrence probability of the extremely high resistance decreased from 16% to 0% by increasing ETD from 50 nm to 90 nm. The same argument can be used to explain the improvement of resistive

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switching uniformity as a result of the ES reduction. SEM images as shown in Fig. 61 support the argument. As shown in Fig. 62(b), no up-drifting trend was observed for both HRS and LRS resistance during the data retention test period. The degradation of the resistance as shown in Fig. 62(a) could be explained by the model proposed in Fig. 63. With thicker Ag electrode and electric field enhancement, more Ag atoms located in the deeper region could take part in the filaments formation process, which resulted in thicker filaments.

FIG. 60. The statistical distribution of the R_{HRS} and R_{LRS} for 200 DC sweep cycles for two devices with different ETD.

FIG. 61. SEM images of the distribution of the Ag filaments right after the cycling operation: (a) device with 50 nm ETD, and (b) device with 90 nm ETD.

FIG. 62. Data retention tests performed at room temperature for 1000 s: (a) device with 50 nm ETD, and (b) device with 90 nm ETD.

FIG. 63. The proposed model for the formation of stable filaments in the device (cross-sectional view) with deeper ETD.

To further check the device reliability performance, both the cycling endurance and the data retention tests were carried out at room temperature with more cycles and longer duration, respectively. As shown in Fig. 64, Fig. 65(a) and (b), both the cycling endurance and the data retention failures occurred earlier in the reference device with 90° EA, 1.3 μm ES, and 90 nm ETD. For the device with 672 nm ES, although the HRS and LRS resistance were drifting up, no set/reset failure was observed after 600 consecutive DC sweep cycles. Furthermore, no significant sign of the resistance degradation was observed after the 10⁵ s data retention test. The data retention test was also performed at an elevated temperature. The resistance states were maintained at 85 °C for 10⁵ s without any degradation as shown in Fig. 65(c).

FIG. 64. Endurance tests performed with more than 200 consecutive DC sweep cycles: (a) device with $1.3\mu\text{m}$ ES, and (b) device with 672 nm ES.

FIG. 65. Data retention tests performed at room temperature for more than 1000 s: (a) device with 1.3 μm ES, and (b) device with 672 nm ES. (c) For the device with 672nm ES, a further data retention test was conducted at elevated temperature for 10^5 s.

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With improved reliability, the multi-level cell operation was investigated in device with 90° EA, 672 nm ES, and 90 nm ETD as well. Three different LRS were achieved by varying the set compliance current (CC) from 5 mA to 1 mA, while the HRS were retained at $\sim 4\text{ K}\Omega$ by fixing the reset stop voltage to -1.5 V. The stable cycling endurance and data retention of the four-level cell are shown in Fig. 66(a) and (b), respectively.

FIG. 66. Multi-level cell operation: (a) cycling endurance, and (b) data retention.

5.4 Conclusion

In summary, the Ag-based RRAM device with planar double wedge-like electrodes was successfully fabricated and characterized for the first time. The device with small EA, narrow ES and deep ETD exhibited better resistive switching uniformity, cycling endurance, and data retention thanks to the electric field confinement and enhancement. Moreover, no trade-offs between the performance indices have been demonstrated during the electrode structure

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engineering process. It is believed that the 3-D electrode structure engineering method discussed in this work will pave the way for performance improvement of the filament-type RRAM devices.

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The thermal budget of the standard integrated circuits (IC) manufacturing process is one of the key considerations in the development of resistive random access memory (RRAM). To investigate the thermal budget effect on device performance, three types of HfO_x -based RRAM devices with different top electrodes are subjected to post-metallization annealing (PMA) at 400 °C for more than three hours. Electrical results show that the initial amount of oxygen vacancies in the HfO_x dielectric layer is strongly dependent on the electrode configuration. A device with the sandwich-like (TiN/Ti/TiN) top electrode exhibits better performance in thermal stability, forming, switching uniformity, and endurance when compared to other devices with a single layer (TiN) or bi-layer (TiN/Ti) top electrode. This is mainly due to the proper engineering of the oxidation reaction at the metal/metal oxide interface. We believe that this work provides a valuable guideline in the design and optimization of RRAM electrodes.

6.1 Introduction

RRAM as one type of emerging non-volatile memories has drawn much attention due to its simple device structure, low programming voltage, fast read/write speed, excellent scalability, and complementary metal oxide semiconductor (CMOS) back-end-of-line (BEOL) process compatibility [8, 30, 86]. To enable the high volume production of RRAM technology, it is important to meet the thermal budget requirement of the standard integrated circuits (IC) manufacturing process. In other words, not only the fabrication process of RRAM stacks but also the post-RRAM process should be carried out within 400 °C [141, 142]. There is a possibility of malfunction of RRAM devices owing to the process-induced thermal stress. The thermal stability from the thermal budget perspective should be taken into consideration at the design stage of

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RRAM devices. The post-metallization annealing (PMA) process can be implemented after the device fabrication to mimic the thermal effects of the post-RRAM process. It is meaningful to investigate the electrical performance of RRAM devices only after the thermal budget test. The accumulated duration of the post-RRAM thermal process including but not limited to chemical vapor deposition, rapid thermal annealing, furnace alloying [143], and polyimide curing [142] is typically more than one hour. However, to date, the duration of the thermal stability test reported has been less than or equal to one hour [144-149]. Thus, the device performance after several hours of annealing at 400 °C has yet to be studied. In this work, three types of RRAM devices with different top electrodes are subjected to PMA at 400 °C for more than three hours. The device performance is compared and analyzed. It is found that the device with sandwich-like (TiN/Ti/TiN) top electrode outperforms the others with higher thermal stability, lower forming voltage, more uniform switching, and better endurance owing to the proper engineering of the oxidation reaction at the metal/metal oxide interface. Experimental results show that the oxygen gettering ability of the Ti (active metal) layer is weakened by the insertion of an optimized TiN (inert metal) layer. The TiN/Ti/TiN tri-layer electrode has been reported by other works [150-152]. Nevertheless, the study on the thermal budget effect has not been conducted. Furthermore, the optimization of the bottom TiN thickness and the device performance at elevated temperature has not been discussed as well. Although our work is a case study, a sandwich-like electrode with inert/active/inert configuration could be considered for other metal oxide RRAM devices to fulfil the thermal budget requirement.

6.2 Experiment

The three types of RRAM devices with different top electrodes are named device A, device B, and device C. Their 3-D schematics are shown in the inset of [Fig. 68](#), [Fig. 72](#), and [Fig. 75](#), respectively.

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All devices are built on the SiO₂ passivated Si wafer with a Ti adhesion layer. The devices share the same bottom electrode (~50 nm Pt) and the dielectric layer (~6 nm HfO₂) which are formed by the DC magnetron sputtering at 25 °C and atomic layer deposition at 250 °C, respectively. The top electrode deposited by the same sputtering system is TiN/Ti (~60 nm/~8 nm), TiN (~60 nm), and TiN/Ti/TiN (~60 nm/~8 nm/~4 nm) for device A, device B, and device C, respectively. The circular pattern of the top electrode with a size of 100 μm is achieved by the i-line UV lithography and lift-off process. The devices are loaded into the center zone of the horizontal furnace which is filled with N₂ gas for the PMA process. Noted that the PMA process is performed on all devices at their pristine states. Fig. 67 shows the comparison of PMA conditions between this work and prior works. The electrical tests are conducted by the Keithley 4200 semiconductor characterization system and the voltage bias is applied to the top electrode while the bottom electrode is grounded. The depth profiling analysis is carried out by the AXIS Supra X-ray photoelectron spectroscopy (XPS).

FIG. 67. Comparison of PMA conditions between this work and prior works.

6.3 Results and Discussion

6.3.1 Dual-layer Top Electrode

To investigate the thermal budget effects on the device characteristics, electrical performance before and after the PMA process should be compared and analyzed. Device A with bi-layer (TiN/Ti) top electrode were studied first. Before the PMA process, a one-time DC forming operation with V_{form} of ~ 2.65 V was required to initialize the resistive switching as shown in Fig. 68. The 10 μA compliance current (CC) was used for all the devices during the forming process to avoid the hard breakdown. All the forming voltages were extracted at the point where the current first reached the compliance level.

FIG. 68. DC forming curve of device A before the PMA (CC=10 μA). The inset shows the 3-D schematics of device A.

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It is well known that a thin reactive Ti buffer layer inserted in between the TiN layer and HfO₂ layer can improve the device performance due to the oxygen gettering effect [21, 153, 154]. However, the DC endurance test as shown in Fig. 69(a) indicated the degradation of the resistance window due to decreased resistance of the high resistance state (HRS) and increased resistance of the low resistance state (LRS). A 0.1 V DC bias was applied to read the resistance. According to a prior study [66], the endurance degradation was caused by the set process-induced interfacial oxidation reaction between the electrode and dielectric layer. In this case, the oxygen ions from the HfO₂ layer migrated into the Ti layer under the electric field and a TiO_x interfacial layer (IL) was formed due to current-induced Joule heating [155]. With continuous cycling, the interfacial region gradually grew, and when it became resistive enough, it served as a roadblock for the movement of the oxygen ions during both the set and reset process. Fig. 69(b) shows the corresponding *I-V* curves of the first and the last DC sweep cycles. It is obvious that the surge current of the 40th DC set was limited by the IL which introduced itself as a series resistor [83] and the magnitude of the reset voltage of the 40th DC reset is larger than that of the 1st DC reset due to the voltage drop induced by the series resistance. Since the process of endurance failure was gradual when compared to the abrupt set/reset failure [67], a high CC (5 mA) was used during the set process to accelerate the Joule heating effect and degrade the device performance at a faster pace.

FIG. 69. (a) DC cycling endurance test with 5 mA set CC before the PMA. (b) The corresponding *I-V* curves of the first and the last DC sweep cycles (set CC=5 mA).

To tackle the shrinkage of the resistance window, the set CC was reduced to 3 mA and the reset stop voltage (SV) (-1.5 V) remained unchanged. As shown in Fig. 70(a) and (b), the stable DC endurance was acquired owing to the reduction of the Joule heating and the reduced amount of oxygen ions involved in the set operation. A similar phenomenon as shown in Fig. 71(a) was observed for the pulse endurance test. Instead of using a short pulse, a rectangular pulse with a 5 ms long pulse width was used to expedite the interfacial oxidation reaction. Three more samples were tested under the same pulse conditions to confirm the endurance failure mode. As shown in Fig. 71(c), the box plots of initial and final R_{HRS} contain the first and the last 25 consecutive data points which were extracted from 250 pulse endurance cycles, respectively. The same method was used to generate the box plots of initial and final R_{LRS} . Consistently, the reduction of the resistance window is observed for all samples, and the same failure mode is indicated by the dotted lines. By

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comparing the pulse endurance as shown in Fig. 71(a) and (b), the degradation of the resistance window was retarded if a set pulse with a smaller voltage amplitude (1 V) was applied. It is worth noting that the reduction of set CC and set pulse height would lead to an increase in R_{LRS} . Thus, there is a trade-off between the endurance and resistance window.

FIG. 70. (a) DC cycling endurance test with 3 mA set CC before the PMA. (b) The corresponding I - V curves of the first and the last DC sweep cycles (set CC=3 mA).

(a)

(b)

(c)

FIG. 71. (a) Pulse endurance test with 1.2 V pulse height before the PMA. (b) Pulse endurance test with 1 V pulse height before the PMA. (c) Box plots of initial and final resistance (R_{HRS} and R_{LRS}) of three more samples before the PMA.

6.3.2 Single-layer Top Electrode

After the PMA process, device A failed to switch due to a high leakage current. The short failure was attributed to the strong oxygen scavenging ability of Ti under the high-temperature condition. Thus, device B without the Ti buffer layer was investigated to validate the concept. Noted that an IL of TiON can be formed at the TiN/HfO₂ interface due to the oxygen scavenging ability of TiN [111, 156]. When compared to the V_{form} of device A, a higher V_{form} of ~ 3.35 V as shown in Fig. 72 (red line) implies that the oxygen reactivity of TiN is much weaker than that of Ti. Hence, device B has fewer oxygen vacancies in the HfO_x dielectric layer. It is worth pointing out that device B survived the PMA process and the V_{form} of the annealed device is ~ 2.55 V as shown in Fig. 72 (blue line). The reduced forming voltage suggests the further generation of oxygen vacancies under the heat treatment, and the annealing-induced IL (TiON) leads to the smooth rising of current due to the self-compliance effect.

FIG. 72. DC forming curve of device B before and after the PMA (CC=10 μ A). The inset shows the 3-D schematics of device B.

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The pulse endurance tests conducted before and after the PMA process are shown in Fig. 73(a) and (b), respectively. The fluctuation of the R_{HRS} and R_{LRS} suggests that the switching uniformity of device B is much worse than that of device A. Since the switching variability is strongly dependent on the chemical activity of the metal electrode [157] and the number of defects generated in the dielectric [80], the abrupt change of the HRS is more likely to be observed in device B with the inert TiN electrode when compared to other types of devices with reactive Ti buffer layer. The intermittent and sudden change of the HRS was further verified by performing the DC reset process with -2 V reset SV as shown in Fig. 73(c). The quick drop of the current (blue curve) was observed when the voltage almost reached the reset SV. On the other hand, the device with the PMA process exhibits a much slower window degradation rate when compared to that of the device without the PMA process. Again, three more samples after the PMA process were tested up to 1000 cycles with the same pulse scheme to verify the resistive switching characteristics. The box plots as shown in Fig. 73(d) were produced by using the same approach mentioned earlier. A larger variation of the resistance and less significant window degradation were noticed when compared to the data shown in Fig. 71(c).

FIG. 73. (a) Pulse endurance before the PMA process. (b) Pulse endurance after the PMA process. (c) I - V curves of gradual and abrupt DC reset after the PMA process. (d) Box plots of initial and final resistance (R_{HRS} and R_{LRS}) of three more samples after the PMA.

A model as shown in Fig. 74 is proposed to describe the difference in the formation of ILs in both unannealed and annealed devices. For the unannealed device, the initial IL is mainly induced by

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switching and it is localized based on the generic filaments model [158]. During the cycling, the diffusion and drift of the oxygen ions can result in the fast growth of localized IL especially in the lateral directions indicated by the thick arrows. However, for the annealed device, the initial IL is induced by annealing and it is uniform as heat is evenly distributed across the interface. The growth of the switching-induced IL is self-retarded in both vertical and lateral directions due to the barrier effect of the preformed IL. Thus, the annealing-induced IL could slow down the degradation of the resistance window.

FIG. 74. The proposed model describes the difference in the formation of ILs in both unannealed and annealed devices. The arrows indicate the growth direction and growth rate of the ILs.

6.3.3 Tri-layer Top Electrode

To achieve both thermal stability and switching uniformity, device C with a sandwich-like (TiN/Ti/TiN) top electrode was designed. Prior reports have demonstrated the improvements in resistance window [150], switching uniformity [152], and power consumption [151] of RRAM devices with a tri-layer (TiN/Ti/TiN) electrode. The motivation of this work is to enhance the thermal stability of the HfO_x-based RRAM device without trade-offs in switching uniformity and

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endurance. We conducted three split runs to optimize the thickness of the bottom TiN layer. We found that if the thickness was too thin (~ 2 nm), the device was not able to withstand the thermal budget (400°C , 3 hrs) and the same short failure occurred. On the contrary, if the thickness was too thick (~ 8 nm), although the device survived from the thermal test, it was prone to hard breakdown ($V_{\text{breakdown}} > 4$ V) possibly due to the formation of dense and thick TiON IL. The optimized thickness was about 4 nm and the DC forming curves of unannealed and annealed devices are shown in Fig. 75. The V_{form} (~ 3.20 V) of device C before PMA is closed to that (~ 3.35 V) of unannealed device B, which suggests the dominance of TiN at the metal/metal oxide interface. The V_{form} (~ 1.15 V) of device C after PMA is smaller than that (~ 2.55 V) of annealed device B, which implies that both Ti and bottom TiN layers took part in the oxygen gettering process.

FIG. 75. DC forming curve of device C before and after the PMA (CC=10 μA). The inset shows the 3-D schematics of device C.

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The XPS analysis was conducted for both unannealed and annealed devices and the oxygen (O 1s) and hafnium (Hf 4f) depth profiles are shown in Fig. 76. The lightly shaded rectangle marks the region of Ti. The diffusion of hafnium atoms under PMA is unnoticeable since the two profiles are well-overlapped. We confirmed the diffusion of oxygen atoms under PMA based on the increased oxygen concentration in the Ti layer. The high leakage current of the annealed device was caused by the reduced oxygen concentration in the HfO_x layer. With proper engineering of the interfacial oxidation reaction, device C survived from the thermal annealing and obtained a much lower forming voltage, which was beneficial to the design of the CMOS circuit. Since the oxygen gettering ability of Ti is a function of thickness, and the required thickness of the bottom TiN layer is proportional to the Ti layer thickness, a thicker Ti layer is not preferred from the thermal budget point of view.

FIG. 76. XPS depth profiling analysis for both unannealed and annealed devices.

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Furthermore, the switching uniformity and endurance of annealed device C were examined by performing the DC and pulse cycling. As shown in Fig. 77(a), good switching uniformity was maintained with 200 consecutive DC sweeps (set CC=3 mA) owing to the TiO_x oxygen exchange layer and there was no significant degradation of the resistance window due to the annealing-induced ILs (TiO_x/TiON). Likewise, the stable pulse endurance as shown in Fig. 77(b) lasted for 1000 cycles. Once again, three more samples were tested up to 1000 cycles to substantiate the device performance. As shown in Fig. 78(c), it is obvious that all samples exhibit better switching uniformity and endurance when compared to that of device A and B. For practical application, an endurance test with a short pulse width is required. Thus, the pulse width was reduced to 200 ns and the pulse heights were unchanged. As shown in Fig. 77(d), we achieved 5×10^5 pulse cycles without endurance failure.

FIG. 77. (a) DC endurance test with 3 mA set CC after the PMA. (b) Pulse endurance test with 5 ms pulse width after the PMA process. (c) Box plots of initial and final resistance (R_{HRS} and R_{LRS}) of three more samples after the PMA. (d) Pulse endurance test with 200 ns pulse width after the PMA process.

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The data retention was studied by conducting the temperature accelerated failure test. Before that, we checked the stability of the HRS and LRS at the elevated temperature. Fig. 78(a) shows the variations of the R_{HRS} and R_{LRS} values with time under the constant read (0.1 V) bias. Since the HRS is more susceptible to the read disturb at 300 °C, the retention of the HRS is of high priority. The HRS retention failure time is defined as the time when the R_{HRS} value decreases to 50% of its starting value. Fig. 78(b) shows the Arrhenius plot with failure time collected at three different temperatures. The activation energy was calculated to be ~1.72 eV and the extrapolated HRS retention time is more than 10 years at 85 °C. The I - V curves at different temperatures are shown in Fig. 78(c). The resistive switching (set CC=3 mA) is insensitive to the variation of temperature since the deviations of the R_{HRS} and R_{LRS} values are insignificant. The good thermal stability could be attributed to the high oxygen vacancy formation energy of the crystallized HfO_2 [159] after the PMA process [160].

(a)

(b)

(c)

FIG. 78. (a) Variations of the R_{HRS} and R_{LRS} values with time under the constant read bias (0.1 V) at 300 °C after the PMA. (b) Arrhenius plot of the HRS retention failure time after the PMA. (c) I - V curves measured at different temperatures after the PMA (set CC=3 mA).

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With the stable resistive switching, the multi-bit operation at room temperature was further investigated. As shown in Fig. 79, a total of five distinguishable resistance states were obtained through tuning the set CC. State 5 is the HRS and state 4 to state 1 are LRS with set CC at 0.6 mA, 1 mA, 2 mA, and 3 mA, respectively. It is noteworthy that there is no discernable window degradation for both the DC endurance (Fig. 79(a)) and data retention (Fig. 79(b)) tests.

FIG. 79. Multi-bit operation at room temperature after the PMA. State 5 is the HRS whereas state 4 to state 1 are LRS achieved with set CC of 0.6 mA, 1 mA, 2 mA, and 3 mA, respectively. (a) Multi-level DC endurance test. (b) Multi-level data retention test.

6.4 Conclusion

The influence of the thermal budget on HfO_x-based RRAM devices has been investigated. The PMA process was implemented to simulate the overall thermal effect. We demonstrated that the device with sandwich-like (TiN/Ti/TiN) top electrode exhibited high thermal stability, low

Chapter 6 Sandwich-like Electrode for Thermal Budget Requirement

forming voltage, uniform switching, and stable endurance. Each layer of the top electrode plays a significant role in the engineering of the interfacial oxidation reaction. The bottom TiN layer serves as an oxygen diffusion barrier during the annealing process to improve the thermal stability, the middle Ti layer acts as an oxygen exchange layer during the switching process to enhance the switching uniformity, and the top TiN layer behaves as a capping layer to prevent oxidation of the middle Ti layer. We believe that this work provides a valuable guideline in the design and optimization of RRAM electrodes.

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The effects of the oxygen plasma treatment (OPT) on the TiN bottom electrode (BE) of the resistive random access memory (RRAM) devices are investigated. Experimental results show that the switching uniformity and resistance window are improved via the BE passivation process. However, the DC forming voltage increases with the processing time. RRAM devices with moderate treatment are integrated with thin film transistors (TFT) to test the functionalities of the 64-bit one-transistor-one-resistor (1T1R) array. The TFT is capable of serving as a current limiter during the operation of the memory device. Further optimizations of both TFT and RRAM devices are required to make their performance compatible.

7.1 Part 1: Passivation of TiN Electrode for Switching Uniformity Improvement

7.1.1 Introduction

It is well known that noble metals such as Pt, Au, Ir, and Ru are quite costly and hard to etch for the semiconductor industry. Nevertheless, these materials are widely used to form the electrodes of RRAM devices due to chemical inertness [161]. The highest ever reported endurance (10^{12} cycles) has been achieved by using the TaO_x-based RRAM device with Pt electrodes [162]. In our previous work (Chapter 6), uniform resistive switching has been demonstrated by engineering the Pt/HfO_x/TiN/Ti/TiN RRAM device. To study the electrode effects on device performance, Pt BE was replaced by TiN which is a conventional fab material in complementary metal oxide semiconductor (CMOS) back-end-of-line (BEOL) interconnects. The schematic of the cross-sectional view of the device with TiN BE is shown in [Fig. 80](#).

FIG. 80. Schematic of the cross-sectional view of the RRAM device with TiN BE.

7.1.2 Results and Discussion

For simplicity, the Pt/HfO_x/TiN/Ti/TiN and TiN/HfO_x/TiN/Ti/TiN RRAM cells are named device A and B, respectively. The fabrication process of device B is almost the same as device A except for the sputtering of the bottom TiN (~50 nm). The DC forming curves of both devices are shown in [Fig. 81](#). The compliance current (CC) was set to 0.5 mA.

FIG. 81. DC forming curves of both devices (CC=0.5 mA).

The forming voltage of device A is ~1.22 V which is close to the value of ~1.15 V described in Chapter 6. The forming voltage (~1.61 V) of device B is higher than that of device A possibly due to the formation of a TiON layer at the bottom TiN/HfO₂ interface. The switching uniformity of device B was much worse than that of device A based on the DC cycling results as shown in Fig. 82. The set CC was 3 mA and the reset stop voltage (SV) was -1.5 V for both endurance tests. The calculated coefficient of variation (σ/μ) of device B was nearly triple that of device A for both high and low resistance states (HRS/LRS). The degradation of the switching uniformity could be caused by the generation of distributed filaments. A model was introduced in the below section to illustrate the distribution of filaments in different types of devices.

FIG. 82. DC endurance with 3 mA set CC and -1.5 V reset SV: (a) device A; (b) device B.

To tackle the problem of unstable switching, a surface oxidation process was proposed. OPT was utilized to passivate the surface of TiN BE before the deposition of HfO₂. The TiON passivation layer (PL) needs to be oxygen-rich to minimize the generation of oxygen vacancies at the TiON/HfO₂ interface. The schematic cross-sectional view of the device with OPT is shown in Fig. 83. Again, this device is named device C for ease of description.

FIG. 83. Schematic of the cross-sectional view of the RRAM device with OPT.

The effects of OPT with the duration of 75 s, power of 800 W, and O₂ flow rate of 800 ml/min was examined first. It was found that the device was prone to hard breakdown due to the thickening of the switching dielectrics (TiON/HfO₂). As shown in Fig. 84(a) blue curve, device C failed to form (remained at pristine state) when the CC was 10 μ A. With a slight increase of the CC to 20 μ A (red curve), the hard breakdown occurred. Since the CC was quite low, the abrupt transition of the current was not observed. Noted that the thickness of HfO₂ of device C is ~6 nm which is the same as that of device A and B. To solve the problem of forming, device C with two different HfO₂ thicknesses were fabricated. As shown in Fig. 84(b), device C with ~4 nm HfO₂ was not able to survive the thermal budget test (400 °C, 3 hrs). The device behaved as a resistor and it was too conductive to switch. The successful initialization process with a forming voltage of ~2.64 V was demonstrated for device C with ~5 nm HfO₂ as shown in Fig. 84(c). The typical *I-V* characteristics of bipolar resistive switching of device C with ~5 nm HfO₂ is shown in Fig. 84(d). The smooth set curve was attributed to the current limiting effect of the PL.

FIG. 84. (a) *I-V* curves of failed DC forming of device C with 6 nm HfO₂. (b) *I-V* curves of failed resistive switching of device C with 4 nm HfO₂. (c) *I-V* curve of successful DC forming of device C with 5 nm HfO₂. (d) *I-V* curves of successful resistive switching of device C with 5 nm HfO₂.

The same set CC (3 mA) and reset SV (-1.5 V) were applied to conduct the endurance test as shown in Fig. 85(c). Good switching uniformity with coefficients of variation of 0.045 (HRS) and

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0.033 (LRS) was achieved. To further study the effects of OPT, four more devices with different durations of treatment were produced. Noted that the thickness of HfO_2 was kept at ~ 5 nm for all the engineering splits. As shown in Fig. 85(a)-(e), the switching uniformity of all devices was much better than that of device B thanks to the passivation of TiN BE. The coefficients of variation of both HRS and LRS were calculated as shown in Fig. 85(f). The σ/μ (HRS) of device C decreases with increasing duration and it starts to saturate when the duration is 75 s. The σ/μ (LRS) of device C seems to be insensitive to the variation of the duration.

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FIG. 85. (a)-(e) DC cycling of device C with different durations of OPT. (f) The calculated coefficients of variation of both HRS and LRS. The σ/μ of device B was plotted at 0 s.

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A model as shown in Fig. 86 was proposed to describe the distribution of the filaments in different types of devices. For device B without OPT, the oxygen vacancies were induced by the oxidation reaction between the TiN BE and HfO_2 switching layer and they were evenly distributed across the bottom interface. During the DC cycling, the oxygen vacancies facilitated the growth of the main filaments as well as the stray filaments. As the variation on the geometry of the stray filaments would also affect the conduction of the current, the overall switching uniformity degraded. For device C with OPT, the generation of the oxygen vacancies at both TiON/ HfO_2 and TiN/TiON interfaces was minimized since the PL contained a rich amount of oxygen. The element analysis of three samples with different durations (10 s, 75 s, and 300 s) of OPT was conducted by the AXIS Supra X-ray photoelectron spectroscopy (XPS) for validation. As shown in Table IV below, the oxygen content increases with the duration and the element ratio between the oxygen and titanium is more than 2 for all the devices. Since fewer defects were created at the bottom interfaces, the distribution of the filaments in device C was localized. Thus, the improvement of switching uniformity was attributed to the formation of the confined filaments.

FIG. 86. The proposed model describes the distribution of filaments in different types of devices.

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Besides the switching uniformity, it was found that the R_{LRS} did not vary with the duration, whereas the R_{HRS} increased with the duration. The correlation between the resistance window and duration of OPT is shown in Fig. 87(a). The enlargement of the resistance window was caused by the increase of the resistivity of the TiON film. It is worth pointing out that the DC forming voltage also increases with the duration as shown in Fig. 87(b). Hence, a trade-off between the forming voltage and the other two performance indices (resistance window and switching uniformity) needs to be taken into consideration when tuning the duration of OPT. The thickness of the PL of three samples with different durations (10 s, 75 s, and 300 s) of OPT was measured by the Bruker D8 Discover X-ray reflectometry (XRR). As shown in Table IV below, the thickness of TiON increases with the duration, which leads to an increase in the forming voltage.

FIG. 87. (a) The correlation between the resistance window and duration of OPT. (b) The correlation between the DC forming voltage and duration of OPT.

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Table IV summarizes the coefficient of variation, resistance window, and forming voltage of all types of devices. The stoichiometry and thickness of the PL of device C were compiled as well. The pronounced enhancement of the switching uniformity was achieved by using the OPT technique. Noble metals can be replaced by conventional fab materials without scarifying the switching stability. Precise tuning of the thickness of the TiON/HfO₂ bilayer is required to further lower the forming voltage.

BE	σ/μ (HRS)	σ/μ (LRS)	Resistance window	Forming voltage (V)	Stoichiometry of PL	Thickness of PL (nm)
Pt	0.084	0.027	11.71	1.15		
TiN	0.247	0.094	4.31	1.61		
TiN (10 s)	0.083	0.031	4.38	2.30	TiO _{2.16} N _{0.23}	4.57
TiN (40 s)	0.072	0.035	5.75	2.52		
TiN (75 s)	0.045	0.033	8.91	2.64		5.28
TiN (150 s)	0.044	0.036	10.20	3.10	TiO _{2.29} N _{0.19}	
TiN (300 s)	0.042	0.037	12.95	3.41		6.85

TABLE IV. Summary of the coefficient of variation, resistance window, and forming voltage of all types of devices. The stoichiometry and thickness of the PL of device C were compiled as well.

Chapter 7 Integration of 1T1R Array

7.2 Part 2: Integration of the 64-bit 1T1R Array

7.2.1 Introduction

For large-area electronics (LAE) application, indium-gallium-zinc-oxide (IGZO) thin film transistor (TFT) has drawn much attention owing to its low cost, high field-effect mobility, good uniformity for large area deposition, and low process temperature [163-165]. In addition, the non-volatile memory is another key element that can be embedded in the LAE circuits for power reduction [166]. Resistive random access memory (RRAM) can be easily integrated with TFT to form the one-transistor-one-resistor (1T1R) architecture due to its non-volatility, simple structure, low operation voltage, and low process temperature [8]. From the image display perspective, TFT as an access transistor passes the image information in the form of electrical bias or current and triggers the data storage by changing the resistance state of the RRAM device. TFT also plays a role in suppressing the current overshoot and stabilizing the operation of the RRAM device. The 5x5 1T1R pixel array with indium-zinc-oxide (IZO) TFT and HfO₂ RRAM has been demonstrated on a sapphire substrate [167]. Here, as shown in [Fig. 88](#), a 64-bit 1T1R array with eight horizontal word/source lines and eight vertical bit lines has been successfully fabricated on the silicon substrate as a proof of concept.

FIG. 88. Photo of a 64-bit 1T1R array sample.

[Fig. 89\(a\)](#) shows the optical image of four adjacent bit cells within the 64-bit 1T1R array. The word lines connected the gate of the TFTs, and they were parallel to the source lines. The RRAM cells were built on top of the drain, and the top electrodes (TE) were connected by the bit lines which were orthogonal to the word lines. Each RRAM cell was controlled by an individual TFT. To have a zoomed-in view of the single bit cell, an optical image as shown in [Fig. 89\(b\)](#) was taken. The RRAM cell was formed inside the square via with a size of 50 μm . The via hole is fully covered by the TE with a size of 100 μm . The channel length (L) and width (W) of the TFT are 20 μm and 600 μm , respectively.

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(a)

(b)

FIG. 89. (a) Optical image of four adjacent bit cells within the 64-bit 1T1R array. (b) Optical image of a single bit cell within the 64-bit 1T1R array.

7.2.2 Fabrication Process of 64-bit 1T1R Array

The main fabrication process and the corresponding cross-sectional schematics of the 64-bit 1T1R array are shown in Fig. 90. Noted that the schematics were drawn based on the “cut” along the AA’ dotted line as shown in Fig. 89(a). The bottom-gate-top-contact (BGTC) TFT was constructed first.

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The word lines which consist of Ti/Al/TiN were deposited by sputtering and patterned by a lift-off process. The Ti (~10 nm) layer was utilized to improve the adhesion between the Al and SiO₂. Due to the relatively high resistivity of TiN (~50 nm), the Al layer (~120 nm) was inserted to reduce the IR drop across the word lines. From the device point of view, the word line also functions as the gate of the TFT. The Al₂O₃ (~40 nm) gate dielectric was conformally formed by atomic layer deposition (ALD) at 250 °C. The IGZO (~50 nm) semiconductor channel, TiN (~50 nm) source/drain, and Ti/Al (~10 nm/~120 nm) source lines were sputtered and patterned (lift-off) in sequence. A 100-nm-thick SiO₂ isolation layer was formed by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C. It is noteworthy that the topology of the SiO₂ layer in the source and gate regions is not shown in the cross-sectional view. The vias were opened on the drain side by reactive ion etching (RIE) process. The exposed surface of TiN was passivated by OPT with a duration of 75 s. The HfO₂ (~5 nm) switching layer was deposited by the same ALD tool with different precursors. The TiN/Ti/TiN (~4nm/~8 nm/~60 nm) TE of the RRAM cells were sputtered and dry-etched. The measurement of the etch step height (77 nm) indicates the full removal of the HfO₂. To obtain a clean interface between the TE and HfO₂, lift-off method was not used to pattern the TE. The Ti/Al (~10 nm/~120 nm) bit lines were sputtered and patterned (lift-off). The contacts to the word and source lines were opened by the RIE process. As the contacts were located at the periphery of the array, the cross-section was not shown here to avoid confusion. At last, the sample was annealed in the furnace filled with N₂ gas at 400 °C for 3 hrs.

Ti/Al/TiN deposition and lift-off (Word line)

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Al₂O₃ deposition (TFT gate dielectric)

IGZO deposition and lift-off (TFT channel)

TiN deposition and lift-off (TFT source/drain)

Ti/Al deposition and lift-off (Source line)

SiO₂ deposition (Isolation)

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SiO_2 etch (RRAM Via)

O_2 plasma treatment (RRAM BE passivation)

HfO_2 deposition (RRAM switching layer)

TiN/Ti/TiN deposition and etch (RRAM TE)

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FIG. 90. Schematic of the cross-sectional view of the 1T1R after each process step. The cross-section was drawn based on the “cut” along the AA’ dotted line as shown in Fig. 88(a).

7.2.3 Results and Discussion

The electrical performance of a single TFT device was examined first. The output curves of the TFT at different gate bias (V_{GS}) are shown in Fig. 91(a). When the V_{GS} is 10 V and V_{DS} (drain bias) is 3 V, the current is about 0.5 mA. The DC forming of the 1T1R was carried out by applying a DC bias of 10 V to the word line and a voltage sweep (0 V→3 V) to the bit line. As shown in Fig. 91(b), the sudden increase of the current was observed at ~2.92 V which was slightly higher than the forming voltage (~2.64 V) of a single RRAM device due to the IR drop across the TFT. As the current was controlled by the TFT, it also served as a current limiter to prevent electrical damage to the RRAM device. The DC set and reset operations of the 1T1R as shown in Fig. 91(c) were conducted similarly. Likewise, the magnitudes of the DC set and reset voltages were increased owing to the voltage drop across the TFT. Fig. 91(d) shows the DC cycling of the 1T1R. The R_{HRS} and R_{LRS} were separated by a resistance window of 1.7. Although the resistance window can be improved by increasing the gate bias, for low-power applications, further engineering of both devices (TFT and RRAM) is essential.

FIG. 91. (a) The output curves of the TFT at different V_{GS} . (b) I - V curve of forming of 1T1R. (c) I - V curves of bipolar resistive switching of 1T1R. (d) DC cycling of 1T1R.

7.3 Conclusion

The OPT method has been implemented to solve the issue of resistive switching variation after replacing the Pt BE with TiN. Due to the OPT-induced TiON interfacial layer, the confined filament could be formed at the expense of increased forming voltage. The resistance window can be improved with a long treatment time without affecting the switching uniformity. RRAM cells with moderate OPT have been successfully integrated with TFTs at the mini array level to demonstrate the possibility of practical application in the field of LAE.

Chapter 8 Conclusion and Recommendations

With the high demand for data storage, resistive random access memory (RRAM) remains a hot topic in research and development. Major roadblocks such as high forming voltage, poor reliability, low thermal stability, unstable resistive switching, and materials incompatibility have to be overcome to achieve the mass production of RRAM devices in semiconductor foundries. In this thesis, various techniques include the optimization of electrical parameters, design of signals, modification of the device structure, and engineering of interfaces have been implemented to address the above challenges. Despite that, the RRAM device equipped with all the ideal characteristics has not been found. Further improvements on the device performance are still required.

8.1 Conclusion

The research works carried out in this thesis are summarized in the following:

In Chapter 3, two important DC operation parameters namely set compliance current (CC) and reset stop voltage (SV) are examined. To achieve stable resistive switching, the optimal ranges of the DC operation parameters are determined based on the observation of the I - V characteristics. The five-level operation is obtained by tuning the set CC. The up drifting of the high resistance state (HRS) that occurred at low set CC (0.5 mA) is resolved by adjusting the reset SV from -2 V to -1.8 V.

In Chapter 4, the electrical noise signal triggered resistive switching is explored. Although noise is often undesirable, the voltage amplitude of the noise signal which triggers the forming is much lower than the unipolar pulse height owing to the facilitation effect of the negative voltage. As a

Chapter 8 Conclusion and Recommendations

result, a novel bipolar pulse writing scheme is proposed to reduce the forming voltage and variability. Experimental data shows that the average and standard deviation of the pulse heights are reduced by more than 30% and 50%, respectively. Conversely, the inhibition effect of the negative voltage is demonstrated for the set process due to the increase of leakage current.

In Chapter 5, a novel device structure with the double wedge-like electrodes is fabricated. The effects of electrode angle (EA), electrode spacing (ES), and electrode trench depth (ETD) on the device performance are studied. Good switching uniformity and reliability have been demonstrated in device with 90° EA, 440 nm ES, and 90 nm ETD owing to the electric field confinement and enhancement.

In Chapter 6, the effects of the thermal budget on device performance have been investigated. A device with the sandwich-like (TiN/Ti/TiN) top electrode is engineered to achieve good performance in thermal stability, forming, switching uniformity, and endurance. Each layer of the top electrode plays a significant role in the engineering of the interfacial oxidation reaction.

In Chapter 7, the effects of the oxygen plasma treatment (OPT) on the TiN bottom electrode (BE) are discussed. The switching uniformity and resistance window are improved via the BE passivation process. RRAM devices with moderate treatment are integrated with thin film transistors (TFT) to form a 64-bit one-transistor-one-resistor (1T1R) array, and the basic functions have been successfully demonstrated.

8.2 Recommendations

To further improve the device performance, the following future works are recommended:

Chapter 8 Conclusion and Recommendations

In this thesis, multi-bit storage is achieved via the DC operation. For practical applications, pulse signals are used for programming and erasing. It is worth exploring the multi-level cell (MLC) operation by engineering the pulse signals.

It is suspected that the negative pulse (2nd half of the bipolar pulse) described in Chapter 4 could solve the problem of current overshoot during the forming/set process since the negative charges can neutralize the excess positive charges. Engineering splits with various pulse widths can be set up to validate the above hypothesis.

To further confine the distribution of filaments, the electrode angle (EA) and electrode spacing (ES) discussed in Chapter 5 can be scaled by using a lithography process (e.g., electron-beam lithography) with high resolution. From the material perspective, Cu as a conventional fab material can replace Ag. To reduce the cell size, a device with vertical wedge-like electrodes could be a solution.

PUBLICATIONS

US Patents:

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1. **J. Sun**, Y. B. Li, Y. Ye, J. Zhang, G. Y. Chong, J. B. Tan, Z. Liu and T. Chen, "3-D Geometric Engineering of the Double Wedge-like Electrodes for Filament-type RRAM Device Performance Improvement," IEEE Access, vol. 8, pp. 4924-4934, 2019. DOI: 10.1109/ACCESS.2019.29628692.

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