Study of the effect of forward gate bias stress on the reliability of AlGa_N/Ga_N HEMTs on Si

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**STUDY OF THE EFFECT OF FORWARD GATE BIAS STRESS
ON THE RELIABILITY OF ALGAN/GAN HEMTS ON SI**

GAO YU

SCHOOL OF MATERIALS SCIENCE AND ENGINEERING

2020

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ON THE RELIABILITY OF ALGAN/GAN HEMTS ON SI**

GAO YU

SCHOOL OF MATERIALS SCIENCE AND ENGINEERING

A thesis submitted to the Nanyang Technological University
in partial fulfilment of the requirement for the degree of
Doctor of Philosophy

2020

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

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30 July 2020

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Date

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Prof Gan Chee Lip

Authorship Attribution Statement

This thesis contains material from one paper published in the following peer-reviewed journal in which I am listed as an author.

Part of the chapter 5 and chapter 6 is published as Gao, Y., Sasangka, W. A., Thompson, C. V., and Gan, C. L. (2019). Effects of forward gate bias stressing on the leakage current of AlGaIn/GaN high electron mobility transistors. *Microelectronics Reliability*, 100, 113432.

The contributions of the co-authors are as follows:

- Prof Gan and Prof Thompson provided the initial project direction and edited the manuscript drafts.
- I prepared the manuscript drafts. The manuscript was revised by Dr. Sasangka.
- I co-designed the study with Dr. Sasangka and performed all the laboratory work at the School of Materials Science and Engineering. I also analyzed the data.
- All the TEM was conducted by me in the Facility for Analysis Characterisation, Testing and Simulation.

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Abstract

AlGaIn/GaN high electron mobility transistors (HEMTs) have shown promising capabilities for high frequency and high-power applications. As 5G technology and autonomous vehicles become more and more attractive, HEMTs will start to play an increasingly important role in the semiconductor industry. While GaN HEMTs are most commonly fabricated on SiC or sapphire substrates, HEMTs on Si is an attractive alternative due to lower processing costs and the ability for monolithic integration with Si-CMOS (Complementary Metal Oxide Semiconductor). However, the wide-scale adoption of GaN HEMTs on Si is still limited by reliability issues because of the greater difference in the coefficients of thermal expansion and higher dislocation densities compared conventional substrates. Previous studies of the reliability of GaN HEMTs on Si have mainly focused on degradation of the drain saturation current, while the origin of gate leakage current degradation has remained poorly understood.

In this dissertation, degradation under forward gate bias stressing was investigated. After stressing, the gate leakage current increased dramatically without much degradation on the drain saturation current. As high leakage current could lead to high power consumption and high noise, it is important and necessary to understand why the leakage current increases during stressing.

First, the current transport mechanisms of fresh devices were studied. Both electrical measurements and simulations were carried out to investigate the electron transport mechanisms, especially in the reverse bias region. It was found that the leakage current for fresh devices was mainly dominated by Fowler-Nordheim tunneling at room temperature.

The devices were then subjected to forward gate bias stressing and the failure criterion was set as the time at which the leakage current reached 1 μA . The degradation was highly accelerated by the stressing voltage. The degradation mainly took place at the Schottky contact, with the barrier height reduced and ideality factor increased over the stressing time.

By further analyzing transport mechanism for stressed devices, it was found that the leakage current was dominated by Poole-Frenkel emission.

Finally, the degraded devices were examined using different material characterization techniques. The stressed devices showed a highly localized leakage path as detected from photon emission microscopy. Transmission electron microscopy was utilized to investigate structural changes at the high leakage path region. From electron energy loss spectroscopy analysis, a localized high carbon region was found in the gate metal. As carbon has a lower work function than the gate metal, and this is likely to cause of a reduction of the barrier height. The carbon is suspected to come from photoresist residue during the metal lift-off process. During electrical stressing, the electrical field is sufficiently high to trigger carbonization at the gate. Then the carbonized carbon residue lowers the barrier height leading to the high leakage path. Furthermore, as the tested devices are Ga-polar device, the carbon residues might also create C_{Ga} or C_{Al} defects and enhance Poole-Frenkel emission after stressing.

In summary, high leakage currents were observed after forward gate bias stressing. It was found that carbon residue from photoresist was the main reason leading to the degradation. Thus, this carbon residue is detrimental for device reliability. In order to improve device reliability, a clean surface between the gate metal and semiconductor is essential. This methods developed in this dissertation provide an integrated experimental approach to investigate AlGaIn/GaN HEMT device reliability, especially for gate leakage failure. By combining electrical characterization, physical characterization and computer-aided simulation, this approach provides a comprehensive understanding of the failure mechanism for improved device reliability.

Lay Summary

A semiconductor device, just like a human body, will fail at some point in time after continuous operation due to degradation of its functional and material properties. The study on the reliability of semiconductor devices is to investigate and understand how a device will degrade over time and the reasons behind it. With this understanding, engineers can define a safe operating condition within the targeted lifetime of the device or improve on the design or processes to develop a more robust device. In order to shorten the time taken for reliability study, devices are normally stressed at accelerated conditions such as higher voltage, current, and temperature than the recommended working conditions.

In this dissertation, the reliability of high electron mobility transistors (HEMTs) is investigated. The HEMTs are mainly made of AlGa_N and Ga_N, and they are being developed for high power and high frequency applications. A variety of reliability tests have been conducted on HEMTs, but there are less studies on its device degradation under forward gate bias condition. Typically, when a device is turned off, a very small off-state current exists due to the leakage current in the HEMT. However, after forward gate bias stressing, the off-state current is increased dramatically. As the high off-state current leads to higher power consumption and higher noise in the signals, this means that the device performance has degraded.

From the electrical measurements of the HEMTs before and after stressing, the gate contact was observed to have degraded after stressing, as the barrier height has decreased while the number of defects under the gate has increased. Both of these phenomenon led to the increase of the off-state current. Moreover, by conducting the temperature dependent electrical measurements coupled with computer-aided simulation, the defect-assisted electron transport mechanism (i.e. Poole-Frenkel emission) was determined to be the dominating factor for the increase in off-state current after stressing.

Furthermore, several physical characterization techniques were used to help identify the type of defects that have contributed to the device degradation. Based on the chemical

analysis, carbon was found to be present in the gate region where high off-state current was detected, but not in the regions where the off-state current was low. As carbon can lower the barrier height in the nickel gate and work as a defect under the gate region, this physical evidence correlates with what has been determined from the electrical measurements. It is believed that the carbon arises from the photoresist residue during the device fabrication. During the forward gate bias stressing, the residue at the gate metal/semiconductor interface decomposed due to the electrical field, which then causes the device degradation through the increase in off-state leakage current.

In summary, the mechanism of device degradation under forward gate bias is investigated and determined. As the photoresist residue at the gate metal/semiconductor interface causes the degradation, a clean interface is critical for improved device reliability. Thus, in order to enhance the device reliability, there should not be any residue at the interface between gate metal and semiconductor. The methods shown in this dissertation provide an integrated experimental approach for studying the device reliability by combining electrical characterization, physical characterization and computer-aided simulation.

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Abbreviations

2DEG	Two-dimensional Electron Gas
A^{**}	Effective Richardson Constant
ADF	Dark Field Detector
AES	Auger Electron Spectroscopy
AFM	Atomic Force Microscopy
CCD	Charge-Coupled Device
CMOS	Complementary Metal-Oxide-Semiconductor
CTE	Coefficients of Thermal Expansion
DF-STEM	Dark-Field Scanning Transmission Electron Microscopy
DI	Deionized
DUT	Device under Test
EDS/X	Energy Dispersive X-ray Spectroscopy
E	Energy Level of Electrons
EELS	Electron Energy Loss Spectroscopy
E_b	Electric Field in Schottky Barrier
E_{br}	Breakdown Field
E_{Fn}	Electron Quasi Fermi Level
E_g	Bandgap
EL	Electroluminescence
EMMI	Emission Microscopy
FIB	Focused Ion Beam
FN	Fowler-Nordheim
GIF	Gatan Image Filter
g_m	Transconductance
HAADF	High-Angle Annular Dark Field
HCR	High-Contrast Resolution
HEMT	High Electron Mobility Transistor
HFET	Heterostructure Field-Effect Transistor
I_{D-leak}	Drain leakage Current

I_{Dmax}	Maximum Drain Current
I_{D-sat}	Drain Saturation Current
I_{G-leak}, I_{Goff}	Gate Leakage Current
JEDEC	Joint Electron Device Council
J_{Gate}	Current Density of the Gate
k_B	Boltzmann Constant
LDMOS	Laterally Diffused Metal-Oxide-Semiconductor Field-Effect Transistor
LED	Light Emitting Diode
LiDAR	Light Detection and Ranging
LMIS	Liquid Metal Ion Source
MCP	Multichannel Plate
M_e	Electron Mass
mHEMT	Metamorphic High Electron Mobility Transistor
MODFET	Modulation-Doped Field-Effect Transistor
MOSFET	Metal-Oxide-Semiconductor Field-effect Transistor
n_i	Intrinsic Carrier Concentration
N_A	Acceptor Concentration
N_D	Donor Concentration
NIR	Near Infrared
pHEMT	Pseudomorphic High Electron Mobility Transistor
P_D	Dissipated Power
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PEM	Photo Emission Microscope
PF	Poole-Frenkel
q	Electron Charge
QM	Quantum Mechanics
ReaxFF	Reactive Force Field
R_D	Drain Resistance
RF	Radio Frequency
RH	Relative Humidity

R_S	Source Resistance
SAED	Selected Area Electron Diffraction
SDD	Silicon Drift Detector
SEM	Scanning Electron Microscopy
SMU	Source Measurement Unit
STEM	Scanning Transmission Electron Microscopy
TCAD	Technology Computer-Aided Design
TDD	Treading Dislocation Density
TDDDB	Time-Dependent Dielectric Breakdown
T	Temperature
TE	Thermionic Emission
TEM	Transmission Electron Microscopy
TLM	Transmission Line Method
UID	Unintentional Doped
v_e	Velocity of Electron
V_{th}	Threshold Voltage
V_G/V_{Gate}	Gate Voltage
V_{DS}	Drain to Source Voltage
v_{sat}	Saturated Drift Velocity
ϵ	Permittivity
Θ	Thermal Conductivity
η	Ideality Factor
ζ	Compensation Factor for PF emission
λ_e	Electron's Wavelength
μ_n	Electron Mobility
ϕ_B	Schottky Barrier Height
ϕ_C	Work Function of Carbon
ϕ_{Ni}	Work Function of Nickle
ϕ_t	Trap energy

Chapter 1

Introduction

In this chapter, the history and latest developments of GaN high electron mobility transistors (HEMTs) on Si substrates will be presented. Comparing to conventional Si semiconductor devices, GaN HEMTs have a relatively high breakdown field and electron mobility, which are ideal for high power and high frequency applications. Furthermore, GaN HEMTs on Si are very attractive for their lower fabrication cost and easier integration ability with Si technology.

1.1 High electron mobility transistor

The high electron mobility transistor (HEMT), also known as modulation-doped field-effect transistor (MODFET) or heterostructure field-effect transistor (HFET), is a field effect transistor in which the current flows between two ohmic contacts (source and drain) and is controlled by the third contact (gate). It is a heterojunction device, which uses two different materials with different bandgaps (such as GaAs/AlGaAs or GaN/AlGaN) to form a high mobility two-dimensional electron gas (2DEG) at the interface [1][1][1].

The HEMT structure was first proposed by Takashi Mimura in 1979. In the 1970s, he focused on the GaAs metal-oxide-semiconductor field-effect transistor (MOSFET) and faced challenges in making inversion- or accumulation-type *n*-channel devices due to the high density of surface states. He then came up with an idea to use a superlattice technique to build the AlGaAs/GaAs heterojunction and control the electron accumulation at the interface. Subsequently, he focused on using a Schottky gate to generate a field to control the electrons at the interface of the GaAs/AlGaAs heterojunction. Finally, the first HEMT device was presented in 1980 [2, 3], as shown in Figure 1.1.

Figure 1.1 The first HEMT structure [3].

The original HEMT was fabricated with *n*-type AlGaAs and GaAs, with the 2DEG forming at the interface due to the bandgap discontinuity. The major efforts to improve HEMT performance have been focused on developing the channel materials to obtain high electron mobility. An InGaAs layer was introduced between AlGaAs and GaAs buffer layers in order to create to increase the carrier mobility in the channel and to have a high bandgap offset with AlGaAs. As there is a lattice mismatch between InGaAs and GaAs, the InGaAs layer needs to be thin to achieve a heterostructure layer with a low threading and misfit dislocation density. This approach creates a pseudomorphic channel and therefore the device is named a pseudomorphic HEMT (pHEMT). In pHEMT, the concentration of indium is less than 35%, otherwise there will be a huge lattice mismatch to the GaAs substrate [4]. Subsequently, metamorphic HEMTs (mHEMTs) were developed by introducing a thick InGaAs buffer layer with graded indium concentration on the top of GaAs substrate. The lattice constant is gradually changed from the GaAs substrate through the thick InGaAs buffer. In this way, the indium concentration can reach as high as 80%, while still maintaining a relatively low dislocation density [4].

In the 2000s, AlGaN/GaN HEMTs started to draw people's attention. Compared to GaAs HEMTs, GaN HEMTs have larger bandgaps, higher heat transfer coefficients and higher electron concentrations. Table 1.1 shows important material properties (bandgap, intrinsic carrier concentration, permittivity, electron mobility, saturated drift velocity, breakdown field and thermal conductivity) and the Johnson's figure of merit (JM) for Si, GaAs and GaN (The crystal structure information of Si, GaAs, GaN and AlN is shown in the appendix). JM is the product of the breakdown field and saturated drift velocity, providing the power-frequency limit based only on material properties [5, 6]. For high power and high frequency transistors, this requires the device materials to have high breakdown voltage and high saturated drift velocity. Thus, from the JM value, GaN is much more promising in high frequency, high power and high voltage applications than GaAs and Si. Due to these encouraging features, GaN HEMTs are extremely attractive for both research and commercial applications.

Table 1.1 Material properties of Si, GaAs, and GaN related to the power performance of HEMTs at high frequency [6]

	Si	GaAs	GaN
E_g (eV)	1.1	1.42	3.39
n_i (cm ⁻³) at $T = 300$ K	1.5×10^{10}	1.5×10^6	1.9×10^{10}
ϵ_r	11.8	13.1	9.0
μ_n (cm ² /(V·s))	1350	8500	1200(Bulk) 2000(2DEG)
v_{sat} (10 ⁷ cm/s)	1.0	1.0	2.5
E_{br} (MV/cm)	0.3	0.4	3.3
Θ (W/(cm·K))	1.5	0.43	1.3
$JM = \frac{E_{br}V_{sat}}{2\pi}$	1	2.7	27.5

1.2 GaN HEMT and its application

GaN is a binary III/V semiconductor material with a wide bandgap [7]. GaN HEMTs are grown in the Wurtzite phase of GaN, as it is the most stable structure under ambient conditions [8, 9]. Furthermore, it has a built-in spontaneous polarization field, which comes from the ionicity of Ga-N covalent bonds and the low inversion symmetry of the Wurtzite structure. This spontaneous polarization is essential for building a high mobility transistor due to the polarization charges built at the AlGaN/GaN interface. To take advantage of the spontaneous polarization field, GaN is grown along the [0001] axis for HEMTs. The resulting surface is either Ga-terminated or N-terminated, depending on the growth method and substrate. The two different terminations determine the polarization field direction which are opposed to each other and have effects on both device fabrication and performance [10]. The two different faces are shown in Figure 1.2.

Figure 1.2 Two different surface: Ga-face and N-face [11].

In addition to spontaneous polarization, GaN is a piezoelectric material, which creates piezoelectric polarization. When there is a mechanical strain applied on the GaN, it will generate an additional electric field. By adding AlGaN on top of GaN, creates a mechanical misfit and strain develops in the GaN. This strain leads to an electric field and which extra carriers into the channel.

The unique properties of HEMTs come from the heterostructure that is formed by AlGaN and GaN. When the AlGaN and GaN are isolated, they have different Fermi levels. Once the AlGaN and GaN are placed together, an abrupt heterojunction is formed at the interface. At the abrupt interface, carriers start to flow from the AlGaN layer to the GaN layer due to spontaneous and piezoelectric polarization, and then the Fermi levels line up. Under thermodynamic equilibrium, a triangular potential well is formed at the interface. From Figure 1.3, at the GaN side of the interface, the conduction band of GaN is below the Fermi level, forming a high concentration 2DEG. If the channel is undoped, there are almost no impurities, which leads to a high electron mobility.

Figure 1.3 Band diagram for AlGaN and GaN (a) before and (b) after having contact.

Compared with conventional MOSFETs, the HEMTs have several advantages. First, there are fewer impurities in the channel, and thus the scattering rate is lower and gives higher channel mobility. Secondly, because there is a high concentration of available charge carriers in the channel, the device can work at much higher current densities. Furthermore, GaN has a higher thermal conductivity and stability, which make GaN HEMTs able to operate at higher temperatures.

Moreover, GaN is a wide bandgap material having a high breakdown voltage, and a low ON-state resistance due to the presence of the 2DEG. GaN HEMTs are very attractive for the high voltage power switches, where the devices are rapidly switched between ON and OFF states. Compared to conventional power devices, GaN HEMTs can achieve high power output and high energy efficiency. Furthermore, the high thermal conductivity ensures that the GaN devices have better heat dissipation, and the wide bandgap gives a low intrinsic carrier concentrations and small thermal currents. Both of these properties make the device more suitable for operation at high temperature. In addition to power switches, GaN HEMTs are also widely used in RF power amplification. In GaN HEMTs, the charge carriers can be formed from the effect of spontaneous polarization and piezoelectric polarization, which lead to additional carriers to the channel. Due to the strong intrinsic polarization, the 2DEG can be formed without doping. The undoped channel gives less channel impurities and higher channel mobility. The high mobility and large

concentration of the 2DEG make the GaN HEMTs able to work at high frequency with high efficiency, which are attractive for wireless communication systems and radar systems.

As for 5G, though there is no standard yet, performance targets are aimed to achieve high data rates, reduced latency, higher system capacity, and massive device connectivity [12]. GaN HEMTs considered to be promising technology for base station power amplifiers. Yole Développement has predicted that GaN devices will be implemented in 5G base station, as Si laterally diffused MOSFETs (LDMOS) have failed to work at the high frequencies required for 5G and GaAs devices performance degrades at such high power [13]. GaN HEMTs are also rugged and can be operated with minimal performance degradation under severe load mismatches at high powers [14].

LiDAR, which stands for Light Detection and Ranging, is a method to measure the distance to a target, by illuminating with a pulsed laser and measuring the reflected pulse [15]. LiDAR systems play key roles systems under development for self-driving cars. They give the vehicles a continuous 360 degree range of visibility and very accurate depth information [16]. In order to get sufficient range, the optical power must be high enough, for which high current drivers are required [17]. And for increasing resolution, the pulse width must be short enough (in nanosecond range) to avoid the overlap between the transmitting and receiving signals [18]. The high power and fast switching speeds of GaN HEMTs are viewed as essential for LiDAR technology. Efficient Power Conversion has already demonstrated a LiDAR that uses a GaN laser driver, which gives much higher resolution than the silicon driver [19]. Furthermore, as GaN HEMTs have higher power efficiency and switching frequencies, it is possible to make adapters with smaller size and fast multi-device wireless chargers based on those devices. These have become important features for consumer electronics devices [20].

1.3 GaN HEMTs on Silicon

Conventionally, GaN is grown on sapphire or SiC substrates rather than silicon substrates. Although, 6 inch sapphire and SiC wafers and 4 inch GaN wafers are available in the market, the fabrication cost is high because crystal growth for these three materials is

difficult and the technology is less developed, compared to Si wafers [21-23]. On the other hand, silicon technology is much more mature, which provides a larger wafer size with much lower cost, giving an attractive option as a substrate for growing GaN [24, 25]. As shown in Figure 1.4, GaN on Si wafers can be fabricated in much larger scale compared to any of its counterparts and the production cost is at least 10 times cheaper than other substrates. Thus, much recent research has focused on the development of GaN HEMTs on Si.

Figure 1.4 Comparison between GaN on different substrates (adapted from ref.[21]).

However, growing GaN on Si is a very challenging task. First, the lattice mismatch between GaN and Si is larger than that between GaN and sapphire, as well as GaN and SiC (shown in Figure 1.4). Due to the huge lattice mismatch between GaN and Si, many defects will be created at the GaN/Si interface and in the GaN film, making it extremely difficult to grow high quality GaN on Si. Secondly, the difference between the coefficients of thermal expansion (CTEs) of these two materials is huge. During the substrate growth process, the difference in CTEs may cause crack formation during the cooling, which sets another challenge of the GaN on Si growth [26]. Thirdly, there is a strong reaction between GaN and Si. The formation of Ga-Si alloy causes a “melt -back” etching reaction [27].

Thus, it is important to design a buffer layer to reduce that defect density. In order to avoid “melt-back”, a buffer layer of AlN is grown and a continuous AlN/Si interface is formed [27]. In order to prevent cracking, one of the solution is to grow a step-graded AlGaIn layer between the AlN buffer layer and GaN material. This transition layer can reduce the stress in the GaN layer, lowering the tendency of crack formation [28]. The other approach is to insert a AlN/GaN superlattice to create a compressive strain, which counteracts the tensile strain in GaN deposition on Si [29]. Furthermore, the strained layers are perpendicularly to the dislocation propagation directions. The dislocations trend to bend at the AlN/GaN interface due to the biaxial strain field of the superlattice, and therefore the density of dislocation can be reduced [30-32]. During the process, thick Si substrates (1 mm) are likely to be adopted to reduce the non-uniformity during the growth and wafer breakage. Additionally, in order to reduce the vertical leakage current, carbon is intentionally doped in the buffer layer as deep level dopant. It substitutes on nitrogen sites, acting as a deep acceptor [33]. This makes GaN:C *p*-type, and the vertical leakage current comes from holes which have lower mobility than electrons, leading to the reduction in leakage current. However, C-doped devices undergo current collapse when they are biased under high off-state high bias [34]. This phenomena can be reduced by an unintentional doped (UID) GaN channel on the top of C-doped GaN layer to separate the 2DEG from the C-dopants [35].

As HEMTs are able to operate under high power condition, their performance is affected by self-heating issues [36]. As Si has higher thermal conductivity than the Sapphire (shown in Figure 1.4), heat from the channel is much easier to dissipate to the substrate than sapphire. However, the GaN on SiC still has a better thermal performance compared to GaN on Si.

On the other hand, GaN HEMTs on Si substrates are perfect for system integration. Moore’s law has been driving the semiconductor industry for more than 5 decades. The IC industry is also pursuing a new trend of innovation, called “More than Moore”. More than Moore means that the semiconductor systems are not only required to continue to scale down according to Moore’s law, but also more importantly to have additional functionalities [37]. Now, systems are made by connecting different discrete components

(board-level integration). As silicon is not a perfect material for applications such as radio frequency (RF) devices and light emitting diode (LED) devices, these devices are usually fabricated from group III and group V materials [38]. If a system has both discrete Si and GaN devices, these devices must be integrated on a printed circuit board (PCB) board which leads to larger system size and higher power/performance loss. GaN on Si technology provides a new way to integrate at the system level. Since all the devices have the same substrate, the new system is able to integrate multifunctional components made using different materials into a single chip (chip-level integration). Figure 1.5 shows an approach to integration of conventional Si CMOS circuits with GaN HEMTs on Si, where the white box is an oxide isolation layer.

Figure 1.5 The schematic cross section of a GaN HEMT and Si CMOS system [39].

Although GaN HEMTs are promising for their fast switching speed, in high power applications, the actual switching speed is limited by large voltage overshoot caused by parasitic inductances in the power and drive loop [40, 41]. Thus, in order to avoid catastrophic failure by voltage overshoot, GaN switches are operated below their maximum speeds in real world applications [42]. Monolithically integrating GaN power switches and their CMOS drivers can be one of the possible solutions to reduce parasitic inductances.

1.4 Reliability of GaN HEMTs on Silicon

Reliability is critical for GaN devices, as the devices are aimed at working in high power and high voltage applications. Although GaN is considered as a robust material that is able to withstand high electric fields and high temperatures, it is important to know what the

limits for GaN devices are. In recent years, an increasing number of reports have shown that the degradation of GaN devices can happen after electrical stress. It is essential to investigate and understand the driving forces for those degradations and what are the physical models behind those failure mechanisms.

There are several failure criteria used by the GaN reliability community, such as the reduction of drain saturation current (I_{D-sat}), the increase of the gate leakage current (I_{G-leak}), and the change in the threshold voltage (V_{th}). When a device meets any of the failure criteria after stressing, it is considered as a failed device. Figure 1.6 illustrates typical failure mechanisms for the GaN HEMTs [43].

Several failure mechanisms written in red (1, 3) in Figure 1.6 are thermally activated degradations, which are more generic failure mechanisms that have been observed in other semiconductor devices as well. These mechanisms are most likely associated with the metallization scheme rather than GaN material itself. Mechanisms indicated in blue (2, 4) are hot-electron related degradations that are present in high voltage field-effect-transistors. These are due to hot-electrons generated by a high electric field, and it they are not unique for GaN devices. The mechanisms (5,6) are particular to GaN devices due to the electrochemical oxidation reactions and trap generation in AlGaIn/GaN layers [44, 45]. It is also believed that these two mechanisms are thermally activated. Although some degradation mechanisms are not due to failure of GaN, it is still important to understand how they affect the reliability of GaN devices.

Figure 1.6 Typical failure mechanisms on GaN HEMTs (adapted from ref [43]).

For GaN HEMTs, a relatively high density of threading dislocations in the device structure, as GaN is commonly grown on foreign substrates [46, 47]. The threading dislocation density (TDD) influences the device performance as well as its reliability [48-51]. It has been reported that devices with higher TDDs degrade faster compared to devices with the low TDDs, in terms of decreasing I_{D-sat} and increasing gate-lag (a delayed response of the channel current to modulation of the applied gate voltage [52]). This is mainly caused by impurity transport through dislocations from the surface to the AlGaN layer. Another group has found that there is pit formation during the off-state stressing. The pits are correlated to the decrease of I_{Dsat} , and pits were found to form at dislocations [25]. As GaN on Si has more dislocations because of the larger mismatch in lattice constants and CTE, dislocation-induced degradation is enhanced for Si-based GaN devices. Hence, it is critical to investigate how GaN HEMTs on Si degrade in comparison with GaN HEMTs on other substrates. Because of the benefits of GaN on Si mentioned earlier, it is necessary to put more focus on the failure modes of GaN HEMTs on Si. Thus, the focus of this thesis is to investigate the reliability of GaN HEMTs on Si and to develop a theoretical model to explain how the devices degrade. A further discussion of the reliability of GaN HEMTs on Si will be presented in the next chapter.

1.5 Device structure and its reliability

As GaN HEMTs have a wide range of applications, different device structures have been designed and fabricated to achieve different properties. For RF power devices, they are aimed to have higher RF performance at larger drain voltage bias. Thus, in this case, devices with field plates are designed to reduce the peak electrical field in the devices. While for the power switch application, normally-off devices are desired and therefore p-GaN instead of Schottky gate structure is introduced.

In conventional HEMTs, the gate is made with Schottky contact, as shown in Figure 1.6. Under the high voltage (field) operation, the gate edge towards to drain side, where the highest electric field is present, starts to degrade first. This may cause the decrease of I_{D-sat} and the increase of I_{G-leak} . In order to reduce the peak electrical field, field plates are introduced to the HEMTs, as shown in Figure 1.7. From the electric field distribution, the field plates can reduce the peak electric field. Therefore, this structure can reduce the field-induced degradation, which is shown in Figure 1.8.

Figure 1.7 Vertical field distribution along the GaN cap layer [53].

Device A is the device without any field plate, device B is the device with gate field plate and device C is the device with both gate and source field plates. All types of devices were stressed under on-state ($V_{DS} = 43$ V, $V_{GS} = 0$ V) and off-state ($V_{DS} = 35$ V, $V_{GS} = -8$ V) stressing for 120 s. Device A shows the most severe degradation, while there is almost no degradation on Device C. Although the degradation still occurred for the field plate devices, the degradation rate is much less compared to the devices without field plates [53].

Figure 1.8 I_{DS} - V_{GS} and g_m - V_{GS} for 3 types of devices before and after stressing [53].

For the p-GaN gate device, as it is a normally-off device, it could experience large forward gate bias during the operation. Thus, the reliability of p-GaN gate under forward gate bias is important to investigate as well. The structure of a p-GaN gate device is shown in Figure 1.9. It is found that the p-GaN gate broke down under a high positive gate bias and the breakdown voltage has a positive temperature dependence. This is due to impact ionization induced avalanche breakdown under a high electrical field across the p-GaN layer [54].

Figure 1.9 (a) A schematic and a TEM cross sectional image of p-GaN device.(b) gate breakdown at four different temperatures [54].

Recently, various GaN HEMT structures have been reported to improve RF performance or power performance, such as, multi-channel GaN, InAlN/GaN, and diamond back barrier devices [55]. The multi-channel devices are fabricated with fin-like structures which are patterned and etched on the surface of GaN HEMTs [56]. This multi-channel device shows high linearity in the RF performance, due to the increase of source and drain access resistance. The InAlN/GaN device has a similar structure as the AlGaIn/GaN HEMT, but it uses InAlN instead of AlGaIn to create 2DEG [57]. The electron mobility in InAlN/GaN is higher than AlGaIn/GaN, so InAlN devices could achieve higher output current and higher current gain cut-off frequency. The diamond back-barrier device can also improve the device performance [58]. The devices are grown on diamond substrate, as diamond has a high thermal conductivity, which could enhance thermally activated reliability during high power applications.

Figure 1.10 Some novel structures for GaN HEMTs. (a) Multi-channel device, (b) InAlN/GaN device and (c) diamond back barrier device [56-58].

Although there are a variety of HEMT structures, Schottky gate HEMT is the device with the most basic structure and many novel structures are made with Schottky gates. Thus, it is still important to understand the degradation mechanisms of Schottky gate HEMTs. By knowing how and why the Schottky gate fails, not only would it help improve the reliability of conventional Schottky gate HEMTs, but also the Schottky gate HEMTs with novel structures. In this dissertation research, only conventional Schottky gate HEMT will be discussed.

1.6 Objective and Scope

Based on the state-of-art theory, the I_{D-sat} degradation of GaN HEMTs is caused by electrochemical oxidation and trap generation in the AlGaIn/GaN layers [45, 59]. Moisture or oxygen from the environment will pass through the passivation layer and reach the AlGaIn surface. With the presence of high electric field during OFF-state stressing and high electron density for ON-state stressing, electrochemical oxidation reactions occur where the electric field is high. Both the electric field and ambient environment strongly impact the reliability of GaN HEMTs.

I_{G-leak} degradation also plays an important role in device reliability. Only the I_{G-leak} degradation under reverse gate bias has been well studied [45, 60-62]. The degradation is correlated with electrochemical oxidation for large reverse bias. For moderate stress conditions, the degradation becomes similar to TDDB (Time-Dependent Dielectric Breakdown) degradation. In addition to reverse gate bias, HEMTs also experience forward gate bias during device operation. However, there is no failure model for I_{G-leak} degradation under forward gate bias. In this thesis, a comprehensive study of I_{G-leak} degradation under forward gate bias stress will be presented.

References

1. Shur, M., *GaAs devices and circuits*. 1987, New York: Plenum Press.
2. Mimura, T., *The early history of the high electron mobility transistor (HEMT)*. IEEE Transactions on microwave theory and techniques, 2002. **50**(3): p. 780-782.
3. Mimura, T., S. Hiyamizu, T. Fujii, and K. Nanbu, *A new field-effect transistor with selectively doped GaAs/n-Al_xGa_{1-x}As heterojunctions*. Japanese journal of applied physics, 1980. **19**(5): p. L225.
4. Sze, S.M. and K.K. Ng, *Physics of semiconductor devices*. 2006: John Wiley & sons.
5. Johnson, E. *Physical limitations on frequency and power parameters of transistors*. in *1958 IRE International Convention Record*. 1965.

6. Mishra, U.K., L. Shen, T.E. Kazior, and Y.-F. Wu, *GaN-based RF power devices and amplifiers*. Proceedings of the IEEE, 2008. **96**(2): p. 287-305.
7. Gallium nitride. 2019; Available from: https://en.wikipedia.org/wiki/Gallium_nitride.
8. Fujikane, M., A. Inoue, T. Yokogawa, S. Nagao, and R. Nowak, *Mechanical properties characterization of c - plane (0001) and m - plane (10 - 10) GaN by nanoindentation examination*. physica status solidi c, 2010. **7**(7 - 8): p. 1798-1800.
9. Serrano, J., A. Rubio, E. Hernández, A. Muñoz, and A. Mujica, *Theoretical study of the relative stability of structural phases in group-III nitrides at high pressures*. Physical Review B, 2000. **62**(24): p. 16612.
10. Li, T., R.P. Joshi, and C. Fazi, *Monte Carlo evaluations of degeneracy and interface roughness effects on electron transport in AlGaIn-GaN heterostructures*. Journal of Applied Physics, 2000. **88**(2): p. 829-837.
11. Cho, E., *GaN Based Heterostructure Growth and Application to Electronic Devices and Gas Sensors*. 2009.
12. 5G. 2019; Available from: <https://en.wikipedia.org/wiki/5G>.
13. Wilson, R. *5G set to adopt GaN, but military protectionism may hit supply*. 2018; Available from: <https://www.electronicshweekly.com/news/5g-set-adopt-gan-military-protectionism-may-hit-supply-2018-02/>.
14. Microwave, F. *GaN's Role in 5G*. 2018; Available from: <http://www.mpdigest.com/2018/07/24/gans-role-in-5g/>.
15. Lidar. 2019; Available from: <https://en.wikipedia.org/wiki/Lidar>.
16. Cameron, O. *An Introduction to LIDAR: The Key Self-Driving Car Sensor*. 2017; Available from: <https://news.voyage.auto/an-introduction-to-lidar-the-key-self-driving-car-sensor-a7e405590cff>.
17. EPC, *How to Build an Ultra-Fast High-Power Laser Driver - That Sees Farther, Better, and at a Lower Cost!*. 2008.
18. Glaser, J.S., *eGaN FETs for Lidar – Getting the Most Out of the EPC9126 Laser Driver*. 2019.
19. EPC. *Lidar*. 2019; Available from: <https://epc-co.com/epc/Applications/Lidar.aspx>.

20. Systems, G. *CONSUMER ELECTRONICS*. 2019; Available from: <https://gansystems.com/market-insights/consumer-electronics/>.
21. Egawa, T., *Development of next generation devices amidst global competition due to their huge market potential*. Ultimate in Vacuum ULVAC, 2012(63): p. 18-21.
22. Fraga, M.A., M. Bosi, and M. Negri, *Silicon carbide in microsystem technology—thin film versus bulk material*. Advanced Silicon Carbide Devices and Processing, 2015: p. 1-30.
23. LLC, M.S. 2020; Available from: <https://www.msosupplies.com>.
24. Gil, B., *III-Nitride Semiconductors and their modern devices*. Vol. 18. 2013: OUP Oxford.
25. Cordier, Y., F. Semond, J. Massies, B. Dessertene, S. Cassette, M. Surrugue, D. Adam, and S. Delage, *AlGaIn/GaN HEMTs on resistive Si (111) substrate grown by gas-source MBE*. Electronics Letters, 2002. **38**(2): p. 91-92.
26. Zhu, D., D.J. Wallis, and C.J. Humphreys, *Prospects of III-nitride optoelectronics grown on Si*. Reports on Progress in Physics, 2013. **76**(10): p. 106501.
27. Semond, F., *Epitaxial challenges of GaN on silicon*. MRS Bulletin, 2015. **40**(5): p. 412-417.
28. Weeks Jr, T.W., E.L. Piner, T. Gehrke, and K.J. Linthicum, *Gallium nitride materials and methods*. 2003, Google Patents.
29. Feltin, E., B. Beaumont, M. Laügt, P.d. Mierry, P. Vennéguès, H. Lahrèche, M. Leroux, and P. Gibart, *Stress control in GaN grown on silicon (111) by metalorganic vapor phase epitaxy*. Applied Physics Letters, 2001. **79**(20): p. 3230-3232.
30. Meneghesso, G., M. Meneghini, and E. Zanoni, *Gallium Nitride-enabled High Frequency and High Efficiency Power Conversion*. 2018: Springer.
31. Gong, J.R., C.W. Huang, S.F. Tseng, T.Y. Lin, K.M. Lin, W.T. Liao, Y.L. Tsai, B.H. Shi, and C.L. Wang, *Behaviors of $Al_xGa_{1-x}N$ ($0.5 \leq x \leq 1.0$)/GaN short period strained-layer superlattices on the threading dislocation density reduction in GaN films*. Journal of Crystal Growth, 2004. **260**(1): p. 73-78.
32. Hiroki, M. and N. Kobayashi, *Flat surfaces and interfaces in AlN/GaN heterostructures and superlattices grown by flow-rate modulation epitaxy*. Japanese Journal of Applied Physics, 2003. **42**(4S): p. 2305.

33. Lyons, J.L., A. Janotti, and C.G. Van de Walle, *Effects of carbon on the electrical and optical properties of InN, GaN, and AlN*. Physical Review B, 2014. **89**(3): p. 035204.
34. Uren, M.J. and M. Kuball. *GaN transistor reliability and instabilities*. in *Advanced Semiconductor Devices & Microsystems (ASDAM), 2014 10th International Conference on*. 2014. IEEE.
35. Bahat-Treidel, E., F. Brunner, O. Hilt, E. Cho, J. Wurfl, and G. Trankle, *AlGaIn/GaN/GaN:C Back-Barrier HFETs With Breakdown Voltage of Over 1 kV and Low R_{on}* . IEEE Transactions on Electron Devices, 2010. **57**(11): p. 3050-3058.
36. Arenas, O., É. Al Alam, V. Aimez, A. Jaouad, H. Maher, R. Arès, and F. Boone, *Electrothermal mapping of AlGaIn/GaN HEMTs using microresistance thermometer detectors*. IEEE Electron Device Letters, 2015. **36**(2): p. 111-113.
37. Arden, W., M. Brillouët, P. Cogez, M. Graef, B. Huizing, and R. Mahnkopf, *More-than-Moore white paper*. Version, 2010. **2**: p. 14.
38. Kazior, T.E., *Beyond CMOS: heterogeneous integration of III–V devices, RF MEMS and other dissimilar materials/devices with Si CMOS to create intelligent microsystems*. Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences, 2014. **372**(2012): p. 20130105.
39. Kazior, T.E., R. Chelakara, W. Hoke, J. Bettencourt, T. Palacios, and H.S. Lee. *High Performance Mixed Signal and RF Circuits Enabled by the Direct Monolithic Heterogeneous Integration of GaN HEMTs and Si CMOS on a Silicon Substrate*. in *2011 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*. 2011.
40. Chu, R., B. Hughes, M. Chen, D. Brown, R. Li, S. Khalil, D. Zehnder, S. Chen, A. Williams, A. Garrido, M. Musni, and K. Boutros. *Normally-Off GaN-on-Si transistors enabling nanosecond power switching at one kilowatt*. in *71st Device Research Conference*. 2013.
41. Luo, F., Z. Chen, L. Xue, P. Mattavelli, D. Boroyevich, and B. Hughes. *Design considerations for GaN HEMT multichip halfbridge module for high-frequency power converters*. in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*. 2014.
42. Hughes, B., J. Lazar, S. Hulsey, M. Musni, D. Zehnder, A. Garrido, R. Khanna, R. Chu, S. Khalil, and K. Boutros. *Normally-off GaN-on-Si multi-chip module boost converter*

with 96% efficiency and low gate and drain overshoot. in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*. 2014.

43. Meneghesso, G., M. Meneghini, A. Tazzoli, N. Ronchi, A. Stocco, A. Chini, and E. Zanoni, *Reliability issues of Gallium Nitride High Electron Mobility Transistors*. International Journal of Microwave and Wireless Technologies, 2010. **2**(1): p. 39-50.
44. Joh, J. and J.A. Del Alamo, *Critical voltage for electrical degradation of GaN high-electron mobility transistors*. IEEE Electron Device Letters, 2008. **29**(4): p. 287-289.
45. Gao, F., S.C. Tan, J.A. del Alamo, C.V. Thompson, and T. Palacios, *Impact of water-assisted electrochemical reactions on the OFF-state degradation of AlGaIn/GaN HEMTs*. IEEE Transactions on electron devices, 2014. **61**(2): p. 437-444.
46. Kaun, S.W., M.H. Wong, S. Dasgupta, S. Choi, R. Chung, U.K. Mishra, and J.S. Speck, *Effects of threading dislocation density on the gate leakage of AlGaIn/GaN heterostructures for high electron mobility transistors*. Applied physics express, 2011. **4**(2): p. 024101.
47. Chen, W., C. Zhou, and K.J. Chen, *High-current-density high-voltage normally-off AlGaIn/GaN hybrid-gate HEMT with low on-resistance*. Electronics Letters, 2010. **46**(24): p. 1626-1627.
48. Ćapajna, M., U.K. Mishra, and M. Kuball, *Importance of impurity diffusion for early stage degradation in AlGaIn/GaN high electron mobility transistors upon electrical stress*. Applied Physics Letters, 2010. **97**(2): p. 023503.
49. Marino, F.A., N. Faralli, T. Palacios, D.K. Ferry, S.M. Goodnick, and M. Saraniti, *Effects of Threading Dislocations on AlGaIn/GaN High-Electron Mobility Transistors*. IEEE Transactions on Electron Devices, 2010. **57**(1): p. 353-360.
50. Green, D.S., S.R. Gibb, B. Hosse, R. Vetury, D.E. Grider, and J.A. Smart, *Control of epitaxial defects for optimal AlGaIn/GaN HEMT performance and reliability*. Journal of Crystal Growth, 2004. **272**(1): p. 285-292.
51. Ćapajna, M., S.W. Kaun, M.H. Wong, F. Gao, T. Palacios, U.K. Mishra, J.S. Speck, and M. Kuball, *Influence of threading dislocation density on early degradation in AlGaIn/GaN high electron mobility transistors*. Applied Physics Letters, 2011. **99**(22): p. 223501.

52. Mitrofanov, O. and M. Manfra, *Mechanisms of gate lag in GaN/AlGaN/GaN high electron mobility transistors*. Superlattices and Microstructures, 2003. **34**(1-2): p. 33-53.
53. Li, W., Q. Wang, X. Zhan, J. Yan, L. Jiang, H. Yin, J. Gong, X. Wang, F. Liu, and B. Li, *Impact of dual field plates on drain current degradation in InAlN/AlN/GaN HEMTs*. Semiconductor science and technology, 2016. **31**(12): p. 125003.
54. Wu, T., D. Marcon, S. You, N. Posthuma, B. Bakeroot, S. Stoffels, M.V. Hove, G. Groeseneken, and S. Decoutere, *Forward Bias Gate Breakdown Mechanism in Enhancement-Mode p-GaN Gate AlGaN/GaN High-Electron Mobility Transistors*. IEEE Electron Device Letters, 2015. **36**(10): p. 1001-1003.
55. Teo, K.H., N. Chowdhury, Y. Zhang, T. Palacios, K. Yamanaka, and Y. Yamaguchi. *Recent Development in 2D and 3D GaN devices for RF and Power Electronics Applications*. in *2020 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*. 2020. IEEE.
56. Joglekar, S., U. Radhakrishna, D. Piedra, D. Antoniadis, and T. Palacios. *Large signal linearity enhancement of AlGaN/GaN high electron mobility transistors by device-level V_t engineering for transconductance compensation*. in *2017 IEEE International Electron Devices Meeting (IEDM)*. 2017. IEEE.
57. Xing, W., Z. Liu, H. Qiu, K. Ranjan, Y. Gao, G.I. Ng, and T. Palacios, *InAlN/GaN HEMTs on Si With High f_{max} of 250 GHz*. IEEE Electron Device Letters, 2017. **39**(1): p. 75-78.
58. Zhang, Y., K.H. Teo, and T. Palacios, *Beyond thermal management: Incorporating p-diamond back-barriers and cap layers into AlGaN/GaN HEMTs*. IEEE Transactions on Electron Devices, 2016. **63**(6): p. 2340-2345.
59. Syaranamual, G.J., W. Sasangka, R.I. Made, S. Arulkumaran, G. Ng, S. Foo, C.L. Gan, and C.V. Thompson, *Role of two-dimensional electron gas (2DEG) in AlGaN/GaN high electron mobility transistor (HEMT) ON-state degradation*. Microelectronics Reliability, 2016. **64**: p. 589-593.
60. Mojaver, H.R. and P. Valizadeh, *Modeling the Reverse Gate-Leakage Current in GaN-Channel HFETs: Realistic Assessment of Fowler–Nordheim and Leakage at Mesa Sidewalls*. IEEE Transactions on Electron Devices, 2018. **65**(8): p. 3156-3162.

61. Sasangka, W.A., G.J. Syaranamual, C.L. Gan, and C.V. Thompson. *Origin of physical degradation in AlGaN/GaN on Si high electron mobility transistors under reverse bias stressing*. in *2015 IEEE International Reliability Physics Symposium*. 2015.
62. Meneghini, M., A. Stocco, M. Bertin, N. Ronchi, A. Chini, D. Marcon, G. Meneghesso, and E. Zanoni. *Electroluminescence analysis of time-dependent reverse-bias degradation of HEMTs: A complete model*. in *2011 International Electron Devices Meeting*. 2011.

Chapter 2

Literature Review

In this chapter, the standard failure criteria for III-V semiconductor devices are discussed first. Next, several different degradation mechanisms of GaN HEMTs are presented. Critical voltage theory and electrochemical oxidation are explained in detail with a focus on how the drain saturation current is degraded under different stressing conditions. While the increase in leakage current is well studied under reverse gate bias stressing, the degradation under forward gate bias remains unclear and further investigation is required. In order to understand how the leakage current changes, three different electron transport mechanisms are discussed to provide a more comprehensive picture of the leakage current degradation.

2.1 Standard reliability criteria

In this section, the standard reliability criteria for III-V transistors will be presented. These criteria (shown in table 2.1) are based on the Joint Electron Device Engineering Council (JEDEC) specification. JEDEC standard is widely used in the semiconductor industry. It indicates the most critical parameters of the transistor reliability. As shown in table 2.1, when one of the parameters exceeds the limit, the device is considered as a failed device.

Table 2.1 Failure criteria adapted from JEDEC [1]

Examination or Test	Symbol	Limit	Unit	Reference point
Gate Reverse Current	ΔI_{gs}	$3\mu A$ or 100%	μA or %	Initial Value
Pinch Off Voltage	ΔV_p	± 15	%	Initial Value
Saturated Drain Current	ΔI_{dss}	± 15	%	Initial Value
Output Power	ΔP_{out}	± 0.5	dB	Initial Value
Transconductance	ΔG_m	± 10	%	Initial Value

Table 2.2 shows a more recent failure criteria of GaN power switch devices from the company transphorm. The degradation of leakage current is defined as 5 to 10 times increase. As the application is power switch, the dynamic on resistance is important as it may affect the output power and is included in the failure criteria.

Table 2.2 Failure criteria of GaN power switch devices from transphorm [2]

Test Specifications		
Parameter	Specification Limit	Max Shift Allowed
I_{dss}	$<40 \mu A$	5X increase (10X increase for environmental testing)
I_{gss}	$<100 \text{ nA}$	Not applicable (low leakage)
Dynamic R_{on}	$62 \text{ m}\Omega$	$< 20\%$
V_{th}	$2.6/1.6 \text{ V}$	$<20\%$

The pinch off voltage can be indicated by the threshold voltage (V_{th}), which is an indicator showing the ON/OFF state of the transistor; if the V_{th} is changed, it is impossible to turn on and turn off the transistor precisely. The gate reverse current is also known as gate leakage current. The increment in gate reverse current will increase the power consumption under OFF-state operation. The saturated drain current degradation is the most common failure mode of semiconductor transistor devices. A decrease in the saturated drain current leads to a reduction of output current and the ON/OFF current ratio. The transconductance defines how fast the source-drain current increases in response to the voltage. Normally, the decline in transconductance is a byproduct of other degradation mechanisms, e.g. saturated drain current degradation. Thus, in this dissertation, the key electrical parameters of interest are threshold voltage, gate reverse current and saturated drain current.

2.2 The origin of the degradation

In this section, several failure models of GaN HEMT degradation are reviewed. As most of the failure mechanisms are field-induced and the electric field under OFF-state operation is higher than that at other conditions, hence the reliability issues during OFF-state condition were of the most concern in the earlier investigations. Then, the degradation under ON-state started to draw people's attention. In both operation conditions (ON and OFF), the model for drain current saturation degradation is well established, while the failure mechanism of leakage current is not very clear. Moreover, when the device is operated under forward gate bias conditions, there is no comprehensive study on its degradation. Thus, in this section, the degradation of saturation current under OFF-state will be discussed first, followed by the ON-state degradation. Then, in the last part, the degradation of leakage current will be reviewed.

2.2.1 Critical voltage theory and inverse piezoelectric effect

In 2006, J. Joh and del Alamo published their results as the first observation of GaN HEMT degradation [3]. The degradation was found after conducting several step-stress experiments. The devices were stressed both in ON-state and OFF-state conditions. The results showed that the electric field or electric bias is the main contributor to the device degradation, while the current might accelerate the degradation by introducing hot

electrons or heating up the channel. Hence, the main concern for GaN HEMTs reliability is the OFF-state reliability, in which a much larger electric field is present.

Figure 2.1 Changes in I_{Dmax} , I_{Goff} , R_D and R_S during the reverse step-stress experiment with $V_{DS} = 0$ V and $V_{DG} = 10$ to 50 V [3].

Figure 2.1 shows the results from the step-stress experiments. After stressing with a negative voltage on the gate, the I_{Dmax} dropped to 60% compared to its original value, while I_{Goff} , R_D and R_S increased. Interestingly, the degradation started only after the reverse gate bias reached a certain point. In this experiment, this voltage, which is named the critical voltage, was 20 V [4].

As the highest vertical field was at the gate edges, defects started to form in the AlGaN layer near the gate edges. These defects became trapping centers. These trapping centers are located at the gate to source/drain regions, leading to a reduction in carrier concentration and then a decrease in the drain saturation current. When a positive gate bias was applied after the step-stress, electron detrapping phenomena were observed, which further proved that electrons were trapped in those regions. To locate the defects, E. Zanoni *et al.* recorded electroluminescence (EL) images during the step-stress experiment [5]. As the reverse voltage increased, the density of hot spots also increased, which indicated an incremental increase in the number of defects. Because the gate metal blocked the signals under the

gate, only hot spots at the source and drain access regions could be recorded. From Figure 2.2, hot spots were detected at the gate edge towards the drain and source, where the electric field was the highest. This indicates that the defect formation might be a field driven effect. In order to prove this, E.A. Douglas *et al.* tested devices with different gate lengths under the same stressing condition [6]. Devices were designed with four different gate lengths: 100 nm, 125 nm, 140 nm and 170 nm, and their critical voltages were -17 V, -22 V, -27 V and -32 V. The critical voltage increased with the channel length. Using 2-D device simulations, it was shown that all the devices had nearly the same maximum electric field (shown in Figure 2.3), showing that the degradation mechanism was a field-driven effect.

Figure 2.2 EL images of TLM (transmission line method) samples during step-stress experiment $V_{DS} = 0$ V and $V_{DG} = 30 \sim 70$ V. Dashed lines indicate the device active area [5].

In 2012, Bajo *et al.* found that the defects at the gate edge are more conducting than at other places [7]. The devices were also stressed in the OFF-state, but with a high V_{DS} (from 30 to 50 V). After being stressed for 760 sec, an increased gate current was observed. Then the devices were etched in HF: H₂O (1:10) to remove the SiN passivation, aqua regia (HNO₃ + 3 HCl) to remove the metal contacts and finally piranha (H₂SO₄ + H₂O₂) for surface cleaning. Both conventional and conducting-tip atomic force microscopy (AFM)

were implemented to characterize the surface properties. Figure 2.4 shows topography and current images of a device surface.

Figure 2.3 Silvaco TCAD simulation of the maximum electric field with different gate length [6].

The dark dots in Figure 2.4(a) are the defects created during the stressing, and the dash lines indicate the gate edges. This device was stressed under both forward and reverse values of V_{DS} , so the defects were on both sides of the gate. From Figure 2.4(b), the current is relatively higher at the defects than at other places, showing the defects are more conductive. The current is higher at the center of the defects, where the pits were formed and the closest regions to the active channel. Thus, it is much easier for electrons to pass through the Schottky barrier in these defect regions. This gives additional conductive paths for electrons to the gate electrode that contributes to the increments of the gate current.

One of the unique properties of GaN and AlGaN is the piezoelectric effect; their lattice constants will change under electric bias. Because of this intrinsic property, the lattice mismatch would be enhanced during electric stressing. One of the theories that explains the degradation takes the inverse piezoelectric effect into consideration [8].

Figure 2.4 (a) AFM topography image and (b) AFM current image of the stressed sample after SiN and metal removal [7].

Due to the lattice mismatch between GaN and AlGaN, there is already an in-plane stress at the interface even without any electric bias. During the stress-step test, when a negative bias is applied to the gate, there is a high electric field present at the gate edges. As the field is not uniformly distributed, the stress from the piezoelectric effect was very high at the gate edges. Once the total stress reaches a critical value, crystallographic defects (e.g. pits) are formed and then cause the electrical degradation. This is most likely to happen at the gate edge where the pits are formed and the highest electric field is present. To prove this hypothesis, Joh and del Alamo [2] electrically stressed devices under an external mechanical force. Devices were stressed with tensile mechanical stress during a step-stress test, and the results showed that the critical voltage reduced by about 2 V [3]. In this case, the in-plane stress between AlGaN and GaN seems to be the cause for the defect formation. When the stressing voltage reached the critical voltage, the additional piezoelectric stress makes the total in-planes stress high enough to create the crystallographic defects.

N.A.Mahadik *et al.* experimentally confirmed the inverse piezoelectric effect using an *in-situ* high resolution X-ray diffraction (XRD) technique [9]. When AlGaN/GaN Schottky diodes were biased, the XRD technique allowed observation of strain variation induced by the bias. The samples were biased under both forward and reverse conditions (from -100 V to 10 V), and XRD measurements were made at each bias point. Figure 2.5 shows clearly the XRD spectrum changes under different electric bias conditions. When the sample is under forward bias, the spectrum shifts to the higher angle region. Meanwhile, under reverse bias, the spectrum shifts to the lower angle side. These results show that the GaN

channel is under different types of strain, in-plane compressive for the forward bias and in-plane tensile for the reverse bias.

Figure 2.5 XRD spectrum shift under different bias conditions: (a) forward bias and (b) reverse bias [9].

In 2012, Ancona *et al.* simulated the total principal stress (mechanical) induced by electrical stress for AlGaIn/GaN HEMTs, using a multi-dimensional thermoelectro-mechanical model [10]. Both ON-state and OFF-state stress conditions were simulated. However, when analyzing the piezoelectric stress as shown in Figure 2.6, the piezoelectric stress contributes only a small portion of the maximum principal stress along the simulated region, which means the piezoelectric stress is insufficient to cause the device degradation itself. The maximum principal stress is about 4 GPa, while the piezoelectric stress is only about 0.5 GPa. This means the piezoelectric stress cannot be the principal factor causing the formation of crystallographic defects. There should be other important parameters like strong electric field, high-energy electron source or elevated junction temperature (for ON-state) that lead to the degradation and the defect formation.

Choi *et al.* experimentally confirmed that the inverse piezoelectric stress was only a small portion of all the stresses in the GaN HEMT devices by using Raman spectroscopy [11]. In Raman spectroscopy, light is injected into the GaN HEMT and the light will interact with molecular vibration, phonons or other excitations. The vibration modes can be detected by the shift of reflected light energy. Some of the modes represent the atomic oscillation in the *c*-plane, which is sensitive to the lattice strain. Both GaN on Si and GaN

on SiC samples were tested, and all of them were tested at normal conditions (without any external stress) and voltage bias conditions. Figure 2.7 shows the result of this experiment. It indicates that the inverse piezoelectric stress is about 500 MPa for all the samples, and the total residual stress is around 3000 MPa for SiC substrate and 3500 MPa for Si substrate.

Figure 2.6 Simulation results in the OFF-state ($V_{DS} = 15$ V and $V_{GS} = -5$ V) vertically across the AlGaN layer from the gate edge towards (drain side) to the channel (2DEG). Showing the maximum principal stress, the piezoelectric stress, the electric field magnitude, and the conduction band energy relative to the gate [10].

Makaram *et al.* found that there was also physical degradation when the device was stressed below the critical voltage [12]. He tested devices with $V_{GS} = -7$ V and $V_{GD} = 8 \sim 50$ V at 150°C . The critical voltage of these devices was around 20 V. However, he found that there was a groove in the device after removing the passivation and metal contact. Meanwhile, many researchers have used transmission electron microscopy (TEM) to further analyze the device degradation. Park *et al.* made TEM lamina from degraded devices to analyze the degradation at the nanoscale [13]. With the help of the nanobeam energy-dispersive x-ray spectroscopy (EDX) technique, he was able to further interpret the formation of defects due to the high drain bias. He applied the EDX technique in defect regions and defect-free regions, and found that an oxygen peak was present in defect regions but not in the defect-

free regions. All these experimental results indicate that in addition to the inverse piezoelectric effect, there are other physical degradation mechanisms that lead to degradation.

Figure 2.7 Inverse piezoelectric stress and residual stress measured by Raman spectroscopy [11].

2.2.2 Electrochemical oxidation

As the degradation might be created by the presence of high electric field and oxygen, Gao *et al.* have studied the correlation between the device degradation and its oxidation [14]. The devices were stressed in the OFF-state under both in ambient air and vacuum conditions at room temperature. After the stressing, defects were found along the gate edge, and Auger electron spectroscopy (AES) was applied to examine the chemical composition of these defects. In the defect regions, the oxygen concentration was much higher than the other regions, suggesting an oxidation process during the OFF-state stress. The defects were formed along the gate edge where the highest electric field was present, which indicated it was a field-enhanced oxidation. When the devices were stressed under vacuum, the degradation was much less than in the ambient air. The top-view scanning electron microscope (SEM) images in Figure 2.8 show the different levels of degradation under those two stress conditions. It is obvious that the stress-created defects are much denser in

the devices stressed in air than those tested in vacuums. This shows a field-enhanced chemical oxidation on the nitride surface causing the device degradation. The oxygen from the air can diffuse through the passivation layer (Al_2O_3) and reach the AlGaN surface.

Figure 2.8 Top- view SEM image of stressed devices at $V_{DS} = 0$ V and $V_{GS} = -40$ V for 6000 s at room temperature after gate removal (a) stressed in ambient air (b) stressed under vacuum condition 3×10^{-5} Torr [14].

In addition to oxygen in the ambient air, there is also moisture in the stressing environment that might contribute to the device degradation. Thus, it is very important to investigate how moisture affects the device performance and reliability. The same authors tested devices at different relative humidity (RH) levels created by heating deionized (DI) water [15]. For the unpassivated devices, I_D - V_G characteristic pulse measurements were conducted both in dry air (RH = 0.01%) and ambient air condition (RH = 40%). The results show that the current collapsed was higher in ambient air, while in dry air there was no clear evidence of current collapse, which has similar features as shown in Figure 2.9. To further prove the effect of moisture, the same type of devices were tested under dry helium gas and wet helium gas. This again showed a similar result that high humidity gave high current collapse, which demonstrated moisture is a main factor causing the poor performance. Devices with different passivations were also studied to investigate whether passivation could block moisture diffusion from the air to the AlGaN surface. Two materials (C_4F_8 and SiO_2) and four different structures (15 nm SiO_2 , 15 nm C_4F_8 , 30 nm SiO_2 , and 15 nm SiO_2 with 15 nm C_4F_8 on the top) were deposited on the device surface.

The devices were characterized under the same conditions as the unpassivated devices. Figure 2.9 gives the test results for the four types of devices.

Figure 2.9 DC and pulsed characteristics under different relative humidity levels with four types of structures [15].

From Figure 2.9, it is clear that the device with C_4F_8 passivation has a better performance under high humidity levels. The high porosity and hydrophilic properties of SiO_2 do not prevent water molecules from reaching the AlGaIn surface. On the other hand, the hydrophobic material C_4F_8 totally eliminates the current collapse phenomenon. By blocking the moisture outside the device, the reliability increased significantly due to the lack of water molecules at the AlGaIn surface.

Gao *et al.* also carried out experiments under the water-saturated oxygen gas, nitrogen gas and carbon dioxide gas and the same types of dry gases conditions. After stressing, SEM and TEM techniques were used to analyze the device degradation. Interestingly, the samples stressed under the water-saturated gas have more and larger pits than the dry gas ones, which shows that water is an essential part of the pitting and degradation. All the pits were oxidized, and larger oxidized pits were found under the water-saturated stress conditions, as shown in Figure 2.10. This suggests that pure oxygen gas is not enough to

cause severe degradation, and the oxygen detected in the pits may originate from the water. This suggests a water-assisted electrochemical oxidation process, which causes the surface pitting at the gate edge and then leads to the device degradation. During the OFF-state stressing, the metal, SiN and AlGaIn form a reaction cell as shown in Figure 2.11. Once the water molecules reach this region, the oxidation process starts. As in the OFF-state stress condition, the gate has a more negative potential as compared to the channel, and the gate metal acts as the cathode and the AlGaIn channel acts as the anode in the reaction.

Figure 2.10 SEM images of AlGaIn/GaN HEMTs stressed in an OFF-stated condition in (a) water-saturated Ar and (b) dry Ar, after the gate metal and passivation removal. Corresponding cross-sectional TEM images at the gate edge of the drain side in (c) water-saturated Ar and (d) dry Ar, before etching [16].

During the oxidation process, water molecules first react with the electrons coming from the gate, and then produce hydroxyl ions and H₂. Meanwhile, the holes reach the AlGaIn layer, leading to decomposition of the layer into Al ions, Ga ions and N₂. Finally, the

negative hydroxyl ions react with the positive Al and Ga ions, leading to the oxidation of Al and Ga ions. All the processes are summarized in the following equations.

So the overall reaction can be represented as:

Figure 2.11 Electrochemical cell at the gate edge [16].

It is not difficult to conclude that the electrons come from the gate as it has the most negative potential, but the holes may be generated in different ways. Gao *et al.* did several

simulations and calculations, and suggested that the holes come from interband tunneling due to the high electric field.

W. Sasangka *et al.* found that the oxidation does not uniformly occur along the gate edge [17]. After AlGaIn/GaN devices were stressed under reverse bias, the gate metal was removed by chemical etching. Pits, which are oxygen rich regions, were found along the gate edge. However, a cross section TEM image (Figure 2.12) shows that the pits are not located at the exact gate edge where the electrical field is maximum, but at dislocations that predominantly have screw components. This is because the energy required to form a pit is much reduced in the dislocation regions than other places.

Figure 2.12 (a) to (c) Cross sectional TEM images of stressed devices before metal removal, taken along the [210] zone axis. Pits are seen to form at locations away from the maximum electric field (E_{max}) (the gate edge). (d). Image of sample (c) taken using a weak beam technique at $\bar{g} = (002)$. (e) Image of sample taken using a weak beam technique at $\bar{g} = (120)$ [17].

W. Sasangka *et al.* also studied the quality of passivation that is essential for device reliability [18]. Two types of devices were tested under reverse bias at 225°C for 500 hr. The difference between those two types of passivation is the SiN density. The degradation trends have two different rates, which are named fast mode and slow mode. W. Sasangka *et al.* concluded that pre-existing oxygen at the SiN/AlGaIn interface contributes to the fast-mode degradation. During the slow-mode phase, the oxygen diffuses from the ambient through the SiN layer, leading to the degradation. The degradation rate is the same for the fast mode between different SiN densities. However, in slow mode, the devices with denser SiN have slower degradation rates. This is due to the faster electrochemical oxidation that has occurred in lower density SiN. When the SiN is oxidized, oxygen from the ambient can diffuse through the degraded area, causing further oxidation at the AlGaIn surface near the gate edge. The higher density SiN shows lower oxygen diffusivity, which slows down the oxygen diffusion from the ambient and improves the device reliability.

While previous researchers have studied the oxidation during OFF-state stressing, G.J. Syaranamual *et al.* found that the electrochemical oxidation plays a role in degradation during ON-state stressing [19]. The devices had much more severe degradation during ON-state stressing than during OFF-state stressing. After the gate metal removal, pits were found not only at the gate edge, but also along the gate-drain access region. No pits were found at the source-gate access region. This was because the electric field at the drain side was much higher than at the source side. As there are a high number of electrons in the channel during the ON-state operation, pit formation is not constrained to be at the gate edge, but extends from gate edge into the gate-drain access region. During the oxidation reaction, electrons are scattered from the 2DEG channel to the AlGaIn surface, where they participate in the electrochemical oxidation process previously described, together with the holes generated by impact ionization and oxygen from the ambient. A schematic of this process is shown in Figure 2.13.

Figure 2.13 Electrochemical oxidation of AlGaIn under ON-state stressing [19].

Recently, Mehdi Rzin et al. have studied the reliability on 0.25- μm AlGaIn/GaN HEMT with Ni/Pt/Au Schottky gate [20]. During the OFF-state or low power stressing, the degradation was not severe. On the other hand, when the devices were biased at On-state stressing with high dissipated power (P_D), there was a significant degradation on the I_{D-sat} and g_m . It is likely due to the electrochemical oxidation at the metal-semiconductor interface. Figure 2.14 shows the cross-sectional TEM and EDX images of the gate contact for a fresh sample. From the TEM image, a clean interface between Ni and AlGaIn is observed. From the EDX image, three smooth and distinct metal layers (Ni/Pt/Au) are present. For the stressed devices which are shown in Figure 2.15, the metal-semiconductor interfaces became rough due to the oxidation in both cases, and Au diffused through the SiN sidewall and then substituted the Ni layer. For the device stressed at higher P_D , the oxidation was much severe, as shown in Figure 2.15(b). The diffusion of Au from the SiN sidewall led to the Schottky junction degradation. However, as the work functions of Au and Ni are similar (1.05 eV for Au and 0.98 eV for Ni), the diffusion of Au might not lead to significant degradation. For the electrochemical oxidation, it is enhanced not only by the high electrical field, but also by the junction temperature. As the highest electrical field is

located at gate edge towards the drain side during stressing, the oxidation would not be uniform along the metal-semiconductor interface, as shown in Figure 2.15(b). The higher electrical field promotes impact ionization process and therefore creates larger number of holes that are essential for the electrochemical oxidation. Furthermore, the higher junction temperature thermally enhances the electrochemical oxidation process.

Figure 2.14 (a) TEM and (b) EDX images of a fresh sample at the gate contact [20].

Figure 2.15 TEM and EDX images of stressed samples: (a) Stressed at $V_{GS} = 1$ V, $V_{DS} = 38$ V and $P_D = 31$ W/mm for 24 hours. (b) Stressed at $V_{GS} = 0$ V, $V_{DS} = 60$ V and $P_D = 35$ W/mm for 24 hours [20].

2.2.3 Gate leakage degradation

In the previous sections, the degradation of drain current was discussed. In addition to the reduction in drain current, the increase in reverse gate leakage current is also a major concern for device reliability. This failure, which leads to operation instability, high power consumption and low noise performance, is usually caused by the degradation of the Schottky diodes under the metal gate of HEMT devices [21]. It has been shown that even for devices stressed under small reverse bias for a sufficiently long time, there will be a catastrophic and permanent increase of gate leakage current.

To develop a better understanding of gate leakage degradation, M. Meneghini *et al.* [22] fabricated a vertical AlGaIn/GaN Schottky diode structure. The devices were tested under reverse bias for 18 hr. After the stress, gate leakage increased more than one order of magnitude, and the C - V measurement showed that defects were generated at the AlGaIn/GaN interface during the stressing. When the contact pad was removed, there were no pits found in the active region, indicating the stress generated point defects [23]. Although the stressing voltages were below the critical voltage, degradation of the gate leakage current was still observed. Furthermore, hot spots were found on the gate edge using Emission Microscopy (EMMI), which is consistent with the increase in gate leakage. The leakage current showed a strong dependence on the bias and a weak dependence on the temperature, as shown in Figure 2.14. By measuring the gate-to-drain and gate-to-source diodes, it was confirmed that the leakage path was below the gate through the AlGaIn layer. The gate leakage degradation is similar to time-dependent degradation, such as gate oxide breakdown in CMOS transistors [24].

Figure 2.14 (a) Voltage dependent failure time distributions and (b) temperature dependent failure times for GaN HEMTs stressed under reverse bias [24]. Failure was defined in terms of the first sudden increase in the gate leakage current during the stressing.

M. Meneghini *et al.* proposed a model to explain the Schottky degradation under reverse bias [25]. The devices were stressed below the critical voltage for about 30 hr. The gate leakage current decreased at the beginning of the test, followed by a sudden increase. During the stressing, EL signals were taken, and the spectrum showed a broad yellow peak. This indicates that electrons injected into the buffer have created donor-acceptor pairs which generate the yellow luminescence. Meanwhile, hot-spots were generated during the experiment and their density increased with the stress time. The authors suggested that the defects were negatively charged and blocked the current flow in the first period of the stress. After a sufficient number of defects were generated, a conductive path formed and led to the gate leakage degradation. A schematic description is shown in Figure 2.15.

While a number of studies have focused on the reverse gate stress, other groups stressed GaN HEMTs under forward gate bias [26]. Devices were stressed under forward gate bias with an increasing voltage for around 17.5 hr. The degradation was found mostly in the gate leakage current, and has little effect on the drain current, as shown in Figure 2.16. However, the physical model behind the forward gate degradation is still unclear.

Figure 2.15 Schematic description of the origin of gate leakage degradation under moderate reverse bias stressing [25].

Figure 2.16 Forward gate bias stressing for 17.5 hr (a) I_D - V_G characteristic and transconductance (b) gate leakage current [26].

Another group stored a number of devices at 325°C without any electrical stress for 1000 hr [27]. I_D - V_G measurements were conducted to characterize the electrical performance after 24, 48, 96, 192, 384, 786, and 1000 hr. I_{D-sat} increased during the thermal stress accompanied with a negative shift of V_{th} , as shown in Figure 2.17. The Focused Ion Beam (FIB) technique was used to examine the cross section of the Schottky contacts. Compared with a fresh device, the thermal-stressed device has an unclear interface between the gate metals, indicating an interdiffusion process. This phenomenon was postulated to be the origin of the leakage current.

Figure 2.17 (a) Saturation drain current, (b) threshold voltage, (c) gate and drain leakage current during the 1000 hr thermal stress [27].

2.3 Current transport mechanisms for the Schottky contact of GaN HEMTs

As mentioned in the previous sections, gate leakage degradation is mainly caused by the instability of the gate Schottky contact [25, 27]. Understanding the gate current transport mechanisms at the Schottky contact is essential for modeling the device reliability.

Thermionic emission (TE), Poole-Frenkel (PF) emission, and Fowler-Nordheim (FN) tunneling can contribute to current transport at the gate Schottky contact over a wide range of electric bias and temperature. TE dominates under forward bias, while PF and FN play significant roles under the reverse bias [28, 29].

2.3.1 Thermionic emission

There are different transport mechanisms through the metal-semiconductor interface under forward bias, which are shown in Figure 2.18 [30]. Process (a) is the emission of electrons over the Schottky barrier at the semiconductor-metal interface. Process (b) is electron tunneling through the barrier. Processes (c) and (d) are the recombinations of electron-hole pairs in the space charge region and neutral region, respectively. For an ideal and high-mobility semiconductor, electron transport is mainly dominated by process (a) (thermionic emission) under forward bias [31].

TE (thermionic emission) theory assumes that the barrier height is higher than $k_B T$ and thermal equilibrium is established at the interface [32]. This theory suggests that the current is limited by the emission process and the quasi-fermi level E_{Fn} remains flat through the depletion region. Thus, the barrier profile is immaterial and the current flow is mainly determined by the barrier height. The current density from the semiconductor to the metal depends on the concentration of electrons with sufficient energy to overcome the barrier height. As this barrier height is voltage dependent, the current density is

$$J_{s \rightarrow m} = A^* T^2 \exp\left(-\frac{q\phi_B}{k_B T}\right) \exp\left(\frac{qV}{k_B T}\right), \quad \text{Equation 2.5}$$

where A^* is the effective Richardson constant, T is the temperature, q is the elementary charge, ϕ_B is the barrier height, k_B is the Boltzmann constant and V is the applied voltage.

While the barrier height for electron emission from the metal to semiconductor is unaffected by voltage, the current flow into the semiconductor can be written as

$$J_{m \rightarrow s} = -A^* T^2 \exp\left(-\frac{q\phi_B}{k_B T}\right). \quad \text{Equation 2.6}$$

Thus, the overall current density for an ideal Schottky diode is given by

$$J_n = A^* T^2 \exp\left(-\frac{q\phi_B}{k_B T}\right) \left[\exp\left(\frac{qV}{k_B T}\right) - 1\right]. \quad \text{Equation 2.7}$$

Figure 2.18 Electron transport mechanisms at the metal-semiconductor interface under forward bias [30].

When the devices are heavily doped or have a high density of defects (e.g. dislocations) as some defects are electrically active and therefore could act as dopants, the barrier becomes thinner and the tunneling current can contribute to the current through the barrier [30]. In this case, field emission (FE) or thermionic-field emission (TFE) starts to become the dominant transport mechanism. FE is purely a tunneling process and mainly depends on the electrical field across the barrier. On the other hand, electrons obtain extra thermal energy and are excited to higher energy for TFE. As shown in Figure 2.19, electrons with higher energy have less tunneling distance than the lower ones, which increases the tunneling possibility dramatically. On the other hand, the density of electrons decreases rapidly with increasing electron energy. Thus, there is an energy level E_m which contributes to the majority of the tunneling current. The tunneling current is given by,

$$J_{tunneling} = \frac{A^{**}T^2}{k_B T} \int_{E_{Fm}}^{q\phi_B} F_s T(E) (1 - F_m) dE, \quad \text{Equation 2.8}$$

where F_s and F_m are the Fermi-Dirac distribution functions of the semiconductor and metal, respectively, and $T(E)$ is the tunneling possibility through Schottky barrier at a particular energy level (E) [31].

By adding the tunneling component, the total forward current density becomes

$$J = J_0 \left[\exp \left(\frac{qV}{\eta k_B T} \right) - 1 \right], \quad \text{Equation 2.9}$$

where V is the applied voltage across the diode, J_0 is the saturation current density determined by extrapolating the forward current density on a semi-log plot to $V = 0$ V, and η is the ideality factor, which indicates the slope of the semi-log plot. In a perfect Schottky contact, the ideality factor is 1, meaning that the electron transport mechanism is pure thermionic emission. In reality, the ideality factor is generally larger than 1 due to the defects at the gate-semiconductor interface. These defects may enhance non-thermionic emissions (e.g. TFE) across the barrier, leading to a larger ideality factor [31].

Figure 2.19 A schematic of field emission and thermionic-field emission [33].

2.3.2 Poole-Frenkel emission

PF emission is also known as field-assisted thermal ionization. For GaN Schottky diodes, it is the dominant electron transport process for reverse leakage current at relatively high temperature under a moderate electric field.

In general, this effect is usually associated with traps inside the semiconductor. The traps must be positively charged when empty and neutral when filled in order to have PF emission [34]. With the presence of an electric field, the positively charged traps lower the Coulombic potential barrier height and thus increase electron emission, which is shown in Figure 2.20.

In Figure 2.20, the solid line represents the Coulombic potential as a function of the distance from the positively charged ion and ϕ_{PF} is the emission barrier (also known as the trap level (ϕ_t)). Under the electric field, the bottom of the conduction band is reduced by $\Delta\phi_{PF}$, where the barrier attenuation is proportional to the electric field

$$\Delta\phi_{PF} = \left(\frac{q}{\pi\epsilon_0\epsilon_s}\right)^{1/2} E_b^{1/2}, \quad \text{Equation 2.10}$$

and q is the electron charge, ϵ_0 is the permittivity of free space, ϵ_s is the high frequency dielectric constant of the semiconductor and E_b is the electric field across the semiconductor.

The current density due to PF emission is governed by

$$J_{PF} = \sigma E_b \exp \left[-\frac{q(\phi_{PF} - \Delta\phi_{PF})}{\xi k_B T} \right] = \sigma E_b \exp \left[-\frac{q(\phi_t - \sqrt{qE_b / (\pi\epsilon_0\epsilon_s)})}{\xi k_B T} \right], \quad \text{Equation 2.11}$$

where σ is the conductivity of the system and ξ is named as the compensation factor, which has values ranging from 1 to 2 depending on the donor and acceptor concentrations [34-36].

Figure 2.20 A schematic of PF emission. The solid line indicates the Coulombic potential without an electric field; while the dash line shows the Coulombic potential profile with an electric field [35].

H. Zhang *et al.* have observed PF emission for AlGaIn/GaN Schottky diodes at room temperature [37]. Both AlGaIn/GaN and GaN diodes were tested under measurements at different temperatures dependent. In the range from 250 K to 400 K, all the diodes showed PF emission. Interestingly, the emission barrier heights are almost the same for both diode structures. The authors conclude that it is most likely that electrons thermally emit from the metal into a dislocation related trap states, which is shown schematically in Figure 2.21. Furthermore, as the ionization process of the trap is temperature dependent, PF emission rate vary at different temperature.

Figure 2.21 Schematic of PF emission in AlGaIn/GaN HEMTs [38].

2.3.4 Fowler-Nordheim tunneling

Fowler-Nordheim (FN) tunneling is a field emission tunneling mechanism. It was first observed in metal-insulator-semiconductor structures [39, 40]. H. Zhang *et al.* applied this model for analysis of AlGaN/GaN diodes [37]. Under high reverse bias, there is a strong band bending in the semiconductor, so the electrons can tunnel through a triangular barrier with a smaller tunneling distance. Due to a shorter tunneling distance, the tunneling probability is increased. Figure 2.22 shows a schematic for FN tunneling.

Figure 2.22 Schematic for FN tunneling in AlGaN/GaN HEMTs [38].

The current density due to FN tunneling is

$$J_{FN} = AE_b^2 \exp\left(-\frac{B}{E_b}\right), \quad \text{Equation 2.12}$$

where $B = 8\pi\sqrt{2m_n^*(q\phi_B)}^3/3qh$, A is a constant, m_n^* is the effective electron mass of the semiconductor, ϕ_B is the barrier height of the gate diode, E_b is the electric field across the barrier, h is the Planck constant and q is the elementary charge. In Equation 2.12, there is no temperature parameter, so the FN tunneling current is independent of temperature, but strongly dependent on the electric field.

2.4 Summary

In this chapter, different failure mechanisms are summarized both for gate leakage and drain saturation current degradation. Equation 2.13 shows the theoretical calculation of the I_{D-sat} based on constant mobility assumption.

$$I_{D-sat} = \frac{W\mu_n C_o}{2L} (V_G - V_T)^2, \quad \text{Equation 2.13}$$

where the W is the channel width, L is the channel length, μ_n is the channel mobility and C_o is the gate capacitance. V_G and V_T are the gate voltage and threshold voltage, respectively. For drain current degradation, normally there is almost no change in the V_T . But for electrochemical oxidation, as the channel composition is changed, the charge or the current may not be constant throughout the channel. From the original drain current shown in Equation 2.14:

$$I_D = \frac{z}{L} \int_0^L |Q_n(x)| v(x) dx, \quad \text{Equation 2.14}$$

where z is the width of the device, $Q_n(x)$ and $v(x)$ are the channel charge and carrier drift velocity inside the channel. During the stressing accompanied by electrochemical oxidation, the value of $Q_n(x)v(x)$ might be diminished in the degraded region, and then causes the I_{D-sat} degradation.

For gate leakage current degradation, there are different failure models, which is probably due to the different types of samples and different stress conditions. As the gate contact is a Schottky contact, under reverse bias, the tunneling current follows Equation 2.15:

$$J_{s \rightarrow m} = \frac{A^{**} T^2}{k_B T} \int_{E_{Fm}}^{q\phi_B} F_s T(E) (1 - F_m) dE, \quad \text{Equation 2.15}$$

where A^{**} is the reduced effective Richardson constant, T is the temperature, k_B is the Boltzmann constant, ϕ_B is the Schottky barrier height and E_{Fm} is the fermi level in the metal. F_s and F_m are the Fermi-Dirac distribution ϕ_B functions for the semiconductor and

metal, respectively. $T(E)$ is the tunneling probability, which depends on the barrier width. Therefore in Bajo's experiments [7], the barrier thickness has reduced, causing the increase in the leakage current. While based on the results of M. Meneghini *et al.* [25], the failure mechanism is different. In this case, the behavior is more similar to dielectric breakdown, which conduction paths develop in the AlGaIn layer. These conduction path act as leakage paths and enhance the leakage current.

Compared to the degradation of I_{D-sat} , the degradation of I_{G-leak} is not well understood. Under forward gate bias stressing, I_{G-leak} is increased dramatically over time [26]. Various models have explained how the leakage current increases under different stressing conditions, but the degradation mechanisms vary among different cases [4, 7, 25]. Thus, it is important and necessary to investigate specifically how the leakage current increases under forward gate bias stressing.

References

1. *Failure criteria*. 2019; Available from: <https://www.jedec.org/>.
2. Kurt Smith, E.G., Jeff Haller, Peter Smith, Rakesh Lal, Yifeng Wu, *Reliability Testing of AlGaIn/GaN Power Switch Devices as Low and High Temperature*. 2017.
3. Joh, J. and J.A. del Alamo. *Mechanisms for electrical degradation of GaN high-electron mobility transistors*. in *Electron Devices Meeting, 2006. IEDM'06. International*. 2006. IEEE.
4. Joh, J., L. Xia, and J.A.d. Alamo. *Gate Current Degradation Mechanisms of GaN High Electron Mobility Transistors*. in *2007 IEEE International Electron Devices Meeting*. 2007.
5. Zanoni, E., F. Danesin, M. Meneghini, A. Cetrionio, C. Lanzieri, M. Peroni, and G. Meneghesso, *Localized Damage in AlGaIn/GaN HEMTs Induced by Reverse-Bias Testing*. *IEEE Electron Device Letters*, 2009. **30**(5): p. 427-429.
6. Douglas, E.A., C.Y. Chang, D.J. Cheney, B.P. Gila, C.F. Lo, L. Lu, R. Holzworth, P. Whiting, K. Jones, G.D. Via, J. Kim, S. Jang, F. Ren, and S.J. Pearton, *AlGaIn/GaN High Electron Mobility Transistor degradation under on- and off-state stress*. *Microelectronics Reliability*, 2011. **51**(2): p. 207-211.

7. Bajo, M.M., C. Hodges, M.J. Uren, and M. Kuball, *On the link between electroluminescence, gate current leakage, and surface defects in AlGaIn/GaN high electron mobility transistors upon off-state stress*. Applied Physics Letters, 2012. **101**(3): p. 033508.
8. del Alamo, J.A. and J. Joh, *GaN HEMT reliability*. Microelectronics reliability, 2009. **49**(9-11): p. 1200-1206.
9. Mahadik, N.A., S.B. Qadri, and M.V. Rao, *In situ strain measurements on GaN/AlGaIn Schottky diodes with variable bias*. Applied Physics Letters, 2008. **93**(26): p. 262106.
10. Ancona, M., S. Binari, and D. Meyer, *Fully coupled thermoelectromechanical analysis of GaN high electron mobility transistor degradation*. Journal of Applied Physics, 2012. **111**(7): p. 074504.
11. Choi, S., E. Heller, D. Dorsey, R. Vetury, and S. Graham, *The impact of mechanical stress on the degradation of AlGaIn/GaN high electron mobility transistors*. Journal of Applied Physics, 2013. **114**(16): p. 164501.
12. Makaram, P., J. Joh, J.A. del Alamo, T. Palacios, and C.V. Thompson, *Evolution of structural defects associated with electrical degradation in AlGaIn/GaN high electron mobility transistors*. Applied Physics Letters, 2010. **96**(23): p. 233509.
13. Park, S., C. Floresca, U. Chowdhury, J.L. Jimenez, C. Lee, E. Beam, P. Saunier, T. Balistreri, and M.J. Kim, *Physical degradation of GaN HEMT devices under high drain bias reliability testing*. Microelectronics Reliability, 2009. **49**(5): p. 478-483.
14. Gao, F., B. Lu, L. Li, S. Kaun, J.S. Speck, C.V. Thompson, and T. Palacios, *Role of oxygen in the OFF-state degradation of AlGaIn/GaN high electron mobility transistors*. Applied Physics Letters, 2011. **99**(22): p. 223506.
15. Gao, F., D. Chen, B. Lu, H.L. Tuller, C.V. Thompson, S. Keller, U.K. Mishra, and T. Palacios, *Impact of moisture and fluorocarbon passivation on the current collapse of AlGaIn/GaN HEMTs*. IEEE Electron Device Letters, 2012. **33**(10): p. 1378-1380.
16. Gao, F., S.C. Tan, J.A. del Alamo, C.V. Thompson, and T. Palacios, *Impact of water-assisted electrochemical reactions on the OFF-state degradation of AlGaIn/GaN HEMTs*. IEEE Transactions on electron devices, 2014. **61**(2): p. 437-444.

17. Sasangka, W.A., G.J. Syaranamual, C.L. Gan, and C.V. Thompson. *Origin of physical degradation in AlGaIn/GaN on Si high electron mobility transistors under reverse bias stressing*. in *2015 IEEE International Reliability Physics Symposium*. 2015.
18. Sasangka, W.A., G.J. Syaranamual, Y. Gao, R. I Made, C.L. Gan, and C.V. Thompson, *Improved reliability of AlGaIn/GaN-on-Si high electron mobility transistors (HEMTs) with high density silicon nitride passivation*. *Microelectronics Reliability*, 2017. **76-77**: p. 287-291.
19. Syaranamual, G.J., W. Sasangka, R.I. Made, S. Arulkumaran, G. Ng, S. Foo, C.L. Gan, and C.V. Thompson, *Role of two-dimensional electron gas (2DEG) in AlGaIn/GaN high electron mobility transistor (HEMT) ON-state degradation*. *Microelectronics Reliability*, 2016. **64**: p. 589-593.
20. Rzin, M., M. Meneghini, F. Rampazzo, V.G. Zhan, D. Marcon, J. Grünenpütt, H. Jung, B. Lambert, K. Riepe, H. Blanck, A. Graff, F. Altmann, M. Simon-Najasek, D. Poppitz, G. Meneghesso, and E. Zanoni, *On-Wafer Fast Evaluation of Failure Mechanism of 0.25- μ m AlGaIn/GaN HEMTs: Evidence of Sidewall Indiffusion*. *IEEE Transactions on Electron Devices*, 2020. **67**(7): p. 2765-2770.
21. Kotani, J., T. Hashizume, and H. Hasegawa, *Analysis and control of excess leakage currents in nitride-based Schottky diodes based on thin surface barrier model*. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, 2004. **22**(4): p. 2179-2189.
22. Meneghini, M., M. Bertin, G. Dal Santo, A. Stocco, A. Chini, D. Marcon, P. Malinowski, G. Mura, E. Musu, and M. Vanzi. *A novel degradation mechanism of AlGaIn/GaN/Silicon heterostructures related to the generation of interface traps*. in *2012 International Electron Devices Meeting*. 2012. IEEE.
23. Marcon, D., J. Viaene, P. Favia, H. Bender, X. Kang, S. Lenci, S. Stoffels, and S. Decoutere. *Reliability of AlGaIn/GaN HEMTs: Permanent leakage current increase and output current drop*. in *Physical and Failure Analysis of Integrated Circuits (IPFA), 2013 20th IEEE International Symposium on the*. 2013. IEEE.
24. Marcon, D., T. Kauerauf, F. Medjdoub, J. Das, M.V. Hove, P. Srivastava, K. Cheng, M. Leys, R. Mertens, S. Decoutere, G. Meneghesso, E. Zanoni, and G. Borghs. *A comprehensive reliability investigation of the voltage-, temperature- and device geometry-*

dependence of the gate degradation on state-of-the-art GaN-on-Si HEMTs. in *2010 International Electron Devices Meeting*. 2010.

25. Meneghini, M., A. Stocco, M. Bertin, N. Ronchi, A. Chini, D. Marcon, G. Meneghesso, and E. Zanoni. *Electroluminescence analysis of time-dependent reverse-bias degradation of HEMTs: A complete model.* in *2011 International Electron Devices Meeting*. 2011.

26. Christiansen, B.D., E.R. Heller, R.A. Coutu, R. Vetury, and J.B. Shealy, *A very robust AlGaIn/GaN HEMT technology to high forward gate bias and current.* Active and Passive Electronic Components, 2012. **2012**.

27. Marcon, D., X. Kang, J. Viaene, M. Van Hove, P. Srivastava, S. Decoutere, R. Mertens, and G. Borghs, *GaN-based HEMTs tested under high temperature storage test.* Microelectronics Reliability, 2011. **51**(9-11): p. 1717-1720.

28. Lumbantoruan, F., C.H. Wu, X.X. Zheng, S.K. Singh, C.F. Dee, B.Y. Majlis, and E.Y. Chang, *Analysis of Leakage Current Mechanism for Ni/Au Schottky Contact on InAlGaIn/GaN HEMT.* physica status solidi (a), 2018. **215**(11): p. 1700741.

29. Turuvekere, S., N. Karumuri, A.A. Rahman, A. Bhattacharya, A. DasGupta, and N. DasGupta, *Gate leakage mechanisms in AlGaIn/GaN and AlInN/GaN HEMTs: comparison and modeling.* IEEE Transactions on electron devices, 2013. **60**(10): p. 3157-3165.

30. Rhoderick, E.H., *Metal-semiconductor contacts.* IEE Proceedings I-Solid-State and Electron Devices, 1982. **129**(1): p. 1.

31. Sze, S.M. and K.K. Ng, *Physics of semiconductor devices.* 2006: John wiley & sons.

32. Bethe, H.A., *Theory of the Boundary Layer of Crystal Rectifiers,* in *Semiconductor Devices: Pioneering Papers.* p. 387-399.

33. Padovani, F. and R. Stratton, *Field and thermionic-field emission in Schottky barriers.* Solid-State Electronics, 1966. **9**(7): p. 695-707.

34. Simmons, J.G., *Poole-Frenkel Effect and Schottky Effect in Metal-Insulator-Metal Systems.* Physical Review, 1967. **155**(3): p. 657-660.

35. Yeargan, J.R. and H.L. Taylor, *The Poole - Frenkel Effect with Compensation Present.* Journal of Applied Physics, 1968. **39**(12): p. 5600-5604.

36. Ren, J., W. Mou, L. Zhao, D. Yan, Z. Yu, G. Yang, S. Xiao, and X. Gu, *A Comprehensive Study of Reverse Current Degradation Mechanisms in Au/Ni/n-GaN Schottky Diodes*. IEEE Transactions on Electron Devices, 2017. **64**(2): p. 407-411.
37. Zhang, H., E. Miller, and E. Yu, *Analysis of leakage current mechanisms in Schottky contacts to GaN and Al_{0.25}Ga_{0.75}N / GaN grown by molecular-beam epitaxy*. Journal of Applied Physics, 2006. **99**(2): p. 023703.
38. Ghosh, S., A. Dasgupta, A.K. Dutta, Y.S. Chauhan, and S. Khandelwal, *Physics based Modeling of Gate Current including Fowler-Nordheim Tunneling in GaN HEMT*.
39. Lenzlinger, M. and E. Snow, *Fowler - Nordheim tunneling into thermally grown SiO₂*. Journal of Applied physics, 1969. **40**(1): p. 278-283.
40. Weinberg, Z., *On tunneling in metal - oxide - silicon structures*. Journal of Applied Physics, 1982. **53**(7): p. 5052-5056.

Chapter 3

Experimental Methodology

In this chapter, the structure of the devices that were tested and the test methodology are presented first. Then, both electrical and material characterization techniques that were used to establish a comprehensive understanding of the device failure mechanisms are described. As not all device parameters can be extracted from electrical measurements or material characterization, the method used to simulate device operation to complement the experimental results is discussed.

3.1 Device structure

The AlGaN/GaN HEMTs on Si substrate were provided by our collaborator from Nanyang Technological University. As shown in Figure 3.1(a), the device is a single-finger device, with three contact pads (Gate, Source and Drain). The cross-sectional structure is shown in Figure 3.1(b). It consists of a Si substrate, followed by an AlN/GaN superlattice to reduce the number of defects during the GaN growth. A thick GaN buffer was grown by metal organic chemical vapor deposition (MOCVD) to create the bandgap discontinuity. An 18 nm $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ barrier was on top of the GaN to create the 2DEG and followed by a 2 nm GaN cap layer. The ohmic contact at the source/drain was made using Ti/Al/Ni/Au (10/120/40/50 nm) and was annealed at 825 °C for 30 s. Then, the gate was fabricated with Ni/Au (150/350 nm) using a lift-off process. Finally, the device was passivated with SiN (120 nm) by using plasma-enhanced chemical vapor deposition (PECVD) at 300 °C. Figure 3.1(c) shows a simplified band diagram of the active region.

Figure 3.1 (a) Optical image of the top view of the test device, (b) cross-sectional transmission electron microscopy image of the tested device, and (c) band diagram of the active region.

3.2 Characterization methodology

3.2.1 Electrical stressing and characterization set-up

All the electric stressing and measurements were done on a probe station with a Keithley 4200-SCS Parameter Analyzer at room temperature and ambient environment. It is critical to obtain accurate electrical data from the tests, so the system was designed to achieve low current and low noise characterization.

As the devices were provided at the die level, they were stressed and tested on a probe station. The probe station is enclosed in a metallic cage to avoid electromagnetic interference. The cage can also work as a light tight enclosure to avoid any light excitation to the devices. In order to have more precise probing, Micromanipulator 450 series vacuum-based manipulators were used to improve the system stability. These manipulators have 100 threads per inch (T.P.I) drives, which is recommended for probing larger than 1 μm geometries. Triaxial probe holders with tungsten tips were used in order to perform low current and low noise testing. The probe station is shown in Figure 3.2.

Figure 3.2 A picture of the electrical testing set-up: the probe station and Keithley 4200-SCS Parameter Analyzer.

For the electrical characterizations, a Keithley 4200-SCS Parameter Analyzer was used. Four source-measurement-units (SMU) are embedded into the system. The SMUs can source either current or voltage, and simultaneous measurements of current and voltage with high resolution (up to 0.2 $\mu\text{V}/100\text{ fA}$) can be made. Furthermore, each SMU is integrated with a voltage source, a current source, an ammeter and a voltmeter into a single unit, which provides better synchronization for I - V measurements. All the features are

essential to monitor device degradation during the testing. The Keithley 4200 system has a built-in computer that enables customized test sequences. This can reduce the time lag between different test phases, which improves the test accuracy.

The device under test (DUT) went through the stress and measurement sequence as shown in Figure 3.3. Two types of measurements, I_D - V_G and I_G - V_G , were conducted. V_G was swept from -10 V to 2 V for both measurements, while V_{DS} was set to 10 V for I_D - V_G and 0 V for I_G - V_G . The stressing conditions were $V_G = 2$ V, 2.5 V, 3 V and 4 V. The measurements were made every 10 min for devices stressed at 2 V, 5 min for 2.5 V and 3 V, and 30 sec for 4 V. Both the stressing and measurements were conducted at room temperature.

Figure 3.3 Schematic illustrating the electrical stress and test sequence. The measurement interval was 10 min for devices stressed at 2 V, 5 min for 2.5 V and 3 V, and 30 sec for 4 V.

3.2.2 Electrical Characterization Techniques

As the Schottky contact controls the ON and OFF state of HEMTs, the quality of the Schottky contact plays a key role in the device performance. To characterize the quality of the Schottky contact, both Schottky barrier height and ideality factor were extracted. There are several methods for measuring the Schottky barrier height, as discussed in ref [1]. One way is to use capacitance-voltage measurements. When applying a small AC voltage superimposed on a DC bias, the incremental charges have different signs at the metal surface and inside semiconductor. Thus, the measured change of charge as a function of the applied voltage is used to calculate the Schottky barrier height. However, as the DUTs

are HEMTs, the gate surface area is much smaller compared to conventional Schottky diode contact areas, so it is difficult to achieve capacitance measurements.

A second way to measure the barrier height is called photoelectric method, which is an accurate and direct method [2]. When monochromatic light is incident on a metal surface, electron-hole pairs may be generated due to the excitation. When electron-hole pairs recombine, a photo current is generated. The photo current (photoresponse R) varies with the incident light wavelength. By extrapolating the square root of the photo current versus the incident light energy, the barrier height can be calculated when the photocurrent reduces to zero, as shown in Equation 3.1,

$$R \propto (h\nu - h\nu_0)^2, \quad \text{Equation 3.1}$$

where h is the Planck's constant, $h\nu$ is the photon energy of the incident light and the $h\nu_0$ is the barrier height from the Fermin level.

However, same as for the capacitance method, not every type of the device can be measured using this method. For the photoelectric method, the metal film should be thin enough that incident light can penetrate to the interface. It is reported that the metal layer (e.g. Ni, W) generally cannot be thicker than 100 nm [3]. For our devices, the gate metal is very thick, which makes it impossible to extract barrier heights using photoelectric measurements.

The third method determine barrier heights is using current-voltage measurements, which is the easiest way the calculate barrier height. For non-heavily doped semiconductors, the I-V characteristics in the forward direction are given by (for $V > 3kT/q$) :

$$J = A^{**}T^2 \exp\left(-\frac{q\phi_B}{k_B T}\right) \exp\left(\frac{q(\Delta\phi + V)}{k_B T}\right), \quad \text{Equation 3.2}$$

where A^{**} is the effective Richardson constant, T is the temperature, q is the electron charge, ϕ_B is the Schottky barrier height, k_B is the Boltzmann constant, $\Delta\phi$ is the barrier lowering due to image-forces and V is the applied voltage across the barrier.

As A^{**} and $\Delta\phi$ are only weakly dependent on the applied voltage, Equation 3.2 be simplified as:

$$J = J_0 \exp\left(\frac{qV}{\eta k_B T}\right), \quad \text{Equation 3.3}$$

where η can be calculated :

$$\eta = \frac{qV}{k_B T} \frac{dV}{d(\ln J)}. \quad \text{Equation 3.4}$$

By extrapolating the forward current density to 0 V on a semi-log plot, the intercept with the current density axis is the saturation current J_0 . The barrier height can be calculated from Equation 3.5:

$$\phi_B = \frac{k_B T}{q} \ln\left(\frac{A^{**} T^2}{J_0}\right). \quad \text{Equation 3.5}$$

3.2.3 Fault localization

As the leakage current is increased during the stressing, it is important to locate the degraded region to understand the physical failure mechanism. According to ref [4], there was not much degradation on the drain saturation current and therefore the failure mechanism may not be related to electrochemical oxidation. Thus, device degradation is expected in the gate Schottky contact region, although no damage was observed either from optical microscope or scanning electron microscopy. The high leakage current observed may induce heating or by electron tunneling, and in both cases, it can generate infrared light from the gate contact. Thus, a photon emission microscope (PEM) can be used to localize the high leakage path along the gate.

PEM is a common technique for failure analysis in a non-destructive way. Photoemission is caused by radiative emission of excited electrons. When an electron transits from a higher energy state to a lower energy state, an electromagnetic wave might be emitted. There are three types of radiative emission, as shown in Figure 3.4 [5, 6]. The first type is called

interband emission, which is caused by the intrinsic band-to-band recombination. The emission energy is close to the bandgap or higher than the bandgap due to hot electrons or holes. The second group involves the electron transiting to or from energy levels inside the band gap. These energy levels are from chemical impurities or physical defects inside the material. As the emission comes from an energy level inside the bandgap, the emission wavelength is longer than the first type. The last group is intraband emission induced by hot electrons or hot holes.

Figure 3.4 Three different types of radiative emission in semiconductors [5].

Several groups have reported that high-leakage semiconductor devices can emit light signals [7-9]. Conventionally, Si CCD detectors have often been used for PEM. However, these can only detect the range of wavelengths within the Si bandgap, and cannot be used to detect intraband emissions. Thus, in order to provide a more comprehensive analysis, CCD detectors with different materials have been introduced to PEM systems. Now, it is possible to implement different detectors to capture signals in different wavelength ranges, as shown in Figure 3.5 [5].

Figure 3.5 The quantum efficiency versus wavelength with Si, InGaAs and MCT (mercury cadmium telluride) detectors [5].

A typical schematic of a PEM is shown in Figure 3.6 [10]. The system consists of a basic microscope with near infrared (NIR) objective lenses and a NIR detector. The DUT is mounted directly under the microscope. First, an optical image of the device is taken. Then, the NIR background signal is captured by shutting down all other light sources and leaving the sample unbiased. After this step, the device is biased and the NIR image is taken. In this procedure, it is insured that all the NIR signals generated from the test sample are detected. Finally, the NIR image is overlaid with the optical image, so that the failure region can be identified.

In this thesis, a SEMICAPS Scanning Optical Microscope System 1100 was employed for initial fault localization. This system includes an InGaAs camera and a Yokogawa GS610 source measurement unit. During the test, DUTs were biased at $V_{DS} = 0$ V with a negative bias on the gate. The DUTs were tested on a chuck at room temperature, which is similar to the testing condition in the probe stations. Due to the increase in leakage current, there might be a high leakage path along the gate region which could emit NIR signals. In order to capture the NIR signals with low noise, during operation, the InGaAs camera was cooled

down to 230 K to achieve a higher signal-to-noise ratio. The InGaAs camera was able to collect the light emission with wavelength from 900 nm to 1400 nm. However, as no spectrometer was integrated with this system, no spectral information from the emitted NIR was captured. The final NIR image obtained was integrated from all the NIR signals between 900 nm to 1400 nm.

Figure 3.6 A schematic structure of a PEM system [10].

3.2.4 Preparation of TEM lamellae

In order to further investigate physical degradation, a focused-ion beam (FIB) was used for transmission electron microscope (TEM) cross-sectional sample preparation. To prepare the TEM sample, an FEI Nova NanoLab 600i DualBeam system was used. Unlike more traditional processes, FIBs can be used to cut TEM samples with high precision locations. The Nova NanoLab 600i has both an e-beam and an ion-beam, which is ideal for sample preparation. The basic FIB system consists of a vacuum system, a working chamber, a liquid metal source, an ion column, a sample stage, imaging detectors, a gas delivery system and a workstation to run the system. Figure 3.7 shows the FEI Nova NanoLab 600i DualBeam system. In the following paragraphs, structure details of the liquid metal source,

ion column and gas delivery system will be discussed, as they are the critical parts for the sample preparation.

Figure 3.7 Image of FIB system.

The structure of a FIB column is shown in Figure 3.8. The ion beam is produced from a liquid metal ion source (LMIS). The LMIS is able to provide an ion beam with ~ 5 nm in diameter. Gallium is the most common material for LMIS, because it has a low melting point, low volatility at melting point, low surface free energy, low vapor pressure, good electrical properties, and excellent emission characteristics [11]. By applying a large electric field, liquid Ga first forms a point source in the Taylor cone shape. Then, once the cone tip is small enough, the field can pull the Ga from the tip and ionize it at the end of the Taylor cone.

When a Ga^+ ion is extracted from the tip, it is accelerated through the FIB ion column with an accelerating energy between 5 to 50 KeV. After the ion beam is refined through the spray aperture, it goes through several lenses to reduce distortion. The first lens is the condenser lens, which is used for probe forming. The octopole is used for alignment and

stigmation correction. By applying different apertures, the beam probe size and current are varied for different applications. The beam current ranges from a few pA to 30 nA. A blanking system is utilized to avoid any unwanted damage to the sample. The lower octopole's purpose is for raster scanning the beam over the sample. The second lens is the objective lens, which is used to focus the beam to obtain the best resolution for imaging. MCP stands for multichannel plate, which is to collect secondary particles (either electrons or ions) to image the sample.

Figure 3.8 The structure of a FIB column [12].

The gas delivery system in the FIB is for delivering different gases to the sample surface, and with the ion beam, this allows ion-induced depositions of metals or insulators on the sample surface. A schematic of the process is shown in Figure 3.9. The reaction principle is similar to laser-induced chemical vapor deposition. The gas precursor is introduced near the region of interest using an inlet capillary. Then, the gas is absorbed on the sample surface, but decomposed only where the ion beam has bombarded. By repeating this process, a film can be built up. In order to have a successful deposition, the gas precursor must have high sticking probability in order to stick on the sample surface, and it must have a faster decomposition rate than its sputtering rate. In this thesis, Pt was used to deposit on top of the sample surface before TEM sample preparation. This step is used to prevent damage of the sample surface while milling with the ion beam.

Figure 3.9 Schematic of the material deposition process in FIB using the gas delivery system [12].

Milling is an important use of an FIB system, and it is the main process during TEM sample preparation. The principle of milling is to remove sample materials by sputtering. As the sample surface is scanned using a high-current ion beam of ions with sufficient energy, the sample below the surface can be damaged during the milling process. That is why before the milling is started, the gas delivery system is used to deposit a protection layer.

In the following paragraphs, the procedure for TEM sample preparation is discussed. There are mainly two types of techniques used to prepare samples using an FIB system: pre-

thinning [13] and lift-out [14]. The pre-thinning method uses a conventional mechanical method to cut small samples from large wafers, and the sample is thinned down to 10-50 μm thick using mechanical polishing. Then the thinned sample is placed into the FIB system for further thinning using ion milling. The mechanical pre-thinning technique damages the full wafer, which is undesirable when there are multiple regions of interest in the same wafer.

The lift-out method, only damages locations near to the milling regions. In this project, the lift-out approach was employed, as there are multiple devices on the same wafer and each device may have multiple locations that need to be analyzed under TEM.

There are no special requirements for the lift-out technique as long as the sample can be fitted inside the FIB chamber. For insulating materials, it is recommended that the sample be pre-coated with carbon or metal to prevent charging issues [15]. The procedure for the FIB lift-out process is illustrated in Figure 3.10. First, the region of interest is covered with a protective metal layer about 2 μm thick (usually W, Pt or C). A metal line is deposited at low beam current at the beginning to avoid any damage to the sample surface. Then, a large stair-step trench is removed by milling from one side of the region of interest and a rectangular trench is milled on the other side. The purpose for making a stair-step trench is to have a window to separate the area of interest from the bulk sample. After this, the sample is tilted to 52° with respect to the ion beam, and the bottom and left side and a portion of the right side is cut using the FIB. A micromanipulator probe is then inserted and bonded with the region of interest with deposited Pt or W. After the bonding, the remaining right side of the sample is cut completely and the area of interest is separated from the bulk sample. Then, the sample is lifted out using the micromanipulator and mounted on a special sample holder. Finally, the sample is further thinned to a thickness of about 100 nm for viewing in a TEM.

Figure 3.10 Schematic of the lift-out TEM sample preparation technique [11].

During the milling or deposition for sample preparation, high energy Ga^+ ions (30 keV in most commercial FIB systems) interact with the specimen [16]. As a result, the ion beam induces surface damage, such as amorphization [17]. It has been reported that the thickness of the amorphous layer is nearly proportional to the energy of the Ga^+ ions [18]. Thus, to avoid amorphization, low energy clean-up is essential for TEM sample preparation. With the low keV cleaning technique, both the quantity and the depth of penetration of Ga are dramatically diminished [19]. So, the final step of the sample preparation is cleaning the sample at 2 keV for both sides of the TEM lamellae.

For the FIB sample preparation, the samples were unlikely to be damaged by the Ga^+ ion as during the final stage of milling, only a small current was used. Furthermore, during the failure analysis, both fresh and stressed samples were prepared by the same technique with the same parameters. All these help to ensure that the different features observed between fresh and stressed samples likely originated from the electrical stressing, and not from the sample preparation.

3.2.5 Material characterizations

TEM is a microscope that allows observation of materials at the nanometer scale. From the device structure shown in Figure 3.1(b), the active device regions are in the nanometer scale regime, thus TEM is essential to examine any physical changes in those regions. Unlike conventional optical microscopes, TEM uses electrons rather than visible light as a source. The resolution of optical microscopes is limited by the wavelength of visible light. As electrons have wave-like characteristics, TEM uses electrons to ‘see’ the sample structures. An electron’s wavelength is related to its energy through de Broglie’s equation:

$$\lambda_e = h/m_e v_e, \quad \text{Equation 3.6}$$

where λ is the electron’s wavelength, h is the Planck’s constant, m is the mass of the electron and v is the velocity of the electron.

Therefore, with higher energy, electrons have shorter wavelengths and the electron microscope will have higher resolution. As high energy electron beam can damage specimens and TEMs that can operate under intermediate accelerating voltages (200-400 kV) are now available; and with advanced spherical-aberration correction, the resolution of a TEM can be below 0.1 nm.

Electrons are a form of ionizing radiation that interacts with specimens. This interaction can generate a variety of different signals from specimens, which give a wide range of information about the specimens. Signals generated from a high energy electron beam’s interaction with a material are illustrated in Figure 3.11.

A TEM collects the electrons that do not deviate far away from the incident beam. Depending on how the electrons are collected, TEM works in different modes, which give a variety of internal structural information about the specimens. Furthermore, by incorporating different kinds of spectrometers into a TEM system, a more comprehensive chemical analysis is achievable. In this dissertation, several types of imaging modes were employed to obtain different structural information in the specimens. Energy-dispersive x-

ray spectroscopy (EDX) and electron energy loss spectroscopy (EELS) were carried out in order to analyze the chemical composition (especially for light elements) in the samples. The details of these techniques will be discussed in the following paragraphs.

Figure 3.11 Different secondary signals generated from a high energy electron beam that interacts with a thin specimen [20].

One of the TEM image modes is High-Angle Annular Dark Field (HAADF) under Scanning TEM (STEM) mode. It analyses inelastically scattered electrons or thermal diffuse scattering from a specimen with a high angle annular dark field (ADF) detector [21]. This technique is highly sensitive to the atomic number of elements within a specimen which produces much clearer Z-contrast images. The HAADF technique was first proposed by Humphreys *et al.* when they found that the contrast from single atoms could be increased when the inner angle of the ADF detector was placed to higher angle [22]. This is because at lower angles, coherent Bragg beams are collected by an ADF detector and the beam signal is not related to the specimen's atomic number directly [23]. By increasing the inner angle, an ADF detector only collects incoherent scattering rather than Bragg beams [24]. Figure 3.12 shows the geometry of a HAADF detector. The detector collects scattered electrons over a few tens of milliradians up to several hundreds of milliradians from the

center. The collected signals in the detector are recorded as a function of the position of the illuminating beam.

Figure 3.12 The schematic of HAADF-STEM [21].

As at higher angles, Rutherford scattering from nuclei dominates and the signal intensity varies approximately as the square of atomic number [25]. The detector only collects scattered electrons, so the vacuum region gives a black image and the higher atomic number gives a brighter image [26]. Furthermore, an ADF detector detects incoherent signals, which produces incoherent images. Incoherent images provide the most direct information about the specimen's structure with high resolution. Figure 3.13 shows the ADF detector intensity for two-point objects (P1 and P2) due to illumination by coherent and incoherent light. From Figure 3.13, there is a clear dip between the two points for incoherent illumination. This means the two objects can be resolved and the minimum distance is much shorter than the coherent illumination (in phase). For the out of phase coherent illumination, although the image resolution is even better than the incoherent one, it is difficult to achieve in real-world applications. Thus, collecting incoherent signals is a practical way to improve resolution. Moreover, in the incoherent image, there is no specific

phase relationship from the source, so the interference effect of electrons does not affect the imaging, which gives a much more straightforward interpretation.

Figure 3.13 Image intensities for two points taken from coherent illumination and incoherent illumination [25].

3.2.6 Chemical analysis

As HAADF mode gives high-contrast and chemically sensitive images, it is possible to distinguish different elements in an image. In order to have a more comprehensive understanding of a device, EDX and EELS are conducted to obtain chemical information. By combining EDX or EELS with STEM technique, high resolution material characterization could be achieved.

EDX is a chemical analytical technique. The EDX system bombards the specimen with an electron beam. This excites the inner shell electrons and creates X-ray spectra that contain elemental information about the specimen [27]. Originally, the analysis of the X-ray spectra was implemented to examine bulk samples with limited spatial resolution (about a few micrometers). Furthermore, the spatial resolution was reduced with the increase in incident electron energy needed for bulk samples, because the penetration and spreading of the electrons is increased and the larger excited region gives lower spatial resolution. Better

resolution is achievable by replacing bulk samples with thinner samples, as show in Figure 3.14. In thin specimens, the spreading of the electrons is diminished and the spatial resolution mainly depends on the incident electron probe size.

Figure 3.14 Comparison between the excited volume for bulk (from electron probe micro analyzer (EPMA) or SEM) and thin samples (from Analytical electron microscopy (AEM)) [20, 28].

According to the Bohr model, an atom consists of a high density positive charge nucleus surrounded by negatively charged electrons. With an increase of the atomic number (proton number), electrons occupy the surrounding orbits from the lowest energy upward. The orbital energy mainly depends on the principal quantum number ($n = 1, 2, 3, \dots$). The smallest orbital is the K shell, followed by L shell and M shell, etc. It is assumed that there is no radiation and energy loss when the electron travels within the same orbit. However, when electrons jump from one orbit to another, they gain or lose energy by absorbing or emitting electromagnetic radiation with a certain energy (frequency). The energy gain or loss is related to the energy difference between the two different orbits.

As the outer orbit has higher energy, electrons lose their energy during the migration to the inner shell. The energy loss from electrons creates X-rays. In the steady state, all the inner shell orbits should be fully occupied, so that there are no vacant states for the outer shell

electrons to jump into in the inner shells. An electron vacancy must be created in order to make provide a place for outer electrons jump into. In TEM, this vacancy is created by high energy electron bombardment.

The X-ray emitted has the energy that is characteristic between the difference in energy of the two different orbits, which is also unique for different elements. As there are several orbits in most atoms, the X-rays may have different energies. The X-ray are mainly named by a Roman letter indicating the shell which contains the electron vacancy, a Greek letter referring to the change in quantum number ($\alpha = 1$, $\beta = 2$, etc.) and a number specifying the intensity of the line within the same shell group with a descending order (1, 2, etc.). Figure 3.15 shows a sketch of different X-rays that are generated from different orbits.

Figure 3.15 A sketch of characteristic X-rays generated by transitions between different orbits [29].

From Figure 3.15, every element is capable of $K\alpha$ emission. With the increase of atomic number, electrons can occupy M shells, which enable to emit $K\beta$ and $L\alpha$ emission in higher energy ranges.

Figure 3.16 shows a typical X-ray spectrum from a TEM thin sample which is NiO deposited on a carbon film and mounted on a Mo grid. This figure shows peaks associated with the emission processes described above and illustrated in Figure 3.15. For Carbon and Oxygen, elements with small atomic numbers, only $K\alpha$ lines are found in the spectrum. However, for heavier elements, such as Nickel and Molybdenum, $K\beta$ lines and $L\alpha$ lines were observed during the characterization. Furthermore, for higher atomic number elements, more than one X-ray energy was detected. This is important if the specimen has multiple different elements and these elements have some overlapping characteristic X-rays. Under this condition, the non-overlapping X-ray lines can be used to analyze the specimen. In the spectrum there are an Iron peak and several Molybdenum peaks which come from the surrounding environment (e.g. the objective-lens pole pieces and sample support grid, respectively) [30].

Figure 3.16 X-ray emission spectrum of a thin film NiO TEM sample on a Mo holder [30].

In addition to EDX, EELS is also a powerful technique for analytical electron microscopy to obtain chemical information from a specimen. Unlike EDX which collects emitted X-rays from the specimen, the EELS technique is based on analysis of the energy distribution of electrons passing through a specimen, which is shown in Figure 3.17. This energy distribution is related to the material properties of a sample, such as the type of elements present, the quantity of each element, and the bonding states of the atoms.

Figure 3.17 Comparison between EDX (XEDS) and EELS signals [20, 28].

When incident electrons pass through a thin specimen, some of the electrons interact with the atoms. However, majority of the electrons are transmitted without losing any energy, while a portion are scattered inelastically and lose energy from the scattering event. As mentioned in the previous paragraph, this event excites the atoms inner-shell electrons to outer shell, and then an electromagnetic wave is emitted (e.g. X-rays) when excited electrons return to lower energy states. These interactions with atoms cause an energy loss of the scattered incident electron beam, which can be detected using a spectrometer. Compared to EDX, the EELS technique is more sensitive to light elements. This is because the X-ray fluorescence decreases dramatically with the atomic number and the EELS detector efficiency (20-50%) is higher than the EDX detector (10%) [31, 32]. Furthermore,

EELS provides the binding information of the specimen, which gives a much deeper chemical analysis.

A schematic of the EELS setup incorporated within a TEM is shown in Figure 3.18 [33]. Electrons are accelerated through the TEM and strike the sample. As the EELS signals are generated below the specimen, the spectrometer is located in the post-column after the viewing screen using a magnetic prism to disperse electrons onto the detector. A spectrum consisting of electron intensity versus electron energy loss is recorded in the camera [20].

Figure 3.18 Schematic of EELS setup [34-36].

As shown in Figure 3.18, an imaging filter detector is located under the TEM viewing screen. The primary goal of the imaging filter is to split different electron energies after passing through the magnetic prism. As the imaging filter is connected to the TEM directly, it works as a lens as well, which is aimed to focus each energy component beam to avoid aberration [34]. The imaging filter has several entrance apertures which determine how many electron beams can pass through for the EELS analysis. The smaller aperture (2.5 mm for Quantum system) can remove the electrons that contribute to small residual aberrations to better energy resolution for EELS [35].

The magnetic prism is used to disperse the electrons according to their different energies. Inside the prism, a magnetic field is perpendicular to the incident electron beam and bends the incident electrons 90°. Under a magnetic field $\vec{B}$, an electron traveling at a speed $\vec{v}$ travels in a circular orbit with radius R , as shown in Equation 3.7

$$R = \left(\frac{\gamma m_0}{eB} \right) v, \quad \text{Equation 3.7}$$

where $\gamma = 1/(1 - v^2/c^2)^{1/2}$ is a relativistic factor, c is the speed of light and m_0 is the rest mass of an electron [31]. As different electron energy losses lead to different electron velocities, the circular orbits of the electrons are different with different energies. Most of electrons do not undergo inelastic scattering. They are called zero-loss electrons which have the highest energy. The zero-loss electrons, which are shown as the brightest spot from the EELS spectrum in Figure 3.18, are bent the least in the prism and appear at the bottom of the dispersion plane. The core-loss electrons lose the most energy, so they are bent most and appear in the top of the energy distribution plane.

In addition to bending and dispersing electron beams, the prism can also work as a lens to focus the electron beams at the plane of the energy selection slit [35]. The energy slit filters the pre-selected electron energy loss range to create Energy-Filtered TEM (EFTEM) images. During the operation of EELS, the energy slit is fully retracted. After passing through the slit, electrons are projected to a spectrum at the dispersion plane of the GIF detector. Between the slit and GIF detector, there are multipole lenses which automatically

correct the image magnification and higher order distortions. Furthermore, they can also correct chromatic aberration induced by the magnetic prism.

When an electron strikes the detector, the phosphor emits a pulse of light. Then the optical stack captures the light and the light propagates immediately to the nearby CCD array. This technique allows the light pulses to be captured with limited spreading, which ensures the spectrum has a high energy resolution [35].

The EELS spectrum data is recorded as a function of scanning position. In the Gatan system, a method called spectrum imaging stores spatially resolved energy loss distribution data. For EELS mapping, it generates a three-dimensional data structure where two dimensions are used to store spatial information for the EELS scan and the third one records the corresponding energy loss spectrum. For an EELS line scan, two-dimensional data is generated with one spatial dimension and spectrum information. The key advantage of the spectrum imaging is the convenience for data processing. Having spectrum information at each spatial data point ensures a completely quantitative compositional or chemical analysis [36].

A typical EELS spectrum is shown in Figure 3.19 [37]. As most electrons go through a specimen without loss of energy, the zero-loss peak has the strongest signal and then the CCD signal has an exponential decay with the energy loss. The low-loss region (<50 eV) provides information about the band structure of a material. There is a peak close to zero-loss signal. This peak represents plasma resonance from the atoms. In the higher loss region, the spectrum has characteristic signals (named “ionization edges”), that indicate the elements present in the specimen. The edge energies refer to the energy loss of an electron beam passing through the specimen [38].

Like EDX, one element may have multiple ionization edges. Thus, it is important to choose the most preferable edge to analyze. Normally, it is not suitable to use the edges below 150 eV, because these edges may overlap with the low-loss region. For the high energy range

(>2000 eV), the signals become noisier, so long exposure times are required. Once the preferred edge is determined, the edge signal is extracted from the raw spectrum [39].

Figure 3.19 A typical energy loss spectrum [37].

To extract the edge signal, the background signal is removed from the raw spectrum. Power law fitting with a further extrapolation is the most common method to estimate the background signals. First, a pre-edge fitting region is identified as the background region before the ionization edge. Then, a power law is used to fit the background area and extrapolated into the edge signal region. This is aimed to calculate the background signals under the edge signal region and extract pure edge signal from the raw spectrum. Figure 3.20 shows an example of the edge signal extraction [40]. The raw spectrum data is shown in dark green. The pre-edge region is defined as the background fitting region which is shown in red. The background signal is fitted and extrapolated along the x-axis. The light green is the extracted edge signal, which can be used for quantitative analysis. In addition to quantifying the chemical components of a specimen, it is possible to deduce the chemical bonding state of the sample by analyzing near edge fine structure from the edge signal, as the near edge fine structure indicates the density of unoccupied states.

Figure 3.20 An EELS spectrum of B K edge and N K edge signals [40].

3.3 Device simulation

As not all the device parameters are easily measured or even possible to measure through experiments, device simulation aids in understanding the device physics during reliability testing. In this dissertation, a Silvaco Technology Computer-Aided Design (TCAD) simulation tool was used to calculate the electric field distribution in the device. The simulator is called Atlas, which provides physically-based two-dimensional simulation for semiconductor devices.

Physically-based simulators are able to predict electrical, mechanical and thermal characteristics based on specific physical structures, models and bias conditions. The device structure is analyzed using a two-dimensional grid of points. During a simulation, grid points are used in finite element analysis of differential equations, and then transport of different carriers and other material properties are simulated. Compared to modeling based on analytic formulae, the advantage of physically-based numerical analysis simulation tools can provide a deeper insight with more physical information. In Atlas, before running a simulation, the physical structure and the electrical bias conditions of a device have to be first defined, and then the physical models are selected in the simulation input file.

Figure 3.21 shows the flow for conducting a simulation in Atlas [41]. DevEdit is an editor for structure and mesh specification for simulated devices. Athena is a process simulator, which predicts the physical structure based on the process flow. DeckBuild is an interactive tool to edit and run the simulation file. All these files are put into the Atlas simulator to conduct the simulation. There are three different outputs. The first one is runtime output which gives the progress and error/warning messages during the simulation. The second is log file, which stores the voltages and currents for all device terminals. The third one is a solution file, which has two-dimensional information of the simulated results at a given bias condition.

Figure 3.21 Simulation flow in Atlas [41].

In addition to these features, Atlas has a specific simulator for compound semiconductor devices. This specific simulator is named Blaze. In addition to the basic simulator, Blaze has a library consisting of material properties of binary, ternary and quaternary semiconductors. Furthermore, it has built-in models to solve for graded and abrupt heterojunctions, which is an ideal simulator for GaN HEMTs [42].

A few physical models were used to improve the simulation results. Auger and Schottky-Read-Hall were selected for the recombination models. Fermi-Dirac distribution was

chosen as the carrier statistic model. Albrecht model was used for calculating the electron mobility at low field. FN tunneling, PF emission and trap-assisted tunneling were implemented to achieve more accurate results for the leakage current. Polarization effect and the strain caused by lattice mismatch were also considered in the simulation.

References

1. Sze, S.M. and K.K. Ng, *Physics of semiconductor devices*. 2006: John wiley & sons.
2. Crowell, C., W. Spitzer, L. Howarth, and E. LaBate, *Attenuation length measurements of hot electrons in metal films*. Physical Review, 1962. **127**(6): p. 2006.
3. Qiao, D., L.S. Yu, S.S. Lau, J.M. Redwing, J.Y. Lin, and H.X. Jiang, *Dependence of Ni/AlGa_N Schottky barrier height on Al mole fraction*. Journal of Applied Physics, 2000. **87**(2): p. 801-804.
4. Christiansen, B.D., E.R. Heller, R.A. Coutu, R. Vetury, and J.B. Shealy, *A very robust AlGa_N/Ga_N HEMT technology to high forward gate bias and current*. Active and Passive Electronic Components, 2012. **2012**.
5. Phang, J.C.H., D.S.H. Chan, S.L. Tan, W.B. Len, K.H. Yim, L.S. Koh, C.M. Chua, and L.J. Balk. *A review of near infrared photon emission microscopy and spectroscopy*. in *Proceedings of the 12th International Symposium on the Physical and Failure Analysis of Integrated Circuits, 2005. IPFA 2005*. 2005.
6. Ivey, H., *Electroluminescence and semiconductor lasers*. IEEE Journal of Quantum Electronics, 1966. **2**(11): p. 713-726.
7. Onodera, K., K. Nishimura, and T. Furuta, *Hot-carrier luminescence in sub-quartermicrometer high-speed GaAs MESFET's*. IEEE Transactions on Electron Devices, 1999. **46**(11): p. 2170-2177.
8. Menozzi, R., M. Pavesi, M. Manfredi, C. Ghezzi, C. Lanzieri, M. Peroni, and C. Canali, *Hot electron and DX center insensitivity of Al/sub 0.25/Ga/sub 0.75/As/GaAs HFET's designed for microwave power applications*. IEEE Transactions on Electron Devices, 1998. **45**(11): p. 2261-2267.
9. Meneghini, M., A. Stocco, M. Bertin, N. Ronchi, A. Chini, D. Marcon, G. Meneghesso, and E. Zanoni. *Electroluminescence analysis of time-dependent reverse-bias*

degradation of HEMTs: A complete model. in *2011 International Electron Devices Meeting*. 2011.

10. De Wolf, I. and M. Rasras, *Spectroscopic photon emission microscopy: a unique tool for failure analysis of microelectronics devices*. Microelectronics Reliability, 2001. **41**(8): p. 1161-1169.

11. Giannuzzi, L.A., *Introduction to focused ion beams: instrumentation, theory, techniques and practice*. 2004: Springer Science & Business Media.

12. Reyntjens, S. and R. Puers, *A review of focused ion beam applications in microsystem technology*. Journal of micromechanics and microengineering, 2001. **11**(4): p. 287.

13. Walker, J.F., D.F. Moore, and J.T. Whitney, *Focused ion beam processing for microscale fabrication*. Microelectronic Engineering, 1996. **30**(1): p. 517-522.

14. Young, R., E.V. Cappellen, and P. Carleson, *Proper sample preparation improves TEM performance*. Test & Measurement World, 1999. **19**: p. 9.

15. Giannuzzi, L.A. and F.A. Stevie, *A review of focused ion beam milling techniques for TEM specimen preparation*. Micron, 1999. **30**(3): p. 197-204.

16. Kato, N.I., *Reducing focused ion beam damage to transmission electron microscopy samples*. Journal of electron microscopy, 2004. **53**(5): p. 451-458.

17. Giannuzzi, L.A., R. Geurts, and J. Ringnalda, *2 keV Ga+ FIB milling for reducing amorphous damage in silicon*. Microscopy and Microanalysis, 2005. **11**(S02): p. 828-829.

18. Mayer, J., L.A. Giannuzzi, T. Kamino, and J. Michael, *TEM sample preparation and FIB-induced damage*. MRS bulletin, 2007. **32**(5): p. 400-407.

19. Thompson, K., B. Gorman, D. Larson, B. van Leer, and L. Hong, *Minimization of Ga induced FIB damage using low energy clean-up*. Microscopy and Microanalysis, 2006. **12**(S02): p. 1736-1737.

20. Williams, D.B. and C.B. Carter, *Transmission Electron Microscopy: A Textbook for Materials Science*. Vol. 2. 2009: Springer Science & Business Media.

21. JEOL. *high-angle annular dark-field scanning transmission electron microscopy*. 2019; Available from: https://www.jeol.co.jp/en/words/emterms/search_result.html?keyword=HAADF-STEM.

22. Humphreys, C., R. Sandstrom, and J. Spencer, *Contrast enhancement from single atoms and from crystals using energy analysis*. Scanning Electron Microsc, 1973: p. 233-241.
23. Donald, A.M. and A.J. Craven, *A study of grain boundary segregation in Cu-Bi alloys using STEM*. Philosophical Magazine A, 1979. **39**(1): p. 1-11.
24. Treacy, M.M.J., A. Howie, and C.J. Wilson, *Z contrast of platinum and palladium catalysts*. Philosophical Magazine A, 1978. **38**(5): p. 569-585.
25. Pennycook, S., *Scanning Transmission Electron Microscopy: Z-Contrast Imaging*, in *Characterization of Materials*. 2012.
26. Nellist, P. and S. Pennycook, *The principles and interpretation of annular dark-field Z-contrast imaging*, in *Advances in imaging and electron physics*. 2000, Elsevier. p. 147-203.
27. *Energy-dispersive X-ray spectroscopy*. 2019; Available from: https://en.wikipedia.org/wiki/Energy-dispersive_X-ray_spectroscopy.
28. Pennycook, S.J. and P.D. Nellist, *Scanning transmission electron microscopy: imaging and analysis*. 2011: Springer Science & Business Media.
29. AMETEK, *X-Ray Fluorescence (XRF): Understanding Characteristic X-Rays*.
30. Egerton, R.F., *Physical principles of electron microscopy*. 2005: Springer.
31. Egerton, R.F., *Electron energy-loss spectroscopy in the electron microscope*. 2011: Springer Science & Business Media.
32. Krause, M.O. and J.H. Oliver, *Natural widths of atomic K and L levels, K α X - ray lines and several KLL Auger lines*. Journal of Physical and Chemical Reference Data, 1979. **8**(2): p. 329-338.
33. Gatan. *EELS info -- Overview*. 2019; Available from: <https://www.eels.info/products/overview>.
34. Gatan. *TEM-GIF intergration* 2019; Available from: <https://www.eels.info/products/tem-gif-integration>.
35. Gatan. *Gatan imaging filter (GIF)*. 2019; Available from: <https://www.eels.info/products/gatan-imaging-filter-gif>.
36. Gatan. *Spectrum Imaging*. 2019; Available from: <https://www.eels.info/about/techniques/spectrum-imaging>.

37. Gatan. *What is EELS?* 2019; Available from: <http://www.eels.info/about/overview>.
38. Hofer, F., F.P. Schmidt, W. Grogger, and G. Kothleitner, *Fundamentals of electron energy-loss spectroscopy*. IOP Conference Series: Materials Science and Engineering, 2016. **109**: p. 012007.
39. Gatan. *Choose suitable edges for quantification*. 2019; Available from: <http://www.eels.info/how/quantification/workflow/choose-suitable-edges-quantification>.
40. Gatan. *Quantify elements within sample*. 2019; Available from: <http://www.eels.info/uses/quantify-elements-within-sample>.
41. Silvaco, *ATLAS User's Manual*. 2019.
42. Silvaco, *2D Device Simulator for Advanced Materials*. 2019.

Chapter 4

Electrical characterizations of unstressed AlGaIn/GaN high electron mobility transistors (HEMTs)

In this chapter, electrical characterizations of unstressed AlGaIn/GaN HEMTs is described. Schottky barrier height, ideality factor and other electrical parameters were extracted from I - V measurements. By combining temperature dependent I_G - V_G measurements and TCAD (Technology Computer-Aided Design) simulations, the mechanism of electron transport in the device was revealed. These parameters are important to provide an indication of the expected performance of pristine devices and to determine the failure criterion for stressed devices.

4.1 Introduction

In this chapter, extraction of electrical parameters of unstressed devices before reliability testing is described. Then, investigations of different electron transport mechanisms are also described, to develop a clear understanding of the behavior and performance of unstressed devices. The implementation of Silvaco TCAD simulations to assist in the electron transport analysis is then discussed.

Extracting the electrical parameters, such as Schottky barrier height and ideality factor, this allows investigation and benchmarking of the performance of pristine devices. A full understanding the initial electrical properties is required for setting of failure criterion and determination of failure modes of stressed devices.

The electron transport mechanisms of unstressed devices may vary depending on the device structure and fabrication process. Several groups have reported the transport mechanisms of fresh devices. In general, thermionic emission controls the forward current while Poole-Frenkel (PF) emission or the Fowler-Nordheim (FN) tunneling mechanism dominates in the reverse bias regime [1-3].

4.2 Electrical Measurement Details

Electrical measurements were conducted to characterize the unstressed devices. The details of the electrical characterizations are shown in Table 4.1. The devices were first tested on a probe station and measured at room temperature using the Keithley 4200. Two types of electrical measurements, I_D - V_G and I_G - V_G characterization, were conducted to investigate the initial performance. During the measurement, the gate voltage was swept from -10 to 2 V. V_{DS} was set to 10 V for I_D - V_G measurements and 0 V for I_G - V_G measurements. η , ϕ_B and I_{G-leak} were extracted from I_G - V_G measurements. These three parameters are commonly used to characterize the quality of a Schottky contact. In addition, I_{D-sat} , I_{D-leak} and V_{th} were extracted from I_D - V_G measurements. These parameters were chosen to check whether the initial performance of the device is within the specifications. Furthermore, based on the Joint Electron Device Engineering Council (JEDEC) standard, these are essential to understand HEMTs reliability [4].

The temperature dependent I - V measurement (I_G - V_G - T) was introduced to determine the electron transport mechanisms of fresh devices. The measurements were conducted at 5 different temperatures from 25°C to 150°C with 25°C intervals. To determine the transport mechanisms, electrical field is an important parameter needed for the analysis. However, as the HEMTs have a limited active area, it is difficult to extract electrical field using voltage-capacitance measurements. Thus, the electrical field was calculated using TCAD simulations.

Table 4.1 Electrical measurement parameters for I_G - V_G and I_D - V_G at 5 different temperatures

Measurements	V_G (V)	V_{DS} (V)	Temperature (°C)
I_G - V_G	-10 to 2	0	25
I_D - V_G	-10 to 2	10	25
I_G - V_G - T	-10 to 2	0	25, 50, 75, 100, 125, 150

Device simulations using the Blaze simulator in Silvaco TCAD were performed to reveal the electron transport mechanisms of the devices. The simulated electrical characteristic was compared with the experimental results (I_G - V_G and I_D - V_G measurements) to validate that the simulation model was correct. Then, the electric field was calculated to help understand the electron transport under reverse bias and the device degradation during forward gate bias stressing (which will be discussed in chapter 6).

The parameters used in the simulated structure are shown in Table 4.2. The gate length was set as 2 μm and the gate to source and gate to drain distances were set at 2 μm . The Al percentage in AlGaIn was set at 26%, which was the same as the actual DUTs and the thickness was set as 18 nm. The gate metal was Nickel, so the metal work function of the gate metal was 5 eV. The 2 nm-thick GaN cap serves to screen current collapse-related traps [5]. Thus, to simplify the simulation, no GaN cap and no collapse-related traps were introduced in the simulation. The GaN buffer thickness was set at 1 μm and the Si substrate thickness was set at 15 μm . The passivation layer was chosen to be Si_3N_4 . As the geometry of the Si_3N_4 does not affect the electric field in the AlGaIn layer, the passivation was flat over the device and the thickness varied from 120 nm (gate region) to 0.62 μm (gate to source/drain access regions). Donor defects were added to the Si, GaN and AlGaIn layers, which may act as point defects or dislocations [6]. Acceptor traps were included near the

bottom of the GaN layer to mimic the improvement of GaN film quality from Si substrate to the device surface [7]. The polarization charge was calibrated by the 2DEG concentration, which will be further discussed in Chapter 4.4.2. The simulation code is included as appendix.

The simulated structure is shown in Figure 4.1. Figure 4.1(a) shows the overall structure with the Si substrate. Figure 4.1(b) is a zoom-in image of several top layers in Figure 4.1(a). These top layers are the critical ones for the simulation, because all the device active regions are located in these layers and electrons are mainly flowing within these layers during the device operation.

Table 4.2 Simulation parameters for HEMT structure

Parameter	Description	Expression	Unit
ϕ_{Ni}	Work function of nickel	5 [8]	eV
L_{Gate}	Gate length	2	μm
L_{GD}	Gate to drain distance	2	μm
L_{GS}	Gate to source distance	2	μm
T_{AlGaIn}	Thickness of AlGaIn	18	nm
T_{GaN}	Thickness of GaN	1	μm
T_{Si}	Thickness of Si	15	μm
Al(x)Ga(1-x)N	Al percentage	26	%

The meshing grid of Figure 4.1(b) is shown in Figure 4.2. To achieve an accurate simulation, a fine mesh was applied to the structure, especially in the active region. As shown in Figure 4.2, the meshing grid is denser at the material interfaces and contacts. The meshing distance was set to 1 nm in the vertical direction in the AlGaIn layer and the adjacent areas. The distance was 100 nm in the horizontal direction at the gate to drain access region. The rest of the regions have larger mesh sizes, as the voltage drop in those areas is small. This inhomogeneous meshing density is aimed to enhance the simulation efficiency by reducing the calculation time, without comprising the accuracy.

Figure 4.1 HEMT structure for TCAD simulations. (a) Overview of simulation structure. (b) Zoom-in view of the active region in the simulated structure.

Figure 4.2 Meshing grid of the HEMT structure and zoom in of the gate edge towards drain region. The green lines represent the meshing grids.

4.3 Results and Discussion

4.3.1 Electrical Measurement Results

Multiple devices were used for the I-V measurements, as show in Figure 4.3. There are a small number of devices (6 out of 30 devices) having initial high leakage current, which are called bad devices. The remaining of devices have a lower leakage current, and they are considered as good devices. The origin of the initial high leakage current is due to the presence of carbon impurities in the gate nickel layer. The detail of this study has been discussed in ref [9]. Only good devices with low initial leakage current will be discussed here.

Figure 4.3 $J_{\text{gate}}-V_{\text{gate}}$ of 30 fresh devices [9].

Figure 4.4 shows the I_D-V_G and I_G-V_G characteristics of 15 good fresh devices. In Figure 4.4, each dotted line represents one electrical characteristic (I_D-V_G or I_G-V_G). Data represented with different colors correspond to different devices. The drain current and the gate current were normalized to the gate width, which is 80 μm .

Figure 4.4 (a) I_D-V_G and (b) I_G-V_G characterizations of 15 fresh devices.

In Figure 4.4(a), from the I_D-V_G characteristic, the average V_{th} is $-2.55 \pm 0.30\text{V}$, and the average I_{D-sat} is $0.44 \pm 0.06\text{ A/mm}$. The device has a very similar structure as the one in ref [10] and all the electrical parameters are close to the reported values [10]. Figure 4.4(b) shows the I_G-V_G characteristic of the fresh device. In Figure 4.4, though there is variation in the $I-V$ characteristics among the devices, it is within the acceptable range and the leakage current values are below the failure threshold ($12.5\text{ }\mu\text{A/mm}$). As all the devices are from the same wafer, the variation is unlikely due to the epitaxy. On the other hand, during the device fabrication, there are many process steps that may have slight deviations, thus it is believed that the variations in $I-V$ characteristics is likely due to device fabrication processes. In the gate reverse biased region, I_{G-leak} increases dramatically from 0 V to -3 V and then reaches saturation. In the forward biased region, the gate current increases exponentially with the gate voltage, which is mainly dominated by thermionic emission. The leakage current (measured at $V_{Gate} = -8.5\text{ V}$) from I_G-V_G and I_D-V_G characterizations have similar values. This may indicate that the leakage current mainly comes from the gate contact.

Figure 4.5 shows how the saturation current density J_0 was extrapolated for a fresh device. This method has been discussed in Chapter 3.2. J_0 was determined by extrapolating the forward gate current to zero voltage. The extrapolation region is normally between 0.3 V to 0.7 V in order to reduce the measurement error and ensure the applied voltage is greater than $3kT/q$. Multiple fresh samples were characterized. The barrier heights (ϕ_B) were extracted as 0.84 ± 0.13 eV and the ideality factors (η) were determined to be 1.68 ± 0.26 .

Figure 4.5 Forward current density versus applied voltage on the gate with $V_{SD} = 0$ V. J_0 was determined by extrapolating the forward current density to zero bias.

The uniformity of the devices is defined as

$$Uniformity [\%] = \left(1 - \frac{\sigma}{\bar{x}}\right) \times 100, \quad \text{Equation 4.1}$$

where σ is the standard deviation of the measured values and the $\bar{x}$ is the average of the measured values [11]. Based on Equation 4.1, the uniformity of the I_{D-sat} is higher than 80%,

and all the other parameters (e.g. V_{th} , ϕ_B and η) have uniformities of more than 85%. Although the uniformity of I_{G-leak} and I_{D-leak} is not as high as the other parameters, the values of the leakage current are considered low compared to values determined for devices with initial high leakage currents ('bad devices') [9]. Thus, all the DUTs are considered have good uniformity.

4.3.2 Simulation Results

Figure 4.6 shows the I_D - V_G electrical characteristics from simulated and experimental results with both liner and log current density scales with $V_{DS} = 5$ V. In the figure, the experimental data is plotted in black and the simulated data is in red. The simulated drain current has a similar shape and values as the measurement in all regimes.

Figure 4.6 I_D - V_G experimental measurement (black) and Silvaco TCAD simulation with $\phi_{Ni} = 5$ eV (red) on (a) linear and (b) log current density scales.

The electrical parameters determined from I_D - V_G electrical measurements and simulations are summarized in Table 4.3. From Table 4.3, the measurement data are seen to be quite close to the simulation data. Furthermore, the 2DEG density was extracted at the middle of the gate at different biases. The V_{DS} was set 0 V to achieve a uniform distribution of the 2DEG density under the gate. The extracted 2DEG density at different gate biases is shown for the simulation results in Figure 4.7. The density of the 2DEG at zero bias is around

$8.2 \times 10^{12} \text{ cm}^{-2}$, which is close to the reported value [10]. The 2DEG concentration shows a dramatic decrease around -3 V and reaches to relatively stabled value at -4 V. This suggests that the channel is fully depleted at around -4 V, which is supported by the measurement data shown in Figure 4.6(b). Thus, it is concluded that the simulation results agree well with the experimental results.

Table 4.3 Comparisons between measurement values and simulation values

Parameter	Measurement	Simulation	Unit
$J_D@0\text{V}$	1.93×10^8	1.95×10^8	A/m ²
$J_D@-6\text{V}$	29.86	29.44	A/m ²
$n_{2\text{DEG}}$	1×10^{13} [10]	8.2×10^{12}	cm ⁻²
V_{th}	-2.52	-2.54	V

Figure 4.7 Simulated 2DEG concentration under the gate contact at different gate biases.

Values of the electric field are essential for analysis of electron transport mechanisms in the reverse bias regime (as discussed in section 2.3). However, it is difficult to calculate values from measurements in for the HEMT structure that was investigated, because the contact area is very small. Thus, the electrical field in the AlGaIn layer was simulated from $V_G = -4 \text{ V}$ to 0 V with $V_{DS} = 0 \text{ V}$. As the source and drain were grounded, the electrical field in the vertical direction was much larger than in the horizontal direction. Thus, only

the electric field in the vertical direction is plotted in Figure 4.8. As shown in Figure 4.8, the highest electric field is present in the AlGaIn layer under the gate contact.

Figure 4.8 Vertical electric field distribution from the simulations. The bias conditions were $V_G = -2$ V with $V_{DS} = 0$ V.

The vertical electrical field (y-direction) distribution along the AlGaIn layer at different gate biases is shown in Figure 4.9. The gate is located between horizontal positions 0 to 2 μm , and the rest of the length are gate to drain and gate to source access regions. As shown in Figure 4.9, the electric field is quite uniform under the gate region and is much higher than that in the access regions. This indicates the electrons are highly accelerated under the gate which contributes to the majority of reverse current. Thus, the simulated electric field under the gate contact was used for fitting with different leakage current models (e.g. PF emission, FN tunneling) to investigate the electron transport mechanisms under reverse bias.

Figure 4.9 Simulated vertical electric field distribution in the AlGaIn layer at three different gate biases.

4.3.3 Electron Transport

The results of I_G - V_G - T measurements are shown in Figure 4.10. The I_G - V_G measurements are plotted as solid lines and the different colors indicate different measurement temperatures. There are several different current regions in the I_G - V_G - T measurements, as labeled in Figure 4.10. Three regions are in the negative gate bias region. Region I is for the most negative bias to the point where 2DEG is fully depleted. In this region, the current shows a weak dependence on both voltage and temperature. Region II is between the 2DEG depletion point to V_{th} , where the current has a strong voltage dependence and weak temperature dependence. Region III is from V_{th} to the zero gate bias condition. In this region, the current shows a strong voltage and temperature dependence. The region F is when the current is under forward gate bias.

Figure 4.10 Measured J_G - V_G ($V_D = 0$ V) at different temperatures superimposed with J_D - V_G ($V_D = 10$ V). Region I is defined from -10 V to -4 V where the 2DEG is fully depleted.

In the forward bias region, current is dominated by thermionic emission. The current shows a weak temperature dependence below 1 V but then increases to show a strong temperature dependence at large forward gate bias.

For the reverse bias regions, region I is defined from the most negative bias to the point where the 2DEG is fully depleted. As shown in the J_D - V_G curve in Figure 4.10, the 2DEG is fully depleted up to about -4 V. In this region, I_{G-leak} shows very weak voltage dependence, compared to other regions. When the gate bias becomes more negative than -4 V, the AlGaIn layer becomes fully depleted, which is indicated as a grey area under the gate in Figure 4.11. The depletion region could not expand any further in the vertical direction, so the vertical leakage current should not continue to increase. As the gate voltage is further decreased, the depletion region expands from the gate edges toward the gate to source/drain access regions, shown as the grey area between the gate edges to the source/drain contacts

in Figure 4.11. The leakage current from the access regions then further contributes to the weak voltage-dependent gate current [12]. Moreover, in this region, the current shows less temperature dependence. As the majority of the current comes from vertical leakage current across the AlGaIn layer, the temperature independence behavior is associated with the vertical current. The vertical leakage mechanism will be discussed later in this section.

Figure 4.11 Depletion region and current flow of region I. The blue shadow indicates the depletion region and the red arrows represent the current flow. (This image is not down to scale).

Unlike region I, there is a strong dependence on temperature of the I - V curve in region III ($V_{th} < V_{Gate} < 0$ V). The area under the gate is not fully depleted (grey area in Figure 4.11 (c) and (d)). There is still a large portion of the 2DEG that forms at the AlGaIn/GaN interface, which is also supported by the simulation results (shown in Figure 4.6). As the device is under a relatively lower negative bias compared with regions I and II, the electric field is not high enough to induce a large vertical leakage current. The leakage current in this region is therefore likely to be dominated by the mesa sidewall current, as schematically shown in Figure 4.12. The 2DEG at the AlGaIn/GaN interface allows possible leakage paths to the gate metallization [13].

A few groups have fabricated GaN HEMTs with multiple mesa sidewalls and therefore the mesa sidewall current could be extracted. Two groups have reported that the mesa sidewall current shows a strong temperature dependence, and this is due to PF emission between the

gate-covered mesa sidewall and the 2DEG [14, 15]. During the device fabrication, the mesa surface is damaged due to the etching process. This creates electron traps on the mesa sidewall surface, which enhances PF emission.

Figure 4.12 (a) The top view of a DUT, (b) the mesa at the contact end of the gate of the device, (c) a cross-sectional schematic of the device structure along the gate at the mesa edge, (d) a cross-sectional schematic of the device structure across the gate.

In region II ($-4 \text{ V} < V_G < V_{th}$), the electric field is high enough that the leakage current via the mesa is not substantial and low enough that the horizontal leakage current (the dominant mechanism of region I) is insignificant. This region is usually used to investigate the transport mechanism of the vertical leakage current [13]. There are two possible mechanisms (FN and PF) which could contribute to vertical leakage current [1].

First, the measured data was fitted with the FN model. The current density for FN tunneling is governed by Equation 2.12. As the FN tunneling is independent of temperature, by

plotting $\ln(J_{Gate}/E_b^2)$ as a function of $1/E_b$ at different temperatures, the slopes should be independent of temperature and proportional to $\sqrt{2m_n^*(q\phi_B)^3}$. Figure 4.13 shows the plot of $\ln(J_{Gate}/E_b^2)$ versus $1/E_b$ at different temperatures, where the J_{Gate} is obtained from the I_G - V_G - T measurements and E_b is derived from the simulation results. These results show that $\ln(J_{Gate}/E_b^2)$ has a weak temperature dependent in the low temperature range (below 375 K).

Figure 4.13 The measured data fitted with to the equation for FN tunneling (Equation 2.12)) for a fresh device.

As the ϕ_B was calculated from the forward gate bias data, the m_n^* can be extracted from the slopes of the lines in Figure 4.13 [1]. The extracted m_n^* can be compared with the reference value to determine if the leakage current follows the FN mechanism. Slopes were calculated from each line to extract the effective electron mass for AlGaIn. At 300 K, the

extracted m_n^* for a fresh device is 0.18. This is within the range of the m_n^* values reported for AlGaIn, which vary from 0.18 to 0.24 [16]. Thus, FN tunneling is likely dominant in the fresh device in region II, especially at room temperature.

To further investigate the transport mechanism, the same data was fitted to the PF emission model. The current density associated with PF emission is governed by Equation 2.11. From Equation 2.11, $\ln(J_{Gate}/E_b)$ is linearly dependent on $\sqrt{E_b}$. Equation 2.11 can be rewritten as,

$$\ln\left(\frac{J_{Gate}}{E_b}\right) = \frac{q}{\xi kT} \sqrt{\frac{qE_b}{\pi\epsilon_0\epsilon_s}} - \frac{q\phi_t}{\xi kT} + \ln C = m(T)\sqrt{E_b} + b(T), \quad \text{Equation 4.2}$$

where

$$m(T) = \frac{q}{\xi kT} \sqrt{\frac{q}{\pi\epsilon_0\epsilon_s}}, \quad \text{Equation 4.3}$$

and

$$b(T) = \frac{q\phi_t}{\xi kT} + \ln C. \quad \text{Equation 4.4}$$

Figure 4.14 shows $\ln(J_{Gate}/E_b)$ versus $\sqrt{E_b}$ at different temperatures. Based on Equation 4.3 and Equation 4.4, $m(T)$ and $b(T)$ can be extracted from the slope and intercept, respectively, at each temperature in Figure 4.13, and C is a constant.

From Equation 4.3 and Equation 4.4, both $m(T)$ and $b(T)$ are expected to be linear functions of $1/T$, and ϵ_s and ϕ_t can be calculated from the slopes of m vs. $1/T$ and b vs. $1/T$ plots [1]. The value of compensation factor depends on the donor and acceptor concentrations in the AlGaIn layer. Differences in the number of donor and acceptor concentrations contribute to differences in the carrier concentrations in AlGaIn, which affects the PF current. For intrinsic AlGaIn, where N_A is close to N_D , the compensation factor is 1. When N_D is much larger than N_A , the compensation factor becomes 2. As the AlGaIn of the device tested is intrinsic, the compensation factor is assumed to be 1 for fresh devices [10].

Figure 4.14 The measured data fitted to the equation for PF emission (Equation 2.11) for a fresh device.

Figure 4.14 shows the experimental data fitted with the PF model. The data does not show a strong dependence on temperature at lower temperature (below 375 K), so the leakage current data is not consistent with the PF emission model. This can be further demonstrated by using the slopes of the lines in Figure 4.13 to determine m as a function of T (Equation 4.3). Figure 4.15 shows m plotted as a function of $1/T$. This data is expected to lie on a line with a slope given by Equation 4.3. Given that the other values in Equation 4.3 are known, the permittivity ϵ_s was determined to be 1.54, which is much lower than the reported value of 5.8 for GaN and 4.6 for AlN [1, 17, 18].

Figure 4.15 Slopes of Equation 4.3 versus temperatures to extract AlGaIn permittivity.

In summary, the reverse current has three different components:

$$I_r = I_{horizontal} + I_{vertical} + I_{mesasidewall}. \quad \text{Equation 4.5}$$

$I_{mesasidewall}$ is dominant in region III, $I_{vertical}$ dominates in region II, and $I_{horizontal}$ is the major component in region I. In addition, for a fresh device, the $I_{vertical}$ is governed by FN tunneling.

4.4 Conclusions

In this chapter, the electrical properties of unstressed AlGaIn/GaN HEMTs are discussed. Under gate forward bias, electron transport follows thermionic emission. Under reverse bias, the dominant mechanism responsible for the leakage current changes with the gate voltage. At low reverse bias voltage ($V_{th} < V_G < 0$ V), the leakage current is dominated by electron transport via the mesa sidewall by PF emission. At intermediate reverse bias

voltages ($-4 \text{ V} < V_G < V_{th}$), the leakage current is dominated by FN tunneling. Finally, at high reverse bias voltages ($-4 \text{ V} > V_G$), the leakage current is still dominated by FN tunneling, but there is an additional component associated with horizontal expansion of the depletion region beyond the gate edges.

In the next chapter, how the leakage current mechanism changes as the device is being stressed under forward gate bias will be discussed.

References

1. Zhang, H., E. Miller, and E. Yu, *Analysis of leakage current mechanisms in Schottky contacts to GaN and Al_{0.25}Ga_{0.75}N / GaN grown by molecular-beam epitaxy*. Journal of Applied Physics, 2006. **99**(2): p. 023703.
2. Turuvekere, S., A. DasGupta, and N. DasGupta, *Effect of barrier layer thickness on gate leakage current in AlGaIn/GaN HEMTs*. IEEE Transactions on Electron Devices, 2015. **62**(10): p. 3449-3452.
3. Turuvekere, S., N. Karumuri, A.A. Rahman, A. Bhattacharya, A. DasGupta, and N. DasGupta, *Gate leakage mechanisms in AlGaIn/GaN and AlInN/GaN HEMTs: comparison and modeling*. IEEE Transactions on electron devices, 2013. **60**(10): p. 3157-3165.
4. *Failure criteria*. 2019; Available from: <https://www.jedec.org/>.
5. Arulkumaran, S., T. Egawa, and H. Ishikawa, *Studies on the Influences of i-GaN, n-GaN, p-GaN and InGaIn Cap Layers in AlGaIn/GaN High-Electron-Mobility Transistors*. Japanese Journal of Applied Physics, 2005. **44**(5A): p. 2953-2960.
6. Zanoni, E., M. Meneghini, G. Meneghesso, D. Bisi, I. Rossetto, and A. Stocco. *Reliability and failure physics of GaN HEMT, MIS-HEMT and p-gate HEMTs for power switching applications: Parasitic effects and degradation due to deep level effects and time-dependent breakdown phenomena*. in *Wide Bandgap Power Devices and Applications (WiPDA), 2015 IEEE 3rd Workshop on*. 2015. IEEE.
7. Silvaco. *ganfetex15.in : GaN HEMT BV versus Gate to Drain distance* Available from: <https://www.silvaco.com/examples/tcad/section8/example15/index.html>.
8. *Electron Work Function of the Elements*

9. Sasangka, W.A., Y. Gao, C.L. Gan, and C.V. Thompson, *Impact of carbon impurities on the initial leakage current of AlGaIn/GaN high electron mobility transistors*. Microelectronics Reliability, 2018. **88-90**: p. 393-396.
10. Arulkumaran, S., S. Vicknesh, G.-I. Ng, L. Selvaraj, and T. Egawa, *Improved Power Device Figure-of-Merit ($4.0 \times 10^8 \text{ V}^2 \Omega^{-1} \text{ cm}^{-2}$) in AlGaIn/GaN High-Electron-Mobility Transistors on High-Resistivity 4-in. Si*. Applied Physics Express, 2011. **4**: p. 4101.
11. Arulkumaran, S., G. Ng, S. Vicknesh, C. Manojkumar, K. Ang, H. Wang, M. Anand, K. Ranjan, S. Selvaraj, and W. Wang, *Uniformity Studies of AlGaIn/GaN HEMTs on 8-in Diameter Si (111) Substrate*.
12. Hayashi, K., Y. Yamaguchi, T. Oishi, H. Otsuka, K. Yamanaka, M. Nakayama, and Y. Miyamoto, *Mechanism study of gate leakage current for AlGaIn/GaN high electron mobility transistor structure under high reverse bias by thin surface barrier model and technology computer aided design simulation*. Japanese Journal of Applied Physics, 2013. **52**(4S): p. 04CF12.
13. Mojaver, H.R. and P. Valizadeh, *Reverse gate-Current of AlGaIn/GaN HFETs: Evidence of leakage at mesa sidewalls*. IEEE Transactions on Electron Devices, 2016. **63**(4): p. 1444-1449.
14. Mojaver, H.R. and P. Valizadeh, *Modeling the Reverse Gate-Leakage Current in GaN-Channel HFETs: Realistic Assessment of Fowler–Nordheim and Leakage at Mesa Sidewalls*. IEEE Transactions on Electron Devices, 2018. **65**(8): p. 3156-3162.
15. Xu, C., J. Wang, H. Chen, F. Xu, Z. Dong, Y. Hao, and C.P. Wen, *The Leakage Current of the Schottky Contact on the Mesa Edge of AlGaIn/GaN Heterostructure*. IEEE Electron Device Letters, 2007. **28**(11): p. 942-944.
16. Hang, D., C.-T. Liang, C. Huang, Y. Chang, Y. Chen, H. Jiang, and J. Lin, *Effective mass of two-dimensional electron gas in an Al_{0.2}Ga_{0.8}N/GaN heterojunction*. Applied Physics Letters, 2001. **79**(1): p. 66-68.
17. GaN -- Optical properties. Available from: <http://www.ioffe.ru/SVA/NSM/Semicond/GaN/optic.html>.
18. AlN -- Band structure and carrier concentration. Available from: <http://www.ioffe.ru/SVA/NSM/Semicond/AlN/bandstr.html#Masses>.

Chapter 5

Electrical degradation of AlGaIn/GaN high electron mobility transistors (HEMTs) under forward gate bias stress^{*}

In this chapter, the electrical degradation of devices stressed under forward gate-bias is discussed. Upon stressing, the gate leakage increased dramatically without a significant change in the drain saturation current. The effect of stressing on the electron transport mechanisms under reverse bias was investigated. Finally, a degradation mechanism is proposed to explain the increase of the leakage current under forward gate bias stressing.

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5.1 Introduction

Most of the previous studies of the reliability of AlGaIn/GaN high electron mobility transistors (HEMTs) focused on the effects of reverse gate bias [1, 2]. Under this condition, the degradation is strongly driven by the high electric field under the gate. Under forward gate bias, the electric field under the gate is relatively lower but the number of electrons flowing across the Schottky interface is very high. The degradation mechanism under this condition is unclear but important to understand [3].

5.2 Experimental Details

AlGaIn/GaN HEMTs were stressed and measured using a probe station and a Keithley 4200-SCS parameter analyzer. A total of 15 devices were stressed under 4 different forward gate bias conditions at room temperature. During stressing, the source and drain contacts were grounded, and the gate contact was subjected to a positive bias. A schematic illustrating the testing sequence is shown in Figure 3.3.

The test methodology consists of I - V measurements and constant voltage stressing. The I - V measurements include I_G - V_G and I_D - V_G measurements. During the I_G - V_G measurements, V_{Gate} was swept from -10 V to 2 V and V_{DS} was kept as 0 V. The I_G - V_G measurements were carried out to characterize the quality of the Schottky contact at the gate/GaN-cap interface. For the I_D - V_G measurements, V_{Gate} was swept from -10 V to 2 V while V_{DS} was kept as 10 V. I_D - V_G measurements were used to characterize the performance of the HEMTs (e.g. V_{th} , I_{D-leak}) during stressing. The stressing conditions were $V_{G-stress} = 2$ V, 2.5 V, 3 V and 4 V with $V_{DS} = 0$ V. The I - V measurements were taken every 10 min for $V_{G-stress} = 2$ V and 5 min for $V_{G-stress} = 2.5$ V and 3 V. Under the condition $V_{G-stress} = 4$ V, the degradation was much faster than the other conditions, and thus the 5 min interval did not provide sufficient time resolution to capture the device degradation process, so the interval was set to 30 sec in this case. The stressing time was 10 min for $V_{G-stress} = 4$ V, and 8 hr for most of the rest conditions, as shown in Figure 5.2.

5.3 Results and Discussions

5.3.1 Electrical Measurement Results

Figure 5.1 shows a typical I - V characteristic for a device after being stressed under $V_{G-stress} = 3$ V over a period of time. The current was normalized by the gate width (80 μm). The gate leakage current increased dramatically during the 8 hr stressing. The leakage current increased suddenly within the first time interval but subsequently increase more slowly. I_{D-leak} and I_{G-leak} showed a similar trends and values, which indicates that I_{D-leak} mainly comes from the gate contact. There is no significant degradation in I_{D-sat} . The drain current before and after stressing is 0.34 A/mm and 0.31 A/mm, respectively. There is also no substantial shift of V_{th} during stressing ($\Delta V_{th} < 0.25$ V). These results suggest that the degradation is unlikely to be related to pit formation via electrochemical oxidation [4] or trap generation under the gate [5].

Figure 5.1 Typical I - V characteristics of a DUT under test at $V_{G-stress} = 3$ V over stressing time a) I_G - V_G characteristic, b) I_D - V_G characteristic.

The evolution of I_{G-leak} over time during stressing under different conditions is shown in Figure 5.2. I_{G-leak} was measured at $V_{Gate} = -8.5$ V during every I_G - V_G characteristic measurement; and the final I_{G-leak} was defined as the I_{G-leak} measured at last measurement phase (after 10-min stressing for $V_{G-stress} = 4$ V and 8-hr stressing for most of the rest conditions), which can be indicated as the last point of each line in Figure 5.2. For most of the devices, I_{G-leak} increased by at least two orders of magnitude. The degradation rate under $V_{G-stress} = 4$ V is much faster than under the other conditions and therefore the measurement interval was set to 30 sec for $V_{G-stress} = 4$ V. As shown in Figure 5.2, I_{G-leak} increases

dramatically within the first period of stressing and then increased more gradually afterwards. Furthermore, there is a huge variation of the I_{G-leak} among devices, even though the stressing conditions were the same. Moreover, no clear voltage dependence of final degradation I_{G-leak} is observed and the final I_{G-leak} overlaps among the four different stressing conditions.

Figure 5.2 I_{G-leak} versus stressing time for 15 nominally identical devices stressed at four different conditions: (a) $V_{G-stress} = 2$ V, (b) $V_{G-stress} = 2.5$ V, (c) $V_{G-stress} = 3$ V, (d) $V_{G-stress} = 4$ V.

The failure criterion was set to be the time at which I_{G-leak} reached 1 μ A (around 12.5 μ A/mm). In Figure 5.2, most of the devices were failed at the early stages of stressing. As

the stressing was kept continuing up to a fixed time, each device had a different final I_{G-leak} . The failure time versus stressing time is plotted in Figure 5.3. As seen in Figure 5.3, the degradation is highly accelerated by the stressing voltage. As one device stressed under $V_{G-stress} = 2$ V did not fail, the lifetime for this device is taken to be at least the maximum stressing time. The average lifetime was 1242 min (20 hr) for stressing under $V_{G-stress} = 2$ V, 101 min (1.7 hr) for $V_{G-stress} = 2.5$ V, 8 min for $V_{G-stress} = 3$ V and only 30 sec for $V_{G-stress} = 4$ V.

Figure 5.3 The average device failure times at four different stressing voltages. The error bars represent the standard deviation of the devices lifetime under each stressing condition.

The Schottky barrier height (ϕ_B) was calculated using Equation 3.5 for data from each I_G - V_G measurement for all devices, and the results are shown in Figure 5.4. The barrier height has a strong correlation with the I_{G-leak} during stressing, except for DUT4. As there was no severe degradation for DUT4, the correlation is not clear. For other devices, as I_{G-leak} increases during stressing, the Schottky barrier height reduces correspondingly. Lower Schottky barrier height leads to higher values of I_{G-leak} . This indicates that thermionic emission was enhanced during stressing. Furthermore, in Figure 5.5, there is a linear

dependence of the barrier height and the logarithm of I_{G-leak} , regardless of stressing voltages. This suggests that all the failed devices have the same failure mode.

Figure 5.4 Schottky barrier height versus I_{G-leak} for 15 nominally identical devices stressed under four different conditions: (a) $V_{G-stress} = 2$ V, (b) $V_{G-stress} = 2.5$ V, (c) $V_{G-stress} = 3$ V, (d) $V_{G-stress} = 4$ V.

Figure 5.5 Schottky barrier height versus I_{G-leak} for 15 nominally identical devices: the combination of four different test conditions.

The ideality factor (η) was calculated using Equation 3.4 for each I_G - V_G measurements and the results are shown in Figure 5.6. As seen here, there is also a strong correlation between the ideality factor and I_{G-leak} . A greater degradation of I_{G-leak} leads to a further increase in the ideality factor above 1, and therefore a greater departure from ideality. An increase in the ideality factor indicates that, in addition to thermionic emission, non-thermionic emission (e.g. Poole-Frenkel (PF) emission, Fowler-Nordheim (FN) tunneling) tends to play an important role in the total leakage current. These phenomena suggest that the degradation mainly occurred at the gate Schottky contact, rather than in the gate to source/drain access regions as there is not much degradation on the I_{D-sat} , which is shown in Figure 5.1.

Figure 5.6 Ideality factor versus I_{G-leak} for 15 nominally identical devices stressed at four different conditions: (a) $V_{G-stress} = 2$ V, (b) $V_{G-stress} = 2.5$ V, (c) $V_{G-stress} = 3$ V, (d) $V_{G-stress} = 4$ V.

A schematic of the degradation mechanism is shown in Figure 5.7. Figure 5.7(a) shows a fresh device with a relatively higher Schottky barrier height. Under reverse bias, both the thermionic emission current and non-thermionic emission (FN) current are low, leading to a small overall leakage current. However, during stressing, the Schottky barrier contact has been degraded over time. As the Schottky barrier height reduces (shown in Figure 5.7(b)), the thermionic emission current is enhanced. The larger ideality factor after stressing suggests non-thermionic emission current (either FN or PF) is also enhanced. As both the thermionic emission current and the non-thermionic emission current are increased during stressing, the total leakage current increases dramatically.

Figure 5.7 Schematic of electron transport at the Schottky contact (a) for fresh low leakage device, (b) for stressed high leakage device.

5.3.2 Electron Transport

Although non-thermionic emission is enhanced after stressing, it is still not clear which emission mechanism is dominant for the reverse leakage current. To develop an understanding of why and how the non-thermionic emission increased after stressing, I_G - V_G - T measurements were conducted for degraded devices to investigate whether the non-thermionic emission had changed after I_{G-leak} increased by around 2 orders of magnitude as compared to a fresh device. Figure 5.8 shows these measurements.

The I_G - V_G - T characteristics of a stressed device are shown as dashed lines in Figure 5.8 and I_G - V_G - T data for a fresh device are plotted in the same figure with solid lines. Similar to the unstressed device, the I - V profile in the reverse bias region of the stressed device can be divided into three regions: region I ($V_G < -4$ V), region II (-4 V $< V_G < V_{th}$), and region III ($V_{th} < V_G < 0$ V). As clearly seen in Figure 5.8, the leakage current of the stressed device is higher than the fresh device in all regions. In region I, the current dependence on voltage is even weaker than for the fresh device. This suggests that the horizontal leakage current ($I_{horizontal}$, which is indicated in Figure 4.11) is much smaller compared to the vertical leakage current ($I_{vertical}$). Although both the $I_{vertical}$ and the $I_{horizontal}$ may increase dramatically after stressing, $I_{vertical}$ is still likely to be dominating after stressing, because

the Schottky barrier height was reduced during stressing. As mentioned in the previous chapter, the region under the gate is fully depleted in region I. Thus, the vertical electric field is constant as the gate voltage is further decreases and therefore the leakage current is constant.

Figure 5.8 I_G - V_G - T measurements for a stressed device that failed after 80 min-stressing ($V_{G-stress} = 2$ V), overlaid with measurements for the same fresh device.

In region III, as the mesa sidewall current ($I_{mesasidewall}$ which is indicated in Figure 4.12) is very small due to the limited mesa sidewall contact area, the increase of I_{G-leak} is mainly caused by the vertical leakage current after stressing. Thus, the vertical leakage current, rather than mesa sidewall current, starts to dominate in this region. It has weaker temperature dependence than region III of fresh device.

Similar with regions I and III, the leakage current in region II of the stressed device is significantly higher than that in the fresh device. The current also strongly depends on the

applied voltage. As explained in chapter 4, the vertical electric field increases with an increase in negative gate voltage and therefore increases the leakage current. However, as the voltage dependence of the stressed device is weaker than the fresh one, this suggests that the electron transport mechanism has been changed during stress.

The leakage currents in region II and region III have a strong voltage dependence and the mesa current is negligible as compared to the vertical current. So, these two regions are most suitable for investigating of the electron transport mechanism of the vertical leakage current in the stressed device.

There are two possible electron transport mechanisms for the vertical leakage current: Fowler-Nordheim (FN) tunneling and Poole-Frenkel (PF) emission. The derivation and analysis approaches are the same to the those described for fresh devices in chapter 4.

Based on Equation 2.11 and Equation 2.12, E_b is a critical value for analysis of the transport mechanisms. However, the Schottky contact was degraded during stressing, so the band structure has changed at the gate contact region (which is shown in Figure 5.7(b)). The change of the band structure leads to a different electric field distribution at the Schottky diode. So, in order to determine an accurate electric field distribution, the simulation parameters have to be modified.

When a Schottky contact is formed, the barrier height is determined by Equation 5.1:

$$\phi_B = \phi_M - \chi, \quad \text{Equation 5.1}$$

where ϕ_M is the work function of the metal and χ is the electron affinity of the semiconductor. After stressing, the barrier height is reduced, which means either the value of ϕ_M or χ has changed. However, there is no clear evidence from the electrical characterization indicating which value(s) has changed during stressing.

The electric field versus applied gate voltage is plotted in Figure 5.9. Each line represents the electric field simulated for different barrier heights. ϕ_{M_fresh} indicates the simulated field of a fresh device. The other lines are the electric fields with reduced barrier heights, which are due to the device degradation. As shown in Figure 5.9, a smaller barrier height leads to a lower electric field across the AlGaIn layer. This is because there is a smaller built-in field when the Schottky barrier height is lower. After stressing, the Schottky barrier height has decreased from 0.88 eV to 0.70 eV. Thus, the barrier height used for the simulations was $\phi_{M_fresh} - 0.2 \text{ eV}$ for the stressed device.

Figure 5.9 Simulated vertical electric field across the AlGaIn layer versus applied gate voltage for different gate work functions.

To test the FN tunneling mechanism hypothesis, the plot of $\ln(J_{Gate}/E_b^2)$ versus $1/E_b$ at different temperatures is shown in Figure 5.10. The data shows a stronger temperature

dependence over the room temperature range (i.e. 27°C to 77°C) after stressing. This may indicate that the transport mechanism is not FN tunneling for stressed device. Furthermore, as the barrier height was calculated from the forward bias region, the effective mass of AlGaN was extracted from the slopes of the lines in Figure 5.10. The effective mass of AlGaN calculated from Figure 5.10 is 0.070 at 300K, which is much lower than the reported values (between 0.22 to 0.4) [6].

Figure 5.10 The measured data fitted with the FN tunneling model (Equation 2.12) for a stressed device.

The analysis based on the PF emission model is shown in Figure 5.11. The data shows a temperature dependence, especially in the room temperature range. The data was fitted with $\xi = 1$, and $m(T)$ versus $1/T$ is plotted in Figure 5.12. From the slope of the line in Figure 5.12, the permittivity of the AlGaN was extracted as 5.7. This value is between the permittivity of AlN (4.6) and GaN (5.8) [7, 8]. Thus, it is likely that the electron transport is controlled by PF emission instead of FN tunneling, for stressed devices at room temperature.

Figure 5.11 I_G - V_G - T data of a stressed device fitted with the PF model (Equation 2.11).

Figure 5.12 The slopes of the fitted lines in Figure 5.11 versus the inverse of the corresponding test temperature. The slope of the fitted line in this figure was used to extract a value for the permittivity, which was found to be in agreement with expected value for AlGaIn.

Interestingly, there might be a correlation between the final I_{G-leak} with the compensation factor. These devices were chosen regardless of stressing voltages and the final I_{G-leak} was extracted from the last measurement phase. From Figure 5.13, the plot indicates that devices having a higher final I_{G-leak} are associated with a higher compensation factor. As mentioned in chapter 2 (Equation 2.11), the compensation factor represents the difference between N_D and N_A . When the compensation is 2, N_D is much larger than N_A . Thus, from Figure 5.13, it can be concluded that higher N_D may enhance the PF emission and therefore induce larger I_{G-leak} . As there is no traditional donors in GaN HEMTs, no donors should be observed in the fresh devices. However, defects which might be induced during stressing could act as donor. These defects will be further verified by material characterizations in the next chapter.

Figure 5.13 Compensation factor versus final I_{G-leak} for 6 devices tested under different stressing conditions.

Based on the transport mechanism analysis and Equation 4.5, the I_r for stressed devices has three different components: $I_{horizontal}$, $I_{vertical}$ and $I_{mesasidewall}$. However, due to the reduction

in barrier height after stressing, $I_{vertical}$ is expected to dominate in the reverse bias region. Furthermore, after stressing, the dominant non-thermionic emission mechanism for reverse leakage current is PF emission, rather than FN tunneling, so the I_G - V_G - T behavior of stressed devices show a different trend compared to the fresh ones.

5.4 Conclusions

In this chapter, the electrical degradation of GaN HEMTs under forward gate bias was analyzed. After stressing, the I_{G-leak} increased dramatically, but not much degradation of the I_{D-sat} was observed. Furthermore, the degradation of I_{G-leak} was highly accelerated by the stressing voltage.

From the electrical characterizations, the Schottky barrier height was found to be reduced and the ideality factor was found to have increased during stressing. These results suggest that the degradation mainly takes place at the gate contact area. Further analysis indicates that after stressing, the leakage current is mainly controlled by PF emission rather than FN tunneling. It is also found that higher values of final I_{G-leak} of failed devices correlated with high values of N_D .

In the next chapter, the material characterizations of the stressed device will be discussed to shed light on how the physical degradation observed could be correlated to the electrical degradation discussed in this chapter.

References

1. Gao, F., S.C. Tan, J.A. del Alamo, C.V. Thompson, and T. Palacios, *Impact of water-assisted electrochemical reactions on the OFF-state degradation of AlGaIn/GaN HEMTs*. IEEE Transactions on electron devices, 2014. **61**(2): p. 437-444.
2. Gao, F., B. Lu, L. Li, S. Kaun, J.S. Speck, C.V. Thompson, and T. Palacios, *Role of oxygen in the OFF-state degradation of AlGaIn/GaN high electron mobility transistors*. Applied Physics Letters, 2011. **99**(22): p. 223506.

3. Christiansen, B.D., E.R. Heller, R.A. Coutu, R. Vetury, and J.B. Shealy, *A very robust AlGaIn/GaN HEMT technology to high forward gate bias and current*. Active and Passive Electronic Components, 2012. **2012**.
4. Sasangka, W.A., G.J. Syaranamual, C.L. Gan, and C.V. Thompson. *Origin of physical degradation in AlGaIn/GaN on Si high electron mobility transistors under reverse bias stressing*. in *2015 IEEE International Reliability Physics Symposium*. 2015.
5. Meneghini, M., A. Stocco, M. Bertin, N. Ronchi, A. Chini, D. Marcon, G. Meneghesso, and E. Zanoni. *Electroluminescence analysis of time-dependent reverse-bias degradation of HEMTs: A complete model*. in *2011 International Electron Devices Meeting*. 2011.
6. Zhang, H., E. Miller, and E. Yu, *Analysis of leakage current mechanisms in Schottky contacts to GaN and Al_{0.25}Ga_{0.75}N / GaN grown by molecular-beam epitaxy*. Journal of Applied Physics, 2006. **99**(2): p. 023703.
7. AlN -- Band structure and carrier concentration. Available from: <http://www.ioffe.ru/SVA/NSM/Semicond/AlN/bandstr.html#Masses>.
8. GaN -- Optical properties. Available from: <http://www.ioffe.ru/SVA/NSM/Semicond/GaN/optic.html>.

Chapter 6

Physical degradation of AlGaN/GaN high electron mobility transistors (HEMTs) under forward gate bias stressing*

In this chapter, the physical degradation of AlGaN/GaN high electron mobility transistors (HEMTs) under forward gate bias stressing is discussed. Various advanced characterization techniques such as photon emission microscopy (PEM), transmission electron microscopy (TEM), and electron energy loss spectroscopy (EELS) were utilized to understand the physical origin of device failure. It was found that carbon residue at the Ni/GaN-cap interface at the gate is responsible for the increase of leakage current during stressing. The carbon residue is likely originated from the photoresist residue that was introduced during the gate lift-off process.

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6.1 Introduction

Although the electrical degradation of HEMTs under forward gate stressing has been observed before, the origin of the physical degradation is still unclear [1, 2]. In the previous chapter, electrical characteristics after AlGaIn/GaN HEMT device degradation were presented and analyzed. It was concluded that a decrease in the Schottky barrier height during testing was the primary cause of increases of the gate leakage current.

Understanding of the physical degradation mechanism is critical for device reliability analyses. First, the lifetime model must be established based on a specific physical degradation mechanism. The physical-based model gives more insight into the degradation, and therefore provides a basis for more accurate lifetime predictions based on results from accelerated testing. Secondly, by knowing the origin of physical degradation, it is possible to give feedback to the process development group to improve device reliability.

The physical degradation mechanism underlying the electrical degradation discussed in Chapter 5 AlGaIn/GaN, which is related to the increase of I_{G-leak} and decrease of barrier height, is not well understood. As the degradation mechanism highly depends on the device process, architecture, material quality, etc. [3, 4], it is essential to investigate the physical degradation mechanisms of the AlGaIn/GaN HEMTs under forward gate bias stressing.

6.2 Experimental Details

To investigate the origin of the physical degradation, several material characterization techniques were utilized. The devices were first examined via non-destructive methods with optical and scanning electron microscopes.

Photon emission microscopy (PEM) was also used to help locate high leakage paths for the failed devices. Under PEM, the devices were subjected to a gate voltage which was more negative than -4 V with $V_{DS} = 0$ V. An InGaAs charge-coupled device (CCD) camera was used to collect the photons emitted from the device.

After localizing the high leakage path, a cross-sectional transmission electron microscope (TEM) sample was prepared using a focused-ion beam (FIB) technique at the high leakage location. In order to enhance the image resolution and reduce contamination for the TEM samples, each lamella was cleaned using low-kV Ga⁺ ion beam polishing followed by use of an Argon/Nitrogen plasma before analysis in a TEM.

Various TEM techniques (e.g. high-angle annular dark-field (HAADF) and selected area electron diffraction (SAED)) were implemented to characterize the devices. Furthermore, chemical analysis tools, such as Energy-dispersive X-ray spectroscopy (EDX) and electron energy loss spectroscopy (EELS), were introduced to obtain elemental information from the specimen. By combining these characterization techniques, the physical degradation under forward gate stressing was studied in detail.

6.3 Results and Discussions

From top view optical microscopy analysis alone, there was no significant observed difference between devices with low leakage currents (fresh devices) and high leakage currents (failed devices), as shown in Figure 6.1. Some of the particles on the devices were likely introduced during sample handling and no correlation between such particles with the high-leakage current was found.

Figure 6.1 Top view optical microscope images of AlGaIn/GaN HEMTs (a) A fresh device with 125 nA/mm leakage current, (b) a stressed device with 12.5 μ A/mm leakage current ($V_{G-stress} = 4$ V), and (c) a stressed device with 1.25 mA/mm leakage current ($V_{G-stress} = 4$ V).

Figure 6.2 shows photon electron microscopy images for three different devices under the same bias condition, $V_G = -8$ V and $V_{DS} = 0$ V. No hot spot is observed in the devices that has a low leakage current (125 nA/mm, (fresh device) and the device with an intermediate leakage current 12.5 μ A/mm. For the device that has a very high leakage current, a few hotspots were observed along the gate edge. The size of hotspots is correlated with the number of emitted photons collected by the near infrared (NIR) detector, which is proportional to the amount of current density that passed through the Schottky contact. From the zoom-in image in Figure 6.2(c), it is expected that the majority of the leakage current passed through the large hotspot region, while a small portion of the leakage current passed through the location of small hotspots. These observations suggest that the degradation of the devices is highly localized only at certain sites along the gate. It is also worth noting that there is a leakage current threshold below which no hotspot is observed. This likely corresponds to the limit of the InGaAs detector used in this experiment. With this information, it is possible to narrow the physical degradation analysis to these hotspots.

Figure 6.2 Photon emission microscopy images of devices with different gate leakage currents I_{G-leak} . (a) A fresh device with 125 nA/mm leakage current, (b) a stressed device with 12.5 μ A/mm leakage current ($V_{G-stress} = 4$ V), and (c) a stressed device with 1.25 mA/mm leakage current ($V_{G-stress} = 4$ V).

Figure 6.3 shows bright field TEM images of a fresh device (random region) and a stressed device with 1.25 mA/mm leakage current (at the large hotspot region). There seems to be no significant difference between the fresh and failed devices. Unlike drain current degradation, there is no pit/oxide at the gate edges [5]. It is also clear that there is no degradation of the SiN passivation layer. These results suggest that the electrochemical oxidation mechanism cannot explain the degradation associated with an increase in I_{G-leak} under forward gate bias stressing [6].

Figure 6.3 Transmission electron microscopy images (bright field) of devices with different leakage current. a) 125 nA/mm (fresh device), no hotspot. b) 1.25 mA/mm (failed device) at hotspot.

Interestingly, a startling difference can be observed between the two devices (low and high leakage) under HAADF image collection mode. As seen in Figure 6.4, a dark region is observed within the nickel layer of the failed device (indicated by white dash line). Under HAADF mode, different contrast in the image correlates with different average atomic number. The dark region in the nickel layer, therefore, suggests that the composition of the gate metal has changed after stressing.

Figure 6.4 High angle annular dark field (HAADF) STEM images of a (a) fresh sample and (b) a stressed sample at a hotspot location. There is a dark region in the nickel layer of the stressed sample, which may indicate the local composition of the Ni layer has changed after stressing.

Chemical analysis using both EDX and EELS shows consistently that the dark region has a very high carbon concentration. As seen in Figure 6.5(a), a carbon peak is observed in the dark region of the failed device, but not in the non-dark region. Chromium peaks appear in both dark and non-dark regions. Cr comes from the TEM specimen chamber, column and apertures due to Rutherford backscattering, rather than from the specimen itself [7]. EELS analysis (Figure 6.5(b)) also shows a similar result, that carbon is present in the dark region of the failed device but not in the non-dark regions. Furthermore, from the EELS spectrum it can be observed that the binding energy of the carbon is 280 eV, which is the incident electron energy loss corresponding to the binding energy of K shell. In both analyses, the carbon is found in the dark region and the concentration is about 20% in atomic percentage. As all the samples were cleaned using low energy Ga^+ ion polishing and using an Argon/Nitrogen plasma, the carbon signals are not from contamination during the TEM sample preparation. Furthermore, the concentration of carbon did not increase during the TEM/EELS analysis, so the carbon signals were not from the TEM sample holder either. Thus, we conclude that the carbon is present in the stressed the sample.

Figure 6.5 (a) EDX point spectra in the dark region and non-dark region of a stressed sample. (b) EELS point spectra in the dark region and non-dark region of a stressed sample. The blue line is an EELS spectrum at the dark region and there is a peak at around 280 eV which is corresponding to carbon. (c) The point positions indicated in a TEM image.

Figure 6.6 shows two EELS line scans of a fresh sample and stressed sample in a hotspot region. The relative carbon composition is extracted from the electron energy loss associated with the K edge. As seen in Figure 6.6(a), the carbon concentration along the nickel layer is close to zero for a fresh device. However, in Figure 6.6(b), for the stressed device in a hotspot region, a high concentration of carbon is detected. From the EELS line scan, the carbon signal has the same distance as the dark region, indicating the whole dark region contains a high concentration of carbon.

Figure 6.6 EELS line scans for (a) a fresh sample and (b) a stressed sample at a hotspot region.

Figure 6.7 shows electron energy loss at 280 eV (which is due to the carbon K shell excitation) for three different TEM samples from one hotspot region and two non-hotspot regions. In Figure 6.7, the ‘hotspot’ and the ‘non-hotspot1’ are from same stress device (which is shown in Figure 6.2(c)) at different regions, and ‘non-hotspot2’ is from a different stressed device with 10 mA/mm leakage current. In a previous study of nominally the same devices but with high initial leakage currents [8], it was shown that hotspot regions always correlated with dark areas, and dark areas were not present away from non-hotspot regions. This is further supported by the ‘non-hotspot2’ data, shown as the blue line in Figure 6.7. No dark area was found in ‘non-hotspot2’ sample and therefore there was no carbon signal in the EELS spectrum. However, interestingly, a dark area was shown in the nickel layer in the ‘non-hotspot1’ sample. The EELS analysis suggests that the dark region also has a high carbon concentration. From the extracted spectra, the carbon energy loss signal at the non-hotspot area is lower than the hotspot area. This indicates that this ‘non-hotspot1’ region may be one of the small hotspots along the gate as the carbon content is relatively lower than the large hotspot region. This ‘non-hotspot1’ region may contribute to a small portion of the leakage current, while the majority of leakage current passed through the location of large hotspot.

Figure 6.7 EELS spectrum at the dark area for a hotspot region and non-hotspot region, and at random point for another non-hotspot region without any dark area.

Interestingly, it is worth noting that the carbon content region in stressed device is located within a single grain of nickel. Figure 6.8(a) shows the diffraction pattern of the nickel grain with high carbon concentration in Figure 6.6(b). The bright spots in Figure 6.8(a) refer to the diffraction pattern of the high carbon content nickel grain, while the weaker spots correspond to the neighboring nickel grains, gold layer and AlGaIn layer. This is mainly because the smallest SAED aperture in the TEM is 150 nm, while the high carbon content nickel grain is less than 140 nm. So, it is impossible to obtain a diffraction pattern which is purely from the nickel grain with the carbon component. The diffraction pattern was analyzed using JEMS software. First, the angle and distance between the diffracted beams and center beam were measured. Then, these measured data were loaded into a database to find the zone axis and orientation. The results from JEMS suggest that the diffraction image was taken at $[120]$ zone axis and the high carbon content nickel is orientated with a (111) plane (which is equivalent to the $(11\bar{1})$ plane) at the AlGaIn surface.

Figure 6.8 (a) SAED image on the carbon region of the TEM lamella in a hotspot region aligned along the $[112]$ zone axis, (b) dark field TEM image by selecting a high intensity diffraction beam from the SAED image, showing that the dark area associated with carbon corresponds to the size, shape and location of a single grain.

An objective aperture was inserted to select one of the bright spots (which is highlighted in a yellow open circle) from the diffraction pattern to obtain a dark field (DF) TEM image. From the DF-TEM image shown in Figure 6.8(b), the bright region is the single grain of

nickel with the selected electron beam. This bright region has the same size, shape and location as the dark region in the HAADF image in Figure 6.4(b). This indicates that the carbon is located within a single grain of nickel.

Two more stressed samples were examined using the same characterization procedure. All of them were found to have a high concentration of carbon located in a single grain of nickel. The work function of nickel is 5 eV, which is higher than the carbon work function ($\phi_C = 4.6$ eV). Several papers have reported that carbon can exist in nickel and lower the overall work function [9, 10]. As the overall work function reduces, the Schottky barrier height becomes smaller as well. In chapter 5 of this thesis, the electrical characterizations showed that a decrease of Schottky barrier height is one of the reasons causing the increase of the leakage current. Thus, the physical evidence of the presence of high carbon content in the nickel layer at hotspot regions suggests that carbon leads to the decrease in the Schottky barrier height at the gate that causes the high leakage current after stressing.

To have a better understanding of the degradation process, it is important to take a look at how the I_{G-leak} increased during stressing. Figure 6.9 shows a typical example of the increase in I_{G-leak} with stressing time. From this figure, there is an initial sudden increase in I_{G-leak} . After this initial jump, there are two degradation stages: a fast stage and a slow stage. Segmented linear regressions were implemented to find the transition point between these two regions, which is the intercept of the red line and the green line shown in Figure 6.9. In the fast stage, I_{G-leak} increased quickly with time. While, in the slow stage, the degradation rate is much slower and most of the devices had already reached the failed criteria before this stage.

Figure 6.9 Typical example of IG-leak vs stressing time of a device stressed under the forward gate bias.

As high carbon content was detected in some nickel grains after forward bias gate stressing, the origin of the carbon content is critical to understand the failure mechanism. It is suspected that the carbon was introduced during the gate fabrication process. In the device fabrication process, the gate was formed using a lift-off process. The process flow is shown in Figure 6.10.

First, the whole epitaxy layer was coated with positive photoresist. Then a mask was inserted between the wafer and UV light source for the lithography process. The photoresist at the gate region was exposed to the UV light, after which the exposed photoresist could be easily removed using a Descum process. The Descum process is a standard method to remove photoresist, by using monatomic oxygen plasma. The UV-exposed photoresist then reacted with the plasma to form ash, and this mixture was removed through a vacuum pump. Next, hydrochloric acid was used to remove native surface oxide (e.g. GaO_x). After the Descum process, a trench was formed between non-UV-exposed photoresist regions. Nickel and gold were deposited on the whole wafer surface by evaporation, covering the gate region as well as the top of non-UV-exposed photoresist, as shown in the fourth step of Figure 6.10. Finally, the remaining photoresist was removed using acetone, which also removed the metal layers on top of the resist simultaneously. Lastly, Si_3N_4 was deposited

over the whole wafer surface by using Plasma-enhanced chemical vapor deposition (PECVD).

Figure 6.10 Schematic of lift-off process for gate metal fabrication.

Hence, the origin of carbon is most likely photoresist residue (hydrocarbon) that had remained after the lift-off process. It is expected that the hydrocarbon was randomly distributed across the wafer after photoresist removal, and some of the areas of residue could be present at the AlGaN/Ni interface. During forward bias gate stressing, the hydrocarbon at the AlGaN/Ni interface could have carbonized first and then migrated into a single grain of nickel. These two degradation mechanisms could explain the two stages of the I_{G-leak} increase shown in Figure 6.9. The initial sudden increase of the leakage current may correspond to the starting point for carbonization process of the residues. Then, carbon at the semiconductor-metal interface reduces the barrier height at the Schottky gate contact. As the forward gate stress continues, the carbon further migrates into nickel. However, it is likely that the carbon concentration at the interface did not change significantly. Thus, the barrier height stays relatively constant during the later stages of stressing, which is supported by the experimental data as shown in Figure 6.11.

Figure 6.11 Barrier height versus stressing time of 15 nominally identical devices stressed at three different conditions: (a) $V_{G\text{-stress}} = 2 \text{ V}$, (b) $V_{G\text{-stress}} = 2.5 \text{ V}$, (c) $V_{G\text{-stress}} = 3 \text{ V}$, (d) $V_{G\text{-stress}} = 4 \text{ V}$.

Figure 6.12 shows a schematic picture of the proposed degradation process. As the degradation mainly takes place at the gate contact, only the gate area is drawn in the figure. In Figure 6.12(a), the small black squares represent carbon residue at sites which are randomly distributed at the AlGaN surface. The solid blue lines in the nickel layer indicate different nickel grain boundaries. Under the forward gate bias stressing, the carbon residue at the AlGaN/Ni interface is carbonized (shown in Figure 6.12(b)), which corresponds to the initial sudden increase of the leakage current. Then, carbon migrates into nickel grains, causing a further moderated degradation, as shown in Figure 6.12(c).

Figure 6.12 A schematic of the proposed device degradation process during forward gate bias stressing. (a) A fresh device before stressing. Carbon residue is randomly distributed along the AlGaN surface. (b) Under forward gate bias stressing, the carbon residue under the gate is carbonized. (c) Then carbon migrates into the metal layer with the assistance of the electric field.

In order to carbonize the photoresist, the electrons must have enough energy to carbonize or dehydrogenate the hydrocarbon. Several groups have reported the energy that is required to dehydrogenate methane (C_xH_y) on different nickel surfaces with different orientations [11-13]. Figure 6.13 indicates the reaction barrier height of the dehydrogenation process of

methane on a nickel surface. The reaction barrier for methane decomposition has been calculated using quantum mechanics (QM) and reactive force field (ReaxFF) methods [12]. The decomposition process of methane is labeled at the horizontal axis. The highest energy that is needed to break a C-H bond is around 35 kcal/mol, which is around 1.5 eV. Thus, as long as the electrons have an energy higher than 1.5 eV during the forward gate stressing, the hydrocarbon can be carbonized.

Figure 6.13 Reaction barrier heights for methane decomposition. Barriers are calculated by using ReaxFF and QM [12].

From theoretical Monte Carlo calculations, the average electron energy reaches 1.5 eV at about 450 kV/cm for Wurtzite GaN, as shown in Figure 6.14 [14]. The electron energy increases dramatically from 250 to 450 kV/cm, and tends to be saturated at higher electric field. From TCAD simulations, the electric field is about 450 kV/cm under $V_{G-Stress} = 1.7$ V (shown in Figure 6.15). Therefore, it is possible for the electrons to carbonize the photoresist residues at this stress condition. This may explain the initial sudden increase of the leakage current. During stressing, the hydrocarbon was carbonized quickly. In the high carbon content region, the overall work function is lower than other places, which leads to the decrease of Schottky barrier height, and thus the increase in the leakage current.

As the electrons obtain enough energy to cause carbonization at $V_G = 1.7$ V, the carbonization process may not happen below 1.7 V at room temperature or at lower

voltages at higher temperatures. From figure 5.3, the degradation is highly accelerated by the applied voltage. When the applied gate voltage is higher than 1.7 V, degradation can take place. The higher gate voltage not only induces higher energy electrons but also provides a larger number of electrons to carbonize the photoresist, which enhances the decomposition rate. For typical use conditions, the source to gate voltage (V_{GS}) is recommended to not exceed 2 V [15, 16]. However, if there is any carbon residue at the Ni/semiconductor interface, it will be detrimental for device reliability if devices are operated above 1.7V.

Figure 6.14 Average electron energy versus the electric field [13].

Figure 6.15 Simulated electric field in the AlGaN barrier under forward gate bias.

It is also necessary to determine how the carbon moves into the nickel grain. During stressing, the maximum stressing current across the gate contact is 0.1 A at $V_{G-Stress} = 4$ V, so the maximum power is 0.4 W. As the gate width is 80 μm , the maximum stressing current density and power density are 1.25 A/mm and 5 W/mm, respectively. Several groups have simulated and measured the channel temperature under similar power dissipation conditions, and the channel temperature is around 100°C during stressing [17, 18]. In Figure 6.4(b), the longest distance of the dark area from the AlGaN surface is 120 nm. The carbon diffusion distance can be approximated using [8]:

$$\delta = \sqrt{Dt}, \quad \text{Equation 6.1}$$

where

$$D = D_0 \exp\left(-\frac{E_a}{kT}\right) \quad \text{Equation 6.2}$$

and E_a is the activation energy, which is around 0.87 eV according to ref [9]. D_0 is a pre-exponential factor, and the value is $2.89 \times 10^{-5} \text{ cm}^2/\text{s}$ [9]. t is the time that is required to diffuse a distance δ . Based on these equations, 300 hr might be needed for carbon to diffuse into the whole Nickel grain, which is much longer than the stressing time.

Thus, the carbon can possibly migrate to the nickel with the assistance of the electric field after the carbonization process. When a carbon atom is bonded to nickel, carbon will be slightly negatively charged. This is due to carbon having a larger electronegativity (2.5) as compared to nickel (1.9). Therefore, during the forward gate bias, the electrical field is high enough to accelerate the migration process.

Furthermore, as mentioned in chapter 5, the compensation factor increases during stressing, which indicates that N_D has increased. Because the hydrocarbon is carbonized during stressing, it is possible that the carbon atoms could replace the atoms (Al or Ga) at the Ni/semiconductor interface to become a donor or acceptor. It has been reported the C_{Al} or C_{Ga} works as donor in AlGaN and GaN [19]. Thus, as an increasing amount of hydrocarbon is carbonized during stressing, more and more carbon atoms could substitute for Al or Ga atoms to create donor states, which leads to an increase of the compensation factor.

It has been reported that different nickel surfaces have different carbonization energy for hydrocarbons, where the (111) surface has the highest carbonization energy [11]. Thus, if the carbonization process could take place on the (111) surface, it also could occur on any other surface with a different orientation. It is important and interesting to investigate whether the orientation relationship between nickel and AlGaN at the surface could affect device reliability and yield.

A total of 6 samples were studied, including two bad devices with high initial leakage currents [8]. All these samples have high carbon content in the nickel layer and the carbon is located in an individual grain of nickel. Figure 6.16 shows orientation data for the high-carbon content grains is plotted in an inverse pole figure using the MTEX toolbox in

MATLAB. As the orientation data is not found in clusters, there might not be any nickel preferred orientation for hydrocarbon decomposition.

Figure 6.16 Inverse pole figure for texture orientation for six high carbon content nickel grains.

6.4 Conclusions

In this chapter, the origin of the high leakage current is established to be related to carbon impurities. The impurity comes from photoresist residue introduced during the lift-off process. During the forward gate bias stressing, the photoresist was postulated to have carbonized and migrated into the nickel layer with the help of the electric field. Furthermore, the carbon is located within a single grain of nickel. However, the crystallographic orientation of the nickel grains does not appear to affect the carbonization process. These results suggest that carbon is detrimental for AlGaIn/GaN HEMT device reliability. To improve future device reliability, especially under forward gate bias, a carbon residue free surface after lift-off is critical. As descum process was used during the device fabrication, it is likely that this cleaning process was not optimized and the process parameters (e.g. process temperature and plasma power) need to be further fine-tuned. Overall, by reducing photoresist residue, devices should be much more robust when subjected the forward gate bias.

References

1. Christiansen, B.D., E.R. Heller, R.A. Coutu, R. Vetury, and J.B. Shealy, *A very robust AlGaIn/GaN HEMT technology to high forward gate bias and current*. Active and Passive Electronic Components, 2012. **2012**.
2. Axelsson, O., M. Thorsell, K. Andersson, and N. Rorsman, *The Effect of Forward Gate Bias Stress on the Noise Performance of Mesa Isolated GaN HEMTs*. IEEE Transactions on Device and Materials Reliability, 2015. **15**(1): p. 40-46.
3. Ren, J., W. Mou, L. Zhao, D. Yan, Z. Yu, G. Yang, S. Xiao, and X. Gu, *A Comprehensive Study of Reverse Current Degradation Mechanisms in Au/Ni/n-GaN Schottky Diodes*. IEEE Transactions on Electron Devices, 2017. **64**(2): p. 407-411.
4. Joh, J., L. Xia, and J.A.d. Alamo. *Gate Current Degradation Mechanisms of GaN High Electron Mobility Transistors*. in *2007 IEEE International Electron Devices Meeting*. 2007.
5. Sasangka, W.A., G.J. Syaranamual, C.L. Gan, and C.V. Thompson. *Origin of physical degradation in AlGaIn/GaN on Si high electron mobility transistors under reverse bias stressing*. in *2015 IEEE International Reliability Physics Symposium*. 2015.
6. Gao, F., S.C. Tan, J.A. del Alamo, C.V. Thompson, and T. Palacios, *Impact of water-assisted electrochemical reactions on the OFF-state degradation of AlGaIn/GaN HEMTs*. IEEE Transactions on electron devices, 2014. **61**(2): p. 437-444.
7. Liao, Y., *Practical Electron Microscopy and Database*. 2018.
8. Sasangka, W.A., Y. Gao, C.L. Gan, and C.V. Thompson, *Impact of carbon impurities on the initial leakage current of AlGaIn/GaN high electron mobility transistors*. Microelectronics Reliability, 2018. **88-90**: p. 393-396.
9. Massaro, T.A. and E.E. Petersen, *Bulk Diffusion of Carbon - 14 through Polycrystalline Nickel Foil between 350 and 700 ° C*. Journal of Applied Physics, 1971. **42**(13): p. 5534-5539.
10. Blakely, J., J. Kim, and H. Potter, *Segregation of carbon to the (100) surface of nickel*. Journal of Applied Physics, 1970. **41**(6): p. 2693-2697.
11. Schouten, F., O. Gijzeman, and G. Bootsma, *Interaction of methane with Ni (111) and Ni (100); diffusion of carbon into nickel through the (100) surface; An aes-leed study*. Surface Science, 1979. **87**(1): p. 1-12.

12. Mueller, J.E., A.C. Van Duin, and W.A. Goddard III, *Development and validation of ReaxFF reactive force field for hydrocarbon chemistry catalyzed by nickel*. The Journal of Physical Chemistry C, 2010. **114**(11): p. 4939-4949.
13. Mueller, J.E., A.C. Van Duin, and W.A. Goddard III, *Competing, Coverage-Dependent Decomposition Pathways for C₂H₂ Species on Nickel (111)*. The Journal of Physical Chemistry C, 2010. **114**(47): p. 20028-20041.
14. Kolník, J., Ľ.H. Oğuzman, K.F. Brennan, R. Wang, P.P. Ruden, and Y. Wang, *Electronic transport studies of bulk zincblende and wurtzite phases of GaN based on an ensemble Monte Carlo calculation including a full zone band structure*. Journal of Applied Physics, 1995. **78**(2): p. 1033-1038.
15. Wolfspeed, *CGH40090PP Datasheet*. 2020.
16. Wolfspeed, *CGH40120F Datasheet*. 2020.
17. Gao, F., *Degradation study of AlGaIn/GaN high electron mobility transistors through electro-thermo-mechanical calculations and thermo-reflectance measurements*, in *Dept. of Materials Science and Engineering*. 2010, Massachusetts Institute of Technology.
18. Kuzmik, J., R. Javorka, A. Alam, M. Marso, M. Heuken, and P. Kordos, *Determination of channel temperature in AlGaIn/GaN HEMTs grown on sapphire and silicon substrates using DC characterization method*. IEEE transactions on electron devices, 2002. **49**(8): p. 1496-1498.
19. Matsubara, M. and E. Bellotti, *A first-principles study of carbon-related energy levels in GaN. I. Complexes formed by substitutional/interstitial carbons and gallium/nitrogen vacancies*. Journal of Applied Physics, 2017. **121**(19): p. 195701.

Chapter 7

Conclusions and Future work

In this chapter, conclusions from studies of the degradation of AlGaIn/GaN devices under forward gate bias stressing are summarized. As discussed in the previous chapters, the increase of the gate leakage current is related to the presence of carbon in the nickel layer in the gate electrode. This conclusion is supported by both electrical and material characterizations. Recommendations for future work are also discussed.

7.1 Conclusions

The goal of this research was to provide a comprehensive understanding of AlGaIn/GaN HEMT degradation under forward gate bias stressing. After stressing, the gate leakage current, I_{G-leak} , increased dramatically without significant degradation of the drain saturation current, I_{D-sat} . By combining both electrical and material characterization techniques, the physical origin of the degradation was determined. After determining the degradation mechanism, possible solutions to improve the device reliability can be proposed. Furthermore, these results can help to benchmark regimes for reliable device operation. Finally, yet importantly, the research described in this dissertation provides a methodology to investigate the failure of HEMT devices, especially for I_{G-leak} degradation.

I_{G-leak} degradation is critical for AlGaIn/GaN HEMT device reliability. A large increase in I_{G-leak} can lead to operation instability and high power consumption. Although I_{G-leak} degradation of AlGaIn/GaN HEMTs has been studied and observed by other groups, the mechanisms may vary depending on different stressing conditions or processing techniques [1, 2]. Thus, the mechanism of I_{G-leak} degradation has to be investigated individually. Furthermore, most earlier studies focused on degradation under reverse gate bias stressing. Only a limited number of papers have reported on the device failure under forward gate bias stress [3, 4]. Moreover, most studies were based on electrical characterizations, with a lack of observation and discussion on the physical origin of failures. In order to fill this gap, both electrical degradation and physical degradation have been investigated in this research described in this dissertation.

Before being subjected to any stressing, the electrical properties of fresh devices were analyzed first. The fresh devices that were used in this study showed high uniformity and low I_{G-leak} . The extracted parameters (e.g. V_{th} , ϕ_B and η) are acceptable compared to the reported AlGaIn/GaN HEMT with a similar structure [5]. To have a better understanding on the performance of fresh devices, the electron transport mechanisms were investigated. From I_G - V_G - T measurements, four different transport regions within the operation range were identified. In the forward bias region, the transport mechanism is mainly dominated by thermionic emission. On the other hand, in the reverse bias region, the current has three

components: mesa sidewall current ($I_{mesasidewall}$), vertical leakage current ($I_{vertical}$) and horizontal leakage current ($I_{horizontal}$). $I_{mesasidewall}$ is the main leakage path from the 0 V to V_{th} , $I_{vertical}$ mainly dominates from the V_{th} to the highest reverse bias, and $I_{horizontal}$ contributes to the addition voltage dependent current from -4 V (when the 2DEG is fully depleted) to the highest reverse bias.

Several leakage mechanisms are well understood [6-8]. Comparison of the experimental data obtained here with electric field simulations indicated that $I_{vertical}$ occurs through the FN tunneling mechanism at room temperature. Both the electrical properties and transport mechanisms are similar with other devices reported in the literature, which means the devices used in this dissertation are representative of these devices in general. Thus, the degradation mechanism discussed in this dissertation is not a unique failure mechanism.

When the devices were stressed under forward gate bias, I_{G-leak} increased dramatically and rapidly, while no significant I_{D-sat} and V_{th} degradation was observed. During the stressing, the electrical characteristics of the Schottky contact was monitored. From the Schottky characteristics, the Schottky barrier height, ϕ_B , was found to decrease, while the ideality factor, η , increased over time. Both of these results suggest that the degradation takes place in the Schottky contact.

I_G - V_G measurements of stressed devices were made at different temperatures to investigate the electron transport mechanisms after stressing. Similar to fresh devices, there are still four different regions of behavior within the operation range. While the leakage current increased in all reverse bias regions in stressed devices, unlike unstressed devices, the voltage and temperature dependences on the leakage current were different. The much higher leakage current and the weaker temperature dependence between 0 V to V_{th} in stressed devices imply that the mesa sidewall current ($I_{mesasidewall}$) is not dominated anymore. As the Schottky barrier height is decreased, it becomes easier for electrons to across the AlGaN layer from the channel to the gate contact and contribute to the vertical leakage current ($I_{vertical}$). Thus, the leakage current is dominated by the $I_{vertical}$ in this region. On the other hand, the weak voltage dependence between -4 V to the highest reverse bias suggests

that the horizontal current ($I_{horizontal}$) is not playing an important role with the region under the gate fully depleted. Same as the fresh devices, $I_{vertical}$ is still the main leakage current between V_{th} to -4 V. Thus, the $I_{vertical}$ is dominated in the entire reverse bias region. The temperature dependence of the $I_{vertical}$ indicates that PF emission, rather than FN tunneling, becomes the dominant transport mechanism in these regions after stressing, which is further supported by the physical characterization.

Several material characterization techniques were used to investigate the physical origin of the degradation. Based on previous studies, the PEM technique was used to locate high leakage paths along the gate contact. TEM lamellae at high leakage path areas were prepared using an FIB to investigate if there was any physical change in the degraded devices. From chemical analysis (i.e. EELS and EDX), carbon was observed in the stressed devices but not in the fresh ones. As carbon has a lower work function than nickel, it reduces the overall work function and therefore the barrier height in the high leakage areas. This increases both the thermionic emission and PF currents. Furthermore, there is a high chance that carbon could replace Al or Ga to create C_{Al} or C_{Ga} . It has been reported that C_{Al} or C_{Ga} can be electron donors in AlGa_N or Ga_N, which contributes to the enhancement of PF emission.

It is postulated that the carbon comes from photoresist residue that is present on the semiconductor surface after the lift-off process used to make the gate Schottky contact. the residue is expected to be randomly and inhomogeneously distributed on the semiconductor surface. During stressing, it is proposed that this carbon residue (hydrocarbon) carbonizes and carbon migrates into the adjacent nickel grain with the assistance of electric field. Thus, the gate metal was contaminated by carbonized residue and therefore the barrier height was lowered. This leads to the increase of I_{G-leak} over time during forward gate bias stressing. Based on this finding, carbon is detrimental for AlGa_N/Ga_N HEMTs reliability. A clean surface between Ni/AlGa_N is critical in order to improve the device lifetime. Therefore, the lift-off process, especially the descum process, should be optimized to enhance the reliability under forward gate bias.

Devices have been stressed at different gate voltages and the degradation is highly accelerated by the applied voltage. High gate voltage not only induces high energy electrons, but also provides a large number of electrons to enhance the carbonization process.

There are a few other studies showing similar degradation as discussed in this dissertation. However, these studies focused mainly on electrical characterizations, and no material characterization to support the origin of physical degradation was shown. This dissertation provides a methodology to investigate HEMT device degradation, by combining both electrical and material characterizations as well as computer-aided simulations. With this procedure, device degradation can be understood more comprehensively.

7.2 Future work

In this dissertation research, a comprehensive study was conducted to investigate how an AlGaIn/GaN HEMT device failed during forward gate bias stressing. What was found is that the stressing voltage (electric field) is the primary driving force causing the carbonization and leading to the degradation. However, there are still some future work which can be done to provide a more complete understanding of the degradation mechanisms.

To provide a complete picture, a large population of samples is required. The devices used in this thesis were from another research group, thus the sample availability was limited which made any further investigation difficult. Thus, in the following sections, some experiments are proposed which may further the understanding of this study.

7.2.1 Statistical study

As a limited number of devices were available for testing, it is difficult to carry out a statistical study. However, it is always interesting and important to learn the failure distribution for devices under any given stressing condition stressing. With a larger number of samples, this could be achieved by stressing more devices at different voltages. Testing of more devices under the same stressing conditions would also provide a more accurate

understanding of the failure time distributions needed for reliability projections. This could lead a deeper understanding of the failure and therefore have a better prediction for the device lifetime.

As the photoresist residue is believed to be randomly distributed across the wafer and correlated to the increase of leakage current, it is also important to investigate where the residue is located and confirm that the residue causes failure during forward gate bias stressing. This could be done by conducting a series of experiments. First, during the device fabrication, inline inspection tools, such as scanning electron microscopes (SEM), could be used to locate carbon residue after the photoresist removal. Then, when the devices are fully fabricated, the devices would be subjected to forward gate bias stressing. After the stressing, the devices with high leakage current could be located on the wafer. By mapping the carbon residue regions and the high leakage current regions together, it be possible confirm the role of residue in device degradation and also make comparisons of statistical variations in residue amounts and locations with statistical variations of lifetimes. This would also provide a systematic method for improvement of descum cleaning processes during the device fabrication.

7.2.2 Temperature dependence study

It is important to understand how the temperature affects the degradation. As the carbonization process can be temperature accelerated, it is interesting and important to understand how the temperature could enhance this process. Furthermore, GaN HEMTs are aimed to work under high temperature and for high power applications, so temperature plays a significant role in real applications. It is important to investigate the temperature dependence of degradation to extrapolate device degradation rates to different application conditions.

In a study of temperature dependence, devices should be stressed under at least three and preferably more different temperatures (e.g. 25 °C, 75 °C, 125 °C) with three stress voltages. Thus, this study could indicate whether the degradation is more voltage accelerated or

temperature accelerated, which gives a deeper understanding of the carbonization process. Furthermore, it helps to benchmark the device safety region at higher temperature.

7.2.3 Constant current stressing

Based on the previous chapters, it has been shown that the stressing voltage has a critical effect on device degradation. In addition to the voltage, the gate current density is also high during stressing. This large current density provides a large number of high energy electrons to accelerate the carbonization process. During the carbonization process, the high energy electrons are responsible for breaking carbon-carbon chemical bonds. Thus, with a larger amount of high energy electrons across the gate contact, the carbonization process should be accelerated. As a large amount of high energy electrons will be present at high current densities, similar with the voltage accelerated experiments, the devices can be subjected to different current stressing conditions. Based on the previous results, the stressing current can be set to (a) fixed value(s) between 25 μA to 100 μA and the current could be applied to the devices with different gate widths (e.g. 20 μm , 40 μm , 80 μm) to induce different current densities. Then, based on the failure times under different stressing conditions, the dependence on the current density would be understood. .

7.2.4 Electroluminescence study

As indicated in chapter 6, photoemission microscopy (PEM) was implemented to locate the failure sites. As only signals from the high I_{G-leak} devices were detectable and these devices were already at the final stages of stressing, it was not possible to investigate how the photon intensity depends on I_{G-leak} during stressing. However, if the sensitivity of the InGaAs camera is improved, it will be very interesting to look at this dependence, as it may indicate how the luminescence is generated. For example, if the logarithm of the intensity/ I_{G-leak} has a linear dependence on the reciprocal of the electric field, it could suggest that the luminescence comes from hot electron injection [9]. With the improvement in the camera sensitivity, it is possible to detect the hotpot with the devices having relatively low I_{G-leak} , so the failure analysis could be done at the early stage of stressing. In this case, carbonization process and carbon diffusion process could be investigated by conducting TEM/EELS at different stressing time.

It is also useful to integrate a spectrometer with the PEM system, because the spectral information of the hotspot could provide information of the trap energy [10]. As it is believed the number of donors is increased after stressing due to carbon impurities, the spectral information could provide supportive evidence showing the increment of donor concentration.

7.2.5 Devices with different process techniques

From the degradation hypothesis, it is believed that the degradation is due to the carbonization of the photoresist residue. The photoresist residue comes from the lift-off process. It is important to understand why this residue was left after the process. As mentioned in the previous chapter, descum process was introduced to clean the photoresist residue. Multiple parameters, such as process temperature, plasma power and gas flow rate affect the cleaning process, which leads to different photoresist loss [11]. In order to investigate the efficiency of a descum process, it is necessary to understand the impact of these parameters. Also, in-line inspection tools (e.g. SEM) have to be implemented to check for photoresist residue. By working with the process group to modify the descum process, it is possible to use different parameters during the lift-off process to investigate which method could improve the device reliability.

In this dissertation research, the gate material of the devices was Ni/Au. As the carbonization energy of hydrocarbon on a Ni surface is 1.5 eV, this energy could be reachable under the operation conditions. The low carbonization energy leads to the reliability problem, especially under forward gate bias. Thus, it is proposed to fabricate a device with other gate metals, such as Pt and Pd, which have a higher carbonization energies and may improve device reliability [12]. In this way, the device may have a longer lifetime when subjected to forward gate bias.

In conclusion, future work could provide a more complete picture of the degradation mechanism under forward gate bias. This would help understand how the electric field, temperature and current affect the carbonization process. It would also help in

identification of operation regimes for best reliability under a variety of working conditions. Furthermore, modification of the device fabrication process may help to improve the device reliability under forward gate bias condition.

References

1. Joh, J., L. Xia, and J.A.d. Alamo. *Gate Current Degradation Mechanisms of GaN High Electron Mobility Transistors*. in *2007 IEEE International Electron Devices Meeting*. 2007.
2. Marcon, D., J. Viaene, P. Favia, H. Bender, X. Kang, S. Lenci, S. Stoffels, and S. Decoutere. *Reliability of AlGaIn/GaN HEMTs: Permanent leakage current increase and output current drop*. in *Physical and Failure Analysis of Integrated Circuits (IPFA), 2013 20th IEEE International Symposium on the*. 2013. IEEE.
3. Axelsson, O., M. Thorsell, K. Andersson, and N. Rorsman, *The Effect of Forward Gate Bias Stress on the Noise Performance of Mesa Isolated GaN HEMTs*. IEEE Transactions on Device and Materials Reliability, 2015. **15**(1): p. 40-46.
4. Christiansen, B.D., E.R. Heller, R.A. Coutu, R. Vetury, and J.B. Shealy, *A very robust AlGaIn/GaN HEMT technology to high forward gate bias and current*. Active and Passive Electronic Components, 2012. **2012**.
5. Arulkumaran, S., S. Vicknesh, G.-I. Ng, L. Selvaraj, and T. Egawa, *Improved Power Device Figure-of-Merit ($4.0 \times 10^8 \text{ V}^2 \Omega^{-1} \text{ cm}^{-2}$) in AlGaIn/GaN High-Electron-Mobility Transistors on High-Resistivity 4-in. Si*. Applied Physics Express, 2011. **4**: p. 4101.
6. Hayashi, K., Y. Yamaguchi, T. Oishi, H. Otsuka, K. Yamanaka, M. Nakayama, and Y. Miyamoto, *Mechanism study of gate leakage current for AlGaIn/GaN high electron mobility transistor structure under high reverse bias by thin surface barrier model and technology computer aided design simulation*. Japanese Journal of Applied Physics, 2013. **52**(4S): p. 04CF12.
7. Zhang, H., E. Miller, and E. Yu, *Analysis of leakage current mechanisms in Schottky contacts to GaN and Al 0.25 Ga 0.75 N / Ga N grown by molecular-beam epitaxy*. Journal of Applied Physics, 2006. **99**(2): p. 023703.

8. Mojaver, H.R. and P. Valizadeh, *Modeling the Reverse Gate-Leakage Current in GaN-Channel HFETs: Realistic Assessment of Fowler–Nordheim and Leakage at Mesa Sidewalls*. IEEE Transactions on Electron Devices, 2018. **65**(8): p. 3156-3162.
9. Meneghini, M., A. Stocco, N. Ronchi, F. Rossi, G. Salviati, G. Meneghesso, and E. Zanoni, *Extensive analysis of the luminescence properties of AlGaIn/GaN high electron mobility transistors*. Applied Physics Letters, 2010. **97**(6): p. 063508.
10. Meneghini, M., A. Stocco, M. Bertin, N. Ronchi, A. Chini, D. Marcon, G. Meneghesso, and E. Zanoni. *Electroluminescence analysis of time-dependent reverse-bias degradation of HEMTs: A complete model*. in *2011 International Electron Devices Meeting*. 2011.
11. Tiwari, C.S., Y.S. Lim, R. Fulton, J. Srinivasan, M. Gisinger, P. Flynn, and L.H. Mak. *Characterization of the Descum Process for Various Silicon Substrates*. in *Meeting Abstracts*. 2013. The Electrochemical Society.
12. Liao, M.-S., C.-T. Au, and C.-F. Ng, *Methane dissociation on Ni, Pd, Pt and Cu metal (111) surfaces—a theoretical comparative study*. Chemical physics letters, 1997. **272**(5-6): p. 445-452.

Appendix

1. Crystal structures of Si, GaAs, GaN, AlN

1.1 Si

Summary

Collection Code 51688

Struct. formula	Si	Structure type	Diamond#C(cF8)#Sn(alpha)
Cell parameter	5.43053(7) 5.43053(7) 5.43053(7) 9 9 9	Space group	F d -3 m S (227)
Cell volume	160.15 [Å ³]	Z	8
Temperature	room temperature	Pressure	atmospheric
Data quality	High quality		
Author	Toebbens, D.M.; Stuesser, N.; Knorr, K.; Mayer, H.M.; Lampert, G.	Title	E9: The new high-resolution neutron powder diffractometer at the Berlin neutron scattering center
Reference	Materials Science Forum (2001) 378, (*) Article ID * (p. 288-293)	DOI	10.4028/www.scientific.net/MSF.378-381.288

Details

Visualization

Published Crystal Structure

Interactive Visualization

Powder Pattern

Interactive Visualization

Chemistry

Sum. formula	Si1	Struct. formula	Si
Molecular weight	28.0860 [u]	Z	8
ANX formula	N	AB formula	A
Chemical name	Silicon		

Published Crystal Structure Data

Cell parameter	5.43053(7) 5.43053(7) 5.43053(7) 9 9 9	Space group	F d -3 m S (227)
Cell volume	160.15 Å ³	Z	8
Crystal system	cubic	Crystal class	m-3m
Laue class	m-3m		
Structure type	Diamond#C(cF8)#Sn(alpha)		
Pearson symbol	cF8		
Wyckoff sequence	a		
Calc. density	2.33 [g/cm ³]		
		Axis ratios	a/b b/c c/a
			1.0000 1.0000 1.0000

EL	Lbl	OxState	Wyck Symb	X	Y	Z	SOF	B
Si	1	+0.00	8 a	0.0	0.0	0.0	1	0.54(1)

Standardized Crystal Structure Data

Cell parameter	5.4305 5.4305 5.4305 90.000 90.000 90.000	Space group	F d -3 m Z (227)
Cell volume	160.15 Å ³	Z	8
Crystal system	cubic	Crystal class	m-3m
Laue class	m-3m		
Structure type	Diamond#C(cF8)#Sn(alpha)		
Pearson symbol	cF8		
Wyckoff sequence	a	Axis ratios	a/b 1.0000 b/c 1.0000 c/a 1.0000
Transformation info	REMARK Transformed from non-centrosymmetric setting.--> F d -3 m TRANS Origin 1/8 1/8 1/8		

EL	Lbl	OxState	Wyck Symb	X	Y	Z	SOF	B
Si	1	+0.00	8 a	0.1250	0.1250	0.1250	1	0.5400

Distances and Angles

Bibliography

Author	Toebbens, D.M.; Stuesser, N.; Knorr, K.; Mayer, H.M.; Lampert, G.	Title	E9: The new high-resolution neutron powder diffractometer at the Berlin neutron scattering center
Reference	Materials Science Forum (2001) 378, (*) Article ID * (p. 288-293)	DOI	10.4028/www.scientific.net/MSF.378-381.288
Get full text	by Google Scholar		

Experimental information

Temperature	room temperature	Pressure	atmospheric
Radiation type	Neutron	Sample type	Powder data
PDF calc.	01-070-5680		
Remarks	Rietveld profile refinement applied	Remarks	Temperature factors available

Additional information

Warnings	No R value given in the paper.
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Compare Published and Standardized Structure

Published Crystal Structure

Standardized Crystal Structure

1.2 GaAs

Summary

Collection Code 259414

Struct. formula	Ga As	Structure type	Sphalerite#ZnS(cF8)
Cell parameter	5.6455(1) 5.6455(1) 5.6455(1) 90 90 90	Space group	F -4 3 m (216)
Cell volume	179.93 [Å ³]	Z	4
Temperature	300 [K]	Pressure	atmospheric
Data quality	Standard quality	R-value	0.0287
Author	Lin, Kung-Liang; Lin, Chih-Ming; Lin, Yu-Sheng; Jian, Sheng-Rui; Liao, Yen-Fa; Chuang, Yu-Chun; Wang, Chuan-Sheng; Juang, Jenh-Yih	Title	Structural properties of pressure-induced structural phase transition of Si-doped GaAs by angular-dispersive X-ray diffraction
Reference	Applied Physics A: Materials Science & Processing (2016) 122, (2) Article ID 117 (p. 1-6)	DOI	10.1007/s00339-016-9660-3

Details

Visualization

Published Crystal Structure

Interactive Visualization

Powder Pattern

Interactive Visualization

Chemistry

Sum. formula	As1 Ga1	Struct. formula	Ga As
Molecular weight	144.6400 [u]	Z	4
ANX formula	AX	AB formula	AB
Chemical name	Gallium arsenide - silicon doped		

Published Crystal Structure Data

Cell parameter	5.6455(1) 5.6455(1) 5.6455(1) 90 90 90	Space group	F -4 3 m (216)
Cell volume	179.93 Å ³	Z	4
Crystal system	cubic	Crystal class	-43m
Laue class	m-3m		
Structure type	Sphalerite#ZnS(cF8)		
Pearson symbol	cF8		
Wyckoff sequence	c a	Axis ratios	a/b 1.0000 b/c 1.0000 c/a 1.0000
Calc. density	5.34 [g/cm ³]		

EL	Lbl	OxState	Wyck Symb	X	Y	Z	SOF	TF
Ga	1	+3.00	4 a	0	0	0	1	
As	1	-3.00	4 c	0.25	0.25	0.25	1	

Standardized Crystal Structure Data

Cell parameter	5.6455 5.6455 5.6455 90.000 90.000 90.000	Space group	F -4 3 m (216)
Cell volume	179.93 Å ³	Z	4
Crystal system	cubic	Crystal class	-43m
Laue class	m-3m		
Structure type	Sphalerite#ZnS(cF8)		
Pearson symbol	cF8		
Wyckoff sequence	c a	Axis ratios	a/b 1.0000 b/c 1.0000 c/a 1.0000
Transformation info	Multiple transformations possible, first one selected		

EL	Lbl	OxState	Wyck Symb	X	Y	Z	SOF	TF
Ga	1	+3.00	4 a	0.0000	0.0000	0.0000	1	
As	1	-3.00	4 c	0.2500	0.2500	0.2500	1	

Distances and Angles

Bibliography

Author	Lin, Kung-Liang; Lin, Chih-Ming; Lin, Yu-Sheng; Jian, Sheng-Rui; Liao, Yen-Fa; Chuang, Yu-Chun; Wang, Chuan-Sheng; Juang, Jenh-Yih	Title	Structural properties of pressure-induced structural phase transition of Si-doped GaAs by angular-dispersive X-ray diffraction
Reference	Applied Physics A: Materials Science & Processing (2016) 122, (2) Article ID 117 (p. 1-6)	DOI	10.1007/s00339-016-9660-3
Abstract	Pressure-induced phase transitions in n-type silicon-doped gallium arsenide (GaAs:Si) at ambient temperature were investigated by using angular-dispersive X-ray diffraction (ADXRD) under high pressure up to around 18.6 (1) GPa, with a 4:1 (in volume ratio) methanol-ethanol mixture as the pressure-transmitting medium. In situ ADXRD measurements revealed that n-type GaAs:Si starts to transform from zinc-blende structure to an orthorhombic structure [GaAs-II phase], space group Pmm2, at 16.4 (1) GPa. In contrast to previous studies of pure GaAs under pressure, our results show no evidence of structural transition to Fmmm or Cmcmm phase. The fitting of volume compression data to the third-order Birch-Murnaghan equation of state yielded that the zero-pressure isothermal bulk moduli and the first-pressure derivatives were 75 (3) GPa and 6.4 (9) for the B3 phase, respectively. After decompressing to the ambient pressure, the GaAs:Si appears to revert to the B3 phase completely. By fitting to the empirical relations, the Knoop microhardness numbers are between HPK = 6.21 and HA = 5.85, respectively, which are substantially smaller than the values of 7-7.5 for pure GaAs reported previously. A discontinuous drop in the pressure-dependent lattice parameter, N-N distances, and V/V ₀ was observed at a pressure of 11.5 (1) GPa, which was tentatively attributed to the pressure-induced dislocation activities in the crystal grown by vertical gradient freeze method. (orig.)		
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Experimental information

Temperature	300 [K]	Pressure	atmospheric
Radiation type	X-Ray	Sample type	Powder data
R-value	0.0287		
Remarks	Rietveld profile refinement applied	Remarks	Authors structure type

Additional information

Keywords	Semiconductor	Keywords	Phase transition
Comments	R = R(p)	Comments	Silicon-doped; charge carrier density: 1.75 x 10 ¹⁴ (cm ⁻³)
Comments	For a pressure of 16.4(1) GPa, see ICSD259415.		
Warnings	At least one temperature factor missing in the paper.		

Compare Published and Standardized Structure

Published Crystal Structure

HM:F -4 3 m
a=5.646Å
b=5.646Å
c=5.646Å
α=90.000°
β=90.000°
γ=90.000°

Standardized Crystal Structure

HM:F -4 3 m
a=5.646Å
b=5.646Å
c=5.646Å
α=90.000°
β=90.000°
γ=90.000°

1.3 GaN

Summary

Struct. formula	Ga N
Cell parameter	3.1972(12) 3.1972(12) 5.207(3) 90 90 120
Cell volume	46.10 [Å ³]
Temperature	100 [K]
Data quality	High quality
Author	Kaminski, M.; Podsiadlo, S.; Wozniak, K.; Dobrzycki, L.; Jakiel, R.; Barcz, A.; Psoda, M.; Mizera, J.
Reference	Journal of Crystal Growth (2007) 303, (*) Article ID * (p. 395-399)

Collection Code 157398

Structure type	Wurtzite#ZnS(2H)
Space group	P 63 m c (186)
Z	2
Pressure	atmospheric
R-value	0.0088
Title	Growth and structural properties of thick Ga N layers obtained by sublimation sandwich method
DOI	10.1016/j.jcrysgro.2006.11.338

Details

Visualization

Published Crystal Structure

HM: P 63 m c
a=3.197 Å
b=3.197 Å
c=5.207 Å
α=90.000°
β=90.000°
γ=120.000°

Interactive Visualization

Powder Pattern

Interactive Visualization

Chemistry

Sum. formula	Ga1 N1
Molecular weight	83.7270 [u]
ANX formula	AX
Chemical name	Gallium nitride - thick layer

Struct. formula	Ga N
Z	2
AB formula	AB

Published Crystal Structure Data

Cell parameter	3.1972(12) 3.1972(12) 5.207(3) 90 90 120
Cell volume	46.10 Å ³
Crystal system	hexagonal
Laue class	6/mmm
Structure type	Wurtzite#ZnS(2H)
Pearson symbol	hP4
Wyckoff sequence	b2
Calc. density	6.03 [g/cm ³]

Space group	P 63 m c (186)
Z	2
Crystal class	6mm

Axis ratios	a/b	b/c	c/a
	1.0000	0.6140	1.6286

EL	Lbl	OxState	Wyck Symb	X	Y	Z	SOF	U
Ga	1	+3.00	2 b	0.6667	0.3333	0.5912(2)	1	0.003(1)
N	1	-3.00	2 b	0.6667	0.3333	0.9688(2)	1	0.004(1)

EL	Lbl	U(1,1)	U(2,2)	U(3,3)	U(1,2)	U(1,3)	U(2,3)
Ga	1	0.002(1)	0.002(1)	0.003(1)	0.	0.	0.
N	1	0.003(1)	0.003(1)	0.004(1)	0.	0.	0.

Standardized Crystal Structure Data

Cell parameter	3.1972 3.1972 5.2070 90.000 90.000 120.000	Space group	P 63 m c (186)
Cell volume	46.10 Å ³	Z	2
Crystal system	hexagonal	Crystal class	6mm
Laue class	6/mmm		
Structure type	Wurtzite#ZnS(2H)		
Pearson symbol	hP4		
Wyckoff sequence	b2		
Transformation info	TRANS -x,-y,-z		

	a/b	b/c	c/a
Axis ratios	1.0000	0.6140	1.6286

EL	Lbl	OxState	Wyck Symb	X	Y	Z	SOF	U
Ga	1	+3.00	2 b	0.3333	0.6667	0.4088	1	0.0030
N	1	-3.00	2 b	0.3333	0.6667	0.0312	1	0.0040

EL	Lbl	U(1,1)	U(2,2)	U(3,3)	U(1,2)	U(1,3)	U(2,3)
Ga	1	0.002000	0.002000	0.003000	0.000000	0.000000	0.000000
N	1	0.003000	0.003000	0.004000	0.000000	0.000000	0.000000

Distances and Angles

Bibliography

Author	Kaminski, M.; Podsiadlo, S.; Wozniak, K.; Dobrzycki, L.; Jakiela, R.; Barcz, A.; Psoda, M.; Mizera, J.	Title	Growth and structural properties of thick Ga N layers obtained by sublimation sandwich method
Reference	Journal of Crystal Growth (2007) 303, (*) Article ID * (p. 395-399)	DOI	10.1016/j.jcrysgro.2006.11.338
Abstract	The synthesis and characterization of GaN thick layers are reported in this paper. The layers were prepared by sublimation sandwich method (SSM). Powder of GaN was used as the source of gallium and ammonia was used as the source of nitrogen. Sapphire with 3 μm GaN thin film grown by MOCVD was used as the substrate. The GaN layers having a current maximum size of 200 μm thickness and 10 mmx10 mm area were obtained. It is also shown that the crystals of best crystalline quality are obtained with a growth rate of 20 μm/h. Characterization of the layers was performed using rocking curve, maps of reflection, structure refinement and SIMS. Quality of the material is good.		
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Experimental information

Temperature	100 [K]	Pressure	atmospheric
Radiation type	X-Ray	Sample type	Single crystal
R-value	0.0088		
Remarks	Temperature factors available		

Additional information

Compare Published and Standardized Structure

Published Crystal Structure

HM: P 63 m c
a=3.197 Å
b=3.197 Å
c=5.207 Å
α=90.000°
β=90.000°
γ=120.000°

Standardized Crystal Structure

HM: P 63 m c
a=3.197 Å
b=3.197 Å
c=5.207 Å
α=90.000°
β=90.000°
γ=120.000°

1.4 AlN

Summary

Collection Code 257810

Struct. formula	Al N	Structure type	Wurtzite#ZnS(2H)
Cell parameter	3.11139(1) 3.11139(1) 4.97841(3) 90 90 120	Space group	P 63 m c (186)
Cell volume	41.74 [Å ³]	Z	2
Temperature	room temperature	Pressure	atmospheric
Data quality	High quality	R-value	0.0633
Author	Wang, J.; Zhao, M.; Jin, S.F.; Li, D.D.; Yang, J.W.; Hu, W.J.; Wang, W.J.	Title	Debye temperature of wurtzite AlN determined by X-ray powder diffraction
Reference	Powder Diffraction (2014) 29, (4) Article ID * (p. 352-355)	DOI	10.1017/S0885715614000542

Details

Visualization

Published Crystal Structure

HM: P 63 m c
a=3.111Å
b=3.111Å
c=4.978Å
α=90.000°
β=90.000°
γ=120.000°

Interactive Visualization

Powder Pattern

Interactive Visualization

Chemistry

Sum. formula	Al1 N1	Struct. formula	Al N
Molecular weight	40.9870 [u]	Z	2
ANX formula	AX	AB formula	AB
Chemical name	Aluminum nitride		

Published Crystal Structure Data

Cell parameter	3.11139(1) 3.11139(1) 4.97841(3) 90 90 120	Space group	P 63 m c (186)
Cell volume	41.74 Å ³	Z	2
Crystal system	hexagonal	Crystal class	6mm
Laue class	6/mmm		
Structure type	Wurtzite#ZnS(2H)		
Pearson symbol	hP4		
Wyckoff sequence	b2		
Calc. density	3.26 [g/cm ³]		
		Axis ratios	a/b b/c c/a
			1.0000 0.6250 1.6001

EL	Lbl	OxState	Wyck Symb	X	Y	Z	SOF	B
Al	1	+3.00	2 b	0.3333	0.6667	0	1	0.442(12)
N	1	-3.00	2 b	0.3333	0.6667	0.38459(33)	1	0.559(33)

Standardized Crystal Structure Data

Cell parameter	3.1114 3.1114 4.9784 90.000 90.000 120.000	Space group	P 63 m c (186)		
Cell volume	41.74 Å³	Z	2		
Crystal system	hexagonal	Crystal class	6mm		
Laue class	6/mmm				
Structure type	Wurtzite#ZnS(2H)				
Pearson symbol	hP4				
Wyckoff sequence	b2				
		</			

EL	Lbl	OxState	Wyck Symb	X	Y	Z	SOF	B
Al	1	+3.00	2 b	0.3333	0.6667	0.0000	1	0.4420
N	1	-3.00	2 b	0.3333	0.6667	0.3846	1	0.5590

Distances and Angles

Bibliography

Author	Wang, J.; Zhao, M.; Jin, S.F.; Li, D.D.; Yang, J.W.; Hu, W.J.; Wang, W.J.	Title	Debye temperature of wurtzite AlN determined by X-ray powder diffraction
Reference	Powder Diffraction (2014) 29, (4) Article ID * (p. 352-355)	DOI	10.1017/S0885715614000542
Get full text	by Google Scholar		

Experimental information

Temperature	room temperature	Pressure	atmospheric
Radiation type	X-Ray	Sample type	Powder data
R-value	0.0633		
Remarks	Rietveld profile refinement applied	Remarks	Temperature factors available

Additional information

Keywords	Semiconductor
Comments	R = R(p)

Compare Published and Standardized Structure

Published Crystal Structure

HM:P 63 m c
a=3.111Å
b=3.111Å
c=4.978Å
α=90.000°
β=90.000°
γ=120.000°

Standardized Crystal Structure

HM:P 63 m c
a=3.111Å
b=3.111Å
c=4.978Å
α=90.000°
β=90.000°
γ=120.000°

2. Simulation code

```
go atlas simflgs="-80 -P 1"
```

```
set polar=0.37
```

```
set t_algan=0.018
```

```
set dg_space=2
```

```
set al_comp=0.26
```

```
set Vg=0
```

```
set wf=5.2
```

```
set Rsd=4600
```

```
mesh width=1
```

```
x.mesh location=-3          spacing=0.5
```

```
x.mesh location=-2          spacing=0.1
```

```
x.mesh location=-1          spacing=0.5
```

```
x.mesh location=0           spacing=0.1
```

```
x.mesh location=1           spacing=0.4
```

```
x.mesh location=2           spacing=0.1
```

```
x.mesh location=2+($dg_space)/2 spacing=$dg_space/2
```

```
x.mesh location=2+$dg_space spacing=0.1
```

```
x.mesh location=2+$dg_space+1 spacing=0.5
```

```
y.mesh location=-0.3        spacing=0.05
```

```
y.mesh location=-0.08       spacing=0.01
```

```
y.mesh location=-0.04       spacing=0.01
```

```
y.mesh location=0           spacing=0.01
```

```
y.mesh location=$t_algan/2   spacing=0.005
```

```
y.mesh location=$t_algan     spacing=0.005
```

```
y.mesh location=0.5          spacing=0.1
```

```
y.mesh location=$t_algan+1   spacing=0.05
```

```
y.mesh location=15           spacing=3
```

```

region number=1 material=GaN y.min=$t_algan y.max=$t_algan+1 substrate
region number=2 material=AlGaN x.comp=$al_comp y.min=0 y.max=$t_algan
region number=3 material=Si3N4 y.max=0
region number=4 material=Silicon y.min=$t_algan+1 y.max=15

electrode name=source x.min=-3 x.max=-2 y.min=-0.04 y.max=0
electrode name=gate x.min=0 x.max=2 y.min=-0.08 y.max=0
electrode name=drain x.min=2+$dg_space x.max=2+$dg_space+1 y.min=-0.04 y.max=0
electrode name=substrate bottom

material material=GaN align=0.68 eab=0.16 \
    taun0=1e-9 taup0=2e-8 nsrhn=4e18 nsrhp=4e18 \
    d.tunnel=4e-6 me.sbt=0.20 mh.sbt=0.20

doping trap acceptor e.level=3.2 conc=2e17 sign=1e-15 sigp=1e-15 degen=2 gaussian
peak=0.9 region=1 char=0.38

doping trap e.level=3.2 donor conc=2e16 uniform region=1 sign=1e-15 sigp=1e-15
degen=2
doping trap e.level=3.2 donor conc=1e17 uniform region=2 sign=1e-15 sigp=1e-15
degen=2
doping trap e.level=3.2 donor conc=2e16 uniform region=4 sign=1e-15 sigp=1e-15
degen=2

inttrap donor e.level=3.23 density=3e13 degen.fac=2 sign=1e-12 sigp=1e-12 \
    intmaterial="Si3N4/AlGaN"
inttrap acceptor e.level=3.23 density=8e12 degen.fac=2 sign=1e-12 sigp=1e-12 \
    intmaterial="silicon/GaN" s.s

material align=0

```

```
models consrh auger fermi temp=300 print albrct
model fnord trap.tunnel trap.coulombic
model polarization calc.strain polar.scale=$polar
mobility region=1 GaNsat.n
impact selb material=GaN
```

```
interface neutralize y.min=1.02 y.max=1.02
```

```
contact name=gate workfunc=$wf
contact name=source workfunc=4.08 resist=$Rsd
contact name=drain workfunc=4.08 resist=$Rsd
contact name=substrate resist=1e11
```

```
method newton climit=1e-4 maxtraps=8 itlimit=60
output band.param con.band val.band charge polar.charge qss e.temp e.velocity ex.velocity
ey.velocity
solve init
```

```
#####for 2deg#####
save outfile=ganfet_doping_0.str
extract init inf="ganfet_doping_0.str"
extract name="2DEG_built_in" 1e-4 * area from curve(depth,impurity="Electron Conc"\
    material="All" mat.occno=1 x.val=1) \
    where x.min=-0.02 and x.max=0.5
save outf=ganfet_1.dat
```

```
#####for IV#####
#save outf=ganfet_0_subs.str
solve previous
solve vstep=0.1 vfinal=5 name=drain previous
```

```
log
outfile=ganfet_algan${t_algan}_polar${polar}_alcomp${al_comp}_wf=${wf}_Rsd${Rs
d}.log
solve previous
#solve vstep=0.05 vfinal=2 name=gate
solve vstep=-0.05 vfinal=-6 name=gate
log off
```