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Comparative Analysis of Si, SiC and GaN Field-Effect Transistors for DC Solid-State Power Controllers in More Electric Aircraft

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Abstract—A dc solid-state power controller (SSPC) is a semiconductor-based circuit breaker used for fault isolation in aerospace applications. Device selection is important to ensure the reliability and performance of the SSPC. In this paper, Si, SiC, and GaN field-effect transistors are compared under steady-state and transient conditions. Experimental results are presented to evaluate the performance and characteristics.

Index Terms—Solid state power controller, dc circuit breaker, dc system protection, more electric aircraft, wide bandgap semiconductor devices.

I. INTRODUCTION

Conventional aircraft are evolving towards more/all-electric aircraft (MEA/AEA), replacing the mechanical, pneumatic and hydraulic subsystems with their electrical counterparts. MEA/AEA provide many advantages such as high efficiency, reduced weight, extended control, less maintenance requirement and fuel saving [1]–[6]. Operational efficiency can further be improved by adopting dc power systems. Some of the notable advantages are absence of reactive power flow, no skin and proximity effect, easier integration of energy storage systems, reduced conversion stages and so on [7]–[10].

Despite the abovementioned advantages, fault isolation is one of the major challenges in these dc power networks due to the absence of current zero-crossing. Conventionally mechanical circuit breakers (MCBs) are used in almost all ac power distribution architectures. In dc systems, there are many disadvantages of MCBs such as higher weight and volume requirements, additional auxiliary circuit requirement, and slow response time, which can lead to catastrophic failure due to a very high fault current ramp rate [6], [7], [9]–[13]. To overcome these drawbacks, semiconductor-based solid-state circuit breakers are a promising solution for dc circuit protection.

A solid-state power controller (SSPC) is a semiconductor-based circuit breaker which has the advantage of fast fault isolation, improved controllability, reduced fault current magnitude, and advanced load management capability. Metal oxide semiconductor field-effect transistor (MOSFET) is one of the semiconductor devices widely used for this application due to the absence of PN junction knee voltage [9]–[14]. The emer-

gence of wide bandgap (WBG) semiconductor technology has pushed the limits of the FET devices [9], [10]. Parameters of these devices are dynamic and highly nonlinear. Prior research works characterizing these WBG FET devices were mainly focussed on converter application [15]. However, the key performance indicators of converter application are different from the circuit breaker application [16]. The semiconductor device not only needs to sustain the short circuit (SC) current, but also break the SC current to isolate the source and the load. Hence, experimental verification (circuit and thermal analysis) is necessary for the selection of appropriate device technology intended for SSPC applications.

On-state losses, case temperature, SC current breaking (SCCB) capability, peak voltage overshoot, fault current ramp rate and gate oxide capability are some of the main characteristics which should be considered while selecting an appropriate device for SSPC. Among the available GaN devices, GaN HEMT with low-voltage Si exhibits robust gate oxide (± 20 V) and requires a simple gate driver [15], which makes it more suitable for SSPC application. Among the available Si and SiC MOSFET devices, trench SiC and super junction Si MOSFETs are stated to have relatively low on-state losses [9], [17], [18]. In this paper, similar voltage and current rating of GaN HEMT [19], trench SiC [20], and super junction Si [21] FETs are selected for the comparison, as depicted in Table I.

The rest of the paper is organized as follows. Section II introduces the basics of SSPC devices. In Section III, the main characteristics of power semiconductors are presented and some comparisons are made for the SSPC application. Section IV summarizes the main conclusions of this paper.

II. SSPC OVERVIEW

Some of the main bidirectional SSPC topologies are diode-bridge, anti-series and anti-parallel configurations [10], [11], [13]. Diode bridge configuration require only one FET device to be turned on/off, but the power losses are higher compared to the other two topologies because three devices are in the load current path. Anti-series and anti-parallel configurations require two FETs, but the losses are lower than the diode bridge configuration. The anti-series configuration has an edge

TABLE I
ELECTRICAL RATING OF THE DEVICES

Part number	Technology	Manufacturer	Package	V_{DSS}	I_D
STW45N65M5	Si	STMicroelectronics	TO-247-3	650 V	35 A
SCT3060ALGC11	SiC	ROHM Semiconductor	TO-247-3	650 V	39 A
GAN063-650WSAQ	GaN	Nexperia	TO-247-3	650 V	34.5 A

Fig. 1. Anti-series SSPC topology.

over the anti-parallel configuration because it requires only one gate driver for both FETs. Hence, the anti-series configuration is the most commonly used SSPC topology [13], [22], illustrated in Fig. 1. During steady-state condition, devices are in the on-state conducting the full load current. During fault condition, devices are turned off by applying an appropriate gate voltage at its terminals. Current flowing in the circuit is diverted to the voltage suppressor, e.g., a transient voltage suppression (TVS) diode or a metal oxide varistor (MOV), which starts dissipating the energy stored in the line inductor. After a short while, current in the circuit decays to zero. In this paper, only one FET is considered as device under test (DUT) because transient characteristics of bidirectional SSPCs are predominantly depend on the conducting FET.

III. OPERATING CHARACTERISTICS OF Si, SiC AND GAN FETs

A. Steady-State Characteristics

During normal condition, the FETs conduct the full load current, which are characterized by an on-state resistance of value $R_{DS(on)}$. Hence, on-state losses of FETs are defined by the following expression:

$$P_{loss} = i_d^2 R_{DS(on)} \quad (1)$$

where, $R_{DS(on)}$ is a dynamic parameter. As inferred from the datasheet [19]–[21], the variation of $R_{DS(on)}$ with temperature for SiC device is much lower than Si and GaN. It can also be deduced from the datasheet that the on-state losses are lowest in GaN, followed by SiC, and finally Si for the majority of the operating temperature range.

The rated value of the steady-state current flowing through the semiconductor device can be selected based on the industry SSPC standards [13], [23]. It is required that the device should be able to withstand ten times the steady-state current for a time interval of 100 μ s. Following the safe operating area (SOA) curve, the maximum value of current that the device is capable of conducting for a short time pulse of 100 μ s is noted.

Fig. 2. Case temperature at constant current operation for: (a) Si, (b) SiC and (c) GaN DUT.

Taking a safety factor ≈ 4 , a steady-state current of ≈ 3 A has been considered. Current rating can be increased by connecting multiple devices in parallel. Some experiments are carried out to evaluate the case temperature for a constant current of ≈ 3 A flowing through the channel of the three devices, as shown in Fig. 2. It can be concluded that the GaN device is able to provide by far the best steady-state performance offering the lowest on-state losses and case temperature compared to SiC and Si. Despite of Si operating at a lower case temperature than SiC, the latter has an edge due to extra 25 $^{\circ}$ C margin in WBG semiconductors.

Fig. 3. (a) Physical structure and (b) thermal network of a semiconductor device.

B. Transient Characteristics

SCCB capability is predominantly influenced by the chip size and the material properties because, during a transient condition, the heat generated due to power loss is not transmitted instantly to the ambient atmosphere, instead it requires some time based on the time constant of the RC thermal network of the device, as shown in Fig. 3. Experiments are carried out to test the SCCB capability based on the parameters depicted in Table II and circuit configuration shown in Fig. 4. A TVS diode is used as the clamping circuit because it offers superior characteristics compared to surge arrestors [10]. In high power applications, the TVS diode can be replaced with a surge arrestor due to the high cost of these diodes [24]. A turn-on gate pulse is given to the DUT during which the current rises to a certain value and then the DUT is turned off, and the current is diverted to the TVS diode. In each subsequent experiment the gate pulse is increased by either 1 μ s or 0.5 μ s. To avoid saturation in inductor L_μ , an air-core inductor is designed with a wire having a cross-sectional area of 1.5 mm² using the methods stated in [25], [26]. The pulse width specified in this paper is generated by a digital signal processor.

Variation in the device characteristics during an SC fault condition is divided into four subintervals. To facilitate the analysis, a snapshot of current and voltage across the Si device for a gate pulse width of 35 μ s is shown in Fig. 5.

- During the subinterval t_1 , DUT is in the linear region, where it behaves as a resistor and the voltage drop across the device is very low. The current through the device increases very rapidly during this interval.
- During the subinterval t_2 , the current through the DUT reaches its upper limit and the channel enters the saturation region. The voltage across the device increases

TABLE II
EXPERIMENTAL PARAMETERS

Parameter	Value
V_{in}	270 V
L_μ	18.48 μ H
R_μ	70 m Ω
Pos. V_{gs}	$\approx +14$ V
Neg. V_{gs}	≈ -3 V ($V_{in} = 25$ V)
	≈ -7 V ($V_{in} = 270$ V)
C_{in}	1.5 mF

Fig. 4. Equivalent circuit for experimental verification.

Fig. 5. Experimental results for a 35- μ s gate pulse width at 270 V of Si DUT.

because it behaves as a current source and the device heats up very drastically during this interval.

- During the subinterval t_3 , the heat generated during the subinterval t_2 has caused an increase in the temperature of the device, which subsequently causes the device current to decrease, analogous to an inductor having a negative inductance value. Simultaneously, the voltage across the device increases to a value greater than the supply voltage. The current waveform continues to decrease until either the device is turned off or it reaches its thermal limits (device damaged).
- During the subinterval t_4 , the gate voltage is changed from a positive value to a negative one. The current flowing through the device is diverted to the TVS diode, which clamps the voltage across the device.

Repetitive test results for 270-V input voltage are shown in Fig. 6(a), where the breaking current is the value of the current flowing through the device just before the end of the respective pulse width. It can be concluded that the breaking current for Si and GaN device is much higher than for SiC

Fig. 6. Experimental results for a (a) repetitive test at 270 V, (b) 36-μs gate pulse width at 270 V of SiC DUT and (c) gate voltage and current comparison.

Fig. 7. Experimental results for a repetitive test at 25 V.

Fig. 8. Experimental results for a 50-μs gate pulse width at 25 V of GaN DUT.

when applying the same gate voltage pulse width. At 5 μs gate pulse width, represented by instant @, GaN DUT is damaged during the fault isolation stage. The length of the subinterval t_2 is less in the case of SiC than Si due to the smaller chip size of the former. At 35 μs gate pulse width, gate oxide of SiC DUT is damaged during the fault isolation stage. At 36 μs gate pulse width, represented by instant Ⓐ, the device channel is restricted to a lower current value due to the damaged gate oxide, as shown in Fig. 6(b).

A comparison of the gate voltage and gate current of a healthy SiC DUT with the damaged SiC DUT is shown in Fig. 6(c). It can be inferred from the plot that the leakage current and driving current to the gate have increased.

The Si and SiC devices are able to provide excellent SCCB capability, while the GaN device is not able to break and sustain short circuit current after few μs. Short circuit fault can be easily identified by measuring the voltage across the devices in the case of Si and SiC. However, in the case of GaN, due to low on-resistance and less SCCB capability, it might be difficult to reliably detect the fault.

1) *Effect of DC-Link Voltage:* DC-link voltage is reduced to 25 V and accordingly, a lower voltage rating TVS diode is connected across the device. Repetitive test results for 25 V input voltage, are shown in Fig. 7. It can be inferred from the

plot that the fault current and saturation current are reduced compared to the experimental results shown in Fig. 6(a). In addition, the devices are able to withstand SC fault for a much longer duration. At 50 μs gate pulse width, represented by instant Ⓒ, the GaN DUT is damaged during the fault isolation stage, as shown in Fig. 8. The GaN DUT is damaged in both voltage levels (25 V and 270 V) in the proximity of the saturation region due to inferior heat dissipation property and smaller chip size.

Snapshots of current and voltage waveforms for a gate pulse width of 45 μs for the three devices are shown in Fig. 9. The peak voltage overshoot across the device depends on the device parameters and leakage inductances in the circuit. It is much higher in the case of GaN, followed by Si, and finally SiC gives the least overshoot.

2) *Effect of Gate-Source Voltage:* Higher gate-source voltage is advantageous as the on-state losses are reduced due to the reduction in $R_{DS(on)}$ [20]. However, it affects some transient properties. Fig. 10 shows repetitive test results at 270-V DC link voltage for SiC DUT under two different gating conditions. It can be inferred from the plot that fault current increases with the increase in the gate-source voltage, due to which there is a reduction in the SCCB capability. At 30-μs gate pulse width, represented by instant Ⓐ, the SiC DUT

Fig. 9. Experimental results for a 45- μ s gate pulse width at 25 V for (a) Si, (b) SiC and (c) GaN DUT.

Fig. 10. Experimental results for a repetitive test at 270 V of SiC DUT under varying gate-source voltage.

at higher gate-source voltage is restricted to a lower current value due to the damaged gate oxide. The point of failure of SiC DUT at lower gate-source voltage is shifted to the right, represented by instant ②.

IV. CONCLUSION

In this paper, Si, SiC, and GaN-based FET devices have been compared for SSPC applications. The devices have been tested based on the steady-state characteristics (comprising of on-state losses and case temperature) and transient characteristics (comprising of rate of rise of fault current, peak voltage overshoot, and SSCB capability). The following conclusions are drawn from the study on the selected devices:

- *Steady-state characteristics:* On-state losses are the lowest in the case of GaN, followed by SiC and Si for the majority of the operating temperature range. Perceptibly, the GaN devices have the lowest case temperature followed by Si and SiC. The operating temperature range of WBG semiconductors (SiC and GaN) is from -55°C to $+175^{\circ}\text{C}$, which is 25°C more than the upper threshold limit of Si devices (-55°C to $+150^{\circ}\text{C}$). Due to this extra margin, the steady-state performance of SiC is better than Si.
- *Transient characteristics:* Under similar gating conditions, the point of failure is highly dependent on the material properties. Repetitive testing was done to evaluate

the point of failure and properties of the DUT. The fault current ramp rate is larger in the case of GaN and Si compared to SiC. Peak voltage overshoot is considerably higher in the case of GaN, followed by Si, which is slightly higher than SiC. SSCB capability of Si and SiC is significantly higher than GaN.

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