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A 0.007 mm² 0.6 V 6 MS/s Low-Power Double Rail-to-Rail SAR ADC in 65-nm CMOS

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Abstract—A 0.007mm² 0.6V 6MS/s 10b double rail-to-rail input range SAR ADC is implemented in 65-nm technology. The extended input range broadens the applications of the low-power SAR ADCs such as compute-in-memory. The proposed ADC occupies less area since it only needs additional two series-connected capacitors and a differential-difference comparator for double rail-to-rail operation. The set-and-down operation reduces the input-referred noise of the comparator by over ten times than complementary switching. The novel metal-insulator-metal and metal-oxide-metal capacitor hybrid cap-DAC architecture minimize the gain error of ADC. The prototype achieves SNR of 53.90-dB, SNDR of 52.12-dB, and SFDR of 60.39-dB, power of 12.98-μW, and FoM of 6.6-fJ/conv.-step.

Index Terms—double rail-to-rail, low-power, SAR ADC, compute-in-memory, power-efficient

I. INTRODUCTION

SUCCESSIVE approximation register (SAR) analog to digital converters (ADCs) have been used in numerous applications because of their low power and moderate speed characteristics [1]. Recently, area- and energy-efficient ADCs are highly demanded in compute-in-memory (CIM) for emerging applications like machine learning where multiply-accumulate (MAC) results in the form of analog signals are converted into multiple digital bits. Since ADCs occupy a large portion of overall power consumption and area [2], it is essential to minimize their power and silicon area. SAR ADC is a promising solution because it is highly digital in signals and compact in size.

One of the most effective methods of reducing the power of SAR ADCs is supply voltage scaling [3]. However, it is difficult to be applied to SAR ADCs for CIM because the conversion range is limited to equal or less than the rail-to-rail input voltage. Reducing the input range leads to a degradation in the signal-to-noise margin in the CIM, which lowers the throughput of the entire system [4].

In this paper, a low-power double rail-to-rail SAR ADC is proposed to broaden the applications of low-power SAR ADCs in CIM or other systems, as shown in Fig. 1. Double rail-to-rail SAR ADCs have been presented in [5] and [6]. However, they used Cap-DACs (CDACs) as a double, occupying most of the

Fig. 1. Concept of low-power double rail-to-rail SAR ADC with compute-in-memory application

SAR ADC area. Therefore, it is not suitable for CIM applications where the ADC size is critical. This paper proposes a double rail-to-rail SAR ADC using only one CDAC at a side to realize the desired function in a small area.

II. DOUBLE RAIL-TO-RAIL SAR ADC

Typical SAR algorithms cannot convert input voltage beyond the rail-to-rail. In an n -bit binary search SAR ADC, the convertible input range is $V_{DD} \sum_{k=1}^n |1/2|^k$, which is smaller than V_{DD} . To overcome this limitation, this paper proposes a double rail-to-rail SAR ADC as shown in Fig. 2. The proposed SAR ADC consists of floating-capacitor-DACs (FC-DACs), a differential-difference comparator (DDC), double-boost sample-and-hold (S/H) switches, and SAR logic. FC-DACs include floating capacitors (C_{FC}) between the main-DAC and the DDC to separate the input sampling nodes (V_{INP} , V_{INN}) and the floating nodes (V_{FP} , V_{FN}) from the top-plates of the DACs (C_{TOP_P} , C_{TOP_N}). The floating capacitors are large enough (312-fF) to meet the thermal and kick-back noise requirement. This configuration makes two different voltage levels (V_{INP} , V_{FP} / V_{INN} , V_{FN}) other than V_{CTOP} , and the conversion result of main DAC couples from V_{CTOP} to both V_{IN} and V_F equally. Since the FC-DACs adapt the monotonic set-and-down switching [7] for enhancing the comparator gain, redundancies are necessary for dynamic offset compensation. The DDC compares two

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Fig. 2. Proposed double rail-to-rail SAR ADC architecture.

differential inputs as explained in Eq. (1).

$$\text{COMP}_{\text{OUT}} = \begin{cases} 1 & , (V_{\text{INP}} - V_{\text{FN}}) - (V_{\text{INN}} - V_{\text{FP}}) > 0 \\ 0 & , \text{otherwise} \end{cases} \quad (1)$$

The double-boost S/H switches are for the linear sampling of the input that exceeds the supply voltage.

Fig. 3 describes the detailed switching procedure and its waveforms through an example of a 3-bit FC-DAC. For simplicity, only the case of MSB conversion of $V_{\text{INP}} > V_{\text{INN}}$ is described. In the sampling phase, the input nodes (V_{INP} , V_{INN}) track the input signals, and the floating nodes (V_{FP} , V_{FN}) are connected to V_{DD} . During this operation, the bottom plates of the DAC are set to V_{DD} for the monotonic set-and-down operation. After the sampling phase, the input nodes sample the input values and the floating nodes are connected to V_{DD} , thereby forming different initial values at two CDAC nodes. In the MSB conversion, the DDC determines the polarity of $(V_{\text{INP}} - V_{\text{DD}}) - (V_{\text{INN}} - V_{\text{DD}})$ by Eq. (1). With MSB = 1 detected by the DDC, the bottom-plate of the MSB capacitor $2C$ on the positive DAC switches to V_{SS} , while that of the negative DAC has no change. After that, $V_{\text{CTOP_P}}$ becomes $V_{\text{CTOP_P}} - 0.5V_{\text{DD}}$.

Fig. 3. A 3b conversion example of the floating-capacitor DAC: (a) switching procedure, (b) waveform of each node, and (c) effective voltage difference.

The change in the $V_{\text{CTOP_P}}$ lowers the voltage levels of the input and the floating nodes simultaneously by $0.5 \times V_{\text{DD}}$ (from V_{INP} to $V_{\text{INP}} - 0.5V_{\text{DD}}$, from V_{FP} to $V_{\text{DD}} - 0.5V_{\text{DD}}$) as depicted in Fig. 3(b). Accordingly, the equivalent voltage difference with the previous state in the positive node becomes V_{DD} for MSB conversion (Fig. 3(c)), which is doubled compared to the conventional scheme. Subsequent conversion cycles for MSB-1 to LSB are executed by the set-and-down switching operation through changing the bottom plates from V_{DD} to V_{SS} . As a result, the proposed ADC's convertible input range is extended to $\pm 2V_{\text{DD}}$. In this work, it is $0 \leq V_{\text{IN}} \leq 1.2$ with $V_{\text{DD}} = 0.6 \text{ V}$.

III. SET-AND-DOWN SWITCHING FOR GAIN ENHANCEMENT

Although the double rail-to-rail conversion enhances the convertible input range, the input signal above the supply voltage deteriorates the comparator's signal-to-noise ratio (SNR). The comparator SNR is dependent on the input voltage because the gain of the comparator is determined by the difference in discharging speed of V_{OP} and V_{ON} nodes in the amplification phase, as illustrated in Fig. 4. The comparator gain is expressed as follows [8].

$$A_v \approx \frac{g_{m_{\text{in}}} V_{\text{THN}}}{I_{\text{CM}}} \quad (2)$$

In other words, the larger the transconductance of the input transistor, the larger the difference in the discharging current. And the smaller I_{CM} increases the duration of amplification, accordingly improving the gain. Therefore, the comparator input voltage above the supply voltage considerably lowers the

Fig. 4. Operation of differential-difference comparator: (a) schematic of comparator and (b) Analysis of gain of pre-amplifier.

Fig. 5. Comparator input-referred noise versus comparator input common-mode voltage

gain of the comparator because the input transistors fall into the triode region, and the current increases at the same time. The lower comparator gain means that the comparator's input-referred noise increases in proportion to the input common-mode voltage, as shown in Fig. 5. In other words, the comparator's SNR degrades as the input common-mode voltage increases.

As shown in Fig. 6, the output voltages of the FC-DAC or the input voltages of the comparator are changed around two virtual voltage levels (V_{CMH} , V_{CML}). We set these points to the input common-mode of the comparator. The high and low common-mode voltages are set to V_{CMH} and V_{CML} . The input common-mode of the comparator affects the gain as described above. The range of the initial value of V_{CMH} is as follows, assuming $V_{INP} > V_{INN}$.

$$V_{DD} \leq V_{INP} \leq 2V_{DD} \quad (3)$$

$$V_{DD} \leq V_{CMH} = (V_{INP} + V_{FN}) / 2 \leq 1.5V_{DD} \quad (4)$$

When applying Eq. (4) to Fig. 5, the worst-case input-referred noise becomes 9.2 mV_{RMS} at $V_{CMH} = 1.5V_{DD}$, which is 6.2 bits in ENOB using the condition of 10-bit and $V_{IN} = \pm 1.2$ V. In the case of switching where the differential nodes move in a complementary manner [9] (Fig. 6(a)), the input common-mode voltage remains unchanged from the MSB conversion to the LSB conversion. Thus, one of the input common-mode (V_{CMH}) remains above V_{DD} . In other words, all of the conversions have to be performed under the poor input-referred noise conditions.

To resolve the above issue, this paper utilizes the set-and-down switching for lowering the input common-mode and improving the SNR of the comparator, as shown in Fig. 6(b). Although the initial condition of the input common-mode is the same as that of complementary switching, the set-and-down switching has the characteristic that the input common-mode continuously decreases as the comparison proceeds. The

Fig. 6. Example of the output of FC-DAC; (a) complementary switching and (b) set-and-down switching

Fig. 7. Effect on ADC gain error according to the position of parasitic capacitance

comparator input-referred noise matter is only needed to be concerned when the difference of the differential signal is small. Since SAR algorithm changes voltage in the direction of reducing signal difference, the number of noise-sensitive input difference cases increase as the conversion proceed. With set-and-down switching, input common-mode voltage with noise-sensitive input difference occurs lower than V_{DD} in most cases. Besides, the input-referred noise of the comparator improves as the conversion proceeds. Rarely, a noise-sensitive case appears near V_{DD} , but the input-referred noise of the comparator at V_{DD} is reasonable as 0.72mV_{RMS}.

IV. PROPOSED CDAC ARCHITECTURE

In the top-plate sampling SAR ADC, the gain error cannot be avoided due to parasitic capacitance. In the CDAC consisting of binary-weighted capacitors, the digital-to-analog conversion is conducted through charge redistribution [10]. The following equation determines the voltage change obtained from the charge redistribution.

$$\Delta V = \frac{C_u(1/2)^n}{C_{TOTAL}} \quad (5)$$

Here, C_u is unit capacitance, n is the n^{th} conversion cycle, and C_{TOTAL} is the sum of the binary-weighted capacitors. The parasitic capacitance other than C_{TOTAL} increases the denominator in Eq. (5), thus causing a gain error as shown in Fig. 7. In general, the gain error follows the following equation.

$$\text{Gain Error} = \frac{C_{TOTAL}}{C_{TOTAL} + C_{PAR_TOP}} \quad (6)$$

where C_{par_top} is the parasitic capacitance on the CDAC top plate. To reduce the top-parasitic capacitance, this paper implemented a customized-MOM capacitor (CMOM-CAP)

Fig. 8. Overall structure of CDAC (a) three-dimensional view of customized-MOM capacitor (b) Arrangement of Main CDAC and MIM capacitor

Fig. 9. The layout floorplan of the CDAC with redundancy.

wrapping the top-plate with the bottom-plate as shown in Fig. 8(a). The dark-colored metal indicates the bottom-plate and the light-colored metal represents the top-plate. The lowest metal (M1) connects the bottom-plate of the unit capacitor vertically to form a weighted capacitor. M2 and M7 wrap the top-plate formed by M3-M6 to reduce the parasitic capacitance between the top plate and the substrate. In M3, M4, and M6, the bottom-plate covers the top plate from the outside in the shape of a finger. This increases the capacitive density and reduces the area of the CDAC. A cross shape is employed in M5 for easier routing.

The unit capacitance of CMOM-CAP is 961-aF, and the parasitic capacitance at the top-plate is 41-aF, which is 5% of the unit capacitance. On the other hand, the bottom-parasitic capacitance is 423-aF, which is 51% of the unit capacitor. However, bottom-parasitic capacitance only increases CDAC driver's load and does not affect the gain error. The size of CMOM-CAP is $1.18 \times 1.24 \mu\text{m}^2$ including routing. The layout floorplan of the CDAC with redundancies adopts inter-digitization by the vertical connection as shown in Fig. 9.

The floating capacitor is used to implement the double rail-to-rail function, also it reduces the sampling capacitance seen from the input driver. The small sampling capacitance reduces the energy of the ADC input driver. However, as shown in Fig. 7, the floating capacitors cause much gain errors because not only the parasitic capacitance of the top-plate but also the bottom-plate are connected to the charge redistribution node. In the case of the binary-weighted capacitor, the bottom-parasitic capacitance simply increases the loading of the driver and does not affect the gain error. Note that only the top-parasitic capacitance, $512C_{\text{PAR_TOP}}$, and the parasitic capacitance of the redundancy, $73C_{\text{PAR_TOP}}$ affect the gain error as Fig. 7. But thanks to the small parasitic capacitance at the top-plate of CMOM-CAP, the parasitic effect from the main-DAC is only about 5%.

However, in the case of floating capacitors, the top-parasitic and the bottom-parasitic induce gain errors. Thus, using CMOM-CAP as a floating capacitor is inappropriate. Metal-insulator-metal (MIM) capacitor is challenging to use as a unit capacitor because of the large minimum capacitance, but it is suitable to be used as a floating capacitor due to its low parasitic. Fig. 8(b) shows the proposed hybrid CDAC configuration, consisting of CMOMs for binary-weighted capacitors and MIMs for floating capacitors. Fig. 10 explains the relationship between the CDAC configuration and the

Fig. 10. Reduction of the input range due to the gain error by capacitor type.

convertible input range. The parasitic capacitance of the conventional finger type and only the CMOM-CAP configuration decrease the input range by 30.5%, 29.5% in simulation, respectively. Since CMOM-CAP shifts the parasitic capacitance from the bottom-plate to the top-plate, the total gain error becomes similar to that of the finger type in this CDAC configuration. However, the proposed hybrid CMOM and MIM configuration only decrease the input range by 10% in measurement because of the reduced parasitic capacitance in the charge redistribution path. This work achieved the input range of $1.55 V_{\text{DD}}$ after including 12.5% redundancy.

V. MEASUREMENT RESULT

The proposed ADC is fabricated in 65nm CMOS. The core area of the ADC is only 0.007 mm^2 ($107 \mu\text{m} \times 67 \mu\text{m}$) as the die micrograph in Fig. 11. The sampling rate is 6 MS/s. The measured power dissipation is $12.98 \mu\text{W}$ with a distribution of 5% for the S/Hs, 16% for the comparator, 28% for the DACs, and 51% for the digital controls. Fig. 12 presents the measured static and dynamic performance at 6 MS/s. Since ADC input in CIM application is DC, static performance is important. DNL and INL show accurate performance as $+0.14/-0.09\text{LSB}$ and $+0.49/-0.46\text{LSB}$, respectively. At 100-kHz input, the measured SNR is 53.90-dB, SNDR is 52.12-dB and SFDR is 60.39-dB. Clock coupling into the input signal induced the harmonic distortion including even-order harmonics. Also, input-floating node mismatch degraded the performance. However, both can be eliminated or improved with careful layout. Table I compares the proposed ADC with other state-of-the-art works. This prototype implements a double rail-to-rail input range in a

Fig. 11. Die micrograph.

Fig. 12. Measured static and dynamic performance.

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART ADCs.

	SOVC16 [5]	ISSCC18 [6]	ESSCIRC17 [1]	This Work
Technology	90nm	90nm	65nm	65nm
Supply voltage(V)	0.3	0.4	1	0.6
Ideal input swing	$\pm 2V_{ref}$	$\pm 2V_{ref}$	$\pm V_{ref}$	$\pm 2V_{ref}$
Sample rate (MS/s)	0.6	0.27	20	6
Resolution (bit)	11	13	10	10
DNL (LSB)	0.63	0.45	3.3	0.14
INL (LSB)	0.72	0.75	3.2	0.49
Power (μW)	0.187	0.638	124	12.98
SNDR (dB)	58.7	73.57	52.7	52.12
FoM ($fJ/c.-s.$)	0.44	0.606	21.1	6.6
Active area (mm^2)	0.035	0.059	0.069	0.007

small area and achieves good static performance. Even though the works in [5] and [6] were implemented in 90nm technology, the area of the proposed ADC is still much smaller than them. Note that the employed general-purpose process for moderate speed ADC induces higher leakage current compared with the low-power process, which comes with higher power consumption and FoM compared to [5] and [6].

VI. CONCLUSION

In this paper, the low-power double rail-to-rail SAR ADC is proposed. By expanding the input range, the supply voltage scaled SAR ADC can be easily applied to systems such as CIM. The double rail-to-rail function is implemented only through a series-connected capacitor and DDC for area efficiency. Also, the input-referred noise of the comparator is improved through the set-and-down switching. Lastly, the gain error of ADC is minimized through the novel hybrid architecture of customized-MOM and MIM capacitors. The proposed work can be applied to various CIM arrays, requiring small area and wide conversion ranges.

REFERENCES

- [1] M. Liu, A. van Roermund and P. Harpe, "A 10b 20MS/s SAR ADC with a low-power and area-efficient DAC-compensated reference," *IEEE European Solid-State Circuits Conference (ESSCIRC)*, 2017, pp. 231-234
- [2] F. Su et al., "A 462GOPs/J RRAM-based nonvolatile intelligent processor for energy harvesting IoE system featuring nonvolatile logics and processing-in-memory," *Symposium on VLSI Technology (SOVT)*, 2017, pp. T260-T261
- [3] M. Zhang, C. Chan, Y. Zhu, and R. P. Martins, "A 0.6-V 13-bit 20-MS/s Two-Step TDC-Assisted SAR ADC With PVT Tracking and Speed-Enhanced Techniques," in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 54, no. 12, pp. 3396-3409, Dec. 2019
- [4] J. Zhang, Z. Wang and N. Verma, "In-Memory Computation of a Machine-Learning Classifier in a Standard 6T SRAM Array," in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 52, no. 4, pp. 915-924, April 2017
- [5] S. Hsieh and C. Hsieh, "A 0.44fJ/conversion-step 11b 600KS/s SAR ADC with semi-resting DAC," *IEEE Symposium on VLSI Circuits (SOVC)*, 2016, pp. 1-2
- [6] S. Hsieh and C. Hsieh, "A 0.4V 13b 270kS/s SAR-ISDM ADC with an opamp-less time-domain integrator," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2018, pp. 240-242
- [7] C. Liu, S. Chang, G. Huang, and Y. Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 45, no. 4, pp. 731-740, April 2010
- [8] B. Razavi, "The StrongARM Latch [A Circuit for All Seasons]," in *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12-17, Spring 2015
- [9] B. P. Ginsburg and A. P. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS With Split Capacitor Array DAC," in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 42, no. 4, pp. 739-747, April 2007
- [10] R. E. Suarez, P. R. Gray and D. A. Hodges, "All-MOS charge-redistribution analog-to-digital conversion techniques. II," in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 10, no. 6, pp. 379-385, Dec. 1975