Modulation and control strategies for neutral-point-clamped converters

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**MODULATION AND CONTROL
STRATEGIES FOR NEUTRAL-POINT-
CLAMPED CONVERTERS**

NEHA BENIWAL
Interdisciplinary Graduate School
Energy Research Institute @ NTU

2021

MODULATION AND CONTROL STRATEGIES FOR NEUTRAL-POINT- CLAMPED CONVERTERS

NEHA BENIWAL

Interdisciplinary Graduate School
Energy Research Institute @ NTU

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2021

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarized materials, and has not been submitted for a higher degree to any other University or Institution.

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Neha Beniwal

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

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Prof. Josep Pou

Authorship Attribution Statement

This thesis contains material from 7 papers published in the following peer-reviewed journals and from papers accepted at conferences in which I am listed as an author.

Chapter 2 is published as N. Beniwal, J. Pou, S. Ceballos, C. D. Townsend, G. Konstantinou, H. D. Tafti, and G. G. Farivar, “Feedforward modulation for the neutral-point-clamped converter with confined capacitor voltage ripples and reduced switching power losses,” *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 4426-4438, Apr. 2020. doi: 10.1109/TPEL.2019.2940077.

The contributions of the co-authors are as follows:

- Prof. J. Pou is the main PI of the project.
- Prof. J. Pou and Dr. S. Ceballos provided the initial project direction.
- I developed the modulation steps in collaboration with Prof. J. Pou and Dr. S. Ceballos.
- I did the initial simulations of the proposed modulation technique in MATLAB/Simulink.
- I built the hardware prototype and performed the experiments at #02-02 Laboratory, Energy Research Institute at NTU (ERI@N) under the supervision of Dr. C. D. Townsend, Dr. H. D. Tafti and Dr. G. G. Farivar.
- I analyzed the results and prepared the manuscript drafts.
- All the co-authors were involved in the discussion of results.
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- I performed the simulations in MATLAB/Simulink and analyzed the results. I also prepared the manuscript drafts.
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Neha Beniwal

*Dedicated to my Father, Dr. B. S. Beniwal,
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Abstract

This thesis presents modulation and control strategies for neutral-point-clamped (NPC) converters. These converters produce ac voltages with lower harmonic distortion and the switches operate with less switching frequencies than traditional two-level voltage-source converters. NPC converters are widely employed in grid integration of renewable energy sources like solar and wind energy, high-power motor drives, shunt active power filters, etc.

The NPC converters suffer from challenges such as, the subsequent increase in switching losses while controlling the capacitor voltage (CV) ripples, neutral-point (NP) voltage instability arising in the presence of nonlinear loads enriched in even-order harmonics, and the divergence of CVs in the presence of nonzero average NP current. The focus of this thesis is to address these challenges and develop more efficient modulation and control techniques for the NPC converters.

In order to find a trade-off solution between the CV ripple magnitude and the switching power losses, a new feedforward compensated modulation technique for the three-phase NPC converter is proposed in this thesis. With this technique, the CVs are limited within a predefined voltage band. An innovative feedforward compensation is introduced to avoid low-frequency distortion on the output voltages of the converter arising due to oscillations in the CVs. Limiting the CV ripples helps in the design of the NPC converter, since the maximum voltage that the dc-link capacitors and the power semiconductors have to withstand is predefined.

Though the proposed feedforward compensated modulation strategy offers a trade-off between the CV ripples and switching losses, its performance deteriorates in the presence of extreme nonlinear loads due to the tendency of the CVs to frequently bounce out of the voltage band leading to higher switching losses. In order to address this drawback, a band-limited three-level (BL-3L) modulation technique is proposed which aims to balance the average CVs without any substantial increase in the switch-

ing losses, thereby concentrating mainly on enhancing the steady state performance of the system. In addition to the predefined voltage band (applied to the CVs), a variable current band is applied to the phase currents. The size of the current band is varied based on the tendency of the operational condition to unbalance the NP. Therefore, the BL-3L modulation is another approach to have a trade-off between the CV ripples and the switching power losses, which ensures the average CVs are balanced even in the presence of nonlinear loads enriched in even-order harmonics.

For bipolar dc-bus applications of NPC converters like feeding multiterminal dc-loads, back-to-back systems and grid-connected photovoltaic (PV) systems, the main challenge is to generate the required nonzero average NP current which, if not compensated, causes the CVs to diverge and hence destabilizes the converter. In order to address this issue, a dual-mode modulation technique is proposed which utilizes the inherent capability of the NPC converter to generate the required average NP current and does not employ any additional hardware. This technique is developed analytically using ac-side voltages and currents, and is applicable for all bipolar dc-bus applications of the NPC converter with balanced CVs. The analytical solution also provides the maximum average NP current injection capacity of the NPC converter, which defines the stable operating region of the converter.

The applications of dual-mode modulation technique are limited to systems with balanced CVs. In order to extend this analysis to applications of the NPC converter with unbalanced CVs, a dual-input NPC inverter-based grid-connected PV system is considered. A control strategy is proposed for this system to asymmetrically control the PV arrays without incorporating any additional external circuit. This is achieved by employing an analytically developed linearization block, similar to the dual-mode modulation technique, which helps in generating the required NP current to counter for the difference in the PV currents.

Experimental results are obtained on a laboratory developed prototype to validate all the proposed modulation techniques under different operating conditions. Finally, this thesis summarizes the work that has been done and presents some directions for future research.

Table of Contents

Abstract	xv
Table of Contents	xvi
List of Figures	xxi
List of Tables	xxvii
List of Acronyms	xxix
1 Introduction	1
1.1 General Background	1
1.1.1 Diode-Clamped Multilevel Converters	2
1.2 Review of Previous Research	5
1.2.1 Capacitor Voltage Balancing Issue	6
1.2.1.1 Review of Capacitor Voltage Balancing Solutions	7
1.2.2 Generation of Nonzero Average NP Current	10
1.2.2.1 Review of Average NP Current Generation Solutions	11
1.3 Motivations and Objectives	13
1.4 Research Contributions	15
1.5 Organization of the Thesis	16
2 Feedforward Compensated Modulation Technique for Three-Phase NPC Converters	19
2.1 Introduction	19
2.2 Review of Two- and Three-Level Modulation Techniques	22
2.2.1 Two-Level Modulation	22
2.2.2 Three-Level Modulation	23

2.2.3	Performance of Two- and Three-Level Modulation under Different Loading Conditions	24
2.2.3.1	Balanced Loading Conditions	26
2.2.3.2	Unbalanced Loading Conditions	26
2.2.3.3	Nonlinear Loading Conditions	27
2.2.3.4	Distortion Analysis	28
2.3	Proposed Modulation Strategy	28
2.4	Experimental Results	36
2.4.1	Balanced Loading Conditions	36
2.4.2	Unbalanced Loading Conditions	38
2.4.3	Initial CV Imbalances	38
2.4.4	Nonlinear Loading Conditions	40
2.4.5	Distortion Analysis	42
2.5	Power Loss Analysis	43
2.6	Relation between Switching Losses and Voltage Band	45
2.7	Conclusions	46
3	Band-Limited Three-Level Modulation for Three-phase NPC Converters	49
3.1	Introduction	49
3.2	Proposed BL-3L Modulation Technique	51
3.3	Experimental Results	57
3.3.1	Balanced Linear Loading Condition	58
3.3.2	Linear Unbalanced Loading Condition	59
3.3.3	Nonlinear Loading Condition	60
3.3.4	Initial CV Imbalance	60
3.3.5	Distortion Analysis	61
3.4	Power Loss Analysis	62
3.5	Performance Comparison between Feedforward Compensated Modulation and the Proposed BL-3L Modulation	65
3.5.1	Comparison Among Different Modulation Techniques for the Three-Phase NPC Converter	67
3.6	Conclusions	68

4	Dual-Mode Modulation Technique for Dual-Input Three-phase NPC Converters	69
4.1	Introduction	69
4.2	Proposed Average NP Current Injection Strategy	71
4.2.1	Average NP Current Generation Mechanism	72
4.2.2	Proposed Linearization Block	74
4.2.3	Calculation of Maximum Average NP Current Injection Capability	76
4.3	Proposed Control Scheme	78
4.4	Experimental Results	81
4.4.1	Dynamic Performance of the Proposed Dual-Mode Modulation Technique	82
4.4.2	Steady State Performance of the Proposed Dual-Mode Modulation Technique	83
4.4.3	Performance of the Proposed Dual-Mode Modulation Technique under Excess Average NP Current Injection	86
4.5	Conclusions	87
5	Control Strategy for Dual-Input NPC Inverter-Based Grid-Connected Photovoltaic Systems	89
5.1	Introduction	89
5.2	Proposed Average NP Current Regulation Strategy	92
5.2.1	Average NP Current Generation Mechanism	92
5.2.2	Effect of Zero-Sequence Voltage on Average NP Current	95
5.2.3	Proposed Linearization Block	96
5.2.4	Calculation of Maximum Average NP Current Compensation Capacity	102
5.3	Proposed Control Strategy	103
5.3.1	Operating Principle	103
5.3.2	Control System	104
5.4	Experimental Results	106
5.4.1	Performance under Step Change of Irradiance	108

5.4.2	Performance under Linear Change of Irradiance	111
5.4.3	Performance with Asymmetrical PV Arrays	113
5.5	Comparative Analysis	115
5.6	Conclusions	116
6	Conclusions and Future Work	117
6.1	Conclusions	117
6.2	Future Work	120
	Appendix A Laboratory Prototype	123
	Appendix B State Machine Model	127
	List of Publications	129
	References	133

List of Figures

1.1	Three-phase NPC converter.	3
1.2	Multiphase NPC converter.	3
1.3	Multiphase four-level diode-clamped converter.	4
1.4	Functional diagram of a multiphase multilevel diode-clamped converter.	4
1.5	Current source on the dc side of a three-phase NPC converter.	6
1.6	Circuit diagram of a three-phase NPC converter with bipolar dc-bus.	11
2.1	Three-phase NPC converter feeding a linear and a nonlinear load.	20
2.2	Picture of the hardware prototype.	25
2.3	Balanced load with $m=1$ using: (a) Two-level modulation and (b) three-level modulation.	26
2.4	Unbalanced load with $m=1$ using: (a) Two-level modulation and (b) three-level modulation.	27
2.5	Nonlinear load with $m = 1$ using: (a) Two-level modulation and (b) three-level modulation.	27
2.6	Harmonic spectra of v_{ab} at $m= 0.7$ with: (a) Two-level modulation, and (b) three-level modulation.	28
2.7	Calculation of NP current and reference NP current.	29
2.8	Proposed feedforward compensated modulation technique.	30
2.9	Balanced load using proposed technique with CV range $[0.5V_{dc} \pm 5\%]$ at m : (a) 1, (b) 0.7, and (c) 0.4.	37
2.10	Balanced load using proposed technique with CV range $[0.5V_{dc} \pm 10\%]$ at m : (a) 1, (b) 0.7, and (c) 0.4.	37
2.11	Unbalanced load using proposed technique with CV range $[0.5V_{dc} \pm 5\%]$ at m : (a) 1, (b) 0.7, and (c) 0.4.	39

2.12	Unbalanced load using proposed technique with CV range $[0.5V_{dc} \pm 10\%]$ at m : (a) 1, (b) 0.7, and (c) 0.4.	39
2.13	Initial voltage imbalance operating with CV range $[0.5V_{dc} \pm 5\%]$ at m : (a) 1 and (b) 0.7.	40
2.14	Initial voltage imbalance operating with CV range $[0.5V_{dc} \pm 10\%]$ at m : (a) 1 and (b) 0.7.	40
2.15	Nonlinear load using the proposed technique with CV range $[0.5V_{dc} \pm 5\%]$ at m : (a) 1, (b) 0.7, and (c) 0.4.	41
2.16	Nonlinear load using the proposed technique with CV range $[0.5V_{dc} \pm 10\%]$ at m : (a) 1, (b) 0.7, and (c) 0.4.	41
2.17	Harmonic spectra of v_{ab} at $m=0.7$ with proposed modulation technique with CV range: (a) $[0.5V_{dc} \pm 5\%]$ and (b) $[0.5V_{dc} \pm 10\%]$	42
2.18	WTHD of the line-to-line voltage waveform at different modulation indices for a balanced load with proposed modulation technique.	43
2.19	Power losses comparison between the proposed modulation technique and two-level modulation. (a) Switching, (b) conduction, and (c) total power losses.	44
2.20	Power losses comparison between the proposed modulation technique and three-level modulation [53]. (a) Switching, (b) conduction, and (c) total power losses.	45
2.21	Switching losses at different phase angles and voltage bands (ΔV) at $m=1$ feeding: (a) A balanced linear load and (b) a nonlinear load.	46
3.1	Calculation of NP current and its reference.	52
3.2	Calculation of variable current band.	53
3.3	Flowchart diagram of the proposed BL-3L modulation technique.	55
3.4	Balanced linear load operating with BL-3L modulation technique at m : (a) 1, (b) 0.7, and (c) 0.4.	58
3.5	Linear unbalanced load operating with BL-3L modulation technique at m : (a) 1, (b) 0.7, and (c) 0.4.	59
3.6	Nonlinear load operating under the proposed BL-3L modulation technique at m : (a) 1, (b) 0.7, and (c) 0.4.	60
3.7	Initial CV imbalance using BL-3L modulation technique at m : (a) 1 and (b) 0.7.	61
3.8	Harmonic spectra of v_{ab} at $m=0.7$ with proposed BL-3L modulation technique with voltage band $[165V, 135V]$	61

3.9	Losses comparison between two-level modulation and the proposed BL-3L modulation with voltage band [765V, 735V]. (a) Switching, (b) conduction, and (c) total power losses.	62
3.10	Losses comparison between three-level modulation [53] and the proposed BL-3L modulation with voltage band [765V, 735V]. (a) Switching, (b) conduction, and (c) total power losses.	63
3.11	Switching losses under band-limited three-level modulation operating with: (a) Linear load and (b) nonlinear load.	64
3.12	Performance with nonlinear load under: (a) Feedforward compensated modulation with confined CV ripples [65] and (b) proposed band-limited three-level modulation.	65
3.13	Losses comparison between feedforward compensated modulation and BL-3L modulation. (a) Switching, (b) conduction, and (c) total power losses.	66
4.1	(a) Variation of maximum NP current over a fundamental time period, and (b) partial saturation under instantaneous NP current approach.	70
4.2	Waveforms of normalized phase voltage and current of phase 'a' with producing: (a) Zero $\bar{i}_{NP}$, (b) positive $\bar{i}_{NP}$ and (c) negative $\bar{i}_{NP}$	73
4.3	Compensating operation mode when: (a) $\alpha \leq 2\pi/3$ and (b) $2\pi/3 < \alpha \leq \pi$	74
4.4	Linearization block to calculate α for different power factor angles.	77
4.5	Variation of the maximum NP average current with respect to I_m under different modulation indices and load phase angles with $\delta = 0^\circ$	78
4.6	(a) Circuit diagram of a three-phase grid-connected NPC converter, and (b) picture of the hardware prototype.	79
4.7	Control scheme: (a) Generation of normalized reference ac-side voltages and (b) computation of duty cycles.	80
4.8	Dynamic performance of the proposed dual-mode modulation technique under different dc-load conditions: (a) Waveforms of v_{ab} , v_{C1} , v_{C2} , i_a , i_b and i_c and (b) waveforms of α (in rad), i_{NP} , $\bar{i}_{NPref}$ and $\bar{i}_{NP}$	82
4.9	Steady-state performance with balanced load: (a) Waveforms of v_{ab} , v_{C1} , v_{C2} , i_a , i_b and i_c , α (in rad), i_{NP} , $\bar{i}_{NPref}$ and $\bar{i}_{NP}$, (b) harmonic spectra of v_{ab} , (c) harmonic spectra of i_a , and (d) waveform of v_{CM}	84
4.10	Steady-state performance with unbalanced load: (a) Waveforms of v_{ab} , v_{C1} , v_{C2} , i_a , i_b and i_c , α (in rad), i_{NP} , $\bar{i}_{NPref}$ and $\bar{i}_{NP}$, and (b) harmonic spectra of v_{ab} , (c) harmonic spectra of i_a , and (d) waveform of v_{CM}	85
4.11	Total harmonic distortion of the line-to-line voltage (v_{ab}) at different values of α	86

4.12	Validation of maximum average NP current injection limits: Waveforms of v_{C1} , v_{C2} , α (in rad), $\bar{i}_{NPref}$ and $\bar{i}_{NP}$	86
5.1	Circuit diagram of a dual-input (PV1, PV2) three-phase NPC inverter-based grid-connected PV system.	90
5.2	Waveforms of normalized ac-side voltages, current and feedforward compensated duty cycles of phase a , i_{NP} and $\bar{i}_{NP}$ when the solar PV arrays are operating at different voltages generating: (a) Appropriately zero $\bar{i}_{NP}$, (b) positive $\bar{i}_{NP}$ and (c) negative $\bar{i}_{NP}$	93
5.3	Operating principle of the linearization block.	94
5.4	$I - V$ and $P - V$ curves for the two solar PV arrays operating at: (a) Same irradiance levels, (b) small difference in irradiance levels, and (c) large difference in irradiance levels.	103
5.5	Proposed control strategy: (a) DC-link voltage management, current controller, and (b) generation of converter voltage references and calculation of duty cycles using the linearization block.	105
5.6	Calculation of the duty cycles using a linearization block.	106
5.7	Picture of the hardware prototype.	107
5.8	Performance of the proposed control strategy when solar array PV2 operates under step change in irradiance: Waveforms of Irr_{PV1} and Irr_{PV2} , v_{PV1} and v_{PV2} , i_{PV1} , i_{PV2} , $\bar{i}_{NPref}$ and $\bar{i}_{NP}$, p_{PV1} , p_{PV2} and p_g , α (in rad).	109
5.9	Performance of the proposed control strategy when solar array PV2 operates under step change in irradiance: (a) PV1 operating points and (b) PV2 operating points.	110
5.10	Harmonic spectra of v_{ab} when Irr_{PV1} is 1000 W/m ² and Irr_{PV2} is: (a) 1000 W/m ² , (b) 800 W/m ² and (c) 600 W/m ²	110
5.11	Harmonic spectra of i_a when Irr_{PV1} is 1000 W/m ² and Irr_{PV2} is: (a) 1000 W/m ² , (b) 800 W/m ² and (c) 600 W/m ²	111
5.12	Performance of the proposed control strategy when solar array PV2 operates with linear change in irradiance: Waveforms of Irr_{PV1} and Irr_{PV2} , v_{PV1} and v_{PV2} , i_{PV1} , i_{PV2} , $\bar{i}_{NPref}$ and $\bar{i}_{NP}$, p_{PV1} , p_{PV2} and p_g , and α (in rad).	112
5.13	Performance of the proposed control strategy with asymmetrical PV arrays: Waveforms of Irr_{PV1} and Irr_{PV2} , v_{PV1} and v_{PV2} , i_{PV1} , i_{PV2} , $\bar{i}_{NPref}$ and $\bar{i}_{NP}$, p_{PV1} , p_{PV2} and p_g , and α (in rad).	114
5.14	Performance of the proposed control strategy with asymmetrical PV arrays: (a) PV1 operating points and (b) PV2 operating points. . . .	114
5.15	Circuit diagram of a conventional three-phase NPC inverter-based grid-connected PV system without NP connection [67, 68].	115

5.16	Performance comparison between the proposed control strategy employing dual-inputs of the NPC inverter and a conventional PV system without using NP connection.	116
A.1	Printed circuit board of the NPC phase leg.	124
A.2	Printed circuit boards of transmitter, receiver, voltage and current sensors.	124
A.3	Stacking of PCBs to build the NPC converter.	125
B.1	State-machine model.	127

List of Tables

2.1	Experimental Parameters	25
2.2	Simulation Parameters for Power Loss Analysis	43
3.1	Comparison Among Different Modulation Techniques	67
4.1	Experimental Parameters	82
5.1	Function $F(\theta, r, k)$ and Solution of α when $i'_{NPre f} \leq 0$ and $v_{PV1} \leq v_{PV2}$	99
5.2	Symmetrical Modifications to Calculate α	101
5.3	Calculation of $ \bar{i}_{NPmax} $ when $i'_{NPre f} \leq 0$ and $v_{PV1} \leq v_{PV2}$	102
5.4	Experimental and Simulation Parameters	107

List of Acronyms and Notations

A. List of Acronyms

BL-3L	Band-Limited Three-Level
CBPWM	Carrier-Based Pulsewidth Modulation
COM	Compensating Operation Mode
CV	Capacitor Voltage
EMI	Electromagnetic Interference
IGBT	Insulated-Gate Bipolar Transistor
MPP	Maximum Power Point
NOM	Normal Operation Mode
NP	Neutral Point
NPC	Neutral-Point-Clamped
NTV-SVM	Nearest Three-Vector Space-Vector Modulation
PI	Proportional Integral
PV	Photovoltaic
PWM	Pulsewidth Modulation
SVPWM	Space-Vector Pulsewidth Modulation
THD	Total Harmonic Distortion
WTHD	Weighted Total Harmonic Distortion

B. List of Notations

C_1, C_2	DC-link capacitors
$d_{NP_a}, d_{NP_b}, d_{NP_c}$	Duty cycles for connecting the three phases to the neutral-point
$d'_{NP_a}, d'_{NP_b}, d'_{NP_c}$	Feedforward compensated duty cycles for connecting the three phases to the neutral-point
$d_{l_a}, d_{l_b}, d_{l_c}$	Duty cycles for connecting the three phases to the negative dc-rail

$d'_{l_a}, d'_{l_b}, d'_{l_c}$	Feedforward compensated duty cycles for connecting the three phases to the negative dc-rail
$d_{h_a}, d_{h_b}, d_{h_c}$	Duty cycles for connecting the three phases to the positive dc-rail
$d'_{h_a}, d'_{h_b}, d'_{h_c}$	Feedforward compensated duty cycles for connecting the three phases to the positive dc-rail
E_{off}	Energy dissipated during turn-off of the semiconductor
E_{on}	Energy dissipated during turn-on of the semiconductor
f	Grid frequency
f_s	Carrier frequency
i_a, i_b, i_c	AC-side currents in abc frame
i_d, i_q	AC-side currents in dq frame
I_m	Maximum value of phase current
i_d^*, i_q^*	AC-side current references in dq frame
I_{d1}, I_{d2}	Bipolar dc-bus average currents
$\bar{i}_{off}$	Average neutral-point current generated due to zero-sequence voltage
i_{NP}	Neutral-point current
i_{NP_x}	Contribution of phase x to neutral-point current
$\bar{i}_{NP}$	Neutral-point current averaged over a fundamental period of the grid voltage
i_{NPmax}	Maximum instantaneous neutral-point current
$\bar{i}_{NPmax}$	Maximum average NP current injection capability of the neutral-point-clamped converter
i_{NPmaxa}	Minimum value of i_{NPmax} in a fundamental period of grid voltage
i_{NPmaxb}	Maximum value of i_{NPmax} in a fundamental period of grid voltage
i_{NPref}	Neutral-point current reference
$\bar{i}_{NPref}$	Neutral-point current reference averaged over a fundamental period of the grid voltage
$i_{NPref_{3L}}$	Neutral-point current reference calculated under three-level modulation
$i_{NPref_{BL}}$	Neutral-point current reference calculated under band-limited three-level modulation
i_{PV1}, i_{PV2}	PV array currents

i_+, i_-	Positive and negative sequence components of ac-side currents
$I_{SC_{PV1}}, I_{SC_{PV2}}$	Short-circuit PV currents
Irr_{PV1}, Irr_{PV2}	PV array irradiance levels
L	Grid connection filter inductor
m	Modulation index
p_{PV1}, p_{PV2}	PV array powers
R_{d1}, R_{d2}	Bipolar dc-bus resistive loads
v_a, v_b, v_c	AC-side phase voltages of the NPC converter
v_{ab}, v_{bc}, v_{ca}	AC-side line-to-line voltages of the NPC converter
v_d^*, v_q^*	AC-side voltage references of the NPC converter in dq frame
$v_{aREF}, v_{bREF}, v_{cREF}$	AC-side phase voltage references of the NPC converter in abc frame
v_a^*, v_b^*, v_c^*	Normalized ac-side phase voltage references of the NPC converter in abc frame
v_a', v_b', v_c'	Normalized ac-side phase voltage references of the NPC converter in abc frame after zero-sequence voltage addition
$v_{a0}', v_{b0}', v_{c0}'$	Locally-averaged output voltage of one phase of the converter respect to the neutral-point
v_{C1}, v_{C2}	DC-link capacitor voltages
V_{CE}	Collector-emitter voltage of the semiconductor
V_{Cmin}	Lower limit of the predefined capacitor voltage band
V_{Cmax}	Upper limit of the predefined capacitor voltage band
v_{CM}	Common-mode voltage
v_{dc}	DC-link voltage
V_{dc}^*	DC-link voltage reference
v_{ga}, v_{gb}, v_{gc}	Grid phase voltages
v_{off}	Total zero-sequence voltage
v_{offc}	Zero-sequence voltage based on capacitor voltage difference
v_{offm}	Min-max based zero-sequence voltage
$V_{OC_{PV1}}, V_{OC_{PV2}}$	Open-circuit PV voltages
v_{PV1}, v_{PV2}	PV array voltages

ΔV	Predefined tolerance band for the capacitor voltages
α	Duration of the compensating operation mode
δ	Phase angle difference between the converter's ac-side voltage and the grid voltage
ϕ	Phase angle difference between the ac-side current and the grid voltage
θ_g	Grid voltage angle

Chapter 1

Introduction

This chapter provides an introduction to neutral-point-clamped (NPC) multilevel converters and their applications. A survey of modulation strategies employed for controlling the NPC converters is also presented. Finally, motivations behind this work and the research contributions of this thesis are discussed.

1.1 General Background

The rising of renewable energy sources, adoption of electric vehicles, development of energy-efficient portable devices, and changing power infrastructure have led to a rapid growth in the field of power electronics [1–3]. Power electronics is the sub-discipline of electrical engineering which helps in the control and transfer of power in an electrical circuit by using power switches. It has wide applications, ranging from a small mobile charger to a large-scale solar energy converter [4].

High power applications require high values of currents and voltages. The current and voltage ratings of a converter are usually determined by the power semiconductors employed. Due to limited maximum rating of semiconductors, the switches are sometimes connected in parallel in order to obtain high currents and in series to obtain high voltages. The series-connected switches suffer from static and dynamic voltage sharing issues. One of the methods to stabilize the voltages across the switches is to clamp them using dc voltage sources or big capacitors. Multilevel topologies make use of this principle, which helps in achieving higher voltages, thus, they are employed in many high power applications [5–7]. Unlike conventional

two-level voltage source converters, multilevel converters produce ac voltages with less harmonic distortion and also operate with less switching frequencies. The popular multilevel converter topologies are flying capacitor converters, cascaded H-bridge converters, diode-clamped converters and modular multilevel converters.

The three-level diode-clamped converter is also known as the neutral-point-clamped (NPC) converter, although some references use the NPC terminology for the diode-clamped converters in general, whether it is a three-level converter or has more than three levels. In this study, the NPC converter refers to the three-level diode-clamped topology only. Since the NPC was introduced in 1981 [8], it has gained wide popularity and is currently used in variety of applications. The major advantages of using an NPC converter over other multilevel topologies are:

- It requires a lower number of capacitors. Even with the addition of clamping diodes, the standpoint cost of the NPC converter is still lower than other multilevel topologies due to fewer reactive components.
- Unlike the cascade converters, the NPC converter can be used with a single dc-link voltage source.

1.1.1 Diode-Clamped Multilevel Converters

The NPC converter is presented in Fig. 1.1. Clamping diodes are used to connect to the neutral point (NP) and hence provide an additional level to the output voltages of the converter. Thus, the dc-side of the NPC converter has a floating NP (0), a positive dc-rail (+1) and a negative dc-rail (-1). The three-phase NPC converter has been extended to multiphase systems, as shown in Fig. 1.2.

Fig. 1.3 shows an m -phase four-level diode-clamped converter. In a diode-clamped converter with n voltage levels, each phase requires $2(n-1)$ power switches and $(n-1)(n-2)$ clamping diodes. On the dc-side, $(n-1)$ capacitors are required, which provide $(n-2)$ middle points, in addition to the positive and negative dc-rails, which are used by all the phases. The functional diagram of an m -phase n -level diode-clamped converter is presented in Fig. 1.4. In this figure, T_{ij} represents the connection of i^{th} phase to j^{th} level and is equal to '1' when the two points are connected, otherwise it is '0'. Expression (1.1) sums up all the possible combinations of the single-pole

Fig. 1.1. Three-phase NPC converter.

Fig. 1.2. Multiphase NPC converter.

Fig. 1.3. Multiphase four-level diode-clamped converter.

Fig. 1.4. Functional diagram of a multiphase multilevel diode-clamped converter.

n -throw switches for each phase.

$$\sum_{j=0}^{n-1} T_{ij} = 1 \quad \text{with} \quad i = \{a, b, c, \dots, m\}. \quad (1.1)$$

Taking the lower dc-link voltage level as reference, the output voltage for each phase is given by,

$$v_{i0} = \sum_{j=0}^{n-1} \left(T_{ij} \sum_{p=1}^j v_{Cp} \right) \quad \text{with} \quad i = \{a, b, c, \dots, m\}. \quad (1.2)$$

Among the diode-clamped converters, the most successful topology is the NPC converter (or three-level diode-clamped topology). The NPC converter applications are widespread and include:

- Grid integration of renewable energy sources like wind [9–13] and solar [14–17].
- High power motor drives [18–22].
- Static reactive power compensators [23–27].
- High-voltage dc transmission systems [28, 29].
- Electric vehicles [30–32].

Despite its popularity, there are many challenges associated with the NPC converters that require deeper insights, as discussed under Section 1.2.

1.2 Review of Previous Research

The challenges encountered with NPC converters vary from applications- to- applications [11, 15, 33–39]. For systems with total dc-link voltage regulated and zero average NP current required [13, 16, 18–22, 30, 32], it is important to keep the dc-link capacitor voltages (CVs) balanced. The unbalance in the CVs is reflected on the ac-side, in turn, deteriorating the quality of ac-side voltages. However, for bipolar dc-bus applications of NPC converters like feeding multiterminal dc-loads, back-to-back systems and grid-connected PV systems [10–12, 14, 15, 17, 31], the main challenge is to generate the required nonzero average NP current to ensure the CVs operate at

their reference values. Lack of generalized solutions for different NPC converter-based applications also constitute a major issue.

Many modulation techniques have been presented in the literature to address these issues. Based on the type of pulsewidth modulation (PWM) employed, these techniques can be classified into two main categories, i.e., space-vector pulsewidth modulation (SVPWM) and carrier-based pulsewidth modulation (CBPWM). In addition, many authors have proposed solutions based on different controllers and by incorporating additional auxiliary converters. These challenges and solutions are discussed in detail in the subsequent subsections.

1.2.1 Capacitor Voltage Balancing Issue

The circuit diagram of a three-phase NPC converter is shown in Fig. 1.5, wherein the load/source is directly connected between the positive (+1) and negative (-1) dc-rails [13,16,18–22,30,32]. For such systems, the main challenge is to keep the CVs balanced.

Fig. 1.5. Current source on the dc side of a three-phase NPC converter.

Moreover, the NP suffers from low-frequency voltage ripples while operating under

high modulation indices and low load power factors [33,34]. These low-frequency CV ripples in turn increase the stress on the converter components and lead to low-frequency distortion in the ac-side voltages.

Pou *et al.* [36] have also discussed other challenges which appear when an NPC converter feeds unbalanced and nonlinear loads. Due to the presence of negative sequence currents under linear imbalances, the amplitude of the CV ripple is higher as compared to balanced linear loads. Moreover, odd-order harmonics from the nonlinear load result in additional low-frequency NP voltage ripples, while even-order harmonics can shift the NP voltage, leading to instability. This results in the employment of oversized power devices and dc-link capacitors.

Therefore, the CV balancing is a prominent issue which further intensifies under the aforementioned operating conditions.

1.2.1.1 Review of Capacitor Voltage Balancing Solutions

In the literature, various modulation techniques have been presented to address the issue of CV balancing, as discussed below:

- SVPWM-based solutions:

In order to keep the CVs balanced, Seo *et al.* [40] developed an SVPWM technique for a three-level inverter by extending the standard two-level SVPWM without using a lookup table. However, the computational complexity is high due to repeated coordinate transformations and shifting of the origin for the duty cycle calculations, which further exacerbates with the increase in the number of voltage levels. In [41], a feedforward modulation approach is proposed for accounting the CV imbalances on the space-vector diagram, and successfully eliminating low-frequency distortion on the output voltages. However, the low-frequency CV ripples are not limited and depend on the operating conditions. In [42], an SVPWM for high modulation indices along with NP voltage balancing is presented. The duty cycles are calculated for different ranges of modulation indices, elongating the control algorithm and therefore making its implementation more difficult. A modulation technique based on nearest-three-vector virtual SVPWM is presented in [43]. Though the technique achieves CV balancing for all modulation indices and power factors, the switching frequency

of the power devices increases significantly and additional high-frequency distortion is observed in the output voltages. An improved version of virtual SVPWM using feedforward compensation is presented in [44], which shows lower switching distortion in the output voltages, however, the subdivisions of the sectors increase the control complexity. In [45], the virtual SVPWM is optimized to develop a new modulation technique, which has lower number of commutations and produces less switching loss. However, the drawback of this technique is the increase in the CV ripples. An improved virtual SVPWM is presented in [46], which eliminates CV ripples with reduced common mode voltage. However, the power devices still switch at higher frequencies.

From the abovementioned SVPWM techniques, it is clear that reduction of the CV ripples is achieved at the cost of higher switching losses. Furthermore, the complexity of SVPWM techniques increase with the increase in voltage levels.

- CBPWM-based solutions:

Dordevic *et al.* [47] presented a comparison among two SVPWM and three CBPWM-based techniques. The results show superior performance of CBPWM techniques on account of execution time, implementation complexity and capability to be extended to multilevel and multiphase converters.

One of the first attempts to address the issue of CV balancing was made by Ogasawara and Akagi [48]. The authors presented a standard CBPWM technique with zero-sequence addition and analyzed the NP voltage variation based on the average current flowing in or out of the NP. They also discussed the importance of adding the zero-sequence voltages for controlling the NP voltage variation. In this modulation scheme, all the phases switch only between two consecutive voltage levels in each switching period, i.e., either between the positive or negative dc-rail and the NP rail. As a result, the observed CVs are sometimes unbalanced with this modulation scheme even after the zero-sequence voltage injection. In [49], another CBPWM technique was proposed wherein the authors used a searching-optimization and precise calculation algorithm to obtain an appropriate zero-sequence voltage to ensure voltage balance between the dc-link capacitors. However, the observed CV ripples are uncontrollable at high modulation indices and low power factors. Pou *et al.* [50] developed a CBPWM strategy-based on zero-sequence voltage injection obtained by using a duality between the nearest three-vector space-vector modulation (NTV-SVM) and si-

nusoidal PWM for mitigating NP voltage oscillations. However, this strategy fails to address the issue of NP voltage stability associated with nonlinear loads. In [51], a general modulation technique for multiphase NPC converters was proposed, wherein one phase is clamped either to the positive dc-rail, negative dc-rail, or to the NP, depending on the modulation index and the error between the reference NP current and the actual NP current. However, this technique also suffers from low-frequency CV ripples, where the ripple amplitude depends on the operating conditions of the converter. In [52], a CBPWM technique with the ability to completely remove the low-frequency ripples in the CVs is proposed. A different approach that achieves similar results, but with improved voltage balancing performance, is presented in [53]. This technique is referred as ‘three-level modulation’ and shows the capability to completely eliminate the CV ripples irrespective of the loading conditions. Though the three-level modulation mitigates the NP voltage issues, the switching losses increase substantially as one of the phases is chosen to switch in three voltage levels, i.e., positive dc-rail, NP rail and negative dc-rail, in one switching period.

Though the above-mentioned CBPWM techniques offer the advantage of simpler implementation as compared to SVPWM techniques, the elimination of CV ripples is still achieved at the cost of increased switching losses.

- Other solutions:

In addition to SVPWM and CBPWM-based solutions, many other solutions have been presented in the literature to address the issue of CV balancing. In [54], a three-phase NPC system is modeled and a predictive controller is used to control the system for power quality applications. However, as the number of phases and levels increases, the model becomes more complex and using predictive control becomes a cumbersome task. In [55], the authors used a current harmonic minimum PWM method in order to reduce the low-frequency NP voltage ripples. Firstly, the optimal 3-order and 9-order harmonic components are calculated, which are then utilized to minimize the current harmonic and low-frequency NP voltage ripple simultaneously. However, this method has operational limitations and might return no solution when the modulation index is large. Yin *et al.* [56] presented an observer-based sliding mode control consisting of three control loops (voltage balancing loop, voltage regulation loop and power tracking control loop). The resultant system ends up being complex

in terms of control structure and increased computations.

In [57], a compensation loop is incorporated with double-width PWM to provide natural balancing to the system. Natural balancing refers to the capability of the NP voltage to settle to half of the dc-link voltage naturally [58]. However, finding an optimal compensation signal with the system's intrinsic limitations is a cumbersome task. Other natural voltage balancing techniques using external circuits have also been proposed in the literature [59, 60], however the addition of extra circuit components increases the system's footprint and cost. As a result, it is generally preferred to develop modulation strategies to address the CV balancing issue rather than adding external circuits.

Many of the above-mentioned solutions also fail to achieve NP voltage stability under nonlinear loads. For a practical NPC converter system, it is very important to develop a solution which stabilizes the NP voltage under all loading conditions. Moreover, the presented techniques show the capability of CV ripple elimination at the expense of switching losses. Thus, finding a trade-off solution between the switching losses and the CV ripple magnitude is required.

From the above discussion, it can be concluded that the CBPWM-based solutions offer advantages in terms of reduced implementation complexity, easier extensibility to multiphase and multilevel systems as compared to the SVPWM-based and the predictive controller-based solutions. In addition, the system's footprint and cost under the CBPWM solutions is lower as compared to the auxiliary converter-based solutions. Thus, in this thesis, a CBPWM modulation strategy is developed to address the aforementioned challenges associated with the NPC converters.

1.2.2 Generation of Nonzero Average NP Current

Fig. 1.6 shows a generalized circuit of a three-phase NPC converter employing the dual-inputs at the dc-side [10–12, 14, 15, 17, 31]. The back-to-back converter can be regarded as a special case of this generalized circuit in which the current sources are replaced by another NPC converter. Similarly, these current sources can be a representation of multiterminal dc-loads or solar PV arrays. For a balanced bipolar dc-bus, such that $I_{d1} = I_{d2}$, no average current flows through the NP. However, a nonzero average NP current flows when unbalanced dc-loads/sources are connected to

the bipolar dc-bus ($I_{d1} \neq I_{d2}$) which, if not compensated, causes the CVs to diverge, and hence destabilizes the converter [38,39].

Fig. 1.6. Circuit diagram of a three-phase NPC converter with bipolar dc-bus.

1.2.2.1 Review of Average NP Current Generation Solutions

In order to generate the required nonzero average NP current under unbalanced dc-bus applications, many solutions have been presented in the literature.

- Auxiliary circuitry-based solutions:

In [11], the authors added an active current compensation device (constituted by a dc-dc boost converter) to the back-to-back NPC converter configuration to balance the dc-link CVs and to supply the additional average NP current required under unbalanced load conditions. The authors in [31] presented a new architecture to charge electric vehicles using the bipolar dc-bus of the grid-integrated NPC converter. An additional voltage balancing circuit (constituted by an extra phase leg) was also employed to facilitate the CV balancing and provide the required average NP current under all operating conditions. Naik

et al. [61] employed an additional auxiliary converter at the dc-link of the NPC inverter in order to achieve independent maximum power point (MPP) tracking of the split sections. The auxiliary converter helps in generating an average NP current to compensate the difference of the two PV array currents. It is constituted by four additional switches, two inductors and one capacitor, thus increasing the complexity of the system. A similar approach is presented in [17], wherein an auxiliary converter constituted by four switches and one inductor is incorporated to the dc-link of the NPC inverter. However, the auxiliary converter only operates under partial shading (when the power difference between the two PV arrays exceed 20%). An MPP tracking for both the PV arrays together, i.e., considering them as one unit, is achieved when the power difference is small. In spite of this, the additional cost of such auxiliary converters could partially overshadow the power generation gain during partial shading in large central inverter-based PV systems.

Thus, the addition of extra circuits and converters in all the previous approaches not only increases the switching losses, but also leads to a bulkier, more expensive and more complex system.

- PWM-based solutions:

Instead of employing additional circuitry, many authors have developed modulation techniques utilizing the inherent capability of NPC converter to generate the required nonzero average NP current and keep the CV balanced when operating with unbalanced dc-loads/sources. Park *et al.* [62] proposed a new CBPWM method to control the dc-link voltages asymmetrically without using any additional hardware. A zero-sequence voltage is utilized to achieve the asymmetric control. In addition, the shape of the carrier waveform is modified according to the instantaneous CVs. However, this modification becomes challenging to implement in real-time. Another solution is presented in [14], wherein the voltages of the two PV arrays connected to the dual-inputs of the NPC inverter are controlled asymmetrically by modifying the three-phase turn-on times. The reference voltages are also modified to reduce the effect of asymmetric CVs on the ac-side output voltage. In [15], a PWM technique based on virtual-space vectors is presented in order to independently control the PV array voltages for a multilevel diode-clamped converter. The authors have also discussed how the voltage control is limited by the operating modulation index

and irradiance difference between the PV arrays, implying that there is only a certain limit of average NP current that can be compensated by the NPC converter.

However, all the above-mentioned techniques fail to provide a quantitative analysis to determine the maximum average NP current compensation capability of the NPC converter.

- Other solutions:

One of the solutions for controlling back-to-back NPC converter-based wind energy systems is to apply the finite control set model predictive control (FCS-MPC) due to its inherent capability of handling multiple objectives and constraints for such nonlinear systems [9, 10, 12]. A CV balancing strategy using optimum-predictive control is also presented in the literature for bipolar back-to-back NPC converters employed in high-voltage dc transmission systems [28].

Although the dc-link CVs can be balanced with predictive control, it has a large computational complexity especially when the prediction horizon is greater than one.

From the above discussion, it is clear that the NPC converter has an inherent capability to generate the required average NP current without using any auxiliary circuitry. However, this current is limited and the aforementioned proposed solutions fail to determine the maximum average NP current compensation capability of the NPC converter. Moreover, the presented solutions are developed for particular applications and lack generality.

1.3 Motivations and Objectives

The growing renewable energy sector, electric vehicles, and power quality devices, encourage the development of new power electronic devices and novel converter topologies. Multilevel converter topologies are the mainstream option in medium- and high-power applications due to their inherent advantages, viz. the power switches have to withstand only a fraction of the voltages generated, the high quality of the waveforms, and the lower electromagnetic interferences (EMI) produced. Among the multilevel topologies, the diode-clamped converter is one of the most analyzed and

used topology, especially the three-level diode-clamped converter (or NPC converter). Nowadays, the NPC converters are being used for grid integration of renewable energy sources, static reactive power compensation, high voltage dc transmission, electric vehicles charging and high power motor drives [9–32].

One of the main challenges of this topology is that the dc-link voltage needs to be equally divided among the dc-link capacitors. A low-frequency NP voltage ripple appears when the converter operates with high modulation indices and low power factor loads, which in turn leads to distortion in the ac-side voltages [33,34]. Moreover, the CVs diverge in the presence of nonlinear loads with even harmonics [36]. Most of the solutions presented in the literature eliminate the CV ripples at the expense of increased switching losses, thus, reducing the efficiency of the system. Furthermore, many of these techniques also fail to demonstrate the NP voltage stability under nonlinear loads.

Another challenge is to generate the nonzero average NP current required under bipolar dc-bus applications of the NPC converter [38,39]. One of the commonly employed solutions is to employ auxiliary circuitry, however, this leads to an increase in system's footprint, cost and losses. Moreover, PWM-based solutions have been presented in the literature which utilize the inherent capability of the NPC converter to produce the required average NP current. However, these solutions fail to calculate the maximum average NP current compensation capability of the NPC converter.

The above-mentioned issues need further insights to enhance the performance of the NPC converters. Thus, the main objectives of this thesis are:

1. Find a trade-off between switching losses and NP voltage ripple magnitude.
2. Eliminate low-frequency distortion on the output voltages irrespective of loading conditions.
3. Develop generalized solutions to generate the required nonzero average NP current for all bipolar dc-bus applications employing the NPC converter with balanced and unbalanced CVs.
4. Determine the maximum average NP current compensation capability of the NPC converter analytically.

5. Develop a control strategy for a dual-input NPC inverter-based PV system (an example of a bipolar dc-bus application of NPC converter with unequal CVs) to asymmetrically control the PV arrays without incorporating any additional external circuit.
6. Build a hardware prototype of diode-clamped converter and validate the proposed modulation techniques experimentally.

The proposed techniques in this work aim to improve the performance of NPC converters and to extend their application fields further.

1.4 Research Contributions

Efficient and simpler modulation techniques for enhancing the performance of NPC converters have been developed in this thesis. These techniques have been validated experimentally on a laboratory prototype. The main contributions can be classified as,

1. Modulation techniques to achieve trade-off between switching losses and voltage ripple magnitude.
 - Objectives:
 - Understanding the operational challenges of the three-phase NPC converter.
 - Comparing different modulation techniques of the NPC converter.
 - Proposing enhanced modulation techniques for the NPC converter to achieve trade-off between the switching losses and the CV ripple magnitude.
 - Contributions:
 - Developed a feedforward modulation technique for the NPC converter with confined CV ripples with no low-frequency distortion and reduced switching power losses.
 - Proposed the band-limited three-level modulation technique to balance the average CVs irrespective of the loading conditions without any substantial increase in the switching losses.

2. Modulation techniques to generate the required nonzero average NP current.

- Objectives:
 - Understanding the need of nonzero average NP current in different NPC converter applications.
 - Finding an analytical solution to generate the required average NP current, considering balanced and unbalanced CVs.
 - Determining the maximum NP current compensation capability of the NPC converter.
- Contributions:
 - Developed a generalized dual-mode modulation technique to control the average NP current, which is applicable to all bipolar dc-bus applications employing the NPC converter.
 - Proposed a control strategy for dual-input NPC inverter-based grid-connected PV system to asymmetrically control the PV arrays without incorporating any additional external circuit.
 - Analytically calculated the maximum NP current compensation capability of the NPC converter with balanced and unbalanced CVs.

1.5 Organization of the Thesis

Chapter 1 has given a background on NPC converters and their applications. This includes a detailed analysis of various challenges associated with the operation of NPC converters. Different solutions based on CBPWM, SVPWM, auxiliary converters and other techniques presented in the literature to address these challenges have also been discussed. In addition, this chapter has provided the motivation behind this work and highlighted the research contributions of this thesis.

Chapter 2 presents a feedforward compensated modulation technique for the three-phase NPC converter with CV ripples confined within a predefined voltage band. The main aim of this technique is to find a trade-off between switching losses and CV ripple magnitude. A feedforward compensation is introduced to avoid low-frequency distortion on the output voltages of the converter arising due to oscillations

in the CVs. Experimental results are provided to evaluate the performance of the proposed technique.

Chapter 3 introduces the band-limited three-level (BL-3L) modulation technique for a three-phase NPC converter with an aim to balance the average CVs. In addition to the predefined voltage band proposed in Chapter 2, this technique employs a variable current band to avoid bouncing of CVs along the voltage band boundaries that occurs under certain loading conditions. The proposed BL-3L modulation technique presents a trade-off between switching losses and CV ripple magnitude under all operating conditions. This chapter also provides experimental results to validate the proposed BL-3L modulation technique.

Chapter 4 proposes the dual-mode modulation technique with the capability to generate an average NP current without employing any additional hardware. This technique is developed analytically and is applicable for all bipolar dc-bus applications of NPC converter with balanced CVs. The analytical solution also provides the maximum average NP current injection capacity of the NPC converter. Experimental results are obtained for a three-phase grid-connected NPC converter feeding dc-loads to validate the performance of the proposed dual-mode modulation technique.

Chapter 5 extends the dual-mode modulation technique to generate the required average NP current with unbalanced CVs. For this analysis, a dual-input NPC inverter-based grid-connected PV system is considered in this chapter. The solution not only aims to asymmetrically control the PV array voltages, but also to develop a complete control strategy taking into account even large differences of irradiance levels. This chapter also presents experimental results to verify the effectiveness of the proposed control strategy.

Chapter 6 summarizes the research contributions of this thesis and the obtained results. This chapter also includes suggestions for further scope of work in this area.

Chapter 2

Feedforward Compensated Modulation Technique for Three-Phase NPC Converters

This chapter proposes a new modulation technique with feedforward compensation for three-phase NPC converters. With the proposed technique, the CV ripples are allowed to vary within certain limits. As the CVs are allowed to oscillate, the modulation technique is developed with feedforward compensation to avoid low-frequency distortion on the output voltages of the converter. Experimental results are presented under different loading conditions to validate the proposed modulation technique.

2.1 Introduction

As discussed in Subsection 1.2.1, most of the solutions presented in the literature to keep the CVs balanced suffer from either large NP voltage ripples or high switching losses. Therefore, it is important to find a trade-off solution between the switching losses and the CV ripple magnitude to cater for applications with different requirements.

This chapter proposes a CBPWM approach, wherein CVs are constrained within a predefined voltage band defined by upper and lower voltage limits, for the system shown in Fig. 2.1. If the CVs reach the limits, one phase switches in three voltage

levels for one or more switching periods to prevent the CVs exceeding the limits. Since the CVs are allowed to oscillate with this technique, a feedforward compensation is proposed to avoid low-frequency distortion in the ac voltages due to the CV imbalances. The proposed modulation technique produces less switching losses than [43, 52, 53]. Furthermore, it also ensures that the maximum voltages on the dc-link capacitors and switching devices are limited, unlike the conventional modulation techniques [48]. In fact, it offers a trade-off between the two requirements (reducing the switching losses and reducing the CV ripples).

Fig. 2.1. Three-phase NPC converter feeding a linear and a nonlinear load.

In most of the previously presented modulation techniques in the literature, the NP voltage ripple is dependent on the converter's operating conditions, thus, there are uncertainties in estimating the maximum voltage across the dc-link capacitors and the semiconductors of the converter. With the proposed modulation scheme, as the CV limits are predefined, the maximum voltage that the power semiconductors and dc-link capacitors have to withstand is also known. This fact is important to optimally design the NPC converter beforehand. As mentioned earlier, the various applications of the NPC converter includes grid-connected NPC converter, medium-voltage drives, grid interfacing of renewable energy resources such as wind and solar, etc. [13, 16, 18–22, 30, 32]. Whenever an unbalanced voltage sag occurs in such systems, a large voltage ripple is observed on the dc-link capacitors. As a result, generally, large bulky dc-link capacitors are employed to limit these ripples. Nevertheless, with the proposed modulation scheme, the CV ripples can be limited to predefined

values even under unbalanced loading conditions. This helps in employing less bulky capacitors at the dc-link, thereby, reducing the system's size and cost. Moreover, the switching losses obtained under the proposed modulation scheme are lower than the case of applying the three-level modulation [53] all the time. This further helps in reducing the operating cost of the converter.

The major advantages of the proposed feedforward compensated modulation technique are:

- As the maximum voltage across the capacitors is predefined, the converter can be optimally designed beforehand.
- There is no need for tuning gains or adjusting parameters because there are no controllers involved.
- When the CVs are within the specified limits, all the phases switch in two consecutive voltage levels, implying low switching losses and high quality output voltages.
- For the short intervals where one phase has to switch in three levels, the phase with additional transitions is carefully selected to reduce switching losses.
- No low-frequency distortion is produced in the output voltages thanks to the feedforward compensation implemented.

The chapter is organized as follows. Section 2.2 provides a review of the two- and three-level modulation techniques. Section 2.3 presents details of the proposed modulation technique. Section 2.4 presents experimental results for a three-phase NPC converter under balanced, unbalanced and nonlinear loading conditions. A power loss analysis comparing the two-level, three-level and the proposed modulation techniques is presented under Section 2.5. Section 2.6 aims to find a quantitative relation between the CV ripple and the switching losses. Finally, Section 2.7 summarizes the main conclusions of this chapter.

2.2 Review of Two- and Three-Level Modulation Techniques

Out of the presented solutions under Subsection 1.2.1 to address the issue of CV balancing, the conventional modulation technique wherein all phases switch in two consecutive voltage levels [48] and the three-level modulation technique [53] are among the prominently employed solutions.

2.2.1 Two-Level Modulation

In this thesis, a traditional CBPWM with min-max based zero-sequence voltage injection is utilized and is subsequently referred to as ‘two-level modulation’ [48, 53]. Under this modulation technique, all the phases switch in two consecutive levels, i.e., either they switch between the positive dc-rail and NP rail or between the negative dc-rail and NP rail, in each switching period. Consider that v_{aREF} , v_{bREF} and v_{cREF} are the phase voltage references to be generated. Firstly, these voltage references are normalized ($v_j^* \in [-1, 1]$) as:

$$v_j^* = \frac{v_{jREF}}{V_{dc}/2} \quad \text{for } j = \{a, b, c\}, \quad (2.1)$$

where, V_{dc} is the total dc-link voltage. A min-max based zero-sequence voltage is added to these normalized voltage references in order to extend the linear modulation region and to better utilize the dc-link voltage,

$$v_j' = v_j^* + v_{offm}, \quad (2.2)$$

where,

$$v_{offm} = -\frac{\max(v_a^*, v_b^*, v_c^*) + \min(v_a^*, v_b^*, v_c^*)}{2} \quad (2.3)$$

The obtained normalized phase voltages with zero-sequence addition are then utilized to calculate the duty cycles. If a phase is switching in two consecutive voltage levels, and the normalized modulation signal is positive, the phase will be switching between the positive dc-rail and the NP [48]. The duty cycles are calculated as:

$$d_{hj} = v_j', \quad d_{lj} = 0 \quad \text{and} \quad d_{NPj} = 1 - v_j', \quad (2.4)$$

where d_{h_j} , d_{l_j} and d_{NP_j} are the duty cycles for connecting phase j to the positive (+1), negative (-1) and NP (0) dc-rails, respectively. If the modulation signal v'_j is negative and the phase is switching in two levels, the corresponding phase will switch between the negative dc-rail and the NP. The duty cycles are given by:

$$d_{h_j} = 0, \quad d_{l_j} = -v'_j \quad \text{and} \quad d_{NP_j} = 1 + v'_j. \quad (2.5)$$

In general terms, the duty cycle of phase j connecting to the NP under two-level modulation is given by [48, 53]:

$$d_{NP_j} = 1 - |v'_j|, \quad (2.6)$$

and the duty cycles of phase j connecting to the negative and positive dc-rails are calculated as:

$$d_{l_j} = \frac{1 - d_{NP_j} - v'_j}{2}; \quad d_{h_j} = 1 - d_{NP_j} - d_{l_j}. \quad (2.7)$$

Accordingly, the NP current over a switching cycle is averaged as:

$$i_{NP} = d_{NP_a} i_a + d_{NP_b} i_b + d_{NP_c} i_c, \quad (2.8)$$

where i_a , i_b and i_c represent the three-phase currents.

The main advantage of employing the two-level modulation is lower switching losses, however the obtained CVs suffer from low-frequency ripples. Moreover, the tendency of the average CVs to diverge under the two-level modulation is dependent on the loading conditions. Under linear load, the average CVs are balanced, however, they can become unbalanced under nonlinear loads.

2.2.2 Three-Level Modulation

Lopez *et al.* [53] presented a modulation technique that aims to balance the instantaneous CVs by switching one phase in three levels when required. Switching a phase in three levels implies that the phase will switch among the positive dc-rail, NP and negative dc-rail in a switching period. This technique also incorporates the same min-max zero-sequence voltage injection (v_{off_m}) as calculated in (2.3). Firstly, the NP current is predicted using (2.6)-(2.8), assuming that all the phases switch in two voltage levels. The reference NP current, which is required to achieve CV balance

after one switching period, under three-level modulation is calculated as:

$$i_{NPref_{3L}} = 2C \frac{v_{C1} - \frac{V_{dc}}{2}}{T_s}. \quad (2.9)$$

In (2.9), C is the value of each dc-link capacitance, v_{C1} is the voltage of lower dc-link capacitor, and T_s is the switching period. Depending on the values of i_{NP} and $i_{NPref_{3L}}$, it is decided whether all the phases will switch in two levels, or one of them will be chosen to switch in three levels. Assume, phases ‘ y ’ and ‘ z ’ are switching in two levels (their NP duty cycles will be calculated using (2.6)) and phase ‘ x ’ is switching in three levels, then, the NP duty cycle for phase ‘ x ’ connected to NP is given by [53]:

$$d_{NP_x} = \frac{i_{NPref_{3L}} - d_{NP_y}i_y - d_{NP_z}i_z}{i_x}. \quad (2.10)$$

The duty cycles for all the phases connecting to negative and positive dc-rails are calculated using (2.7).

The three-level modulation helps in completely removing the low-frequency CV ripples and in attaining balanced CVs under all loading conditions. However, the major drawback is the substantial increase in the switching losses due to switching in three voltage levels.

2.2.3 Performance of Two- and Three-Level Modulation under Different Loading Conditions

The performance of two- and three-level modulation techniques are validated by employing a laboratory hardware prototype for the circuit diagram shown in Fig. 2.1. More details of the developed prototype are provided under Appendix A. The prototype is constituted by a three-phase NPC converter feeding a star-connected R-L load and a nonlinear load, as shown in Fig. 2.2. Hall-effect voltage (LV 25-P) and current (LA 55-P) are employed for sensing the voltages and currents, respectively. The proposed feedforward compensated modulation technique is implemented using dSPACE 1007 and a programmable DC power supply (Chroma 62050H-600S) is utilized to maintain the dc-link voltage. An oscilloscope (Yokogawa DLM4038) is employed to observe and record the waveforms. The experimental parameters of the system are provided in Table I.

Fig. 2.2. Picture of the hardware prototype.

Table 2.1: Experimental Parameters

Parameter	Value
DC-link voltage, V_{dc}	300 V
DC-link capacitors (each), $C1, C2$	130 μ F
Carrier frequency, f_s	2 kHz
AC-side frequency, f	5 Hz

The hardware prototype has large dc-link capacitors and, in order to obtain significant CV ripples at 50 Hz, very large currents would be required. The amplitude of the low-frequency CV ripple is proportional to the relationship $I_{rms}/(fC)$, where I_{rms} is the rms value of the output current, f is the fundamental frequency and C is the capacitance of the dc-link capacitors. From this relationship it can be observed that, if C is fixed and I_{rms} is limited, the CV ripples can be increased by reducing the operating frequency. Thus, the ac-side frequency is chosen 5Hz to obtain noticeable CV ripples with the corresponding value of dc-link capacitor.

The two- and three-level modulation techniques are tested under balanced, unbalanced and nonlinear loading conditions.

2.2.3.1 Balanced Loading Conditions

For this test, a balanced R-L load with the parameters $R_{a,b,c}=25\ \Omega$ and $L_{a,b,c}=6.3$ mH is star-connected to the converter, with switch S open in Fig. 2.1. Fig. 2.3(a) shows the waveforms of CVs (v_{C1} and v_{C2}), line-to-line voltage (v_{ab}) and load currents (i_a , i_b and i_c) at modulation index $m=1$ using the two-level modulation, while Fig. 2.3(b) shows the waveforms using the three-level modulation [53]. As it can be seen from these figures, using the two-level modulation, the average CVs are balanced but the CVs suffer from large low-frequency ripples. Under the three-level modulation, the low-frequency ripples are completely eliminated.

Fig. 2.3. Balanced load with $m=1$ using: (a) Two-level modulation and (b) three-level modulation.

2.2.3.2 Unbalanced Loading Conditions

Fig. 2.4(a) shows the same waveforms under an unbalanced load ($R_{a,b}=25\ \Omega$, $R_c=50\ \Omega$, $L_{a,b,c}=6.3$ mH, and switch S open) at $m=1$ using the two-level modulation, while Fig. 2.4(b) shows the waveforms using the three-level modulation [53]. Here, the degree of imbalance (i_-/i_+) is equal to 0.25. The CV ripples are almost double with this unbalanced load than with the balanced load under the two-level modulation (Fig. 2.4(a)). Using the three-level modulation, the CVs are balanced though at the price of more switching in three levels, thereby, increased switching losses.

Fig. 2.4. Unbalanced load with $m=1$ using: (a) Two-level modulation and (b) three-level modulation.

2.2.3.3 Nonlinear Loading Conditions

The switch S in Fig. 2.1 is closed to connect the half-bridge diode rectifier feeding a resistive load ($R_s = 104 \Omega$) to the NPC converter in addition to the star-connected R-L load ($R_{a,b,c} = 25 \Omega$ and $L_{a,b,c} = 11.3 \text{ mH}$). The added nonlinear load is highly enriched in second-harmonic currents which tends to cause CV instability [36]. Fig. 2.5 shows the performance of the two- and three-level modulation techniques under this nonlinear load with $m = 1$. From these results, it is visible that the average CVs are unbalanced under the two-level modulation, while the CVs are completely balanced under the three-level modulation.

Fig. 2.5. Nonlinear load with $m = 1$ using: (a) Two-level modulation and (b) three-level modulation.

2.2.3.4 Distortion Analysis

Fig. 2.6 shows the harmonic spectra of the line-to-line voltage (v_{ab}) using the two- and three-level modulation techniques obtained under balanced loading conditions at $m = 0.7$. In Fig. 2.6(a), low-frequency harmonics are present near the fundamental component of v_{ab} , i.e. between 0 Hz to 100 Hz, due to CV imbalances. As a result, the weighted total harmonic distortion (WTHD) obtained under the two-level modulation is higher. The three-level modulation technique produces voltages with larger total harmonic distortion (THD) compared to the two-level modulation, as it requires a phase to switch in three-levels within a switching period all the time [53].

Fig. 2.6. Harmonic spectra of v_{ab} at $m = 0.7$ with: (a) Two-level modulation, and (b) three-level modulation.

The aforementioned results verify that using the two-level modulation, the CVs suffer from low-frequency ripples and the average CVs are unbalanced under nonlinear loads enriched in even-order harmonics. The CVs are balanced under the three-level modulation irrespective of the loading conditions. However, the switching losses are higher and the produced ac-side voltages suffer from further distortion.

2.3 Proposed Modulation Strategy

The proposed modulation technique is a trade-off between the two- and three-level modulation techniques, and provides a compromised solution in terms of switching losses and CV ripple magnitude. With this technique, the CVs, v_{C1} and v_{C2} , are free to vary within a range $[0.5V_{dc} \pm \Delta V]$, wherein V_{dc} is the total dc-link voltage and ΔV represents the specified tolerance band for the CVs. In the proposed modulation strategy, when the CVs are within the specified limits, all the phases switch

in two consecutive voltage levels, i.e., under the two-level modulation. This helps in achieving lower switching losses and high quality output voltages. When the CVs are outside the limits $[V_{Cmin}, V_{Cmax}]$, one phase is chosen to switch in three voltage levels (similar to the three-level modulation technique) to ensure that the CVs stay within the limits. Here, V_{Cmin} represents $[0.5V_{dc} - \Delta V]$ and V_{Cmax} represents $[0.5V_{dc} + \Delta V]$. Thus, the three-level modulation is employed for short intervals to reduce the switching losses. However, the variation of CVs causes distortion in the ac-side voltages. A feedforward compensation is thus required to compensate for such voltage imbalances.

Figs. 2.7 and 2.8 show the various steps involved in the proposed modulation technique.

Fig. 2.7. Calculation of NP current and reference NP current.

Fig. 2.8. Proposed feedforward compensated modulation technique.

Firstly, the NP current and the NP current reference are estimated using the steps shown in Fig. 2.7. Depending on the obtained values of these currents, it is decided whether a phase will switch in two or three voltage levels (Fig. 2.8). The various steps involved are described next.

Step-I. Calculation of reference NP current

If the CVs are outside the $[V_{Cmin}, V_{Cmax}]$ band, the locally-averaged NP current needs to be regulated to achieve CV balance, which is calculated using (2.9) [53].

Step-II. Calculation of the NP current

The next step is to calculate the NP current to determine the switching pulses of the NPC converter. The step by step procedure to derive the NP current is illustrated in the following in accordance to Fig. 2.7.

- Calculation of normalized modulation signals.

The original normalized modulation signals are calculated using (2.1).

A zero-sequence (v_{off}) is added to these modulation signals such that:

$$v_{off} = v_{offm} + v_{offc}, \quad (2.11)$$

in which, v_{off_m} is calculated using (2.3) and,

$$v_{off_c} = \pm \frac{v_{C2} - v_{C1}}{v_{C2} + v_{C1}}. \quad (2.12)$$

Here, v_{off_c} is required to balance the average voltages of the dc-link capacitors. The sign in (2.12) for v_{off_c} is taken as positive when the converter operates as an inverter and negative when it operates as a rectifier. The normalized modulation signal with the added zero sequence is indicated as v'_j :

$$v'_j = v_j^* + v_{off} \quad \text{with} \quad j = \{a, b, c\}. \quad (2.13)$$

- Calculation of duty cycles without feedforward compensation.

Considering that all the three phases are switching in two consecutive voltage levels, the duty cycles without the feedforward compensation (d_{hj} , d_{lj} and d_{NPj}) are calculated using (2.6)-(2.7).

- Calculation of duty cycles incorporating feedforward compensation.

For mitigating the effect of CV imbalance on the ac side voltages, a feedforward compensation is incorporated as formulated below.

The locally-averaged output voltage of one phase of the converter (phase j) respect to the NP (v'_{j0}) is given by:

$$v'_{j0} = d_{hj}v_{C2} - d_{lj}v_{C1}. \quad (2.14)$$

If phase j is switching in two levels and the reference signal is positive, phase j will be switching between the positive rail and the NP [48], such that,

$$d_{lj} = 0 \quad \text{and} \quad v'_{j0} = d_{hj}v_{C2}. \quad (2.15)$$

Assuming the CVs are balanced, i.e., $v_{C1}=v_{C2}=V_{dc}/2$:

$$v'_{j0} = d_{hj} \frac{V_{dc}}{2}. \quad (2.16)$$

However, if the CVs are unbalanced, the duty cycle needs to be compen-

sated to produce the same reference voltage at the output, as follows:

$$v'_{j0} = d'_{h_j} v_{C2}, \quad (2.17)$$

where d'_{h_j} is the feedforward compensated duty cycle of phase j connecting to the positive dc-rail. The compensated duty cycle can be obtained from equating (2.16) and (2.17):

$$d'_{h_j} = d_{h_j} \frac{V_{dc}}{2v_{C2}} \quad (2.18)$$

The remaining duty cycles for phase j are calculated as follows:

$$d'_{l_j} = d_{l_j} = 0, \quad (2.19)$$

$$d'_{NP_j} = 1 - d'_{h_j}, \quad (2.20)$$

where d'_{l_j} and d'_{NP_j} are the feedforward compensated duty cycles of phase j connecting to the negative and NP rails, respectively. The duty cycles (2.18)-(2.20) are feedforward compensated; therefore, they produce the reference output voltage even under CV imbalances.

Similarly, if the reference signal is negative and phase j is switching in two levels, the corresponding phase will switch between the negative rail and the NP, such that:

$$d_{h_j} = 0 \quad \text{and} \quad v'_{j0} = d_{l_j} v_{C1}. \quad (2.21)$$

Again, assuming that the CVs are balanced, i.e., $v_{C1}=v_{C2}=V_{dc}/2$:

$$v'_{j0} = d_{l_j} \frac{V_{dc}}{2}. \quad (2.22)$$

However, for producing the same reference voltage when the CVs are imbalanced, the duty cycle needs to be compensated as:

$$v'_{j0} = d'_{l_j} v_{C1}. \quad (2.23)$$

From (2.22) and (2.23), the feedforward compensated duty cycles are

calculated as follows:

$$d'_{l_j} = d_{l_j} \frac{V_{dc}}{2v_{C1}} \quad (2.24)$$

$$d'_{h_j} = d_{h_j} = 0 \quad (2.25)$$

$$d'_{NP_j} = 1 - d'_{l_j}. \quad (2.26)$$

Thus, the modified duty cycles for phase j that is switching in two consecutive levels are obtained as:

$$d'_{h_j} = d_{h_j} \frac{V_{dc}}{2v_{C2}}, \quad (2.27)$$

$$d'_{l_j} = d_{l_j} \frac{V_{dc}}{2v_{C1}}, \quad (2.28)$$

$$d'_{NP_j} = 1 - d'_{h_j} - d'_{l_j}. \quad (2.29)$$

For the phase that is switching in three levels, calculation of the compensated duty cycles requires more elaboration. Let's suppose the phase that is switching in three levels is phase x , while phases y and z are switching in two levels. Phase x has to produce the desired locally-averaged output voltage for that phase, i.e.:

$$v'_{x0} = d'_{h_x} v_{C2} - d'_{l_x} v_{C1}. \quad (2.30)$$

Simultaneously, the NP current has to meet the NP current reference:

$$i_{NP} = d'_{NP_x} i_x + d'_{NP_y} i_y + d'_{NP_z} i_z = i_{NPref3L} \quad (2.31)$$

Since phases y and z are switching in two levels, their duty cycles are calculated using (2.27)-(2.29). From (2.31), the NP duty cycle for phase x can be obtained as follows:

$$d'_{NP_x} = \frac{i_{NPref3L} - d'_{NP_y} i_y - d'_{NP_z} i_z}{i_x} \quad (2.32)$$

Equation (2.32) provides the NP duty cycle for phase x to achieve the desired NP current. The other duty cycles for phase x (i.e., d'_{h_x} and d'_{l_x}) need to be calculated with the objective of generating the reference voltage for that phase, even under unbalanced dc-link CVs.

Since the sum of the three duty cycles has to be one at all times, the duty cycle for connecting phase x to the lower voltage level is:

$$d'_{l_x} = 1 - d'_{h_x} - d'_{NP_x}. \quad (2.33)$$

Substituting (2.33) in (2.30), and taking into account that $v_{C1} + v_{C2} = V_{dc}$:

$$d'_{h_x} = \frac{v'_{x0} + (1 - d'_{NP_x})v_{C1}}{V_{dc}} \quad (2.34)$$

The output voltage for phase x is related to its normalized magnitude as follows:

$$v'_{x0} = v'_x \frac{V_{dc}}{2} \quad (2.35)$$

Therefore, substituting (2.35) in (2.34):

$$d'_{h_x} = \frac{v'_x}{2} + \frac{(1 - d'_{NP_x})v_{C1}}{V_{dc}}. \quad (2.36)$$

The feedforward compensated duty cycles for the phase that is switching in three levels (phase x in this example) are given by (2.32), (2.33) and (2.36).

- Computation of NP current.

Using the calculated feedforward compensated duty cycles, the locally-averaged NP current over a switching cycle is calculated as:

$$i_{NP} = d'_{NP_a} i_a + d'_{NP_b} i_b + d'_{NP_c} i_c. \quad (2.37)$$

Step-III. Determination of phases switching in two or three levels and calculation of duty cycles

It is expected that all the phases will switch in two consecutive voltage levels most of the time. However, a phase may be required to switch in three levels if the CVs are outside the $[V_{Cmin}, V_{Cmax}]$ band. This will be determined at each switching period from v_{C1} , V_{Cmin} , V_{Cmax} and i_{NP} . All different possible cases are discussed in the following.

Case-I. $V_{Cmin} \leq v_{C1} \leq V_{Cmax}$

In this case, all the phases are switched in two consecutive voltage levels

as the CVs are within the limits. The duty cycles for all the phases remain the same as calculated in (2.27)-(2.29).

Case-II. $v_{C1} < V_{Cmin}$ and $i_{NP} \leq 0$

In this case, the voltage of the lower capacitor needs to increase. As the NP current goes in the direction to charge this capacitor, no special action is required and all the phases switch in two consecutive voltage levels. The duty cycles remain unchanged and are the same as in (2.27)-(2.29).

Case-III. $v_{C1} > V_{Cmax}$ and $i_{NP} \geq 0$

Since a positive NP current will decrease the CV v_{C1} , no further action is required. Therefore, all phases switch in two levels and the duty cycles remain the same as in (2.27)-(2.29).

Case-IV. $v_{C1} < V_{Cmin}$ and $i_{NP} > 0$

As $v_{C1} < V_{Cmin}$ and the NP current goes in the discharging direction, a phase switches in three levels to change the direction of the NP current. First of all, it is necessary to check what is the phase or phases that can change the direction of the NP current. For this, contribution of phase j to the NP current is eliminated by imposing $d'_{NP_j}=0$, and checking if i_{NP} using (2.37) changes its sign, i.e., $i_{NP} < 0$. The phases that meet this condition can be chosen to switch in three levels. In a three-phase system, there will be one or two phases that meet this requirement.

If only one phase can change the direction of the NP current, then that phase will be chosen to switch in three levels. In the case that two phases have the capacity to change the direction of the NP current, the phase with lower absolute value of the current is chosen to switch in three levels. This will minimize the switching power losses.

It is assumed that phase x is chosen to switch in three levels, and the other two phases are indicated as phases y and z . The duty cycles for phases y and z will remain unchanged, i.e., those calculated using (2.27)-(2.29), as both phases will be switching in two levels. The duty cycles for phase x will be calculated using (2.32), (2.33) and (2.36).

If the duty cycle calculated for d'_{NP_x} using (2.32) is negative, then d'_{NP_x} is imposed to be zero, and d'_{l_x} and d'_{h_x} are calculated with this assumption from (2.33) and (2.36), respectively. Under this condition,

phase x will be switching between the positive and negative dc-rails. The sign of the NP current will be such that it helps CV balance, although the reference current (2.9) will not be achieved.

Case-V. $v_{C1} > V_{Cmax}$ and $i_{NP} < 0$

In this case, the NP current will charge the lower dc-link capacitor further, which is already charged above the maximum voltage limit (V_{Cmax}). The NP current (i_{NP}) and the reference NP current ($i_{NPref3L}$) have opposite signs, similar to Case-IV, though the directions of the currents are opposite between these two cases. Again, in this case, one phase has to switch in three levels to be able to change the direction of the NP current. The process of determining the phase that switches in three levels and the corresponding duty cycles is similar to Case IV.

The calculated duty cycles (d'_{NPj} , d'_{lj} , d'_{hj}) are then compared with one carrier signal, using CB1 PWM technique mentioned in [63], to produce the switching pulses for all the power devices of the NPC converter via the state-machine model (Appendix B). The state machine model has been implemented in practice to avoid any forbidden commutation state of the converter.

2.4 Experimental Results

To validate the performance of the proposed feedforward compensated modulation technique, different experimental tests are performed on a hardware prototype with the specifications provided in Section 2.2.3.

2.4.1 Balanced Loading Conditions

Figs. 2.9 and 2.10 show the waveforms of v_{C1} , v_{C2} , v_{ab} , i_a , i_b and i_c for the proposed technique at different values of m under the same balanced loading conditions as discussed in Section 2.2.3.1 (Switch S open, $R_{a,b,c} = 25 \Omega$ and $L_{a,b,c} = 6.3 \text{ mH}$). Fig. 2.9 shows the results when the limits of the CVs are defined as $[0.5V_{dc} \pm 5\%]$, i.e., $[142.5\text{V}, 157.5\text{V}]$, for modulation indices $m = 1$, $m = 0.7$ and $m = 0.4$.

Fig. 2.9. Balanced load using proposed technique with CV range $[0.5V_{dc} \pm 5\%]$ at m : (a) 1, (b) 0.7, and (c) 0.4.

Fig. 2.10. Balanced load using proposed technique with CV range $[0.5V_{dc} \pm 10\%]$ at m : (a) 1, (b) 0.7, and (c) 0.4.

In Figs. 2.9(a) and 2.9(b), the proposed modulation technique alters between two- and three-level modulation, while in Fig. 2.9(c) the modulation operates only in two-level modulation as the CVs are within the specified limits even though all the phases switch in two levels.

The waveforms in Fig. 2.10 are obtained by applying the proposed modulation technique with voltage range $[0.5V_{dc} \pm 10\%]$, i.e., $[135\text{V}, 165\text{V}]$. Similar to the previous case, for $m=1$ and $m=0.7$, the proposed modulation alters between two- and three-level modulation and for $m=0.4$, it operates with two-level modulation all the time.

As it can be observed from Figs. 2.9 and 2.10, for most of the cases the CVs are maintained within the specified range and the load currents are sinusoidal despite CV imbalances, which is achieved thanks to the implemented feedforward compensation. However, in Figs. 2.9(a) and 2.10(a), the CVs go a bit beyond the predefined band. This is due to the presence of switching ripples, which can be mitigated if the switching frequency increases.

2.4.2 Unbalanced Loading Conditions

Figs. 2.11 and 2.12 show the same waveforms for the proposed technique operating with the unbalanced load employed in Section 2.2.3.2 (Switch S open, $R_{a,b}=25\ \Omega$, $R_c=50\ \Omega$, $L_{a,b,c}=6.3\ \text{mH}$). These results demonstrate that the proposed modulation can operate under unbalanced conditions, while maintaining the CVs within V_{Cmax} and V_{Cmin} and generating sinusoidal output currents.

2.4.3 Initial CV Imbalances

An initial voltage imbalance is forced on the dc-link capacitors, such that $V_{C1}=200\ \text{V}$ and $V_{C2}=100\ \text{V}$ under balanced R-L load condition. Figs. 2.13 and 2.14 show the same waveforms for different m . The CVs are quickly regulated within the defined $[V_{Cmin}, V_{Cmax}]$ band. Therefore, the proposed modulation technique has the capability to regulate the CVs irrespective of the initial voltage imbalance.

Fig. 2.11. Unbalanced load using proposed technique with CV range $[0.5V_{dc} \pm 5\%]$ at m : (a) 1, (b) 0.7, and (c) 0.4.

Fig. 2.12. Unbalanced load using proposed technique with CV range $[0.5V_{dc} \pm 10\%]$ at m : (a) 1, (b) 0.7, and (c) 0.4.

Fig. 2.13. Initial voltage imbalance operating with CV range $[0.5V_{dc} \pm 5\%]$ at m : (a) 1 and (b) 0.7.

Fig. 2.14. Initial voltage imbalance operating with CV range $[0.5V_{dc} \pm 10\%]$ at m : (a) 1 and (b) 0.7.

2.4.4 Nonlinear Loading Conditions

Figs. 2.15 and 2.16 show waveforms for the proposed technique for different m under nonlinear loading conditions as in Section 2.2.3.3 (Switch S closed, a half-bridge diode rectifier feeding a resistive load ($R_s = 104 \Omega$) in parallel to a star-connected R-L load ($R_{a,b,c} = 25 \Omega$ and $L_{a,b,c} = 11.3 \text{ mH}$)). Fig. 2.15 shows the results when the limits of the CVs are defined as $[0.5V_{dc} \pm 5\%]$ for modulation indices $m = 1$, $m = 0.7$ and $m = 0.4$. The proposed modulation technique applies three-level modulation for some intervals with $m = 1$ and $m = 0.7$, while for $m = 0.4$ the modulation operates only in two-level modulation as the CVs are within the specified limits, therefore all the phases switch in two levels. Fig. 2.16 shows the same waveforms with the CV limits as $[0.5V_{dc} \pm 10\%]$. From these figures, it is clear that the proposed modulation scheme is able to limit the CVs within the predefined voltage limits even when operating with nonlinear loads that inject second-harmonic currents.

Fig. 2.15. Nonlinear load using the proposed technique with CV range $[0.5V_{dc} \pm 5\%]$ at m : (a) 1, (b) 0.7, and (c) 0.4.

Fig. 2.16. Nonlinear load using the proposed technique with CV range $[0.5V_{dc} \pm 10\%]$ at m : (a) 1, (b) 0.7, and (c) 0.4.

2.4.5 Distortion Analysis

Fig. 2.17 shows the harmonic spectra of v_{ab} with the proposed modulation technique with two different CV limits (V_{Cmax} and V_{Cmin}) under balanced loading conditions. Unlike the two-level modulation (Fig. 2.6(a)), the proposed modulation technique does not suffer from the low-frequency harmonics as it employs the proposed feedforward compensation. Moreover, as the proposed modulation technique is a combination of the two- and three-level modulation, it shows THD and WTHD between them (Fig. 2.6). When defining a wide tolerant band, the technique operates with the two-level modulation all the time because the CVs fit within the band, resulting in lower THD values. If $V_{Cmax}=V_{Cmin}=V_{dc}/2$, i.e. the tolerance band is zero, the proposed modulation technique operates in the three-level mode all the time, as in [53]. Moreover, the THD obtained with the proposed modulation technique is mainly influenced by the high-frequency harmonic content of the output voltages. But such high-frequency harmonic components can be easily filtered by using a low-pass filter.

Fig. 2.17. Harmonic spectra of v_{ab} at $m=0.7$ with proposed modulation technique with CV range: (a) $[0.5V_{dc} \pm 5\%]$ and (b) $[0.5V_{dc} \pm 10\%]$.

Fig. 2.18 shows the variation of WTHD values with different modulation indices operating with a balanced linear load. For low modulation indices the CV ripples are small and the two-level modulation is applied all the time. This is why the curves overlap each other. On the other hand, when the modulation index is larger, a small tolerance band produces higher WTHD values because of the larger intervals operating in three levels. In any case, the increase of WTHD is relatively small because the harmonics that cause additional distortion are at relatively high frequencies (around the switching frequency and beyond).

Fig. 2.18. WTHD of the line-to-line voltage waveform at different modulation indices for a balanced load with proposed modulation technique.

2.5 Power Loss Analysis

When a phase switches in three-levels, the switching losses increase because there are more transitions involved in a switching period. The proposed modulation technique reduces the intervals where one phase switches in three levels as compared to [43, 52, 53]. It is hence a trade-off solution between the switching power losses and the CV ripple magnitude. A power loss analysis is performed considering the insulated-gate bipolar transistor (IGBT) DIM1200NSM17-E000, having a maximum collector-emitter voltage of 1700V and a continuous collector current of 1200A. The manufacturer's datasheet provides a curve to calculate the energy dissipated in every turn-on (E_{on}) and turn-off (E_{off}) of the semiconductor as a function of the current and for a given collector-emitter voltage (V_{CE}). The least square method (implemented in a toolbox supplied by MATLAB) is employed to find equations that fit these curves. The switching pulses generated by comparing the carrier and reference duty cycles helps in identifying the switching instants and conduction times of IGBTs and diodes. Using this data and the loss equations, the switching and conduction losses are calculated under different modulation techniques [64]. The simulation parameters for this analysis are provided in Table 2.2. The limits of the CVs are defined as $[0.5V_{dc} \pm 6.67\%]$, i.e., [700V, 800V].

Table 2.2: Simulation Parameters for Power Loss Analysis

Parameter	Value
DC-link voltage, V_{dc}	1500 V
Rated power	1.5 MW
Carrier frequency, f_s	2.5 kHz
AC-side frequency, f	50 Hz

Fig. 2.19 shows the power losses of the proposed modulation technique and the two-level modulation under different modulation indices and load phase angles. In Fig. 2.19(a) the switching losses of the two techniques are equal when the proposed modulation technique operates with the two-level modulation predominantly. When the proposed modulation applies the three-level modulation during some intervals, the obtained switching losses, and hence total losses, are higher with the proposed modulation technique. Fig. 2.19(b) shows that the conduction losses are similar for both cases. The small differences between the conduction losses are due to the type of device that is conducting (IGBT or diode).

Fig. 2.19. Power losses comparison between the proposed modulation technique and two-level modulation. (a) Switching, (b) conduction, and (c) total power losses.

In Fig. 2.20, the proposed modulation technique is compared with the three-level modulation [53]. Figs. 2.20(a) and (c) show that the switching and the total power losses, respectively, produced with the proposed modulation technique are less than the three-level modulation. This is due to the fact that the proposed modulation technique does not operate solely in the three-level mode, and only for some intervals if required. From Figs. 2.19 and 2.20, it is demonstrated that the switching and total losses with the proposed modulation technique are, in general terms, higher and lower than those produced with the two-level and the three-level modulations, respectively.

Fig. 2.20. Power losses comparison between the proposed modulation technique and three-level modulation [53]. (a) Switching, (b) conduction, and (c) total power losses.

2.6 Relation between Switching Losses and Voltage Band

From the above analysis, it is clear that for narrower CV limits, the performance of the proposed modulation moves close to the three-level modulation. The equivalent switching frequency increases in such a case and the switching losses obtained are close to the three-level modulation. When the CV limits are wider, the performance is closer to the two-level modulation. If the band is increased sufficiently, the proposed modulation technique exactly behaves like the two-level modulation. The proposed technique aims to find a trade-off between the voltage ripple magnitude and the switching loss. When trying to lower switching losses, some control on the CV ripples is lost and vice versa. It is difficult to obtain a direct relationship between the switching action number and the voltage band as it is dependent on operating factors like modulation index, phase angle and type of load, as can be seen from Fig. 2.21. The simulation parameters are same as Table 2.2 and the modulation index is taken as 1. Fig. 2.21(a) shows the switching losses when the proposed feedforward compensated modulation technique is used to feed a balanced linear load at different phase angles and voltage bands (ΔV) at $m=1$. When $\Delta V=0$, the proposed modulation technique operates like a three-level modulation resulting in maximum switching losses. As the voltage band increases, the switching losses start decreasing until the

point when the proposed modulation technique starts operating as a two-level modulation. This happens when the voltage band is equal to the CV ripple observed with the two-level modulation and no phase is required to switch in three levels anymore. After reaching this point, the switching losses are almost constant for that particular phase angle and modulation index. Fig. 2.21(b) shows the switching losses when a NPC converter feeds a nonlinear load using proposed modulation scheme under different phase angles and voltage bands at $m=1$. The switching loss pattern obtained is different from Fig. 2.21(a). With nonlinear load, switching a phase in three levels becomes more prominent to limit the CVs within the predefined band. From these figures, it is clear that it is difficult to obtain a direct relationship between switching action number and range and thus, it has not been studied further in this Chapter.

Fig. 2.21. Switching losses at different phase angles and voltage bands (ΔV) at $m=1$ feeding: (a) A balanced linear load and (b) a nonlinear load.

2.7 Conclusions

The modulation strategy proposed in this chapter uses a voltage band to offer a compromise solution between the two- and three-level modulation strategies at the expense of allowing the CVs to oscillate freely within this voltage band. As the proposed modulation strategy alternates between the two- and three-level modulations, an innovative feedforward compensation strategy, that is applicable to both two-level and three-level operating modes, is developed to eliminate the adverse effect of CV ripples on the ac-side voltages. If the CVs go beyond the predefined voltage limits, one phase of the converter switches in three levels to lead the CVs within the tolerance band again. With the proposed modulation technique, the power losses are the same as those produced with the two-level modulation when the CVs are within the limits, and a bit higher if the CVs tend to go beyond the limits. In any case the losses

are always lower than those produced by modulation techniques where one phase is switching in three levels all the time. Hence, the proposed modulation technique represents a trade-off solution between the voltage ripple magnitude and the switching power losses. Experimental results operating with balanced, unbalanced and nonlinear loads have been obtained to verify the capability of the modulation technique in regulating the CVs within the specified limits. The modulation technique has also been tested under strong initial CV imbalances. Limiting the CV ripples helps in the design of the NPC converter, since the maximum voltage that the dc-link capacitors and the power semiconductors have to withstand is predefined.

Though the prospered modulation strategy in this chapter achieves the main objectives of confining the CV ripples and reducing the switching losses, its performance deteriorate in presence of nonlinear loads that have the tendency to diverge the CVs. This deteriorated performance is a direct consequence of the diverging CVs frequently bouncing out of the voltage band, which triggers the modulation to operate in the higher loss three-level mode to force the CVs back in the band. This drawback is addressed in next Chapter wherein a current band is introduced, in addition to the existing voltage band, to balance the average CVs and effectively counter the CVs diverging drive.

Chapter 3

Band-Limited Three-Level Modulation for Three-phase NPC Converters

In this chapter, a band-limited three-level modulation technique is proposed for a three-phase NPC converter with the aim to balance the average CVs under all operating conditions. In addition to a predefined voltage band, a variable current band is employed in the proposed band-limited three-level modulation to ensure that the CVs do not bounce along the voltage band and average CVs are always balanced. Experimental results are obtained under different loading conditions for validating the performance of the proposed modulation scheme. A performance comparison is also presented between the feedforward compensated modulation and the proposed band-limited three-level modulation in this chapter.

3.1 Introduction

In order to attain a trade-off between the switching losses and the CV ripple magnitude, Chapter 2 presented a feedforward compensated modulation technique, wherein the CV ripples are regulated within a predefined voltage band by intermittently switching between the two- and three-level modulation. A major drawback of this technique is that the CVs can ‘bounce’ along the voltage band boundaries under certain nonlinear load conditions, leading to steady-state imbalance in average CVs

and more switching losses. This phenomenon arises due to the steady state differences in the average CVs as the feedforward compensated modulation technique only aims to produce the required instantaneous NP current (2.9). Thus, it is important to take the average CV difference into account in order to develop an effective modulation technique for the NPC converters.

The proposed BL-3L modulation aims to balance the average CVs irrespective of the loading conditions without any substantial increase in the switching losses, thereby concentrating mainly on enhancing the steady state performance of the system. This scheme employs two operational bands as mentioned below:

- Fixed voltage band- Applied to the CVs.

This band limits the maximum voltage across the dc-link capacitors. If any of the CVs go beyond the predefined voltage limit, one of the phases is chosen to switch in three voltage levels using the three-level modulation [53]. Within the voltage band, the NP voltage ripples are allowed to remain.

- Variable current band- Applied to the phase currents.

This band ensures average CV balance by switching a phase in three voltage levels intermittently. Within the voltage band, the number of times that a phase is switched in three levels is limited by the variable current band, i.e., a phase is only switched in three-levels in sampling periods where the absolute value of the corresponding phase current is low, i.e., when the phase current resides within the current band. The size of the current band is varied based on the tendency of the operational condition to unbalance the NP, which ensures that the number of sampling periods where the switching in three levels is minimized.

As switching a phase in three levels is limited, the obtained switching losses are lower than the conventional three-level modulation [53]. Therefore, the proposed BL-3L modulation scheme facilitates a trade-off between the CV ripple magnitude and the switching losses.

However, as the instantaneous CVs are allowed to vary within the voltage band, low-frequency distortion is produced in the ac-side voltages. For eliminating this low-frequency distortion, a feedforward compensation is employed in the proposed BL-3L

modulation scheme, same as the one introduced in Chapter 2. The main benefits of the proposed modulation scheme are as follows:

- The average CVs are balanced irrespective of the loading conditions.
- The NPC converter design process is made easier as the predefined voltage band limits the maximum voltage across the switches and the dc-link capacitors.
- A variable current band is defined to limit switching in three voltage levels, thereby, reducing the incurred switching losses compared to the conventional three-level modulation.

The rest of this chapter is organized as follows. Section 3.2 explains the steps involved in the proposed BL-3L modulation technique. Experimental results are presented in Section 3.3 to validate the performance of the proposed BL-3L modulation technique. A power loss analysis comparing two-level, three-level and the proposed BL-3L modulation technique is presented under Section 3.4. The performance of the feedforward compensated modulation (presented in Chapter 2) is compared with the proposed BL-3L modulation technique under Section 3.5. Section 3.6 summarizes the main conclusions of this chapter.

3.2 Proposed BL-3L Modulation Technique

The proposed BL-3L technique aims to balance the average, rather than instantaneous, CVs under all loading conditions. A voltage band is defined for limiting the maximum voltage across the dc-link capacitors. If any of the CVs goes beyond the defined voltage limit, one of the phases is chosen to switch in three voltage levels using the three-level modulation [53]. Within the voltage band, the NP voltage ripples are allowed to remain while the average CVs are balanced. In addition to the voltage band, a variable current band is also defined, which restricts phases switching in three levels only to those instants where the absolute value of their corresponding phase current resides within the current band. Moreover, feedforward compensated duty cycles are incorporated to eliminate the effect of CV imbalances on the ac-side voltages. The step-by-step procedure for the proposed technique is shown in Figs. 3.1-3.3 and is explained below:

Fig. 3.1. Calculation of NP current and its reference.

Step-I. Calculation of the reference NP current

As the proposed technique aims to balance the average voltage of the two capacitors, the reference NP current is calculated as (Fig. 3.1):

$$i_{NPref_{BL}} = C \frac{\overline{v_{C1} - v_{C2}}}{T_s}, \quad (3.1)$$

$\overline{v_{C1} - v_{C2}}$ represents the average of the difference between the CVs and is obtained by using a low pass filter with a cut-off frequency of $(0.1f)$ Hz, where f is the ac-side frequency.

Step-II. Calculation of the NP current

The NP current is calculated using feedforward compensated duty cycles and ac-side currents, as presented under *Step-II* in Section 2.3.

The obtained feedforward-adjusted duty cycles after v_{off} addition has the tendency to balance the average CVs, and is the only balancing mechanism that is required under balanced linear loads. However, under unbalanced linear loads and nonlinear loads, v_{offc} is insufficient to regulate the CVs, as will be shown in Section 3.3. An additional ‘push’ is still required to achieve voltage balance under these operational conditions, which is obtained by switching one of the three phases in three levels. Unlike the three-level modulation, in the proposed modulation technique if the CVs are within the predefined voltage band, switching a phase in three levels is prohibited unless its current is within the calculated variable current band, thereby, incurring lower switching losses over the former.

Step-III. Calculation of the variable current band

Fig. 3.2 shows the calculation of the variable current band using two controller feedback loops, which is explained next.

Fig. 3.2. Calculation of variable current band.

- In the first controller feedback loop, the difference between the two CVs (v_{C1} and v_{C2}) is fed to a low pass filter (with cut-off frequency of $0.1f$ Hz) for obtaining the average voltage difference. If the calculated difference is large, the band limit will increase consequently, increasing the probability of switching a phase in three-levels and thus, helping to balance the average CVs. It is noted that the necessary use of the absolute value of the average CVs (as the current band cannot be negative) precludes use of an integral component to eliminate steady state error.

- A second controller feedback loop is required to remove the steady state error by eliminating the dc component of the NP current, which causes divergence of the average CVs.

This is achieved by using the second control loop to force the average of the NP current (i_{NP}) calculated in (2.37) to be equal to the average NP current, which no longer flows to the NP due to switching periods in which the three-level modulation is applied via the variable current band ($\overline{i_{NP_x}}$). Suppose phase 'x' is chosen to switch in three levels as it has the tendency to compensate the NP current in the right direction and its current is within the current band. The contribution of phase x to NP current (i_{NP_x}) that no longer flows to the NP is calculated using (2.27)-(2.29), as follows:

$$i_{NPx} = d'_{NPx} i_x. \quad (3.2)$$

The phase switching in three levels is decided using reference NP current ($i_{NPref_{BL}}$) and NP current (i_{NP}) (as will be discussed in *Step IV*). If the average of i_{NP} is equal to the average of i_{NP_x} (the current that is no longer injected into the NP), then there is no average current that unbalances the NP. The $\overline{i_{NP}}$ and $\overline{i_{NP_x}}$ are obtained by low pass filtering (with cut-off frequency of $0.1f$ Hz) (2.37) and (3.2), respectively.

Calculating the variable current band using the abovementioned feedback loops restricts the number of switching periods where switching in three levels occurs. Consequently, this reduces the switching losses while still provides the additional push required to balance the average CVs.

Step-IV. Calculation of feedforward compensated duty cycles

Depending on the values of v_{C1} , i_{NP} , $i_{NPref_{BL}}$, $i_{NPref_{3L}}$ and the voltage/current band limits, it is decided whether all the phases will switch in two levels, or one among them will be chosen to switch in three levels, as shown in Fig. 3.3 and explained below:

Case-I. ($v_{C1} > V_{Cmax}$) or ($v_{C1} < V_{Cmin}$)

Here, V_{Cmax} and V_{Cmin} are the CV limits defined to restrict the voltage ripples on the dc-link capacitors. When the CVs go beyond the pre-

Fig. 3.3. Flowchart diagram of the proposed BL-3L modulation technique.

defined limits, the three-level modulation [53] is applied and a phase is chosen to switch in three levels depending on the values of $i_{NPref3L}$ and i_{NP} . These predefined CV limits not only help in limiting the voltage stress on the capacitors but also enhance the transient balancing response of the system. Unlike [53], the normalized voltage reference is calculated using (2.13) and the duty cycles are feedforward compensated in the proposed modulation technique. The feedforward compensation helps in avoiding low frequency distortion in the ac voltages due to CV imbalances. For the phases switching in two levels, the feedfor-

ward duty cycles are calculated using (2.27)-(2.29). The feedforward duty cycle of the phase switching in three voltage levels is computed using (2.32), (2.33) and (2.36).

Under this case, as the phase switching in three levels is chosen using the three-level modulation, the value of i_{NP_x} is 0.

Case-II. ($V_{Cmin} \leq v_{C1} \leq V_{Cmax}$) and $(i_{NP} \times i_{NPref_{BL}}) > 0$ and $|i_{NP}| \leq |i_{NPref_{BL}}|$

As the CVs are within limits, and the NP current is in the same direction as the reference NP current, no additional action is required. All the phases are chosen to switch in two levels and their feedforward compensated duty cycles are calculated using (2.27)-(2.29). In this case, as all the phases are switching in two levels, the value of i_{NP_x} is 0.

Case-III. ($V_{Cmin} \leq v_{C1} \leq V_{Cmax}$) and $(i_{NP} \times i_{NPref_{BL}}) < 0$

In this case, the direction of NP current is opposite to the direction of the required NP current. As a result, one of the phases is required to switch in three levels. The prerequisite for a phase switching in three levels is that its phase current is within the calculated variable current band limit. The absolute values of the phase currents are compared to the current band one-by-one. The phases lying within the current band are then tested if they have the capability to compensate the NP current in the required direction. Suppose phase 'x' has a phase current within the band, then $d'_{NP_x} = 0$ in (2.37) and the new i'_{NP} is calculated. If $(i'_{NP} \times i_{NPref_{BL}}) > 0$ or $(i'_{NP} \times i_{NPref_{BL}}) < 0$ such that $|i'_{NP}| < |i_{NP}|$, then phase 'x' is allowed to switch in three levels. If there are more than one phase satisfying these conditions, the phase with lower value of phase current is chosen to switch in three levels. On the other hand, if no phase satisfies these conditions, all phases switch in two levels. Eqs. (2.27)-(2.29) are utilized to calculate the feedforward compensated duty cycles for the phases switching in two levels. Suppose phase 'x' is chosen to switch in three levels, while phases 'y' and 'z' switch in two levels, the feedforward duty cycle for phase 'x' connecting to NP is calculated as:

$$d'_{NP_x} = \frac{i_{NPref_{BL}} - d'_{NP_y} i_y - d'_{NP_z} i_z}{i_x}. \quad (3.3)$$

Using the value of d'_{NP_x} calculated above, the feedforward compensated duty cycle for connecting phase 'x' to the positive and negative dc-rails are calculated from (2.36) and (2.33), respectively. The i_{NP_x} contribution of phase 'x' switching in three levels for determining the band is calculated using (2.27)-(2.29) and (3.2).

Case-IV. ($V_{Cmin} \leq v_{C1} \leq V_{Cmax}$) and $(i_{NP} \times i_{NPref_{BL}}) > 0$ and $|i_{NP}| > |i_{NPref_{BL}}|$

As the magnitude of the NP current is greater than the required NP current, one phase is required to switch in three levels to reduce i_{NP} magnitude lower than $i_{NPref_{BL}}$. Similar to Case-III, firstly, the phases below the variable current band are selected. Then, the phases are tested if they can compensate the NP current magnitude in the required manner. Let's suppose, phase 'x' has a phase current within the band, imposing $d'_{NP_x}=0$ in (2.37), the new i'_{NP} is calculated. If $(|i'_{NP}| < |i_{NPref_{BL}}|)$ or $(|i'_{NP}| > |i_{NPref_{BL}}|)$ such that $|i'_{NP}| < |i_{NP}|$, then phase 'x' is suitable for switching in three levels. If there are two phases which are suitable, the phase with lower phase current is chosen to switch in three levels. On the other hand, if no phase satisfy these conditions, all phases will continue switching in two levels. The feedforward compensated duty cycles for phases switching in two levels are calculated using (2.27)-(2.29), while for the phase switching in three levels are calculated using (3.3), (2.36) and (2.33). The i_{NP_x} contribution of phase 'x' switching in three levels required for the band calculation is evaluated using (2.27)-(2.29) and (3.2).

The obtained duty cycles are then compared to a triangular carrier signal for generating the switching pulses for the NPC converter, using CB1 PWM from [63] via the state-machine model (Appendix B).

3.3 Experimental Results

To validate the performance of the proposed BL-3L modulation technique, different experimental tests are performed on a hardware prototype with the specifications provided under Section 2.2.3. In addition, the voltage band limit, $[V_{Cmax}, V_{Cmin}]$, is predefined as [165V, 135V] for these tests.

3.3.1 Balanced Linear Loading Condition

A balanced star-connected RL load is connected to the three-phase NPC converter with S open in Fig. 2.1, same as Section 2.2.3.1. Fig. 3.4 shows the waveforms of v_{ab} , v_{C1} , v_{C2} , i_a , i_b , i_c and the variable current band at different modulation indices operating with the proposed BL-3L modulation.

Fig. 3.4. Balanced linear load operating with BL-3L modulation technique at m : (a) 1, (b) 0.7, and (c) 0.4.

From these figures, it is clear that the average of the CVs is equal irrespective of the modulation index and also, the voltages lie within the predefined voltage band, i.e. [165V, 135V], unlike the case of two-level modulation (Fig. 2.3). As the average difference between the two CVs is very small, the obtained variable current band is also very small, thereby, limiting the switching in three-level modulation to very few instants.

3.3.2 Linear Unbalanced Loading Condition

Under linear imbalances, negative sequence currents are present which lead to additional NP voltage ripples in comparison to balanced linear loads [36]. Fig. 3.5 shows the same waveforms when the star-connected RL load has a load imbalance, same as Section 2.2.3.2 operating under the proposed BL-3L modulation.

Fig. 3.5. Linear unbalanced load operating with BL-3L modulation technique at m : (a) 1, (b) 0.7, and (c) 0.4.

From the figures, it is clear that the average CVs are balanced within a fundamental period. Also, the obtained NP voltage ripples are limited within the voltage band, i.e. [165V, 135V], under all cases.

3.3.3 Nonlinear Loading Condition

Fig. 3.6 shows the same waveforms under nonlinear loading conditions as in Section 2.2.3.3 operating with the proposed BL-3L modulation technique at different modulation indices. It is clear that the average CVs are balanced even in the presence of nonlinear load and lie within the predefined voltage band $[165\text{V}, 135\text{V}]$ under all modulation indices.

Fig. 3.6. Nonlinear load operating under the proposed BL-3L modulation technique at m : (a) 1, (b) 0.7, and (c) 0.4.

3.3.4 Initial CV Imbalance

Fig. 3.7 shows the performance under proposed BL-3L modulation when an initial imbalance is forced, such that $V_{C1} = 200\text{ V}$ and $V_{C2} = 100\text{ V}$, while feeding the same nonlinear load as in Subsection 3.3.3. As the initial imbalance is greater than the

predefined voltage band limit, i.e. $[165\text{V}, 135\text{V}]$, the proposed BL-3L modulation technique operates as three-level modulation [53] all the time until the CVs reach the voltage band. As the bandwidth of the loop responsible for regulating the current band is low (due to presence of a low pass filter), the transient response is relatively slow. However, in steady state (which is the targeted case for which the variable current band has been designed), the average CVs are balanced and the obtained CVs lie within the predefined voltage band.

Fig. 3.7. Initial CV imbalance using BL-3L modulation technique at m : (a) 1 and (b) 0.7.

3.3.5 Distortion Analysis

Fig. 3.8 shows the harmonic spectra of v_{ab} obtained under the proposed BL-3L modulation technique operating with balanced linear load.

Fig. 3.8. Harmonic spectra of v_{ab} at $m= 0.7$ with proposed BL-3L modulation technique with voltage band $[165\text{V}, 135\text{V}]$.

In comparison to Fig. 2.6, the THD and WTHD of the proposed BL-3L modulation technique lies in between the two- and three-level modulation techniques.

Moreover, no low-frequency components are observed even in the presence of CV imbalance with the proposed technique. This is due to the incorporation of feedforward compensated duty cycles which eliminate the effect of CV imbalances on the output voltages.

3.4 Power Loss Analysis

The switching losses increase whenever a phase switches among three voltage levels within a switching period due to increased number of transitions. The main aim of the proposed BL-3L modulation technique is to balance the average CVs under all operating conditions by restricting the phases to switch in three levels to fewer instants. For comparing the losses of the proposed BL-3L modulation technique with two- and three-level [53] modulation techniques for practical systems, different simulation tests are performed by employing the characteristic curves from Section 2.5. The simulation parameters are same as Table 2.2.

Fig. 3.9 shows the loss comparison between the two-level modulation and the proposed BL-3L modulation technique at different modulation indices and load phase angles for a linear load.

Fig. 3.9. Losses comparison between two-level modulation and the proposed BL-3L modulation with voltage band [765V, 735V]. (a) Switching, (b) conduction, and (c) total power losses.

As with the proposed BL-3L modulation technique one of the phases switches in three voltage levels to limit the CVs within predefined limits and to balance the average CVs, the obtained switching losses are higher than the two-level modulation. The conduction losses of both of techniques are almost the same as the only difference lies in the conducting device (IGBT/diode) at various instants. The total losses operating under proposed BL-3L modulation technique are higher than those obtained under the two-level modulation.

In Fig. 3.10, the switching and total losses obtained under the proposed BL-3L modulation are lower as compared to the three-level modulation under all operating conditions. This is due to the fact that switching a phase in three levels is restricted to fewer instants under the proposed BL-3L modulation technique. From Figs. 3.9 and 3.10, it is clear that the total losses obtained under the proposed BL-3L modulation lies between the two- and three-level modulation, with significant dependency on power factor.

Fig. 3.10. Losses comparison between three-level modulation [53] and the proposed BL-3L modulation with voltage band [765V, 735V]. (a) Switching, (b) conduction, and (c) total power losses.

Fig. 3.11 presents the switching losses obtained under the proposed BL-3L modulation under different modulation indices and phase angles with different loading conditions and voltage bands. From Fig. 3.11, it is clear that the obtained switching losses are lower with a wider voltage band irrespective of the loading conditions. With a narrow voltage band, switching a phase in three levels happens more frequent to

maintain the CVs between the narrow band. From these results, it can be concluded that for narrow voltage bands, the performance of the proposed modulation moves close to the three-level modulation. The equivalent switching frequency increases in such a case and the switching losses obtained are close to the three-level modulation. When the CV limits are wider, the performance is closer to the two-level modulation. If the band is increased sufficiently, the proposed modulation technique exactly behaves like the two-level modulation. Therefore, the proposed BL-3L modulation technique basically presents a trade-off between the voltage ripple magnitude and the switching losses. For achieving lower switching losses, some increased CV ripple is required and vice versa.

Fig. 3.11. Switching losses under band-limited three-level modulation operating with: (a) Linear load and (b) nonlinear load.

Considering the switching losses obtained with voltage band [840V, 660V] in Figs. 3.11(a) and (b), as the voltage band is large, the BL-3L modulation technique operates within the band limits. The performance with the balanced linear load for this band is very close to the two-level modulation (Fig. 3.9(a)), while the corresponding losses are higher with nonlinear load. This difference arises due to the variable current band. For balanced linear load, the obtained variable current band is very small and switching a phase in three levels is rare. However, with the nonlinear load, the CVs tend to diverge leading to a dc component in the NP current, thereby, increasing the variable current band. As a result, switching a phase is more prominent under nonlinear loads, thus leading to more switching losses.

3.5 Performance Comparison between Feedforward Compensated Modulation and the Proposed BL-3L Modulation

Fig. 3.12(a) shows the waveforms of v_{ab} , v_{C1} , v_{C2} , i_a , i_b , i_c and the phase switching in three-levels ($a/b/c/\text{None}$) at $m = 1$ under feedforward compensated modulation technique while feeding a nonlinear load. The simulation parameters are provided in Table 2.2 and the voltage band limit is set at $[840\text{V}, 660\text{V}]$.

Fig. 3.12. Performance with nonlinear load under: (a) Feedforward compensated modulation with confined CV ripples [65] and (b) proposed band-limited three-level modulation.

From this figure, it is clear that the feedforward compensated modulation achieves its objective of confining the CV ripples within the predefined voltage band. However, the CVs tend to bounce along the voltage band boundaries. As the CV reaches the band limit, one of the phases switches in three levels to keep the voltage within the band. However, the nonlinearity in the load tries to diverge the CVs more and more [36]. Due to the opposing nature of these two, the CVs keep on bouncing along the band. As a result, the switching transitions increase leading to an increase in switching losses as well. Thus, it is important to regulate the average CVs. The proposed BL-3L modulation aims to balance the average CVs irrespective of the loading conditions. Fig. 3.12(b) shows the same waveforms while operating under

same loading conditions. From this figure, the importance of variable current band in balancing the average CVs is clearly visible. The CVs do not bounce along the voltage band. The main objective of adding the voltage band to the BL-3L modulation is to limit the maximum CV ripples across the capacitors. Consequently providing an advantage of designing the converter beforehand. Moreover, if we look closely at Fig. 3.12(b), the switching transitions are fewer in comparison to Fig. 3.12(a). As a result, the switching losses obtained with feedforward compensated modulation are 2.13 times the switching losses obtained with BL-3L modulation under this operating condition.

Fig. 3.13 shows the loss comparison between the feedforward compensated modulation and the proposed BL-3L modulation at different modulation indices and positive sequence phase angles while feeding a nonlinear load.

Fig. 3.13. Losses comparison between feedforward compensated modulation and BL-3L modulation. (a) Switching, (b) conduction, and (c) total power losses.

From Fig. 3.13(a), the switching losses for the feedforward compensated modulation are higher than the proposed BL-3L modulation for positive sequence phase angles between -90° to 90° for most of the modulation indices. This is due to the increase in switching transitions as the CVs bounce along the voltage band. As a result, the obtained total losses under feedforward compensated modulation are also higher than the proposed BL-3L modulation technique under certain operating conditions.

3.5.1 Comparison Among Different Modulation Techniques for the Three-Phase NPC Converter

Table 3.1 sums up the comparison among the two-level modulation, three-level modulation [53], feedforward compensated modulation [65] and the proposed BL-3L modulation technique on account of different parameters. From the comparison, it is clear that the proposed BL-3L modulation technique provides a trade-off between the voltage ripple magnitude and the switching losses.

Table 3.1: Comparison Among Different Modulation Techniques

	Two-Level Modulation	Three-Level Modulation [53]	Feedforward Compensated Modulation (Chapter 2)	Proposed BL-3L Modulation
Maximum voltage applied to the dc-link capacitors and semiconductors	It depends on the operating point (CV ripple amplitude)	The lowest ($V_{dc}/2$)	Predefined by maximum limit (V_{Cmax})	Predefined by maximum limit (V_{Cmax})
Average CVs	Dependant on the loading conditions	Always balanced ($V_{dc}/2$)	Dependant on the loading conditions	Always balanced ($V_{dc}/2$)
Switching losses	The lowest	The highest	Much lower than three-level modulation	Much lower than three-level modulation
Operation under nonlinear loads with even harmonics	May become unstable	Always stable	Stable (CVs can ‘bounce’ along the voltage band increasing switching losses)	Always stable
Low frequency distortion in the output voltages	Exist due to the low-frequency CV ripples	No (due to absence of low-frequency CV ripples)	No (feedforward compensated)	No (feedforward compensated)
High frequency distortion in the output voltages	The lowest	The highest	Low	Low

3.6 Conclusions

In this chapter, a band-limited three-level (BL-3L) modulation technique has been presented, which balances the average CVs irrespective of loading conditions without increasing the switching losses substantially. The main aim of the proposed BL-3L modulation is to enhance the steady state performance of the system. A voltage band has been employed in this chapter to limit the maximum voltage across the dc-link capacitors and semiconductors, which gives a freedom to design the NPC converter beforehand. Within the voltage band, a variable current band is defined which restricts switching a phase in three levels to fewer instants, thereby, reducing the switching losses as compared to the three-level modulation. Moreover, feedforward compensated duty cycles are utilized to mitigate the low-frequency ripples in the output voltages that occur due to CV imbalance. The performance of the proposed BL-3L modulation technique has been tested under balanced linear, linear imbalance and nonlinear loads. Under all the loading conditions, the average CVs are balanced and the voltages adhere to the predefined voltage limits. Moreover, the obtained losses under the proposed BL-3L modulation technique lies in between the losses obtained under the two-level and three-level modulation. This chapter also showed that unlike the feedforward compensated modulation, the CVs do not bounce along the voltage under nonlinear loading conditions with the proposed BL-3L modulation technique.

Chapter 4

Dual-Mode Modulation Technique for Dual-Input Three-phase NPC Converters

This chapter presents a dual-mode modulation technique which aims to control the average current flow into the NP of the NPC converter without the need for any additional hardware. This technique is developed analytically by only employing the converter's ac-side voltages and currents, thus, providing a generalized solution to balance average CVs in NPC converters. The maximum average NP current injection capacity of the NPC converter under dual-mode modulation technique is also determined in this chapter. In addition, the performance of the proposed modulation technique is validated experimentally for various loading conditions.

4.1 Introduction

As pointed out under Section 1.2.2, it is important to compensate the nonzero average NP current arising from unbalanced dc loads to ensure that the CVs do not diverge. This chapter addresses this challenge by developing a PWM based solution to utilize the inherent capability of the NPC converter to generate the required average NP current over a fundamental period. Most of the previous attempts to control the NP current were focused on controlling the instantaneous NP current [15, 53, 65].

Fig. 4.1(a) shows the variation of maximum value of instantaneous NP current

Fig. 4.1. (a) Variation of maximum NP current over a fundamental time period, and (b) partial saturation under instantaneous NP current approach.

(i_{NPmax}) that can be generated over a fundamental time period with the assumption of a sinusoidal ac-side voltage and current. Due to the time-varying nature of i_{NPmax} , the required NP current ($\bar{i}_{NPref}$) can be linearly controlled only when its value is less than i_{NPmaxa} . When $\bar{i}_{NPref}$ lies between i_{NPmaxa} and i_{NPmaxb} , the controller is partially saturated as shown in Fig. 4.1(b). Consequently, the generated average NP current is lower than $\bar{i}_{NPref}$. The controller output becomes completely saturated when $\bar{i}_{NPref}$ exceeds i_{NPmaxb} at which point the NPC converter generates the maximum possible average NP current. In order to avoid partial saturation of the controller, this chapter proposes a dual-mode modulation technique to control the average NP current. The proposed modulation technique is generic and can be applied for balancing the CVs in all bipolar dc-bus applications employing NPC converters such as wind energy systems, grid-integrated solar photovoltaic systems, static reactive power compensators, electric vehicle charging systems, etc.

The proposed dual-mode modulation technique, as the name suggests, has two operating modes: normal operation mode (NOM) and compensating operation mode (COM). In NOM, all the phases switch in two consecutive voltage levels in each switching period, i.e., either between the positive or negative dc-rail and the NP. In COM, at least one of the phases switches between the positive and negative dc-rails in a switching period to inject the required average NP current. An analytical solution is developed to determine the duration of these two operation modes within each fundamental cycle based on the converter's operating condition. The main contributions of the proposed dual-mode modulation technique are:

- The proposed modulation strategy is based on controlling the average NP current rather than the instantaneous NP current.
- In the proposed technique, average NP current is correlated to a new control

variable (α) by employing a linearization block, which allows for having a linear control system design unlike the modulation strategies controlling the instantaneous NP current that have to deal with partial control output saturation.

- This linearization block analytically calculates the control output by using the ac-side voltages and currents, and the required average NP current over the fundamental period.
- The maximum average NP current injection capability of the NPC converter under dual-mode modulation technique is analytically calculated, which indicates the stable operating range of the converter.
- The proposed modulation technique is applicable to all bipolar dc-bus applications employing the NPC converter.
- A dq -based control scheme is presented using the proposed dual-mode modulation technique for a three-phase grid-connected NPC converter feeding bipolar dc-loads with the aim of balancing the dc-link CVs.

The organization of the chapter is as follows. Section 4.2 introduces the proposed analytical solution for injecting the required average NP current and explains the two operation modes. Section 4.3 proposes a control strategy employing the analytically developed linearization block for the case of a three-phase grid-connected NPC converter feeding bipolar dc-loads. Section 4.4 provides experimental results to validate the performance of the proposed modulation technique, while Section 4.5 concludes the outcomes of this work.

4.2 Proposed Average NP Current Injection Strategy

This section presents the mechanism to generate the required average NP current arising due to unbalance in dc-loads.

4.2.1 Average NP Current Generation Mechanism

In order to generate a nonzero average NP current, it is important to understand the factors affecting the NP current. The NP current (i_{NP}) is calculated using (2.8). The obtained i_{NP} is averaged over the fundamental grid voltage period in order to obtain the average NP current ($\bar{i}_{NP}$). It is clear that the duty cycle connecting the respective phase to the NP, in turn the modulation technique employed, determines $\bar{i}_{NP}$.

Consider the modulation technique presented in [48], wherein each phase switches only in two consecutive voltage levels over a switching period similar to two-level modulation. The normalized ac-side voltage references under [48] do not employ any zero-sequence voltage. Therefore, the NP duty cycle for phase j (d_{NPj}) is given as [48]:

$$d_{NPj} = 1 - |v_j^*|, \quad (4.1)$$

where, v_j^* represents the normalized ac-side voltage reference of phase ' j ' in the abc frame without the zero-sequence addition. The waveforms of normalized voltage and current of phase ' a ', i_{NP} and $\bar{i}_{NP}$ are shown in Fig. 4.2(a). The results in this figure are obtained using (2.8) and (4.1), with the assumption of a sinusoidal balanced ac-side voltage reference and current, i.e., $v_a^* = m \cos(\theta_g + \delta)$ and $i_a = I_m \cos(\theta_g - \phi)$.

As can be seen, in this modulation strategy, the contribution of phase ' a ' to $\bar{i}_{NP}$ is zero. The effect of the remaining phases can also be analyzed in a similar manner. As a result, the average NP current adds to zero over a fundamental period when all the phases switch in two consecutive voltage levels (shown in Fig. 4.2(a)). Therefore, in applications requiring an average NP current, this modulation technique is not effective.

In [53], the authors analyzed the three-level modulation technique for a single dc voltage source without utilizing the NP. Nevertheless, the study showed that switching one or more phases in three voltage levels is an effective way of controlling the NP current. In a simpler way, if phase ' j ' switches only between the positive and the negative dc-rails in a switching period, then $d_{NPj} = 0$. This feature provides a freedom to inject or withdraw current in/from the NP in order to generate the required average NP current $\bar{i}_{NP}$, as shown in Figs. 4.2(b) and (c). These figures demonstrate how the $\bar{i}_{NP}$ changes by modifying d_{NPj} . By switching a phase between

Fig. 4.2. Waveforms of normalized phase voltage and current of phase ‘a’ with producing: (a) Zero $\bar{i}_{NP}$, (b) positive $\bar{i}_{NP}$ and (c) negative $\bar{i}_{NP}$.

the positive and negative dc-rails for an α interval within a fundamental period, the symmetry of i_{NP} is disturbed resulting in a net nonzero $\bar{i}_{NP}$. d_{NP_j} is zero for the α interval while it is calculated using (4.1) for the rest of the interval. Here, α represents the duration of COM and the rest of the interval is NOM. The α interval for each phase is placed symmetrically on the positive or negative peak of the phase current, which determines the direction of $\bar{i}_{NP}$. Fig. 4.2(b) shows that the NP current contribution of phase a is zero within the α interval. As the α interval coincides with negative i_a , the resultant $\bar{i}_{NP}$ is positive. In Fig. 4.2(c), a negative $\bar{i}_{NP}$ is obtained by making $d_{NP_j} = 0$ when i_j is positive. Therefore, an average NP current over a fundamental cycle can be easily generated by switching the phases between the positive and negative dc-rails for an interval α . If $\alpha \leq 2\pi/3$, only one phase switches between the positive and negative dc-rails (Fig. 4.3(a)). However, if $2\pi/3 < \alpha \leq \pi$, two phases switch between the positive and negative dc-rails simultaneously (Fig. 4.3(b)). The maximum $|\bar{i}_{NP}|$ is obtained at $\alpha = \pi$.

Fig. 4.3. Compensating operation mode when: (a) $\alpha \leq 2\pi/3$ and (b) $2\pi/3 < \alpha \leq \pi$.

4.2.2 Proposed Linearization Block

In this chapter, a linearization block is proposed for calculating α in order to inject/withdraw the required amount of NP current to maintain the dc-link CVs balanced. The magnitude of $\bar{i}_{NPref}$ is equal to the total average current generated under COM. The main advantage of the proposed analytical solution is its capability to linearly control the NP current by using the ac-side voltage references and currents. Considering all three phases contribute equally to produce an average NP current, the contribution of one phase is equal to one-third of $\bar{i}_{NPref}$. Moreover, due to the sinusoidal symmetry of the ac-side currents and reference voltages, the calculated α will not vary by changing the sign of $\bar{i}_{NPref}$. Assuming symmetry among all three phases, the average NP current contribution of phase a is one-third of $\bar{i}_{NPref}$ as follows,

$$\frac{\bar{i}_{NPref}}{3} = \frac{1}{2\pi} \int_{\phi-\alpha/2}^{\phi+\alpha/2} (1 - |v_a^*|) i_a d\theta_g. \quad (4.2)$$

With the assumption of sinusoidal voltage and current,

$$\frac{\bar{i}_{NPref}}{3} = \frac{1}{2\pi} \int_{\phi-\alpha/2}^{\phi+\alpha/2} (1 - |m \cos(\theta_g + \delta)|) I_m \cos(\theta_g - \phi) d\theta_g. \quad (4.3)$$

If ϕ lies in the first quadrant, such that $0 \leq \phi \leq \pi/2$, then from Fig. 4.3:

$$\phi + \frac{\alpha}{2} \leq \frac{\pi}{2} - \delta \implies \alpha \leq \pi - 2\delta - 2\phi. \quad (4.4)$$

Equation (4.3) can be written as,

$$\frac{\bar{i}_{NPre f}}{3} = \frac{1}{2\pi} \int_{\phi-\alpha/2}^{\phi+\alpha/2} (1 - m \cos(\theta_g + \delta)) I_m \cos(\theta_g - \phi) d\theta_g. \quad (4.5)$$

Integrating (4.5) with respect to θ_g yields,

$$\frac{\bar{i}_{NPre f}}{3} = \frac{I_m}{4\pi} \left[-m \cos(\phi + \delta) \sin \alpha - \alpha m \cos(\phi + \delta) + 4 \sin\left(\frac{\alpha}{2}\right) \right]. \quad (4.6)$$

The MATLAB curve-fit tool is utilized to approximate the sine functions as quadratic functions for obtaining a direct solution. These approximations have less pronounced effects on the solution as their R^2 (measure of goodness-of-fit) value is very close to 1 and are valid for $\alpha = [0, \pi]$. Therefore, $\sin \alpha$ and $\sin(\alpha/2)$ are approximated as,

$$\begin{aligned} \sin \alpha &= -0.4162\alpha^2 + 1.308\alpha - 0.0475 \\ \sin\left(\frac{\alpha}{2}\right) &= -0.08449\alpha^2 + 0.5972\alpha - 0.02353. \end{aligned} \quad (4.7)$$

Accuracy of these approximated functions are validated by the root mean square error of less than 0.02 and 0.01 for $\sin \alpha$ and $\sin(\alpha/2)$, respectively. Substituting (4.7) in (4.6) and rearranging, a quadratic equation as a function of α is obtained as,

$$\begin{aligned} (0.4162m \cos(\phi + \delta) - 0.33796)\alpha^2 + (-2.308m \cos(\phi + \delta) + 2.3888)\alpha \\ + \left(0.0475m \cos(\phi + \delta) - 0.09412 - \frac{4\pi \bar{i}_{NPre f}}{3I_m} \right) = 0. \end{aligned} \quad (4.8)$$

Solving (4.8) for α :

$$\alpha = \frac{28850m \cos(\phi + \delta) - 29860 \pm 12500\sqrt{q}}{10405m \cos(\phi + \delta) - 8449}, \quad (4.9)$$

where,

$$\begin{aligned} q &= 5.2477m^2 \cos^2(\phi + \delta) - 10.805m \cos(\phi + \delta) + 6.9699m \frac{\bar{i}_{NPre f}}{I_m} \cos(\phi + \delta) \\ &\quad - 5.6597 \frac{\bar{i}_{NPre f}}{I_m} + 5.5791. \end{aligned} \quad (4.10)$$

If the condition in (4.4) is not met, then (4.3) can be written as:

$$\begin{aligned} \frac{\bar{i}_{NPre f}}{3} = & \frac{1}{2\pi} \left[\int_{\phi-\alpha/2}^{\pi/2-\delta} (1 - m \cos(\theta_g + \delta)) I_m \cos(\theta_g - \phi) d\theta_g \right. \\ & \left. + \int_{\pi/2-\delta}^{\phi+\alpha/2} (1 + m \cos(\theta_g + \delta)) I_m \cos(\theta_g - \phi) d\theta_g \right]. \end{aligned} \quad (4.11)$$

Integrating (4.11) with respect to θ_g yields,

$$\begin{aligned} \frac{\bar{i}_{NPre f}}{3} = & \frac{I_m}{4\pi} \left[-2m \sin(\phi + \delta) \sin^2 \left(\frac{\alpha}{2} \right) + (2\delta + 2\phi - \pi) m \cos(\phi + \delta) \right. \\ & \left. + 4 \sin \left(\frac{\alpha}{2} \right) \right]. \end{aligned} \quad (4.12)$$

Rearranging (4.12),

$$2m \sin(\phi + \delta) \sin^2 \left(\frac{\alpha}{2} \right) - 4 \sin \left(\frac{\alpha}{2} \right) - (2\delta + 2\phi - \pi) m \cos(\phi + \delta) + \frac{4\pi \bar{i}_{NPre f}}{3I_m} = 0. \quad (4.13)$$

Equation (4.13) is a quadratic equation of $\sin(\alpha/2)$, which can be solved to obtain α as,

$$\alpha = 2 \sin^{-1} \left(\frac{2 \pm \sqrt{p}}{2m \sin(\phi + \delta)} \right), \quad (4.14)$$

where,

$$p = 4 + m^2(2\delta + 2\phi - \pi) \sin(2\phi + 2\delta) - \frac{8m\pi \bar{i}_{NPre f}}{3I_m} \sin(\phi + \delta). \quad (4.15)$$

Similar steps are taken to calculate α under different power factor angles and the solutions are summarised in Fig. 4.4. The calculated α determines the duration of COM.

4.2.3 Calculation of Maximum Average NP Current Injection Capability

The maximum magnitude of NP average current injection is obtained at $\alpha = \pi$ radians. By setting $\alpha = \pi$ in (4.2) and integrating, the following relations are obtained:

 Fig. 4.4. Linearization block to calculate α for different power factor angles.

$$|\bar{i}_{NPmax}| = \begin{cases} \frac{3I_m}{2\pi} \left[2 - m \sin(\phi + \delta) + \left(\phi + \delta - \frac{\pi}{2} \right) m \cos(\phi + \delta) \right], & 0 \leq \phi \leq \pi, \\ \frac{3I_m}{2\pi} \left[2 + m \sin(\phi + \delta) - \left(\phi + \delta + \frac{\pi}{2} \right) m \cos(\phi + \delta) \right], & -\pi \leq \phi \leq 0, \end{cases} \quad (4.16)$$

where $|\bar{i}_{NPmax}|$ represents the maximum average NP current injection capability of the NPC converter under the proposed dual-mode modulation technique. Fig. 4.5 shows the variation of $|\bar{i}_{NPmax}|$ with respect to I_m under different modulation indices (m) and load phase angles (ϕ) with $\delta = 0^\circ$. As can be seen, the $|\bar{i}_{NPmax}|$ increases as the modulation index decreases. Moreover, the effect of ϕ on $|\bar{i}_{NPmax}|$ is more prominent at higher m .

Fig. 4.5. Variation of the maximum NP average current with respect to I_m under different modulation indices and load phase angles with $\delta = 0^\circ$.

4.3 Proposed Control Scheme

The proposed dual-mode modulation technique is applicable to all bipolar dc-bus applications employing NPC converters as it only requires the converter's ac-side voltages and currents and the average NP current reference for its implementation. For validating the analytical solution obtained to apply the dual-mode modulation technique, a three-phase grid-connected NPC converter feeding bipolar dc-loads, as shown in Fig. 4.6, is considered.

The overview of the proposed control strategy is shown in Fig. 4.7 and the functionality of different components is explained below.

(a)

(b)

Fig. 4.6. (a) Circuit diagram of a three-phase grid-connected NPC converter, and (b) picture of the hardware prototype.

(a)

(b)

Fig. 4.7. Control scheme: (a) Generation of normalized reference ac-side voltages and (b) computation of duty cycles.

1. DC-link voltage management

The sum of dc-link CVs is compared to the dc-link voltage reference (V_{dc}^*) and is fed to a PI controller in order to generate the d -component of the ac-side current reference i_d^* .

2. Current controller

A dq -based current controller is employed to generate the ac-side voltage references of the NPC converter in the dq frame (v_d^*, v_q^*).

3. Generation of converter voltage references

The ac-side voltage references in dq frame are transformed into normalized abc form (v_a^*, v_b^* and v_c^*).

4. Calculation of average NP current reference

In order to keep the dc-link CVs balanced, v_{C1} is compared to half of the dc-

link voltage reference (V_{dc}^*) and the difference is fed to a PI controller to obtain $\bar{i}_{NPref}$.

5. *Calculation of the duration of the compensating mode*

The obtained $\bar{i}_{NPref}$, m , δ , I_m and ϕ values are utilized to calculate α using the equations shown in Fig. 4.4. If the average NP current reference is greater than the maximum average NP current injection capability of the NPC converter, α saturates at π radians.

6. *Computation of duty cycles*

Depending on the operation mode, the duty cycle connecting the phases to the NP is computed. When applying COM, the phase switching between the positive and negative dc-rails has its NP connecting duty cycle zero, while the rest of the phases switch in two consecutive voltage levels and their NP duty cycles are calculated using (4.1). When applying NOM, all the phases switch in two consecutive voltage levels.

The duty cycles for connecting phase ‘ j ’ to the negative and positive dc-rails are calculated as [53]:

$$d_{l_j} = \frac{1 - d_{NP_j} - v_j^*}{2}, \text{ and } d_{h_j} = 1 - d_{NP_j} - d_{l_j}. \quad (4.17)$$

The calculated duty cycles are then compared with the carrier signal to generate the switching pulses of the NPC converter [63] via the state-machine model (Appendix B).

4.4 Experimental Results

For validating the performance of the proposed dual-mode modulation technique, different tests have been performed on a laboratory prototype (as described under Section 2.2.3) with the circuit diagram shown in Fig. 4.6. In addition to the dSPACE controller and the NPC converter, a grid emulator (GE&EL 15 kVA Cinergia) is employed. The parameters of the experimental setup are provided in Table 4.1.

Table 4.1: Experimental Parameters

Parameter	Value
DC-link voltage reference, V_{dc}^*	350 V
DC-link capacitors (each), $C1, C2$	2.2 mF
Carrier frequency, f_s	2 kHz
Grid phase voltage (rms)	110 V
Power factor	1
Grid frequency, f	50 Hz
Grid connection filter inductor, L	5 mH

4.4.1 Dynamic Performance of the Proposed Dual-Mode Modulation Technique

Fig. 4.8 shows the dynamic performance of the proposed dual-mode modulation technique when the bipolar dc-bus load varies. When $R_{d1} = R_{d2} = 50 \Omega$, the average NP current reference ($\bar{i}_{NPref}$) is zero. From the results, it is clear that the generated average NP current ($\bar{i}_{NP}$) tracks the $\bar{i}_{NPref}$ and the CVs are balanced under balanced bipolar dc-bus load.

Fig. 4.8. Dynamic performance of the proposed dual-mode modulation technique under different dc-load conditions: (a) Waveforms of v_{ab} , v_{C1} , v_{C2} , i_a , i_b and i_c and (b) waveforms of α (in rad), i_{NP} , $\bar{i}_{NPref}$ and $\bar{i}_{NP}$.

Under unbalanced bipolar dc-bus loads ($R_{d1} \neq R_{d2}$), a nonzero $\bar{i}_{NPref}$ is required to balance the CVs. From Fig. 4.8(b), it can be seen that with the proposed dual-mode modulation technique, the generated $\bar{i}_{NP}$ follows $\bar{i}_{NPref}$. The angle α (duration of COM) increases with the increase in load imbalance as expected. As a result, the

steady state CVs are balanced even in the presence of dc-load imbalance, as shown in Fig. 4.8(a). It is clear that the proposed dual-mode modulation technique has the capability to generate negative average NP current and maintain balanced CVs.

4.4.2 Steady State Performance of the Proposed Dual-Mode Modulation Technique

For analyzing the performance of the proposed dual-mode modulation technique comprehensively, Figs. 4.9 and 4.10 show the steady-state performance under balanced load ($R_{d1} = R_{d2}$) and unbalanced load ($R_{d1} \neq R_{d2}$), respectively. The CVs are balanced under both the cases. However, the THD of v_{ab} observed is higher under unbalanced dc-load as compared to balanced dc-load. This is due to the fact that with unbalanced dc-loads, the proposed modulation technique operates for longer duration in the COM, resulting in larger harmonic components at high frequencies. This is also observed in Fig. 4.11 that as the duration of COM, i.e., α increases, the THD of v_{ab} increases. Consequently, the ac-side currents show more distortion under unbalanced load, as observed from the THD of i_a . Figs. 4.9 and 4.10 also show the common-mode voltage (v_{CM}) obtained at steady-state which is given by:

$$v_{CM} = \frac{v_{a0} + v_{b0} + v_{c0}}{3}. \quad (4.18)$$

From Figs. 4.9(d) and 4.10(d), it is observed that as α increases, the high frequency components of v_{CM} also increase. Therefore, one of the drawbacks of the proposed modulation technique is that higher common-mode voltages are observed at higher values of α . As a result, for applications susceptible to electromagnetic interference arising from common-mode voltages, a filter needs to be designed and incorporated along with the proposed dual-mode modulation technique.

Fig. 4.9. Steady-state performance with balanced load: (a) Waveforms of v_{ab} , v_{C1} , v_{C2} , i_a , i_b and i_c , α (in rad), i_{NP} , $\bar{i}_{NPref}$ and $\bar{i}_{NP}$, (b) harmonic spectra of v_{ab} , (c) harmonic spectra of i_a , and (d) waveform of v_{CM} .

Fig. 4.10. Steady-state performance with unbalanced load: (a) Waveforms of v_{ab} , v_{C1} , v_{C2} , i_a , i_b and i_c , α (in rad), i_{NP} , $\bar{i}_{NPref}$ and $\bar{i}_{NP}$, and (b) harmonic spectra of v_{ab} , (c) harmonic spectra of i_a , and (d) waveform of v_{CM} .

Fig. 4.11. Total harmonic distortion of the line-to-line voltage (v_{ab}) at different values of α .

4.4.3 Performance of the Proposed Dual-Mode Modulation Technique under Excess Average NP Current Injection

As mentioned before, the maximum average NP current that the NPC converter can inject corresponds to $\alpha = \pi$ radians. Fig. 4.12 shows the performance of the proposed dual-mode modulation technique when R_{d1} is varied resulting in an increase in $|\bar{i}_{NPref}|$.

Fig. 4.12. Validation of maximum average NP current injection limits: Waveforms of v_{C1} , v_{C2} , α (in rad), $\bar{i}_{NPref}$ and $\bar{i}_{NP}$.

From the figure, it is clear that α increases $|\bar{i}_{NPref}|$ and reaches its maximum value of π radians when the required $|\bar{i}_{NPref}|$ is greater than the maximum average NP current injection limit. Under this condition, the CVs become unbalanced. If

an application requires an average NP current reference greater than $|\bar{i}_{NPmax}|$, an external circuit should be added to keep the CVs balanced.

4.5 Conclusions

In this chapter, a dual-mode modulation technique has been presented to balance the dc-link CVs under all bipolar dc-bus applications employing NPC converters. Using a combination of two modes, the modulation technique controls the average NP current to keep the CVs balanced. An analytical solution has been developed using the NPC converter's ac-side voltages and currents in order to determine the durations of the two modes. Experimental results confirm the effectiveness of the proposed dual-mode modulation technique under the steady-state and dynamic operations. Moreover, the analytical solution provides the maximum average NP current injection capability of the NPC converter with the proposed dual-mode modulation technique, which defines the stable operating region of the converter.

The presented analytical solutions are only valid under the assumption of balanced CVs, which limits the utilization of the proposed dual-mode modulation strategy. This shortcoming motivates extending the analysis to applications of NPC converters with unbalanced CVs. An example of such an application is a dual-input NPC inverter-based grid-connected PV system. The main objective of this system is to asymmetrically control the two PV arrays to extract the maximum possible power. The main challenge is observed when the two PV arrays operate at different irradiance levels, in turn, requiring a nonzero average NP current. Most of the solutions presented in the literature employ additional auxiliary converters to address this challenge. However, the additional cost of such auxiliary converters could partially overshadow the power generation gain during partial shading in large central inverter-based PV systems. In order to address this challenge, a control strategy to independently control the PV arrays without incorporating any additional external circuit is proposed in the next Chapter. This strategy extends the approach of linearization block presented in this chapter to generate nonzero average NP current under CV imbalance.

Chapter 5

Control Strategy for Dual-Input NPC Inverter-Based Grid-Connected Photovoltaic Systems

This chapter presents a control strategy for a dual-input NPC inverter-based grid-connected PV system to asymmetrically control the PV arrays without incorporating any additional external circuit. This is achieved by employing an analytically developed linearization block, which helps in generating the required NP current to counter for the difference in the PV currents. The analysis also provides the maximum NP current compensation limits of the NPC inverter. Experimental tests are conducted on a laboratory prototype to validate the performance of the proposed control strategy.

5.1 Introduction

A dual-input three-phase NPC inverter-based grid-connected PV system, as shown in Fig. 5.1, has an inherent advantage of achieving separate maximum power points (MPPs) for the PV strings. This results in increased PV power extraction in comparison to conventional PV systems without the NP connection.

Fig. 5.1. Circuit diagram of a dual-input (PV1, PV2) three-phase NPC inverter-based grid-connected PV system.

In Fig. 5.1, the PV arrays are connected to the bipolar dc-bus of the NPC inverter. When both PV arrays operate under the same irradiance levels ($I_{PV1} = I_{PV2}$), no average current flows through the NP and both PV arrays operate at their corresponding MPPs. Contrarily, under partial shading or array mismatch, both PV arrays need to operate at different MPPs to extract maximum power, resulting in $I_{PV1} \neq I_{PV2}$. If the difference between I_{PV1} and I_{PV2} is not compensated by the NP current, the CVs start diverging and the power conversion efficiency decreases due to the inability of the PV arrays to achieve their corresponding MPPs. Thus, it is important to compensate the required nonzero average NP current. As discussed in Section 1.2.2, modulation techniques are employed to utilize the inherent capability of NPC converter to generate this current. However, the maximum NP current injection capability of the NPC converter is limited as explained in Section 4.2. Thus, it is important to design a control strategy that is able to extract the maximum power from the solar PV arrays for the whole range of operating conditions without the addition of an external circuit.

In this chapter, a control strategy is presented for a dual-input NPC inverter-based grid-connected PV system with the objective of extracting the maximum possible power under all operating conditions. This is achieved by using a linearization block that takes actions directly proportional to the required NP current, similar to the dual-mode modulation technique. The proposed linearization block also quantifies

the maximum NP current compensation capability of the NPC converter. The proposed control strategy ensures that both PV arrays operate at their respective MPPs under partial shading and panel mismatch if the required NP current reference is less than the maximum NP current compensation capability of the NPC converter. However, if the required NP current exceeds this limit, one of the PV arrays is operated at its MPP while the operating point of the other PV array is chosen to extract the maximum possible power without incorporating any additional hardware. The advantages of the proposed control strategy are:

- It enables asymmetrical control of the PV arrays.
- It takes into account all the possible operating conditions without incorporating any auxiliary hardware.
- A feedforward compensation is incorporated in order to neutralize the effect of asymmetric PV array voltages on the ac-side voltages.
- In the proposed control strategy, the difference between the two PV currents, i.e., the NP current reference, is translated to duty cycles using a linearization block.
- The proposed linearization block is developed analytically by integrating the NP current contribution of each phase.
- The proposed block also gives the maximum average NP current compensation capability of the NPC inverter.

The chapter is organized as follows. Section 5.2 introduces the average NP current generation mechanism and the proposed linearization block. Section 5.3 provides the operating principles and the overview of an overall control system. Section 5.4 provides the experimental validation of the proposed control strategy. Section 5.5 presents simulation results to compare the performance of the proposed control strategy employing the dual-inputs of the NPC inverter to a conventional PV system without NP connection. Section 5.6 summarizes the conclusions of this chapter.

5.2 Proposed Average NP Current Regulation Strategy

As discussed under Section 5.1, for the dual-input three-phase NPC inverter-based grid-connected PV system (Fig. 5.1), the difference between I_{PV1} and I_{PV2} needs to be compensated in order to obtain a stable operation of the PV system. This difference in the current determines the required average NP current reference ($\bar{i}_{NPref}$). Thus, the main aim of the proposed control strategy is to switch the NPC inverter in such a way that the generated nonzero average NP current ($\bar{i}_{NP}$) compensates the $\bar{i}_{NPref}$.

5.2.1 Average NP Current Generation Mechanism

From Section 4.2.1, it is clear that the required nonzero average NP current can be generated by using a combination of NOM and COM (proposed dual-mode modulation technique). However, the whole analysis is carried out under the assumption that the CVs are balanced. The unbalance in the CVs, if not compensated, deteriorates the quality of ac-side voltages (Section 1.2.1). In order to ensure that the PV arrays can operate at different voltages without influencing the ac-side voltages, it is important to incorporate a zero-sequence voltage and feedforward compensation as explained in Section 2.3.

A zero-sequence voltage (v_{offc}) based on the difference in the PV voltages, is added to the normalized ac-side voltage reference (v_j^* from (2.1)) as follows:

$$v_j' = v_j^* + v_{offc}, \text{ with } j = \{a, b, c\} \text{ and } v_{offc} = \frac{v_{PV2} - v_{PV1}}{v_{PV2} + v_{PV1}}. \quad (5.1)$$

The added zero-sequence shifts the position of the ac-side references in accordance to the imbalance in the CVs. This zero-sequence voltage does not appear in the line-to-line ac-side voltages and its effect on the NP current can be easily accounted for as discussed in the next subsection. Thus, the duty cycles when the phase switches between two consecutive voltage levels is calculated using (2.6) and (2.7), wherein v_j' is given by (5.1).

Since the PV voltages are variable, the feedforward compensation is incorporated. The feedforward compensated duty-cycles under NOM are calculated (from Section

2.3) as:

$$d'_{hj} = d_{hj} \frac{v_{dc}}{2v_{PV2}}; d'_{lj} = d_{lj} \frac{v_{dc}}{2v_{PV1}}; d'_{NPj} = 1 - d'_{hj} - d'_{lj}, \quad (5.2)$$

where $v_{dc} = v_{PV1} + v_{PV2}$ and d'_{hj} , d'_{lj} and d'_{NPj} are the feedforward compensated duty cycles for connecting phase j to the positive, negative and NP dc-rails, respectively. The updated NP current is calculated using (2.37).

Fig. 5.2(a) shows the waveforms of normalized ac-side voltage, current, feed-forward compensated duty cycle of phase a , i_{NP} and $\bar{i}_{NP}$ when the PV arrays are operating at different voltages ($v_{PV1}=0.8$ pu and $v_{PV2}=1.2$ pu, where 1 pu represents $v_{dc}/2$). These waveforms are obtained using (2.37) and assuming sinusoidal ac-side voltage and current, i.e., $v_a^* = m\cos(\theta_g + \delta)$ and $i_a = I_m\cos(\theta_g)$. Moreover, as a grid-connected solar PV system is considered in this chapter, the operating power factor is taken as 1 ($\phi = 0$ rad) to ensure maximum power conversion efficiency.

Fig. 5.2. Waveforms of normalized ac-side voltages, current and feedforward compensated duty cycles of phase a , i_{NP} and $\bar{i}_{NP}$ when the solar PV arrays are operating at different voltages generating: (a) Appropriately zero $\bar{i}_{NP}$, (b) positive $\bar{i}_{NP}$ and (c) negative $\bar{i}_{NP}$.

As the resultant v_{offc} is positive, the v'_a obtained is greater than v_a^* . From Fig. 5.2(a), it is clear that when all the phases switch between two consecutive voltage levels, the average NP current contribution of phase a is very small, but not zero as in Fig. 4.2(a). This small average NP current is a consequence of unbalance in the CVs. The remaining phases can also be analyzed in the same manner. Therefore, the

obtained $\bar{i}_{NP}$ is very small over a fundamental period when all the phases switch in two consecutive voltage levels. However, if the dc-link CVs are balanced ($v_{offc} = 0$), the average NP current contribution will be, in turn, zero same as Fig. 4.2(a).

A higher magnitude of zero-sequence voltage (v_{offc}) leads to a larger nonzero average NP current ($\bar{i}_{off}$), however, this provides limited flexibility to control the generated current and to operate the PV arrays at their respective MPPs. Thus, it is important to incorporate COM, similar to Section 4.2.1, to achieve more freedom to inject the required average NP current ($\bar{i}_{NPref}$) for obtaining stable operation of the PV system.

Under COM, the phase switches between the positive and negative dc-rails, such that $d_{NPj} = 0$. The feedforward compensated duty cycles for phase j under COM are given as (derived in Section 2.3),

$$d'_{NPj} = 0; d'_{hj} = \frac{v'_j}{2} + \frac{v_{PV1}}{v_{dc}}; d'_{lj} = 1 - d'_{hj}. \quad (5.3)$$

Figs. 5.2(b) and (c) shows the same waveforms when a phase switches under COM for α interval and switches in NOM for rest of the interval. Disregarding $\bar{i}_{off}$, the generated $\bar{i}_{NP}$ is positive when the α interval coincides with the negative phase current (Fig. 5.2(b)) and is negative if the α interval coincides with the positive phase current (Fig. 5.2(c)). The α interval is placed symmetrically on the peak of the phase current same as the dual-mode modulation, as shown in Fig. 5.3. Moreover, the maximum average NP current compensation capability of the NPC inverter is obtained at $\alpha = \pi$, same as the case of dual-mode modulation. Thus, the control strategy proposed in this chapter is similar to dual-mode modulation but with an additional capability to operate the solar PV arrays at different voltages.

Fig. 5.3. Operating principle of the linearization block.

5.2.2 Effect of Zero-Sequence Voltage on Average NP Current

This subsection shows the calculation of average NP current generated due to zero-sequence voltage.

Using (2.6), (2.7) and (5.2), the feedforward compensated duty cycle for connecting phase j to the NP for positive normalized modulation signal ($v'_j \geq 0$) is given as,

$$d'_{NP_j} = \frac{v_{dc}}{2v_{PV2}}(1 - v'_j). \quad (5.4)$$

Similarly, the d'_{NP_j} for negative normalized modulation signal ($v'_j < 0$) is given as,

$$d'_{NP_j} = \frac{v_{dc}}{2v_{PV1}}(1 + v'_j). \quad (5.5)$$

The effect of zero-sequence voltage (v_{offc}) on the average NP current is easily determined by assuming all the phases are switching between two consecutive voltage levels. Considering each phase contributes equally to $\bar{i}_{off}$,

$$\frac{\bar{i}_{off}}{3} = \frac{1}{2\pi} \int_0^{2\pi} d'_{NP_a} i_a d\theta_g, \quad (5.6)$$

$$\begin{aligned} \frac{\bar{i}_{off}}{3} = \frac{1}{2\pi} & \left[\int_{-\pi/2-\beta-\delta}^{\pi/2+\beta-\delta} \frac{v_{dc}}{2v_{PV2}} \left(1 - m \cos(\theta_g + \delta) \right) I_m \cos(\theta_g) d\theta_g \right. \\ & \left. + \int_{\pi/2+\beta-\delta}^{3\pi/2-\beta-\delta} \frac{v_{dc}}{2v_{PV1}} \left(1 + m \cos(\theta_g + \delta) \right) I_m \cos(\theta_g) d\theta_g \right]. \end{aligned} \quad (5.7)$$

Here (Fig. 5.3),

$$\beta = \left| \cos^{-1} \left(\frac{v_{PV1} - v_{PV2}}{mv_{dc}} \right) - \frac{\pi}{2} \right|. \quad (5.8)$$

For ease of understanding and representation, a function $F(\theta_g, r, k)$ is defined as,

$$F(\theta_g, r, k) = \frac{-1}{2\pi} \int r(1 - m \cos(\theta_g + \delta + k)) I_m \cos(\theta_g) d\theta_g. \quad (5.9)$$

Integrating with respect to θ_g , function F is obtained as,

$$F(\theta_g, r, k) = \frac{rI_m}{8\pi} \left(m \sin(\delta + k + 2\theta_g) - 4 \sin(\theta_g) + 2m\theta_g \cos(\delta + k) \right). \quad (5.10)$$

Eq. (5.7) in terms of function F is written as,

$$\frac{\bar{i}_{off}}{3} = -F(\theta_g, r_p, 0) \Big|_{-\pi/2-\beta-\delta}^{\pi/2+\beta-\delta} - F(\theta_g, r_n, \pi) \Big|_{\pi/2+\beta-\delta}^{3\pi/2-\beta-\delta}, \quad (5.11)$$

$$\text{where } r_p = \frac{v_{dc}}{2v_{PV2}} \text{ and } r_n = \frac{v_{dc}}{2v_{PV1}}. \quad (5.12)$$

Using (5.10), (5.11) and (5.12), $\bar{i}_{off}$ is given as,

$$\bar{i}_{off} = \frac{3I_m}{4\pi} \cos(\delta) [m(r_p + r_n)(-2\beta + \sin(2\beta)) - m\pi(r_p - r_n) + 4(r_p - r_n) \cos(\beta)]. \quad (5.13)$$

From (5.13), it is clear that $\bar{i}_{off}=0$ when the dc-link CVs are balanced as $r_p = r_n$ and $\beta=0$.

5.2.3 Proposed Linearization Block

In this chapter, the required difference between the two PV currents ($\bar{i}_{NPre f}$) is translated into α . Similar to the dual-mode modulation technique, the area integrated over the α interval is proportional to the difference between the required average NP current ($\bar{i}_{NPre f}$) and the average NP current generated by the zero-sequence voltage ($\bar{i}_{off}$), as it can be seen from Fig. 5.2. Due to asymmetry observed in the reference voltages, the calculated α will be different for positive and negative value of same magnitude of $\bar{i}_{NPre f}$. Considering all the phases contribute equally to $i'_{NPre f}$, wherein $i'_{NPre f} = \bar{i}_{NPre f} - \bar{i}_{off}$, the contribution of each phase is equal to one-third of the required current. Thus,

$$\frac{i'_{NPre f}}{3} = \frac{-1}{2\pi} \int_{-\alpha/2}^{\alpha/2} d'_{NP a} i_a d\theta_g. \quad (5.14)$$

The negative sign ahead of area integrated over the α interval denotes that the average NP current generated is in the opposite direction (Figs. 5.2(b) and (c)). Using (5.4), (5.5) and (5.14), α is calculated to generate the required $\bar{i}_{NPre f}$.

If $i'_{NPre f} \leq 0$ and $v_{PV1} \leq v_{PV2}$, such that $\pi/2 + \beta - |\delta| \geq 0$, (5.14) can be written as,

$$\frac{i'_{NPre f}}{3} = \frac{-1}{2\pi} \int_{-\alpha/2}^{\alpha/2} \frac{v_{dc}}{2v_{PV2}} \left(1 - m \cos(\theta_g + \delta)\right) I_m \cos(\theta_g) d\theta_g, \quad (5.15)$$

provided that $\alpha \leq 2\alpha_1$, where $\alpha_1 = |\pi/2 + \beta - |\delta||$.

Thus, (5.15) in terms of $F(\theta_g, r, k)$ is given as,

$$\frac{i'_{NPre f}}{3} = F(\theta_g, r_p, 0) \Big|_{-\alpha/2}^{\alpha/2}. \quad (5.16)$$

Using (5.10), (5.16) is calculated as,

$$\frac{i'_{NPre f}}{3} = \frac{r_p I_m}{4\pi} \left[m \cos(\delta) \sin \alpha + \alpha m \cos(\delta) - 4 \sin \left(\frac{\alpha}{2} \right) \right]. \quad (5.17)$$

In order to obtain an analytic solution, the sine functions are approximated as quadratic functions using (4.7). Substituting (4.7) in (5.17) and rearranging, a quadratic equation in terms of α is obtained as,

$$\begin{aligned} (0.4162m \cos(\delta) - 0.33796)\alpha^2 + (-2.308m \cos(\delta) + 2.3888)\alpha \\ + \left(0.0475m \cos(\delta) - 0.09412 + \frac{4\pi i'_{NPre f}}{3r_p I_m} \right) = 0. \end{aligned} \quad (5.18)$$

Solving (5.18) for α :

$$\alpha = \frac{28850m \cos(\delta) - 29860 + 12500\sqrt{q}}{10405m \cos(\delta) - 8449}, \quad (5.19)$$

where,

$$\begin{aligned} q = 5.2477m^2 \cos^2(\delta) - 10.805m \cos(\delta) \\ - 6.9699m \frac{i'_{NPre f}}{r_p I_m} \cos(\delta) + 5.6597 \frac{i'_{NPre f}}{r_p I_m} + 5.5791. \end{aligned} \quad (5.20)$$

If the solution of α obtained under (5.19) is greater than $2\alpha_1$, (5.16) can be written as,

$$\frac{i'_{NPre f}}{3} = \begin{cases} F(\theta_g, r_p, 0) \Big|_{-\alpha/2}^{\alpha_1} + F(\theta_g, r_n, \pi) \Big|_{\alpha_1}^{\alpha/2}, & \delta \geq 0 \\ F(\theta_g, r_n, \pi) \Big|_{-\alpha/2}^{-\alpha_1} + F(\theta_g, r_p, 0) \Big|_{-\alpha_1}^{\alpha/2}, & \delta < 0. \end{cases} \quad (5.21)$$

Taking the case of $\delta \geq 0$, (5.21) upon solving yields (similar procedure applies to

$\delta < 0$ case),

$$\begin{aligned} \frac{i'_{NPre f}}{3} = \frac{I_m}{8\pi} \left[m(r_p + r_n) \sin(2\alpha_1 + \delta) - mr_n \sin(\delta + \alpha) - 4(r_p + r_n) \sin\left(\frac{\alpha}{2}\right) \right. \\ \left. + m\alpha(r_p - r_n) \cos(\delta) + 2m\alpha_1(r_p + r_n) \cos(\delta) - mr_p \sin(\delta - \alpha) \right. \\ \left. + 4(-r_p + r_n) \sin(\alpha_1) \right]. \end{aligned} \quad (5.22)$$

Rearranging (5.22),

$$\begin{aligned} m(r_p + r_n) \sin(2\alpha_1 + \delta) - mr_n \sin(\delta + \alpha) - 4(r_p + r_n) \sin\left(\frac{\alpha}{2}\right) \\ + m\alpha(r_p - r_n) \cos(\delta) + 2m\alpha_1(r_p + r_n) \cos(\delta) - mr_p \sin(\delta - \alpha) \\ + 4(-r_p + r_n) \sin(\alpha_1) - \frac{8\pi i'_{NPre f}}{3I_m} = 0. \end{aligned} \quad (5.23)$$

To solve (5.23), α is calculated as a linear function of Δv using Taylor series as,

$$\alpha = \alpha_o + \left. \frac{\partial \alpha}{\partial \Delta v} \right|_{\Delta v=0} \Delta v, \quad (5.24)$$

where $\Delta v = v_{PV1} - v_{PV2}$ and α_o is the solution of (5.23) when $\Delta v = 0$ (implying $\beta = 0$, $\bar{i}_{off} = 0$ and $r_p = r_n = 1$). α_o is obtained as,

$$\alpha_o = 2 \sin^{-1} \left(\frac{2 - \sqrt{p}}{2m \sin(\delta)} \right), \quad (5.25)$$

where,

$$p = 4 - (2m \sin(\delta)) \left(m \sin(2\alpha_1 + \delta) - m \sin(\delta) + 2\alpha_1 m \cos(\delta) - \frac{4\pi \bar{i}_{NPre f}}{3 I_m} \right) \quad (5.26)$$

and $\frac{\partial \alpha}{\partial \Delta v}$ at $\alpha = \alpha_o$ is calculated as,

$$\frac{\partial \alpha}{\partial \Delta v} = \left[\frac{8 \cos(\delta) - 4 \sin(\alpha_1) + m \cos(\delta)(\alpha_o + \sin(\alpha_o) - 2\pi) + 2mv_{dc}(\cos(\delta) + \cos(2\alpha_1 + \delta)) \frac{\partial \alpha_1}{\partial \Delta v}}{-mv_{dc} \sin(\delta) \sin \alpha_o + 2v_{dc} \cos\left(\frac{\alpha_o}{2}\right)} \right] \quad (5.27)$$

Using (5.24), (5.25) and (5.27), the complete solution for α is obtained. The

solution set for calculating α under different cases has been summarized in Table 5.1 when $i'_{NPre f} \leq 0$ and $v_{PV1} \leq v_{PV2}$. Due to the periodic nature of the reference ac-side voltages and the ac-side currents, the solution of α can be easily extended to other cases by using symmetrical modifications, as shown in Table 5.2.

Table 5.1: Function $F(\theta, r, k)$ and Solution of α when $i'_{NPre f} \leq 0$ and $v_{PV1} \leq v_{PV2}$

<p>CASE-I. $\pi/2 + \beta - \delta \geq 0$</p> $\frac{i'_{NPre f}}{3} = F(\theta_g, r_p, 0) \Big _{-\alpha/2}^{\alpha/2} \text{ only if } \alpha \leq 2\alpha_1, \text{ where } \alpha_1 = \pi/2 + \beta - \delta .$ $\alpha = \frac{28850m \cos(\delta) - 29860 + 12500\sqrt{q}}{10405m \cos(\delta) - 8449},$ <p>where $q = 5.2477m^2 \cos^2(\delta) - 10.805m \cos(\delta) - 6.9699m \frac{i'_{NPre f}}{r_p I_m} \cos(\delta)$</p> $+ 5.6597 \frac{i'_{NPre f}}{r_p I_m} + 5.5791.$
$\frac{i'_{NPre f}}{3} = \begin{cases} F(\theta_g, r_p, 0) \Big _{-\alpha/2}^{\alpha_1} + F(\theta_g, r_n, \pi) \Big _{\alpha/2}^{\alpha/2}, & \delta \geq 0 \\ F(\theta_g, r_n, \pi) \Big _{-\alpha/2}^{-\alpha_1} + F(\theta_g, r_p, 0) \Big _{-\alpha/2}^{\alpha/2}, & \delta < 0 \end{cases} \text{ only if } \alpha > 2\alpha_1,$ <p>where $\alpha_1 = \pi/2 + \beta - \delta .$</p> $\alpha = \alpha_o + \frac{\partial \alpha}{\partial \Delta v} \Big _{\Delta v=0} \Delta v, \text{ where } \alpha_o = 2\sin^{-1} \left(\frac{2 - \sqrt{p}}{2m \sin(\delta)} \right),$ $\text{and } \frac{\partial \alpha}{\partial \Delta v} = \left[\frac{8 \cos(\delta) - 4 \sin(\alpha_1) + m \cos(\delta)(\alpha_o + \sin(\alpha_o) - 2\pi) + 2mv_{dc}(\cos(\delta) + \cos(2\alpha_1 + \delta)) \frac{\partial \alpha_1}{\partial \Delta v}}{-mv_{dc} \sin(\delta) \sin \alpha_o + 2v_{dc} \cos(\frac{\alpha_o}{2})} \right],$ <p>here, $p = 4 - 2m \sin(\delta) \left(m \sin(2\alpha_1 + \delta) - m \sin(\delta) + 2\alpha_1 m \cos(\delta) - \frac{4\pi}{3} \frac{i'_{NPre f}}{I_m} \right).$</p>

Table 5.1: Function $F(\theta, r, k)$ and Solution of α when $i'_{NPre f} \leq 0$ and $v_{PV1} \leq v_{PV2}$ (continued)

<p>CASE-II. $\pi/2 + \beta - \delta < 0$</p> $\frac{i'_{NPre f}}{3} = F(\theta_g, r_n, \pi) \Big _{-\alpha/2}^{\alpha/2} \text{ only if } \alpha \leq 2\alpha_2, \text{ where } \alpha_2 = \pi/2 - \beta - \delta - \pi .$ $\alpha = \frac{28850m\cos(\delta) + 29860 - 12500\sqrt{q}}{10405m\cos(\delta) + 8449},$ <p>where $q = 5.2477m^2\cos^2(\delta) + 10.805m\cos(\delta) + 6.9699m\frac{i'_{NPre f}}{r_n I_m} \cos(\delta)$</p> $+ 5.6597\frac{i'_{NPre f}}{r_n I_m} + 5.5791.$
$\frac{i'_{NPre f}}{3} = \begin{cases} F(\theta_g, r_p, 0) \Big _{-\alpha/2}^{-\alpha_2} + F(\theta_g, r_n, \pi) \Big _{-\alpha/2}^{\alpha/2}, & \delta \geq 0 \\ F(\theta_g, r_n, \pi) \Big _{-\alpha/2}^{\alpha_2} + F(\theta_g, r_p, 0) \Big _{\alpha_2}^{\alpha/2}, & \delta < 0 \end{cases} \text{ only if } 2\alpha_3 \geq \alpha > 2\alpha_2,$ <p>where $\alpha_2 = \pi/2 - \beta - \delta - \pi$ and $\alpha_3 = \pi/2 - \beta + \delta - \pi$.</p> $\alpha = \alpha_o + \frac{\partial \alpha}{\partial \Delta v} \Big _{\Delta v=0} \Delta v, \text{ where } \alpha_o = 2\sin^{-1}\left(\frac{2 - \sqrt{p}}{2m\sin(\delta)}\right),$ $\text{and } \frac{\partial \alpha}{\partial \Delta v} = \left[\frac{8\cos(\delta) + 4\sin(\alpha_2) + m\cos(\delta)(\alpha_o + \sin(\alpha_o) - 2\pi) - 2mv_{dc}(\cos(\delta) + \cos(2\alpha_2 - \delta))\frac{\partial \alpha_2}{\partial \Delta v}}{-mv_{dc}\sin(\delta)\sin\alpha_o + 2v_{dc}\cos(\frac{\alpha_o}{2})} \right],$ <p>here, $p = 4 + 2m\sin(\delta)\left(m\sin(2\alpha_2 - \delta) + m\sin(\delta) + 2\alpha_2m\cos(\delta) + \frac{4\pi}{3}\frac{i'_{NPre f}}{I_m}\right).$</p>

Table 5.1: Function $F(\theta, r, k)$ and Solution of α when $i'_{NPre f} \leq 0$ and $v_{PV1} \leq v_{PV2}$ (continued)

$\frac{i'_{NPre f}}{3} = \begin{cases} F(\theta_g, r_p, 0) \Big _{-\alpha/2}^{-\alpha_2} + F(\theta_g, r_n, \pi) \Big _{-\alpha_2}^{\alpha_3} + F(\theta_g, r_p, 0) \Big _{\alpha_3}^{\alpha/2}, & \delta \geq 0 \\ F(\theta_g, r_p, 0) \Big _{-\alpha/2}^{-\alpha_3} + F(\theta_g, r_n, \pi) \Big _{-\alpha_3}^{\alpha_2} + F(\theta_g, r_p, 0) \Big _{\alpha_2}^{\alpha/2}, & \delta < 0 \end{cases}$ <p style="text-align: center;">only if $\alpha > 2\alpha_3$, where $\alpha_3 = \pi/2 - \beta + \delta - \pi$.</p> $\alpha = \frac{-2.308r_p m \cos(\delta) + 2.3888r_p - \sqrt{(2.308r_p m \cos(\delta) - 2.3888r_p)^2 - q}}{0.67592r_p - 0.8324r_p m \cos(\delta)},$ <p>where $q = 4 \left(0.3379r_p - 0.4162r_p m \cos(\delta) \right) \left[2(r_p - r_n)(\sin(\alpha_2) + \sin(\alpha_3)) \right.$ $\left. - m \left(\frac{r_p + r_n}{2} \right) \left(\sin(2\alpha_3 + \delta) + \sin(2\alpha_2 - \delta) \right) - 0.0475r_p m \cos(\delta) \right.$ $\left. - (\alpha_2 + \alpha_3)(r_p + r_n) m \cos(\delta) + 0.09412r_p - \frac{4\pi}{3} \frac{i'_{NPre f}}{I_m} \right]$.</p>
<p>Here, $\frac{\partial \alpha_1}{\partial \Delta v} = \frac{-\text{sign} \left(\cos^{-1} \left(\frac{\Delta v}{mv_{dc}} \right) - \frac{\pi}{2} \right) \text{sign} \left(\frac{\pi}{2} + \beta - \delta \right)}{\sqrt{m^2 v_{dc}^2 - \Delta v^2}},$</p> <p>and $\frac{\partial \alpha_2}{\partial \Delta v} = \frac{-\text{sign} \left(\cos^{-1} \left(\frac{\Delta v}{mv_{dc}} \right) - \frac{\pi}{2} \right) \text{sign} \left(\beta - \frac{\pi}{2} + \delta - \pi \right)}{\sqrt{m^2 v_{dc}^2 - \Delta v^2}}$</p>

 Table 5.2: Symmetrical Modifications to Calculate α

Conditions	Change of variables in Table 5.1
$v_{PV1} \leq v_{PV2}$ $i'_{NPre f} \leq 0$	No change
$v_{PV1} \leq v_{PV2}$ $i'_{NPre f} > 0$	$\delta \longrightarrow \delta + \pi$ $i'_{NPre f} \longrightarrow -i'_{NPre f}$
$v_{PV1} > v_{PV2}$ $i'_{NPre f} \leq 0$	$\delta \longrightarrow \delta + \pi$ $v_{PV1} \longrightarrow v_{PV2}$ $v_{PV2} \longrightarrow v_{PV1}$
$v_{PV1} > v_{PV2}$ $i'_{NPre f} > 0$	$i'_{NPre f} \longrightarrow -i'_{NPre f}$ $v_{PV1} \longrightarrow v_{PV2}$ $v_{PV2} \longrightarrow v_{PV1}$

5.2.4 Calculation of Maximum Average NP Current Compensation Capacity

As discussed earlier, it is important to quantize the maximum average NP current that can be compensated by the NPC inverter. This limit is needed for the stable operation of the PV system, as discussed in the next section. The maximum average NP current compensation capacity of the NPC inverter ($|\bar{i}_{NPmax}|$) is obtained when $\alpha = \pi$ and is shown in Table 5.3 for each case. Using Tables 5.2 and 5.3, the value of $|\bar{i}_{NPmax}|$ is easily calculated under all the operating cases.

Table 5.3: Calculation of $|\bar{i}_{NPmax}|$ when $i'_{NPref} \leq 0$ and $v_{PV1} \leq v_{PV2}$

CASE-I. $\pi/2 + \beta - \delta \geq 0$	
$ \bar{i}_{NPmax} = \begin{cases} \frac{3r_p I_m}{4\pi} (m\pi \cos(\delta) - 4) + \bar{i}_{off}, & \text{if } \alpha \leq 2\alpha_1, \\ \frac{3I_m}{8\pi} \left(m(r_p + r_n) \sin(2\alpha_1 + \delta) - 4(r_p - r_n) \sin(\alpha_1) \right. \\ \quad \left. + 2\alpha_1 m(r_p + r_n) \cos(\delta) + m(r_p + r_n) \sin(\delta) \right. \\ \quad \left. + \pi m(r_p - r_n) \cos(\delta) - 4(r_p + r_n) \right) + \bar{i}_{off}, & \text{if } \alpha > 2\alpha_1. \end{cases}$	
CASE-II. $\pi/2 + \beta - \delta < 0$	
$ \bar{i}_{NPmax} = \begin{cases} \frac{3r_n I_m}{4\pi} (-m\pi \cos(\delta) - 4) + \bar{i}_{off}, & \text{if } \alpha \leq 2\alpha_2, \\ \frac{3I_m}{8\pi} \left(4(r_p - r_n) \sin(\alpha_2) + \pi m(r_p - r_n) \cos(\delta) \right. \\ \quad \left. - m(r_p + r_n) \sin(2\alpha_2 - \delta) - 4(r_p + r_n) \right. \\ \quad \left. - 2\alpha_2 m(r_p + r_n) \cos(\delta) \right. \\ \quad \left. + m(r_p + r_n) \sin(\delta) \right) + \bar{i}_{off}, & \text{if } 2\alpha_3 \geq \alpha > 2\alpha_2, \\ \frac{3I_m}{8\pi} \left(4(r_p - r_n)(\sin(\alpha_2) + \sin(\alpha_3)) - 8r_p \right. \\ \quad \left. - m(r_p + r_n)(\sin(2\alpha_2 - \delta) + \sin(2\alpha_3 + \delta)) \right. \\ \quad \left. - 2(\alpha_2 + \alpha_3)(r_p + r_n)m \cos(\delta) \right. \\ \quad \left. + 2\pi r_p m \cos(\delta) \right) + \bar{i}_{off}, & \text{if } \alpha > 2\alpha_3. \end{cases}$	

5.3 Proposed Control Strategy

This section provides the details of the operating principles of the proposed control strategy and also presents the overview of the overall control system.

5.3.1 Operating Principle

The proposed control strategy aims to asymmetrically control the solar PV arrays and extract the maximum possible power. The operating principle of the proposed control strategy is explained as follows. Fig. 5.4 presents current-voltage ($I - V$) and power-voltage ($P - V$) curves for different possible operating conditions for the two solar PV arrays.

Fig. 5.4. $I - V$ and $P - V$ curves for the two solar PV arrays operating at: (a) Same irradiance levels, (b) small difference in irradiance levels, and (c) large difference in irradiance levels.

In Fig. 5.4(a), both PV arrays operate at the same irradiance levels (no partial shading). In this case, a zero or a small current (due to panel mismatch) flows through the NP, which can be easily compensated by the proposed control strategy.

Thus, both PV arrays operate at their respective MPPs (operating points A and B) in this case. Fig. 5.4(b) shows the case when the PV arrays operate at different irradiance levels, such that the difference between the currents at points A and B is less than the maximum average NP current compensation capability of the NPC inverter ($\bar{i}_{NPmax}$). Under this case, the proposed control strategy ensures that both PV arrays operate at their respective MPPs. In Fig. 5.4(c), the difference in the irradiance levels increases further such that the difference between the currents at A and B is higher than $\bar{i}_{NPmax}$. As the required NP current cannot be compensated, both PV arrays cannot operate at their respective MPPs simultaneously. In this case, to obtain the maximum possible power extraction, the PV array with lower power operates at its MPP ((B) in Fig. 5.4(c)) while the other array operates at the right side of its MPP (A'), in such a way that the difference between their currents matches $\bar{i}_{NPmax}$.

Therefore, the operating principle of the proposed control strategy revolves around the NP current required and the maximum average NP current compensation capability of the NPC inverter.

5.3.2 Control System

An overview of the proposed control strategy is shown in Fig. 5.5. Different components of the control system are explained below:

1. DC-link voltage management

Firstly, the PV array voltages and currents are utilized to determine the PV array powers. The PV array with lower power is named as PV-*l* and is utilized to generate the *d*-component of the ac-side current reference (i_d^*), while the array operating with higher power named as PV-*h* is employed to generate the average NP current reference ($\bar{i}_{NPref}$). This is done to ensure that the array with a lower irradiance operates at its MPP and the other array operates at the right side of its MPP (if operation on MPP is not feasible). A perturbation and observation (P&O) MPP tracking technique is employed to generate the voltage references (V_{PV-l}^* and V_{PV-h}^*) [66]. v_{PV-l}^* and v_{PV-h}^* are compared to v_{PV-l} and v_{PV-h} (measured voltages) and fed to PI controllers to generate i_d^* and $\bar{i}_{NPref}$, respectively.

(a)

(b)

Fig. 5.5. Proposed control strategy: (a) DC-link voltage management, current controller, and (b) generation of converter voltage references and calculation of duty cycles using the linearization block.

2. Current controller

The ac-side voltage references in dq frame (v_d^* and v_q^*) are generated using a typical dq -based current controller, as shown in Fig. 5.5.

3. Generation of converter voltage references

v_d^* and v_q^* are transformed into abc frame (v_a^* , v_b^* and v_c^*) using the dq -to- abc transformation.

4. Calculation of duty cycles using the linearization block

In the proposed control strategy, for the required $\bar{i}_{NPref}$, a value of α is obtained, which is then translated to duty cycles. During the α interval, the NP duty cycle for the phase switching between the positive and negative dc-rails is zero

and the duty cycles for connecting the respective phase to the positive and negative dc-rails are calculated using (5.3), as shown in Fig. 5.6.

Fig. 5.6. Calculation of the duty cycles using a linearization block.

For the remaining time period, the phase switches between two consecutive voltage levels and the duty cycles are calculated by using (5.2).

The obtained duty cycles are compared to the carrier signal to generate the switching pulses of the NPC inverter [63] via the state-machine model (Appendix B).

5.4 Experimental Results

In order to validate the performance of the proposed control strategy, experimental tests have been performed on a laboratory prototype (as described under Section 2.2.3) with the circuit diagram shown in Fig. 5.1. In addition to the dSPACE controller and the NPC converter, two PV emulators (using GE&EL 15 kVA Cinergia and Chroma 62050H-600S) and a grid simulator (Chroma programmable ac source 61511) are employed. The setup is shown in Fig. 5.7 and the parameters of the prototype are listed in Table 5.4.

Fig. 5.7. Picture of the hardware prototype.

Table 5.4: Experimental and Simulation Parameters

Parameter	Value
Grid phase voltage (rms)	110 V
Grid frequency, f	50 Hz
Grid filter inductor, L	10 mH
Carrier frequency, f_s	2 kHz
DC-link capacitors (each), C_1, C_2	2.2 mF
Open-circuit PV voltages, $V_{OC_{PV1}}, V_{OC_{PV2}}$	224.59 V
Short-circuit PV currents, $I_{SC_{PV1}}, I_{SC_{PV2}}$	5.146 A
MPP PV voltage (1000 W/m ² , 50° C), $V_{MP_{PV1}}, V_{MP_{PV2}}$	175 V
MPP PV power (1000 W/m ² , 50° C), $P_{MP_{PV1}}, P_{MP_{PV2}}$	800 W

5.4.1 Performance under Step Change of Irradiance

Figs. 5.8 and 5.9 shows the performance of the proposed control strategy when PV2 undergoes a step change in irradiance, while PV1 operates at a constant irradiance. Fig. 5.8 shows various waveforms of the experimental setup under the mentioned step change of irradiance. Fig. 5.9 tracks the operating points of the PV arrays on the PV curve with respect to time. The operating points of PV1 are denoted by ‘o’ while PV2 are represented by ‘+’.

During Interval 1 of Fig. 5.8, both PV arrays operate at the same irradiance level, i.e., $Irr_{PV1} = Irr_{PV2} = 1000 \text{ W/m}^2$, hence, the required $\bar{i}_{NPref}$ is very close to zero and the required α is very small in this case. From Figs. 5.8 and 5.9, it is clear that both PV arrays operate at their MPPs under this condition with $v_{PV1} = v_{PV2} = 175 \text{ V}$ and $p_{PV1} = p_{PV2} = 800 \text{ W}$. This result validates the operating condition discussed under Fig. 5.4(a), i.e., MPP is achieved by both PV arrays while operating with the same irradiance levels.

During Interval 2, Irr_{PV2} changes to 800 W/m^2 with PV1 operating at 1000 W/m^2 , hence, the required $\bar{i}_{NPref}$ increases. As a result, α also increases in order to generate an average NP current equal to the required $\bar{i}_{NPref}$. The solar array PV2 tracks its new MPP ($v_{PV2} = 169 \text{ V}$ and $p_{PV2} = 640 \text{ W}$), while array PV1 remains at the same operating point ($v_{PV1} = 175 \text{ V}$ and $p_{PV1} = 800 \text{ W}$). This interval shows the condition discussed under Fig. 5.4(b) where the required $\bar{i}_{NPref}$ is less than $\bar{i}_{NPmax}$. During this interval, $\bar{i}_{NPref}$ is generated by switching a phase in three voltage levels for α duration. Moreover, both PV arrays still track their respective MPPs.

During Interval 3, the required $\bar{i}_{NPref}$ exceeds $\bar{i}_{NPmax}$ when Irr_{PV2} changes to 600 W/m^2 with $Irr_{PV1} = 1000 \text{ W/m}^2$. Under this condition, the solar array PV2 tracks its new MPP ($v_{PV2} = 162 \text{ V}$ and $p_{PV2} = 480 \text{ W}$) and α saturates at π radians in order to generate the maximum $\bar{i}_{NP}$. Under this condition, the solar array PV1 operates at the right side of its MPP so that the difference between the PV currents equals $\bar{i}_{NPmax}$. This helps in achieving stable operation of the grid-connected PV system without incorporating any additional auxiliary converter. This result validates the condition discussed under Fig. 5.4(c) wherein the required $\bar{i}_{NPref}$ is greater than $\bar{i}_{NPmax}$.

Therefore, from Figs. 5.8 and 5.9, it is clear that the proposed control strategy

Fig. 5.8. Performance of the proposed control strategy when solar array PV2 operates under step change in irradiance: Waveforms of Irr_{PV1} and Irr_{PV2} , v_{PV1} and v_{PV2} , i_{PV1} , i_{PV2} , $\bar{i}_{NPre}$ and $\bar{i}_{NP}$, p_{PV1} , p_{PV2} and p_g , α (in rad).

effectively extracts the maximum possible power under all operating conditions. Fig. 5.10 shows the harmonic spectra of v_{ab} and Fig. 5.11 depicts the harmonic spectra of i_a under different irradiance levels of PV2. As the irradiance difference increases, α increases in order to provide the required average NP current. The increase in α implies that the chosen phase is switching for longer duration in three voltage levels. If $2\pi/3 < \alpha \leq \pi$, two phases switch in three voltage levels simultaneously. The increase in α results in more harmonic components at high frequencies, thereby increasing the THD of line-to-line voltage and grid current as visible from Figs. 5.10 and 5.11.

Fig. 5.9. Performance of the proposed control strategy when solar array PV2 operates under step change in irradiance: (a) PV1 operating points and (b) PV2 operating points.

Fig. 5.10. Harmonic spectra of v_{ab} when $I_{rr_{PV1}}$ is 1000W/m^2 and $I_{rr_{PV2}}$ is: (a) 1000W/m^2 , (b) 800W/m^2 and (c) 600W/m^2 .

Fig. 5.11. Harmonic spectra of i_a when Irr_{PV1} is 1000 W/m^2 and Irr_{PV2} is: (a) 1000 W/m^2 , (b) 800 W/m^2 and (c) 600 W/m^2 .

5.4.2 Performance under Linear Change of Irradiance

Fig. 5.12 shows the same waveforms when solar array PV2 is subjected to a linear change of irradiance while PV1 operates at a constant irradiance of 1000 W/m^2 .

Initially, $Irr_{PV1} = 1000 \text{ W/m}^2$ and $Irr_{PV2} = 500 \text{ W/m}^2$, which results in an $\bar{i}_{NPref}$ larger than $\bar{i}_{NPmax}$. Under this case, solar array PV2 tracks its MPP, while solar array PV1 operates at the right side of its MPP. α is saturated at π radians, such that $\bar{i}_{NP} = \bar{i}_{NPmax}$.

As the irradiance of solar array PV2 increases, its current and power increase as it tracks its MPP. Besides, initially the required $\bar{i}_{NPref}$ is greater than $\bar{i}_{NPmax}$ and α is saturated at π radians. Consequently, as i_{PV2} increases, i_{PV1} increases as well and PV1 starts moving towards its MPP. After $\bar{i}_{NPref}$ goes below $\bar{i}_{NPmax}$, α starts

Fig. 5.12. Performance of the proposed control strategy when solar array PV2 operates with linear change in irradiance: Waveforms of Irr_{PV1} and Irr_{PV2} , v_{PV1} and v_{PV2} , i_{PV1} , i_{PV2} , $\bar{i}_{NPref}$ and $\bar{i}_{NP}$, p_{PV1} , p_{PV2} and p_g , and α (in rad).

decreasing. At this point, the converter is able to compensate for the difference in PV currents and PV1 reaches its MPP. When $Irr_{PV1} = Irr_{PV2} = 1000 \text{ W/m}^2$, both the solar arrays operate at their respective MPPs and the obtained α is small. The required $\bar{i}_{NPref}$ is also close to zero in this operating condition.

A vice-versa operation is observed when the irradiance of solar array PV2 starts decreasing. With decreasing Irr_{PV2} , α increases when the required $\bar{i}_{NPref}$ is lower than $\bar{i}_{NPmax}$. During this time, both solar PV arrays operate at their respective MPPs. While $\bar{i}_{NPref} > \bar{i}_{NPmax}$, α is saturated at π radians. The solar array PV2 tracks its MPP while the solar array PV1 operating point shifts to the right-side of its MPP in order to generate an $\bar{i}_{NP}$ equal to $\bar{i}_{NPmax}$. As can be seen from this figure, the dynamic of v_{PV1} is synchronized with the saturation of α . This indicates that the proposed control strategy can control the two PV arrays independently as

long as the maximum NP current limit is not reached ($\alpha < \pi$). Hence, while $\alpha < \pi$, v_{PV1} can remain at its MPP irrespective of Irr_{PV2} dynamic. For $\alpha = \pi$ radians, the condition is the same as in Fig. 5.4(c) and PV1 operates at the right side of its MPP. The results shown in Fig. 5.12 verify the effectiveness of the proposed control strategy for extracting the maximum possible power from PV arrays under linear increase/decrease of irradiance.

5.4.3 Performance with Asymmetrical PV Arrays

In order to validate the performance of the proposed control strategy for asymmetrical PV arrays, two PV arrays with different open-circuit voltages and short-circuit currents ($V_{OC_{PV1}} = 224.59$ V, $I_{SC_{PV1}} = 5.146$ A, $V_{OC_{PV2}} = 192.5$ V and $I_{SC_{PV2}} = 4.8$ A) are used. Fig. 5.13 shows the waveforms when PV2 is subjected to a step change in irradiance, while PV1 operates at a constant irradiance. Fig. 5.14 track the operating points of the PV arrays on the PV curve with respect to time. The operating points of PV1 are denoted by ‘o’ while PV2 are represented by ‘+’.

During Interval 1 of Fig. 5.13, both PV arrays operate at the same irradiance level, i.e., $Irr_{PV1} = Irr_{PV2} = 1000$ W/m², the required $\bar{i}_{NPref}$ is very small in this case. From Figs. 5.13 and 5.14, it is clear that both PV arrays operate at their MPPs under this condition with $v_{PV1} = 175$ V, $p_{PV1} = 800$ W and $v_{PV2} = 150$ V, $p_{PV2} = 640$ W. During Interval 2, Irr_{PV2} changes to 800 W/m² with PV1 operating at 1000 W/m², hence, $\bar{i}_{NPref}$ increases. As a result, α also increases in order to generate an average NP current equal to $\bar{i}_{NPref}$. The solar array PV2 tracks its new MPP ($v_{PV2} = 145$ V and $p_{PV2} = 512$ W), while array PV1 remains at the same operating point ($v_{PV1} = 175$ V and $p_{PV1} = 800$ W). During Interval 3, $\bar{i}_{NPref}$ exceeds $\bar{i}_{NPmax}$ when Irr_{PV2} changes to 600 W/m² with $Irr_{PV1} = 1000$ W/m². Under this condition, the solar array PV2 tracks its new MPP ($v_{PV2} = 139$ V and $p_{PV2} = 384$ W) and α saturates at π radians in order to generate the maximum $\bar{i}_{NP}$. Under this condition, the solar array PV1 operates at the right side of its MPP so that the difference between the PV currents equals $\bar{i}_{NPmax}$. Therefore, it is clear that both PV arrays operate at their respective MPPs when $\bar{i}_{NPref} \leq \bar{i}_{NPmax}$, even with asymmetrical PV arrays. If $\bar{i}_{NPref} > \bar{i}_{NPmax}$, α saturates at π radians and, as desired, solar array PV2 tracks its MPP while PV1 operates at the right side of its MPP.

Fig. 5.13. Performance of the proposed control strategy with asymmetrical PV arrays: Waveforms of Irr_{PV1} and Irr_{PV2} , v_{PV1} and v_{PV2} , i_{PV1} , i_{PV2} , $\bar{i}_{NPref}$ and $\bar{i}_{NP}$, p_{PV1} , p_{PV2} and p_g , and α (in rad).

Fig. 5.14. Performance of the proposed control strategy with asymmetrical PV arrays: (a) PV1 operating points and (b) PV2 operating points.

5.5 Comparative Analysis

Simulation tests are performed to compare the performance of the proposed control strategy employing the dual-inputs of the NPC inverter (Fig. 5.1) to a conventional PV system without NP connection by using the parameters provided in Table 5.4. In the conventional system, both PV1 and PV2 are connected in series between the positive and the negative dc-rails of the NPC inverter, as shown in Fig. 5.15 [67,68].

Fig. 5.15. Circuit diagram of a conventional three-phase NPC inverter-based grid-connected PV system without NP connection [67,68].

Therefore, a single MPP tracking for both PVs is used in the conventional system. However, the configuration employed in this chapter employs the dual-inputs of the NPC inverter to independently control the solar PV arrays to achieve separate MPPs. The total PV power extracted from the two PV arrays under different cases of irradiance differences is shown in Fig. 5.16.

The irradiance of PV1 array is kept at 1000 W/m², while the irradiance of PV2 array is decreased from 1000 W/m² in steps of 50 W/m² at intervals of one second. From this figure, it is clear that with the proposed solution, the power extracted from the solar PV arrays under all the cases of partial shading is higher compared to the conventional PV system.

Fig. 5.16. Performance comparison between the proposed control strategy employing dual-inputs of the NPC inverter and a conventional PV system without using NP connection.

5.6 Conclusions

In this chapter, a control strategy for dual-input NPC inverters-based grid-connected PV systems has been presented. The strategy has been designed to extract the maximum possible power from the PV arrays under all operating conditions without incorporating any additional auxiliary converter. A feedforward compensation has also been incorporated to compensate the effect of asymmetric PV array voltages on the grid-side voltages. In addition, a linearization block has been analytically developed, which helps in translating the required NP current reference to duty cycles. The maximum average NP current compensation capability of the NPC inverter has also been quantified using the proposed linearization block, which gives a freedom to operate both solar PV arrays at MPP until the converter becomes saturated. Once the required NP current reference is higher than the maximum average NP current compensation limit, the converter saturates and the developed control strategy allows to operate the PV array with lower irradiance at its MPP, while the other PV array is operated at the maximum possible power under saturated conditions. In this way, the efficiency of the whole system is optimized. Experimental results verify the effectiveness of the proposed strategy in extracting the maximum possible power under all operating conditions.

Chapter 6

Conclusions and Future Work

This chapter summarizes the work that has been done and presents the directions for future research work.

6.1 Conclusions

This thesis has presented modulation and control techniques to improve the CV balancing in NPC converters. The main conclusions are summarized as follows:

- A new modulation technique with the capability to limit the CV ripples within specified limits has been presented for a three-phase NPC converter. A feed-forward compensation has also been incorporated in order to compensate for the negative effect of the CV imbalances on the output voltages. Though the switching losses are higher than with the two-level modulation, the voltage controllability is better with the proposed technique. Moreover, the losses are always lower than those produced by modulation strategies where one phase is switching in three levels all the time. Therefore, the proposed feedforward compensated modulation technique represents a trade-off solution between the voltage ripple magnitude and the switching power losses. As the CV ripples are allowed to vary within specified limits, it is easy to design the NPC converter, since the maximum voltage that the dc-link capacitors and the power semiconductors have to withstand is predefined.

The proposed feedforward compensated modulation technique has been tested with balanced, unbalanced and nonlinear loads on a laboratory prototype to validate its capability to regulate the CVs within the specified limits. Even with large initial CV imbalances and nonlinear loads enriched with even-order harmonics, the proposed modulation strategy limits the CV ripples within the specified limits.

- The BL-3L modulation technique has been proposed for a three-phase NPC converter to balance the average CVs under all operating conditions. In addition to a predefined voltage band, this modulation technique employs a variable current band. If the instantaneous CVs exceed the voltage band, then an appropriate phase-leg is switched in three-level modulation to guarantee the CVs do not diverge further. If the instantaneous CVs reside within the voltage band, a variable current band is used to regulate switching in three voltage levels in order to obtain lower switching losses as compared to the conventional three-level modulation technique. Therefore, the proposed BL-3L modulation technique presents a trade-off between the switching losses and the CV ripple.

Experimental results, obtained on the developed laboratory prototype, under different loading conditions verify the effectiveness of the proposed BL-3L modulation technique to achieve balanced average CVs. A performance comparison among the two-level, three-level, feedforward compensated and BL-3L modulation techniques has also been presented. The results showed that the BL-3L modulation technique has the capability to balance the average CVs even in the presence of highly nonlinear loads enriched in second harmonics.

- In order to address the challenge of generating a nonzero average NP current without employing any additional hardware, a dual-mode modulation technique has been presented for the NPC converter. The two operating modes are the normal operation mode (NOM) and the compensating operation mode (COM). In the NOM, the phase switches between two consecutive voltage levels in a switching period. Under the COM, the phase switches between the positive and the negative dc-rails in a switching period, implying that the NP duty cycle of that phase is zero. An analytical solution has been developed to determine the duration of these two operation modes within each fundamental cycle based on the converter's operating condition. An advantage of this solution is that it can be generalized for balancing the average CVs in all applications employing

NPC converters. The proposed solution also determines the maximum average NP current injection capacity of the NPC converter under the dual-mode modulation technique, which indicates the stable operating range of the converter.

The performance of the proposed dual-mode modulation technique has been validated experimentally for a three-phase grid-connected NPC converter feeding bipolar dc-loads. The steady-state and dynamic performances of the proposed technique have been analyzed under different dc-load conditions. The obtained results verify the capability of the analytically developed solution to keep the CVs balanced. Moreover, it has been observed that the CVs diverge when the required NP current exceeds the maximum average NP current injection capability of the NPC converter.

- The proposed dual-mode modulation technique has been extended to generate a nonzero average NP current for a dual-input NPC inverter-based grid-connected PV system. The control strategy has been designed to achieve asymmetrical control of the PV arrays without incorporating any additional external circuit. An analytically developed linearization block is utilized to counter for the difference in the PV currents. In addition, the maximum NP current compensation limits of the NPC inverter with unbalanced CVs have also been determined. If the required NP current reference is less than the maximum limit, both PV arrays operate at their MPPs. However, if the required current exceeds the limit, one of the PV arrays operates at its MPP while the output power of the other PV array is reduced to satisfy the NP current limit.

Experimental tests have been conducted on a laboratory prototype to validate the performance of the proposed control strategy under step and linear change of irradiance. The obtained results showed that the solar PV arrays operate at their respective MPPs when the required NP current reference is less than the maximum limit and only one of the PV arrays operate at its MPP when the maximum limit is exceeded. Similar conclusions are obtained when the proposed control strategy is employed with asymmetrical PV arrays. A comparative analysis to a conventional PV system without using NP connection shows that with the proposed solution, the power extracted from the solar PV arrays under all cases of partial shading is higher.

6.2 Future Work

Apart from the work presented in this thesis, there are various interesting topics related to the NPC converters which require further exploration. These suggestions are described as follows:

- The effect of min-max based zero-sequence voltage injection (v_{offm}) on the maximum average NP current limit ($\bar{i}_{NPmax}$) can be analyzed for an NPC converter. $\bar{i}_{NPmax}$ plays an important role in determining the stable operation range of the converter in applications that impose a nonzero average NP current, like NPC converters feeding multiterminal dc loads, back-to-back-connected NPC converters-based wind and high voltage dc transmission systems, etc. In this thesis, the $\bar{i}_{NPmax}$ limits have been determined for NPC converter with balanced and unbalanced CVs in Chapters 4 and 5, respectively. However, the zero-sequence voltage injection (v_{offm}) was not taken into account. As the added v_{offm} affects the NP duty cycles, and in turn the NP current, it is necessary to analyze its effect.
- Comparing different modulation techniques on the basis of their maximum average NP current compensation capability and determine the best solution for applications requiring a nonzero average NP current is another future research direction in line with the topic of this thesis. This will also help in analyzing the effect of different modulation techniques on the stable operating range of the converter.
- The linearization blocks presented in Chapters 4 and 5 to translate the required average NP current to duty cycle involve switching the phase in compensating operation mode (COM) for an α span. This span is placed around the positive or negative peak of the phase current. Another solution to produce the required average NP current can be to distribute this α span into smaller intervals and develop a dual-layer modulation technique. The main objectives of this modulation technique will be to achieve faster dynamics and reduced mathematical computations compared to the conventional approach of dual-mode modulation technique.
- In Chapter 5, a dual-input NPC inverter-based grid-connected PV system is considered, wherein the maximum NP current compensation capability of the

NPC converter has been analytically calculated. These limits can be incorporated with the PV natural balancing to feed constant power to the grid. It will be interesting to explore this solution and test the performance of the system under different irradiance levels.

- Another research direction is to extend the modulation strategies presented in Chapters 2 and 3 to multiphase NPC converters to minimize the switching losses and NP voltage ripples. There will be multiple combinations which can reduce the NP voltage ripples in multiphase systems. However, the solution with lower switching loss should be selected while designing an optimized modulation technique to achieve a trade-off between the voltage ripple magnitude and the switching loss.
- The research focus for this thesis has been on three-level NPC converters. As a next step, the solutions presented in this thesis can be extended to multilevel diode-clamped converters. Most of the techniques for diode-clamped converters proposed in the literature are based on complex implementations and are not generalized. Therefore, the modulation techniques for the diode-clamped converters need to be further explored to develop simpler and generalized solutions.

Appendix A

Laboratory Prototype

In order to validate the performance of the proposed modulation and control techniques presented in the thesis, a hardware prototype of a five-phase five-level diode-clamped converter has been developed in the laboratory. In this thesis, the five-level converter is operated as a three-level converter, by employing two levels as transition points. Consider the functional diagram of the multiphase multilevel diode clamped converter shown in Fig. 1.4. For a five-level converter, the dc-side has 5 levels as $n = 5$, namely, 0, 1, 2, 3 and 4. Out of these, 1 and 3 are taken as the transition points to operate this converter as a three-level converter. ‘0’, ‘2’ and ‘4’ are employed as the negative dc-rail, the NP and the positive dc-rail, respectively. Each phase connects to these transition points for small waiting time in order to avoid unexpected switching states during level transitions.

The laboratory developed prototype is controlled using a dSPACE 1007 controller. An optical transmitter is used to transmit the switching pulses from the controller. A receiver is employed to receive these pulses and feed to the gate driver (SEMIDRIVER high power IGBT driver SKHI 10/12). In order to have a flexible system, the phase legs of the NPC converter are designed individually. In this thesis, three-phase NPC converter is employed to validate the proposed modulation techniques. Moreover, sensors (Hall-effect based LV 25-P and LA 55-P) are employed to measure the system’s voltages and currents. The information from these sensors is fed to the controller using the dSPACE ADC channels.

Printed circuit boards of the NPC phase leg, transmitter, receiver and sensor are designed using the Altium Designer, as shown in Figs. A.1 and A.2.

Fig. A.1. Printed circuit board of the NPC phase leg.

Fig. A.2. Printed circuit boards of transmitter, receiver, voltage and current sensors.

These PCBs are first soldered and tested. All these PCBs are then stacked, as shown in Fig. A.3, to build the NPC converter.

Fig. A.3. Stacking of PCBs to build the NPC converter.

The obtained NPC converter is then incorporated with different loads and sources, as shown in Figs. 2.2, 4.6(b) and 5.7, to validate the performance of different modulation techniques.

Appendix B

State Machine Model

The calculated switching pulses, obtained by comparing the duty cycles and the carrier signal, are first fed to a state machine, as shown in Fig. B.1. The state machine model has been implemented in practice to avoid any forbidden commutation state of the converter. It plays an important role in case the semiconductors of the converter are not able to deal with the total dc-link voltage. The state-machine model also helps in reducing the dv/dt while operating in three voltage levels.

Fig. B.1. State-machine model.

The state of the switches is determined by the next state of switches $S4$ and $S3$. The duration of the holding states (State H1 and H2) is in the order of magnitude of dead-time and it does not affect the operation of the converter.

In order to understand the functioning of the state-machine model, let's assume the current state of phase j is at high-level such that the states of switches [S4 S3 S2 S1] is [1 1 0 0] and the next state is low-level with switching state [0 0 1 1]. The state of the switches [S4 S3] is [0 0] for this change. From the state-machine model, the transition steps are as follows:

From this, it is clear that switching a phase in three voltage levels, i.e., between positive and negative dc-rails, is a four-step process. This process helps in reducing the dv/dt and also in avoiding forbidden commutation states.

The duty cycles generated from the state machine are then compared with the carrier signal to generate the switching pulses of the NPC converter [63].

List of Publications

Accepted Journal Papers

- [1] **N. Beniwal**, J. Pou, S. Ceballos, C. D. Townsend, G. Konstantinou, H. D. Tafti, and G. G. Farivar, “Feedforward modulation for the neutral-point-clamped converter with confined capacitor voltage ripples and reduced switching power losses,” *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 4426-4438, Apr. 2020.
- [2] **N. Beniwal**, C. D. Townsend, G. G. Farivar, J. Pou, S. Ceballos, and H. D. Tafti, “Band-limited three-level modulation for balancing capacitor voltages in neutral-point-clamped converters,” *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9737-9752, Sep. 2020.
- [3] **N. Beniwal**, G. G. Farivar, H. D. Tafti, J. Pou, S. Ceballos, G. Konstantinou, and C. D. Townsend, “A dual-mode modulation technique for controlling the average neutral point current in neutral-point-clamped converters,” *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 6079-6091, May 2021.
- [4] **N. Beniwal**, H. D. Tafti, G. G. Farivar, S. Ceballos, J. Pou, and F. Blaabjerg, “A control strategy for dual-input neutral-point-clamped inverter-based grid-connected photovoltaic system,” *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 9743-9757, Sep. 2021.
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Accepted Conference Papers

- [7] **N. Beniwal**, J. Pou, C. D. Townsend, and S. Ceballos, “Enhancing the natural voltage balancing capability of neutral-point-clamped converters under carrier-based pulsewidth modulation,” in *Proc. of IEEE 4th Southern Power Electron. Conf. (SPEC)*, Singapore, 2018, pp. 1-6.
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- [10] **N. Beniwal**, G. G. Farivar, S. Ceballos, N. B. Y. Gorla, and J. Pou, “Effect of zero-sequence voltage on the maximum average neutral-point current limit in neutral-point-clamped converters,” presented in *Proc. of 47th Annual Conf. of the IEEE Ind. Electron. Society (IECON)*, Toronto, Canada, 2021.
- [11] Z. Jiang, **N. Beniwal**, S. Ceballos, J. Pou, H. D. Tafti, and G. G. Farivar, “Analysis of the average neutral-point current limits of the neutral-point-clamped converter under three-level modulation,” in *Proc. of 46th Annual Conf. of the IEEE Ind. Electron. Society (IECON)*, Singapore, 2020, pp. 4079-4084.
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Papers to be Submitted

- [17] **N. Beniwal**, G. G. Farivar, H. S. Lam, S. Ceballos, N. B. Y. Gorla, J. Pou, S. Y. R. Hui, and F. Blaabjerg, “A dual-layer pulsewidth modulation technique for average neutral point current control in neutral-point-clamped converter,” to be submitted to *IEEE Trans. Power Electron.*.
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