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A Comparison of the Battery Fault Tolerance of Modular Multilevel Converters with Half-Bridge and Full-Bridge Submodules

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Abstract—The modular multilevel converter (MMC) is a promising option to integrate battery energy storage systems (BESSs) into the power system. Both half-bridge submodules (SMs) and full-bridge SMs can be used to implement an MMC. For MMC-based BESS, it is important to have sufficient battery fault tolerance, which means the system can operate normally even when some SMs have faulty batteries or no batteries. This paper analyzes and compares the battery fault tolerance of MMC-based BESSs with half-bridge and full-bridge SMs. According to the quantitative comparison, the MMC with full-bridge SMs has considerably higher tolerance to battery faults when the active power requirement is relatively high. Simulation and experimental results are provided for the verification of the proposed analysis.

Index Terms—Battery energy storage system (BESS), fault tolerance, modular multilevel converter (MMC).

I. INTRODUCTION

Due to the increase of renewable energy generation, grid-connected battery energy storage systems (BESSs) are growing rapidly. Modular multilevel converters (MMCs) are popular and flexible candidates to connect BESSs to the power system, especially for medium/high-voltage applications that require a dc-terminal [1]. Compared to the conventional two-level converters, multilevel converters provide evident advantages, such as modularity and better harmonic performance at lower switching frequencies. [2].

Fig. 1(a) depicts the circuit diagram of one phase of MMC-based BESS, where the SMs can be either half-bridge SMs as in Fig. 1(b) or full-bridge SMs as in Fig. 1(c). The half-bridge SM can only output a positive or zero voltage, while the output voltage of a full-bridge SM can be positive, zero or negative. Since the half-bridge SM has fewer components and lower power losses, it is more commonly used in MMC applications without batteries [3]. Nevertheless, the full-bridge SM provides some advantages, such as blocking the dc-fault

Fig. 1. Circuit diagram of the MMC: (a) Single phase system, (b) half-bridge SM, and (c) full-bridge SM.

Fig. 2. Connecting the batteries to SM: (a) Directly, and (b) through a dc-dc converter.

current of the converter, while the half-bridge SM cannot. Hence, the full-bridge SM is preferred in some applications.

When the MMC is used to connect batteries to the grid, it is preferred to integrate the battery units into the SMs instead of the dc-link of the MMC, because it provides higher flexibility for the battery management, e.g., balancing the states of charge (SoC) [4]. Moreover, by integrating the battery units into the

SMs, a long string of batteries, whose operation is limited by the weakest unit, can be avoided [5]. Battery units can be directly connected to the dc-link of the SM or through a dc-dc converter, as depicted in Figs. 2 (a) and (b), respectively. Though the dc-dc converter in Fig. 2(b) is a boost converter, other topologies can also be applied.

For the BESSs based on the MMC, it is important to have battery fault tolerance, which means the system can still work with batteries of some SMs being faulty. When the integrated batteries become faulty, the corresponding SMs cannot process active power anymore, hence the active power requirement has to be shared by the remaining SMs with healthy batteries. Nevertheless, the SMs with faulty batteries can still operate as a standard SM without batteries, providing output voltage and reactive power to support the operation of the converter. Moreover, in some applications, batteries are integrated into some SMs of each arm instead of all the SMs [6]. Hence, the remaining SMs cannot provide/absorb active power, which is equivalent to the existence of battery faults.

A problem under the aforementioned scenarios is, the MMC requires a certain percentage of SMs in each arm to process the required active power [7], [8]. In other words, if too many SMs in one arm have faulty batteries, the MMC can fail to meet the active power requirement. Therefore, the battery fault tolerance of a BESS can be assessed with the maximum percentage of SMs with faulty batteries that the converter can tolerate. The knowledge of the battery fault tolerance is helpful for the system control with battery faults and design optimization, like how many SMs can be integrated with renewable resources instead of batteries.

There has been some investigations on the battery fault tolerance of the MMC-based BESS [6], [9]–[11]. It is revealed that the tolerance varies with the operating condition of the MMC. However, these investigations are limited to the MMC with half-bridge SMs or the hybrid MMC that combines half-bridge SMs without batteries and full-bridge SMs with batteries [6]. So far, there is no investigation on the battery fault tolerance of the MMC-based BESS with full-bridge SMs.

To address this gap, this paper proposes a general analysis of the battery fault tolerance of the MMC-based BESS, which can be applied to half-bridge and full-bridge SMs. Moreover, as both SMs can be used to construct an MMC-based BESS, this paper compares the fault tolerance abilities of the MMC with half-bridge SMs and the MMC with full-bridge SMs, which can help to decide which kind of SMs should be used in different applications. The results indicate that, compared to the MMC with half-bridge SMs, the MMC with full-bridge SMs has considerably higher battery fault tolerance. Simulation and experimental results are provided to verify the proposed analysis.

The remainder of this paper is organized as follows. Section II proposes a method to assess the battery fault tolerance of the MMC-based BESS, which can be applied to both half-bridge and full-bridge SMs. Section III compares the battery fault tolerance of the BESSs with half-bridge SMs and

full-bridge SMs. To verify the proposed analysis, simulation and experimental results are provided in Sections IV and V. Finally, Section VI summarises the main conclusions of the paper.

II. ASSESSMENT OF BATTERY FAULT TOLERANCE

As reported in [7], [8], there exist certain limits for the amount of active power that can be processed by a subset of SMs in one arm of the MMC. The fault tolerance of an MMC-based BESS is decided by the active power limits of SMs. For example, if 30% of the SMs in one arm can provide the required active power, the MMC-based BESS can operate even with faulty batteries in 70% of the SMs. In other words, the battery fault tolerance of an MMC-based BESS can be assessed with the knowledge of the SM active power limits. The derivation of active power limits of half-bridge SMs has been analyzed in [7], [8]. This section first extends the analysis to full-bridge SMs and then investigates the battery fault tolerance for both choices of SMs. The proposed analysis focuses on one arm of the MMC with N SMs and can be readily applied to other arms.

A. Active Power Limits of Full-Bridge Submodules

The active power of one SM is calculated as:

$$\bar{P}_{SMi} = \frac{1}{T} \int_{t_0}^{t_0+T} v_{SMi}(t) i_{arm}(t) dt, \quad (1)$$

where T represents the fundamental voltage period, i_{arm} is the arm current, v_{SMi} and $\bar{P}_{SMi}$ are the instantaneous output voltage and active power of the i th SM, respectively. A positive value of $\bar{P}_{SMi}$ means this SM absorbs active power. The value of v_{SMi} can change within $[-v_C, v_C]$, where v_C represents the capacitor voltage. To achieve the maximum power of an SM, its output voltage should be maximum when the arm current is positive and should be minimum when the arm current is negative. This can be generalized to an arbitrary combination of n SMs, where $n \in [1, N]$. Hence, the maximum power of n SMs can be derived as:

$$\begin{aligned} \bar{P}_{max}^n &= \frac{1}{T} \int_{t_0}^{t_0+T} v_{max}^n(t) i_{arm}(t) dt, \\ v_{max}^n(t) &= \begin{cases} v_{max}^n(t) & \text{if } i_{arm}(t) \geq 0; \\ v_{min}^n(t) & \text{if } i_{arm}(t) < 0, \end{cases} \end{aligned} \quad (2)$$

where $\bar{P}_{max}^n$ represents the maximum active power of n SMs, v_{max}^n and v_{min}^n represent the maximum and minimum allowed output voltage of n SMs, respectively. Similarly, the minimum power of n SMs can be derived as:

$$\begin{aligned} \bar{P}_{min}^n &= \frac{1}{T} \int_{t_0}^{t_0+T} v_{min}^n(t) i_{arm}(t) dt, \\ v_{min}^n(t) &= \begin{cases} v_{min}^n(t), & i_{arm}(t) \geq 0; \\ v_{max}^n(t), & i_{arm}(t) < 0. \end{cases} \end{aligned} \quad (3)$$

The derivation of v_{max}^n and v_{min}^n is as below.

Fig. 3. Maximum and minimum output voltages of n SMs over a fundamental cycle: (a) Maximum output voltage (v_{max}^n), and (b) minimum output voltage (v_{min}^n).

The instantaneous output voltage of n SMs is represented as v_{SM}^n . Considering the capacitor voltages, it is derived

$$-nv_C \leq v_{SM}^n \leq nv_C, \quad (4)$$

where nv_C represents the capacitor voltage of the n SMs. However, (4) does not mean the maximum of v_{SM}^n is always nv_C and the minimum is always $-nv_C$, because the output voltages of all SMs in one arm should sum up to the arm voltage reference v_{arm}^* :

$$v_{SM}^n + v_{SM}^{N-n} = v_{arm}^*, \quad (5)$$

where v_{SM}^{N-n} represents the output voltage of the remaining $N-n$ SMs. Hence, v_{SM}^{N-n} should be within $[-(N-n)v_C, (N-n)v_C]$ and it can be derived:

$$v_{arm}^* - (N-n)v_C \leq v_{SM}^n \leq v_{arm}^* + (N-n)v_C. \quad (6)$$

Combining (4) and (6), it yields:

$$v_{max}^n(t) = \min[nv_C, v_{arm}^* + (N-n)v_C]. \quad (7)$$

$$v_{min}^n(t) = \max[-nv_C, v_{arm}^* - (N-n)v_C]. \quad (8)$$

Fig. 3(a) depicts the maximum v_{SM}^n in a fundamental period, which verifies (7). As observed, during the interval $[t_1, t_2]$, when nv_C is lower than $v_{arm}^* + (N-n)v_C$, the maximum v_{SM}^n is nv_C . Accordingly, the output voltage of the remaining $N-n$ SMs (v_{SM}^{N-n}) compensates for the arm voltage reference and hence is $v_{arm}^* - nv_C$. During the intervals $[t_0, t_1]$ and $[t_2, t_3]$, when nv_C is higher than $v_{arm}^* + (N-n)v_C$, v_{SM}^{N-n} is saturated at its minimum $-(N-n)v_C$. Hence, the maximum v_{SM}^n is $v_{arm}^* + (N-n)v_C$.

Similarly, Fig. 3(b) depicts the minimum v_{SM}^n in a fundamental period, which verifies (8). During the intervals $[t_0, t_1]$ and $[t_2, t_3]$, when $v_{arm}^* - (N-n)v_C$ is lower than $-nv_C$,

the minimum v_{SM}^n is $-nv_C$. Accordingly, the output voltage of the remaining $N-n$ SMs (v_{SM}^{N-n}) compensates for the arm voltage reference and hence is $v_{arm}^* + nv_C$. However, when $v_{arm}^* - (N-n)v_C$ is higher than $-nv_C$ in the interval $[t_1, t_2]$, v_{SM}^{N-n} is saturated at its maximum $(N-n)v_C$. Thus, the minimum v_{SM}^n is $v_{arm}^* - (N-n)v_C$.

B. Battery Fault Tolerance

If an MMC-based BESS can provide the required active power with faulty batteries in at maximum n_{max} SMs, the battery fault tolerance of this BESS, represented as F , can be assessed as:

$$F = \frac{n_{max}}{N} \times 100\%. \quad (9)$$

The derivation of n_{max} (and F) can be discussed in two conditions, viz. with a charging arm power ($\bar{P}_{arm} > 0$) and with a discharging arm power ($\bar{P}_{arm} < 0$), where $\bar{P}_{arm}$ represents the active power requirement of this arm.

In the condition of charging arm power, n_{max} is decided as:

$$n_{max} = n, \bar{P}_{max}^{N-n} \geq \bar{P}_{arm} \wedge \bar{P}_{max}^{N-n-1} < \bar{P}_{arm}. \quad (10)$$

The rationale behind this expression is as follows. Since n_{max} is defined as the maximum number of SMs with faulty batteries that the BESS can tolerate, the remaining $N-n_{max}$ SMs should be able to absorb the required arm power. Hence, the maximum power limit of the $N-n_{max}$ SMs should not be lower than the active power requirement of this arm, i.e. $\bar{P}_{max}^{N-n_{max}} \geq \bar{P}_{arm}$, which leads to the left part of (10). Meanwhile, if battery faults occur in $n_{max} + 1$ SMs, the remaining $N-n_{max} - 1$ SMs will fail to absorb the required arm power. Thus, the maximum power limit of the $N-n_{max} - 1$ SMs should be lower than the active power requirement of this arm, i.e. $\bar{P}_{max}^{N-n_{max}-1} < \bar{P}_{arm}$, which leads to the right part of (10).

In the condition of discharging arm power, n_{max} is decided as:

$$n_{max} = n, \bar{P}_{min}^{N-n} \leq \bar{P}_{arm} \wedge \bar{P}_{min}^{N-n-1} > \bar{P}_{arm}. \quad (11)$$

The rationale behind this expression is as follows. According to the definition of n_{max} , when battery faults occur in n_{max} SMs, the remaining $N-n_{max}$ SMs should be able to provide the required arm power. As mentioned before, the discharging power is denoted with a negative value. For example, a discharging power of 1 MW is denoted as -1 MW. Thus, if the minimum power limit of the remaining $N-n_{max}$ SMs is not higher than the required arm power, these SMs can provide the required arm power, which leads to the left part of (11), i.e. $\bar{P}_{min}^{N-n_{max}} \leq \bar{P}_{arm}$. Meanwhile, if battery faults occur in $n_{max} + 1$ SMs, the remaining $N-n_{max} - 1$ SMs will fail to provide the required arm power. Thus, the minimum power limit of the $N-n_{max} - 1$ SMs should be higher than the active power requirement of this arm, i.e. $\bar{P}_{min}^{N-n_{max}-1} > \bar{P}_{arm}$, which leads to the right part of (11).

Fig. 4. Battery fault tolerance (F) with (a) charging arm power ($\bar{P}_{arm} \geq 0$), and (b) discharging arm power ($\bar{P}_{arm} \leq 0$).

As an example, Figs. 4(a) and (b) depict how to assess the battery fault tolerance of an MMC-based BESS with charging and discharging arm powers, respectively. In these figures, full-bridge SMs are considered operating with unity power factor and the modulation index is 0.9. The power values are normalized to the absolute value of the arm power, i.e., $|\bar{P}_{arm}|$, while the number of SMs is normalized to the total number of SMs in this arm. According to Fig. 4(a), where $\bar{P}_{arm} \geq 0$, the SMs maximum power limit is higher than the arm power requirement (100%) when the number of SMs is not less than 36%. In other words, 36% of SMs with healthy batteries will be sufficient to absorb the arm power. Hence, the battery fault tolerance is 64%. Similarly, in Fig. 4(b), where $\bar{P}_{arm} \leq 0$, the SMs minimum power limit is lower than the arm power requirement (-100%) when the number of SMs is not less than 36%. Hence, the battery fault tolerance is 64%. The examples also indicate that the proposed analysis is applicable regardless of the amount of active power requirement and number of SMs, as normalized values are used in the analysis.

III. COMPARISON OF THE BATTERY FAULT TOLERANCE

This section investigates and compares the battery fault tolerance of the MMCs with half-bridge and full-bridge SMs under various operating conditions. The results are displayed in Fig. 5. As mentioned before, the provided results are applicable regardless of the number of SMs and the amount of active power requirement, which is related to the output voltage and current of the converter.

Fig. 5. Investigation results: (a) Battery fault tolerance of an MMC with half-bridge SMs, (b) battery fault tolerance of an MMC with full-bridge SMs, and (c) difference between the battery fault tolerance of the two systems.

Fig. 5(a) provides the battery fault tolerance (F) of an MMC-based BESS with half-bridge SMs under various operating conditions, where the modulation index (m_a) varies from 0.2 to 1 and the phase shift (φ) between the output voltage and current varies from 0 to 180°. Zero circulating currents are assumed in this investigation. Hence, when the phase shift is within $[0, 90^\circ]$, the BESS is discharged. When the phase shift is within $[90^\circ, 180^\circ]$, the BESS is charged. As observed, when the MMC operates with the maximum modulation index ($m_a = 1$) and unity power factor ($\varphi = 0/180^\circ$), the MMC-based BESS has the worst battery fault tolerance ($F = 15.5\%$). In other words, the MMC-based BESS cannot tolerate the battery faults in more than 15.5% of SMs per arm. As the modulation index decreases or the phase shift approaches 90°, which means the active power requirement decreases, the battery fault tolerance of the BESS improves. When the

TABLE I
PARAMETERS OF THE SYSTEMS

Parameter	Simulation	Experiment
Number of SMs per arm, N	5	4
Capacitor voltage reference, V_C	2.4 kV	25 V
Nominal output current (Peak), I_o	1 kA	15 A
Nominal output voltage (Peak), V_o	5.4 kV	100 V
Fundamental frequency, f	50 Hz	50 Hz

phase shift is exactly 90° , which means zero active power requirement, the battery fault tolerance reaches its maximum, 100%.

Fig. 5(b) provides the battery fault tolerance (F) of an MMC-based BESS with full-bridge SMs under the same scenarios. Similarly, the battery fault tolerance of the MMC-based BESS improves as the modulation index decreases or the phase shift approaches 90° . When the MMC operates with the maximum modulation index ($m_a = 1$) and the unity power factor ($\varphi = 0/180^\circ$), the MMC-based BESS has the worst battery fault tolerance ($F = 59.5\%$). In other words, the BESS with full-bridge SMs can tolerate the battery faults in more than half the SMs under all the operating conditions.

Fig. 5(c) displays the difference between the battery fault tolerance of the two MMCs. As observed, when the MMC operates with a large modulation index and near to the unity power factor, which means a large amount of active power requirement, the BESS with full-bridge SMs has a significantly higher tolerance of battery faults than the BESS with half-bridge SMs. For example, when $m_a = 1$ and $\varphi = 0$, the battery fault tolerance of the BESS with full-bridge SMs is higher by 44%. As active power is usually the dominant power component in the operation of BESSs, it can be concluded that MMC-based BESS with full-bridge SMs has a considerably higher tolerance to battery faults than the system with half-bridge SMs. This is because the operation of full-bridge SMs is more flexible as they can provide negative output voltages. The half-bridge SMs can be charged only when the current is positive and discharged only when the current is negative, as their output voltage is either zero or positive. However, the charging and discharging of full-bridge SMs do not rely on the current direction.

In this sense of battery fault tolerance, the full-bridge SM is a better candidate than the half-bridge SM for the MMC-based BESSs. For example, if an MMC is designed to have some SMs with battery integration and the rest SMs with renewable energy integration, the required number of SMs with battery integration will be much lower by using full-bridge SMs.

IV. SIMULATION RESULTS

To verify the proposed analysis, simulation results are obtained on two MMC-based BESSs, one constructed with half-bridge SMs and the other with full-bridge SMs. The parameters of the two BESSs are similar, as provided in Table

Fig. 6. Simulation results on half-bridge SMs: (a) Power references and measured active powers of the SMs, (b) SM capacitor voltages, and (c) arm voltage and converter output voltage.

I. Both converters are discharged with unity power factor, and zero circulating current reference is considered in the simulation.

A. Simulation Results on Half-Bridge SMs

When half-bridge SMs are used, the battery fault tolerance of the MMC-based BESS is 27.5%. As the simulated MMC has five SMs per arm, this BESS can only tolerate the battery fault in one SM. Simulation results are provided in Fig. 6.

In Fig. 6(a), $\bar{P}_{SMi}$ and $\bar{P}_{SMi}^*$ represent the measured active power and references of the i th SM, which are normalized to the absolute value of the total arm power. Waveforms of the fifth SM are omitted because they are similar to the waveforms of the fourth SM. In Fig. 6(b), v_{Ci} represents the capacitor voltage of the i th SM. In Fig. 6(c), v_{dc} represents the sum of capacitor voltages of five SMs, v_{arm}^* represents the arm voltage reference, and v_o is the output voltage of the MMC.

Fig. 7. Simulation results on full-bridge SMs: (a) Power references and measured active powers of the SMs, (b) SM capacitor voltages, and (c) arm voltage and converter output voltage.

Initially, the power reference is -20% for each SM, which means each of them is discharging with 20% of the arm power. As observed, each SM can track the corresponding power reference and the capacitor voltages are balanced.

At $t=0.1$ s, the batteries of the first SM are disconnected. Thus, the active power reference ($\bar{P}^*_{SM1}$) of this SM becomes zero, while the remaining four SMs are discharged to provide the total arm power. As observed, the SMs can still track the power references and the capacitor voltages are also balanced.

At $t=0.4$ s, the batteries of the second SM are also disconnected. Hence, the power reference of this SM also becomes zero, while the remaining three SMs are required to provide the total arm power. However, as mentioned before, this BESS can only tolerate battery faults in one SM. Therefore, the SMs cannot track the power references and the capacitor voltages

Fig. 8. Power references and measured average powers of the SMs in the experiments.

diverge. Because the first and second SMs are discharging without the integration of batteries, their capacitor voltages decrease continuously. Consequently, as indicated in Fig. 6(c), the summation of capacitor voltages of the SMs becomes lower than the arm voltage reference, and hence, the converter output voltage is distorted.

B. Simulation Results on Full-Bridge SMs

When full-bridge SMs are used, the battery fault tolerance of the MMC-based BESS is 64.0%. As the simulated MMC has five SMs per arm, this BESS can tolerate battery faults in three SMs, while the BESS with half-bridge SMs can only tolerate battery faults in one SM. The simulation results are provided in Fig. 7, with similar scenarios to that of the simulation on half-bridge SMs.

As observed from Fig. 7(a), the SMs can track their corresponding power references in all scenarios. The capacitor voltages in Fig. 7(b) are also stable and the output voltages in Fig. 7(c) are properly synthesized.

The simulation results are aligned with the conclusion of the comparison results in Section III, i.e., the BESS with full-bridge SMs has a higher tolerance to battery faults than the BESS with half-bridge SMs.

V. EXPERIMENTAL RESULTS

Experimental results are obtained on one arm of the MMC-based BESS with four full-bridge SMs. This arm is built by the series connection of four Imperix PEH 2015 full-bridge power modules. Two series-connected RS 537-5488 lead-acid batteries are directly connected to the dc-side of each SM. A resistor of 6.8Ω and an inductor of 5 mH are connected to the ac-side as a load. In this experimental condition, the battery fault tolerance of the arm at this operating point is 37.5%, which means this BESS can tolerate battery faults in one SM only.

Fig. 8 displays the measured average powers and references of the SMs in the experiments. Initially, all the power references are -25%, which means the total arm power

requirement is equally shared by the four SMs. The measured powers of all the SMs track the references. At $t = 2.4$ s, it is assumed that the batteries of the first SM are faulty and disconnected. Hence, its power reference ($\bar{P}_{SM1}^*$) becomes zero while the remaining 3 SMs are required to provide the total arm power. As observed, the SMs can track the power references, which verifies the system can operate normally even when one SM is disconnected from batteries.

At $t = 4.2$ s, it is assumed that the batteries of the second SM are also faulty and its power reference becomes zero, while the third and fourth SMs are required to provide the total arm power. However, as mentioned before, this BESS can only tolerate battery faults in one SM. As observed, the SMs cannot track their corresponding power references, which verifies the system cannot tolerate battery faults in more than one SMs.

VI. CONCLUSION

This paper has investigated and compared the battery fault tolerance of the MMC-based BESSs with half-bridge and full-bridge SMs. The results indicate that the MMC with full-bridge SMs has higher tolerance to battery faults, especially when the active power requirement is high. Thus, in applications that require high fault tolerance, full-bridge SMs are better candidates than half-bridge SMs. Simulation and experimental results have been provided to verify the effectiveness of the proposed analysis.

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