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Analysis, Design and Implementation of a Non-isolated Switched Inductor/Capacitor Converter with Low Voltage Spikes

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In order to take the advantage of boost capability and filtering characteristics of the switched inductor/capacitor, a non-isolated switched inductor/capacitor (NSI/C) converter is proposed. The topological structure of the non-isolated switched inductor/capacitor converter is analyzed in detail, and the DC steady-state model is established in continuous conduction mode (CCM). The voltage gain of the converter and the stress of the switch in the converter are theoretically deduced and compared with the existing converters; the parameter design of the inductance and capacitance is calculated. The simulation model was built in MATLAB/Simulink, and the correctness of the theoretical calculation for the proposed converter was verified by simulation results. Finally, the experimental prototypes of the proposed converter and the non-isolated high step-up (NHS) converter were built. Through the comparison of experimental results, the feasibility and validity of the design scheme for the proposed converter are verified. © 2021 Institute of Electrical Engineers of Japan. Published by Wiley Periodicals LLC.

Keywords: DC-DC converter; voltage gain; switched inductor; switched capacitor

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1. Introduction

In recent years, DC power supplies have been widely used in communications, computers, mobile phones, mobile devices, automotive lighting systems, photovoltaic power generation systems, and wind power generation systems due to their advantages of the output voltage not existing crossing-zero [1–3]. However, the voltage of the DC power supply is generally low. For example, the lead-acid battery of a hybrid electric vehicle produces voltage of 12 V, but the lighting system of an automobile needs 85 V to work properly, so a high-gain DC converter is required to boost the voltage [4]. The boosting principle of the DC converter is to use the energy storage characteristics of inductor or capacitor, by applying the Pulse Width Modulation (PWM) technique and changing switch frequency to achieve the purpose of increasing the output gain [5].

The DC converters can be divided into two types: isolated and non-isolated. The isolated converters include full bridge,

forward-flyback, high-frequency transformer, push pull, and half bridge converters. The isolated converter, whose input is AC and output is DC, uses transformer to separate input and output [6,7]. Due to the introduction of high-frequency transformer, the isolated converter is more convenient to boost voltage. High gain can be obtained by changing the duty ratio and switching frequency, or by changing the turn ratio of the transformer [8]. However, the introduction of high-frequency transformer causes the drawbacks of large switch stress, large volume, and heavy weight, as well as low efficiency due to the existence of transformer leakage inductance [9]. In order to overcome these problems, active clamp circuits and non-dissipative snubber circuits have been proposed, but they increase the cost of the converter, and the control process goes complicated [10]. On the contrary, non-isolated converters have the advantages of low switch stress, small size, and high efficiency. The non-isolated converters include the Buck, Boost, Buck-Boost [11], NHS [12], QZS [13], SL [14], SC [14], Ćuk [15] and Zeta [16] converters. The non-isolated converters comprise input and output common ground type and non-common ground type converters. The DC-DC converter is a bridge between low-voltage input and high-voltage output in application systems and is required to have the advantages of low switch stress and high efficiency. Some converters mentioned above, such as Buck and Buck-Boost converters, have step-down function; others, such as Boost, Buck-Boost, NHS, QZS, SL, SC, Ćuk and Zeta converters, have boost function. The traditional Boost converter achieves the purpose of boosting by changing the duty ratio and switching

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frequency. In theory, when the duty ratio of the Boost converter is infinitely close to 1, the voltage gain can be infinitely large, but in fact, the larger the duty ratio, the more obvious the influence of parasitic parameters of the device, and the lower the anti-electromagnetic interference ability. Through the introduction of switched inductor/capacitor structure, the output gain of SL and SC converters has been improved. However, the stress of the semiconductor device increases, and then the efficiency decreases. AH-SLC and SH-SLC converters can obtain ten times greater voltage gain by replacing the inductor with the switched inductor [17–19]. However, it is difficult for SL converter to realize so much voltage gain. But the gains of AH-SLC and SH-SLC converters are still not enough for some circumstances that require higher gain.

In order to realize high voltage gain, low voltage stress, and voltage ripple, a series of non-isolated high step-up DC-DC converters are proposed in reference 12; the voltage gain, switch stress, and topology of the series of non-isolated converters are analyzed and compared. Reference 12 focuses on the analysis of the non-isolated high step-up (NHS) converter. However, when the main switch of the converter is on, the charging time of C_2 by input voltage and capacitor C_1 is very short, resulting in a large voltage spike when the semiconductor devices are turned off, which is harmful to the load. The larger voltage spike is also the main reason for the low efficiency of the converter. In order to solve this problem, this paper proposes a non-isolated switched inductor/capacitor (NSI/C) converter. The proposed converter uses switched inductor/capacitor structure, which not only plays a boost function, but also buffers the input current, and alleviates the problem of voltage spikes effectively. Finally, two experimental prototypes were built: the proposed converter and the NHS converter. Through the comparison of experimental results, it is verified that the proposed converter has a higher voltage gain than the NHS converter and reduces the voltage spikes of semiconductor components.

2. The Proposed Converter

The NHS converter in reference 12 is shown in Fig. 1, and the proposed converter is shown in Fig. 2. Based on the NHS converter, the proposed converter has changed the topology of the NHS converter by adding capacitors C_3 , C_4 , and inductor L_3 , and its topological structure is shown in Fig. 2(a). In order to further raise the output gain of the NSI/C Type-1 converter, the NSI/C Type-1 converter topology is improved, and the NSI/C Type-2 converter is proposed and shown in Fig. 2(b).

The main waveform of NSI/C Type-2 converter is shown in Fig. 3; from top to bottom is: drive signal of PWM, the voltage of S_1 , the current flowing through L_1 – L_4 , the voltage of capacitors C_1 , C_2 , C_3 , C_5 , and C_4 , the voltage and current stress of D_0 .

According to Fig. 3, when the NSI/C Type-2 converter works in CCM, the proposed converter has two working modes, as shown in Fig. 4.

In Mode 1 $[t_0-t_1]$, the switch S_1 is turned on; diodes D_1 , D_3 , D_4 , and D_0 are turned off by the reverse voltage; the equivalent circuit is shown in Fig. 4(a). During this period the input voltage V_i and C_2 charge the inductor L_1 through S_1 ; V_i and the C_1 charge the L_2 ; the capacitor C_3 charges the inductor L_3 ; the capacitor C_5 charges the inductor L_4 and C_4 ; the capacitor C_0 charges the load. According to the Kirchhoff Voltage Law (KVL), the steady-state

Fig. 1. The topological structure of the NHS converter

(a)

(b)

Fig. 2. The topological structure of the proposed converter. (a) NSI/C Type-1. (b) NSI/C Type-2

Equation (1) can be obtained.

$$\begin{cases} -V_i + V_{L1} - V_{C2} = 0 \\ -V_i + V_{L2} - V_{C1} = 0 \\ -V_{C3} + V_{L3} = 0 \\ -V_{C5} + V_{L4} + V_{C4} = 0 \\ -V_{C0} + V_o = 0 \end{cases} \quad (1)$$

In Mode 2 $[t_1-t_2]$, the switch S_1 is turned off; D_2 is turned off; the equivalent circuit is shown in Fig. 4(b). During this period L_1 charges C_1 through D_1 ; L_2 charges C_2 through D_1 ; L_1 , L_2 , and V_i charge capacitor C_3 ; L_1 , L_2 , L_3 , and V_i charge capacitor C_5 ; L_1 , L_2 , L_3 , L_4 , and V_i charge the load. The steady-state Equation (2)

Fig. 3. The main waveform of the NSI/C Type-2 converter

is available:

$$\begin{cases} V_{L1} + V_{C1} = 0 \\ V_{L2} + V_{C2} = 0 \\ -V_i - V_{C1} - V_{C2} + V_{L3} + V_{C5} = 0 \\ V_{L4} + V_{C4} = 0 \\ -V_i - V_{C1} - V_{C2} + V_{L3} + V_{L4} + V_{C0} = 0 \\ -V_i - V_{C1} - V_{C2} + V_{C3} = 0 \end{cases} \quad (2)$$

According to the Volt-Second Balance of Inductor, Equation (3) can be obtained:

$$\begin{cases} V_{C1} = V_{C2} = \frac{D}{1-2D} V_i \\ V_{C3} = \frac{1}{1-2D} V_i \\ V_{C4} = \frac{D}{(1-D)(1-2D)} V_i \\ V_{C5} = \frac{1}{(1-D)(1-2D)} V_i \end{cases} \quad (3)$$

Therefore, the output voltage of the NSI/C Type-2 converter can be obtained:

$$V_0 = \frac{1+D}{(1-D)(1-2D)} V_i \quad (4)$$

3. Analysis of the Proposed Converter

3.1. Voltage gain According to Equation (4), the voltage gain of the NSI/C Type-2 converter can be obtained and shown in Equation (5), and for comparison, the gains of Boost, NHS, Buck-Boost converters, and the converter in reference [18] are as follows.

$$G = \frac{V_0}{V_i} = \frac{1+D}{(1-D)(1-2D)} V_i \quad (5)$$

The voltage gain of the NHS converter is given by [12]:

$$G = \frac{V_0}{V_i} = \frac{2-D}{(1-D)^2} \quad (6)$$

Fig. 4. The equivalent circuit of the NSI/C Type-2 converter. (a) Mode 1. (b) Mode 2

The voltage gain of the Boost converter is shown in Equation (7):

$$G = \frac{V_0}{V_i} = \frac{1}{1-D} \quad (7)$$

The voltage gain of the converter in reference [18] is shown in Equation (8):

$$G = \frac{V_0}{V_i} = \frac{1+D}{1-2D} \quad (8)$$

3.2. Voltage stress of the switch When S_1 is turned off, the voltage stress of S_1 in the NSI/C Type-2 converter is as follows:

$$V_{S1} = V_{C5} = \frac{1}{(1-D)(1-2D)} V_i \quad (9)$$

3.3. Voltage stress of the diodes When S_1 is turned on, the diodes D_1 , D_3 , D_4 , and D_0 are turned off, the voltage stresses of D_1 , D_3 , D_4 , and D_0 in the NSI/C Type-2 converter are obtained, respectively:

$$\begin{cases} V_{D1} = V_{D3} = \frac{1}{1-2D} V_i \\ V_{D4} = V_{D0} = \frac{1}{(1-D)(1-2D)} V_i \end{cases} \quad (10)$$

When D_2 is turned off, the voltage stress of D_2 in the NSI/C Type-2 converter is as follows:

$$V_{D2} = \frac{D}{(1-D)(1-2D)} V_i \quad (11)$$

The switch and diodes voltage stresses of other converters are shown in Table I.

Table I. Comparison between the proposed converter and other DC-DC converters

Reference converter	Converter configuration	Converter components	Voltage gain	Switch stress	Duty ratio limit	Remarks
Boost converter		Inductors-1 Capacitors-1 Diodes-1 Switch-1	$G = \frac{1}{1-D}$	$V_S = \frac{1}{1-D} V_i$ $I_{S1} = D I_{in}$	1	Common ground between the input and output of the converter Voltage gain improvement is not significant The structure is simple High voltage stress Common ground between the input and output of the converter
Quadratic Boost converter		Inductors-2 Capacitors-2 Diodes-3 Switch-1	$G = \frac{1}{(1-D)^2}$	$V_{S1} = \frac{1}{(1-D)^2} V_i$ $I_{S1} = D(2-D) I_{in}$	1	Common ground between the input and output of the converter The structure is simple High voltage stress Common ground between the input and output of the converter
NHS converter		Inductors-2 Capacitors-3 Diodes-4 Switch-1	$G = \frac{2-D}{(1-D)^2}$	$V_{S1} = \frac{1}{(1-D)^2} V_i$ $I_{S1} = \frac{1+D-D^2}{2-D} I_{in}$	1	Common ground between the input and output of the converter High switching and diode losses Poor efficiency
Quasi Z-source DC-DC converter		Inductors-2 Capacitors-3 Diodes-4 Switch-1	$G = \frac{1-D}{1-2D}$	$V_{S1} = \frac{1}{1-2D} V_i$ $I_{S1} = \frac{D}{1-D} I_{in}$	0.5	Common ground between the input and output of the converter Continuous input & Output current High voltage stress The voltage gain is not high enough Continuous input & Output current
Quasi Z-source DC-DC converter with switched capacitor [18]		Inductors-3 Capacitors-5 Diodes-3 Switch-1	$G = \frac{1+D}{1-2D}$	$V_{S1} = \frac{1}{1-2D} V_i$ $I_{S1} = \frac{3D}{1+D} I_{in}$	0.5	Common ground between the input and output of the converter Continuous input current High voltage gain At the same voltage gain, the switch stress is low
NSI/C Type-2 converter		Inductors-4 Capacitors-6 Diodes-5 Switch-1	$G = \frac{1+D}{(1-D)(1-2D)}$	$V_{S1} = \frac{1}{(1-D)(1-2D)} V_i$ $I_{S1} = \frac{2D(2-D)}{1+D} I_{in}$	0.5	Common ground between the input and output of the converter Continuous input current High voltage gain At the same voltage gain, the switch stress is low

3.4. Current stress of the components Based on the principle of Ampere-Second Balance of Capacitor, the average current flowing through the capacitor in one cycle is 0. According to Fig. 4, the currents flowing through capacitors C_1 , C_2 , C_3 , C_4 , C_5 , and C_0 are as follows:

$$\begin{cases} \int_0^{DT} (i_{L1_on} - i_{in_on})dt + \int_{DT}^T (i_{L1_off} - i_{in_off})dt = 0 \\ \int_0^{DT} (-i_{L1_on})dt + \int_{DT}^T (i_{L2_off} - i_{in_off})dt = 0 \\ \int_0^{DT} (-i_{L3_on})dt + \int_{DT}^T (i_{in_off} - i_{L3_off})dt = 0 \\ \int_0^{DT} (-2i_{L4_on})dt + \int_{DT}^T (i_{L3_off} - i_{L4_off})dt = 0 \\ \int_0^{DT} (i_{L4_on} - I_R)dt + \int_{DT}^T (i_{L4_off} - I_R)dt = 0 \end{cases} \quad (12)$$

In Equation (12), i_{L_on} , i_{L_off} , i_{in_on} , and i_{in_off} are the inductor currents and the input currents when the switch S_1 is on or off. When the switching frequency is high enough and inductor is large enough, the inductance under different modes meets the following requirements:

$$I_L = \frac{1}{DT} \int_0^{DT} i_{L_on} dt = \frac{1}{(1-D)T} \int_{DT}^T i_{L_off} dt \quad (13)$$

Substituting Equation (13) into (12), Equation (14) can be obtained:

$$\begin{cases} I_{L1} = I_{L2} = \frac{1+D}{(1-D)(1-2D)} I_0 \\ I_{L3} = \frac{1+D}{1-D} I_0 \\ I_{L4} = I_0 \end{cases} \quad (14)$$

When the switch S_1 is turned on, the current flowing through S_1 can be obtained:

$$i_{S1} = \frac{4-2D}{(1-D)(1-2D)} I_0 \quad (15)$$

When the switch S_1 is turned off, and diodes D_1 , D_3 , D_4 , and D_0 are turned on, the currents flowing through the diodes D_1 , D_3 , D_4 , and D_0 are shown in Equation (16), respectively:

$$\begin{cases} i_{D1} = \frac{1+D}{(1-D)^2(1-2D)} I_0 \\ i_{D3} = \frac{1+D}{(1-D)^2} I_0 \\ i_{D4} = \frac{1}{1-D} I_0 \\ i_{D0} = \frac{1}{1-D} I_0 \end{cases} \quad (16)$$

When D_2 is turned on, the current flowing through D_2 is:

$$i_{D2} = \frac{2(1+D)}{(1-D)(1-2D)} I_0 \quad (17)$$

Therefore, it can be deduced that the average current flowing through S_1 and diodes can be obtained:

$$\begin{cases} I_{S1} = \frac{2D(2-D)}{(1-D)(1-2D)} I_0 \\ I_{D1} = \frac{1+D}{(1-D)(1-2D)} I_0 \\ I_{D2} = \frac{2D(1+D)}{(1-D)(1-2D)} I_0 \\ I_{D3} = \frac{1+D}{1-D} I_0 \\ I_{D4} = I_{D0} = I_0 \end{cases} \quad (18)$$

4. Parameter Design for the NSI/C Type-2 Converter

The voltage and current stresses of each component have been calculated theoretically in Section 3. The parameter design of the proposed converter will be discussed in this section.

4.1. Parameter design for the inductors When the switch S_1 is off or on, the inductance satisfies the differential Equation (19):

$$L = \frac{v_L dt}{di_L} \quad (19)$$

where di_L is the inductor current ripple when S_1 is on or off. If the ripple range of the inductor current is limited to $x\%$, then di_L can be expressed in Equation (20):

$$\Delta i_L = di_L = \frac{v_L dt}{L} = x_L \% I_L \quad (20)$$

Then, from Fig. 4, Equations (1), (2), and (20), Equation (21) can be obtained:

$$\begin{cases} L_1 = \frac{(1-D)T \cdot V_{C1}}{x_{L1} \% I_{L1}} \\ L_2 = \frac{(1-D)T \cdot V_{C2}}{x_{L2} \% I_{L2}} \\ L_3 = \frac{DT \cdot V_{C3}}{x_{L3} \% I_{L3}} \\ L_4 = \frac{(1-D)T \cdot V_{C4}}{x_{L4} \% I_{L4}} \end{cases} \quad (21)$$

Substituting (3) and (14) into (21), the inductance L_1 , L_2 , L_3 , and L_4 should satisfy the following equations:

$$\begin{cases} L_{1 \min} \geq \frac{D(1-2D)(1-D)^3 R_L}{(1+D)^2 x_{L1} \% f_s} \\ L_{2 \min} \geq \frac{D(1-2D)(1-D)^3 R_L}{(1+D)^2 x_{L2} \% f_s} \\ L_{3 \min} \geq \frac{D(1-D)^2 R_L}{(1+D)^2 x_{L3} \% f_s} \\ L_{4 \min} \geq \frac{D(1-D) R_L}{(1+D) x_{L4} \% f_s} \end{cases} \quad (22)$$

4.2. Parameter design for the capacitors Capacitor has the function of storing energy and filtering in the converter. Through periodic charging and discharging processes, high gain can be achieved. In actual working circumstances, the size of capacitors needs to be considered because it affects the volume of the converter.

The differential equation of the capacitor satisfies (23):

$$C = \frac{i_{C_on} dt}{dv_C} \quad (23)$$

where dv_C is the capacitor voltage ripple when S_1 is off or on, i_{C_on} is capacitor current when S_1 is on; If the ripple range of the capacitor voltage is limited to $x_C\%$, then, dv_C can be expressed in (24):

$$\Delta v_C = dv_C = \frac{i_{C_on} dt}{C} = x_C \% V_C \quad (24)$$

Then, from Fig. 4, (12), (23), and (24), (25) can be obtained:

$$\begin{cases} C_1 = \frac{(1+D)I_0}{(1-D)V_i x_C \% f_s} \\ C_2 = \frac{(1+D)I_0}{(1-D)V_i x_C \% f_s} \\ C_3 = \frac{D(1-2D)(1+D)I_0}{(1-D)V_i x_C \% f_s} \\ C_4 = \frac{(1-D)(1-2D)I_0}{V_i x_C \% f_s} \\ C_5 = \frac{D(1-D)(1-2D)I_0}{V_i x_C \% f_s} \end{cases} \quad (25)$$

Equation (25) is a parameter design criterion for capacitors. The capacitance is inversely proportional to the switching frequency.

When the switch S_1 is turned on, the current flowing through the output filter capacitor C_0 is I_0 . The differential equation is expressed in (26):

$$C_0 = \frac{I_0 dt}{x_C \% V_0} \quad (26)$$

In (26), $dt = DT$. Equation (4) is substituted into (26), and the following results can be obtained:

$$C_0 = \frac{D(1-D)(1-2D)I_0}{(1+D)V_i x_C \% f_s} \quad (27)$$

5. Loss Analysis and Efficiency Calculation

In this section, the power losses of switch, diodes, inductors, and capacitors are calculated in detail, and the efficiency of the proposed converter is derived.

5.1. Power losses of switch Switch losses include switching loss and conduction loss. The switch losses can be described in (28):

$$P_S = P_{S_w} + P_{r_s} = P_{S_w} + r_s I_{S(rms)}^2 \quad (28)$$

where P_S , P_{r_s} , and P_{S_w} represent the total losses of the switch, switch conduction loss, and switching loss, respectively. The switching loss can be described in (29):

$$P_{S_w} = \frac{1}{2} V_{S_on} i_{S_on} (t_r + t_f) \cdot f_s = \frac{(2-D)(t_r + t_f) f_s V_i V_0}{(1-D)^2 (1-2D)^2 R_L} \quad (29)$$

where t_r is the turn-on delay time, and t_f is the turn-off delay time.

$I_{S(rms)}$ is the effective current passing through the switch when the proposed converter switch is turned on. The effective current can be described in (30):

$$I_{S(rms)} = \sqrt{\frac{1}{T} \left(\int_0^{DT} i(t)^2 dt + \int_{DT}^T i(t)^2 dt \right)} = \frac{2(2-D)\sqrt{D}}{(1-D)(1-2D)} \frac{V_0}{R_L} \quad (30)$$

Switch conduction loss is expressed in (31):

$$P_{r_s} = \frac{4D(2-D)^2}{(1-D)^2 (1-2D)^2} \frac{V_0^2}{R_L^2} r_s \quad (31)$$

5.2. Power losses of diodes Diodes conduction losses are expressed in (32):

$$P_{VF} = V_F \sum_{i=0}^4 I_{Di} = \frac{4(D^2 - D + 1)}{(1-D)(1-2D)} \frac{V_0}{R_L} V_F \quad (32)$$

where V_F is forward voltage, and I_{Di} is average current flowing the diode.

5.3. Power losses of inductors The effective currents passing through the inductors can be obtained in (33):

$$\begin{cases} I_{L1(rms)} = I_{L2(rms)} = \frac{1+D}{(1-D)(1-2D)} \frac{V_0}{R_L} \\ I_{L3(rms)} = \frac{1+D}{1-D} \frac{V_0}{R_L} \\ I_{L4(rms)} = \frac{V_0}{R_L} \end{cases} \quad (33)$$

Fig. 5. Voltage gain of the converters

Fig. 6. The voltage stress of switch

Inductors conduction losses are expressed in (34).

$$P_{r_L} = r_{L1} I_{L1(rms)}^2 + r_{L2} I_{L2(rms)}^2 + r_{L3} I_{L3(rms)}^2 + r_{L4} I_{L4(rms)}^2 \quad (34)$$

where, r_{L1} , r_{L2} , r_{L3} , and r_{L4} are the internal resistances of the inductors L_1 , L_2 , L_3 , and L_4 , respectively.

5.4. Power losses of capacitors Capacitors conduction losses are expressed in (35):

$$P_{r_C} = \sum_{k=0}^6 r_{Ck} \cdot I_{Ck(rms)}^2 \quad (35)$$

where r_{Ck} and $I_{Ck(rms)}$ are the internal resistances and the effective currents of the capacitors, respectively. The effective currents can be expressed in (36):

$$\begin{cases} I_{C1(rms)} = I_{C2(rms)} = \frac{\sqrt{D}(1+D)}{(1-D)^{3/2}(1-2D)} \frac{V_0}{R_L} \\ I_{C3(rms)} = I_{C4(rms)} = I_{C5(rms)} = I_{C0(rms)} = \frac{V_0}{R_L} \end{cases} \quad (36)$$

Fig. 7. The current stress of switch

Table II. The parameters of the components

Components	Parameters
V_i (input voltage)	5 V
f_s (switching frequency)	50 kHz
L_1, L_2 (inductors)	47 μ H, $r_L = 5$ m Ω
L_3, L_4 (inductors)	0.47 mH, $r_L = 10$ m Ω
C_1, C_2 (capacitors)	100 μ F, $r_C = 15$ m Ω
C_3 (capacitor)	10 μ F, $r_C = 10$ m Ω
C_4, C_5 (capacitors)	4.7 μ F, $r_C = 5$ m Ω
S_1 (MOSFET)	IRFB4229PBF, $r_S = 12$ m Ω , $t_r = 31$ ns, $t_f = 21$ ns
D_1, D_2, D_3, D_4, D_0 (diodes)	MBR30100CT, $V_F = 0.7$ V
C_0 (capacitor)	100 μ F/450 V, $r_C = 15$ m Ω
R_L (load)	100 Ω

Therefore, capacitors conduction losses are expressed in (37).

$$P_{rC} = r_{C1}I^2_{C1(rms)} + r_{C2}I^2_{C2(rms)} + r_{C3}I^2_{C3(rms)} + r_{C4}I^2_{C4(rms)} + r_{C5}I^2_{C5(rms)} + r_{C0}I^2_{C0(rms)} \quad (37)$$

Based on (28)–(37), the total power losses can be expressed in (38):

$$P_{losses} = P_{Sw} + P_{rS} + P_{VF} + P_{rL} + P_{rC} \quad (38)$$

Therefore, the efficiency of the NSI/C Type-2 converter can be derived and expressed in (39):

$$\eta = \frac{P_0}{P_{in}} = \frac{P_0}{P_0 + P_{losses}} = \frac{1}{1 + P_{losses}/P_0} \quad (39)$$

This efficiency calculation method is also suitable for other converters.

6. Comparison with Other DC-DC Converters

Based on the similarity of the converter topology and the operation principle of the converter, traditional Boost, Quadratic Boost, Quasi Z-source DC-DC converter, NHS, and Quasi Z-source DC-DC converter with switched capacitor are selected for performance comparison analysis to verify the advantages

Fig. 8. The experimental prototypes of the NSI/C Type-2 and NHS converters

 Fig. 9. The experimental waveforms. (a) Output voltage of the NSI/C Type-2 converter. (b) Output voltage of the NHS converter. (c) Switch voltage stress of the NSI/C Type-2 converter. (d) Switch voltage stress of the NHS converter. (e) D_0 voltage stress of NSI/C Type-2 converter. (f) D_0 voltage stress of the NHS converter. (g) C_1 voltage stress of the NSI/C Type-2 converter. (h) C_5 voltage stress of the NSI/C Type-2 converter

of the NSI/C Type-2 converter; the converter configuration, converter components, voltage gain, switch stress, duty ratio limit, advantages and disadvantages are also shown in Table I.

According to Table I, the performance curve of the NSI/C Type-2 converter and other DC-DC converters are drawn in Figs 5–7.

6.1. Comparison of the output voltage The output voltage gain of the proposed NSI/C Type-2 converter is plotted in Fig. 5 as a function of the duty ratio D .

Compared with traditional Boost, Quadratic Boost, Quasi Z-source DC-DC converter, NHS, Buck-Boost converters, and the converter in reference [18], it can be seen from Fig. 5 that the voltage gain of the NSI/C Type-2 converter is higher than that of other DC-DC converters.

6.2. Comparison of stress Figure 6 shows the switch voltage stress of different converters under the same voltage gain. It can be seen from Fig. 6 that the switch voltage stress of the Buck-Boost, Boost, and Quasi Z-source DC-DC converters are higher than that of the proposed converter. When the voltage gain is greater than 9, the switch voltage stress of the NHS converter is higher than that of the proposed converter.

As shown in Fig. 7, the proposed converter has the same current stress as Boost converters and the converter in reference [18] under the same voltage gain. It can be seen from Fig. 7 that the switch current stress of the Buck-Boost converter is significantly higher than that of other converters.

7. Experimental Results

In order to verify the boost capability of the proposed converter, an experimental prototype was built. The component parameters are shown in Table II.

The experimental prototype of the NSI/C Type-2 converter is shown in Fig. 8, including the basic NSI/C Type-2 converter circuit, PWM (using 555 timer to generate switching pulse signal and lift voltage through KD501), the output filter capacitor, and the load. Moreover, an experimental prototype of the NHS converter was built to compare with the proposed converter.

Figure 9(a) shows the output voltage of the proposed converter when $V_i = 5$ V and $D = 0.38$, the output voltage $V_o = 43$ V; Label 2 (green line) is the input voltage and Label 4 (pink line) is the output voltage. Figure 9(b) shows the output voltage of the NHS converter, and under the same input and duty ratio as the NSI/C Type-2 converter, the output voltage $V_o = 19$ V. Figure 9(c) and (d) are the switch voltage stress of the proposed converter and the NHS converter at the same output voltage; Label 1 (yellow line) represents the PWM switching signal; Label 3 (blue line) represents the voltage stress of the switch. A comparison between Fig. 9(c) and (d) indicates that the proposed converter eliminates the voltage spikes of the switch, and the voltage stress of the switch is lower than that of the NHS converter. Figure 9(e) and (f) are the voltage stress of D_0 when the NSI/C Type-2 converter and the NHS converter have the same output voltage. Figure 9(g) and (h) are the voltages of the capacitors C_1 and C_5 of the proposed converter, which are 7.2 V, 30 V, respectively, consistent with (3).

Substitute the design parameters of Table II and the output voltage obtained from experiments into the (29), (31), (32), (34), and (37), then the power losses of switch, diodes, inductors, and capacitors can be obtained, respectively. Therefore, when the

Fig. 10. The proportion of different losses

Fig. 11. Comparison between the experimental and the theoretical efficiencies

output power is 65 W, the power losses of each component are shown in Fig. 10. Among them, the power losses of the diodes are the largest. Therefore, how to reduce the power losses of the diodes is particularly important to improve the converter efficiency.

The conversion efficiency of the experimental and the theoretical of the NSI/C Type-2 converter under the condition of duty ratio $D = 0.1-0.45$, $R_L = 100 \Omega$ are compared and shown in Fig. 11. In addition, the actual conversion efficiency of the NHS converter under the same input conditions is also shown in Fig. 11. It can be seen from Fig. 11 that when $D = 0.3$, the conversion efficiency of the proposed converter is significantly higher than that of the converter in other cases, and the conversion efficiency of the NSI/C Type-2 converter is significantly higher than that of the NHS converter. In fact, the experimental efficiency is lower than the theoretical efficiency, because the loss caused by the components at work is greater than the theoretical loss.

8. Conclusion

In photovoltaic power generation systems, fuel cell systems, and hybrid electric vehicle power systems, in order to solve the problem of the low voltage of the DC power supply, scholars have proposed many converters, which can be divided into

isolated converters and non-isolated converters according to their structures. The converters also have input and output common ground type and non-common ground type, and selection is made according to the actual working circumstances. In order to improve the voltage gain, reduce switch stress and voltage spikes of semiconductor devices, a non-isolated switched inductor/capacitor (NSI/C) converter is proposed.

In this paper, the topology, DC steady-state model, voltage gain, and switch stress of the NSI/C Type-2 converter are theoretically calculated. The parameter design of the converter is deduced. The NSI/C converter utilizes the high boosting capability and filtering characteristics of the switched inductor/capacitor structure, which effectively reduces the input current ripple and the voltage spikes of semiconductor devices and improves the efficiency of the converter. Finally, two experimental prototypes were built: one for NSI/C Type-2 converter and the other one for NHS converter. By comparison, the proposed converter has a higher voltage gain. Under the same voltage output, the switch voltage stress of the proposed converter is lower than that of the NHS converter, and the voltage spikes of the semiconductor device is reduced.

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