System design and characterisation of integrated liquid cooling solutions for 3D-stacked modules

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**System Design and Characterisation of Integrated Liquid
Cooling Solutions for 3D-Stacked Modules**

Submitted by

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ABSTRACT

Heat densities for electronic packages are increasing as the demand for many functionalities on a single package had resulted in single chip modules being stacked vertically to increase the amount of transistors that can be put on a given footprint. In this study, a liquid cooling solution is proposed to remove the heat from a stacked package with two modules each dissipating 100 W/cm^2 .

A first order estimate of the thermal resistance using thermal network modeling showed that the resistance across the solderjoints (interconnects) and the microchannel heat sink are of equal magnitude and hence focus is placed on minimising these two resistances. In a closed loop system design, when an external heat exchanger is included, the thermal resistance across it also becomes critical. A compact modeling approach is used to replace the interconnect layer with an effective material conductivity obtained from detailed modelling of a solderball considering the spreading/constriction effects. For the microchannel heat sink, a dual inlet/outlet configuration had been shown to have significant advantages over a single inlet/outlet. Flow distribution in the microchannel heat sink had been demonstrated to have a significant impact on its thermal performance. Plenum designs are used to influence the flow distribution within the microchannels to achieve lower temperature gradients and better thermal performance. The thermal performance of the carrier with a dual inlet/outlet with a reducing plenum had been shown numerically to have a thermal resistance of $0.15 \text{ }^\circ\text{C/W}$ at the design flowrate of 230 ml/min . Temperature variation on the die is also less than 7°C . The pressure drop from inlet to outlet is also relatively low at 326.3 mbar .

A system approach methodology is used to design the optimum liquid cooling solution. The liquid cooling solution integrated with the stacked 3D flip-chip package had been demonstrated experimentally. Hydraulic characterisation was performed and experimental pressure drop was found to be generally lower than

predicted. The total thermal resistance of a 3D module had been determined to be 0.57 °C/W. The carrier accounts for 65% of the total thermal resistance. The thermal performance of the carrier had been shown to be equivalent to studies done in this area. Moreover, the current work demonstrated that the integration of electrical and fluidic interconnects is possible within the same package area through the use of the solder sealing ring. Deviations from the design due to process limitations had been accounted for and will be the subject of further investigations.

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LIST OF SYMBOLS

Package terminology

BGA	Ball Grid Array
FC	Flip Chip
fcCSP	flipchip Chip Scale Package
I/O	Input/Output
MQFP	Metric Quad Flat Package
MCM	Multi Chip Module
PBGA	Plastic Ball Grid Array
PCB	Printed Circuit Board
QFP	Quad Flat Package
SCP	Single Chip Package
TIM	Thermal Interface Material
TSV	Through Silicon Via

Symbols

a	Equivalent source radius, m
b	Equivalent sink radius, m
Bi	Biot number, $Bi = hL/k_s$, dimensionless
C	Heat capacity, m C _p , W/K
D _h	Hydraulic diameter, m
f	Fanning friction factor, $\Delta p D_h / (2L\rho V^2)$, dimensionless
f _{app}	Apparent Fanning friction factor, dimensionless
H	Height of offset strip fins, m
h	Heat transfer coefficient, W/m ² .K or Reflow height of solderballs, m
K(∞)	Incremental pressure drop number for fully developed flow, dimensionless
k	Thermal conductivity, W/m.K

L	Length of offset strip fins in flow direction, m
LMTD	Logarithmic Mean Temperature Difference, °C
NTU	Number of Transfer Units, UA/C_{min} , dimensionless
Nu	Nusselt number, hD_h/k_f , dimensionless
OSF	Offset strip fins
P	Wetted Perimeter of microchannel, m
Pr	Prandtl number, $\mu C_p/k_f$, dimensionless
Po	Poiseuille number fRe , dimensionless
R	Thermal Resistance, $\Delta T/Q$, °C/W
Re	Reynolds number, $\rho U_m D_h/\mu$, dimensionless
S	Spacing between offset strip fins m
t	Thickness of offset strip fins or thickness of sink, m
UA	Overall conductance, W/K
U	Velocity in microchannels
x	Axial coordinate in flow direction, m
x^+	Normalised axial coordinate, $x / D_h Re Pr$, dimensionless

Subscripts

avg	Average
con	Constriction
conv	Convection
ca	Case-ambient
eff	Effective
f	Fluid
hy	Hydrodynamic
in	Inlet
ja	Junction-ambient
jc	Junction-case
m	Mean
mat	Material

min	Minimum
sp	Spreading
s	Solid
th	Thermal

Greek

ε	Relative size ratio of source radius to sink radius a/b or effectiveness of heat exchanger, dimensionless
μ	Dynamic viscosity of fluid, Pa.s
ρ	Density of fluid, kg/m ³
τ	Ratio of sink thickness to sink radius, t/b , dimensionless

1 INTRODUCTION

1.1 Background

Technology has improved our way of life from simple chores to high level applications. This advancement is achieved through the use of sophisticated appliances that employ complicated electronics circuits. The changeover to CMOS technology from bipolar transistors reduced the power consumption. However, as the scales of integration are getting larger, power dissipation over the die area is increasing.

Figure 1-1 Transistors count for different integration scales

The demand for faster clock speed over the years (**Fig. 1-1**) had increased the number of transistors on die from 2000 transistors in the 1940s to about 820 million in the 2007. The input/output (I/O) requirements are typically representative of the type of application. A hand calculator having transistor counts of 400 to 4500 requires about 48 I/Os and a supercomputer more than 10,000. This requirement for large I/O count had changed the way packages are designed, particularly in the way the signals are interfacing with the environment

outside of the die. For low I/O count, packages such as quad flat packages (QFP) are used. The leadframes are commonly found on the periphery of the package. For higher I/Os count, array packages are needed. Packages such as ball grid array (BGA) and flip chip (FC) array are used, and the I/O counts are determined by the pitch and die size of the package. The package structures are shown in Fig 1-2 with their cross sections.

The trend in the electronics industry is towards package miniaturization, due to the consumers' demands for smaller, lightweight and portable appliances. As a result, the increasing power dissipation is occurring across a smaller die area, and the heat density is increased significantly. As an example, to achieve an I/Os count of 64, the MQFP requires a package size of 14 mm by 14 mm and for the fcCSP only a 5 mm by 5 mm package size with 0.5 mm pitch, with an area reduction of about 85%.

Source: <http://www.amkor.com/go/packaging>

Figure 1-2 Cross Sectional View of typical packages used (a) Metric Quad Flat Package (b) Plastic Ball Grid Array (c) flip chip Chip Scale Packaging

Single chip packages (SCP), such as those described above perform single task such as processing, memory or storage. On top of being able to handle these

tasks efficiently, the multi-functionality of a package is also desired from consumer electronics as it reduced the need for different packages performing different functions. The ability to process, retain and store information on a single package is hence vital to system designers of electronic systems as more value added activities can be added. This introduces the concept of Multi-Chip-Modules (MCM) where the SCPs are distributed on a horizontal plane of the substrate. The smaller package sizes from SCP allow a variety of functionalities to be added on and this generally generates a non-uniform power map on the substrate. The horizontal distribution of packages though enhancing the capability of the package faces one very important constraint, which is the “real estate” that is available due to package miniaturisation.

Source: <http://www.amkor.com/go/packaging>

Figure 1-3 Cross Sectional View of a MCM PBGA package

In order to be able to keep up with the integration scales and the miniaturisation trend, the use of stacked packages that exploits the space above the substrate is used. Stacked packages, also known as System-in-Package (SiP) are becoming the packaging choice as many stacks can be placed on top of the other. This has the benefits of the MCM with the footprint of a SCP. However, the heat density of these stacked packages is very high as compared to the SCP due to the increased heat load over the same footprint. Apart from the increased functionalities on a smaller footprint, stacked packages are attractive from the

process point of view. Many processes can be integrated together to manufacture the package hence reducing cost. The assembly and testing process can also be reduced due to testing of two dies simultaneously reducing the cost. Potential applications for stacked packages are in high performance portable military electronics system where the need to integrate logic and memory functions within a small footprint is desired.

In order to evaluate the thermal performance of the package, the structure of the package is described in details. Referring to Fig 2, a package typically consists of a die (chip) where the circuitry design is imprinted. In order to communicate with the external world, the die makes use of interconnects to send and receive signals. Two different types of interconnects can be used, and they are wirebonds and flip chip. Die attach is used as a thermal interface material to join the die to the substrate. For flip chip, the solderballs are placed on copper pads. An underfill material, typically epoxy based resin is used. The whole package is then encapsulated to protect the die from external environment, such as shock, vibration and moisture. Copper metallization within the die and substrate allow the signals to be sent and received from the die. In stacked packages, the substrate is also known as the carrier. The package is then placed on a PCB through larger solderballs or leadframes that extend from the sides of the package.

In a package, different materials with vastly different material properties are used. This is a result of the requirements of the package where the materials are required to be at the extremes of their scales. Material properties such as electrical permittivity, electrical conductivity and thermal conductivity are common properties needed for insulation or conduction. Referring to Fig 2(b) of the PBGA, the die is made of silicon and a die attach made of epoxy resin is placed on the rigid laminate/BT substrate. Gold wirebonds are used as interconnects with the copper metallization within the substrate creating vias. The whole package is encapsulated in a mould compound of epoxy resin.

Solderballs of tin-lead composition are placed beneath the substrate to be placed on board. The different materials inside have different thermal conductivities and coefficients of thermal expansion. Hence, this influences the temperature distribution within the package and subsequently the thermo-mechanical stresses.

ITRS Power dissipation trends

Figure 1-4 ITRS Power Roadmap

The 2005 ITRS power roadmap suggested that by the year 2020, the power dissipation of the package is expected to rise up to 200 W for high performance packages (**Fig. 1-4**). With this increasing amount of heat density to handle and the exponential nature of component failures with temperature, thermal management plays a very important role for a package to last its desired working lifespan. Hence, it is desired to understand the way this heat is rejected to the ambient by looking at the thermal resistances along the package. To characterise the package, a resistance R_{ja} , which defined the resistance from junction to ambient, is used (**Fig. 1-5**). This resistance is a sum of two resistances (R_{jc} and R_{ca}) along the heat path. Firstly, the heat is transferred from the junction to the case. The resistance (R_{jc}) along this path is mainly within the package, and is largely conduction losses, due to material and spreading effects. The second

resistance (R_{ca}) is from the case to ambient. The resistance is related to the environment external to the package and is convective in nature. In thermal management of electronic packages, the goal is to minimise these resistances in order to have a lower junction temperature and higher power dissipation.

Figure 1-5 Heat path in a package with the red arrows showing the R_{jc} and blue arrow showing R_{ca}

The conventional method of removing heat from these packages is through a heat sink attached on top of the package to increase the heat transfer area. This is used to minimise the R_{ca} of the package. A fan is also mounted on top to increase the average velocity of the air to increase h (**Fig. 1-6**). R_{ca} can be minimised further by running the fan at higher speed to keep up with the increasing heat load subject to acoustic limits. In a study by Saini and Webb [2002] to maximise the heat dissipation from a heat sink and fan assembly, the maximum power that can be dissipated over a 80 mm by 60 mm base area footprint (maximum allowable area in chassis) is estimated to be 86.7 W. Running the fan speed higher by 25% increases the power dissipation to 95 W but acoustic limits are well over the recommended limit of 32dBa. Hence, alternative methods to enhance the heat transfer, such as by liquid cooling are needed in order to have high heat dissipation with acceptable junction temperature. Typical maximum operating junction temperature of electronic devices is 85°C for electronics to operate

reliably. The use of liquid as a coolant instead of air is due to the higher heat transfer coefficient obtainable because of its superior thermophysical properties such as dynamic viscosity μ , specific heat capacity C_p and thermal conductivity k . The Prandtl number $Pr = \mu C_p / k$ of water compared to air is of an order of magnitude larger ($Pr_{\text{water}} = 5.28$ and $Pr_{\text{air}} = 0.7$ at 25°C). Pr is the ratio of the kinematic viscosity and thermal diffusivity and compares the rate of growth of the velocity and thermal boundary layers. The higher Pr of water results in longer thermal developing length, increasing the average heat transfer coefficient over the surface. Hence, the surface area needed for heat transfer will be greatly reduced which is desirable for product miniaturisation. However, the dielectric properties of the liquids determine its uses in direct/non-direct contact applications, with the non-direct contact usage requiring an interface to prevent spillage and introduce an additional resistance. The use of liquid cooling also requires a pumping loop to circulate the coolant around the loop, which complicates the design of the package. When the components are assembled together to form a cooling solution, it often fails to anticipate other effects, which are present because one component may not be able to fulfill the requirements of others. Hence, it is desirable to incorporate the design of heat transfer enhancement features and component selection in a single design process.

Source: <http://www.pacificgeek.com/product.asp?id=45681>

Figure 1-6 Air cooled heat sink with fan mounted on top

The ability to predict the temperature in the package is very critical to package designers because material properties used in packaging are temperature dependent. The stress related failures are thermo-mechanical failures, which result if there is a coefficient of thermal expansion mismatch. The mismatch is given as the difference between the thermal coefficients of expansion of the sandwiched materials, and the resulting displacement is just a product of the mismatch with the temperature across. This can cause delamination of the die from the attached surface. A degradation of mechanical properties such as yield strength across the solderballs can occur at elevated temperatures if the design yield strength used did not include thermal effects, thus causing failures at the solderjoints. For the polymers used in packaging, as the temperature is increased, it will be closer to the glass transition temperature and hence, there will be an abrupt change in properties from glassy to rubbery state. This can happen in the underfill material that is used to absorb the coefficient of thermal expansion mismatch as its properties changed.

1.2 Motivation

Thermal management in 3D stacked modules is very challenging. As the number of stacks is increased, cooling the intermediate stacks posed a serious problem as the heat load cannot be transferred to the printed circuit board or heat sink without passing through the top and bottommost stack. This limits the type of functionalities that can be incorporated within the package as the average temperature is increased. Hence, the need to design intermediate cooling layers with heat transfer features within the stacked module is very critical.

In recent years, the use of using microchannels had gained prominence in the cooling of electronics. Channels having small hydraulic diameters (D_h) are etched onto the inactive side of the chip and run parallel in the streamwise direction. The enhancement achieved with the use of microchannels is due to the convective process involved which can be described by the heat transfer

coefficient, h . A dimensionless parameter, Nusselt number (Nu) is used to characterise this mode of heat transfer. For a rectangular microchannel having channel width a and height b , the Nu and hydraulic diameter D_h can be expressed as in equation (1.1) and (1.2)

$$Nu = \frac{hD_h}{k_f} \quad [1.1]$$

$$D_h = \frac{4A_c}{P} = \frac{4ab}{2(a+b)} = \frac{2ab}{a+b} \quad [1.2]$$

where k_f is the thermal conductivity of the fluid. Hence, for a constant Nu , a small D_h will mean that the h values associated with microchannels are very large. This provides the basic ideas for the design of cooling solutions. However, this enhancement comes with a penalty of having a large pressure drop across the length. This would have a great impact on the pumping requirements. Although flow is generally restricted to the laminar regime, the relationship between pressure drop and D_h will have to be carefully considered when implementing such schemes.

The heat transfer and flow in a microchannel heat sink can be analysed by using heat exchanger theory. Macro scale laws are scaled down to compare theoretical and experimental results to evaluate microchannel heat sink performance. A review of experimental results had been presented by Morini [2004]. Many studies had been performed on the fundamentals of heat transfer and fluid mechanics but the application of such studies on a system level requires understanding the interaction between the various components within the integrated thermal solution. This means identifying the dominant resistance to minimise those present along the heat path.

1.3 Objectives

The objectives of this project are two-fold.

Firstly, it is desired to design a closed loop liquid-cooled system that optimises

the heat dissipation from a stacked package structure, i.e. it takes up a minimum amount of space in the package, but allows the heat to be transferred from the die to the liquid with the smallest temperature differential.

Secondly, the cooling solution must be able to be integrated with the package using process technology commensurate with industry practice. The test vehicle must also include sensors that enable the hydraulic and thermal performance of the cooling system to be characterized.

1.4 Scope of work

With the above objectives, thermal solutions for a 3D stacked module consisting of two single chip packages with an interposer in between are investigated. The interposer consists of through silicon vias (TSV) and openings for electrical and fluidic interconnections. In particular, a cooling solution based on single-phase liquid flow in a microchannel array with the use of a micro pump and an external heat exchanger unit is to be designed and implemented. Heat removal from the die to ambient is realised through features to be processed on carriers found within the stacked package, making use of current semi-conductor process technology. All the cooling system components will be integrated into the stacked package.

The scope of work involved in this project includes:-

- A review of current air-cooling and liquid cooling technologies is to be done to understand the limitations of air-cooling methods.
- A review of enhancement methods for heat transfer at micro and macroscale is needed to evaluate possible options for further development.
- The modelling of individual components and the entire system is to be done to optimise the design of the cooling solution.
- The design of heat transfer features that are compatible with semiconductor processes is needed to remove the heat effectively.

- The design and setup of a test rig for hydraulic and thermal characterisation is needed to conduct experiments for hydraulic and thermal testing of the cooling solution.
- The comparison of experimental results with modelling is needed to determine any shortcomings in the design.

1.5 Organisation of report

Chapter 1 presents the introduction of this area of study and the motivation for this project.

Chapter 2 provides a review of the literature of works done on microchannels. Enhancement techniques and principles for heat transfer are discussed. Manifold designs are discussed as well.

Chapter 3 gives an overview of the components in the liquid cooling solution and the structure, the fabrication process and assembly of the stacked package.

Chapter 4 presents the numerical modelling work done for the components of the liquid cooling solutions.

Chapter 5 looks at how the experiments are carried out and the instrumentation involved.

Chapter 6 presents the results from the modelling and experiments and discusses about the findings.

Chapter 7 concludes the report and presents recommendations for future studies.

2 LITERATURE REVIEW AND THEORY

2.1 Literature review

The literature on microchannel flows had been growing steadily. Many studies were done on establishing the validity of the down-scaling of macro laws to suit microchannel flow. However, there is generally no consensus between various researchers on the criteria for which macro laws will not apply. A generally acceptable approach would be to consider the Knudsen number as to which continuum approach can be used.

2.1.1 Numerical and experimental heat transfer and fluid flow

Marazana et al. [2004] investigated the axial conduction problem for flow in mini- and microchannels. The work focused on developing guidelines to resolve the incoherence of data from heat transfer experiments. A new parameter, M is proposed to quantify the amount of axial conduction. A generalised model using thermal quadrupole method is used to model the exact heat conduction along the wall. Numerical solutions in the convection-diffusion model were done to look at the bulk temperature rise axially. For $M < 0.32$, a non-linear variation of bulk temperature and heat flux was observed. Axial conduction effects were found to affect the heat exchanger efficiency greatly if taken into account. An optimum conductivity for the solid material can also be found to minimise axial conduction effects.

Constructal theory proposed by Bejan [1997] had also been applied on microchannels design. Muzychka [2005] analyzed the heat transfer from microchannels under the fixed volume and pressure drop constraints. Using simplified analytical results and the method of intersecting asymptotes, expressions for optimum duct dimensions were derived. Many duct shapes were than compared using the heat transfer per unit volume (Q^*) as a basis. Although

these are first order estimates, comparison with literature had shown that the results were in good agreement. Nevertheless, this method providing the optimum dimensions for fundamental shapes enables a quick design review of all possible shapes and conventional methods of analysis should be used to obtain more accurate results.

Lee and Garimella [2006] had done numerical studies on heat transfer in rectangular channels with aspect ratios from 1 to 10, with the aspect ratio defined as the ratio between the long and short sides. A thin wall (no axial conduction) is used for the channels. Refinements along the channel length, particularly in the entrance region to take into account of developing effects were shown to be essential in obtaining a good estimate of pressure drop and Nu . Correlations for the local and average Nu and dimensionless thermal entry length were proposed and found to be in good agreement with conventional correlations and experimental data.

Li et al. [2006] numerically investigated the heat transfer properties in trapezoidal and triangular channels based on the field synergy principles (FSP). The data was then compared with experimental readings. The experimental results were lower than the numerical and can be accounted for due to data reduction. However, the concept of FSP had proven to be capable of explaining the degree of enhancement due to the synergy between velocity field and temperature gradient field associated with different cross sectional geometry.

Qu et al. [2006] developed a numerical model for adiabatic flow in a microchannel 222 μm wide 694 μm deep and 12 cm long using an analytical solution for fully developed flow and compared it with their experiments. Pressure drops were measured as well. Good agreement was achieved between the numerical models and experimental results for the velocity profile, suggesting that the Navier-Stokes equations can still be used to describe flow in

microchannels for the range of Re from 196 to 2215. Pressure drop from correlations and computations were also within limits of the errors.

Pega et al. [2007] used liquid and vapour R134a in their experiments to determine the friction factors in laminar, transition and turbulent regimes. Hydraulic diameters ranging from 69.5 to 304.7 μm and aspect ratios from 0.09 to 0.24 were used. A profilometer was used to measure the cross sectional areas and surface roughness. The Re was varied from 112 to 9180. In laminar region, the Poiseuille number is observed to be constant and varied with aspect ratio as in macro flow. The transition to turbulent flow occurred at a critical Re between 2150 and 2290 which is earlier than macro-flow. In the turbulent region with different surface roughness, the friction factors were considerably higher than that predicted with correlation by Churchill [1977].

Lee and Garimella [2007] investigated two phase flow in rectangular microchannels and developed new correlations for overall pressure drop and local heat transfer. Their experiments were compared with existing correlations to obtain the errors expected. An asymptotic model was chosen for the heat transfer model. The pressure drop is decomposed into the frictional and acceleration component. The functional form for the Chisholm constant which is used to calculate the two phase multiplier for pressure drop estimate included the mass flux and hydraulic diameter. Pressure drop correlation comparison showed the mean error to be between 16.4 to 55%. Heat transfer data showed that the errors can be as large as 92%. The new correlations were developed from regression analysis and shown to have errors of less than 15%.

2.1.2 Microscale enhancement techniques

Kandlikar et al. [2004] developed an algorithm to iteratively solve for the mass flow rate, fin thickness and channel spacing to minimise the pressure drop across a single pass arrangement for a given required power dissipation and channel

depth. Developing effects were also taken into account in the algorithm. The solution is then shown on a parametric plot. Offset strips fins are also shown to perform as well as straight fins but at a lower flowrate, which is advantageous from a micropump point of view. Single pass and split pass arrangements were compared and contrasted. The split pass was shown to be able to handle higher heat fluxes at lower pressure drop due to the shorter flow length.

Wei and Joshi [2004] investigated the use of stacked microchannel heat sinks in liquid cooling. Such configurations offer the advantages of reducing the flowrate needed to achieve a certain heat removal as compared to a single stack. A thermal resistance network is used to establish the parameters for optimum performance. The number of layers and the flow rate are found to be important parameters. When the flow rate is high, the thermal conductivity of the microchannel material is important as well.

Steinke and Kandlikar [2004] compared conventional straight microchannel structures with enhanced structures made by short fin strips offset periodically. The strips were pointed at the ends to reduce form drag. The channel spacing, fin length and fin spacing were varied to study their effects. The experiments conducted showed that all the enhanced geometries showed lower thermal resistances and higher pressure drop, trends that were also observed in the use of offset strips in compact heat exchangers. Larger heat fluxes are also being able to handle. There is also no significant improvement in performance when the geometrical parameters are varied. A new parameter called pumping flux is proposed when using the coefficient of performance (COP) as a performance metric. The enhanced surfaces had COP of an order magnitude higher than that of straight microchannels.

Wang et al. [2006] investigated flow through slightly curved channels and reported numerical work done to simulate the secondary flow generated by

centrifugal forces. Among the data reported, the Nu and $f.Re$ are higher than straight channels due to creation of Taylor vortices within the channel which provide the enhancement. The effect increases with Dean's number, a modified Reynolds number that takes into account the radius of curvature of the path and the diameter of the channels.

Steinke and Kandlikar [2006] reviewed the single-phase enhancement techniques used in conventional channels and compact heat exchanger for application in microchannels and minichannels. Surface roughness can be achieved in minichannels with the use of shaped memory alloys inserted into channels. Channels with triangular or square grooves or flow obstacles along the flow path are ideal choices for implementation due to better manufacturing capabilities. Curved channels, especially in microchannels, with a large ratio of radius of curvature to channel dimensions are suitable for use to gain enhancement due to the decrease in velocity gradients as a result of centrifugal forces pushing the fluid off the geometrical center. Fluid additives to increase the heat capacity of the fluid due to melting of solid particles had been experimentally investigated in conventional channels. The particles used are 50 μm in diameter in a 1.57 mm radius duct, with enhancement increasing with higher concentration. Smaller size particles are being developed for use in mini and microchannels.

Enhancement methods based on vorticity principles were investigated by Wei et al. [2007] where dimples were placed in a single row in a microchannel. Dimpled surfaces are attractive for its lowest pressure drop penalty among others such as rib turbulators and protrusions. Comparing with a plain surface, the dimpled surface can have higher Nu numbers due to the separated and re-circulated flow generated. The dimple streamwise pitch is also important as flow development downstream is affected by the secondary flow caused by vortex shedding.

2.1.3 Macroscale enhancement techniques

Sparrow et al. [1979] did comparative studies between staggered and in-line arrays of strip fins and a parallel plate under laminar flow. A thin fin (thickness small compared to channel dimension) analysis was used. Important geometrical parameters are the channel length and the channel spacing. A unit cell was defined to ensure that both in-line and staggered arrays have the same hydraulic diameter. For heat transfer, the in-line array was better in performance than staggered array as the heat transfer area was larger per cell. Higher velocities were also present and accompanied by a high pressure drop as well. When compared with the parallel plate, the interrupted surfaces performed substantially under the constraints of fixed mass flowrate and fixed heat transfer area.

Patankar and Prakash [1981] studied the effects of fin thickness on laminar flow and heat transfer on interrupted surfaces. Different fin thicknesses (t), non-dimensionalised with the distance between the centre of two fins (H), were explored. Recirculation effects were more prominent behind the trailing edge at higher Re and t/H . The increased frontal area for a thicker fin showed up in a higher f value, which combined the drag force and the wall friction. However, the heat transfer rate is not increased substantially when the pressure drop is increased, indicating that the drag force can be a major contributor. At the leading edge, the boundary layer is also shown to be disturbed by the deflection of the streamlines. Higher h values are found at the leading and trailing edges and higher Re giving a better distribution of heat fluxes.

Ligrani et al. [2001] presented a comparison of heat transfer augmentation techniques used commonly to cool internal passages of turbine blades. They include rib turbulators, pin fins, swirl chambers and dimpled surfaces. The principle mechanism for the improved heat transfer is the creation of secondary flow and vortices which improved mixing within layers and also promotes turbulent transport quantities. The level of enhancement is compared based on

additional heat transfer and pressure drop over that of a plain smooth surface. Swirl chambers and rib turbulators produced the highest augmentation accompanied by high pressure drop, while dimpled surfaces have lower heat transfer and pressure drop as well. However, if the performance were based on Reynolds' analogy, dimpled surfaces are the best choice.

Giovanni [2004] investigated the effects of rib turbulators heat transfer augmentation in a rectangular channel. Rib height (3 mm and 5 mm) and orientations (45°, 60° and 90°) were varied and continuous and broken ribs were used in the experiments. Local Nusselt maps were derived from liquid crystal imaging techniques. The ribbed surfaces were compared with smooth surfaces as well. Comparing the average Nusselt numbers obtained, broken ribs at 90° have the highest, while the lowest are for ribs angled at 45°. The frictional pressure drop also revealed the same trend. Higher rib heights are also shown to be better thermally but worse in hydraulic performance. Another trend observed was that the frictional factor was independent of Reynolds number.

Sahiti et al. [2005] looked at pin elements for enhancement for heat transfer and indicated that enhancement techniques should look at increasing h and area simultaneously, with pin elements having a height to diameter ratio of 15 being used in the experiment having an enhancement factor of 70 compared to a bare surface. The heat transfer coefficient was plotted against specific power and pin element surfaces performed better than bare surfaces.

2.1.4 Compact modeling of interconnects layer

Refai et al. [2003] used the area-average method to define an effective through plane conductivity for parallel heat paths and a one-dimensional resistant method for effective in-plane conductivity for series heat paths. However, the effects of spreading and constriction were ignored.

Ying and Toh [1999] developed analytical solution for a single solderball joint by solving the energy equation in cylindrical coordinates. The total resistance is the sum of material resistances across the plates and solderball, the spreading and constriction within the solderball and the spreading and constriction within the plates. The solution was presented in terms of Bessel functions and summed up to 20 terms. The total resistance was compared with a numerical model and found to be in good agreement.

Johnson et al. [1997] modelled the exact geometry of a solderball using Ansys software and the effective through plane conductivity was derived from a one-dimensional resistance model. However the use of an imposed temperature difference does not reflect the dependence of the spreading/constriction resistance on the Biot number.

Lee et al. [1995] investigated spreading resistance through analytical modeling for various boundary conditions. The shape of the source and plate was shown to have no effect on the spreading resistance and two disc with equivalent radii of 'a' and 'b' are used. The solution was presented in terms of Bessel functions and is a function of relative size ratio $\varepsilon=a/b$, relative thickness t of the plate, $\tau = t/b$ and Biot number ($Bi=hL_c/ks$). For τ greater than 0.6, the solution is independent of boundary conditions and approached the flux tube solution where the thickness of the plate approaches infinity. A simple approximation for finite plate thickness was also given with boundary conditions specified in terms of an external resistance.

2.2 Principles of Heat Transfer Enhancement

Enhancement techniques can be categorised depending on the fundamental mechanisms behind the improvement. In the laminar flow regime, transport properties are governed by energy transfer within laminas across the boundary layer. In turbulent flow, transport is realized through eddies and mixing within

fluid. Therefore, most enhancement techniques focus on manipulating boundary layer development. Important geometrical dimensions and their effects on the phenomena are discussed. Enhancement techniques can be classified as follows:-

- (a) New boundary layer development
- (b) Secondary flow generation
- (c) Localised turbulence

Based on these techniques, they are then scaled down to the microscale level to study the enhancement achievable.

2.2.1 Boundary layer development

When a fluid flows past a stationary body, boundary layer development occurs due to the no-slip condition at the walls, causing velocity variation from zero at the wall to the free-stream velocity. Temperature variation also occurred with the fluid closest to the wall assuming its temperature and varying to the free-stream temperature. All these variations occurred across a very thin layer called the boundary layer. In internal flow, this divides the flow length into two regions, the developing and the fully developed region.

In the fully developed region, the velocity and thermal boundary layers have merged (**Fig. 2-1**) and the velocity/temperature profiles are invariant in the stream-wise direction. These conditions simplify the differential equations greatly and many analytical studies had been done to characterise flow and temperature quantities in this regime.

Figure 2-1 Developing and fully developed region in channel flow

In the developing region, pressure, inertia and frictional forces are balanced by changes in momentum fluxes that are constantly changing due to the varying velocity profile. Hence, in the developing region, pressure drop is usually higher than fully developed conditions. For the temperature field, h is very high in the developing region as the temperature gradient at the solid-fluid interface is very large due to the thin thermal boundary layer and reached its asymptotic value in fully developed condition. For long channels, the developing region is usually shorter than the fully developed part and hence, can be ignored. However, in microchannels, the effects of the developing region cannot be ignored if short lengths are used and must be accounted for. The friction factor f is consequently replaced by f_{app} , where it includes effects from both regions.

Dimensionless parameters can be used to describe the fluid flow and temperature field. The axial distances x_{hy}^+ and x_{th}^+ are used to determine entry length for flow and temperature, respectively and they differ by the Pr . In this study, water is used as the fluid with $Pr > 1$. The consequence of this is that fully developed conditions for flow and developing conditions for temperature field can be assumed.

2.2.2 Offset Strip fins (OSF)

Probably the best compact heat exchanger geometry to make use of this phenomenon of new boundary layer development is the offset strip fins (OSF) geometry either in inline or staggered configurations (**Fig. 2-2**). This geometry is characterized by an array of short length fins. As the fluid enters the channel between the two fins, profile development takes place and breaks when it leaves the channel and repeats itself downstream. The repeating start of each boundary layer is also called periodic flow, as pressure and temperature downstream can be predicted from values upstream. The velocity and temperature profile is often in the developing region and high h values can be obtained together with an increase in pressure drop. Comparing with the plate heat exchanger geometry, the enhancement obtained more than outweigh the increase in pressure drop. The

size of the exchanger is also reduced considerably.

Figure 2-2 Offset strips geometry (a) Inline (b) Staggered

For the OSF geometry, the pressure drop is mainly associated with the shear stress as the flow is in the developing region if the fins' thickness is considered small compared to the channel dimensions. However, as the thickness increases, the fin acts like a bluff body in the flow field. This results in form drag and separation effects occurring at the leading and trailing edges. Re-circulation occurs at the leading edge, re-attachment of the flow occurs at a distance L downstream from the leading edge, and a wake develops behind the fins. The shape of the fins is not limited to rectangles. The effect of the form drag can be reduced by fins with elliptic/aerofoil shapes as the frontal area is reduced. Possible difficulties that may be encountered with such shapes will be during the manufacturing of these odd shapes. From a fluid/heat transfer point of view, these shapes are good alternatives to rectangular shapes. Important dimensionless ratios are the channel aspect ratio S/H , fin aspect ratio t/H and blockage ratio t/S , where H is the fin height. The aspect ratio of the channel S/H affects the profile development along the channel. The fin aspect ratio is a measure of the conduction losses along the fin. The t/S ratio determines the significance of frontal area on the overall pressure drop.

The definition for the cross sectional area used in the hydraulic diameter for this geometry should take into account of all possible heat transfer area, and in addition to the prime area $S \times L$ and finned area $2 \times H \times L$ where L is the stripped fin length, should include the fin cross sectional area $t \times H$ as well. The hydraulic diameter is then given by equation 2.1.

$$D_h = \frac{4SHL}{2(SL + HL + Ht) + St} \quad [2.1]$$

2.2.3 Secondary flow generation

Another way to enhance heat transfer will be to displace the maximum velocity off the geometrical center. This results in large gradients across the boundary layer which is typical of turbulent flow. Curved channels exploit the centrifugal force induced when flow moved through it. The centrifugal force will push the fluid away from the geometrical centre and create secondary flow within the cross section, creating Dean vortices.

Turbulent regime is characterised by enhanced convective heat transfer due to the thinner thermal boundary layer and pressure drop. Energy transport is realised through eddies created within the sublayers compared to conduction through laminas in laminar flow. Therefore, it is desirable to have an early transition into turbulent regime in order to have better heat transfer. However, the penalty is often in pumping power, especially in microchannels. Hence, this method of enhancement is often not used.

Local turbulence can be achieved by tripping the flow along the channel length with obstructions, such as rib turbulators that do not block the flow passage significantly. The angle of attack, which is the angle formed by the rib, and the flow axis, the rib pitch and the rib height are important parameters. The angle of attack determines the frontal area and mainly affects the pressure drop. Numerical and experimental studies done indicated an angle of 45° for optimum thermal-hydraulic conditions. The fin height affects the velocity gradients due to the reduction in core area. The rib pitch is associated with the re-attachment of the boundary layer.

2.2.4 Manifold designs

In the design of microchannel heat sink for liquid cooling purpose, the search is

often in the direction of getting higher h values and packing as many fins (increasing area, A) onto the base as possible. However, another area that ought to be look into is the distribution of the flow. The flow in the microchannels can be analysed as a series of streams carrying the energy away from the finned area in parallel flow as in a heat exchanger. The mixed mean temperature T_m is useful when we need to describe the average energy state at any axial location in a channel. For constant heat flux boundary condition, T_m varies linearly in the axial flow direction. An energy balance on a control volume can be done to show that the change in mixed mean temperature dT_m is inversely proportional to mass flow rate. Consider the case where the channels have different capacity rates (**Fig. 2-3**). In the fully developed region, h is a constant, and hence the Number of Transfer Units (NTU) [Equation 2.2] will be different on the two finned surfaces. This results in two different effectiveness values for each channel and alters the wall temperature (T_s) accordingly.

$$NTU = \frac{UA}{C_{\min}} \quad [2.2]$$

where UA is the overall heat conductance on each side and $C_{\min}$ is the channel having the lower heat capacity.

Figure 2-3 Temperature gradient across channels with $T_{m1} > T_{m2}$

In typical compact heat exchangers, the degree of mal-distribution can be described by a parameter called the “ineffectiveness”. Such mal-distribution typically limits the potential of the heat exchanger. For electronic systems,

temperature non-uniformity can lead to uneven thermal stresses on die and solderballs which will affect the reliability of the package. Mal-distribution can be induced by (a) operating conditions and (b) geometry. Operating conditions induced mal-distribution and is often due to viscosity and density variation. Geometry induced mal-distribution is caused by tolerances in manufacturing, passage to passage non-uniformity and manifold design. The last point will be described in greater detail as this is one where the designer has the most control over in the process.

The footprint on a package is fixed, and as a result, there is competition for space from many other components. In this package, electrical I/Os are found on the periphery and they provide the electrical and signal paths for the operation of the package. In general, advanced packages have many such I/Os due to the functional requirements and hence, will occupy a big proportion of the space available. Hence, there is a limitation on port sizes that can be made on the package for coolant entry/exit. However, from a flow distribution point of view, we would want this to be as large as the width of the heat sink as possible. An interesting effect occurs when we have flow entering/leaving the plenums into the channels. Depending on the flow arrangements (U-type or Z-type), different pressure profiles can occurred in the plenums (**Fig. 2-4**).

Figure 2-4 (a) U-type (b) Z-type arrangement and pressure distribution in plenums

For example, in a Z-type arrangement, as flow leaves the supply plenum into the channel, pressure increases downstream and when it joins the return plenum, the pressure along the return plenum will decrease. This is a result of conversion between dynamic and static pressure. And because the driving potential for flow across the channels is the pressure difference between the supply and return plenum, the variation of pressure in the supply/return plenum is of outmost interest.

In an ideal case, in order for flow to distribute itself evenly from a small manifold size to the width of all the channels and be collected back would require a long section of diverging-converging nozzle. However, such ideal case rarely exists because of the space constraints on the package. Hence, due to such limitation, several designs are proposed to overcome the difficulty to achieve the objective of even flow distribution through the use of momentum equations and optimisation techniques. The ultimate objective would be to design the manifolds to achieve the least thermal gradient across the chips.

3 DESIGN AND FABRICATION OF TEST ASSEMBLY

3.1 Overview of liquid cooling solution

A liquid cooling solution features several components performing different functions integrated together (**Fig. 3-1**). It also includes an external air/liquid - cooled heat exchanger to reject the heat to the ambient. At the same time, a thermal interface material (TIM) is used.

Figure 3-1 Schematic of components within Liquid cooling solution

Water is circulated in the system through a miniature pump mounted on top of the package, interfaced by an adaptor. The adaptor is needed to distribute flow from the single inlet to the two inlets of the package and collect the flow from the two outlets into a single outlet. An external liquid heat exchanger unit is placed on top to remove the heat to another cooling device. In the experiment, a cold plate is used on top of this external heat liquid heat exchanger and bond with a thermal interface material to remove the heat away. The one-dimensional thermal network is shown in Fig 3-2.

Figure 3-2 Overall thermal resistance network

3.2 Thermal test die

Heat dissipation and temperature sensing are realised through resistors and diodes found on the thermal test die. The basic cell (**Fig. 3-3**) had a size of 1 mm by 1 mm with a diode in the middle and connected by the A and C pads. The heating resistor is connected by the R pads. In the test vehicle, 100 such cells are being attached on the carrier.

Figure 3-3 Basic cell of a TTSC1 thermal test chip

3.3 Carrier Fabrication and Assembly

3.3.1 Carrier structure

The stacked module (**Fig. 3-4**) consists of two carriers bonded to a silicon interposer. The fluidic sealing is achieved through a metal/solder sealing ring. The stacked module is then attached to the printed circuit board using larger solderballs and underfilled. The footprint of the package is 15 mm by 15 mm, with a height of 2.8 mm. The test die is bumped with 60 μm solderballs and underfilled. The fabrication and assembly of the 3D stacked modules was done at the Institute of Microelectronics (IME) and described below.

Figure 3-4 Package Structure of Stacked Module

3.3.2 Carrier fabrication

The carriers in the package serve two main functions. Firstly, it provides the base area for which microchannels can be etched on to remove heat effectively from the die. Secondly, the fluidic and electrical interconnections are formed on the periphery to enable cooling medium/signals to be received or sent. Traces on the carrier enable the resistances on the test die to work as heater and the diodes to work as temperature sensing elements. The bottom carrier (CR1) and top carrier (CR2) are distinguishable only from their bottom side. For CR2, the bottom side has a trace layout identical to that of the top side while CR1 has one identical to that on the PCB (**Fig. 3-5**).

Figure 3-5 Schematic of Carrier Layout with microchannels and copper traces

Figure 3-6 Top view of CR2

Five diodes are used to measure the temperatures on the die. They are located in the middle (CR1-M), top (CR1-T), bottom (CR1-B), left (CR1-L) and right (CR1-R). Resistors are formed on the bottom and top chains, forming an effective resistance of $55\ \Omega$. The orientation is rotated two right angles for the CR2.

Figure 3-7 Process steps involved in carrier fabrication

The fabrication process begins with a 200mm (8”), 725 μm thick wafer (**Fig. 3-7a**). A 3 μm thick silicon dioxide (SiO_2) layer is deposited on the wafer by plasma enhanced chemical vapour deposition (PECVD) and the TSVs/fluidic channel are patterned (**Fig. 3-7b**). This is followed by a 2 μm photoresist coating and patterning for the vias (**Fig. 3-7c**). As the depth of the TSVs and channels are different, the through-via is etched 230 μm deep before the photoresist coating is stripped (**Fig. 3-7d**). The through-via is then etched a further 170 μm depth together with the microchannel, corresponding to the microchannel half channel height (**Fig. 3-7e**). The SiO_2 layer is then stripped by BOE (**Fig. 3-7f**). The backside of the wafer is then grind to 400 μm thickness to expose the vias (**Fig. 3-7g**). A 1 μm thick passivation layer of SiO_2 is then deposited on the channel side and back side of the wafer (**Fig. 3-7h**). Underbump metallisation (UBM) is deposited and patterned on the channel side and back side of the wafer (**Fig. 3-7i & 3-7j**). 1 μm thick SiO_2 is deposited on the back side and patterned for the

carrier passivation layer (**Fig. 3-7k**). The fluidic ports are then laser drilled (**Fig. 3-7l**). The Au/Sn solder is then deposited on the wafer and patterned (**Fig. 3-7m**). The process is completed by bonding two such wafers together at 350°C for 15 minutes with a compressive strength of 4.7 MPa (**Fig. 3-7n**).

Figure 3-8 Carrier with die footprint removed

Figure 3-9 Two wafers bonded to form a carrier

3.3.3 Carrier assembly

The bonded carrier wafer is diced using mechanical dicing tool of 15 mm x 15 mm size. CR1 and CR2 designs are combined on the same wafer. The singulated carrier chips are selected for the 3D module assembly. The assembly processes involves pick and place of the chip on the carrier and reflow to attach the chip with the carrier. The pick and place of the test chip is using SRT (Sierra) with a force of 1 kg. The duration for place and hold is 10 s. Then the solderballs of 300 μm diameters are manually placed on the carrier and reflowed in the BTU oven with two different profiles. Profile 1 uses SnAgCu at a peak temperature for

255°C for 30 s. Profile 2 uses SnPb at a peak temperature of 198°C for 30 s. The underfill is dispensed at chip to carrier and CR1 to the board. Asymtek (A-512) is used for underfilling a polymer material U8443-14 supplied by Namic. The process parameters are as follows.

- 4 bar pressure
- Underfill pattern: I shape
- 4 passes
- Needle size: 30G (chip) and 25G (board)

The substrate is held at 110°C during underfilling. Then the underfill is cured temperature at 150°C for 30 minutes in a convection oven. The 3D module assembly steps are described below. The test chip is attached to CR1 and CR2 and reflowed with profile 1 (**Fig. 3-10**). After the reflow process, underfill is done.

Figure 3-10 Die on carriers with underfill before and after reflow profile 1

After this process, the interposer is bumped with 300 μm solderballs (**Fig. 3-11**). When this is completed, the interposer is attached to CR1 (**Fig. 3-12**). At the same time, solderballs are placed on the board (**Fig. 3-13**). The interposer-CR1 assembly is then placed onto the board (**Fig. 3-14**). The reflow process in these steps uses profile 1.

Figure 3-11 Schematic of interposer reflow process

Figure 3-12 Schematic of CR1 and interposer attachment

Figure 3-13 Solderballs placement on board and reflow

Figure 3-14 Schematic of interposer-CR1-board assembly

For CR2, solderballs are attached to the pads on bottom side using profile 2 (**Fig. 3-15**). After these steps, the interposer-CR1-board assembly and CR2 are attached together using profile 2 (**Fig. 3-16**). Lastly, underfill is dispensed between the CR1 and board.

Figure 3-15 Schematic of CR2 reflow process

Figure 3-16 Schematic of carriers assembled on board

3.4 Micropump selection

Having discussed the importance of the microchannel heat sink performance for acceptable junction temperature, and the external heat exchanger to reject heat to ambient, focus is now placed on the micropump, which delivers the working fluid (water) in a closed loop for the other components to perform their functions. The objective of the micropump is to deliver the required flowrate with the pressure to overcome the system losses. Two miniature pumps had been identified as potential candidates for use in the cooling system. They are gear pumps with variable speed control. Beside the head-flow requirements, another selection criterion is the footprint and height of the miniature pumps, as this will affect the compactness of the system. Another aspect in miniature pump selection is the type of fittings available commercially to connect the tubing. For P1, it is supplied by Micropump Inc. and the interface is through two 1/8" NPT fittings to connect to either a 1/4" or 1/8" tubing. The footprint is a 30 mm diameter circle with a height of 70 mm. For P2, it is supplied by Flightworks Inc (**Fig. 3-17**) and can only be connected to 4 mm tubing. The footprint from this pump is 37.1 mm by 34 mm and a height of 16 mm. By comparing the two, the lower profile height of P2 has a greater advantage over P1 in making the system compact.

Figure 3-17 Micropump from Flightworks (P2)

4 NUMERICAL MODELLING

4.1 Thermal Modelling and Simulation

The commercial CFD package used in this project is ICEPAK, which is tailored for thermal analysis of electronic packages. It runs on the ICEM mesh generation and FLUENT solver. The equations of mass continuity, momentum and energy are discretised and solved iteratively to analyse the pressure, velocity and temperature field in the solution domain. The equations are given in vector form

$$\text{Continuity:} \quad \frac{\partial \rho}{\partial t} + \nabla \cdot \vec{V} = 0 \quad [4.1]$$

$$\text{Momentum:} \quad \frac{\partial (\rho \vec{V})}{\partial t} + \rho (\vec{V} \cdot \nabla \vec{V}) = -\nabla p + \nabla \cdot (\vec{\tau}) + \rho \vec{g} + \vec{F} \quad [4.2]$$

$$\text{Energy:} \quad \frac{\partial (\rho h)}{\partial t} + \nabla \cdot (\rho h \vec{V}) = \nabla \cdot [(k + k_t) \nabla T] + S_h \quad [4.3]$$

where ∇ is the gradient operator, $\vec{V}$ is the velocity vector, p is static pressure, $\rho \vec{g}$ is the gravitational body force, $\vec{F}$ is the momentum source term, $\vec{\tau}$ is the stress tensor, h is sensible enthalpy with 298.15 K as reference temperature, T is temperature, S_h is volumetric heat source, k is thermal conductivity, k_t is the conductivity due to turbulent transport and μ is the dynamic viscosity.

Before any numerical work on the packages is done, a benchmark problem on a similar but simplified model with exact analytical solution was modelled to validate the accuracy of the software. Values of fully developed laminar h for rectangular channels with different aspect ratios and the two commonly encountered boundary conditions, constant heat flux and constant temperature were reported by Kays [2005] and Shah [2003] in many handbooks. Solutions for the velocity profiles were solved analytically and used for the energy equation. A channel with aspect ratio of 1 was used in this benchmark problem. The channel

dimensions are $50 \mu\text{m} \times 50 \mu\text{m} \times 10 \text{ cm}$ with a wall thickness of 10microns. The wall thickness is small to minimised axial conduction effects. Since silicon has a high conductivity (100 W/m.K), a constant heat flux boundary condition is imposed. The corresponding Nu number is 3.6 for a four-sided heating condition. The dimensionless hydrodynamic and thermal entry length occurs at $x_{hy}^+ = 0.05$ and $x_{th}^+ = 0.1$, respectively. The definitions for the dimensionless hydrodynamic and thermal entry length are given in equation [4.4] and [4.5] as

$$x_{hy}^+ = \frac{x}{ReD_h} \quad [4.4]$$

$$x_{th}^+ = \frac{x}{RePrD_h} \quad [4.5]$$

where x is the flow length, Re is the Reynold's number based on the hydraulic diameter and mean flow velocity as the characteristic length and velocity ($Re = \rho U D_h / \mu$), Pr is the Prandt number of the fluid ($Pr = \mu C_p / k$) and D_h is the hydraulic diameter.

Under the assumptions of uniform temperature peripherally, the implied orthotropic conductivities of the material are high peripherally and low in stream-wise direction. In this model, the conductivity is set to $1 \times 10^5 \text{ W/m.K}$ in x and z direction and $1 \times 10^{-9} \text{ W/m.K}$ in y direction. Boundary conditions imposed on the geometry are as followed (**Fig. 4-1**):

Figure 4-1 Geometry used in benchmark problem

- (i) At $z = 0$, $\frac{\partial T}{\partial x} = q''$ (uniform heat flux $1 \times 10^6 \text{ W/m}^2$)
- (ii) At $x = 0$, $\frac{\partial T}{\partial x} = q''$ (uniform heat flux $1 \times 10^6 \text{ W/m}^2$)
- (iii) At $x = 0.06 \text{ mm}$, $z = 0.06 \text{ mm}$, $\frac{\partial U}{\partial x} = \frac{\partial U}{\partial z} = 0$ and $\frac{\partial T}{\partial x} = \frac{\partial T}{\partial z} = 0$

for symmetry boundary conditions, i.e. no heat/mass flux across boundary

- (iv) At $y = 0$, $U = 1 \text{ m/s}$ and $T_m = 20^\circ\text{C}$ (uniform inlet velocity and temperature)

The quarter model enables more meshes to be generated and the mesh is refined near the wall to capture the temperature and velocity gradients. The Re for the flow is 62 and x_{hy} and x_{th} are thus 0.312 mm and 1.69 mm, respectively. The channel length in the stream wise direction is 10 mm, which is much longer than the hydrodynamic and thermal entry length and hence fully developed velocity profile can be assumed. In laminar heat transfer, h is constant in the fully developed region. Grid independent tests were conducted and converged at a mesh density of 120K elements. Axial mixed mean temperature can be calculated using equation 4.6.

$$T_m(x) = T_{m,in} + \frac{q''_{avg} P}{\dot{m} C_p} x \quad [4.6]$$

in order to estimate the h values in the fully developed thermal region. The variation in heat flux along the surfaces can be represented by an average value if we defined q''_{avg} to be $Q/\text{Wetted Cross-sectional Area}$. With this, h was found to be $22842 \text{ W/m}^2\cdot\text{K}$. The calculated Nu number thus is 3.625 and comparing with the analytical solution of 3.6, the difference in values is less than 1%. From this study, the software is shown to be able to predict thermal performances of microchannel heat sink.

4.2 Thermal resistance model

Thermal resistances based on one-dimensional heat conduction can be used as a first order estimate of the magnitude of each individual resistances and their contribution to the overall thermal resistance. They defined the extent to which efforts in resistance minimisation are needed. The heat flow path can be defined as follows: -

- (i) Junction to interconnects ($R_{\text{interconnects}}$)
- (ii) Solderballs to heat sink base ($R_{\text{sp}} + R_{\text{mat}}$)
- (iii) Heat sink base to fins and to fluid (R_{fin})
- (iv) Fluid temperature raise (R_{conv})

The thermal resistances within each path consist of material, spreading, constriction, convective and bulk resistances. Material resistance occurs as a result of temperature difference across a thickness of finite area. Spreading and constriction resistances occur due to the difference in size between a source and sink and hence heat flow lines are not parallel to one another. Convective resistance is due to heat transfer from a solid to fluid across a temperature difference between wall and fluid and as a result, causes temperature rise along the stream-wise direction due to energy balance for constant heat flux boundary conditions. An assumption used here is that the effectiveness of the microchannel heat sink is very close to unity. These resistances are influenced by geometry and/or fluidic properties. A detailed calculation is provided in the appendix.

In this model, an effective conductivity is derived based on an area-averaged conductivity of solderballs and air. The junction temperature predicted is 98°C based on an inlet temperature of 50°C. Looking at Fig. 4-2, the resistance across the interconnects is 57% of the overall thermal resistance. The rest of the resistances, which is essentially the heat sink resistance, are 43%. Hence, in trying to achieve lower junction temperature, efforts to introduce enhancement techniques to improve the heat transfer and reduce the $R_{\text{interconnects}}$ should be of the same proportion.

Figure 4-2 Thermal resistances within a package

From this resistance model, detailed numerical modelling of the solderball layer to account for the spreading and constriction effects and also the microchannel heat sink is needed. Also, the numerical modelling can be de-coupled into two problems, one that of conduction in the interconnects layer and the other of the microchannel heat sink. The boundary condition at the interface between these layers would be a uniform “ h_{eff} ” at the bottom of the solderball layer and a uniform heat flux q'' to the microchannel heat sink (**Fig. 4-3**).

Figure 4-3 Boundary conditions imposed for the two models

4.3 Numerical modelling of chip interconnect layer

From the analytical model, an effective orthotropic thermal conductivity is used for the chip interconnect layer, with the in-plane conductivity much smaller than the through-plane. The through-plane conductivity can be derived from the analysis of a parallel network of resistances across the solderball layer. The in-plane conductivity is assumed to be small due to the low conductivity of the underfill material or air compared with the solderball material. In order to estimate the resistances across the solderball layer, numerical modelling is used. The spreading, material and constriction resistances across a single solderball need to be properly accounted for in order to estimate the effective thermal resistance of the layer. However, to model the full array of solderballs would be computationally expensive due to the small scales involved. Loh et al. [2000] used the equivalent volume method to replace each spherical ball with an equivalent cube with a height that of the reflow height (**Fig. 4-4**). This method had been shown to have the best approximation to the thermal resistances across a single solderball and is adopted here.

Figure 4-4 The equivalent volume method to replace solderball geometry

A quarter model was developed for a single cell of size 1 mm by 1 mm used in the TTSC1 thermal test chip (**Fig. 4-5**). The solderball array is depopulated with eight solderballs around the periphery. The geometry of the single module is

shown below with lines of symmetry together with the solderball layout. The overall test chip is 10 mm by 10 mm and consists of 100 such cells.

Figure 4-5 Layout of solderballs on a single TTSC 1 cell

Two different interconnects architecture are proposed and they are flip chip and wirebonding. For both interconnects, uniform heat flux is applied to the top layer of the silicon chip. An effective “convective” resistance based on the sum of the heat sink and convective resistances are assigned to the bottom of the heat sink base layer. The hatched area represents the model used with the symmetry conditions.

Figure 4-6 Layout of components under thermal test chip

Different geometries and underfill materials were proposed with the objective to minimize the resistances across this layer. There were three different reflow heights (75, 60 and 30 μm) used in the modeling. Solder with a thermal conductivity of 57W/m.K is used. The two underfill materials include solder paste ($k = 2 \text{ W/m.K}$) and air ($k = 0.026 \text{ W/m.K}$). For 30 μm reflow height, only air is used as the underfill as solder paste cannot be applied evenly beneath the die. A copper slug is also used in the modelling to investigate its benefits on reducing the thermal interface. For wirebonding, a bond line thickness of 25 μm is used. Solder paste of different conductivities ($k = 2, 10$ and 50 W/m. K) were used. Different die heights (0.2 and 0.65 mm) were used in the model. In flip chip interconnects, the heat is supplied beneath the die and the thermal resistance of a module can be calculated based on equation 4.7.

$$R_{\text{module}} = \frac{T_{\text{source}} - T_{\text{sink}}}{Q} - R_{\text{material 1}} - R_{\text{material, 2}} \quad [4.7]$$

$R_{\text{interconnects}}$ can then be derived by dividing R_{module} by the total number of modules. For wirebonding, heat is supplied from the top of the die. Hence, $R_{\text{interconnects}}$ is the ratio of the temperature difference between the top of the die and the bottom of the bondline and the total power input.

Figure 4-7 Thermal resistances across solderballs layer for different reflow height

From Fig. 4-7, the resistance decreases as the reflow height is decreased. The use of a better conductivity underfill material also helped in achieving lower resistances. For wirebonding, lower $R_{\text{interconnects}}$ can be achieved through the use of a lower chip height and higher conductivity solder paste (**Fig. 4-8**). Comparing the two different architectures proposed, wirebonding should be chosen due to its lower resistances. However, looking from the functional point of view, flip chip interconnects have many advantages as compared to wirebonding. They include:-

- i. Carrier size reduction to near die size
- ii. Shorter interconnect paths hence shorter processing time
- iii. Large number of I/O
- iv. Lower failure rate as compared to wirebonding

All these advantages help in reducing the package size, extending mean time to failure and improved functionality. By using a better underfill material, comparable resistances can be obtained from flip chip interconnects.

Figure 4-8 Comparison of thermal resistances for die-attached for different solder paste conductivity and chip height

In flip chip interconnects, the use of a copper slug is also explored. The copper slug has dimensions of 5 mm by 5 mm with the thickness similar to the reflow height and is placed centrally within the package, replacing the solderballs in the area. The resistance of the solderball array is derived by dividing R_{module} by 50, which is the total number of modules found on the periphery. A thermal conductivity of 390 W/m.K was used for copper.

The use of a copper slug within the solderballs reduced $R_{\text{interconnects}}$ by an average of 20% (**Fig. 4-9**). The use of a higher conductivity underfill diminished the effects of the copper slug, while its effects are more prominent when air is used. However, there is a large temperature variation on die which is around 20°C (**Fig. 4-10**). This posed a very serious problem and can be further compounded when the three-dimensional effect such as spreading within the heat sink base is taken into account.

Figure 4-9 Comparison of $R_{\text{interconnects}}$ with/out copper slug

Figure 4-10 Variation of temperature on die for 60 μ m reflow height with a copper slug

A detailed model of a truncated sphere between two substrates was also used to represent the solderball joint and modelled in ANSYS to account for spreading and constriction effects within the solderball (**Fig. 4-11**). In this model, the copper pad diameter d_2 is used. The geometrical dimensions for the solderball are given in Table 4-1.

Table 4-1 Geometrical dimensions (μ m) for ANSYS modeling

Reflow height, h	Pad diameter, d_2	Solderball diameter, d_1
30	50	60
60	80	100
75	80	100

In the numerical modelling of the solderball with ANSYS, a command file known as the Ansys Parametric Design Language (APDL) file is read into the program. The model was meshed with elements Brick 8 Node 70. The through-plane node count was increased to study grid independence but due to the limitation of the academic license, the number of nodes can only be increased to almost 32000 nodes. The grid was thus said to have converged. Energy balance across the top and bottom surfaces of the upper and lower substrate was done to ensure that the edges were adiabatic.

Figure 4-11 Numerical model of solderball in Ansys

Using these dimensions, the total resistance R_T across the solderball was derived based on the same equation used in the compact modelling approach. The results of the modelling are shown in Table 4-2. An analytical solution was also derived to compare the numerical results. The spreading and constriction within the substrates (R_{con} and R_{spr}) was based on the flux tube solution by Negus and Yovanovich [1984] and compared with numerical results. The use of the flux tube solution represents the lower limit of the resistance where it is boundary condition independent and has an infinite thickness. The material resistance is represented by a cylinder with the same diameter d_1 as the solderball maximum diameter. The analytical solution had ignored the effects of spreading and constriction within the solderball.

Figure 4-12 Heat flow lines and isotherms in a flux tube solution

Figure 4-13 (a) Geometrical dimension of a solderball (b) Heat flux lines and resistance components used in analytical model

Table 4-2 Total thermal resistance of one solderball for different reflow heights

Reflow height (μm)	$R_{th, num} (^{\circ}\text{C}/\text{W})$	$R_{th, analy} (^{\circ}\text{C}/\text{W})$	$\varepsilon = a/b$
30	339.84	327.25	0.177
60	228.13	203.34	0.283
75	262.48	235.17	0.283

From Table 4-2, we can see that the resistance across the 30 μm reflow height is the largest. The difference in spreading and constriction resistances between the 30 μm and 60/75 μm reflow heights is due to the different equivalent radius ratio ($\varepsilon = a/b$, where a is the source's radius and b is the sink's radius). There are small differences between the 60 μm and 75 μm reflow height and is due to the material resistance across the solderball for these heights. Comparison of the numerical and analytical results showed that the analytical results underestimated the resistances with errors within -3% to -10%. The under-estimation could be due to the finite thickness of the substrates and the spreading and constriction effects within the solderball. Using the numerical model, we can represent the total resistance R_T across the solderball as spreading, material and constriction resistance (R_{sb}) within the solderball and spreading (R_{spr}) and constriction (R_{con}) within the substrate using the analytical solution (**Fig. 4-14**).

Figure 4-14 Comparison of the different resistances across a solderball

From Fig. 4-14, the material resistance contributed the largest proportion to the overall resistance. The larger material resistance is due to the ratio of the reflow height, h to the cross sectional area based on the solderball diameter, which is larger for the 30 and 75 μm reflow height than the 60 μm . Hence, reflow height is an important consideration when minimising the interconnects resistance.

Figure 4-15 Heat flux lines across solderball for 30 μm reflow height

Figure 4-16 Heat flux lines across solderball for 60µm reflow height

The heat flux lines for the 30 µm and 60 µm reflow heights are shown in Fig. 4-15 and 4-16. By looking at the change in area from the top pad diameter to the solderball maximum diameter and back to the bottom pad diameter, we can see that the heat flux lines are diverging and converging. The constriction/spreading effects can be seen by the non parallel paths of the heat flow lines when it passed from/to the silicon material.

Having fully modelled a single solderball joint in detail, a more accurate representation of the resistances of the solderballs can be used to model the single cell in the TTSC1 thermal test chip when used with the underfill. The spreading, constriction and material resistances (R_{sb}) in a solderball can be obtained from the detailed modelling by deducting the constriction (R_{con}) and spreading (R_{spr}) resistances from the overall resistance. The two resistances can be approximated by the flux tube solution. A cube with the same reflow height and pad cross sectional area having a conductivity derived from R_{sb} was used to replace the solderballs beneath the test chip (**Fig. 4-17**). A quarter model was also used to numerically model the layer. The pad cross sectional area was chosen as the effects of spreading and constriction within the plates into the

solderball can be estimated through this compact model instead of the pitch which is used to prepare the detailed model.

Figure 4-17 Cube used in compact modeling with material properties

The comparison between results obtained earlier by the equivalent volume method and the detailed model shows that by using the actual pad area and with a better estimation of the resistances within the solderball, a 17% reduction in $R_{\text{interconnects}}$ could be achieved (**Fig 4-18**) The reduction is due to the lower $h/(k_{\text{eff}}A)$ derived from the detailed model. However, this does not refute the fact that the equivalent volume method is erroneous. It just shows that this method is only suitable to study the effects of relative size ratio on spreading/constriction effects for the same reflow height.

Figure 4-18 Comparison of interconnect resistance for compact model using the equivalent volume and detailed models

Figure 4-19 Temperature contours across the first row of solderballs showing the constriction and spreading effects

The interconnect layer resistance is strongly dependent on three parameters, underfill conductivity, solderball and cell pitch. The pitch determined the number of balls allowable beneath the die while the underfill conductivity determined the effective resistance in the parallel path between the solderballs and underfill. Apart from the configuration discussed above, three more possible solderball arrangements are possible. The original layout has a 250 μm pitch between the solder balls and a 500 μm pitch between cells (**Fig. 4-20a**). The second layout has the same pitches but the balls at the corners are removed (**Fig. 4-20b**). The third layout has a 500 μm pitch between solder balls and 1 mm spacing between cells (**Fig. 4-20c**). The last layout is fully populated with solderballs with a 200 μm pitch (**Fig. 4-20d**).

Figure 4-20 Solderball layout with (a) 8 solderballs, 0.25 mm pitch (b) 4 solderballs, 0.25 mm pitch (c) 2 solderballs, 0.5 mm pitch (d) 25 solderballs, 0.2 mm pitch

Having determined the effective resistance in a single joint, the effects of pitch sizes can be analysed. 1 W is applied uniformly across one cell. Table 3 showed the results of the numerical modelling. The use of a smaller pitch had reduced the resistance significantly, from 0.23 to 0.07°C/W, due to the greater number of solderballs, hence increasing the conductive path. The use of fully populated array of solderballs instead of peripheral joints also helped in reducing the resistance as the heat does not need to spread to reach the peripheral joints.

Table 4-3 Thermal resistance of different solderball pitch layout

Model	(a)	(b)	(c)	(d)
R_{th} (°C/W)	0.15	0.20	0.23	0.07

From Table 4-3, we can see that the thermal resistance of the interconnect layer is strongly dependent on the solderballs available for heat transfer. This is another important variable beside the resistance of the carrier to achieve lower junction temperatures.

4.4 Carrier design

In this project, the microchannels are etched on the carriers instead of on the chip. A base model is generated and all designs are compared with it. Since the two packages are identical, modelling is done on one package and extended to the other. The $R_{\text{interconnect}}$ used in the model is $0.2^{\circ}\text{C}/\text{W}$. Constant properties of water taken at the average temperature of 55°C is used ($\rho = 986 \text{ kg}/\text{m}^3$, $\mu = 0.000501 \text{ kg}/\text{m.s}$, $k = 0.6463 \text{ W}/\text{m.K}$ and $C_p = 4178 \text{ J}/\text{kg.K}$).

4.4.1 Single Inlet/Outlet microchannel heatsink

The most common microchannel heatsink geometry is that of a single inlet and single outlet. The fluid enters from the inlet into the supply plenum and distributes itself across the microchannel before collecting back at the outlet. This simple geometry (**Fig. 4-21**) is the easiest to fabricate and can be analysed as a parallel plate heat sink.

Figure 4-21 Geometry of carrier showing the inlet/outlet (Not to scale).

A numerical model of the microchannel heat sink together with the die and interconnects was done. Taking advantage of the symmetry condition, a half model with created. The geometrical dimensions of the model are:-

- Die size of 10 mm by 10 mm
- Heatsink base of 10.3 mm by 11 mm
- 68 fins of width 50 μm and length 10 mm
- 69 channels of width 100 μm and height of 350 μm
- Inlet/Outlet size of 4.5 mm

The design specifications at the package level are listed as follows:

- Remove 100 W/cm^2 of heat flux from the die to cooling fluid
- Maximum rise of die temperature over fluid inlet temperature to be less than 35°C
- Temperature variation on the die to be less than 10°C
- Available carrier footprint is 15 mm by 15 mm

The inlet temperature of water is fixed at 50°C. This design (S1) forms the basis of comparison of other designs to be implemented. The design flowrates are 100, 200 and 230 ml/min for each carrier where the last flowrate is the maximum flowrate the pump can deliver for a single carrier.

4.4.2 Plenum design

The flow distribution across channels is governed by pressure differences between the supply and return plenums. The conversion of static to dynamic pressure changes the pressure profile within the plenum. Hence, it is desirable to distribute flow such that the heat transfer per unit area within the channels is the same to minimise temperature variation.

Figure 4-22 Control volume used in the Bernoulli equation

To understand the pressure variation in the supply plenum, the Bernoulli equation (4.8) is written between two successive fins where point 2 is downstream of point 1 (**Fig. 4-22**).

$$P_1 + \frac{1}{2}\rho V_1^2 = P_2 + \frac{1}{2}\rho V_2^2 \quad [4.8]$$

When the flow enters into the channel, the continuity equation requires that $Q_1 = Q_2 + Q_c$ where Q_c is the flowrate entering into the channel. Hence, for a constant cross sectional area, ($A_1=A_2$), V_2 will be smaller than V_1 and pressure will rise downstream. The assumption used is that the plenums are large enough such that losses (L/D) along the plenum are negligible. The reverse phenomenon is seen in the return plenum and hence the pressure decreases downstream. From this reasoning, it is readily seen that the changes in the cross-sectional area within the plenums have implications on the pressure variation in the plenum. For a plenum with a constant height, the changes in the cross sectional area would mean determining the functional relationship of the fin length with distance across the width. This provided the basis of the choice of shape that is proposed to solve the flow mal-distribution issue.

From the literature review, studies on flow distribution had primarily been restricted to heat exchangers. London [1968] derived the functional form of the shape of the plenum using inviscid theory. Three common flow configurations,

parallel also known as Z-type, counterflow also known as U-type and a free discharge and the corresponding plenum designs are used. A constant area for the return plenum is used. Important geometric parameter to take note for the profile is the ratio of inlet and outlet size (z_0/y_0). From this, we can see that to have good flow distribution, the plenum area should decrease downstream (**Fig. 4-23**). The profile shown is given by equation 4.9, with the distance non-dimensionalised by the flow length ($X^* = X/L$).

$$\frac{z}{y_0} = \frac{1 - X^*}{\left[\left(\pi^2 / 4 \right) (X^*)^2 + (y_0 / z_0)^2 \right]^{1/2}} \quad [4.9]$$

Figure 4-23 Parallel header design according to London, 1968.

Through these theoretical studies, shape functions for the supply and return plenums are proposed for use in microchannel heat sink to improve flow distribution. In a limited space such as on the carrier, the finned area should be maximised with the objective to obtain a flow distribution such that the temperature gradient is minimised. The shapes of the plenums used are described briefly.

Figure 4-24 Carrier design (a) S1 (b) CR1 (c) CR2. (Not to scale)

Many plenum designs had been explored and two are being proposed to compare with the base model (Fig. 4-24). The two designs are the same, except for the fins layout on the carrier. There are two inlets and outlets of 1.5 mm and 3 mm by 0.5 mm for flow entry/exit, respectively. The modelling was done on a quarter model based on symmetry conditions. The first design (CR1) has a constant supply plenum width of 1.5 mm while that of the return is 0.5 mm. The second design (CR2) had a reducing plenum width downstream of the flow. The tapering of the plenum can be seen in Fig. 4-24.

Figure 4-25 Plenum width as a function of downstream distance

The use of a two inlets/outlets design had several advantages over the single inlet/outlet design. In a liquid microchannel cooling solution, high core pressure drop across the channels results in either very low flowrates or a pump with large dimensions. This will affect either the thermal performance or the overall size of the cooling solution. Pressure drop across the microchannels is due to two effects. The first effect is from the inertia effects in the developing region due to the changing velocity profile with a quadratic dependence on mean velocity. The second is due to the laminar frictional flow with a linear dependence on mean velocity. With the new design, a quarter of the flow is passing through the carriers. This flow configuration results in a shorter flow length (L) and lower mean velocities (U) within the channels, hence reducing the pressure drop as given by equation 4.10.

$$dP = \frac{2(f Re)\mu L}{D_h^2} U + K(\infty) \frac{1}{2} \rho U^2 \quad [4.10]$$

From a thermal point of view, the proposed designs had two benefits over the base design. The shorter flow length caused smaller increases in the mixed mean temperature of the flow. Higher Nu_m number per unit length can also be achieved as the developing region is covering a substantial portion of the flow length (**Fig. 4-26**). These two factors can result in small temperature difference between wall and fluid for a constant heat load.

Figure 4-26 Local Nu number variation with distance

In the numerical modelling of the microchannel heat sink, two different grids were generated. The difference between the first and second grids is the presence

of artificial flow openings in the microchannels in the first grid. The use of these artificial openings is to gather information of mass flow rate passing through each microchannel. With the presence of these openings, the mesh generated can only be a structured grid, and hence, resulting in a large mesh count. For the second grid, the openings were removed and unstructured grid was used to model the details near the microchannel leading and trailing edge, where the velocity vectors were expected to have large gradients due to the turning into and out of the microchannels. Gradients near the wall and the entry region were refined to capture the thin boundary layers and the entrance effects. Due to the fine meshing details required in the microchannel heat sink, a non-conformal meshing was used. The interface location was chosen such that there is minimal variation in field parameters. This non-conformal mesh enabled a fine mesh to be embedded within a coarse mesh so that external to the microchannel heat sink, the mesh count is greatly reduced for computational efficiency. A grid independence study was also done in the package modeling. The pressure drop from inlet to outlet and the maximum temperature at the die is monitored to check for convergence. The first grid converged at 1,500,000 elements and the second grid at 1,000,000 elements, with changes in pressure drop of less than 7% and temperature by less than 3% based on inlet temperature.

Figure 4-27 Meshing details of microchannel heat sink

Figures 4-28, 4-29 and 4-30 showed the temperature contours on the die for the three carrier designs for the three design flowrates. The results are summarised in table 4-4. From the temperature contours, the base model (S1) and CR1 had maximum temperature in excess of 85°C for all the flowrates. For CR2, the maximum temperature is within the design junction temperature of 85°C above 200 ml/min. CR1 and CR2 also had lower temperature variation than S1. The use of a two inlets/two outlets design had lowered the head requirements to deliver the flowrates into the carrier. At the highest flowrate of 230 ml/min, S1 required 150% and 50% more head than CR1 and CR2, respectively.

Figure 4-28 Temperature contours on die at 100 mL/min

Figure 4-29 Temperature contours on die at 200 mL/min

Figure 4-30 Temperature contours on die at 230 mL/min

Table 4-4 Summary of microchannel heatsink performances

Flowrate (ml/min)	Design	Pressure drop (mbar)	Maximum Temperature (°C)	Temperature variation (°C)
100	S1	158.1	98.74	22.51
	CR1	55.45	97.20	8.62
	CR2	76.7	93.39	9.42
200	S1	398.7	92.10	18.49
	CR1	169.7	91.80	9.56
	CR2	253.1	87.20	7.84
230	S1	484.7	91.11	17.90
	CR1	211.0	90.90	9.40
	CR2	326.3	86.31	7.64

The flow distribution within the microchannel heat sink is investigated to understand its implication on the thermal performance. In order to compare between the designs, the flowrate in each channel is normalised with the average flowrate in a uniform flow situation (**Fig. 4-31**). The heat fluxes through the base of the microchannels are also shown (**Fig. 4-32**).

Flow distribution for different microchannel designs

Figure 4-31 Flow distribution in S1, CR1 and CR2 at 200 mL/min

Variation of heat flux through base of microchannel fins

Figure 4-32 Heat flux through base of microchannels at 200 mL/min

Comparison of thermal entry length for different microchannel designs

Figure 4-33 Comparison of thermal entry length for S1, CR1 and CR2

From Fig. 4-31, the flow distribution is most severe in the case of CR1. The effect of such a flow distribution is the high temperature region near the inlet. For S1, the flow distribution improved but the long flow length had caused a high streamwise temperature gradient. For CR2, the distribution had been even out, except for the first three channels. From Fig 58, the heat distribution for each case is similar. Hence, the poor thermal performance for S1 and CR1 can be attributed to the maldistribution of the flow, what reduced the microchannel heat sink effectiveness. The dimensionless fin length is also plotted in Fig. 4-32 based on a flowrate of 200 ml/min. Using correlations from Lee et al. [2006], fully developed thermal conditions prevails for x^+ greater than 0.038. We can see that for CR2, developing thermal conditions formed a substantial portion of the flow length along all the channels. For S1 and CR1, fully developed condition is significant for the channels at the edges. This will have an impact on the average heat transfer coefficients along the channels. However, in spite of these disadvantages, the microchannel area had enhanced the heat transfer through the base area greatly, with 75% to 80% of the flow going through it, while the rest are convected through the prime area. About 5% of the total heat passed through the edges of the package. From this analysis, CR2 will be chosen for further investigation with a design flowrate of 200 ml/min.

The effect of flowrates on the flow distribution is analysed next for CR2. For the three flowrates of 100, 200 and 300ml/min, the flow distribution curve is the same except for the first and last few channels (**Fig. 4-34**). The effect of an increase in the flowrate on the flow distribution is hence a scaling factor to the average velocities within the channels.

Figure 4-34 Effects of total flowrate on flow distribution in CR2

4.4.3 Thermal aspects of carrier fabrication process

Deep channels with narrow spacing are desirable as the effectiveness of the microchannel heatsink is increased. However, they require much thicker wafer than the channel depth, and it is difficult to form Through-Silicon-Via (TSV) in the thicker wafers. 200 mm (8") wafer of 400 μm thickness is acceptable for the TSV interconnection and micro-channel etching for this work.

Figure 4-35 Cross section of microchannels etched on carrier

Deep channels of depth 350 μm etched on a wafer weaken mechanical strength and pose difficulties in handling the wafers. Due to thin wafer handling, an alternative process is used to achieve the desired channel depth of 350 μm . Two carrier wafers with channel depth of 170 μm has been fabricated and bonded together. The wafers are bonded using 5 μm thick AuSn solder on each side. This increased the microchannel heat sink base thickness to 230 μm . A significant change from the original design is the introduction of the interfacial gap of 10 μm as shown in Fig. 4-35.

Numerical modeling of a microchannel heat sink alone without the solderballs and die was performed. This treatment is to enable more meshes to be used to model the flow and temperature field in the gaps. A quarter-model was used, due to symmetry. A constant heat flux boundary condition (100 W/cm^2) was used as the heating source from the die. The interfacial gap between the fins is 10 μm .

Figure 4-36 Geometry of Split and continuous fins

In order to understand the implication of such a fabrication process, the heat flow path from source to outlet is analysed. A hydraulic modelling showed that there is very little cross flow over from one channel to another due to the small velocity vectors. Hence, the space created by the gap can be treated as being filled with a solid medium having a conductivity of water as a simplification to reduce the mesh used. Looking at Fig. 4-36, the heat path showed how the heat moved from source to the water. From the source, where 25 W is generated, a very small percentage goes to the periphery. The rest goes to the finned and primed area, with the prime area dissipating 4.4 W. The rest of the heat is being transferred along the fins. However, because of the reduction in channel height,

the tip of the half fin has a convective boundary condition. At this point, 65% of the total heat that had entered through the base into the fins had already been convected out through the sides. The rest of the heat is transferred to the lower half of the channels to be picked up by the water through the sides. Comparing this to a microchannel heat sink without the gap, the maximum temperature of the heat sink surface had increased from 48°C to 54°C.

Figure 4-37 Heat path of microchannel heatsink having a gap (left) without a gap (right)

Using the simplification earlier, whereby the gap is replaced by a solid material with conductivity that of water (0.63 W/m.K), a numerical model was done that included the solderballs and die (**Fig. 4-37**). The microchannel heat sink base had also increased from 100 μm to 225 μm .

Figure 4-38 Heat path of microchannel heat sink with die and solderballs

From the modelling, a thicker base had allowed about 7% more heat to be spread to the periphery (from 1 W to 2.8 W). However, the heat path remained relatively the same as before. The study had shown that the gap between the channels had a significant effect on the thermal performance of the microchannel heat sink. Using the heat sink resistance as a comparison, with the fluid inlet temperature as reference temperature, there is a 25% increase in resistance from 0.15 °C/W to 0.21°C/W. This increase can be attributed to the effective area of heated surface being reduced dramatically.

4.5 External heat exchanger

The heat from the package will need to be rejected to the ambient and hence, an external heat exchanger will need to be placed on top. As it is integral to the package, a size constraint of 50 mm by 50 mm is placed on the footprint. The heat exchanger design focused on design for heat duty, i.e. to reject 200 W to the ambient (25°C). The boundary conditions used in the modelling are constant temperature surface, which correspond to a coldplate or heatpipe being placed on top and a constant heat flux boundary condition, corresponding to either another liquid heat exchanger on top to bring the heat to a remote site or a large air-cooled heat sink.

Figure 4-39 Schematic of external heat exchanger design

An aluminium plate heat exchanger is designed with the dimensions chosen such that current manufacturing technology is able to fabricate (**Fig. 4-39**). A minimum thickness of 1 mm is required to ensure structural integrity during wire-cutting. The fin height chosen is 10 mm to maximise the area efficiently from a one-dimensional fin model. Channel widths are 1 mm and 0.5 mm to have a greater number of fins on the base. The length of the channels is 30 mm. Inlet and outlet to the heat exchanger is a 6 mm diameter opening. The total height of the heat exchanger is 18 mm. In the modelling, the opening is replaced by a square with equivalent hydraulic diameter.

To understand the importance of the boundary conditions and the role of the heat exchanger on the other side of the one being designed, a numerical model of the heat exchanger rejecting 200 W was done. Two channel widths of 1 mm and 0.5 mm were used for comparison. The two boundary conditions discussed earlier were used.

Figure 4-40 Temperature profile on external heat exchanger base for constant temperature and constant heat flux conditions

From Fig. 4-40, the change in mixed mean temperature for water is fixed for a given flowrate and heat load. In order to reject 200W, the inlet temperature will vary depending on the flowrate and effectiveness of the heat exchanger. In both boundary conditions, the heat exchanger with the smaller channel width performed better, with a heatsink resistance of $0.0404^{\circ}\text{C}/\text{W}$ for a constant temperature of 47°C . Using the constant heat flux boundary condition, the

resistance is found to be $0.0496^{\circ}\text{C}/\text{W}$. However, if we were to take the air-side into consideration, to reject 200W to the ambient at 25°C would require that the resistances on that side to be $(40^{\circ}\text{C} - 15^{\circ}\text{C} / 200\text{W})$ $0.075^{\circ}\text{C}/\text{W}$. This posed a very serious concern on the air-side of the heat exchanger as the choice of air-cooling technologies maybe limited due to the smaller thermal resistances required.

4.6 System level modelling

A system level modelling of the cooling system has some advantages in the design phase. Firstly, the micropump selection can be done by inputting the head/flow curve into the system to obtain the modelling operating points. Secondly, it allows the components to interface together and detect any significant deviation across the boundaries. Lastly, it is able to identify which components are not performing to its expected behavior. This is very important as individual component modelling often assumed that the other components within the loop are functioning as expected.

An important concept in system modelling is length scales. In the microchannel heat sink, heat transfer and skin friction occurs across the boundary layers which are much smaller than the channel dimensions of $100\text{ }\mu\text{m}$ by $350\text{ }\mu\text{m}$. For the heat exchanger, it is mainly across the channels measuring 1 mm by 10 mm . To effectively represent all such details in a single system model is computationally inefficient and a waste of computing resources. Hence, the use of compact modelling methodologies is useful to reduce the modeling effect.

Another important consideration in the system modelling is the flow passages within the adapter. However, to model intersecting cylindrical volumes in ICEPAK posed serious problems in mesh quality. Hence, a simplification is used whereby the cylindrical passages are replaced by square passages having equivalent cross sectional area. This is valid since the pressure drop is strongly dominated by minor losses due to the bends, expansions and contractions and loss coefficients are based on area ratio.

4.6.1 Package Compact Modelling

Figure 4-41 Compact model of single carrier

The microchannels within the carrier play a very important role in the transport phenomena of mass and energy. To derive a compact model for the package, the 3D resistance in ICEPAK is used (**Fig. 4-41**). Since the fin length in the detailed layout is not a constant, the array of fins is divided into three segments. Each segment consists of a pseudo-fluid with an effective conductivity, linear and quadratic loss coefficients to model the heat transfer and pressure drop. Because the available flow area is reduced, the velocity and temperature profiles are altered. Hence, they need to be corrected by introducing an effective conductivity, loss coefficients and area ratio. The effective conductivity is specified such that the heat path through the pseudo-fluid blocks is the same as in the detailed modeling. The linear loss coefficients is used to model the linear dependence of frictional losses in laminar flow on velocity and the quadratic term is to account for the developing effects and minor losses within the microchannels.

An estimate of the loss coefficients can be made by considering the Poiseuille number and $K(\infty)$ for channels having a 100 μm : 350 μm aspect ratio ($Po = f.Re = 26$ and $K(\infty) = 2.538$). The values are adjusted such that the error in pressure drop is 5%. The final values are 25, 25, 28 m/s and 8, 5, 4 for the linear and

quadratic loss coefficients, respectively. For the effective conductivity, they are 35, 20, 15 W/m.K. The heat transfer through the top and the pressure drop across the 3D resistance blocks between the detailed and compact model are compared in Figs. 4-42 and 4-43. The figures showed that the compact model had captured the pressure drop and heat flow path within the package well.

Comparison of heat flow through individual resistance block

Figure 4-42 Comparison of heat transfer in detailed and compact models

Comparison of pressure drop between detailed and compact models

Figure 4-43 Comparison of pressure drop across carrier for detailed and compact models

5 EXPERIMENTAL SETUP

Before the experiments began, the operating conditions of the system are determined. This is useful for error analysis and calibration of instruments.

- Flowrate: $200 \text{ mL/min} < G_{\text{system}} < 420 \text{ mL/min}$
- Pressure: $0.5 \text{ bar} < dP_{\text{system}} < 1 \text{ bar}$
- Maximum temperature on chip : 100°C
- Maximum liquid temperature rise in carrier : 14°C
- Minimum liquid temperature rise in coldplate : 1.5°C

5.1 Experimental Instrumentation

5.1.1 Die surface temperature measurement

The thermal test chip incorporates the temperature sensing diodes and heating resistors. The diodes are characterised according to JEDEC standards JESD51-1 “Integrated Circuits Thermal Measurement Method – Electrical Test Method (Single Semiconductor Device)”. The calibration is done in a constant temperature oven over the range of temperature ($40\text{-}100^{\circ}\text{C}$) in 15°C increments. The K factor is obtained by plotting the temperature scale against the temperature sensing parameter (TSP) which is the voltage output of the diode and is given by the gradient of the straight line joining all the points. The voltage from the diode was measured using a Keithley Sourcemeter 2400. The uncertainty is 0.012% of reading and 1.5 mV. From this, an error band can be constructed to estimate the uncertainty in voltage readings (**Fig. 5-1**).

5.1.2 Fluid and surface temperature measurements

The thermocouples used in the experiments are type “K” 30AWG thermocouple wires. Ten wires are calibrated with a thermal calibration machine, ThermalCal (**Fig. 5-2**) in two different ranges, five wires from 30-55°C and the other five from 45-70°C. Calibrating the wires in the lower range is for used on the coldplate surface temperature measurements while the rest are for measuring fluidic and heat exchanger surface temperature. Data logging is done through an Agilent 34970A data logger. The total uncertainty in temperature measurement is $\pm 1.5^{\circ}\text{C}$ ($\pm 1^{\circ}\text{C}$ for instrument and $\pm 0.5^{\circ}$ for type K 30 AWG thermocouple).

Figure 5-2 ThermalCal used in thermocouple calibration

The calibration procedures are as follows: First, the thermocouples were connected to the data logger. Next, the source's temperature was adjusted to desired reading. When steady state temperature is reached, the thermocouples were inserted into the hole. The readout was recorded for five consecutive readings and averaged. The procedures were repeated for other source's temperatures. A linear plot of the thermocouple reading against the source reading was constructed to obtain the gain and offset (**Fig. 5-3**).

Figure 5-3 Thermocouple Calibration line showing gain and offset

5.1.3 Power Measurement

The power supply to the board is from a Xantrex XHR 150-7 DC supply (**Fig. 5-4**). It has a range of 150V and 7A. The uncertainty in voltage measurement is 1%

of full scale and in current is 1.15% of full scale. Hence, the total uncertainty in power measurement is 1.56%.

Figure 5-4 Power supply used in experiments

5.1.4 Pressure measurement

For pressure drop, the readings are taken by a differential pressure transducer from Endress and Hauser PMD235 in the range of 0-500mbar and 0-7bar. The 0-7bar transducer was calibrated in the range of 100mbar to 2 bar using a dead weight tester (**Fig. 5-5**). From 100-600mbar, the interval is 50mbar increment while from 600mbar-2bar, the increment is 100mbar.

Figure 5-5 Dead weight tester (Left) Dead weight resting on piston (Right)

The steps involved in calibration are as follows. First, the pressure transducer was connected to the dead weight tester through flexible tubing. The knob was adjusted such that the piston is floating and rotating freely. The dead weight was

then placed on the piston and rotated. The readout from the transducer was recorded. The steps were repeated for the rest of the points. A linear plot of the pressure of the dead weight against the transducer was constructed (**Fig. 5-6**).

The instrumentation uncertainty from using the 0-500 mbar or 0-7 bar transducer to measure differential pressure across the package is a combination of three effects, linearity, thermal and static pressure effects. The sensor total uncertainty is the root mean square of the three effects. From the manufacturer catalog, the specifications are

- Linearity error is 0.2% of set span
- Thermal effects error is (0.2% of TD + 0.2%) of set span
- Static pressure effects is 0.2% of nominal

The set span is the range which the transducer is used for (500 mbar or 7 bar). The turn down (TD) is the ratio of the upper range limit and the set span (500 mbar/500 mbar or 16 bar/7 bar).

5.2 Experimental Procedures

5.2.1 Carrier hydraulic test procedures and setup

The schematic of the hydraulic test setup to measure the pressure drop is shown in Fig. 5-7. The single carrier/stacked carriers are inserted into the cavity in the adapter and sealing is achieved with a thin Teflon sheet. The entire assembly is then held by screws onto the PCB. The differential pressure transducer is connected between the inlet and outlet of the adapter. The flow range is within 150 to 500 ml/min at 50 ml/min interval. The experiment is repeated four times for a 98% confidence interval. The steps taken in the experiment were as follows. The PCB is tilted at a small angle. The adapter and carriers was filled up with DI water and bubbles were allowed to escape to the outlet. The knob on the rotameter was adjusted to desired flowrate. The pressure drop was recorded when the flowrate is steady.

Figure 5-7 Schematic of carriers with adapter showing pressure drop measurements

The uncertainty associated with the pressure measurement consists of two parts. The first is that of the instrumentation uncertainty and the second is that of the repeatability uncertainty between tests for one sample. As only one carrier was used, the uncertainty from multiple samples cannot be determined. The resultant uncertainty is the root mean square of all the uncertainties involved. The calculation of the uncertainty involved determining the type of transducer range

needed to be used at the tested flowrate. The 0-500 mbar transducer was used to measure the adapter pressure drop and the lower flow range for the single and stacked carriers. The 0-7 bar transducer was used for values higher than 500 mbar.

Table 5-1 Maximum uncertainty from pressure drop measurements

Component	Instrument uncertainty (%)	Repeatability uncertainty (%)	Overall uncertainty (%)
Adapter	5.92	0.64	6.0
Single carrier with adapter	22.46	1.00	22.5
Stacked Carriers with adapter	8.79	1.98	9.0

5.2.2 Carrier thermal setup and test procedures

The experimental setup to determine the thermal characteristics of the carrier is shown below (**Fig. 5-8**). Single and stacked carriers were tested. For the stacked carrier, only the bottom die is powered up. The die is powered from 40 W to 100 W. The water inlet and outlet temperatures were measured to quantify the energy balance. To compare between the modelling and experimental results, the temperature difference between the diode and the inlet temperature is used. The flowrate used is 400 ml/min. For thermal resistance calculation, the arithmetic mean of the temperatures on the diodes is used to represent the average surface temperature.

Two different methods were used to determine the temperature rise on the die for the stacked package. The first method involved a single carrier mounted on the PCB and only half the flowrate (200 ml/min) was passed through into the carrier. Heat input was from 40 W/cm² to 100 W/cm². The testboard used in this method is A5. The second method involved two carriers stacked but with the lower carrier powered. Temperatures on both dies were recorded. The testboard used is A3.

Figure 5-8 Test setup for thermal characterization of carriers

The uncertainty from measuring the average temperature rise of diodes over the inlet temperature is from 3% to 8%. For the calculation of the overall thermal resistance, the uncertainty is from 7% to 12%.

5.2.3 Heat exchanger testing

In order to determine the effectiveness and efficiency of the heat exchanger, a coldplate is used simultaneously during the experiment to receive the heat rejected by the heat exchanger. It is made from copper with a single inlet and outlet with six passes (**Fig. 5-9**). The liquid flowrate in the coldplate is very high (50 ml/s), and hence will not be dominating the overall thermal resistance. A thermal interface material (TIM) from Thermalloy is used as the bonding material. The thermal conductivity is 0.7 W/m.K. Electrical power is supplied to strip heaters to provide heating.

Figure 5-9 Coldplate used in the heat exchanger experiment

A total of eight thermocouple wires were used in the experiments, with six measuring surface temperatures and two measuring fluidic temperatures. Four thermocouples (T/C 1-4) were mounted on the coldplate and 2 were mounted on the heat exchanger (T/C 5 and 6) as shown in Fig 80. The inlet and outlet temperatures were measured by T/C 7 and 8. The purpose of mounting thermocouples separately on the coldplate and heat exchanger was to determine the interface resistance due to the TIM. Because the actual heat transfer surface is inaccessible to sensor contact, surface temperatures are measured round the periphery for the coldplate and near to the inlet (T/C 6) and outlet (T/C 5) for the heat exchanger. Due to the high conductivity of copper and aluminium, the temperature variation is not expected to be high. Surface temperature is measured by inserting the thermocouple bead into a shallow cavity drilled on the surface (**Fig. 5-10**). The cavity is filled with a conductive epoxy paste ($k = 2.3 \text{ W/m.K}$) and the thermocouple is held in position by applying a layer of bonding material with low thermal conductivity.

Figure 5-10 Diagram of thermocouple mounting on surface

The schematic of the experiment is shown in Fig. 5-11 and the experiment is done in a closed loop. The reservoir is used to fill up the tubing and heat exchanger and removed when the space is filled up. A clamp with a force gage is used to hold the heat exchanger to the coldplate tightly with a contact pressure of 200 kPa. The thermocouples were attached to a data logger for temperature logging. In the experiment, temperature measurements for the coldplate inlet and outlet temperatures were not measured. This is because of the low temperature rise (1°C) which made measurements difficult due to sensor accuracy. Before the experiment commenced, the water inlet temperature is measured and found to 27°C .

Figure 5-11 Schematic of heat exchanger experiment

Based on the system modelling, the flow range is expected to be between 400 ml/min to 500 ml/min to dissipate 200 W from the stacked module. Hence, the heat exchanger characterisation is based on three design flow rates, 300, 400 and 500 ml/min.

5.2.4 Miniature pump testing procedures

Figure 5-12 Schematic of micropump testing setup

A schematic of the testing setup to determine the pump characteristics is shown in Fig. 5-12. The testing procedures involved operating the pump four times from wide open to shut down and vice versa for each rotating speed. The average of the heads obtained at each flow point for all four tests is used to draw a smooth curve to represent the head/flow curve. For P1, the variable speed change is through the use of a potentiometer. The rotating speed is obtained by measuring the frequency of a 0-5 V square wave on an oscilloscope. For P2, the voltage can be varied to adjust the head flow curve up to a maximum of 7.2 V.

5.3 Uncertainty estimation

The estimation of the uncertainties of the derived quantities such as thermal resistance, effectiveness and overall heat transfer coefficient of heat exchanger are discussed in this section. The methodology to derive the uncertainty is shown for a single data point and similar approach is used for the rest of the data collected.

5.3.1 Thermal resistance of package

The thermal resistance, R_{th} of a package is defined in equation 5.1 as

$$R_{th} = (T_{avg} - T_{in}) / Q \quad [5.1]$$

$$Q = I \times V \quad [5.2]$$

where T_{avg} is the average surface temperature, T_{in} is the fluid inlet temperature, Q is the power dissipated, I is the current supplied and V is the voltage supplied. The thermal resistance for board A5 at 100 W with water flow in at 200 mL/min is used as a sample calculation. Similar approach is also used for estimating the interconnect resistance.

$$T_{avg} = 100.6 \pm 0.83^\circ \text{C}, T_{in} = 39.3 \pm 1.5^\circ \text{C}$$

$$T_{avg} - T_{in} = 100.6 - 39.3 \pm (0.83 + 1.5) = 61.3 \pm 2.33^\circ \text{C}$$

$$I = 1.33 \pm 0.08 \text{A}$$

$$V = 32.1 \pm 1.6 \text{V}$$

$$\frac{\delta(R_{th})}{R_{th}} = \sqrt{\left(\frac{\delta(T_{avg} - T_{in})}{T_{avg} - T_{in}}\right)^2 + \left(\frac{\delta I}{I}\right)^2 + \left(\frac{\delta V}{V}\right)^2} = \sqrt{\left(\frac{2.33}{61.3}\right)^2 + \left(\frac{0.08}{1.33}\right)^2 + \left(\frac{1.6}{32.1}\right)^2} = 7\%$$

$$R_{th} = 0.61 \pm 0.045^\circ \text{C} / \text{W}$$

5.3.2 Effectiveness and Overall heat transfer coefficient of heat exchanger

The effectiveness ε , of a heat exchanger is defined as in equation 5.3 as

$$\varepsilon = (T_7 - T_8) / (T_7 - T_{b,avg}) \quad [5.3]$$

where T_7 and T_8 are the liquid temperature to the inlet and outlet of the heat exchanger, respectively and $T_{b,avg}$ is the average base temperature in contact with the thermal interface material. The effectiveness of the heat exchanger at 300 mL/min is used as a sample calculation.

$$\varepsilon = (T_7 - T_8) / (T_7 - T_{b,avg})$$

$$T_7 = 57.8 \pm 1.5^\circ \text{C}, T_8 = 49.7 \pm 1.5^\circ \text{C}, T_5 = 44.0 \pm 1.5^\circ \text{C}, T_6 = 40.5 \pm 1.5^\circ \text{C}$$

$$T_{b,avg} = 0.5(T_5 + T_6) = 42.3 \pm 1.5^\circ \text{C}$$

$$T_7 - T_8 = (57.8 - 49.7) \pm (1.5 + 1.5)^\circ \text{C} = 8.1 \pm 3^\circ \text{C}$$

$$T_7 - T_{b,avg} = (57.8 - 42.3) \pm (1.5 + 1.5)^\circ \text{C} = 15.5 \pm 3^\circ \text{C}$$

$$\frac{\delta \varepsilon}{\varepsilon} = \sqrt{\left(\frac{\delta(T_7 - T_8)}{T_7 - T_8} \right)^2 + \left(\frac{\delta(T_7 - T_{b,avg})}{T_7 - T_{b,avg}} \right)^2} = \sqrt{\left(\frac{3}{8.1} \right)^2 + \left(\frac{3}{15.5} \right)^2} = 41\%$$

$$\varepsilon = 0.52 \pm 0.21$$

The overall heat transfer coefficient U is defined as in equation 5.4

$$U = Q / (\text{LMTD} \times A) \quad [5.4]$$

where A is the area which the overall heat transfer is based on, Q is the power dissipated and LMTD is the logarithmic mean temperature difference given in equation 5.5.

$$\text{LMTD} = [(T_7 - T_6) - (T_8 - T_5)] / \ln[(T_7 - T_6) / (T_8 - T_5)] \quad [5.5]$$

Defining the temperature differences dT_{in} and dT_{out} as in equations 5.6 and 5.7,

$$dT_{in} = T_7 - T_6 \quad [5.6]$$

$$dT_{out} = T_8 - T_5 \quad [5.7]$$

the LMTD can be represented in another form as in equation 5.8

$$\text{LMTD} = [dT_{in} - dT_{out}] / [\ln(dT_{in}) - \ln(dT_{out})] \quad [5.8]$$

$$dT_{in} = 57.8 - 44.0 \pm (1.5 + 1.5)^\circ \text{C} = 13.8 \pm 3^\circ \text{C}$$

$$dT_{out} = 49.7 - 40.5 \pm (1.5 + 1.5)^\circ \text{C} = 9.2 \pm 3^\circ \text{C}$$

$$\partial(\text{LMTD}) = \sqrt{\left(\frac{\partial(\text{LMTD})}{\partial(dT_{in})} \times \delta(dT_{in}) \right)^2 + \left(\frac{\partial(\text{LMTD})}{\partial(dT_{out})} \delta(dT_{out}) \right)^2}$$

$$\frac{\partial(\text{LMTD})}{\partial(dT_{in})} = \frac{1}{[\ln(dT_{in}) - \ln(dT_{out})]} - \frac{[dT_{in} - dT_{out}]}{dT_{in} [\ln(dT_{in}) - \ln(dT_{out})]^2}$$

$$\frac{\partial(\text{LMTD})}{\partial(dT_{out})} = \frac{-1}{[\ln(dT_{in}) - \ln(dT_{out})]} + \frac{[dT_{in} - dT_{out}]}{dT_{out} [\ln(dT_{in}) - \ln(dT_{out})]^2}$$

$$\frac{\partial(\text{LMTD})}{\partial(dT_{\text{out}})} = 0.438, \quad \frac{\partial(\text{LMTD})}{\partial(dT_{\text{out}})} = 0.575$$

$$\partial(\text{LMTD}) = \sqrt{\left(\frac{\partial(\text{LMTD})}{\partial(dT_{\text{in}})} \times \delta(dT_{\text{in}})\right)^2 + \left(\frac{\partial(\text{LMTD})}{\partial(dT_{\text{out}})} \times \delta(dT_{\text{out}})\right)^2}$$

$$\partial(\text{LMTD}) = \sqrt{(0.438 \times 3)^2 + (0.575 \times 3)^2} = 2.16^\circ \text{C}$$

$$\text{LMTD} = 11.34 \pm 2.16^\circ \text{C}, Q = 200 \pm 3.12 \text{ W}$$

$$\frac{\delta(\text{UA})}{\text{UA}} = \sqrt{\left(\frac{\partial(\text{LMTD})}{\text{LMTD}}\right)^2 + \left(\frac{\partial Q}{Q}\right)^2} = \sqrt{\left(\frac{2.16}{11.34}\right)^2 + \left(\frac{3.12}{200}\right)^2} = 0.19$$

$$\text{UA} = 17.63 \pm 3.35 \text{ W / K}$$

$$U = 7052 \pm 1340 \text{ W / m}^2 \cdot \text{K}$$

6 RESULTS AND DISCUSSION

This section of the report focuses on the thermal and hydraulic experiments performed on individual components within the cooling system and as an integrated system.

6.1 Results

6.1.1 Carrier hydraulic characterisation

The system demand curve comprises head losses from (a) Stacked carriers (b) Adapter and (c) Heat exchanger. Losses within tubes and fittings are small and ignored due to the lower velocities within the tubing. An experiment was done to characterise the carriers and adapter together to obtain the system's demand curve.

Figure 6-1 Experimental results of pressure drop across adapter and carriers

The system demand curve appears parabolic (**Fig. 6-1**). This shows that the losses within the system are dominated by minor losses within the adapter, and

the inertia losses within the microchannels. The system demand curve consists of two major components, the adapter and the carriers. The losses from the adapter were experimentally determined to estimate its proportion in the overall system demand curve.

Figure 6-2 Schematic of experimental setup to measure adapter losses

The adapter is connected to the test rig and immersed deep in a large beaker of water (**Fig. 6-2**). The flow network for such an arrangement is shown in Fig. 6-3. In such a setup, two additional losses were introduced; they are the sudden expansion from the openings to the carrier inlets ($R_{\text{expansion}}$) and the sudden contraction at the openings to the inlet to the carriers ($R_{\text{contraction}}$) which do not exist when the adapter is used with the carriers. By immersing the adapter deep in the large beaker, the free surface can be used as a reference point so that these losses can be accounted for by using loss coefficients from handbooks. The pressure recovery at the adapter outlet can also be estimated. The other losses (R_1 to R_4) represent the flow turning, expansion and constriction within the adapter.

Figure 6-3 Flow network diagram of experimental network

Figure 6-4 Pressure drop variation in adapter

The adapter losses can be estimated by equation 6.1:

$$\begin{aligned} \text{Adapter losses} &= dP_{\text{adapter 1}} + dP_{\text{adapter 2}} \\ &= \text{Measured } dP + \text{Pressure recovery} - dP_{\text{expansion}} - dP_{\text{contraction}} \end{aligned} \quad [6.1]$$

Values of loss coefficients for expansion and contractions for different area ratio can be found in handbooks [Idelchik]. In the experiment, the area ratio is zero as the beaker is large compared to the opening sizes. The loss coefficients for expansion and contraction are 1 and 0.8, respectively.

Figure 6-5 Pressure drop across adapter before and after correction

Figure 6-5 shows that the additional losses contributed 15% to the overall pressure drop. Having corrected the losses from the adapter, the losses from the carrier can be estimated. In the case of the adapter with a single carrier, the losses from the carrier are about 75% of the total system losses (**Fig. 6-6**).

Figure 6-6 Proportion of carrier and adapter losses with system losses

The experimental results for the pressure drop across the carrier are compared with the modelling results. In all cases, the modelling over-predicted the carrier losses by 74 to 82%.

Figure 6-7 Comparison between modelling and experiment pressure drop

6.1.2 Interconnect thermal characterisation

In the thermal resistance network, the resistance of the interconnects were found to be a significant portion of the overall thermal resistance. An experiment was done to characterise this resistance. A test die (10 mm by 10 mm) was bumped on a large substrate (22 by 22 by 0.75 mm³) and placed centrally. The assembly is then mounted onto a cold plate and a thin layer of thermal interface material is applied in between. On the test die, the diode temperatures measured were in the middle, left and right locations. The cold plate surface and plate top surface temperature were also measured using thermocouples. The location of the thermocouple on the plate top surface is far away from the heated area located 3 mm from the edges (**Fig. 6-8**).

Figure 6-8 Schematic of setup used to determine interconnect resistance

A numerical model was used to obtain surface average temperatures to calculate the resistances. The numerical model was first calibrated to simulate actual testing conditions. As the TIM thickness is unknown, the numerical model had to be solved iteratively by comparing the temperature measured by the thermocouple and in the model. The ambient temperature was chosen to be the coldplate surface temperature. A “ h_{eff} ” value derived from the material resistance of the TIM is used as the boundary condition for the bottom surface of the plate. The bondline thickness of the TIM is found to vary between 45 μm to 50 μm with errors of less than 5% in the measured temperature within the range of testing power from 60 W to 85 W. The reference temperature used here is the coldplate surface temperature. The uneven TIM layer is represented by 2 “ h_{eff} ” values, 15555 $\text{W}/\text{m}^2\cdot\text{K}$ and 14000 $\text{W}/\text{m}^2\cdot\text{K}$ for 45 μm and 50 μm , respectively.

Figure 6-9 Numerical model of experimental setup

To compare the experiments and modeling results, the temperature difference between those recorded by the diodes and the average surface temperature on the carrier beneath the die is used. Figures 6-10, 6-11 and 6-12 showed that the temperature differences measured experimentally had errors of 2% to 24% for the middle diode, -12% to 5.6% for the left diode, while that of the right diode is between -17% to -7% compared to those obtained numerically.

Figure 6-10 Comparison of temperature rise of middle diode in model and experiment

Figure 6-11 Comparison of temperature rise of left diode in model and experiment

Figure 6-12 Comparison of temperature rise of right diode in model and experiment

For resistance calculations, the numerical model uses the average surface temperatures between the die and carrier surface for the temperature differences. In the experiments, the arithmetic mean of the diodes' temperature is used. The error in the estimation of the resistances in the experiment is from 4% to 8%. A straight line was fitted to both the numerical and experimental interconnect thermal resistances. A lower regression coefficient of 0.8423 was obtained for the experimental results.

Figure 6-13 Temperature rise across interconnect layer with power

6.1.3 Carrier thermal characterisation

Figure 6-14 shows the average temperature rise from inlet on the die from 40 W/cm² to 100 W/cm². The diodes readings are given in the appendix.

Figure 6-14 Temperature rise on die for different powers

Figure 6-15 Total thermal resistance for carriers

From the data of thermal resistance generated for A3 and A5, the average total thermal resistance was experimentally found to be $0.596 \pm 7\%$ °C/W and $0.557 \pm 6\%$ °C/W. The thermal resistance used for comparison is based on average temperature rise on die from inlet. Compared with the experiments, the thermal resistance is underestimated by 58% in the numerical model.

Table 6-1 Comparison of overall thermal resistance for model and experiment

	Model	Experiment	Deviation (%)
R_{th} (°C/W)	0.410	0.577	44.3

In order to show that the technology is scalable to multiple stacks, the energy balance across the carrier is analysed. The inlet and outlet temperatures across the carrier on testboard A14 were measured and tabulated for a flowrate of 400ml/min. The testboard had resistor heating on both carriers but no diode reading on the top die. The uncertainty in measuring the flowrate is $\pm 2.5\%$. The uncertainty in measuring temperature differences between inlet and outlet is between $\pm 35\%$ to 68% due to the smaller temperature differences. Hence, the uncertainty in measuring the heat gained by the water is dominated by uncertainty in temperature measurements.

Table 6-2 Energy balance across carrier (A5)

Power supply (W)	$T_{out} - T_{in}$ (°C)	Heat gain (W)
100.7	3.63	100.9
151.9	5.47	151.9
202.7	7	194.4

6.1.4 External heat exchanger characterisation

Table 6-3 shows the comparison of the modelled pressure drop with those obtained experimentally. The modelling results agreed well with the experiments with errors less than 20%. Hence, the heat exchanger offered very little flow resistance to the overall pump load and can be neglected during pump sizing.

Table 6-3 Modelling and Experimental pressure drop for heat exchanger

Flowrate (ml/min)	Pressure drop (mbar)		
	Model	Experiment	Error
300	7.3	8.1	-9.8%
400	12.6	14.1	-10.6%
500	19.4	23.8	-18.5%

From Tables 6-4 to 6-6, for all the flowrates, the surface temperatures on the heat exchanger and coldplate remained constant. This implied that the coldplate is behaving like an infinite heat sink. Looking at the heat exchanger outlet temperature, based on the coldplate's operating conditions, the heat exchanger is able to return 50°C to the carriers for cooling, which is identical to what was assumed in the modelling. Comparing the surface temperatures on the heat exchanger and coldplate, there is a significant increase in temperature of 13°C due to the TIM. This is a very large resistance in the overall thermal budget and clearly showed the disadvantage of bonding through a TIM.

Table 6-4 Heat exchanger surface, inlet/outlet temperatures in experiments

Flowrate (ml/min)	Surface temperatures		Fluid temperatures	
	Left / T ₆ (°C)	Right / T ₅ (°C)	Inlet / T ₇ (°C)	Outlet / T ₈ (°C)
300	44.2	40.8	57.8	49.7
400	44.8	41.3	56.6	50.1
500	44.2	41.0	55.1	49.7

Table 6-5 Coldplate Surface temperatures measurement

Flowrate (ml/min)	T ₁ (°C)	T ₂ (°C)	T ₃ (°C)	T ₄ (°C)
300	30.9	30.7	30.6	31.3
400	31.1	30.8	30.9	31.5
500	31.0	30.6	30.8	31.4

Table 6-6 Energy balance across heat exchanger

Flowrate (ml/min)	$T_7 - T_8$ (°C)	Heat rejected (W)	
300	8.1	168.7	89.2%
400	6.5	180.5	95.5%
500	5.4	187.5	99.2%

Next, the energy balance across the heat exchanger is analysed. The electrical power input is 150 V and 1.26 A resulting in a power of 189W to heat up the water passing through the heaters. At lower flowrates, based on the fluid temperature differences, the heat rejected by the heat exchanger is 90% of the overall heat gained in the heaters. This is due to the measurement errors from the low flowrates and temperature.

Comparison of overall heat transfer coefficient "U" between modelling and experiments

Figure 6-16 Comparison of overall heat transfer coefficient between modelling and experiments based on edge temperatures

In order to compare the experimental results with modelling, instead of a constant heat flux or constant temperature surface, a convective boundary condition is used. The choice of a convective boundary condition is to account

for the coldplate and TIM thermal resistance in the heat exchanger design, similar to the experiments done for the interconnect resistance whereby the numerical model is calibrated. Having obtained them experimentally, a heat transfer coefficient based on the heat exchanger base area (50 mm by 50 mm) can be derived from the resistance, where it is given by the logarithmic mean temperature difference (LMTD) between the cold plate inlet and outlet temperatures and the heat exchanger surface temperatures. The heat transfer coefficient is found to be $5076 \text{ W/m}^2\text{.K}$ and used in the modelling. The heat rejection is to the water inlet temperature of 27°C . From the modelling, the axial temperature profile is plotted against distance and shown in Fig 98. The peak in temperature on the edge is in the same plane as the inlet. A transverse plot of temperature is also shown to estimate the variation from the inlet to the edge, which is about 2°C .

Figure 6-17 Axial variation of temperature along edge of heat exchanger

Figure 6-18 Transverse temperature variation in heat exchanger

From these temperatures, data reduction is performed to calculate the overall heat transfer coefficient U and the ε -NTU relationship using equations 5.3 to 5.8. Comparing between the readings, the modeling is able to predict the heat transfer across the heat exchanger. The experimental errors from estimating the overall heat transfer coefficient and effectiveness are from 19 % to 21 % and 46% to 68%, respectively, due to the smaller temperature differences between the thermocouples. Looking at the ε -NTU graph (**Fig. 6-19**), the model predicted a higher effectiveness across the three design flowrates. The experimental results are also compared with a copper microchannel heat sink [Webb, 2007] at the same flowrate of 360 mL/min. The unit thermal resistances, normalised by the base footprint area, of the aluminum and copper heat sink are comparable at 125 °C.mm²/W and 64.8 °C.mm²/W, respectively, considering the effects of thermal conductivity. At the same flowrate, the effectiveness of the external heat exchanger is also lower at 0.45 compared to 0.63 for the copper heat sink.

Figure 6-19 ϵ -NTU relationship comparison between modeling and experiments

Having shown that the modelling is able to capture the flow and heat transfer characteristics inside the heat exchanger, a more detailed analysis of the thermal performance can be done. Firstly, using the edge temperatures to represent the temperature profile of the heat exchanger base is an underestimate as the hottest point on the base is at the inlet and the heat will spread to the edge. Hence, the overall heat transfer coefficient will be lower. Secondly, defining a resistance based on two points on a surface to determine the heat transfer characteristics of a surface may not be representative of the heat transport. Rather, an average temperature based on area-averaging is often a better choice. Looking at the lower flowrates (300 and 400 ml/min), the lower prediction could be due to the higher temperature variation in mixed mean temperature causing difference LMTD.

Figure 6-20 Overall heat transfer coefficient based on edge and average temperature

6.1.5 Miniature pump characterisation

An experiment was done to characterise the two pumps and compare the head flow performance with regards to the system demand curve.

Figure 6-21 Pump head/flow curve with system demand curve

Figure 6-21 shows the average head flow curve for the micropumps P1 and P2. The maximum variation of the pressure at the test points is about 6.5%. The solid lines are for P1 operating at 3000 and 3600 rpm, respectively. The dashed lines are for P2 operating at two different voltages 6 V and 7.2 V. The flow range for P2 is much larger than P1, with the 7.2 V spanning a range from 300 ml/min to 450 ml/min. The choice of micropump is determined by the operating point when the system demand curve intersects the head flow curve. The operating flowrate is then used to determine if it meets the cooling requirements. A system demand curve for the adapter and stacked carriers was used to obtain the system operating points under different pump operating conditions as shown in Table 6-7.

Table 6-7 Summary of operating points for different pump conditions in module assembly

Pump type	Operating conditions	Head (bar)	Flowrate (mL/min)
P1	3000 rpm	0.65	410
	3600 rpm	0.89	480
P2	6 V	0.58	390
	7.2 V	0.81	450

Based on the operating points, P1 is able to operate at a higher flowrate when running at 3600 rpm. Higher flowrate is also possible from this pump when the frequency is adjusted. However, this has a detrimental effect on the lifespan of the pump. In the micropump selection, footprint and height is also an important selection criterion as much as hydraulic characteristic. P2 offer this significant advantage with a height of 15 mm compared to that of P1. The flowrate obtained from this pump is also slightly lower. Hence, P2 is chosen as the micropump to be used in the integration.

The flowrates from P2 at 6 and 7.2 V were also compared with those from the system modelling. In both cases, the system modelling predicted a higher flowrate for each operating conditions, implying lower pressure drop.

Table 6-8 Comparison of flowrates between numerical model and assembly module

Voltage (V)	Flowrate, numerical (mL/min)	Flowrate, module (mL/min)
6	400	390
7.2	460	450

6.2 Discussions

From the experimental results, higher temperature rise was recorded on the die compared to the modelling results. The overall thermal resistance measured in the experiments was $0.577\text{ }^{\circ}\text{C/W}$ compared to $0.41\text{ }^{\circ}\text{C/W}$ in simulations. The overall resistance was broken down into $R_{\text{interconnects}}$ and R_{carrier} to understand the contribution of each resistance to the total.

In an experiment done to determine $R_{\text{interconnects}}$, it was found that errors resulting from non-uniform TIM below the substrate were significant and affected the experimental results. The calibration of the numerical model to match actual testing conditions was also found to affect the experimental results as well. A thermal resistance of $0.245\text{ }^{\circ}\text{C/W}$ was found experimentally compared to $0.229\text{ }^{\circ}\text{C/W}$ numerically with an absolute error of 6%. From this analysis, numerical modelling of the interconnect layer with a uniform TIM bondline thickness showed that the actual resistance is $0.207\text{ }^{\circ}\text{C/W}$.

The experimental and modeling hydraulic/thermal characteristics of the carriers are showing several discrepancies. The thermal resistance measured is $0.377\text{ }^{\circ}\text{C/W}$ compared to $0.21\text{ }^{\circ}\text{C/W}$ from modeling which represent a 44% difference. Two possible reasons can be attributed to such errors from modelling.

Firstly, lower flowrates through the upper half of the carrier increase the overall thermal resistance of the carrier. There are two possible reasons for such flow diversion. Although care was taken to remove air from the carrier in the modeling, smaller bubbles can still be trapped within the microchannels, at the upper half of the carriers. This caused blockage in the channels, increasing the

flow resistance and diverting more flow to the lower half. The next reason can be due to the decrease of the flow area in the upper half, due to the material expansion when heated. This can also have an effect on the distribution of flow within the upper and lower half. One possible way to detect such changes would be to measure the pressure drop across the module when it is thermally active. The increase in overall flow resistance manifests itself through an increase in pressure drop across the module.

The second reason for the differences in modelling and experimental results can be attributed to the flow allocation to each inlet. The deviation in flow can be due to air bubbles clogging the exit of the adapter reducing the flow area. A numerical model was done to quantify the degradation in thermal performance when such a situation arises. The half model of a carrier is used due to imbalance of flow. Due to the large number of mesh required in the modeling, the thermal resistance of the interconnects were not considered. The heating in the model is represented by a constant heat flux of 100 W/cm^2 .

Figure 6-22 Normalised pressure drop across microchannels

Figure 6-23 Temperature contours on source for different flow allocation

Figure 103 shows the pressure drop across the microchannel heatsink which is normalised by that of the symmetrical flow allocation to inlets. The plot showed the degree of flow distribution in one half of the carrier due to imbalance flow. The temperature contours on the heating source are also shown in Fig 104. The different allocation of flow to the inlets had caused considerable increase in thermal resistance of the carrier, from $0.21\text{ }^{\circ}\text{C/W}$ to $0.35\text{ }^{\circ}\text{C/W}$ in the 20%-80% imbalance case. This could have affected the thermal performances of the carrier and represented a significant thermal resistance due to the heat having to spread to the channels having more flow through it.

The assembly of the components as an integrated solution and system operation had also posed some difficulties as well. On the whole, the closed loop integrated liquid cooling solution had been demonstrated to be performing its function with steady state temperatures measured at most of the sensors on the die and was ran continuously for two hours before the micropump's seizure due to mechanical locking of the gears. The findings from the vendor showed that the tolerances on the gears were interfering with the gears meshing smoothly. The sealing between the adapter and stacked 3D silicon module also required identifying the proper sealing material and compression load. The use of a Teflon sheet with six M2.5 screws along the periphery was able to provide the necessary sealing without breaking the carriers during tightening.

The experimental results obtained in this work were compared with those of a similar fin structure obtained experimentally by other researchers. The unit thermal resistance based on inlet temperature, the pressure drop and pumping power were used as a basis of comparison at a flowrate of 200 mL/min except for the pressure drop in the second work which is at 50 mL/min. The first work [Brunsweiler, 2008] was based on a microchannel heat sink with parallel fins of 200 μm height and 100 μm thickness spaced 100 μm apart. The second work [Wei, 2007] was based on a two layered stack microchannel heat sink with channel sizes of 50 μm and 250 μm with fin thickness of 50 μm . Both had a chip area of 1 cm^2 while the current work had an area of 1.13 cm^2 .

Table 6-9 Comparison of pressure drop, unit thermal resistance and pumping power

	Pressure drop (mbar)	Pumping Power (W)	R_{th} ($^{\circ}\text{C}.\text{mm}^2/\text{W}$)
Current work	146	0.048	42
Brunschweiler	500	0.16	19
Wei	45	0.0038	12.5

The comparison showed that the pumping power is reduced by an order of magnitude in the current work compared to the first work, indicating the improvement of using a two inlets/outlets design. However, the unit thermal resistance is twice that obtained. The second work obtained lower pressure drop and unit thermal resistance through stacking two layers of microchannel heat sink. However, the area of application for this is only for single die package.

These two works compared focused on the thermal and hydraulic performance of the package. In this work, apart from these design aspects, significant work was also done to investigate ways to integrate electrical and fluidic interconnects within the same package area. The various process limitations such as thin wafer handling and discontinuity of copper in TSVs encountered may have affected the

thermal solution. However, a 3D package structure with integrated electrical and fluidic interconnects had been developed and demonstrated to be performing leak-free.

In the experimental work done, several issues arose during data collection that may affect the accuracy of the data. More work is required to understand the problems further.

Firstly, the sample size used in the experiments is very small. For the stacked modules, two samples were used in the hydraulic/thermal characterisation. For the single module testing, only one was available for hydraulic/thermal testing. In the thermal characterisation of stacked modules, although both dies had been powered up to a maximum of 100W, the lack of diode readings on the top module had prevented any useful conclusions from being made further. The repeatability tests between samples can be improved further by having more samples readily available for testing.

Secondly, large fluctuations when measuring diode's voltage were seen during active operation of the package, which may also undermine the accuracy due to averaging. The diodes reading at all five locations may not be available simultaneously due to interconnects' issues, which may affect the averaging of the surface's temperature as well.

Lastly, calibrating the numerical model to suit actual testing conditions is needed due to non-ideal testing setup. The improper application of TIM and clamping of the external heat sink-coldplate assembly may have skewed the results. This can be further improved by designing suitable fixtures to hold the testing equipments in place for more repeatable results in future.

7 CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

In this study, a methodology was developed to look at an integrated liquid cooling solution for stacked or 3-D packages. This means that the solution developed must be compatible with the process technology used in the fabrication so that design features are integral to the package rather than as an added-on component. The key findings of the study are summarised below.

Although the liquid cooling solution is based on microchannel heat transport, the approach taken in this study differs from most others. Instead of trying to maximise the heat transfer enhancement of a microchannel heatsink solely, the current approach looks at the different thermal resistances from junction to ambient, and identifies those that are dominant and hence needs to be minimised. This system level approach using thermal resistance network can offer a first order estimate of the resistances within the package and hence provide a proper balance of effort to lower these resistances identified. For the single module found in the stacked package, these comprise the resistance across the interconnects, the microchannel heat sink and the external heat exchanger unit which are of similar order of magnitudes.

In the interconnects optimization, two architectures are proposed, namely flip-chip and wirebonding. Thermal optimisation with the constraints from the functionality requirements from the package showed that the solderballs used in flip-chip interconnects are favourable for high pin density packages and die-size reduction. The use of a higher conductivity underfill material also aid in reducing the thermal resistance by providing an alternative heat path. The underfill material also minimises the coefficient of thermal expansion mismatch. A finite element analysis of the heat conduction within the solderball showed that representing the truncated sphere by a cylinder having a diameter that of the

solderball's maximum diameter is adequate with errors of 10% in estimating the thermal resistance across it. A low solderball height to pad area ratio is also found to be essential to be able to obtain lower resistances.

For the microchannel heat sink, the flow configuration with dual inlets/outlets had been shown numerically to reduce the pressure drop as the flow length is reduced significantly and lower local velocities are developed in the channels. Flow distribution within a microchannel heatsink had also been found to affect its thermal performance, particularly with the use of a reducing supply plenum. The smaller rise in mixed mean temperature and a higher average " h " in the channels for a reducing supply plenum design had resulted in enhanced thermal performance to dissipate 100 W/cm^2 with an acceptable maximum junction temperature. Based on a fluid inlet temperature of 50°C and a flowrate of 200 ml/min , the maximum junction temperature of 85°C can be achieved, resulting in a carrier thermal resistance of 0.15°C/W . The temperature variation across the die is also low at 7.84°C . The limitations in carrier fabrication had introduced a significant thermal resistance to the carrier thermal resistance, increasing it to 0.21°C/W .

The R_{th} across the heat exchanger is found to be strongly dependent on the boundary conditions imposed in order for the heat exchanger to dissipate 200 W to ambient. The R_{th} across the external heat exchanger is 0.0404°C/W for a constant temperature surface of 47° and for a constant heat flux of 8 W/cm^2 ; the R_{th} is 0.0496°C/W . Another consideration in the design of the heat exchanger is the additional thermal resistances introduced by the TIM and coldplate in the experiment.

Figure 7-1 Liquid cooling solution developed in the project

Experiments were done to characterise the thermal performance of three different configurations of the stacked modules. The configurations tested were single die on single carrier, single bottom die on two carriers and two dies on two carriers. The dies had been powered up to a maximum of 100 W/cm^2 . The results showed a higher overall thermal resistance of $0.577 \text{ }^\circ\text{C/W}$ compared to modeling of $0.41 \text{ }^\circ\text{C/W}$. The overall resistance had been broken down into R_{carrier} and $R_{\text{interconnect}}$, in the ratio 65%:35%. The possible reasons for such deviation could be due to lower flowrates flowing through the top/heated half of the carrier.

In the heat exchanger characterisation, the thermal performance required to reject 200 W to the ambient had been satisfied by the proposed design. In the experiments, the heat exchanger / TIM / coldplate assembly had been able to remove the heat efficiently and return water of 50°C for cooling the stacked module.

7.2 Recommendations

The scope of work undertaken in this project had been very challenging. Issues related to the practical implementation of single-phase liquid cooling in microchannels had been identified and resolved. The need to develop thermal solutions compatible with current semiconductor processes was also emphasised in the carrier design. Recommendations for future development are listed below.

7.2.1 Bonding of wafers

Carrier bonding to create the desired microchannel height is highly undesirable as it creates a significant thermal resistance at the interface. The requirements of wafer thinning to expose the TSV and also the electrical connectivity across the TSV for different channel depth represent an optimization problem whereby an optimal wafer thickness can be found that maximises both process and thermal needs.

7.2.2 Interfacing with external cooling devices

In order to decouple the package cooling system from the external heat rejection system, a coldplate was used to receive the heat from the heat exchanger, which requires a TIM to bond between the two entities, and an inevitable thermal resistance. For a heat load of 200W, this represented about 14°C of temperature rise above the coldplate surface temperature for a contact pressure of 200 kPa. The reduction of this thermal resistance can dramatically decrease the inlet water temperature to the carrier. This can be achieved through the use of better bonding technologies such as reactive soldering if the choice of the external cooling device is unknown. A more significant improvement can be made by integrating the coldplate into the heat exchanger such that the cold and hot streams are separated by just the finned walls in a counterflow arrangement. However, this requires that proper sealing to prevent crossflow from one channel to another and also complicated manifold designs be done.

7.2.3 Flow distribution in microchannels

Flow distribution in the microchannel heat sink array had been identified to play a very important part in its thermal performance besides choosing the optimum channel size, fin thickness and length. An analytical model for the flow distribution using a two-dimensional Navier Stokes equation can be used to derive the pressure profiles in the supply and return plenum. Lubrication theory can be used to simplify the problem. Coupled with the flow resistance network, the desired flow distribution across the microchannel arrays can be obtained with much better accuracy than the current iterative approach. Techniques such as infrared micro PIV can be used experimentally to compare the flow modeling with experimental results.

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APPENDIX

$$Q=100W$$

$$\text{Chip} = 10\text{mm} \times 10\text{mm} \times 0.6\text{mm},$$

$$\text{Solder balls} = 10\text{mm} \times 10\text{mm} \times 0.1\text{mm},$$

$$\text{Fins} = 0.05\text{mm} \times 0.4\text{mm} \times 10.6\text{mm}$$

$$\text{For silicon, } k=100 \text{ W/m.K}$$

$$\text{For solderball layer, } k_z = 3.6 \text{ W/m.K}$$

Thermophysical properties of water based on $T=52.5^\circ\text{C}$

$$\text{Pr} = 3.42, \rho = 987 \text{ kg/m}^3, C_p = 4177 \text{ J/K.kg}, k = 0.643 \text{ W/m.K}, \mu = 5.26 \times 10^{-4} \text{ N.s/m}^2$$

Thermal resistance

A thermal network can be derived based on a series of resistances from junction to carrier inlet.

$$R_{\text{total}} = R_{\text{interconnect}} + R_{\text{fin}} + R_{\text{hs base}} + R_{\text{conv}}$$

Material resistance across solder balls

$$R_{\text{interconnects}} = \frac{L}{kA} = \frac{0.0001}{3.6 \times 0.01^2} = 0.277^\circ\text{C/W}$$

Fin resistance

$$\text{Channel spacing} = 0.1\text{mm}, \text{fin length} = 0.4\text{mm}, \delta = 0.05\text{mm}$$

$$\text{Aspect ratio } \alpha = 0.1/0.4 = 0.25$$

$$D_h = \frac{4A}{2P} = \frac{4 \times 100 \times 400}{2 \times (100 + 400)} = 160 \mu\text{m}$$

$$\text{No of channels, } N_{\text{channels}} = \frac{10.5}{0.1 + 0.05} + 1 = 71$$

$$\text{No of fins, } N_{\text{fins}} = 70$$

$$\text{For a } dT = 7^\circ\text{C},$$

$$\dot{m} = \frac{Q}{C_p dT} = \frac{100}{4177.24 \times 7} = 0.00342 \text{ kg/s}$$

$$V_c = \frac{\dot{m}_c}{\rho * A} = \frac{0.00342/71}{987.118 * 0.0001 * 0.0004} = 1.22 \text{ m/s}$$

$$Re = \frac{987.118 * 1.22 * 0.00016}{0.000526} = 366.29$$

$$L_t = 0.1 * Re * Pr * D_h = 0.1 * 366.29 * 3.42 * 0.00016 = 20.04 \text{ mm} \gg 10.6 \text{ mm}$$

$$L_h = 0.075 * Re * D_h = 0.075 * 366.29 * 0.00016 = 4.395 \text{ mm}$$

Therefore, flow is thermally developing and hydrodynamically developed at end of channels. Developing region for flow is about 40%. Based on 3 sided-channel heating, constant circumferential temperature and uniform heat flux axially and fully developed laminar flow and thermally developing flow,

$$x^* = \frac{x}{Re * Pr * D_h} = \frac{0.0106}{366.29 * 3.42 * 0.00016} = 0.0528$$

$$Nu(x^*, 3) = Nu(x^*, 4) \frac{Nu_{fd}(x^*, 3)}{Nu_{fd}(x^*, 4)} = 5.6 * \frac{5.7325}{5.3365} = 6.015$$

$$h = \frac{Nu.k}{D_h} = \frac{6.015 * 0.643}{0.00016} = 24175 \text{ W/m}^2.\text{K}$$

$$m = \left(\frac{2h}{k\delta} \right)^{1/2} = \left(\frac{2 * 24175}{100 * 0.00005} \right)^{1/2} = 3109.66 \text{ m}^{-1}$$

$$L_c = L + \frac{\delta}{2} = 0.4 + \frac{0.05}{2} = 0.425 \text{ mm}$$

$$\eta_f = \frac{\tanh mL_c}{mL_c} = 65.61\%$$

$$A_f = 2 \times 0.4 \times 10.6 = 8.48 \text{ mm}^2$$

$$A_b = 0.1 \times 10.6 = 1.06 \text{ mm}^2$$

$$A_t = 70 * 8.48 + 71 * 1.06 = 668.86 \text{ mm}^2$$

$$\eta_0 = 1 - \frac{N_{fins} A_f}{A_t} (1 - \eta_f) = 0.6947$$

$$R_{t,o} = \frac{1}{\eta_0 h A_t} = 0.089 \text{ } ^\circ\text{C} / \text{W}$$

Convective resistance based on fluid inlet temperature

$$R_{\text{conv}} = \frac{1}{m C_p}$$

$$R_{\text{conv}} = \frac{1}{0.00383 * 4177.24} = 0.0699 \text{ } ^\circ\text{C/W}$$

Spreading and material resistance in heat sink base

$$a = \frac{L_{\text{chip}}}{\sqrt{\pi}} = 0.00564, \quad b = \frac{L_{\text{carrier}}}{\sqrt{\pi}} = 0.0062, \quad \tau = \frac{t}{b} = 0.0645 \quad (<0.6),$$

$$\varepsilon = \frac{a}{b} = 0.9096$$

$$\lambda_c = \pi + \frac{1}{\sqrt{\pi \varepsilon}} = 3.7618$$

$$h_{\text{ext}} = \frac{1}{R_f A_p} = \frac{1}{(0.0699 + 0.089) * 0.0106 * 0.0105} = 56543 \text{ W/m}^2.\text{K}$$

$$\text{Bi} = \frac{h_{\text{ext}} b}{k_{\text{carrier}}} = 3.505, \quad \phi_c = \frac{\tanh(\lambda_c \tau) + \lambda_c / \text{Bi}}{1 + (\lambda_c / \text{Bi}) \tanh(\lambda_c \tau)} = 1.0444$$

$$R_s = \frac{0.5(1 - \varepsilon)^{1.5} \phi_c}{k \sqrt{A_s}} = 0.01419 \text{ } ^\circ\text{C} / \text{W}$$

$$R_{\text{mat}} = \frac{L}{k A_p} = 0.03628 \text{ } ^\circ\text{C} / \text{W}$$

Junction temperature

$$R_{\text{total}} = R_{\text{int erconnect}} + R_{\text{fin}} + R_{\text{hs base}} + R_{\text{conv}} = 0.4871 \text{ } ^\circ\text{C/W}$$

$$\frac{T_j - T_{\text{out}}}{Q} = R_{\text{total}}$$

$$T_j = 0.4871 * 100 + 50 = \underline{98.71} \text{ } ^\circ\text{C}.$$

Ansys APDL file for solderball geometry and mesh

```
/filn,sball
```

```
! Parameter Section
```

```
! =====
```

```
! x1 = x-coordinate of solder ball base
```

```
! y1 = y-coordinate of solder ball base
```

```
! z1 = z-coordinate of solder ball base
```

```
! w1 = width and length of substrate
```

```
! h1 = half-height of solder ball
```

```
! h2 = height of upper substrate
```

```
! r1 = mid-span solder ball radius
```

```
! r2 = lower/upper solder ball radius
```

```
! r3 = copper land radius (future use)
```

```
! msize = 3D mesh divisions
```

```
! psize = 2D planar element size
```

```
!
```

```
x1=4.5
```

```
y1=2.5
```

```
z1=1.0
```

```
w1=5.0
h1=0.5
h2=0.8
r1=1.0
r2=sqrt(r1**2-h1**2)
r3=1.5
msize=3
psize=0.5
!
! Query user if underfill is desired
!
*ask, uf, Underfill flag [0=no;1=yes], 0
*if,uf,eq,0,then
/title, SBALL.INP: Solder Ball Macro (Without Underfill)
*else
/title, SBALL.INP: Solder Ball Macro (With Underfill)
*endif
!
/prep7
!
/pnum,mat,1
/num,1
/view,1,1,1,1
/vup,1,z
!
et,1,57
et,2,70
!
! Define x-y projection of solder ball and
! surrounding area.
```

```
!  
k,1,x1,y1  
wpave,x1,y1,0  
rect,-(.5*w1),(.5*w1),-(.5*w1),(.5*w1)  
wpro,45  
pcirc,r3  
pcirc,r2  
aovl,all  
aglua,all  
l,1,2  
l,1,3  
l,1,4  
l,1,5  
asbl,all,all  
!  
! Extrude and mesh lower substrate  
!  
eshape,2,0  
esize,psize,0,  
amesh,all  
eplo  
type,2  
mat,1  
esize,,msize  
vext,all,,,0,0,z1  
!  
! Create 5 local coordinate systems to assist in volume  
! generation stage:  
!  
! 11 - cartesian at ball base
```



```
! 12 - cylindrical at ball base
! 13 - spherical at ball center and rotated 45 degrees (rotz)
! 14 - cylindrical at ball center
! 15 - cartesian at ball center (for reflecting mesh)
!
local,11,0,x1,y1,z1
local,12,1,x1,y1,z1
local,13,2,x1,y1,(z1+h1),45,0,0,1,1,
local,14,1,x1,y1,(z1+h1)
local,15,0,x1,y1,z1+h1
/psymb,csys,1
!
! Locate coordinates for subsequent areas
! and volumes
!
numcmp,line
numcmp,kpoi
csys,12
k1=kp(r3,45,0)
k2=kp(r3,135,0)
csys,12
k3=kp(r2,45,0)
k4=kp(r2,135,0)
csys,11
k5=kp((.5*w1),(.5*w1),0)
k6=kp(-(.5*w1),(.5*w1),0)
!
! Create solder ball curved surface area
!
csys,13
```

```
*get,kpmx,kp,,num,max
k7=kpmx+1
k8=kpmx+2
k,k7,r1,0,0
k,k8,r1,90,0
a,k3,k7,k8,k4
!
! Create solder ball lower quarter volume
!
csys,11
k9=kpmx+3
k10=kpmx+4
k,k9,0,0,h1
k10=kp(0,0,0)
v,k10,k3,k4,k9,k7,k8
!
! Create underfill lower quarter volume 1
!
csys,13
k11=kpmx+5
k12=kpmx+6
k,k11,r3,0,0
k,k12,r3,90,0
a,k1,k11,k12,k2
v,k3,k1,k2,k4,k7,k11,k12,k8
!
! Create underfill lower quarter volume 2
!
csys,15
k13=kpmx+7
```

```
k14=kpmx+8
k,k13,w1/2,w1/2,0
k,k14,-w1/2,w1/2,0
v,k1,k5,k6,k2,k11,k13,k14,k12
!
! Mesh solder ball (lower quarter section)
!
esize,,msize
*get,vmx,volu,,num,max
/com, set ball material
mat,2
vmesh,vmx-2
!
! Mesh underfill (lower quarter section)
!
mat,3
vmesh,vmx-1,vmx
!
! Reflect solder ball (and underfill) in vertical
! direction.
!
csys,14
vgen,4,vmx-2,vmx,,0,90,,
csys,15
*get,vmx2,volu,,num,max
vsel,s,,,vmx-2,vmx2
vsymm,z,all
eplo
!
! Extrude and mesh upper substrate
```

```
!  
csys,0  
asel,s,loc,z,z1+(2*h1)  
mat,1  
type,2  
vext,all,,0,0,h2,,0,0,  
!  
! Check to see if underfill is present  
!  
*if,uf,eq,0,then  
vsel,s,mat,,3  
vclear,all  
vdel,all,,1  
alls  
*endif  
!  
! Cleanup non-essential entities  
!  
numm,node  
numm,kpoi  
eplot  
save  
!  
! You can now copy the solder ball (and  
! underfill) to other parts of the model.  
!
```

Diode readings for A5

Power (W)	T _{in} (°C)	CR1-T (°C)	CR1-M (°C)	CR1-R (°C)	CR1-T (°C)	Average (°C)	Error (°C)	R _{th} (°C/W)	Error (°C/W)
40.304	32.6	20.636	21.120	24.205	20.993	21.739	1.762	0.539	0.127
50.470	33.9	25.980	26.788	30.494	26.616	27.469	1.601	0.544	0.105
59.890	34.8	31.162	32.236	36.516	32.022	32.984	1.495	0.551	0.092
70.680	36.0	38.098	39.352	44.503	39.293	40.312	1.511	0.570	0.084
80.465	37.1	44.499	45.610	51.483	45.608	46.800	1.663	0.582	0.079
90.294	38.3	52.123	52.420	59.063	52.575	54.045	1.872	0.599	0.075
100.548	39.3	60.416	59.062	66.528	59.272	61.319	2.088	0.610	0.072

Diode readings for A3

Power (W)	T _{in} (°C)	CR1-B (°C)	CR1-M (°C)	CR1-R (°C)	CR1-L (°C)	Average (°C)	Error (°C)	R _{th} (°C/W)	Error (°C/W)
40.180	33.1	22.291	23.706	23.719	20.798	22.628	1.933	0.563	0.075
50.232	34.5	27.972	30.034	29.870	26.384	28.565	1.747	0.569	0.063
60.390	35.3	33.736	36.810	36.521	32.365	34.858	1.620	0.577	0.056
70.596	37.2	39.558	44.223	43.752	38.982	41.629	1.631	0.590	0.052
80.080	38.4	45.206	51.931	51.333	46.052	48.630	1.720	0.607	0.050
90.270	39.4	51.026	60.442	59.556	53.975	56.250	1.846	0.623	0.049
99.876	40.8	57.156	69.316	68.246	62.523	64.310	2.040	0.644	0.048