Development of carbon nanotubes for interconnection applications

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2009

Yung, W. K. P. (2009). Development of carbon nanotubes for interconnection applications.
Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/18692>

<https://doi.org/10.32657/10356/18692>

**NANYANG
TECHNOLOGICAL
UNIVERSITY**

DEVELOPMENT OF CARBON NANOTUBES FOR
INTERCONNECTION APPLICATIONS

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2009

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A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2009

**For my family, who offered me unconditional love and support throughout the
course of this thesis.**

Acknowledgements

It is a pleasure to thank all the wonderful people who made this thesis possible.

It is difficult to overstate my gratitude to my Ph.D. supervisor, Prof. Tay Beng Kang. His wide knowledge and his logical way of thinking have been of great value for me. His understanding, encouraging and personal guidance have provided a good basis for the present thesis.

I am deeply grateful to my supervisor, Dr. Wei Jun, for his detailed and constructive comments, and for his important support throughout this work. Throughout my thesis-writing period, he provided encouragement, sound advice, good teaching, good company, and lots of good ideas. I would have been lost without him.

I would like to express my sincere gratitude to my supervisor, Dr. Wang Zhenfeng, whose help, stimulating suggestions and encouragement helped me in all the time of research for and writing of this thesis.

I would like to thank the many people from SIMTech as well as NTU who have helped me. I am especially grateful to Ms. Neo Bee Geok, Mr. Hasman Bin Hassan, Ms. Teh Hsieh Foong, Mr. Lai Foo Khuen Steve and Mr. Mohaime Bin Mohahidin

I am indebted to my many student colleagues in SIMTech and NTU for providing a stimulating and fun environment in which to learn and grow.

Lastly, and most importantly, I wish to thank my family. To my parents, Sin Oi Ying and Yung King Wai, they bore me, raised me, supported me, taught me, and loved me. To my beloved husband, Wen Jie, all I can say is it would take another thesis to express my appreciation to you. Your patience, love and encouragement have upheld me, particularly in those many days in which I get discouraged. To them I dedicate this thesis with love.

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Abbreviations

CNTs	Carbon Nanotubes
VLSI	Very-Large-Scale Integration
3-D	Three Dimensional
HFCVD	Hot Filament Chemical Vapor Deposition
UBM	Under Bump Metallization
MMLS	Multi Metal Layer System
IC	Integrated circuit
ILD	Interlayer Dielectrics
I/O	Input/Output
SSI	Small-Scale Integration
ITRS	International Technology Roadmap for Semiconductors
Cu	Copper
Λ	Mean Free Path
J	Current Density
J_{max}	Maximum Current Density

P	Power dissipation (P)
Low-k	Low Dielectric Constant
ESD	Electrostatic Discharge
WEEE	European Union Waste Electrical, Electronic Equipment Directive (WEEE)
RoHS	Restriction of Hazardous Substances Directive
CTE	Thermal Expansion Coefficient
SWCNTs	Single Walled Carbon Nanotubes
MWCNTs	Multi Walled Carbon Nanotubes
C	Chiral Vector,
n,m	Chiral Indices
$a1,a2$	Lattice Indices
PECVD	Plasma Enhanced Chemical Vapor Deposition
R	Resistance
C	Capacitance
CMP	Chemical–Mechanical Polishing

c_g	Capacitance to Ground
c_m	Capacitance Between Adjacent Line
W_{opt}	Optimal Wire Width
c_o	Light Speed in Free Space
A_r	Aspect Ratio Of Interconnect
ρ	Resistivity of Conductor
R_oC_o	Repeaters Intrinsic RC Component
RLC	Resistance, Inductance, Capacitance (Electric Circuit)
EM	Electromigration
Sn–Pb	Tin–Lead
C–C	Carbon–Carbon
a-C	Amorphous-carbon
TEM	Transmission Electron Microscope
FCCVD	Floating Catalytically Chemical Vapor Deposition
Fe	Iron
CVD	Chemical Vapor Deposition

SEM	Scanning Electron Microscope
Ni	Nickel
RBM	Radial Breathing Mode
Cr	Chromium
Al	Aluminum
Kw	Kilowatts
FESEM	Field Emission Scanning Electron Microscope
CCVD	Catalyst Chemical Vapor Deposition

Summary

This thesis records the development of carbon nanotubes (CNTs) material, fabrication techniques and process for interconnection application in very-large-scale integration (VLSI) and flip chip interconnects. For CNT to be used as VLSI interconnect, a self assembly fabrication technique for joining individual CNT into a three dimensional (3-D) CNT network is developed using a simple two steps plasma enhanced chemical vapor deposition (PECVD). Electrical transport property of the 3-D CNT network within a polystyrene matrix was found to exhibit electron tunneling conductivity. The finding indicates that CNTs in the network are well joined with ohmic contact. A simple process for joining CNT bumps is also developed, which is applicable in the first level flip chip interconnect. In this method, the die and carrier are assembled by applying a downward force to the die and forcing the CNT bumps on die to be “inserted” into the ones on its carrier. Electrical measurement was conducted on the assembled CNT structure and was found to be of many magnitudes higher than the conductivity of silver paste. CNT VLSI on-chip interconnect and CNT flip chip first level interconnect fabrication process using the two CNT joining techniques are also proposed.

To synthesis CNTs with desired structures, investigation on the effects of different deposition conditions, catalyst and catalyst support layers on the nanotubes grown were conducted. In the first study, the effects of C_2H_2 concentration, deposition time, temperature and working pressure on non-aligned CNT growth by hot filament chemical vapor deposition (HFCVD) were investigated. It was realized that deposition temperature had the most

significant effect on CNT growth rate. An increase in film thickness suffered from reducing density in the case of increased C_2H_2 concentration, deposition time and deposition temperature. Higher working pressure led to the growth of denser and longer nanotubes.

Aligned CNT growth on varied thickness of nickel catalysts by HFCVD and PECVD is also studied. It was found that catalyst thickness has significant effects on the diameter of the nanotubes. The CNTs from PECVD are also found to be better aligned than the ones from HFCVD.

To study the effects of different catalyst supporting layers on CNT growth, CNTs were grown by HFCVD on Ni catalyst layer with Al, Cu and Cr as under-CNT-metallization layers. It was found that the level of interaction between Ni catalyst layer and under-CNT-metallization layer has significant effects on CNTs growing characteristics. With these results, a multi metal layer system (MMLS) comprising of Al/Cr/Ni on SiO₂ substrate was chosen as under bump metallization (UBM) for CNT growth in flip chip interconnect applications. It has been demonstrated that the problem of diffusion was resolved by the present of Cr layer in-between the Al and Ni layers.

In this work, the discovery of the two novel CNT joining techniques could begin as a starting point for fabricating complex CNT based VLSI and flip chip interconnections. The findings from the CNT deposition study would be useful for selection of metal and designing approach of integrating nanotubes in interconnects applications.

1 Introduction

1.1 Integrated Circuit (IC) Technology

Integrated circuit (IC) is a miniaturized electronic circuit that has been fabricated in the surface of a thin silicon substrate. The circuit within an IC consists mainly of semiconductor devices as well as passive components, such as transistors, capacitors and resistors. Depending on the designed layout of those components, flow of electricity within the circuitry can be manipulated in a plethora of various logic behaviors.

Since the invention of IC technology in 1958, it has become ubiquitous in modern consumer electronics, computers, cellular phones and almost all of the other digital appliances. The evolution of IC has also triggered a chain reaction of breakthrough in all areas of science and technology, from biotechnology to space travelling. Undeniably, our life will continue to revolutionize with the advancement in IC.

1.1.1 Very Large-Scale Integration (VLSI) on-Chip Interconnect Technology

Within an IC, on-chip interconnects serve as the pathways for distribution of signal as well as providing power to different components such as transistors and passive components.

There are 3 categories of on-chip interconnect with the hierarchy as follows:

- Local interconnects – Very short interconnects at the device level

- Semi-global interconnects – Intermediate interconnects connecting devices within a block
- Global interconnects – Long interconnects between blocks (including power, ground and clocks).

The cross-section of a hierarchical wire scaling is shown in Figure 1.1. In general, local interconnects are the shortest level of interconnect. They are used to electrically connect localized electrical features that are a few microns away, for example, connection among the gate, source and drain of a transistor. Local interconnects are also the finest interconnects within an IC, with cross-sectional dimension in sub-nanometer range. The larger semi-global interconnects are intermediate interconnects that provide transport pathways between components within the circuit blocks. At the most top circuit level, interconnects are commonly known as global interconnection, they are used to connect the different blocks of components and often route across an entire chip. In the present high-performance designs, the distance may be as far as 2 to 3 cm, which is several orders of magnitude larger than the thickness and height of the global wire.

Figure 1.1 Sample cross-section of hierarchical wire scaling.

Electrically conductive contacts link up the first level interconnects with active regions or devices through openings in the first-level dielectric layer. This high resistivity dielectric layer is usually silicon dioxide, which separates the active regions from both global and local interconnects as shown in Figure 1.1. Dielectric layers that separate one global interconnect level from another are known as interlayer dielectrics (ILD). The vertical openings in between the different levels of ILD form conductive channels that are necessary for connections between different levels in the sandwich structure. These vertical interconnects are designated as via. Modern processes often employ copper as interconnect material, which displays more ideal properties than the former aluminum wire.

1.1.2 First-Level Interconnects Technology

First level interconnection refers to the interconnections made between the circuitry within an IC chip to its packaging. Besides acting as electrically conductive paths from IC chip to its package, first level interconnects also provide several essential functions. Thermally, these interconnects are the crucial channels for dissipating heat generated from the IC. Mechanically, they provide support to the integrity of the IC chip and to prevent short circuiting.

Depending on the application, first level interconnects can be constructed with wire bonding or flip chip assembly technique as shown in Figure 1.2. The popular flip chip assembly technique was first invented in the 60s. It has the advantages of higher input/output

(I/O) pins count and higher electrical performance. Ever since higher levels of integration demands are required in IC technology, flip chip assembly technique has been adopted in an aggressive way. There are various types of flip chip interconnect materials, solder is the most commonly used one at first level interconnects for flip chip bonding.

Figure 1.2 Cross sectional view of the two types of first level interconnects. Wire bonding (left) and flip chip (right).

1.2 Challenges for Interconnect Technology

Since the development of semiconductor technology was initiated in the 60s, the IC industry has evolved at an extremely fast rate. The number of transistor per chip has increased from only a few in the first IC, namely Small-Scale Integration (SSI) [1], to tens of billions of memory transistors in the latest "Very Large-Scale Integration" (VLSI) microprocessor chip [2]. Packaging technique for modern advanced IC has also migrating from wire bonding to flip chip packaging with major increase in I/O pin density. These advancements enable new version of electronics products to equip with more functionality, faster speed, lighter and smaller than the preceding ones. However, as scaling down

continues and the complexity of circuitry on chip increases, many new challenges start to surface and hinder the progress of creating next generation of electronic devices.

1.2.1 Challenges for on-Chip Interconnect

The overall performance of an IC is affected largely by its interconnect current-carrying capacity, parasitic resistance, inductance and capacitance. Consequently interconnection has become one of the most critical limiting issues as VLSI's scaling of technology continues into deep sub-micron region. The International Technology Roadmap for Semiconductors (ITRS) [3] predicted the future requirement for on-chip interconnects as shown in Table 1.1, emphasized the need for outré fine, reliable and high-speed interconnects for future IC. While reducing the physical size of active semiconductor devices (e.g. transistors) results in faster and lower power consumption circuits, reducing the physical size of interconnects may limit VLSI's performance.

Table 1.1 ITRS prediction on the future requirements for VLSI on-chip interconnect.
The listed areas have no known solution.

Year of production	2014	2015	2016	2017	2018	2019	2020
Total interconnect length (m/cm ²) –	3571	4000	4545	5000	5555	6250	7143
$J_{\max}$ (A/cm ²) – intermediate wire (at 105 °C)	1.06E+07	1.14E+07	1.47E+07	1.54E+07	1.80E+07	2.23E+07	2.74E+07
Metal 1 wiring pitch (nm)	56	50	44	40	36	32	28
Effective resistivity (μΩ-cm) Cu intermediate wiring	5.2	5.58	6.01	6.33	6.7	7.34	8.19

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(with width dependent scattering)							
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As the physical dimension of current copper (Cu) on-chip interconnects decreases into the sub-micron region, several concerns for future development have been identified below:

1. Finite size effect for Cu – Resistivity of a metallic wire increases when its dimension is less than or equal to its mean free path (λ). The electron-surface and grain-boundary scatterings start accumulating to the intrinsic scattering from phonons, which causes the electrons scattering time to reduce [4,5]. The mean free path for Cu is ~40nm [6], hence if its feature size approaches the mesoscopic regime of below 40nm as predicted by ITRS roadmap [3], it will suffer from high resistivity. Moreover, the diffuse scattering from the interface of the metallic barrier layer, found between Cu and the dielectric will lead to an additional fundamental increase in resistivity of Cu interconnects. This increase in interconnects resistivity as shown in Figure 1.3 will increase transmission delay and thus slow down the IC's overall operating speed [6].

Figure 1.3 Scaling effect on the electrical resistivity of Cu interconnects.

2. Electromigration of Cu – Electromigration is the transport of atoms driven by an electric current. This often causes the formation of void in very fine interconnects and results in device operational failure. Metal like Cu is highly susceptible to electromigration at high current density (J) of $> 10^6 A/cm^2$ [7]. The Cu electromigration issue becomes worsen as the interconnects dimension continue to be scaled down and the requirement of current density increases inversely. As predicted by ITRS roadmap [3], from the year of 2014 onwards, the maximum current density (J_{max}) would exceed $1.06 \times 10^7 A/cm^2$. This predicted current density are far beyond the current carrying capacity of sub-micro Cu interconnect as shown

in Figure 1.4 [8,9]. Reliability of ICs would be significantly lowered if the concern of electromigration is not addressed properly.

Figure 1.4 Maximum allowable current carrying density (J_{max}) for sub-micro interconnects.

3. Limitation in physical size – It is important for local interconnects to have resistance and capacitance that are comparable to that of its driver or logic gate. In order to do so, local interconnect must be several gate pitches long to have resistance that are similar to that of its driver and with the smallest gate length in diameter for meeting the small gate capacitance [10]. Fine and higher aspect ratio wires are therefore required for local level interconnects.

The minimum physical size of local Cu wires is restricted by two factors: the limitation in fabrication process and the electromigration issue. Today, local Cu interconnects have to maintain an aspect ratio of no lower than 1.5 to prevent electromigration. Current fabrication method is also incapable to produce very fine Cu interconnect, as thickness variation is introduced during the chemical–mechanical-polishing process, causing the formation of void.

4. Joule Heating of Cu – Joule heating refers to induce heating of Cu during power dissipation in the interconnects. Power dissipation (P) at interconnection is related to the current and the resistance governed by the relation $P=I^2R$, where I denotes the current through interconnect and R refers to the interconnect resistance. Aggressive down scaling of interconnects has permitted more metal levels, an increase in current density and the use of low dielectric constant (low-k) materials with very low thermal conductivity. With those unfavorable features, joule heating from the sub-micro interconnects will cause significant increase in IC temperature. This rise in temperature will impact interconnects reliability in the following three ways: Firstly, it limits the maximum allowable current density to keep temperature in check. This limit, in turn, has also indirectly affected the scaling limit of interconnects [11]. Secondly, it deduces the life expectancy of interconnection. As interconnection's lifetime is exponentially dependent on the inverse of metal temperature [12], high operational current will shorten interconnect lifetime. Thirdly, it will be more prone to failure when subjected to short duration of high peak current. Sub-micron interconnects have lower resistance against thermally induced open-circuit metal failure, e.g. circuit conditions like electrostatic discharge (ESD) [13]. Thermal effects of Cu interconnects will fast emerge as an urgent reliability concern for future IC development.

1.2.2 Challenges for First Level Interconnect

The common challenge of today's IC design is to achieve electrical pathway for increasing speed, power and total device functionality while decreasing size. The advancement in interconnect technology has been emphasized at the wafer level. These continuous leap frog developments in wafer level technology are becoming more difficult for first level interconnect technology to keep pace with. In the near future, flip chip interconnect fabrication predicted by ITRS [3] will face challenges like decrease in I/O pitch size from 60 μm in 2004 to 20 μm beyond 2009 (ITRS prediction) [3,14], a reduction in interconnect height to less than 50 μm , and an increase in interconnects density to more than 5000 per die [15]. In line with technical limitations, the government agency has also put the pressure on industries to do away to the current lead dependent interconnection to meet green environmental standards. To address these demands, yet to maintain performance of interconnects, solder as the most popular first level interconnect material will soon be unable to satisfy the needs, as the below listed problems become ever more significant:

Electromigration is becoming the fundamental problem that limits the miniaturization of metallic interconnects. Electromigration refers to current-induced displacement of atoms taking place in conductive materials and is a serious issue for metallic interconnects [16]. This phenomenon occurs as a result of the combining effects of direct momentum exchange from the applied electric field and the moving electrons. The current induced mass transport combines with divergence in mass flux, which causes the removal of material from one site to build up material in another site. This will result in void formation in locations where atoms are removed or a short circuit in location where material is built up. To avoid

electromigration and maintain interconnects reliable, the current carrying capacity of noble metal interconnect is strictly limited to $\sim 10\text{nA/nm}^2$. With smaller dimension, resistance against electromigration for all metals is relatively lower. Thus, an even severer restriction is posed for the ever-smaller interconnects.

Lead free interconnects – Lead-content found in common solder poses various problems for interconnect application. Although the use of lead can maximizes material strength, and resistance to creep [17], the toxicity of lead [18] is not eco-friendly. Lead is identified as one of the most significant environmental health threats to humans, especially to pregnant women, infants, and children up to six years of age [19-21]. According to the European Union Waste Electrical Electronic Equipment Directive (WEEE) and Restriction of Hazardous Substances Directive (RoHS), lead had to be limited or banned from electronics product by the year of 2008. This has led to extensive studies in lead-free alternative materials for interconnects. Replacements for conventional soldering operation with silkscreen printing solder paste are now obtainable and Sn/Ag/Cu solders are widely accepted. However, the lead-free replacements to the conventional Sn60/Pb40 posted some short comings for electronic assembly. The lead-free joints produce mechanically weaker connections [22], which reduce the reliability of devices. Another reliability issue is the formation of "tin whiskers", where tiny slim crystals of tin slowly grow out of the solder joint. Over years, these tin crystals can bridge and cause short circuit.

Manufacturing of very fine pitch interconnects – Due to the increase in I/O density with the higher transistor density on-chip. The required pitch size of first level interconnect

will be limited to 20 μm beyond 2009 (ITRS prediction) [3]. The current first level interconnects are usually formed by reflowing solder into a hemispherical shape. The continuous scaling down of first level interconnects will soon cause the fabrication method to reach its limit in forming outré fine interconnects.

Mechanical strength – Connection between the bare IC chip and its package is expected to withstand temperature cycling and humidity stresses under normal operating conditions [23]. The device lifetime depends largely on the lifetime integrity of its interconnects. In today's electronic devices, the fatigue cracking of solder interconnects is usually caused by thermal expansion coefficient (CTE) mismatch among the chip, solder interconnects, and substrate during their operation with the increase in temperature (As shown in Figure 1.5). The utilization of high-lead die bump and eutectic tin/lead substrate solder joint considerably reduce the amount of thermomechanical stress transfer to the ILD layer, but is not ideal for the lead-free request from the industry. Most of the lead-free solder produces sub-standard or mechanically weaker joints than tin/lead solder, which may affect the device reliability. [22,23].

Figure 1.5 CTE mismatch of IC chip, interconnects and substrate due to temperature cycling.

Thermal reliability – One of the important roles that first level interconnects have, is to dissipate heat from the IC chip to its substrate. With the continuous increase in IC circuit

complexity, more heat will be generated on future IC. First level interconnect by solder material will face difficulty in fulfilling its duty for the thermal management. Typical solder has a thermal conductivity of $36 \text{ W/m}\times^\circ\text{K}$, which is sufficient for heat dissipation when the interconnect density is very high. However, as the physical dimension of interconnects reduces, additional source will be needed for providing heat dissipation, e.g. heatsink. This will result in an increase in overall IC packaging cost and will not be preferred.

Electrical properties – To make device smaller, lighter, and at the same time operate at higher signal speed and bandwidth, electrical parasitic is the key area to be addressed. The electrical conductivity of standard eutectic tin-lead solder only has 11.5% of copper, which is $1.72 \mu\Omega/\text{cm}$ [24]. The ever higher operation temperature of interconnects will further reduces its conductivity, causing it to become bottleneck for high speed operating device. Moreover, solder bump first level interconnects with reduced size will not be able to endure high current density and electromigration, which will soon become a big reliability problem [25].

1.3 Carbon Nanotubes

1.3.1 Introduction

In the year of 1991, a new form of carbon, namely carbon nanotubes (CNTs) was discovered from the roost residues in a fullerene synthesis experiment by Iijima [26]. This one dimensional quantum wires are in the form of graphene cylinder closed at either end with cap. At molecular level, carbon atoms are arranged in hexagonal structure (sp^2 bonded) [27] in graphene, wrapped up as nanotubes and capped with carbon atoms in pentagonal rings.

1.3.2 Types of Carbon Nanotubes

There are two main categories of CNTs, single walled CNT (SWCNT) and multi walled CNT (MWCNT). SWCNT refers to CNT comprised of single layer of graphene sheet, while MWCNT refers to CNT constituted of co-centric single walled nanotubes with different diameters. The typical length of CNTs ranges from one to tens microns, with diameter from 0.4 nm to 3 nm for SWCNT and 1 nm to 1 μm for MWCNT.

As mentioned from pervious paragraph, structures of nanotubes are cylindrical roll up graphene sheet. The rolling up direction of the graphene sheet is represented by a pair of indices (n, m) and a chiral vector, $c = na_1 + ma_2$. The indices in the chiral vector refer to the number of carbon atoms around the circumference and down the axis of the nanotubes. From this chiral vector, nanotubes can be classified into three types: If $m = 0$, nanotube belongs to the “zigzag” type, if $n = m$, nanotube belongs to the “armchair” type, and the rest is considered as “chiral” type. Figure 1.6 illustrates the graphene honeycomb lattice with the lattice indices (a_1, a_2) and chiral vector of CNTs. A $(8, 4)$ chiral tube with chiral vector $c = 8a_1 + 4a_2$ is shown with the 4 graphene lattice points represented by circles, the first and the last points coincide when the sheet is rolled up. Perpendicular to c is the tube axis z , the minimum translational period is given by the vector $a = -4a_1 + 5a_2$. The vectors c and a form a rectangle, which is the unit cell of the tube, if it is rolled along c into a cylinder. The zigzag and armchair patterns are along the chiral vector of zig-zag and armchair tubes, respectively. The rolled up “zigzag”, “armchair” and “chiral” CNTs are shown in Figure 1.7 [28].

Figure 1.6 Illustration of the chiral vector and chiral angle of a (8, 4) chiral CNT. The zigzag and armchair patterns are along the chiral vector of zig-zag and armchair tubes, respectively.

Figure 1.7 Different geometric structure of CNTs (a) chiral, (b) zigzag and (c) armchair.

1.3.3 Electrical Properties

Due to the symmetry and unique atomic structure of graphene, the electrical behavior of nanotubes is greatly affected by their chirality. Nanotube can be either 0 eV conductor or semiconductor. This can be determined using chiral vector. For example, if $2n + m = 3q$ (where $q = \text{integer}$), the nanotube is metallic, otherwise it is semiconductive. Therefore, all armchair nanotubes ($n = m$) are metallic. For zigzag and chiral nanotubes that do not satisfy $2n + m = 3q$, their bandgaps can be estimated with Equation 1.1 [29]:

$$E_{\text{gap}} = 2 \theta a_{\text{C-C}}/d \quad 1.1$$

Where E_{gap} is the bandgap, θ is the C-C tight binding energy, 2.5 eV, $a_{\text{C-C}}$ is the carbon bond length (0.142nm) and d is the diameter of the nanotube. CNTs are one-dimensional conductor. Since the electrons and holes in CNTs can only propagate forward or backward, they can neither allow angular scattering of electrons nor allow any occurrence of holes in typical conductive metal. In CNTs, limitation in phase space does not allow any electrical resistance issues caused by backscattering during the reversal of the momentum by carriers. For this reason, nanotubes are known to be ballistic conductor [30-32] as the occurrences of backscattering is not possible.

1.3.4 Thermal Properties

Thermal conductivity of CNTs changes depending largely on temperature as shown in Figure 1.8. At very low temperature, the conductivity was found to be more linear. From

temperature 25 K to 40 K, the line increases in slope and from 40K to above room temperature, the thermal conductivity arises monotonically [33]. Equation 1.2 can be used to model the temperature dependent thermal conductivity of CNTs:

$$k_{zz} = \Sigma C v_z^2 \tau \quad 1.2$$

k_{zz} is the slope of the line, C is the heat capacity, v is the sound velocity (around 1×10^6 cm/s), and τ is the relaxation time, (around 10-11 s). The calculated thermal conductivity for a single rope of CNTs at room temperature varies between 1800 - 6000 W/m-K. This unusual high thermal conductivity of CNTs (higher than diamond) is believed to be the result of its large phonon mean free paths of CNTs [34].

Figure 1.8 Thermal conductivity of CNTs vs. Temperature

1.3.5 Mechanical Properties

The mechanical properties of carbon based CNTs are closely related to the nature of the bonds between carbon atoms. The atomic number for carbon is 6, with its atomic physics notation in $1s^2 2s^2 2p^2$. When carbon atoms combine to form the graphene body of CNTs, sp^2 hybridization occurs. $1s$ -orbital and $2p$ -orbital join to form three hybrid sp^2 -orbitals at 120° to each other as shown in Figure 1.9. This in-plane σ -bond is a strong covalent bond that binds the carbon atoms in CNTs, and which explains its outé high stiffness and high mechanical strength.

Figure 1.9 Illustration of sp -hybridized sp^2 -orbitals.

1.3.6 Growth Mechanism

The CNT growth mechanism with CVD is still a subject of controversy. More than one mechanism might be operative during the growth of CNTs. In this section, an introduction of the current most agreeable hypothesis will be presented. In CVD technique, catalyst particles are believed to be necessary for CNT growth because they are often found at the tip inside the nanotubes or embedded in the middle of the tubes. The most reported catalysts are metals that are ferromagnetic and good solvents for carbon, such as Ni, Co and Fe [35-37]. These metal particles have to be present in the form of nanosized particles and are usually produced by breaking down the thin catalyst layer by thermal or chemical energy. It is suggested that carbon feedstock decomposes at high temperature on top of the metal particles on the substrate [38,39]. As the dissociation of carbon feedstock (into carbon and hydrogen) is a highly exothermic reaction, it causes a local heating effect on the catalyst particles. The carbon atoms which have been set free on the surface of the catalyst are absorbed into the catalyst and form a solid solution with the metal. The carbon then diffuses to a colder location while the hydrogen reduces the catalyst locally, resulting in a carbon gradient and a temperature gradient within the catalyst particle. When the catalyst particles become supersaturated, the carbon then precipitates out as a nanotube [40]. Whether the metal particle detaches from the substrate (tip growth) or it is remaining attached to the substrate (root growth) is explained by a weaker or stronger metal-substrate adhesion, respectively [41]. A simple diagram showing the CNT growth process is presented as Figure 1.10.

Figure 1.10 Illustration of base growth and tip growth mechanisms

1.4 Motivation

To alleviate the problems faced by interconnect technology of both on-chip and packaging level, different innovative materials are being extensively studied as replacements for copper or tin-lead solder, respectively. CNT is a newly discovered nanowire that has been foreseen as one of the most promising candidate materials for the future. Their thermal, electrical as well as mechanical properties have shown to be victorious over most of the current interconnect materials.

With their superior properties, CNTs have recently been proposed as possible candidate materials for future VLSI metal interconnects [42,43]. A comparison between CNTs to some of the most commonly used and potential VLSI interconnect materials is presented in Table 1.2.

Table 1.2 Properties of CNTs, current and potential materials for VLSI interconnects

		Current materials	Potential materials
Material Properties	Carbon nanotubes (CNTs)	Copper (Cu)	Optics fiber
Physical dimension	Self-assemble nano material 0.4nm to hundreds of nm in diameter and aspect ratio of >100	Limited by fabrication method	Limited by fabrication process, the size of transmitter (TM) , receiver (RE) and converter (CN)
Electrical Conductivity	$10^6 \sim 10^8 \Omega^{-1} \text{cm}^{-1}$ [44,45]	$588000 \Omega^{-1} \text{cm}^{-1}$ [46]	Nil
Max. current density	10^{10} A/cm^2 [37]	500 A/cm^2 [47]	Nil
Thermal Conductivity (Room temp)	1000-2000W/(m.k) [37,48]	401W/(m.k) [46]	Nil
Latency (150 Gpbs/ μm)	1.5 ns [49]	2.3ns [49]	0.3ns [49]
Disadvantages	Lack of developed technology	Scaling of size causes further increase in latency and heat Reliability problem from electromigration	Scaling of device is largely limited by the size of TM, RE and CN Extra power consumption of TM, RE and CN High heat

First level interconnect can be seen as the extension of on-chip interconnect to the outside world. For that reason, future requirements of first level interconnect are similar and closely related to that of on-chip interconnect. Reasonably, the advanced properties of CNTs will also be useful for fulfilling the future needs of first level interconnect and an excellent candidate material to be considered. Comparison between CNTs and typical solder are summarized in Table 1.3. Lead free and alternative first level materials are also included in the table.

Table 1.3 Properties of CNTs, current used and potential materials for first level interconnects

		Current materials	Potential materials		
Material	Carbon nanotubes (CNTs)	Tin -lead solder (63Sn/37Pb)	Lead - free solder (77.2Sn/20.0In/2.8Ag)	Copper bump	Gold stud
Properties					
Physical dimension	Self-assemble nano material 0.4nm to hundreds of nm in diameter and aspect ratio of >100	Limited by fabrication method	Limited by fabrication process	Limited by fabrication method	Limited by fabrication method
Electrical Conductivity	$10^6 \sim 10^8 \Omega^{-1} \text{cm}^{-1}$ [44,45]	$68500 \Omega^{-1} \text{cm}^{-1}$ [50]	$58800 \Omega^{-1} \text{cm}^{-1}$ [50]	$588000 \Omega^{-1} \text{cm}^{-1}$ [46]	$450000 \Omega^{-1} \text{cm}^{-1}$ [46]
Max. current density	10^{10} A/cm^2 [37]	4200 A/cm^2 [51]	4200 A/cm^2 [51]	5900 A/cm^2 [47]	$3.3 * 10^{12} \text{ A/cm}^2$ [52]
Thermal Conductivity (Room temp)	1000-2000W/(m.k) [48,37]	50.9 W/(m.k) [53]	53.5 W/(m.k) [53]	401 W/(m.k) [46]	318 W/(m.k) [46]
Mechanical Young's modulus	0.4 - 4.15 Tpa [54]	27 Gpa [50]	39 Gpa [50]	128 Gpa [46]	78 Gpa [46]
Tensile strength	150 Gpa [55]	31 Mpa [50]	47 Mpa [50]	220 Mpa [46]	100-200 Mpa [46]
Disadvantages	Lack of developed technology	Contain lead Reliability problem from electromigration Thermal conductivity not sufficient for thermal management of chip	Mechanical joint from lead-free is weak Tin whiskers formed will cause reliability issue Thermal conductivity not sufficient for thermal management of chip	Scaling of size causes reduced in speed and high heat Reliability problem from electromigration	Scaling of size causes reduced in speed and high heat Non cost efficient

1.5 Objectives

For using CNTs on on-chip or first level interconnect applications, CNTs have to bridge at least two terminals at low electric contact resistance. However, carbon nanostructure assembly has proven to be difficult as the pertinent size scales proscribe direct tinkering or bonding. Currently developed techniques to assemble such nanostructures include sophisticated high cost manual micromechanical methods and the CNT structural damaging chemical processing [56-60]. Although hypothetically practicable, large scale assembly of CNT-based interconnecting network with these techniques is neither easy nor ideal. Therefore, innovations in fabrication methodology and new architectures of CNTs assembly are required for advancing the widespread technological application of CNT interconnect technology. This work would be an exploratory study of using CNTs as interconnect material and with the aim to develop new techniques suitable for integrating CNTs to both on-chip or first level interconnect technology. The objectives of this project are:

1. Establish an understanding of the current development of CNT assembly techniques based on existing literature.
2. Develop assembly technique for joining individual CNT, which potentially lead to the fabrication of on-chip CNT interconnects.

3. Develop assembly technique for joining bulk CNT film, which potentially lead to the fabrication of first level CNT interconnects.
4. Characterize the electrical properties of the assembled CNT structure with newly developed techniques.
5. Identify the requirements for interconnect industry and attempt to fabricate CNTs that are suitable for interconnect applications by plasma enhanced chemical vapor deposition (PECVD) method.

1.6 Major Contribution of this Thesis

The major contribution of this thesis lies in the exploratory study of applying CNTs to on-chip and first level interconnects. This study will enable greater understanding on issues related to utilizing CNTs and their potentials in the field of interconnect technology. In addition, the proposed CNT interconnect structure and manufacture methodologies will be useful for subsequent development work in related areas. Contributions of this work are summarized as below:

1. Development of an easily adaptable methodology for self-assembly of individual CNT in network structure with no post chemical processing. - It is impractical for the industry to embrace sophisticated manual methods that are very low in yield and high in cost. Our developed method is by chemical vapor deposition, which is

high in yield and low in cost. The lack of post chemical processing of our proposed method is also simple and does not damage CNTs atomic structure. The self-assembly nature of our method also enables the formation of covalent bonded CNT junctions, which allows electrical transport with low barrier.

2. Development of an easily adaptable methodology for joining CNT bumps, which utilized typical flip chip industrial equipments - It is unrealistic for the industry to embrace a new interconnect technology that requires changing out their expansive fabrication equipments. It would be easier for them to adapt technology that enables the use of their existing facility. Our developed method consists of processes like sputtering and photolithography, which are already commonly practiced within the packaging industry.
3. Successfully fabricated CNT interconnect structures - Our developed methods have been examined and have good yield in fabricating CNT interconnects. Issues concerning these fabrication processes have been addressed and highlighted. They can be a starting point for future development of VLSI on-chip and first-level CNT interconnect fabrication.
4. Performance of the fabricated CNT interconnect structures was evaluated – Characterization of the interconnected structures has been carried out. The information will be useful for evaluations on the potential of CNT interconnect or act as a benchmark for future optimization of CNT interconnect.

5. Controllable CNT film deposition for interconnects - Different effects of the growth parameters and catalyst layers on the CNTs grown by both thermal and plasma enhanced chemical vapor deposition technique were studied. With the understanding of the effects of CNT growth environment, parameters and catalyst on CNTs, the growth conditions can be configured for depositing CNTs that are suitable for interconnect application.

1.7 Organization of the Thesis

Chapter one provides an overview of the thesis and a general background on interconnect technology as well as CNTs.

Chapter two contains an overview on CNT interconnect technology, it begins with examining the potential of CNTs for interconnect applications and follows by reviewing current methods for connecting or assembling CNTs.

Chapter three contains detailed descriptions on the CNT growth study by both thermal and plasma enhanced chemical vapor deposition technique. The effects of different parameters, such as growth conditions and catalyst, on nanotubes growth are presented and discussed.

Chapter four contains detailed descriptions on the design of an under metallization layer system, which is for CNT growth as interconnect material. The effects of such metallization

layer on the CNT structure with various growth conditions are presented. For CNTs to be used in electronics applications, CNTs would need to be deposited on top of different metallization layers. Therefore, the design of metallization layer system that has minimal effect on CNT structure and quality would be essential.

Chapter five is divided into two main areas;

1. Insertion method of CNTs with potential application in first level interconnect - This section begins with a detailed description on the methodology that was designed to join CNT bumps in between a top and a bottom substrates with flip chip bonding. The advantages and uniqueness of this fabrication process are also mentioned. This is followed by experimental details and results on the various characterization tests of the fabricated CNT interconnect structure. A proposed methodology for creating CNT on-chip interconnect by such technique is presented at the end of this section.
2. CNT self assembly technique with potential application as on-chip interconnect - This part of the chapter starts with a detailed report on the methodology that was designed to create a simulated interconnection between separated individual aligned CNTs. The advantages of this unique fabrication method and the mechanisms for the network formation have been explained and emphasized in this section. The experimental details and results on the various characterization tests of the fabricated CNT interconnect structure are reported. A proposed methodology for created CNT VLSI interconnects by such technique is presented at the end of this section.

Development of Carbon Nanotubes for Interconnection Applications

Chapter six discusses the future dissection of CNT interconnects. This chapter also offers a brief summary of the results and a conclusion for this thesis.

2 Literature Review

2.1 CNTs Current Carrying Capability and Resistance to Electromigration

High current density and electromigration, are two most critical issues that affect interconnect performance as well as reliability. Hence, a review on CNTs current carrying capability and their resistance to electromigration are provided.

CNTs have demonstrated to exhibit excellent electrical property. With their strong carbon-carbon (sp^2) bonds, CNTs are believed to endure very high current density and extremely high electromigration resistance [61-63]. They have been reported to tolerate extremely high current density from 10^6 to 2.4×10^8 A/cm² without significant damage. Wei et al. demonstrated that electron flux of $\sim 10^9$ A/cm² could be passed through a MWNT at 300 °C for a short duration without destroying it [64-68]. To determine CNTs stability under high current density, similar experiment was later repeated by the same group for a period of over two weeks (Figure 2.1). The MWNT was reported to withstand carry densities of up to 10^9 A/cm², without any measureable change in its morphology and resistance (Figure 2.2) [63]. A study on the limit of energy transport in MWNTs was showed by Collins et al. [69]. They realized that nanotubes fail via a series of sharp, equally sized current steps as presented in Figure 2.3(a). It is very different from typical metal wires, which fail in a continuous accelerating manner when subjected to electromigration. It was suggested that those steps are caused by sequential destruction of individual nanotube shells. The initiation of the failure was also suggested to be very sensitive to air exposure, as nanotubes can be oxidized at high

power ($>300 \mu\text{W}$) as shown in Figure 2.3(b). If they are kept in vacuum, CNTs are believed to reach a even higher and their full current carrying capacities.

Figure 2.1 AFM image showing two tungsten leads connected to an individual CNT.

Figure 2.2 Resistance stability of CNTs. The experiments were conducted by both two probe and four probe measurements. The current density is higher than 10^9 A/cm^2 at ambient temperature of 250°C in air. The measurements lasted about 2 weeks without any observable defects.

CNTs have also been identified as potential material to improve electromigration resistance of copper interconnects. The electromigration property of Cu/carbon nanotube (CNT) composites has been investigated by Yang et.al [70]. In their study, the Cu/CNT composite segments were subjected to a current density of 1.2×10^6 A/cm² and their failure rate was measured. It was found to be four times lower than that of the pure copper. They believed that the slower electromigration rate of the Cu/CNT composite is due to the embedded CNTs which act as trapping centers and reduce the diffusion of electro-induced migrating atoms.

From those studies, it can be seen that CNTs, particularly MWNTs (with large number of shells), are promising as reliable, nanometer-sized metallic wires and microcircuit interconnects. However, it must also be noticed that most of those studies were conducted in a very controlled environment. Thus more study with CNT properties under typical operation condition is still required to determine its actual potential as interconnects.

Figure 2.3 Time trace of the current and dissipated power during a MWNT breakdown.

(a) The current exhibits a staircase of stable currents separated by 12 mA steps. (b)

Dissipated power indicates that stable values of current (or MWNT resistance) occur only when the power is below 300 mW

2.2 Performance of Carbon Nanotubes Interconnects

CNT with its unique mechanical, electrical and thermal properties can potentially addresses many interconnection challenges when they are optimally unitized. Modern physical and circuit models of CNTs are reviewed to determine their potential performance in local, semi-local, global as well as first level interconnects. They are also compared to the current materials used.

2.2.1 Local Interconnects

Local interconnects are usually very short and have minimum wiring pitch that current technology can produce. Sub-micro local interconnects need to have comparable resistance R and capacitance C to the components they connect. Resistance is usually the dominant factor for the overall performance of interconnects with larger critical length. But for many local interconnects, the critical length has scaled down to a dimension beyond which their capacitance becomes larger than the input capacitance of a typical receiver. Figure 2.4 shows critical lengths of interconnect, beyond which resistance or capacitance becomes larger than the output resistance or input capacitance of a typical driver or receiver. The high interconnect capacitance would increase cross talk, RC delay and even higher power dissipation (CV^2f loss). Any decrease in interconnects capacitance while maintaining its driver compatible resistance can improve the performance of local interconnects. However, to reduce the local interconnects capacitance for matching that of the logic gate, the cross sectional area of local interconnects must be smaller than ten gate pitches long [71]. Short, but high aspect ratio interconnects are therefore required for local level connection.

Figure 2.4 Critical lengths beyond which interconnect resistance (upper curve) or capacitance (lower curve) becomes larger than the output resistance (upper curve) or input capacitance (lower curve) of a typical driver or receiver versus interconnect length.

As length of gate pitch scales dramatically with technology advances, aggressive reduction of local interconnects dimension has become unavoidable. Shorter local interconnects with ever higher aspect ratio and smaller sub-micro cross sectional diameter are required to meet scaling demand in electronic devices. This will soon become one of the biggest challenges for copper local interconnects. In today's processors, the physical dimension of copper interconnects has an aspect ratio no larger than 1.5, to prevent electromigration [72]. Even when electromigration can be mitigated (e.g. by deep subambient cooling), the interconnect aspect ratio is restricted by the fabrication process limitation. For example, the thickness variation in copper metallization induced during chemical-mechanical polishing (CMP) might result in void for very small local interconnects

CNTs with diameters in nanometers range can offer considerable reduction in lateral capacitance if they are used as local interconnect. The values per unit length of capacitance to ground c_g , capacitance between adjacent line c_m , average capacitance and capacitance variation of copper and CNT interconnects are calculated as shown in Table 2.1 [73]. In Table 2.1 both CNT and copper interconnects are assumed to locate above a thick dielectric layer. During switching, an interconnect can have its adjacent lines stay quiet, $c = (2 c_m + 2 c_g)$, switch in same $c = 2 c_g$ or opposite $c = (4 c_m + 2 c_g)$ direction. Hence, the average capacitance is $2 c_m + 2 c_g$. The capacitance of CNT interconnects has been calculated to be 50% less than that of copper interconnects. The dynamic delay variation $c = (4 c_m + 2 c_g)/2c_g$ caused by switching pattern of adjacent interconnects is also shown to be significantly reduced from 3.2 to 1.7 as presented in Table 2.1 For short interconnects, CNTs are also out performing copper wires in speed as shown in Figure 2.5. The speed up offered by CNT interconnects is plotted against interconnect length normalized to gate pitch of 14 nm, 18 nm and 22 nm [74]. The capacitance shows significant reduction when compared to copper interconnect with equal dimension. However, the comparison in this literature is based on metallic SWNTs bundle, which might not be practical. Till today, it is still not possible to fabricate CNTs with controlled chirality, it is therefore not possible to obtain SWNT bundle consists of metallic tubes only. So it is still questionable if CNT bundle which consisted of a mixture of semi-conducting and metallic tubes can outperform copper wire in this aspect. Another issue concerning this study is regarding the surface roughness of the nanotube interconnect. Since, it consisted of multiple tubes, rather than the case for copper wire, it is believed that the surface roughness is much higher than that of typical copper wire. As

surface roughness can increase electrostatic capacitance of an interconnect [75], the higher surface roughness of nanotube interconnect might increase its total capacitance.

Table 2.1 Capacitance value for copper wire and CNTs

	Copper Wires	Mono-layer CNTs
Capacitance to ground, c_g	35.6 aF/ μm	27.2 aF/ μm
Line-to-line capacitance, c_m	358.6 aF/ μm	9.9 aF/ μm
Average capacitance, $2c_m + 2c_g$	148.5 aF/ μm	74.5 aF/ μm
Capacitance variation, $(4c_m + 2c_g) / 2c_g$	3.16	1.73

Figure 2.5 The speed up offered by CNT interconnects versus length in gate pitch for various technology generations. [74]

CNTs have demonstrated that they are capable of carrying high current capacity of $> 10^9$ A/cm² for a period of over 2 weeks with no observable failure and degradation in electrical properties [76]. Comparing to copper, CNTs have a current carrying capacity many orders of magnitude higher than that of copper [77]. Even through a duration of 2 weeks is still far from meeting the reliability requirement for actual interconnect application, their current carrying capacity remarkably outperformed copper wire. Similar study can be conducted with a much longer duration to determine the lifetime of CNTs under such high current density. Being a self-assembled nanomaterial, CNTs by nature have diameters in nanometer range with typical length up to tens micrometers, enabling them to reach aspect ratio of >1000 easily.

There might still be doubts in applying CNT as local interconnects. Nevertheless, when considering all the favorable properties of CNTs, they are convincingly foreseen as one of the most potentially promising materials for future local interconnects.

2.2.2 Semi-Global and Global Interconnects

Semi-global interconnects are usually routed above the local level, with longer and larger cross-sectional dimension. Their delay is mainly contributed by their resistance and capacitance (RC) component. Repeaters are sometime added to improve their speed when the RC delay has become proportional to the square root of their RC product [74]. As the physical dimension of semi-global interconnects is much larger than its contact area, the total resistance is mainly determined by the material resistivity, rather than their contact resistance.

Since CNTs have lower resistivity than typical copper wires, they can be used as semi-global interconnect for reducing interconnect latency. It has been shown that the smaller the interconnect width, the better the improvement of CNT interconnects over copper interconnects as shown in Figure 2.6. This improvement applies for both cases with or without using a receiver. But such improvement does not always apply. In contrast to the inelastic scattering in Cu wires, elastic scattering occurs in CNTs. The resistance of a CNT, considering the length dependent scattering contribution is given by:

$$R = (h/4e^2) \exp(L/2l_{\text{mfp}}) \quad 2.1$$

Where $h/4e^2$ is the quantum resistance of CNT, L is the length of the nanotube and l_{mfp} is the mean free path of the electrons [3,19]. From this prediction, it is shown that the nanotube resistance will exceed the resistance of copper wire when its length is greater than $10 l_{\text{mfp}}$. It is not a problem with local interconnect which is very short in length. This also will not posted problem to the much larger global interconnect, as the total resistance of a CNT bundle is:

$$R_{\text{bundle}} = R_{\text{cnt}}/n_{\text{cnt}} \quad [75] \quad 2.2$$

With R_{cnt} is the resistance of an individual CNT and n_{cnt} is the number of CNT in the bundle. The large number of nanotubes in global interconnect could enable significant reduction in total resistance. However, for semi global interconnects, since their dimension are smaller (consist of less number of tubes) and their length is almost within the affected range (around $10 l_{\text{mfp}}$). This length dependent resistance might induce problem for using

CNT as semi-global interconnects. One solution will be to deposit smaller diameter CNT, such that more CNTs can be packed in the bundle for the required dimension and the total resistance can be reduced. It is also important to note that the perdition from this literature is based on pure metallic CNT bundle, the present of semi-conducting in actual CNT bundle would have negative effects on the conductivity of CNT as semi interconnect.

Figure 2.6 The improvement in interconnect RC delay for semi-global interconnects versus wire width.

Global interconnects has the largest physical dimension within an IC. Because of the rapid increase in clock frequency, inductance is significantly affecting wire delay and crosstalk of the multilevel global interconnects. Among these global interconnect lines, the

ones that influence the crosstalk on the other lines are termed as the aggressors, while the affected lines are referred to as the victims [78]. To prevent those issues, optimization in interconnect wire widths is important to achieve a large bandwidth density and a small latency. The optimal wire width is the bandwidth per unit width when reciprocal latency product is maximized [78], it can be defined by the Equation 2.3:

$$W_{\text{opt}} = 2.53c_0\sqrt{c_g/\epsilon_r \rho/A_r(R_oC_o)} \quad 2.3$$

Where C_o is the light speed in free space, ρ is the resistivity of conductor, A_r is the aspect ratio of interconnect, c_g is the capacitance per unit length, and R_oC_o is the repeaters intrinsic RC component. With the optimal wire width applied, interconnects can maintain to operate in the shallow Resistance, Inductance, Capacitance electric circuit (RLC) region. It also reduces crosstalk noise and improves energy dissipation without trading off too much of the bandwidth density. Scaling of copper global interconnects below the optimized width can push them into operating in the deep RLC region, which delay decreases very gradually with reducing resistance. Capitalizing on the high aspect ratio of CNTs, if they are to be used to replace the current copper interconnects, wire width can be reduced significantly and bandwidth density can be further improved without entering the deep RLC region. The optimal wire width of CNTs against copper wire is as shown in Figure 2.7, where optimal wire width reduction is proportional to the square root of resistivity. With lower resistivity, bandwidth density can also be improved without any increase in latency and crosstalk. It shows that by using MWCNT bundle as interconnect, the optimal wire width can be reduced by as much as 40% and therefore improving the bandwidth density by up to 60%. However,

this estimation from literature assumed all tubes present are metallically conductive, which is not possible in CNT growth. Therefore, it is believed that the calculation of optimal wire width would need to take this issue into consideration.

Figure 2.7 Optimal global wire width versus technology generation for copper wires and SWCNT-bundles and MWCNT-bundles. Bandwidth density is inversely proportional to the optimal wire width, and various interconnect technologies have the same delay when $W=W_{opt}$. [79]

2.2.3 Vias

In technologies beyond 50 nm, resistance from vias and their contacts would overwhelmingly dominate the interconnect resistance of other levels [80]. The intermetal-

layer distance, which determines the length of vias, does not scale as quickly as local and global level interconnects. The long vias would have much higher resistance than that of other level interconnects and it would make up most of the overall resistance. In conjunction, the local vias are also required to make connection to the first metal layer which has much smaller cross-sectional area than them. This mismatch in pitch contacts results in high contact resistance, which causes delay in operating speed and downgrades the overall device performance. Self-heating has also become one of most critical problems for the vias with small dimension and high resistance. It limits vias current carrying capacity and exacerbates their electromigration and thermal constraints, which reduces their time to fail and hence affects their reliability. The impacts of high resistance on vias reliability are shown in

Figure 2.8 Self-consistent metal temperature of local vias (due to self-heating and electromigration) for different duty ratios as technology scales. Reference die temperature =105°C as per ITRS.

Figure 2.8 and Figure 2.9 [81]. The interconnect temperature was shown to increase significantly with smaller technology node. Electromigration and thermal constraints make the current density requirements unachievable beyond the 45 nm technology node.

Figure 2.9 Maximum allowed J_{rms} for local vias under self consistent joule heating and electromigration lifetime constraints evaluation for different technologies (reference die Temp=105°C). The arrows on both sides of the axes show the design rule current densities required to support the ITRS specified intermediate wiring current.

The outstanding electrical and thermal properties of CNTs described in the earlier section allow CNT vias to replace copper vias in interconnect technology. Even when CNTs are partially used as vias with copper, the vias temperature rise is much lower, as shown in

Figure 2.10 [82]. Figure 2.11 demonstrates that the lower temperature contributed by CNT vias can offer up to two orders of magnitude improvement in the EM mean-time-to-failure of Cu global interconnects. The intrinsic resistivity of CNTs is lower than that of copper. With the lower resistance of CNT vias, overall delay can also be shortened [82]. But for CNT to outperform copper as vias, very highly packed nanotubes are needed. In a CNT vias, any space or air gap present between the nanotubes would reduce the effective electrical and thermal conductance greatly, as those parameters are directly related to the number of conductive channels (number of CNTs) within the vias. It is possible to produce super dense CNTs [83,84], however to deposit this dense structure in vias structure is still a challenge.

Figure 2.10 Maximum temperature rise for Cu interconnects and vias vs. CNT bundle vias integrated with Cu interconnects. For CNT bundles, the shaded region shows the range $1750 \text{ W/mK} < K_{th} < 5800 \text{ W/mK}$ [85]. Reference (substrate) temperature = 378 K.

Figure 2.11 Cu interconnect electromigration (EM) lifetimes as a result of high interconnect temperatures normalized to EM lifetime at reference temperature (378 K), when vias are composed of Cu and CNT bundles respectively.

2.2.4 First Level Interconnects

First level interconnect technology has moved from the older method of gold wire bonding to the solder bump flip chip packaging. It enables electrical components to shrink considerably and permits larger numbers of I/O terminations. In the packaging level, the number of solder joints per package has been increased significantly for meeting the ever increasing changes. This in turn has increased the amount of solder consume per chip. The most commonly used solder is tin-lead (Sn-Pb). It has been found that even small amount of

lead is detrimental to the health of living things. With the widely increased usage of tin–lead solder, the significance of lead poisoning became more detrimental. Such environmental concern has created a need to move beyond conventional lead containing solder to a more eco-friendly material. An attractive and potentially viable material for replacing solder is CNTs, which has been suggested to be significant less health hazard to human for small amount of exposure, especially MWCNTs (larger physical size) [86-91]. Table 2.2 presents some of the in vivo studies of the toxicity of CNTs that supports this belief. It has been demonstrated that under normal circumstances, it did not show any harmfulness to human. Inflammation was induced when they are deliberately implanted to the tissue. There are also no sign of acute toxicity to internal organs when living things are in contact with small amount of CNTs. The amount of consumption for damage to occur would have to be induced to the body by high dose CNT distillation or injection. However, there are also studies that pointed out the potential hazard of CNTs. In a toxicity study conducted by Seo et Al. [92], it has shown that carbon-based nanomaterials can lead to cell death. They found that CNT toxicity is aspect ratio dependent and which is explained by the amount of dangling bonds present. Higher amount of active surface sites in the nanotubes surface have shown a reduction of surviving cells in the experiment. In another study, workers who breathed in CNT were found more likely to develop lung diseases [93]. The study also discovered different toxicity level for different CNT types. Longer and functionalized CNTs were more toxic than shorter and larger nanotubes [92,94]. Information concerning the potential hazards related to CNTs is rare and still under debate. Therefore, attention needs to be paid on the toxicity issues, particularly to applications where CNTs might have direct contact with living thing, such as in biomedical devices. It is equally important to develop safety procedures for

personnel working in CNT research environments for safe use of the material. Meanwhile, it can be recommended that, if CNTs are to be commercialized and applied to consumer products, they should be well-encapsulated. This will avoid any direct contact between these materials and living thing or pose as environmental hazards.

Table 2.2 Vivo studies of CNTs toxicity

Amount of CNTs	Model	Expose condition	Expose duration	Toxicity	Mechanism of Toxicity
CNT soot with high content [86]	Human and rabbits	Patch test, (Human skin) Ocular instillation (Rabbit eye test)	96, 24, 48 and 72hr	No association with skin irritation or allergenic risks	Dermatological trials have not shown sign of health hazard
Pristine Arc-CNT 25mg [87]	Guinea pigs	Intratracheal instillation	4 weeks	Not induce any abnormalities of pulmonary function or measureable inflammation	Working with CNT is unlikely to be associated with any health risks
Hat stacked CNT Not specified [88]	Rats	Clusters were implanted in the subcutaneous tissue	1 and 4 weeks	Normal process of inflammation for foreign bodies, without serve inflammatory response was observed. No acute toxicity in subcutaneous tissue. No inhibition of wound healing	Water solubility and characteristic structure composed
MWNTs 0.5, 2 and 5mg/rat [89]	Rats	Intratracheal instillation	1 and 2 months	Not ground MWNT accumulate in the airways. Ground MWNT was cleared more rapidly. Both MWNT induced inflammatory and fibrotic reactions. Also both have caused pulmonary lesions at 2 months	Length appears to modulate clearance kinetics. Biopersistence. Intrinsically toxic to the lung

Nevertheless, CNTs is definite beneficial as first level interconnects in the aspect of meeting the progressive technological demands in miniaturization. The focus on using CNTs as interconnects has fall on on-chip level, therefore not as much attention has been paid on analyzing the use of CNTs as first level interconnects. However, the continuous leap frog development in wafer level technology is becoming more difficult for flip chip interconnect technology to keep pace with. Utilizing CNTs as first level interconnects would have electrical, thermal and mechanical advantages and improvement in many areas. Electrical properties of CNTs are well known to be exceptional. Being a ballistic conductor [5,6], interconnects made of CNTs would have low resistivity. For large size interconnects such as first level interconnects, bundles of CNTs can be employed for reducing their electrical resistance further. The effective resistance of a highly packed CNT bundle can be calculated by Equation 2.4.

$$R_{total} = R_{single}/n_{cnt} \quad 2.4$$

Where R_{total} is the total resistance and R_{single} is a single CNTs resistance. n_{cnt} represents the number of metallic CNTs presented in the bundle. The conductivity could be further improved by intertube electrons transport if the CNTs are in good contact with each other. CNTs conductivity has been reported to reach $10^6 \sim 10^8 \Omega^{-1}\text{cm}^{-1}$ [48,49], which is much higher than that of typical solder ($68500 \Omega^{-1}\text{cm}^{-1}$). Any improvement in electrical conductivity of first level interconnects would increase their signal transfer rate and increase devices operating speed. The graphene sp^2 bonds in the nanotubes structure are strong, enabling them to have high resistance to electromigration and diffusion to other materials.

This is essential for interconnects reliability, particularly when they are scaled down with increased current density. Another major concern in interconnect reliability arises from the CTE mismatch between the rigid semiconductor chip (low CTE) and the circuit board (high CTE). This large CTE mismatch between chip and circuit board can produce large strain on the first level interconnect, leading to fatigue failure. This problem is exacerbated when the chip geometry is large and the dimension of interconnects is minimized to achieve high I/O density. A potential solution to this concern is to use high aspect ratio interconnect materials with low stiffness for lowering the stress building up at the interface. However, achieving compliance with simple metallic structures is difficult because of their very complicated fabrication process and inherently high stiffness [95]. CNTs being self-assembled quantum wires with aspect ratio of more than 1000, can be use for creating fine interconnects with high respect ratio. The low stiffness [96] and high tensile ductility of CNTs would also be ideal to ease out the stresses build up by CTE mismatch between the die and its carrier [97-99]. To increase devices data transmission rate and operating frequency, output power of IC must be increased. However, such increase would increase the amount of heat generated on chip. Theoretically and experimentally, CNTs have demonstrated a thermal conductivity near to or higher than that of diamond [100-105]. This is equivalent to 20 times higher than the conductivity of typical solder material. If CNTs are applied as first level interconnects, heat generated on chip could be removed rapidly to the substrate, accordingly the chance of overheating and thermal damage to the chip can be reduced.

2.3 Joining Technique for CNTs

Excellent electrical and microstructural properties of CNTs have been well demonstrated experimentally [77]. Future on-chip and off-chip (first level) interconnects with CNTs acting as the potential material [106] have also been proposed. Nevertheless, to realize the applications of CNTs in electronics as different level interconnects, the ability to create high quality connection between individual nanotubes or bulk CNT films has been recognized as the key determining factor.

2.3.1 Joining Technique for Individual CNTs

Typically, CVD deposited CNTs appear as individual “tube” structure. To reach the goal on fabricating CNT on-chip interconnect and CNT based electronics, CNTs would need to be connected or joined to each other. The total resistance of CNT systems consists of the intrinsic resistance of CNTs and the contact resistance between them. If CNTs are not well connected, the contact resistance would dominate the overall resistance of the interconnect structure. Consequently, the contact or joint between CNTs plays a crucial role in determining if the anticipated ballistic electrons transport of CNTs is likely to occur. In order to produce ideal CNT contacts, many innovative methods for joining CNTs have been developed. Those techniques can be classified into manual and self-assembly. Manual methods show promise with regard to manipulating and placing nanotubes at discrete locations. Cox et al. [107] from University of Surrey has successfully welded CNTs on a selective basis. Their technique is based on controlled heating of the CNT joint, which reconstructs the stacking carbon-carbon (C-C) structure at the CNT interface to form an

amorphous carbon (a-C) joints. No welding material is needed in their approach. Arc-discharge-produced nanotubes were used in their experiment and the nanotubes were manipulated by a pair of moveable tungsten tips within a SEM as shown in Figure 2.12. A cycle of voltage between 0 to 53 V was applied across the crossed nanotubes for the heating effect, so as to establish the electrical contact. Typically after ten cycles, the CNTs were mechanically jointed and they were able to obtain a stable I-V behavior from the jointed structure. Similar method was also used by H. Hirayama et.al. [108] . By enforcing a voltage of 2 V to a SWCNT and an electrostatically attached CNT, a permanent joint was established. The I-V characteristic was found to be stable with nonlinearity and symmetric in the polarity change (Figure 2.13).

Figure 2.12 (a) SEM image of the tungsten tips selecting the CNTs, (b) Nanotube construction of letters A, T, and I using six nanotubes.

Experiments have demonstrated that electron irradiation could also create molecular junctions between crossed CNTs [109-112]. M. Terrones et al. [109] reported the formation of molecular junctions on crossed CNTs by electron beam welding. Various CNT geometries are created in situ within a transmission electron microscope (TEM) as presented in Figure 2.14. In their experiment, electron beam exposure of CNTs under high temperature had created structural defects which encouraged the joining of tubes via cross-linking of dangling bonds. Their observations are also supported by molecular dynamics simulation (Figure 2.15). Y.G. Wang et al.[110] used similar method in creating CNT junctions. However in their study, they have suggested different mechanisms for e-beam irrational joining of CNTs. Rather than atomic rearrangement of CNT interface, they believe that hydrocarbon contamination was deposited on the CNT joints during the e-beam irritation and which acted like solder material for the CNTs. Their in situ electrical measurement showed that the multi-walled nanotube junction has a linear current–voltage behavior as shown in Figure 2.16. The jointed nanotubes were also subjected to a pull test and the breaking point occurred at the “tube” region, with the joint undamaged (Figure 2.17). This illustrated that the CNT junction is mechanically strong.

Figure 2.13 The contacted bundles exhibit symmetric, nonlinear $I-V$ characteristics

Figure 2.14 (a) A SWCNT crossing with an individual SWCNT (b) 60 sec of electron irradiation promotes a molecular connection between the thin and the wide tube, forming an “X” junction. Schematics show that this junction is twisted out of the plane. Molecular models of each image are provided on the right side

Figure 2.15 Sequences of merging CNTs into a X junction. (a) top view of the crossed CNTs (b) two links between the two CNTs is formed (side view). (c) the connection between the two tubes is almost fully established, with some dangling bonds (green) (d) surface reconstruction occurs and the carbon system approaches an X junction.

Figure 2.16 I-V measurement of the CNTs with e-beam creased micro-junction.

Figure 2.17 The tensile behavior of the nanotubes shows the failure of the nanotube, which illustrates that the junction has excellent mechanical properties.

Besides electron irradiation, ion irradiation was also found to create molecular junction between crossed single-walled or multi-walled CNTs [113-116]. M. S. Raghuveer et al. [117] have demonstrated that the use of 10 and 30 keV focused beams of Ga^+ ions could weld, thin, slice and alter the structure or composition of MWCNTs at precise locations. They observed that amorphization had occurred on the irradiated CNTs, which they suggested to be the result of irradiation-induced destruction of the conjugated p bonds. Ga implantation in CNTs was also found to take place during the process. It is believed that the molecular CNT joints are formed by cross-linking of dangling bonds resulted from vacancies produced by ion bombardment. They have also demonstrated welding of CNTs to other materials, such as SiN membrane. Due to the transformation in atomic composition of the nanostructure after ion irritation, the electrical properties are assumed to change accordingly. Other research groups [115] have also managed to joint CNTs by employing carbon ion irritation.

The above mentioned manual joining techniques such as welding, allow joints or connections to be made at a precise and predetermined location. It seems to be an effective

way to create complicated CNT network structure for electronics applications. However, there are some disadvantages to those techniques. Firstly, manual techniques are very low in yield. Only limited number of joints can be made at once. It also requires unconventional fabrication equipments (e.g. TEM), which are very expensive and are not made for large scale production of welding. Some of the techniques applied, such as ion induced irradiation method, caused serious destruction of the nanotubes structure. The nanotubes were observed to transfer into carbon nanowires after exposed to ion irradiation [115]. As nanotubes properties largely depend on their atomic structure, any damage or destruction might degrade their properties significantly. Until today, the developed methods are still too low in yield, complicated, high in cost and impractical for commercial production of CNT junctions.

Figure 2.18 SEM micrographs of (a) overlapping nanotubes marked A and B, prior to irradiation, and after exposure to (b) 10^{16} and (c) 2×10^{16} ions cm^{-2} of 10 keV Ga^+ ions; (d) an example of a nanotube network formed by several welds indicated by arrows; (e) SEM micrograph showing a CNT welded to the edge of the SiN membrane by exposure to 10^{17} cm^{-2} of 30 keV Ga^+ ions.

Self-assembly techniques or the “bottom up” approaches for joining CNT have shown to be promising in easing some of the issues of manual approaches. In those self-assembly techniques, the nanostructures are formed by self-organization of atoms during their fabrication process. Those processes are usually developed from modifying typical CNT growth process, with specially designed template or catalyst. Silicon nanostructures such as sphere [118-120], pillar [121] can be used as template for deposition of CNT network structure by CVD CNT growth process. The CNT network formed is shown in Figure 2.19. Connectivity between the nanostructures was made by nanotubes, however the density of the CNT network by such method is low. NASA [122] has reported to use porous, collapsible polystyrene/divinylbenzene microspheres as micron-scale templates for the construction of SWCNT networks. SWCNTs were found connected to each other and linking the microsphere as presented in Figure 2.19(e).

Figure 2.19 Network of CNTs by using Si nanostructure as template (a-d) and (e) [118-121] polystyrene/divinylbenzene microspheres as template [122]

Decoration technique has been developed for depositing nanoparticles on the surface of nanostructure. The materials that can be deposited range from biomolecules, like chitosan [123] to common metals, like Ag, Cu and Au [124-126]. Sun et al. [127] combine the decoration technique and conventional CVD CNT deposition process for forming hierarchical CNT structures on carbon fibers. In their approach, primary MWCNTs were pre-treated in concentrated HNO_3 and decorated with Co/Ni catalytic sites. The decorated MWCNTs were then underwent an CVD CNT growth process. Their resulted secondary MWCNTs appear as branches on the primary MWCNTs as presented in Figure 2.20. Such method however posts two problems. As CNTs being hydrophobic in nature and with low surface tension of wetting (200mN per meter) [128], it is difficult to direct adhere high surface tension metals like Co or Ni [129] onto their surface. An oxidation pretreatment of CNTs by strong oxidizing acids is needed to obtain a homogeneous distribution of Co/Ni particles on the CNT surface. Highly concentrated acids are hazardous to users and the pre-treatment process is complicated. This pre-treatment of CNTs also induces large amount of damages to the CNT atomic structure, which might degrade their properties. It is also worth noting that to withstand the acid treatment process, only larger CNTs or carbon fibers are suitable for such approach. This might not be ideal for applications that require CNTs with nano-scale dimension. On this account, Y. Hao et al. [130] modified the method by using dense fluidized bed and floating catalytically chemical vapor deposition method (FCCVD) to deposit secondary CNTs (Figure 2.21). It was demonstrated that small CNT branches can be formed on the tips or sidewalls of CNTs as shown in Figure 2.22. FCCVD is a modified version of conventional CVD CNT deposition process. The CNTs are prepared by flowing a hydrocarbon and a reactive gases mixture, which dosed with a small amount of catalyst,

through a horizontal tube reactor [131,132]. The substrate for CNT deposition is located in the middle or end (lower temperature region) section within the tube furnace. Catalyst particles that flow through the tube furnace would be deposited on or trapped by the lower temperature substrate and which could activate CNT growth. Ting et al. [133] fabricated CNT branching webs which consist of two-dimensional H-junction, multiple Y-junctions, and three-dimensional multiple CNT junctions by using the concept of FCCVD with a patterned substrate. Their single crystal silicon substrate was patterned with steps and was scratched upon CNT deposition. They used a typical FCCVD horizontal furnace and the catalyst source (iron powder) was placed on a ceramic boat, positioned at a distance of 5 cm away from the substrate upstream. Their arrangement allows evaporation-deposition of the catalyst powder to occur, such that nanosize catalysts were deposited on the Si substrate and trapped within the scratches. CNT network was then grown through the pyrolysis of methane on the catalysts as shown in Figure 2.23.

Figure 2.20 (a) SEM micrograph of secondary MWCNTs grown with ethylene at 800 °C on primary MWCNTs. (b) TEM micrograph of secondary MWCNTs. (c) Close up with arrows 1, 2 and 3 pointing to three shapes of Co/Ni tips.

Figure 2.21 Growth mechanism of the branching CNTs in FB-FCCVD. Drops of the catalyst solution (a) evaporated to form small metal clusters (b), which aggregate (c) and catalyze the growth of CNTs (d). In the second CNT growth process, catalyst particle adhered on a CNT (e), forming a local active surface (f) and catalyzing the new generation of CNTs (g) by the correlated growth mechanism. When the branching nanotubes close the end, the growth of branches deactivates (h).

Self-assembly techniques for joining CNTs or creating CNT network have advantages over manual technique in yield, cost and are less complicated. However, there are still some downside need to be resolved. One of the examples would be the ability to control the growing site for secondary CNTs. Methods that used FCCVD have proven to activate deposition of CNT network, but since the catalyst is deposited by random deposition, the

CNT network often formed on the entire surface of primary CNTs and substrate. For CNT network that formed by using nano template, the feature size of the templates is the key factor in determining if CNT network could be formed. It usually requires templates that are in nano-scale, which is difficult to fabricate. Types of materials that can be used as templates are also limited. They should not react with the catalyst materials and remain stable under high temperature of CNT growth ($>600^{\circ}\text{C}$). All those restrictions might challenge the use of those methods for nanoelectronics applications.

Figure 2.22 Branch structure in CNTs . The branches on tips or sides of CNTs are indicated by arrows. The insert shows the HRTEM of a cluster of branches

Figure 2.23 CNTs grown on Si substrate. It shows the present of Y-junction CNTs, H-junction CNTs and 3D CNT webs.

2.3.2 Joining Technique for CNT Bump

To make good connection between CNTs to electrode pad for first level interconnect application, special technique have to be developed. Chen et al. [134] have reported an interesting way to fabricate an electrode-CNT-electrode system. Oriented, freestanding and structured CNT bundle was deposited and sandwiched between two electrodes by microwave plasma CVD. They used a special multi-layered catalyst structure, which consisted of Cu/Ni/Al/Fe/Al/Ni/Si, with Fe as the catalyst material sandwiched between the multilayered electrode metal layers. Schematic of their possible CNT growth mechanism is presented in Figure 2.24. They suggested that the catalyst layer (Fe) had broken down into nano particles after the preheating process, which were activated for CNT growth during the CVD process. The sandwiched CNTs pushed the metal layers upward with their growth, forming the metal

layer-CNT-metal layer structure. The overall resistance of the sandwiched CNT bundle and the two CNT-terminal contacts is measured to be about 37Ω , equivalent to $14.7\text{ k}\Omega/\text{tube}$. Their corresponding conductance is close to the quantum limit conductance G_0 of nanotubes, which shows that the two CNT-metal interfaces have very low contact resistance. Such direct assembly technique of CNT bundle have potential for first level interconnect application, however they have yet to demonstrate the size/weight limit that the CNT bundle can support for such sandwich structure. For large metal pad that are used by first level interconnect, the weight and size of the pad might affect the lifting process of the CNTs and/or diffusion of carbon into the catalyst layer. Those problems might inhibit the growth of the sandwich CNT bundle.

Another more commonly used method for joining bulk CNTs is by using metal as connective material. Fujitsu [135] used typical photolithography technique in patterning catalyst for CVD CNT growth process. High density CNT bumps were grown on the patterned catalyst sites. Gold which acted as the connective metal was then plated on the surface of the CNT bumps (Figure 2.26). Thermal compression method was then used for assembling those CNT bumps to the electrodes. Teo et al. [136] embed CNT bumps into solder for first level interconnects application. The CNT bumps were first wetted with titanium, nickel and gold for enhancing their wettability to solder. Solder paste was then applied onto the CNT pads as shown in Figure 2.27(a)-(c). Reflowing process was used for connecting the CNT solder pads to the electrodes (Figure 2.27(d)).

Figure 2.24 Schematic of a possible CNT growth mechanism using sandwiched catalysts.

Those methods demonstrated some efficient ways in assembling CNTs to electrode pad/substrate with good mechanical strength. Those processes are also compatible with current microelectronics fabrication sequences and technology. Nevertheless, in aspect to electrical connection, the quality of metal-CNT contact has yet been addressed. Contact resistance of metal-CNT interface has been reported with much diverted results. It ranged from orders of $\text{M}\Omega$ [137-139] to values as low as one resistance quantum ($\sim 12.9 \text{ k}\Omega$) [140].

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Such variation is the result of various bonding configurations of metal atoms to CNTs and the type of metal used [141]. For low contact resistance, the bond of metal to CNTs should ideally be covalent and the metal used should be the early 3-d elements (such as Sc, Ti, and V). Due to their atomic difference in nature, there has yet been an effective way in creating covalent bond of metal to CNTs for such contact. In addition, the specified metals may not be compatible with current microelectronics fabrication processes.

(a)

Figure 2.25 Sketch of the set-up used to measure I–V characteristics of sandwich grown, self-assembled two-terminal CNT devices. The flat Pt/Ir current probe is with contact area of $25 \mu\text{m}^2$ and can be positioned with an accuracy of $0.1 \mu\text{m}$ onto the top terminal.

(b) Measured I –V characteristics of self-assembled, as-grown two-terminal device comprising a bundle of multi-walled CNTs

Figure 2.26 CNTs bumps with gold plated surface

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Figure 2.27 (a) CNT-deposited chip, (b) Solder deposition and (c) CNT-Solder joint after reflow, (d) The assembled CNT flip chip structure

3 Growth of Carbon Nanotubes

With interconnect technology reaching some fundamental scaling limits in the near future, problems pertaining to thermal reliability and electromigration endurance have to be overcome. This realization has sparked an intense study for new device principles, technologies and new materials. CNTs have received a lot of attention recently, due to their unique electrical, mechanical and thermal properties as well as high resistance to electromigration [142-145]. With such exceptional properties, CNT would be an ideal material for fabricating on-chip and first level interconnects. It is believed that by applying CNTs as the interconnect material, the size, electrical and thermal requirements of future interconnect could be met. However, to investigate the potential of CNTs for interconnect applications, it is essential to deposit CNTs with desired structures, such as diameter, length, alignment, deposition site and density with consideration of specified application's precondition. Hence, this chapter will focus on CNT synthesis with a series of studies on the effects of different deposition conditions on the CNT structure.

3.1 Review on Carbon Nanotube Growth

In the last decade, different CNT synthesis processes have been developed. So far, arc discharge [146-148], laser vaporization [149-151], and chemical vapor deposition (CVD) are the most common and well-explored techniques [152-158]. Among them, CVD techniques have drawn a lot of attention due to their advantages, such as lower processing temperature, higher quality and the ability to control CNT structure.

3.1.1 CVD Techniques

In the following section, two of the most commonly used CVD techniques, namely thermal CVD (TCVD) and plasma enhanced CVD (PECVD) are introduced.

3.1.1.1 TCVD

With TCVD technique, CNT synthesis is achieved using thermal energy (e.g. resistively heated coil or filament) to decompose gas phase carbon source to gaseous carbon molecule. A schematic of a typical TCVD system is shown in Figure 3.1. Most commonly used carbon sources include methane, carbon monoxide and acetylene. The reactive atomic carbon molecules will diffuse towards a heated substrate, which is coated with a thin layer of catalyst material. This catalyst layer is crucial for the formation of CNTs and is usually ferromagnetic metal such as iron, nickel or cobalt. Active process gases such as hydrogen or ammonia is supplied before and during the CNT growth for assisting thermal break down of the catalyst film. The detail explanation of the role of catalyst and the reactive gases are discussed in the previous chapter. The process temperature of such CVD technique is usually ranged from 600 °C to as high as 1000°C [4,5]. Process parameters such as pressure, carbon feedstock to process gases ratio, time etc. are critical for CNTs formation and can be adjusted to control their structure.

Figure 3.1 Schematic of a typical TCVD

3.1.1.2 Plasma Enhanced CVD (PECVD)

TCVD operate under the most basic principle of CVD process. Different CVD techniques for CNT synthesis have been developed for deposition of different type of CNTs. Plasma enhanced chemical vapor deposition is one of the techniques that is developed for deposition of aligned CNTs. Schematic of a typical PECVD system is shown in Figure 3.2. Similar to TCVD, carbon feedstock enters the process chamber and decomposes into carbon molecules. Substrate with a layer of catalyst is heated during CNT growth process and gases are applied to break down catalyst later in the process. The only exception between the two techniques is the application of plasma for PECVD. High voltage plasma generated during

the growth process would yield vertically aligned CNTs. With adding energy source provided by plasma, the growth temperature for PECVD process is lower than that of typical TCVD. The degree of alignment of CNTs by PECVD is largely affected by the plasma power and will be looked upon in the later chapter.

Figure 3.2 Schematic of a typical PECVD

3.1.2 Review on CNTs Growth

The synthesis conditions, catalyst and the catalyst support for CVD technique were reported to have significant effects on the nanotubes structure. Jae-Hee Han et al. [159] have shown that an increase in the deposition temperature increases the average diameter and deposition rate of CNTs. This increase in diameter and deposition rate is explained by the

increase in diffusion and surface reaction rate of reactant species at elevated temperatures. In the same study, deposition temperature of below 550 °C was found to be too low to decompose acetylene and thus hindered CNT deposition. Similar results have also been reported elsewhere [160]. Jae-Hee Han et al. have also discovered that by increasing the amount of NH_3 , with a constant flow rate of C_2H_2 , the average diameter of CNTs was decreased from 200 to 100 nm [159]. According to their explanation, this phenomenon is caused by the etching effect of NH_3 and the reduction of carbon atoms tendency to crystallize into graphite structure. Chhowalla et al. [161] reported that by increasing the concentration of C_2H_2 in CNT deposition process, the CNT deposition rate increases at the initial stage of the deposition process and decreases dramatically in the later stage of the deposition process. The vice versa trend was also found for CNT diameter. The initial increase in deposition rate was attributed to the higher concentration of carbon feedstock in the plasma, which was complemented with the etching by ammonia. However at C_2H_2 concentrations of above 50%, the vertical nanotube formation could not keep pace with the quantity of carbon extruded from the metal catalyst, causing the lateral formation to dominate. This resulted in the decrease in deposition rate and increase in diameter. Li et al. [162] observed that by increasing deposition pressure, the deposition rate would increase. The increase in deposition rate was caused by the higher concentration of carbon atoms within the deposition environment for CNT formation. A study conducted by Hee Jin Jeong et al. [160] discovered that the CNTs length increases with increased deposition time, however the increase in CNTs length would stop after reaching a threshold deposition time. The deposition rate of CNTs was also found to decrease with increased deposition time. The decrease in deposition rate is explained by the cap formation mechanism, which suggests that the catalyst cap would be

etched continuously during synthesis process and therefore reduce the rate of CNT synthesis. The relationship between CNT synthesis and the different controlling conditions is summarized in Table 3.1

Table 3.1 Summary of the effects of synthesis condition on CNTs

	Deposition Rate	Diameter
+ Deposition Temperature	+	+
+ NH ₃ Concentration	Not reported	-
+ C ₂ H ₂ Concentration	+ -	- +
+ Deposition pressure	+	Not reported
+ Time	-	Not reported

+ Increase

- Decrease

+ - Increase followed by decrease

- + Decrease followed by increase

Classified by their alignment, CNTs can be classified into aligned and non-aligned types. Non-aligned CNTs are randomly distributed and mostly non-oriented tubes, whereas aligned ones are usually vertically aligned particular to the substrate surface. The first successful nanotubes growth by CVD method is in the year of 1993 [163]. It was until 1996 that the CVD method was firstly developed for aligned CNT synthesis [156]. The alignment of the tubes could be achieved by: (1) Embedding catalyst in Si [164], (2) Growing tubes in very high density which forces the tubes to align parallel to each other [165-167] and (3) By growing CNTs under plasma or biasing conditions. [156-170]. Currently the plasma and the biasing methods are the most commonly used, as they are simpler and have controllability for

aligning CNT. Both non-aligned and aligned CNTs have their own unique properties which could be beneficial for interconnect applications.

3.2 Carbon Nanotubes Growth

In the following sections, the synthesis of CNTs using hot filament CVD (HFCVD) and plasma enhanced CVD (PECVD) with varied deposition conditions were conducted and their effects on the nanotubes morphology as well as structure were studied. The presented information was used for optimizing and controlling process parameters for manufacturing CNTs with pre-determined morphologies in relatively high purity and in high yields.

3.2.1 CVD systems

Two CVD systems are employed for CNT synthesis throughout the study. They are HFCVD and PECVD. The detailed descriptions of the two systems are presented in the next section.

3.2.1.1 HFCVD

HFCVD makes use of resistively heated filament for the growth of CNT and is considered as a type of TCVD. For the synthesis of CNTs in our study, a HFCVD system has been employed. The system consists of a quartz tube furnace, which is surrounded by filament. During its operation, the filament is resistively heated to provide the required process temperature of about 600 °C. Process gases and carbon feedstock are controlled by

mass flow controllers and fed into the chamber through a gas feeder on top of the furnace. The 2" substrate holder is located in the central region of the furnace. This system was initially designed for growing non aligned CNT and later modified for growing aligned CNTs. Modifications were made to electrically connect the substrate holder to ground as anode with another conductive plate installed 2 cm above the substrate holder as cathode. The cathode is connected to an external power source for the supply of biased voltage, which is used for the growth of aligned CNTs. A schematic of the modified system is shown in Figure 3.3.

Figure 3.3 Schematic of the HFCVD system

3.2.1.2 PECVD

In our study, a customized PECVD system was used for the growth of aligned CNT and its schematic diagram is shown in Figure 3.4. This system was manufactured by Nanoinstruments Pte Ltd, a Cambridge based company that deals with manufacturing of

nanotubes deposition systems. It consists of a 4" (in diameter) isolated graphite stage as substrate holder. The graphite stage can be heated to a maximum temperature of 1000 °C and is controlled with a fully programmable ramp segment. The plasma discharge stage and a gas inert located 5 cm upon it, are serving as anode and cathode, respectively. The system can either be a RF biased or DC pulsed plasma for aligning CNTs. The gas inert system has shower head design to ensure uniform distribution of gases. Mass flow controllers are used for controlling the flow of one process and a single carbon feedstock gas to a maximum concentration of 500 sccm for each of the 2 gases. The reading of chamber pressure and independent gas pressure are made possible with a set of pressure sensor, installed in the chamber and gas pipe lines, respectively.

Figure 3.4 Schematic of PECVD system

3.3 Non-Aligned Carbon Nanotubes by HFCVD

Structure and morphology of nanotubes are largely affected by their growth condition [171-174]. Therefore, a set of experiments were conducted by HFCVD to study the effects of

growth condition on the structure of non-aligned CNTs. To make sure that the variations of the nanotube structure are caused solely by the growth condition, Ni foils were employed as the catalyst layer and the deposition substrate for nanotubes growth.

3.3.1 Experimental Procedures

Ni foils with thickness of 500 μm was used. CNTs were grown in a hydrogen H_2 environment with acetylene C_2H_2 as the carbon feedstock by using a HFCVD system.

Prior to the synthesis process, Ni foils were ultrasonically cleaned in alcohol and dried with nitrogen gas flow. After the cleaning process, they were transferred to the HFCVD chamber. A base pressure of 2E^{-2} mbar was achieved within the chamber before introducing H_2 . The working pressure was monitored and controlled at designed values of 5, 10 and 20 mbar. At the same time, the system was heated to the pre-set temperatures of 450 $^{\circ}\text{C}$, 550 $^{\circ}\text{C}$ or 650 $^{\circ}\text{C}$. The growth of CNTs was then activated by introducing carbon feedstock C_2H_2 to the chamber. The C_2H_2 concentration and the deposition time varied from 5% to 25% and from 10 to 30 minutes respectively.

The surface morphology of the CNTs was analyzed by scanning electron microscope (SEM, JEOL JSM 5910LV) at 20 kV. The chemical bond structures in the CNTs were analysed by Raman spectrometer. Raman spectra were obtained with a Renishaw 1000 spectrometer using argon laser beam of 514.5 nm as the excitation source. The laser output power was set to 5 mW during measurement.

3.3.2 Results and Discussions - Effects of C₂H₂ Concentration

CNTs were deposited by HFCVD with different concentrations of C₂H₂. Flow rates of C₂H₂ varied from 10 to 50 sccm while H₂ flow rate, deposition temperature, deposition time, and working pressure were kept constant at 200 sccm, 550 °C, 30 minutes and 20 mbar, respectively. Figure 3.5 shows the SEM micrographs of CNTs grown from C₂H₂ concentrations of 5%, 10% and 25%. The thickness of the CNT films increased as a function of C₂H₂ concentration. A higher C₂H₂ concentration produced a thicker film. The length of the nanotubes increased as higher concentration of C₂H₂ was introduced. However, the density of nanotubes decreased as C₂H₂ concentration increased from 10% to 25%. It is believed that the increase in film thickness was caused by the increase in nanotube length. As all the samples have equal deposition time of 30 mins, it indicated that the increase in CNT film thickness was caused by the increased carbon content in chamber when high C₂H₂ concentration was introduced. From the low magnification images, it can be seen that the films composed of CNT clusters (the white patches on the CNT film). With an increase in C₂H₂ concentration, the size of the cluster became larger. Look into the CNT clusters, it is observed that the nanotubes had a diameter of around 200 nm for all C₂H₂ concentrations. It means that the C₂H₂ concentration does not have influence on the nanotube diameter. For C₂H₂ concentrations of 5% and 10%, relatively uniform CNTs were achieved. For C₂H₂ concentration of 25%, it is noticed that certain amount of amorphous carbon appears as white patches (Figure 3.5(f)) present on those large nanotubes clusters of Figure 3.5(e). Some of these nanotube clusters dropped off during handling, which indicated that the nanotubes were not grown directly from the substrate but on top of the grown nanotubes.

Figure 3.5 SEM micrographs with different magnifications of CNTs grown at different concentrations of C_2H_2 . (a) 50X and (b) 1000X for 5% C_2H_2 , (c) 50X and (d) 1000X for 10% C_2H_2 , (e) 50X and (f) 1000X for 25% C_2H_2 .

3.3.3 Results and Discussions - Effects of Deposition Time

Figure 3.6 shows the SEM micrographs of nanotubes grown with deposition time of 10, 20 and 30 mins at working pressure of 20 mbar. Other synthesis process parameters were kept constant to study the effects of deposition time on nanotubes growth. From pervious results, a more uniform CNT film can be obtained at C_2H_2 concentration of 5-10%. Therefore, 5% C_2H_2 was used to grow the CNTs here. The thickness of CNT films increased as deposition time increased. The diameter of nanotubes is around 200 nm for all of the samples. It can be clearly seen from the SEM images in Figure 3.6 that more uniformly deposited nanotube films were formed with shorter deposition time. No nanotube cluster was found (Figure 3.6(a)) and very short nanotubes can be observed from the high magnification image (Figure 3.6(b)) on Ni foil with deposition time of 10 mins. The nanotube clusters presented on Ni foil when the deposition time was prolonged to 20 mins (Figure 3.6(c)) and 30 mins (Figure 3.6(e)). 20 mins deposition time generated smaller clusters than 30 mins deposition time. The length of nanotubes increased as a function of deposition time, but density of nanotubes varied inversely to the deposition time. The increase in length of nanotubes in this case, was caused by the long exposure time of Ni foil to carbon feedstock.

Figure 3.6 SEM micrographs with different magnifications of CNTs grown at different deposition time. (a) 50X and (b) 1000X for 10 mins, (c) 50X and (d) 1000X for 20 mins, (e) 50X and (f) 1000X for 30 mins.

Another set of CNT deposition with varied deposition time of 10, 20 and 30 mins at working pressure of 10 mbar were also carried out. Figure 3.7 shows the SEM micrographs of nanotubes grown. Similar to CNT films deposited with higher pressure of 20 mbar, nanotubes length increased as the deposition time increased. For the CNTs deposited with pressure of 10 mbar, the density of nanotubes did not vary obviously as in the case of working pressure of 20 mbar. This resulted in a more uniform CNT films.

Figure 3.7 SEM micrographs with different magnifications of CNTs grown at different deposition time. (a) 50X and (b) 1000X for 10 mins, (c) 50X and (d) 1000X for 20 mins, (e) 50X and (f) 1000X for 30 mins.

3.3.4 Results and Discussions - Effects of Deposition Temperature

Figure 3.4 shows the SEM micrographs of nanotubes grown at temperatures of 450 °C, 550 °C and 650 °C while other process parameters remained constant. No nanotube was found on Ni foil at deposition temperature of 450 °C (Figure 3.4(a) and Figure 3.4(b)). Uniformly grown CNTs can be found on the other two Ni foils at deposition temperatures of 550 °C and 650 °C. CNT film deposited at 650 °C is thicker than that at deposition temperature of 550 °C.

Figure 3.8 SEM micrographs with different magnifications of CNTs grown at different deposition temperatures. (a) 50X and (b) 1000X for 450°C, (c) 50X and (d) 1000X for 550°C, (e) 50X and (f) 1000X for 650°C

The CNTs have similar diameter of around 200 nm for all deposition temperatures. However, much longer tubes were found on film at temperature of 650 °C. The density decreased when higher deposition temperature was applied. This increase in CNTs length suggested that growth rate of nanotubes increased for higher deposition temperature.

3.3.5 Results and Discussions - Effects of Deposition Pressure

Figure 3.9 shows the SEM micrographs of nanotubes grown at deposition pressures of 5, 10 and 20 mbar while other process parameters remained constant. Nanotube films were found to grow on all the samples. Variation of working pressure affected the diameters and density of CNTs. Diameter of nanotubes decreased from the average of 200 nm as shown in Figure 3.9(b) to the average of 80 nm as shown in Figure 3.9(f) when the pressure increased from 5 mbar to 20 mbar. Nanotubes film with the highest deposition pressure of 20 mbar also has higher density than films grown from lower pressure, but the effect of working pressure on the length of nanotubes was not significant. At lower deposition pressure, less nucleation sites were formed which resulted in larger CNTs. At higher deposition pressure, more CNT

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seeds were nucleated on Ni foil. With sufficient supply of C_2H_2 , these CNT seeds grew faster. Therefore, denser and longer CNTs were obtained at higher pressure.

Figure 3.9 SEM micrographs with different magnifications of CNTs grown at different deposition pressures. (a) 50X and (b) 1000X for 5 mbar, (c) 50X and (d) 1000X for 10 mbar, (e) 50X and (f) 1000X for 20 mbar.

3.3.6 Raman Analysis

Raman spectroscopy is an effective way to obtain the detailed bonding structure of CNTs. Being a routine and non-destructive method, it is widely used to characterize the quality of nanotubes [175-177].

Figure 3.10 shows Raman spectra of the CNTs synthesized by HFCVD with varied deposition parameters. The first order Raman spectra of all samples presented two strong peaks at around 1348 and 1605 cm^{-1} which are common for typical characteristics of graphitic CNTs. Common appellations for these two peaks are D line and G line, respectively. There is no significant deviation of peaks' value, which shows similar carbon bonding structure for all nanotubes films. The G line in this Raman spectra was attributed to the presence of crystalline graphite (sp^2 band), indicating that the nanotubes are highly graphitized, while the D peak was attributed to the defects in the graphite crystal which should be from the curved graphite sheet on the nanotubes caps. The D peak also reflected the disorder graphite present in nanotubes as defects and/or as amorphous carbon presented [178]. In nanotubes deposition, those two structures are not desired, therefore lower I_G/I_D intensity ratio of G and D peaks would mean a lower structure quality of the nanotubes film. In contrast, if the ratio of $I_G/I_D > 1$, it can conclude that the CNT structure deposited consists of CNTs with high level of graphitization and low defect [179]. To obtain the areas of the D and G peaks for the calculation, a Gaussian fitting with background subtraction was performed onto the raw Raman data and as shown in Figure 3.10(c). It was discovered that most of the HFCVD deposited CNT film have a ratio of $I_G/I_D < 1$, with the highest C_2H_2 concentration sample has the lowest grading. It is believed to be caused by the high amount

of atmosphere carbon. The high concentration of carbon sources decomposed from C_2H_2 may have excessive amount of carbon atoms needed for graphitic nanotubes on the catalyst surface, hence deposited as amorphous carbon. The only CNT film with $I_G/I_D > 1$, is the one deposited from pressure of 10 mbar and with 10 mins of deposition time. From SEM study, this CNT film has also found to have the most uniform CNT distortion. Spectra shown here assembled spectra of multi-walled nanotubes reported elsewhere [180, 181]. Also, the radial breathing mode (RBM) peaks at around 200 and 300 cm^{-1} on the Raman spectra which respond to single wall nanotubes [182] were not observed from the Raman spectra in Figure 3.10 indicating that nanotubes presented are multi-walled.

Figure 3.10(b) shows the spectra of Ni foils after nanotubes growth at temperature of 450 °C (a) and pure Ni substrate (b). The spectrum of Ni foil after CNT growth at temperature of 450 °C shows similar result as the spectrum of pure Ni. There are only weak peaks at D line and G line for spectrum line a, which may be caused by the small amount of amorphous carbon deposited on the Ni foil during its exposure to the carbon feedstock. This result can further prove that no CNT was deposition at temperature of 450°C.

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(a)

(b)

C ₂ H ₂ Concentration	Gaussian Fit: I _G / I _D
5%	0.855434059
10%	0.827116473
15%	0.812871964

Deposition Time (20mbar)	
10mins	0.875016858
20mins	0.862709498
30mins	0.855434059
Deposition Time (10mbar)	
10mins	1.018016082
20mins	0.953768609
30mins	0.855434059
Deposition Temperature	
450 °C	N.A.
550 °C	0.855434059
650 °C	0.830473967
Deposition Pressure	
5mbar	0.953847323
10mbar	1.018016082
20mbar	0.855434059

(c)

Figure 3.10 Raman spectra of CNTs grown on Ni foils with varied deposition parameters. (a) Raman spectra of Ni foil after CNT growth at temperature of 450 °C and (b) pure Ni substrate

3.3.7 Conclusions

The effects of deposition conditions on film thickness, density, diameter and length of CNTs by HFCVD have been studied. The results indicated that by using conventional HFCVD, nanotubes can only be grown above deposition temperature of 450 °C. The film thickness of nanotubes increased as a function of C₂H₂ concentration, deposition time, deposition temperature and working pressure. Deposition temperature followed by deposition time had the most dominant effect on CNTs length. The CNT density can be maintained with the increase in film thickness by applying high pressure of up to 10 mbar. Higher pressure

also encourages the growth of denser and longer nanotubes. The diameter of nanotubes was in the range of 80 to 300 nm.

Taking references to the effects of growth condition on nanotubes, the relationship between the deposition parameters and the nanotube structure was established. A recipe of parameters was used for the following nanotube growth study.

3.4 Growth of Aligned Carbon Nanotubes using HFCVD

Deposition of aligned CNTs can be achieved by a modified HFCVD with biased voltage. In this study, aligned CNTs growth from various catalyst thicknesses were studied using the in-house modified HFCVD, as described in Chapter 3.2.1.1. This study will enable us to understand the effects of catalyst thickness on nanotubes growth and to determine the capability of our modified HFCVD system in depositing aligned CNTs.

3.4.1 Experimental Procedures

Different thicknesses of Ni catalyst layer were deposited on Si <100> wafer by RF magnetron sputtering at room temperature. The thicknesses are 25, 50, 100 and 200 nm.

Prior to the growth of CNTs, all substrates were cleaned with acetone and blew dry with nitrogen. The growth of CNTs was performed in HFCVD at temperature of 600 °C. At the same time, 500V of biased voltage was applied. Upon the growth of CNTs, catalyst layers were annealed for 10 mins in hydrogen at 2×10^{-2} mbar. During this annealing process, a

gas flow of 100 sccm of H_2 was introduced while the temperature ramped up to around 600 °C in the chamber. The growth of CNTs was then activated by introducing 10 sccm of C_2H_2 to the chamber for 30 mins. System was then cooled down to room temperature before the substrates were loaded out.

Contact mode AFM was employed to study the morphology of as-deposited Ni catalyst layers. The surface morphology of the grown CNT films was analyzed by scanning electron microscope (SEM, JEOL JSM 5910LV) at 20 keV. A micro-Raman (Renshaw 1000) spectrometer using a 514.5 nm Ar laser light was used to analyze the CNT films. The laser output power was set to 5 mW during the measurement.

3.4.2 Results and Discussions

AFM images in Figure 3.11 show the surface morphology of Ni films with different thicknesses of catalyst layers. It is found that the Ni films were made up of uniformly deposited nano Ni clusters. The grain size of the nano clusters was increased as the layer thickness increased, however their density decreased with increase in layer thickness. The nano cluster structure was caused by the RF power applied during the sputtering process [183,184] and which was kept constant for all Ni films. For films with longer deposition time, more nano clusters were deposited onto the Ni film. Among these nano clusters some overlapped would merge to form larger Ni cluster, resulting in decreased density of nano clusters on the surface and varied size clusters. With Ni thickness of 200nm, more clusters merged together. The surface was found to consist of large clusters only.

Figure 3.11 AFM images of Ni films with various thicknesses of (a) 25 nm, (b) 50 nm, (c) 100 nm, (d) 200 nm and (e) scanning parameter

CNTs grown by HFCVD on the Ni films were showed in Figure 3.12. The initial morphology of the Ni films has very important effects on the structure. The non-uniform cluster size of Ni film with 100 nm thickness resulted in various diameter nanotubes. On the other hand, Ni films with uniform cluster size, similar diameter nanotubes were observed. Figure 3.13 shows the diameter and density changes of nanotubes as a function of Ni film thickness and nano cluster size. The similar result was also reported elsewhere [185]. The high SEM magnification image in Figure 3.12(e) has shown that varied diameter nanotubes

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were each capped with similar size Ni particle indicating that a “tip growth” mechanism was adapted.

Figure 3.12 SEM micrographs of nanotubes grown on Ni layers by HFCVD with similar synthesis condition. The corresponding thicknesses of the Ni layer are 25, 50, 100 and 200 nm in images (a), (b), (c) and (d), respectively. Image (e) is a high magnification image of the nanotubes. Ni particle with size similar to that of the tube diameter can be observed on the tip of each nanotube.

The alignment of nanotubes is indirectly affected by the initial thickness of the Ni films. As shown in Figure 3.12(a) and Figure 3.12(b), nanotubes films from initial Ni thickness of 25 and, 50 nm are one directionally and well aligned. However the nanotubes from initial Ni thickness of 100 nm and 200 nm are not completely aligned. The variation may be caused by the large diameter nanotubes formed on thicker Ni films. Large Ni particles on the tip of nanotubes are more readily affected by the gas flow in the system, which flow in an opposite direction to the growth. Any movement of the nanotube during its growth is likely to affect the graphene formation, creating defects on the nanotube, resulted in cured nanotubes.

The two graphs in Figure 3.13 show the relationship between the initial Ni thickness and the size of the nano clusters formed on the surface. As the thickness of Ni increased, the size of the nanoclusters formed increased as presented in Figure 3.13(a). The effects of the varied nanocluster sizes on the nanotubes grown are show on Figure 3.13(b). Diameters of the nanotubes grown are similar to those of the nanocluster presented on the surface. It was realized that, controlling the thickness of the catalyst thickness can control the diameter of the nanotubes grown.

Figure 3.13 The average Ni island size versus initial Ni layer thickness (a) and the average nanotube diameter versus average Ni cluster size (b).

3.4.3 Raman analysis

Figure 3.14 shows the Raman spectra of CNTs grown from different thicknesses of Ni catalyst layer by HFCVD. The G peak at 1598cm^{-1} was due to the C-C stretching Raman

active modes, indicating the formation of graphitic layers [179], and the D peak at 1372 cm^{-1} corresponded to the disordered graphite structures, such as caps or defects of nanotubes and amorphous carbon presented can be clearly observed for all nanotubes films [180]. With G peak representing perfect graphene structure higher than the disordered graphene D peak, it was confirmed that all nanotubes grown are well structured. The I_G/I_D intensity ratios for nanotubes from different catalyst thicknesses are similar. It shows that variation of catalyst thickness does not have much effect on the structure of nanotubes grown and the amount of amorphous carbon present. The lacks of the RBM peaks near 200 cm^{-1} to 300 cm^{-1} , corresponding to single walled nanotubes, prove that the nanotubes grown are multiwalled [186,187].

(a)

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(b)

(c)

Figure 3.14 Raman spectra of nanotubes grown on Ni layers with similar synthesis condition. The corresponding thickness of the Ni layer is 25, 50, 100 and 200 nm in images (a), (b), (c) and (d), respectively.

3.4.4 Conclusions

The effects of Ni catalyst layer thickness on the growth of vertically aligned CNTs by HFCVD were studied. A strong correlation was found between the catalyst film thickness with the diameter and density of nanotubes. As for the nano cluster size and density, which determined the structure of nanotubes films grown, they were affected by the initial film thickness. These observations suggest a possibility in controlling the diameter and density of the nanotubes grown by varying the initial thickness of the catalyst layer. It was also realized that for our HFCVD deposited nanotubes, the degree of alignment is largely affected by their diameter. Perfect vertically aligned CNT can only be achieved with small diameter nanotubes.

3.5 Growth of Aligned Carbon Nanotubes using PECVD

From the previous HFCVD study, large diameter CNTs (>400nm) are found not very well aligned and curly. To obtain better vertically aligned and straighter CNTs, a PECVD was employed. The detailed description of this system can be found at pervious Chapter 3.2.1.2. Major problems that affect the growth of aligned CNTs in HFCVD can be eliminated with the special features of our customized PECVD:

1. A “shower head” design of the reactive gas inlet
2. A more stable plasma generator.

All reactive gases enter the PECVD chamber through the narrow hole, which creates a high velocity flow of gases surrounding the substrate. Such gas flow in the system would induce movement to “growing” nanotubes and lead to the formation of curlier tubes. They are particularly visible on the ones with larger Ni particle on their tip. By introducing the reactive gases through a shower head design, not only that it enables a more uniform distribution of gases, it also reduces the gas flow velocity. An uninterrupted and constant plasma supply will allow the aligned growth of CNT to be maintained throughout the process.

3.5.1 Experimental Procedures

Although the mechanism of the two CVD systems is very similar, a study is conducted to ensure that the change of system would not create any significant effect on the

growth of CNTs. Same type of substrate, catalyst and similar growth parameters from our previous set of experiments were applied and repeated with the use of PECVD.

Firstly, 25, 50, 100 and 200 nm of Ni catalyst layers were deposited on Si <100> wafer by RF magnetron sputtering at room temperature. The substrates were then cleaned with acetone and blew dry with nitrogen. The growth of CNTs was performed in PECVD at temperature of 600 °C. Concurrently, plasma generated by 500V of biased voltage was applied. Upon the growth of CNTs, catalyst layers were annealed for 10 mins. During this annealing process, H₂ was introduced while the temperature ramped up to around 600 °C in the chamber. The growth of CNTs was then activated by introducing of C₂H₂ to the chamber for 30 mins. System was then cooled down to room temperature before the substrates were loaded out.

The surface morphology of the grown CNT films was analyzed by scanning electron microscope (SEM, JEOL JSM 5910LV) at 20 keV. A micro-Raman (Renshaw 1000) spectrometer using a 514.5 nm Ar laser light was used to analyze the CNT films. The laser output power was set to 5 mW during the measurement.

3.5.2 Results and Discussions

Figures 3a-3d show the SEM micrographs of the resulted CNTs from PECVD. The images are aligned next to the images of the CNTs from HFCVD with the same initial catalyst thickness.

Figure 3.15 SEM micrographs of nanotubes grown on Ni layers by PECVD and HFCVD with similar synthesis condition. The corresponding CNTs by PECVD with thicknesses of Ni layer are 25, 50, 100 and 200 nm in images (a), (b), (c) and (d), respectively. The corresponding CNTs by HFCVD with thicknesses of Ni layer are 25, 50, 100 and 200 nm in images (e), (f), (g) and (h), respectively.

It was found that similar deposition trend applied to both samples deposited by HFCVD and PECVD. As the thickness of Ni layer increased, the diameter of the nanotubes grown also increased. Nevertheless, there are some differences between the two set of samples. The CNTs deposited from PECVD have shown significant improvement in their alignment. Especially for samples with initial Ni thickness of 100 nm and 200 nm, the large CNTs are much more vertically aligned than the ones by HFCVD. For thinner Ni catalyst layer (25 nm and 50 nm), the diameter of the PECVD deposited nanotubes were found to be larger than the ones that deposited by HFCVD.

Figure 3.16 The average CNT diameter versus initial Ni layer thickness for HFCVD and PECVD system

3.5.3 Conclusions

It has been demonstrated that PECVD is more superior in depositing aligned CNTs than the modified HFCVD system. The nanotubes are perfectly aligned, even for nanotubes with very large diameter. Since better aligned CNTs are more suitable as interconnect material, PECVD system will be employed for the following experiments.

4 Under CNT Metallization Layers for CNT Growth

In packaging technology, under bump metallization (UBM) is the interface metal layer system between the interconnect and circuitry bond pad. It is an essential component within the flip chip structure as it is needed to provide a strong, stable, low electrically resistant connection between the interconnect and the circuitry. There are several requirements that UBM must meet: it must adhere well both to the underlying circuitry material and to the surrounding IC passivation layer. It should hermetically seal the circuitry materials from the environment. The UBM also provides a strong barrier to prevent diffusing of interconnect material into the underlying layers. The widely used UBM compositions are Al-Cr-Au, Cr-Cu, Ti-TiW-Cu, Ti-Ni-Al, etc. [188-191]. Figure 4.1 shows a typical solder bump interconnect with Metal/Cr/Au UBM for flip chip packaging.

Figure 4.1 (a) Typical solder bump with UBM for flip chip packaging

For CNTs to be integrated in electronics device as interconnect material, they would need to be deposited unitedly with multi metal layer system such like UBM. Therefore, the ability to control deposition of CNTs with the consideration of underlying metal layer configuration is necessary. However, most of the CNT deposition studies conducted so far have been focusing solely on CNTs by catalyst with silicon or quartz substrate and the effects of using multi metal layer system as the catalyst supporting layer were seldom taken into account. The deposition trends that have been concluded from the existing CNT deposition studies might no longer applicable to CNTs deposited on multi metal layer system, as the catalyst layer might be significantly affected by the multi metal layers system under it.

4.1 Effects of Catalyst Supporting Layer

Understanding the role of metal supporting layer in CNT deposition process is essential for designing the suitable UBM for CNT deposition. Cu and Al are commonly used in IC technology, while Cr is the common barrier layer, hence investigating the effects of using them as supporting layer for catalyst would be necessary. In this set of experiments, Cu, Al or Cr was deposited as catalyst supporting layer for Ni catalyst and their effects are studied by PECVD

4.1.1 Experimental Procedures

Silicon <100> with 500 nm of silicon oxide or metal deposited onto silicon <100> with 500 nm silicon oxide was used as substrate for CNT growth. The metal supporting layers Cu, Al or Cr were first individually deposited on Si <100> wafer with 500 nm of

silicon oxide as insulating layer. Subsequently, a 50 nm of Ni film was deposited as catalyst layer on the metal layer or bare silicon with 500 nm of silicon oxide. All metal layers were deposited by magnetron sputtering at room temperature. The catalyst and its supporting layer deposition processes were carried out in a high vacuum environment by the same sputtering system. Si substrates were only unloaded after both metal supporting layer and Ni catalyst layer were deposited, to prevent oxidation of the supporting metal layer.

For CNT growth, all samples were cleaned with acetone and blew dry with nitrogen before loaded into the PECVD chamber. The nanotubes growth condition was kept constant for all samples. Growth temperature for nanotubes was held at 600 °C. Prior to the growth of nanotubes, substrates were annealed for 10 mins in hydrogen at the pressure of 2E^{-1} mbar. During this annealing process, a gas flow of 100 sccm of H_2 was introduced while the temperature was ramped up to 600 °C in the chamber. The growth of CNTs was then activated by introducing 10 sccm of C_2H_2 to the chamber for 10 mins. At the same time, 500V of biased voltage was applied during the growth of nanotubes. The system was then cooled down to room temperature before the substrates were unloaded. The surface morphology of the CNT films was analyzed by scanning electron microscope (SEM, JEOL JSM 5910LV) at 20 kV. A micro-Raman (Renshaw 1000) spectrometer with a 514.5 nm Ar laser light was used to analyze the grown CNT films. The laser output power was set to 5 mW during the measurement.

4.1.2 Result and Discussions

4.1.2.1 Effects of Catalyst Support Layer on the Growth of Carbon Nanotubes

Figure 4.2 shows the micrographs of nanotubes grown on Ni catalysts without metal supporting layer and with Al, Cu and Cr supporting metal layers by PECVD, growth condition was kept constant. It was discovered that certain support layers affected the growing process significantly.

CNTs grown from Ni catalyst without the metal support layer are shown in Figure 4.2(a). It was observed that the nanotubes are high in density and with a uniform diameter of around 80 nm. Small diameter nanotubes are more likely to be affected by van der Waals force between them and the nanotubes are not fully aligned, but with their tips slightly bended towards each others. As silicon oxide is a more stable material at high temperature in comparison with metal, it is believed that they did not react with Ni catalyst layer as much as metal supporting layer. Therefore, the CNTs should be grown from the thin Ni layer with a small amount of silicide and resulted in the small diameter.

When Al was used as supporting layer, no growth of nanotubes was obtained. From the SEM image as shown in Figure 4.2(b), only particles with diameters ranging from 100 nm to 1 μ m can be observed on the surface of the substrate. The melting temperature for Al is 650 $^{\circ}$ C, which is close to the process temperature, so it is believed that Al should be in liquid state and formed a liquid Al-Si layer under the Ni catalyst during the growth process. It has been reported that Al-Si would form during high temperature nanotubes synthesis

process. Such high solubility of this Al-Si layer might embed and trap the Ni clusters [192, 193]. As there was no catalyst material exposed on the surface, growth of nanotubes was inhabited.

In contrast to that, the SEM images in Figure 4.2(c) and Figure 4.2(d) show well grown, one-directionally aligned nanotubes with uniform diameter were grown on Ni with Cu and Cr as supporting layers. The density of nanotubes deposited with Cu was also similar to that on Cr supporting layer. But the diameters of the nanotubes on Cr were smaller (~150 nm) than that on Cu (~200 nm). Even though the process temperature is yet to reach the melting point of Cu (1050°C), it is possible that the high growth temperature may have caused interaction between the Ni nanocluster and Cu supporting layer to result in the formation of NiCu alloyed clusters. Nanotubes were suspected to grow from those NiCu nanoclusters rather than pure Ni. Despite the fact that Cu does not have direct effect on the nanotubes growth, the formation of Cu-M alloy with M begin ferromagnetic catalyst metal such as Ni has been reported [194, 195] not to courage nanotubes growth. The larger diameter nanotubes observed on Cu may due to the interaction of the Ni catalyst layer with Cu. During the annealing process, interaction and diffusion of Ni into Cu might have increased the thickness of the active catalyst layer. This thicker catalyst layer then formed into larger catalyst clusters, resulting in larger diameter nanotubes.

Cr has been commonly used as barrier layer for wafer processing due to its high resistance to diffusion. Since the process temperature was much lower than the melting point of Cr (around 1800 °C), it is believed that the interaction between Cr and Ni should be

minimal, therefore Cr did not affect the Ni clusters as much as Al and Cu for the nanotubes growth. However, certain degree of alloying between Cr and Ni still occurred, and so slightly increased the active catalyst clusters thickness, causing it to have nanotubes that are larger than those which are directly grown on silicon oxide.

Figure 4.2 SEM micrographs of nanotubes grown on Ni layer without metal supporting layer and Ni layers with different supporting metal layers. The corresponding supporting layer in images (a), (b), (c) and (d) are without metal layer, Al, Cu and Cr respectively.

The phenomenon of nano particles subsiding into metal substrate has also been experimentally shown by Ajayan and Marks [196]. They suggested that the propensity of a nano particle to subside is sensitive to the surface free energy of the substrate. This finding is

in close agreement with our experiment results – the surface energy for Al, which is believed to embed the nano particles more readily, is the lowest when compared to Cr and Cu. In particular, Cr, which is believed to have the least interaction with the catalyst, has the highest surface energy [197].

4.1.2.2 Raman Analysis

The Raman spectra of the nanotubes films grown by PECVD on Ni that are directly deposited on silicon oxide layer and on Cr and Cu as catalyst support layers are shown in Figure 4.3. The first order Raman spectra of both samples presented two strong peaks at around 1350 and 1600 cm^{-1} which are common for typical characteristics of graphitic CNTs. Common appellations for these two peaks are D line and G line, respectively. The G line in these Raman spectra was attributed to the presence of crystalline graphite (sp^2 band), indicating that the nanotubes are highly graphitized. While the D line was attributed to the pentagonal carbon ring in the curved graphite sheet on the nanotubes caps. The D peak also reflected the disordered graphene present in nanotubes as defects and/or as amorphous carbon presented [179]. In nanotubes deposition, these two structures are not desired. Therefore higher I_G/I_D intensity ratio of G and D lines would mean a higher structure quality nanotubes film [180]. It was observed from the samples' Raman spectra that I_G/I_D ratio around one for nanotubes grown on Ni without metal supporting layer and with Cr supporting layer, while the I_G/I_D ratio is the lowest and less than one for nanotubes film on Cu supporting layer. This shows that the nanotubes grown on Cu supporting layer have more disordered graphene structures. This may be caused by the formation of inhomogeneous

NiCu clusters during nanotubes growth. Studies have shown that the inhomogeneous chemical composition of the materials in the catalyst particles would cause different carbon diffusion rate in different locations of the catalyst cluster. Therefore, the growth speed varied at different part of the nanotube [187, 198]. This resulted in forming pentagonal carbon rings and defects on the graphitic cylinder body of the nanotubes.

(a)

Figure 4.3 Raman spectra of CNTs grown on Ni layer without metal supporting layer (a) and Ni layers with Cu (b) and Cr (c) as supporting layers.

4.1.3 Conclusion

The effects of different catalyst support layers on CNT growth by PECVD were investigated. It was found that reaction of the catalyst with its supporting layer has significant effects on the growth of nanotubes. The SEM images show that no nanotubes can be grown when Al was used as catalyst support layer. On the other hand, high density and well-aligned nanotubes were observed on Ni that is deposited on silicon oxide layer and with Cu or Cr as catalyst support layers. From Raman analysis of the nanotubes, it was noted that the Cu catalyst support layer affected the quality of the nanotubes grown. For Cr as catalyst support layer, its effects on the nanotubes growth were minimal. The findings would need to be considered when designing approach to integrate nanotubes into interconnects for integrated-circuit manufacturing.

4.2 Effects of under CNT Metallization Layers on Carbon Nanotubes Growth

UBM in current flip chip technology is often built on aluminum (Al), which is a common choice for electrodes material, because of its low electrical resistivity. However, Al has been shown to inhibit the growth of CNTs. Chromium (Cr) with its high melting point, is frequently used as barrier layer for preventing cross diffusion between layers within UBM. From previous study, Cr has also shown to have minimal effect on CNT growth process. In this study, a multi metal layer system (MMLS) comprising of Al electrode material, Cr barrier layer, and Ni catalyst on SiO₂ substrate was chosen as CNT deposition platform for flip chip interconnect applications. The proposed CNT interconnect structure with the MMLS

system is illustrated in Figure 4.4. Deposition of CNTs without Cr barrier layer within the MMLS system was carried out to determine the functionality of Cr barrier layer in the multi metal layer system. Followed by that, the effects of process parameters such as deposition temperature, C_2H_2 concentration, deposition pressure, and deposition time on the CNT deposition with the MMLS are reported. As SiO_2 is highly stable under high temperature process, the results from MMLS system are compared to Ni/ SiO_2 benchmark system, which composed of Ni catalyst layer directly sited on SiO_2 substrate. This enabled us to identify the effects of MMLS system from the deposition condition. Since Al has been proven to inhabit CNT growth, if the use of this MMLS could enable CNT growth, such system can also be applied to other electrode material with similar issue as Al.

Figure 4.4 Under-CNT-metallization layer Al/ Cr/ Ni catalyst layer for CNT interconnect

4.2.1 Experimental Details

The vertically aligned CNTs were deposited using PECVD system. Prior to the CNT deposition process, MMLS system which consisted of 1 μm of Al electrode material, 100 nm of Cr barrier layer and 30 nm of Ni (Al/Cr/Ni), was deposited on SiO_2 substrate by RF magnetrons sputtering. Similar method was also used for depositing Al/Ni (1 μm /30nm) system and the benchmark system of Ni (30nm) on SiO_2 substrate respectively.

The multi metal layer systems were then transported to the deposition chamber of the PECVD system for CNT growth. During the deposition process, the chamber temperature was ramped up to between 500°C and 800°C with an increment of 100°C/min. Once the temperature had been raised to the required value, annealing was carried out for 2 minutes with 240 sccm gas flow of NH_3 . The NH_3 gas flow was maintained at 240 sccm throughout the CNT growth process. The deposition pressure is then adjusted to values of between 9 mbar to 15 mbar. The CNT deposition was then activated by introducing carbon feedstock C_2H_2 to the chamber. The C_2H_2 concentration was controlled at 5, 10, 15 or 20 %. Concurrently to the introduction of carbon feedstock, plasma power of 80 kilowatts (kW) and ~ 500V bias voltage was applied for alignment of CNTs. The deposition time was varied from 15 minutes to 60 minutes. For each set of experiments, only one parameter was varied, while other parameters remained constant. The default values are shown in Table 4.1.

Table 4.1 Default parameters value of the CNT synthesis process

Deposition Temperature	C_2H_2 Concentration	Deposition pressure	Deposition Time
600°C	10%	13 mbar	15mins

The morphology of the deposited CNTs is observed by SEM JEOL-5910l operating at 15 kV. The crystalline structure of the CNTs was studied by unpolarized visible Raman Spectroscopy with a 514.5nm Ar ion laser excitation.

4.2.2 Results and Discussion

4.2.2.1 Effects of the Absent of Cr Barrier Layer under Varies Deposition Temperature

To prove the necessity of using Cr in the MMLS, nanotubes were deposited with the absence of Cr barrier layer. The Ni catalyst was directly deposited onto Al layer, which was subjected to PECVD CNT deposition processes with temperature ranged from 500 °C to 800 °C, while keeping other parameters constant. The results are compared to those obtained from MMLS system, which has undergone similar deposition conditions. Ni catalyst layer which sat directly on SiO₂ substrate without any metal supporting layer has also been used for CNT deposition. It acted as a benchmark system for comparison propose.

SEM micrographs in Figure 4.5(a)-Figure 4.5(d) show the CNTs from benchmark system with deposition temperature ranged from 500 °C to 800 °C. No deposition of CNTs can be observed from the sample at deposition temperature of 500 °C (Figure 4.5(a)), which is caused by insufficient energy. It is believed that the deposition temperature of 500 °C is too low for nanotubes formation, as C₂H₂ may not able to decompose effectively at this temperature. Also, the low temperature may not provide enough energy for carbon atoms to graphitize [199]. Similar finding was also discovered by Jae-Hee Han et. al. [135]. The

deposition of CNTs only started to occur when the deposition temperature was above 600°C, as shown in (Figure 4.5(b)-Figure 4.5(d)). The average diameter and length vs. deposition temperature for the deposited CNTs on benchmark sample are shown in Figure 4.6(a) and Figure 4.6(b). It was observed that there is an increase in nanotubes diameter and length as the deposition temperature increases. This CNT deposition trend is in good agreement with the one found by Jae-Hee Han et. al. [159].

The absence of CNTs for multi metal layer system without Cr barrier layer at 500 °C, 600 °C, 700 °C and 800 °C was clearly shown in Figure 4.5(e)-Figure 4.5(h), respectively. The white color substances shown in the images are believed to be Ni, with the Al layer underneath. It can be observed that as the temperature increased, the diffusion of Ni into the thick underneath Al layer was getting more severe. From our benchmark system, it has been proven that 500 °C is too low for CNT formation, therefore the focus of this study would be on samples with deposition temperatures of 600 °C to 800 °C. The SEM image for 600 °C in Figure 4.5(f) has shown that certain amount of Ni still present on the surface, however as the temperature approaches 800 °C, almost none of the Ni catalyst can be observed in the image. It is possible that the high thermal energy provided for CNT deposition process leads to serious diffusion of Ni into Al layers. This diffusion between the Ni catalyst layer and the underneath Al metal layer have resulted in a significant decrease in the amount of catalyst material exposed on the substrate surface and consequently prohibited the deposition of CNTs.

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Figure 4.5 SEM micrographs of CNT deposited on benchmark, Al/Ni and MMLS system at different temperatures. Benchmark (Ni): (a) 500 °C, (b) 600 °C, (c) 700 °C and (d) 800 °C. With Al/Ni: (e) 500 °C, (f) 600 °C, (g) 700 °C and (h) 800 °C. With MMLS (Al/Cr/Ni): (i) 500 °C, (j) 600 °C, (k) 700 °C and (l) 800 °C.

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Figure 4.6 Plot of averages nanotubes length and nanotubes diameter as a function of (a-b) deposition temperature, (c-d) C_2H_2 concentrations, (e-f) deposition pressure and (g-h) deposition time for MMLS and benchmark system.

Cr is sputtered as a barrier layer between the Ni catalyst layer and Al electrode layer within MMLS system, which was then used for CNT deposition process at deposition temperatures ranged from 500 °C to 800 °C. Similar to the benchmark system, CNTs can be

observed from MMLS system at deposition temperatures of 600 °C to 800 °C, as shown in Figure 4.5(i)–Figure 4.5(l). By comparing the deposition trend observed from MMLS system to the ones from the benchmark system in Figure 4.6(a) and Figure 4.6(b), it was discovered that the increase trend in nanotubes diameter and length as the deposition temperature rises, applies to CNTs from both MMLS and benchmark system. Under close comparison of the nanotubes from MMLS and benchmark system, it can however be found that the deposition rate is slower for MMLS system. The diameter of the nanotubes deposited is also found to be larger for the MMLS system. These phenomena can be explained by the increase in thickness of the effective catalyst layer. Although the process temperature is far from Cr melting point, certain interaction between the Cr layer and Ni catalyst layer may still takes place and result in the formation of NiCr alloyed layer. Even though Cr does not have catalytic effect on nanotubes deposition, the formation of certain metal-catalyst alloy does not discourage nanotubes deposition [200-202]. Thus, nanotubes were suspected to deposit from this relatively thicker NiCr layer rather than pure Ni. Since thicker catalyst layer would form larger catalyst clusters and the diameter of nanotubes is directly proportional to catalyst cluster size, larger diameter nanotubes were deposited [203]. The slower deposition rate of nanotubes from MMLS system can also be explained by the formation of NiAl catalyst layer, as the catalyst layer consisted of Cr, the catalytic effect is affected and therefore reduces the deposition rate. The deposition mechanism of CNTs on benchmark, Al/Ni and MMLS are illustrated in Figure 4.7

Figure 4.7 Illustration of annealed system prior to the CNT synthesis process and post CNT synthesis process on (a-b) benchmark system, (c-d) Multi system without Cr barrier layer and (e-f) MMLS.

4.2.2.2 Raman Analysis

The Raman spectrum for the CNTs deposited by PECVD on MMLS system at various deposition temperatures of 500 °C to 800 °C are shown in Figure 4.8(a) and Figure 4.8(b).

G peaks which situated within the range of 1550 cm^{-1} to 1600 cm^{-1} and D peaks which situated within the range of 1350 cm^{-1} to 1400 cm^{-1} were found on the Raman spectra of CNTs from deposition temperature of $600\text{ }^{\circ}\text{C}$ to $800\text{ }^{\circ}\text{C}$. The G and D peaks are common for typical characteristics of graphitic CNTs. The G peak in the Raman spectra was attributed to the presence of crystalline graphite (sp^2 band), indicating that the nanotubes are highly graphitized. While the D peak was attributed to the pentagonal carbon ring in the curved graphite sheet on the nanotubes caps. The present of those peaks together with the SEM images from the previous chapter further confirms the presence of CNTs at the various temperatures. There are no radial breathing modes which are associated with single walled CNTs [180], thus indicating that the CNTs are multi-walled in nature.

Development of Carbon Nanotubes for Interconnection Applications

(b)

(c)

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(d)

(e)

	500 °C	600 °C	700 °C	800 °C
G-peak (cm^{-1})	Nil	1591.8	1588.2	1589.6
D-peak (cm^{-1})	Nil	1397.0	1394.2	1375.0
	5%	10%	15%	20%
G- peak (cm^{-1})	1591.2	1587.7	1587.3	1590.0
D- peak (cm^{-1})	1393.5	1384.2	1394.2	1375.0
	9mbar	11mbar	13mbar	15mbar
G- peak (cm^{-1})	1588.7	1591.0	1591.8	1593.8
D- peak (cm^{-1})	1392.1	1381.0	1397.0	1386.2
	15 mins	30 mins	45 mins	60 mins
G- peak (cm^{-1})	1586.5	1589.0	1591.5	1590.8
D- peak (cm^{-1})	1390.1	1383.1	1396.0	1386.3

(f)

Figure 4.8 Raman spectra of CNTs deposited on MMLS configuration with different (a-b) deposition temperatures, (c) C_2H_2 concentrations, (d) deposition pressures and (e) deposition time for MMLS and benchmark system. (f) Respective D and G peaks value.

The D peak reflected the disordered grapheme present in nanotubes as defects and/or as amorphous carbon [179]. In nanotubes deposition, these two structures are not desired. Therefore higher I_G/I_D intensity ratio of G and D peaks would mean a higher structure quality nanotubes film. The I_G/I_D ratios were calculated from the areas under peaks and presented for nanotubes from various temperatures in Figure 4.9(a). It shows that there is a drop in the I_G/I_D ratio from 700 °C to 800 °C because of the decrease in defects within the nanotubes at higher temperature. The low temperature limited graphitization of CNTs which increased the condensation of amorphous carbon and so resulted in the lower I_G/I_D ratio for the temperature

of 600 °C and 700 °C. From the SEM images in the previous section (Figure 4.5(l)), the nanotubes formed at a temperature of 800 °C are better aligned as compared to those formed at lower temperatures of 600 °C and 700 °C. This explains the higher I_G/I_D ratio of CNTs formed at 800 °C, as more aligned and well ordered samples correspond to lower I_G/I_D . The higher temperature of 800 °C provides sufficient energy for graphitization of the CNTs and the SEM images show well formed CNTs that are well aligned, thus giving credence to the trend observed in Raman analysis. The trend observed from this study also is similar to that reported by Chhowalla et. al. [161].

Figure 4.9 I_G/I_D ratio for effects of (a) deposition temperature, (b) C₂H₂ concentrations, (c) deposition pressure and (d) deposition time for MMLS and benchmark system.

4.2.2.3 Influence of Different Deposition Conditions

In this section, the CNTs were deposited on MMLS and benchmark system with varying deposition conditions such as C₂H₂ concentration, deposition pressure and deposition time.

The average height and diameter of the CNTs vs. the various deposition conditions are shown in Figure 4.6(c)-Figure 4.6(h).

4.2.2.4 Effects of C₂H₂ concentrations

The C₂H₂ concentrations of 5% to 20% were controlled by the amount of C₂H₂ with respect to the fixed amount of ammonia in the PECVD chamber. From the table in Figure 4.6(c) and Figure 4.6(d), it can be observed that the nanotubes deposited from benchmark and MMLS system have adopted similar deposition trend. As C₂H₂ concentration increases, the deposition rate of the CNTs initially increases and follows by a decrease. The initial increase in deposition rate from C₂H₂ concentration of 5% to 10% is expected as higher concentration of carbon feedstock with sufficient etchant gas NH₃ was presented in the plasma. Under those conditions, the nanotubes are believed to be dominated by vertical growth, which can be used to explain the drop in CNT diameter [161]. However, at C₂H₂ concentration from 15%, the amount of carbon diffused into the catalyst particle has exceeded the rate of vertical graphization, therefore lateral growth has dominated, giving rise to the bigger diameter and slower deposition rate of CNTs. Additionally, as the relative amount of NH₃ presented in plasmas is less for the higher C₂H₂ concentration, the etching rate from NH₃ is reduced. Consequently, it enhanced the deposition of amorphous carbon on the nanotubes structure. Very similar result has also been highlighted and explained by Chhowalla et al. [161].

The graphs in Figure 4.8(c) show the Raman spectra at various C_2H_2 flow rates and the calculated I_G/I_D ratios are presented in Figure 4.6(b). There is a decrease in the I_G/I_D ratio for higher C_2H_2 concentration, as the C_2H_2 concentration provided is beyond the graphitization rate, which results in defects on CNTs as well as deposition of amorphous carbon [161].

4.2.2.5 Effects of Deposition Pressure

Figure 4.6(d) and Figure 4.6(e) show the average diameter and length of nanotubes deposited on benchmark and MMLS system by PECVD in respect to deposition pressure. The general trend of an increase in deposition rate and decrease in diameter of CNTs with increased deposition pressure was applied for nanotubes from both systems. This can be explained by the increased amount of carbon feedstock and reactive gases in the chamber. The increased carbon feedstock has provided more sources of carbon atoms for nanotubes formation and so caused an increase in deposition rate. Unlike in the study regarding the effects of C_2H_2 concentration, the amount of NH_3 in this case has also been increased, which has raised the etching rate of carbon and resulted in CNTs with smaller diameter. Figure 4.8(b) shows the Raman spectra of CNTs from MMLS system with various deposition pressures. Both G and D peaks can be clearly observed from all the samples Raman spectra, which indicate the presence of CNTs. The I_G/I_D ratios of the CNTs (Figure 4.9(c)) increased when the chamber pressures increased from 9 to 11 mbar and followed by a drop for the pressures from 11 to 13 mbar. The I_G/I_D ratios reminded constant for the pressures from 13 mbar to 15mbar. The decrease in the I_G/I_D can be attributed to the high defect content in the

nanotubes. At the high deposition pressures of 11 and 15 mbar, more nucleation sites were formed which resulted in CNTs growing extremely close together and competing for the dissociated carbon feedstock. This increased competition for carbon atoms then contributed to a less perfect graphitization of CNTs, resulting in the sudden decrease in I_G/I_D ratio. The lower I_G/I_D ratio at 9 mbar can be attributed to the reduced available carbon feedstock, which might cause vacancy related defects in CNTs [162].

4.2.2.6 Effects of Deposition Time

Figure 4.6(g) and Figure 4.6(h) show the average length and diameter of the CNTs deposited on benchmark and MMLS system by PECVD from 15 to 60 mins. The length of the CNTs deposited increased with time linearly from 15 to 45 minutes and started to reduce in increment from 45 to 60 minutes. This should be caused by the lifetime of the catalyst particles. Catalyst particles would reduce in their effectiveness overtime, and eventually loss their CNT formation effect. This is caused by the progressive deposition of amorphous carbon layer on the catalyst particles surface, which ‘poison’ the particles and prevented further diffusion of carbon through the catalyst particle [204]. It was believed that as the time increased for the CNT deposition process from 45 to 60 minutes, it has reached the state where the Ni catalyst particles start to reduce its effectiveness, and therefore reducing the deposition rate of nanotubes. Figure 4.8(e) presents the Raman spectra of the CNTs for various deposition times. Their I_G/I_D ratios are calculated and shown in Figure 4.9(d). There is not much variation between the I_G/I_D ratios of CNTs grown for, 15 minutes and 30 minutes. The lower I_G/I_D ratio of CNTs with shorter deposition time is attributed to high

defect content and the higher I_G/I_D ratios with longer deposition times is attributed to a longer time allowed for annealing as well as restructuring of CNTs, resulting in better graphitized CNTs [161].

4.2.3 Conclusion

In conclusion, we have studied the effects of our designed MMLS on the deposition of CNTs by PECVD under various deposition conditions. And the results are summarized in Table 4.2.

Table 4.2 Effects of various parameters on the deposition of CNTs

	With MMLS (Al/Cr/Ni)	
	Deposition Rate	Diameter
+ Deposition Temperature	+	+
+ C ₂ H ₂ Concentration	+ -	+ -
+ Deposition Pressure	+	-
+ Deposition Time	-	-
	Benchmark (Ni)	
	Deposition Rate	Diameter
+ Deposition Temperature	+	+
+ C ₂ H ₂ Concentration	+ -	- +
+ Deposition Pressure	+	-
+ Deposition Time	-	-

+ Increase

- Decrease

+ - Increase followed by decrease

- + Decrease followed by increase

CNTs could not be deposited on Al/Ni system on SiO₂ substrate. This phenomenon is caused by nonexistent catalytic seed areas on the surface of the multi metal layer system for formation of CNTs. This is the result of serious diffusion of Ni catalyst layer into the thick Al electrode layer underneath, as the system was exposed to the high thermal and plasma energy during the PECVD process. The problem can be resolved by adding a Cr layer in-between the Al and Ni layers as studied in this paper. Cr has very high melting point and high resistance to diffusion, thus preventing the Ni from diffusing into the thick Al layer. The study on the effects of varying parameters on the deposition of nanotubes was conducted on both MMLS (Al/Cr/Ni on SiO₂ substrate) and benchmark system (Ni on SiO₂ substrate). As SiO₂ is highly stable at high temperature, the variations of nanotubes deposition under different conditions with the benchmark system are believed to be caused purely by the varied deposition condition. By comparing the results from both configurations, the effects of the multi layer structure and the deposition conditions are identified. It is realized that similar trend of effects was applied for both systems. This suggested that Cr is an effective barrier layer for the deposition of CNTs. The findings would be useful for selection of metal and designing approach of integrating nanotubes in interconnects applications.

5 Joined CNTs in Network – VLSI interconnects

In this section, a detailed description on two novel assembly and joining methods for individual CNTs and CNT bumps are presented. Fabrication of such CNT structure could be a suitable solution for producing on-chip CNT and first level interconnects.

5.1 Reactivation of Residential Catalyst on Tip Grown CNTs for Self - Assembly Three Dimensional CNT Network

Carbon nanotubes (CNTs) have been foreseen as the next generation material for interconnects because of their unusual nano-scale structure, superior electrical, thermal and mechanical properties. They can be used as interconnects for the novel CNT-based components such as: field-effect transistors [205-207], diodes [208] and sensors [209]. In order to realize the fabrication of interconnects with CNTs, engineers must be able to fabricate CNT junctions. Development of advanced assembly techniques has therefore become one of the key factors for nanotubes to have widespread technological application in industry. However, it is difficult to assemble CNT as the pertinent size scales proscribe direct tinkering or bonding. Currently, the methods used for CNT connection rely on sophisticated high cost manual assembly approaches [210-212] and self-assembly process which requires catalyst particles decoration on grown CNTs [213-215] as discussed in Chapter 2. These approaches either destroy the nanotube structure or have difficulty in selecting nucleation sites for redeposition of CNTs. Large scale adoption and integration of CNTs in devices can only be feasible if simple, high yield and large scale CNT assembly processes are available at low cost. In this regard, a self-assembly approach for fabricating three dimensional (3-D)

CNT network was developed, by reactivating the residual catalyst presented on tip grown CNTs. The fabricated self-assembled 3D CNT network consists of arrays of vertical primary aligned CNTs interconnected by lateral two dimensional (2-D) secondary and tertiary CNT networks. This simple and low cost assembly technique can facilitate the fabrication of complex interconnected CNT circuitry. In particular, it provides a solution to the problem of connecting individual CNTs in a self-assembled way as required for interconnects. For consistent and coherent integration into interconnect technologies, the CNT–CNT junction should be electrically conductive. Hence, a comparative study of the electrical transport property of the 3-D CNT network and aligned CNTs in polystyrene was conducted to investigate the electrical behavior of the 3-D CNT network. A proposed CNT on-chip interconnect by the CNT network self-assembly technique is also included in the later section.

5.1.1 Experimental Procedures

The 3-D CNT network was fabricated by a simple two steps PECVD process. Figure 5.1 shows a schematic of the process sequence. A p-type silicon <100> wafer with 500 nm thermal oxide was used as the substrate, and a nickel catalyst layer with a thickness of about 30 nm was deposited onto the substrate by magnetron sputtering at room temperature. The oxide layer between the silicon and Ni catalyst was employed to minimize the migration and aggregation of catalyst nanoparticles formed upon heating. A PECVD system was used to grow CNTs. Once the base pressure in the PECVD chamber reached 2×10^{-2} mbar, ammonia was introduced at a flow rate of 240 sccm and the pressure inside the plasma chamber was maintained at 2.9 mbar. Sample was then heated to 800 °C and annealed for 2 minutes.

Subsequently, acetylene was injected into the chamber at a flow rate of 60 sccm to initiate CNT growth and a 500 V of biased voltage was applied for aligning the CNT growth direction. Simultaneous to the aligned CNT growth, an amorphous carbon (a-C) layer was also deposited onto other areas of the graphite heating plate. The deposited a-C layer could be serviceable for secondary CNT formation in the later process. Throughout the 15 minutes aligned CNT growth process, the chamber pressure was kept constant at 8.2 mbar. For the growth of secondary CNTs, the sample with aligned CNTs was flipped onto the a-C layer which coated on the heating plate. The sample with aligned CNTs was annealed for 2 minutes at 700 °C. During this annealing process, a gas flow of 240 sccm of ammonia was introduced and the pressure was maintained at 2.9 mbar. Then, the sample was then heated to 800 °C and acetylene was injected into the chamber at a flow rate of 50 sccm to initiate the secondary CNT growth. The duration of the secondary CNT growth was 20 minutes and the chamber pressure was kept constant at 13 mbar. The formed 3-D CNT network was then analyzed using a high-resolution scanning electron microscope (SEM, Jeol JSN-5910LV), a field emission scanning electron microscope (FESEM, Jeol JSM 6340F) and a transmission electron microscope (TEM, Jeol JEM 2010) operated at 300 kV. For the TEM analyses, CNTs were transferred to a perforated carbon foil on a copper grid.

Figure 5.1 Schematic of the 3-D CNT network formation process sequence. Deposition of Ni on Si substrate (a), growth of aligned primary CNTs at 800 °C (b), flipping sample onto a-C layer (c), formation of secondary CNTs from the tips of aligned primary CNTs (d), and the 3-D CNT network (e).

The incorporation of 3-D CNT network with polystyrene was performed by free standing method [216,217]. The polystyrene powders were dissolved in a toluene solvent, at a weight ratio of 1 wt% and 2 wt%. The polymer solutions were mild sonicated for 2 hours in a sonic bath and left for 24 hours before use. Then the polymer solutions were spin-coated onto the 3-D CNT network samples at a speed of 500 rpm for 120 seconds. The coated 3-D CNT network samples were then cured for 12 hours at 140 °C for evaporating the toluene. Reference samples were also prepared with pure polystyrene incorporated with aligned CNTs by the same free standing method. These samples were used as benchmark and compared to

the composite samples with 3-D CNT network. All the samples were analyzed using SEM. The electrical properties of CNT-polymer composites were measured by two probes technique using Keithly 197 and Fluke meters. Standard techniques were used to measure I-V characteristics at temperatures of 20 °C and 100 °C. The measurement was conducted under vacuum ($\sim 7 \times 10^{-6}$ mbar), with Ag coating as electrodes at two edges of the nanotubes composites. Wire was directly attached to those electrodes for connection as shown in Figure 5.2. The samples were then placed on a temperature-controlled stage for I-V measurement at high temperature. Voltages from -1 V to 1 V with 50 mV step were applied to the two edges of composites and the current was measured. Repeated cycles of measurements were performed to check the consistency of the data.

Figure 5.2 A schematic of the setup used for performing the measurement.

5.1.2 Results and Discussion

The morphology of vertically grown aligned primary CNT by PECVD is presented in Figure 5.3(a), while Figure 5.3(b) and Figure 5.3(c) depict the distribution of the secondary

CNTs which link the aligned primary CNTs together. The aligned primary CNTs and the secondary CNTs are deposited from the first and second PECVD processes, respectively. From a higher resolution SEM image in the Figure 5.3(d), tens of secondary CNTs can be seen emanating from the aligned primary CNTs. The diameter of these secondary CNTs ranged from 5 to 15 nm, whereas the aligned primary CNTs are larger with a diameter ranged from 100 to 200 nm and an average length of 1 μm . The top view of 3-D CNT network is presented in Figure 5.3(c), showing that the dense mat of secondary CNTs is uniformly formed out from each aligned primary CNT.

Figure 5.3 SEM images of the aligned CNTs and 3-D CNT network. Aligned primary CNTs (a), side view of 3-D CNT network (b), tenths of secondary CNTs emanated from the tip of the aligned primary CNTs (c), and the joint between aligned primary CNTs and secondary CNTs at high magnification (d).

Figure 5(a)-Figure 5(e) present TEM images of the selected aligned primary CNTs and secondary CNTs from the 3-D CNT network. The aligned primary CNTs are found to be tip grown as indicated by the position of the catalyst particle in the tube, as shown in Figure 5.4(a). The TEM images in Figure 5.4(b) and Figure 5.4(c) reveal that both aligned primary CNTs and secondary CNTs are multi-walled CNTs with well-graphitized walls and devoid of amorphous carbon. The emanation of the secondary CNTs from the aligned primary CNTs is also verified from the TEM images in Figure 5.4(d), which shows a secondary CNT with diameter of around 10 nm emanating out from the tip of an aligned primary CNT with diameter of around 100 nm. Further branching of the secondary CNTs has also been observed from the Figure 5.4(e), which shows a tertiary CNT grown out of a secondary CNT tip. The crystallinity of the CNTs within the 3-D CNT network has been confirmed from Raman spectroscopy, which shows the distinguishing G band at $\sim 1,590\text{ cm}^{-1}$ and a D band at $\sim 1,351\text{ cm}^{-1}$ (Figure 5.5)

Figure 5.4 TEM images of the 3-D CNT network. The well structured wall of the aligned CNTs (a), the aligned CNTs with catalyst particle on the tip (b), secondary CNTs (c), secondary CNTs emanated from the tip of the primary CNTs (d), and small tertiary CNTs branching out (e).

Figure 5.5 Raman spectrum of the 3-D CNT network sample with two strong peaks at ~1351 cm⁻¹ (D peak) and ~1590 cm⁻¹ (G peak), which is common for typical characteristics of well structured CNTs

In Figure 5.6(a), a simple growth model is proposed to describe the 3-D CNT network formation process. At the initial stage, the high temperature from the heating plate breaks down the carbon-carbon (C-C) bond within the a-C layer. The detached carbon atoms then diffuse and reach the catalyst particle in the aligned primary CNT tip as shown in Figure 5.6(b). Under the stress of increased carbon concentration within the catalyst particle and with the help from the thermal energy provided by the heating plate, carbon atoms are forced out of the particle in graphitic structure. However, as the catalyst is embedded within the cap of the aligned primary CNTs, the nucleation site is restricted. Hence, the graphitic layers could only emerge discontinuously from different sections of the catalyst particle, leading to the growth of the secondary CNTs. The growth of the secondary CNTs is then sustained by the supply of carbon atoms from the acetylene introduced. Similar to the aligned primary CNTs, the secondary CNTs are grown by the tip growth mechanism, whereby each

secondary CNT is capped by a smaller catalyst particle, which is detached from the larger one located on the aligned primary CNT tip. The catalyst on the secondary CNT tip forms additional nucleation site for tertiary CNT branches. Formation of the connected aligned primary CNTs, secondary CNTs and tertiary CNT branches results in a complex 3-D CNT network as shown in Figure 5.6(c).

Figure 5.6 3-D CNT network formation mechanism. Aligned CNTs with tip in contact with the a-C film and heating plate (a), as the heating plate temperature increases, carbon diffusion from the a-C film to the catalyst particle on aligned CNT tips takes place (b), and formation of 3-D CNT network (c).

5.1.3 Electrical Measurement

Properties characterization of CNT structure is challenged by their nano-scaled feature. As their physical properties are very different from any typical bulk material, common electrical characterization techniques could no longer applied for an accurate measurement. Recently, researchers have developed ways to measure individual CNT properties. In those methods, SEM is usually used for aiding in manipulation and placement of a single CNT to electrodes for measurement. Although these techniques are feasible to individual CNT, those methods are not applicable to special CNT structure, such like our

developed CNT network. Therefore, an indirect approach is developed for characterizing our CNT network. In this method, the CNT structure is embedded into a polymer material as composite and the electrical properties are studied. The polymer matrix can serve as a host and prevent any change or damage of the CNT structure during characterization. And by analyzing the I-V characteristics of the composite, the electrical properties of our CNT network can be better understood.

5.1.3.1 Detail and Background of the Characterization Method

Our conducting CNT network was embedded in polymer for electrical transport study. The polymer matrix allows the unique structure of our developed CNT network to be preserved and hence maintain its initial electrical properties. The embedded CNT network can be considered as conductive filler to the polymer composite. It has been reported that the electrical properties of insulating polymer change dramatically with the present of conductive filler. And this transformation is largely controlled by the embedded filler structure. Over the years, much effort has been put into studying different properties of polymer-filler composite. Mechanism for the conduction within polymer-filler composite has also been well understood. Thus, by obtaining the I-V characteristics of our CNT network-polymer composite and employing the concepts for explaining conduction within filler-polymer composite, we can gain a better understanding on the underlying transport mechanism of the embedded CNT network. This method provides a non-invasive approach for studying the electrical transport of CNT network, which is also applicable for other conductive nano structure.

Before we could analyze the I-V characteristics of our CNT network in the polymer composite, it is necessary to first understand the mechanism behind typical filler-polymer composite's conduction. The charge transport in conductive filler-polymer composites can be explained by two main concepts

(1) Hopping across conducting segments.

(2) Tunnelling between conducting segments

For dispersed conductive fillers in an insulating polymer matrix, the conductive sites are separated by thin layer of insulating polymer matrix. When subjected to electrical field, Schottky barriers formed at those junctions would affect electron flow for conduction. This conduction can be described by Mott's law for variable range hopping and highly anisotropic ('quasi-1D') conduction. In this phenomenon, the electron mobility is largely affected by the applied electric field and temperature. As higher electric field can enable more electrons to overcome the Schottky barrier, the conductivity of the composite would increase with an increase in electric field [218,219]. Similarly, when temperature increased, thermal energy assists and excites more electrons to overcome the barrier, which caused an increase in composite conductance. Affected by these two factors, the I-V characteristic of composite with dispersed fillers has a non-linear nature. The conductivity should also be highly temperature dependent and increase with higher temperature.

For conductive network structure embedded in an insulating polymer matrix, the conductive sites are electrically connected. In such situation, the conductivity of the composite material is largely contributed by electron tunnelling. This is where electrons are tunnelled through the conductive sites without passing through the insulating polymer matrix. As electrons need not overcome large barrier for conduction, electrical field would not have significant effect on the conductivity. When temperature increases, the conductivity would increase with thermal excited electrons, however the effect will not be as significant as in the case of hopping conduction. The electrical behaviour of the composite is mainly determined by the network structure of the fillers and essentially independent from the insulating polymer matrix [218]. If the conductive fillers are electrically connected with ohmic contact, the composites resulting conductivity should have metallic behaviour. In another words, if the IV characteristic of a composite is not electric field dependent (linear characteristic) and low temperature dependent, it proves that the fillers embedded in the polymer are electrically connected.

For these studies, a comparative study of the electrical properties of polystyrene, CNT network-polymer and aligned CNT-polymer were conducted. The data used in the comparison were obtained using the same two probe electrical resistance measurement method and the same specimen configuration. The conventional four probe method can eliminate the effects of contact resistance for electrical measurement. However, this technique is not suitable for very high resistivity sample, like the polystyrene sample in our experiment. Two probe method is one of the standard and most commonly used method for the measurement of insulating and high resistive sample with resistivity beyond the range of

four probe method (reading $>10^6 \Omega$) [219]. Therefore, it has been applied in our experiment. The same measurement set up was used for all samples and so comparative study can be applied, even with the presence of contact resistance.

5.1.3.2 Details and Results of Electrical Characterization

Free standing method was used to incorporate the 3-D CNT network and aligned CNTs into polymer matrix. In order to understand the effects of the free standing method on the as-grown CNT structures, a thin layer of polystyrene was deposited onto the 3-D CNT network and aligned CNTs by free standing method for observation under SEM. Diluted polystyrene solution (weight ratio of 1 wt%) was used in this study. The morphologies of 3-D CNT network and aligned CNTs within the polymer matrix are shown in Figure 5.7(a) and Figure 5.7(c) respectively. It is found that both CNT structures are well dispersed in the polymer matrix and the original structures of the CNTs are not affected. The dispersion of CNTs is required to obtain homogenous electrical properties of the CNT-polymer composites and for the composites to fully exhibit the electrical properties of the 3-D CNT network or the aligned CNTs, the nanotubes should retain their original structure within the polymer matrix.

Figure 5.7 SEM images of the 3-D CNT network and aligned CNT reinforced polymer composites. 3-D CNT network-polymer composites with a diluted polymer solution (a), 3-D CNT network-polymer composites with higher concentration of polymer solution (b), aligned CNT-polymer composites with a diluted polymer solution (c), and aligned CNT polymer composites with higher concentration of polymer solution (d).

A comparative study of the electrical transport property of the 3-D CNT network and aligned CNTs in polystyrene as well as polystyrene was conducted to investigate the electrical behavior of the 3-D CNT network. The CNT network and aligned CNT structure were embedded into polystyrene and their I-V characteristics were measured. The CNT-polystyrene composite system can serve as a desirable specimen for investigating the electrical property of the CNT. The CNT composite samples were prepared with a higher

concentrated polystyrene solution (weight ratio of 2 wt%). Thicker consistent polymer coating with better coverage was achieved on the 3-D CNT network and aligned CNTs as shown in the insert of Figure 5.7(b) and Figure 5.7(d), respectively.

Two point probe technique was used to measure the resistance of the sample. In the two point probe method, two voltage probes are placed at a fixed spacing distance. Voltage from -1 V to 1 V was sent through one probe and passes through the second probe. The current between the two probes is measured. Figure 5.8(a) and Figure 5.8(b) show the I-V plots of the 3-D CNT network and aligned CNT polymer composites at two temperatures (20 °C and 100 °C). By combining the current measurements and the applied voltage into the two surface probes, it is possible to calculate material surface resistance and resistivity using Equation 5.1 and Equation 5.2:

$$R_s = V/I \quad 5.1$$

$$\rho = R (L/W) \quad 5.2$$

Surface resistance, R_s (Ω) is defined as the ratio of a DC voltage drop to the current between two electrodes. The surface resistivity ρ (Ω/sq) is determined by the ratio of DC voltage drop length L to the surface current per unit W . In our case, the dimension for L and W is both 5mm and hence the measured R_s can conveniently assume to be the materials resistivity. The average resistivity of 3D CNT network, aligned CNT composite and polystyrene at room temperature are as shown in Figure 5.9(a). While pure polystyrene is

insulating materials of resistivity $>10^{12} \Omega/\text{sq}$ [220], it shows a considerable lower surface resistivity for polystyrene with CNTs. The 3D CNT network content in the composite has transformed the polymer composite to a highly conductive polymer of resistivity $2.07 \times 10^3 \Omega/\text{sq}$ at room temperature. This resistivity is also one order of magnitudes lower than the surface resistivity ($2.85 \times 10^4 \Omega/\text{sq}$) of the aligned CNT polymer composite. The measured surface resistivity is also lower than that of the free standing CNT composite ($1.67 \times 10^4 \Omega/\text{sq}$) produced by E. Lahiff et al. [218]. The actual surface resistivity of CNT composite is believed to be even lower, as the calculated R_s consisted of both variable of interest R_s and parasitic contact resistance R_c made between the material surface and the probes touching the surface. $2R_c$ as shown in Equation 5.3:

$$R_{\text{total}} = \text{Voltage(V)}/\text{Current(I)} = 2R_c + R_s \quad 5.3$$

Without eliminating the contact resistances, the electrical transport mechanism can still be understood by analyzing the I-V characteristic of the composite materials. At lower temperature of 20°C (Figure 5.8(a)), the 3-D CNT network-polymer composite shows a linear behavior similar to that of metallic material, while semiconducting like nonlinear plot characterizes the aligned CNT-polymer composite (Figure 5.8(b)).

Figure 5.8 I–V measurements performed on the 3-D CNT network-polymer composite at temperatures of 20 °C and 100 °C (a), I –V measurements performed on the dispersed aligned CNT-polymer composite at temperatures of 20 °C and 100 °C (b), and the surface resistivity of the 3-D CNT network and aligned CNT polymer composites at 20°C and 100°C (c)

The composite with 3-D CNT network also has twice the electrical conductivity of that with aligned CNTs at a temperature of 100 °C and the linearity of the I-V plot remains for the 3-D CNT network–polymer composite. For the aligned CNT-polymer composite, the I-V plot is nonlinear. The conductivity of the aligned-CNT composite at 100 °C is also found to be ~7 times higher than that of the sample at 20 °C (Figure 5.8(c)).

Figure 5.9 Surface resistivity of polystyrene and polystyrene with CNTs at room temperature

According to Kaiser's description [221], the conductivity behavior of CNT-polymer composite is governed by two simple models: conduction with hopping or tunneling through small electrical barriers. Based on the I-V behavior of the 3-D CNT network-polymer composite, the most possible mechanism of electron transport is by electron tunneling through the CNTs. In electron tunneling conductivity, the electron transfer is mostly by tunneling through the junction between the connected CNTs, and as a result the electrical properties of the composite are independent from the ones of the host [219]. Consequently, the I-V characteristic of the 3-D CNT network-polymer composite can be clearly understood by studying the electrical properties of the CNT network. In general, there are three

categories of CNTs, namely zigzag, chiral, and armchair. All armchair nanotubes are metallic, as well as one-third of all possible chiral nanotubes. Therefore it can be assumed that the CNTs present in the 3-D CNT network structure contain a mixture of semiconducting and metallic tubes. For quasi-one-dimensional conductors under the conditions that carriers cannot circumvent other barriers or defects to conduction, theory of interrupted metallic conduction has been proposed to explain the mixed metallic/nonmetallic behavior of highly conductive polymer and complex reticulation of CNTs [222]. The high conductance of the 3-D CNT network-polymer composite observed at lower temperature (20 °C) is the outcome of well joined CNTs. When the barriers between the metallic regions are low, a high amount of electron transport can be seen even at low temperature. Alternatively, temperature increase would assist thermal fluctuations tunneling of electron. However, due to the scattering of carriers by phonons, the overall improvement in conductance is limited, which resulted in a high and yet low temperature dependent conductivity of the 3-D CNT network. The highly coupled secondary nanotubes within the 3-D CNT network acted as percolating paths for conduction, so that ohmic behavior with linear I-V plot takes place. The situation is rather different for the case of the aligned CNT polymer composite. Its I-V characteristic is very similar to that of typical dispersed CNT polymer composite and which fits well with the electron hopping model. In spite of the excellent dispersability and wetting of the CNTs in the polymer matrix, there is small distance/gap between the tubes. This small layer of polymer between the nanotubes acts as a large barrier for electron transport. Conduction happens only when electron hopping occurs among the conductive fillers within the matrix. This explains why the conductivity of the aligned CNT-polymer composite is much lower. This intertube barrier is also expected to restrict electron transport at lower applied voltage,

which is the cause for the nonlinear I-V behavior. At higher temperature, the electron transport rate could increase significantly due to the thermal activated electron hopping action. [222-224] As observed from the considerable increase in the conductivity of the aligned CNT-polymer composite at 100 °C.

In respect to electrical performances, 3-D CNT network has shown to exhibit electron tunneling conduction, which is more superior to the electron hopping conduction of dispersed align CNTs. The experimental observations have proven that the 3-D CNT network with unique electrical connectivity is an important material with potential applications in the area of interconnects.

5.1.4 Proposed CNT Network Formation Process for VLSI Structure

The approach of CNT network formation can be used for creating CNT VLSI interconnect system, whereby the aligned vertical CNTs apply as vias and CNT network applies as horizontal interconnects. A schematic diagram of the proposed CNT VLSI interconnect formation is depicted in Figure 5.10(a)-Figure 5.10(c). Active and passive components are fabricated on silicon chip (Figure 5.10(a)) prior to deposition of the separating dielectric (Figure 5.10(b)). By lithography, patterned mask is coving selective areas of the dielectric layer as shown in Figure 5.10(c). The uncovered areas are then etched through the dielectric and stop in the component layers (Figure 5.10(d)). Catalyst material is deposited on the dielectric layer and into the etched area (Figure 5.10(e)). Subsequently, the catalyst material on the dielectric layer is removed with the mask. Active catalyst particles

are formed on the etched area, from which the aligned CNT can be grown using PECVD. Similar process with catalyst chemical vapor deposition (CCVD) of CNT has been demonstrated by Infineon Technologies for the structured creation of single CNT in vias [225]. The connection between the aligned CNT is by the network formation as presented in Figure 5.10(b). Detail description of the CNT network formation process is presented in earlier section. The growing sites of the CNT network could be determined by two factors: the patterned a-C film on the substrate holder and the distance between the aligned CNTs. If connection is needed between the CNTs, they can be placed with a closer distance and with a-C film in contact with their tip during network CNT deposition process as shown in Figure 5.10. This proposed process is highly compatible with current IC processing technology. The active circuitry on the silicon substrate can be fabricated with conventional microelectronics processing techniques. The methods used for creating via structure and the deposition of catalyst consisted of lithography patterning, etching and typical thin film deposition technique, respectively. The most commonly used dielectric layers for IC includes silicon oxide based and polyimide material [226]. Ideally, glass transition temperature T_g of a material should be higher than the highest processing temperature encountered. So, silicon oxide based dielectric material with high glass transition temperature (ranged from 800°C to 1160°C) is recommended for the proposed method, as it can also protect the embedded active circuitry from the high process temperature of CNT growth. The current advances in CNT deposition processes have also proven that CNT deposition can be achieved with a much lower temperature. Recorded in published journals, the deposition temperature can be lowered to a temperature below 400°C [227-228]. Upon the maturity of those low temperature CNT deposition processes, the use of polyimide dielectric with T_g ranged from

around 300 °C to 500°C, e.g. pyromellitic dianhydride-oxydianiline polyimide with $T_g = 377\text{--}400$ °C and biphenyl dianhydride-p-phenylenediamine with $T_g = 477\text{--}500$ °C [228], would also be possible.

Figure 5.10 Proposed CNT network formation process for VLSI application (a) Deposition of components, (b) Deposition of dielectric, (c) Deposition and patterning of mask, (d) Dielectric etching, (e) Deposition of catalyst, (f) Growing of aligned CNTs, (g) Growing of CNT network and (h) Aligned CNTs as vias and CNT network as nanowires.

5.1.5 Conclusions

In this study, self-assembled 3-D network structures of CNTs were obtained by applying a single catalyst deposition and a simple two steps PECVD method. The synthesis of interconnection between CNTs is very critical for the development of CNT interconnection. The formation of 3-D CNT network not only shows the possibility of creating 3-D complex CNT interconnected structures, it could also provide a functional base material for the development of nanoscale biological or electronic devices.

5.2 Join CNT Bump – First Level Interconnects Flip Chip

Lead-content found in common solder poses various problems for interconnect application. Although the use of lead can maximize material strength, and resistance to creep [229], the toxicity of lead [230] is not eco-friendly [231,232]. Lead free alternatives, such as tin-silver-copper [233,234] and tin-copper [235], were developed to replace tin-lead solder interconnection materials [236,237]. Nevertheless, lead-free solder has disadvantages such as higher melting temperatures and low metal surface wettability. Performance wise, lead-free solder properties are close to that of typical solder, with similar electrical, thermal and mechanical characteristic.

In the quest for product miniaturization, integrated circuit (IC) size is reduced inversely proportional to device density [238-240]. As circuit density increases, the number of input/output (I/O) pins on IC packaging increases exponentially with significant drop in pin pitches [241,242]. According to International Technology Roadmap for Semiconductors

(ITRS) [243], the number of packaged pins per chip will continue to increase ~10% each year and will approach as high as 5000 pins for high performance ICs in the coming decade. The peripheral I/O flip chip direct chip attach is predicted to scale down to < 20 μm pitch and area array flip chip packaging is expected to reach 100 μm pitch by the year of 2014. At this scale, current interconnection technology will become an obstacle to provide reliable high speed connections for smaller devices. To address these problems, metal wire-bumped flip chip connection [244,245] was developed. Copper stud bumps [246] were formed using conventional wire-bonding machine as packaging interconnects. This low cost technique offers application simplicity because it enables direct bumping and only requires equipments that are widely available. In addition, Cu also has a much higher electrical and thermal conductivity compared to solder. The disadvantage of metal bumping lies in its serial process. As the number of bumps increases, bumping time increases proportionally. As interconnect miniaturization continues, electromigration and reliability issue will be more apparent when current density in metal interconnection surges.

CNTs are one dimensional nanowire with superior electrical, thermal and mechanical properties. CNTs are also non-toxic and environmentally friendly. For these reasons, they have been considered as future building block materials for many active and passive components within electronic devices [247-250]. In particular, with CNT nano feature size and high resistance to electromigration, they are an ideal material for fabricating sub-micro or nano flip chip interconnects with outstanding performance.

5.2.1 Experimental Detail

Figure 5.11 illustrates the fabrication process sequence of CNT interconnection bumps. Aligned carbon nanotube (ACNT) film is deposited onto two identical Ni coated Cr/Al electrode surfaces, with p-type silicon <100> wafer with 500 nm thermal oxide used as the top and bottom substrates. A 30nm thick of Ni catalyst layer is applied for growing CNTs forest with a desired density of 6 tubes/ μm^2 [204]. The 100nm/1 μm thick of Cr/Al electrode layer and 30 nm thick of nickel catalyst layer are pre-deposited onto the top and bottom substrates by magnetron sputtering at room temperature. A PECVD system is used to synthesize the CNTs. Once the base pressure of 2E^{-2} mbar is achieved in the PECVD chamber, ammonia is introduced at a flow rate of 240 sccm. The pressure inside the plasma chamber is maintained at 2.9 mbar. All samples are heated to 800 °C and annealed for 2 minutes. Subsequently, acetylene is allowed into the chamber at a flow rate of 60 sccm to initiate ACNT growth and a 500 V of biased voltage is applied for vertically aligning the CNTs. The chamber pressure is kept constant at 8.2 mbar, throughout the 60 minutes CNT growth process.

Figure 5.11 Illustration of CNT insertion process sequence (a-c), top view of the assembled sample (d), and cross-sectional view of the assembled sample (e).

To assemble CNT bumps, the samples surfaces with the ACNTs are faced each other in angular alignment, as observed with a low power microscope. Different insertion length of the contacted CNT between the top and bottom substrates is accomplished by placing different amount of weights onto the top substrate. This weight is then removed from the structure. Once interlocking has taken place, the top substrate is supported by the bottom substrate and the two substrates are considered “joined”. The minimum load applied for interlocking is 0.03 g which is benefited from the top substrate weight and the maximum load used is 3.00003 kg.

The cross sectional images of the assembled samples are observed using a high-resolution scanning electron microscope (SEM, Jeol JSN-5910LV) for determining the length of CNT penetration region. Electrical properties of the “inserted” structure are measured by four point probe technique using Keithly 230 programmable voltage source and Keithly 590 CV analyzer. A current is applied across the “inserted” CNTs through probes 1 and 2, which are connected to one side of the top and bottom CNT substrates, respectively. The voltage drop of the CNTs is then measured between probes 3 and 4, which are connected to the other end of the top and bottom substrates, respectively. An illustration of the measurement set up is shown in Figure 5.12 and the applied current ranges from 50 mA to -50 mA with a 10 mA interval. Reference sample was prepared using silver as the interconnect material with similar set up. This sample is used as benchmark and the electrical performance is compared to that of the “inserted” CNT structure. Repeated cycles of measurements were performed for all samples to check the consistency of the data.

Figure 5.12 A schematic of the four-point-probe measurement set-up. The current is applied through probes 1 and 2 and the voltages measured between probes 3 and 4

5.2.2 Results and Discussion

The morphology of vertically grown primary ACNTs is presented in Figure 5.13(a). The ACNTs have an uniform diameter of around 200 nm and an uniform length of around 15 μm as shown in Figure 5.13(b)-Figure 5.13(e). These images illustrate that the CNT bumps from the top and bottom substrates have interpenetrated and interlocked. Predictably, the degree of interpenetration of the CNT bumps has shown to be consistent with the amount of the assembly force applied. The corresponding “penetration” length to the amount of assembly force is shown in Table 5.1. SEM results in Figure 5.13(b) shows the penetration of CNT in test vehicle 1, under no additional loading condition. In this condition with only the weight of the substrate at 0.03 g acting on it, the CNT penetration length is measured to be around 3.5 μm (~23% of the CNTs length). Whereas for test vehicle 4, shown in Figure 5.13(e), the largest assembly weight of 3.00003 kg has enabled full interpenetration length of 15 μm . Enabling the tips of the CNTs from the top substrate to have contact with the surface of the bottom substrate and vice versa. SEM image of the CNT bump that has went through 50 cycles of interpenetration and detach process is presented in Figure 5.13(f). It reviews that the interpenetration action does not cause any damage to the CNT bump structure. In another word, the process is considered reworkable, which allows easy readjustment and replacement of components if used as interconnects for flip chip packaging.

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Figure 5.13 SEM images of the as grown CNT bump (a), the cross sectional views of the CNT structures after their assembly process: test vehicle 1 (b), test vehicle 2 (c), test vehicle 3 (d) and test vehicle 4 (e), and the CNT bump that has went through 50 cycles of interpenetration and detachment processes (f).

Table 5.1. The corresponding “penetration” length of CNTs versus the assembly force

Test vehicle	1	2	3	4
Force (Kg)	0.00003	1.00003	2.00003	3.00003
Penetration length (μm)	3.6	7.3	11.1	15

For interconnection applications, it is desired that the contact resistance between the interconnect bump and bond pad or electrode can be as low as possible. Conventional way of joining CNT bumps by metallic adhesive [48] may provide reasonable mechanical adhesion, however often encountering problems such as high contact resistance. This high contact resistance is caused by the unique electronic structure of nanotubes, which gives rise to weak electronic coupling at the Fermi surface [251-253]. This is due to the weakly bonded metal-CNT contact made at the tip of the as-grown CNTs. Improved electron transport seems feasible using the penetration method, as the weak metal-CNT contacts are replaced by the CNT-CNT contacts. The electrical behavior of CNT-CNT contacts is predicated to resemble directional graphene-graphene stacking. A simple four point probe measurement set up for measuring the current to voltage (I-V) characteristic of CNT test vehicles is shown in Figure 5.12. The measured voltages are presented in Figure 5.14, with applied current varying from 50 mA to -50 mA. The measured resistance value is composed of the probe-to-electrode contact resistances, the electrode-to-CNT contact resistances, and the intrinsic resistance of the CNT bump. Hence, the obtained results are analyzed by comparing to that of a test vehicle with silver paste as interconnect material. The linear I-V curve in Figure 5.14(b) indicates the metallic characteristic of the as-grown multi-walled CNTs as well as the ohmic contacts between the CNTs. The resistance of the CNT test vehicle is found to be magnitudes

lower than that of test vehicle with silver paste as presented in Figure 5.14(a). Based on theoretical calculation and experimental measurements, CNT bumps exhibit very low intrinsic resistance, which is much lower than typical metal. The lower resistance of the CNT bumps suggests that the total contact resistance presented in the system is low enough for the test vehicle to benefit from the excellent electron transport properties of CNTs, therefore showing lower resistance than the test vehicle with silver paste. Resistance of the inserted CNT structure is also found to decrease with the increase in the penetration depth as presented in Figure 5.14. The linear decrease in resistance with increase in penetration depth further proves that the CNT-CNT contacts are having metallic behavior and are ohmic. The lower resistance measured from the interpenetrated CNT structure has demonstrated the advantage of our approach with respect in creating low contact resistance, CNT-based interconnects.

Figure 5.14 I-V measurement of test vehicle 4 with inserted CNT bump and silver paste (a) and test vehicles 1 to 4 (b).

5.2.3 Proposed CNT Flip Chip Interconnect Formation Process

The CNT ‘insertion’ technique can be used as interconnection bump in flip chip packaging system. A schematic of the proposed CNT interconnect formation is depicted in Figure 5.15(a)-Figure 5.15(c). For fabricating CNT flip chip interconnection, metallization layers followed by catalyst layer on IC die and its carrier are first deposited. Lithography technique is used for patterning the metallization layers and catalyst layer as presented in Figure 5.15(a). Upon removal of the mask and the formation of patterned metallization layers and catalyst layer, ACNTs are grown on the patterned IC and carrier (Figure 5.15(b)). Subsequently, the IC can be flipped and aligned with its carrier for bonding (Figure 5.15(c)) by typical flip chip packaging alignment equipment. With the appropriate amount of force applied onto the IC, the CNT bumps on the IC and its carrier will insert and joined as shown in Figure 5.15(d). The proposed process is based on current IC packaging technology, therefore it can be easily incorporated into current production with minimal effort. The active circuitry within the IC is embedded into silicon chip and which should enable it to withstand the high process temperature of CNT growth. For more temperature sensitive IC, low temperature CNT growth technique can be applied to prevent any damages to the delicate IC [229,230].

Figure 5.15 Proposed CNT insertion process for flip chip application. Deposition of under CNT metallization and catalyst layer (a), deposition of CNTs (b), Align die to its carrier (c), and assembly of die to its carrier with downward force (d).

5.2.4 Conclusions

Simple insertion assembly technique for PECVD deposited CNT bumps leads to the formation of highly electrical conductive structure for flip chip interconnect application. The CNT bumps from top and bottom substrates have shown to adhere well to each other and

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exhibit low contact resistance. The measured total resistance is lower than that of silver paste, thus illustrating the feasibility of low resistance CNT-based interconnects.

6 Conclusion and Recommendation

The main objective for this study lies in the exploratory study of the application of CNTs to interconnect and gains comprehensive understanding on issues related to utilizing CNTs and their potential in the field of interconnect technology. In this study, for CNT to be applied as VLSI and first level flip chip interconnect material, two novel joining techniques for individual CNTs and CNT film were developed and electrically tested. In order to incorporate CNT into electronics applications, an under CNT metallization system has been designed. The effects of different deposition conditions on CNT structure which enables better control in CNT morphology have also been studied.

This conclusion and recommendation chapter is divided into two parts: (1) summary of experiments on different part of this study with their results and discussions and (2) suggestions on future work for further development.

6.1 Summary of Experiments

Two easily adaptable methodologies for joining individual CNTs and CNT bumps were developed. The joining method for individual CNTs is a self-assembly two step PECVD CNT deposition process – A layer of tip grown aligned CNT film is first deposited on selected region of the substrate. Upon the completion of the first PECVD process, no chemical treatment was conducted on the CNT film for sustaining the Ni catalyst particle on the tip of the CNT. The substrate with aligned CNT film is then flipped and with the tip of the aligned CNT in contact with an a-C coated substrate holder for the second PECVD CNT

deposition process. The carbon atoms, which diffuse from the heated a-C film into the Ni catalyst particle on the CNT tip, would then activate the secondary CNT growth. Those smaller secondary CNT with diameter of less than 10 nm would bridge the primary aligned CNTs and create a network structure. Electrical measurement was conducted on the CNT network and electron tunneling behavior was observed. This indicated that current was able to flow through the primary aligned CNTs by using secondary CNT as interconnect. Our method enables the formation of CNT network without the need to embrace the current sophisticated methods that are very low in yield and high in cost. The lack of post chemical processing in our process also prevents damage to the CNT structure, which might downgrade its excellent properties. The self-assembly nature of our method also enables the formation of covalent bonded CNT junctions, which allows electrical transport with low electrical barrier.

Another joining method was developed for joining PECVD deposited CNT bumps, which is an easily adaptable process applicable in the first level flip chip interconnect. In this method, first level interconnects pads on both die and its carrier are first deposited with high density aligned CNT bumps. By employing typical flip chip bonder, the flipped die and its carrier can be aligned with the CNT bumps facing each other. The die and carrier can then be assembled by applying a downward force to the die and forcing the CNT bumps on die to be “inserted” into the ones on its carrier. Electrical measurement was conducted on the assembled CNT structure and was compared to similar structure assembled with silver paste. The conductivity of the CNT bump was found to be magnitude higher than that of the silver paste, demonstrating a much superior electrical properties over typical metal. It is impractical

for the industry to embrace a new interconnect technology that requires changing out their expansive flip chip fabrication equipments. Therefore our developed method is also more easily adaptable for the industry.

An under CNT metallization system was designed for incorporating CNTs to electrical application. The effects of different under metallization layers such as Al, Cu and Cr on the CNT growth by PECVD were studied. It was realized that the use of Al as under CNT metallization layer would prohibit the growth of CNTs, as the serious diffusion of Ni catalyst to the Al layer has prevented the exposure of Ni to the carbon feedstock. CNT grown on Cu has found to have bigger diameter and Cr has found to have minimal effects on the CNT growth. With the understanding on the influence of the different metallization layers on CNT, a multi metal layer system (MMLS) of Ni/Cr/Al is developed. Ni is the catalyst layer, while Cr is the barrier layer. Al is selected to be the electrode material. The use of this MMLS has proven to enable better control of CNT growth with minimal effects from its under metallization layer.

Different effects of the growth parameters and catalyst layers on CNT growth by HFCVD and PECVD were studied. The results indicated that nanotubes cannot be deposited with temperature below 500 °C. It also has shown that nanotube film thickness increased as a function of C_2H_2 concentration, deposition time, deposition temperature and working pressure. Deposition temperature followed by deposition time has the most dominant effects on the CNT length. The CNT density can be maintained with the increase in film thickness by applying higher deposition pressure. Higher deposition pressure also encourages the

growth of denser and longer nanotubes. Our experiments also demonstrated that by controlling the thickness of catalyst layer, the CNT diameter can be controlled. And the CNTs deposited from PECVD were found better aligned than the ones from HFCVD. With the understanding on CNT growth environment, growth parameters, and catalyst effects, growth conditions can be configured for CNT film deposition that is suitable to interconnect application.

6.2 Future Work

Three possible areas that could be further focus on with this work are listed below:

1. Theoretical studies on the formation of the CNT network. Work in this area could be assisted by existing literature and theoretical modeling of CNT growth. This could aid in understanding and better control of the developed process.
2. Fabricate the CNT interconnect structure with the proposed CNT joining techniques. Characterization of such interconnects structure and compared to that of current interconnect material. It could test the feasibility of those techniques in actual interconnect applications.
3. Develop an appropriate electrical characterization technique for CNT film. Currently, most of the techniques used for measuring CNT electrical conductivity are for individual tubes. There is lack of standard procedures and process for measuring CNT film properties. By developing such technique,

the effects of morphologies of nanotube film and interactions among the nanotubes on the overall electrical conductivity can be studied.

Appendix I: List of Publications

Patent filed

1. Patent 200705183-2: A method for electrical interconnection and an interconnection structure
2. ID-J-07-025: A method for forming three dimensional carbon nanotubes network

Submitted papers

1. K.P. Yung, J. We and B.K. Tay, “Formation and assembly of carbon nanotube bumps for interconnection applications”, Diamond and Related Materials, (under review)
2. K.P. Yung, J. We and B.K. Tay, “Self assembled three dimensional network of carbon nanotubes (CNTs)”, Diamond and Related Materials, (under review)

Published papers

1. K.P. Yung, J. Wei, B.K. Tay and Z.F. Wang, Effects of under CNT Metallization Layers on Carbon Nanotubes Growth, Modern Physics Letters B, v22, n19, 1827(2008)
2. K.P. Yung, J. Wei, B.K. Tay and Z.F. Wang, Effects of Catalyst Layers on growth of carbon nanotubes growth, Material Research Innovations, v 10, n 3 84(2006)

3. E. Teo, K.P. Yung, C. Chau and B.K. Tay, Carbon nano-mattress, *Advanced Materials*, 19, 2941(2007)
4. X.B. Yan, B.K. Tay, Y. Yang and K.P. Yung, Fabrication of three-dimensional ZnO-carbon nanotube (CNT) hybrids using self-assembled CNT micropatterns as framework, *Journal of Physical Chemistry C*, v 111, 17254(2007)
5. P. Zhang, B.K. Tay, Y.B. Zhang, S.P. Lau and K.P. Yung, The reversible wettability of Ti containing amorphous carbon films by UV irradiation, *Surface and Coatings Technology*, v 198, n 1-3, 184(2005)

International conference

Published papers

1. K.P. Yung, J. Wei, B.K. Tay and Z.F. Wang, CVD growth of carbon nanotubes on different combinations of catalyst layer and substrates, *Proceeding of Nanotech 2004 Conference*, Singapore
2. K.P. Yung, J. Wei, Z.F. Wang and B.K. Tay, Morphology and microstructure of carbon nanotubes grown by hot filament chemical vapor deposition, *Proceeding of the 6th Electronics Packaging Technology Conference (EPTC2004)*, Singapore, 138(2004)

3. K.P. Yung, B.K. Tay Z.F. Wang, J. Wei and A. Chandrasekaranb, Effects of catalyst on carbon nanotubes growth, Proceeding of International Conference on Materials for Advanced Technologies (ICMAT 2005), Singapore
4. K.P. Yung, J. Wei and B.K. Tay, Effects of catalysts support layer on carbon nanotubes growth, Proceeding of ASME International Mechanical Engineering Congress & Exposition (IMECE 2005), Orlando, Florida, 247(2005)
5. K.P. Yung, J. Wei and B.K. Tay, Electroless plating of nickel on carbon nanotubes film, Proceedings of 7th Electronics Packaging Technology Conference (EPTC 2005), 636(2005)
6. K.P. Yung, Z.F. Wang, J. Wei and B.K. Tay, Effects of a-C:Fe catalyst deposition method on the growth of carbon nanotubes,,: Proceeding of IEEE Conference on Emerging Technologies - Nanoelectronics (NanoSingapore 2006), 388(2006)
7. K.P. Yung, J. Wei, Z.F. Wang and B.K. Tay, Growth of carbon nanotubes on metal containing amorphous carbon films, Proceeding of ASME International Mechanical Engineering Congress & Exposition (IMECE 2007), Seattle, Washington, 43(2008)
8. K.P. Yung, J. Wei, Z.F. Wang and B.K. Tay, Carbon Nanotubes (CNTs) as Conductive Filler for Polymer Composite, IEEE International Nanoelectronics Conference 2008 (INEC 2008), Shanghai, China

9. K.P. Yung, J. Wei, Z.F. Wang and B.K. Tay, Formation of Carbon Nanotube-Polymer Composites with Different Concentrations of Polystyrene Solution, Proceedings of the ASME International Mechanical Engineering Congress and Exposition, IMECE 2008, Boston, Massachusetts

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