Analysis of high-dielectric constant gate stack reliability for nanoscale CMOS devices application via scanning tunneling microscopy

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**NANYANG
TECHNOLOGICAL
UNIVERSITY**

**ANALYSIS OF HIGH-DIELECTRIC CONSTANT GATE
STACK RELIABILITY FOR NANOSCALE CMOS
DEVICES APPLICATION VIA SCANNING TUNNELING
MICROSCOPY**

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MICROSCOPY**

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SUMMARY

The novelty of this study lies in the application of the scanning tunneling microscopy (STM), to study the electronic properties of the high- κ gate stack at nanometre scale. The samples are the $\text{HfO}_2/\text{SiO}_x$ and the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stacks.

Based on tunneling and energy band theory, the polycrystalline structure with grain size of ~ 27 nm of the high- κ and the amorphous SiO_x can be imaged independently at different biasing polarity. The polarity dependent STM current can therefore allow the demarcation of electronic traps in the high- κ and the SiO_x layer. This allows the evolution of electronic traps in each layer to be separately probed and studied under process condition change and electrical stress.

By subjecting the high- κ gate stack to different post-deposition annealing (PDA) temperatures, electrical weak spots and non-uniformity induced by PDA can be revealed by STM. Lateral resolved I - V characteristics extracted from leakage sites are found to exhibit either stress induced leakage current (SILC) or barrier height lowering (BHL) behaviors. STM observation of thermally induced localized low resistance path under tip injection and increase in leakage sites density in annealed gate stacks explain the reduced Weibull slope upon PDA.

Intrinsic breakdown mechanism is studied in an area without pre-existing traps. High- κ layer is observed to have a larger trap generation rate as compared to the SiO_x layer. This can be explained by a higher anode hole injection coefficient due to a higher surface plasmon generated hot-hole current at the W tip/high- κ interface.

Characteristics of the electronic traps are shown to have significant influence on trap evolution in the gate stack under electrical stress. We show that: (i) SILC traps

near the cathode inhibit trap generation in the dielectric layer near the anode. We attribute this observation to an inelastic-trap-assisted-tunneling model; (ii) SILC traps near the cathode may evolve into BHL as lattice displacement due to electron charging which occurs physically at the trap location could accelerate the wear-out of the neighboring region; and (iii) traps with BHL characteristics at the anode could accelerate the breakdown of the dielectric layer next to the cathode due to enhanced electric field.

In addition, correlation of the leakage current to oxygen-vacancy defects is demonstrated. Oxygen-vacancy is proposed to be one of the major defect structures in a high- κ dielectric which results in the formation of localized leakage current, hence electrical non-uniformity of the gate stack. A change in conduction mechanism and improved electrical uniformity are observed when a sample with a high density of oxygen-vacancy is subjected to N₂ annealing. A possible structure of the nitrogen-passivated oxygen-vacancy is proposed based on the localized electrical property and physical characteristics obtained by x-ray photoemission spectroscopy and transmission electron microscopy. The conduction mechanism of the annealed sample is proposed to be space-charge-limited-current (SCLC). Improvement in the breakdown strength of the high- κ gate stack subjected to ramp-voltage-stress is also observed after N₂ anneal. The improvement may be related to a limited current flow through the gate stack in the high stress voltage regime due to SCLC.

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LIST OF ABBREVIATIONS

AFM	atomic force microscopy
ALD	atomic layer deposition
BEEM	ballistic electron emission microscopy
BHL	barrier height lowering
BINC	breakdown induced negative charge
C-V	capacitance-voltage characteristic
CAFM	conductive atomic force microscopy
CBM	conduction band minima
CCI	constant current imaging
CCS	constant current stress
CHI	constant height imaging
CITS	constant current tunnelling spectroscopy
CMOS	complementary metal-oxide semiconductor
CN	coordination number
CVS	constant voltage stress
DAC	digital-to-analog converter
DBIE	dielectric breakdown induced epitaxy
D_{it}	density of interface charge
DT	direct tunneling
e-beam	electron beam
EHP	electron hole pairs
EOT	electrical oxide thickness
FEL	fast entry lock
FWHM	full-width half-maximum
HRBS	high-resolution Rutherford backscattering
resolution	
HREELS	high-resolution electron-energy loss
spectroscopy	

HV	high voltage
I - V	current - voltage characteristic
IL	interfacial layer
I_t	tunneling current
iTAT	inelastic trap-assisted tunneling
J - V	current density – voltage characteristic
LDOS	local density of state
MEIS	medium energy ion scattering
MOCVD	metallo-organo chemical vapor deposition
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MOSCAP	MOS capacitor
NDR	negative differential resistance
PDA	post deposition annealing
PLD	pulsed laser deposition
PVD	physical vapor deposition
RP	rotary pump
RTO	rapid thermal oxidation
RVS	ramp voltage stress
SCM	scanning capacitance microscopy
SILC	stress-induced leakage current
SiON	Silicon Oxynitride
SIS	substrate injectin stress
SPA	semiconductor parameter analyzer
SPM	scanning probe microscopy
STM	scanning tunnelling microscopy
STOM	scanning tunnelling optical microscopy
STS	scanning tunnelling spectroscopy
TAT	trap-assisted tunnelling
TDDb	time-dependent dielectric breakdown
TEM	transmission electron microscopy
TIS	tip injection stress
tof-SIMS	time-of-flight secondary ion mass spectroscopy
TP	turbo molecular pump

TSP	titanium sublimation pump
UHV	ultra-high vacuum
VBM	valence band maxima
V_o^0	neutral Oxygen vacancy
V_o^+	Oxygen vacancy losing one electron
V_o^{++}	Oxygen vacancy losing two electrons
V_s	sample bias
WKB	Wentzel-Kramers-Brillouin approximation
XPS	x-ray photoelectron spectroscopy

LIST OF SYMBOLS

μ	micro
K_B	Boltzmann's constant
κ or ϵ	dielectric constant
q	electronic charge
β	Weibull slope
$\text{\AA}$	Angstrom
σ	capture cross section
ρ	density of state
φ	wave function
α_h	anode hole injection coefficient
P_h	hole generation probability
θ_h	hole tunneling probability
ω_{sp}	surface plasmon generation threshold
φ_{eff}	effective electron tunnel barrier
m_{ins}	tunneling mass in the insulator
N_t	volume density of traps
E_f	Fermi level
E_t	energy level of electronic trap
E_{relax}	relaxation energy

Chapter 1 INTRODUCTION

1.1 Background

Thermally grown amorphous Silicon dioxide layer on single crystalline silicon substrate has served as the gate insulator of transistors in modern complementary metal-oxide-semiconductor (CMOS) technology for more than four decades. It offers exceptional qualities in CMOS processing, for instance, good SiO₂/Si interface (interface state densities of $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ is achievable), low electron and hole trapping rate, high thermal and electrical stability as well as superior electrical isolation properties. Scaling of the oxide thickness continues to offer higher capacitance in the metal/oxide/semiconductor (MOS) structure, which leads to larger drive current, therefore improved transistor speed.

1.1.1 Scaling and its challenges

Moore's law, published as a simple observation by Gordon Moore in 1965 [1], has become a prophetic observation about integration that has been made a reality. It was stated in Moore's law that innovations in technology would allow a doubling of the number of transistors in a given space every year (the rate was adjusted to every two years to account for the growing complexity of chips in an updated article in 1975 [2])

and that the speed of those transistors would increase and manufacturing costs would drop as the technology advanced (Fig. 1.1).

Scaling the process geometries makes more space available to pack in more transistors, as well as to converge different types of devices and functions, onto the chip. Furthermore, smaller transistor size also results in higher speed and lower operating voltage.

Fig. 1.1 Scaling trend of different products in comparison with the projection by Moore's Law. The increase rate was adjusted to doubling every two years to account for the growing complexity of chips [1, 2]

To continue the trajectory predicted by Moore's Law means shrinking the nominal size of the devices that populate the silicon. One of the biggest challenges is the exponential increase in the leakage current (flow of current when the transistors are 'off'), which results in higher power consumption (Fig. 1.2). More heat is generated as a result of higher power consumption and the efficiency of cooling techniques must

therefore also increase to dissipate the heat. A more fundamental problem is the physical limits of atomic structure. As continuous scaling of metal-oxide-semiconductor field-effect transistor (MOSFET) has pushed the thickness of the SiO_2 layer down to a few atomic layers, lifetime projection predicts that an oxide of 22 Å physical thickness would not satisfy the industry's reliability requirement using a power supply of 1 V[3].

1.1.2 Requirement for high- κ material as a replacement for the gate dielectric

In response to the challenges mentioned in the last section, a concerted global effort is directed at both conventional and unconventional technologies that will remove obstacles to the next evolutionary step in scaling. Revolutionary approaches include introducing innovations in materials, transistor design, and packaging.

Fig. 1.2 Active and leakage power consumption with device scaling [4]. Leakage power consumption is approaching active power consumption with device scaling, signifying the critical needs for replacement of SiO_2 gate dielectric.

A replacement for the gate dielectric requires [5, 6]:

1. The dielectric constant to be high enough for a reasonable number of years of scaling, yet low enough to avoid undesirable fringing field at the source and drain electrode which can result in barrier lowering [7] and degrade short-channel performance. Typical value for the desired dielectric constant is in the range of 25 – 30.
2. The dielectric to have good thermodynamic stability in direct contact with silicon to avoid interfacial SiO_x or silicide formation which might increase the equivalent oxide thickness (EOT) or short out the field effect. This condition requires the oxide to have a higher heat of formation than SiO_2 .
3. The dielectric to be kinetically stable and compatible to current CMOS process, especially to retain stability against crystallization at processing temperature up to 1000 °C for 5 s, which is typical of a rapid thermal annealing process in the CMOS fabrication flow.
4. The dielectric to have a good Si-oxide interface in terms of roughness, electrical quality and defect density. As a rule of thumb, the interface trap density should not exceed $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. Grain boundaries in poly-crystalline film may introduce additional defects at the interface. Hence, an amorphous dielectric layer is the preferred choice.
5. The dielectric to have a potential barrier greater than 1 eV to inhibit conduction by Schottky emission of electrons or holes into the oxide bands. The band gap should be larger than 5 eV.
6. The dielectric bulk to have a low density of active electrical defects, which give rise to electronic states in the oxide band gap. Defects are undesirable as trapped charge at the defects give rise to threshold voltage instability and

reduction in carrier mobility. Moreover, they are the starting point for electrical failure and breakdown of the oxide.

The outstanding electrical properties of SiO_2 present a significant challenge for any alternative gate dielectric, not only in process integration but also in the reliability of the nanoscale transistors. Except for offering higher capacitance with thicker film and lower direct tunnelling leakage current, transistors with high- κ dielectrics as gate insulators have been shown to perform poorer in terms of thermal stability, uniformity, hole and electron mobility, interface trap density, and reliability [8]. Although already in production, continuous improvement in integrating high- κ material into the CMOS process remains a focus of research. Furthermore, as the primary component in most electronic devices, the reliability of the nanoscale MOSFET, which has incorporated a high- κ material as the gate dielectric, is of utmost important. Therefore, the investigation on the reliability of high- κ gate stack has aroused general interest among the microelectronics community.

1.1.3 Reliability of high- κ gate dielectric

Unlike the SiO_2 gate oxide, which has more than four decades of history, the knowledge base of newer high- κ / SiO_x gate stacks is very limited. In recent years, conventional electrical characterization study based on the MOS capacitor has reported very interesting observations which are yet to be understood. For instance, the Weibull slope of the high- κ gate stack subjected to gate injection stress is much smaller than that of substrate injection stress. Interpretation of this observation in the context of the percolation model, which was developed based on observations made on the SiO_2 gate dielectric, leads to unrealistic outcomes for instance, large defect size of 10 nm in diameter [9, 10]. Furthermore, as interfacial SiO_x is unavoidable at the high-

κ /Si substrate interface, it is unclear how electronic traps in each individual layer (i.e. high- κ and interfacial SiO_x) will influence the overall reliability of the gate stack.

1.2 Motivation

Electronic properties of nanodevices are susceptible to small perturbations in properties such as dimension, structure, roughness and defects. There is therefore a crucial need for precise metrology. Insertion of a variety of new materials into the conventional MOSFET for potential emerging replacement technologies presents further challenges for metrology. The ability to measure the physical, chemical and electronic properties that control the final device electrical characteristics will be important to the research and development of future electronic devices.

Conventional reliability study based on macroscopic MOS capacitor structure is only meaningful when the device under study has excellent uniformity and low pre-existing defect density. Area averaging in macroscopic measurements can also mask out important information related to microscopic defects. Inherent non-uniformity in most high- κ thin films therefore present significant challenges to macroscopic measurement or characterization techniques.

The motivation of this thesis is to use superior lateral resolution of Scanning Tunnelling Microscopy (STM) to circumvent the inherent non-uniformity issues in high- κ gate stacks, and directly measure the electrical properties of electronic defects at nanometre spatial resolution. Based on the understanding derived from tunnelling and band theory, electronic traps in each layer can be separately probed and studied under different process conditions and electrical stress.

1.3 Objectives

The project is aimed at advancing the fundamental understanding of the reliability physics of novel gate stacks, primarily:

- To understand the physics behind the polarity dependence of the Weibull slope of the breakdown distribution of advanced high- κ gate stacks.
- To reveal the role of pre-existing electronic traps in the individual layers on the reliability of the entire high- κ gate stack.
- To explore the role of oxygen vacancies in electrical uniformity and reliability performance of the high- κ gate stack.

1.4 Organization of Thesis

This thesis is divided into seven chapters, organized as follows:

- *Chapter One* provides the background, the motivation, the objectives and the contributions of this project.
- *Chapter Two* is a literature review on the research work that has been done and reported for high- κ gate dielectric reliability.
- *Chapter Three* explains the procedures and details of experiments that were carried out in our studies.
- *Chapter Four* establishes the fundamentals of polarity dependent STM observation of the multi-layered high- κ gate stack $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x/\text{Si}$. Process dependent electrical performance of the high- κ gate stack is reviewed.
- *Chapter Five* is a detailed study of electronic trap evolution in the high- κ gate stack $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x/\text{Si}$. The role of pre-existing defects on the overall reliability is highlighted.

- *Chapter Six* investigates oxygen vacancies in HfO_2 . A two-step annealing procedure is implemented to investigate the role of oxygen vacancies in generating localized leakage paths. High density of oxygen vacancies leads to increased electrical non-uniformity and poorer reliability of the gate stack.
- *Chapter Seven* provides conclusions and recommendations for future work.

1.5 Original Contributions

The novelty of our study lies in the application of the scanning tunneling microscope (STM) to study nanoscopic electronic properties of high- κ gate stacks. All the STM experiments are undertaken under ultra-high vacuum (UHV). We report the first scanning probe microscopy study of La_2O_3 gate oxide, STM methods to measure multi-barrier structure (as always present in high- κ gate stack), correlation between oxygen vacancies to local leakage current, and the effect of nitrogen passivation in terminating local leakage path. The most important findings of this study are summarized as follows.

All high- κ gate stacks contain at least two barriers for electrons to overcome, in contrast to SiO_2 . To investigate thin high- κ gate stack by STM one must measure a multilayer structure, for instance, $\text{HfO}_2/\text{SiO}_x/\text{Si}$. We developed STM techniques for probing a multi-barrier system by changing the bias conditions, such that the electrical properties of the different layers of the stack and/or the interfaces can be investigated.

STM measurement of a multi-barrier system was demonstrated on Sc_2O_3 (3 nm)/ La_2O_3 (4 nm)/ SiO_x (1 nm) using bias dependent imaging. STM at sample bias of +3.5 V imaged the conduction band of the La_2O_3 whereas STM controlled at -4 V

revealed the SiO_x IL layer. A very important point to note is that this type of STM experiment can only undertaken under UHV conditions, as in our work. Under ambient of high vacuum conditions, contamination (water, oil, carbonates, etc) will be present on the surface. Under negative sample bias this is not an issue because electrons are extracted from the clean Si/SiO_x interface. However, under positive sample bias the contamination leads to electrochemical reactions (anodic oxidation) or the presence of additional materials at the tip-surface interface (electro-deposition), giving erroneous data for electron transport across the interface.

We report the first ever scanning probe data taken on the high- κ material La_2O_3 . This material has been proposed as a potential gate dielectric after the introduction of HfO_2 on the semiconductor road map. The $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ samples were supplied by collaborator in Japan who also undertook detailed current-voltage (I - V) and capacitance-voltage (C - V) measurements on the same samples. The Sc_2O_3 is a dielectric which has barrier height similar to La_2O_3 , that protects the underlying La_2O_3 from exposure to moisture.

For the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack, a large number of local I - V curves, each measured over an area of about a few nm^2 , records two distinct and highly localized characteristics. One type of local I - V exhibits the stress-induced leakage current (SILC) behavior typically observed on the macroscopic MOS capacitor. Traps in the high- κ and SiO_x which give rise to such I - V behavior are delineated. More importantly, local soft breakdown paths in the high- κ and SiO_x layer are separately indentified. The I - V curves at these locations are laterally shifted to lower voltage, indicative of a net lowering of the tunneling barrier. The study also shows that a soft breakdown path in the high- κ layer exhibits a much lower effective resistance under tip injection biasing.

This observation can explain very well the small Weibull slope typically observed under gate injection stressing of large area MOS structure.

The most important milestone lies in the experimental demonstration of how traps are generated in the respective layers of the gate stack with or without the influence of as-processed traps. This is perhaps the first experimental demonstration of such a phenomenon at the nanometer scale, in real time and real space. In the absence of as-processed traps, the high- κ layer is more susceptible to trap generation. This observation is discussed in the context of current trap generation models and is shown to be best explained by an anode hot-hole effect induced by an inherently lower surface plasmon threshold energy at the metal/high- κ interface and a higher hole trapping rate in the relatively thick high- κ layer. The insight into the role of as-processed traps in the reliability of the gate stack is derived from the observed mismatch in the locations of the worst-case trap generations in the two layers of the gate stack. For instance, traps in the interfacial SiO_x layer are found to suppress the generation of traps in the high- κ layer at the same location. The converse is also observed to be true. These findings are explained by inelastic trap-assisted tunneling, which results in “cooler” anode hot electrons and thus reduced trap generation in the adjacent dielectric layer at a given location. Experimental observations further show that the inelastic trap-assisted tunneling can lead to the wearout of the neighboring region of the pre-existing SILC traps and where there exists a percolation path in one layer, wear-out of another layer will be accelerated due to enhanced electric field.

In addition, a two-step annealing procedure has successfully demonstrated the role of oxygen vacancies in the density of localized leakage paths in a HfO_2 gate stack. Passivation of oxygen vacancies by Nitrogen incorporation is shown to result in suppression of low-voltage leakage current and drive the current into a self-limiting

regime at high voltages. Improvement in the breakdown strength of the HfO_2 subjected to ramp-voltage stress is also observed after Nitrogen incorporation. This improvement may be related to limitation of the current flow through the gate stack in the high stress voltage regime.

In summary, significant results on conventional (HfO_2) and advanced ($\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3$) high- κ gate stack has been achieved. The STM analysis provides a platform to advance our fundamental understanding of the reliability physics of novel gate stacks.

Chapter 2 LITERATURE REVIEW

2.1 Introduction

Scaling of Silicon Oxynitride (SiON) has reached its limits. Sourcing for a suitable replacement for SiON has been an active research topic in recent years. The requirements for the alternative gate oxide are [5, 6] (i) A dielectric constant of 25~30, (ii) good thermodynamic stability with silicon, (iii) compatibility with current CMOS process, (iv) high quality Si-oxide interface, (v) large band gap and a Si-oxide barrier larger than 1 eV and (vi) low density of active electrical defects. These stringent requirements have limited the list of possible candidates to Al_2O_3 , ZrO_2 , HfO_2 , Y_2O_3 , La_2O_3 , Sc_2O_3 , and a series of Lanthanides, such as Pr_2O_3 , Gd_2O_3 and Lu_2O_3 [6]. A comparison of leakage current of various oxides with different EOT at 1 V is shown in Fig. 2.1 [6] for HfO_2 [11] and ZrO_2 [12], La_2O_3 [13], and Al_2O_3 [14]. Significant reduction of leakage current is evidenced with high- κ gate stacks as compared to SiO_2 of the same EOT.

Successful implementation of novel high- κ dielectrics in future CMOS technologies would require one to not only overcome the impending process integration problems but also the reliability challenges presented by these relatively

new materials. There have been several serious problems for high- κ gate dielectric to be incorporated into the current CMOS technology, among which are, (i) uncontrolled interfacial layer growth during deposition or post deposition annealing, (ii) nanocrystal formation and phase separation in silicates during heat treatment, resulting in increased leakage current, (iii) pre-existing fixed charges inside the high- κ film, resulting in large flatband voltage (V_{FB}) shift and mobility degradation, (iv) high density of interface states, (v) contamination from the precursors used for Atomic Layer Deposition (ALD) or metallo - organo chemical vapor deposition (MOCVD) and (vi) yield and reliability of the film. Moreover, high- κ dielectrics have an inherently higher concentration of non-equilibrium defects in the bulk as they have a higher coordination number and their metal-oxide bonding is ionic in nature. This results in poorer electrical performance as compared to SiO_2 , especially in the aspects of charge trapping, mobility and threshold voltage shifts. This chapter will provide a brief comparison of the most commonly known high- κ process technologies, followed by a detailed review of the electrical performance and reliability of transistors employing high- κ thin films as the gate dielectric. As the STM technique is becoming increasingly popular for thin film characterization, a brief introduction on STM theory will also be presented, followed by a detailed review of its recent application to high- κ dielectric study.

Fig. 2.1 A comparison of leakage current of various oxides with different EOT at 1 V.

[6]

2.2 High- κ deposition techniques and their problems

2.2.1. Deposition techniques

Electrical properties of the high- κ gate stack can vary widely depending on surface preparation, deposition and annealing method and condition [15]. Hence it is crucial to understand the fundamentals of each deposition technique. MOCVD, ALD and Physical vapor deposition (PVD) are among the most commonly accepted high- κ deposition techniques. For surface preparation, the most widely adopted techniques are the HF-last surface treatment, the chemical oxide last surface treatment and the wet-clean method using ozone [16].

MOCVD uses volatile metal organics as a precursor, which are introduced into the chamber and oxidized during deposition onto the substrate. Good uniformity of the high- κ thin film can be achieved by MOCVD as the liquid phase precursor can limit particle formation during deposition. Variation in pressure and gas flow allows

variation in the film composition. Deposition temperature ranges between 400 to 600 °C and the quality of the high- κ oxide is independent of the substrate surface.

In ALD, the thin film is grown by means of chemical reactions at the surface. The surface reactions are self-limiting, hence allowing accurate thickness control, good uniformity, conformality and smoothness. Typical deposition temperature ranges from 300 to 400 °C. In contrast to conventional CVD, surface preparation is crucial to achieving good quality thin films. Good quality surface is required such that a steady growth rate per cycle can be achieved from the beginning of the process.

As compared to CVD and ALD techniques, PVD's main advantage is contamination (by precursor molecules) free. Metal target sputtering followed by controlled oxidation, especially oxidation by reactive oxygen from plasma or UV irradiation, has allowed decent control of the interfacial layer thickness as well as the film composition, due to a low process temperature. For instance, the HfO_2 thickness may be controlled by a pre-deposited Hf metal layer of a given thickness while the interfacial layer thickness adjusted by controlling oxidation treatment time [5]. Alternatively, oxide can be directly evaporated by high energy electron beam and deposited on the substrate, which is the Electron Beam Evaporation method. Deposition by Electron Beam Evaporation in UHV condition also allows better control of the interfacial SiO_x layer by maintaining the substrate at a relatively low temperature, for instance, 300 °C. Native oxide can be desorbed from Si substrate in UHV by flash heating the Si surface beyond 1200 °C before oxide deposition.

However, there are also problems in PVD deposition. For example, it was shown by quantitative modeling of medium energy ion scattering (MEIS) data that as-deposited Lanthanum oxide prepared by electron beam evaporation is made up of non-stoichiometric $\text{La}_{0.32}\text{Si}_{0.02}\text{O}_{0.65}$ instead of the stoichiometric La_2O_3 . High defect density,

which gives rise to electronic states in the band gap of the oxide, is therefore expected in the thin film. These electrically active defects are detrimental to the device performance and they could be the precursor for electrical breakdown of the gate dielectric [6]. Hence, understanding of the electrical properties of the traps and their distribution within the oxide is crucial. However, non-area/thickness scalability of the I - V characteristic was also observed for La_2O_3 MOS structure [17] due to local thickness and composition variation [18]. Conventional macroscopic electrical characterization on MOS capacitor (MOSCAP) or MOSFET structure therefore results in uncertainty in interpretation at the microscopic level. STM can be used to address this issue by directly measuring I - V characteristics at electrically active defects and comparing with defect-free area.

2.2.2. Interface preparation

The interface between the high- κ gate dielectric and the substrate plays a crucial role in determining the electrical performance of the device [19], for example, mobility [20] and time-dependent dielectric breakdown [21]. Si-surface treatment is therefore important in interface engineering. Chemical oxides formed on H-terminated Si surface using ozonated cleaning chemistries and thermal oxides/oxynitrides by rapid thermal oxidation (RTO) are among the most popular methods used in Si-surface treatment [22]. Chemical oxide has been shown to provide a better control over standard thermal oxide/oxynitride in minimizing both fixed charge and interfacial oxide growth in the high- κ film.

2.2.3. Post deposition annealing

Post deposition annealing (PDA) is usually necessary to reduce leakage current through the high- κ gate stack. Although reduction of leakage current with PDA was reported, the reduction was mainly attributed to the growth of interfacial layer (IL) or high- κ layer [23-26]. Fig. 2.2 illustrates the effect of leakage current and electrical oxide thickness (EOT) of thin HfO_2 gate stacks [27].

Despite the observed reduction in leakage current, negative flatband voltage shift in the C - V characteristic is observed after PDA (Fig. 2.3) [28]. The negative shift of flatband voltage can be interpreted as increase in positive fixed charge density or reduction of negative fixed charge density. The positive fixed charge density (or compensation of negative fixed charged density) introduced during PDA had been attributed to formation of silicate, especially at the interface between La_2O_3 and Si substrate [29]. The density of midgap interface states was also found to increase with PDA [28]. The C - V curves appear more “stretched out” along the voltage axis, which indicates that interface state density has increased with PDA. A summary of the effect of PDA temperature on fixed charge density and interface states density is shown in Fig. 2.4. It is seen that suppression of positive fixed charge generation is only effective with post-metallization annealing (i.e. atomic hydrogen anneal). These defects were therefore attributed to hydrogen-induced overcoordinated oxygen centers.

Reduction in the Weibull slope in time-dependent dielectric breakdown (TDDB) plots of the breakdown distribution of high- κ gate stacks subjected to substrate injection stress has also been observed after annealing. The reduced Weibull slope (Fig. 2.5) implies that fewer traps are needed to form the percolation path that shorts the cathode to the anode [30], hence, there is an increase in the density of process-induced traps after PDA.

High density of electronic traps within the high- κ bulk could have enormous influence on the viability of incorporating high- κ into the standard CMOS process. Detailed understanding of the localized physical and electronic properties of pre-existing and PDA induced electronic traps are therefore crucial to process development.

Fig. 2.2 PDA effect on leakage current and EOT of thin HfO₂ gate stacks [27]

Fig. 2.3: C-V characteristics of as-deposited and annealed Au/ZrO₂(3.6nm)/SiO_x/n-Si gate stacks [28]

Fig. 2.4 PDA effect on (a) fixed charge density in ZrO_2 bulk and (b) interface states density [28]

2.3 Time dependent dielectric breakdown

TDDDB study in high- κ gate stack has reported a relatively small value of the Weibull slope (β) as compared to the conventional SiO_2 gate dielectric. β is a reflection of the number of traps needed to be generated to construct the breakdown path as predicated in the percolation model [31]. β in TDDDB distribution of the high- κ gate stack can be more than four times smaller than its SiO_2 counterpart with the same physical thickness. At present, there is no physical explanation for this observation [9]. An intrinsic material based explanation for the small β value postulates an unrealistically large defect size of about 10 nm in diameter based on the percolation model

established for SiO₂ gate dielectric. In an extrinsic mechanism, a small β value implies a high density of as-processed defect.

Another exceptional observation is the bias polarity dependence of β [30]. As shown in Fig. 2.5, β is independent of high- κ thickness during gate injection [9]. In contrast, when electron is injected from the substrate, β scales positively with high- κ thickness, suggesting formation of percolation paths in the high- κ layer leading to dielectric breakdown [30].

Bias polarity dependent β could be a result of polarity dependent trap generation in the high- κ gate stack, as demonstrated widely by different research groups [32-36]. Fig. 2.6 [5] shows trap density in (a) the HfO₂ bulk and (b) at the SiO₂/Si interface with stressing time. Trap density in the HfO₂ bulk is extracted from the difference between a high and low frequency charge pumping current and SiO₂/Si interface trap density is extracted from high frequency charge pumping current. Higher trap generation rate in the HfO₂ bulk is observed at positive gate voltage stress, when the gate acts as anode during the electrical stress. Similarly, higher trap generation rate at the SiO₂/Si interface was observed at negative gate voltage, when the substrate is the anode. In summary, trap density in the dielectric layer next to the cathode is hardly affected by electrical stress whereas trap density in the dielectric layer next to the anode is increased.

Fig. 2.5 Weibull slope (β) vs. Al_2O_3 thickness in an $\text{Al}_2\text{O}_3/\text{SiO}_2$ gate stack with SiO_2 IL of 1.5nm. β during gate injection stress is independent on Al_2O_3 thickness and annealing condition. β during substrate injection stress increases with Al_2O_3 thickness and is reduced in annealed samples. [5]

Fig. 2.6 Trap density (a) in HfO_2 bulk and (b) at the SiO_2/Si interface versus stressing duration at both positive and negative gate voltage (V_g) stress. During positive V_g stress, breakdown triggered at 30th second [5]

It can be observed from Fig. 2.6 that trap generation rate was more than 3 times larger in the bulk HfO_2 as compared to the SiO_2/Si interface (comparing filled circle in (a) and open circle in (b), both layers are next to anode). This observation implies that the high- κ layer is more susceptible to trap creation upon electrical stress. Higher trap generation rate and lower breakdown electric field (E_{BD}) in high- κ thin film compared to SiO_2 have been reported widely [37, 38]. Fig. 2.7 shows the power law correlation

between E_{BD} and κ . Current density at breakdown (J_{BD}) was superimposed onto the graph for reference to ensure that the observed low E_{BD} is not due to extrinsic factors. A fundamental relationship exists between E_{BD} and κ , approximately $E_{BD} \propto \kappa^{-1/2}$ [37, 38]. The correlation was found to hold over nearly two decades of dielectric constant [37]. A thermochemical model was proposed by McPherson *et al.* to explain the lower E_{BD} of high- κ gate dielectric [38]. In the model, local electric field, with contributions from the external applied field (E_{ext}) as well as dipolar field, distorts and weakens polar-molecular bonds, resulting in lower activation energy for bond breakage. Dipolar field is a function of dielectric constant and the effective local electric field (E_{loc}) can be expressed as [38]:

$$E_{loc} = [(2 + \kappa)/3]E_{ext} \quad (2-1)$$

Therefore, a higher κ value results in a higher effective E_{loc} .

The enthalpy of activation for bond breakage decreases with increasing E_{loc} [38],

$$\Delta H = \Delta H_0^* - p_0 E_{loc} = \Delta H_0^* - p_0 [(2 + \kappa)/3]E_{ext} \quad (2-2)$$

where ΔH_0^* is the activation energy required for permanent metal-ion displacement from the normal local bonding environment and p_0 is the molecular dipole-moment component opposite to the applied field. Theoretically, the ultimate dielectric breakdown strength, E_{BD} , is ($\Delta H = 0$) [38]

$$E_{BD} = \frac{\Delta H_0^*}{p_0 \left(\frac{2 + \kappa}{3} \right)} \quad (2-3)$$

giving $E_{BD} \propto \kappa^{-1}$

The difference between theory ($E_{BD} \propto \kappa^{-1}$) and experimental observations ($E_{BD} \propto \kappa^{-1/2}$) was attributed to the partial offset of the local field by an increase of activation energy due to higher coordination number (CN) in most high- κ materials.

Fig. 2.7 Correlation between breakdown strength (E_{BD}) and dielectric constant (κ). The correlation follows a power law, $E_{BD} \propto \kappa^{-1/2}$ [37].

Thermochemical model has successfully predicted the Lorentz relation between E_{BD} and κ , it cannot explain higher trap generation rate in the high- κ layer compared to the SiO_x layer observed in a single gate stack. This is due to the reduction of E_{ext} by a factor of κ (based on the electric field continuity condition [39]) in the high- κ layer that cancels off the E_{loc} enhancement by $(2+\kappa)/3$ shown in equation 2-1. The effective E_{loc} is therefore comparable in both SiO_x and high- κ layers. In addition, while as grown traps are negligible in modern SiON , they are found to exist in high density in high- κ dielectric. For instance, trap density in ALD HfO_2 layer was reported to be $\sim 10^{13} \text{ cm}^{-2}$ [40, 41]. This is further supported by non-area scalability of the J - V characteristics [17] and low Weibull slope [9] of the high- κ gate stack. High- κ dielectrics differ from SiO_2 in that their bonding is ionic and they have higher coordination number (CN). Being ionic and having a high CN results in high concentration of non-equilibrium defects [6]. The defects exist within the high- κ bulk induce energy states within the bandgap, hence modifying the localized electrical

properties. The interpretation of the electrical data from macroscopic MOSCAP structure is therefore not straight forward and the intrinsic mechanism of higher trap generation rate in the high- κ layer has not been identified.

Moreover, two distinct capture cross sections (σ) of the order of 10^{-14} and 10^{-16} cm^2 were extracted by the pulsed I_d - V_g method [42, 43] and attributed to two different types of as-grown electron traps in HfO_2 . It was reported by Degraeve *et al.* that σ of the traps responsible for breakdown is $\sim 0.8 \times 10^{-14}$ cm^2 [32]. The result indicates that as-grown traps in the high- κ layer may pose serious reliability issues to the high- κ gate stack, hence further processing steps are necessary to annihilate the as-grown traps. However, there is a contradicting observation [44]. Crupi *et al.* reported that the traps involved in high voltage stress induced leakage current are different from the as-grown trap that causes hysteresis in the I_d - V_g characteristics. The contradiction was explained by non-uniformity of electrical property or existence of different types of traps within the bulk, such that some of the as-grown traps are indistinguishable from the electrical stress induced traps [45]. The existence of traps with different properties gives rise to ambiguity in the analysis of the results of conventional macroscopic characterization techniques due to area-averaging. STM, which has the capability of acquiring laterally resolved electrical characteristics, is therefore attractive in unveiling different types of trap within the high- κ film.

In summary, this section provides a general overview on the existing electrical study on TDDDB of advanced high- κ gate stacks. Interesting observations have been reported. However, physical understanding in the electrical study is still lacking. The major difficulty encountered in the macroscopic electrical study is the high density of as-processed defects, which renders the intrinsic wear-out process indistinguishable from extrinsic breakdown of the gate stack.

2.4 Stress induced leakage current

In addition to TDDDB, stress induced leakage current (SILC), namely the excess low field conductivity produced by a high field stress, has been a major phenomenon of concern for the reliability of MOS devices with SiO₂ thickness below 10 nm. SILC in conventional SiO₂ is stable with time and thermal annealing. SILC becomes the dominant failure mode as it precedes destructive breakdown. SILC was also observed in MOS devices with high- κ gate stack and found to increase linearly with the number of generated high- κ defects [44]. It was reported to be a function of polarity (Fig. 2.8a), injected fluence and stress voltage (Fig. 2.8b) [44]. SILC in high- κ gate stack is of particular interest as the excess of current at low voltage is expected to offset the benefit of switching the gate dielectric to high- κ material since the main driving force for dielectric replacement is leakage current reduction.

Fig. 2.8 SILC data for HfO₂ (a) Polarity dependence of SILC (b) Injected fluence and stress voltage dependence of SILC. [44]

SILC has been modeled (Fig. 2.9) by field enhancement due to trapped positive charge [46-48] (a); trap-assisted elastic tunneling [49-52] (b); local thinning due to a conductive filament [53, 54] (c), and trap-assisted inelastic tunneling (d). Models (a)

and (b) do not account for the energy loss as evidenced in experiments. For model (c), although the experimental observed energy loss of the tunnel electrons could be interpreted as the voltage drop in the filament region, the observed energy loss has a constant value independent of electron fluence, which disagree with the model as the filament grows (i.e. increased energy loss) with increased fluence.

To account for the energy loss during the tunneling process, the trap-assisted inelastic tunneling model was is the most appropriate (Fig. 2.8d). Electrons tunnel from the cathode into one neutral trap and the energy level of the electron-trapped center shifts to a deeper level than the original position (E_{relax}), possibly associated with the reconstruction of the defect structure. Subsequently, the electron tunnels out to the anode and the energy level of the trap recovers to the original position. Tunneling current is modeled as a two step process [55]. Energy loss during electron trapping is taken into consideration based on the observation from carrier separation measurement [56] that the energy loss observed experimentally is roughly constant, at the value of 1.5 eV, irrespective of the gate voltage and the Fowler-Nordheim (FN) stress polarity (positive or negative gate voltage during FN stressing). The increase in hole current was much smaller than the increase in electron current (i.e. lower quantum yield) after SILC was induced by FN stressing. The quantum yield showed no dependence on the electron fluence during the FN stressing and the amount of SILC. The possibility that the observed SILC was due to valence band electron trap assisted tunneling was excluded due to the fact that there was no increase in substrate hole current (the holes leaving the Si/SiO₂ interface and flowing into the substrate after the valence band electron tunneled into the gate) after the SILC was induced.

Fig. 2.9 SILC modeled by (a) field enhancement due to trapped positive charge (b) trap-assisted elastic tunneling (c) local thinning due to a conductive filament and (d) trap-assisted inelastic tunneling.

The physical origin of the energy relaxation in SiO_2 dielectric was suggested to arise from the defects in SiO_2 accompanied by a strong electron-lattice interaction. It was reported that the strong electron-lattice interaction in SiO_2 can cause the change in

the energy level of the defects with the capture of electrons during trap assisted tunneling [57]. Oxygen vacancies with large lattice distortion has been proposed as the physical origin of the trap involved in SILC as the defect level of oxygen vacancies can change between neutral and electron trapped condition [58].

2.5 STM

Since the invention of STM by Binnig and Rohrer [59, 60] and its successful demonstration of resolving surface topographies in real space of the Si (111) 7×7 reconstructed surface [61] and Au (110) reconstructed surface [62], the scanning probe microscopy (SPM) family has developed as a most important technique in surface investigation with atomic resolution. As the physical size of electronic devices scales to the nanometer range, STM appears to be an attractive technique which can provide fundamental physical insight for better understanding of nanoscale electronic properties and device performance. In this section, the underlying theory of STM will be briefly discussed.

2.5.1. STM theory for a conducting material

Classical physics tells us that the only way for an electron to surmount an energy barrier is to have energy larger than the barrier. Quantum physics, however, predicts that there is a finite probability for an electron to exist within the energy barrier, and hence tunneling through the energy barrier is possible.

In STM, a sharp metal tip is brought very close ($<10\text{ \AA}$) to a conducting surface. With a bias voltage applied across the tip-sample junction, electrons quantum mechanically tunnel across the gap and a measurable tunneling current is produced.

STM theory was developed from vacuum tunneling. In order to understand the correlation between STM current and width of the vacuum gap (z), a single electron approach to the tunneling problem will be used as a first approximation. The simple 1-D model is shown in Fig. 2.10, where an electron with mass m is incident on a rectangular potential barrier.

Fig. 2.10 1-D model for STM current calculation. A rectangular energy barrier (region II) represents the vacuum gap of width α , height V_0 .

To calculate the STM current, we need to know the probability of electron tunneling through the barrier. This can be done by matching wave functions and the first-order derivative of the three regions (I, II and III in Fig. 2.10) at the interfaces. By solving the Schrodinger equation, wave functions in the three regions can be expressed as:

$$\varphi_I = \exp^{ikz} + R \cdot \exp^{-ikz}, \text{ where } k = \sqrt{\frac{2mE}{\hbar^2}} \quad (2-4)$$

$$\varphi_{II} = A \exp^{\omega z} + B \exp^{-\omega z}, \text{ where } \omega = \sqrt{\frac{2m(V_0 - E)}{\hbar^2}} \quad (2-5)$$

$$\varphi_{III} = T \exp^{ikz} \quad (2-6)$$

The coefficients R, T, A and B may be determined from boundary conditions, i.e. the wave functions, and their derivatives are continuous at the interfaces.

The current density (j) is defined as:

$$j = \frac{\hbar}{2im} \left(\varphi^* \frac{\partial \varphi}{\partial x} - \frac{\partial \varphi^*}{\partial x} \varphi \right) \quad (2-7)$$

The transmitted current density (j_t) is,

$$j_t = \frac{j_{III}}{j_I} = \frac{1}{1 + (\omega^2 + k^2)^2 / (4k^2 \omega^2) \sinh^2 \omega \alpha} \quad (2-8)$$

For a strongly attenuating barrier,

$$j_t = \frac{4k^2 \omega^2}{(\omega^2 + k^2)^2} \exp^{-2\omega \alpha} \quad (2-9)$$

where $\omega = \sqrt{\frac{2m(V_0 - E)}{\hbar^2}}$ is the decay rate. Equation 2-9 shows that, typically, the tunneling current is exponentially dependent on the barrier width, α , and the square root of the effective barrier height, $\sqrt{(V_0 - E)}$. In STM, the effective barrier height can be extracted from measuring current as a function of tip-sample separation (a I - z characteristic) at a fixed sample bias. Using equation 2-9 gives the simplistic expression,

$$(V_0 - E) = \frac{\hbar^2}{8m} \left(\frac{d \ln I}{dz} \right)^2 \approx 0.95 \cdot \left(\frac{d \ln I}{dz} \right)^2 \quad (2-10)$$

Several attempts had been made to calculate STM current using different methods and tip models for more realistic situations. Tersoff and Hamann's model is the most

widely used STM current model. Tersoff *et al.* first applied Bardeen's transfer Hamiltonian approach to STM with the assumption that the tip has a uniform density of states and only s-wave functions are important. Tunneling current is calculated through the overlap of the tip and sample wavefunctions using Fermi's golden rule. However, the density of states at the Fermi energy of a tungsten tip (the most commonly used tip) is dominated by d states rather than by s states. Chen therefore further extended Tersoff and Hamann's model by replacing the s-wave tip model with a d-wave tip model [63]. Lang simulated a STM image of a Na atom by treating the sample and tip as two planar metallic electrodes with an adsorbed atom on each electrode [64]. Binnig *et al.* also modified the tunnel current expression by considering the image force effect [65]. The distance dependence of STM current is not affected in the presence of an image force, although the absolute value of the current is drastically affected.

In general, the STM current can be expressed as [66]:

$$I = \frac{2\pi e}{\hbar} \sum_{\mu,\nu} \left\{ f(E_\mu) [1 - f(E_\nu + eU)] - f(E_\nu + eU) [1 - f(E_\mu)] \right\} |M_{\mu\nu}|^2 \delta(E_\nu - E_\mu) \quad (2-11)$$

where $f(e)$ is the Fermi function; U is applied voltage; E_μ (E_ν) is energy of the state φ_μ (φ_ν) in the absence of tunneling and $\delta(E_\nu - E_\mu)$ describes conservation of energy for the case of elastic tunneling. The tunneling matrix element between the unperturbed electronic states φ_μ of the tip and φ_ν of the sample surface, $M_{\mu\nu}$, can be expressed as [66]

$$M_{\mu\nu} = -\frac{\hbar^2}{2m} \int ds (\varphi_\mu^* \nabla \varphi_\nu - \varphi_\nu \nabla \varphi_\mu^*) \quad (2-12)$$

When a voltage U is applied to the sample, only states lying between E_ν and $E_\nu + eU$ participate in tunneling. By varying the applied voltage U , one can select the electronic states that contribute to the tunneling current. Thus the STM I - V characteristic gives a

measure of the local electronic density of states at a range of energy as determined by the range of voltage sweep. This technique is called scanning tunneling spectroscopy (STS). It is very powerful as it can distinguish whether a certain feature on the STM topography image is due to electronic states or surface roughness. For illustrative purpose, STM current can be approximately expressed as [66]:

$$I = \int_0^{eV} \rho(E) T(E, qV) dE \quad (2-13)$$

where $\rho(E)$ is the surface DOS of the sample, $T(E, qV) = \exp(-2\omega\alpha)$ (equation 2-9) is the transmission probability of the electron. The I - V data is typically converted to show $(dI/dV)/(I/V)$ (i.e. the normalized conductance) versus V because for a simple 1-D model tunnel barrier[67],

$$\frac{dI/dV}{I/V} = \frac{\rho(qV) + \int_0^{qV} \frac{\rho(E)}{T(qV, qV)} \frac{d}{d(qV)} [T(E, qV)] dE}{\frac{1}{qV} \int_0^{qV} \rho(E) \frac{T(E, qV)}{T(qV, qV)} dE} \quad (2-14)$$

$T(E, qV)$ and $T(qV, qV)$ appear as ratios in equation 2-14. Their exponential dependences on the barrier width, α and voltage, V tend to cancel. Therefore, the denominator of the equation can be viewed as providing a “normalization” for $\rho(E)$ and the normalized conductance reflects surface DOS of the sample.

2.5.2. STM theory for an ultrathin dielectric layer

The calculation of electron tunnelling probabilities through oxide films on Si substrate is still at the development stage, although the problem is attracting increasing interest because STM current can be detected when the oxide thickness is scaled down to a few nanometer. Therefore, STM turns out to be a very useful technique to study the

properties of an ultrathin gate dielectric as it provides the advantage of high spatial resolution, with the capability of acquiring lateral resolved electrical characteristics.

Iwasaki's group [68] performed calculations of electron tunnelling probabilities through oxide films on Si surfaces by employing an exactly solvable 1-D model, as shown in Fig. 2.11. For simplicity, band bending and image forces in both electrodes are neglected. The transmission coefficient is calculated by matching the exact solution of the 1-D Schrodinger equation in each layer. Fig. 2.12 shows the resulting simulated I - V and I - z characteristics. The calculation reproduces the measured I - V characteristic well and the I - z characteristic has a similar exponential dependence as the general I - z characteristic on conducting samples.

Fig. 2.11 1-D model for electron tunneling from a W tip to a n-Si substrate, across a thin oxide layer. Band bending and image potentials in both electrodes are neglected [68]

Fig. 2.12 (a) STM I - V characteristic measured for a SiO_2/Si sample (solid curve) together with the calculated result (dotted curve). Tip-to-sample separation during the measurement was determined by a feedback setting of +8 V, 0.3 nA. The calculation was done with $z = 0.2$ nm. (b) Calculated tunneling probability as a function of tip-to- SiO_2/Si interface separation for a clean Si (solid curve) and for a 0.6 nm oxide on Si (dotted curves) sample for a bias voltage of 1, 2, 3, 4 and 6 V. [68]

2.5.3. Overview of STM studies on ultrathin gate dielectric

Scanning Probe Microscopy (SPM) is a useful technique to investigate local structures. On insulating samples, conductive atomic force microscopy (CAFM) and scanning capacitance microscopy (SCM) are commonly used techniques for studying local leakage currents and trapped charges, respectively. However, their spatial resolution is insufficient to investigate atomic-scale defects. STM is typically used only on conductive samples, however, if an insulating film is less than a few nanometers in thickness, direct tunneling (DT) current (> 1 pA) becomes measurable using STM. The feasibility of using STM allows one to take spatially resolved measurements of the tunneling current flowing from a sharp metal tip through the thin insulating layer to the substrate, hence probing the localized bulk property of the ultrathin insulator. The knowledge that the tip is always highly conducting and metallic is significant. In

CAFM and SCM, as used on thick dielectric films, the electronic nature of the tip apex is usually highly uncertain and variable [69].

2.5.3.1. Conventional SiO₂ and SiON

SiO₂ or SiON has played a crucial role in the advancement of the planar MOSFET. Experimental studies on the oxidation of Si surfaces by x-ray photoelectron spectroscopy (XPS) [70] and high-resolution electron-energy loss spectroscopy (HREELS) [71, 72] are well documented. These studies revealed the chemical composition at the interfaces and the adsorption sites of oxygen atoms. However, the understanding on the initial oxidation process is lacking. The combination of STM and scanning tunneling spectroscopy (STS) is a very powerful tool in obtaining information on atomic arrangements and local electronic structures involved in the oxidation of surfaces. Changes in electronic structure due to oxygen adsorption and the formation of oxide layers on Si can be observed using spatially resolved STS spectra [73]. For example, Ikegami *et al.* performed *in-situ* UHV STM and STS during oxide formation on Si(100). Oxidation was done by exposing a Si (100)-2×1 clean surface to atomic oxygen at room temperature in the pressure range of 1×10^{-8} to 4×10^{-7} torr [73]. Their results suggested that oxidation nucleated from back bond sites. Fig. 2.13 shows the evolution of the oxidation process when a clean Si (100) – 2×1 surface is exposed to 1 L (1 L = 1×10^{-6} Torr s) to 15 L ((b) to (d)) of oxygen. Bright protrusions appeared upon oxidation. With prolonged oxygen exposure, larger bright protrusions and a higher density of dark areas are observed. The Si(100) – 2×1 dimer structure is still observable in Figs. 2.13b and 2.13c. STS on the clean Si (100) 2×1 surface (Fig. 2.14) shows three peaks at –0.7 eV, 0.3 eV and 1.2 eV (bias voltage is applied to the

sample), which correspond to the π_b bond state, π_a^* antibonding state and back-bond states, respectively. π_b and π_a^* are the bonding and antibonding states of a π interaction between the dangling bonds on each of the Si dimer atoms (bright lines on a clean Si (100) 2×1 surface as in Fig. 2.14a) whereas back-bond states localize between the dimer rows. Upon exposure to oxygen, STS at the bright protrusions showed attenuated local density of state (LDOS) whereas the back bond states vanished (Fig. 2.15). This indicates that the bright protrusion is the oxidized state. The oxygen atom absorbed at the bridge bond of the dimers is invisible while the neighboring Si atoms can be observed as bright spots. As the oxygen atom has larger electronegativity upon oxidation, electrons are transferred from Si to oxygen, resulting in the attenuated LDOS at the bright spots.

After an exposure of 15 L (fig.2.13d), the surface was completely covered by disordered bright protrusions and the Si (100) 2×1 reconstructed surface was lost. STS of different surface features almost overlap each other, indicating a spatially uniform LDOS (Fig. 2.16). Moreover, the dangling bond states (π_b and π_a^*) have completely disappeared. At an oxide thickness of 0.4 nm (exposure 10^4 L), bulk property of the oxide can be observed from the STS, where valence band maxima and conduction band minima of both the oxide and the Si substrate can be observed as peaks in the STS (Fig. 2.17).

Fig. 2.13 STM images of (a) clean Si (100) – 2×1 surface and the surfaces after (b) 1 L, (c) 4.5 L and (d) 15 L oxygen exposure. Scan area for (a) and (b) is $9.0 \times 9.7 \text{ nm}^2$ with a sample bias of -1.3 V . Scan area for (c) and (d) is $16 \times 18 \text{ nm}^2$ with sample bias of -1.4 V in (c) and $+3.0 \text{ V}$ in (d). [73]

Fig. 2.14 STS of a clean Si (100) 2×1. S1 corresponds to π_b bond state, S2 to π_a^* antibonding state, and S3 to back bond states. [73]

Fig. 2.15

STS of the Si (100) 2×1 surface exposed to 4.5 L oxygen. The average oxide thickness is 0.02 nm. STS on the clean Si (100) 2×1 (dashed line) is reproduced for comparison. Insert shows a typical line profile of the STM image. STS in the bright (protrusion) and the dark regions were averaged from the height range indicated as Region I and Region II, respectively. [73] The reduced LDOS at Region I suggests that the bright protrusion on the oxidized surface is the oxidized state of a Si atom.

Fig. 2.16

STS spectra of the Si surface after 15 L oxygen exposure at room temperature. The average oxide thickness is 0.2 nm. Insert shows a typical line profile of the STM image. STS spectra are taken from different height features, as indicated by regions I, II and III in the insert. [73]

Fig. 2.17 Averaged STS spectrum of a Si surface upon exposure to 10^4 L oxygen at room temperature. The average oxide thickness is 0.4 nm. Band edges of Si and SiO_2 can be identified. [73]

The above example was discussed in some detail to highlight the capability of STM to study highly local surface phenomena; in the above case, the initial stages of SiO_2 oxidation. Since dielectric breakdown is a localized phenomenon, many research groups have also turned to SPM techniques to complement conventional electrical measurement. Research in oxide reliability by SPM can be traced back to the early 1990s. Murrell *et al.* [74] and S. J. O'Shea *et al.* [75] were the first to utilize high resolution SPM techniques and addressed the non-uniformity problem in thick SiO_2 . They established the validity of CAFM in the study of thick oxide (~ 12 nm) and showed that the measured charge-to-breakdown and extracted work function (obtained by fitting the experimental data to the Fowler-Nordheim tunneling current expression) were in agreement with those obtained using MOSCAP structures [178], provided the “ohmic” condition of the tip was maintained.

In ref. 179, the authors addressed several experimental issues, including the importance of UHV environment in uncapped oxide study, and the effect of tip material on the value of the measured breakdown voltage. Watanabe *et al.* laid the

foundation for STM analysis on ultra thin oxide (~ 0.3 nm) based on band theory [76]. The band diagram of the system under study in ref. 100 (an ultra thin SiO_2 layer on n-Si) is reproduced in Fig. 2.18. Assuming the vacuum gap between the tip and sample is 1 nm, at a sample bias below 4.0 V the oxide acts as a tunneling barrier and STM images show the Si/ SiO_2 interface. On the other hand, when the sample bias is larger than 4.0 V, electrons tunnel into the oxide surface and the STM image represents oxide surface morphology. The ability of STM to image different interfaces depending on the applied bias will prove to be useful in our study of high- κ gate stacks.

Fig. 2.18 Band alignment between a n-Si substrate and W tip when +6.0 V (solid line) and +4.0 V (dashed line). Biases are applied to the sample [73].

Studies on ramp voltage stress (RVS) of SiO_2 by STM [77, 78] and CAFM [75, 178, 180-181] have been reported. It was observed that trapped charge is created during RVS to the FN tunneling regime. Based on the statistical distribution of breakdown voltage with different distance between the breakdown locations, Yasue [77] concluded that each breakdown location should have a minimum separation distance of 454 nm such that the measurement of breakdown voltage will not be affected by the trapped charge of neighboring breakdown spots. Zhang *et al.* [79], Porti

et al. [180], Fiorenza *et al.* [181] and Daniel *et al.* [78] have verified that the trapped charge induced during high voltage RVS is negative. Negative charge continues to accumulate until breakdown occurs, upon which a conductive spot surrounded by a less conductive ring is imaged [181]. Porti *et al.* further quantified that the required breakdown induced negative charge (BINC) are 25 and 35 electrons for current limiting and non-current limiting breakdown, respectively [180]. Zhang *et al.*, observed hillock formation prior to a breakdown event [79]. They attributed the hillock formation to Si substrate deformation, formed by a mechanism similar to that responsible for dielectric breakdown induced epitaxy (DBIE) [80, 81]. The area affected by breakdown is another topic of interest in the study of dielectric breakdown. The conventional method of area extraction can result in inaccuracy as the conduction mechanism at the breakdown location is ambiguous. Without knowledge of the physical and compositional properties of the breakdown path, the values of most parameters, e.g. effective mass of electron, dielectric constant, etc. are uncertain. SPM techniques offer direct measurement on the breakdown area. It has been shown that the breakdown area is larger than the tip-sample contact in CAFM [178] and can be controlled by limiting the breakdown current to 10^4 nm^2 and 10^5 nm^2 for current limiting and non-current limiting cases, respectively.

The process of wear-out under electrical stress has also been investigated under constant current stress (CCS) or constant voltage stress (CVS) over a certain area during STM [82-84] or AFM [85, 178, 181] imaging. Leakage spots are generated during CCS within the stressed area and the generation of leakage spots is found to be dependent on polarity [82], voltage [82, 83] and temperature [83]. Watanabe *et al.* exclude the role of electric field on trap generation during electrical stress based on the observation that leakage spot generation is polarity dependent [82]. The average STS

data, including the generated leakage spots, shows a negative shift compared to the averaged STS of a fresh oxide. The density of positive charge is estimated to be $1.7 \times 10^{13} \text{ cm}^{-2}$ from the negative shift and is comparable to the density of leakage spots. Hence, it was deduced that each leakage spot carries one positive charge⁴⁸. Stable and unstable defects which exhibit negative differential resistance (NDR) are observed on ultrathin SiON during STS acquisition. A stable defect has a broader peak with a full-width half-maximum (FWHM) of 1 V, whereas an unstable defect shows a peak with FWHM of 0.3 V. It is observed that stable defects can originate from unstable structures when the atomic-scale structure changes from an intrinsic Si-Si bond to a Si cluster during STM imaging. Nitrogen incorporation is shown to suppress the expansion of the damaged region but increase the intrinsic defect density [84]. In CVS experiments, the breakdown area is shown to be dependent on bias voltage [178] and the breakdown voltage is dependent on the biasing polarity [85]. The dependence of breakdown voltage on polarity is attributed to electric field enhancement at the tip [85].

The reports reviewed so far focused on uncapped SiO₂ or SiON, which can be far from being representative of the breakdown event on a working device. An experiment which is closer to the real world situation was reported by Porti *et al* [178]. In this experiment, breakdown was induced on a poly-Si gated MOSCAP structure by CVS using a semiconductor parameter analyzer (SPA). The poly-Si gate was then removed by etching in 10 % HF (5 s, to remove native oxide) followed by 10 % KOH (20 min). After the removal of the poly-Si gate, the bare oxide was imaged by CAFM. A single breakdown spot of area $\sim 2.5 \times 10^5 \text{ nm}^2$ was identified. The local conductivity at the breakdown spot was several orders of magnitude higher than the rest of the oxide. The local *I-V* curve measured by CAFM on the breakdown spot was similar to *I-V* measurements obtained on uncapped SiO₂ which had been driven to breakdown using

CAFM. The important implication from this result is that CAFM induced breakdown is a good representation of breakdown in a real device.

2.5.3.2. High- κ dielectrics

The electrical properties of high- κ dielectric have been studied using the conventional MOSCAP and MOSFET structure [20, 86]. The I - V characteristic has been found not to scale with area and thickness [17], indicating non-uniformity and the existence of localized leakage sites. As information obtained from MOSCAP or MOSFET structures is macroscopically averaged across a relatively large area, important information can be overlooked. Therefore, several research groups [87-90] started to study the properties of high- κ thin film using SPM. SPM study has been performed on high- κ materials such as HfO_2 [87, 89], HfSiO [88], HfSiON [88], ZrO_2 [89], Al_2O_3 [91, 92], etc. Most high- κ studies using SPM have concentrated on HfO_2 and these are summarized below. There are a few papers dealing with Al_2O_3 and ZrO_2 etc. Our study is the first to use SPM on La_2O_3 high- κ films.

Nitrogen incorporation, by means of plasma nitridation [93] or N_2 PDA [26, 94, 95, 96] into a HfO_2 film has been studied by CAFM. It was found that plasma nitridation is effective in terminating leakage paths in the high- κ film, thus improving uniformity. On the other hand, the density of localized conductive spots was found to increase upon N_2 annealing. Furthermore, the forward and reverse I - V curve for the annealed sample did not overlap each other, suggesting the presence of trapped charge generation upon I - V measurement. The effect of PDA temperature on the electrical behavior was investigated by CAFM [96], in combination with HR-TEM analysis. It was concluded that the increase in inhomogeneity on the sample subjected to annealing temperature beyond 900°C was due to the structural transition to a

polycrystalline film. Homogeneity of the HfO_2 and ZrO_2 film is also found to decrease with increasing film thickness due to increase surface roughness and crystalline fraction [89].

High- κ gate stacks differ from SiO_2 in that a SiO_x interfacial layer will be present for all high- κ films deposited on Si. The presence of at least a two-layer film (the high- κ bulk dielectric and the IL) changes the interpretation and SPM measurement approach required. Different conduction regimes are identified from a typical I - V characteristic (Fig. 2.19). For HfO_2 , these conduction regimes may be classified as (A) at low bias, carrier injection through a triangular HfO_2 barrier and a trapezoidal IL SiO_x barrier, (B) carrier injection at energies above the HfO_2 barrier and (C) dielectric breakdown [87]. It was found that, during substrate injection stress, conduction regime (B), which is controlled by the IL, remained invariant during low-field stress while the high- κ controlled conduction regime (A) shifted to lower voltage. During high-field stress, increments in current were observed in the high- κ controlled conduction regime (A), suggesting defect generation in the high- κ [97, 98] whereas IL-controlled conduction regime (B) showed an increase in current and noise, suggesting progressive breakdown of the IL layer. In short, defects are generated in the high- κ layer during low field stress and breakdown of the IL, leading to breakdown of the gate stack, occurs with increased electric field. These CAFM observations are in agreement with a device-level study [98], where degradation is shown to be dependent on the IL thickness. The major result is that traps can be generated in both the high- κ and IL layer during electrical stress but it is the IL breakdown that leads to irreversible breakdown of the entire gate stack.

Fig. 2.19 Different conduction regimes ((A) to (C)) identified from a typical I - V characteristic of a HfO_2 gate stack before breakdown (square). Conduction mechanism in (A) is attributed to tunneling through a triangular HfO_2 and trapezoidal SiO_x energy barrier (insert A: band diagram in the voltage regime A). Conduction mechanism in (B) is attributed to tunneling through a trapezoidal SiO_x energy barrier above the HfO_2 barrier (insert B: band diagram in the voltage regime B). Increase in leakage current in regime C is attributed to breakdown of the HfO_2 gate stack, upon which the I - V characteristic changes irreversibly. Typical I - V characteristic after breakdown is shown in circles, marked D. [87]

Reversible breakdown and switching between different conduction states were also observed in CAFM experiments [87]. In irreversible breakdown, the I - V characteristic is changed upon breakdown, suggesting a change in the conduction mechanism. The I - V characteristic of the irreversible breakdown area is stable and reproducible [87]. On the other hand, hysteresis of the I - V was observed in the case of reversible breakdown. Hysteresis appeared to prevent complete formation of a breakdown path, resulting in a reversible breakdown I - V characteristic.

In addition to RVS at a single location, constant voltage stress of an entire area shows degradation of the scanned area, where increased “bright spot” density is observed [90, 93]. The bright spots correspond to points of increased current flow (at constant voltage) arising from local degradation of the dielectric. The generation of

bright spots within the scanned area was shown to be independent of the biasing polarity and the current at the bright spot increased exponentially with bias [90].

Despite the progress made in nanoscale characterization and understanding of high- κ materials, there remain many major problems which can be greatly assisted by the use of SPM techniques. These problems include physical understanding on the PDA induced Weibull slope reduction, direct investigation of the mutual influence of electronic traps in the high- κ and the IL, direct correlation between atomic structural defects in the high- κ to transport mechanism and reliability performance of the gate stack, etc. In this thesis we directly address some of the above issues, namely (i) the physical understanding of the macroscopic electrical and TDDB analysis from nanoscopic perspective by STM; (ii) the intrinsic breakdown mechanism in a $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack at a localized area without the influence of pre-existing traps; (iii) influence of pre-existing electronic traps with different characteristics to the breakdown evolution in a $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack. Electrical stress is applied locally at a pre-existing electronic trap and further trap evolution in the vicinity of the pre-existing traps is monitored; and (iv) correlation between oxygen vacancy and the transport mechanism and reliability performance of a $\text{HfO}_2/\text{SiO}_x$ gate stack.

Chapter 3 Experiments

3.1 Introduction

Electrical characteristics of nano-scale devices are extremely susceptible to small perturbations in properties such as dimension, structure, roughness and defects. Furthermore, insertion of new materials into the conventional MOSFET, for instance, replacement of the SiO₂ or SiON gate dielectric with a high- κ material, presents further challenges. There have been several reports on the physical/electrical inhomogeneity of the ultrathin high- κ gate dielectric stack [17, 26, 95]. Inhomogeneity of the high- κ dielectric renders conventional characterization techniques (for example, *I-V*, *C-V* measurements on MOSCAP or MOSFET) difficult to interpret due to inconsistency and non-area/thickness scalability. Hence, precise metrology, especially metrology with high spatial resolution, is necessary [99].

The STM technique was conventionally developed to investigate electrical properties and morphology of conducting materials. However, since the thickness gate dielectric thickness has scaled down to a few nanometers, a tunneling current can be detected, allowing STM to be employed in the study of the ultrathin gate dielectric layer. The physical arrangement of the STM during the STM analysis (W tip with diameter of ~ 20 nm on a blanket gate stack) is fundamentally similar to a MOS capacitor having

nanometer-size W gate. Current injection occurs through the energy barrier defined by the tip and sample materials. The magnitude of the current is dictated by the width of the tunnel gap. Thus, provided a current flows and the tunnel gap is incorporated in the modeling, we can correlate the nanoscopic observation to the macroscopic J - V and C - V characteristics. Previous study has also justified the correlation between the conventional electrical measurement and nanoscopic SPM measurement techniques [178]. The STM technique, including the instrumentation, tip preparation and operation modes, will be presented in section 3.2. Deposition of the ultrathin high- κ gate stack is elaborated on in section 3.3. Lastly, the conventional conductance technique used in determining interface trap density in the macroscopic MOS capacitor structure, is presented in section 3.4.

3.2 STM Experiment

Fig. 3.1 shows a schematic view of a STM, where a very sharp metal tip is brought close to the sample (typically < 1 nm). When a bias voltage is applied across the tip-sample junction, electrons quantum mechanically tunnel across the gap and the resultant STM current is sensed by an ammeter. The current exponentially decays with increasing separation z (equation 2-9) and a very small change in z induces a large change in the tunneling current. In consequence, STM has an extreme magnification capability, down to the atomic scale, and z can be controlled in high precision.

Fig 3.1 (a) Schematic view of a STM [63, 100]. (b) The high precision of STM is due to the exponential dependence of tunneling current on z . In this particular figure, K and k are system (STM tip and sample under test) dependent constant whereas V is the sample bias voltage (with tip grounded).

3.2.1. STM instrumentation

The major instrument used in this research is an Omicron UHV STM, complete with a sample preparation chamber. The various components constituting the microscope can be classified into four categories, i.e. the scanning unit, electronics, computer automation and the mechanical unit. The scanning unit is responsible for the lateral and vertical motion of the STM tip. Electronics is required to establish the feedback loop for the tunneling current. Computer automation is necessary to acquire and store STM scan. The mechanical unit includes vacuum pumps and gauges for achieving UHV.

3.2.1.1. Scanning unit

The scanning unit of the STM is realized using piezoelectric drivers. An electric field applied across a piezoelectric material causes a change in the crystal structure, with expansion in some directions and contraction in others. A compact single tube scanner

(Fig. 3.2) is usually chosen for full three-dimensional movement of the tip and for its simplicity and high sensitivity. As shown in Fig. 3.2, the outer electrode is segmented into four equal sectors of 90° . Opposite sectors are driven by signals of the same magnitude but of the opposite sign. This gives, through bending, a two dimensional x, y movement. The inner electrode is driven by the signal required to move in the z direction.

Fig. 3.2 Schematic diagram of a single tube scanner

3.2.1.2. Electronics

Fig. 3.3 shows a block diagram of a general STM electronic system. The sample bias voltage is supplied by a computer controlled digital-to-analog converter (DAC). The tunneling current is measured by a preamplifier with a gain of $10^6 \sim 10^9$ V/A. The tunneling signal, which is exponentially dependent on z , can then be linearized by a logarithmic amplifier to improve the dynamic range (optional, but is important for samples with a relatively rough surface). The measured tunneling current is then compared with the required feedback value (or set point) and the resultant error signal is fed into a controller, which usually consists of a proportional (P) amplifier and an

analog integrator (I). The feedback signal from the controller output is finally fed into a high-voltage amplifier, which generates the amplified voltage signal applied to the z piezoelectric drive.

A sample-and-hold amplifier is inserted in the feedback circuit before the PI controller. It allows the error signal to be set to zero during a hold period so that the z piezo drive voltage does not change and the separation between sample and tip is kept constant.

Fig 3.3 Block diagram of STM electronic system.

3.2.1.3. Computer automation

A fully computer-automated STM system includes data acquisition, data processing and data visualization. The data acquisition software allows easy on-line change of experimental parameters such as sample bias voltage, tunneling current, feedback gain and scan area. The data analysis software allows 2-D Fourier transform, autocorrelation functions, etc. The data processing software includes interpolation and smoothing routines, a selection of filters including median, Fourier filters, etc. Finally,

a variety of means of data visualization, including a line scan representation and a grey-scale top-view representation can be derived from the raw data.

3.2.1.4. Ultra-high vacuum system

Anodic oxidation in STM experiment on Si surfaces in ambient has been well documented [101-104]. Water vapor (or adsorbed water) and oxygen in the ambient can dissociate to form the OH^- and O^{2-} ion, respectively. OH^- and O^{2-} ions diffuse through the native oxide to the SiO_2/Si interface (anode) during positive sample bias. The diffusion can be enhanced by the STM tip, where a localized electric field exists. As OH^- and O^{2-} ions enter the SiO_2/Si interface, they react with the H terminated P_b paramagnetic centers ($\text{H}-\text{Si} \equiv \text{Si}_3$), resulting in an oxidation process [103]. In the case where the OH^- and O^{2-} ions cannot diffuse completely through the oxide layer (i.e. remain in it), anodic oxidation is still possible by the reaction between OH^- or O^{2-} ions and E' paramagnetic centers that exist within the oxide bulk.

In order to avoid anodic oxidation in our experiment, an UHV environment is therefore essential. An UHV system has a pressure range of 10^{-10} mbar. Our UHV STM system pressure is sustained by a titanium sublimation pump (TSP) and a sputter ion pump.

Fig. 3.4 The UHV system consisting of a fast entry lock chamber, a preparation chamber and a STM analysis chamber.

The UHV STM system is made up of a fast entry lock (FEL) chamber, a preparation chamber and a STM chamber, as shown in Fig. 3.4. The sample or tip is loaded into the preparation and STM chamber via the fast entry lock chamber. As shown in the pumping system diagram (Fig. 3.5), the FEL chamber is pumped down to high vacuum level ($\sim 10^{-6}$ torr) by a rotary pump (RP), followed by a turbo molecular pump (TP), before the valve between the FEL chamber and the preparation chamber is open for sample/tip transfer. Tip sharpening, sample degassing and UHV annealing can be done in the preparation chamber. The sample/tip can then be transferred into the STM chamber for STM analysis. Up to eight samples or tips can be stored under

UHV in a carousel stage. Both preparation and STM chambers are maintained at UHV level at all times. The pressure level is monitored by hot cathode ion gauges, one in each of the preparation and STM chamber.

Fig 3.5 Pumping system diagram which shows the three main chambers (the analysis, preparation and fast entry lock chambers) and the respective pumps, gauges and valves.

3.2.2. Tip preparation

3.2.2.1. Tip etching

An important step in the successful operation of a STM is tip preparation. The tips should have a minimal radius of curvature (~ 10 nm) at the apex. Moreover, the diameter should be narrow enough to trace the morphology of the sample surface yet thick enough to keep the resonance frequency sufficiently high. Tungsten (W) or

Platinum Iridium (PtIr) wires were chosen as appropriate tip material due to their hardness. The W tip can only be used for experiments in UHV as W can oxidize in air, whereas PtIr tip can be used for STM experiments both in UHV and in ambient. W is preferred for UHV because very sharp tips can be readily made by electrochemical etching. An electron-beam (e-beam) bombardment after the tip is transferred into the UHV changer removes the native oxide on the W tip.

High quality W tip can be fabricated by electrochemical reaction under steady state DC condition with W and noble metals (for example, Au, Ag or Cu) as electrodes and Potassium Hydroxide (KOH) as an electrolyte [105]. The reaction governing the electrochemical etching is:

Figs. 3.6 and 3.7 show the “loop” etching setup used. A drop of etchant solution (2mol/l KOH) is placed on a Cu wire ring (the cathode). Surface tension enables the drop of KOH solution to stay on the ring. The W wire to be etched (the anode) is placed through the loop; capillary force creates a meniscus of solution around the tip wire. There exists a concentration gradient, hence a difference in etching rate, at the meniscus due to the diffusion of OH⁻ ions to the tip. Electrochemical reaction (3-1) starts when a voltage (<5 V) is applied across the Cu ring and the W wire. It takes a few minutes for the etching process to complete. The lower section of the wire falls away from the ring and is carefully collected in a narrow-walled cylinder, shorter than

the length of the lower tip, so that the tip apex does not touch the side wall. The tip was then cleaned by rinsing with distilled water, followed by ethanol, before it was transferred into the UHV chamber.

A distinct difference in the shape of the upper tip (i.e. that remaining above the Cu ring after etching process) and the lower tip (i.e. the dropped-off section) was observed. The upper tip generally has a conical profile due to surface tension, whereas the lower tip has a tapered profile. The lower tip is used for STM imaging in our experiments as it is much sharper. Typical optical microscope images of the upper and lower tip are shown in Fig. 3.8.

Fig. 3.6 Set-up for tip etching.

Fig 3.7 Schematic illustration of the W tip etching process – the “loop” technique.

Fig 3.8 Optical microscope image with $\times 5$ magnification of (a) the upper tip (b) the lower tip.

3.2.2.2. Tip sharpening

After the W tip is etched, it is transferred into the UHV system. Before the tip can be used for STM imaging, a tip sharpening process using high energy e-beam bombardment is necessary to remove the native oxide, which forms immediately after the etched tip is exposed to the ambient. Fig. 3.9 shows a photograph and a schematic diagram of the set up for tip sharpening within the UHV preparation chamber. The W filament supplies the electron beam required. The tip is placed about 2cm below the W filament, which is biased at 4 V with current of 1 A. The temperature of the tip holder

is raised to 400 °C and a voltage applied to the tip, which is ramped from 100 V to 1 kV, in increments of 100 V. The high voltage accelerates electrons from the W filament to the tip, where electrons gain high energy from the large electric field. An increase of current (to tens of μA) is observed when the native W oxide is ablated by the e-beam.

Fig 3.9 Photograph and schematic diagram of the tip cleaning and sharpening set up inside the preparation chamber.

3.2.3. STM modes of operation

There are many different ways in which data can be acquired using STM. We describe below the modes of operation found most useful for our research.

3.2.3.1. Constant current imaging (CCI)

During image acquisition, the tip is scanned across the sample. The motion of the tip is controlled by the piezoelectric scanner in the x and y directions. The feedback control adjusts the tip height (i.e. the z piezoelectric element of the scanner) to maintain a constant tunnel current (Fig. 3.10). The feedback signal, which is the tip height (also

known as the corrugation amplitude), is displayed as the STM image. The speed of scanning in the CCI mode is restricted by the time constant of the feedback circuit arising from the mechanical response time of the piezoelectric element. The STM CCI image gives convoluted information, being a mix of the surface morphology and local electronic properties of the sample.

Fig 3.10 Schematic illustration of the STM Constant Current Imaging mode (CCI).

3.2.3.2. Constant height imaging (CHI)

Fig. 3.11 Schematic illustration of STM Constant Height Imaging mode (CHI).

A drawback of the CCI mode is the finite response time of the feedback loop, which limits the scan speed and acquisition time. Alternatively, the feedback loop can be switched off as used in the constant height imaging mode (CHI). Modulation of the tunneling current reflects the topography provided that the response of the preamplifier is faster than the scan speed. Performance is improved in the CHI mode as the microscope is insensitive to most low-frequency disturbances, e.g. mechanical vibration. In addition, piezoelectric hysteresis of the scanning unit appears to be reduced and thermal drifts is less important because the image acquisition time can be rapid.

In general, STM data is collected using the CCI mode when imaging large areas or rough surfaces. The CHI mode is only used for imaging small surface areas, which are nearly atomically flat.

3.2.3.3. Scanning Tunneling Spectroscopy (STS)

In STS, the tip is positioned on the surface at a specific x/y location and current flowing between the tip and the substrate is recorded while the voltage is ramped over a predefined range. This yields a local I - V curve. During STS acquisition, the feedback loop is switched off and the relative positions of the sample and tip are therefore fixed. Generally, STS is repeated several times (~ 5) at each location and the averaged I - V signal is recorded. The dependence of the measured STS on z can be compensated by normalizing the differential conductance dI/dV to the total conductance, I/V , as discussed in section 2.5.1. The normalized quantity reflects the electronic density of states by minimizing the influence of the absolute value of z .

3.2.3.4. Constant current tunneling spectroscopy (CITS)

The ability to probe the local electronic structure down to atomic scale has great potential for investigation of surface chemical reactivity on an atom-by-atom basis. In order to eliminate the problem of thermal drift, which makes it virtually impossible to position the tip over a specific surface feature and acquire STS data, Constant Current Tunneling Spectroscopy (CITS) can be done. CITS is a technique to measure the local I - V characteristic at every pixel in an image. The method uses a sample-and-hold amplifier to alternately gate the feedback control on and off. When the feedback is active, a constant setpoint voltage V is applied to the sample and the tip height is adjusted to maintain a constant tunneling current as set by the user (i.e. the normal CCI mode). When the feedback is deactivated, the applied sample voltage is linearly ramped between two preselected values and the tunneling current is recorded at a fixed tip height. After the I - V curve is acquired, the applied bias voltage is set back to the chosen setpoint voltage V and the feedback system is reactivated. By acquiring the I - V curves while scanning the tip (note: at a sufficiently low speed to allow for reliable I - V data acquisition), a constant current topography image and spatially resolved I - V characteristics can be simultaneously obtained. From the spatially resolved I - V information, images of the current flow at chosen bias voltages, V' , different from the setpoint voltage V_s , can be formed. The current images depend on the contour that the tip follows during scanning, which is determined by the setpoint voltage V_s and current. Essentially, these current images represent the spatial distribution of the tunneling current measured at V' normalized by the tunneling current at V_s . Contrast in the current images can arise either from differences of surface electronic states or from surface morphology. Hence, one has to be cautious in the interpretation of CITS

current images before associating specific ‘topographic’ features to individual electronic states.

The presence of low frequency noise in our STM makes it difficult to always acquire decent CITS images. Despite the use of several low pass filters, the noise in the measured current persisted. However, with careful selection of the scanning parameters, it was possible to solve the problem. As observed on an oscilloscope, the STM needed a time in the range of a few microseconds to stabilize every time the sample voltage was ramped to the next voltage level during a CITS measurement. By setting a sufficiently long delay time in the CITS acquisition software ($\sim 1280 \mu\text{s}$), we were able to obtain a reliable current reading. Note that one cannot use arbitrarily long delay and acquisition times because this would lead to problems related to thermal drift. Hence a trade-off between scanning speed and I - V acquisition is necessary.

3.2.3.5. Ramp voltage stress (RVS)

The breakdown strength of the gate dielectric stack was examined by RVS. RVS is the same as STS, with (i) a much wider voltage range compared to that used for normal STS characterization of the film properties and (ii) the feedback control is not activated in-between each STS measurement. This is necessary because otherwise the tip would retract to compensate for the increased conductivity of the dielectric upon breakdown. Hence, direct comparison between RVSs can be done without complications arising from changes in tip-sample separation z .

To avoid ambiguity caused by thermal drift, RVS should be completed within a few seconds. This ensures that any change in the observed I - V characteristic is not from changing of tip position due to thermal drift, but arises from the electrical stressing of the dielectric material.

3.3. Sample preparation

The samples under STM investigation are (i) sample A: $\text{HfO}_2/\text{SiO}_x$ gate stack on p-Si substrate and (ii) sample B: $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack on n-Si substrate, subjected to different post deposition annealing (PDA) temperatures. Sample A (the $\text{HfO}_2/\text{SiO}_x$ gate stack) was produced in Institute of Materials Research and Engineering. Sample B (the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack) was produced at Frontier Collaborative Research Center in Tokyo Institute of Technology.

The HfO_2 (sample A) was deposited by pulsed laser deposition (PLD) on a p-type Si(100) substrate in UHV with the background pressure controlled at 5×10^{-10} Torr. After the deposition of Hf metal by sputtering, the wafer was transferred to a plasma oxidation chamber without breaking the vacuum. An oxygen plasma was then produced by an inductive coupled coil with a rf power of 100 W at a pure oxygen pressure of 1.0 Pa.

The $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack (sample B) was formed on an n-Si substrate by e-beam vapor deposition in UHV. The doping concentration of the Si substrate is $3 \times 10^{15} \text{ cm}^{-3}$. The resistance of the Si substrate (a few ohms) is relatively negligible when compared to the oxide film ($\sim \text{G}\Omega$). In addition, an ohmic contact is formed at the backside. Hence, the resistance of the substrate is a linear function and there is no influence to the exponential I - V or I - z correlation. The results of our study are consistent with p-type Si as electron tunneling dominates for both p and n-type Si substrate. Hole tunneling is relatively negligible in our study due to the asymmetrical band structure of the gate stack under study. The Si substrate was first dipped in sulfuric peroxide solution at 85°C for 5 min to remove organic contamination. The solution is made up of 4 parts of H_2SO_4 (96%) and 1 part of H_2O_2 (30%). A subsequent dip in a diluted hydrofluoric acid (1% HF) bath helped remove native oxide layers and achieve a stable hydrogen-terminated surface. Once cleaned, the

substrate was then transferred into the UHV chamber for subsequent electron-beam evaporation of the La_2O_3 and Sc_2O_3 dielectrics. In the growth chamber, a sintered La_2O_3 target, which was the evaporation source, was irradiated with an electron beam of 5 keV energy. With the target heated, LaO_x molecules were evaporated and a thin layer of LaO_x film was deposited on the Si-substrate. A similar procedure was repeated using a Sc_2O_3 target after the La_2O_3 deposition. Hence, a thin layer of Sc_2O_3 was deposited on top of the La_2O_3 thin film. The Sc_2O_3 serves as a protection for the hygroscopic La_2O_3 layer. The background pressure in the growth chamber was approximately 10^{-7} Pa during deposition and the substrate temperature was maintained at 300 °C during the deposition. The physical thickness of the film was monitored using a crystal oscillator. The gate stacks were subjected to post-deposition annealing at 300 °C, 500 °C and 700 °C in nitrogen for 5 minutes. Samples for STM analysis received no further processing steps. Ohmic contact is formed by evaporating a layer of metal of similar Fermi level (in this case, Ag was chosen for n-Si substrate). Samples for macroscopic electrical measurement went through further lithography and W deposition steps for capacitor fabrication.

Table 3.1 shows physical thickness of each layer and electrical oxide thickness (EOT) for the respective samples. Physical thickness is measured from high-resolution transmission electron microscopy (HR-TEM) whereas EOT is approximated from C - V measurement. There is no distinct interface between the Sc_2O_3 and La_2O_3 interface for the 500 °C N_2 PDA sample. This unique physical structure of the 500 °C N_2 PDA sample also explains the exceptional electrical properties of this particular sample, for example, 500 °C N_2 PDA sample shows lowest gate leakage current and lowest interface trap density (both observed from frequency dependent C - V measurement and STM). It should be emphasized that the composition in each layer may not be the stoichiometric oxide as its name suggests (e.g. Sc_2O_3). The naming of each layer by its

stoichiometric composition is only for consistency purpose. The electrical (by J - V , C - V and STM) and the physical (tof-SIMS and XPS) properties will be further investigated in Chapter 4.

	Sc ₂ O ₃ (nm)	La ₂ O ₃ (nm)	SiO _x (nm)	EOT
As deposited	2.4	4.7	0.9	1.3
300 °C N ₂ PDA	2.6	4.5	1.2	1.5
500 °C N ₂ PDA	7.9		1	1.9
700 °C N ₂ PDA	2.3	4.5	2	2.8

Table 3.1 Physical thickness of the Sc₂O₃/La₂O₃/SiO_x gate stack with N₂ PDA at different temperature. TEM result is in courtesy of X. Li; C - V data is in courtesy of K. Kakushima.

3.4. Conductance measurement

Macroscopic electrical characteristics of the high- κ thin films are measured by J - V , C - V and the conductance method using MOS capacitor structures. Conductance measurement was first proposed by Nicollian and Goetzberger to determine interface trap density (D_{it}) [106]. The technique provides high sensitivity and has the capability of detecting D_{it} as low as $10^9 \text{cm}^{-2} \cdot \text{eV}^{-1}$. The conductance method measures the equivalent parallel conductance G_p of a MOS capacitor as a function of biasing voltage and frequency. G_p represents the loss mechanism due to interface trap capture and emission of carriers, i.e. the information on D_{it} .

Fig. 3.12a shows the simplified equivalent circuit of a MOS capacitor. It consists of the oxide capacitance C_{ox} , substrate capacitance C_s , and capacitance contributed by interface traps C_{it} . The capture-emission of carriers by interface traps is a lossy process, and is represented by the resistance R_{it} . The circuit can be replaced by Fig. 3.12b, with C_p and G_p given as:

$$C_p = C_s + \frac{C_{it}}{1 + (\omega\tau_{it})^2} \quad (3-2)$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1 + (\omega\tau_{it})^2} \quad (3-3)$$

where

$$C_{it} = q^2 D_{it} \quad (3-4)$$

$$\omega = 2\pi f \quad (3-5)$$

$$\tau_{it} = R_{it} C_{it} = [v_{th} \sigma_p N_A \exp(-q\phi_s / K_B T)]^{-1} \quad (3-6)$$

and f is the measurement frequency, q is the electron charge, v_{th} , σ_p and N_A are the thermal velocity, mobility and doping concentration of the majority carrier, respectively, ϕ_s is the work function of the substrate and K_B is the Boltzmann constant. Capture and emission occurs primarily by traps located within a few $K_B T/q$ above and below the Fermi level, but not at a single energy level as implied from equations (3-2) and (3-3). Therefore the dispersion or distribution of the time constant (τ_{it}) must be taken into consideration. The normalized conductance is modified as,

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \ln[1 + (\omega\tau_{it})^2] \quad (3-7)$$

Equations 3-3 and 3-7 show that G_p is easier to interpret than the capacitance due to the absence of C_s in the equation. G_p/ω has a maximum at $\omega \sim 2/\tau_{it}$ and the corresponding $D_{it} = 2.5 G_p/q\omega$. Hence, D_{it} can be determined readily from the maximum of G_p/ω .

The LRC meter used in our experiments assumes the device to consist of the parallel C_m - G_m combination as shown in Fig. 3.12c. Assuming negligible series resistance, G_p can be written in terms of the measured parameters C_m and G_m as,

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (3-8)$$

Fig. 3.12 Equivalent circuits for conductance measurement; (a) MOS-capacitor with interface trap time constant $\tau_{it}=R_{it}C_{it}$, (b) simplified circuit of (a), and (c) measured circuit.

In summary, the experimental procedures for sample preparation and characterization techniques are reviewed in this chapter. Sample deposition techniques include PLD and e-beam evaporation methods. Nanoscale analysis by STM in different operating modes and macroscopic interface trap density measurement by conductance measurement on a MOS capacitor are discussed.

Chapter 4 THERMAL EFFECTS IN HIGH- κ GATE STACK – A NANOSCOPIC PERSPECTIVE

4.1 Introduction

Adoption of high- κ gate dielectric in the advanced metal-oxide-semiconductor (MOS) field-effect transistor is a logical extension to mitigate the exponentially increasing gate leakage that arises from the downscaling of the ultra-thin SiO₂. But several major concerns remain, one of them being the reliability of the high- κ gate stack [5, 9, 38, 107]. Statistical studies have shown that the shape parameter or slope β of the Weibull distribution of the time-to-breakdown of MOS structure employing the high- κ dielectric is much smaller than that of the SiO₂ counterpart [5, 9, 38, 107]. Explaining this result in the context of the percolation model would require the assumption of an unrealistically large defect size (~ 10 nm for a κ value of 20). Moreover, β is observed to be (i) much smaller for a high- κ gate stack subjected to gate injection stress (as compared to substrate injection stress) and (ii) independent of the thickness of the high- κ dielectric [5]. A small Weibull slope has serious implications on the reliability margin of the high- κ gate stack, in terms of its area scalability [38, 107]. On the other hand, contemporary studies [25, 26] based on scanning probe microscopy have

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revealed the existence of localized conduction paths in the high- κ gate stack after thermal annealing, and the density of these conduction paths increases with annealing temperature. Since gate dielectric breakdown is a localized event which takes place by the formation of some conductive paths in the gate dielectric, the task then is to examine the electrical characteristics of these thermally induced conduction paths to clarify the physics behind the polarity dependent statistical distributions of the breakdown time as observed from electrical stressing of the large-area MOS structure. This issue will be addressed in Chapter 4 from a nanoscopic perspective, leveraging on the high lateral resolution of STM.

Section 4.2 summarizes the deposition and characterization techniques used on the gate stack under study, i.e the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$. The fundamentals of the polarity dependent STM image is established in section 4.3. Topography images of the polycrystalline high- κ layer can be obtained at positive sample bias. The grain size distribution of the polycrystalline layer is in good agreement with the TEM plan-view image. An amorphous like image (with granular structure of diameter smaller than 5 nm), similar to SiO_2 topography images in the literature, is obtained at negative sample bias. Topography images at negative sample bias correspond to the morphology and electrical property of the SiO_x/Si interface. This polarity dependence imaging enables the demarcation of the electronic traps in the high- κ or interfacial SiO_x layer. The principle of the polarity dependent STM current is then applied to study the effect of post deposition annealing (PDA) on the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack in section 4.4. We show that the current through the localized conduction paths under gate injection biasing may be increased over that observed under substrate injection biasing to a much greater value with increasing annealing temperature. This observation implies that thermal annealing has a greater impact in lowering the

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tunneling barrier at the metal/high- κ interface than that of the Si/SiO_x interface. As a consequence, these localized conduction paths exhibit a much lower resistance under gate injection biasing, rendering the high- κ gate stack more susceptible to breakdown under gate injection stress (hence, smaller β). In section 4.5, we report the observation of different types of localized I - V characteristics in the gate stack. Two possible explanations are proposed for the leakage characteristics, namely barrier height lowering and trap-assisted tunneling.

4.2 Experiments

The Sc₂O₃/La₂O₃/SiO_x gate stack was formed on an n type Si substrate via electron-beam vapor deposition in ultra-high vacuum. The Sc₂O₃ serves as a protective layer for the hygroscopic La₂O₃. Samples for STM received no further processing, except for some which were subjected to post-deposition annealing at 300, 500 or 700 °C in nitrogen. STM imaging was achieved using a tungsten tip in ultra-high vacuum ($\sim 10^{-10}$ Torr). The tip was always grounded and a bias was applied to the sample. Before STM imaging, the sample was ultrasonically cleaned in acetone, followed by isopropyl alcohol. The profile of the gate stack was examined using high-resolution transmission electron microscopy (HR-TEM). Chemical composition was examined by x-ray photoemission spectroscopy (XPS) and time-of-flight secondary ion mass spectroscopy (tof-SIMS). Macroscopic electrical characteristics are also studied in terms of current density-voltage (J - V) measurement and capacitance-voltage (C - V) measurement.

4.3 Nano-characterization by scanning tunneling microscopy -- Polarity dependent tunneling current

Fig. 4.1 depicts transmission electron microscope (TEM) images of the dielectric stack. An amorphous Sc_2O_3 layer and a polycrystalline La_2O_3 layer are evident (Fig. 4.1b). For the latter, a mean grain size of approximately 22 nm is obtained from the plan-view TEM image (Fig. 4.1b). Based on the layer thickness information obtained from the cross-sectional TEM image (insert) and STM current-distance (I - z) analysis (Fig. 4.2), we can estimate the sample bias needed to image different layers of the gate stack.

Using the I - z results, the vacuum gap (i.e. spacing between the metal tip and high- κ) was estimated to be in the range of 0.2~0.4 nm for the STM biasing conditions used in this work. In Fig. 4.2 $z = 0$ is the position where the STM is controlling (i.e. 20 pA) during operation. The tunnel gap collapses (i.e. the tip is essentially in contact with the surface) at $z \approx -0.3$ nm. This is where the tunneling current starts to deviate from the exponential dependency when the tip is driven towards the sample.

Using the reported band gap value and dielectric constant of each material [108, 109], an energy band diagram at zero bias can be constructed, as shown in Fig. 4.3. The energy barrier from the Si Fermi level to the conduction band minima of Sc_2O_3 , La_2O_3 and SiO_x are approximately 2.2, 2.6 and 3.6 eV, respectively [108, 109]. Using κ values of 14, 21, and 3.9, for Sc_2O_3 , La_2O_3 and SiO_x , respectively and modeling the 4 layers (including the vacuum gap) as 4 capacitors in series, the voltage drop across a given dielectric layer V_n can be estimated as

$$V_n = \frac{\frac{t_n}{\kappa_n}}{\sum_{n=1}^4 \frac{t_n}{\kappa_n}} \times V_s, \quad (4-1)$$

where t_n and κ_n are the physical thickness and the relative permittivity of the given dielectric layer, and V_s is the sample bias. Here, n is the layer number (Fig. 4.3) where $n = 1$ denotes the vacuum gap, $n = 2$ the Sc_2O_3 layer, $n = 3$ the La_2O_3 and $n = 4$ the interfacial SiO_x layer. At positive sample bias, one estimates that at a bias of +3.3 V (giving $V_1 + V_2 + V_3 = 2.6$ eV) to +3.6 V (giving $V_1 + V_2 = 2.2$ eV, the Sc_2O_3 conduction band edge), the conduction band of the La_2O_3 layer would be probed. It is important to stress that the calculated voltage range +3.3 V to +3.6 V only provides an indication to assist experimental measurements. Even within this simple model there are several unknown factors, such as localized changes in barrier height, the voltage drop across the n-Si inversion layer (at most 0.6 V, which increases the voltages to probe the La_2O_3 layer by about 17 %), and the precise STM tip geometry (this effect is small; our simulations show that the voltage distribution across the 0.4 nm vacuum gap in the simplified parallel plate geometry of equation 4-1 is exactly the same when the tip is modeled as a sphere with radius of 5 nm).

Fig. 4.1 (a) Cross section TEM of the as-deposited $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ high- κ gate stack, (b) the corresponding plan-view TEM. Courtesy of X. Li and L. J. Tang.

Fig. 4.2 Five reproducible I - z characteristics taken at a single location. The STM control conditions, which defines the $z = 0$ tip to sample separation are -4 V, 20 pA. The vacuum gap is found to vary between 0.2 to 0.4 nm.

Figure 4.3 Band diagram of the system under study. Thickness estimated from TEM micrograph are 3 nm ($n = 2$), 4 nm ($n = 3$) and 1 nm ($n = 4$). The vacuum gap ($n = 1$) is taken as 0.5 nm.

At a negative sample bias, the tunneling current is contributed by electrons from the conduction and valence bands of the n-Si substrate. The former dominates the tunneling current, by virtue of an approximately 1 eV lower potential barrier. As the

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tunneling current is most sensitive to the structure of the electron-emitting interface [110], the interfacial SiO_x layer can be imaged and studied under negative sample biasing. Theoretical evidence to support this argument is shown below, by the calculation of tunneling probability at different biasing polarity using the Wentzel-Kramers-Brillouin (WKB) approximation. The two high- κ layers (i.e. the Sc_2O_3 and La_2O_3 layers), which have similar barrier height, are therefore grouped as one high- κ layer to simplify calculation (Fig. 4.4). The κ value and effective layer thickness can be estimated as,

$$\frac{t_2}{\kappa_2} + \frac{t_3}{\kappa_3} = \frac{t_{H\kappa}}{\kappa_{H\kappa}} \quad (4-2)$$

giving $\kappa_{H\kappa} = 7$ and $t_{H\kappa} = 3$ nm. The definition of the variables used in the WKB approximation is shown in Fig. 4.4. Note that the numbering for each layer has been redefined with Sc_2O_3 and La_2O_3 combined into one high- κ layer ($n=2$). The numbering system in Fig. 4.4 will be the reference in the tunneling calculation based on the WKB approximation. Fig. 4.5 shows the band diagrams of the three-layer model during (a) negative and (b) positive sample bias.

The quantum mechanical tunneling probability is given by equation 4-3 based on the WKB approximation [111, 112], where k_n^{im} is the imaginary part of the complex electron wave vector k_n (equation 4-4) of the tunneling electrons within layer n . A one-band parabolic dispersion relationship was used to calculate k_n (equation 4-5). The tunneling probability (T_t) can be expressed as a function of the total energy (E) with respect to the conduction band edge of each layer ($E_n^c(x)$) and x_n . x_n is the distance from the cathode interface to the classical turning point of the n^{th} layer, k_t is the transverse component of the wave vector k_n , m_n is the effective mass of the tunneling electron in the n^{th} layer, and V is the applied biasing voltage. A detailed derivation of

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x_n is presented for either direct tunneling or Fowler-Nordheim tunneling in each layer under tip (equations 4-10 to 4-12) and substrate (equations 4-16 to 4-18) injection bias. The potential profile in each layer is shown in equations 4-7 to 4-9 for tip injection and equations 4-13 to 4-15 for substrate injection.

Fig. 4.4 Energy band diagram of a simplified gate stack with Sc_2O_3 and La_2O_3 grouped as one high- κ layer ($n = 2$). The SiO_x layer is labeled $n = 3$ in the WKB calculation.

Fig. 4.5 Band diagram used in the WKB calculation at (a) negative sample bias (i.e. substrate injection) and (b) positive sample bias (i.e. tip injection). The thicknesses and barrier height are not to scale.

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$$T_i(E, k_i) = \exp - \frac{4\pi}{h} \sum_{n=1}^3 \int_{x_{n-1}}^{x_n} k_n^{im}(E, k_i, x) dx \quad (4-3)$$

$$k_n = k_i + ik_n^{im} \quad (4-4)$$

$$k_n^2(x) = \frac{8\pi^2 m_n}{h^2} [E - E_n^C(x)] \quad (4-5)$$

$$T_i \propto \exp - \frac{4\pi}{h} \left\{ \int_{x_2}^{x_3} \sqrt{-2m_{ox}(E - E_{ox}^C(V, x))} + \int_{x_1}^{x_2} \sqrt{-2m_{h\kappa}(E - E_{h\kappa}^C(V, x))} + \int_0^{x_1} \sqrt{-2m_{vac}(E - E_{vac}^C(V, x))} dx \right\} \quad (4-6)$$

Tip injection case

$$E_{vac}^C(V, x) = E_1^C(V, x) = \phi_{tip} - \frac{V_1}{t_1} x \quad (4-7)$$

$$E_{h\kappa}^C(V, x) = E_2^C(V, x) = \phi_{tip} - V_1 - \delta_{12} - (x - t_1) \frac{V_2}{t_2} \quad (4-8)$$

$$E_{ox}^C(V, x) = E_3^C(V, x) = \phi_{tip} - V_1 - \delta_{12} + \delta_{23} - (x - t_1 - t_2) \frac{V_3}{t_3} \quad (4-9)$$

$$x_1 = \begin{cases} t_1, & V_1 \leq \phi_{tip} \\ t_1 \frac{\phi_{tip}}{V_1}, & V_1 > \phi_{tip} \end{cases} \quad (4-10)$$

$$x_2 = \begin{cases} t_1 + t_2, & V_1 + V_2 \leq \phi_{tip} - \delta_{12} \\ t_1 + t_2 \frac{\phi_{tip} - V_1 - \delta_{12}}{V_2}, & V_1 + V_2 > \phi_{tip} - \delta_{12} \geq V_1 \\ t_1, & V_1 > \phi_{tip} - \delta_{12} \end{cases} \quad (4-11)$$

$$x_3 = \begin{cases} t_1 + t_2 + t_3, & V \leq \phi_{tip} - (\delta_{12} - \delta_{23}) \\ t_1 + t_2 + t_3 \frac{V_3 - (V - \phi_{sub})}{V_3}, & V > \phi_{tip} - (\delta_{12} - \delta_{23}) \text{ and } V_1 + V_2 \leq \phi_{tip} - (\delta_{12} - \delta_{23}) \\ t_1 + t_2, & V_1 + V_2 > \phi_{tip} - (\delta_{12} - \delta_{23}) \end{cases} \quad (4-12)$$

Substrate injection case

$$E_{ox}^C(V, x) = E_3^C(V, x) = \varphi_{sub} - \frac{V_3}{t_3} x \quad (4-13)$$

$$E_{H\kappa}^C(V, x) = E_2^C(V, x) = \varphi_{sub} - V_3 - \delta_{23} - (x - t_3) \frac{V_2}{t_2} \quad (4-14)$$

$$E_{vac}^C(V, x) = E_1^C(V, x) = \varphi_{sub} - V_1 - V_2 - \delta_{23} + \delta_{12} - (x - t_1 - t_2) \frac{V_1}{t_1} \quad (4-15)$$

$$x_3 = \begin{cases} t_3, & V_3 \leq \varphi_{sub} \\ t_3 \frac{\varphi_{sub}}{V_3}, & V_3 > \varphi_{sub} \end{cases} \quad (4-16)$$

$$x_2 = \begin{cases} t_2 + t_3, & V_2 + V_3 \leq \varphi_{sub} - \delta_{23} \\ t_3 + t_2 \frac{\varphi_{sub} - V_3 - \delta_{23}}{V_2}, & V_2 + V_3 > \varphi_{sub} - \delta_{23} \geq V_3 \\ t_3, & V_3 > \varphi_{sub} - \delta_{23} \end{cases} \quad (4-17)$$

$$x_1 = \begin{cases} t_1 + t_2 + t_3, & V \leq \varphi_{sub} - (\delta_{23} - \delta_{12}) \\ t_3 + t_2 + t_1 \frac{V_1 - (V - \varphi_{tip})}{V_1}, & V > \varphi_{sub} - (\delta_{23} - \delta_{12}) \text{ and } V_2 + V_3 \leq \varphi_{sub} - (\delta_{23} - \delta_{12}) \\ t_3 + t_2, & V_2 + V_3 > \varphi_{sub} - (\delta_{23} - \delta_{12}) \end{cases} \quad (4-18)$$

The tunneling probability under tip (closed square) and substrate (open circle) injection bias calculated using the WKB approximation is shown in Fig. 4.6. The contribution from hole tunneling is relatively insignificant due to a larger hole energy barrier arising from the asymmetrical band alignment (the electron barrier is 3.3eV and the hole barrier is 4.5eV at Si/SiO_x interface). The calculation shows that tunneling probability is asymmetrical, with lower probability under tip injection bias at low voltage. Lower tunneling probability could come from an additional voltage drop across the inversion layer in the n-Si substrate when biased positive. A cross-over is observed at ~ 4.5 V, beyond which the tip injection tunneling probability is larger than

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the substrate injection probability. The cross-over happens when both the high- κ and IL go into the FN tunneling regime under tip injection bias. The cause of the cross-over may be explained using Figs. 4.7 and 4.8 showing the band diagram of the gate stack corresponding to the different voltage regimes.

Fig. 4.6 Tunneling probabilities (T_t) at both polarities in different tunneling regimes. A cross-over for tip (closed square) and substrate (open circle) injection current occurs at ~ 4.5 V when both high- κ and IL enter into the FN tunneling regime.

Fig 4.7 shows tunneling probability under tip injection bias. Three distinct regions can be observed. The calculation starts at sample bias of 0.8 V with the assumption that the voltage drop across the substrate is 0.7 V in inversion. The low voltage regime labeled (a) is attributed to the direct tunneling mechanism where electrons encounter three trapezoidal energy barriers. Fowler-Nordheim (FN) tunneling through the high- κ (with direct tunneling through the vacuum and SiO_x interfacial layer) explains a steeper slope in regime (b). The curve saturates at regime (c) where current flow is dominated by direct tunneling through the vacuum layer. Tunneling mechanism in each layer is dependent on the band bending due to an applied bias. All the possible combination of tunneling mechanisms has already been taken into account during the calculation as clearly outlined above (equations 4-10 to 4-12).

A similar observation is applicable to substrate injection bias (Fig. 4.8) where the three distinct tunneling regimes are attributed to: (a) direct tunneling through all three layers, (b) FN tunneling through the IL with direct tunneling through the vacuum, and (c) FN tunneling through the oxide layer. Tunneling probability in regime (c) under tip injection bias is larger than that under substrate injection bias as the vacuum layer is much thinner than the SiO_x interfacial layer.

Fig. 4.7 Tunneling probability vs sample bias under tip injection biasing. Different tunneling regimes can be identified, as described by the inserted band bending diagrams. The solid arrows indicate electron flow.

Fig. 4.8 Tunneling probability vs sample bias during substrate injection bias. Different tunneling regimes can be identified, as described by the inserted band bending diagrams. The solid arrows indicate electron flow.

By choosing STM conditions in regime (b) for tip and substrate injection, both high- κ and IL can be probed independently. Two factors that contribute to the different sensitivity of tunneling probability to the different layers are:

- (i) Asymmetry of the stacked structure: Owing to the asymmetric stacked structure, band bending is asymmetrical at different biasing polarities. Hence, FN tunneling can occur independently within each layer at different bias. For example, regime (b) during tip (Fig. 4.7) and substrate (Fig. 4.8) injection are the FN tunneling regime for high- κ and IL, respectively.
- (ii) Tunneling mechanism: As shown in Fig. 4.9, tunneling is far more sensitive to the barrier variation at the electron injecting interface i.e. the cathode. The electron collecting interface (i.e. the anode) has insignificant contribution to the total tunneling

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current. The calculation was performed by assuming an electronic trap with diameter 6 Å [113] located near the cathode or the anode of a single layer dielectric material with barrier height of 2.3 eV (i.e. the conduction band offset between La_2O_3 and Si). The electronic trap is assumed to induce energy states from 1 eV to 1.6 eV below the conduction band minima of the dielectric [114]. Hence, tunneling probability is calculated with a barrier height lowered by an amount varying from 1 eV to 1.6 eV at 2 V (for direct tunneling) and 3 V (for FN tunneling).

Therefore, during tip injection, tunneling probability is most sensitive the tip/high- κ interface whereas during substrate injection, tunneling probability is most sensitive to the Si/SiO_x interface.

Fig. 4.9: Variation of tunneling probability with lowering of barrier height at the cathode/dielectric interface (open square for DT current, solid line for FN current) and dielectric/anode interface (closed square for DT current, dotted line for FN current). The barrier height lowering simulates the presence of an electronic trap. Tunneling probability is much lower and is insensitive to the barrier height lowering at the dielectric/anode interface.

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Fig. 4.10a shows a STM topography image obtained at a sample bias of +3.5 V, with a feedback tunneling current of 20 pA. A tunneling current of 20 pA is selected to avoid crashing the tip onto the (insulating) sample, yet is sufficiently large to maintain good signal to noise ratio. Granular structure of diameter varying from 10 to 40 nm is evident. The CITS image at +2 V is shown in Fig. 4.10b. CITS images at sample bias ranging from +1 to +2.5 V consistently show a higher tunneling leakage at the edge of the grains, due possibly to dangling bonds at the grain boundary. Fig. 4.10c depicts topographical profile along the line AB cutting across a grain. The corresponding current profile (Fig. 4.10d) shows a distinctly lower leakage current within the grain, in contrast to the much higher leakage current at the boundary. This direct observation of a high leakage current at the grain boundary of a high- κ gate dielectric lends support to the hypothesis of grain boundary assisted breakdown of HfO_2 [115]. In order to obtain the grain size distribution from the STM image, a larger area of 200 nm $\times$ 200 nm is scanned at +3.5 V, 20 pA. The STM image, together with a TEM plan-view of the same sample, is shown in Fig. 4.11. The STM image and TEM plan-view were taken from different part of the same sample. Hence, the distribution of the grain size is compared instead of mapping each grain of both images. Estimation of the grain diameter from both techniques is shown in Fig. 4.12. The estimated grain size can be approximated by a Gaussian distribution. The average grain sizes are 22 nm and 27 nm, obtained from STM and TEM plan-view technique, respectively. The slightly larger grain size observed in STM, as compared to that estimated from planar TEM, may be attributed to a finite tip size.

Fig. 4.10 (a) STM topography at +3.5 V, 20 pA. The positive bias condition images the high- κ interface. The z scale ranges from 0 to 6 nm; (b) corresponding CITS current map at +2 V. The variation in current is from 0 to 5 pA; (c) line profile of the topography along line AB, cutting across a grain; (d) corresponding current profile along line AB.

Fig. 4.11 (a) STM topography of an 200 nm×200 nm area; (b) plan view TEM for the same gate stack. Plan view TEM result is in courtesy of L. J. Tang.

Fig. 4.12 Grain size measured from STM (blue line) and plan-view TEM (red line) techniques. Plan-view TEM result is in courtesy of L. J. Tang.

Scanning at -4 V, an amorphous like image was revealed (Fig. 4.13a). As discussed above, under a negative sample bias, the tunneling current is more sensitive to the barrier of the electron-emitting interface, i.e. the interface between SiO_x and Si. Hence the STM image at -4 V provides convoluted information on the SiO_x/Si morphology and electrical properties. The STM topography shows a root-mean-square roughness of 0.34 nm and granular structures of ~ 5 nm diameter. In order to separate the electrical properties from morphology, a CITS image was used for comparison (Fig. 4.13b). The bright features in the CITS image correspond to regions with higher tunneling current at a given voltage. A higher tunneling current can arise from electrical defects (e.g. oxygen vacancy, crystal defects) or a smaller physical thickness. High tunneling current regions due to a thinner film will appear dark in the STM image (Fig. 4.13a) but bright in the CITS image (Fig. 4.13b). These locally thinner film regions are labeled “T”, highlighted by dash-dot circles in Fig. 4.13. On the other hand, an electrical defect giving rise to a higher leakage current will appear bright in both STM and CITS images. Such defects are labeled “E”, highlighted by solid circles

in Fig. 4.13 and their density estimated from the CITS image is $\sim 4 \times 10^{11} \text{ cm}^{-2}$. The direct observation of leakage current induced by thickness variation (i.e., the type T bright spots) gives a physical explanation to the lack of thickness/area-scalability of I - V characteristic of the La_2O_3 MOS capacitor [17]. The existence of defect/electronic traps induced leakage current (i.e. the type E bright spots) provides direct evidence for the coexistence of both space-charge-limited [116] and direct tunneling [17] current.

Fig. 4.13 (a) STM topography at -4 V, 20 pA. The negative bias condition images the SiO_x/Si interface. The z scale ranges from 0 to 3 nm; (b) corresponding CITS current map at -2 V. The variation of current is 0 to 5 pA.

In summary, the capability of STM for nanocharacterization of an advanced tri-layer dielectric gate stack $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ is demonstrated. The electronic characteristics of the polycrystalline La_2O_3 layer and the amorphous SiO_x interfacial layer are imaged and compared. We probed the conduction band of the La_2O_3 layer with a sample bias of +3.5 V (Fig. 4.10) to reveal granular structures of diameter ranging from 10 to 40 nm. By imaging at a -4 V sample bias (Fig. 4.13), we were able to observe the SiO_x interfacial layer. With CITS information, we estimated that localized leakage spots have a planar density of $4 \times 10^{11} \text{ cm}^{-2}$. Knowledge of the

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distribution of high tunneling current regions in each layer, as revealed by STM analysis, can improve our understanding of the leakage performance of high- κ gate dielectric stacks in field-effect transistors. The use of polarity dependent tunneling is extended to study the effect of post-deposition annealing to the leakage current performance of the high- κ gate stack, which is presented in section 4.4.

4.4 Thermal stability of the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack

A reduced β upon PDA has been reported [9]. The reduced β suggests thermally generated extrinsic defects by PDA. As demonstrated in section 4.3, localized leakage sites can be physically identified using the CITS technique. The technique can therefore be used to examine the effect of post-deposition annealing (PDA) on the leakage current performance of high- κ gate stacks. An additional benefit of the CITS technique is its ability to provide decoupled information on the spatial distribution and electrical properties of localized electrical weak spots. We find the main cause of leakage current is either a pure increase in leakage density (as implied by the broadening of current distribution within a scanned area, analysed in section 4.4.1) or a possible structural change (as implied by a change in localized I - V characteristics, analysed in section 4.4.2). The observations can be related to I - V obtained using traditional, macroscopic capacitor structures. Other characterization methods are also used in the PDA study. HR-TEM provides physical profile of the gate stack; XPS provides bonding information; and tof-SIMS provides compositional profile.

4.4.1 PDA effect on electrical uniformity

Fig. 4.14 shows the STM topography image (row I), CITS current map at 2 V (row II) and -2 V (row III) for (a) as-deposited, (b) 300 °C, (c) 500 °C and (d) 700 °C annealed samples.

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Based on the argument established in section 4.3, the CITS current maps at +2 V reflect the electrical quality of the high- κ layer in each sample. Similarly, CITS current maps at -2 V reflect the electrical quality of the interfacial SiO_x layer. Thermally induced increase in leakage density can be readily observed from the CITS data, especially for the 300 °C and 700 °C annealed sample. For quantification purposes, we do the following analysis (see Fig. 4.15 and Fig. 4.16):

1. Obtain a cumulative count of the tunneling current from each pixel of the CITS current map, normalized to the total number of pixels.
2. Normalize the current value (i.e. x-axis) to the current at the 50th percentile (I_0). This procedure minimizes variation in the *absolute* value of the current arising from changes in the tip-to-sample tunnel distance, i.e. the vacuum gap.
3. Leakage spot density is arbitrarily defined as the percentage of pixels with a current value above $1.2I_0$.

The normalized cumulative leakage current distribution at +2 V (row II in Fig. 4.14) and -2 V (row III in Fig. 4.14) are shown in Fig. 4.16a and (b), respectively. The leakage current distribution for the 300 °C and 700 °C annealed samples are more “stretched-out” compared to the leakage current distribution for the as-deposited samples. This suggests an increase in non-uniformity of the electrical properties or sample thickness; effects discussed fully in the following sections. Leakage spot density in the high- κ and interfacial SiO_x layers, based on the definition above, are summarized in Fig. 4.17. It is observed that the low temperature annealed (300 °C) sample has the highest leakage spot density both in the high- κ and the SiO_x interfacial layer, occupying ~ 46 % of the entire scanned area. The 700 °C annealed gate stack has leakage spot area density of 39 % and 32 % in the high- κ and the SiO_x interfacial layer, respectively. The as-deposited and the 500 °C annealed sample exhibit the

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best electrical uniformity, with 30 % and 25 % leakage spot density in the high- κ and the SiO_x interfacial layer, respectively.

Fig. 4.14 CITS data on (a) as deposited gate stack, (b) 300 °C, (c) 500 °C and (d) 700 °C PDA gate stack. The STM control condition (giving the topography of row I) are -4 V, 20 pA. The range of the current is shown for each CITS current image.

Figure 4.15 Method of quantification of leakage spot density. This example is for the CITS current image at +2 V for the as deposited $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack. In subsequent analysis (see Fig. 4.16) the current is normalized to $I_o = 3.3 \times 10^{-4}$ nA

Fig. 4.16 Normalized current distributions of the CITS current map at (a) +2 V and (b) -2 V. CITS is acquired from scan area of 50 nm×50 nm area for the respective gate stacks.

Figure 4.17 Leakage spot density estimated from CITS negative current map (red filled circles) and positive current map (black open circle) as a function of PDA temperature.

The IL (i.e. SiO_x) trap density extracted from the CITS technique can be compared to the interface trap density extracted from conductance measurement [117] on MOS capacitors. C - V characteristics of the four samples at 100 kHz are shown in Fig. 4.18. Large hysteresis is observed for the as-deposited gate stack. Capacitance under accumulation decreases with increasing N₂ PDA temperature. This decrease can be attributed to growth of physical thickness due to IL formation during annealing, which can be evidenced by the thickness measurement done by TEM (refer to Table 3.1). Measurement of frequency dependent capacitance and conductance for the gate stacks subjected to PDA are shown in Fig. 4.19 to Fig. 4.21 for the extraction of the interface trap density (D_{it}). D_{it} extracted from conductance measurement (Fig. 4.22) qualitatively agrees with the CITS observations. The extracted D_{it} of the 500 °C annealed gate stack show the lowest value compared to the 300 °C and 700 °C annealed gate stack. D_{it} of the as-deposited gate stack cannot be found reliably due to large hysteresis. High D_{it} in the 300 °C and 700 °C annealed sample could be one of the possible factors that causes higher leakage current in the MOS capacitor structures, as shown in Fig 4.23. This is due to the fact that energy states can be induced

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within the oxide band gap in the presence of interface traps. As in the STM studies, the MOS stack annealed at 500 °C shows the lowest leakage and best J - V performance. Although the reproducibility of the macroscopic J - V curves of the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack is not as excellent as its SiO_2 counterpart, a general trend can be identified for different annealing conditions. Fig. 4.23 shows the general J - V characteristics of samples with different annealing conditions. Both tunneling (exponential law) and space charge limiting current (SCLC, power law) are observed. This is in agreement with the previous reports [17, 116], where both tunneling and SCLC conduction mechanisms have been adopted to explain the conduction mechanism of the La_2O_3 gate stack. Conduction in the as deposited and 500 °C annealed gate stack are dominated by tunneling whereas conduction in the 300 °C and 700 °C annealed gate stack are dominated by SCLC due to higher density of traps, as evidenced by both STM and C - V analysis. Though a higher leakage current is induced by the electronic traps in the low voltage regime for the 300 °C and 700 °C annealed gate stack, the current becomes self-limiting in the high voltage regime (before breakdown, i.e. the sudden jump in J - V curves in Fig. 4.23) by SCLC mechanism.

Figure 4.18. C - V curve of $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3$ annealed in nitrogen at different temperature. The capacitance reduced with increasing annealing temperature. C - V measurement at $f=100\text{kHz}$. Courtesy of K. Kakushima.

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Fig. 4.19 (a) C_m -V and (b) the corresponding G_m -V of the 300 °C annealed gate stack at different frequency. Courtesy of K. Kakushima.

Fig. 4.20 (a) C_m -V and (b) the corresponding G_m -V of the 500 °C annealed gate stack at different frequency. Courtesy of K. Kakushima.

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Fig. 4.21 (a) C_m - V and (b) the corresponding G_m - V of the 700 °C annealed gate stack at different frequency. Courtesy of K. Kakushima.

Fig. 4.22 Interface trap density D_{it} extracted from conductance measurement. The data point enclosed in the circles are the peak interface trap densities in the respective gate stacks. Courtesy of K. Kakushima.

Fig. 4.23 J - V curve of $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3$ annealed in nitrogen at different temperature. Best leakage performance is achieved after nitrogen annealing at 500°C . Courtesy of K. Kakushima.

4.4.2 PDA effect on localized electrical property

A map of the tunneling current at a given bias may be constructed from the I - V spectra taken at each individual pixel in the CITS technique. Fig. 4.24a shows a typical tunneling current map (at -2.5 V) of the as-deposited gate stack. High local conductivity is reflected as bright shades in the current map. In Fig. 4.24b, the average tunneling currents at locations marked by the circles in Fig. 4.24a are plotted as a function of the applied bias. The solid (or dash-dot) lines in Fig. 4.24a demarcate locations of relatively high (or low) conductivity. Tunneling current is observed in the negative bias regime, but not in the positive bias regime (Fig. 4.24b). The negligible current in the positive bias (tip injection) regime may be ascribed to a much “thicker” effective barrier due to the high- κ layer, as well as a lower electric field across the gate stack due to depletion of the n-Si, as demonstrated in the WKB tunneling probability calculation in section 4.3. The thinner effective barrier of the SiO_x layer yields a greater electron transmission probability under negative bias.

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Fig. 4.25 depicts the tunneling current map (at -2.5 V) and the tunneling current spectra of the 300°C annealed gate stack. Contrary to Fig. 4.24b, a large tunneling current, corresponding to the bright shades marked by the solid lines in Fig. 4.25a, is apparent in the positive bias regime. However, no significant difference between the tunneling spectra taken over bright and normal shades is observed in the negative bias regime. The STM images show a greater density of high-leakage paths in the annealed gate stack. The bright shade density ($\sim 6.4 \times 10^{11} \text{ cm}^{-2}$) of the annealed gate stack is $\sim 5\times$ higher than that of the as-deposited gate stack ($\sim 1.2 \times 10^{11} \text{ cm}^{-2}$). The leakage paths in the annealed sample now exhibits greater tunneling current under positive biasing, despite a lower effective electric field due to n-Si depletion. The result indicates that thermal annealing induces the generation of localized leakage paths having a lower effective barrier to electron transport from the tungsten tip to the substrate, as compared to electron transport from the substrate to the tungsten tip. Similar observations are apparent for the gate stack annealed at 500°C and 700°C (Fig. 4.26 and Fig. 4.27). In contrast to the samples annealed at 300°C and 700°C , the lower conduction regimes of the gate stack annealed at 500°C (Fig. 4.26) show asymmetrical I - V with limited tip injection current. Despite the maintenance of low conductivity at positive bias over much of the surface annealed at 500°C , the leakage remains significant because of the large increase in current flow through the bright regions.

The tunneling current characteristics may be described by an exponential function, i.e. $I_t \sim \exp(\alpha|V_s|)$, where V_s is the applied bias and α is some characteristic constant of the leakage path in the specific bias regime. Clearly, for the annealed gate stack, α in the positive bias regime is much larger than that in the negative bias regime. Owing to the exponential current-voltage dependence, the effective resistance R of the leakage path decreases exponentially with increasing V_s , i.e. $R \sim [\alpha \exp(\alpha|V_s|)]^{-1}$. The decrease in R with respect to V_s is much more significant in the positive bias regime. It has generally been

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agreed that dielectric breakdown is a localized event which arises from the formation of conductive paths in the gate dielectric. These low-resistance paths readily short the gate to the substrate under high voltage stress, inducing catastrophic physical damage to the gate stack. The much lower resistance of the leakage paths may explain why some high- κ gate stacks fail preferentially under high-voltage gate (i.e. tip) injection stress [9].

In summary, scanning tunneling microscopy of the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack presents valuable insights into understanding the impact of thermal annealing on the macroscopic current-voltage characteristics and the charge-to-breakdown Weibull distribution during gate injection. In samples which were subjected to post-deposition anneal, the total increase of leakage current does not merely come from the increase in leakage area, but also from thermally induced localized high-leakage paths exhibiting a much lower effective resistance under tip injection biasing. The result suggests that these low-resistance paths are potential breakdown precursor sites under high-voltage gate injection stressing. The STM results show that low temperature (300 °C) PDA and high temperature (700 °C) PDA will both lead to an increase in leakage density and increased tip injection current at the localized leakage sites. Although the as-deposited sample shows good uniformity and low leakage current at tip injection bias, the large C - V hysteresis observed in the as-deposited film implies a high density of traps which can be charged and discharged during the voltage ramp. PDA at 500 °C appears to be the optimum annealing temperature where the STM data shows good uniformity and limited tip injection current.

Fig. 4.24 As-deposited $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack. (a) I_t map ($12 \text{ nm} \times 12 \text{ nm}$) constructed from the I - V curve obtained at $V_s = -2.5$ V for each pixel in an STM image obtained at -5 V, 20 pA. The brighter (darker) shades correspond to high (low) leakage spots. (b) Average I - V characteristics for the bright (solid line) and normal (dash-dot line) shades marked in (a). The 2 I - V curves are forced to coincide at the set point $V_s = -5$ V and $I_t = 20$ pA. Higher tunneling current at low V_s is evident at regions of brighter shades. Inserts show schematic energy band diagrams of the W tip/vacuum/ $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x/\text{n-Si}$ system under positive and negative bias.

Fig. 4.25 $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack subjected to 300 °C PDA in nitrogen. (a) I_t map ($50 \text{ nm} \times 50 \text{ nm}$) constructed from the I - V curve obtained at $V_s = -2.5$ V for each pixel in an STM image obtained at -4 V, 20 pA. The brighter (darker) shades correspond to high (low) leakage spots. (b) Average I - V of the bright (solid line) and normal (dash-dot line) shades marked in (a). Substantial increase in the tunneling current under tip injection biasing is evident after annealing (compared with Fig. 4.24 (b)).

Fig. 4.26 $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack subjected to 500 °C PDA in nitrogen. (a) I_t map (200 nm $\times$ 200 nm) constructed from the I - V curve obtained at $V_s = -2.5$ V for each pixel in an STM image obtained at -4 V, 20 pA. The brighter (darker) shades correspond to high (low) leakage spots. (b) Average I - V characteristics of the bright (solid line) and normal (dash-dot line) shades marked in (a). I - V at the normal sites remains asymmetrical with limited injection current at +4 V, whereas at bright spots substantial increase in the tunneling current under tip injection biasing is evident.

Fig. 4.27 $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack subjected to 700 °C PDA in nitrogen. (a) I_t map (50 nm $\times$ 50 nm) constructed from the I - V curve obtained at $V_s = -2.5$ V for each pixel in an STM image obtained at -4 V, 20 pA. The brighter (darker) shades correspond to high (low) leakage spots. (b) Average I - V characteristics of the bright (solid line) and normal (dash-dot line) shades marked in (a), showing very large leakage current at the bright shades under tip injection biasing.

4.4.3 PDA effect on film composition

Tof-SIMS and XPS are able to reveal some information on the thermally induced increase in leakage current density and localized leakage current by investigating the compositional profile and bonding information of the PDA samples. However, the exact answer to the atomic scale cause of leakage remained ambiguous due to certain experimental limitations and therefore only plausible reasons are given in light of the SIMS and XPS data.

Tof-SIMS profiles for the elements Sc, La and Si are shown in Fig. 4.28, for the as-deposited and PDA treated gate stacks. Three layers, may be inferred from the tof-SIMS data. The interface between different layers is not abrupt, even for the as-deposited sample (Fig. 4.28a), i.e. there is intermixing of the layers. Profiles of each of the three elements are plotted separately (Fig. 4.29) for better visualization of the influence of PDA temperature on the intermixing of each layer. It can be observed from the Si profile (Fig. 4.29a) that Si diffusion into the La_2O_3 layer region occurs at a temperature as low as 300 °C. Fig. 4.29b shows the La profile and the insert zooms into the region as highlighted by the circle. It is observed that intermixing of La and Sc starts at a PDA temperature of 500 °C and becomes more significant at 700 °C, as evidence by the presence of La at the surface (i.e. depth = 0 nm), showing that La spreads into the entire gate stack after the 700 °C anneal. Concurrently, a small reduction of Sc at the surface can be observed for the 700 °C annealed sample. Recall that the physical thickness of the as-deposited Sc_2O_3 , La_2O_3 and SiO_x layers are 3 nm, 4 nm and 1 nm, respectively. Therefore, the appropriate position of the SiO_x/Si interface as measured by TEM is depth = 8 nm. This is in agreement to the tof-SIMS oxygen profile where the oxygen intensity drops by approximately an order of magnitude at depth ~ 9 nm. After annealing at 500 °C, the Sc_2O_3 layer is no longer

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apparent in the TEM (Fig. 4.30a). After annealing at 700 °C, the amorphous interfacial layer increases in thickness (~ 2 nm) and roughness (Fig. 4.30b). These TEM findings are in qualitative agreement with the SIMS data.

It has been generally found for high- κ films that a rapid silicidation reaction competes with the oxidation process and results in the co-existence of different phases within the high- κ gate stack [118]. Recent studies reported preferential formation of La-silicate materials over the oxide due to a very efficient mechanism for Si diffusion in La metal and/or La oxide [118, 119, 120]. Both silicates and stoichiometric oxide co-exist even in the as-deposited film [120]. Although the presence of Si can be seen in the tof-SIMS data, the chemical bonding needs to be complimented by XPS analysis. In the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack the exact chemical bonding cannot be directly observed from the XPS data due to overlapping of XPS spectrum. Nonetheless, XPS provides some clue to explain the existence of high leakage paths in the 300 °C and 700 °C annealed samples.

In XPS, the Si 2p and La 4d spectra are overlapped; hence deriving the Si bonding structure from the Si 2p spectrum is ambiguous. Similarly, as oxygen can be bonded to Si, La or Sc in different layers of the gate stack (or even within the same layer), the O 1s spectrum is not helpful. The La 3d and Sc 2p spectra, were therefore chosen to provide some clues to the chemical structure of the gate stack.

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Fig. 4.28 Si, La and Sc tof-SIMS profile in (a) as-deposited sample and samples which were subjected to PDA at (b) 300 °C, (c) 500 °C and (d) 700 °C. The interface between layers is not abrupt and inter diffusion of material is apparent, especially after high temperature anneal. The appropriate depth of the SiO_x/Si interface is 8 – 9 nm. Courtesy of C. C. Lee and N. Yakovlev.

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Fig. 4.29 (a) Si profile of the four samples showing significant Si diffusion into the La oxide layer; (b) corresponding La profile. The insert shows a magnified view at the surface (depth = 0). La pile up at the oxide/Si interface beyond 500 °C is observed; (c) corresponding Sc profile. The insert shows a magnified view of the surface (depth = 0). Reduction in Sc intensity occurs at the surface for the 700 °C annealed sample and a concurrent increase of La intensity is observed, signifying interdiffusion between the two layers. The appropriate depth of the SiO_x/Si interface is 8 – 9 nm. Courtesy of C. C. Lee and N. Yakovlev.

Fig. 4.30: TEM micrographs of 500 °C and 700 °C PDA treated $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack. (a) $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack after 500 °C PDA in nitrogen. The Sc_2O_3 layer is no longer apparent due to the intermixing of Sc_2O_3 and La_2O_3 layers as evidenced by tof-SIMS data (Fig. 4.29 (b) and (c)). (b) $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack after 700 °C PDA in nitrogen. Si diffusion into the La_2O_3 region results in significant increase in thickness and roughness of the amorphous interfacial layer. Courtesy of X. Li.

The Sc 2p spectrum is shown in Fig. 4.31a. The Sc oxide layer only interacts with the La oxide layer. The major peak at 403.3 eV in the Sc 2p spectrum for the as-deposited and 300 °C annealed gate stack is the non-stoichiometric Sc oxide phase. A shift of 0.5 eV to lower binding energy 402.8 eV can be observed after the 500 °C and 700 °C anneal, is the formation of stoichiometric Sc_2O_3 . The tof-SIMS data shows the intermixing of La and Sc after the 500 °C and 700 °C anneal which suggests that the formation of LaScO silicate also occurs. Fig. 4.31 (b) shows the La 3d spectrum. The spectrum has distinctive binding energies at 834.5 eV and 839.5 eV for La_2O_3 and at 836.5 eV and 840.5 eV for LaSiO [118]. The presence of –OH bond is evident in the as-deposited and 300 °C PDA gate stacks, as suggested by the shift of the La_2O_3 peak to higher binding energy. The shift of the peak in the as-deposited gate stack is attributed to $\text{La}(\text{OH})_3$, but not LaSiO as there is no Si diffusion in the La oxide as observed from tof-SIMS data. Although the tof-SIMS data

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shows Si diffusion in the La oxide for the 300 °C annealed gate stack, the shift of the peak does not suggest the presence of LaSiO in the La oxide as the shift is not present in the 500 °C annealed gate stack, which has a similar La tof-SIMS profile at the La oxide/Si oxide interface. There is a shift in the lower energy peak from the as-deposited value (836.8 eV) to the 300 °C value (835.3 eV) – this suggests the peak is a mixture of La_2O_3 and $\text{La}(\text{OH})_3$ components. A strong peak is identified at the binding energy of La_2O_3 for the 500 °C annealed gate stack, suggesting the formation of stoichiometric La_2O_3 at this annealing temperature. Annealing at 700 °C moves the major peaks away from the pure La_2O_3 binding energy. The tof-SIMS data shows Sc and Si are abundant in the La oxide layer which again strongly suggests that silicates are formed. E. g. the kink at 840.5 eV suggests the presence of LaSiO silicates.

In summary, based on the data from tof-SIMS and XPS, we suggest the following:

- As deposited gate stack consists of $\text{La}(\text{OH})_3$;
- Gate stack after 300 °C anneal consists of La_2O_3 and $\text{La}(\text{OH})_3$;
- Gate stack after 500 °C anneal consists of La_2O_3 and possibly some La-Sc-O;
- Gate stack after 700 °C anneal consists of La_2O_3 , La-Si-O and possibly some La-Sc-O

Based on the above analysis, electrical weak spots, as observed from CITS, could arise from defects at the imperfect interface between different phases. The co-existence of different phases is significant in the 300 °C and 700 °C annealed gate stacks, which have demonstrated high density of leakage current and high localized tip injection current. The presence of –OH bonding does not lead to high leakage current and leakage current density in the as-deposited gate stack. This could be explained by electron trapping at the positively charged defect states during substrate injection, as evident by the large hysteresis in the C - V characteristics of the as-deposited gate stack (Fig. 4.18). When the sample bias is ramped

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towards positive voltage (tip injection), the electron does not have sufficient energy to surmount the SiO_x barrier and detrapp from the defect state. Tip injection current therefore remains insignificant.

Fig. 4.31 XPS for the as-deposited and PDA samples for the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack. (a) Sc 2p spectra. (b) La 3d spectra. Binding energies for stoichiometric La_2O_3 and LaSiO from the reported literature [118] are shown for reference. (vertical lines). Courtesy of S. J. Wang.

4.5 Localized I - V characteristics

In the previous two sections, localized leakage paths are observed to be present in the gate stack. Localized leakage implies the presence of electronic traps. Based on the polarity dependence of the tunneling current, it is possible to demarcate the electronic traps in the high- κ and IL. In this section, observation using CITS of two distinct localized leakage characteristics in the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack is reported. Possible explanations for these leakage characteristics are also proposed, namely barrier height lowering and trap-assisted tunneling. These leakage characteristics have also been observed by Seko *et al.* in the $\text{Al}_2\text{O}_3/\text{La}_2\text{O}_3$ composite using conductive atomic force microscopy in ambient [121]. However, due to the problem of anodic oxidation, only substrate injection was possible in Seko's experiment.

Fig. 4.32a depicts a set of CITS data showing: (I) topography image at 20 pA and -4 V sample bias, (II) current map at a low negative sample bias (-2.3 V), (III) current map at low positive sample bias ($+2.3$ V) and, (IV) current map at a high positive sample bias ($+4$ V). Contrast of the current images is adjusted such that pixels having leakage current (at the specified sample bias) in the top fifth percentile of the current distribution (as measured over the entire image) are shown uniformly bright. The purpose of the contrast adjustment is to identify the most leaky locations within the scanned area. Different current maps are observed at different biases, signifying the presence of distinct localized leakage paths.

First, we observe that some bright spots occur at all positive voltages (Fig. 4.32a (III) and (IV)). These are categorized as type A leakage sites. The I - V curve extracted from a typical type A leakage site (Fig. 4.33a, filled circle) shows a near-parallel shift towards lower voltages, as compared to the reference curve (Fig. 4.33a, open rectangle). Note that in Fig. 4.33, we plot the average current per pixel area as a function of the sample bias. The I - V curves depicted are therefore independent of the effective area of the leakage site. The

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reference I - V curve is an average for all pixels in the entire image area excluding leakage sites.

Next, some bright spots are observed at a low positive sample bias (Fig. 4.32a (III)) but they do not show up as bright in the current map at high positive sample bias (Fig. 4.32a (IV)). These are named as type B leakage sites. The I - V characteristic of type B leakage is similar to that of stress induced leakage current (SILC), i.e. a larger current, as compared to the reference curve, is observed at a low sample bias [122].

As the sample bias is increased, the current value approaches and merges with that of the reference I - V curve (Fig. 4.33a, solid line). Similar behavior is observed at negative bias. The corresponding locations are named as type C leakage (Fig. 4.33a, closed triangle). Type C leakages are only observed at a low negative sample bias (Fig. 4.32a (II)).

Leakage sites are also seen whose I - V curves are shifted parallel (with respect to the reference curve) towards lower voltage under a negative sample bias; these are named as type D leakage sites. However, they cannot be identified in the CITS data of Fig. 4.32a since the STM feedback control was set at -4 V, 20 pA. Hence, the current map at -4 V should show uniform contrast because an increase in current at a type D leakage site is compensated by the STM feedback changing the tip-sample distance to maintain a constant tunneling current. To reveal the existence of type D leakage sites, CITS is acquired with STM feedback set at $+3.5$ V, 20 pA, as shown in Fig. 4.32b for the same area as that depicted in Fig. 4.32a. Columns II, III and I - V in Fig. 4.32b show the current maps at -3.5 , -2 and $+2$ V respectively. Type D leakage sites can now be observed in Fig. 4.32b (II and III) and the corresponding I - V curve is shown in Fig. 4.33b (filled circle). In Fig. 4.32b (I - V), type B leakage can also be observed at the same position as in Fig. 4.32a (III), although some of them appear to have recovered during the second CITS measurement. A similar observation applies to the type C leakage site (compare Fig. 4.32a (II) and Fig. 4.32b (III)),

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where the solid line shows reproducible type C leakage and the dotted line shows recovered type C leakage). The I - V curves of type B and C leakage sites are shown in Fig. 4.33b (solid line and filled triangle respectively). Type A leakage cannot be observed in Fig. 4.32b at +3.5 V STM feedback due to the same reason that type D leakage cannot be observed in the CITS data of Fig. 4.32a at -4 V STM feedback.

Fig 4.32: (a) CITS measurement data with STM feedback control set at -4 V, 20 pA. The data shows the topography image (I) and tunnel current (I_t) at (II) -2.3 V, (III) $+2.3$ V and (IV) $+4$ V. Type A leakage sites appear as bright shades in both (III) and (IV). Type B leakage sites only appear as bright shades in (III) and cannot be seen in (IV). Type C leakage sites only appear in (II). Type D leakage sites cannot be identified under the negative polarity STM control conditions. Type T sites (IV, dash dot circle) show high leakage current and also lower topography, and could therefore arise from a locally thinner film.

(b) CITS measurement of the same area as in (a), but with the STM feedback control set at $+3.5$ V, 20 pA. The data shows the topography image (I) and I_t at (II) -3.5 V, (III) -2 V and (IV) $+2$ V. In this case, type A leakage sites cannot be identified. Type B leakage sites appear as bright shades in (IV). Type C leakage sites appear as bright shades in (III) but not in (II). Type D leakage sites appear as bright shades in both (II) and (III). Type T sites (IV, dash dot circle) show high leakage current and also lower

Fig 4.33: I - V characteristics of the different types of leakage sites. Also shown are the reference curves, which are the averaged I - V curves for the image area, excluding the leakage sites. CITS measurement was carried out at a feedback set point of (a) -4 V, 20 pA and (b) $+3.5$ V, 20 pA.

The near-parallel shift in the I - V curve of type A (or D) leakage site in the positive (or negative) sample bias regime implies that the tunneling mechanism at these leakage sites remains the same as that of the trap-free location but the tunneling barrier height is lowered. It should be noted that more leakage current will also flow if the local film thickness is decreased. Such regions show up as bright spots in the current map with corresponding dark (i.e. thinner) spots in the CCI. These are labeled as type T in Fig. 4.32 and are not considered further because from the STM data alone the leakage could be due to either a thinner film or barrier height lowering. The type A (or D) leakage is not a consequence of a locally thinner film and is therefore electronic in nature. STM tunneling probability at different sample biases is calculated for the three-barrier system based on the WKB approximation, as described in Section 4.3. Fig. 4.34a shows the calculated tunneling current as a function of positive sample bias, for different cathode (i.e. high- κ layer) barrier heights. When the barrier height is decreased, a parallel shift in the tunneling probability

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curve towards lower voltage is evident (Fig. 4.34a). A similar observation is applicable for the tunneling probability at negative sample bias (Fig. 4.34b). Hence, the near-parallel shift in the I - V curves of type A and D leakage may be ascribed to a lowering of electron tunneling barrier at these locations.

The similarity between the I - V characteristics of type B and C leakage sites and those of SILC implies that tunneling via trap states localized in a certain energy interval in the dielectric bandgap is responsible for the observed increased leakage [122]. Since type B leakage sites are reflected in the tip injection current, the associated trap states are located in the high- κ layer. Trap states responsible for the type C leakage sites are located in the interfacial SiO_x layer. Increased tunneling leakage arises only when the applied voltage causes the Fermi level of the emitting electrode to align with the trap states. For instance, under a positive sample bias (tip injection), increased tunneling leakage occurs when the tip Fermi level is aligned with trap states in the high- κ bandgap at a specific bias. The I - V curve will merge back to the reference curve once the tip Fermi level moves away from the trapped state energies. A more detail modeling of the SILC leakage will be presented in Chapter 5 based on further observations during the reliability study of this high- κ gate stack.

In conclusion, we have shown that two different types of localized leakage (A, D) and (B, C) sites exist in the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack. It is proposed that type A and D leakage sites are due to lowering of the conduction band minimum of the high- κ and interfacial SiO_x layer respectively. Type B and C leakage sites are due to trap-assisted-tunneling through the high- κ and interfacial SiO_x layer respectively.

Fig. 4.34 calculated tunneling current as a function of positive sample bias, for different cathode barrier heights. When the barrier height is decreased (from the ideal barrier height, at an interval of 0.5 eV), a parallel shift in the tunneling probability curve towards lower voltage is evident (a) modeling of tunneling current at type A leakage site by lowering of high- κ layer's energy barrier; (b) modeling of tunneling current at type D leakage site by lowering of IL SiO_x 's energy barrier.

4.6 Summary

In summary, we show that the STM provides a valuable tool in studying localized leakage in the advanced high- κ gate stack and we presented the first STM data obtained on the new high- κ materials La_2O_3 [129]. Demarcation of high- κ and IL traps can be obtained based on polarity dependent STM current. Application of the CITS technique in the study of PDA effect on the high- κ gate stack reveals both formation of localized low resistance path and increase in non-uniformity upon annealing. The localized low resistance path and the increase electrical non-uniformity give rise to the increase leakage in macroscopic I - V measured on MOS capacitor structures. XPS and tof-SIMS data suggest that localized leakage could be due to the defects at the interface of different phases which co-exist in the

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film. The formation of low resistance path in the high- κ layer provides a physical explanation for the polarity dependent Weibull slope, where the high- κ gate stack is found to be more susceptible to breakdown under gate injection stress. Two distinct I - V characteristics are observed for the leakage current at the low resistance path, where higher leakage current could be attributed to an early onset of Fowler-Nordheim tunneling (barrier height lowering) or trap-assisted-tunneling.

Chapter 5 WEAR-OUT PROCESS IN THE HIGH- κ GATE STACK

5.1 Introduction

The mandatory switch to the high- κ /SiO_x gate stack in order to continue the scaling of CMOS presents significant challenges not only to process integration but also to the reliability of the nanoscale transistor. As compared to the SiO₂ gate oxide, which has more than four decades of history, the reliability knowledge base of the newer high- κ /SiO_x gate stack is very limited.

Electronic traps have been identified to play a crucial role in the wear-out/breakdown process of thin gate oxides. During the wear-out phase of the SiO₂ gate dielectric, traps were generated inside the oxide [123] and at the oxide interfaces [124] by the voltage applied across the oxides and/or the current flowing through the oxide [125]. The density of these traps would eventually become high enough to result in a locally high current density, which triggers thermal runaway in the localized region [126].

Most of the reported study on the reliability of high- κ gate stack has not reach a consensus. For instance, IL was identified as the “weakest link” of the high- κ gate

stack, irrespective of stress polarity [182]. On the other hand, polarity dependent trap generation in the high- κ or in the IL has also been reported [5]. The dissenting views could be attributed to the inherently high density of non-stoichiometric defects in the high- κ material and the SiO_x IL, which could mask the intrinsic trap evolution due to area-averaging in traditional MOS capacitor tests. Physical understanding at the nanometer scale is therefore important. Furthermore, as an interfacial SiO_x layer is unavoidable, or even favorable for some transistor characteristics (for instance, mobility), it is therefore interesting to find out how the traps in one layer influence the wear-out process of another layer.

In Chapter 4, we have shown that STM can reveal localized electronic traps in the individual layers of the high- κ gate stack. Post deposition annealing induced large amount of electronic traps in the high- κ gate stack. The density of thermally induced weak spots (leakage paths) is $\sim 4.6 \times 10^{13} \text{ cm}^{-2}$ and $4.7 \times 10^{13} \text{ cm}^{-2}$ in the high- κ and IL, respectively. With such a high area density, the role of these as-processed electronic traps on the subsequent reliability under electrical stress cannot be neglected. The objective of this chapter is therefore to exploit the capability established in Chapter 4 to study the evolution of electronic traps in each layer under electrical stress either in a trap-free area or in an area with as-processed electronic traps.

We show that; (i) in the absence of as-processed electronic traps, the high- κ layer is more susceptible to electrical stress induced wear-out. This observation is discussed in the context of current trap generation models and is shown to be best explained by anode hot-hole effects induced by inherently lower surface plasmon threshold energy at the metal/high- κ interface and a higher hole trapping rate in the relatively thick high- κ layer. The result is presented in section 5.3. (ii) as opposed to the uncorrelated breakdown in the ultrathin SiO_2 gate oxide [127], pre-existing traps are observed to

have a crucial influence on trap generation in the bi-layer high- κ gate stack. Depending on the electrical characteristics of the as-processed traps (SILC or barrier height lowering), electrical induced wear-out can either be inhibited or accelerated. Three major observations on the influence of as-processed electronic traps are discussed in section 5.4. An inelastic trap-assisted tunneling model is adopted for explaining the experimental observations. The model further reveals the energy distribution of the SILC trap and the energy loss of the hot electrons due to inelastic tunneling. Based on the experimental observations, different possible stages of breakdown evolution in the high- κ gate stack are proposed in section 5.5.

5.2 Experiments

The electrical property of a leakage site is characterized by its local I - V curve acquired during the CITS scan, where the sample bias (V_s) is ramped from -4 V to $+4$ V and the corresponding tunneling current (I_t) is collected. Demarcation of local electronic traps with different I - V characteristics in the high- κ or IL can be found (see section 4.5). Electrical stress was applied by extending the I - V measurement to higher voltages. Two types of electrical stress were studied, i.e. substrate injection stress (by extending I - V to higher negative V_s) and tip injection stress (by extending I - V to higher positive V_s).

The samples used in this study were $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stacks annealed at different temperatures in nitrogen. Sample preparation has been described in section 3.3. The study on intrinsic trap generation was carried out on $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stacks annealed at 500 °C (section 5.3) due to its good electrical uniformity (see section 4.4). As for the study on the role of as-processed traps on electrical stress

induced trap evolution, $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stacks annealed at 300 °C was chosen (section 5.4) due to the high density of as-processed traps.

5.3 Intrinsic trap generation by anode hole injection

A major concern in incorporating high- κ material into CMOS transistors is the limited knowledge on the intrinsic reliability of the high- κ gate stack. Owing to thermal instability, structural defects are formed in the high- κ gate stack during fabrication [6]. Several authors [9, 94, 95] had shown, via scanning probe techniques, the presence of localized leakage paths in the high- κ gate stack after thermal annealing. As a consequence, the time-to-breakdown of large-area MOS capacitors is often predominated by preexisting traps [9], as is evident from a reduced β [31]. In this section, we investigate electrical stress induced trap generation in a $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack with PDA at 500° C in nitrogen. Depth profiling by high-resolution Rutherford backscattering spectroscopy (HRBS) showed minimal diffusion of La after annealing [128]. Using the high spatial resolution of the STM enables regions of the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack of good thickness and electrical uniformity (i.e. negligible preexisting traps) to be identified for intrinsic wear-out study.

Fig. 5.1a (I) shows the z map (i.e. the topography during CCI) of a $50 \times 50 \text{ nm}^2$ area. The respective current maps at $V_s = -2.3, +2.3$ and $+4 \text{ V}$ are shown in Fig. 5.1a (II, III and IV). A uniform image is apparent in all cases, indicating excellent thickness and electrical uniformity of the scanned area. The solid line in Fig. 5.2 depicts the average I - V curve of the scanned area. Significant increase in current for $V_s < -2 \text{ V}$ may be ascribed to direct tunneling through the ultra-thin SiO_x layer (insert (i)). The current in the positive bias regime is negligibly small, due to the much thicker high- κ layer (and hence a much larger tunneling barrier) (insert (ii)). This observation also implies that the high- κ layer has negligible

preexisting traps. Since the presence of traps in the vicinity of the injecting electrode exert the greatest change to the tunneling probability [110], the locations of stress induced traps in the high- κ layer and in the vicinity of the SiO_x layer may be distinguished via mapping of the tunneling current under substrate injection (negative V_s) and tip injection (positive V_s) biasing respectively [129].

The effect of a trap on the electron tunneling probability at the injecting electrode decreases with its distance from the electrode [110]. Although the influence on one interface is reduced, influence of a trap deeper in the dielectric on the tunneling probability at the opposite electrode would correspondingly increase. Thus, differences in stress induced trap generation in the high- κ and SiO_x may be assessed through the relative difference in the increase of stress induced leakage current under substrate- (negative V_s) and tip-injection (positive V_s) biasing [129], respectively.

Fig. 5.1b shows the z map and the associated current (I_t) maps of a second consecutive scan of the same area. The contrast of the current maps has been adjusted such that only locations having current values in the top 5% of the distribution appear bright. The purpose is to locate the “worst-case” stress generated traps. The negative current map (Fig. 5.1b (II)) remains uniform, indicating negligible trap generation in the SiO_x layer after the first scan. On the other hand, localized bright spots are observed in the positive current maps (Fig. 5.1b (III and IV)), signifying occurrence of trap generation in the high- κ layer. It should be highlighted that there are no bright spots in Fig. 5.1a (III and IV) during the first scan and Fig. 5.1b (II) during the second scan. However, bright shades are observed in Fig. 5.1b (III) at a relatively small positive V_s . From these observations, we infer that trap generation in the high- κ happened during the -4 to 0 V sweep, i.e. substrate electron injection, of the second scan. For $V_s < -2$ V, electrons from the n-Si conduction band directly tunnel through the ultrathin SiO_x and enter the high- κ conduction band (insert (i); Fig. 5.2). Due to a lower high- κ conduction

band edge as compared to SiO_x , these electrons appear “hot” and they thermalize through electron-lattice interaction in the high- κ bulk and/or at the tip/high- κ interface, resulting in trap generation. As will be shown later, a much larger relative increase of I_t under tip injection bias indicates that most of the traps are located close to the tip/high- κ interface, implying that an interface-related trap generation mechanism dominates over a bulk mechanism. The open circles in Fig. 5.2 depict a typical local I - V curve taken at the bright spots in Fig. 5.1b (III and IV). Onset of tunneling leakage at a much lower positive V_s indicates significant lowering of the tip/high- κ interface barrier, confirming that substantial generation of traps has occurred in the high- κ layer during the -4 to 0 V sweep of the second scan.

After the fifth consecutive scan over the same area, bright spots can be observed in both the negative (Fig. 5.1c (II)) and positive (Fig. 5.1c (III and IV)) current maps. The presence of bright spots in the negative current map implies that trap generation has also occurred in the vicinity of the SiO_x layer.

Fig. 5.3a shows the statistical distribution of the tunneling current (normalized to the average current of the 1st scan) at $V_s = -2.3$ V, of each scan. The corresponding current distribution at $V_s = +4$ V is shown in Fig. 5.3b. As compared to the negative current distribution (Fig. 5.3a), a more significant increase in the positive tunneling current is observed. These results imply that the high- κ layer is more susceptible to electrical stress induced wear-out as compared to the SiO_x layer. Moreover, a much larger spread in the positive current distribution after stress suggests that trap generation without pre-existing traps is a random process. To estimate the rate of trap generation in the two layers, we plot in Fig. 5.3b the percentage P of the scanned area having leakage current greater than a predetermined threshold (arbitrarily defined to be the 95th percentile of the current distribution of the second scan) as a function of the scan time T . The slope of the P vs. time plot yields an estimate for the trap generation

rate. The initial trap generation rate in the high- κ layer is ~ 0.8 %/min (before IL SiO_x traps are generated), about 40 times that in the IL SiO_x layer (~ 0.02 %/min). The subsequent lowering of trap generation rate in the high- κ layer, upon trap generation in the IL SiO_x layer, to 0.3 %/min will be addressed later. These results indicate: (i) high- κ is more susceptible to electrical stress induced wear-out as compared to SiO_x and (ii) most of the traps generated in the high- κ are close to the tip/high- κ interface.

Fig. 5.1 CITS data of a 500 °C PDA Sc₂O₃/La₂O₃/SiO_x gate stack. Column (I) depicts the topography (z) maps of a 50 x 50 nm² area obtained at a constant tunneling current of 20 pA; the bias voltage was -4 V. Bright (dark) shades correspond either to local increase (decrease) in gate stack thickness or conductance (due to electronic structure variation). Column (II), (III) and (IV) depict the respective current maps (I_t) at bias voltage -2.3 , $+2.3$ and $+4$ V. Row (a), (b) and (c) denote the z and current maps of the selected area after the first, second and fifth scan. The relatively uniform z and current maps in row (a) imply excellent thickness and electrical uniformity of the selected area. The contrast of the current maps in row (b) and (c) is adjusted such that only locations exhibiting leakage current above the 95th percentile of the current distribution of the scanned area appear bright. This is to locate the “worst-case” trap generation regions, i.e. the leakiest spots in the gate stack.

Fig. 5.2 Solid line denotes the average tunneling current (I_t) versus sample bias voltage (V_s) characteristic of the $50 \times 50 \text{ nm}^2$ scanned area. The open circles denote a typical I - V_s characteristic of the bright spots observed in the positive current maps (Fig. 1 (b-III) and (b-IV)) during the second scan. Significant increase in tunneling current is observed in the positive bias regime only. Insets: Energy band diagrams of the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack under (i) negative and (ii) positive biasing. For all measurement, the bias voltage was applied to the substrate contact; negative (positive) biasing thus corresponds to substrate (tip) electron injection.

Fig. 5.3 Statistical distribution of the tunneling current of the $50 \times 50 \text{ nm}^2$ area for bias voltage (a) $V_s = -2.3$ V and (b) $V_s = +4$ V. The current is normalized to the average current of the 1st scan. A substantial increase in the average current at $V_s = +4$ V implies significant trap generation in the high- κ layer. The increased spread further indicates non-uniform trap generation. On the other hand, a relatively small increase in current for $V_s = -2.3$ V shows much smaller trap generation rate in the SiO_x layer. (c) Percentage P of the scanned area exhibiting tunneling current greater than a predefined current threshold. The filled (open) squares denote results obtained under negative (positive) biasing, which probes trap generation in the SiO_x (high- κ) layer. The slope of the plot provides an estimate for the average trap generation rate. The current threshold is defined as the 95th percentile of the respective tunneling current distribution for $V_s = -2.3$ V and $+4$ V after the second scan.

Currently, there are two schools of thought on the physics behind trap generation in the gate dielectric. The first is commonly known as the “thermochemical model”, which attributes trap generation to bond breakage caused by thermal and local electric field induced perturbation. By the Lorentz relation [37], the local electric field in a dielectric is given as

$$E_{\text{loc}} = ((2 + \epsilon) / 3)E \quad (5-1)$$

where E is applied field and ϵ is dielectric constant. The Lorentz relation indicates that high- κ has an intrinsically higher E_{loc} , and hence a smaller enthalpy of activation for bond

breakage [37], as compared to SiO_2 . However, in a high- κ/SiO_x stack, the ratio of applied field across the high- κ ($E_{\text{H}\kappa}$) to that across the IL SiO_x (E_{IL}) is

$$E_{\text{H}\kappa} / E_{\text{IL}} = \epsilon_{\text{IL}} / \epsilon_{\text{H}\kappa} \quad (5-2)$$

Hence,

$$E_{\text{loc,H}\kappa} / E_{\text{loc,IL}} = \epsilon_{\text{IL}}(2 + \epsilon_{\text{H}\kappa}) / (\epsilon_{\text{H}\kappa}(2 + \epsilon_{\text{IL}})) \sim 1 \quad (5-3)$$

The local field in the high- κ and SiO_x are therefore comparable. Hence, the thermochemical model cannot satisfactorily explain the difference in the trap generation rate in the high- κ and SiO_x .

The key driving forces behind the second school of thought are electron energy and current. It is proposed that energetic electrons arriving at the anode release hydrogen species [130] and/or induce hot holes [131] which are transported back towards the cathode, resulting in positive charge and neutral trap generation. Owing to an asymmetrical energy band structure, I_t is intrinsically higher in the negative V_s regime, i.e. substrate injection bias (Fig. 5.2). This, however, does not completely account for a higher trap generation rate in the high- κ . As shown in Fig. 5.3a, trap generation in SiO_x is not increased despite a significant increase in the average I_t during subsequent tip injection bias (Fig. 5.3b).

Some authors explained greater trap generation in high- κ in terms of the hydrogen release mechanism, by presuming a higher hydrogen concentration at the metal/high- κ interface as compared to the SiO_x/Si interface [132]. It is speculated that the density of hydrogen traps at the metal/high- κ interface is higher due to material difference [132], but dissenting view exists [33]. In our case, hydrogen depth profiling via HRBS [128] revealed similar hydrogen concentration at the SiO_x/Si interface and the high- κ surface of the 500 °C annealed sample (Fig. 20 of ref. 128). This observation does not support the view that greater trap generation in the high- κ is a consequence of the hydrogen release mechanism.

A larger anode hot-hole injection coefficient (α_h) at the tip/high- κ interface, as compared to the SiO_2/Si interface, however, provides a plausible explanation for the higher trap generation rate in high- κ . The probability for defect generation at a given interface is related to α_h , which may be expressed as the product $P_h \theta_h$. P_h is the probability for generating a hole by a hot electron arriving at the anode interface. θ_h is the probability for a hot-hole to tunnel back to the cathode. Impact ionization [133] and surface plasmon deexcitation [134, 135] have been identified as the main mechanisms generating electron hole pairs (EHP) in the bulk or at the surface, respectively. Due to Coulomb screening in the metal and Si, generation of hot holes via impact ionization in the anode has a relatively low efficiency [136]. On the other hand, it is more likely for hot electrons to induce surface plasmons while they are still unscreened at the anode interface. Generation of hot holes by the decay of surface plasmons at a metal surface has been evidenced experimentally and the fact that the plasmon is generated at the metal surface increases the probability that the hole gets back injected into the oxide even though the life time of a hole in metal is in the femto second regime [136]. Fig 5.4 illustrates the process of EHP generation by emission and decay of surface plasmons. Firstly, electrons accelerate and gain energy while traveling from the cathode to the anode (1 in Fig. 5.4). A significant fraction of the energetic electrons lose energy at the anode/oxide surface by emitting surface plasmons (2 in Fig. 5.4). Surface plasmons decay and EHP are excited (3 in Fig. 5.4). A fraction of EHP recombine and emit as photons whereas the holes for the remaining EHP get reinjected back towards the cathode (while electrons get injected to the anode) and are trapped in the oxide (4 in Fig. 5.4). The threshold energy $\hbar\omega_p$ for surface plasmon excitation at a SiO_2/Si interface has been consistently observed at about 7.5 eV by Electron Energy Loss Spectrum (EELS) [134]; $\hbar\omega_p$ at the W surface is predicted to be 3 eV [137] and further supported by the localized

light emission spectra in STM [138, 139] or scanning tunneling optical spectroscopy (STOM) [140], where a peak at a wavelength of 500nm (corresponds to 2.5 eV) is attributed to the contribution from the STM W tip. This implies that for the range of voltage considered in this study, the surface plasmon effect is negligible at the SiO_x/Si interface while it is relatively significant at the metal/high- κ interface.

Fig. 5.4 Illustration of EHP generation by surface plasmon emission. (1) Electrons accelerate and gain energy while traveling from the cathode to the anode. (2) A significant fraction of the energetic electrons lose energy at the anode/oxide surface by emitting surface plasmons. (3) Surface plasmons decay and EHP are excited. (4) A fraction of EHP recombine and emit as photons whereas the holes for the remaining EHP get reinjected back towards the cathode and are trapped in the oxide.

Studies on light emission from STM/STOM suggest that the plasmon decays radiatively into a photon with a quantum efficiency of $10^{-6} \sim 10^{-4}$ photon/electron [138, 141]. While a portion of the generated EHPs recombines and emit as photons, hot holes that do not recombine get injected back towards the cathode. In Fig. 5.5, θ_h at the metal/high- κ and SiO_x/Si interfaces are compared as a function of applied bias. Hole energy barriers are estimated from the reported band gap values of La_2O_3 and SiO_2 [6]. The overall hole tunneling probability through the dielectric stack was calculated as the product of the tunneling probabilities through the individual layers (Fig. 4.5),

assuming ballistic transport (valid for ultra-thin dielectrics). The larger θ_h at the SiO₂/Si interface at low bias regime, however, cannot compete with the exponentially decaying surface plasmon generation rate below the threshold energy (ω_{sp}) of 9 eV for SiO₂/Si interface. In addition, the actual number of energetic electrons reaching SiO₂/Si interface (during tip injection, i.e. positive V_s) is about three orders lower as compared to electrons entering the metal/high- κ interface (during substrate injection, i.e. negative V_s) before stress (solid line in Fig 5.2). This further reduces the number of surface plasmon, hence the number of hot hole, at the SiO₂/Si interface, leading to an overall smaller α_h even though θ_h is larger. It should be emphasized that θ_h is calculated based on the assumption that the hole tunnels through the entire gate stack reaching the cathode. Trap generation by hot-hole injection occurs when the back-injected holes are trapped in the dielectric. In the case where the hot hole is trapped within the dielectric, we should expect a much higher tunneling probability at low bias regime at the metal/high- κ interface due to a smaller hole energy barrier. An intrinsically greater anode hot-hole effect at the metal/high- κ interface thus explains why high- κ (being next to the anode) is more susceptible to wear-out during substrate injection stress.

It is observed that the trap generation rate reduces from 0.8 %/min to 0.3 %/min after the third scan, when IL SILC starts to populate the stressed area (Fig. 5.3c). Fig. 5.6a shows an overlay of leakage sites exhibiting SILC characteristic (dark shades, attributed to traps in the IL) and leakage sites exhibiting *barrier height lowering* characteristic (bright shades, attributed to traps near the high- κ surface) after the fifth scan. A general mismatch between the two features is evidenced. I - V curves extracted from the locations without IL traps (bright shades in Fig. 5.6a) shows barrier height lowering characteristics in the high- κ (i.e. with positive I_t parallel shifted to a lower voltage, closed circle in Fig. 5.6b). On the other hand, barrier height lowering in the high- κ is less significant in the presence of IL SILC

traps (Fig. 5.6b, open circle, extracted from dark shades in Fig. 5.6a). This implies that the presence of IL SILC traps at a given location suppresses trap generation in the high- κ at the same location. The following sections provide further experimental evidence on the spatial mismatch of leakage paths in the high- κ and the IL and a proposed mechanism for the apparent suppression of trap generation at a location where traps exhibiting SILC characteristic already exist.

In summary, electronic trap generation in the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate dielectric stack under RVS during CITS is investigated via STM. It is shown that in an optimized gate stack of negligible preexisting traps, trap generation in the high- κ still proceeds at a much higher rate as compared to that in the SiO_x . The observation may be consistently ascribed to a greater anode hot-hole effect at the metal/high- κ interface as compared to that at the SiO_x/Si interface. The finding has serious implication on the reliability of metal-gate/high- κ stacks.

Fig. 5.5 Hole tunneling probability from the SiO_x/Si and metal/high- κ interface as a function of sample bias voltage.

Fig. 5.6 Superposition of the CITS images at -2.3 V (Fig. 5.1 (c II)) and $+4$ V (Fig. 5.1 (c IV)). The white (or black) shade corresponds to localized high-leakage sites (top fifth percentile) in the high- κ (or IL) layer. The “leakiest” spots in the two layers generally do not coincide. (b) I - V extracted at a bright shade in the -2.3 V CITS image (i.e. at a location with electronic traps in the IL) (open square) as compared to the I - V at a position without traps in the IL layer (filled square). A parallel shift of the positive I to a lower voltage is evidenced at the location with IL trans.

5.4 Role of “pre-existing” traps on subsequent trap generation

In section 5.3, we examined intrinsic wear-out of the high- κ gate stack. After trap generation has occurred at a given location in a given layer, the immediate question would be how these traps would affect subsequent trap generation at the same location. A more detailed understanding of the underlying mechanisms of trap evolution and the mutual role and interaction of the two dielectric layers is thus crucial to advancing a physical model for high- κ gate stack breakdown. However, conventional electrical analysis on MOSCAP structures is likely to mask out important information due to area-averaging. In this section, we examine the role of localized electronic traps in the IL on the evolution of trap generation in the high- κ and vice versa by applying electrical stress locally on the individual traps. We outline three key observations leading to an improved phenomenological model showing how breakdown can be triggered by pre-existing or electrically induced electronic traps. The three scenarios

discussed below are observed for both the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ and the $\text{HfO}_2/\text{SiO}_x$ gate stack, but for clarity only the results for $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ are presented.

5.4.1 Substrate injection stress

As shown in section 5.3, electrons thermalize at the anode resulting in trap generation primarily in the dielectric layer nearest to the anode. In this section, substrate injection stress is applied to generate electronic traps in the high- κ . Substrate injection stress is implemented by extending the I - V to higher negative voltage during CITS acquisition. The effect of as-processed electronic traps with different characteristics (SILC or barrier height lowering) and locations (in the high- κ or IL) on trap generation in high- κ by substrate injection stress is studied. Three scenarios are laid out and discussed as below.

Scenario I: Suppression of trap generation in the anode layer in the presence of cathode SILC traps

Fig. 5.7 shows the CITS of an area of $50 \text{ nm} \times 50 \text{ nm}$ (a) before and (b) upon substrate injection stress. Substrate injection stress was done by extending I - V measurement to $V_s = -5 \text{ V}$. I_t map at -2 V delineates the regions of thermal induced SILC (i.e. the as-processed electronic traps exhibiting SILC, abbreviated as tSILC in subsequent discussion) located in the IL. During high voltage stress, electronic traps are expected to be generated in the layer near the anode (i.e. the high- κ layer) due to hot electron thermalization [5]. However, it is noticed that the generation of traps in the high- κ is not a completely random process in the presence of pre-existing traps in the IL. It can be observed from the I_t map that, with the presence of IL tSILC traps (dotted circles in

the I_t map at -2 V of Fig. 5.7a), there are no new traps generated in the high- κ layer (dotted circles in the I_t map at $+4$ V of Fig. 5. 6b at the corresponding locations). Conversely, new traps in the high- κ layer are preferentially generated at locations without IL SILC traps (solid circles in the I_t map at (a) -2 V and (b) $+4$ V of (b) of Fig. 5.7). Dash-dotted circles highlight the evidence for scenario III, which will be discussed later. For better visualization, the I_t map at $+4$ V of row (a) is subtracted from that of row (b) to delineate locations with significant increase in I_t (which implies new traps generated) at $+4$ V (Fig. 5.8a). Fig. 5.8a is overlapped with the I_t map at -2 V of Fig. 5.7a, which signifies IL tSILC traps, and the superimposed image is shown in Fig. 5.8b. In Fig. 5.8b, the dark shades show increase in I_t at $+4$ V (corresponding to the bright shades in Fig. 5.8a) and the bright shades show tSILC IL traps (corresponding to the bright shades in the I_t map at -2 V of Fig. 5.7a). The bright and dark shades in Fig. 5.8b are found to be spatially mismatched. This gives further evidence to the argument that IL SILC traps can inhibit further trap generation in the high- κ layer at the same location, as presented in section 5.3 (Fig. 5.6). In fact, both thermally and electrically induced SILC traps show the tendency of suppressing trap generation in the anode.

Fig. 5.7 CITS of an area of $50 \text{ nm} \times 50 \text{ nm}$ at -4 V , 20 pA from the 300°C PDA $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack, (a) before and (b) upon substrate injection stress. In the presence of IL tSILC traps (dotted circles in the I_t map at -2 V of row (a)), there is no new traps generated in the high- κ layer (dotted circles in the I_t map at $+4 \text{ V}$ of row (b)) at the corresponding locations. New traps in the high- κ layer are preferentially generated at locations without IL SILC traps (solid circles in the I_t map at -2 V of row (a) and I_t map at $+4 \text{ V}$ of row (b)). Dash-dotted circles give evidence for scenario III, which will be discussed later.

Fig. 5.8 (a) Difference of I_t at $+4 \text{ V}$ before and after substrate injection stress. Bright shades show locations with relatively significant increase in I_t . (b) Superposition of (a) with the I_t map at -2 V of Fig 5.7 (a). Location which exhibit increase in positive I_t (signifying new trap generation in the high- κ) are spatially different from the locations with pre-existing tSILC IL traps.

Fig. 5.9 shows I - V curves extracted from four different features, i.e. a combination of presence/absence of IL tSILC traps with the presence/absence of pre-existing leakage due to high- κ barrier height lowering. The positive x-axis shows I - V extracted from locations with pre-existing high- κ leakage due to barrier height lowering. Positive y-axis shows I - V from locations exhibiting IL SILC characteristics before substrate injection stress. In the first and second quadrant, the I - V at positive bias is comparable before and after substrate injection stress in the presence of IL SILC traps. Even with pre-existing high- κ leakage (first quadrant), the pre-existing leakage does not show further degradation. New traps generated in the high- κ , leading to barrier height lowering of the high- κ layer, in the absence of IL SICL traps can be evidenced in the third quadrant, with the positive I - V shifted to a lower voltage after substrate injection stress. Further degradation of the pre-existing high- κ leakage is shown in the forth quadrant, where there is no SILC traps in the IL.

Fig. 5.9 I - V curves describing scenario I.

In scenario I, the spatial mismatch between the IL SILC traps and the increase in leakage current due to trap generation in the high- κ is observed. This observation implies tunneling through trap assisted tunneling via IL SILC traps could suppress further trap generation in the high- κ . Observation of scenario I therefore suggests an energy loss of the tunneling hot electrons at the SILC traps, resulting in “cooler” electrons at the anode [55, 142, 143]. A trap-assisted tunneling (TAT) model which includes relaxation [56] (i.e. inelastic TAT model, or iTAT) is thus adopted for the explanation of scenario I. For simplification, the multi-barrier high- κ /SiO_x/Si system, together with the vacuum barrier of the STM experiment, is modeled as a single barrier system. Fig. 5.10 shows the I - V curve averaged from trap free locations. This I - V is fitted to a direct tunneling (DT) current equation, as shown in equation 5-4 [111] and 5-5 [144],

$$TP(E, t_{eff}, E_{ox}) = \text{Exp}\left[-\frac{4\sqrt{2m_{ins}}}{3\hbar q E_{ox}}\{E^{3/2} - (E - qE_{ox}t_{eff})^{3/2}\}\right] \quad (5-4)$$

$$J(\phi_{eff}, t_{eff}, E_{ox}) = \frac{n_v m_d K_B T}{2\pi^2 \hbar^3} \int_0^\infty TP(\phi_{eff} + E, t_{eff}, E_{ox}) \text{Ln}(1 + \exp(\frac{E_{ox}t_{eff} - E}{K_B T})) dE \quad (5-5)$$

Where TP is the tunneling probability of an electron through a trapezoidal barrier, J is the total direct tunneling current by Ezaki-Tsu model, E is the electron energy barrier with respect to the Fermi level of the cathode, E_{ox} is the electric field of the oxide barrier, ϕ_{eff} is the effective electron tunnel barrier, t_{eff} is the effective barrier thickness, m_{ins} is the tunneling mass in the insulator, n_v is the valley degeneracy in the cathode and m_d is the density-of-state mass in the cathode. The constant in equation 5-5 involves several parameters with uncertain values. For example, various value has been reported for m_{ins} in SiO₂. In addition, exact area involves in tunneling is not

known (although an estimation of ~ 20 nm is made for W tip curvature). The constant in equation 5-5 is therefore normalized to the STM feedback set point current for fitting purpose. The same rule applies for the subsequent fitting for iTAT model.

The effective barrier height (ϕ_{eff}) and thickness (t_{eff}) of the single barrier model are determined as 5 eV and 3.8 nm, respectively. The effective mass m_{ins} in the single barrier model is found to be $0.26m_0$. These values are extracted by fitting the trap-free I_t to DT model. Without the presence of electronic traps, the multi-layer system can be equate to a single barrier with 5 eV barrier height and 3.8 nm thickness. A ϕ_{eff} of 5 eV is comparable to the largest electron energy barrier (the Fermi level of the W tip to vacuum, ~ 4.5 eV) and a t_{eff} of 3.8 nm is in agreement with the equivalent oxide thickness (SiO_2) thickness of the multi-barrier system, i.e.

$$t_{\text{eff}} \approx \frac{t_1}{\frac{\kappa_1}{\kappa_4}} + \frac{t_2}{\frac{\kappa_2}{\kappa_4}} + t_3 = \frac{0.5}{1} + \frac{3}{7} + 1 = 3.45(\text{nm}) \text{ (where } n = 1 \text{ to } 3 \text{ corresponds to the}$$

respective layers as shown in Fig. 4.5)

Fig. 5.10: Fitting of DT model (insert) to “trap free” I - V data.

The equivalent single barrier model can then be inserted into the iTAT model, which is graphically described in Fig. 5.11. Electrons tunnel from the cathode through the barrier and are trapped by the electronic traps. Upon capturing an electron, the energy level of the traps responsible for the TAT tunneling change by a value of E_{relax} . It is assumed that there is no elastic out-tunneling from the trap to the anode in this model. No energy loss can be observed if there is conventional elastic out-tunneling from the trap to the anode as the elastic out-tunneling current will dominate the total current due to a shorter trapping time as compared to the energy relaxation time. The possible mechanism for energy relaxation will be discussed later. Subsequently after the energy relaxation, the electron is emitted from the trap (with relaxed energy) to the anode.

Fig. 5.11: Inelastic trap-assisted tunneling model.

The total iTAT current can be formulated by incorporating an energy relaxation model into the conventional trap-assisted tunneling model. In the conventional TAT model (equation 5-6 and 5-7), tunnel-in current (J_{in}) from the cathode to the trap and the tunnel-out current (J_{out}) have to balance through the concentration (N_t), occupancy (ρ) and physical location (z) of the trap for maximum probability of occurrence of the

iTAT mechanism. As the substrate bias we applied during STM experiment is smaller than the energy barrier height of the DT model, we therefore only consider the direct tunnel current (equation 5-5).

Assuming the traps are located at a longitudinal distance z from the cathode, J_{in} and J_{out} can be expressed by the following equations:

$$J_{in}(z, E_{ox}) = \sigma N_t(z, E_{ox})(1 - \rho(z, E_{ox}))J(\phi_{eff}, z, E_{ox}) \quad (5-6)$$

$$J_{out}(z, E_{ox}) = \sigma N_t(z, E_{ox})\rho(z, E_{ox})J(\phi_{eff}', t_{eff} - z, E_{ox}) \quad (5-7)$$

Energy relaxation is taken into consideration by the term ϕ_{eff} in the J_{out} expression (equation 5-7), where

$$\phi_{eff}' = \phi_{eff} - zE_{ox} + qE_{relax} \quad (5-8)$$

Maximum tunneling probability occurs at $J_{in} = J_{out}$, hence

$$\rho(z, E_{ox}) = \frac{J(\phi_{eff}, z, E_{ox})J(\phi_{eff}', t_{eff} - z, E_{ox})}{J(\phi_{eff}, z, E_{ox}) + J(\phi_{eff}', t_{eff} - z, E_{ox})} \quad (5-9)$$

and the tunneling current via the traps located at z , $J_{tat}(z, E_{ox})$, is

$$J_{tat}(z, E_{ox}) = \sigma N_t(z, E_{ox}) \frac{J(\phi_{eff}, z, E_{ox})J(\phi_{eff}', t_{eff} - z, E_{ox})}{J(\phi_{eff}, z, E_{ox}) + J(\phi_{eff}', t_{eff} - z, E_{ox})} \quad (5-10)$$

The total tunneling current (J_{tot}) is calculated by integrating J_{tat} with respect to z , thereby including all possible physical locations of traps in the longitudinal direction.

$$J_{tot}(E_{ox}) = \int_0^{t_{eff}} J_{tat}(z, E_{ox}) dz \quad (5-11)$$

In Fig. 5.12, we fit an I - V curve extracted from SILC trap sites to the iTAT formulation. The trap-free I - V is fitted to the DT model and is shown for comparison.

Fig. 5.13 shows that an I - V with SILC traps can also be fitted to a DT model but results in an unphysical value for the effective barrier (i.e. $\phi_{\text{eff}} = 10$ eV).

Fig. 5.12 The dotted-line shows the calculated tunneling current by the iTAT mechanism. Enhanced low voltage current and almost self-limiting high voltage current of the experimental measured I - V from locations with IL SILC traps (open square) can be well modeled by the iTAT mechanism. I - V extracted from trap free location (closed square) can be fitted to the direct tunneling model at low bias with an effective barrier height of 5 eV (solid line).

Fig. 5.13 Experimental I - V from SILC trap sites (open square) fitted to an inelastic trap-assisted tunneling model (dashed-dot line) and direct tunneling model (dashed line). Fitting to the direct tunneling model results in an unphysical effective barrier height of 10 eV.

The calculated iTAT current fits well to the experimental I - V extracted from leakage sites which exhibit the SILC characteristic (both thermally and electrically induced high- κ and IL SILC traps). Therefore, leakage current at the locations with SILC traps can be explained by an inelastic trap-assisted tunneling mechanism. The presence of E_{relax} implies a decrease in electron energy at the anode by losing energy during the tunneling process. Lower trap generation probability is thus expected at the anode due to thermalization of the “cooler” electrons. This explains why the presence of SILC traps could delay wear-out, and thus increase the reliability margin of the high- κ gate stack.

From the iTAT model, the energy profile of SILC traps can be estimated and the amount of energy loss through inelastic tunneling is extracted. As shown in equation 5-10, the total iTAT current depends proportionally on the trap density N_t . For better accuracy in extracting the value of E_{relax} , knowledge of the energy distribution of N_t is necessary. Furthermore, N_t provides information on how traps distribute with respect to electron energy. An expression for the total current J_{tot} [55], which reduces the integration and excludes the unknown E_{relax} , is discussed below and allows N_t to be estimated. Using

$$\rho_{\text{max}}(z, E_{\text{ox}}) = \frac{J(\phi_{\text{eff}}, z, E_{\text{ox}})J(\phi_{\text{eff}}', t_{\text{eff}} - z, E_{\text{ox}})}{J(\phi_{\text{eff}}, z, E_{\text{ox}}) + J(\phi_{\text{eff}}', t_{\text{eff}} - z, E_{\text{ox}})} = \frac{1}{2}J(\phi_{\text{eff}}, z, E_{\text{ox}}) \quad (5-12)$$

With J given by equation 5-5. Substituting equation 5-12 into equation 5-10, gives,

$$J_{\text{tot}}(E_{\text{ox}}) \approx \frac{t_t \sigma N_t(z_t, z_t E_{\text{ox}})}{2} J(\phi_{\text{eff}}, z_t, E_{\text{ox}}) \quad (5-13)$$

where t_t is defined as

$$t_t = \frac{J_{\text{tot}}}{J_{\text{tat}}(z_t)} \quad (5-14)$$

and z_t is the electrical “location” of the trap which results in the maximum J_{tat} , as illustrated by Fig. 5.14. The validity of the approximation is verified in Fig. 5.15, where z_t is shown to be relatively independent on the applied bias.

Hence, N_t can be calculated by comparing the experimental I - V curve to the approximated J_{tot} (equation 5-15), with t_t and σ taken as constants. In our case, $t_t \sim 0.46$ nm (Fig. 5.14) and σ is typically in the range of 10^{-14} to 10^{-16} cm² [42, 43] for HfO₂ gate stacks.

$$J_{\text{tot}}(E_{\text{ox}}) \approx \frac{t_t \sigma N_t(z_t, z_t E_{\text{ox}})}{2} J(\phi_{\text{eff}}, z_t, E_{\text{ox}}) = J_{\text{experiment}}(E_{\text{ox}}) \quad (5-15)$$

$$t_t \sigma N_t(z_t, z_t E_{\text{ox}}) = \frac{2 J_{\text{experiment}}(E_{\text{ox}})}{J(\phi_{\text{eff}}, z_t, E_{\text{ox}})} \quad (5-16)$$

$t_t \sigma N_t$ may be interpreted as the percentage volume of the dielectric occupied by traps.

Fig. 5.14: J_{tat} with respect to distance from the cathode (z). Maximum J_{tat} occurs at z_t .

Fig. 5.15: z_t at different applied voltage V_s . z_t is found to be relatively independent of V_s .

Trap location within the equivalent single barrier model is always assumed to be at the *electrical* center of the barrier, which results in the highest tunneling probability in the inelastic trap-assisted tunneling model. The *electrical* center does not

necessarily correspond to the *physical* center in the dielectric layer. This is especially true in our case where the band alignment of multi-layer dielectric is asymmetrical. As already established in the literature [110] and shown in Chapter 4, tunneling current is most sensitive to the barrier of the injecting interface. We therefore determine the trap location (either in the high- κ layer or in the IL) by whether the SILC characteristic occurs at positive V_s (tip injection, traps located in high- κ) or negative V_s (substrate injection, traps located in the IL). Irrespective of the physical location of the trap, the assumption that the trap is at the *electrical* center of the single barrier model still holds as long as $J_{in} = J_{out}$, giving the largest tunneling probability. The single barrier model with ϕ_{eff} and t_{eff} has been shown to be representative of the gate stack with multiple barriers in Fig. 5.10. In addition, sensitivity of tunneling current to trap location has been investigated in chapter 4. Based on these two understandings, building the iTAT model on the single barrier equivalent system provides sufficient description of the role of electronic traps in the ideal gate stack (i.e. trap free). This simplification allows us to omit complicated equations using parameters from individual layers. In fact, a multi-layer model could be less practical, bearing in mind that the interfaces between adjacent layers are not abrupt (as evidenced by tof-SIMS).

Traps with SILC characteristics, in the IL or high- κ layer, can be generated thermally by PDA or electrically under an externally applied electric field. To calculate N_t of the SILC traps, $J_{experiment}(E_{ox})$ is taken from the I - V extracted from CITS at locations exhibiting SILC characteristic. For example, Fig. 5.16 shows CITS data of a 300 °C annealed sample before any applied electrical stress. Leakage sites due to SILC traps in the high- κ layer are depicted by the dotted circles labeled B. Leakage sites due to SILC traps in the IL are depicted by dash-dot circles labeled as C. Leakage sites labeled as A exhibit characteristics of barrier height lowering. All these

leakage sites are induced thermally during the PDA process at 300°C. Thermally induced leakage sites exhibiting SILC characteristic are abbreviated as tSILC.

Fig. 5.16: First CITS scan of a fresh area of a 300°C annealed $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack. (a) Topography at -4 V, 20 pA; (b) corresponding I_t map at -2 V, (c) $+2$ V, and (d) $+4$ V. Thermally induced leakage sites with type A, B and C characteristics (as defined in section 4.5) are observed in this first CITS scan. i.e. no electrical stressing has yet occurred over this scanned area.

The I - V characteristics of leakage sites labeled B (i.e. SILC traps in the high- κ layer) are extracted from the different CITS I_t maps (Note: other areas of the surface are also scanned in addition to Fig. 5.16 and this CITS data is also processed to enable general conclusions to be reached). Fig. 5.17a shows a typical logarithmic plot of N_t extracted using equation 5-16 and the experimental I - V data from one of the leakage sites. The resulting exponential traps distribution could be responsible for the space charge limited current (SCLC) observed in some La based high- κ gate stack transistors [17]. It could also be the origin of the observed conduction band tail in ballistic electron emission microscopy (BEEM)[147].

I - V data in the negative V_s regime is used in equation 5-16 to calculate the N_t of tSILC traps in the IL. It is observed that N_t of IL tSILC traps varies from site to site. Two main distributions are observed, as depicted in Fig. 5.17b. Filled squares in Fig. 5.17b show N_t with an exponential energy distribution, which is similar to the case of high- κ tSILC traps. Open squares show N_t with a completely different distribution,

suggesting IL tSILC traps of a different nature. This second type of IL tSILC traps shows an approximate Gaussian distribution with respect to electron energy with a peak at an energy state deeper into the bandgap. The difference between high- κ and IL tSILC traps could arise from the fact that the IL is a non-stoichiometric SiO_x layer. Various types of defects could co-exist in the IL, resulting in the observed variation of trap energy distributions.

Fig. 5.17: N_t distribution with respect to energy of (a) thermally induced SILC traps located in high- κ layer (b) thermally induced SILC traps located in IL layer (c) electrically induced SILC traps in high- κ layer and (d) electrically induced SILC traps in IL layer. The Fermi level (E_f) of the tip/substrate is taken as the reference level. The conduction band minima (CBM) is at electron energy = 5 eV, i.e. the extracted effective barrier height at a *trap free* location. The distribution maximum is normalized to 1 for all data sets.

In addition to thermally induced traps, electrically induced traps are also observed after electrical stress is applied to the scanned area. Electrical stress induced SILC traps are abbreviated as eSILC in the subsequent discussion.

I - V curves from different sites of high- κ and IL eSILC are extracted from the CITS data for the calculation of their respective N_t . The N_t of high- κ eSILC has an exponential energy distribution, similar to the high- κ tSILC traps, as shown in Fig. 5.17c. The N_t of eSILC traps in the IL differs significantly from the IL tSILC traps. Fig. 5.17d shows the typical N_t extracted from most leakage sites with eSILC traps in the IL. It has a Gaussian distribution at low energy with the peak located at a deeper energy level in the bandgap (~ 1.5 eV) compared to that of the IL tSILC traps (~ 2.5 eV).

With the knowledge of N_t , we are able to estimate the value of energy loss (E_{relax}) due to resonance tunneling for the respective SILC traps. The degree of energy relaxation may be an important parameter in determining the reliability of a layer, and hence the gate stack. N_t calculated from I - V curves can be substituted into the exact expression of the inelastic tunneling current J_{tot} in equation 5-10 and 5-11 to extract E_{relax} .

A defect can contribute to leakage current only when E_{relax} is smaller than the defect energy level (E_t , with respect to the Fermi energy E_f of the anode). If E_{relax} is larger than E_t , there will be no available unoccupied state at the anode for the electron which has escaped from E_t after energy relaxation because the electron energy is below E_f . An electron tunnels from the cathode to the defect states when the Fermi level of the cathode lies at or above the defect energy state. Once the defect state is charged with an electron, the defect changes its structure because it can lower the energy of the electron by deforming or reconstructing the lattice. This results in a

downward shift of the defect level (which is now charged with an electron). The time to relax the structure is assumed to be shorter than the residence time of the electron on the defect states. The trap-assisted tunneling therefore is an inelastic process and the excess energy, which equals the shift of the energy level between the charged and uncharged state, can be lost in the form of heat [148].

Given that $E_{\text{relax}} \cong 0.9 \pm 0.3$ eV, approximately a quarter of the electron energy is relaxed via the SILC traps. The electrons become “cooler” when they arrive at the anode, hence reducing trap generation probability in the dielectric layer next to the anode (Scenario I). Nevertheless, E_{relax} can still be released as heat, which leads to the observation of Scenario II.

Scenario II: Evolution of SILC traps into a percolation path

Whilst delaying the formation of percolation path throughout the entire gate stack by “hampering” trap generation in the layer next to the anode (i.e. scenario I), SILC traps in both layers of the gate stack are observed to develop into a leakage path showing barrier height lowering upon further electrical stress. The observation is depicted in Fig. 5.18. Pre-existing high- κ SILC traps are depicted as bright shades in Fig. 5.18a. Fig. 5.18b shows an increase of tunneling current at a relatively high voltage (+4 V) upon substrate injection stress. The I - V curve of these leakage sites is shifted to a lower voltage after substrate injection stress. The electrical signature implies barrier height lowering induced by a possible structural change, for instance, formation of percolation path. Fig. 5.18c is the superposition of (a) and (b). The overlap of bright shades in (a) and (b) appear as the brightest shades (in red) in (c).

Fig. 5.19 shows I - V curves extracted from a bright shade in Fig. 5.18c (i.e. the overlap of bright shades in Figs. 5.18a and 5.18b). The I - V curve at a bright shade in

Fig 5.18a (at the same location as that in Fig. 5.18c) is also shown for comparison. The I - V suggests the presence of SILC traps in the IL before substrate injection stress (SILC characteristic appears also in the negative V_s regime), in addition to SILC traps in the high- κ . As described in scenario I, the presence of IL SILC traps are supposed to hamper further degradation of the corresponding high- κ layer. However, degradation of the SILC traps into a leakage site with lowered barrier height is evidenced in scenario II (Fig. 5.18 and 5.19), which *cannot* be attributed to electron thermalization. This is because reduced electron energy is expected in the anode (high- κ) when SILC traps are present in the cathode (IL). Thermalization of the “cooler” electrons would therefore reduce the trap generation probability in the anode. A possible mechanism arises because, as mentioned above, tunneling via SILC traps has been shown to be an inelastic event. Energy loss during iTAT is possibly caused by the defect energy shift due to lattice deformation upon capturing an electron. At the same time, lattice distortion at the location with SILC traps could accelerate the wear-out of the neighboring region. In addition, electron energy loss accompanying the downward shift of the defect energy when it is charged by an electron could be transformed into heat. Therefore, evolution of SILC traps in the high- κ into a percolation path of lowered barrier height due to enhanced trap generation rate at neighboring regions of the SILC traps is possible.

Scenario II is independent of stress polarity. As long as there is resonant tunneling via SILC traps, evolution of the traps within the same layer can be observed both at the anode (as discussed above, Fig. 5.18 and 5.19) and the cathode (Fig. 5.20 and 5.21). Bright shades in Figs. 5.20a and 5.20b depict pre-existing IL SILC traps and high- κ SILC traps, respectively. Fig. 5.20c shows the next CITS image over the same area. An increase of leakage current due to lowering of the IL barrier height is observed at

the location with pre-existing IL SILC traps (note: the CITS does not extend to high V_s during I - V acquisition and is limited to 3.5 V). This is supported by the change of I - V curve at negative voltages from the SILC characteristics (Fig. 5.21c, closed rectangle, enhanced leakage current only occurs at low voltage) to barrier height lowering characteristics (Fig. 5.21c, open rectangle, parallel shift of the I - V curve to lower voltage as compared to the reference I - V). For clearer visualization, Figs. 5.20a and 5.20c are overlaid and shown in Fig. 5.21a. The overlap of IL SILC traps with generated IL leakage due to barrier height lowering gives further evidence that SILC traps will subsequently evolve into a full percolation path within the IL. This may cause possible structural modification of the IL, hence a lowering barrier height of the IL.

As also observed in Fig. 5.21a, not all generated leakage is due to the evolution of SILC traps (see regions enclosed by solid circles in Figs. 5.21a and 5.21b; they do not overlap with the bright shades which depict IL SILC traps). These leakage sites come from hot electron thermalization at the IL (the anode) in the absence of the corresponding high- κ SILC traps during tip injection stress, i.e. scenario I. The mismatch between increased current in the IL (bright) with pre-existing high- κ SILC traps (dark) is apparent, as shown in Fig. 5.21b.

Fig.5.18: CITS images of the 300 °C PDA $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack with STM feedback setting -4 V, 20 pA. Scenario II: (a) Bright shades due to pre-existing high- κ SILC traps, obtained by subtracting the I_t map at $+4$ V from the corresponding I_t map at $+2$ V (this highlights leakage sites which show up only at low positive voltage, but not at high voltage, i.e. the SILC characteristic) (b) Bright shades show increase of current at $+4$ V upon substrate injection stress, obtained by subtracting the I_t map at $+4$ V before stressing from that after stressing. (c) Superposition of (a) and (b). The brighter shades correspond to overlapping of bright shades in (a) with bright shades in (b).

Fig. 5.19: I - V extracted from the brighter shades in Fig. 5.18 (c), showing that SILC traps in the high- κ evolve into a leakage path of lowered barrier height (I - V curve shifted parallel towards lower V_s) within the high- κ , even in the presence of IL SILC traps which are supposed to suppress trap generation in the high- κ . The reference curve is averaged from the entire scan area, excluding the leakage sites.

Fig. 5.20: CITS images of the 300 °C PDA $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack taken with STM feedback setting at + 3.5 V, 20 pA. (a) I_t map showing pre-existing IL SILC traps. The image is obtained by subtracting the I_t map at -3.5 V from the I_t map at -2 V to highlight leakage sites exhibiting enhanced I_t only at low voltage. (b) Pre-existing high- κ SILC traps, i.e. the I_t map at $+2$ V. (c) Stress induced leakage sites exhibiting barrier height lowering (in the IL), obtained by subtracting the I_t map at -3.5 V of the first CITS scan from that of the second CITS scan.

Fig. 5.21: (a) Superposition of Fig. 5.20 (a) and (c). The brighter shades show the overlap of IL SILC traps with subsequent increase in leakage due to barrier height lowering of the IL, i.e. scenario II. (b) Superposition of Fig. 5.20 (b) and (c). Mismatch between the shaded regions is generally observed, except at the brighter shades observed in (a). Stress induced leakage sites in the IL due to hot electron thermalization are enclosed by the same circles in (a) and (b) (scenario I). (c) I - V extracted from the brighter shades in (a), where pre-existing SILC traps exist in both the high- κ and the IL. SILC traps in the IL evolve into a percolation path within the layer when stressed in the subsequent CITS image. Evolution of SILC traps into a percolation path within the layer is more significant in the IL, probably due to a physically thinner IL (as compared to the high- κ layer), hence less trap generation is needed to form a percolation path in the IL.

Scenario III: Enhanced generation in the cathode in the presence of an anode percolation path

During substrate injection stress, electronic traps are expected to be generated in the high- κ layer due to hot electron thermalization at the anode. However, trap generation at the IL can be observed during substrate injection stress (dash-dotted circle in Fig. 5.7b). Further investigation into trap generation in the IL during substrate injection stress shows that IL trap generation is not random but occurs preferentially at pre-existing high- κ leakage sites which exhibit barrier height lowering characteristics. The electric field across the IL is enhanced at the position where a percolation path (i.e. low resistance path [145, 146]) is formed in the high- κ and this phenomenon is scenario III.

Experimental evidence for scenario III is shown in Fig. 5.22. Fig. 5.22a shows the CITS I_t map at +4 V before substrate injection stress. Bright shades signify leakage sites exhibiting barrier height lowering characteristics. The voltage was then extended to -5 V for substrate injection stressing during the next CITS image over the same area. To observe leakages generated in the IL, the I_t map at -4 V before stressing (which registers a uniform current of 20 pA over the entire area because the STM feedback is at -4 V, 20 pA) is subtracted from the I_t map at -4 V after stressing. The I_t image at -4 V deviates from 20 pA if any traps are generated because the I - V during the CITS starts at -5 V. Fig. 5.22b is superimposed on Fig. 5.22a for comparison and the resultant image is shown in Fig. 5.22c. It is observed that most of the substrate injection stress induced leakage sites in the IL occur at locations where leakage sites pre-exist in the high- κ , as shown by the brighter shades in Fig. 5.22c. However, some of the stress induced IL traps do not coincide with the pre-existing high- κ traps, as highlighted in the circle in Fig. 5.22b. This exceptional case in Scenario III can be

explained by the mechanism of Scenario II, where leakage in the IL can evolve from IL SILC traps. Evidence for this interpretation is shown in Fig. 5.23. Fig. 5.23a is reproduced from Fig. 5.22b and Fig. 5.23b shows the region of SILC traps in the IL before substrate injection stress (this data is an I_t map at -2 V before stress). It is seen that generated IL traps which do not coincide with high- κ traps coincide with the IL SILC traps (for example, those highlighted by the circle in Fig. 5.22b and Fig. 5.23a).

I - V curves showing these observations are shown in Fig. 5.24. In Fig. 5.24a, traps are generated in the IL (open square, parallel shift of I - V to a lower voltage) at the location with pre-existing high- κ traps, which exhibit barrier height lowering characteristics (filled square, increase in current at positive V_s). In Fig. 5.24b, no pre-existing trap occurs in the high- κ but IL SILC traps exist before stress, as evidenced by the absence of current increase at positive V_s and enhanced current at small negative V_s (filled square). A subsequent I - V extracted from the same feature after stressing shows an increase in leakage at all negative voltages (open square), suggesting leakage in the IL with barrier height lowering characteristics resulting from the pre-existing IL SILC traps (scenario II).

Scenario III can be explained by a local enhancement of electric field in the IL where a low resistance path pre-exists in the high- κ layer. An electrostatic simulation (using QuickField) of the IL electric field is shown in Fig. 5.25. The low resistance path in the high- κ layer is modeled as a reduced thickness but shown schematically as a percolation path in Fig. 5.25a. A bias of 4 V is applied at the substrate. The potential drop across the IL is greatly enhanced in the presence of the low resistance path in the high- κ (Fig. 5.25b, closed symbols), as compared to the location without electronic traps in the high- κ (Fig. 5.25b, open symbols).

Fig. 5.22: CITS data of the 300 °C PDA $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack with STM feedback setting -4 V, 20 pA. Scenario III: (a) I_t map at $+4$ V. Bright shades signify leakage sites exhibiting barrier height lowering characteristic in the high- κ layer. (b) Difference between the I_t maps at -4 V before and upon substrate injection stress. Bright shades signify generated IL leakage sites with barrier height lowering characteristic. The bright shades enclosed by the circle evolve from IL SILC traps, as described under scenario II. (c) Superposition of (a) and (b), showing most stress induced IL traps are located at pre-existing high- κ leaky sites exhibiting barrier height lowering characteristic. Due to the reduced resistance, the local electric field across the IL is increased. The corresponding I - V characteristics are shown in Fig. 5.24 (a).

Fig. 5.23: The special case (the circled region in Fig. 5.22 (b)) showing the co-existence of scenario II and III: (a) Data of Fig. 5.22 (b). The leakage sites occur at pre-existing high- κ leakage sites showing barrier height lowering characteristic, except for the leakage sites enclosed by the circle. The leakage sites enclosed by the circle coincide with pre-existing IL SILC traps as shown in (b). The corresponding I - V curves are shown in Fig. 5.24 (b).

Fig. 5.24 (a) I - V curves extracted from bright shades in the overlaid image in Fig. 5.22 (c). (b) I - V curves extracted from the bright shades circled in Fig. 5.22 (b), showing the evolution of SILC traps into a complete percolation path and induced barrier height lowering.

Fig. 5.25: Electric field simulation for Scenario III. (a) Enhanced electric field across the IL is observed in the presence of a pre-existing percolation path in the high- κ layer. The lines show positions of equipotential. The low resistant percolation path is modeled as a reduced physical thickness in the high- κ layer. (b) Potential with respect to distance from the Si/SiO_x interface. There is an increased potential drop in the IL, hence enhanced electric field, in the presence of the low resistance path in the high- κ . The SiO_x/high- κ interface occurs at distance = 1 nm.

5.4.2 Tip injection stress

The three scenarios described above can also be observed during tip injection stress. In this case, the SiO_x IL is next to the anode and the high- κ layer is next to the cathode.

Scenario I: Suppression of trap generation in the anode layer in the presence of cathode SILC traps

During tip injection, hot electrons thermalize in the cathode, generating defects in the dielectric layer next to the anode, i.e. the IL. Similar to Scenario I for substrate injection stress (section 5.4.1), high- κ SILC traps are found to suppress trap generation in the IL, as shown in Fig. 5.26. The bright regions resulting from an increase in leakage current at negative V_s (i.e. due to stress induced IL electronic traps), exhibiting either SILC (Fig. 5.26a) or barrier height lowering (Fig. 5.26b) characteristic, do not match the positions of pre-existing high- κ SILC traps (Fig. 5.26c). The superposition image of (a), (b) and (c) is shown in Fig. 5.22d.

Fig. 5.27a shows an I - V curve extracted at a location without high- κ SILC before tip injection stress is applied (filled square). Subsequent stress generates new traps in the IL which exhibit SILC characteristic (open square, enhanced current at low negative V_s). In the presence of SILC traps in the high- κ layer, we notice that it is less likely to generate IL traps at the corresponding locations, as evidenced by the I - V curves of Fig. 5.27b extracted from a location with high- κ SILC traps before (filled square) and after (open square) tip injection stress. SILC traps are present in the high- κ layer before stress as suggested by the enhanced current at low $+V_s$, yet no further degradation of the I - V curve at negative V_s is noticed after stress. At the same time, we observe that SILC traps in the high- κ layer evolve into a complete leakage path

with increased leakage current observed at positive V_s . This will be elaborated under scenario II.

Fig.5.26: Scenario I during tip injection stress. CITS results for 30 nm $\times$ 30 nm area from the 300 °C PDA $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack obtained under a feedback setting of -4 V, 20 pA. (a) Stress induced IL traps exhibiting SILC characteristic (bright shades). The image was obtained by subtracting the I_t map at -2 V before stress from that after stress. (b) Stress induced IL leakage sites with the barrier height lowering characteristic implied by the increase of the tip-sample control separation due to increased conductivity. The image was obtained by subtracting the CCI image before stress from that after stress. (c) Pre-existing high- κ SILC traps. The image was obtained by subtracting the I_t map at $+4$ V from the I_t map at $+2$ V; bright shades depict location with leakage at low $+V_s$ but not at high $+V_s$. (d) Superimposed image of (a), (b) and (c). Dark shades signify locations with pre-existing high- κ SILC traps (as in (c)), bright shades signify stress induced leakage sites (superposition of (a) and (b)). A mismatch of bright and dark shades can be observed.

Fig. 5.27: I - V characteristics extracted from locations with (a) and without (b) high- κ SILC traps. Traps in the IL are preferentially generated at locations without high- κ SILC traps.

Scenario II: Evolution of SILC traps into a percolation path

While traps are expected to be generated at the IL (i.e. the layer next to the anode) during tip injection stress, wear-out of the high- κ layer (the layer closest to the cathode) can be observed. Two mechanisms on how wear-out can occur in high- κ under tip injection stress are discussed in scenarios II and III.

As already shown under scenario I, tunneling via the SILC traps is an inelastic process which involves energy transfer to the lattice through electron trapping at the defect induced energy states within the dielectric bandgap. Therefore, defects are expected to further evolve in the vicinity of pre-existing SILC traps, as evidenced in Fig. 5.28. Bright shades in Figs. 5.28a and 5.28b delineate high- κ SILC traps observed in the first CITS scan and high- κ leakage sites showing barrier height lowering characteristic in the subsequent CITS scan, respectively. As shown in (c), bright shades in (b) are found to coincide with those in (a) (shown as brighter shades in (c)), except for those enclosed by the circles. The overlap of bright shades suggests leakage sites in (b) evolve from SILC traps in (a). That is, it suggests the evolution of SILC

traps into a percolation path in the high- κ (e.g. due to possible structural change of the high- κ) showing barrier height lowering characteristic. Fig. 5.28d shows I - V curves extracted from locations with pre-existing high- κ SILC traps that evolve into a percolation path in the high- κ layer.

The exceptional case observed in scenario II, as demarcated in Figs. 5.28b and 5.28c by the circles, falls into scenario III, which will be explained in the next section.

Fig. 5.28: CITS data from the 300 °C PDA $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack with STM feedback setting at -4 V, 20 pa. Scenario II during tip injection stress: (a) Bright shades show locations with pre-existing high- κ SILC traps. The image was obtained by subtracting the I_t map at $+4$ V from the I_t map at $+2$ V (to highlight leakage sites occur at low $+V_s$ but not at high $+V_s$) during the first CITS. (b) Increase of leakage current at $+4$ V observed as a second CITS scan was performed over the same area. The image was obtained by subtracting the I_t map at $+4$ V of the first CITS from that of the second CITS. (c) Superposition of (a) and (b). Brighter shades correspond to the overlap of features in (a) with features in (b). The bright shades follow the contour of bright shades in (b), signifying that the stress induced leakage sites in the high- κ during tip injection stress evolve from the pre-existing high- κ SILC traps. (d) I - V extracted from locations where high- κ SILC traps evolve into a percolation path exhibiting barrier height lowering characteristic.

Scenario III: Enhanced trap generation in the cathode in the presence of an anode percolation path

Under substrate injection stress, trap generation in the IL is observed to be enhanced due to an increased voltage drop across the IL in the presence of a high- κ percolation path. On the other hand, trap generation in the high- κ is not significantly enhanced in the presence of an IL percolation path during tip injection stress. Fig. 5.29a shows stress induced SILC traps in the high- κ during tip injection stress. During substrate injection stress, trap generation in the IL is proposed to arise from the presence of percolation paths in the high- κ . However, during tip injection stress, we do not see a strong correlation between cathode trap generation and pre-existing anode (IL) percolation paths. The majority of pre-existing IL leakage sites (bright shades in Fig. 5.29b) do not result in trap generation in the high- κ , as shown in Fig. 5.29c. The bright shades in Fig. 5.29c show that only a minority of cases arise where traps are generated in the high- κ at locations where IL leakage sites exist. Even in these minority cases, the I - V curves (Fig. 5.29d) show insignificant change in the high- κ properties.

The difference in Scenario III between the substrate and tip injection stress results can be explained by a smaller electric field enhancement in the high- κ in the presence of a percolation path in the IL. During substrate injection stress, if there exists a percolation path in the high- κ , an additional voltage drop of approximately 40 % of V_s (estimated by equation 4-1 in section 4-3) will occur across an IL of 1nm. This will result in a large increase in electric field across the IL. On the other hand, during tip injection stress, an additional 20% of V_s will drop across a high- κ layer of 7 nm thickness, resulting in a relatively insignificant enhancement of electric field across the

high- κ layer. This explains the weak correlation between pre-existing percolation paths in the anode and trap generation in the cathode during tip injection stress.

Fig. 5.29: Scenario III during tip injection stress. CITS obtained from the 300 °C PDA $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ gate stack under a feedback setting of +4 V, 20 pA. (a) Increase of leakage current at +2 V observed as a second CITS scan was performed over the same area, i.e. the stress induced SILC trap in the high- κ . The image was obtained by subtracting the I_t map at +2 V of the first CITS from that of the second CITS. (b) Pre-existing IL leakage sites exhibiting barrier height lowering characteristic. Image obtained from the first CITS I_t map at -4 V. (c) Superposition of (a) and (b). The brighter shades correspond to the overlap of the bright spots in (a) with the bright spots in (b). The majority of the IL leakage sites do not accelerate high- κ wear-out. (d) Local I - V curves obtained at the bright shades in (c). Stress induced SILC in the high- κ layer is relatively insignificant even in the presence of IL leakage sites.

5.5 Breakdown evolution

Section 5.4.1 and 5.4.2 show the importance of pre-existing traps on subsequent trap generation under electrical stress. Based on the physical insights derived from the

three scenarios, under both substrate and tip injection stress, a model is proposed for the evolution of breakdown in a high- κ gate stack for each stress polarity.

Fig. 5.30 graphically shows the proposed evolution of breakdown under substrate injection stress (described in section 5.4.1). Fig. 5.30a shows an area with as-processed (thermally induced by PDA) IL SILC traps and high- κ percolation path. By as-processed we mean the sample is thermally treated (PDA) but electrical stressing has not occurred. Locations marked with label I to III describe the observed scenarios I to III in Section 5.4.1. An as-processed (filled circles) IL trap with SILC characteristic (marked as II) and a high- κ leakage site exhibiting barrier height lowering (i.e. a percolation path in the high- κ layer, marked as III) are shown in an area before substrate injection stress is applied (Fig. 5.30a). The shaded area in the high- κ layer (marked with I) shows a location with suppressed trap generation probability in the presence of an IL SILC trap, due to the mechanism described under scenario I in section 5.4.1.

Fig. 5.30b shows the area after substrate injection stress. Traps are generated (open circle) with a higher probability in the high- κ layer due to hot electron thermalization at the anode. No trap is generated at the shaded area in the high- κ (mechanism as described in scenario I). The IL SILC trap (II) will further evolve into a full percolation path in the IL due to trap generation (open circles) in the neighboring region of the pre-existing IL SILC trap by the mechanism described in scenario II. At the location with as-processed high- κ percolation path (III), a reduced voltage drop in the high- κ results in enhanced electric field in the IL layer, hence a higher trap generation probability in the IL, as explained under scenario III. Therefore, trap generation in the IL can be observed at locations with a pre-existing high- κ percolation path.

Traps generated in Fig. 5.30b (open circles in (b)) can be viewed as pre-existing traps (closed circles in (c)) in subsequent stress cycles (Fig. 5.30c). In Fig. 5.30c, the as-processed IL SILC trap (marked as II in (a) and (b)) evolves into a percolation path in the IL and the SILC characteristic (inelastic trap assisted tunneling) is extinguished. As there is no longer energy loss via the inelastic tunneling process, traps are now generated favorably in the corresponding high- κ layer. Stress induced traps (generated in (b)) percolate the high- κ layer forming a low conductivity path in the high- κ (III), initiating trap generation in the IL by the mechanism proposed under scenario III. The as-processed high- κ percolation path, with further trap generation in the corresponding IL, evolves into a full percolation path shorting the cathode to the anode, triggering a breakdown event in the entire high- κ gate stack.

Fig. 5.30: Proposed soft breakdown evolution under substrate injection stress. Filled circles in (a) show as-processed traps and open circles in (b) and (c) show newly generated traps. The shaded region shows the location where trap generation is suppressed (Scenario I). Trap generation is expected at the high- κ (anode) during substrate injection stress except at the location with IL SILC (Scenario I, see I in (b)). SILC in both IL and high- κ can further evolve into a full percolation path exhibiting barrier height lowering (Scenario II, see II in (b)). With the formation of a full percolation path in the high- κ , the corresponding IL experiences enhanced electric field, leading to trap generation process (Scenario III, see III in (c)). Soft breakdown is triggered when traps line up shorting the cathode to the anode.

Fig. 5.31 graphically shows the evolution of breakdown under tip injection stress (described in section 5.4.2). Fig. 5.31a shows an area with as-processed high- κ SILC traps and an IL percolation path. Locations marked with label I to III describe scenarios I to III in Section 5.4.2. As-processed (PDA, filled circles) high- κ traps having SILC characteristic (marked with II) and an IL leakage site exhibiting barrier height lowering (i.e. a percolation path in the IL, marked as III) are shown before tip injection stress is applied (Fig. 5.31a). The shaded area in the IL (marked as I) shows a location with suppressed trap generation probability in the presence of a high- κ SILC trap due to the proposed mechanism described under scenario I in section 5.4.2. Fig. 5.31b shows the area after tip injection stress. Traps are generated (open circle) with a higher probability in the IL due to anode hot electron thermalization. No trap is generated at the shaded area in the IL (mechanism as described in scenario I, section 5.4.2). The high- κ SILC trap (II), however, will further evolve into a percolation path in the high- κ due to trap generation (open circles) in the neighboring region of the trap by the proposed mechanism described in scenario II. At the location with an as-processed IL percolation path (III), reduced voltage drop in the IL results in enhanced electric field in the high- κ layer, hence increase trap generation probability in the high- κ , as explained by scenario III in section 5.4.2. Therefore, trap generation in the high- κ may be observed at locations with pre-existing IL percolation paths. However, because of the relatively thick high- κ layer used in our study, the electric field enhancement is small and the trap generation rate is not significantly increased (Fig. 5.29).

Traps generated in Fig. 5.31b (open circles in (b)) can be viewed as pre-existing traps (closed circles in (c)) in subsequent stress cycles (Fig. 5.31c). In Fig. 5.31c, the as-processed high- κ SILC trap (marked as II in (a) and (b)) evolves into a percolation path in the high- κ and the SILC characteristic (inelastic trap-assisted tunneling) is

extinguished. As there is no longer energy loss via the inelastic tunneling process, traps are now generated favorably at the same location in the IL (II). Stress induced traps (generated in (b)) percolate the IL forming a low conductivity path in the IL (III), initiating trap generation in the high- κ layer by the mechanism described under scenario III (section 5.4.2). The as-processed IL percolation path, with further trap generation in the high- κ layer, evolves into a full percolation path shorting the cathode to the anode, triggering a breakdown event in the entire high- κ gate stack.

The physical model of the breakdown evolution provides important implications to the reliability performance of the high- κ gate stack. The model suggests that a high density of as-processed electronic traps is likely to be the limiting factor to the reliability of the gate stack. On the other hand, as-processed SILC traps in the IL could provide additional reliability margin to the high- κ gate stack by delaying the trap generation in the high- κ . Although the SILC trap in the high- κ could evolve into a percolation path in the high- κ , electric field enhancement across a thick high- κ film is not significant in the presence of a percolation path in the IL. Effort in further reducing the process induced electronic traps, particularly in the high- κ layer, is therefore crucial in improving the reliability of the high- κ gate stack.

Fig. 5.31: Proposed soft breakdown evolution under tip injection stress. Filled circles in (a) show as-processed traps. Open circles in (b) and (c) show newly generated traps. Generated traps (open circle) in (b) can be viewed as pre-existing traps (filled circle) in subsequent stress cycles (c). The shaded region shows locations where trap generation is suppressed (Scenario I). Trap generation is expected at the IL (anode) during tip injection stress except at the locations with high- κ SILC, i.e. Scenario I (see I in (b)). SILC in both the IL and high- κ can further evolve into a full percolation path exhibiting barrier height lowering (Scenario II, see II in (b)). With the formation of a full percolation path in the IL, the corresponding high- κ experiences enhanced electric field leading to trap generation across our relatively thick film (Scenario III, see III in (c)). However, due to a relatively small electric field enhancement, this process is expected to be slow. Soft breakdown is triggered when traps line up shorting the cathode to anode.

5.6 Summary

In summary, pre-existing traps with different electronic characteristics are found to have different influence on the evolution of trap generation. This is in contrast to breakdown in ultrathin SiO_2 gate dielectric, where defect generation is found to be spatially and temporally uncorrelated to the pre-existing defects. Three scenarios (I – III), which are applicable to both substrate and tip injection stress, are proposed: (I) SILC traps at the dielectric layer next to the cathode could suppress trap generation at the corresponding location in the overlying layer next to the anode; (II) SILC traps in the dielectric layer next to the cathode could evolve into a percolation path within the layer, and (III) leakage sites which exhibit barrier height lowering characteristics at the anode could accelerate breakdown in the dielectric layer next to the cathode.

The physical implication for Scenario I is that trap-assisted tunneling via the SILC trap is an inelastic process. Electron energy loss during the inelastic tunneling process results in a “cooler” electron at the anode. We show that an inelastic trap-assisted tunneling model, which includes a downward shift of defect energy level (i.e. E_{relax}) upon electron trapping at the defect states, successfully reproduces the experimental I - V curves which are extracted from the locations with SILC traps. E_{relax} is attributed to structural deformation when the defect is charged by an injecting electron, and electron energy could then be released in the form of heat. The energy release explains trap evolution in the vicinity of pre-existing SILC traps, i.e. scenario II. Scenario III suggests there is an enhanced electric field across the dielectric layer next to the cathode in the presence of a percolation path in the dielectric layer next to the anode. Based on the three scenarios, a qualitative physical breakdown model in the high- κ gate stack is proposed [Fig. 5.30 and 5.31]. The model suggests that a high density of as-processed electronic traps in the high- κ layer is likely to be the limiting factor in the reliability of high- κ gate stack. On the other hand, as processed SILC traps in the IL could provide additional reliability margin to the gate stack by delaying trap generation in the high- κ . Although the SILC trap in the high- κ could evolve into a percolation path in the high- κ , electric field enhancement across the relatively thick high- κ is not significant in the presence of a percolation path in the IL.

Energy profiling of the SILC traps in the high- κ or IL provides further physical insights to the electrical analysis at the macroscopic MOSCAP level. SILC traps in the high- κ with an exponential distribution could be responsible for the space-charge limited current (SCLC) observed in MOSCAP measurement. The co-existence of DT and iTAT (due to SILC traps) current within an area comparable to the gate area in advanced 45 nm CMOS technology provides a physical explanation as to why both

SCLC and DT current had been observed on MOSCAPs from the same deposition process. In addition, thermally induced IL SILC traps exhibit a wide variation in energy distribution. This implies co-existence of various types of defects in the non-stoichiometric SiO_x interfacial layer. E_{relax} is estimated to be 0.9 ± 0.3 eV. No significant difference can be identified between thermally and electrically generated SILC traps.

In conclusion, the quality of the high- κ layer, in particular, plays a dominating role in improving the reliability of the high- κ gate stack. Further improvement in integrating high- κ material into CMOS technology should focus on reducing thermal annealing induced electronic traps in the high- κ layer.

Chapter 6 OXYGEN VACANCIES IN HFO₂ GATE STACK

6.1 Introduction

The physical structure of the percolation path which induces dielectric breakdown has received increasing attention. In SiO₂ or SiON, the defect structures responsible for dielectric breakdown have been proposed to be oxygen-vacancy defects [150-152] or hydrogen related defects [153-155]. Highly localized microstructural damage, such as dielectric breakdown induced epitaxy (DBIE), is also observed in both soft and hard breakdown devices [81, 156,157]. In the high- κ dielectric gate stack, in addition to DBIE, “post-mortem” analysis of gate oxide breakdown by TEM showed the formation of a self healing insulating cap (SHIC) [158]. These observed physical structures at the breakdown location, however, do not necessarily imply that they are the structures which are also responsible for accelerating breakdown of the dielectric. Knowledge of the physical structures that accelerate dielectric breakdown remains scarce. In this chapter, we correlate one of the possible physical defect structures, the oxygen vacancy (labeled V_o), to the breakdown strength of the dielectric.

We have applied the polarity dependence of STM current to the study of thermally and electrically induced localized leakage sites in the Sc₂O₃/La₂O₃/SiO_x gate stack in chapters 4 and 5. Similar observations also apply to the HfO₂/SiO_x gate stack. In this chapter, we intentionally create V_o by annealing the HfO₂/SiO_x gate stack in UHV. The leakage current performance and breakdown strength of the HfO₂/SiO_x gate stack and their correlation with V_o is undertaken. Annealing temperatures below 600 °C are chosen for this study to avoid the creation of other possible non-stoichiometric defects, for instance, the formation of Hf silicate or silicide at higher anneal temperature. Passivation of the oxygen vacancies by N₂ is found to improve the leakage current performance and the breakdown strength of the dielectric gate stack.

6.2 Experiments

The HfO₂ thin film was prepared by pulse laser deposition [159]. The sample was subjected to annealing at 430 °C in UHV for an hour to create V_o before the STM study. After STM analysis the sample was transferred to a vacuum furnace for annealing in N₂ at 500 °C for 1 hour. After the N₂ anneal, the sample was again transferred to the STM chamber for further analysis. This method provides a means for N₂ to be incorporated into high- κ films for defect passivation. The permittivity of the resultant HfO_xN_y is not significantly higher than that of the HfO₂ since the volume concentration of the incorporated nitrogen is small (approximately 1% as estimated from the XPS N1s peak). The thickness of the as-deposited HfO₂ and the HfO₂ subjected to the two-step anneal were measured by high-resolution transmission electron microscopy (TEM).

In the STM experiments, we measured constant current images (CCI) and current imaging tunneling spectroscopy (CITS). CCI was acquired at a feedback setting of +4

V, 0.1 nA before N₂ anneal. The bias voltage for CCI was increased to +5 V after N₂ anneal to account for the increase in film thickness. The measurement voltage range during CITS was restricted to ± 2 V (bias applied to the substrate), aimed at probing the HfO₂ bandgap states responsible for low-voltage leakage.

The breakdown strength of the HfO₂ was also examined via ramp-voltage stress (RVS) using STM. During RVS, the feedback control was turned off and the tip remained at a fixed separation (typically ~ 5 Å) from the HfO₂ surface. The voltage was then ramped from 0 to -10 V. The negative voltage applied to the substrate corresponds to substrate injection biasing. Three consecutive RVS were done at a given position without turning on the feedback in-between the three voltage ramps, i.e., the tip remains at a fixed separation from the HfO₂. This allows differences between the I - V curves acquired concurrently during the three RVS to be observed if the HfO₂ degrades.

6.3 Oxygen vacancies

Structural defects form localized energy states in the bandgap of the HfO₂ [34, 41, 160]. The trapping of electrons and/or holes at these localized energy states has been shown to result in instability of electrical performance, such as threshold voltage shift [161-163] and carrier mobility degradation [15, 161]. Ab-initio simulation [164] has suggested V_o to be a major source of the structural defects in the high- κ gate dielectric. Direct correlation between structural defects and leakage current down to nanometer scale has not, however, been attempted.

Simulation results [165] show a band gap state of 3.8 eV above the HfO₂ valence band maxima (VBM) can be induced by the presence of a neutral V_o (labeled V_o^0). The energy state is occupied by two electrons. The energy level rises to 4.7 eV and 5.2 eV above the HfO₂ VBM when the neutral oxygen vacancy loses one electron (V_o^+) and

two electrons (V_o^{++}), respectively (Fig. 6.1a). V_o can also act as an electron trap as it may undergo an asymmetrical relaxation when an additional electron is placed on the vacancy [166], giving rise to fast electron traps [73, 162, 167]. At a positive substrate bias in STM, there are two sources of current. Electrons in the filled gap states (Fig. 6.1a (I)) can be collected at the Si conduction band or electrons tunnel from the tip to the Si conduction band via the empty gap states at/below the tip Fermi level (Fig. 6.1b). At a negative substrate bias, the current is mainly contributed by electrons in the p-Si conduction band (inversion layer) tunneling to the tip conduction band via the empty gap states (Fig. 6.1c). We analyze the CITS data in the context of the above framework for the oxygen vacancy in the HfO₂.

Fig. 6.1: Band diagram of the HfO₂ gate stack during an STM experiment. Energy level (I) represents neutral oxygen vacancy defect states, V_o^0 , with 2 electrons occupying the energy state. Losing one electron from V_o^0 , the energy state is raised to level II. Losing both electrons from V_o^0 , the defect state is raised to level III. Band diagrams at (a) zero bias, (b) positive substrate bias, and (c) negative substrate bias.

6.3.1 Nitrogen passivated V_o in HfO₂

The finding that V_o is a major source of defects suggests that by annealing the HfO₂ in an oxygen-rich ambient, it would be possible to reduce the defect density via annihilation of the oxygen vacancy. However, post-deposition annealing (PDA) in O₂ leads to a spontaneous growth of the SiO_x interfacial layer (IL) [15]. Because of the corresponding increase in EOT, PDA in O₂ is thus deemed not viable for improving the quality of HfO₂, as far as the development of CMOS technology is concerned.

Incorporation of nitrogen into the high- κ film has been proposed as an alternative to passivate V_o . Nitrogen is believed to passivate V_o by forming the Hf-N bond. It is also believed that the Hf-N bond effectively suppresses crystallization, and hence enhances thermal stability [168, 169], allowing the HfO₂ to remain amorphous up to 1100 °C [170]. However, simply annealing the HfO₂ in N₂ would in fact exacerbate the inhomogeneity of the film and the density of electrical weak spots, as shown by conductive atomic force microscopy (CAFM) [26, 94-95]. Nitrogen incorporation by this means is inefficient since the large N₂ molecule cannot easily diffuse into the high- κ film. An unreasonably high temperature is required for N₂ to dissociate even in the presence of a metallic element [166]. Hence, other means of incorporating nitrogen into HfO₂, e.g. via the use of suitable precursors during the deposition process [170,171], surface treatment of the substrate [170, 171], plasma nitridation [93] etc., have been explored. Using CAFM, Watanabe et al. [93] showed a reduction in the density of localized leakage paths in the HfSiO/HfO₂/SiO₂ gate stack following plasma nitridation. This observation suggests that defect states in the high- κ film are indeed passivated by nitrogen, but it remains unclear if the improvement is related to the proposed interaction between nitrogen and V_o .

To clarify the physical mechanisms behind the improvements associated with nitrogen incorporation, we examine both the physical and electrical characteristics of HfO₂ annealed in a two-step process. The HfO₂ was first annealed in UHV; this step was aimed primarily at creating an oxygen-deficient HfO₂. The HfO₂ was then annealed in N₂. Evidence of the existence of nitrogen in the HfO₂ is given by XPS, demonstrating the capability of direct nitrogen incorporation into an oxygen-deficient HfO₂ via an N₂ PDA. Reduction in the low-voltage tunneling current under gate injection biasing is revealed by STM. A qualitative understanding of the STM measurement results is presented based on band theory, in conjunction with existing first-principles simulation data for the oxygen vacancy in the HfO₂ [166]. Moreover, it is observed that the breakdown strength of the HfO₂ subjected to the two-step anneal is improved. Evidence suggests that the improvement is linked to space-charge limited conduction, which limits the current flow across the gate stack under high stress voltage condition. Possible mechanisms are discussed.

6.3.1.1 Physical analysis

Figs. 6.2a and 6.2b show TEM micrographs of the as-deposited HfO₂ and the HfO₂ subjected to the two-step anneal, respectively. The as-deposited HfO₂ thickness is 4.5 nm and the SiO_x IL thickness is 1.7 nm (Fig. 6.2a). After the two-step anneal, there is no significant IL growth, consistent with previous results [15,166]. However, the HfO₂ thickness is increased from 4.5 nm to 5.1 nm (Fig. 6.2b). The increase in the HfO₂ thickness could have arisen from swelling caused by the incorporation of nitrogen and the relaxation of the Hf-Hf bond (as discussed below).

XPS analysis shows the presence of nitrogen within the two-step annealed film. Fig. 6.3a shows XPS N 1s spectra, with peaks at the N-N, Hf-N and Si-N binding

energy. This result contrasts with another study of annealing HfO₂ in N₂ [172], which showed no incorporation of nitrogen into the HfO₂ film. The difference is most likely due to the high density of oxygen vacancies in our sample arising from the UHV anneal prior to the N₂ anneal. Diffusion of nitrogen into the UHV annealed HfO₂ is possible as physical paths for diffusion are now available with a high density of oxygen vacancies. N₂ diffusion into the HfO₂ is then followed by bond formation between the oxygen vacancies and N₂ as proposed by Gavartin *et al.* [166]. Thus, a prior UHV anneal provides a route to incorporate nitrogen into the HfO₂ during a subsequent N₂ anneal.

Fig. 6.2 Cross-section TEM micrograph of (a) as-deposited HfO₂ gate stack, with 4.5 nm HfO₂ and 1.7 nm SiO_x interfacial layer (IL), (b) HfO₂ gate stack after the two-step anneal, where the HfO₂ thickness is increased to 5.1 nm and the IL thickness remains unchanged.

Fig. 6.3 (a) XPS N 1s spectra of the two-step annealed sample, showing direct evidence of the presence of N-N, Hf-N and Si-N bonding within the film. The three lines show the fit to the data (dots) and represent deconvoluted peaks of the N-Hf, N-Si, and N-N bonds. (b) Valence band offset extracted from the XPS analysis by extrapolating from the leading edge of the lowest binding energy peak, and is estimated to be 2.6 eV for the two-step annealed sample.

We postulate that nitrogen incorporation occurs within the following physical framework. A nitrogen interstitial molecule is more electronegative than a neutral oxygen vacancy (V_o^0) [166] and charge will be localized at the N_2 molecule. Hence, the nitrogen molecule is predominantly doubly negative, while the vacancy is doubly positive, as illustrated by the electron exchange reaction equation: $N_2^0 + V^0 \Rightarrow N_2^{--} + V^{++}$. The reaction is exothermic, releasing energy of 0.7 eV. A comparison with other possible reactions between N_2 and V_o shows this is the most stable configuration [166]. Further, the configuration of the N_2 passivated oxygen vacancy has an electronic configuration (i.e., $N_2^{--} + V^{++}$) similar to the neutral VN2 complex [165] (two nitrogen atoms substitute for oxygen next to the vacancy), and the main difference between nitrogen molecule and nitrogen atom passivation is on their capability to react, and hence immobilize the oxygen interstitial [166]. We adopt this explanation and use the reported values from the calculation of the neutral VN2 complex [165]. As reported, the localized charge causes relaxation of Hf ions and

increases the Hf-Hf separation to 3.90 - 3.94 Å from the bulk value of 3.54 Å [165] i.e., an increase of 11 %. This is comparable to the ~14 % increase of the HfO₂ thickness after N₂ anneal (Fig. 6.2). From the XPS data shown in Fig. 6.3b, the valence band offset of the N₂ annealed HfO₂ is estimated to be 2.6 eV, about 1 eV smaller than the reported value for pure HfO₂ (3.65 eV) [159, 164]. The reduction can be attributed to the occupancy of the N 2p states above the oxide valence band edge by electrons from neutral oxygen vacancies [165].

6.3.1.2 Electrical analysis by STM

Fig. 6.4 shows the respective CCI and CITS images (at +0.5 V, +2 V and -2 V) of the HfO₂ gate stack after (a) UHV anneal and (b) N₂ anneal. The feedback setting during CCI acquisition of the UHV annealed sample (Fig. 6.4a) is 4 V and 0.1 nA. The feedback bias setting after the N₂ anneal was increased to 5 V and 0.1 nA (Fig. 6.4b). The feedback bias must be increased to compensate for the reduced conductivity of the film after the two-step anneal to avoid mechanical contact between the sample and tip. The need to increase the sample bias to keep the tunneling current at a given level suggests an overall reduction in the leakage current after the two-step anneal.

This improvement is depicted more explicitly in Fig. 6.5. Fig. 6.5a shows the current distribution of the four CITS images (+2 V and -2 V data for both Figs. 6.4a and 6.4b). The y-axis shows the normalized cumulative number of the pixels having current less than a given value (x-axis). The absolute value of the current is smaller for the two-step annealed sample, reflecting an improvement in the leakage current (as noted above) at that biasing regime. Significant reduction in the width of the current distributions for both polarities is also evident after the two-step anneal, which implies enhanced spatial uniformity of the tunneling current characteristics. As there are

several uncertainties in comparing the absolute value of the current (i.e., the effect of the film thickness and the tip-to-sample separation), in Fig. 6.5b, we normalize the current of Fig. 6.5a to the respective current value at the 50th percentile of the distribution. The normalized current distribution confirms the improved uniformity in electronic response across the scanned area after the two-step anneal.

The reduction in the average HfO₂ conductivity may be ascribed to an increase of the high- κ thickness (i.e. a physical factor), as observed from TEM. A change in the film thickness of 10 % (i.e., from 4.5 nm to 5.1 nm) changes the tunneling current by a factor of 1.5 to 2. This is a crude estimate based on the change in the tunneling current expected at a fixed voltage for either the direct or Fowler-Nordheim tunneling regime. The average conductivity of the two-step annealed HfO₂ is decreased by a factor of ~ 3 , as shown in Fig. 6.5a. Thus, the influence of the increased film thickness cannot be discounted.

However, overall enhancement in the spatial uniformity of the tunneling current characteristics (Fig. 6.5b) implies that electronic changes within the HfO₂ also play a substantial role. This inference is further supported by the “disappearance” of bright spots (i.e. localized conductive paths) in the current maps (Fig. 6.4b) of the N₂ annealed HfO₂. The proposed framework (discussed in section 6.3.1.1.) on the passivation of the oxygen vacancies, introduced during the UHV anneal, by the subsequent N₂ anneal appears plausible and shows very good agreement with the observed improvement in the low-voltage leakage current (Fig. 6.6).

Fig. 6.4: (a) Constant current image CITS images at +0.5 V, +2 V and –2 V of the HfO₂ gate stack after the UHV anneal, and (b) after N₂ anneal. The feedback setting during the CITS acquisition was 4 V, 0.1 nA for (a) and 5 V, 0.1 nA for (b).

Fig. 6.5: Plots of normalized current distribution, as determined by the analysis of the corresponding CITS image. The y-axis is the cumulative number of pixels in a CITS image (normalized to 1) having current below the value shown on the x-axis. (a) Current distribution as a function of the measured STM current for the HfO₂ annealed in UHV (filled symbols) or annealed in the UHV followed by N₂ (two-step anneal; open symbols). Significant improvement in electrical homogeneity is observed after the two-step anneal. (b) Current distributions normalized to the current at the 50th percentile.

In Fig. 6.6, the I - V characteristics are obtained at leakage sites (i.e., the regions of highest current flow) before and after the N₂ anneal. The voltage range (± 2 V) chosen for CITS is sufficiently small such that energy states within the HfO₂ bandgap are probed. Before the N₂ anneal (i.e. after the UHV anneal), a considerable increase of current is observed at $\sim \pm 0.6$ V. The current can be attributed to resonant tunneling via the oxygen-vacancy induced gap states, which are situated ~ 0.55 eV and above from the tip/substrate Fermi level. On the other hand, such an increase in current is not observed at ± 0.6 V for the HfO₂ subjected to a subsequent N₂ anneal (i.e. the two-step anneal). Gap states due to the oxygen vacancy are shifted above the conduction band of HfO₂ with N₂ incorporated into the oxygen vacancy. In the absence of the bandgap states, resonance tunneling, e.g. trap-assisted tunneling and/or Poole-Frenkel conduction are inhibited, and hence the low-voltage leakage current is suppressed.

Fig 6.6: Low voltage (± 2 V) local I - V characteristic at a leaky site on the UHV annealed HfO₂ (filled). After N₂ anneal (open), the significant reduction in current in the low voltage regime (open) is due to passivation of gap states in the HfO₂.

6.3.2 Role of V_o and N₂ passivated V_o in HfO₂/SiO_x reliability

When the I - V measurement is extended to a wider voltage range, electronic states with energy levels beyond the HfO₂ band gap can be probed. The solid line in Fig. 6.7a shows the fresh I - V curves of the UHV annealed HfO₂ taken over the extended voltage range. The substrate bias was ramped from 0 to -10 V as compared to the much smaller range of ± 2 V used previously. It should be mentioned that tunneling current is only observed beyond -3.7 V. The onset of tunneling at ~ -3.7 V may be attributed to electrons which tunnel from the p-Si conduction band (inversion layer) to the conduction band minimum (CBM) of the HfO₂. The rapid increase in current may be ascribed to an abrupt increase in the density of states near the HfO₂ CBM [173]. The regime beyond -3.7 V is commonly referred as HfO₂ controlled Fowler-Nordheim tunneling [87], as depicted by the triangular HfO₂ barrier in the insert of Fig. 6.7a. With further increase in the applied voltage, the current exceeded the amplifier saturation point (10 nA), and hence the exact value of tunneling current could not be determined.

The solid line in Fig. 6.7b shows the corresponding fresh I - V curve for the N₂ annealed HfO₂. In this case, the onset of tunneling occurs at a less negative voltage of ~ -2.4 V. This observation suggests a lowering of the CBM in the N₂ annealed HfO₂. Band gap reduction was observed in HfO_xN_y by fitting spectroscopic ellipsometry data [174]. The extracted band gap reduction is more than the theoretically as well as experimentally observed reduction in the valence band offset [159, 164]. This suggests that the CBM of the HfO₂ is also lowered when nitrogen is incorporated, in agreement with our observation of the onset of tunneling current at a less negative substrate bias (insert of Fig. 6.7b; solid line). The band gap reduction which occurs with nitrogen incorporation can be attributed to the generation of short Hf-N bonds [182]. The

tunneling current initially increases with the applied bias but becomes “quasi-saturated” beyond -4 V. This “self-limiting” regime of the I - V curve can be fitted to a power-law, i.e. $I \propto V^\gamma$, with an exponent γ of 1.65. An exponent of 1.5 and 2 has been observed for space charge limited conduction in the vacuum [175] and a trap-free solid [176], respectively. An exponent of 1.65 therefore suggests that the self-limiting regime of the I - V curve arises from space-charge limited conduction across the HfO₂/SiO_x stack. A possible mechanism is illustrated in the insert of Fig. 6.7b. Due to a downward shift in the HfO₂ CBM (solid line), HfO₂ controlled Fowler-Nordheim tunneling correspondingly occurs at a lower bias. At a higher bias, direct tunneling (across the thin SiO_x barrier) from the Si conduction band into the HfO₂ conduction band becomes possible. Because the SiO_x is very thin (~ 1 nm), a high electron injection rate from the substrate results in net charging of the HfO₂ (due to a rapid build-up of electronic charge in the HfO₂ conduction band), leading to space charge limited conduction across the high- κ layer. Deviation of the measured exponent (1.65) from the theoretical value of 2 expected from the Mott-Gurney law may be ascribed to the vacuum gap between the W tip and the HfO₂ layer.

The self-limiting current in the high voltage regime consistently explains the apparent improvement in the breakdown strength of the N₂ annealed HfO₂ in comparison to the UHV annealed HfO₂. The breakdown strength of the HfO₂ is examined by subjecting it to multiple RVS. Substrate injection is chosen to induce breakdown in the high- κ layer [34]. After the UHV anneal, breakdown of the HfO₂ can be progressively induced within 3 RVS cycles (Fig. 6.7a). A parallel shift of the I - V curves to lower voltages can be consistently observed, which implies progressive breakdown by barrier height lowering upon formation of a percolation path [177]. After the N₂ anneal, the breakdown strength improves, as evidenced in Fig. 6.7b where

no breakdown of the HfO₂ can be observed within the 3 RVS cycles. Only stress induced leakage current is observed after the second RVS. These observations indicate an overall improvement in the breakdown strength of the N₂ annealed HfO₂. Apart from a reduced pre-existing trap density (hence more trap generation is needed to reach the critical density required for percolation path formation), it is believed that the self-limiting current in the high-voltage regime further limits trap generation rate in the N₂ annealed HfO₂. It should be mentioned that the data in Fig. 6.7 is not site dependent and can be consistently reproduced at different positions on the HfO₂/SiO_x surface.

Fig 6.7: Three consecutive RVS cycles (without feedback turning on in-between each RVS) on the HfO₂ (a) after the UHV anneal and (b) after the UHV and N₂ (two-step) anneal. The two-step annealed HfO₂ (b) exhibits improved breakdown strength because no significant change can be observed under the same stress conditions as applied to the UHV annealed HfO₂ (a). The insert in (a) is a band diagram showing F-N tunneling through a triangular HfO₂ barrier, which corresponds to the regime where current increases sharply with respect to applied voltage. The insert in (b) shows the band diagram corresponding to the self-limiting current regime. The dotted line shows the band gap before N₂ anneal. With N₂ incorporation, band gap reduction is depicted by the solid line. Direct electron injection across the thin SiO_x causes a rapid build-up of electronic charge in the HfO₂ conduction band, leading to space-charge limited conduction across the HfO₂/SiO_x stack, as characterized by a power-law I - V relationship.

6.4 Summary

The incorporation of nitrogen into HfO₂ during PDA in N₂ is demonstrated via a two-step anneal; the first anneal in UHV and subsequently in N₂. Direct evidence for the presence of nitrogen in the HfO₂ is provided by XPS. HfO₂ thickness is increased following the two-step anneal, resulting in an overall decrease in the average film conductivity. More importantly, the two-step annealed HfO₂ exhibits enhanced spatial uniformity of *I-V* characteristic, which implies that the observed improvement is also linked to electronic changes within the HfO₂ network. Band theory analysis, in conjunction with existing ab-initio simulation data on V_o induced gap states in HfO₂, consistently explain the reduction in low-voltage leakage under gate injection biasing, as observed via STM. This implies that the electronic changes are related to the passivation of oxygen vacancies in the HfO₂ by nitrogen. Improvement in the breakdown strength of the two-step annealed HfO₂ is revealed through ramp-voltage stress. Evidence suggests that breakdown strength improvement is associated with space-charge limited current conduction through the high-κ gate stack, which limits trap generation in the HfO₂ in the high stress voltage regime. A physical framework involving band gap narrowing of HfO_xN_y, which in turn decreases the bias voltage needed for transition from HfO₂ controlled Fowler-Nordheim injection to direct tunneling across the ultra-thin SiO_x, provides a plausible explanation for the prominent space-charge limited conduction in the two-step annealed HfO₂.

Chapter 7 CONCLUSION AND RECOMMENDATIONS

7.1 Conclusion

Our study on advanced high- κ gate stacks based on detailed analysis from STM experiments provides useful insights to the evolution of electronic traps under electrical stress, and hence has implications to the reliability physics of transistors with high- κ dielectric as gate materials. The major milestones achieved in this project can be summarized as:

- (i) Demarcation of electronic traps in the high- κ and SiO_x interfacial layer via spatially resolved I - V measurement under different polarity.
- (ii) Identification of individual electronic traps responsible for two distinct localized I - V characteristics, i.e. traps which exhibit Stress Induced Leakage Current (SILC) behavior and traps which correspond to a soft-breakdown characteristic.
- (iii) Understanding of thermal effects on the high- κ gate dielectric by measuring electrical uniformity and I - V of localized leakage sites of as-deposited and Post-Deposition Annealed (PDA) samples. Localized weak spots are shown to increase in density and decrease in effective resistance under tip injection

biasing (which can be identified with the electrical property of the high- κ layer) upon high temperature PDA. An intermediate PDA temperature (500 °C) for optimum uniformity and C - V characteristics is identified.

(iv) Real time visualization of trap generation in each layer under electrical stress.

A distinct trend in trap generation at locations with or without pre-existing traps is observed. Briefly, three scenarios (I - III) were identified for locations with pre-existing traps. (I) SILC traps at the cathode layer could suppress trap generation in the corresponding anode layer. (II) SILC traps at the cathode layer could evolve into a percolation path. (III) Leakage which shows barrier height lowering at the anode could accelerate breakdown in the cathode. The observations can be attributed to inelastic trap-assisted tunneling via SILC traps and enhanced electric field in the cathode layer in the presence of a percolation path in the anode layer. At locations without pre-existing traps, electronic traps are generated at a higher rate in the high- κ due to a higher anode hole injection coefficient. The results have important implication for high- κ gate stack reliability aspect because trap generation in high- κ gate stack is shown to be correlated to pre-existing electrical defects, in contrast to the uncorrelated breakdown observed in ultra-thin SiO_2 gate dielectric.

(v) Modeling of SILC traps with inelastic trap-assisted tunneling and derivation of trap distribution with respect to electron energy. The models provided a good comparison with I - V data, allowing, for example, thermally and electrical induced traps to be compared.

(vi) Identification of leakage contributed from neutral oxygen vacancies. A two-step annealing process using N_2 is shown to passivate the oxygen vacancies.

The proposed annealing method successfully improves the uniformity, leakage performance and reliability of the high- κ gate stack.

7.2 Recommendations

We believe that this project could be further extended. Some possible directions for future investigations and studies are given as follows:

- Using equation 4-1 to estimate the transition between DT and FN tunneling regime is an first order approximation. For better accuracy, onset of FN mechanism can be extracted by constant- k -attenuated-transmission (CKAT) tunneling model. CKAT model preserves resonant tunneling characteristics due to electrons reflection at the triangular barrier (during FN tunneling). This distinct characteristics in FN tunneling regime provides a clearer transition with higher accuracy. However, several experimental concern should be taken into consideration. Firstly, measurement temperature must be low such that thermal noise can be suppressed. Otherwise, Gundlach oscillation can be hardly observed. Secondly, the physical thickness of the film should be thin enough to allow significant tunneling current [183].
- To identify the dominant trap generation mechanism in the presence of pre-existing electronic traps exhibiting different I - V characteristics. Three scenarios have been shown in Chapter 5. However, the fact that all three scenarios co-exist in most cases poses difficulty in decoupling the three scenarios and quantifying the trap generation rate in each respective case.
- Improved uniformity, leakage performance and reliability of the HfO_2 gate stack was shown using the two-step nitrogen annealing process. Similarly, the use of La

to passivate HfO_2 could be investigated. La incorporation serves as an alternative in removing oxygen vacancies and improving the breakdown strength of HfO_2 . In addition, La incorporation has been reported to resolve the issue of Fermi level pinning, increase crystallization temperature in the HfO_2 thin film and increase the κ value and band gap. Theoretical calculations have shown increased V_o formation energy in the vicinity of a La atom, and atomic scale (STM) verification would be of interest.

- UHV STM could also be done to measure and image films as experiments were conducted in-situ. For instance, annealing could be undertaken as a variable temperature STM, allowing the evolution of individual traps to be monitored with changing temperature in real time. In-situ passivation experiments (for example, with nitrogen) are also feasible.

Author's Publications**Journal papers:**

- [1] **Y. C. Ong**, D. S. Ang, K. L. Pey, S. J. O'Shea, K. E. J. Goh, C. Troadec, C. H. Tung, T. Kawanago, K. Kakushima, H. Iwai "Bilayer gate dielectric study by scanning tunneling microscopy", *Appl. Phys. Lett.* 91, 102905 (2007)
- [2] **Y. C. Ong**, D. S. Ang, K. L. Pey, Z. R. Wang, S. J. O'Shea, C. H. Tung, T. Kawanago, K. Kakushima, and H. Iwai, "Electronic trap characterization of the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3$ high-kappa gate stack by scanning tunneling microscopy", *Appl. Phys. Lett.* 92, 022904 (2008)
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International conferences:

- [1] **Y. C. Ong**, S. J. O'Shea, D. S. Ang, K. L. Pey, T. Kawanago, K. Kakushima, H. Iwai, "Scanning Tunneling Microscopy on bi-layer gate dielectric stack of $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3/\text{SiO}_x$ ", *International Conference on Nanoscience and Technology*, Sweden, 2007
- [2] **Y. C. Ong**, D. S. Ang, S. J. O'Shea, K. L. Pey, T. Kawanago, K. Kakushima, H. Iwai "Characterization of the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3$ High-k Gate Stack by STM", *International Conference on Solid State Devices and Materials*, Japan, 2007

- [3] **Y. C. Ong**, D. S. Ang, S. J. O'Shea, K. L. Pey, T. Kawanago, S. J. Wang, C. H. Tung, K. Kakushima, H. Iwai, "Thermal Stability of High- κ Dielectrics – A Nanocharacterization Perspective", *International Conference on Solid State Devices and Materials*, Japan, 2008
- [4] **Y. C. Ong**, D. S. Ang, S. J. O'Shea, K. L. Pey, T. Kawanago, K. Kakushima, H. Iwai, C. H. Tung, "Trap Generation in $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3$ High- κ Gate Stack by Nanoscale Electrical Stress", *International Conference on Solid State Devices and Materials*, Japan, 2008
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