Development of process technology for fabrication of 4H-SiC silicon carbide schottky barrier diodes

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**Development of Process Technology
For
Fabrication of 4H-SiC Silicon Carbide Schottky Barrier Diodes**

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Summary

In recent times, 4H-SiC has been at the center of power semiconductor device research due to its superior material properties such as large bandgap ($E_g \sim 3.26$ eV), high breakdown electric field ($E_c \sim 3$ MV/cm which is almost 10 times that of Si), high saturated electron velocity ($\sim 2.0 \times 10^7$ cm/s which is almost 2 times that in Si), high thermal conductivity ($K \sim 4.9$ W/cm.K) and most importantly ability to form a stable native oxide SiO_2 . Schottky barrier diodes (SBDs) based on 4H-SiC offer superior dynamic performance (< 20 nC reverse recovery charge for a 1200 V, 1A SBD), almost 100 times lower specific-on resistance compared to Si SBDs and PiN diodes. The higher bandgap results in much higher schottky barrier height compared to Si and GaAs resulting in extremely low leakage currents even at elevated temperatures ($> 300^\circ\text{C}$ operation).

Edge termination and passivation is a critical technology for power devices to fully realize their voltage blocking potential. The objective of this research was to develop the process technology for fabrication of high voltage 4H-SiC SBDs. We decided to use a simple edge termination technique based on Field-Plate (FP) termination. The simplicity of FP termination lies in the fact that unlike other termination techniques such as guard rings, mesa and Junction Termination Extensions (JTE), it does not need high temperature ion-implantations. Such high temperature implantation requires the substrate to be maintained at $700\text{-}1000^\circ\text{C}$ during implantation. It also needs subsequent extreme high temperature anneals in excess of 1500°C to reduce implantation damage. There are also design issues such as the need to optimize ring spacing. FP termination technique has long been a power horse of Si power device technology using thick SiO_2 field oxide and poly silicon as electrode overlapping the oxide. For past decade or so since its first application to SiC power device

technology, FP technique was found wanting and insufficient. A simple and straight forward adaptation of this technology from Si to SiC by using SiO₂, suffers major drawbacks due to the lower dielectric constant (k) of SiO₂ ($k \sim 3.9$ which is almost 2.5 times lower than that of SiC $k \sim 9.7$) and the resulting extreme electric fields. In this work we optimized FP termination using a higher dielectric constant material AlN ($k \sim 8.1 - 8.4$). Apart from its higher dielectric constant, AlN is an excellent candidate to replace SiO₂ due to its high thermal conductivity ($\sim 3.0-3.8$ W/cm.K), moderately higher bandgap ($E_g \sim 6.2$ eV) and breakdown strength (~ 6 MV/cm), similar bond length and thermal expansion coefficient to SiC. Furthermore its properties can be enhanced by addition of hydrogen to form hydrogenated AlN which leads to smoother surface and a decrease in oxygen impurities and film stress. The film also becomes denser and there is a suppression of formation polycrystalline phases. Consequently sputter deposited AlN_x and AlN_y:H has been used to form FP terminated SBDs. The devices have been studied with and without an intermediate thermal SiO₂. The intermediate thermal SiO₂ improve the conduction and valence band offset between 4H-SiC and the Al-based dielectrics and reduces leakage currents. These devices have been compared with conventional SiO₂ FP devices fabricated in this study using PECVD SiO₂. We have also studied these Al-based dielectrics which includes AlN_x, AlN_y:H and AlO_z as passivation dielectrics for unterminated 4H-SiC SBDs.

During the course of this study, extensive 2D device simulations using Medici^{TM} from Synopsis were employed to optimize the FP design in terms of dielectric thickness and metal overlapping the dielectric. The device simulations provided extensive insights in to electric field distributions and ways to minimize edge field enhancements. Reasonably good match has been obtained between the simulated and experimental breakdown voltages for unterminated and FP terminated SBDs.

RF magnetron reactive sputtering from a pure Al (99.999%) target in N_2/Ar and $N_2:H_2$ (80%:20%)/Ar gas mixture has been utilized to deposit AlN_x and $AlN_y:H$ while PECVD has been used to deposit SiO_2 . We have studied these dielectrics with and without an intermediate thermal oxide layer. The deposited Al-based dielectrics have been characterized physically using XRD and electrically using $C-V$ and $I-V$ measurements on MIS capacitors. Physical characterization revealed suppression of c-axis preferred orientation of $AlN(0002)$ when hydrogen was introduced into the film leading to an amorphous and dense structure for $AlN_y:H$. Also $AlN_y:H/SiO_2$ stacking structure was the best electrically with an equivalent oxide field strength as high as 13-14 MV/cm which is a remarkable improvement over thermal SiO_2 and PECVD- SiO_2/SiO_2 stacks which had a breakdown strength of ~ 10 MV/cm. AlN_x/SiO_2 had a slightly lower breakdown strength due to its polycrystalline structure which increased grain boundaries and leakage current through the device. The breakdown sequence and the phenomena of multi-step breakdown seen on these high- k dielectrics/ SiO_2 stacks have been studied using measurements of dielectric relaxation current on MIS capacitors. On the composite stack in terms of breakdown, the thermal SiO_2 proved to be the weakest link for as-deposited dielectrics. Extreme electric field which is almost 2.5 times in the SiO_2 compared to that in the Al-based dielectric coupled with defects generated by electrons that have been injected in to the SiO_2 leads to its eventually destruction. Nevertheless SiO_2 is needed to reduce leakage currents due to the low conduction/valence band offset between 4H-SiC and the high- k dielectrics. On the contrary, in a dielectric stack that has undergone a 950 °C rapid thermal annealing (RTA), the high- k dielectric tends to breakdown first due to formation of defects and grain boundaries as a result of the annealing.

We investigated the use of Al-based dielectrics, including sputter deposited AlN_x , $AlN_y:H$ and AlO_z , as passivation layer for unterminated 4H-SiC SBDs. The larger dielectric

constants of the Al-based dielectrics reduce the surface fields and hence improve the long-term reliability of the devices. It was found that using a stack of Al-based dielectrics with a thin thermal oxide ($\sim 5\text{-}15\text{ nm}$) as the passivation layer, the leakage currents of the SBDs is substantially reduced. The thin thermal oxide serves as an interfacial layer between the Al-based dielectrics and 4H-SiC, without which the interface quality will be poor with a very high density of negative charge. Moreover, there will also be increased tunneling leakage current through the dielectric due to the small conduction band offset between the Al-based dielectrics and 4H-SiC. Besides, if the Al-based dielectrics were to form directly on the 4H-SiC, there will also be increased surface leakage current due to sputter induced damage on the 4H-SiC. We found a remarkable reduction by almost two to three orders of magnitude in the leakage currents for SBDs passivated by Al-based dielectrics (AlN_x , $\text{AlN}_y\text{:H}$, AlO_z) with an interfacial SiO_2 compared to unpassivated devices. The result is also much better than the about one order of magnitude reduction in the leakage currents seen when using the conventional PECVD SiO_2 for the passivation. These Al-based dielectric passivations will greatly benefit devices like MESFETs where SiO_2 , Si_3N_4 passivation are known to degrade device gain under continuous wave operation due to self heating and low passivation heat conductivity.

Following the work on the passivation of 4H-SiC SBDs, we have successfully developed the process technology for the fabrication of high voltage FP terminated 4H-SiC SBDs, using the high- k dielectric aluminum nitride (AlN) as the FP. Unterminated SBDs were also fabricated in this study for comparison. These devices were noted to suffer from premature breakdown due to electric field enhancements at the edges of the Schottky contact. For example, with a 4H-SiC doping concentration $N_D = 2 \times 10^{15}/\text{cm}^3$, the breakdown voltage V_B achievable is only 600-700 V for the unterminated SBDs. This is just about 20-30% of the ideal theoretical breakdown voltage for such devices of $\sim 2100\text{ V}$. In contrast,

for the PECVD SiO₂/SiO₂ and Al-based dielectrics/SiO₂ FP terminated SBDs fabricated, V_B has substantially increased to ~1100 V and ~1750 V respectively. The reverse bias leakage current at higher voltages is almost one order of magnitude lower for the Al-based dielectric/SiO₂ FP devices compared to PECVD SiO₂/SiO₂ based FP devices, while the forward turn-on characteristics up to 573 K are comparable. Thus we not only gain on V_B but also reap the benefits of reduced power losses when using Al-based dielectric/SiO₂ instead of conventional PECVD SiO₂/SiO₂ as FP.

Through our work, we have made an effort to bring to forefront the relevance of FP technique for SiC using alternative dielectrics with higher k . As the SiC technology faces rapid industrialization, the technique has a potential to be adopted in future commercial SiC devices such as SBDs and MESFETs.

Table of Contents

Acknowledgements.....	I
Summary.....	III
Table of Contents.....	VIII
List of Acronyms.....	XII
List of Figures.....	XIV
List of Tables.....	XXI
1. Introduction.....	1
1.1 Background.....	1
1.2 Motivation.....	3
1.3 Objectives.....	5
1.4 Major Contribution of the thesis.....	6
1.5 Organization of the thesis.....	9
2. SiC Material Properties and Metal-Semiconductor Contacts.....	12
2.1 SiC Material Properties and Crystal Structure.....	12
2.2 Electronic Properties of SiC.....	15
2.3 Ohmic Contact Formation on SiC.....	17
2.4 Schottky Contacts on SiC and Schottky barrier diodes.....	19
2.4.1 Schottky Contact Interface Physics.....	19
2.4.2 Current Density-Voltage Relationship for SBD and Parameter Extraction.....	24
2.4.3 Schottky barrier heights on 4H-SiC.....	25
2.5 Edge Termination Techniques for High Voltage SiC Devices.....	26

2.6 Conclusions.....	35
3. Numerical Simulations of 4H-SiC Schottky Barrier Diodes.....	36
3.1 Physics of Numerical Simulations.....	37
3.2 Physical Models for 4H-SiC Simulations.....	38
3.2.1 Recombinations.....	38
3.2.2 Lifetimes.....	39
3.2.3 Intrinsic Carrier Concentration n_{ie}	40
3.2.4 Band Gap	40
3.2.5 Band Gap Narrowing.....	41
3.2.6 Incomplete Ionization.....	41
3.2.7 Mobility.....	43
3.2.8 Impact Ionization.....	44
3.3 Numerical Simulation of Ideal and Unterminated 4H-SiC SBDs.....	46
3.4 Numerical Simulation of Unterminated 4H-SiC SBDs with a Secondary Layer of Passivation.....	49
3.5 Numerical Simulations of FP Terminated 4H-SiC SBDs.....	53
3.6 Conclusions.....	67
4. Dielectrics Characterization.....	69
4.1 Process Details.....	69
4.2 Dielectric Physical Characterization.....	72
4.3 Dielectrics Electrical Characterization.....	75
4.4 Breakdown Phenomena of Al-based Dielectrics.....	88
4.5 Conclusions.....	94
5. Unterminated 4H-SiC Schottky Barrier Diodes.....	97
5.1 Sample Description and Fabrication Process Details.....	97

5.2 Capacitance Voltage ($C-V$) Measurements for N-type Nitrogen Dopant Profile.....	100
5.3 Unterminated SBD Performance Characterization.....	101
5.3.1 Temperature Dependence of $J-V$ Characteristics.....	102
5.3.2 Kink in the Forward Bias $J-V$ Characteristics of SBDs.....	103
5.3.3 Schottky Metal Dependence of Barrier Height.....	104
5.3.4 Epilayer Doping Effects on Forward Bias $J-V$ Characteristics...	106
5.3.5 Effects of Schottky Contact Annealing on the Forward $J-V$ Characteristics.....	107
5.4 Breakdown Voltage Measurements of Unterminated 4H-SiC SBDs.....	109
5.5 Passivation of 4H-SiC Unterminated Diodes Using Al-based High- k Dielectrics.....	112
5.5.1 Passivation Experimental Details	113
5.5.2 Passivation Experimental Results and Discussion.....	114
5.6 Conclusions.....	125
6. Field Plate Terminated 4H-SiC Schottky Barrier Diodes.....	127
6.1 FP Terminated Device Process and Fabrication Details.....	127
6.2 FP Terminated SBDs Forward Bias Characterization Results.....	132
6.3 FP Terminated SBDs Breakdown Voltage Characterization.....	134
6.4 2-step Breakdown of FP terminated 4H-SiC SBDs.....	142
6.5 Comparisons of Experimental and Simulated Results.....	144
6.5.1 Comparison of Experimental and Simulated Unterminated 4H-SiC SBDs.....	144
6.5.2 Comparison of Experimental and Simulated FP terminated 4H-SiC SBDs.....	146

6.5.3 Electric Field profile of FP terminated 4H-SiC SBDs along the schottky edge with 2-step Breakdown.....	149
6.6 Conclusions.....	151
7. Conclusions and Recommendations for Future Work.....	152
7.1 Conclusions.....	152
7.2 Recommendations for Future Work.....	157
Author's Publications.....	159
Bibliography.....	161
Appendices.....	169
A. Rights and Permissions.....	169

List of Acronyms

ALD	Atomic Layer Deposition
CVD	Chemical Vapour Deposition
C-V	Capacitance-Voltage
DI	Deionized
DT	Direct Tunnelling
EOT	Equivalent Oxide Thickness
FE	Field Emission
FP	Field Plate
FMR	Floating Metal Ring
HF	Hydro Fluoric Acid
HM	Hard Mask
IL	Intermediate Layer
JBS	Junction Barrier Schottky
JTE	Junction Termination Extension
J-V	Current Density-Voltage
M-S	Metal-Semiconductor
MIS	Metal-Insulator-Semiconductor
PECVD	Plasma Enhanced Chemical Vapour Deposition
PR	Photoresist
RESP	Resistive Schottky Barrier Field Plate
RF	Radio Frequency
RT	Room Temperature

RTA	Rapid Thermal Annealing
SBD	Schottky Barrier Diode
SBH	Schottky Barrier Height
SBKD	Soft Breakdown
TE	Thermionic Emission
TTT	Thermionic Trap-assisted-tunneling
XRD	X-ray Diffraction

List of Figures

Fig. 2.1	The (a) diamond and (b) zinc blende unit cell. For SiC, the large bright atoms are Si and the small dark atoms are C. The tetrahedral bonding of (c) C atom surrounded by 4 Si atoms and (d) Si atom with nearest 4 C atoms...	13
Fig. 2.2	The different order of stacking in SiC is shown: (a) the position of the first layer of atoms of Si and C is illustrated as A whereas the next layers can be shown as B and C. The top- and side-view of 3C-, 4H-, and 6H-polytype stacks are shown in (b), (c), and (d), respectively [25].....	14
Fig. 2.3	Energy band diagram for the ideal case (Schottky-Mott limit) with the absence of surface states a) metal and semiconductor separated by large distance b) metal and semiconductor in intimate contact.....	20
Fig. 2.4	Band diagram for a non ideal metal-semiconductor interface under forward bias. An insulating layer of thickness δ exists between the metal and semiconductor and surface states are filled to the level ϕ_0	21
Fig. 2.5	6H-SiC SBDs using a) FMR and b) RESP from Bhatnagar <i>et al.</i> [39].....	26
Fig. 2.6	(a) Schematic of Schottky diodes with p-epi guard ring formed by LOCOS process (b) breakdown J - V characteristics for the same structure [40].....	27
Fig. 2.7	Edge Terminations of SiC SBDs using a) High resistive region using Ar implantation [41], b) Using a p- doped guard ring using B+ implantation [42].....	28
Fig. 2.8	Edge Termination using Oxide Field plate from V. Saxena <i>et al.</i> [10].....	29
Fig. 2.9	Relationship between breakdown voltage and Field Plate oxide thickness for doping $N_A=1 \times 10^{16}/\text{cm}^3$ [45].....	30

Fig. 2.10	Schematic cross-sections of Schottky diode structures with (a) single-zone and (b) double-zone JTE [46].....	30
Fig. 2.11	Reverse leakage current characteristics of JTE and Floating guard rings terminated 4H-SiC PiN diodes with and without FP [11].....	32
Fig. 2.12	Reverse leakage of passivated and unpassivated diodes [11].....	33
Fig. 2.13	a) Schematic cross section of a 10 kV 4H-SiC JBS diode, (b) Reverse blocking characteristics of a 0.88-cm ² 10 KV JBS diode at different temperatures [48].....	34
Fig. 3.1	Structural schematic of 4H-SiC SBD for a) an ideal structure b) an unterminated structure. Figure not exactly to the scale.....	47
Fig. 3.2	Simulated breakdown voltage for different doping for unterminated and ideal 4H-SiC SBD.....	48
Fig. 3.3	Structural schematic of 4H-SiC unterminated SBD with a secondary layer of passivation used for numerical simulation.....	50
Fig. 3.4	Electric field distribution at reverse bias voltage of 580 V for unterminated 4H-SiC SBD with a layer of secondary passivation a) SiO ₂ /thermal-SiO ₂ with $k=3.9$ and $Q_F= +5 \times 10^{11}/\text{cm}^2$ b) AlN/thermal-SiO ₂ with $k=8.2$ and $Q_F= -5 \times 10^{11}/\text{cm}^2$	51
Fig. 3.5	Schematic of FP terminated 4H-SiC SBD used for numerical simulations. The device has an intermediate layer of SiO ₂ with a thickness of 0.05 μm , while t_{di} refers to the total dielectric thickness including the intermediate SiO ₂ . Figure not exactly to scale.....	53
Fig. 3.6	Simulated results of breakdown voltage vs. dielectric thickness of a SiO ₂ /SiO ₂ FP terminated 4H-SiC SBD.....	55
Fig. 3.7	Peak electric field within SiC bulk and within FP dielectric SiO ₂ at 500 V	

	of reverse bias for SiO ₂ /SiO ₂ FP terminated 4H-SiC SBD.....	56
Fig. 3.8	Electric Field distribution for SiO ₂ /SiO ₂ FP device for 2 different thickness a) $t_{di} = 0.1 \mu\text{m}$, b) $t_{di} = 1.3 \mu\text{m}$ at 500 V of reverse bias around the vicinity of schottky corner. The inset shows the zoom-in of the regions of peak electric field.....	58
Fig. 3.9	Band-Band generation distribution as a result of impact ionization for a) $t_{di} = 0.1 \mu\text{m}$, b) $t_{di} = 1.3 \mu\text{m}$ at 500 V of reverse bias. In the inset shows the zoom-in of the region of maximum impact ionization.....	59
Fig. 3.10	Simulated results of breakdown voltage vs. dielectric thickness for an AlN/SiO ₂ FP terminated 4H-SiC.....	60
Fig. 3.11	Peak electric field within SiC bulk and within FP dielectric AlN and intermediate SiO ₂ at 500 V of reverse bias for AlN/SiO ₂ FP terminated 4H-SiC SBD.....	62
Fig. 3.12	Peak electric field within a) FP dielectric at secondary Corner S b) SiC bulk at 500 V of reverse bias.....	63
Fig. 3.13	Electric Field distribution at 500 V of reverse bias for AlN/SiO ₂ FP terminated at a dielectric thickness of a) $t_{di} = 0.1 \mu\text{m}$ and b) $t_{di} = 1.3 \mu\text{m}$	65
Fig. 3.14	Band to band generation map of AlN/SiO ₂ FP terminated 4H-SiC SBD for a) $t_{di} = 0.1 \mu\text{m}$ and b) $t_{di} = 1.3 \mu\text{m}$	66
Fig. 4.1	XRD spectra of sputter deposited AlN _x films on SiO ₂ /Si substrate (a) as-deposited (b) after 950 °C/60 s N ₂ anneal.....	73
Fig. 4.2	XRD spectra of sputter deposited AlN _y :H films on SiO ₂ /Si substrate (a) as-deposited (b) after 950 °C/60 s N ₂ anneal.....	74
Fig. 4.3	High frequency (1MHz) C-V curves of MIS capacitors with the dielectric a) as-deposited on thermal SiO ₂ b) after a 950°C RTA in N ₂ for 60 s on	

	thermal SiO ₂	77
Fig. 4.4	High frequency (1MHz) C - V curves of MIS capacitors with as-deposited dielectrics on 4H-SiC without thermal SiO ₂	78
Fig. 4.5	Flat-band voltage shift ΔV_{FB} for different Al-based dielectric thickness.....	82
Fig. 4.6	Flat-band voltage shift ΔV_{FB} as a function of RF sputtering power.....	83
Fig. 4.7	High Frequency (1 MHz) C - V curves of samples deposited with RF power at 450 watts showing emergence of hysteresis due to sputter induced damage.....	84
Fig. 4.8	Leakage current density (J) vs. equivalent oxide field (E) characteristics at 27°C for MIS capacitors with a) dielectric as-deposited b) after a 950°C/60s RTA in N ₂	86
Fig. 4.9	Schematic of 4H-SiC MIS capacitor with the Al-based dielectric/SiO ₂ stack showing the direction of J_g and J_{relax}	88
Fig. 4.10	J_g and J_{relax} as a function of electric field measured on MIS capacitors with as-deposited AlN _y :H/SiO ₂ dielectric stack as well on capacitor sample with just the thermal SiO ₂ as a dielectric.....	90
Fig. 4.11	Energy-band diagram visualization of the stacked capacitor in accumulation.....	91
Fig. 4.12	J_g and J_{relax} as a function of electric field measured on a MIS capacitor sample with AlN _x /SiO ₂ dielectric stack annealed at 950°C for 60 s in N ₂	93
Fig. 5.1	Optical picture of fabricated unterminated diode after passivation.....	99
Fig. 5.2	Capacitance-Voltage measurements on different doping samples for n-type dopant profile extraction at ambient and at 473 K.....	101
Fig. 5.3	Forward current density- voltage (J - V) characteristics of a Ni/4H-SiC SBD at different temperatures. The inset shows the J - V characteristics on a linear	

scale.....	102
Fig. 5.4 Ni/4H-SiC SBD RT Forward J - V characteristic showing a kink in the turn-on region.....	103
Fig. 5.5 Forward bias J - V characteristics of metal/4H-SiC SBD formed using different metals. The inset shows the J - V characteristics on linear scale.....	105
Fig. 5.6 Experimental barrier height plotted against schottky metal work function. The schottky contacts have been formed with metals as-deposited.....	106
Fig. 5.7 Forward turn-on characteristics of Pt/4H-SiC SBD formed on epilayers with different drift layer doping N_D . The inset shows the J - V characteristics on a linear scale.....	107
Fig. 5.8 Barrier height and specific on resistance (R_{on}) trends vs. Temperature for Ni Schottky contacts as deposited and with Schottky contact annealing (450°C for 5 min in N ₂) for $N_D = 1 \times 10^{16} / \text{cm}^3$. Also shown is the barrier height and R_{on} for Pt 4H-SiC SBDs with $N_D = 3 \times 10^{15} / \text{cm}^3$ for R_{on} temperature dependence comparison with lower doped Ni SBDs.....	108
Fig. 5.9 Experimental breakdown voltage V_B for unterminated 4H-SiC SBDs for different N_D	110
Fig. 5.10 Leakage current characteristics of unterminated 4H-SiC SBDs up to the point of breakdown.....	111
Fig. 5.11 a) Leakage current characteristics with and without passivation of 4H-SiC SBD samples but with an intermediate thermal oxide layer.....	115
Fig. 5.11 (b) Leakage current characteristics with and without passivation of 4H-SiC SBD samples but without intermediate thermal oxide layer.....	118
Fig. 5.12 (a) Ideality factor (η) (b) Barrier height (ϕ_B) of 4H-SiC SBDs with and without passivation.....	120

Fig. 5.13	High frequency (1 MHz) C - V characteristics of 4H-SiC SBDs with and without $\text{AlN}_y\text{:H}$ as passivation.....	122
Fig. 6.1	Schematic of Process flow used for fabrication of FP terminated 4H-SiC SBDs.....	128
	a) Sample after initial clean, sacrificial oxidation, device quality SiO_2 growth and ohmic contact formation.....	128
	b) Sample after dielectric deposition and patterning with double coated layer of PR AZ1518 baked for 45 min to form a hard mask.....	129
	c) Sample after dielectric dry etch using RIE and wet etch using a sequential wet etch in KOH based AZ400K followed by etch in dilute HF to strip the thermal oxide.....	130
	d) Sample after patterning for schottky metal deposition with some overlap on the dielectric.....	131
Fig. 6.2	a) Schematic of the 4H-SiC Schottky diode fabricated detailing the epilayer thickness, doping concentration (N_D), length of metal overlapping the deposited dielectrics (t_{overlap}) and thickness of the deposited dielectric (t_{dep}). The figure is not to the scale. (b) Optical picture of a completed device with a 10 μm overlap.....	132
Fig. 6.3	Forward turn-on characteristics of the FP terminated SBDs at 300 K and 573 K.....	133
Fig. 6.4	Experimental breakdown voltage (V_B) as a function of the dielectric thickness (t_{dep}) for devices with 200 μm diameter.....	135
Fig. 6.5	Leakage current characteristics for the FP terminated SBDs with optimal dielectric thickness ($t_{\text{dep}} = 0.8 \mu\text{m}$ for $\text{AlN}(\text{:H})/\text{SiO}_2$ and $t_{\text{dep}} = 0.45 \mu\text{m}$ for	

	PECVD-SiO ₂ /SiO ₂ devices) and unterminated SBDs up to point of breakdown. For comparison also shown is the characteristic of a Cree 600 V, 1 A SBD.....	137
Fig. 6.6	Leakage current characteristics for the FP terminated devices for different dielectric thickness (t_{dep}).....	139
Fig. 6.7	Illustration of the various components and paths of reverse leakage current for a FP SBD.....	140
Fig. 6.8	Reverse bias leakage current characteristics of 4H-SiC FP terminated SBDs using as-deposited Al-based dielectric/SiO ₂ dielectric stack illustrating a 2-step breakdown. Inset shows a schematic of the diode indicating the possible locations of breakdown depending upon dielectric thickness.....	142
Fig. 6.9	Comparison of experimental and simulated V_B for unterminated 4H-SiC SBDs with different N_D	144
Fig. 6.10	Simulated and experimental V_B comparison for SiO ₂ /SiO ₂ FP terminated 4H-SiC SBD.....	147
Fig. 6.11	Simulated and experimental V_B comparison for AlN _x /SiO ₂ and AlN _y :H/SiO ₂ FP terminated 4H-SiC SBD.....	148
Fig. 6.12	Electric field along a vertical cutline at secondary corner S for AlN/SiO ₂ FP SBD with t_{dep} =0.05 μ m and t_{dep} =0.45 μ m.....	149

List of Tables

Table 2.1 Comparison of properties of SiC and other semiconductors.....	15
Table 2.2 Ohmic contacts on n-type α (6H or mixed)-SiC.....	18
Table 3.1 Dopants in SiC and their ionization energy with the lattice site.....	42
Table 4.1 Key parameters extracted from the C - V and J - V measurements on the MIS samples.....	79
Table 5.1 Leakage currents at -200 V reverse bias for 4H-SiC SBD devices with diameter 200 μm , with and without deposited passivation.....	116

Chapter 1

Introduction

In this chapter, we present the motivation and objectives of our research, which focuses on the design and development of process technology for the fabrication of high voltage 4H-SiC Schottky barrier diodes (SBDs). In essence, the SBDs fabricated employ the field plate (FP) termination technique with Al-based high- k dielectrics as the FP to achieve higher breakdown voltage. This is followed by a summary of the major contributions of this work. The organization of this thesis will be discussed next, and finally the work to be presented in the subsequent chapters of this thesis will be reviewed.

1.1. Background

Traditional integrated circuits based on silicon (Si) cannot operate at temperatures more than 200 °C due to its intrinsic physical properties. In contrast, devices based on wide band gap semiconductors such as gallium nitride (GaN), silicon carbide (SiC) and diamond (C) can operate at temperatures as high as 400 °C. Among these semiconductors, SiC has emerged as the most promising material due to several advantages that it possesses. These include its outstanding physical properties of high breakdown electric field strength ($E_c \sim 3$ MV/cm), high electron saturation drift velocity ($\sim 2 \times 10^7$ cm/s) and high thermal conductivity ($K \sim 4.9$ W/cm.K) [1–3]. In addition, the availability of commercial substrates (4-inch wafers as of year 2007) and known device processing techniques render SiC very attractive for a wide variety of high power, high frequency and high-temperature device applications. It should be noted that among the wide band gap semiconductors, SiC is the only compound semiconductor that can be thermally oxidized to form a high quality native

Chapter 1 Introduction

oxide, that is silicon dioxide, similar to the oxide formed on Si. Therefore, it is possible to grow thermal oxide on SiC as masks for device processing, as device passivation layers and gate dielectrics. As a result, all devices found in Si integrated circuit technology, including high quality and stable metal oxide semiconductor (MOS) transistors, can also be fabricated using SiC.

The most common polytypic forms of SiC used for device fabrication are 4H-SiC and 6H-SiC, due to their availability of substrates and epitaxial growth techniques. In this work, we have employed the 4H-SiC polytype for the fabrication of high voltage SiC SBDs. This polytype is preferred because of its larger energy band gap ($E_g \sim 3.26$ eV), higher electron mobility parallel to the c-axis ($\mu_{cll} \sim 1000$ cm²/V.s) and absence of mobility degradation due to anisotropy as seen in 6H-SiC [3].

At present, some SiC devices are commercially available. For example, 300 V, 600 V and 1200 V SiC Schottky rectifiers with current ratings of 1-10 A are marketed by Cree Inc. These rectifiers provide designers with near ideal performance in high voltage switching operations and have already benefited a number of applications. These include Power Factor Correction (PFC) circuits in AC-DC power supplies and in AC motor drives where these SiC rectifiers enable operations at higher frequencies with increased efficiencies.

Another class of SiC device which has rapidly gained acceptance is SiC MESFETs which are being employed in a variety of hybrid and monolithic high power microwave amplifiers. These SiC MESFETs offer a number of advantages compared to GaAs MESFETs. For example, the output impedance of the total periphery required for a 40 W GaAs amplifier would be about 20 times lower than that needed for a 40 W SiC MESFET,

Chapter 1 Introduction

leading to much lower losses in an output matching network for the latter. In addition, the 5 to 10 times power density available from a SiC device compared to an equivalent GaAs amplifier makes it possible to achieve higher total power with a single chip. Cree offers commercially S-band power MESFETs with a nominal gate length of 0.7 μm and channel doping of about $3 \times 10^{17} \text{ cm}^{-3}$. These devices are capable of very high power levels due to their high breakdown voltage of 150 V. Cree has addressed trapping issues by improving the surface passivation as well as developing substrates that are free of deep level impurities. This coupled with the use of semi-insulating SiC substrates with resistivities greater than $10^{10} \Omega\text{-cm}$ have resulted in the best combination of power density and power added efficiency (PAE) reported to date for SiC MESFETs of 5.2 W/mm and 63% respectively at 3.5 GHz [4]. SiC MOSFETs is another class of devices that will potentially benefit the power device community. However, at present such devices are still not commercially available. This is due to the extremely low channel mobilities seen for the devices due to the high interface trap densities, believed to be attributed to the carbon clusters present at the thermally grown 4H-SiC/SiO₂ interface [5, 6].

1.2 Motivation

Due to its wide band gap and high breakdown electric field strength, high voltage SBDs fabricated using 4H-SiC exhibit relatively lower leakage current and on-resistance. The wider band gap of 4H-SiC allows Schottky barrier heights (ϕ_B) as high as 1.5 eV to be achieved readily [2, 3]. This gives rise to extremely low levels of leakage currents which are several orders of magnitude lower than the corresponding Si devices, even at elevated temperatures. Due to the high breakdown electric field strength, a 4H-SiC SBD will have a breakdown voltage (V_B) that is almost 10 times higher than the same device fabricated using Si. More importantly, the specific on-resistance (R_{on}) of the 4H-SiC device will be about

Chapter 1 Introduction

100 times lower than that of Si SBD of the same size. Therefore these 4H-SiC SBDs have the potential to be valuable alternative to Si-based switching devices for applications where both high power and high speed are required.

High voltage SiC devices need a suitable edge termination technique to reduce field crowding at the contact edges [7-9]. Various edge termination techniques like Mesa, floating guard rings and junction termination extension (JTE) are effective, but involve ion-implantations with substrate maintained at 800-1000 °C during implantation, followed by high temperature annealing in excess of 1500 °C to recover implantation crystal damage. Such techniques are therefore complicated. Alternatively, a simpler field plate (FP) termination technique that does not require implantation and high temperature anneals can be used [10]. It involves just an extension of the metal electrode of the device over a dielectric and therefore the fabrication process is much simpler. The FP termination can also be employed concurrently with the other implantation based termination techniques to further reduce leakage currents and improve breakdown voltages of devices [11].

The FP termination technique has been successfully applied to Si SBDs, with SiO₂ conventionally used as the FP dielectric [12]. However, the technique when applied to 4H-SiC SBDs using SiO₂ as the FP dielectric did not produce favorable results. This is mainly attributed to the lower dielectric constant of SiO₂ compared to SiC, which leads to extreme surface electric fields. The almost 2.5 times lower dielectric constant (k) of SiO₂ ($k = 3.9$) compared to SiC ($k = 9.7$), coupled with a high critical field (E_C) of ~3 MV/cm for SiC results in high electric field in SiO₂ and poses unique reliability challenges. It is estimated that at breakdown of SiC, the electric field (E) in the oxide dielectric could be as high as 7.5 MV/cm. Thus we may ultimately face reliability issues for high voltage 4H-SiC

Chapter 1 Introduction

devices, and this has deterred the wide spread use of the simple FP technique in SiC power device technology.

1.3 Objectives

The FP termination technique, which has long been a powerhouse of Si power devices, has been found insufficient and wanting for SiC. The problem can be overcome if the SiO₂ FP dielectric is replaced by other dielectrics with higher dielectric constants, the so-called high- k dielectrics [13, 14]. This will help reduce the electric fields in the dielectrics and increase the breakdown voltage of the devices. The objective of this project is to design, simulate, fabricate and optimize FP termination for 4H-SiC SBDs using a high- k dielectric AlN as the FP dielectric, which has a higher dielectric constant (k) of $\sim 8.1 - 8.5$. Apart from its higher k values, AlN is an excellent candidate to replace SiO₂ due to its high thermal conductivity ($K \sim 3.0-3.8$ W/cm.K), moderately higher bandgap ($E_g \sim 6.2$ eV) and breakdown field strength [15]. Furthermore its properties can be enhanced by the addition of hydrogen to form hydrogenated AlN (AlN_y:H) which will lead to smoother surface and a decrease in oxygen impurities and film stress. Such films are also denser and there is a suppression polycrystalline phase formations [16, 17]. This will lead to much lower leakage currents through the hydrogenated dielectric film due to reduced grain boundaries.

In this work, we have studied AlN_x and AlN_y:H deposited using the RF magnetron sputter technique to form FP terminated 4H-SiC SBDs. We have studied these devices with and without an intermediate thermal SiO₂ layer. The intermediate SiO₂ layer helps to improve conduction and valence band offset between 4H-SiC and Al-based dielectrics. The magnetron sputter technique has been chosen as it can deposit high quality AlN_x and AlN_y:H films at low temperatures. Furthermore, the sputtering process provides reasonably

Chapter 1 Introduction

high throughput at low installation and maintenance cost. The results obtained for $\text{AlN}_x/\text{SiO}_2$ and $\text{AlN}_y\text{:H}/\text{SiO}_2$ FP terminated 4H-SiC SBDs have been compared to conventional CVD- $\text{SiO}_2/\text{SiO}_2$ based FP devices fabricated using plasma enhanced chemical vapour deposited (PECVD) SiO_2 . These Al-based dielectrics, together with aluminum oxide AlO_x , were also investigated as a secondary layer of passivation dielectrics for 4H-SiC. The devices have been characterized in terms of their breakdown voltage, reverse bias leakage currents, forward bias characteristics from room temperature (RT) up to 300 °C. Various figures of merit for the devices such as their specific-on resistance (R_{on}), barrier height (ϕ_B) and ideality factor (η) have been extracted. The experimental results obtained have been compared to results obtained from numerical simulations.

1.4 Major Contributions of the Thesis

The original major contributions of this thesis are summarized as follows:

- a) Extensive numerical simulations were carried out to design and optimize FP terminated 4H-SiC SBDs based on high- k dielectrics using the 2-D device simulator Medici^{TM}. [18, 19]. The optimal dielectric thickness for obtaining maximum possible breakdown voltage (V_B) was evaluated and found to be close to 0.5 μm for SiO_2 and around 0.7-0.8 μm for higher dielectric constant materials which include Si_3N_4 and Al_2O_3 . These simulations provided us with a good starting point and formed the basis of our subsequent experimental work.
- b) Numerical simulations were also carried out to demonstrate a unique dual-step FP technique for the optimal use of high- k dielectrics [20]. We could demonstrate, using a dual step structure with a top layer of Si_3N_4 and bottom layer of SiO_2 , an

Chapter 1 Introduction

improvement in breakdown voltages by as much as 20% compared to single step SiO_2 and Si_3N_4 FP structures. The electric fields within the dielectric using a dual step structure are also found to be much reduced. This could be used to exploit and gain maximum leverage out of some higher dielectric constant (k) materials which generally tend to have lower breakdown strengths. The idea was to place the higher breakdown strength dielectric SiO_2 on top to sustain high electric field while a bottom high- k layer can shield and reduce the overall field strength in the device by virtue of its higher k value.

- c) The use of Al-based high- k dielectrics (AlN_x , $\text{AlN}_y\text{:H}$, AlO_z) as a secondary passivation layer for 4H-SiC SBDs was investigated experimentally. The results were compared to conventional passivation based on thermal SiO_2 and PECVD SiO_2 [21]. We found a reduction in leakage currents by almost two to three orders of magnitude using Al-based dielectrics compared to around one order of magnitude using conventional PECVD SiO_2 as passivation. The Al-based passivations gave rise to much reduced surface electric fields by virtue of their higher dielectric constants, and consequently lowered the edge related tunneling leakage currents. $\text{AlN}_y\text{:H}$ was found to be the best of all, leading to improvements in barrier heights by as much as 0.1-0.2 eV and reduced surface states by as much as 30%, attributed to passivation of surface dangling bonds by hydrogen. It was found that an interfacial layer (IL) of thermal SiO_2 (~5-15 nm) is needed between 4H-SiC and the deposited Al-based dielectrics, without which the leakage current increases due to low conduction and valence band offset between the overlying passivation and 4H-SiC. In the absence of interfacial SiO_2 there is increased surface leakage current too due to sputter damage and increased tunneling leakage current through the passivation dielectric itself. Also

Chapter 1 Introduction

the interface quality is poor without the IL SiO_2 which gives rise to a very high density of negative charge.

- d) High voltage FP terminated 4H-SiC SBDs using Al-based high- k dielectrics/ SiO_2 were demonstrated experimentally for the first time. Our results indicate that V_B as high as 1750 V, which is more than 80% of the ideal theoretical value, can be achieved using Al-based dielectrics. This constitutes an improvement by more than 600 V, or almost 30% of the ideal theoretical V_B , over conventional oxide based FP devices fabricated in this study using PECVD- $\text{SiO}_2/\text{SiO}_2$. The characteristics of the devices have been compared with those obtained from numerical simulations. The internal electric field distribution and impact ionization data have been used to explain the trends in the breakdown of the devices with different dielectric thicknesses. Excellent match of experimental and simulated V_B has been found especially for the range of dielectric thickness where the breakdown is dominated by edge related impact ionization. A 2-step breakdown seen for some devices have been explained by the internal electric field distribution at Schottky contact edge.
- e) Multi-step breakdown phenomena seen for some metal-insulator-semiconductor (MIS) capacitors as well as SBDs with Al-based dielectrics/ SiO_2 stack have been investigated using measurements of dielectric relaxation currents on MIS capacitors. The breakdown mechanism comprises a sequential breakdown of the SiO_2 followed by the Al-based dielectric for the as-deposited dielectrics. The SiO_2 breakdown is triggered by defects generated in the SiO_2 due to electron injection under extreme electric field. The electric field is almost 2.5 times in the SiO_2 compared to that in the Al-based dielectric. The breakdown of the Al-based dielectric may or may not follow instantaneously depending on the voltage at which the SiO_2 undergoes a

Chapter 1 Introduction

breakdown. The breakdown sequence is reverse for devices annealed at 950°C due to degradation in the Al-based dielectric breakdown strength as a result of formations of defects and grain boundaries upon annealing.

The novelties of our work are summarized as follows:

- a) Demonstration of high voltage FP terminated 4H-SiC SBDs using Al-based high- k dielectrics/SiO₂ stack for the first time. The breakdown voltage which is almost 80% of the maximum possible V_B could be achieved using these high- k FPs as termination.
- b) Demonstration of Al-based high- k dielectric/SiO₂ stack with a breakdown voltage which is about 1.3 times higher compared to conventional SiO₂ dielectric for the first time. The phenomena of multi-step breakdown and breakdown modes were successfully studied for these stacks using dielectric relaxation currents.
- c) Successfully developed and validated numerical simulation model with results that was consistent with experimental breakdown voltages. These numerical simulations were utilized to understand the physical mechanism involved in the breakdown of these FP terminated SBDs.
- d) High- k Al-based dielectric with a thin interfacial thermal SiO₂ was shown to serve as an excellent passivation layer for 4H-SiC. The higher dielectric constant of these dielectrics was shown to reduce electric field enhancement at edges, which in turn give rise to reduced tunneling leakage currents and improved breakdown voltages

1.5 Organization of the thesis

The thesis is organized into seven chapters as follows:

Chapter one describes the motivation behind this project, the objectives of our research, the main contributions of this work and the organization of the thesis.

Chapter 1 Introduction

Chapter two presents a discussion of SiC as a semiconductor, its physical structure, polytypes and its physical properties in comparison with other semiconductors such as Si, GaAs, GaN and diamond. We also outline the advantages of using SiC, in particular the 4H polytype, for device fabrication. Next we present the physics and operation of Schottky barrier diode (SBD), its various figures of merits and the techniques used to extract some important parameters of SBD. The basic processing technology behind SiC device fabrication that includes ohmic and schottky contact formation is then presented. The chapter is concluded with a discussion of the most commonly used edge termination techniques for high voltage SiC SBDs.

Chapter three begins with an introduction to the device simulator Medici^{TM} from Synopsis that has been used in this work. We explain the various models incorporated and parameters used for the numerical simulations of 4H-SiC SBDs, in particular in the simulation of electrical breakdown of the devices. Thereafter we move on to explain the simulated results for various unterminated as well as FP terminated 4H-SiC SBD structures incorporating an AlN/SiO₂ dielectric stack. The results are compared to conventional SiO₂ FP terminated devices. In this chapter, the electric field distributions within the dielectrics and within 4H-SiC, regions of high impact ionizations in 4H-SiC and field crowding effects at schottky contact edges have been analyzed to provide an insight into the detailed operation of the SBD.

Chapter four discusses the process used for dry thermal oxidation of 4H-SiC. We also present the details of our process employed to deposit Al-based and SiO₂ dielectrics using the sputtering and the PECVD techniques respectively. We present the results obtained from the physical and electrical characterization of our sputter deposited Al-based dielectric films as well as our PECVD SiO₂ and thermal SiO₂ films on 4H-SiC. The physical

Chapter 1 Introduction

characterization involved x-ray diffraction measurements, while the electrical characterization was on capacitance-voltage (C - V) and current density-voltage (J - V) measurements. The breakdown strength of these dielectrics/ SiO_2 stacks and their net charge densities are investigated. We also detail our investigation of multi-step breakdown of these dielectric stacks using relaxation current measurements.

Chapter five presents the fabrication and process details as well as the electrical characterization results of our experimental n-type 4H-SiC unterminated SBDs. Various SBD parameters such as breakdown voltage (V_B), reverse bias leakage current (J_r), ideality factor (η) and schottky barrier height (ϕ_B) have been studied as a function of the operating temperature, schottky metal type, passivation effects, schottky metal annealing conditions and drift layer doping (N_D). We also present our study of leakage current reductions and schottky barrier height (ϕ_B) improvements with surface passivation using Al-based high- k dielectrics.

Chapter six describes in detail the fabrication process of FP terminated SBDs and the measurement results of our fabricated devices with FP terminations utilizing a stack of Al-based high- k dielectrics/ SiO_2 . For comparison we also studied devices with the intermediate SiO_2 layer. The results have been compared with FP terminated SBDs fabricated using PECVD- $\text{SiO}_2/\text{SiO}_2$ stack and with just the thermal SiO_2 as the FP dielectric. A systematic study of breakdown voltage and leakage currents due to variation in the dielectric thickness has been carried out. We also compare the simulations results of unterminated and FP terminated SBDs with our experimental results.

Chapter seven presents the conclusions of our research work and recommendations for future work.

Chapter 2

SiC Material Properties and Metal-Semiconductor Contacts

In this chapter the basic physical and material properties of SiC and its comparison to some other wide band gap semiconductors will be discussed. The theory of metal-semiconductor contact formation on SiC, the physics of Schottky barrier diodes (SBDs) and the equations and methodology used for the extraction of SBD's parameters will be presented. This is followed by a literature review on the formation of good ohmic contacts, which is needed to reduce undue power losses in SiC devices. Termination techniques that have been used to improve the breakdown voltages and performance of SBDs will be discussed.

2.1 SiC Material Properties and Crystal Structure

Silicon carbide (SiC) is a compound of silicon and carbon and occurs in nature as the extremely rare mineral moissanite [22]. Due to the extreme rarity of natural moissanite, most silicon carbide is man-made. Most often it is used as an abrasive where it is often known by the trademark carborundum. The simplest manufacturing process involves combining silica sand and carbon at a high temperature, between 1600 °C and 2500 °C. Purer silicon carbide can be made by the more expensive process of chemical vapor deposition (CVD). Commercial large area single crystal silicon carbide is grown using a physical vapor transport technique commonly known as the modified Lely method [23].

The crystal structure of SiC consists of arrangement of Si and C atoms in a regular repeatable pattern. SiC occurs in the so called Zinc-blende structure [24] as shown in

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

Fig. 2.1. It consists of a hexagonal frame with a carbon atom situated above the center of a triangle of Si atoms and underneath a Si atom belonging to the next layer. The distance, a , between neighboring silicon or carbon atoms is approximately $3.08 \text{ \AA}$ for all polytypes of SiC [24]. The carbon atom is positioned at the center of mass of the tetragonal structure outlined by the four neighboring Si atoms such that the distance between the C atom to each of the Si atoms is the same and equals $1.89 \text{ \AA}$. The distance between two adjacent silicon planes is approximately $2.52 \text{ \AA}$. The stack of Si and C atoms in the SiC unit cell does not repeat alternately. The stacking order of planes of unit cell can differ greatly and hence give rise to different SiC polytypes. The height of a unit cell, c , varies depending upon the polytype.

Fig. 2.1 The (a) diamond and (b) zinc blende unit cell. For SiC, the large bright atoms are Si and the small dark atoms are C. The tetrahedral bonding of (c) C atom surrounded by 4 Si atoms and (d) Si atom with nearest 4 C atoms are shown as well.

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

Fig. 2.2 The different order of stacking in SiC is shown: (a) the position of the first layer of atoms of Si and C is illustrated as A whereas the next layers can be shown as B and C. The top- and side-view of 3C-, 4H-, and 6H-polytype stacks are shown in (b), (c), and (d), respectively [25].

Three different planes commonly known as A, B, and C can be defined as shown in Fig. 2.2 (a), where each consists of a double layer of Si and C atoms. Different polytypes are referred to by using the Ramsdell notation [25]. For example, if it has two repeating layers and a hexagonal structure, it is referred to as 2H-SiC. If we stack the layers ABC, we have a cubic crystal when viewed along an axis diagonal to the hexagonally close packed plane,

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

and it is referred to as 3C-SiC. Figure Fig. 2.2 (b) shows the top-view and side-view of the stacking order of 3C-SiC. Similarly, stacking orders of ABAC and ABCACB are called 4H-SiC and 6H-SiC respectively, and the corresponding top-view and side-view of the stacking orders are shown in Fig. 2.2 (c) and (d). There all altogether more than 500 known polytypes in SiC, and they are generally classified into two groups labeled as β -SiC and α -SiC. The former refers to cubic 3C-SiC, whereas the latter refers to all the other polytypes that include 6H-SiC and 4H-SiC.

2.2 Electronic Properties of SiC

Table 2.1 Comparison of properties of SiC and other semiconductors.

Properties	Si	GaAs	3C-SiC	6H-SiC	4H-SiC	2H-GaN	Diamond
Bandgap E_g [eV]	1.12	1.43	2.4	3	3.2	3.4	5.5
Lattice Const. [$\text{\AA}$]	$a=5.43$	$a=5.65$	$a=4.36$	$a=2.08,$ $c=15.12$	$a=3.08,$ $c=10.08$	$a=3.189$ $c=5.185$	$a=3.567$
Critical field E_c [MV/cm]	0.25	0.3	2	2.5	2.2	3	5
Sat velocity V_{sat} [10^7 cm/s]	1	1	2.5	2	2	2.5	2.7
Electron mobility μ_n [$\text{cm}^2/\text{V.s}$]	1300	8500	1000	$C_p=415$ $C_{II}=87$	$C_p=947$ $C_{II}=1141$	400	2200
Hole mobility μ_p [$\text{cm}^2/\text{V.s}$]	480	400	40	80	120	30	1600
Dielectric Const. ϵ_r	11.9	13	9.7	10	10	9.5	5
Thermal con. K [W/cm.K]	1.5	0.5	4.9	4.9	4.9	1.3	20
Thermal Exp coeff. [$10^{-6}/\text{K}$]	2.6	5.73	3	4.5	4.5	5.6	0.8
Density [g/cm^3]	2.3	5.3	3.2	3.2	3.2	6.1	3.5
Melting pt [$^\circ\text{C}$]	1420	1240	2830	2830	2830	2500	4000
Direct/Indirect band gap	I	D	I	I	I	D	I

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

The different polytypes differ only in the stacking order of double layers of Si and C atoms, however, this leads to them having very different electronic and optical properties. In a review article by Philip G. Neudeck [26] a comparison has been made between different wide-band gap semiconductors as shown in Table 2.1. From the figures of merit such as band gap, critical electric field and saturation velocity, one may see that SiC is only surpassed by diamond and GaN in performance in terms of ability to operate at extremely high temperatures, at high frequency and ability to sustain high breakdown voltages with very low specific on resistance. However, in the case of diamond the known dopants have energy levels that are much deeper in the band gap than those in SiC, which would make room temperature operation of diamond devices very inefficient. While over the years GaN has been slowly gaining popularity, the advantage of SiC over GaN lies in its ability to form a good native oxide as passivation and gate dielectrics as well as availability of large area substrates, mature epitaxial growth techniques and device processing technology. As is clear from the table, 4H-SiC's substantially higher carrier mobility compared to 6H-SiC render it the polytype of choice for most SiC electronic devices. Furthermore, the inherent mobility anisotropy that degrades conduction parallel to the crystallographic c-axis in 6H-SiC will particularly favor 4H-SiC for vertical power devices [3].

Ever since the first one-inch diameter 6H-SiC wafers became available commercially in 1990, there has been a tremendous pace of development in SiC semiconductor device technology. Wafers of 6H-SiC and 4H-SiC are commercially available with an increased diameter of up to 4-inch in 2006. A range of SiC based electronic products are also available commercially, which include microwave amplifier and a power diode by CREE; a Schottky barrier diode for AC-AC and DC-DC converters by Infineon; a low loss diode switch by ABB Semiconductor and a microwave transistor for radar by Northrop Grumman.

2.3 Ohmic Contact Formation on SiC

Ohmic contacts are electrical connections between a metal and a semiconductor which exhibit linear current-voltage (I - V) characteristics with low resistance. Metal-semiconductor (M-S) combinations generally upon preparation are not ohmic but instead rectifying, especially for wide band gap semiconductors such as SiC. Ohmic contacts may be considered a limiting case of the more general class of Schottky contacts. A metal-semiconductor combination that upon preparation has Schottky characteristics can be converted into an ohmic contact with certain processing steps such as alloying at high temperature that modify the Schottky barrier. Although there are metal-semiconductor combinations which are ohmic as prepared, these too have a Schottky barrier at the metal-semiconductor interface which is either too low or too thin to produce an asymmetric I - V characteristic. Low resistance n-type ohmic contacts to SiC are predominately fabricated by annealing a refractory metal (Ni, Pt, Ti etc.), thereby forming a silicide with a lowered Schottky barrier height at the metal-SiC interface. P-type contacts on the other hand generally use Al or Al alloys (Al-Ti) which upon annealing enable Al to diffuse into the SiC thus resulting in ohmic properties since Al acts as p-type dopant. Table 2.2 summarizes ohmic contact data reported on n-type α -SiC (4H-, 6H-) [27-30]. Contacts have been deposited on SiC with a wide range of doping concentrations and processed under a variety of conditions. Reported specific contact resistances vary between 1×10^{-6} and $1 \times 10^{-2} \Omega\text{-cm}^2$.

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

Table 2.2 Ohmic contacts on n-type α (6H or mixed)-SiC.

Metallization	Deposition Method	Annealing Conditions	$r_c(\Omega \text{ cm}^2)$	SiC carrier Conc.(cm^{-3})	Method of r_c meas.
Cr	melting	melting ($>2130^\circ\text{C}$)	N.R	N.R	-
Ni	e-beam evap.	$1000^\circ\text{C}/20 \text{ s}$	1.7×10^{-4}	4.5×10^{17}	TLM
TiN	ion-assisted e-beam evap.	$600^\circ\text{C}/30 \text{ min}$	4×10^{-2}	$\sim 1 \times 10^{18}$	TLM
TiW	sputtering	O_2 plasma + $600^\circ\text{C}/5 \text{ min}$	7.8×10^{-4}	4.7×10^{18}	Circular TLM
Ni	e-beam evap.	$950^\circ\text{C}/5 \text{ min}$	mid 10^{-2}	4.7×10^{18}	4-pt probe
Ni-Cr (60/40 wt%)	sputtering	$950^\circ\text{C}/5 \text{ min}$	1.8×10^{-3}	4.7×10^{18}	Circular TLM
W	thermal evap.	1200 to 1600°C	5×10^{-3} to 1×10^{-4}	3×10^{18} to 1×10^{19}	4-pt probe
TiW	sputtering	$750^\circ\text{C}/5 \text{ min}$	8×10^{-4}	7 to 8×10^{18}	Circular TLM
Ti	thermal evap.	none	1×10^{-4} to $< 2 \times 10^{-5}$	2×10^{18} to 1×10^{20}	Circular TLM
Mo	sputtering	none	$\sim 1 \times 10^{-4}$	$> 1 \times 10^{19}$	4-pt probe & TLM
Ta	sputtering	none	$\sim 1 \times 10^{-4}$	$> 1 \times 10^{19}$	4-pt probe & TLM
Ni/3C-SiC	resistive evap.	$1000^\circ\text{C}/30 \text{ s}$	$< 1.7 \times 10^{-5}$	1 to 2×10^{18}	Cox and strack
Ni	e-beam evap.	$950^\circ\text{C}/2 \text{ min}$	$< 5 \times 10^{-6}$	7 to 9×10^{18}	TLM
Ni	sputtering	$1050^\circ\text{C}/5 \text{ min}$	10^{-3} to 10^{-4}	9.8×10^{17}	TLM
W/Ti/Ni	thermal evap.	$1050^\circ\text{C}/5 \text{ min}$	10^{-3} to 10^{-4}	9.8×10^{17}	TLM
Ni	thermal evap.	$1000^\circ\text{C}/5 \text{ min}$	1×10^{-6}	4.5×10^{20}	Contact area
Ti-Al	thermal evap.	$1050^\circ\text{C}/5 \text{ min}$	$< 1 \times 10^{-3}$	4.5×10^{20}	Contact area
TiC	CVD; 1260°C	etched at 1300°C for 15 min in H_2	1.3×10^{-5}	4.0×10^{19}	TLM

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

The Ni/6H-SiC system has been characterized electrically and physically by Crofton *et al.* [31]. Specific contact resistances of $< 5 \times 10^{-6} \Omega\text{-cm}^2$ were measured following 2 min/950°C vacuum anneals of Ni layers deposited on epilayers with doping concentrations of between 7 and $9 \times 10^{18}/\text{cm}^3$. Physical characterization using Rutherford backscattering spectrometry (RBS) and Auger electron spectroscopy (AES) showed that during the anneal cycle, Ni and SiC react to form Ni_2Si with movement of C away from the interface during formation of the silicide [31]. The choice of metal for the formation of silicide ohmic contacts to n-type material is not limited to Ni. Other metals including Co, Pt, and Ta have been shown to form silicides with physical and electrical properties similar to those of nickel silicide [32]. Platinum's beneficial properties include its refractory nature with high melting point and oxidation resistance.

2.4 Schottky Contacts on SiC and SBDs

In this section, we will discuss the interface physics and band alignment after a metal comes in contact with semiconductor, the current density-voltage relationship for a SBD and ways to extract some key performance parameters for a SBD. We also review some literature results of schottky barrier heights formed on 4H-SiC using various metals.

2.4.1 Schottky Contact Interface Physics

When a metal and a semiconductor are brought into contact, their respective Fermi-levels must coincide in thermal equilibrium as shown in Fig. 2.3(b). There are two limiting cases, an ideal case referred to as Schottky-Mott limit and a practical case known as the Bardeen limit, that describe the characteristics of the metal-semiconductor contact [33]. Fig. 2.3(b) shows the energy band diagram for the ideal case (Schottky-Mott limit) with the absence of surface states.

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

In this case the barrier height for n-type semiconductor (ϕ_{Bn}) is the difference between the metal work function (ϕ_M) and electron affinity (χ_s) of the semiconductor given as follows,

$$q\phi_{Bn} = q(\phi_M - \chi_s) \quad (2-1)$$

Fig. 2.3 Energy band diagram for the ideal case (Schottky-Mott limit) with the absence of surface states a) metal and semiconductor separated by large distance b) metal and semiconductor in intimate contact.

For a given semiconductor and a metal, the sum of the barrier height on n- (ϕ_{Bn}) and p-type (ϕ_{Bp}) semiconductor is expected to be equal to the energy bandgap.

$$q(\phi_{Bn} + \phi_{Bp}) = E_g \quad (2-2)$$

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

This relationship for Schottky-Mott limit implies that the control of the barrier height is achieved by the choice of the metal. Experimentally, however, it is found that Schottky diodes formed on many of the III-V semiconductors do not show this behavior. Thus, the Schottky limit is not a complete description of all metal-semiconductor interfaces. Recent evidence for SiC suggests that SiC approximates Schottky behavior with most metals [3, 33].

Fig. 2.4 Band diagram for a non ideal metal-semiconductor interface under forward bias V .

An insulating layer of thickness δ exists between the metal and semiconductor and surface states are filled to the level ϕ_o .

The second limiting case is the Bardeen limit where a large density of states is present at the semiconductor-metal interface as depicted in Fig. 2.4. In the Bardeen limit the

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

barrier height (ϕ_B) is completely independent of the metal work function (ϕ_M), in contrast to the Schottky-Mott limit and the Fermi level is pinned by the high density of surface states [33]. Surface states are electronic states localized at the surface of the semiconductor crystal produced by the interruption of the perfect periodicity of the crystal lattice. The states can be occupied or empty depending on their position in energy relative to the Fermi level at the surface. We may define a neutral level (ϕ_O) as the energy level (measured relative to the valence band) to which the surface states are filled when the surface is neutral. If the states are filled to energy greater than ϕ_O , the surface possesses a net negative charge and the states are acceptor-like in behavior; if the states are filled to a level below ϕ_O , the surface has a net positive charge and the states behave in a donor-like manner. The parameter ϕ_O is convenient in describing surface states and its value depends on the particular surface under consideration. Assume that a thin insulating layer separates the metal from the semiconductor, and the layer is thin enough to be transparent to electron flow but yet can withstand a potential difference across it. If the number of surface states is large, then the Fermi level at the surface of the semiconductor will be at ϕ_O . The potential difference $\phi_M - \phi_S$ will appear entirely across the interfacial layer since the charge in the surface states will fully accommodate the necessary potential difference. Thus, no change in the charge within the depletion region of the semiconductor is necessary when a metal is brought into contact with the semiconductor. Hence, ϕ_B is independent of ϕ_M , E_{FS} at the surface of the semiconductor is the same as the Fermi level in the metal E_{FM} , and we obtain the Bardeen limit barrier height as,

$$q\phi_B = q(E_g - \phi_O) \quad (2-3)$$

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

In general the barrier energy ϕ_B will be somewhere between the Schottky limit and the Bardeen limit. Cowley and Sze [34] were the first to analyze the general case accounting for both surface states and work functions. Consider the metal-semiconductor interface shown in Fig. 2.4, where the semiconductor is n-type. It can be shown from their results that ϕ_B^0 , the barrier energy with no electric field inside the semiconductor (i.e., the flat-band condition), is given by

$$\phi_B^0 = \gamma(\phi_M - \chi_s) + (1 - \gamma)(E_g - \phi_0) \quad (2-4)$$

$$\gamma = \epsilon_i / (\epsilon_i + q\delta D_s) \quad (2-5)$$

where q is the electronic charge, ϕ_M the metal work function, χ_s the semiconductor affinity, E_g the semiconductor energy gap, ϕ_0 the interface neutrality level which determines the magnitude of charge transfer and the resulting interface dipole, δ the thickness of the interfacial region between the metal and the semiconductor and ϵ_i the dielectric permittivity of the interfacial region. The parameter γ accounts for the slope of the ϕ_B vs. ϕ_M curve. Eqn. (2-1) and (2-3) are limiting cases of this relation. The dimensionless parameter γ varies between zero and unity, depending primarily on the density of surface states. If $q\delta D_s \ll \epsilon_i$, then $\gamma \sim 1$ and this equation reduces to the Schottky limit. If $q\delta D_s \gg \epsilon_i$, then $\gamma \ll 1$ and this equation reduces to the Bardeen limit.

2.4.2 Current Density-Voltage Relationship for SBD and Parameter Extraction.

Using the ideal thermionic emission theory, it can be shown that application of a voltage to a Schottky diode will yield a current density-voltage (J - V) characteristics that is given by [33]

$$J = J_s \left[\exp \left(\frac{q(V - JR_{on})}{\eta kT} \right) - 1 \right] \quad (2-6)$$

$$J_s = A^{**} T^2 \exp \left[\frac{-q\phi_B}{kT} \right] \quad (2-7)$$

where A^{**} is the effective area Richardson's constant, R_{on} is the series on resistance, ϕ_B refers to the barrier height, η is the ideality factor, k is the Boltzmann's constant, T is the temperature.

The series resistance R_{on} can be obtained by differentiating V with respect to $\ln J$ to obtain

$$\frac{\delta V}{\delta(\ln J)} = R_{on} J + \frac{\eta kT}{q} \quad (2-8)$$

Thus the series resistance can be obtained from the plot of $\frac{\delta V}{\delta(\ln J)}$ vs. J in the region of high current density.

In a region where J is very small, effect of R_{on} can be neglected and eqn. (2-6) is reduced to

$$J = J_s \left[\exp \left(\frac{qV}{\eta kT} \right) - 1 \right] \quad (2-9)$$

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

Therefore the barrier height ϕ_B can be obtained from the y-intercept of the $\ln J$ vs. V curve where the effective area-Richardson's constant A^{**} is $146 \text{ Acm}^{-2}\text{K}^{-2}$ for 4H-SiC [3]. For V much larger than kT/q the exponential term dominates and we have

$$J = J_s \left[\exp \left(\frac{qV}{\eta kT} \right) \right] \quad (2-10)$$

Thus the ideality factor (η) can be determined from the slope of the $\ln J$ vs. V curve as given by

$$\eta = \frac{q}{kT \left(\frac{\delta V}{\delta (\ln J)} \right)} \quad (2-11)$$

2.4.3 Schottky Barrier Heights on 4H-SiC

There have been several reports on the metal/4H-SiC systems [35-37]. Itoh and Matsunami [35] measured the barrier heights of several metals (Au, Ni, and Ti) to 4H-SiC (n-type) by I - V , C - V characterization. Undoped epilayers ($10 \text{ }\mu\text{m}$) grown by step-controlled epitaxy on substrates with a donor concentration of $1.0 \times 10^{18} / \text{cm}^3$ were used for the samples. The donor concentration N_D in the epilayer estimated from C - V characteristics was 7.0×10^{15} to $4.0 \times 10^{16} / \text{cm}^3$. Schottky contacts were formed by thermal evaporation through a shadow mask. Using the ideal thermionic emission theory, barrier heights of 1.73 eV (Au), 1.62 eV (Ni), and 0.95 eV (Ti) for Si-faces, and 1.80 eV (Au), 1.60 eV (Ni), and 1.16 eV (Ti) for C-faces were calculated. Note that there are differences in the barrier heights between Si- and C-faces, and the barrier heights for C-faces are in general 0.1 to 0.3 eV larger than those for Si-face. Almost all barrier heights obtained for Au, Ni, and Ti from C - V characteristics were about 0.1 to 0.3 eV larger than those deduced from I - V characteristics for both Si- and C-faces. C - V characteristics are affected by series resistances and the presence of a thin

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

interfacial oxide-like layer between the Schottky metal and the semiconductor. The real bias voltage applied to the depletion layer deviates from the measured voltage and is usually lower. Thus the barrier heights are larger than the actual values estimated from C - V characteristics [38].

2.5 Edge Termination Techniques for High Voltage SiC Devices

For high voltage Schottky diodes to reach the ideal parallel plane breakdown voltage, it is necessary to have an edge termination around the periphery of the diodes to reduce electric field crowding at the diode edge. Several techniques of edge terminations have been shown to reduce the electric field crowding, resulting in higher breakdown voltages for Schottky diodes.

Fig. 2.5 6H-SiC SBDs using a) FMR and b) RESP from Bhatnagar *et al.* [39].

M. Bhatnagar *et al.* [39] reported a study on floating metal rings (FMR) (see Fig. 2.5(a)) and resistive Schottky barrier field plate (RESP) (see Fig. 2.5 (b)) for 6H-SiC Schottky barrier diodes. For FMR diodes a breakdown in excess of 400 V was obtained

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

using a 3-ring termination with ring spacing of $0.8\ \mu\text{m}$ in comparison to 220 V obtained for an unterminated device. For the RESP device it consists of a thin layer of Ti oxidized in air to control the sheet resistance between $1\ \text{K}\Omega/\text{sq}$ to $10\ \text{M}\Omega/\text{sq}$. The breakdown voltage was increased to 500V for a $100\ \mu\text{m}$ RESP at $1\ \text{M}\Omega/\text{sq}$ [39].

K. Ueno *et al.* [40] reported p-epi guard ring (see Fig. 2.6 (a)) formed by a local oxidation process (LOCOS). The n-drift region and p-type region, which form the guard-ring in completion, were grown by the chemical vapor deposition (CVD) technique at 1500°C on C-face 6H-SiC sublimation wafers. The doping concentration and thickness were $1.3 \times 10^{16}/\text{cm}^3$ and $4.7\ \mu\text{m}$ respectively for the n-drift region, and $7 \times 10^{16}/\text{cm}^3$ and $0.9\ \mu\text{m}$ respectively for the p-region. A breakdown voltage in excess of 550 V was obtained in comparison to approximately 200 V for diodes without a guard ring (see Fig. 2.6 (b)).

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Fig. 2.6 (a) Schematic of Schottky diodes with p-epi guard ring formed by LOCOS process
(b) breakdown J - V characteristics for the same structure [40].

Alok and Baliga [41] investigated an edge termination with a resistive layer created by high dose argon (Ar^+) ion implantation, resulting in close to the ideal parallel plane

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

breakdown voltage (see Fig. 2.7 (a)). Other groups [42, 43] also investigated similar edge termination using boron (B+) implantation (see Fig. 2.7 (b)) for higher resistive regions at the edge to improve the reverse breakdown voltage. Schottky rectifiers formed by Ar+ implantation to form highly resistive amorphous layers at the periphery of the Schottky contacts showed large leakage current density even at low reverse bias voltages ($5 \times 10^{-2} \text{ A/cm}^2$ at 100 V), which may result from severe implant damage in the implanted edge-layers. This would cause high power losses during turn-off. However, by using highly resistive crystalline layers formed by B+ implantation and subsequent annealing to form edge termination for the Schottky rectifiers, high breakdown voltages over 1100 V have been achieved between temperatures of 24°C and 150°C.

Fig. 2.7 Edge Terminations of SiC SBDs using a) High resistive region using Ar implantation [41], b) Using a p- doped guard ring using B+ implantation [42].

In a study carried out by D.J. Morrison *et al.* [44] the effects of post-implantation annealing on the electrical characteristics of Ni 4H-SiC Schottky barrier diodes terminated using self-

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

aligned Ar^+ ion implantation was investigated. Low temperature (400-700°C) annealing was shown to increase the equivalent resistance of the edge termination by two orders of magnitude without significantly affecting the breakdown voltage. The leakage currents were shown to be substantially reduced. V. Saxena *et al.* [10] also reported improved breakdown voltage with oxide field plate termination with the structure shown in Fig. 2.8(a). The Ni/4H-SiC diodes fabricated in this study typically had breakdown voltages of 1000 V (47% of ideal punch through), with some diodes achieving as high as 1200 V. In another work related to oxide field plate (FP) terminated p-type 4H-SiC SBDs, Tarplee M *et al.* [45] suggested a design rule for FP oxide optimal thickness equal to $t_{\text{epi}}/20$ where t_{epi} is the epilayer thickness. Thus based on their work and as seen in Fig. 2.9, for an epilayer thickness of 10 μm , the optimal FP oxide thickness will be roughly around 0.5 μm

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Fig. 2.8 Edge Termination using Oxide Field plate from V. Saxena *et al.* [10].

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

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Fig. 2.9 Relationship between breakdown voltage and Field Plate oxide thickness for doping

$$N_A = 1 \times 10^{16} / \text{cm}^3 \text{ [45].}$$

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Fig. 2.10 Schematic cross-sections of Schottky diode structures with (a) single-zone and (b)

double-zone JTE [46].

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

Among other edge termination techniques we have the junction termination extension (JTE). A JTE terminated Schottky device on n-type material employs a moderately p-doped ring, which surrounds the metal contact and is electrically connected to it as shown in Fig. 2.10 (a). A Mahajan *et al.* [46] analyzed single- and double-zone junction termination extension (JTE) structures for 4H-SiC Schottky diodes using numerical simulations. The disadvantage of an optimal JTE design is that it requires precise control of the sheet density of dopants in the JTE layer to achieve the desired breakdown characteristics. In this type of structure, breakdown can occur either near the boundary between the end of the metal contact and the JTE region (point A in Fig. 2.10 (a)) or near the end of the JTE region (point B in Fig. 2.10 (a)). Optimization consists of obtaining simultaneous breakdown in these two regions. It was found that the single-zone JTE can yield high breakdown voltages if the activated JTE dose is controlled precisely. Using double-zone JTE (see Fig. 2.10 (b)), greater tolerance with respect to JTE dose and dopant activation can be achieved as compared to single-zone JTE

Fig. 2.11 Reverse leakage current characteristics of JTE and Floating guard rings terminated 4H-SiC PiN diodes with and without FP [11].

In another development and as seen in Fig. 2.11, Raúl Pérez *et al.* [11] saw a great improvement in reverse leakage currents and an improvement in breakdown voltages of their JTE terminated 4H-SiC PiN diodes with additional SiO₂ FP terminations. This again shows the usefulness of FP termination and the way it beautifully complements other termination techniques such as guard rings and JTE to improve the breakdown voltages and reduce leakage currents by reducing the extreme surface fields.

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Fig. 2.12 Reverse leakage of passivated and unpassivated diodes [11].

In the same study and as shown in Fig. 2.12, for PiN diodes without FP and using only JTE terminations, a primary layer of SiO₂ passivation helped tremendously to increase the avalanche breakdown voltage and improve the blocking voltages of these devices. This further reinforces the idea that primary layer of passivation in form of a FP is needed to achieve best blocking voltage capabilities in these high voltage rectifiers.

There is an important family of Schottky diodes known as Junction Barrier Schottky (JBS), which is truly revolutionary. Schottky barrier diodes have a tendency to show much softer reverse breakdown characteristics than p-n junction diodes in a given semiconductor system. This is due to the lower barrier height of the Schottky contact as compared to the built-in potential in a p-n junction diode and the lowering of Schottky barrier height under reverse bias. To achieve a combination of superior blocking performance of a p-n junction

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

diode with the low forward voltage drop of a Schottky diode, Baliga [47] proposed the JBS diode structure, which was first demonstrated in 1984 in Si diodes. The JBS diode consists of an interconnected grid of implanted p-wells in the n- drift layer, sitting just beneath the Schottky contact. The p-n junctions pinch off the current flow in the intervening space between the p-wells under reverse bias. As the p-n junctions pinch off, they effectively form a p-n junction diode, which screens the lower barrier height of the Schottky barrier junction. Under the forward bias operation, the implanted p-wells are simply inactive because the Schottky barrier metal does not form an ohmic contact to the implanted p-type grid, and the forward voltage drop is governed by the properties of the Schottky barrier rather than the implanted p-n junction.

Fig. 2.13 a) Schematic cross section of a 10 kV 4H-SiC JBS diode, (b) Reverse blocking characteristics of a 0.88-cm² 10 KV JBS diode at different temperatures [48].

The same concept of JBS has been used by researchers at Cree in demonstrating a 10 KV 4H-SiC junction barrier Schottky (JBS) diodes [48]. It is now possible to replace PiN

Chapter 2 SiC Material Properties and Metal-Semiconductor Contacts

diodes with these 4H-SiC SBDs for 10 KV inverter modules that can switch at 20 KHz. With recent technological advancements, growth of high quality, low defect densities and high growth rate 4H-SiC epitaxial layers needed for these very high voltage devices [49, 50] is now possible, with thick ($> 100 \mu\text{m}$) epitaxial layers and low doping densities ($N_d < 9 \times 10^{14}/\text{cm}^3$) demonstrated. Figures 2.13 (a) and (b) show the structure of their 10 KV 4H-SiC JBS diodes and the reverse blocking characteristics of these diodes respectively. As implemented in SiC, the JBS diodes in this study consist of an interconnected grid of boron or aluminum ion-implanted wells. The diodes have been fabricated by first implanting aluminum in a gridded pattern across the active area of the wafer to provide the p-n junction barrier of the JBS diode. The diodes were then terminated with a boron-implanted JTE. The implanted boron was then activated using annealing at 1650°C after which the surface of the diodes was passivated with SiO_2 . A backside ohmic contact was deposited and annealed. Windows were then opened over the diodes, into which the Ni Schottky metal and, subsequently, an Al overlayer were deposited to form an additional FP termination.

2.6 Conclusions

In conclusion, in this chapter we presented some basic background information of SiC, its material and electronic properties and its crystallographic structures for different polytypes. We discussed some techniques used to form ohmic contact formation on SiC which is primarily by silicidation using high temperature annealing. We also discussed some physics behind metal-semiconductor Schottky contacts, origin of barrier height pinning through the Bardeen's model and the electronic current-density relationship for a Schottky diode. We discussed ways of extracting the Schottky diode parameters such as barrier height, ideality factor and on resistance. Finally we reviewed some literature on Schottky barriers formed on 4H-SiC using various metals and edge termination strategies commonly used for high voltage 4H-SiC Schottky barrier diodes.

Chapter 3

Numerical Simulations of 4H-SiC Schottky Barrier Diodes

Numerical simulations of devices are useful for analytical and predictive purposes. They allow a rather realistic insight into electronic devices without the need to actually manufacture such devices. Various physical parameters and phenomena can be analyzed at any location inside the devices. This greatly reduces time and cost in semiconductor research and development, and enriches understanding of device physics.

The simulator used in this work is Medici^{TM} from Synopsis [51]. Medici is a powerful device simulator program that can be used to simulate behavior of MOS, bipolar transistors, diodes and other semiconductor devices. It models the two-dimensional distribution of potential and carrier concentrations in a device. The program solves the Poisson's equation and both electron and hole continuity equations and can be used to predict the electrical characteristics of devices under any bias conditions. Medici uses a non-uniform simulation grid and can model arbitrary device geometries with both planar and non-planar surface topologies. A number of models can be incorporated into the program for accurate simulations, which include band-gap narrowing, carrier recombination, impact ionization, mobility, lifetime etc. Medici also incorporates both Boltzmann and Fermi-Dirac statistics, and takes into account incomplete ionization of impurities.

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

In this chapter we begin by examining the fundamental equations solved by Medici, the electrical models and parameters used to perform the numerical simulations. Later in the chapter we will present the results of our numerical simulations using Medici for various 4H-SiC SBD structures, focusing primarily on FP termination.

3.1 Physics of Numerical Simulations

As will be explained in subsequent section, a simple framework of fundamental equations or equation assembly models (EAS Models) are solved by the simulator. These models define the basic structure of the equation system determined by drift-diffusion or hydrodynamic transport. To account for physical effects the EAS models use the so-called physical models, which calculate material properties depending on temperature, electric field and so forth.

The primary function of Medici is to solve the three partial differential equations (eqn. (3-1), (3-2), and (3-3)) self-consistently for the electrostatic potential ψ and for the electron and hole concentrations n and p , respectively. The Poisson's equation to be solved is given by

$$\epsilon \nabla^2 \psi = -q(p - n + N_D^+ - N_A^-) \quad (3-1)$$

where ψ is the intrinsic Fermi potential, N_D^+ and N_A^- are the ionized donor and acceptor impurity concentrations. The electron and hole concentrations n and p are in turn governed by the continuity equations given by

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

$$\frac{\delta n}{\delta t} = \frac{1}{q} \vec{\nabla} \cdot \vec{J}_n - U_n + G_n \quad (3-2)$$

$$\frac{\delta p}{\delta t} = -\frac{1}{q} \vec{\nabla} \cdot \vec{J}_p - U_p + G_p \quad (3-3)$$

where U_n and G_n represent the rates of electrons recombination and generation, while U_p and G_p represent the corresponding rates for holes. The terms J_n and J_p represent the electron and hole current densities respectively. The eqn. (3-2) and (3-3) can be simplified and written as functions of ψ , n and p , consisting of drift and diffusion components,

$$\vec{J}_n = q\mu_n \vec{E}_n n + qD_n \vec{\nabla} n \quad (3-4)$$

$$\vec{J}_p = q\mu_p \vec{E}_p p - qD_p \vec{\nabla} p \quad (3-5)$$

In the above, D_n and D_p are the electron and hole diffusivity while $\vec{E}_n$ and $\vec{E}_p$ are electric field experienced by electron and holes respectively. Neglecting band gap narrowing and assuming Boltzmann carrier statistics we have

$$\vec{E}_n = \vec{E}_p = \vec{E} = -\vec{\nabla} \psi \quad (3-6)$$

3.2 Physical Models for 4H-SiC Simulations

In this section we will describe the various physical models used for our simulations and also specify the model parameters specifically being used for 4H-SiC.

3.2.1 Recombinations

The terms U_n and U_p in eqn. (3-2) and (3-3) represent net electron and hole recombination, respectively. That is

$$U = U_n = U_p = U_{SRH} + U_{Auger} \quad (3-7)$$

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

where U_{SRH} and U_{Auger} represent Shockley-Read-Hall and Auger recombinations respectively. The Shockley-Read-Hall recombination rate is given by

$$U_{SRH} = \frac{pn - n_{ie}^2}{\tau_p [n + n_{ie} \exp(\frac{ETRAP}{KT})] + \tau_n [p + n_{ie} \exp(-\frac{ETRAP}{KT})]} \quad (3-8)$$

In the above equation, n_{ie} is the effective intrinsic carrier concentration, τ_n and τ_p are the electron and hole lifetimes respectively, which are concentration dependent. The parameter $ETRAP$ represents the difference between the trap energy levels E_t and the intrinsic energy E_i . Auger recombination occurs at a high level of doping due to direct band-to-band recombination between an electron and hole across the band gap, accompanied by a transfer of energy to another free electron or hole.

$$U_{Auger} = AUGN(pn^2 - nn_{ie}^2) + AUGP(np^2 - pn_{ie}^2) \quad (3-9)$$

where the Auger coefficients for electrons and holes for 4H-SiC are $AUGN = 5 \times 10^{-31} \text{ cm}^{-6} \text{ s}^{-1}$ and $AUGP = 2 \times 10^{-31} \text{ cm}^{-6} \text{ s}^{-1}$ respectively [52].

3.2.2 Lifetimes

The electron and hole lifetimes are concentration dependent, and are given by

$$\tau_n(x, y) = \frac{TAUN0}{1 + \frac{N_{total}(x, y)}{NSRHN}} \quad (3-10)$$

$$\tau_p(x, y) = \frac{TAUP0}{1 + \frac{N_{total}(x, y)}{NSRHP}} \quad (3-11)$$

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

where N_{total} refers to the total dopant concentration which is basically a sum of n-type and p-type dopants. The terms τ_n and τ_p are electron and hole lifetimes. The other terms refer to constants which for 4H-SiC, the parameters used are given by $TAUN0 = 1.0 \times 10^{-7}$ sec, $NSRHN = 5.0 \times 10^{16} / cm^3$, $TAUP0 = 1.0 \times 10^{-7}$ sec and $NSRHP = 5.0 \times 10^{16} / cm^3$ for holes [53].

3.2.3 Intrinsic Carrier Concentration n_{ie}

The electronic band structure and effective masses in SiC are complex because of several non-parabolic bands in the reciprocal k-space. But for operational range of our devices we can assume Boltzmann's statistics for carrier concentration that is given by

$$n_{ie}(T) = \sqrt{N_c(T)N_v(T)} e^{\frac{-E_g}{2KT}} \quad (3-12)$$

where n_{ie} is the intrinsic carrier concentration, E_g is the band gap of SiC, N_c and N_v are the conduction and valence band density of states for SiC. For our simulations the room temperature values of N_c and N_v are taken from the reference [3, 54] and are equal to $1.689 \times 10^{19} / cm^3$ and $2.494 \times 10^{19} / cm^3$ respectively. The intrinsic carrier concentration in 4H-SiC is extremely low due to its wide band gap as a result of which SiC devices can operate up to very high temperatures.

3.2.4 Band Gap

The band gap of 4H-SiC and its dependence on temperature are given as follows,

$$E_g(T) = E_g(0) - \frac{EGALPH(T^2)}{T + EGBETA} \quad (3-13)$$

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

$$E_g(T) = E_g(300) + EGALPH \left[\frac{300^2}{300 + EGBETA} - \frac{T^2}{T + EGBETA} \right] \quad (3-14)$$

The room temperature band gap parameters for 4H-SiC are given by [55] where we have $E_g(300) = 3.26$ eV, $EGALPH = 4.59 \times 10^{-4}$ eV/K and $EGBETA = 530$ K.

3.2.5 Bandgap Narrowing

At high levels of doping carrier-carrier interaction, carrier-impurity interaction and overlap of electron wave functions can cause spatial variation of bandgap. As a result the bandgap decreases as doping increases. This bandgap narrowing effect has not been measured for SiC but only theoretically studied for different polytypes of SiC by Pearson *et al.* [56] and U. Lindefelt [57]. Generally a model which is valid for Si as given below is used for the simulation of SiC devices.

$$\Delta E_g = \frac{9.0 \times 10^{-3} q}{2KT} \left[\ln \frac{N_{total}(x, y)}{1.0 \times 10^{17}} + \sqrt{\left(\ln \frac{N_{total}(x, y)}{1.0 \times 10^{17}} \right)^2 + 0.5} \right] \quad (3-15)$$

$$n_{ie}(x, y) = n_i \exp(\Delta E_g) \quad (3-16)$$

3.2.6 Incomplete Ionization

In the case of 4H-SiC the energy levels of the dopants are much deeper and as a result the dopants are not fully ionized in SiC even at room temperature. This phenomenon, which occurs in Si but only at very low temperatures, is known as dopant freeze-out. The ionization energies of commonly used dopant atoms in SiC are shown in Table 3.1.

Table 3.1 Dopants in SiC and their ionization energy with the lattice site.

Type	Dopants	Ionization Energies		
		4H-SiC (meV)	6H-SiC (meV)	Si
N-type (Donors)	Nitrogen	42 (hex), 84 (cub)	82 (hex), 137 (cub)	45
	Phosphorous	53 (hex), 93 (cub)	82 (hex), 115 (cub)	45
P-type (Acceptors)	Boron	285	300	45
	Aluminium	191	210	67
	Gallium	281	290	72

Al (substituting Si site) and N (substituting C site) are the most commonly used acceptor and donor impurities for SiC respectively. Doping with nitrogen (N) leads to a donor with two different energy levels below the conduction band due to the existence of two different lattice sites, one with cubic surrounding and the other with hexagonal surrounding. Nevertheless, for actual simulations these two donor levels can be lumped together and replaced by a single level [58].

The ionization rate is given by [59]

$$I_D = \frac{N_D^+}{N_D} = \frac{-1 + \sqrt{1 + 4g_c \frac{N_D}{N_C} \exp\left(\frac{E_C - E_D}{kT}\right)}}{2g_c \frac{N_D}{N_C} \exp\left(\frac{E_C - E_D}{kT}\right)} \quad (3-17)$$

where $E_C - E_D$ is the energy difference between the conduction band minimum and the donor level while N_D^+ is the number of ionized donors. For the donor levels of 4H-SiC at 300 K, $E_C - E_D$ is 66 meV [59] with a donor degeneracy factor $g_c = 2$ and the effective density of states $N_C = 1.689 \times 10^{19} / \text{cm}^3$ [3, 54]. The shallowest p-type doping can be

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

achieved using Al acceptors with $E_A - E_V = 191$ meV for 4H-SiC and $g_c = 4$. In the case of Ga, $E_A - E_V = 281$ meV [59].

3.2.7 Mobility

The carrier mobilities, μ_n and μ_p , of electrons and holes respectively account for scattering mechanisms in electrical transport. The concentration and temperature dependence of μ_n and μ_p at low electric field E referred to as μ_n^0 and μ_p^0 can be described using an analytical expression derived empirically as given below

$$\mu_n^0 = \text{MUN.MIN} + \frac{\text{MUN.MAX} \left(\frac{T}{300} \right)^{NUN} - \text{MUN.MIN}}{1 + \left(\frac{T}{300} \right)^{XIN} \left(\frac{N_{total}(x, y)}{NREFN} \right)^{ALPHAN}} \quad (3-18)$$

$$\mu_p^0 = \text{MUP.MIN} + \frac{\text{MUP.MAX} \left(\frac{T}{300} \right)^{NUP} - \text{MUP.MIN}}{1 + \left(\frac{T}{300} \right)^{XIP} \left(\frac{N_{total}(x, y)}{NREFP} \right)^{ALPHAP}} \quad (3-19)$$

where for 4H-SiC $\text{MUN.MIN} = 0$ cm²/V.s, $\text{MUN.MAX} = 947$ cm²/V.s, $NREFN = 1.94 \times 10^{17}$ /cm³, $ALPHAN = 0.61$, $NUN = -2.15$ and $\text{MUP.MIN} = 15.9$ cm²/V.s, $\text{MUP.MAX} = 124$ cm²/V.s, $NREFP = 1.76 \times 10^{19}$ /cm³, $ALPHAN = 0.34$ and $NUN = -2.15$ [60].

The mobilities are more anisotropic for 6H-SiC than for 4H-SiC. The ratio between electron mobilities perpendicular and parallel to the c-axis are 0.83 for 4H-SiC and 5 for 6H-SiC [60]. The high electron mobilities in 4H-SiC and its low anisotropy favor the use of this

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

polytype. At high electric fields, the carriers drift velocity V saturates due to increased phonon scattering and reaches the saturation velocity V_{sat} . This field dependence of the mobilities can be modeled using Caughey-Thomas expression, which accounts for reduced mobility at high fields.

$$\mu_{n,p}(E) = \frac{\mu_{n,p}^o}{\left[1 + \left(\frac{\mu_{n,p}^o E}{V_{sat}}\right)^\beta\right]^{1/\beta}} \quad (3-20)$$

In the above $\mu_{n,p}^o$ is the low-field electron or hole mobility as defined by eqn. (3-18) and (3-19), $V_{sat} = 2 \times 10^7 \text{ cm/s}$ and $\beta = 2.0$ for 4H-SiC [61].

3.2.8 Impact Ionization

If the field across a metal-semiconductor (M-S) junction is high enough, impact ionization will occur since carriers can gain enough kinetic energy to knock off electron-hole pairs. Avalanche breakdown occurs when this process of carrier multiplication runs away, that is, when the multiplication factor becomes infinite. For a simple M-S junction we have the maximum electric field E_{max} occurring at the M-S interface and the corresponding depletion width W is given by [62]

$$E_{max} = \frac{qN_D W}{\epsilon_o \epsilon_r} \quad (3-21)$$

$$V = \frac{qN_D W^2}{2\epsilon_o \epsilon_r} \quad (3-22)$$

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

where ϵ_r is the relative permittivity of the semiconductor, which is equal to 9.7 for 4H-SiC [3] and V is the applied voltage. When the $E_{\max}$ reaches the critical electric field E_c of the semiconductor, breakdown occurs. E_c depends on the temperature and doping concentration of the semiconductor, and it also increases with the band gap of the semiconductor. The wider band gap of 4H-SiC gives rise to E_c which is close to 3 MV/cm, which is almost 10 times that of Si. Thus 4H-SiC devices can sustain much higher voltages over Si devices with identical doping and size.

For n-type 4H-SiC, at room temperature E_c can be easily calculated from an empirical relationship by Konstantinov *et al.* [63]

$$E_c = \frac{2.49}{1 - \left(\frac{1}{4}\right) \left(\log \frac{N_D}{1.0 \times 10^{16}} \right)} \text{ MV / cm} \quad (3-23)$$

A first principle method of estimating the breakdown voltage is based on calculating the generation rate of electron-hole pairs due to impact ionization using

$$G'' = \alpha_{n,II} \frac{\left| \vec{J}_n \right|}{q} + \alpha_{p,II} \frac{\left| \vec{J}_p \right|}{q} \quad (3-24)$$

where $\alpha_{n,II}$ and $\alpha_{p,II}$ are the electron and hole ionization coefficients respectively, and $\vec{J}_n$, $\vec{J}_p$ are the electron and hole current densities respectively. We also have

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

$$\alpha_{n,\parallel} = a_n \exp\left(\frac{-b_n}{E_{\parallel}}\right) \quad (3-25)$$

$$\alpha_{p,\parallel} = a_p \exp\left(\frac{-b_p}{E_{\parallel}}\right) \quad (3-26)$$

where $E_{\parallel}$ is the electric field component in the direction of current flow. For 4H-SiC we have $a_n = 7.33 \times 10^6 \text{ cm}^{-1}$, $b_n = 2.2 \times 10^7 \text{ V/cm}$ and $a_p = 3.5 \times 10^6 \text{ cm}^{-1}$, $b_p = 1.4 \times 10^7 \text{ V/cm}$ [63, 64].

The simulator evaluates the breakdown voltage of the device by evaluating the ionization integral given by eqn. (3-27) below, which is indirectly extracted from eqn. (3-24) to (3-26). At breakdown the ionization integral as given by left side of eqn. (3-27) exceeds unity.

$$\int_0^w \alpha_{n,\parallel} \exp\left[\int_0^w (\alpha_{n,\parallel} - \alpha_{p,\parallel}) dx\right] dx = 1 \quad (3-27)$$

3.3 Numerical Simulation of Ideal and Underminated 4H-SiC SBDs

Figures 3.1 (a) and (b) show the structure of the ideal and underminated 4H-SiC SBD used for numerical simulations using Medici^{TM}. The structure consists of a 10 μm epilayer doped n-type with nitrogen from a low-doped value of $N_D = 3 \times 10^{14} / \text{cm}^3$ to a high value of $1 \times 10^{17} / \text{cm}^3$. The substrate is highly doped n+ to a value of $6.8 \times 10^{18} / \text{cm}^3$. A backside ohmic contact has been formed to the substrate while a schottky contact with a diameter of 200 μm has been formed on the top of the epilayer using Pt metal with a barrier height close to 1.45 eV. By an ideal structure we mean a structure which offers no edges and its only

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

purpose is to evaluate the maximum possible breakdown voltage which can be achieved for that structure. In a practical device, a suitable termination technique is needed to minimize electric field enhancements at the schottky corner to achieve breakdown voltage close to the ideal value.

Fig. 3.1 Structural schematic of 4H-SiC SBD for a) an ideal structure b) an unterminated structure. Figure not exactly to the scale.

For the unterminated diodes, we assume the diode surface has been passivated using a thermal SiO_2 layer 20 nm thick, which generally helps to protect the schottky contacts in experimental devices from processing contaminations and reduce surface leakage currents due to moisture and environmental factors. To make the simulations more realistic we assume a nominal interface charge density $Q_F = +5 \times 10^{11} \text{ /cm}^2$ at the SiO_2 /4H-SiC interface [65].

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

Fig. 3.2 shows the simulated breakdown voltages for the above structures with different doping concentrations N_D . For the ideal diodes, as the N_D is reduced, V_B increases rapidly and finally saturates when N_D is below $1 \times 10^{16}/\text{cm}^3$. This is because for a low-doped epilayer with a thickness of $10 \mu\text{m}$, the depletion layer punch-through readily to the highly doped substrate under increasing applied voltage. When this happens, the electric field at the schottky interface increases rapidly and the breakdown voltage is clamped at around 2000 V.

Fig. 3.2 Simulated breakdown voltage for different doping for unterminated and ideal 4H-SiC SBD.

In comparison, the breakdown voltage is much higher for the ideal case with a thicker epilayer of $100 \mu\text{m}$. For example a device with $N_D = 2 \times 10^{15}/\text{cm}^3$ and epilayer thickness of $100 \mu\text{m}$ undergoes a breakdown at ~ 5720 V compared to 2040 V for the device with an

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

epilayer thickness of 10 μm . As seen from Fig. 3.2, the unterminated diodes show a much lower V_B compared to ideal V_B due to premature breakdown as a result of extreme electric field enhancement at the Schottky edges. The exact nature of this edge field enhancement and its implications will be apparent later on when we present the results on the electric field distribution for simulated unterminated diodes passivated using $\text{SiO}_2/\text{thermal-SiO}_2$ and $\text{AlN}/\text{thermal-SiO}_2$.

3.4 Numerical Simulation of Unterminated 4H-SiC SBDs With a Secondary Layer of Passivation.

We have simulated unterminated 4H-SiC SBDs with a secondary layer of deposited passivation. While a primary layer of thermal SiO_2 is enough to electrical passivate the device, it cannot protect the final device top layer metals and interconnect layers. A secondary layer of deposited passivation such as CVD SiO_2 is necessary to protect the top layer metals and also to reduce packaging stress. We also realize, the secondary layer of passivation has a direct impact on electric field enhancements at schottky corners. Thus replacing CVD SiO_2 with a higher k dielectric such as sputter deposited AlN would be quite beneficial in terms of reducing edge field enhancements which will lead to reduced leakage currents, improved breakdown voltage and better reliability.

Fig. 3.3 shows the structure of the SBD passivated using a secondary layer passivation which is either the conventional CVD SiO_2 or a higher k dielectric in form of sputter deposited AlN . A primary layer of thermal- SiO_2 was incorporated to serve as an intermediate layer to improve the conduction/valence band offset between the overlying AlN passivation and 4H-SiC. We have assumed a dielectric constant $k = 3.9$ with a nominal positive interface charge $Q_F = +5 \times 10^{11}/\text{cm}^2$ for the $\text{SiO}_2/\text{thermal-SiO}_2$ passivation and a

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

$k = 8.2$ with a negative interface charge of $Q_F = -5 \times 10^{11} / \text{cm}^2$ for the AlN/ thermal-SiO₂ passivation [66, 67].

Fig. 3.3 Structural schematic of 4H-SiC unterminated SBD with a secondary layer of passivation used for numerical simulation.

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

Fig. 3.4 Electric field distribution at reverse bias voltage of 580 V for unterminated 4H-SiC SBD with a layer of secondary passivation a) SiO₂/thermal-SiO₂ with $k=3.9$ and $Q_F = +5 \times 10^{11} / \text{cm}^2$ b) AlN/thermal-SiO₂ with $k=8.2$ and $Q_F = -5 \times 10^{11} / \text{cm}^2$. The device with SiO₂ passivation undergoes a breakdown at 580 V while the device with AlN passivation can sustain almost 700 V.

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

The origin of negative charge for Al-based dielectric will be discussed later in detail in Chapter four. Figures 3.4 (a) and (b) show the electric field distribution in the vicinity of the schottky corner for unterminated diodes passivated with SiO₂ and AlN respectively, and under 580 V of reverse bias. Increasing the dielectric constant of the passivation layer has a direct influence on the surface electric fields and in particular on the edge fields. As seen from Fig. 3.4, the edge field is reduced by more than 30-40% from a peak value of ~7.8 MV/cm at the schottky contact edge to ~5 MV/cm when the passivation dielectric is switched from conventional SiO₂ to AlN. The breakdown voltage in this case improves from ~580 V to ~700 V. The extreme field at the schottky corners reduces the width of the triangular barrier and increases the tunneling leakage currents. These edge related tunneling leakage currents which contribute to a significant part of the overall leakage current, especially at room temperature [68], will be greatly reduced if the passivation layer dielectric constant k is increased by switching from conventional SiO₂ to AlN. Also based on the fact that the measured reverse leakage current of SiC SBDs has been reported to be orders of magnitude higher than that given by the thermionic emission theory [69], the schottky barrier height lowering (SBHL) effect [68] as described in eqn. (3-28), has to be considered for SiC.

$$\Delta\phi_B = \alpha E^{1/2} + \beta E \quad (3-28)$$

In the above $\Delta\phi_B$ refers to the barrier height lowering, whereas on the right hand side the square root dependence on electric field term corresponds to the image force, while the linear term corresponds to the dipole effect, and α and β are fitting parameters. Therefore, with a reduced electric field, the SBHL effect will also be diminished and the leakage currents will be further reduced. This reduced surface electric field also brings along other

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

benefits to the device performance such as higher breakdown voltages and improved reliability.

3.5 Numerical Simulations of FP Terminated SBDs

Fig. 3.5 Schematic of FP terminated 4H-SiC SBD used for numerical simulations. The device has an intermediate layer of SiO_2 with a thickness of $0.05 \mu\text{m}$, while t_{di} refers to the total dielectric thickness including the intermediate SiO_2 . Figure not exactly to scale.

The structure of the simulated FP terminated 4H-SiC SBD is as shown in Fig. 3.5. The structure consist of a $10 \mu\text{m}$ epilayer doped n-type to a value of $N_D = 2 \times 10^{15} / \text{cm}^2$. The metal overlaps the dielectric by $10 \mu\text{m}$ which equals the epilayer thickness and represents the maximum value of depletion layer thickness in the vertical direction. The lateral depletion has an extension slightly smaller than $10 \mu\text{m}$. Thus the metal overlap of $10 \mu\text{m}$ will completely overshadow the lateral depleted region. The breakdown voltage will saturate for metal overlap beyond $10 \mu\text{m}$ [45], which is also seen from our simulation results. The

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

dielectric for the FP plate is a stack of either SiO₂ ($k = 3.9$) or AlN ($k = 8.2$) with an intermediate layer of thermal SiO₂. The thickness of the intermediate SiO₂ is fixed at 0.05 μm , while the total dielectric thickness t_{di} which includes the intermediate SiO₂ layer can vary up to 1.8 μm . Again we have assumed a nominal positive interface charge $Q_F = +5 \times 10^{11}/\text{cm}^2$ for the SiO₂/SiO₂ stack and a negative charge $Q_F = -5 \times 10^{11}/\text{cm}^2$ for the AlN/SiO₂ stack [65-67].

The breakdown of the device occurs either when there is breakdown within 4H-SiC due to impact ionization or the FP dielectric undergoes a breakdown due to the electric field within it exceeding its breakdown strength. We have assumed the breakdown strength of SiO₂ and AlN to be ~ 10 MV/cm [14] and ~ 7 MV/cm [70] respectively. As seen in Fig. 3.5 we define 2 principle corners for the device, the primary corner ‘P’ at the 4H-SiC/Pt metal interface and a outermost secondary corner ‘S’ which lies at the dielectric/Pt metal interface. The impact ionization related breakdown within 4H-SiC generally occurs at the corner P while the dielectric breakdown occurs at corner S.

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

Fig. 3.6 Simulated breakdown voltage vs. dielectric thickness of a $\text{SiO}_2/\text{SiO}_2$ FP terminated 4H-SiC SBD.

The simulated breakdown voltage vs. dielectric thickness for the $\text{SiO}_2/\text{SiO}_2$ FP device is shown in Fig. 3.6. For comparison we also have the V_B for unterminated device of ~550 V shown in the same plot. As seen from the figure, there exists an optimum SiO_2 thickness ($t_{optSiO_2} \sim 0.4 \mu\text{m}$) at which V_B has a peak value of ~1200 V. This breakdown voltage is more than twice that of the corresponding unterminated device, and it constitutes an improvement of ~30% of the ideal breakdown voltage of ~2100 V.

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

Fig. 3.7 Peak electric field within SiC bulk and within FP dielectric SiO₂ at 500 V of reverse bias for SiO₂/SiO₂ FP terminated 4H-SiC SBD.

The peak electric fields within SiC bulk (E_{SiCmax}) and within SiO₂ (E_{oxmax}) at 500 V of reverse bias for different t_{di} are shown in Fig. 3.7. The 500 V of reverse bias is an arbitrary voltage reference point used for sake of comparison. It is representative of any other voltage point from comparison point of view. Fig. 3.7 explains the initial increase and subsequent decrease in V_B with respect to t_{di} as seen in Fig. 3.6. As seen from Fig. 3.7, when t_{di} is small, E_{oxmax} which occurs at the secondary corner S is very high but reduces as t_{di} increases. Thus the breakdown that dominates at lower dielectric thickness, which occurs at the corner S due to dielectric breakdown, improves as t_{di} is increased. At the same time, it is

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

observed that E_{SiCmax} which occurs at the primary corner P increase with t_{di} . This is due to a decreasing influence of the FP on the corner electric field relief as t_{di} is increased. Thus at large t_{di} the device is more likely to breakdown at the corner P due to impact ionization in 4H-SiC, which accounts for the reduction in V_B with increasing t_{di} . Therefore we have a peak V_B that occurs in the transition region where the electric fields in the SiO₂ and 4H-SiC are minimized, as shown in Fig. 3.7.

As seen in Fig. 3.7, the peak bulk electric field E_{SiCmax} increases continuously with t_{di} except for very low thickness of $t_{di} = 0.05 \mu\text{m}$, where the electric field is stronger and out of the increasing trend. The reason for this behaviour will be clear from the 2D electric field visualization as seen in Fig. 3.8, which shows the electric field distribution for two different dielectric thicknesses of $t_{di} = 0.1$ and $1.3 \mu\text{m}$ under a reverse bias voltage of 500 V. When the thickness is very low, the peak dielectric field E_{oxmax} at the corner S is so strong that E_{SiCmax} lies within SiC just beneath the corner S rather than at the corner P as in the case of larger thickness ($t_{di} > 0.05 \mu\text{m}$). This is the reason for a drop in E_{SiCmax} as t_{di} is increased from $0.05 \mu\text{m}$ to $0.1 \mu\text{m}$. Thereafter, E_{SiCmax} is monotonically increasing with t_{di} , as E_{SiCmax} always occurs at primary corner P for thickness beyond $0.1 \mu\text{m}$. On the other hand, E_{oxmax} always occurs at the corner S irrespective of t_{di} and is much lower at higher t_{di} (see Fig.3.8).

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

Fig. 3.8 Electric Field distribution for SiO₂/SiO₂ FP device for 2 different thickness
a) $t_{di} = 0.1 \mu\text{m}$, b) $t_{di} = 1.3 \mu\text{m}$ at 500 V of reverse bias around the vicinity of schottky corner. The inset shows the zoom-in of the region of peak electric field within SiC.

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

Fig. 3.9 Band-Band generation distribution as a result of impact ionization for
a) $t_{di} = 0.1 \mu\text{m}$, b) $t_{di} = 1.3 \mu\text{m}$ at 500 V of reverse bias. In the inset shows the zoom-in of
the region of maximum impact ionization.

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

Figures 3.9 (a) and (b) show the band-to-band electron hole pair generation map for the same structure as a result of impact ionization for two different thicknesses of $t_{di} = 0.1 \mu\text{m}$ and $1.3 \mu\text{m}$ respectively under a reverse bias voltage of 500 V. As seen, the peak generation occurs beneath the corner S at lower thickness but shifts to the corner P as the thickness is increased. The magnitude is several orders higher for thicker t_{di} (see Fig. 3.9) due to the reducing influence of FP on the field relief being provided at the primary corner P as the dielectric thickness is increased.

Fig. 3.10 Simulated results of breakdown voltage vs. dielectric thickness for an AlN/SiO₂ FP terminated 4H-SiC.

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

Next we discuss the results of breakdown simulations for an AlN/SiO₂ FP terminated device as shown in Fig. 3.10. For comparison, we also present the results of SiO₂/SiO₂ FP device in the same graph. As can be seen, V_B improves to as much as 1600 V which is almost 80% of the ideal V_B of ~2100 V, compared to a peak V_B of 1200 V for the SiO₂/SiO₂ FP device. The optimal thickness is shifted to $t_{optAlN} = 0.7 \mu\text{m}$ for the AlN/SiO₂ FP device compared to 0.4 μm for the SiO₂/SiO₂ FP device. Figure 3.11 shows the peak electric fields E_{SiCmax} within SiC, the peak electric field E_{oxmax_IL} within the SiO₂ intermediate layer and the peak electric field E_{AlNmax} within the AlN dielectric. We have defined a transition region as a region where the dielectric peak field is less than 50% of its breakdown strength (i.e 5 MV/cm for SiO₂ and ~3.5 MV/cm for AlN) and the peak SiC electric field is not more than 1.5 times the minimum electric field value as seen in field versus t_{di} characteristics. As compared to the results for the SiO₂/SiO₂ FP device shown in Fig. 3.7, the transition region is wider for the AlN/SiO₂ FP device. Thus the V_B versus t_{di} curve is much flatter for AlN/SiO₂ FP terminated device, rendering the V_B much less sensitive to variations in t_{di} , which is advantageous from the process and manufacturing point of view.

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

Fig. 3.11 Peak electric field within SiC bulk and within FP dielectric AIN and intermediate SiO₂ at 500 V of reverse bias for AIN/SiO₂ FP terminated 4H-SiC SBD.

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

Fig. 3.12 Peak electric field within a) FP dielectric at Corner S b) SiC bulk at 500 V of reverse bias.

We also compared the peak dielectric field E_{ALNmax} that occurs at the corner S for the AlN/SiO_2 FP device, E_{oxmax} for the $\text{SiO}_2/\text{SiO}_2$ FP device and peak SiC bulk field E_{SiCmax}

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

which generally occurs at the corner P under a reverse bias of 500 V. The results are shown in Figs. 3.12 (a) and (b). The advantages of using AlN, which has a higher dielectric constant compared to SiO₂, as the FP dielectric is very much obvious. As seen from Fig. 3.12 (a), the peak dielectric field in case of AlN//SiO₂ FP SBD is much lower (roughly by a factor of 2.5×) than in case of SiO₂/SiO₂ FP device. As seen from Fig. 3.12(b), E_{SiCmax} is also much lower for the AlN/SiO₂ FP device compared to the SiO₂/SiO₂ FP device. This not only improves the breakdown voltage but also helps reduce the edge related tunneling leakage currents and improve the long term reliability of the device.

As indicated in Fig. 3.10, in the case of AlN/SiO₂ FP terminated SBDs, breakdown for $t_{di} \geq 0.7 \mu\text{m}$ is due to impact ionization induced breakdown as a result of field enhancement at the corner P. On the other hand, for $t_{di} < 0.7 \mu\text{m}$ breakdown occurs within the AlN dielectric at the corner S. At very low dielectric thickness, that is for $t_{di} \leq 0.2 \mu\text{m}$, the intermediate SiO₂ layer tends to breakdown due to extreme electric field at the corner S within the AlN, which percolates down into the SiO₂ layer and is magnified almost 2.5 times due to the difference in the dielectric constant between SiO₂ and AlN. Fig. 3.13(a) and (b) show the 2D electric field distribution for two different dielectric thicknesses $t_{di} = 0.1 \mu\text{m}$ and $1.3 \mu\text{m}$ respectively under a 500 V reverse bias voltage. As seen from Fig. 3.13(a) the extreme electric field at the secondary corner S and within the AlN layer for $t_{di} = 0.1 \mu\text{m}$ percolates down to the SiO₂ layer, get magnified by ~2.5 times and propagates further in to the SiC layer. As a result, the peak electric field within SiC too lies under the corner S. On the contrary, as seen from Fig. 3.13(b), the peak electric field in SiC lies at primary corner P in case of $t_{di} = 1.3 \mu\text{m}$.

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

Fig. 3.13 Electric Field distribution at 500 V of reverse bias for AlN/ SiO_2 FP terminated at a dielectric thickness of a) $t_{di} = 0.1 \mu\text{m}$ and b) $t_{di} = 1.3 \mu\text{m}$.

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

Fig. 3.14 Band to band generation map of AlN/SiO₂ FP terminated 4H-SiC SBD for
a) $t_{di} = 0.1 \mu\text{m}$ and b) $t_{di} = 1.3 \mu\text{m}$.

The 2D map of band to band generation of electron hole pairs as a result of impact ionization for the AlN/SiO₂ FP device for $t_{di} = 0.1 \mu\text{m}$ and $t_{di} = 1.3 \mu\text{m}$ can be visualized in Fig. 3.14(a) and (b). As seen from Fig. 3.14(a), the maximum band to band generation

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

occurs in SiC directly under the corner S for $t_{di} = 0.1 \mu\text{m}$ while as seen from Fig. 3.14(b) it occurs in the vicinity of corner P for $t_{di} = 1.3 \mu\text{m}$. The reason for different location for the peak generation rates is the same as explained previously. This is due to the peak of electric field within SiC which lies beneath corner S for $t_{di} = 0.1 \mu\text{m}$ while its lies at corner P for thicker dielectric $t_{di} = 1.3 \mu\text{m}$. As seen from Fig. 3.14 (a) and (b), band to band generation rates are several orders of magnitude higher for the device with a thicker dielectric ($t_{di} = 1.3 \mu\text{m}$). As the thickness is increased, impact ionization at the corner P starts to dominate due to reducing influence of FP while the electric field in the dielectric at the corner S starts to mitigate.

3.6 Conclusions

In conclusion, in this chapter, we discussed the basic fundamentals of numerical device simulations and the framework of equations and physical model solved by the simulator. We also presented the literature values of model parameters specific to 4H-SiC used for our simulations. Numerical simulations of ideal diodes with practical epilayer thickness of $10 \mu\text{m}$ reveal a second order increase in V_B with N_D which eventually clamps at $\sim 2000 \text{ V}$. This is due to the fact that the depletion layer is readily punched to the substrate when N_D is lower than $1 \times 10^{16}/\text{cm}^3$. The ideal V_B is much higher for thicker epilayer. The V_B is $\sim 5720 \text{ V}$ when the epilayer is $100 \mu\text{m}$ thick. Thus thick epilayers with lower doping are needed to achieve extremely high blocking voltages. Underminated diodes on the other hand show a much lower V_B which is just $\sim 20\text{-}30\%$ of these ideal values due to extreme field enhancement at schottky corner. A layer of passivation with a higher k in form of AlN was found to reduce the corner electric fields by as much as $30\text{-}40\%$ and correspondingly improve V_B . The V_B for an unterminated device improved from $\sim 580 \text{ V}$ to $\sim 700 \text{ V}$ when the passivation was switched from CVD SiO_2 to sputter deposited AlN. FP termination using $\text{SiO}_2/\text{SiO}_2$ dielectric was found to increase V_B to as much as $50\text{-}60\%$ of ideal V_B . A peak V_B

Chapter 3 Numerical Simulations of 4H-SiC Schottky Barrier Diodes

of ~ 1200 V was achieved at a SiO_2 thickness of ~ 0.4 μm . The V_B could be improved to as much as 80% of the ideal V_B using the higher k dielectric stack in form of AlN/ SiO_2 FP device. In this case, a peak V_B of ~ 1600 V can be achieved at an AlN thickness of ~ 0.7 μm . For all these FP devices, a systematic study on V_B as a function of dielectric thickness was carried out. The breakdown is dominated by dielectric breakdown for lower dielectric thickness and edge related impact ionization induced breakdown for higher dielectric thickness. A transition region exists between these two regions, where V_B attains a maximum value.

Chapter 4

Dielectrics Characterization

In this chapter, we begin by discussing the process used to deposit Al-based high- k dielectrics, followed by the physical and electrical characterization results of these dielectrics. The dielectrics have been characterized on capacitor structures, results of which are being presented in this chapter. Nevertheless the aim is to use them to form Field Plate (FP) terminated 4H-SiC SBDs, and as secondary passivation layer which will be discussed in subsequent chapters. The properties of the Al-based high- k dielectrics are also compared to those of thermal SiO₂ and PECVD SiO₂ dielectrics, which have also been used for the same purpose as Field Plate dielectrics and as passivation layer for 4H-SiC SBDs. We will also present our investigation of multi-step breakdown seen on Al-based dielectrics/SiO₂ stack using measurements of dielectric relaxation currents.

4.1 Process Details

The dielectrics used in this study have been deposited on 4H-SiC samples to form metal-insulator-semiconductor (MIS) structures, have been extensively characterized and will be discussed in following sections. Finally those dielectrics have been used for formation of FP terminated SBDs and as passivation dielectric on unterminated SBDs and will be discussed in subsequent chapters. The process details are as follows:

- 1) The 4H-SiC samples which have been diced into 5mm × 5mm pieces first underwent a cleaning process. The samples were first degreased in acetone, isopropyl alcohol (IPA) and rinsed in deionized (DI) water. The samples were then cleaned using the

Chapter 4 Dielectrics Characterization

standard Radio Corporation of America (RCA) cleaning process to remove organic and heavy metal contamination on the surface. The samples were then stripped of native oxide by dipping in 1:10 dilute HF and then rinsed in DI water for 10 mins. The samples then underwent a sacrificial oxidation process. A sacrificial SiO₂ layer ~50 nm thick was grown on the surface by oxidation in pure O₂ at 1150°C for 3 hours. The samples have been loaded and unloaded in the oxidation furnace at 850°C. The sacrificial oxide was then stripped in dilute HF to prepare a fresh surface for device processing.

- 2) The samples were then oxidized in dry O₂ at 1150 °C for 2 hrs, followed by 1 hr anneal in N₂ at 1100 °C. The samples have been loaded and unloaded into the furnace tube at 850 °C. The thickness (t_{IL}) of the thermal oxide formed was ~40 nm for the 2 hours of oxidation process. The thermal oxide grown was used as an intermediate layer (IL) between the Al-based high- k dielectrics and 4H-SiC. These samples with t_{IL} ~40 nm have been used to form MIS capacitors. The thermal oxide layer serves the dual purpose of reducing interface charge and improving the band-offset between the dielectrics and 4H-SiC, which in turn lowers the tunneling leakage currents [14]. For comparison, some samples were prepared without the oxide layer, by stripping the layer in dilute HF. After clearing the oxide on the backside of the wafers with HF, a backside ohmic contact was formed using sputter deposited Pt, which was then subjected to a 950 °C rapid thermal anneal (RTA) in N₂ for 60 s.
- 3) The dielectrics used to form MIS capacitors include thermal SiO₂; plasma enhanced chemical vapor (PECVD) deposited SiO₂ and sputter deposited Al-based dielectrics. The PECVD SiO₂ dielectrics were deposited at 350 °C using silane (SiH₄) and

Chapter 4 Dielectrics Characterization

nitrous oxide (N_2O) with flow rates of 50 sccm and 250 sccm respectively. The deposition rate was $\sim 250 \text{ \AA}/\text{min}$. The Al-based dielectrics were deposited using the 13.56 MHz RF magnetron reactive sputtering technique. The sputtering was carried out using a pure Al target (99.999%). An Ar/ N_2 mixture was used for the deposition of AlN_x , while a gas mixture of Ar and forming gas ($\text{N}_2:\text{H}_2$) (80%:20%) was used for the deposition of $\text{AlN}_y:\text{H}$. The Ar flow rate was maintained at 10 sccm while the N_2 and $\text{N}_2:\text{H}_2$ flow rates were maintained at 25 sccm. The RF power was fixed at 350 watts and the substrate holder was intentionally cooled via chilled water circulating within the chuck. The deposition rates for AlN_x and $\text{AlN}_y:\text{H}$ were around $0.2 \text{ }\mu\text{m}/\text{hr}$ and $0.1 \text{ }\mu\text{m}/\text{hr}$ respectively. The thickness of the deposited dielectrics (t_{dep}) was $\sim 60 \text{ nm}$ for MIS capacitor structures. We also prepared a few MIS samples with t_{dep} at 30 nm, 100 nm and 150 nm mainly to ascertain some interface properties and net dielectric charge for different dielectric thicknesses. A few MIS samples have the dielectrics deposited at sputtering RF power of 200 watts and 450 watts to study the effects of sputtering power on sputter induced damage on the surface. For MIS samples, the effects of annealing the dielectrics at $950 \text{ }^\circ\text{C}$ for 60 s in N_2 were also investigated.

- 4) Al with a thickness of $\sim 300 \text{ nm}$ and a diameter of $200 \text{ }\mu\text{m}$ was deposited as the gate for MIS capacitors. A HP 4156C semiconductor parameter analyzer was used to investigate the forward J - V characteristics of SBDs over a temperature range from -50°C to 300°C . It was also used to study the gate leakage current density (J_g) and relaxation current density (J_{relax}) of MIS capacitors. A HP 4284A LCR meter was used for C - V measurements for MIS capacitors at 1 MHz.

Chapter 4 Dielectrics Characterization

- 5) For structural characterization using x-ray diffraction (XRD), AlN_x and $\text{AlN}_y\text{:H}$ films of around 100 nm were deposited on 100 nm SiO_2 coated p-type (100) Si substrate using the same process conditions as for FP deposition. A Siemens D5005 XRD spectrometer with $\lambda_{\text{Cu } K\alpha} = 1.5405 \text{ \AA}$ radiation operated at 40 kV and 40 mA was used for the measurements. The effects of annealing the Al-based dielectrics at 950°C for 60 s in N_2 on their structural properties were also investigated.

4.2 Dielectric Physical Characterization

Figures 4.1 and 4.2 show the XRD spectra of AlN_x and $\text{AlN}_y\text{:H}$ films respectively. As seen from Fig. 4.1(a), the as-deposited AlN_x shows a minor diffraction peak at $2\theta \sim 36.10^\circ$ associated with the (0002) preferential orientation of 2H-AlN (Joint Committee on Powder Diffraction Standards JCPDS c25-1133). This suggests that even the as-deposited AlN_x is partially polycrystalline. In contrast, as seen from Fig. 4.2(a), the as-deposited $\text{AlN}_y\text{:H}$ diffraction pattern shows no peaks, suggesting that this film is completely amorphous. Our results are in agreement with those reported by Y. J. Yong *et al.* [16] where suppression of the c-axis preferred orientation of AlN (0002) was noted when hydrogen was introduced into the film. The XRD spectrum of the AlN_x film annealed at 950°C as seen in Fig. 4.1(b) shows stronger peak corresponding to the AlN (0002). Similarly, the XRD spectrum of $\text{AlN}_y\text{:H}$ film as seen from Fig. 4.2(b) shows the emergence of AlN (0002) peak after a 950°C anneal.

Chapter 4 Dielectrics Characterization

Fig. 4.1 XRD spectra of sputter deposited AlN_x films on SiO_2/Si substrate (a) as-deposited (b) after 950 °C/60 s N_2 anneal.

Chapter 4 Dielectrics Characterization

Fig. 4.2 XRD spectra of sputter deposited $\text{AlN}_y\text{:H}$ films on SiO_2/Si substrate (a) as-deposited (b) after $950^\circ\text{C}/60\text{ s N}_2$ anneal.

Chapter 4 Dielectrics Characterization

To qualitatively compare the density of AlN_x and $\text{AlN}_y\text{:H}$ thin films, they were subjected to wet etch at room temperature in KOH based AZ400K developer solution diluted to a ratio of 2:1 in DI water. It is a well-known fact that the wet etch rate (WER) under identical conditions is inversely proportional to the film density and film quality, as the reaction occurs favorably at grain boundaries and defect sites [71]. In our case the AlN_x and $\text{AlN}_y\text{:H}$ films exhibited WERs of ~ 7 nm/min and ~ 3 nm/min respectively, and thus it is deduced that the $\text{AlN}_y\text{:H}$ films are denser than the AlN_x films. This is consistent with that reported in literature where hydrogenated AlN was found to be denser than non-hydrogenated AlN [16, 17]. Besides this advantage, the as-deposited $\text{AlN}_y\text{:H}$ films which are amorphous are expected to have much better dielectric breakdown strength and lower leakage current due to the presence of less grain boundaries [72]. They are therefore expected to be more suitable as FP dielectric.

4.3 Dielectrics Electrical Characterization

Figure 4.3(a) shows the 1 MHz C - V curves of the MIS capacitors with as-deposited $\text{AlN}_y\text{:H}$, AlN_x and PECVD SiO_2 as dielectrics on top of an IL thermal SiO_2 . These samples are denoted as $\text{AlN}_y\text{:H}/\text{SiO}_2$, $\text{AlN}_x/\text{SiO}_2$ and PECVD $\text{SiO}_2/\text{SiO}_2$ respectively. The CV curve of the sample with just the IL thermal SiO_2 alone is also shown. Figure 4.3(b) shows the corresponding C - V curves for the samples annealed at 950°C . Figure 4.4 shows the C - V curves for the MIS capacitors with as-deposited dielectrics but without the IL thermal SiO_2 . These samples with Al-based dielectrics showed substantial leakage current after 950°C RTA and thus their C - V characteristics upon annealing were not investigated. For the results shown in Figs. 4.3 and 4.4, the voltage was swept at ~ 0.5 V/s from inversion to accumulation and back to inversion. These are labeled as forward and reverse sweeps respectively, and the results are correspondingly represented by symbols and lines in

Chapter 4 Dielectrics Characterization

Figs. 4.3 and 4.4. All the measurements were carried out without illumination and the results reveal deep depletion characteristics.

As seen from Figs. 4.3(a) and 4.3(b) there is no hysteresis observed for all the dielectrics with the IL thermal SiO₂. From Fig. 4.4, it can be seen that devices with PECVD SiO₂ and without the IL thermal SiO₂ too show absence of hysteresis. In contrast, the Al-based dielectric devices without IL thermal SiO₂ show moderate amount of hysteresis, which is indicative of charge trapping due to presence of slow traps. For the dielectrics with IL thermal SiO₂, even though we do not see any hysteresis, we cannot rule out the presence of low density of slow traps formed due to defects at the dielectric/thermal SiO₂ interface. The thermal SiO₂ (~ 40 nm) is too thick to permit substantial amount of electron injection from the substrate within the voltage sweep range.

Chapter 4 Dielectrics Characterization

Fig. 4.3 High frequency (1MHz) C-V curves of MIS capacitors with the dielectric

a) as-deposited on thermal SiO₂ b) after a 950°C RTA in N₂ for 60 s on thermal SiO₂.

Symbols represents forward sweep from inversion to accumulation while line represents the reverse direction from accumulation to inversion.

Chapter 4 Dielectrics Characterization

Fig. 4.4 High frequency (1MHz) C - V curves of MIS capacitors with as-deposited dielectrics on 4H-SiC without thermal SiO_2 . Symbols represents forward sweep from inversion to accumulation while line represents the reverse direction from accumulation to inversion.

Table 4.1 shows the dielectric constants (ϵ_r) for the deposited dielectrics, flat-band voltages (V_{FB}), effective dielectric charge (N_{eff}) and effective dielectric strengths (E_c) extracted from the C - V and J - V measurements. The parameter ϵ_r was calculated from the maximum accumulation capacitance (C_i). The parameter $\epsilon_{r,stack}$ refers to dielectric constant of the composite stack while EOT is the equivalent oxide thickness of the stack. In the case of samples with IL thermal SiO_2 , we use the fact C_i is a series capacitance of deposited

Chapter 4 Dielectrics Characterization

dielectric capacitance (C_r) and IL thermal SiO₂ capacitance (C_{IL}), where C_{IL} is known ($t_{IL} \sim 40$ nm, $\epsilon_{IL} = 3.9$). N_{eff} was obtained from $(-\Delta V_{FB}C_i)/qA$, where ΔV_{FB} is the V_{FB} shift from the ideal value, A is the area of the capacitor and q is the electronic charge. The ideal flat-band voltage (V_{FB}) was deduced from an ideal CV curve obtained using Medici™ device simulation with an Al gate (work function= 4.1 eV).

Table 4.1 Key parameters extracted from the C - V and J - V measurements on the MIS samples. In the table below 950°C denotes 4H-SiC samples where the dielectric has undergone a 950°C/60 s RTA in N₂.

Dielectric		ϵ_r	$\epsilon_{r,stack}$	EOT (nm)	V_{FB} (V)	$N_{eff} \equiv$ /cm ² ($\times 10^{12}$)	E_c (MV/cm)
AlN _x /SiO ₂	As-dep.	8.5	5.73	66.52	2.35	-0.72	12.2
	950°C RTA	8.6	5.76	66.21	-1.64	0.56	10.3
AlN _y :H/SiO ₂	As-dep.	8.4	5.74	67.72	1.77	-0.53	13.3
	950°C RTA	8.6	5.8	67.1	-1.49	0.51	11
PECVD-SiO ₂ /SiO ₂	As-dep.	4	3.96	99.77	-2.73	0.62	10.1
	950°C RTA	4	3.94	100.37	-2.41	0.55	9.9
Thermal SiO ₂	As-dep.	3.9	3.9	39.4	-3.05	0.68	10.1
	950°C RTA	4	4	38.9	-3.15	0.71	10
AlN _x	As-dep.	8.2	8.2	27.36	4.73	-3.5	8.6
AlN _y :H	As-dep.	8.2	8.2	28.12	3.81	-2.8	10.2
PECVD-SiO ₂	As-dep.	3.8	3.8	62.91	-1.1	0.46	8.9

As can be seen, for the as-deposited AlN_x/SiO₂ and as-deposited AlN_y:H/SiO₂ samples, V_{FB} is positive and ΔV_{FB} are +2.15 V and +1.57 V respectively from the ideal V_{FB} of ~0.2 V. This shows a presence of negative charge in the as-deposited Al-based dielectric films. The presence of negative charge in Al-based dielectric films on 4H-SiC had also been reported

Chapter 4 Dielectrics Characterization

by other researchers [73-76]. Presence of negative fixed charge is typical of Al incorporated high- k dielectrics even when deposited on Si [77-80]. In particular a very high density of fixed negative charge ($Q_F = -3$ to $-8 \times 10^{12}/\text{cm}^2$) has been reported in Aluminum oxide Al_2O_3 and Al incorporated Hafnium oxide (HfAlO_x) films on Si [77-80]. The main mechanism for this fixed negative charge in AlO_x films is a change in coordination number of Al^{3+} from six (octahedral) to four (tetrahedral) at the $\text{AlO}_x/\text{SiO}_2$ interface as revealed by the XPS results [77]. Co-ordination number is the number of atoms, ions or molecules that a central atom or ion holds as its nearest neighbours in a complex, a crystal or a coordination compound. Tetrahedrally coordinated Al^{3+} is believed to be a source of fixed negative charge in AlO_x film [77-79]. The change in co-ordination number only happens within one monolayer from interface and does not impact the bulk of AlO_x film [78]. Thus the fixed negative charge resides mainly at the $\text{AlO}_x/\text{SiO}_2$ interface. Bae *et al.* [79] saw huge increase in negative charge when Al was added to their HfO_2 high- k dielectric to deposit HfAlO dielectric using CVD. The amount of negative charge in their dielectric increased as the proportion of Al was increased from 20% to 38% which is due to excess tetrahedral Al^{3+} at the $\text{AlO}_x/\text{SiO}_2$ interface. The negative charge in Al_2O_3 film on Si was found to decrease with thicker interfacial layer (IL) SiO_2 [77]. This observation is quite similar to that of Cheong *et al.* [73] where they observed the negative charge in their atomic layer deposited (ALD) deposited Al_2O_3 film on 4H-SiC decreased as thicker IL thermal oxide was introduced between Al_2O_3 and 4H-SiC. K Jang *et al.* [80] found the negative charge in their AlON film on Si reducing with reducing oxygen component and increasing nitrogen content.

In case of our $\text{AlN}_x/\text{SiO}_2$ and $\text{AlN}_y\text{:H}/\text{SiO}_2$ dielectrics on 4H-SiC there are few sources of charge which includes:-

1. Negative fixed charge from $\text{AlN}_x/\text{SiO}_2$ and $\text{AlN}_y\text{:H}/\text{SiO}_2$ interface due to change in coordination number of Al^{3+} from six (octahedral) to four (tetrahedral) at the SiO_2

Chapter 4 Dielectrics Characterization

interface. Even though our dielectric films were deposited in an N_2/Ar and $N_2:H_2/Ar$ gas mixture respectively, there is some inherent contamination of our AlN film by residual oxygen in the sputtering chamber which gives rise to AlO_x at the SiO_2 interface.

2. Positive fixed charges from $SiON_x/4H-SiC$ interface. The thermal SiO_2 has been thermally nitrided at $1100^\circ C$ in pure N_2 during oxidation growth and hence referred to as $SiON_x$ in this case. The positive fixed charge originates from the dangling bonds on the $4H-SiC$ surface. Though this is well-known phenomenon even for Si and needs no further explanation, the evidence is in form of positive charge seen on our thermal SiO_2/SiC samples.
3. Acceptor like electron traps (border traps) from defects at the Al-based dielectric/ SiO_2 interface. The Al-based dielectric/ SiO_2 interface is believed to be highly imperfect as-deposited due to sputter damage to the SiO_2 bulk a few monolayers thick in the close proximity of Al-based dielectric/ SiO_2 interface.
4. From interface traps at the $SiO_2/4H-SiC$ interface which partly arise from sputter damage. These interface traps act as fixed charge when not located in the majority carrier band edge [75].

As seen from Table 4.1, the negative charge on our $AlN_y:H/SiO_2$ dielectric stack is lower than AlN_x/SiO_2 . This can be explained based on the fact that addition of hydrogen to the film reduces oxygen contamination of the film [16, 17]. Thus the negative charge is lower with lower oxygen content as the film resembles more like AlN rather than Al_2O_3 . This is similar to observations of K Jang *et al.* [80]. There is minimal contribution of negative charge from the Al-based dielectric bulk since our separate experiments with different

Chapter 4 Dielectrics Characterization

Al-based dielectric thickness revealed an almost linear shift of V_{FB} with dielectric thickness as seen in Fig. 4.5 implying there is almost no change in net charge density.

Fig. 4.5 Flat-band voltage shift ΔV_{FB} for different Al-based dielectric thickness. Almost linear shift indicates almost constant net charge density N_{eff} .

We also found an increase in ΔV_{FB} with increased sputtering power as seen from Fig. 4.6 implying an increase in net negative charge with increased sputtering power. At higher sputtering power, the Al-based dielectric films are expected to be Al rich since other sputtering conditions such as gas flow rates, chamber pressure are the same. Thus Al and tetrahedral Al^{+3} concentration is expected to be higher at higher sputtering power, which explains the increase in negative charge with increased sputtering power [79]. Also sputter induced damage is expected to increase with increased sputtering power leading to higher interface and border traps.

Chapter 4 Dielectrics Characterization

Fig. 4.6 Flat-band voltage shift ΔV_{FB} as a function of RF sputtering power.

The sputter damage also manifests itself in a form of increased hysteresis due to formation of slow trapping centers as a result of sputter damage. As seen from Fig. 4.7, hysteresis that was absent or negligible at low sputtering power becomes significant as the sputtering power is increased to 450 watts.

Chapter 4 Dielectrics Characterization

Fig. 4.7 High Frequency (1 MHz) C-V curves of samples deposited with RF power at 450 watts showing emergence of hysteresis due to sputter induced damage. Symbols represents forward sweep from inversion to accumulation while line represents the reverse direction from accumulation to inversion.

As seen from Fig. 4.3(b) and listed in Table 4.1, the V_{FB} shifts to a small nominal negative value which is similar to that of thermal oxide on 4H-SiC after a 950°C anneal in N_2 . It implies the net dielectric charge is positive after anneal. This shows dominance of positive fixed charge from $SiON_x/SiC$ interface over the negative charge from tetrahedral Al^{+3} and trapped electron charge. The fixed positive oxide charge at $SiO_2/4H-SiC$ interface is known to increase tremendously after rapid thermal annealing [81, 82]. Also annealing will lead to partial recovery of sputter induced damage which will reduce electron and interface traps which will reduce the negative charge further. M Avice *et al.* [74] noted the

Chapter 4 Dielectrics Characterization

presence of negative charge in their CVD grown Al_2O_3 film, which was reduced with increasing annealing time. For the case of PECVD $\text{SiO}_2/\text{SiO}_2$ samples, it is noted that the V_{FB} is quite similar to that of the samples with only thermal oxide film.

The as-deposited PECVD SiO_2 samples without the IL thermal SiO_2 , as shown in Table 4.1, shows a nominal V_{FB} of -1.1 V and a low N_{eff} of $4.6 \times 10^{11}/\text{cm}^2$. In contrast, the as-deposited Al-based dielectrics samples without the IL thermal SiO_2 have large V_{FB} of +4 to +5 V, indicating the presence of excess negative charge. Cheong *et al.* [73] similarly observed negative charge on their atomic layer deposited (ALD) Al_2O_3 dielectrics on bare 4H-SiC, and the amount was reduced as an increasingly thicker IL thermal oxide was introduced between the Al_2O_3 and 4H-SiC. This is similar to observations of K. Torii *et al.* [77] where they saw extremely high density of negative charge in their Al_2O_3 film on Si when the IL was ultrathin (< 0.4 nm) which reduced as IL thickness was increased. The negative charge on our dielectric stack is slightly higher compared to negative charge ($Q_F = -3 \times 10^{11}/\text{cm}^2$) seen in AlN MIS structures grown epitaxial on 6H-SiC [76]. We believe this is due to some inherent contamination of our AlN_x and $\text{AlN}_y\text{:H}$ film by residual oxygen in sputtering chamber. Nevertheless, the negative charges seen on our $\text{AlN}_x/\text{SiO}_2$ and $\text{AlN}_y\text{:H}/\text{SiO}_2$ on 4H-SiC are of much lower densities than $\text{Al}_2\text{O}_3/\text{SiO}_2$ dielectric stack on 4H-SiC as reported by other researchers [73, 74].

Chapter 4 Dielectrics Characterization

Fig. 4.8 Leakage current density (J) vs. equivalent oxide field (E) characteristics at 27°C for MIS capacitors with a) dielectric as-deposited b) after a 950°C/60 s RTA in N_2 . The voltage has been swept at ~ 0.5 V/s with device in accumulation.

Chapter 4 Dielectrics Characterization

Figures 4.8(a) and 4.8(b) show the leakage current characteristics of the MIS capacitors in accumulation with the dielectric as-deposited and after a 950 °C anneal respectively. As some of the dielectrics here consist of a stack of deposited dielectric/thermal SiO₂, for a meaningful comparison the current density (J) has been plotted with respect to an equivalent oxide field (E_{ox}). It can be calculated as $(V_g - V_{FB})/EOT$ where V_g is the applied gate voltage and EOT is the equivalent oxide thickness [83]. The voltage V_g step size varied between 0.5-1.0 V, and the ramp rate was maintained uniform at around 0.1 MV/cm-sec. We define E_c as the point where the leakage current increases by at least one order of magnitude compared to the current at the previous voltage step, or reaches a threshold value of 1 mA/cm².

As seen from Table 4.1, Al-based dielectrics exhibit excellent E_c with the AlN_y:H/SiO₂ sample being the best of all due to its dense amorphous structure. There is a reduction in the E_c of the AlN_y:H/SiO₂ sample after annealing at 950°C. We attribute this to phase transformation from amorphous to polycrystalline, as revealed from the XRD results. The latter is known to suffer from defects and grain boundaries that reduce the electric field that is sustainable in the dielectric [72]. The leakage currents through AlN_x dielectric tends to be much higher than through the AlN_y:H dielectric especially after 950°C RTA (see Fig. 4.8(b)). We attribute this to the much larger degree of polycrystallinity in AlN_x dielectric after annealing as seen from XRD results previously. The PECVD-SiO₂/SiO₂ film is comparable to the pure thermal oxide sample in terms of E_c , both of which remained unchanged after annealing.

The AlN_y:H and AlN_x samples without the IL thermal SiO₂ exhibit comparatively higher leakage current and much lower E_c . This is attributed to the lower conduction band offsets between the dielectrics and 4H-SiC. It is to be noted, the conduction band offset

Chapter 4 Dielectrics Characterization

between 4H-SiC and the dielectric is ~ 3.2 eV in presence of intermediate SiO_2 but drastically reduces to ~ 1.5 eV in absence of SiO_2 layer. Thus we see almost three to four orders higher leakage in absence of SiO_2 . Also seen is the fact, leakage currents through $\text{AlN}_y\text{:H}$ are much lower compared to AlN_x dielectric which we attribute to its dense amorphous nature. There was marked increase in the leakage currents and further degradation in E_c (refer to Fig. 4.8(b)) when those $\text{AlN}_y\text{:H}$ and AlN_x samples without the IL thermal SiO_2 underwent annealing.

4.4 Breakdown Phenomena of Al-based Dielectrics.

The discussion so far was limited to determining dielectric breakdown strength without going into the mechanisms responsible for their gradual degradation and ultimate breakdown. A basic understanding of their breakdown mechanism would be important towards improving their breakdown strength and reliability. In this section, we will discuss the multi-step breakdown modes visible on MIS capacitor samples, which have been investigated using measurements of dielectric relaxation currents on these capacitors.

Fig. 4.9 Schematic of 4H-SiC MIS capacitor with the Al-based dielectric/ SiO_2 stack

showing the direction of J_g and J_{relax} .

Chapter 4 Dielectrics Characterization

Figure 4.9 shows a schematic of the MIS capacitor with the direction of leakage current (J_g) and relaxation current (J_{relax}) measured using a ramp-relax test [84]. The capacitors were tested for breakdown in accumulation by applying a positive V_g , while J_{relax} was measured after V_g was reduced to +2.5 V, which is slightly higher than the flat-band voltage (V_{FB}) of these capacitors, and after a wait time of 100 ms. V_g has been ramped up from 0 to 100 V at a uniform ramp rate of ~0.1 MV/cm.sec with the V_g step size limited to 1.0 V. When an external field is applied to a high- k dielectric, it separates bound charges resulting in polarization, which gives rise to a compensating internal field. When the external field is released, hopping of free charges neutralizes the internal bound charges and results in a relaxation current. As the dielectric conductivity is low, this is a slow process and follows a “Curie-von Schweidler” time-dependence of $1/t^n$, with n slightly less than 1 [85]. J_{relax} is almost negligible in a perfect dielectric like SiO₂ [86]. Thus the integrity of a high- k dielectric in a high- k dielectric/SiO₂ stack can be studied by the presence of J_{relax} . Once the high- k dielectric undergoes a breakdown, J_{relax} will cease to exist. It should be noted that J_{relax} has a direction opposite to that of J_g and is temperature insensitive [85-87].

Figure 4.10 shows J_g and J_{relax} versus electric field for a capacitor sample consisting of AlN_y:H/SiO₂ stack as-deposited. The electric field here represents an effective oxide field defined as $(V_g - V_{FB})/EOT$ where V_{FB} is the flat-band voltage and EOT is the equivalent oxide thickness. Table 4.1 discussed previously has the quantitative information on each of the above parameters which include EOT , V_{FB} etc. For reference we also show the currents measured on a capacitor sample with just the thermal SiO₂.

Chapter 4 Dielectrics Characterization

Fig. 4.10 J_g and J_{relax} as a function of electric field measured on MIS capacitors with as-deposited AlN_y:H/SiO₂ dielectric stack as well on capacitor sample with just the thermal SiO₂ as a dielectric. Symbols denote positive current while line denotes opposite direction with negative current.

Chapter 4 Dielectrics Characterization

As can be seen, the sample with just the thermal SiO_2 shows a typical 1-step breakdown, and J_{relax} is positive, in the same direction as J_g . Therefore, it is a leakage current rather than a relaxation current. For the capacitor with the as-deposited $\text{AlN}_y\text{:H/SiO}_2$ we can see two dominant breakdown modes labelled as 1-step and 2-step breakdown. In the case of 2-step breakdown (refer to Die 1 in Fig. 4.10), as the voltage was ramped up, the electric field which is almost 2.5 times in the SiO_2 compared to that in $\text{AlN}_y\text{:H}$ subjects the SiO_2 to immense electrical stress. Coupled with this, hot electrons injected from the substrate into the SiO_2 generate defects within the SiO_2 and increase interface states at the $\text{SiO}_2\text{/4H-SiC}$ interface, degrading the SiO_2 [88] as depicted in the energy band diagram shown in Fig. 4.11.

Fig. 4.11 Energy-band diagram visualization of the stacked capacitor in accumulation.

Chapter 4 Dielectrics Characterization

At one point the SiO_2 undergoes a breakdown giving rise to an abrupt increase in J_g . J_{relax} which existed throughout as evident from the negative sign maintains its direction, but with an increased magnitude due to enhanced field across $\text{AlN}_y\text{:H}$ resulting in a larger polarization. When the voltage is further increased, the $\text{AlN}_y\text{:H}$ dielectric undergoes a breakdown too. At this point, J_{relax} ceases to exist, and its flow direction has been changed to positive, implying a leakage current. In the case of 1-step breakdown of the stack (refer to Die 2 in Fig. 4.10), the only breakdown occurs at a much higher voltage. In this case too we believe the SiO_2 breakdown occurs first triggered by defect generation in the oxide. Consequently, the entire large voltage appears solely across the $\text{AlN}_y\text{:H}$ dielectric triggering its instantaneous destruction. Variations in the SiO_2 quality lead to the SiO_2 on a small percentage of dies that are less resistant to defect formation under applied electrical stress. They therefore experienced early breakdown and account for the 2-step breakdown of the composite stack observed. As-deposited $\text{AlN}_x/\text{SiO}_2$ stack exhibits similar breakdown modes though with slightly lower breakdown strength. We can explain this difference based on our earlier work, using XRD measurements where we found as-deposited AlN_x was polycrystalline and less dense in contrast to $\text{AlN}_y\text{:H}$ which was completely amorphous as-deposited. A $950^\circ\text{C}/60\text{ s}$ RTA induced phase transformation such that both AlN_x and $\text{AlN}_y\text{:H}$ are quite comparable electrically in terms of breakdown strength and mechanisms.

Chapter 4 Dielectrics Characterization

Fig. 4.12 J_g and J_{relax} as a function of electric field measured on a MIS capacitor sample with AlN_x/SiO₂ dielectric stack annealed at 950°C for 60 s in N₂. Symbols denote positive current while line denotes opposite direction with negative current.

Chapter 4 Dielectrics Characterization

Figure 4.12 shows J_g and J_{relax} versus electric field for a capacitor sample consisting of $\text{AlN}_x/\text{SiO}_2$ stack with a $950^\circ\text{C}/60$ s RTA in N_2 . On these set of samples we found 3 dominant breakdown modes. The first one (Die 1 in Fig. 4.12) involves an initial stage with multiple soft breakdown (SBKD) of AlN_x . Each of these SBKD appears as a minor jump in J_g , which we hypothesize, is due to formation of a local percolation path in AlN_x [89]. J_{relax} still exists beyond these points but shows a minor drop or discontinuity due to increased J_g and reduced polarizability of AlN_x . Annealing leads to phase transformation in AlN_x from amorphous to polycrystalline form, leading to increased bulk defects, such as ionic defects due to nitrogen vacancies, and formation of grain boundaries [72]. As the voltage is further increased, AlN_x undergoes a hard breakdown as evident from the fact that J_{relax} increases sharply and becomes positive, which implies that the relaxation current has ceased to exist. J_g also shows substantial increase at this point. Beyond this point, we see a final breakdown at higher voltages involving the SiO_2 layer. Thus we have labelled Die 1 as high- k first to indicate AlN_x underwent a breakdown first followed by SiO_2 layer as the voltage was further increased. The second breakdown mode (Die 2 in Fig. 4.12) again involves an initial multiple SBKD of AlN_x , but this time it is followed by a single simultaneous breakdown of SiO_2 and AlN_x . Each SBKD point of AlN_x gives rise to a small but an abnormal increase in J_g , which in turn accelerates defect formation in the SiO_2 . Thus the breakdown strength in this case is lower than similar breakdown mode seen on as-deposited samples (Die 2 in Fig. 4.10), which might explain the degradation seen due to annealing. The third breakdown mode not shown in Fig. 4.12 is similar to Die 1 shown in Fig. 4.10, involving the SiO_2 breakdown first, but again involves initial multiple SBKD of AlN_x .

4.5 Conclusions

In summary, we presented and discussed the characterization results of sputter deposited Al-based dielectrics (AlN_x and $\text{AlN}_y\text{:H}$), PECVD SiO_2 and thermal SiO_2 which were used to

Chapter 4 Dielectrics Characterization

form MIS capacitors on 4H-SiC. The dielectrics were characterized with and without an intermediate thermal SiO₂ on 4H-SiC. These dielectrics will be utilized as FP dielectrics and as passivation dielectrics for 4H-SiC SBDs. We presented the process details used to deposit these dielectrics. Physical characterization of sputter deposited Al-based dielectrics revealed AlN_y:H is denser as compared to non-hydrogenated AlN_x and amorphous as-deposited. Thus AlN_y:H is better suited in device application due to absence of grain boundaries and reduced leakage current. Electrical characterization of these dielectrics using *C-V* measurements reveal a presence of net negative charge for Al-based dielectrics and a net positive charge for PECVD SiO₂ and thermal SiO₂. The negative charge is believed to arise from a change in the coordination number of Al³⁺ from six (octahedral) to four (tetrahedral) at the Al-based dielectric/SiO₂ interface and from acceptor like electron traps from defects at the Al-based dielectric/SiO₂ interface as well interface trapped charge at the SiO₂/4H-SiC interface. Border traps and interface traps partly arise due to sputter induced damage of the surface. The sputter damage recovers partially after annealing at 950°C. Consistent with our previous statement, we found the negative charge reducing with reduced sputtering power due to reduced sputtering damage and lower concentration of tetrahedral Al³⁺. There was minimal contribution to this charge from Al-based dielectric bulk as deduced from almost linear shift in flat-band for different dielectric thickness. The *C-V* measurements reveal almost no hysteresis in *C-V* characteristics on samples with thermal SiO₂ IL. In contrast, the Al-based dielectric devices without IL thermal SiO₂ show moderate amount of hysteresis, which is indicative of charge trapping due to presence of slow traps. Also the amount of negative charge is much higher in absence of the thermal SiO₂ IL which is consistent with the results seen by other researchers. Leakage current characterization of these dielectrics showed Al-based dielectrics exhibiting excellent E_c with the AlN_y:H/SiO₂ sample being the best of all due to its dense amorphous structure. There is a reduction in the E_c of the AlN_y:H/SiO₂ sample after annealing at 950°C. We attribute this to phase transformation

Chapter 4 Dielectrics Characterization

from amorphous to polycrystalline, as was also revealed from the XRD results. The latter is known to suffer from defects and grain boundaries that reduce the electric field that is sustainable in the dielectric. The PECVD-SiO₂/SiO₂ film is comparable to the pure thermal oxide sample in terms of E_c , both of which remained unchanged after annealing. The AlN_y:H and AlN_x samples without the IL thermal SiO₂ exhibit comparatively higher leakage current and much lower E_c . This is attributed to the lower conduction band offsets between the dielectrics and 4H-SiC. There was marked increase in the leakage currents and further degradation in E_c when those AlN_y:H and AlN_x samples without the IL thermal SiO₂ underwent annealing.

The multi-step breakdown phenomena of sputter deposited aluminum nitride based high- k dielectric and thermal SiO₂ stack on 4H-SiC was investigated using measurements of dielectric relaxation currents on MIS capacitors. On the composite stack in terms of breakdown, SiO₂ proved to be the weakest link for as-deposited dielectrics. Nevertheless it is needed to reduce leakage currents due to the low conduction/valence band offset between 4H-SiC and the high- k dielectrics. Extreme electric field which is almost 2.5 times in the SiO₂ compared to that in the Al-based dielectric coupled with defects generated by electrons being injected into the SiO₂ leads to its eventual destruction. The breakdown of the Al-based dielectric may or may not follow instantaneously depending on the voltage at which the SiO₂ undergoes a breakdown. On the contrary, in a dielectric stack with a 950°C RTA, the high- k dielectric tends to breakdown first due to formations of defects and grain boundaries as result of annealing. This work demonstrated as-deposited AlN_y:H/SiO₂ stack on 4H-SiC with almost 30-40% higher breakdown strength compared to pure SiO₂. It truly opens up the possibility of using an alternative to SiO₂ in the form of Al-based high- k dielectric/SiO₂ stack for high voltage SiC devices.

Chapter 5

Unterminated 4H-SiC Schottky Barrier Diode

In this chapter we present the details of our fabrication process for unterminated 4H-SiC Schottky barrier diodes. The devices will be characterized in terms of their DC electrical properties. The effects of doping concentration, annealing conditions and passivation using a secondary layer of Al-based high- k dielectrics on the electrical characteristics of the devices will be presented and discussed. The barrier height dependence of different metal as schottky contacts with different metal work function will be evaluated. The breakdown voltages of unterminated SBDs with different drift layer doping concentration will also be presented.

5.1 Sample Description and Fabrication Process Details.

The samples used for these experiments consisted of 3 different sets of epilayer ready wafers, with a 10 μm n-type epilayer grown on 2" 4H-SiC (0001) 8° off-axis highly doped substrates, purchased from Cree Inc. The n-type nitrogen doping concentrations (N_D) of the epilayers in the three sets of samples are designed to be $2 \times 10^{15}/\text{cm}^3$, $3 \times 10^{15}/\text{cm}^3$ and $1 \times 10^{16}/\text{cm}^3$. The substrate doping has been estimated to be between $6.8 \times 10^{18}/\text{cm}^3$ to $1 \times 10^{19}/\text{cm}^3$. It was designed to be high in order to form good ohmic contacts at the back of the substrate after annealing. The wafers have been diced in to 5 mm $\times$ 5 mm pieces and used for device fabrication.

The process steps that are involved in the fabrication of SBDs are summarized as follows:

- 1) The bare samples were first degreased in acetone, isopropyl alcohol (IPA) and rinsed in deionized (DI) water. The samples were then cleaned using the standard Radio

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

Corporation of America (RCA) cleaning process to remove organic and heavy metal contamination on the surface. The samples were then stripped of native oxide by dipping in 1:10 dilute HF and then rinsed in DI water for 10 mins.

- 2) The samples then underwent a sacrificial oxidation process. A SiO₂ layer ~50 nm thick was grown on the surface by oxidation in pure O₂ at 1150°C for 3 hours. The samples have been loaded and unloaded in the oxidation furnace at 850°C. The sacrificial oxide was then stripped in dilute HF. The samples were again oxidized using the same process as above except that the oxidation duration was shortened to 1 to 2 hours to grow a device quality oxide ~10 to 20 nm thick followed by an additional 1 hour anneal in pure N₂ at 1100°C. This oxide acts as a layer of surface passivation for the final device, reducing surface leakage currents as well as protects the schottky periphery against strong electric fields and physical contaminations such as photoresist during processing. Nevertheless, we also prepared a few samples where this thermal oxide was etched off in dilute HF. These samples devoid of thermal oxide were specifically used in experiments involving study of surface passivation of 4H-SiC SBDs and its impact on electrical characteristics.
- 3) The SiO₂ on the back of the sample was then etched in dilute HF by covering the front side with photoresist. Ni or Pt metal around 100-200 nm thick has then been deposited on the backside. Following this rapid thermal annealing (RTA) was performed at 950°C/3 mins in N₂ to form silicided ohmic contacts at the backside of the wafers.
- 4) The front side of the samples where the schottky contact will be formed was patterned with circular openings, with diameters ranging from 200 µm to 900 µm.

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

The oxide in the openings was then etched using dilute HF solution and immediately loaded into the sputtering chamber or e-beam evaporation chamber to deposit one of the schottky metals (Pt, Ni, Ti, Au) with a thickness ranging from ~ 200 - 300 nm. The schottky contact formed may sometimes be subjected to a low temperature RTA at 450°C for 5 min in N₂.

- 5) For devices with a secondary layer of passivation, passivation dielectric which was either PECVD SiO₂ or Al-based high-*k* dielectrics (AlN_x, AlN_y:H, AlO₂) was then blanket deposited on the samples with a thickness of ~100-200 nm. The samples were then patterned using a passivation mask which will expose circular central openings on the schottky contacts with diameters ranging from 100 μm to 450 μm. The secondary passivation dielectric was then etched using reactive ion etching (RIE) based on a CF₄/O₂ gas mixture for SiO₂ and a BCl₃/Cl₂ gas mixture for Al-based dielectrics. The samples were then subjected to a post-passivation etch annealing at 300°C for 1 hour in nitrogen ambient. An optical picture of the fabricated final device is shown in Fig. 5.1.

Fig. 5.1 Optical picture of fabricated unterminated diode after passivation.

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

- 6) The fabricated devices were characterized electrically using a computer controlled semiconductor parameter analyzer HP4156C for forward bias measurements up to 5 V and reverse bias leakage current measurements up to -200 V. A HP4284A LCR meter has been used for C - V measurements at 1 MHz with a 25 mV signal and DC bias ranging from +1 V to -40 V. A high resolution Tektronix 370B curve tracer with a computer control has been used for breakdown voltage measurements. A cascade probe station with a faraday cage ensures extremely low levels of parasitic leakage making it possible to measure low levels of leakage currents with high accuracy. The probe station accompanied by a Temptronics temperature controller with a chiller enabled measurements at temperatures ranging from -50°C to 300°C.

5.2. Capacitance Voltage (C - V) Measurements for N-type Nitrogen Dopant Depth Profiling.

Unterminated diodes fabricated on samples from different sections of the wafers in this study have been subjected to C - V measurements using HP4284A LCR meter at 1 MHz to electrically probe the depth profile of N_D . The slope of measured inverse capacitances per unit area (A^2/C^2) as a function of the applied voltage (V) can be used to extract N_D . The slope corresponds to $2/\epsilon_{SiC}\epsilon_o q N_D$, where ϵ_{SiC} is the relative dielectric constant of 4H-SiC, ϵ_o is the permittivity of free space and q is the electronic charge. Figure 5.2 shows the dopant concentration as extracted from a typical $1/C^2$ versus V plot. N_D has a range of $1.75 - 2.2 \times 10^{15} / \text{cm}^3$, $2.9 - 3.5 \times 10^{15} / \text{cm}^3$, and $0.89 - 1.3 \times 10^{16} / \text{cm}^3$ for the three sets of samples, which are close to the designed values. Also shown in the same plot is the characteristic of the lowest doped sample at a temperature of 473 K. As is evident from the parallel shift in the characteristics, there is no additional ionization of dopants in this

temperature range. The dopant profile is an important input for us to estimate the breakdown voltage and assess the effectiveness of any edge termination technique.

Fig. 5.2 Capacitance-Voltage measurements on different doping samples for nitrogen dopant profile extraction at ambient and at 473 K.

5.3 Unterminated SBD Performance Characterization

The SBDs fabricated in this study using the 3 sets of samples with different N_D have been subjected to DC characterization at various temperatures. In this section, we will study the effects of temperature variations and epilayer doping concentrations on the forward bias turn on characteristics of these SBDs. The dependence on Schottky barrier heights on different metals has also being evaluated. Also impact of low temperature schottky contact annealing on the turn-on characteristics of the SBDs has been evaluated.

5.3.1 Temperature Dependence of J - V Characteristics.

Fig. 5.3 Forward current density- voltage (J - V) characteristics of a Ni/4H-SiC SBD at different temperatures. The inset shows the J - V characteristics on a linear scale. The current is clamped at 0.1 A which is the maximum permissible for HP4156C Semiconductor Parametric analyzer.

Figure 5.3 shows the current density versus voltage (J - V) characteristics for a SBD with Ni schottky metal as-deposited formed on the medium doped sample with $N_D = 3 \times 10^{15} / \text{cm}^3$. The devices were characterized over a range of temperature from 300 K to 573 K. The forward current density drops with increasing temperature due to a reduction in electron mobility while leakage current increases as per thermionic emission theory [90].

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

Nevertheless, as seen the leakage currents are low, even at a temperature as high as 573 K. From the J - V curves, the barrier heights were deduced to vary from ~ 1.5 eV at 300 K to ~ 1.4 eV at 573 K. One of the reasons for the small drop in barrier height is band-gap lowering which occurs at higher temperature, [10] while the other reasons could be entropy of electron hole pair transitions in some defect states matching the entropy of electron hole pair generation due to band gap narrowing, as a result of thermal energy increase [91].

5.3.2 Kink in the Forward Bias J - V Characteristics of SBDs.

Fig. 5.4 Ni/4H-SiC SBD RT Forward J - V characteristic showing a kink in the turn-on region.

Most SBDs fabricated in our study showed good agreement with thermionic emission current model with a single linear region in the current density-voltage (J - V) plots.

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

However, some devices exhibited a kink in the turn-on characteristics as shown in Fig. 5.4. These devices exhibit a higher level of leakage current as compared to normal devices without the kink. As seen from Fig. 5.4, we observe two linear regions with different ideality factors and barrier heights. At lower voltages, a region with a lower Schottky barrier height (SBH) $\phi_{BL}=1.15$ eV and an ideality factor $\eta_L=1.0564$ is seen, while at higher voltages, the SBH and ideality factor have increased to $\phi_{BH}=1.45$ eV and $\eta_H=1.1303$ respectively. These two schottky diodes conduct in parallel giving rise to the overall current [92]. The two diodes have different areas which add up to the area of the original device. This deviation from the ideal schottky barrier interface can be explained in terms of defects such as difference in the crystal symmetry of the metal with respect to the semiconductor or variation in orientation at the metal–semiconductor interface, due to localized faceting of the interface which has been observed to create inhomogeneities in the SBH [93]. Other reasons attributed for this anomaly includes contamination of schottky metal, formation of mixture of different metallic phases of schottky metal with different Schottky barrier heights, dopant clustering [93].

5.3.3 Schottky Metal Dependence of Barrier Height

The J - V characteristics of the Schottky devices formed with various metals as-deposited are shown in Fig. 5.5. We have extracted the barrier heights for the SBDs and the results are shown in Fig. 5.6 as a function of the metal work function. Our barrier height results are quite consistent with those found in the literature. [10, 27-30] It can be seen that the barrier height is correlated to the metal work function suggesting that the pinning of the Fermi level is only partial. It is further noted that the contact formed using Ti has the smallest Schottky barrier height of ~ 0.87 eV, while that formed using gold (Au) gives the largest barrier height

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

of ~ 1.77 eV. The Ti device has the smallest turn-on voltage and also exhibits the largest leakage current due to increased thermionic emission over the barrier.

Fig. 5.5 Forward bias J - V characteristics of metal/4H-SiC SBD formed using different metals. The inset shows the J - V characteristics on linear scale. The current is clamped at 0.1 A which is the maximum permissible for HP4156C Semiconductor Parametric analyzer.

Fig. 5.6 Experimental barrier height plotted against schottky metal work function. The schottky contacts have been formed with metals as-deposited. Clearly there is some dependence of barrier height on metal work function which suggests the pinning of Fermi level is only partial.

5.3.4 Epilayer Doping Effects on Forward Bias J - V Characteristics.

We have plotted the forward turn-on characteristics of a Pt/4H-SiC SBD formed on epilayers with the highest and lowest drift layer doping N_D as shown in Fig. 5.7. As seen the device with the highest doping of $N_D = 1 \times 10^{16} / \text{cm}^3$ shows the highest current density due to its much lower turn-on resistance R_{on} . The drawback in having a higher N_D is a lowering of the blocking voltage capability. Thus a suitable compromise has to be struck between having a low R_{on} and large V_B .

Fig. 5.7 Forward turn-on characteristics of Pt/4H-SiC SBD formed on epilayers with different drift layer doping N_D . The inset shows the J - V characteristics on a linear scale.

The current is clamped at 0.1 A which is the maximum permissible for HP4156

Semiconductor Parametric analyzer.

5.3.5 Effects of Schottky Contact Annealing on the Forward J - V Characteristics.

The effects of a low temperature Schottky contact annealing using a 450°C/5 min anneal in N_2 was evaluated on few samples with $N_D = 1 \times 10^{16} / \text{cm}^3$ and Ni as Schottky metal. We have plotted in Fig. 5.8 the R_{on} and barrier heights for the as-deposited and annealed (450°C for 5 min in N_2) Ni schottky contacts at different temperatures. Thus these two samples with Ni schottky contacts with and without anneal can be used to study the impact of annealing on Schottky characteristics. Also plotted in the same figure, we have the R_{on} and barrier heights of as-deposited Pt SBDs on samples with $N_D = 3 \times 10^{15} / \text{cm}^3$ at different temperatures. Thus

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

the temperature dependence of R_{on} can be compared for the two different doped samples (Ni/4H-SiC as-dep. with $N_D = 1 \times 10^{16} / \text{cm}^3$ and Pt/4H-SiC as-dep. with $N_D = 3 \times 10^{15} / \text{cm}^3$). The contribution to R_{on} is mainly from the series resistance of the drift layer and the back side ohmic contact resistance. Thus even though the Schottky metal for the two samples mentioned above are different, the R_{on} comparison is still meaningful.

Fig. 5.8 Barrier height and R_{on} trends vs. Temperature for Ni Schottky contacts as deposited and with Schottky contact annealing (450°C for 5 min in N_2) for $N_D = 1 \times 10^{16} / \text{cm}^3$. Also shown is the barrier height and R_{on} for Pt 4H-SiC SBDs with $N_D = 3 \times 10^{15} / \text{cm}^3$ for R_{on} temperature dependence comparison with lower doped Ni SBDs.

As seen R_{on} is the smallest for the highest doped epilayer. A curve fit of the R_{on} with temperature (T) indicates a $\sim T^{2.2}$ temperature dependence which is quite similar to

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

$1.1 \times 10^{-8} T^{2.1}$ ohm-cm² observed by Itoh *et al.* [94]. The only difference between their and our structure is the fact that they used gold (Au) as schottky metal and the N_D for their 4H-SiC epilayer was around 5×10^{15} /cm³. Also seen from the figure is that N₂ annealing has increased the SBH slightly, possibly due to reduction in surface states which will partially relieve the pinning of the Fermi level at the surface. Also the initial increase in barrier height for as-deposited Ni/n- (1×10^{16} /cm³) SBD could be due to annealing effect with increased temperature.

5.4 Breakdown Voltage Measurements of Unterminated 4H-SiC SBDs.

Figure 5.9 shows the box plot distribution of the breakdown voltage V_B for the 3 sets of SBDs with different N_D . We define V_B as the voltage where either the leakage current exceeded 10 μ A or increased by more than one order of magnitude compared to that measured in the previous voltage step. The schottky contacts for all these samples were formed using as-deposited Pt metal. The devices have an active area with a diameter of 200 μ m. Around 25-40 devices have been measured for each doping type and used for the box plot representation. The center line within the box plot represents the median; the upper and lower boundaries of the box represent the 75th and 25th percentile data points respectively while the upper and lower whiskers represent 95th and 5th percentile points respectively. The dots represent the outliers. As seen V_B degrades drastically as the doping is increased, with the devices undergoing a premature breakdown due to extreme field enhancements at the device periphery.

Chapter 5 Underminated 4H-SiC Schottky Barrier Diodes

Fig. 5.9 Breakdown voltage V_B for underminated 4H-SiC SBDs for different N_D .

Chapter 5 Underminated 4H-SiC Schottky Barrier Diodes

Fig. 5.10 Leakage current characteristics of underminated 4H-SiC SBDs up to the point of breakdown.

The typical leakage currents (I - V) characteristics up to the point of breakdown for the 3 sets of devices with different N_D are shown in Fig. 5.10. The abrupt jump as seen in the leakage current is typical of edge related breakdown, which is unlike avalanche multiplication induced breakdown where the rise in the leakage current is relatively gradual.

5.5 Passivation of 4H-SiC Unterminated Diodes Using Al-based High- k Dielectrics.

A layer of passivation not only protects a device from environmental hazards but also plays a dominant role in improving its electrical characteristics. A SiO₂ passivation layer has been shown to improve the forward blocking voltage of 4 kV 4H-SiC thyristors [95] and lower the reverse leakage currents in 4H-SiC mesa PiN diodes by reducing the surface states [96]. SiO₂ and SiN based films have been far most acceptable and reliable form of passivation for almost past four decades. Nevertheless this has been changing. A recent application has shown the benefits of using AlN rather than conventional SiN as passivation. A low-loss high power switching device with high current handling capacity, which could be useful for high-power systems such as inverters for home electric appliances and switching power supplies, was demonstrated based on an AlGaIn/GaN heterogeneous transistor (HFET) on sapphire with thick poly-crystalline AlN (poly-AlN) as passivation [69]. With AlN as passivation, it was shown the breakdown of HFET immensely improved and leakage currents reduced. The thermal profile of the device was shown to be much more uniform and stable due to excellent thermal conductivity of AlN passivation film.

SiO₂, which is the most commonly used passivation dielectric for SiC devices, has a dielectric constant $k \sim 3.9$ which is almost 3 times lower than that of SiC of 9.7, and as a result experiences extreme electric field on the surface of the devices. Though Si₃N₄ with a higher and more comparable $k \sim 7.5$ is a good replacement for SiO₂ in terms of lowering the electric field, it is not suitable for high temperature (as high as 300°C) 4H-SiC device applications due to its low thermal conductivity. In contrast, AlN and Al₂O₃ are excellent candidates with high thermal conductivities, moderately higher k and similar bond length as well as thermal expansion coefficients to SiC [15]. In fact, Ligatchev *et al.* [97] have shown that AlN deposited on SiC has much lower defect densities compared to those deposited on Si. With the addition of hydrogen to AlN film, the film becomes denser; roughness is

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

reduced and the film becomes stress free [16, 17], which is perfectly suited for application as a passivation dielectric. We investigated the application of SiO₂ deposited by the plasma enhanced chemical vapor deposition (PECVD) technique and sputter deposited AlN_x, AlN_y:H and AlO_z as passivation layers for 4H-SiC SBDs. Some SBDs were incorporated with a thin intermediate layer of thermally grown SiO₂, since thermal SiO₂ can improve the interface quality by offering an increased conduction and valence band-offset (~3.2 eV with interfacial SiO₂ vs. ~1.5 eV without interfacial SiO₂ for conduction band) and reduced interface charge [73, 98].

5.5.1 Passivation Experimental Details

The samples used for these experiments consist of the medium doped samples with $N_D = 3 \times 10^{15}/\text{cm}^3$. The samples were processed as per the steps outlined in Section 5.1. Pt metal has been used as schottky metal and also for ohmic contact formation. We would like to again emphasize the fact that while most samples retain their thermal oxide, a few samples had the thermal oxide surrounding the schottky contact etched off by a dip in dilute HF just before the deposition of the secondary passivation layer.

A number of passivation materials, which include PECVD silicon dioxide (SiO₂), sputter deposited aluminum nitride (AlN_x), hydrogenated aluminum nitride (AlN_y:H) and aluminum oxide (AlO_z) were then deposited to a thickness of around 1000 Å. The PECVD oxide was deposited at 350°C using silane (SiH₄) and nitrous oxide (N₂O) with a flow rate of 50 sccm and 250 sccm respectively. AlN_x, AlN_y:H and AlO_z were deposited using a 13.56 MHz RF magnetron sputtering system (Denton) from a pure Al target (99.99%) in an Ar/N₂, Ar/N₂/H₂ and Ar/O₂ environments respectively. In all the above depositions, the Ar flow rate was maintained at 10 sccm while those of N₂, N₂:H₂ (80%:20%) and O₂ were maintained at 25 sccm. The substrate holder was intentionally cooled through chilled water

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

circulating within the chuck. The sputtering RF power was kept to a low value of 200 W to reduce sputtering induced damage on 4H-SiC. The sputter deposition rate was ~ 0.05 $\mu\text{m/hr}$ for $\text{AlN}_y\text{:H}$, ~ 0.1 $\mu\text{m/hr}$ for AlN_x and ~ 0.025 $\mu\text{m/hr}$ for AlO_z . The samples were then subjected to a post-passivation etch annealing at 300°C for 1 hour in a nitrogen ambient. For comparison, we also have some control samples which were not passivated at all. This was done by having the thermal oxide removed and with no passivation layer deposited.

5.5.2 Passivation Experimental Results and Discussion

As discussed previously in Chapter 4, we have characterized the Al-based dielectrics on MIS capacitor structures to extract some basic electrical parameters such as dielectric constant and net dielectric charge. Our C - V measurements revealed a value of dielectric constant of k around 8.2 to 8.5 for AlN_x and $\text{AlN}_y\text{:H}$, a k around 9.1 to 9.3 for AlO_z and a k around 3.8 to 4 for PECVD SiO_2 . It also revealed a presence of a net positive charge for the PECVD oxide and a net negative charge for the Al-based dielectrics. The dielectric net negative charge are of much higher densities on AlO_z dielectric ($Q_F = -1$ to $-3 \times 10^{12}/\text{cm}^2$) as compared to AlN_x and $\text{AlN}_y\text{:H}$ (refer to Table 4.1). These results are consistent with those reported in the literature [65-67, 73-76]. As was discussed in the chapter 4, without the presence of a thin interfacial thermal oxide layer, the Al-based dielectrics are leaky due to small conduction band offset, exhibits low breakdown strength, and very high density of net negative charge.

Fig. 5.11(a) illustrates typical leakage current characteristics up to -200 V of reverse bias voltage for 200 μm diameter samples with an interfacial layer of thermal SiO_2 (except for the control sample). These samples with only thermal oxide layer were measured before passivation deposition and are shown in the figure with symbols shaded in dark. This has been done in order to gauge the initial level of leakage current which can vary from device

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

to device due to normal dispersion. Following this the passivation layers were deposited and the same devices were remeasured and shown in the figure using the same symbols but without any dark fill. Thus identical symbols with and without dark fill corresponds to the same device without and with deposited passivation respectively.

Fig. 5.11(a) Leakage current characteristics with and without passivation of 4H-SiC SBD samples but with an intermediate thermal oxide layer.

Also shown is the leakage current characteristic of the control sample, which is totally devoid of any kind of passivation that includes the thermal oxide and deposited dielectric. As can be seen the control sample is quite leaky and the leakage current increases sharply with the reverse bias voltage. If we define the breakdown voltage as the voltage at which the leakage current exceeds 1 nA then clearly the control sample has a much lower

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

breakdown voltage of around -200 V. This is much lower than the breakdown voltage of -400 to -500 V from our measurements for devices with just thermal oxide and before passivation deposition. This clearly highlights the importance of having at least a thermal oxide on the surface, which helps in reducing parasitic surface leakage due to moisture and some other factors, as well as to some extent helps in protecting the schottky corners against edge effects. Table 5.1 shows the leakage current levels as extracted at -200 V of reverse bias before and after passivation. The leakage current reduction ratio refers to the ratio of leakage current before and to that after passivation. It basically signifies the amount by which leakage current reduced (if leakage current ratio is greater than 1) or increased (if ratio is less than 1) after passivation deposition. As seen from Table 5.1 there is a reduction in the leakage currents with a passivation layer deposited. For the PECVD SiO₂ the reduction in the leakage current at -200 V reverse bias is about 5 times from an initial value of 27.11 pA without deposited SiO₂ to a final value of 5.33 pA with deposited SiO₂. This reduction is smaller compared to those observed for the samples with Al-based dielectrics of almost 10 to 200 times in magnitude (refer to Table 5.1).

Table 5.1 Leakage currents at -200 V reverse bias for 4H-SiC SBD devices with diameter 200 μm , with and without deposited passivation.

Deposited passivation dielectric	Leakage current without passivation (A)	Leakage current with passivation (A)	Leakage reduction ratio
PECVD SiO ₂	2.711×10^{-11}	5.33×10^{-12}	5.1
AlN _x	2.269×10^{-11}	2.413×10^{-12}	9.4
AlN _y :H	6.35×10^{-11}	3.368×10^{-13}	188.5
AlO _z	1.094×10^{-10}	5.723×10^{-12}	19.11

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

In particular, for the device illustrated in the Fig. 5.11(a) with AlO_x passivation, the initial level of leakage current before AlO_x passivation is slightly higher with the device showing typical signs of edge related tunneling, as evident from the sharp rise in the leakage current at the extreme end of the voltage sweep [99]. The increased edge electric field reduces the width of tunneling barrier, resulting in an increase in the tunneling currents at these locations. As can be seen there is almost ~20 times reduction in the leakage current after AlO_x passivation, with the final leakage current characteristics quite smooth if not perfectly flat. We can attribute this to the fact that AlO_x has a higher dielectric constant compared to PECVD SiO_2 , which leads to a lowering of field enhancement at the edge. This is also true for other Al-based dielectric films. The net negative charge within the Al-based dielectric depletes the 4H-SiC surface of electrons around the periphery of the schottky contact reducing surface recombination and leading to a further reduction in the leakage currents. Among the Al-based dielectrics, the most effective in reducing the leakage current is $\text{AlN}_y\text{:H}$ where we see a reduction by almost 188 times in magnitude for the device illustrated in Fig. 5.11(a). It is believed the hydrogen in the passivation layer plays a key role in passivating the surface dangling bonds and thus reducing the surface states. This results in a larger barrier height and leads to a further reduction in the leakage currents. We would like to highlight the fact that the 300°C post-passivation anneal does not degrade the schottky contact since 300°C is too low a temperature to cause any real interface reaction between 4H-SiC and Pt schottky metal. Pt/4H-SiC contact is thermally very stable given the inert and refractory nature of Pt metal. This is further reinforced by the fact that some of our control samples, which are totally devoid of any passivation and subjected to a 300°C anneal similar to the passivated samples, showed no change in their electrical characteristics before and after anneal. Nevertheless the 300°C anneal does help passivated samples in terms of providing thermal energy to distribute the hydrogen within the film and also helps with the densification of the passivation film.

Fig. 5.11(b) Leakage current characteristics with and without passivation of 4H-SiC SBD samples but without intermediate thermal oxide layer.

Figure 5.11(b) shows the leakage current characteristics for samples without the intermediate SiO_2 layer. Again identical symbols with and without dark fill corresponds to the same device without and with the deposited passivation layer respectively. As can be seen, there is a marked increase in the leakage current for devices after deposition of sputtered Al-based dielectrics (symbols without dark fill) compared to measurements before passivation deposition (symbols with dark fill). This can be attributed to the poor interface quality and increased leakage current through the passivation dielectric itself due to the small conduction band offset between the passivation layer and 4H-SiC. The surface damage caused by sputtering also leads to an increased surface leakage current, increased surface states and reduced barrier and hence results in an overall increase in the leakage

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

current under reverse bias. For the PECVD SiO₂, the leakage current is again reduced by about one order of magnitude compared to before SiO₂ deposition. This can be attributed to the fact that our PECVD SiO₂ film has excess hydrogen from the reactant gas SiH₄ that has been diluted to 10% in H₂. Again low surface damage from the PECVD deposition with the presence of excess hydrogen helps to passivate the dangling bonds, increase the barrier height and reduce the leakage currents.

Forward bias measurements have also been carried out to compare the ideality factor (η) and barrier height (ϕ_B) with and without the passivation layer. Figure 5.12(a) and (b) show the box plot distribution of η and ϕ_B respectively based on measurements of about 25 devices per device type. For reference the η and ϕ_B of the control sample are around 1.1 and 1.32 eV respectively. If we compare devices with a particular passivation dielectric with and without the passivation layer, it is evident from the figures that for the samples with the interfacial thermal SiO₂ layer, while η is almost the same there is an improvement in ϕ_B by around 0.05-0.1 eV. An increase by as much as 0.2 eV for ϕ_B has been obtained for samples with AlN_y:H passivation, which is also consistent with the much reduced leakage currents seen in the earlier measurements.

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

Fig. 5.12 (a) Ideality factor (η) (b) Barrier height (ϕ_B) of 4H-SiC SBDs with and without passivation.

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

From the discussion in Chapter two, the interface/surface state density D_{it} is related to ϕ_B through [33, 100]

$$\phi_B = \gamma(\phi_M - \chi_s) + (1 - \gamma)(E_g - \phi_{i0}) \quad (4-1)$$

$$\gamma = \varepsilon_i / (\varepsilon_i + q\delta D_{it}) \quad (4-2)$$

where q is the electronic charge, ϕ_M is the metal work function, χ_s the semiconductor affinity, E_g the 4H-SiC energy gap, ϕ_{i0} the interface neutrality level which determines the magnitude of charge transfer and the resulting interface dipole, δ the thickness of the interfacial region between the metal and the semiconductor, ε_i the dielectric permittivity of the interfacial region and γ accounts for the slope of ϕ_B vs. ϕ_M curve. For an ideal metal-semiconductor interface with no Fermi level pinning, $\gamma=1$. It is noteworthy that the lower the D_{it} (i.e., when electronic passivation occurs), the more $\gamma \rightarrow 1$, and ϕ_B improves as in our case and approaches the theoretical Schottky–Mott limit of $\phi_M - \chi_s$. For the samples without the intermediate SiO₂ layer, there is an increase in η and reduction in ϕ_B indicating a deterioration of the interface due to the sputter damage and increase in surface states at the Pt/4H-SiC interface.

The samples with intermediate thermal oxide and AlN_y:H dielectrics have been further investigated using 1 MHz C - V measurements. The measured inverse capacitances per unit area (A^2/C^2) as a function of the applied voltage (V) with and without the AlN_y:H dielectric are shown in Fig. 5.13. The part of C^{-2} vs. V curve under forward bias is used to account for the interface states analyzed using Fonash's model [101]. The reason being

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

under forward bias, the deep donor levels are below the Fermi level, unionized and hence do not contribute to the capacitance. Under forward bias only the shallow donors and interface states control the slope of C^{-2} vs. V curve.

Fig. 5.13 High frequency (1 MHz) C-V characteristics of 4H-SiC SBDs with and without $\text{AlN}_y\text{:H}$ as passivation.

The C-V relation for a schottky diode can be then expressed as [100, 101]

$$\frac{A^2}{C^2} = \left(\frac{1}{1 + \alpha} \right) \frac{2}{\epsilon_{\text{SiC}} \epsilon_o q N_D} (V_{bi} - V - \frac{kT}{q}) \quad (4-3)$$

$$\alpha = \frac{q N_s \delta}{\epsilon_i} \quad (4-4)$$

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

where A is the area of the Schottky barrier contact, C is capacitance, $\epsilon_{SiC}=9.7$ is the relative permittivity of SiC, ϵ_o is the permittivity of free space, k is the Boltzmann constant, T is the absolute temperature, N_D is the dopant concentration, V_{bi} is the built-in voltage and N_s is the surface state density. An approximate calculation for α , assuming a non-intimate metal-SiC interface consisting of oxide with $\delta=10 \text{ \AA}$ and with the highest value of N_s as high as $1 \times 10^{13}/\text{cm}^2$ (justified by our deduction of N_s to be discussed shortly), reveals that α is still much smaller compared to 1. Thus we can comfortably ignore α in eqn. (4-4). From the plot of A^2/C^2 vs. V , we can deduce N_D from the slope for the samples with and without passivation, and they are found to be $2.542 \times 10^{15} \text{ cm}^{-3}$ and $2.60 \times 10^{15} \text{ cm}^{-3}$ respectively. From the intercepts on the voltage axis, the V_{bi} for samples with and without passivation are deduced at room temperature to be 1.496 V and 1.341 V respectively.

The Schottky barrier height $q\phi_B$ is related to V_{bi} by the relationship

$$q\phi_B = qV_{bi} + qV_n \quad (4-5)$$

where $V_n = (kT/q)\ln(N_c/N_D)$ is the potential difference between the conduction band and the Fermi level of the n -type 4H-SiC. $N_c = 1.689 \times 10^{19} \text{ cm}^{-3}$ is the density of states in the conduction band for 4H-SiC [3, 54] while the value of N_D used was deduced from the slope of the A^2/C^2 vs. V curve previously. This leads to a $q\phi_B$ of 1.569 eV and 1.725 eV before and after passivation deposition respectively.

For n -type semiconductors, the Schottky barrier height $q\phi_B$ is given by

$$q\phi_B = q\phi_M - q\phi_s + qV_n \quad (4-6)$$

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

where $q\phi_m = 5.65$ eV [3] is the work function of the Schottky metal (Pt in this case) and $q\phi_s$ is the surface work function of n -type 4H-SiC given by

$$q\phi_s = qV_n + \chi_s + q|V_s| \quad (4-7)$$

In the above $q|V_s|$ is the surface band bending energy which is related to N_s by the relationship

$$q|V_s| = \frac{(qN_s)^2}{2\epsilon_s N_D} \quad (4-8)$$

We can deduce the surface state density N_s by assuming $\chi_s = 3.8$ eV [3] for 4H-SiC and by using eqn. (4-6) to (4-8), with a $q\phi_b$ of 1.569 eV and 1.725 eV without and with deposited passivation respectively. We deduced $N_s = 8.847 \times 10^{10}/\text{cm}^2$ without deposited AlN_y:H and $N_s = 5.839 \times 10^{10}/\text{cm}^2$ with AlN_y:H deposited. At this point, we would like to mention that our earlier assumption that α is much smaller compared to 1 and can be neglected in eqn. (4-3) has been vindicated from the values of N_s as deduced above. α as seen from eqn. (4-4) is directly proportional to N_s and was very small for value of N_s as high as $1 \times 10^{13}/\text{cm}^2$. Thus α in actual case will be almost three orders smaller for our values of N_s . Our C - V results are again consistent with our I - V measurements results, which show that with passivation there is an improvement in ϕ_b as result of the reduced surface band bending V_s and reduced surface state density N_s by as much as 30%.

5.6 Conclusions

In conclusion, in this chapter, fabrication process details and electrical characterization results of unterminated 4H-SiC SBDs were studied. The C - V measurements revealed the n-type doping N_D for 3 sets of samples purchased from Cree Inc. were around $2 \times 10^{15} \text{ cm}^{-3}$, $3 \times 10^{15} \text{ cm}^{-3}$ and $1 \times 10^{16} \text{ cm}^{-3}$ which are close to their designated values. A study of effects of temperature variations on the forward turn-on characteristics reveals stable forward bias operation even at 573 K with extremely low levels of reverse bias leakage currents. There is an increase in R_{on} and slight reduction in barrier height as temperature increases from 300 K to 573 K. A kink in the forward turn-on characteristics seen sometimes has been attributed to inhomogeneities of barrier height due to localized faceting of the interface. SBDs formed using various metals reveals the barrier height is quite correlated to metal work function suggesting the pinning of Fermi level on 4H-SiC is only partial. Among the metal studied (Ti, Ni, Pt, Au) it was found that the contact formed using Ti has the smallest Schottky barrier height of $\sim 0.87 \text{ eV}$, while that formed using gold (Au) gives the largest barrier height of $\sim 1.77 \text{ eV}$. For SBDs formed using different drift layer doping, the device with the highest doping of $N_D = 1 \times 10^{16} / \text{cm}^3$ shows the highest current density due to its much lower turn-on resistance R_{on} . The drawback in having a higher N_D is a lowering of the blocking voltage capability. The breakdown voltage reduced from between 600-700 V for $N_D = 2 \times 10^{15} / \text{cm}^3$ to 300-400V when N_D increases to $1 \times 10^{16} / \text{cm}^3$. A low temperature annealing of schottky metal using $450^\circ\text{C}/5 \text{ min}$ in N_2 was shown to increase the SBH slightly, possibly due to reduction in surface states which will partially relieves the pinning of the Fermi level at the surface. A comprehensive study of passivation of 4H-SiC SBDs using Al-based dielectric was carried out. It was shown this passivation scheme can give rise to a remarkable reduction in reverse bias leakage currents, improvement in barrier height and ideality factor. These improvements can be attributed to the higher values of k on these dielectrics which leads to reduced edge electric field enhancements, a net negative charge which leads to a

Chapter 5 Unterminated 4H-SiC Schottky Barrier Diodes

surface depletion reducing surface recombinations, a reduction in surface leakage currents and surface states. It was found that an interfacial layer of thin thermal oxide (~5-10 nm) is necessary to gain these advantages since without the interfacial oxide the interface quality is poor with very high density of negative charge. In addition without the interfacial oxide, there is increased tunneling leakage current through the dielectric due to small conduction band offset with 4H-SiC and increased leakage due to sputter induced surface damage. Other advantages of Al-based passivations include much better heat dissipation due to high thermal conductivity which reduces self heating effects which has been know to be a major cause of gain reduction under continuous wave operation in power devices such as MESFETs.

Chapter 6

Field Plate Terminated 4H-SiC Schottky Barrier Diodes

In this chapter we present the fabrication process and discuss the experimental results obtained for Field Plate (FP) terminated 4H-SiC Schottky barrier diodes (SBDs) formed using the Al-based dielectrics. The results will be compared with those obtained for FP terminated SBDs based on conventional SiO₂. We will also draw comparison between the results obtained for FP terminated 4H-SiC SBDs and the simulation results presented in Chapter three, as well as the results for unterminated SBDs presented in Chapter five.

6.1 FP Terminated Device Process and Fabrication Details

The details of the fabrication process of 4H-SiC FP terminated SBDs are discussed below. While the final structure of the fabricated device is as shown in Fig. 6.2, the process steps needed to fabricate the same are being illustrated in the schematic process flow as shown in Figs. 6.1(a)-(d).

- 1) The samples used for these experiments consist of the lowest doped drift layer samples with $N_D = 2 \times 10^{15} / \text{cm}^3$ and 10 μm thick epilayer purchased from Cree Inc., which have been diced into 5mm $\times$ 5mm pieces. The C - V measurements to confirm the n-type nitrogen doping have been presented in Fig. 5.2.
- 2) The samples have been first degreased in Acetone and IPA and rinsed in DI water thoroughly. They were then subjected to a standard RCA clean, followed by a dip in dilute HF to strip the native oxide and rinsed in DI water for 10 mins. The samples

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

then underwent a sacrificial oxidation process. A sacrificial SiO_2 layer ~ 50 nm thick was grown on the surface by oxidation in pure O_2 at 1150°C for 3 hours. The samples have been loaded and unloaded in the oxidation furnace at 850°C . The sacrificial oxide was then stripped in dilute HF to prepare a fresh surface for device processing

- 3) The samples were then oxidized in dry O_2 at 1150°C for 3 hrs, followed by 1 hr anneal in N_2 at 1100°C . The samples have been loaded and unloaded into the furnace tube at 850°C . A thin layer of thermal oxide grown with a thickness (t_{IL}) ~ 50 nm was used as an intermediate layer (IL) between the Al-based high- k dielectrics and 4H-SiC. For comparison, some samples were prepared without the oxide layer, by stripping the layer in dilute HF. After clearing the oxide on the backside with HF, a backside ohmic contact was formed using sputter deposited Pt, which was then subjected to a 950°C rapid thermal anneal (RTA) in N_2 for 60 s. The structure of the device after sacrificial oxidation and ohmic contact formation phase is as depicted in Fig. 6.1(a).

**Perform Clean, Sacrificial Oxidation
followed by device quality thermal SiO_2 growth**

Fig. 6.1 (a) Sample after initial clean, sacrificial oxidation, device quality SiO_2 growth and ohmic contact formation.

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

- 4) Following this the FP dielectrics were deposited, using the plasma enhanced chemical vapor deposition (PECVD) technique for SiO_2 and 13.56 MHz RF magnetron reactive sputtering for Al-based dielectrics. The process details have been presented in Chapter four. The thickness of the deposited dielectrics (t_{dep}) ranges from around 0.05 μm to 1.3 μm . Based on our dielectric characterization results from chapter four which showed the dielectric breakdown strength degraded on annealing, no post deposition annealing of these dielectric films was performed. This was done to maintain the amorphous nature of these RT sputter deposited dielectrics.
- 5) The dielectrics were subsequently patterned using a double coated layer of photo resist (PR) AZ1518 as depicted in Fig. 6.1(b). The samples were baked for 45 min at 105 $^{\circ}\text{C}$ after PR development and such that the PR served as a hard mask (HM). The double coating ensured a thick photo resist HM ($\sim 5 \mu\text{m}$) which was needed to withstand subsequent dielectric reactive ion etching (RIE).

Fig. 6.1 (b) Sample after dielectric deposition and patterning with double coated layer of PR AZ1518 baked for 45 min to form a hard mask.

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

- 6) A Cl_2 (25 sccm)/ BCl_3 (100 sccm)/Ar (10 sccm) plasma formed at a RF power of 300 watts was used to dry etch AlN_x and $\text{AlN}_y\text{:H}$. This was then followed by a wet etch using AZ400K developer. AZ400K, a potassium hydroxide (KOH) based solution, was used to wet etch the Al-based dielectrics to avoid RIE damage to the 4H-SiC surface. For those samples with PECVD SiO_2 as FP, a CF_4 (100 sccm)/ O_2 (10 sccm) plasma formed at a RF power of 150 watts was used to etch the PECVD SiO_2 . Good control of the dry etch rate was needed to avoid any RIE induced damage to the 4H-SiC surface. Hence the thickness of the deposited dielectrics and the etch rates have been closely monitored using a NanoCalc-2000 thin film reflectometry system [102]. Finally, the remaining thermal oxide for those samples with the IL was wet etched in dilute HF solution. The structure of the device after dielectrics dry and wet etch is as depicted in Fig. 6.1(c). The resist, which served as HM, was finally stripped very cleanly using a warm (60°C) solution of resist stripper AZ300T.

Fig. 6.1 (c) Sample after dielectric dry etch using RIE and wet etch using a sequential wet etch in KOH based AZ400K followed by etch in dilute HF to strip the thermal oxide.

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

- 7) The samples were again patterned with circular openings for the schottky metal deposition. All samples underwent a 5 sec dip in dilute HF to remove native oxide just before being loaded into the sputter chamber for Schottky metal deposition. The structure of the device just before Schottky metal Pt deposition is as shown in Fig. 6.1(d). Pt with a thickness of around 200-300 nm was sputter deposited and lift-off in acetone to form devices with an active area diameter of 200 μm , overlapping the dielectric by 10 μm and 25 μm for two sets of devices.

Fig. 6.1 (d) Sample after patterning for schottky metal deposition with some overlap on the dielectric.

The final structure of the fabricated device is shown in Fig. 6.2(a). Figure 6.2(b) is an optical picture of an actual completed device with a 10 μm overlap. There is minimal alignment error, with an actual measurement of the overlap close to 10.2 μm as seen in the picture.

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

Fig. 6.2 a) Schematic of the 4H-SiC Schottky diode fabricated detailing the epilayer thickness, doping concentration (N_D), length of metal overlapping the deposited dielectrics ($t_{overlap}$) and thickness of the deposited dielectric (t_{dep}). The figure is not to the scale (b)

Optical picture of a completed device with a 10 μm overlap.

6.2 FP Terminated SBDs Forward Bias Characterization Results

The fabricated SBD devices were first tested for their turn-on characteristics at two different temperatures of 300 K and 573 K. Based on the characterization results of MIS capacitor presented in Chapter 4, only as-deposited Al-based dielectrics were investigated since annealing has been found to degrade the dielectric breakdown strength. Figure 6.3 shows the typical current density-voltage (J - V) characteristics of the devices with $t_{dep} = 0.45 \mu\text{m}$ (refer to Fig. 6.2(a)).

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

Fig. 6.3 Forward turn-on characteristics of the FP terminated SBDs at 300 K and 573 K.

As seen the devices exhibit excellent characteristics with forward current density (J_F) reaching 100 A/cm^2 at roughly 1.7-1.9 V at 300 K. The same J_F of 100 A/cm^2 is achieved at around 2.7 V when measured at 573 K, due to the much higher drift resistance (R_{on}) as a result of the reduced electron mobility. The measurements at 300 K reveal an ideality factor (η) between 1.02-1.09, indicating a good Pt/4H-SiC interface with no RIE related damage to the surface. The barrier heights (ϕ_b) for the devices extracted from the J - V characteristics are between 1.31-1.49 eV at 300 K. These are reduced to 1.15-1.28 eV at 573 K. One of the reasons for the small drop in barrier height is band-gap lowering which occurs at higher temperature [10], while the other reasons could be entropy of electron hole pair transitions in some defect states matching the entropy of electron hole pair generation due to band gap narrowing, as a result of thermal energy increase [91].

6.3 FP Terminated SBDs Breakdown Voltage Characterization

The devices were characterized in terms of their breakdown voltage V_B using a high resolution Tektronix 370B curve tracer. We define V_B as the voltage where either the leakage current exceeded 10 μA or increased by more than one order of magnitude compared to that measured in the previous voltage step. The voltage step-size varied from around 16 V to 40 V depending on the voltage sweeping range needed, which in turn was determined by the dielectric used. Figure 6.4 shows the V_B vs. dielectric thickness (t_{dep}) characteristics. Also shown for comparison is the V_B of unterminated devices and FP devices with just thermal oxide as the dielectric, which corresponds to $t_{dep} = 0 \mu\text{m}$.

The unterminated devices show a premature breakdown at voltages between 600-700 V due to extreme electric field enhancement at the schottky corners. This is much lower than the ideal parallel plane breakdown voltage of around ~ 2100 V deduced for this structure with a 10 μm epilayer [103], as also from our simulation results (refer to Chapter three, Fig. 3.2) . In contrast, for devices with just thin thermal oxide as the FP, an improved V_B up to 800 V can be obtained. For the other devices with FPs of $\text{AlN}_y\text{:H/SiO}_2$, $\text{AlN}_x\text{/SiO}_2$ and PECVD $\text{SiO}_2\text{/SiO}_2$, much larger V_B as high as 1600 V can be obtained. Thus these Al-based dielectric/ SiO_2 FP devices can achieve breakdown voltage which is almost 80% of the maximum achievable V_B . Our results are comparable to V_B obtained using conventional single zone JTE SBDs where V_B as high as 71-81% of the maximum achievable V_B can be obtained depending on the JTE length [11]. V_B increased to as much as 87% of the maximum possible V_B using a double zone JTE structure [11].

Fig. 6.4 Breakdown voltage (V_B) as a function of the dielectric thickness (t_{dep}) for devices with 200 μm diameter.

As can be seen in Fig. 6.4, for all the dielectrics investigated there is a peak V_B at a certain optimum thickness. Below the optimum thickness, breakdown within the dielectric stack is dominant. Increasing t_{dep} will reduce the electric field within the dielectric stack and thus results in higher V_B . As t_{dep} is increased beyond the optimum thickness, the FP increasingly loses its influence on the field relief being provided at the schottky corners of the Pt/4H-SiC interface. Consequently corner breakdown dominates and results in lower V_B . The V_B improves to as much as 1100 V at an optimum thickness of around 0.45 μm for FP devices with PECVD $\text{SiO}_2/\text{SiO}_2$ as the dielectric. This is slightly better than ~1000 V reported by Saxena *et al.* [10] for their samples, which we mainly attribute to the lower

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

N_D of our samples. The V_B for $\text{AlN}_x/\text{SiO}_2$ and $\text{AlN}_y\text{:H}/\text{SiO}_2$ FP devices are around 1620 V and 1750 V respectively at an optimum thickness of around 0.8 μm . The much higher V_B seen for Al-based dielectric devices compared to PECVD SiO_2 devices is due to their larger dielectric constants ($\sim 2.2\times$), which lowers the electric field at the schottky corners, as well as their larger dielectric field strengths (E_c). In addition, we have a net negative charge within the Al-based dielectric/ SiO_2 composite stack (refer to our characterization results in chapter 4), which provides as much as 20-50% additional field relief [99]. The 10% higher V_B observed for $\text{AlN}_y\text{:H}$ devices compared to AlN_x devices is attributed to its denser amorphous structure with reduced oxygen impurities and grain boundaries [16,17].

Figure 6.5 shows typical reverse bias I - V characteristics up to the point of breakdown for the FP devices with different dielectrics at their respective optimum thickness, as well as the results for unterminated devices. It can be seen that the leakage current is much lower for the FP devices compared to the unterminated device. Also seen is the fact that the leakage currents at higher voltages for the Al-based FP devices are almost one order of magnitude lower than those of SiO_2 based FP devices. This is attributed to the much better field relief provided by the Al-based dielectrics.

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

Fig. 6.5 Leakage current characteristics for the FP terminated SBDs with optimal dielectric thickness ($t_{dep} = 0.8 \mu\text{m}$ for $\text{AlN}(\text{:H})/\text{SiO}_2$ and $t_{dep} = 0.45 \mu\text{m}$ for PECVD-SiO₂/SiO₂ devices) and unterminated SBDs up to point of breakdown. For comparison also shown is the characteristic of a Cree 600 V, 1 A SBD. Inset shows a part of the same characteristics on a linear scale which highlights abrupt edge related breakdown for our diodes and avalanche junction breakdown for Cree diodes.

For comparison, we have also measured and plotted the leakage current characteristics of a 600 V 1 A SBD from Cree. We speculate that these Cree diodes use some kind of guard rings or JTE as edge termination. As seen for all our FP diodes and unterminated diodes that the breakdown is associated with a sudden increase in leakage

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

currents at the point of breakdown, which is typical of catastrophic edge related breakdown. The diodes when remeasured after breakdown showed unusually high reverse bias leakage currents even at very low bias voltages, but however, exhibited normal forward bias characteristics. In contrast, the Cree diode shows an exponentially increasing leakage current (linear characteristics on a log scale) and there is no abrupt increase in the leakage current even when these 600 V diodes are biased to as much as 800 V. This is due to avalanche junction breakdown rather than corner or edge related breakdown. The difference is obvious when seen on linear scale as shown in the inset of the same figure. The breakdown seen on the Cree diode is non-destructive and repeated measurements up to 800 V yielded identical characteristics. Thus it is safer to use FP devices with voltage ratings higher than the anticipated maximum voltage in the application, or use FP in conjunction with other p-n junction based termination schemes, which will ensure avalanche breakdown [11, 48]. It is noted that R. Pérez *et al.* [11] reported a great reduction in the leakage currents and an increase in V_B for their JTE terminated 4H-SiC PiN diodes incorporated with FP, as compared to their JTE terminated devices without FP.

A region wise qualitative comparison of leakage current conduction mechanism under reverse bias for FP devices with optimum thickness, i.e. for PECVD-SiO₂/SiO₂ devices with $t_{dep}=0.45\text{ }\mu\text{m}$ and AlN(:H)/SiO₂ devices with $t_{dep}=0.80\text{ }\mu\text{m}$, has been made and are shown in Fig. 6.6 The comparison has been aided using the leakage current trends of FP devices with thicker dielectrics $t_{dep}=1.3\text{ }\mu\text{m}$, the leakage current of an unterminated device and the leakage current of an AlN_y:H device with $t_{dep}=0.80\text{ }\mu\text{m}$ but without the IL thermal oxide.

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

Fig. 6.6 Leakage current characteristics for the FP terminated devices for different dielectric thickness (t_{dep}). It highlights the rapid rise in leakage currents due to direct tunneling at higher voltages and higher thickness. Tunneling currents through the dielectric dominates the reverse leakage currents on diodes without IL.

Figure 6.7 illustrates some of the reverse leakage current components and paths for our diodes. Among these, the component related to space charge generations and diffusion current can be neglected due to the wide band gap of 4H-SiC [104]. Also the component related to tunneling currents through the dielectric at the outer edge is small in the presence of the IL thermal oxide due to its large barrier and the presence of a parallel low barrier path through the schottky metal.

Fig. 6.7 Illustration of the various components and paths of reverse leakage current for a FP SBD.

As seen in Fig. 6.6, for a given dielectric as the thickness is increased from the optimum thickness ($0.8\ \mu\text{m}$ for Al-based dielectric and $0.45\ \mu\text{m}$ for PECVD SiO_2) to $1.3\ \mu\text{m}$, the leakage currents which overlap initially deviate and increase sharply at higher voltages. The reason for this behavior is that at lower voltages the leakage current is dominated by thermionic emission (TE) [105] and thermionic trap-assisted-tunneling (TTT) [99, 106] which is distributed across the entire active area of the schottky contact and independent of the edge effects. The electric field profile within the interior of the contact and slightly away from the contact edges is quite similar for different t_{dep} . Thus at lower voltages the leakage

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

currents are quite similar for different t_{dep} . At higher voltages direct tunneling (DT) at schottky contact edges dominates which are strongly influenced by edge fields [99, 106]. The DT current is a sum of thermionic field emission (TFE) and field emission (FE) currents. As t_{dep} is increased to 1.3 μm , the FP loses much of its influence and subsequently the devices experience extreme electric field at the periphery of the Pt/4H-SiC interface. At the schottky contact edge, the increased electric field reduces the width of tunneling barrier leading to an increase in the tunneling current. The same dominance of DT current explains the more than one order of magnitude difference in the reverse leakage currents when comparing CVD SiO₂ FP devices and Al-based FP devices at higher voltages. The reason for this behaviour is again the same, which is due to much stronger edge fields on CVD SiO₂ FP devices due to lower dielectric constant of CVD SiO₂.

Comparing the AlN_y:H FP devices with and without intermediate thermal oxide, it is seen that the latter is quite leaky especially at high voltages where we see a sharp rise in the leakage current. In this case, the leakage current is due to tunneling through the dielectric itself, which is now dominant because of the low conduction band offset between AlN_y:H and 4H-SiC.

6.4 2-step Breakdown of FP terminated 4H-SiC SBDs

Fig. 6.8 Reverse bias leakage current characteristics of 4H-SiC FP terminated SBDs using as-deposited Al-based dielectric/ SiO_2 dielectric stack illustrating a 2-step breakdown. Inset shows a schematic of the diode indicating the possible locations of breakdown depending upon dielectric thickness.

Figure 6.8 shows the reverse bias leakage current characteristics of FP terminated SBDs utilizing a stack consisting of as-deposited Al-based dielectric and SiO_2 . The results for $t_{dep} = 0.45 \mu\text{m}$ and $1.3 \mu\text{m}$ are shown. The devices with $t_{dep} = 1.3 \mu\text{m}$ always exhibit a normal 1-step breakdown. On the other hand, an unusual 2-step breakdown is noted for some devices with $t_{dep} = 0.45 \mu\text{m}$. A detailed description of the effects of t_{dep} on the breakdown voltage of SBD has been explained previously. In short, as the dielectric thickness is

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

increased beyond a certain optimum value (which is $t_{dep} = 0.80 \mu\text{m}$ in our case), the Field Plate loses its influence on the field relief being provided at the schottky contact edge, and breakdown within 4H-SiC at the schottky corner at the 4H-SiC/dielectric interface (see inset, Fig. 6.8) dominates. Below the optimum thickness, breakdown within the dielectric stack at the outer most edge of the Schottky contact dominates. For devices with $t_{dep} = 1.30 \mu\text{m}$, we see a 1-step breakdown due to edge related 4H-SiC breakdown. On the other hand, the 2-step breakdown seen for devices with $t_{dep} = 0.45 \mu\text{m}$ is due to an initial breakdown of the SiO_2 within the dielectric stack. The SiO_2 , instead of $\text{AlN}_y\text{:H}$ or AlN_x , undergoes a breakdown first. The reason is, if we assume either $\text{AlN}_y\text{:H}$ or AlN_x undergo a breakdown first, then the strong edge electric fields which was being supported by the composite stack consisting of Al-based dielectric/ SiO_2 will now have to be supported by the thin thermal SiO_2 layer alone. It is known from the breakdown voltage results on some of our best diodes with just the thermal SiO_2 as field plate dielectric, that they could at most sustain 800 V. Thus the edge electric field at voltages in excess of 900 V where we experience the first breakdown on these devices with 2-step breakdown will be much stronger. Consequently, instantaneous breakdown of thermal SiO_2 will follow. Thus the only way a 2-step breakdown could happen is with the breakdown on thermal SiO_2 layer first. With the breakdown of SiO_2 , the entire voltage now appears solely across $\text{AlN}_y\text{:H}$ or AlN_x . Without the SiO_2 that provides a high barrier for electron injection from the metal into 4H-SiC through the dielectric stack, we see an abrupt jump in the leakage current due to increased tunneling through the $\text{AlN}_y\text{:H}$ or AlN_x layer. Beyond this first breakdown point, we see a higher level of leakage current in AlN_x devices compared to $\text{AlN}_y\text{:H}$ devices. This may be attributed to $\text{AlN}_y\text{:H}$ being more dense, smoother and amorphous as-deposited, which leads to reduced grain boundaries and hence lower leakage current. As the voltage is further increased, $\text{AlN}_y\text{:H}$ or AlN_x final breakdown occurs and the device leakage current shoots up to a clamp value of $10 \mu\text{A}$. The 2-step breakdown was not observed for other Al-

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

based dielectric with $t_{dep} = 0.05 \mu\text{m}$ and $0.20 \mu\text{m}$ as the layer is too thin to withstand the high voltage and corresponding high electric field after the SiO_2 breakdown. On the other hand, for t_{dep} greater than $0.45 \mu\text{m}$, i.e. 0.80 and $1.3 \mu\text{m}$ Schottky corner edge related breakdown rather than dielectric breakdown dominates and thus no 2-step breakdown observed for these samples.

6.5 Comparisons of Experimental and Simulated Results

In this section, we compare the experimental results of unterminated 4H-SiC SBDs with different drift layer N_D and FP terminated SBDs having different dielectric thickness with the simulation results presented in Chapter three.

6.5.1 Comparison of Experimental and Simulated Unterminated 4H-SiC SBDs.

Fig. 6.9 Comparison of experimental and simulated V_B for unterminated 4H-SiC SBDs with different N_D .

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

Figure 6.9 shows the experimental breakdown voltage V_B (taken from Fig. 5.9) and the simulated V_B (taken from Fig. 3.2) for unterminated SBDs. As is obvious from the figure, there is a reasonable match between the experimental and simulated results. However, we also observe a certain consistent underestimation of the experimental V_B from simulations. We attribute this to several reasons. One of the reasons for the slight underestimation in simulations could be partly due to some slight over estimated values of impact ionization parameters obtained from published results [63, 64], which we have used for our simulation. In a way, this reasoning is justified based on the fact that our simulated values of ideal 4H-SiC diode structures with thick epilayers ($\sim 100 \mu\text{m}$) were consistently lower than those calculated analytically using the eqn. (6-1)-(6-2) suggested by Konstantinov *et al.* [63].

$$V_B = \frac{\epsilon_{sic} \epsilon_o E_c^2}{2qN_D} \quad (6-1)$$

$$E_c = \frac{2.49}{1 - \left(\frac{1}{4}\right) \log\left(\frac{N_D}{10^{16}}\right)} \quad (6-2)$$

For example, the critical electric field E_C for $N_D = 2 \times 10^{15}/\text{cm}^3$ is $\sim 2.12 \text{ MV/cm}$ and the V_B calculated is around 6026 V for the $100 \mu\text{m}$ epilayer structure. Our simulated V_B for the same structure is around 5720 V. Other factor could be slightly lower values of doping N_D for our samples as compared to the values that we have used for the simulations. Among other reasons could be slightly lower interface charge Q_F in the oxide which acts as surface passivation in the experimental device. For our simulations we had assumed an interface charge $Q_F = +5 \times 10^{11}/\text{cm}^2$ in the oxide surrounding the schottky contact.

6.5.2 Comparison of Experimental and Simulated FP terminated 4H-SiC SBDs.

Next we compare our experimental results for FP terminated diodes (taken from Fig. 6.4) with our simulated results (taken from Figs. 3.6 and 3.10). The results are shown in Figs. 6.10 and 6.11 for SiO₂/SiO₂ and Al-based dielectrics/SiO₂ FP devices respectively. We can partition the comparison into two regions, the dielectric breakdown dominated region for thickness t_{di} lower than the optimum thickness and the corner related impact ionization dominated breakdown region for thickness t_{di} higher than the optimum thickness. The t_{di} here represents the total thickness which includes the thickness of the deposited dielectrics and intermediate SiO₂ layer which is around ~0.05 μm thick.

As can be seen from both Figs. 6.10 and 6.11 the degree of mismatch in the dielectric breakdown dominated region is high. There could be several possible reasons. First and foremost, the simulated V_B in this region are the best possible, since we have assumed the SiO₂ and AlN breakdown field at their ideal values of 10 MV/cm and 7 MV/cm respectively. Based on the measurements of our MIS capacitor samples we estimate the breakdown of our SiO₂ layer close to 9-10 MV/cm and for the Al-based dielectrics to be between 5-6.5 MV/cm. In reality, our dielectric breakdown strength could be lower when deposited on the SBDs. We speculate that the dielectric dry etch processes, BCl₃/Cl₂ based RIE for Al-based dielectric and CF₄/Cl₂ based RIE for SiO₂, may have led to plasma damage to the dielectrics. Though we have measured the dielectric breakdown strength on capacitors as detailed in Chapter four, the MIS structures were not subjected to dry etch and hence not susceptible to plasma damage. Another possible reason may be the edge roughness at the schottky contact which could have induced much higher electric fields in experimental devices than estimated from our simulations. Some other possible reasons for the lower breakdown of the dielectrics we speculate could be due to some porosity, stoichiometric and thickness variations of the dielectric film.

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

Fig. 6.10 Simulated and experimental V_B comparison for $\text{SiO}_2/\text{SiO}_2$ FP terminated 4H-SiC SBD.

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

Fig. 6.11 Simulated and experimental V_B comparison for $\text{AlN}_x/\text{SiO}_2$ and $\text{AlN}_y:\text{H}/\text{SiO}_2$ FP terminated 4H-SiC SBD.

In contrast, the degree of mismatch is low in the region dominated by impact ionization breakdown (see Fig. 6.10 and 6.11). The slight inconsistency between the experimental and simulation results could be attributed to slightly higher impact ionization coefficients used in simulations, uncertainty in exact doping concentration N_D on experimental devices, differences in actual and assumed interface charge where we have assumed a nominal $|Q_F| = 5 \times 10^{11} / \text{cm}^2$ for the simulations but the actual charge may deviate from the assumed value. Edge roughness is another factor which could play a role and could account for small difference seen in the simulated and actual breakdown values.

6.5.3 Electric Field profile of FP terminated 4H-SiC SBDs with 2-step Breakdown.

Fig. 6.12 Electric field along a vertical cutline at secondary corner S for AlN/SiO₂ FP SBD with $t_{dep}=0.05\ \mu\text{m}$ and $t_{dep}=0.45\ \mu\text{m}$.

To explain and provide physical insight into the 2-step breakdown phenomenon observed for the SBDs, we looked at the electric field distribution in AlN and SiO₂ along a vertical cutline (shown in the inset of Fig. 6.12) along the secondary corner S where the dielectric breakdown takes place. The extraction has been done for two different thicknesses of deposited dielectric t_{dep} 0.05 μm and 0.45 μm . The extraction has been done at 900 V for 0.05 μm device and at 1200 V for 0.45 μm device. The rationale for selecting these voltages

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

for electric field profile check is the fact that these are approximately the voltages where the experimental SBDs with the respective dielectric thickness undergo a breakdown (refer to Fig. 6.11). Thus these two voltages serve as a good reference point to visualize the actual situation in terms of electric field profile within the devices. In Chapter three (see Fig. 3.13) we explained that for AlN thickness less than $0.2\ \mu\text{m}$, it is the SiO_2 layer which invariably undergoes a breakdown due to extremely strong fields emanating from the corner S in AlN, which percolates down to SiO_2 layer and get magnified ~ 2.5 times due to the dielectric constant difference. On the other hand, for AlN thickness greater than $0.2\ \mu\text{m}$ and up to $0.7\ \mu\text{m}$, it is the AlN which undergoes a breakdown as the electric field within it reaches $\sim 7\ \text{MV/cm}$.

As can be seen from Fig. 6.12 at 900 V, the electric field for $t_{\text{dep}} = 0.05\ \mu\text{m}$ is much stronger in SiO_2 than in AlN, and almost close to its breakdown strength of $10\ \text{MV/cm}$. Thus invariably it is the SiO_2 layer which undergoes a breakdown first, after which the AlN layer which is too thin to withstand the resultant field also undergoes a simultaneous breakdown. Thus only a single step breakdown is visible on these devices. Referring to the case of $t_{\text{dep}} = 0.45\ \mu\text{m}$ device at its breakdown voltage of 1200 V, the field in SiO_2 is quite strong reaching $\sim 7\ \text{MV/cm}$ while the peak electric field within AlN which lies at a distance of $\sim 0\ \mu\text{m}$ from the secondary corner 'S' is around $5.3\ \text{MV/cm}$ which is close to its practical breakdown limit. Thus it is very likely that AlN will undergo a breakdown at this point in the experimental devices. However in that case, the SiO_2 layer which is too thin to withstand the resulting extreme field will immediately undergo a breakdown too, and hence will not lead to a 2-step breakdown. The other scenario is some inherent weakness in the SiO_2 layer resulting in its breakdown at some lower voltage of say around 900-1000 V as seen from Fig. 6.8. This could possibly give rise to the 2-step breakdown phenomenon seen for the SBDs since the thicker Al-based dielectric layer can withstand further voltage ramp. Thus

Chapter 6 Field Plate Terminated 4H-SiC Schottky Barrier Diodes

the 2-step breakdown observed for $t_{dep} = 0.45 \mu\text{m}$ is attributed to an early breakdown of the SiO_2 layer due to some intrinsic weakness, defect or stress.

6.6 Conclusions

In summary, we presented the process and fabrication details of FP terminated 4H-SiC SBDs. In this work, we demonstrated for the first time high voltage 4H-SiC SBDs with FP termination using high- k $\text{AlN}_x/\text{SiO}_2$ and $\text{AlN}_y\text{:H}/\text{SiO}_2$ dielectric stack. Our results indicate that a V_B as much as 1750 V, which is more than 80% of the ideal theoretical breakdown voltage, can be obtained using the above dielectrics. This is an improvement in V_B in excess of 600 V, or more than 30% of the ideal breakdown voltage, as compared to PECVD- $\text{SiO}_2/\text{SiO}_2$ FP device which has a breakdown of ~ 1100 V. The leakage currents at higher voltages is almost one order of magnitude lower for the Al-based dielectric/ SiO_2 FP devices compared to CVD- $\text{SiO}_2/\text{SiO}_2$ based FP devices, while the forward turn-on characteristics up to 573 K are comparable. Thus we not only gain on V_B but also reap the benefits of reduced power losses. We attribute these improvements to three main factors namely i) a much reduced electric field enhancement at the schottky corners as a result of the higher dielectric constant of the Al-based dielectrics, which is almost $\sim 2.2\times$ that of CVD SiO_2 ii) a net negative charge within the dielectric film providing additional field relief and iii) an improved ($\sim 1.3\times$) effective dielectric breakdown strength. The results of experimental unterminated and FP terminated SBDs were compared to device simulation results. We found reasonably good match of experimental and simulated unterminated diode breakdown voltage. A 2-step breakdown seen on some FP terminated devices could be explained using electric field profile at the schottky corner. It could also explain the sequence of dielectric breakdown which basically involves breakdown of intermediate thermal oxide layer first in the composite $\text{AlN}_x/\text{SiO}_2$ or $\text{AlN}_y\text{:H}/\text{SiO}_2$ stack.

Chapter 7

Conclusions and Future Work

We will present in this chapter the conclusions of our research and recommendations for future work.

7.1 Conclusions

The field plate (FP) termination technique has long been a power horse for Si power device technology using thick SiO₂ field oxide and poly silicon as an electrode overlapping the field oxide. It is a simple and effective edge termination technique that alleviates the electric field at the Schottky contact edges and increases the breakdown voltage of the power devices. The FP termination technique is also attractive as it avoids the hassles and complexity of implantation as needed in other edge termination techniques, and hence it is also cost effective.

In this project we studied the application of FP termination technique to high voltage 4H-SiC Schottky barrier diodes (SBDs). A straight forward adaptation of this technology from Si to SiC by using SiO₂ as the FP suffers major drawbacks due to the lower dielectric constant of SiO₂, which results in extreme electric fields at Schottky contact edges. To overcome the problem and render the FP termination technique effective for SiC power devices, we have studied the use of alternate dielectrics with higher dielectric constants (k) as the FP. Specifically, the FP dielectric SiO₂ which is conventionally used for Si devices has been replaced with a dielectric stack consisting of an Al-based dielectric on top of SiO₂. The Al-based dielectrics studied include sputter deposited aluminum nitride (AlN_x) and

Chapter 7 Conclusions and Future Work

hydrogenated aluminum nitride (AlN_yH). The use of such high- k Al-based dielectrics overcomes the problems associated with the low dielectric constant of SiO_2 and the resulting extreme surface electric fields. The SiO_2 in the dielectric stack was thermally grown on 4H-SiC, and acts as an intermediate layer between the Al-based dielectrics and 4H-SiC. It is needed as the SiO_2 /4H-SiC interface will have a much larger conduction/valence band offset compared to the Al-based dielectrics/4H-SiC interface. This will lower the tunneling leakage currents through the dielectric, improve the interface properties and reduce excess dielectric negative charge which may result if the Al-based dielectrics were to form directly on 4H-SiC. We have also studied these Al-based dielectrics which includes AlN_x , AlN_yH and Aluminum oxide (AlO_z) as a passivation dielectric for 4H-SiC unterminated SBDs. The electrical performance of these Al-based dielectrics as passivations were compared to conventional oxide based dielectrics using PECVD SiO_2 and thermal SiO_2 . The reverse bias leakage currents on these SBDs was found to be two to three orders lower for SBDs passivated using the Al-based dielectrics as compared to conventional SiO_2 passivated devices.

The FP terminated 4H-SiC SBDs were first studied through extensive numerical simulations to study the effects of the thickness and dielectric constant of the dielectric on their breakdown voltages. The simulation results also provide an extensive insight into the device behavior in terms of electric field distribution and identify those regions of the SBDs that are subject to maximum impact ionization. We simulated an ideal 4H-SiC Schottky diode with a structure identical to our experimental SBDs having a 10 μm epilayer thickness and an epilayer doping of $N_D = 2 \times 10^{15}/\text{cm}^3$. The breakdown voltage (V_B) for this ideal structure was close to 2100 V. In contrast, unterminated 4H-SiC SBDs simulated in this study using the same structure show a premature breakdown at around 600 V due to extreme electric field enhancement at the schottky contact edges. With an objective to reduce

Chapter 7 Conclusions and Future Work

schottky edge electric field enhancement and improve V_B , field plate terminated 4H-SiC SBDs using a stack of AlN/SiO₂ was simulated. It was compared to conventional SiO₂/SiO₂ based FP terminated devices. For the SBDs terminated with SiO₂/SiO₂ and AlN/SiO₂, the maximum breakdown voltages V_B are obtained when the FP thicknesses are close to 0.4 μm and 0.7 μm respectively. The corresponding V_B are ~ 1200 V and ~ 1600 V. The V_B for SiO₂/SiO₂ FP terminated SBDs is almost 60% of the ideal V_B , and it is also better than unterminated devices with V_B which is about 30% of the ideal value. However, the V_B is even higher and almost close to 80% of the ideal value using AlN/SiO₂ FP termination. These numerical simulations clearly highlight the advantages of using a AlN/SiO₂ FP termination yielding much higher V_B .

For our experimental work, we first studied the Al-based dielectrics deposited using RF magnetron reactive sputtering. The films were characterized in terms of their electrical breakdown strength and breakdown mechanisms using metal-insulator-semiconductor (MIS) capacitor structures. Among the Al-based dielectrics investigated, AlN_y:H was found to be the best by virtue of its dense amorphous nature. X-ray diffraction (XRD) shows that AlN_y:H is amorphous as-deposited, compared to AlN_x which is polycrystalline. Thus AlN_y:H is better suited for device applications due to its reduced grain boundaries and consequently lower leakage currents. We have demonstrated that as-deposited AlN_y:H/SiO₂ stack exhibits almost 30-40% higher dielectric breakdown strength compared to pure SiO₂. The multi step breakdown phenomenon seen on MIS capacitors using the Al-based dielectrics with an intermediate layer of SiO₂ was investigated using measurements of dielectric relaxation currents. On these composite stacks, SiO₂ was found to be the weakest link in terms of electrical breakdown for the as-deposited dielectrics. Nevertheless it is needed to reduce leakage currents due to the low conduction/valence band offset between 4H-SiC and the high- k dielectrics. Extreme electric field which is almost 2.5 times in the

Chapter 7 Conclusions and Future Work

SiO_2 compared to that in the Al-based dielectrics, coupled with defects generated by electrons injected into the SiO_2 leads to its eventual destruction. The breakdown of the Al-based dielectric may or may not follow instantaneously depending on the voltage at which the SiO_2 undergoes a breakdown. On the contrary, in a dielectric stack that has undergone a 950 °C rapid thermal annealing (RTA), the high- k dielectric tends to breakdown first due to formation of defects and grain boundaries as a result of the annealing.

We investigated the use of Al-based dielectrics, including sputter deposited AlN_x , $\text{AlN}_y\text{:H}$ and AlO_z , as passivation layer for unterminated 4H-SiC SBDs. These Al-based dielectrics could be valuable replacement for conventional SiO_2 and Si_3N_4 based passivation schemes, which are known to suffer from low passivation heat conductivity and lower dielectric constants. The larger dielectric constants of the Al-based dielectrics reduce the surface fields and hence improve the long-term reliability of the devices. Their very high thermal conductivity also leads to reduced self heating. It was found that using a stack of Al-based dielectrics with a thin thermal oxide (~5-15 nm) as the passivation layer, the leakage currents of the SBDs is substantially reduced. The thin thermal oxide serves as an interfacial layer between the Al-based dielectrics and 4H-SiC, without which the interface quality will be poor with a very high density of negative charge. Moreover, there will also be increased tunneling leakage current through the dielectric due to the small conduction band offset between the Al-based dielectrics and 4H-SiC. Besides, if the Al-based dielectrics were to form directly on the 4H-SiC, there will also be increased surface leakage current due to sputter induced damage on the 4H-SiC. We found a remarkable reduction by almost two to three orders of magnitude in the leakage currents for SBDs passivated by Al-based dielectrics (AlN_x , $\text{AlN}_y\text{:H}$, AlO_z) with an interfacial SiO_2 compared to unpassivated devices. The result is also much better than the about one order of magnitude reduction in the leakage currents seen when using the conventional PECVD SiO_2 for the passivation.

Chapter 7 Conclusions and Future Work

Following the work on the passivation of 4H-SiC SBDs, we have successfully developed the process technology for the fabrication of high voltage FP terminated 4H-SiC SBDs, using the high- k dielectric aluminum nitride (AlN) as the FP. Unterminated SBDs were also fabricated in this study for comparison. These devices were noted to suffer from premature breakdown due to electric field enhancements at the edges of the Schottky contact. For example, with a 4H-SiC doping concentration $N_D = 2 \times 10^{15}/\text{cm}^3$, the breakdown voltage V_B achievable is only 600-700 V for the unterminated SBDs. This is just about 20-30% of the ideal theoretical breakdown voltage for such devices of ~ 2100 V. In contrast, for the PECVD $\text{SiO}_2/\text{SiO}_2$ and Al-based dielectrics/ SiO_2 FP terminated SBDs fabricated, V_B has substantially increased to ~ 1100 V and ~ 1750 V respectively. The reverse bias leakage current at higher voltages is almost one order of magnitude lower for the Al-based dielectric/ SiO_2 FP devices compared to PECVD $\text{SiO}_2/\text{SiO}_2$ based FP devices, while the forward turn-on characteristics up to 573 K are comparable. Thus we not only gain on V_B but also reap the benefits of reduced power losses when using Al-based dielectric/ SiO_2 instead of conventional PECVD $\text{SiO}_2/\text{SiO}_2$ as FP. We attribute these improvements to three main factors, namely i) a much reduced electric field enhancement at the schottky corners as a result of the higher dielectric constant of the Al-based dielectrics, which is almost ~ 2.2 times that of CVD SiO_2 , ii) a net negative charge within the Al-based dielectrics providing additional field relief and iii) an improved (~ 1.3 times) effective dielectric breakdown strength. Comparing the experimental results with those obtained from numerical simulations, we found reasonably good match in terms of V_B for Al-based dielectric/ SiO_2 FP as well as PECVD $\text{SiO}_2/\text{SiO}_2$ FP devices especially for the range of dielectric thickness where the breakdown is dominated by edge related impact ionization.

7.2 Future Work

As a part of our future work, a simple modification of the single step FP termination structure proposed in this work could be carried out to further improve the breakdown voltage. It would involve the optimization of the Al-based dielectric profile with a shallow angle (5° – 20°) bevel. Beveling has been a common feature in mesa based edge termination techniques [107] and has been numerically shown to be very beneficial for FP termination technique too [108]. Beveling helps to further alleviate the electric field crowding at the Schottky corner and improve the breakdown voltage. We believe the combined benefits of employing the higher dielectric constant AlN and adopting beveling to reduce electric field crowding will be enormous. Further numerical simulations will need to be carried out to evaluate the optimized bevel angle and the corresponding dielectric thickness for achieving maximum blocking voltage. This we believe will certainly help to take us even closer towards achieving a perfect parallel plane breakdown for the SBDs.

In this thesis, we studied the breakdown mechanism of Al-based dielectrics/SiO₂ stack using measurements of dielectric relaxation current. As discussed in Chapter 4, the intermediate layer of SiO₂ is the weakest link in the as-deposited Al-based dielectric/SiO₂ stack and is generally responsible for breakdown of the stack. The intermediate SiO₂ layer is under immense electrical stress due to high electric field which is almost 2.5 times of magnitude in SiO₂ compared to that in Al-based dielectric as a result of their dielectric constant difference. These extreme electric fields coupled with high levels of leakage current through the stack degrade the intermediate SiO₂ leading to its eventual breakdown. However, an understanding of the dominant leakage current conduction mechanisms such as Fowler-Nordheim (F-N) tunneling or Poole Frenkel (PF) emission or Schottky emission (SE) at high electric field through these Al-based dielectrics/SiO₂ stacks is not known. The leakage currents and dielectric breakdown are strongly affected by the dominant leakage

Chapter 7 Conclusions and Future Work

current conduction mode which in-turn is directly influenced by fabrication process conditions such as SiC substrate surface treatment, thermal SiO₂ growth conditions, Al-based dielectric deposition conditions, post-deposition thermal treatment. An extension of our work, could involve a study of leakage current conduction modes through these Al-based dielectric/SiO₂ stacks. It is essential to evaluate process improvements and resulting leakage current reductions. Any improvements in leakage current will go a long way in improving the breakdown strength of these Al-based dielectric/SiO₂ stacks [109]. This will benefit the Al-based dielectrics/SiO₂ FP terminated SBDs in terms of breakdown voltage as well as in terms of reduced tunneling leakage current through the FP dielectrics at Schottky contact edges.

Author's Publication List

Journal Papers

- 1) **A. Kumta**, Rusli, C. C. Tin and J. Ahn, "Design of Field-Plate Terminated 4H-SiC Schottky Diodes using High- k Dielectrics," Journal of Microelectronics Reliability, vol. 46, pp. 1295-1302, 2006.
- 2) **A. Kumta**, Rusli and C.C. Tin, "Design and analysis of a Dual-step Field-Plate terminated 4H-SiC Schottky Diode using SiO₂/High- k dielectric stack," Materials Science Forum, vol. 527-529, pp. 1171-1174, 2006.
- 3) **A. Kumta**, Rusli and J. H. Xia, "Field-plate terminated Pt/n-4H-SiC SBD using Thermal SiO₂ and sputter deposited AlN Dielectric Stack," Materials Science Forum, vol. 600-603, pp 987-990, 2009.
- 4) **A. Kumta**, Rusli and J. H. Xia, "Passivation of 4H-SiC Schottky Barrier Diodes using Aluminum based Dielectrics," Journal of Solid State Electronics, vol. 53, pp. 204-210, 2009.
- 5) **A. Kumta**, Rusli and J. H. Xia "Breakdown phenomena of Al-based dielectric/SiO₂ stack on 4H-SiC." Applied Physics Letters, vol. 94, pp. 233505, 2009.
- 6) **A. Kumta**, Rusli and J. H. Xia, "Field-plate Terminated 4H-SiC Schottky diodes Using Al-based High- k Dielectrics," IEEE Trans. Electron Devices, vol. 56, No. 12, Dec. 2009.

Conference Papers

- 1) **A. Kumta**, Rusli, C. C. Tin, S. F. Yoon, J. Ahn, "Numerical Simulations of Field-Plate Terminated 4H-SiC Schottky Diodes Using SiO₂ and High-*k* dielectrics," the 2nd International Conference Materials for Advanced Technologies (ICMAT 2003), Singapore, December 7-12 , 2003.
- 2) **A. Kumta**, Rusli and C.C. Tin, "Design and analysis of a Dual-step Field-Plate terminated 4H-SiC Schottky Diode using SiO₂/High-*k* dielectric stack," International Conference on Silicon Carbide and Related Materials 2005 (ICSCRM 2005), Pittsburgh, Pennsylvania, USA, September 18-23, 2005.
- 3) **A. Kumta**, Rusli and J. H. Xia, "Field-plate terminated Pt/n-4H-SiC SBD using Thermal SiO₂ and sputter deposited AlN Dielectric Stack," International Conference on Silicon Carbide and Related Materials 2007 (ICSCRM 2007), Otsu, Japan, October 14-19, 2007.

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- 2) Figure 11 and Figure 12 from " R. Pérez, D. Tournier, A. P. Tomas, P. Godignon, N. Mestres, J. Millan, Planar Edge Termination Design and Technology Considerations for 1.7 KV 4H-SiC PiN Diodes," IEEE Trans. Electron Devices, vol. 52, pp. 2309-2316, Oct. 2005."
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