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Song, Pengyu

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DESIGN OF DELTA-SIGMA MODULATOR FOR ULTRASOUND IMAGING

SONG PENGYU

School of Electrical and Electronic Engineering

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ABSTRACT

The design and implementation of a high speed continuous-time delta-sigma modulator is presented in this report. The modulator is designed for a portable ultrasound digital beamformer to digitize ultrasound signal centered at 3.5MHz with fractional bandwidth of 0.6. A CMOS third-order low-pass modulator was simulated and implemented at 200MHz sampling frequency. An improved low power transconductor with reduced mobility degradation was designed and realized. With full circuit simulation, the modulator achieves a dynamic range of 59.6dB and consumes only 4.20mW RMS power at 1.8V supply voltage. The layout was implemented using Chartered 0.18μm CMOS process. The core layout occupies 0.073mm^2 and the entire die including 24 pads occupies 1.54mm^2. Comparing with the existing circuits, the proposed structure dissipates relatively lower power and achieves comparable resolution.

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List of Abbreviations

AAF	Anti-aliasing filter
ADC	Analog-to-digital converter
A/D	Analog-to-digital
CIFB	Cascaded integrators with distributed feedback
CIFF	Cascaded integrators with weighted feedforward
CMFB	Common-mode feedback
CRFB	Cascaded resonators with distributed feedback
CRFF	Cascaded resonators with weighted feedforward
CSM	Chartered Semiconductor Manufacturing
CT	Continuous-time
CW	Continuous-wave
DAC	Digital-to-analog converter
DSM	Delta-sigma modulator
DT	Discrete-time
D/A	Digital-to-analog
ENOB	Effective number of bits
ESR	Equivalent series resistance
FFT	Fast Fourier transform
FOM	Figure of merit
FS	Full scale
GBW	Gain-bandwidth product
HUS	Home ultrasound system
IBN	In-band noise
IM3	Third-order intermodulation distortion
LSB	Least-significant bit
MOD1	First-order modulator
MOD2	Second-order modulator
MOD3	Third-order modulator
MOD4	Fourth-order modulator
MSA	Maximum stable amplitude
NBW	Noise bandwidth
NRZ	Non-return-to-zero
NTF	Noise transfer function
OSR	Over sampling ratio
PAC	Periodic AC
PDF	Probability density function
PCB	Printed circuit board
PSD	Power spectral density
PSS	Periodic steady-state
RMS	Root mean square
RZ	Return-to-zero

SAR	Successive-approximation register
SC	Switched-capacitor
SNDR	Signal-to-noise-and-distortion ratio
SNR	Signal-to-noise ratio
STF	Signal transfer function
S/H	Sample and hold

List of Symbols

a	Loop filter coefficient
A_0	DC gain of transconductor/opamp
b	Loop filter coefficient
c	Loop filter coefficient
C	Capacitor, capacitance
$dac(t)$	Impulse response of DAC
g	Loop filter coefficient
g_m	Small signal transconductance
G_m	Transconductor transconductance
E	Quantization error
$E(z)$	Quantization error in z-domain
f_B	Signal bandwidth
f_N	Nyquist rate
f_o	Unity gain frequency
f_s	Sampling frequency
I_{out}	Output current
$l_1(t)$	Impulse response of loop filter L_1
L	Inductor, inductance
$L_0(z)$	Loop filter (modulator input path) in z-domain
$L_1(z)$	Loop filter (modulator output path) in z-domain
N	Modulator order
k	Quantizer equivalent gain
K	Oversampling ratio
M	Quantizer number of steps
n	Number of sample
$NTF(z)$	Noise transfer function in z-domain
P	Power consumption
r_0	Small signal drain-source resistance
R	Resistor, resistance
R_{out}	Output resistance
s	Laplace-domain variable
$S_e(f)$	Power spectral density of quantization noise
$STF(z)$	Signal transfer function in z-domain
t	Time
t_d	Excess loop delay
T_s	Sampling period
$U(z)$	Modulator input in z-domain
$v(n)$	Quantizer output in discrete-time
$v(t)$	Quantizer output in continuous-time
V_{in}	Input voltage
V_{out}	Output Voltage
$V(z)$	Quantizer output in z-domain
$x(n)$	Signal in discrete-time

$x(t)$	Signal in continuous-time
$X(f)$	Spectra of signal
$y(n)$	Quantizer input in discrete-time
$y(t)$	Quantizer input in continuous-time
$Y(z)$	Quantizer input in z-domain
z	Discrete-time frequency variable
α	Relative time of DAC rising edge
β	Relative time of DAC falling edge
Δ	Quantizer step size
θ	Mobility empirical fitting parameter
μ	Carrier mobility
μ_{eff}	Effective mobility
μ_p	Zero-field mobility
σ_e	Standard deviation of quantization noise
σ_β	Standard deviation of clock jitter
φ	Clock phase
ω_B	Signal bandwidth in radians
ω_o	Unity gain frequency in radians
ω_s	Sampling frequency in radians

Chapter 1 Introduction

1.1 Background

Over the last fifty years, ultrasound imaging has developed into one of the most commonly used non-invasive methods for obtaining diagnostic medical images. After tissue structure was found to be differentiable using ultrasound echoes between 1940s and 1950s, A-mode was first used in applications e.g. visualization of body structures [1] followed by B-mode e.g. clinical two-dimensional slice image in the 1970s [2]. In A-mode scanning, the reflected echo amplitude is displayed against the depth of the scanned object. B-mode scanning can produce the strength of the reflected echo as the brightness of the pixels in a two-dimensional plane. Thus, B-mode produces more information such as echo direction and 2D image [2]. Later on, more advanced functions like Doppler processing and more sophisticated systems like phased array systems were made possible by advances in analog delay lines and the reduced size of analog processing elements by the 1980s [3], which were still making use of analog processing techniques in the late 80s. Only since the late 1980s, has the analog beamformer been gradually replaced by the digital beamformer through the development of analog-to-digital (A/D) conversion and CMOS digital circuits. Digital beamformers offer several advantages over analog beamformers, including higher precision, programmability, stability and reliability. Moreover, complex signal processing can be easily realized in digital domain. With digital beamformer, the ultrasound scanner becomes more flexible due to its programmability [4] and more compact in size.

Most ultrasound imaging systems are limited for use in hospitals and clinics due to their bulkiness and cost. On the other hand, the need for home-based imaging systems, which can remotely monitor patients (for example, high risk pregnant women and patients with chronic conditions), is growing rapidly. As compared to other imaging systems like X-ray computed tomography and nuclear medicine, the ultrasound imaging system is much safer and relatively easier to operate [5]. Hence, a home ultrasound system (HUS) which is portable, small in size, low power and low cost is needed and has a high potential to be commercialized. However, conventional digital beamformers employing phase rotation [6] and interpolation [7, 8] techniques tend to be very complex in terms of hardware and therefore cannot be integrated inside the ultrasound probe. A high performance and expensive cable is required to transmit analog signal between the ultrasound transducer and the beamformer, which limits the potential to be used as a portable devices.

Delta-sigma beamforming was first proposed in 1993 [9] to reduce the overall beamformer hardware complexity, cost and power consumption. Since then, it was developed and improved over the last decade in order to achieve low cost low power beamformer for ultrasound imaging system [3, 10-12]. Compared to conventional beamforming methods employing Nyquist rate analog-to-digital converters (ADCs), delta-sigma beamformer is more amenable to single-chip integration due to the simpler hardware of delta-sigma modulator (DSM). Furthermore, with oversampling technique, high delay resolution can be achieved at the same time without additional interpolation.

A DSM is an analog signal encoder based on redundant data through oversampling [9]. A simple DSM consists of a sampler, a single-bit quantizer (comparator), a single-bit DAC (switch) and a first-order loop filter (integrator). The input of the DSM in analog form is sampled and modulated into a one-bit stream in digital form, which can be used for data processing in digital domain. Compared to Nyquist rate A/D conversion, the DSM is less sensitive to circuit imperfections and requires less hardware [9].

1.2 Motivation

As one of the most critical components in delta-sigma beamformer, the design of the DSM for the HUS is of great interest. There are several challenges and issues in the design of DSM for digitizing the ultrasound signal. Firstly, the center frequency of the medical ultrasound signal ranges from 2MHz to 10MHz [5] as compared to a typical DSM sampling frequency of several kHz [9]. In this project the center frequency is chosen as 3.5MHz with fractional bandwidth of 0.6, resulting in a signal bandwidth of 5MHz if a low-pass DSM is used. In order to achieve sufficient signal-to-noise ratio (SNR) through oversampling, the sampling frequency has to be hundreds of MHz. This high sampling frequency is difficult for conventional discrete-time (DT) DSM to operate at [13, 14], due to its settling time constraint. Secondly, digital beamformer requires an ADC for each receive channel, large numbers of DSMs (for example, 32 in this project) are needed for multiple channels in the beamformer. Therefore, the DSMs must be low power and small size in order to be integrated into a single chip for HUS. Thirdly, single-bit quantization in delta-sigma beamforming has been shown to be more efficient than

multi-bit quantization in terms of hardware [3]. Thus, a one-bit quantizer is employed in this project.

The extreme high sampling frequency motivates the loop filter inside the DSM to be built in continuous-time (CT) form rather than in DT form. The main advantage is that the settling time constraint in CT DSM is less stringent compared to that in DT DSM [15, 16]. This fundamental advantage is based on the displacement of the sampler inside the modulator loop [16]. In general, CT DSM also provides other benefits such as implicit anti-alias filtering and reduced requirement on sample and hold (S/H) circuit [16]. Consequently, CT DSM offers better power efficiency for signal with relatively wideband. Although the first CT DSM was demonstrated in discrete form in 1986 [17], research work on CT DSM has only become popular since mid 1990s. Some books [15, 16, 18] are listed in the references while among them, the first two books [15, 16] are frequently referenced due to their importance in the area. Two other books [13, 14] are mostly referenced regarding the system design and synthesis of DT DSM. Some programming codes in [14] are utilized in the system design.

1.3 Objectives

This project aims to investigate and design a CT DSM suitable for a portable ultrasound digital beamformer featuring simple hardware, small size and low power. The system design was performed in Matlab/Simulink and the transistor level design was carried out in Cadence Virtuoso Custom Design Platform. Chartered Semiconductor Manufacturing (CSM) CMOS 0.18μm process was used with 1.8V supply voltage. The proposed CT

DSM was designed, layout, simulated and compared with other state of the art modulators. The comparison studies on existing designs are listed in section 2.5. The target specifications for the proposed CT DSM are shown below in Table 1.1. The specifications are discussed and explained in Chapter 3.

Table 1.1 Target Specifications.

System Simulator	Matlab/Simulink
Circuit Simulator	Cadence Virtuoso Custom Design Platform
Technology	CSM CMOS 0.18μm with 1-poly 6-metal
Modulator Order	3rd
Modulator Type	CT low-pass
Architecture	Single loop feedforward
Input Bandwidth	5MHz
Over Sampling Ratio (OSR)	20
Sampling Frequency	200MHz
Noise Transfer Function (NTF) Type	High pass Butterworth with one optimized zero
Maximum NTF Out-of-band Gain	1.6
Quantizer Resolution	1-bit
Digital-to-analog Converter (DAC) Type	Non-return-to-zero (NRZ)
Dynamic Range	≥ 50dB
Effective Number Of Bits (ENOB)	≥ 8 bits
Maximum Internal States	≤ 0.8 (normalized to feedback level)
Anti-aliasing	Inherent
Power Supply	1.8V

1.4 Organization of the Thesis

This report is divided into five chapters:

Chapter 1 gives the background, motivation and objectives of this project. It also includes the organization of this report.

Chapter 2 reviews the modulator architectures, including both DT and CT DSMs. A brief introduction on DSM is given at the beginning of the chapter, followed by basic theory of sampling and quantization. A general model of DSM is presented and CT DSM is discussed in more details. At the end of this chapter, prior works on the CT DSM is studied.

Chapter 3 presents and discusses the system level design and simulation. As mentioned in Chapter 2, the system level design starts from a DT DSM model. The DT synthesis and simulation are covered, followed by DT-to-CT transformation and CT DSM simulation. At the end, system level design of a CT DSM used for dual-mode ultrasonic application is presented.

Chapter 4 presents and discusses the transistor level design and simulation. After the system level design and simulation, transistor level implementation is discussed on various blocks, including transconductors, quantizer and DAC. Full circuit simulation is presented. Furthermore, layout implementation and consideration are also included.

Chapter 5 summarizes this report with conclusions and future works.

Chapter 2 Delta-Sigma Modulator

Over the last two decades, data conversion techniques including analog-to-digital and digital-to-analog (D/A) conversion have developed rapidly. In many applications such as communication, instrumentation, medical imaging and consumer electronics, the signal is favored to be processed in the digital domain due to noise insensitivity and programmability [9]. Some of them, for instance wireless communication and ultrasound imaging, require the front-end ADC with high/medium resolution and wide bandwidth capability [3, 19-26]. Conventionally, pipeline and successive-approximation register (SAR) ADCs are dominant in such applications due to their high throughput rate and acceptable resolution as shown in Figure 2.1.

Figure Source: Analog Devices Inc., Analog Dialogue, 2005

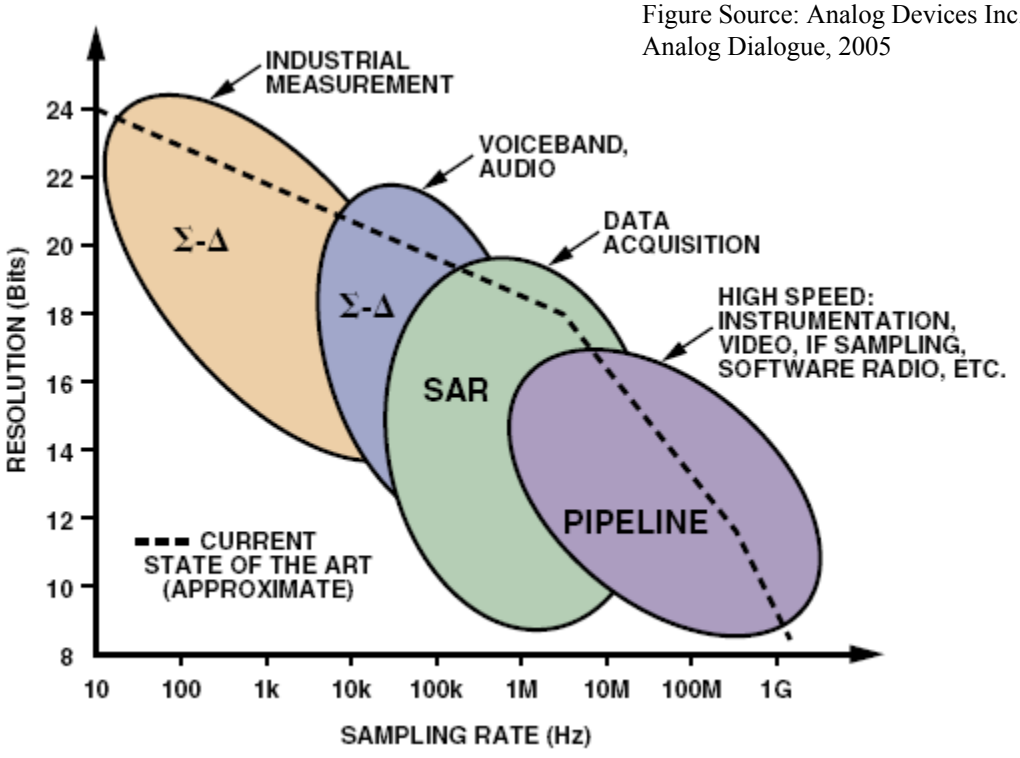

Figure 2.1 ADC Resolution vs. Sampling Rate for Different Applications.

On the other hand, oversampling delta-sigma ADCs are typically employed when high resolution is needed [13, 14]. Comparing with the Nyquist rate ADCs, the main advantage of the DSMs is that they are much less sensitive to the non-idealities of the building blocks, due to the extensive use of digital signal processing [13, 14]. Therefore, higher resolution can be achieved.

Recently, research has successfully shown CT DSM type ADCs as an alternative to the Nyquist rate high speed ADCs with relaxed requirements and higher power efficiency [3, 19-26]. Nevertheless, they do have a number of drawbacks such as sensitivity to excess loop delay and clock jitter, which will be discussed and presented in details later.

2.1 A Brief Introduction on Delta-Sigma Modulator [13, 14]

As shown in Figure 2.2, the basic concepts used in a DSM are oversampling, digital filtering and noise shaping. Figure 2.2 (a) shows a noise spectrum of a Nyquist-rate ADC with sampling frequency of f_s, where the analog input signal's bandwidth is limited between DC and $f_s/2$. The quantization noise, which is the error generated by the finite resolution ADC in the quantization process, is uniformly spread over the whole bandwidth $f_s/2$.

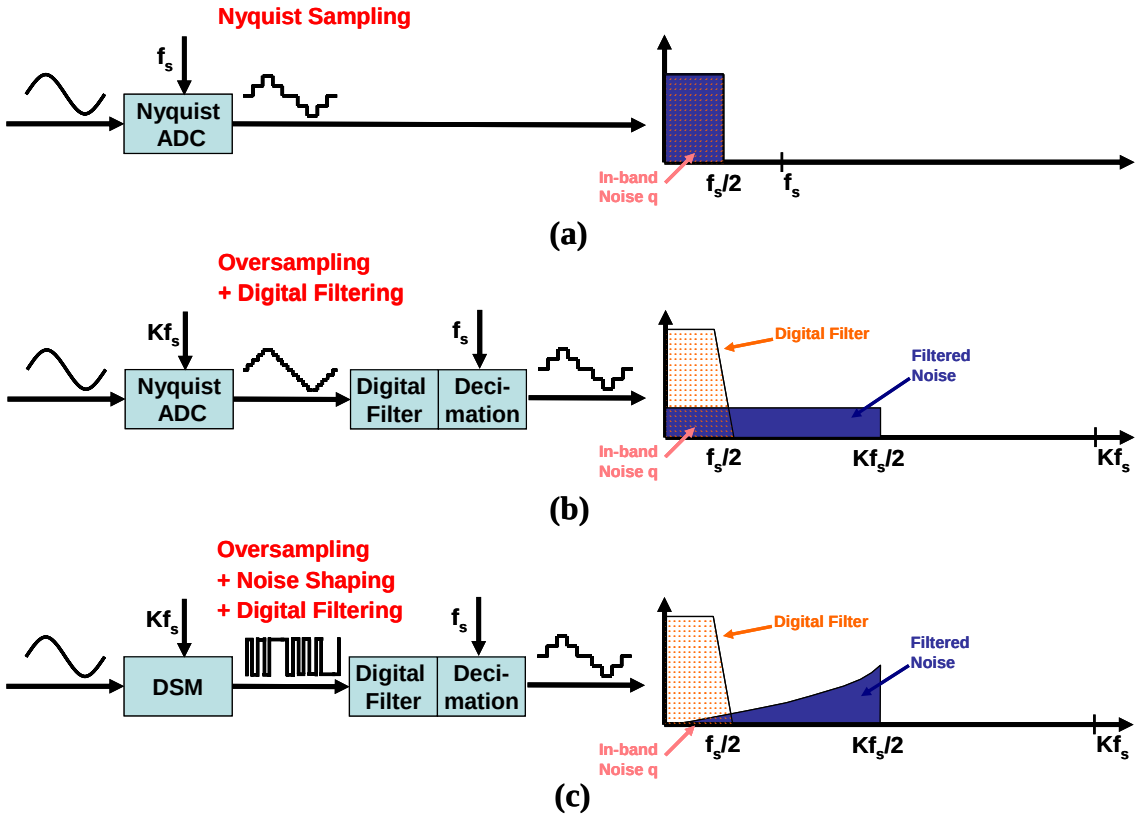

Figure 2.2 In-band Noise Spectrum with (a) Nyquist Sampling (b) Oversampling (c) Oversampling and Noise Shaping.

In Figure 2.2 (b), the same ADC is used but the sampling frequency has been increased by a factor of *K*. The input bandwidth remains as $f_s/2$ and the quantization noise is uniformly spread over half of the sampling frequency, $Kf_s/2$. The out-of-band noise can be removed by a digital filter and the remaining in-band noise is much less. For each doubling of *K*, the in-band noise is reduced by 3dB, resulting in a 3dB increase in terms of SNR.

Figure 2.2 © shows the noise shaping concept in a DSM in order to further filter the in-band quantization noise. The analog input is converted into a one bit data stream by the

DSM and the in-band information is modulated in the data stream. The effect is to shape the quantization noise so that most of it occurs outside the band. Therefore, the SNR can be greatly increased with the help of oversampling and noise shaping. With a higher order DSM, more noise will be pushed outside of the band, resulting in more efficient noise shaping.

A simplified structure of a first-order DSM is illustrated in Figure 2.3. Basically, it consists of an integrator (loop filter), a comparator as a one-bit ADC (quantizer) and a (voltage/current) switch as a one-bit DAC. As in any negative feedback system with a sufficient high loop gain, the average value of the signal at the input of the integrator (loop filter) must be zero. Therefore, the low frequency portion of the output of the DAC must equal to the input of the DSM. Assuming the DAC is ideal, the in-band signal of the DAC's input (the output data stream) must equal to the modulator input. In other words, the analog input of the DSM is converted into digital data stream and the in-band information is modulated in the data stream. The digital form can then be reconstructed by digital filtering and decimation as illustrated previously in Figure 2.2. More details on sampling, quantization and modulator will be explained in the following sections in this chapter.

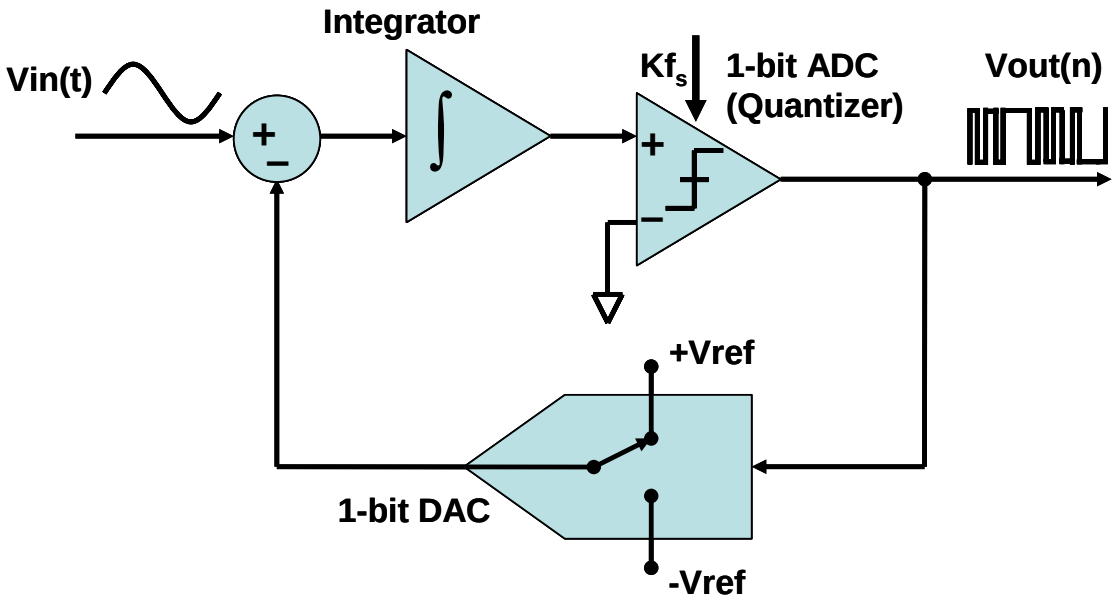

Figure 2.3 Simplified First-order Delta Sigma Modulator

2.2 Sampling and Quantization

2.2.1 Oversampling

A/D conversion can be separated into two operations: uniform sampling in time and quantization in amplitude [27]. A CT signal $x(t)$ is sampled periodically at uniformly spaced time intervals T_s or fixed sampling frequency $f_s = 1/T_s$. In the time domain, the samples of the signal can be written as $x[n] = x(nT_s)$, where n represents the number of a particular sample. In the frequency domain, infinite numbers of periodically repeated copies of the original signal spectrum are created at multiples of f_s [28] as shown in Figure 2.4, where f_B is the signal bandwidth. The spectra of the sampled signal can be expressed as:

$$X_s(f) = \frac{1}{T_s} \cdot \sum_{-\infty}^{\infty} X(f - k \cdot f_s) \tag{2.1}$$

The equation reveals that sampling in the time domain translates into convolution of the signal spectrum with a periodic Dirac pulse train in the frequency domain [28].

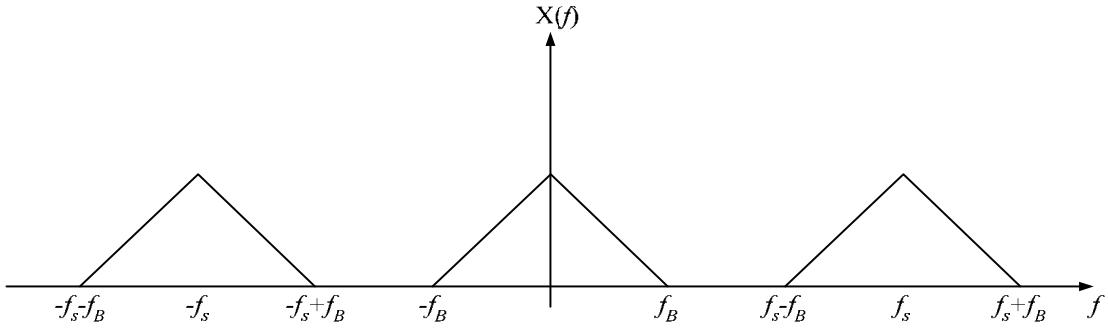

Figure 2.4 Sampled Data Spectra.

Theoretically, if the repeated spectra do not overlap, the original signal can be reconstructed with a suitable filter. Thus the signal must be band limited to half of the sampling frequency, or $f_s \geq 2f_B = f_N$ which is the well known Nyquist theorem [28], where f_N is called the Nyquist rate. In practice, an anti-aliasing filter (AAF) is often used before the signal is sampled in order to ensure that the signal is band limited to $f_s/2$. However, when $f_s = 2f_B$ an impractical AAF with very sharp transition at the edge of f_B has to be designed. On the other hand, analog filters with a gentle roll-off are easier to design and tend to be more power and area efficient [16]. Therefore, even Nyquist rate ADCs are sampled at a slightly higher frequency than f_N, usually 1.5-10 times [29]. The ratio between the sampling frequency and the Nyquist rate is defined as oversampling ratio (OSR):

$$OSR = \frac{f_s}{f_N} = \frac{f_s}{2f_B} \tag{2.2}$$

2.2.2 Quantizer and Quantization Noise

Unlike the sampling operation which is completely invertible in theory, the quantization process inevitably introduces errors since an infinite number of input values are mapped to a finite number of output values. A device which carries out quantization process is called a quantizer as shown in Figure 2.5. The transfer function curve and the quantization error curve of a bipolar 4-step mid-tread quantizer are shown in Figure 2.6. The input step size is defined as one least-significant bit (LSB) size which equals to two units and the output step size of the quantizer is represented by Δ which also equals to two units. As shown in Figure 2.6 (a), it is often desirable to approximate the transfer curve with a straight line $v = k \cdot y$, where k is the equivalent gain of the quantizer and usually assumed to be one [14]. A more precise definition for the quantization error e is the difference between the actual output (solid line) and the approximate output (dashed line). The quantization error curve with no-overload input range is illustrated in Figure 2.6 (b). The no-overload input range is defined as from – (M + Δ/2) to + (M + Δ/2), where M is the number of steps and it equals to four here. In the no-overload range, the quantization error is always limited within ± Δ/2.

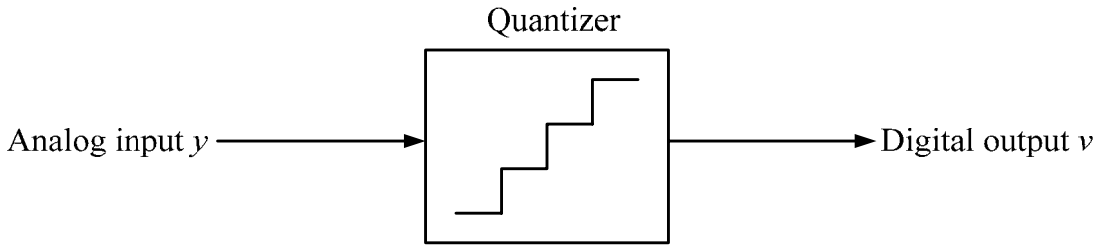

Figure 2.5 Quantizer.

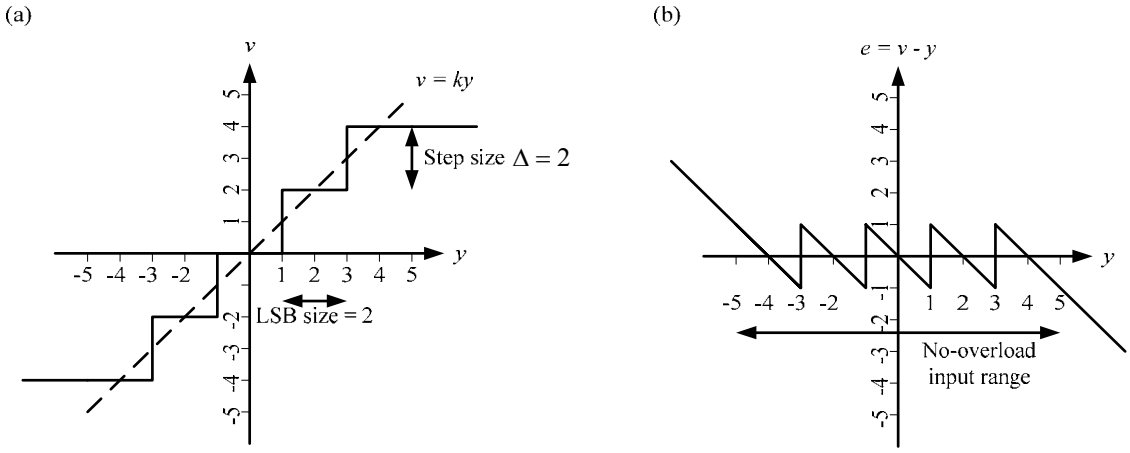

Figure 2.6 (a) Transfer Function and (b) Quantization Error of A Bipolar 4-step Mid-tread Quantizer.

Ideally, a quantizer is fully deterministic and hence the quantization error e and the quantizer output v are fully determined by the input y. However, if y changes rapidly and sufficiently large amounts from sample to sample and y stays in the no-overload range, e tends to be uncorrelated with y and its probability density function (PDF) is uniformly distributed between $\pm\Delta/2$ in amplitude. Therefore, it is possible to transform the deterministic quantization error e to the stochastic linear quantization noise e. This also

replaces a highly nonlinear system with a relatively simple linear system as shown in Figure 2.7.

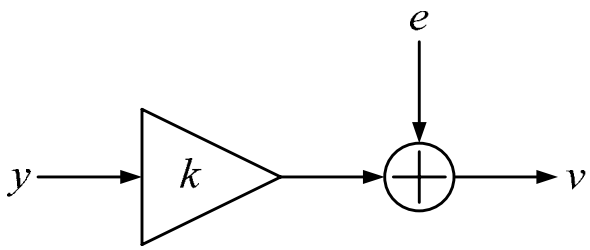

Figure 2.7 Quantizer Linear Model.

The linear approximation of a quantizer yields the following properties [16]:

1. *e* is random.
2. *e* is uncorrelated with *y*.
3. the PDF of *e* is uniform between ± Δ/2.
4. the power spectral density (PSD) of *e* is white

A linear model of the quantizer can be represented as in Equation (2.3), where *e* is the added quantization noise assumed to be uniformly distributed between ±Δ/2 and k is the equivalent quantizer gain which is usually assumed to be one.

$$v = ky + e \tag{2.3}$$

Also, the quantization noise power can be expressed as in Equation (2.4) [29]. However, such assumption is not always valid, especially when the input of the quantizer *y* is

constant or periodically varying with a frequency harmonically related to f_s [14], even when y is in the no-overload range.

$$\sigma_e^2 = \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 \cdot \frac{1}{\Delta} de = \frac{\Delta^2}{12} \tag{2.4}$$

It should be noted that in this model, the quantization noise power is fixed since $\Delta = 2$. As the quantizer resolution increases, the full scale (FS) also increases accordingly. Therefore, the SNR of the quantizer increases proportionally with the resolution of the quantizer. With the white noise assumption, the two-sided PSD of quantization noise can be written as:

$$S_e(f) = \frac{\Delta^2}{12} \frac{1}{f_s} \tag{2.5}$$

The total in-band noise (IBN) after an ideal digital filter can be calculated as:

$$IBN = \int_{-f_B}^{f_B} S_e(f)\, df = \frac{\Delta^2}{12} \frac{2f_B}{f_s} = \frac{\Delta^2}{12} \frac{1}{OSR} \tag{2.6}$$

This is another benefit from oversampling besides the relaxed requirement of the AAF: the IBN decreases by one half or equivalently 3dB or 0.5-bit with OSR doubled. It will be

shown in next section that together with noise shaping, oversampling reduces the IBN more efficiently.

Single-bit or binary quantizer is used in this project in order to simplify the beamforming hardware [3]. Usually binary quantization employs mid-rise quantizer and its transfer function curve is shown in Figure 2.8. Unlike in a multi-bit quantizer, the gain in a single-bit quantizer is not easily defined. In Figure 2.8, one can draw infinite number of lines to represent the effective gain of the single-bit quantizer as there are infinite sets of *y* mapping to only two values of *v*. The ambiguity of the gain is due to the fact that *v* only depends on the polarity but not the magnitude of *y*.

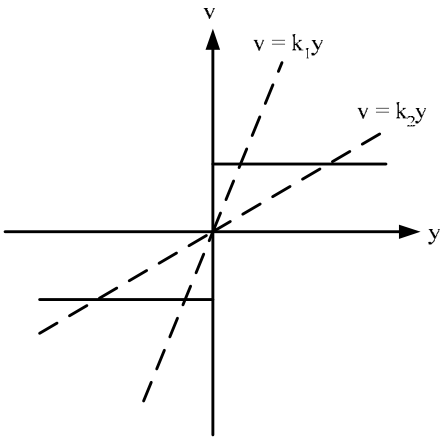

Figure 2.8 Single-bit Quantizer Transfer Function Curve.

In [14], a statistical way of obtaining *k* is proposed by extensive numerical simulations. The gain is defined in Equation (2.7), where E[ ] represents the mean value. The not-well-defined gain of a single-bit quantizer also makes the whole DSM system less stable compared to that with a multi-bit quantizer. This issue will be studied in section 2.3.2. Nevertheless, the main advantage of single-bit quantizer is that the corresponding single-

bit D/A conversion is inherently linear, resulting in simple DAC design and hardware [13, 14].

$$k = \frac{E\left[|y|\right]}{E\left[y^2\right]} \tag{2.7}$$

2.3 Delta-Sigma Modulator

2.3.1 Model of Discrete-Time Delta-Sigma Modulator [14]

A widely used model of DT DSM with single-quantizer is shown in Figure 2.9, where capital letters *U*, *Y* and *V* represent the input of the DSM, the input of the quantizer and the output of the quantizer in the z-domain respectively. The loop filter is a two-input (L_0 and L_1) one-output (Y) system, whose transfer function can be expressed as:

$$Y(z) = L_0(z)U(z) + L_1(z)V(z) \tag{2.8}$$

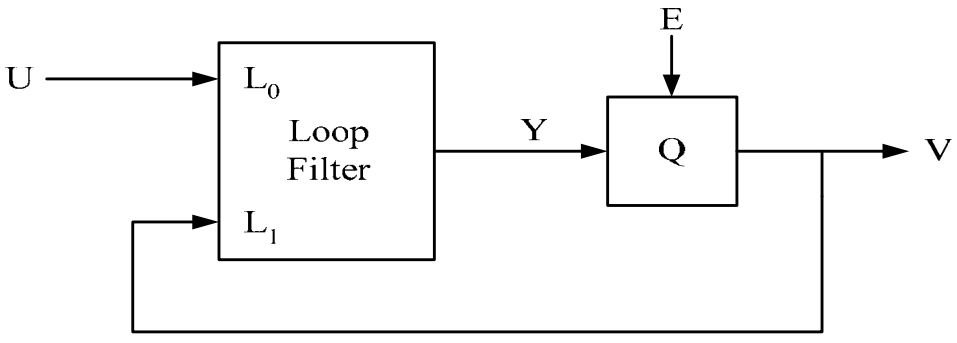

Figure 2.9 General Model of a Single-Quantizer DSM.

With the linear model of the quantizer and assuming the reference voltage is unity, the output of the quantizer can be expressed in Equation (2.9), where *E(z)* is the quantization error:

$$V(z) = Y(z) + E(z) \tag{2.9}$$

With Equations (2.8) and (2.9), the modulator output *V(z)* can be re-written as:

$$V(z) = \frac{L_0(z)}{1 - L_1(z)} U(z) + \frac{1}{1 - L_1(z)} E(z) \tag{2.10}$$

The loop filter output is:

$$Y(z) = STF(z)U(z) + \left[NTF(z) - 1 \right] E(z) \tag{2.11}$$

The noise transfer function (NTF) and signal transfer function (STF) are defined as:

$$NTF(z) = \frac{1}{1 - L_1(z)} \tag{2.12}$$

$$STF(z) = \frac{L_0(z)}{1 - L_1(z)} \tag{2.13}$$

and conversely,

$$L_0(z) = \frac{STF(z)}{NTF(z)} \tag{2.14}$$

$$L_1(z) = 1 - \frac{1}{NTF(z)} \tag{2.15}$$

So Equation (2.10) can be re-written as:

$$V(z) = STF(z)U(z) + NTF(z)E(z) \tag{2.16}$$

or,

$$V(z) = U(z)z^{-1} + E(z)\left(1 - z^{-1}\right) \tag{2.17}$$

Hence, the output of the DSM can be intuitively viewed as a linear combination of the modulator input $U(z)$ after being filtered by $STF(z)$ whose magnitude is close to unity in-band, and the quantization error $E(z)$ after being filtered by $NTF(z)$ whose magnitude is very low in-band. In other words, the quantization error (as well as any non-idealities associated with the quantizer itself) is shaped by $NTF(z)$ before being added to the modulator output. This unique noise shaping property makes the DSM superior and efficient in achieving high resolution compared to the Nyquist converters.

The choice of $STF(z)$ and $NTF(z)$ can be arbitrary [14, 29]. In order to eliminate the in-band power of the quantization noise, the $NTF(z)$ is designed to be a high-pass filter, i.e.,

small amplitude in-band and large amplitude out-of-band. The $STF(z)$ is normally designed to be flat through all frequency. Therefore, Equation (2.12) implies that $L_1(z)$ must be as large as possible in-band in order to reduce the magnitude of $NTF(z)$ and Equation (2.13) suggests that $L_0(z)$ must also be large in the same range to make $STF(z)$ close to unity. Usually, this is achieved by letting $L_0(z)$ and $L_1(z)$ share the same set of poles. In a simple case the input signal $U(z)$ is only delayed by k clock periods and the quantization error $E(z)$ is differentiated by N times, where N is the order of the DSM, resulting in:

$$STF(z) = z^{-k} \tag{2.18}$$

$$NTF(z) = \left(1 - z^{-1}\right)^N \tag{2.19}$$

For first-order modulator (MOD1), let k equal to one and N equal to one, then:

$$\left|STF(z)\right| = \left|z^{-1}\right| = 1 \tag{2.20}$$

$$\left|NTF(z)\right| = \left|\left(1 - z^{-1}\right)\right| = \left|1 - e^{-j2\pi f/f_s}\right| = 2\sin\left(\frac{\pi f}{f_s}\right) \tag{2.21}$$

With the PSD calculated from Equation (2.5), one can simply derive the maximum SNR for a single-bit quantizer MOD1 as [14, 29]:

$$SNR_{\max}/dB = 1.76 - 5.17 + 30\log(OSR) = -3.41 + 30\log(OSR) \tag{2.22}$$

Similarly, by choosing k equals to one and N equals to two, a simple MOD2 can be designed and its maximum SNR can be shown as [14, 29]:

$$SNR_{\max} / dB = 1.76 - 12.9 + 50\log(OSR) = -11.14 + 50\log(OSR) \tag{2.23}$$

Therefore, oversampling together with noise shaping improves the SNR effectively, 1.5 bits/octave for MOD1 and 2.5 bits/octave for MOD2, while oversampling without noise shaping can only achieve 0.5 bits/octave.

From Equation (2.19), the $NTF(z)$ and $L_1(z)$ for MOD1 can be derived as shown below:

$$NTF(z) = \left(1 - z^{-1}\right)^1 \tag{2.24}$$

$$L_1(z) = 1 - \frac{1}{NTF(z)} = 1 - \frac{1}{\left(1 - z^{-1}\right)^1} = -\left(\frac{z^{-1}}{1 - z^{-1}}\right) \tag{2.25}$$

It can be seen that $L_1(z)$ can be constructed as a delaying integrator with a negative sign (minus at feedback).

Similarly for MOD2:

$$NTF(z) = \left(1 - z^{-1}\right)^2 \tag{2.26}$$

$$L_1(z) = 1 - \frac{1}{NTF(z)} = 1 - \frac{1}{\left(1-z^{-1}\right)^2} = \frac{\left(z^{-1}\right)^2 - 2z^{-1}}{\left(1-z^{-1}\right)\left(1-z^{-1}\right)} = \left(\frac{z^{-1}}{1-z^{-1}}\right)\cdot\left(\frac{z^{-1}-2}{1-z^{-1}}\right) = \left(\frac{z^{-1}}{1-z^{-1}}\right)\cdot\left(-1-\frac{1}{1-z^{-1}}\right) \quad (2.27)$$

The block diagrams of the simple MOD1 and MOD2 are shown in Figure 2.10 and Figure 2.11 respectively. It should be noted that the DAC is omitted in the figures since a unity reference is assumed. However, in practice, Equation (2.19) is not always used to synthesize NTF, especially for higher order (greater than two) modulator. One reason is that higher order NTF generated by Equation (2.19) is susceptible to instability which will be discussed in the next section.

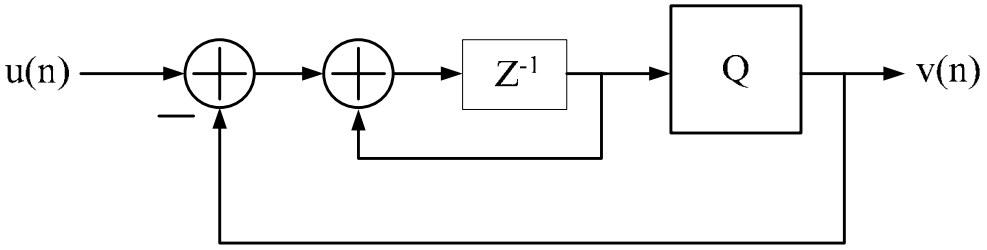

Figure 2.10 MOD1.

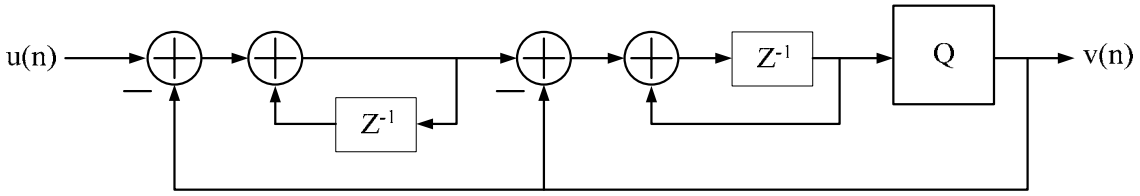

Figure 2.11 MOD2.

2.3.2 Stability of Single-Bit Delta-Sigma Modulator

From Equations (2.9) to (2.13), the stability seems to be solely determined by $L_1(z)$ since it is the only variable in the denominator in Equation (2.10) so by $NTF(z)$ from Equation (2.12). However, in practice it has been demonstrated that the input magnitude and therefore the STF are also relevant in determining the stability of the modulator [14]. This is basically due to the fact that the quantizer is nonlinear but the equations are derived from the linearized quantizer model. As a result, the quantizer resolution also affects the stability. Thus, more often determining how large an input the modulator can handle without being unstable is of more interest than whether the modulator is unconditionally stable. In fact, a higher order single-loop single-bit DSM can hardly be stable when the input magnitude is very close to the feedback reference. In summary, the stable input range is determined by $STF(z)$, $NTF(z)$ and the resolution of the quantizer. In this section, the stability issue is only studied for single-bit DSM, while stability considerations on multi-bit DSM can be found in [13, 14]. Furthermore, since $STF(z)$ is essentially like a pre-filter, the stable input range is primarily determined by $NTF(z)$.

It is clear that MOD1 is unconditionally stable with arbitrary inputs less than or equal to the feedback reference and MOD2 is very likely to be stable in practice when the input magnitude is smaller than 0.8-0.9 (assume the feedback reference is normalized to unity)[14]. In a higher order modulator, especially in single-bit DSM, the stable input range is usually a few dB below the feedback reference [14]. To design a single-bit DSM, the (modified) Lee criterion [30, 31] is widely used. The Lee criterion states that a binary DSM is likely to be stable if the maximum gain of the NTF is smaller than 1.5. This

criterion is neither sufficient nor necessary but it still proves to be useful in most cases. For moderate order (three to four) modulators, slightly higher values are tolerable, while for very high order modulators (greater than seven), 1.4 is used instead of 1.5 in the criterion [14]. A sufficient and necessary condition for the maximum NTF gain is still unavailable and even Lee criterion has no solid theoretical foundations. Thus, usually extensive simulations are necessary to confirm the stability after one NTF is chosen based on Lee criterion.

Since the effective quantizer gain k in single-bit quantizer is not well defined, several techniques including root-locus plot, Bode plot and Nyquist plot were proposed to predict the range of the gain for stable operation. Unfortunately, all these techniques are based on the same linear quantizer model but in fact the quantizer is highly nonlinear and its gain is signal dependent. Consequently, all the techniques based on the linear model cannot be used to predict instability accurately in practice [14]. Therefore, again extensive simulations are necessary to check the stability of the modulator, especially on the design of a high order single-bit DSM.

2.3.3 Optimization of Noise Transfer Function

Since the STF only serves to filter the input signal, it is less important than the NTF in determining the peak SNR [14]. This is because the STF is ideally unity gain in-band whereas the NTF is used to filter the in-band quantization noise. Hence, maximizing the SNR in system level is often achieved by optimizing the NTF. In the previous section, the MOD1 and the MOD2 models shown in Figure 2.10 and Figure 2.11 are both synthesized

with Equation (2.19) by setting N equals to one and two respectively. In this case, all the NTF zeroes are located at z equals to one and all the NTF poles are located at z equals to zero. In fact, it can be shown that significant SNR improvement (for MOD2 and higher order modulators) can be obtained by spreading the zeroes on the unit circle and by locating the poles within the unit circle. Consequently, the IBN is reduced (by spreading the zeroes) and the stability is improved due to the reduced out-of-band NTF gain (by moving the complex poles close to zeroes).

Before optimizing the NTF zeroes, it is always assumed that the poles of the NTF have little effect on the IBN [14]. This approximation is usually true since the STF also shares the poles with the NTF and the STF is designed to be flat in-band. Thus the effect of the NTF poles on the transfer function is usually minimal in-band. The principle of optimizing zeroes is to minimize the IBN with respect to the zeroes while the optimal zeroes are found by equating the partial derivatives of the integral to zero. As a simple example, let a pair of zeroes of MOD2 be $e^{\pm j\alpha}$, where α is normalized to ω_s. Thus the NTF can be written as below, where $D(z)$ consists of the poles of $NTF(z)$:

$$NTF\left(j\omega\right)=\frac{\left(z-e^{j\alpha}\right)\left(z-e^{-j\alpha}\right)}{D\left(z\right)} \tag{2.28}$$

Assuming the quantization noise is white and |D(z)| is flat in-band, the IBN can be approximated as:

$$\begin{aligned} IBN(\alpha) &= \int_0^{\omega_B} S_e(f)\cdot NTF(j\omega)\,d\omega = S_e(f)\cdot\frac{1}{D(z)}\cdot\int_0^{\omega_B}\left|\left(z-e^{j\alpha}\right)\left(z-e^{-j\alpha}\right)\right|d\omega \\ &\approx S_e(f)\cdot\frac{1}{D(z)}\cdot\int_0^{\omega_B}\left(\omega^2-\alpha^2\right)d\omega = \frac{1}{5}\omega_B^5-\frac{2}{3}\omega_B^3\alpha^2+\omega_B\alpha^4 \end{aligned} \tag{2.29}$$

Differentiating Equation (2.29) with respect to α and equating the result to zero gives the optimum zeroes as:

$$\alpha_{opt} = \frac{\omega_B}{\sqrt{3}} \tag{2.30}$$

Figure 2.12 and Figure 2.13 plot the NTF poles (crosses) and zeroes (squares) and NTF frequency response with and without optimized zeroes respectively. Clearly, the optimization of zeroes in MOD2 results in 3.5dB SNR improvement with OSR equals to 64. Similarly, zeroes in higher order NTF can also be optimized in this way. Optimum zero locations for higher order modulators up to eighth-order can be found in Table 2.1[14].

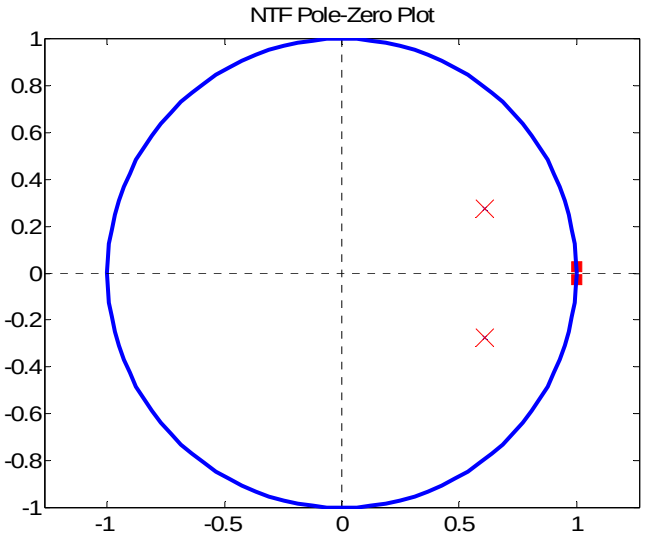

Figure 2.12 Second-order NTF Pole-Zero Plot.

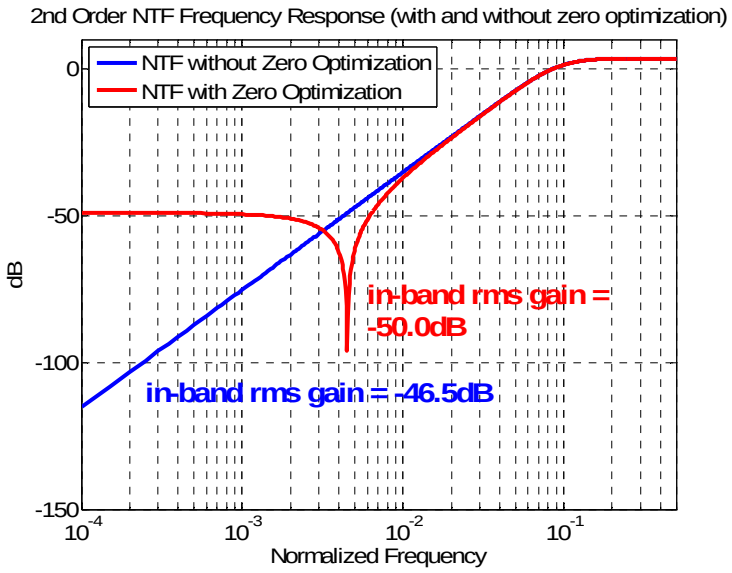

Figure 2.13 Second-order NTF Frequency Response.

Table 2.1 Optimized Zero Location.

Order	Zero locations normalized to bandwidth	SNR improvement (dB)
1	0	0
2	±0.57735	3.5
3	0, ±77460	8
4	±0.33998, ±0.86114	13
5	0, ±0.53847, ±0.90618	18
6	±0.23862, ±0.66121, ±0.93247	23
7	0, ±0.40585, ±0.74153, ±0.94911	28
8	±0.18343, ±0.52553, ±0.79667, ±0.96029	34

To determine the poles, the NTF has to be realizable in the first place, meaning $H(\infty) = 1$ [14]. This is to prevent any delay-free loop, which is unrealizable physically, to be formed. Secondly, and probably more important for a single-bit DSM, the out-of-band NTF gain should be set properly to satisfy the stability requirement. When optimizing the zeroes, the influence of the poles on the magnitude of the NTF gain in-band is assumed to be minimal. Also, since the STF shares the same poles with the NTF, the NTF denominator needs to be flat in-band.

Usually, to synthesize and optimize the NTF, one can use either the cookbook design provided in [13], or software tools like [23, 32]. In this project, the Matlab toolbox developed by the first author of [14] is utilized to design the DT DSM in system level.

2.3.4 Loop Filter Architectures for Low-pass Delta-Sigma Modulators

There are many ways to realize the loop filter inside the DSM, and in [14] the loop filters are classified into four types: cascaded integrators with distributed feedback (CIFB), cascaded resonators with distributed feedback (CRFB), cascaded integrators with weighted feedforward (CIFF) and cascaded resonators with weighted feedforward (CRFF). In general, the majorities of the modulators can be categorized into two classes: feedback type and feedforward type as shown in Figure 2.14. Figure 2.14 can be used to construct higher order modulator, for example, third-order modulator (MOD3) and forth-order modulator (MOD4). The modulator order is determined by the number of integrators in the loop filter. Therefore, three integrators are used to build a MOD3 in Figure 2.14. Similarly MOD4 contains four integrators. The details of determining the feedback and feedforward coefficients of the modulator will be discussed in the next chapter.

As discussed in the previous section, zero optimization in the NTF can be used to improve the SNR. Here in Figure 2.14 the zero is created by the local feedback g_1. The DAC is used to convert the digital output (e.g., +1 or -1) into analog feedback (e.g., +1.8V or -1.8V) to the filter.

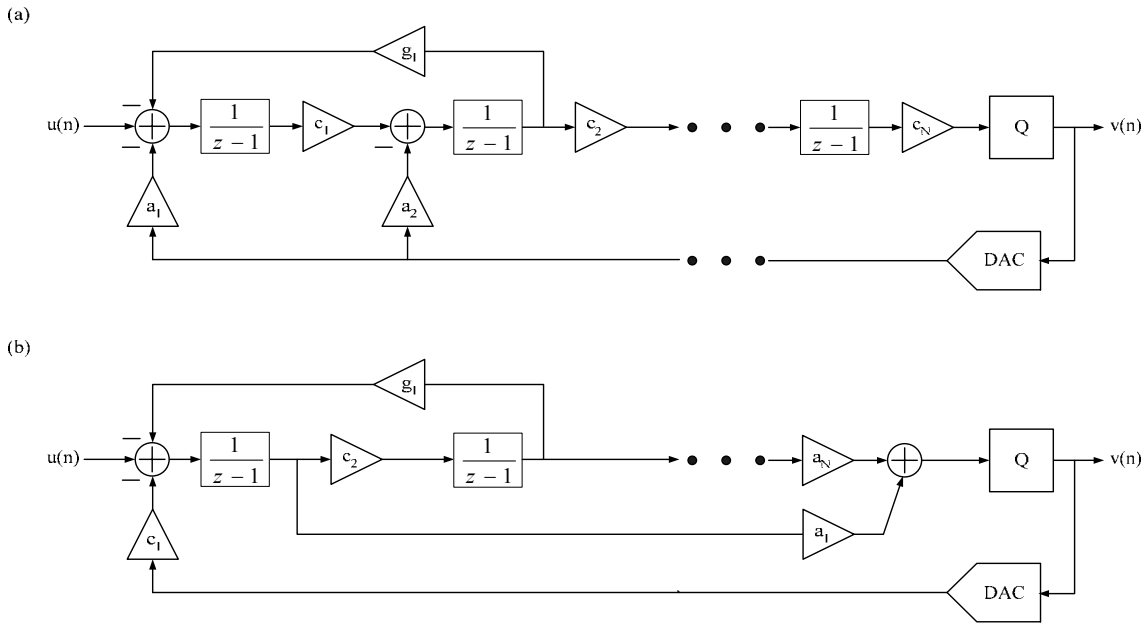

Figure 2.14 Implementation of Nth-order Delta-Sigma Modulator with (a) Distributed Feedback and Local Feedback (b) Weighted Feedforward and Local Feedback.

The feedback type loop filter has two major drawbacks. Firstly, the number of DAC branches equals to the order of the DSM so that all the integrators need to handle fast varying DAC pulses. On the other hand, the feedforward type DSM has only one DAC branch feedback to the input regardless of the modulator order. Secondly, the integrator outputs contain significant portion of the input signal [16], which places strict requirement in terms of swing capability and linearity on the integrators. This can be explained as: for instance, in the feedback type loop filter, since the input to the second integrator has to be zero-averaged, the weighted output of the first integrator must equal to the weighted output of the DAC. The DAC contains the input signal itself and the shaped quantization noise. Thus, the output of the first integrator must also contain the

input signal (scaled) to fully cancel the DAC feedback. Similarly, all the other integrators except the last one must also carry certain portion of the input signal.

2.4 Continuous-Time Delta-Sigma Modulator

As mentioned earlier, there are two types of implementations in designing a DSM, namely DT DSM (in discrete-time) and CT DSM (in continuous-time). Both of them have their own advantages and disadvantages. The following sections will discuss why CT DSM is chosen and how it is transformed from a DT form. At last, the CT filter implementation will be studied.

2.4.1 Comparison between Discrete-Time and Continuous-Time Delta-Sigma Modulator

Over the last two decades, most published DSMs are realized in DT (discrete-time) form due to the advent of the switched-capacitor (SC) circuits in the 1980s. This is mainly because SC filters are more accurate and more linear than their counterpart CT (continuous-time) filters. For example, the time constant of SC filters relies on the relative matching of capacitors and the absolute value of clock frequency, and both of them can be controlled quite accurately in modern IC process. On the other hand, the time constant of CT filters is determined by the product of different types of devices (i.e., RC or C/G_m), whose absolute variation is up to 30% [29]. Therefore, tuning is inevitable in CT filter design, resulting in increased power consumption as well as hardware complexity. Despite all these drawbacks, CT DSMs are gaining increased interests in both research and industry mainly due to two key advantages: relaxed speed requirement

and inherent anti-aliasing. The loop filter representations for DT and CT DSMs are illustrated in Figure 2.15.

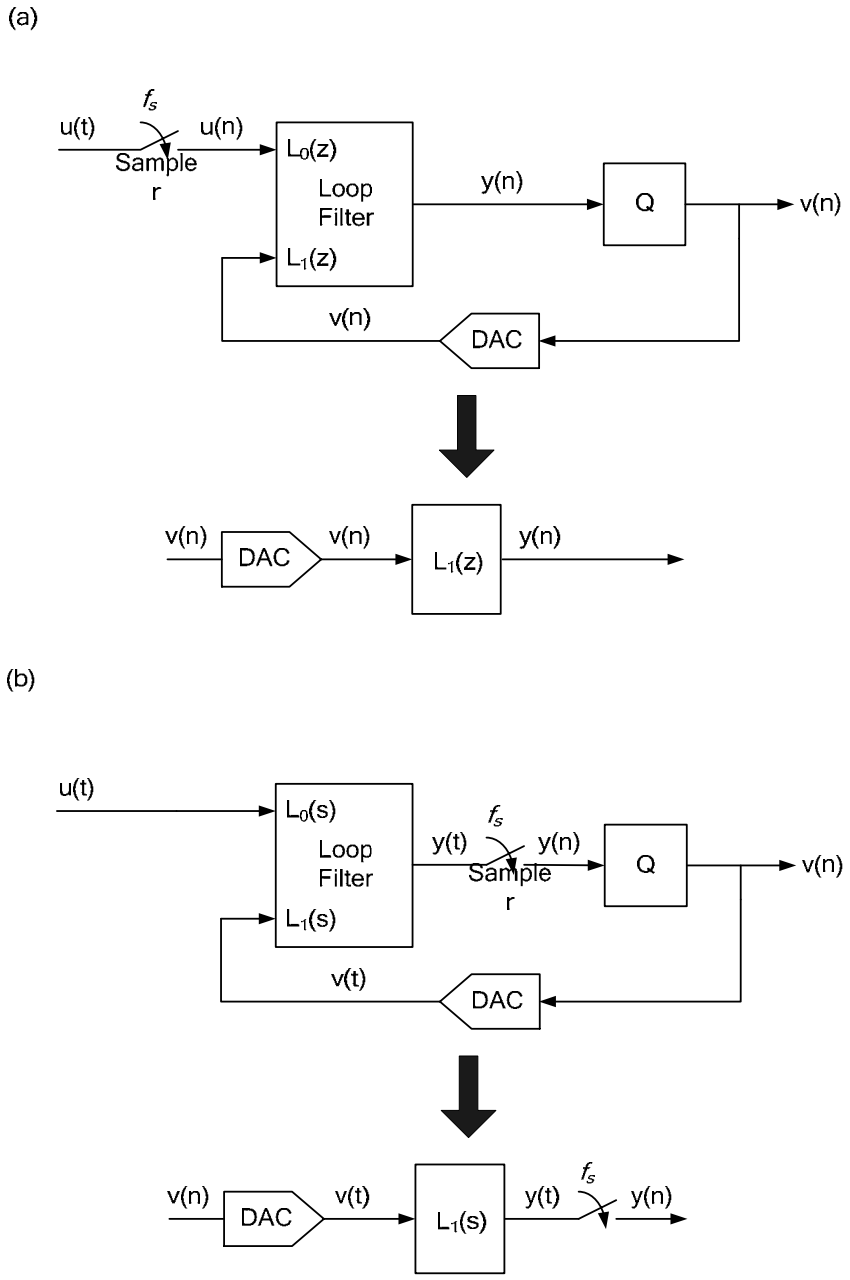

Figure 2.15 Loop Filter Representations for (a) Discrete-Time Modulator (b) Continuous-Time Modulator.

CT DSMs process signal in continuous form inside the loop filter, so the operational amplifier (opamp) speed requirement is reduced. Theoretically, CT DSMs are able to operate at a clock frequency one order higher than that can be achieved by DT DSMs. This also implies that CT DSMs can digitize signal with much wider bandwidth than DT DSMs can do. In practice, three to five times in terms of bandwidth improvement can be expected [16].

The sampler is placed after the CT filter in CT DSMs. The CT filter preceding the sampler is an AAF (anti-aliasing filter) providing certain degree (equals to the order of the modulator) of alias suppression. As a result, no dedicated AAF is needed in CT DSMs. Moreover, since the sampling operation is inside the loop filter, any non-idealities of the sampler will be shaped by the loop filter in the same way that the quantization noise is shaped. Hence, the S/H circuit (often combined with the quantizer) is much easier to design, while for other high speed data converters, the high speed S/H can be even more difficult to realize than the converters themselves [29].

Table 2.2 gives the comparison between DT and CT DSMs. The main issues listed in the table will be discussed in the remaining part of this report. To digitize the ultrasound signal with 5 MHz bandwidth, the CT DSM is chosen due to its higher sampling frequency compared to that of the DT DSM.

Table 2.2 Comparison between DT DSM and CT DSM.

	Discrete-Time (DT)	Continuous-Time (CT)
Popularity	Dominant in industry. Majority in research.	Start to get popular just recently, mainly in wireless communication.
Mapping	Easy to map mathematics onto implementation.	No direct mapping; normally need to transform to DT first.
Fs limit	Max sampling frequency is limited by settling time and opamp bandwidth, ~20% of GBW of opamp.	Max sampling frequency is limited by quantizer regeneration time and DAC update rate, one order higher than DT DSMs in theory.
Anti-aliasing	AAF is much relaxed but still required.	Inherent anti-aliasing: AAF can be eliminated.
Linearity and accuracy	High linearity and accuracy, depends on capacitor matching.	Low linearity and accuracy due to matching between different types of elements.
Power Consumption	Relatively high due to switching.	Less switching activities, in general lower than DT.
DAC Non-idealities	Not very sensitive to clock jitter.	Very sensitive to loop delay and clock jitter.

2.4.2 Discrete-Time to Continuous-Time Transformation

A CT loop filter can be synthesized either directly in the CT domain like in [23] or indirectly from the DT domain to the CT domain. This is because plenty of literature and software are available for the design of DT DSM. As a result, one can start the CT DSM design with the synthesis of a DT DSM and then transform the DT DSM into the equivalent CT DSM. The two most common transformation methods are the modified Z-transformation [16, 33] and the impulse-invariant transformation [15]. In this project, the impulse-invariant transformation is used because the modified Z-transformation does not generate correct result once excess loop delay is included in the model [15].

The condition to make a DT DSM and a CT DSM equivalent can be derived as follows: in the time domain, same waveforms must be applied at the inputs of both modulators.

For any given input waveforms in the CT domain if the two modulators are able to produce the same output bit stream in the DT domain, the two DSMs are said to be equivalent. Furthermore, the DT domain signals at the inputs of both quantizers must also be identical in order to generate the same outputs. Therefore, it can be concluded that the two DSMs are equivalent if, for the same input waveform, their quantizer input signals are equal at sampling instants [15].

As shown in Figure 2.15 on page 33, the loop filter representations for DT DSM and CT DSM are given. Although the sampling operation is inside the quantizer, the sampler is moved outside of the quantizer for illustration without altering the overall behavior. For both modulators, the loop is open around the quantizer and the modulator input is set to be zero. Therefore, two open-loop linear systems are formed without the quantizer which is a highly nonlinear system.

As shown in Figure 2.15 on page 33, the inputs and the outputs of the loop filters are DT quantities in both DT and CT open-loop systems, the two systems are equivalent as long as their outputs $y(n)$ are the same at sampling instants, with their inputs $v(n)$ being an impulse. In other words, the DT DSM and the CT DSM are equivalent if the impulse responses of their open-loop systems are identical at sampling instants, leading to [15]:

$$Z^{-1}[L_1(z)] = \mathcal{L}^{-1}[DAC(s)\cdot L_1(s)]|_{t=nT_s} \tag{2.31}$$

or in the time domain [33]:

$$l_1(n) = \left[dac(t) * l_1(t) \right] |_{t=nT_s} = \int_{-\infty}^{\infty} dac(\tau) \cdot l_1(t-\tau) d\tau \,|_{t=nT_s} \tag{2.32}$$

where $dac(t)$ and $l_1(t)$ are the impulse response of the DAC and the filter $L_1(s)$ respectively.

To simplify the transformation, the equivalence between s-domain and z-domain loop filter poles up to third-order is summarized in Table 2.3 [15]. In this project, the conversion is performed using this algorithm in Matlab.

Table 2.3 s-domain Equivalences for z-domain Loop Filter Poles.

z-domain pole	s-domain equivalent, $s_k = \ln(z_k)$	Limit for $z_k = 1$
$\frac{y_0}{z - z_k}$	$\frac{r_0}{s - s_k} \times \frac{y_0}{z_k - 1}$ $r_0 = s_k$	$\frac{r_0}{s - s_k}$ $r_0 = y_0$
$\frac{y_0}{(z - z_k)^2}$	$\frac{r_1 s + r_0}{(s - s_k)^2} \times \frac{y_0}{z_k (z_k - 1)^2}$ $r_1 = q_1 s_k + q_0$ $r_0 = q_1 s_k^{\,2}$ $q_1 = -z_k$ $q_0 = z_k - 1$	$\frac{r_1 s + r_0}{(s - s_k)^2}$ $r_1 = -0.5 y_0$ $r_0 = -y_0$
$\frac{y_0}{(z - z_k)^3}$	$\frac{r_2 s^2 + r_1 s + r_0}{(s - s_k)^3} \times \frac{y_0}{z_k^{\,2} (z_k - 1)^3}$ $r_2 = 0.5 q_2 s_k - q_1$ $r_1 = -q_2 s_k^{\,2} + q_1 s_k + q_0$ $r_0 = 0.5 q_2 s_k^{\,3}$ $q_2 = 2 z_k^{\,2}$ $q_1 = 0.5 + 1.5 z_k^{\,2} - 2 z_k$ $q_0 = (2 z_k - 1)^2$	$\frac{r_2 s^2 + r_1 s + r_0}{(s - s_k)^3}$ $r_2 = 0.333 y_0$ $r_1 = -y_0$ $r_0 = y_0$

It should be noted that the impulse-invariant transformation does not guarantee the equivalence in the signal path, i.e., the STFs of the DT and the CT modulators are not necessarily equivalent after the transformation. Nevertheless, the transformation still proves to be very useful since the STF is not as important as the NTF. In fact, the STF of CT DSM even provides inherent anti-aliasing which makes it quite different from that of DT DSM.

2.4.3 Continuous-Time Filter Implementation

In literature, most CT filters in CT DSM are implemented based on G_mC integrators [20, 22, 24, 34-39], or active G_mC integrators (also called Miller integrators or G_mC opamp integrators) [19, 40], or active RC integrators [21, 23, 25, 26, 41-46]. Other alternatives [16] including LC resonators (bulky inductor required), current-mode integrators (less accurate), log-domain integrators (lower frequency) and active MOSFET-C integrators (less accurate) are not commonly used.

As shown in Figure 2.16 (a), a G_mC integrator consists of a transconductor G_m and a capacitor C in an open-loop configuration. The common-mode feedback (CMFB) circuit is not shown in the figure. The input voltage is converted into current by the transconductor and then integrated on the capacitor to produce the output voltage, which can be expressed in the frequency domain as:

$$V_{out}(s) = \frac{I_{out}(s)}{sC} = \frac{G_m \cdot V_{in}(s)}{sC} \tag{2.33}$$

with the unity gain frequency:

$$\omega_0 = \frac{G_m}{C} \tag{2.34}$$

Where:

$$I_{out} = I_{out}^{+} - I_{out}^{-} \tag{2.35}$$

$$V_{out} = V_{out}^{+} - V_{out}^{-} \tag{2.36}$$

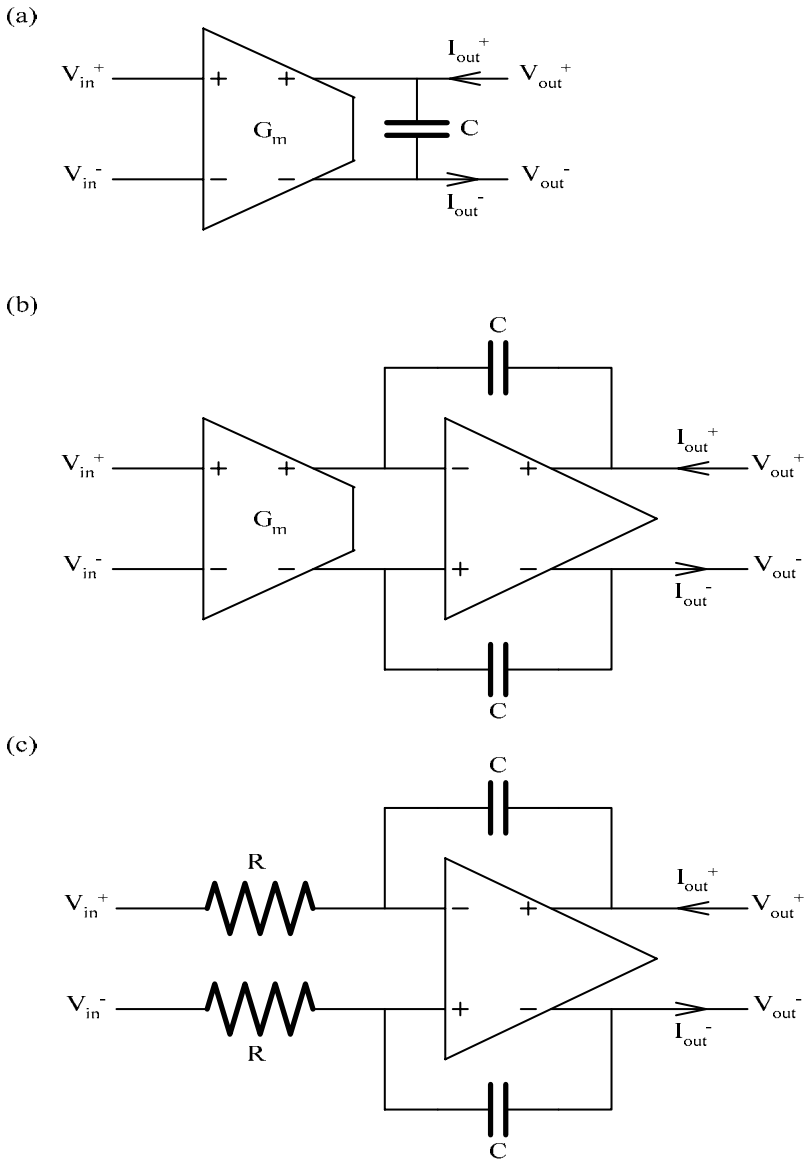

Figure 2.16 (a) G_mC Integrator (b) Active G_mC Integrator (c) Active RC Integrator.

It should be noted that compared with the active RC type integrator whose opamp drives a resistive load, the transconductor in G_mC integrator does not need a low-impedance

output stage. Thus, together with its open-loop feature, the G_mC integrator is faster than the other two and can be designed for wideband operation [47]. Moreover, the G_mC integrator is easily tunable and consumes less power than the other two integrators in low to medium dynamic range and high speed applications [47].

However, the G_mC integrator has two main drawbacks. One of them is the sensitivity to parasitic capacitance at the output of the integrator [29], which directly alters the effective unity gain frequency as well as the frequency response of the implemented filter. Besides, like any nonlinear system, the moderate linear transconductor produces harmonics (if the input is single-tone) or intermodulation distortion (if the input contains multiple tones) at the output of the integrator. The non-idealities of the G_mC integrator degrade the overall system performance in terms of dynamic range of the modulator.

To overcome the issue of the parasitic capacitance, in active G_mC integrator as shown in Figure 2.16 (b), an opamp is used and the influence of the parasitic capacitor becomes secondary since the output of the transconductor is now connected to the input of the opamp which is virtual ground. Nevertheless, the linearity of the transconductor is still limited and the opamp will consume significant amount of power if wide-band is required. Figure 2.16 (c) illustrates an active RC based integrator employing resistors for voltage-to-current conversion. In general, the passive integrated resistor is much more linear than the active transconductor so higher achievable SNR is expected when using active RC integrator. The price paid is that the required wide-band opamp is power hungry and low impedance stage is needed at the output of the opamp to drive the resistive load. In

literature, many CT DSMs based on G_mC integrators utilize one active RC integrator as the first stage [22, 34-36, 39] since it is the most critical stage and any non-idealities in the voltage-to-current conversion will be referred to input directly without any shaping [15, 16].

By considering the advantages and disadvantages of all the three types of integrators, since only medium dynamic range (8-bit) but wide-bandwidth (5MHz) as well as high sampling frequency (200MHz) are required in this project and more importantly the low power is the primary goal, G_mC type integrator was chosen to implement the CT filter.

2.5 Study of Prior Works

A summary of recently implemented (year 2000 – 2006) CT DSMs with measurement results is listed in Table 2.4. All of them were published in IEEE journal papers, mainly from IEEE Journal of Solid-State Circuits (JSSC).

In Table 2.4, effective number of bits (ENOB) is used to represent the resolution achieved by the modulator. It is defined as [29]:

$$ENOB = \frac{DR - 1.76}{6.02} \tag{2.37}$$

where DR is the dynamic range of DSM. DR is defined as [16] the ratio of the root mean square (RMS) value of the maximum input sinusoidal signal amplitude, for which the structure still operates correctly (referred as the maximum stable amplitude (MSA)), over the RMS value of the smallest detectable input sinusoidal signal (where 0dB SNR occurs). The MSA is defined as the maximum input amplitude, at which the modulator still operates correctly [16]. Most publications choose this level to be the input amplitude where the SNR drops 6dB below the peak value SNR.

ADC performance is often quantified by a figure of merit (FOM) which is related to power dissipation, ENOB and bandwidth f_B and it can be used to compare different modulator implementations. The FOM is defined as:

$$FOM = \frac{P}{2^{ENOB} \times (2 \times f_B)} (Joules / Conversion) \tag{2.38}$$

FOM can also be understood as the total amount of energy required for a successful A/D conversion with specified signal bandwidth and accuracy.

From Table 2.4, it is observed that most of the listed CT DSMs were designed to convert bandwidth in range of MHz and the modulator orders are from two to four. Many G_mC realizations of loop filter do not implement all integrators with G_mC type, but rather rely on active RC as the first stage to optimize the overall performance. By comparing the recent published works (2004 – 2008) with the earlier ones (2000 – 2002), it can be found that CT DSMs with multi-bit quantizer are becoming more popular, mainly because with

multi-bit quantizer the modulator is more stable and can achieve higher resolution. The main drawback of the multi-bit DSM is the nonlinearity of its DAC, resulting in more hardware used for improving the linearity [16].

Table 2.4 Performance of CT DSMs from Year 2000 to Year 2008.

Ref	Order	Q-Bit	Technology	ENOB	f_B/Hz	f_s/Hz	Power/mW	Implementation	FOM/pJ
[19]	4	1	Bipolar	6.2-12.3	1-62M	4G	3200	Active G_mC	351.0
[20]	2	1	Bipolar	6.9	990M	18G	1500	G_mC	6.6
[21]	6/10	1	Bipolar	12.0	25M	2.5G	6000	Active RC	29.3
[37]	2	1	Bipolar	6.4	250M	8G	1800	G_mC	44.1
[40]	4	1	Bipolar	8.0-12.7	1-60M	4G	3200	Active G_mC	104.2
[41]	2	1	BiCMOS 0.65	10.3	1M	100M	21.8	Active RC	8.6
[43]	3	1	CMOS 0.50	13.0	25K	2.4M	0.135	Active RC	0.3
[44]	3	5	CMOS 0.50	14.3	1.1M	35.2M	62	Active RC	1.4
[34]	4	1	CMOS 0.35	13.3	100K	13M	1.8	(RC as 1st stage) G_mC	0.9
[46]	2	4	CMOS 0.35	17.3	20K	5.12M	18	Active RC	2.8
[35]	5	1	CMOS 0.25	13.3	330K	21.07M	8	(RC as 1st stage) G_mC	1.2
[24]	2	3	CMOS 0.25	8.7	20M	320M	20	G_mC	1.2
[48]	5	1	CMOS 0.25	11.0	2M	150M	2.7	RC + GmC	0.3
[36]	4	1.5	CMOS 0.18	11.3	1.92M	153.6M	3.3	(RC as 1st stage) G_mC	0.3
[42]	2	4	CMOS 0.18	11.0	1M	48M	2.2	Active RC	0.5
[38]	2	1	CMOS 0.18	12.8	1.23M	2G	18	G_mC	1.0
[39]	2-2	4	CMOS 0.18	10.8	10M	160M	122	(RC as 1st stage) G_mC	3.3
[22]	4	1	CMOS 0.18	14.5	1M	64M	2	(RC as 1st stage) G_mC	0.0
[25]	3	4	CMOS 0.18	7.8-12.2	10-20M	100-200M	103	Active RC	11.6
[49]	3	4	CMOS 0.18	12.5	7.5M	240M	89	RC	1.0
[23]	4	4	CMOS 0.13	10.8	15M	300M	70	Active RC	1.3
[45]	3	4	CMOS 0.13	13.0	2M	104M	3	Active RC	0.1
[26]	3	4	CMOS 0.13	12.0	20M	640M	20	Active RC	0.1
[62]	2	1	CMOS 0.13	6.0	5M	160M	0.72	RC	1.1
[63]	2	2	CMOS 0.13	8.2	20M	640M	6	G_mC	0.49

Among all the designs in Table 2.4, [24] and [39] are the closest to the proposed implementation. The technologies used in [24] and [39] are CMOS 0.25 and CMOS 0.18, compared to CMOS 0.18 in this design. The bandwidths are 20MHz and 10MHz respectively, which are relatively close to the signal bandwidth 5MHz in this project. The sampling frequencies are 320MHz and 160MHz, while 200MHz is chosen in this project. Furthermore, both of them use G_mC as filter implementation.

Chapter 3 System Level Design and Simulation

As mentioned in the previous chapter, the synthesis of a CT DSM usually starts from design of a DT DSM which will then be transformed into a CT DSM afterwards. In this designed system, ultrasound signal was used as the input for simulations and the beamformed image was to be generated by employing the designed CT DSM in the system.

3.1 Discrete-Time Delta-Sigma Modulator Synthesis and Simulation

3.1.1 Optimum Modulator Order and Oversampling Ratio

In order to achieve an 8-bit resolution and to fulfill low power consumption requirement with 5MHz signal bandwidth, the OSR used should be as low as possible. Usually, lower OSR can be achieved by employing high order modulator once the quantizer resolution and the modulator architecture are fixed. However, as will be explained in this section, in the case of relatively low OSR (smaller than 32), high order modulator is not very efficient.

As given in Table 1.1 at the end of Chapter 1, the specified dynamic range is about 50dB or approximately 8-bit resolution. With 10dB margin in the system design to overcome the non-idealities from circuit elements, the required dynamic range is about 60dB, so the peak SNR will be around 57dB if 3dB overload loss is assumed. In [14], empirical peak SNR values are provided for single-bit modulators of different orders. It can be used to

determine the modulator order as an initial solution once the peak SNR is specified. For 57dB peak SNR, the OSRs for MOD2, MOD3 and MOD4 are 28, 20 and 16 respectively. For higher order modulators (5^{th} to 8^{th}), the OSR ranges from 12 to 14. Comparing the 2 ranges of OSR required, it can be seen that the reduced sampling frequency does not justify the additional hardware cost due to the increased order. Therefore, low order modulators (2^{nd} to 4^{th}) will be studied in terms of NTF frequency response, NTF in-band gain and dynamic range performance.

As shown in Figure 3.1, the NTF frequency responses for MOD2, MOD3 and MOD4 are plotted with out-of-band gain equals to 1.6. Although the Lee criterion states that a DSM is likely to be stable when the maximum gain of the NTF is smaller than 1.5, the value is somehow conservative for the modulators with relatively low order (MOD2, MOD3 and MOD4). The gain value 1.6 is chosen based on extensive simulations rather than the Lee criterion to make sure all the modulators are stable. In Figure 3.1, the NTF zeroes are not optimized resulting in DC zeroes for all the modulators.

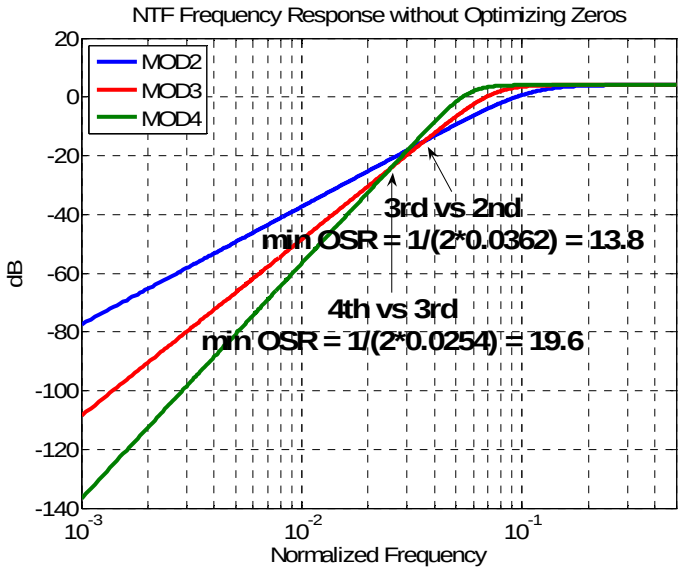

Figure 3.1 Low Order NTF Frequency Response without Optimized Zeroes.

To complete the analysis on optimum modulator order and OSR, NTFs with optimized zeroes for different order modulators are to be studied. Two cases are included here: (1) optimize all the zeroes (2) for even order modulators, put at least two zeroes at DC and optimize the rest. The results are shown in Figure 3.2 and Figure 3.3 respectively with OSR of 20. The NTF in-band gain and the dynamic range are summarized in Table 3.1. It can be seen that MOD3 has 10dB larger dynamic range than MOD2 when all the zeroes are optimized. In addition, even with the same OSR, MOD4 only shows 3dB better in terms of dynamic range with additional hardware and poorer stability.

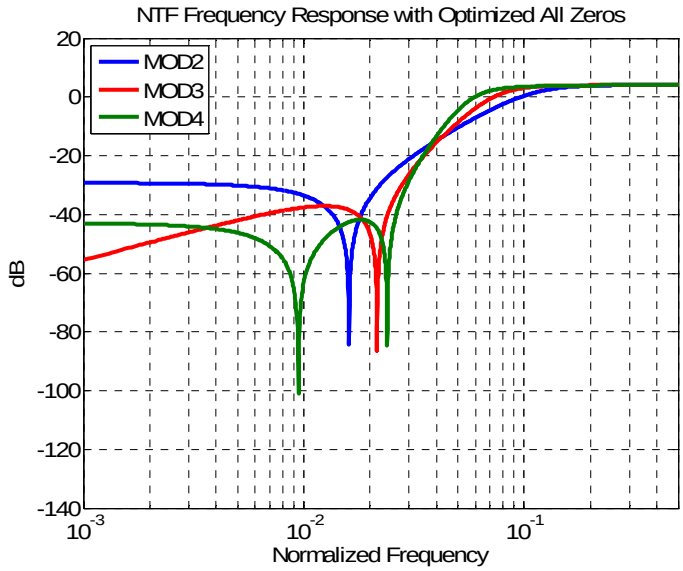

Figure 3.2 Low Order NTF Frequency Response with Optimized All Zeroes.

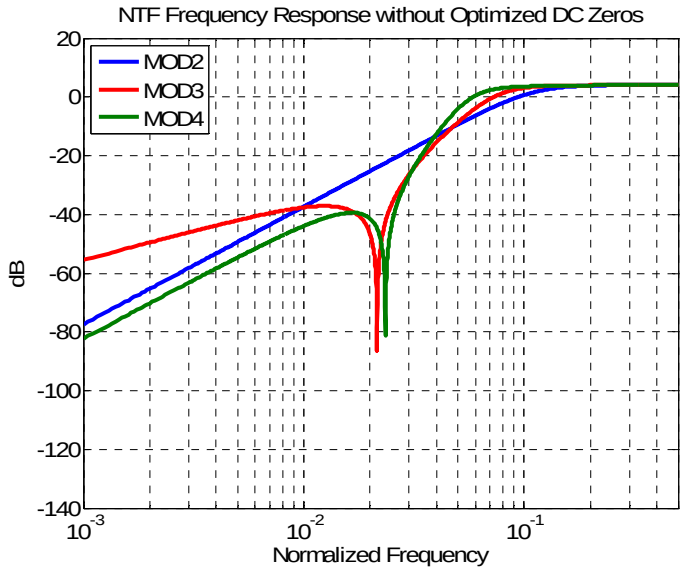

Figure 3.3 Low Order NTF Frequency Response without Optimized DC Zeroes for Even Order Modulators.

Table 3.1 NTF In-Band Gain and Dynamic Range Summary (OSR = 20).

	MOD2		MOD3		MOD4	
	NTF Gain	DR	NTF Gain	DR	NTF Gain	DR
No Opt	-24.8dB	52.5dB	-33.0dB	55.5dB	-34.2dB	56.0dB
Opt All	-31.9dB	44.5dB	-41.2dB	63.5dB	-47.4dB	66.5dB
Opt Partially	-24.8dB	52.5dB	-41.2dB	63.5dB	-45.4dB	66.0dB

In conclusion, to achieve 8-bit resolution with 10dB design margin, MOD3 with OSR equals to 20 is the optimum modulator in terms of dynamic range, hardware complexity and stability.

3.1.2 Noise Transfer Function Synthesis

Commonly used high pass filter types including Butterworth type, Chebyshev I type and Elliptic type can be employed as the NTF. As plotted in Figure 3.4 together with the NTF in-band gain, Chebyshev I and Elliptic types filters exhibit significant passband ripple which degrades modulator stability greatly [50]. Therefore, the Butterworth high pass filter is preferred due to its maximally flat amplitude within the passband. The NTF out-of-band gain is set to be 1.6 according to Lee criterion since third-order is not considered as very high order. Simulations in the time domain have been performed in order to ensure the modulator is stable with reasonable input amplitude. The locations of poles and zeroes of the synthesized NTF are plotted in Figure 3.5 and the synthesized transfer function using Butterworth type filter is:

$$NTF = \frac{(z-1)(z^2-1.985z+1)}{(z-0.3423)(z^2-1.805z+0.9059)} \tag{3.1}$$

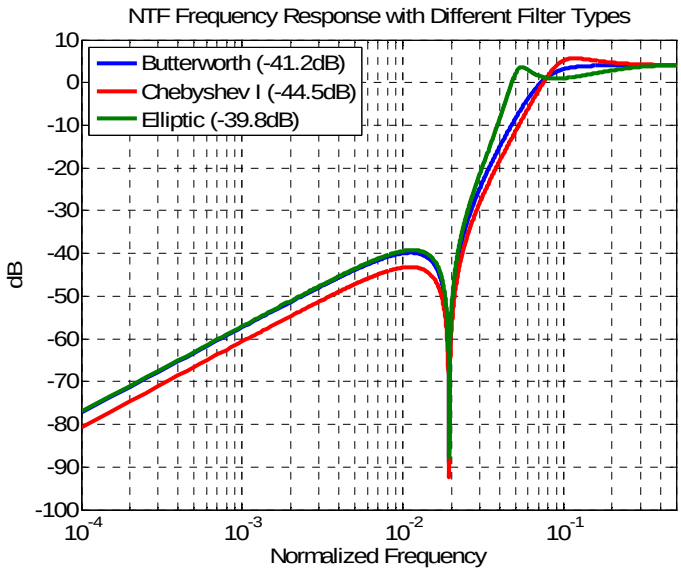

Figure 3.4 NTF Frequency Response with Different Filter Types.

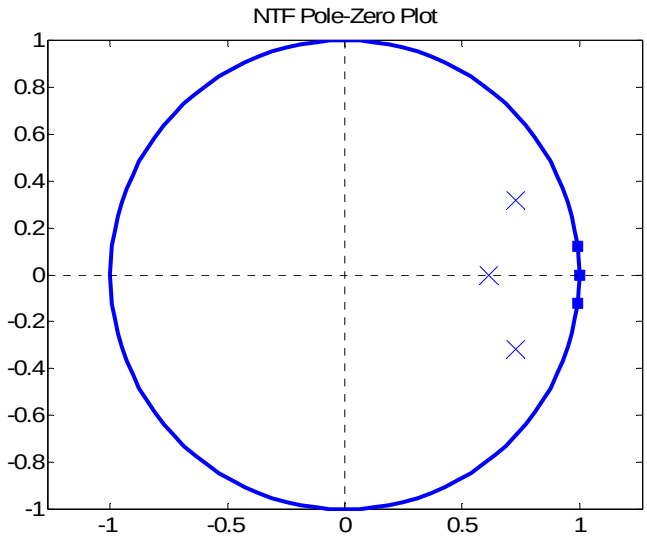

Figure 3.5 Synthesized NTF Pole and Zero Locations.

3.1.3 Time Domain Simulation and Power Spectral Density Estimation

Time domain simulation is often performed after the NTF is synthesized. Important parameters like PSD, dynamic range etc, can be calculated by running Fast Fourier transform (FFT) [28]. The number of FFT is chosen to be 2^{12} or 4096 for sufficient accuracy while limiting the simulation time, especially when transistor-level simulation is considered. The Hann window is used to shape the output data before running FFT to reduce the noise leakage. Moreover, in order to further reduce the signal leakage in FFT, the test signal frequency is chosen to be in an FFT bin:

$$f_{in} = n\frac{f_s}{4096} = \frac{n}{4096} \tag{3.2}$$

where the sampling frequency is normalized to one and n is chosen to be a prime number in order to reduce undesirable FFT harmonics in the spectrum. Here n is set to be 13.

In addition, with the specified OSR the signal bandwidth can be calculated as:

$$f_B = \frac{f_s}{2 \cdot OSR} = \frac{1}{40} = 0.025 \tag{3.3}$$

With the chosen n, the signal bandwidth is more than seven times higher than the test frequency, so harmonics up to seventh-order of the test signal will be included in-band. Consequently, the resultant SNR is in fact the signal-to-noise-and-distortion ratio (SNDR), which is in general lower than the SNR. This is quite important for transistor-

level realization since certain non-idealities especially nonlinearities of elements introduce harmonic distortions in-band and thus degrade the achievable resolution. Conversely, a test signal with frequency higher than half of the bandwidth will not introduce any harmonics in-band, thus resulting in only SNR instead.

As an example, with input amplitude equals to -12dB relative to the DAC feedback reference, the simulated input and output waveforms in the time domain are illustrated in Figure 3.6.

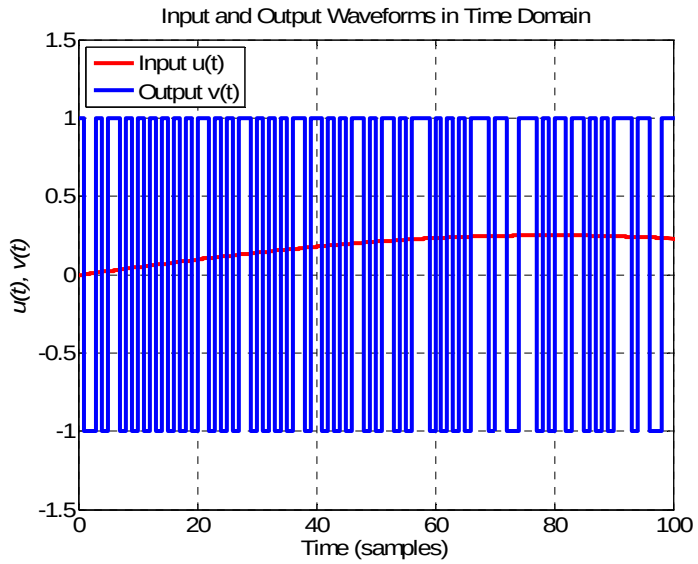

Figure 3.6 Input and Output Waveforms in the Time Domain.

From Figure 3.6, one can hardly tell any useful information from the time domain simulation. The time domain output is used to perform the FFT and the resultant PSD is shown in Figure 3.7. The SNR value can be calculated from Figure 3.7 by taking the ratio of the signal over the IBN. In this example, since the IBN is about -61.0dB and with the

signal equals to -12dB, the SNR is supposed to be 49dB instead of 50.7dB. This small discrepancy is due to the way of signal calculation for the Hann window. By using the Hann window, the bulk of the signal occupies three bins, which are the calculated signal bin and the two adjacent bins on its left and right. Nevertheless, this small discrepancy regarding the SNR calculation is usually not an issue, as unlike the single-tone signal power is concentrated in only a few bins, the quantization noise power is on average evenly distributed over all FFT bins. In other words, as the number of FFT doubles, the noise floor will drop 3dB but the total noise power will still remain the same. Thus, another parameter named noise bandwidth (NBW) has to be indicated on the spectrum at the same time [14], so the actual noise power of each bin is the product of the noise density and the NBW.

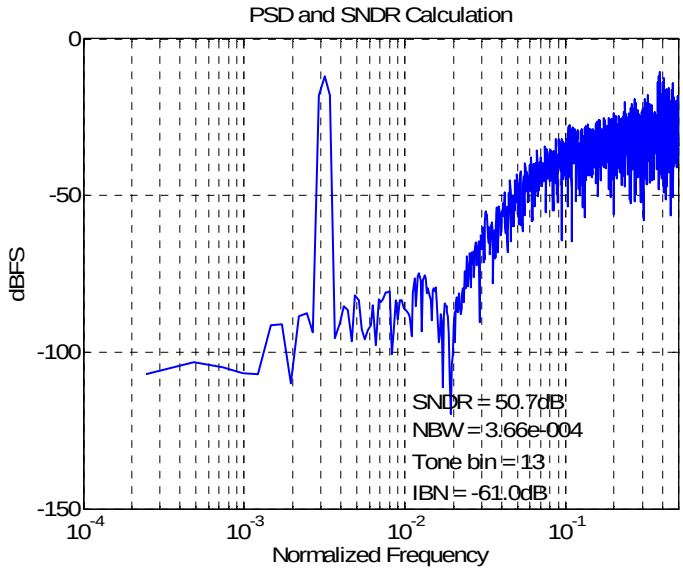

Figure 3.7 PSD and SNR Calculation.

3.1.4 Noise Transfer Function Realization and Dynamic Range Measurement

As discussed in Section 2.3.4, the feedforward type loop filter requires only one DAC and the linearity requirement of the integrator is more relaxed compared with that of the feedback type filter. Thus, a third-order CRFF type filter is used to realize the modulator, which is shown in Figure 3.8. The loop filter equations can be then set up as in Equation (3.4) and (3.5):

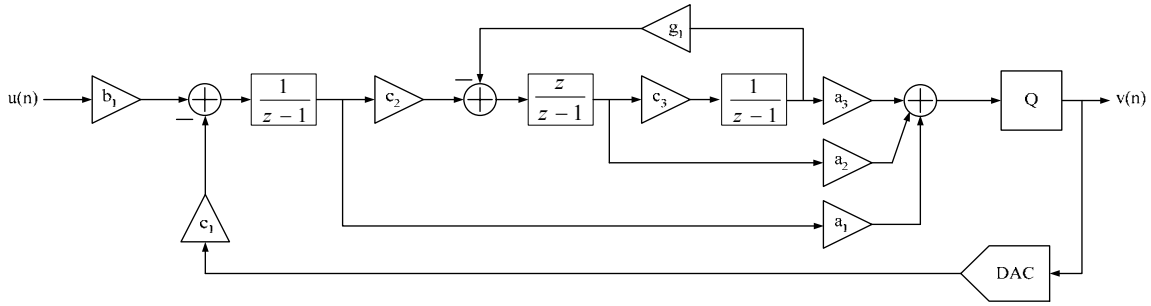

Figure 3.8 DT MOD3 with CRFF Loop Filter.

$$L_0(z) = b_1 \frac{(a_1 + a_2c_2))z^2 - \left[a_1(2 - c_3g_1) + a_2c_2 - a_3c_2c_3\right]z + a_1}{(z-1)\left[z^2 - (2 - c_3g_1)z + 1\right]} \tag{3.4}$$

$$L_1(z) = -c_1 \frac{(a_1 + a_2c_2)z^2 - \left[a_1(2 - c_3g_1) + a_2c_2 - a_3c_2c_3\right]z + a_1}{(z-1)\left[z^2 - (2 - c_3g_1)z + 1\right]} \tag{3.5}$$

The coefficients in Equation (3.5) can be determined with Equation (2.15) and Equation (3.1).

In Equation (3.4), b_1 is normally set to be equal to c_1 in order to obtain a flat STF. Therefore, the coefficients can be calculated as:

$$a_1 = 0.6123 \; a_2 = 0.3938 \; a_3 = 0.0590$$
$$b_1 = 1$$
$$c_1 = 1 \; c_2 = 1 \; c_3 = 1$$
$$g_1 = 0.0148$$

It should be noted that the above coefficients are unscaled, so the internal states of the modulator will occupy an unspecified range. In order to restrict the state range to a known and practical value, dynamic range scaling has to be performed. Since a CT solution is to be designed after all, the dynamic range scaling will be performed in the CT modulator. Nevertheless, the scaling does not affect the modulator performance in the system level simulation since the integrator outputs are not limited by saturation.

After the loop filter is realized, numerous SNR simulations with different input amplitudes are performed. The result is shown in Figure 3.9, where the MSA is -2.5dBFS and the dynamic range is approximately 63.5dB or 10-bit.

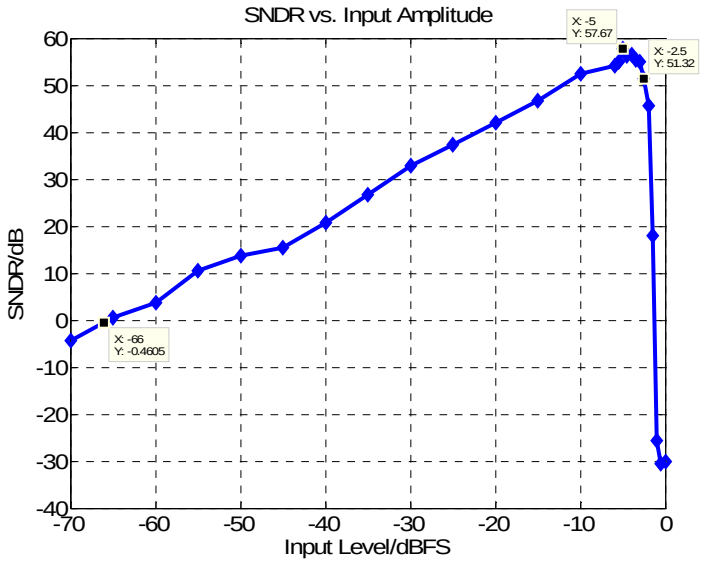

Figure 3.9 SNR vs. Input Amplitude.

3.2 Discrete-Time to Continuous-Time Transformation of Delta-Sigma Modulator

Before proceeding to DT-to-CT conversion, the CT MOD3 with feedforward topology is modified by including an extra half clock cycle delay [26] after the quantizer as shown in Figure 3.10. This delay relaxes the settling requirement of the quantizer and prevents any quantizer delay to affect the loop behavior. To compensate for the half clock cycle delay, an additional feedback path k is directly connected to the input of the quantizer. Therefore, the effect of the feedback path k needs to be taken into consideration in DT domain as in the method proposed in [26]. It should be noted that the coefficient k does not affect dynamic range scaling. Also, the duration of the delay can be chosen arbitrarily, but a longer delay needs to be compensated by using a larger feedback factor resulting in

higher power consumption. Thus, half clock cycle is selected since it is the smallest available delay.

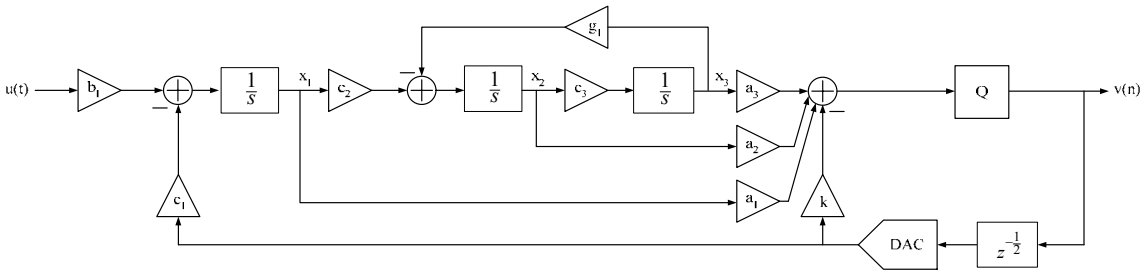

Figure 3.10 CT MOD3 with Feedforward Loop Filter.

Numerically, Equation (3.5) can be written as:

$$L_1(z) = \frac{-0.9161z^2 + 1.46z - 0.6123}{z^3 - 2.985z^2 + 2.985z - 1} \tag{3.6}$$

To have a half clock cycle delay, the equivalent transfer function with halved sampling time is derived as:

$$L_1\left(z^{\frac{1}{2}}\right) = \frac{-0.4166z + 0.7486z^{\frac{1}{2}} - 0.3406}{z^{\frac{3}{2}} - 2.996z + 2.996z^{\frac{1}{2}} - 1} \tag{3.7}$$

Divide both sides by half clock cycle delay ($z^{-1/2}$):

$$\begin{aligned} L_1\left(z^{\frac{1}{2}}\right)\cdot z^{\frac{1}{2}} &= \frac{-0.4166z+0.7486z^{\frac{1}{2}}-0.3406}{z^{\frac{3}{2}}-2.996z+2.996z^{\frac{1}{2}}-1}\cdot z^{\frac{1}{2}} \\ &= \frac{-0.4996z+0.9076z^{\frac{1}{2}}-0.4166}{z^{\frac{3}{2}}-2.996z+2.996z^{\frac{1}{2}}-1}-0.4166 \end{aligned} \tag{3.8}$$

Therefore, the new feedback coefficient also known as the auxiliary feedback coefficient k can be extracted:

$$k = 0.4166 \tag{3.9}$$

The new loop filter transfer function is the remaining part of Equation (3.8):

$$L_1\left(z^{\frac{1}{2}}\right) = \frac{-0.4996z+0.9076z^{\frac{1}{2}}-0.4166}{z^{\frac{3}{2}}-2.996z+2.996z^{\frac{1}{2}}-1} \tag{3.10}$$

From Equation (2.31) and Equation (3.10), the CT loop filter transfer function $L_1(s)$ for NRZ type DAC can be calculated using Matlab as:

$$L_1(s) = -\frac{0.9139s^2+0.3321s+0.0681}{s\left(s^2+0.0148\right)} \tag{3.11}$$

For CT MOD3 with feedforward loop filter without the auxiliary feedback and half clock cycle delay, the transfer function $L_1(s)$ can be represented as:

$$L_1(s) = -\frac{a_1c_1s^2 + a_2c_1c_2s + (a_1c_1c_3g_1 + a_3c_1c_2c_3)}{s(s^2 + c_3g_1)} \tag{3.12}$$

Moreover:

$$L_0(s) = \frac{a_1b_1s^2 + a_2b_1c_2s + (a_1b_1c_3g_1 + a_3b_1c_2c_3)}{s(s^2 + c_3g_1)} \tag{3.13}$$

Again, before dynamic scaling, coefficients c_1 to c_3 are set to be one and b_1 is set to be equal to c_1. By mapping Equation (3.12) to (3.11), the coefficients for the CT DSM can be calculated as:

$a_1 = 0.9139$ $a_2 = 0.3321$ $a_3 = 0.0546$
$b_1 = 1$
$c_1 = 1$ $c_2 = 1$ $c_3 = 1$
$g_1 = 0.0148$
$k = 0.4166$

The original coefficients for the DT DSM are repeated below for easy comparison. It can be seen that with coefficients *b*, *c* and *g* unchanged, the CT feedforward coefficients *a* are different from that of the DT DSM in order to maintain the equivalence. As mentioned previously, coefficient *k* is added to compensate the half clock cycle delay.

$a_1 = 0.6123\ a_2 = 0.3938\ a_3 = 0.0590$
$b_1 = 1$
$c_1 = 1\ c_2 = 1\ c_3 = 1$
$g_1 = 0.0148$

Internal states x_1, x_2 and x_3 are required to be scaled in order to make sure that the outputs of the integrators will not be clipped in transistor level realization. The saturation of integrators generates harmonics and degrades the SNR. As shown in Figure 3.11, the dynamic range scaling is performed by reducing all incoming branches by a factor k and by multiplying all outgoing branches by the same factor k to compensate the attenuation [14]. In this way, the outputs of the integrators are altered without affecting the loop filter characteristic. Here, the maximum value of all internal states is set to be 0.8FS.

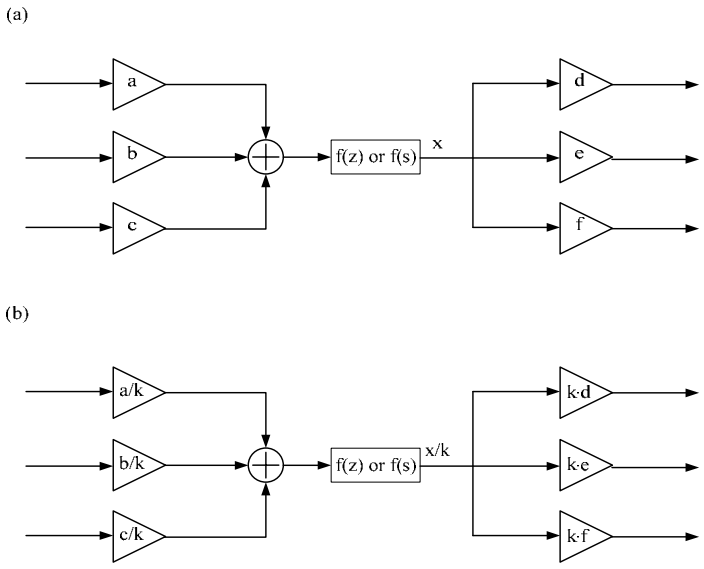

Figure 3.11 Internal States Scaling.

The internal states may not reach their maximum values when a single-tone sinusoidal signal is present at the input. However, in practice there may be other tones present at the same time. In [14], the worst case, which is the maximum values internal states are reached before the modulator becomes unstable, can be excited by employing a slowly raised DC input with certain level of random noise. The random noise has a mean of zero and a standard deviation of 1%. The test signal in the time domain is shown in Figure 3.12.

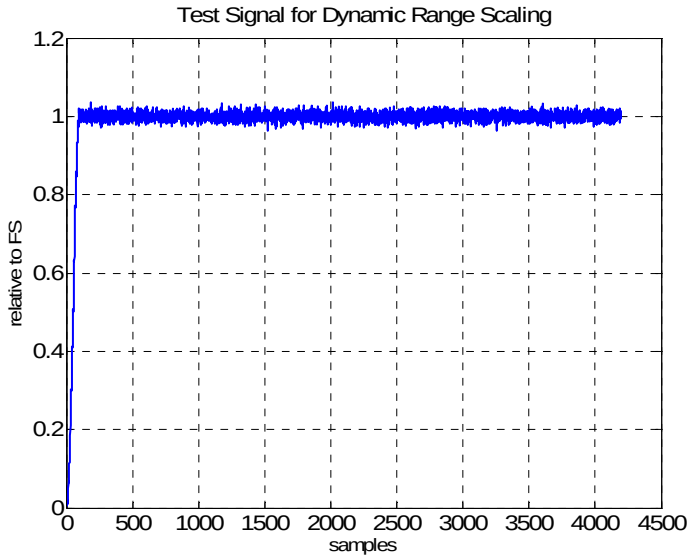

Figure 3.12 Test Signal for Dynamic Range Scaling.

The resultant scaled coefficients are:

$a_1 = 3.0660$ $a_2 = 3.6782$ $a_3 = 4.0378$
$b_1 = 0.2980$
$c_1 = 0.2980$ $c_2 = 0.3029$ $c_3 = 0.1497$
$g_1 = 0.0989$
$k = 0.4166$

The maximum values of internal states against different input levels are plotted in Figure 3.13. It can be seen that the maximum states are not reached until the modulator is unstable.

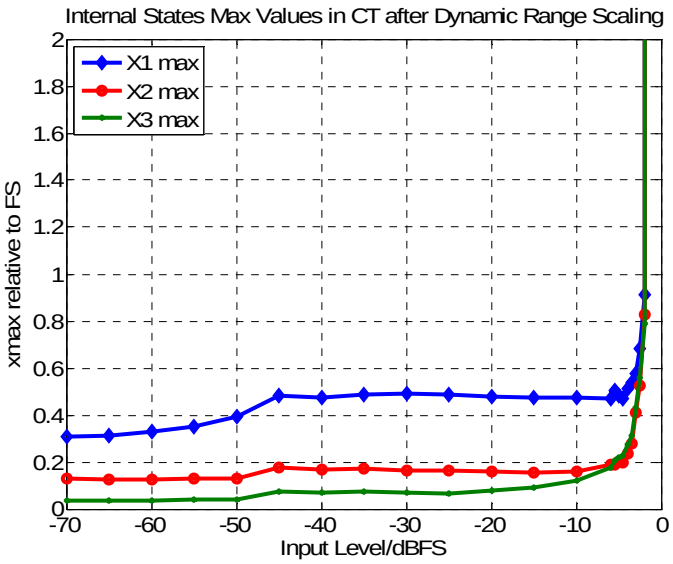

Figure 3.13 Internal States Maximum Values Plot after Scaling.

3.3 Continuous-Time Delta-Sigma Modulator Simulation

3.3.1 Comparison between Discrete-Time and Continuous-Time Modulators

The designed CT DSM is simulated and compared with the original DT DSM and the results are shown in Figure 3.14 and Figure 3.15. It can be observed that the performance of the CT DSM is very close to that of the DT DSM. The small discrepancy between the two modulators is due to the difference between the STF of the DT DSM and that of the CT DSM, which provides inherent anti-aliasing protection in the CT DSM.

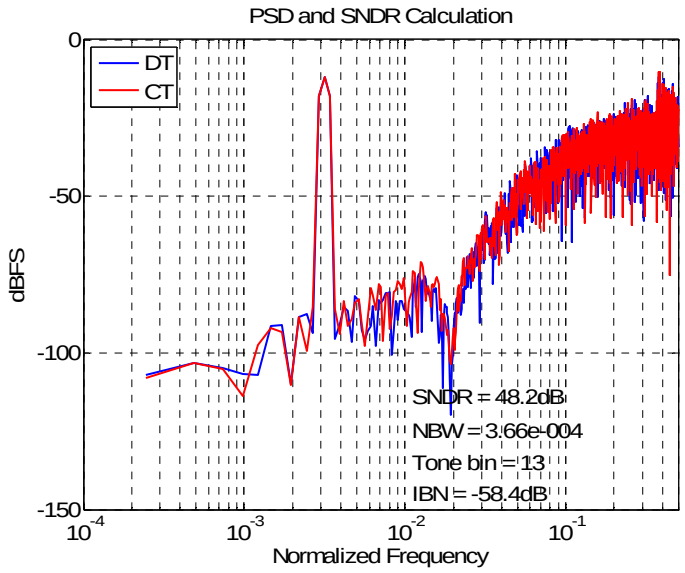

Figure 3.14 PSD Comparison.

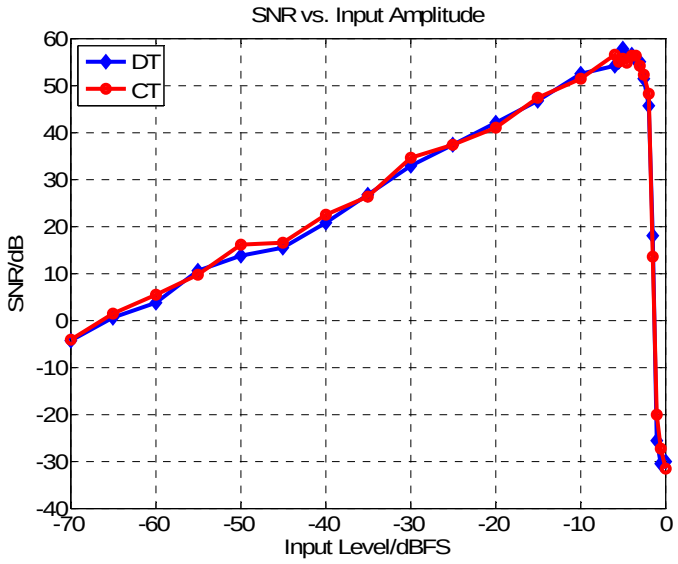

Figure 3.15 SNR vs. Input Amplitude Comparison.

3.3.2 Inherent Anti-Aliasing Filter in Signal Transfer Function

As mentioned previously, CT DSMs have inherent AAF. Intuitively, it can be understood as that the input signal is filtered by the CT loop filter before it is sampled at the quantizer, so that the potential aliasing signals can be removed or attenuated by the loop filter. In a CT DSM, the input signal is integrated periodically, which is referred to as boxcar integration, before being sampled [33]. The boxcar integration can be expressed by a convolution of the input signal with a rectangular pulse in the time domain, or as a multiplication of the input spectrum with a sinc function which has infinite attenuation at f_s and relatively large (depending on modulator order) attenuation around f_s [15, 16].

In a DT DSM, the modulator output can be expressed as a combination of the filtered input signal and the filtered quantization noise as in Equation (2.16), where all the

quantities are in DT domain. In a CT DSM, the output and the quantization noise are in DT domain while the input signal is in CT domain. As a result, the NTF remains in DT domain but the STF has to be a mixture of DT and CT transfer functions [14]. Thus, instead of the DT relationship $STF = L_0(Z)NTF(Z)$, in a CT DSM [14]:

$$STF = L_0(s)\,NTF(z) \tag{3.14}$$

Then the CT STF can be calculated as shown below:

$$STF = \frac{\left(0.9139s^2 + 0.3321s + 0.0681\right)}{s\left(s^2 + 0.0148\right)} \cdot \frac{(z-1)\left(z^2 - 1.985z + 1\right)}{(z-0.6142)\left(z^2 - 1.455z + 0.6312\right)} \tag{3.15}$$

The frequency response against the normalized frequency is plotted in Figure 3.16. As expected, the STF shows anti-aliasing protection near multiples of the sampling frequency. The smallest suppression is still 50dB at $0.975f_s$, which will be aliased back to the edge of the passband. In addition, the STF exhibits 7.2dB peaking out of the passband. As mentioned previously, this is also the main drawback of feedforward loop filter topology. In a typical ultrasound application environment, the out-of-band noise is relatively small and therefore the out-of-band gain of the feedforward loop filter will not affect the system performance. The modulator with -6dB input and an aliasing signal which is at frequency (f_s-f_B) is simulated and the PSD is plotted in Figure 3.17. Clearly, the folded aliasing signal is attenuated by about 50dB

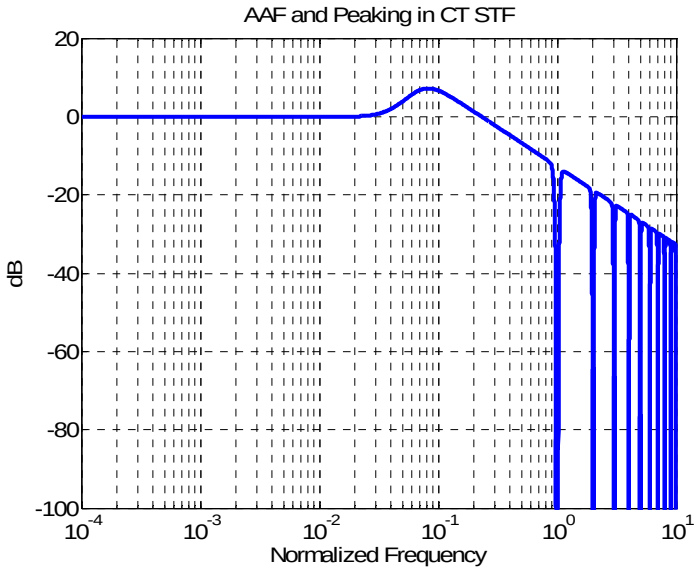

Figure 3.16 AAF and Peaking in CT STF.

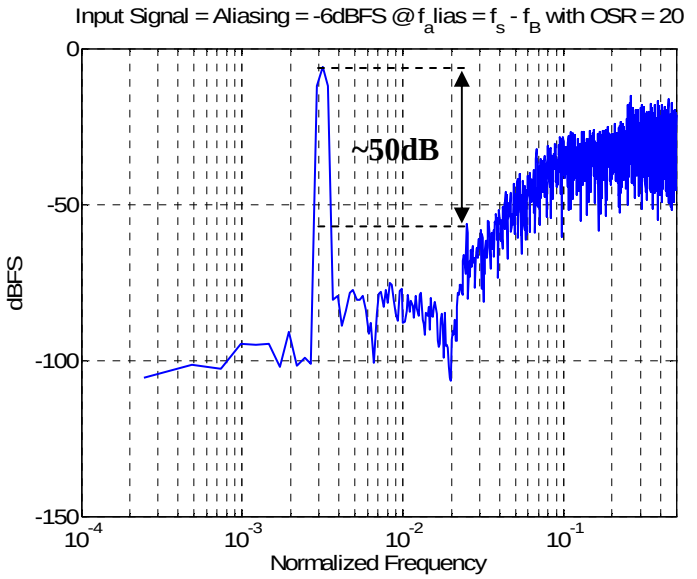

Figure 3.17 PSD of the Designed CT DSM with Inherent AAF.

3.3.3 Non-Idealities Simulations

Basically, a CT DSM consists of three major building blocks: a CT loop filter, a clocked quantizer (low resolution ADC) and a feedback DAC. Non-idealities in CT DSM are mainly from these three blocks while the input stage of the loop filter and the outmost DAC are most critical since any non-idealities from them such as noise and distortion are not shaped at all. In general, both of them are required to be as accurate as the whole system. On the other hand, any errors introduced by the remaining stages of the loop filter are suppressed by at least first-order noise shaping. Also, any non-idealities of the quantizer are shaped in the same way as the quantization noise being suppressed. In this section, non-idealities from the most critical blocks will be briefly covered and simulated, including excess loop delay, clock jitter, finite integrator gain and nonlinear transconductor.

In order to study the effect of non-idealities from DAC, two commonly used rectangular DAC pulses are introduced first: non-return-to-zero (NRZ) and return-to-zero (RZ). Other types which are not rectangular based will not be discussed in this report. As shown in Figure 3.18, NRZ DAC pulse remains non-zero in the whole sampling period while RZ DAC pulse is zero during certain portion of the sampling period depending on two coefficients α and β. Normally, α is set to be 0 and β is set to be 0.5. RZ DAC is preferred when unequal DAC pulse rise and fall time and excess loop delay are considered, while NRZ DAC is superior in terms of clock jitter insensitivity.

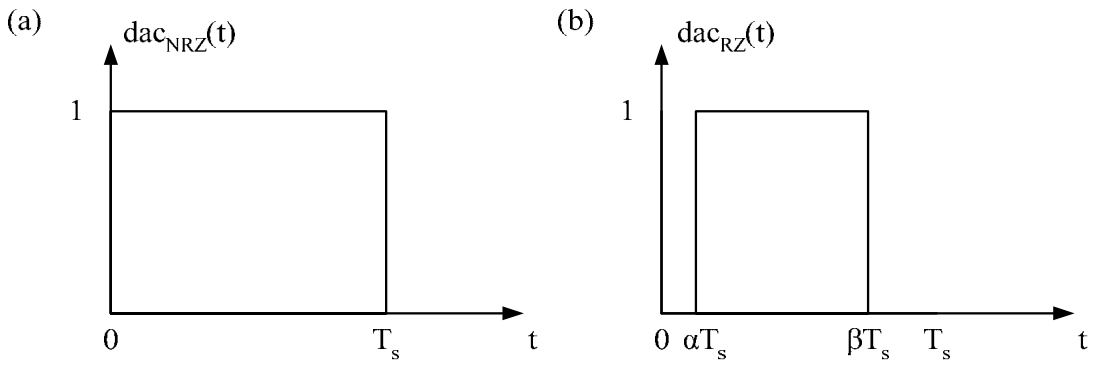

Figure 3.18 DAC Pulse Shape in One Sampling Period (a) NRZ (b) RZ.

3.3.3.1 Excess Loop Delay Simulation

In practice, there exists a non-zero delay between the quantizer clock edge and the DAC pulse [15]. This delay is called excess loop delay or loop delay in short. Basically, it is due to non-zero transistor switching time. Most of the time, the effect of this delay can be classified into two categories based on different DAC pulses. For RZ DAC with excess loop delay equals to t_d, as long as the pulse stays within one clock period, i.e. β is smaller than one, only coefficient mismatch is expected. Thus, the quantization noise may rise and the MSA may drop, but the order of the loop filter remains unchanged [16], resulting in less degradation.

For NRZ DAC (and for RZ DAC with t_d greater than half sampling period), as shown in Figure 3.19, any excess loop delay will shift a part of the DAC pulse into the next clock cycle. It has been found that the pulse shift at the next clock cycle increases the order of the modulator, thus the MSA will be reduced and the noise shaping performance will be degraded [15].

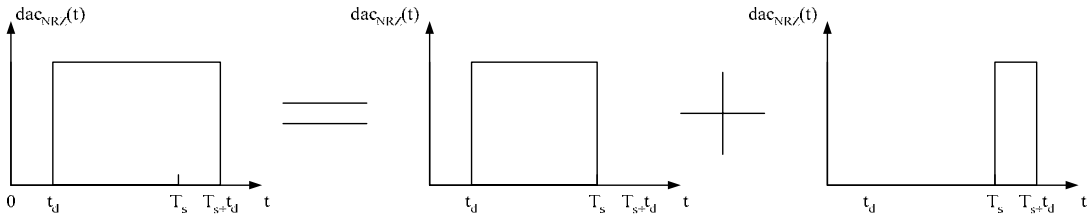

Figure 3.19 Excess Loop Delay Effect in NRZ DAC Pulse.

Excess loop delay is simulated by introducing delay in the feedback path and observing the change of the dynamic range and the peak SNR input amplitude. As shown in Figure 3.20, both the dynamic range and the amplitude drop as the loop delay increases. When the loop delay exceeds 40% of the clock period, the modulator becomes totally unstable.

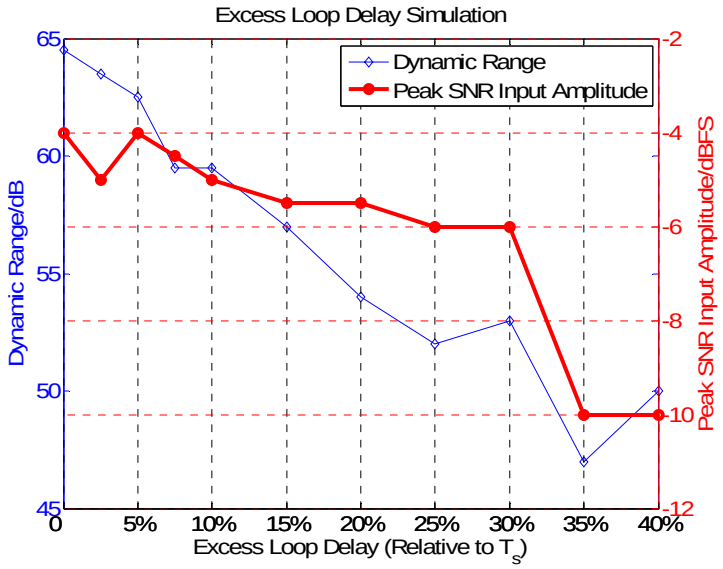

Figure 3.20 Excess Loop Delay Simulation.

3.3.3.2 Clock Jitter Simulation

One of the major disadvantages of CT DSMs is their sensitivity to clock jitter, which is the statistical variation of the sampling frequency of the clock. Clock jitter affects the sampled quantizer and the feedback DAC. Again, any error due to jitter in the sampled quantizer will be shaped by the loop filter and very often it can be neglected in practice [16]. However, in the DAC any error due to jitter will be integrated over time and the resulting increased noise will be input-referred directly. The variation of the feedback pulse length modulates the amount of feedback charge and the resulting error adds directly to the modulator input through the outmost DAC.

Typically, NRZ DAC has 4.6dB in terms of SNR better jitter performance compared to RZ DAC [15, 16]. This 4.6dB or almost 0.8-bit advantage makes NRZ DAC superior to RZ DAC in many applications, regardless of the fact that RZ DAC is less affected by excess loop delay. In this project, NRZ DAC is chosen for the benefit of the 0.8-bit

Jitter sensitivity of the designed CT DSM is simulated by varying the standard deviation of the clock jitter. If jitter is modeled in time, the required time step has to be smaller than the smallest clock jitter. Since jitter is random, the time step can be impractically small and therefore the simulation time can be extremely long. A fast simulation method in [51] is employed here in order to reduce the simulation time. In this method, the uncertainties of the clock edges are transformed into uncertainties of the pulse area which can be easily controlled by the feedback level. From Figure 3.21, it can be seen that the modulator is

not very sensitive to jitter when the standard deviation is below 10^{-3}. The measured dynamic ranges for different jitter values are summarized in Table 3.2.

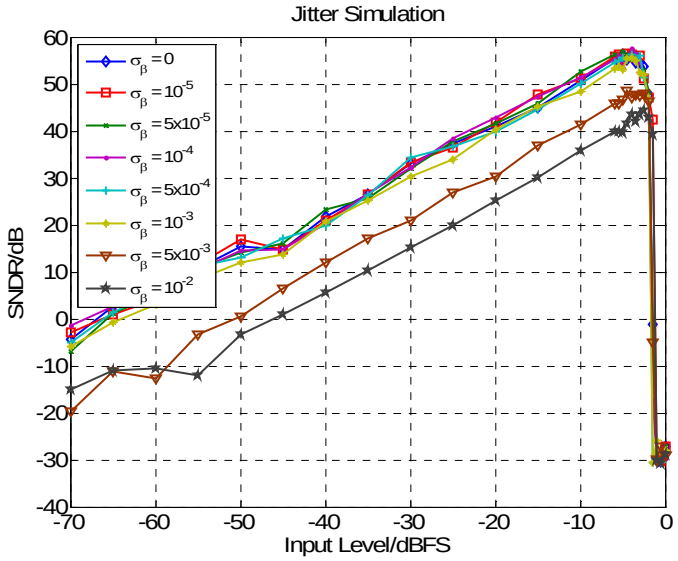

Figure 3.21 Jitter Simulation.

Table 3.2 Dynamic Range vs. Jitter.

Standard Deviation σ_β	0	10^{-5}	$5x10^{-5}$	10^{-4}	$5x10^{-4}$	10^{-3}	$5x10^{-3}$	10^{-2}
Dynamic Range	64.5dB	63.5dB	63.5dB	63.5dB	63.5dB	61.5dB	49.0dB	44.5dB

3.3.3.3 Finite Integrator Gain Simulation

The single-ended models for G_mC and active RC integrators with finite output resistance and finite opamp gain respectively are shown in Figure 3.22.

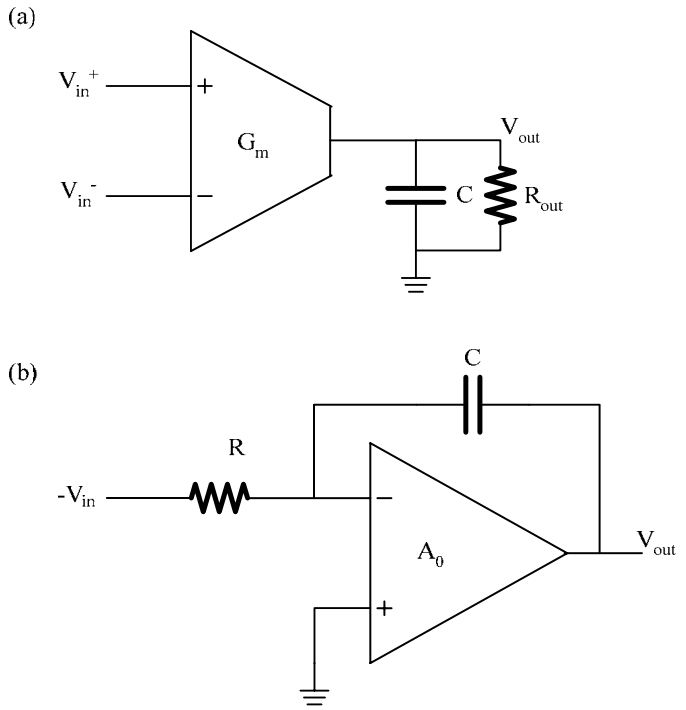

Figure 3.22 (a) G_mC Integrator with Finite Output Resistance (b) Active RC Integrator with Finite DC Gain.

It can be calculated for G_mC integrator:

$$\frac{V_{out}}{V_{in}} = G_m \cdot \left(R_{out} // C\right) = \frac{G_m R_{out}}{1 + sRC} = \frac{1}{\frac{1}{A_0} + \frac{sC}{G_m}} \tag{3.16}$$

where $A_0 = G_m R_{out}$ is the DC gain of the transconductor.

Also for active RC integrator:

$$\frac{V_{out}}{V_{in}} = \frac{1}{\frac{1}{A_0} + sRC\left(1 + \frac{1}{A_0}\right)} \approx \frac{1}{\frac{1}{A_0} + sRC} \tag{3.17}$$

where A_0 is the DC gain of the opamp.

By comparing Equation (3.16) and (3.17), it can be shown that the finite transconductor output resistance in G_mC integrator has similar effect as that of the finite gain of the opamp in active RC integrator. This is often referred as leaky integration and the noise floor is raised due to this non-ideality. In [14] and [16], it has been found that in opamp case, the DC gain of the amplifier should be in the range of OSR or more precisely A_0 should be at least greater than the OSR. Therefore, for G_mC integrator the output resistance is required to be:

$$R_{out} \geq \frac{OSR}{G_m} \tag{3.18}$$

The finite integrator gain can be modeled in Equation (3.16). The IBN with -6.0dB input amplitude is used to quantify the effect of finite integrator gain. From Figure 3.23, where Av1 to Av3 represent the DC gain of the first to the third integrators respectively, the minimum required DC gain 30dB for all the three integrators is quite close with that predicted by Equation (3.18), i.e. the minimum gain equals to the OSR value (20V/V or 26dB).

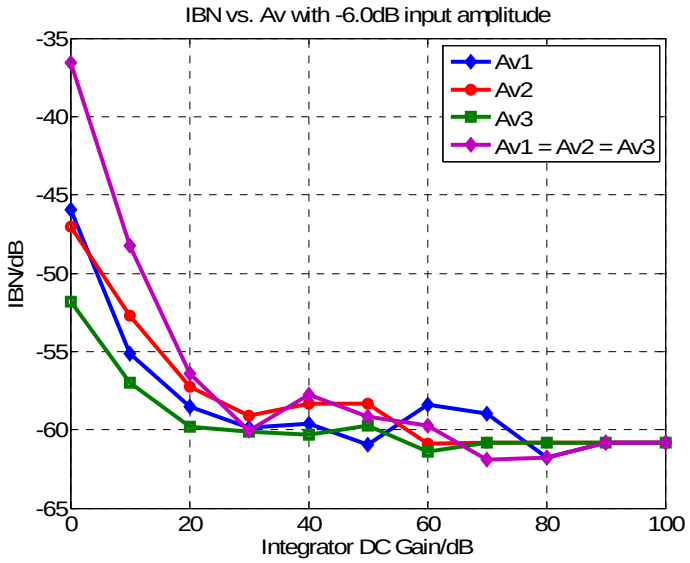

Figure 3.23 Finite Integrator Gain Simulation.

3.3.3.4 Nonlinear Transconductance Simulation

Another error source from the transconductor is the variation of the transconductance with respect to the input. The nonlinearity of the first transconductor, which is used as the voltage-to-current converter, adds directly to the input signal without any shaping and it contributes the main portion of harmonic distortion, or even intermodulation distortion if more than one tone is applied at input [52]. Usually the linearity of the first integrator is required to meet that of the overall modulator. The requirements of other succeeding stages are much more relaxed due to the noise shaping of the loop filter. Unlike the active RC integrator implementation, the G_mC integrator is an open loop system and thus it is generally less linear than the active RC integrator with feedback [47]. Therefore, the design of the first transconductor is one of the most critical tasks in terms of linearity and power consumption in the overall system.

There are several ways, including harmonic distortion, 1-dB compression, intermodulation distortion etc, to model nonlinearities. Among all of them, third-order intermodulation distortion (IM3) is often preferred [52, 53] for higher accuracy. Here, IM3 with respect to carrier will be used to quantify the effect of nonlinear transconductance in terms of the IBN. There are seven transconductors in the CT DSM and a general differential third-order system is used to model the transconductance in every block. The transfer function can be written as:

$$I = \left(k_1 V + k_2 V^2 + k_3 V^3\right) G_m \tag{3.19}$$

where G_m is the nominal transconductance. Here, k_1 is set to be one and k_2 is set to be zero in a fully differential system. In a weak nonlinear system, k_3 is usually negative, e.g., in a typical transconductor. As a result, IM3 in dB can be approximated as [54]:

$$IM3 \approx 20\log\left(\frac{3}{16}|k_3|A^2\right) = 20\log|k_3| - 26.54dB \tag{3.20}$$

where A is the peak input amplitude and it is set to be -6dB with respect to feedback level in the equation. Therefore, different IM3 values can be represented by k_3 and the result is plotted in Figure 3.24. It can be seen that the first transconductor, which is used to convert the input voltage to current, has the most stringent requirement on linearity. The IBN starts to degrade when IM3 equals to -50dBc. The linearity requirement on the other transconductor blocks is relatively more relaxed.

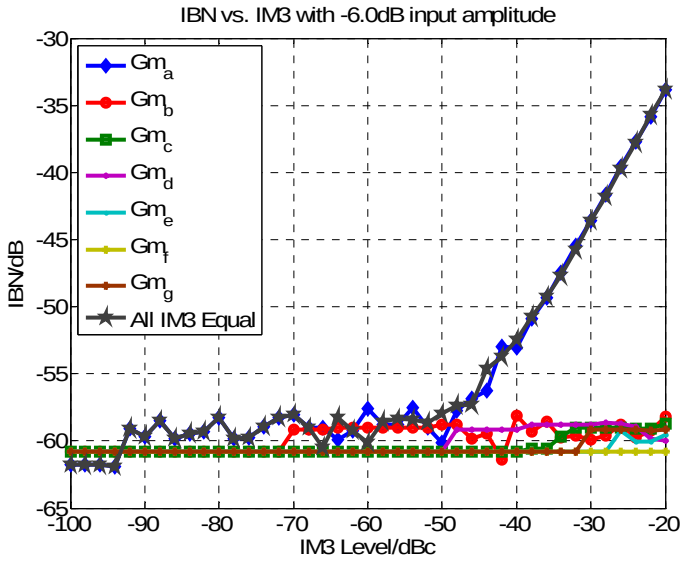

Figure 3.24 IM3 Simulation.

3.4 Ultrasound Signal Simulation [55]

The simplified structure of a delta-sigma beamformer with 32 receive channels is shown in Figure 3.25. The inputs of the beamformer receive ultrasound echoes and the pre-amplifiers amplify the echoes before they are converted into digital form by the DSMs. The digital outputs from the DSMs are then stored in delay resisters which are either shift registers or memories. Delay control signals select samples through multiplexers from the delay registers to the summer. A decimation filter is used to reconstruct the signal of the summed output.

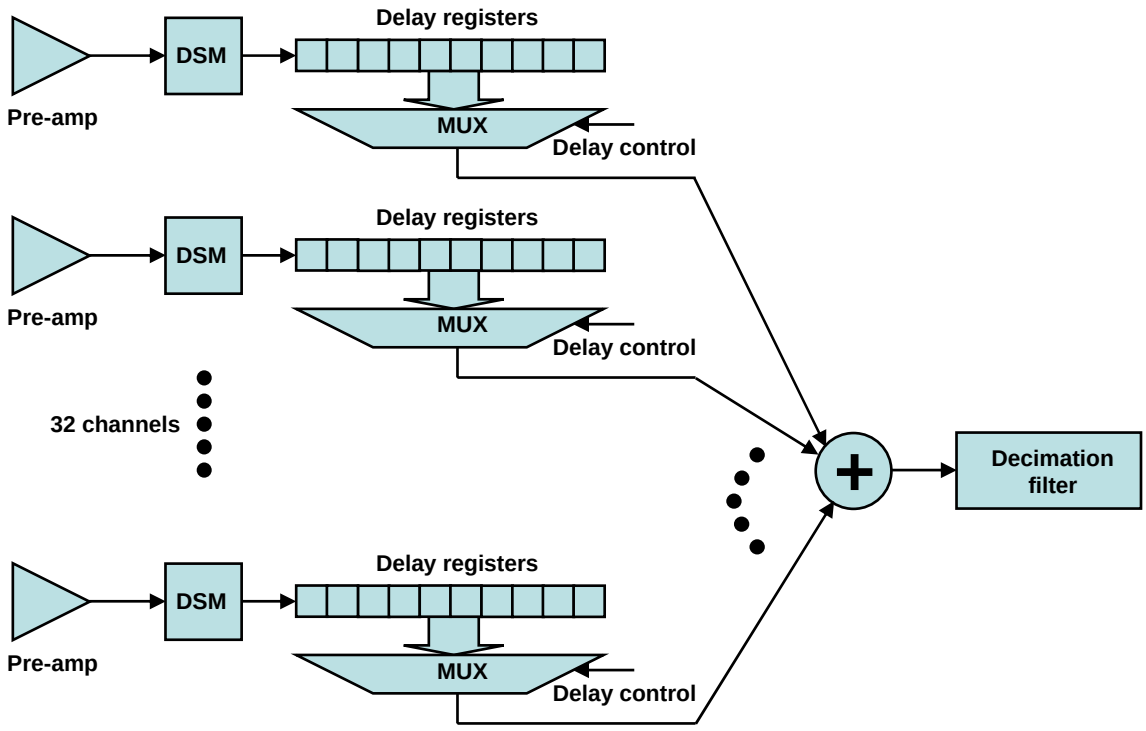

Figure 3.25 Digital Beamformer Block Diagram.

The performance of the delta-sigma receive beamformer was simulated after the incorporation of the designed CT DSM with the insert zero method [3]. The block diagram of the simulation setup is shown in Figure 3.26. A 128-element linear transducer array is used to convert ultrasound signal to electrical signal and vice versa. The transducer can be configured to both transmit and receive signals. In transmitting mode, 32 transducer elements are fired at the same time and a scanline is formed It is then shifted by one element at a time to scan over the area covered by the transducer. Therefore, 97 scanlines can be generated by the 128-element transducer. A multiplexer/demultiplexer is used to select signals between the transducer and the 32-channel beamformer which employs the designed CT MOD3

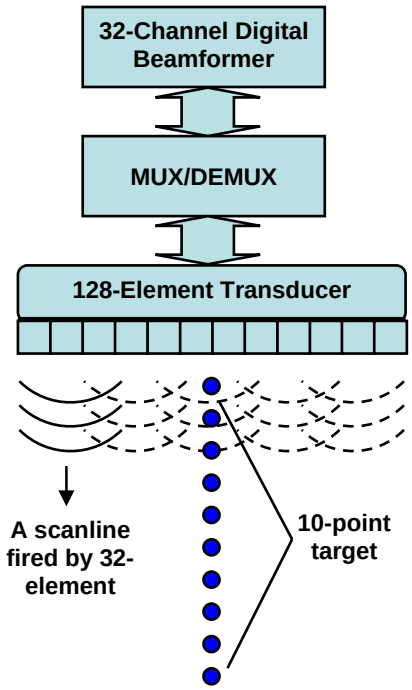

Figure 3.26 Beamforming Simulation Setup.

The simulation was performed using a point phantom data generated by Field II program [56]. The data are the ultrasound echoes, reflected from 10-point target lining 10mm apart along the central scanline, and received by the transducer With a sampling rate of 200MHz, the designed DSM was used to digitize the 3.5MHz, 0.6 fractional bandwidth ultrasound signal. As an example shown in Figure 3.27, the beamformer is able to produce a proper image after beamforming with distinct 10 point targets.

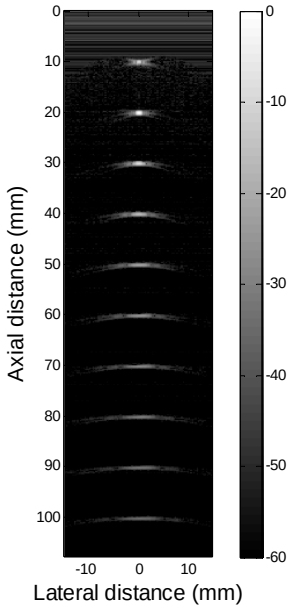

Figure 3.27 Beamforming Image Generated by the Designed CT MOD3.

3.5 System Level Design of A Reconfigurable Continuous-Time Delta-Sigma Modulator for Dual-Mode Ultrasonic Application [57]

In the continuous-wave (CW) Doppler operation, the dynamic range of the signal per channel with a 200kHz bandwidth is about 110dB or approximately 18-bit. As a result, conventional ultrasound machine uses a separate analog beamformer followed by a very accurate baseband ADC. In this way, signals from different channels can be summed and down-converted in the analog domain and the dynamic range requirement can be reduced for the baseband ADC. However, the analog beamformer is more sensitive to the circuit noise and more difficult to be programmed. In addition, the relatively low resolution

ADCs for B-mode cannot be reused in the CW Doppler mode, resulting in an increase of hardware complexity.

Here, a reconfigurable CT DSM, which can be used in both B-mode and CW Doppler mode, is proposed. In B-mode operation, system simulation has shown that a 3rd-order low-pass DSM with an oversampling ratio (OSR) of 20 (i.e., a sampling frequency of 200MHz) is the optimum combination for achieving the required 8-bit resolution. By utilizing building blocks in the low-pass modulator, a 4th-order bandpass DSM with an OSR of 500 can then be designed by adding three more transconductors and one more integration capacitor. A resolution of 18.8-bit can be achieved for the CW Doppler signal centered at 3.5MHz with a bandwidth of 200kHz. By sharing most of the blocks in different operating modes, power consumption and chip area can be reduced.

The bandpass DSM is reconfigured based on the available low-pass DSM structure. Figure 3.28 and Table 3.3 are repeated here for easy reference.

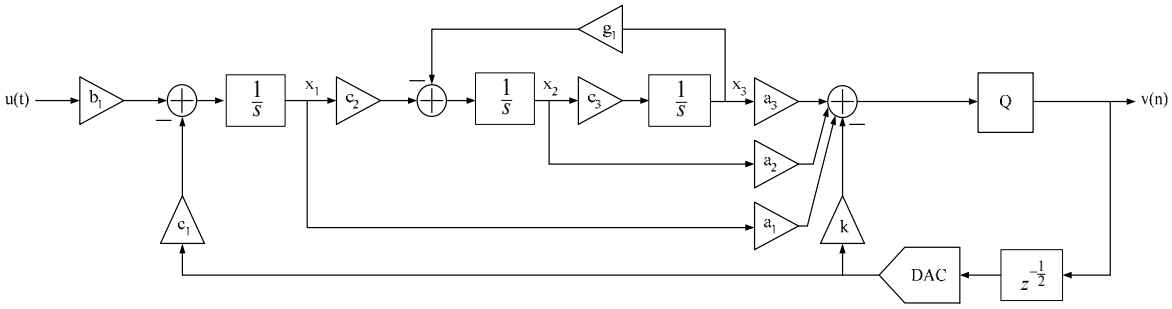

Figure 3.28 3rd-order Low-pass DSM in B-Mode.

Table 3.3 Low-pass DSM Coefficient.

a_1	3.0660	b_1	0.2980	c_1	0.2980	g_1	0.0989	k	0.4166
a_2	3.6782			c_2	0.3029				
a_3	4.0378			c_3	0.1497				

A beamformer employing a bandpass DSM in the CW Doppler mode has two main advantages over one with a baseband Nyquist ADC or a low-pass DSM: elimination of down conversion operations and exclusion of DC offset as well as low frequency flicker noise. The bandpass DSM was designed from the low-pass modulator so that all the blocks can be reused. A DT 4^{th}-order bandpass loop filter with two pairs of optimized NTF zeroes was synthesized first. The loop filter $L_1(z)$ which is the transfer function from the modulator output to the quantizer input can be expressed as:

$$L_1(z) = \frac{-0.9275z^3 + 2.366z^2 - 2.06z + 0.6094}{z^4 - 3.976z^3 + 5.952z^2 - 3.976z + 1} \tag{3.21}$$

From Equation (3.21), the CT form of the loop filter can be derived using impulse-invariant transformation. Again, the auxiliary DAC coefficient can be calculated first and then removed from the loop filter expression to simplify the derivation. The new k is calculated to be 0.4193 which is quite close to the previous one 0.4166. Thus, the auxiliary DAC in the low-pass modulator can provide almost the same function with very slight mismatch from the theoretical value. The new loop filter without k can be derived as:

$$L_1(s)=\frac{-0.9244s^3-0.3552s^2-0.09813s-0.01211}{\left(s^2+0.01169\right)\cdot\left(s^2+0.01249\right)} \tag{3.22}$$

Based on the low-pass modulator structure, a 4th-order bandpass feedforward DSM can be constructed as shown in Figure 3.29. Compared with Figure 3.28, three transconductors (b_2, g_2 and a_4) and one integration capacitor ($1/s$) need to be added. The location of the first feedback path also needs to be shifted. The loop filter transfer function of Figure 3.29 can be expressed as in Equation (3.23). In addition, Equation (3.24) is derived by replacing the numerical coefficients which are from the previous low-pass modulator.

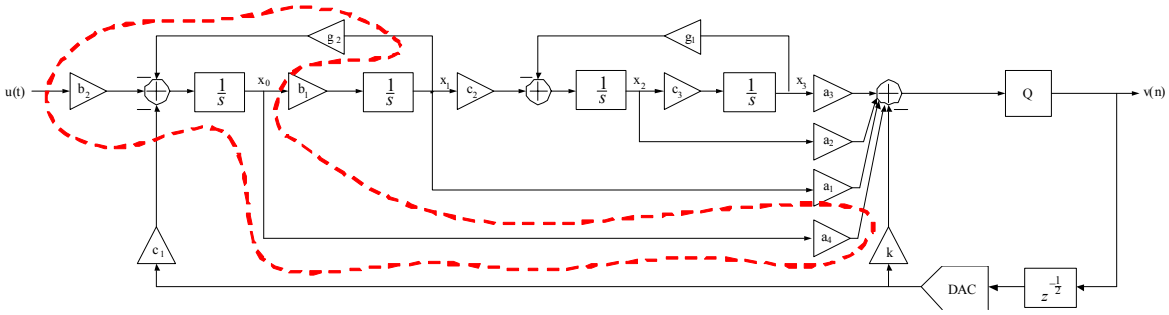

Figure 3.29 4th-order Bandpass DSM in CW Doppler Mode.

$$L_1(s)=\frac{-c_1\left[a_4s^3+a_1b_1s^2+\left(a_2b_1c_2+a_4c_3g_1\right)s+b_1\left(a_1c_3g_1+a_3c_2c_3\right)\right]}{\left(s^2+b_1g_2\right)\left(s^2+c_3g_1\right)} \tag{3.23}$$

$$L_1(s)=\frac{-0.298a_4s^3-0.2723s^2-0.298\cdot\left(0.3320+0.0148a_4\right)\cdot s-0.0203}{\left(s^2+0.298g_2\right)\cdot\left(s^2+0.0148\right)} \tag{3.24}$$

Apparently, there are two pairs of poles in $L_1(s)$, which are also the zeroes of the NTF. Among the two, one pair is fixed at $s = \pm 0.1217\,j$ and the other pair can be tuned to the desired value through g_2. Since the zeroes of the NTF are only to optimize the noise shaping and if the locations of the fixed zeroes are sufficiently close to the desired ones, the performance of the modulator is expected to be only slightly affected. On the other hand, the numerator of $L_1(s)$ determines the pole locations of the NTF thus it directly affects the stability of the modulator. Consequently, the numerator of Equation (3.24) has to be made as close as possible to that of Equation (3.22). It can be seen that it is impossible to map the numerator of Equation (3.24) to that of Equation (3.22) exactly because a_4 is the only degree of freedom in Equation (3.24). One way of introducing another degree of freedom is to include an additional feedback path. However, this brings in one more DAC block, resulting in increased hardware complexity as well as power consumption.

With only the coefficients of s^3 being equal in Equation (3.22) and Equation (3.24) which are controlled by a_4, the resultant modulator was unstable. As shown in Figure 3.30, the corresponding NTF (it is in DT form since both its input and output are DT quantities) has a maximum out-of-band peaking of 11.4dB, making the modulator unstable even at very small input magnitude.

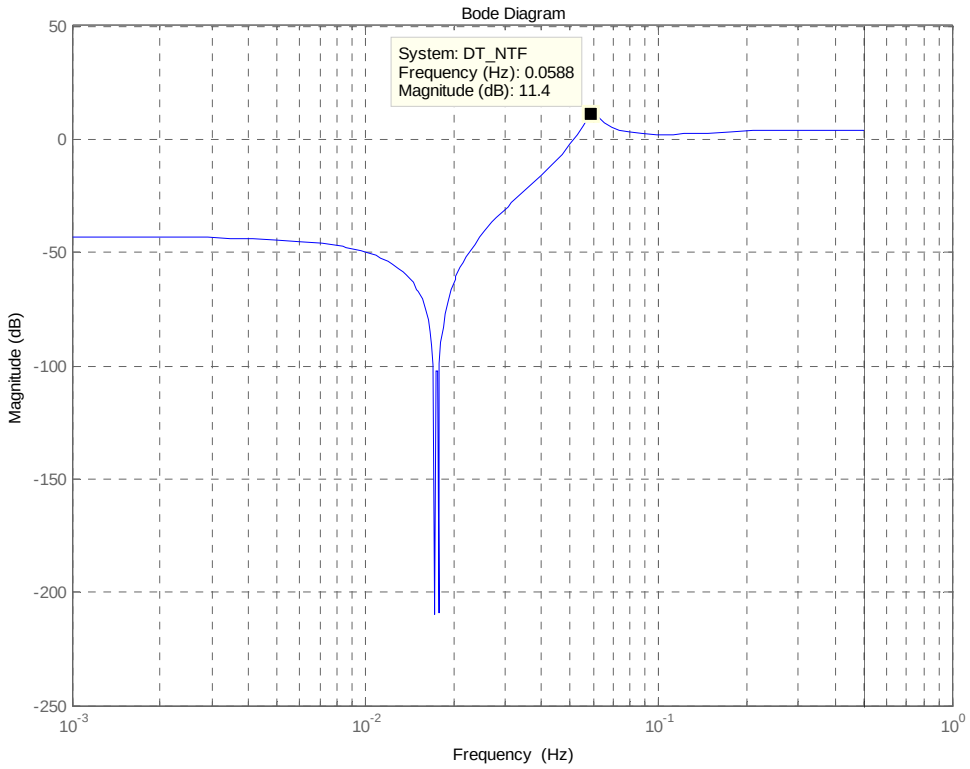

Figure 3.30 NTF with 11.4 dB Maximum Out-of-band Gain.

In order to improve the stability of the modulator, the coefficient of s^2 in Equation (3.23) is to be tuned to that in Equation (3.21). This can be done by increasing either a_1 or b_1. Increasing b_1 decreases both coefficients of s^1 and s^0 and in fact both of them are already smaller than the desired values. On the other hand, increasing a_1 only affects the coefficient of s^0 and the amount of drop of that coefficient is also less compared with that if b_1 is increased. Numerous simulations were performed by varying a_1 and when a_1 is 1.6 times as the original value, the modulator performance in terms of dynamic range is the best. As shown in Figure 3.31, the maximum out-of-band gain of the NTF has been reduced to be less than 6dB. The new coefficients for the bandpass modulator for CW

Doppler mode are summarized in Table 3.4. To switch between the two modes, only a few additional switches are needed in the implementation.

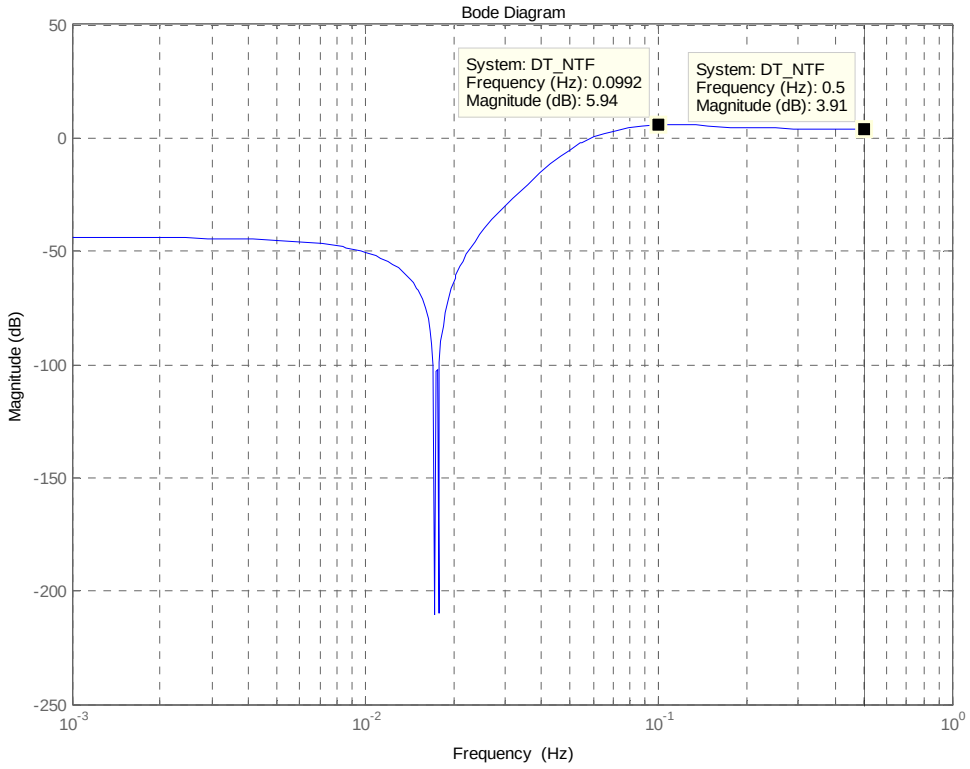

Figure 3.31 NTF with 5.94 dB Maximum Out-of-band Gain.

Table 3.4 Bandpass DSM Coefficients.

a_1	4.9056	b_1	0.2980	c_1	0.2980	g_1	0.0989	k	0.4166
a_2	3.6782	b_2	0.2980	c_2	0.3029	g_2	0.0392		
a_3	4.0378			c_3	0.1497				
a_4	3.1020								

The proposed structure was simulated in Matlab and the time domain outputs were used to extract the PSD as well as the SNR value. The numbers of data collected to perform the FFT for the low-pass and the bandpass modulators are 4096 and 16384

respectively. The PSD plots are shown in Figure 3.32 with frequency normalized to the sampling frequency. The SNR values are 55.1dB and 112.8dB for the low-pass and the bandpass modulators respectively with an input of -6dBFS. In Figure 3.33, the dynamic ranges of the low-pass and the bandpass modulators are 62.5dB and 115.0dB respectively. These results are summarized in Table 3.5.

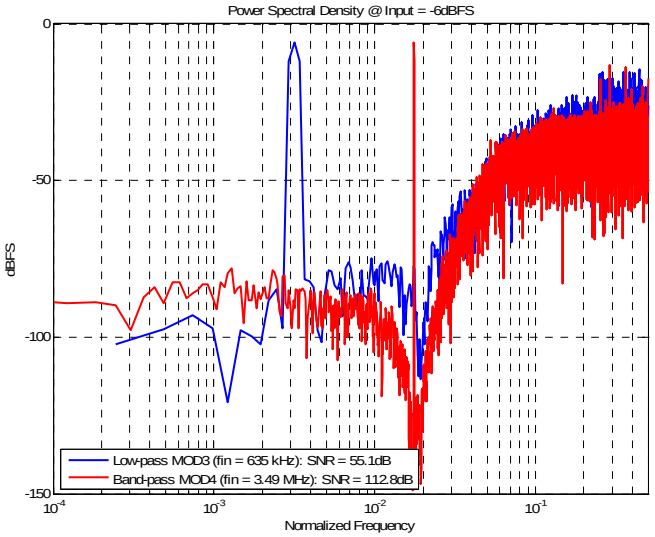

Figure 3.32 PSD of Low-pass and Bandpass DSMs.

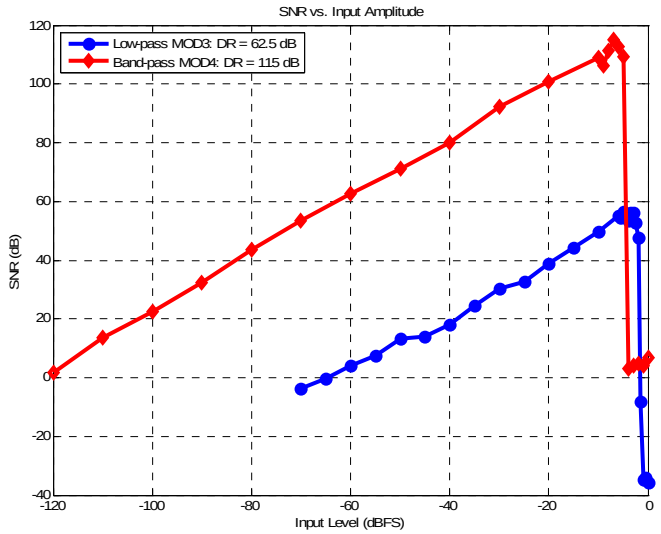

Figure 3.33 SNR vs. Input Amplitude of Low-pass and Bandpass DSMs.

Table 3.5 Low-pass and Bandpass DSM Summary.

	Low-pass DSM	Bandpass DSM
Operating Mode	B-mode	CW Doppler
Modulator Order	3rd	4th
Sampling Frequency	200MHz	200MHz
Center Frequency	3.5MHz	3.5MHz
Signal Bandwidth	5MHz	200kHz
Peak SNR	56.7dB	115.0dB
Dynamic Range	62.5dB	115.0dB
Effective Number of bits	10.1-bit	18.8-bit

In order to evaluate the robustness of the proposed structure, every coefficient of both low-pass and bandpass modulators was modeled by a normal distribution which contains 100 randomly generated data. Each distribution has a mean of the corresponding nominal coefficient value and a standard deviation of 0.03, so that the variations are mostly limited within ±10% of the mean value. Simulations were performed with an input of -10dBFS at which both modulators are less sensitive to the input overload. As shown in Figure 3.34, the low-pass DSM is quite robust against the coefficient variation and its

SNR ranges from 49.0dB to 54.0dB. On the other hand, the bandpass DSM is relatively more sensitive to the coefficient variation with its SNR distributing from 96.5dB to 113.0dB, partially due to its high SNR value.

Due to project time constraint, the bandpass structure was studied and simulated in system level and only low-pass structure was implemented in transistor level and sent for fabrication.

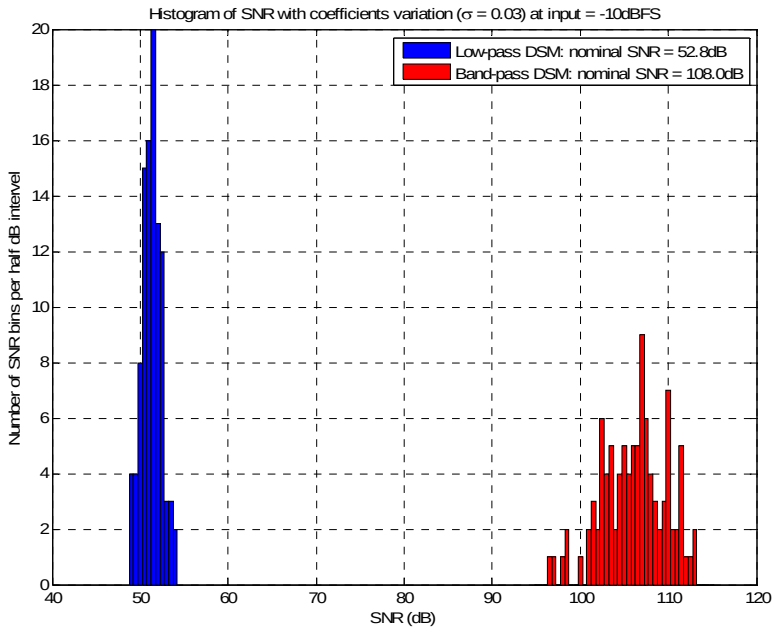

Figure 3.34 Histogram of SNR with Coefficient Variation.

Chapter 4 Transistor Level Design and Simulation

4.1 Circuit Block Specifications

The designed CT MOD3 in circuit blocks is shown in Figure 4.1 which is implemented from Figure 3.10 (repeated below as shown in Figure 4.2). Compare Figure 4.1 with Figure 4.2, it can be seen that all the coefficients except c_1 and k are implemented as transconductors, which are used to convert voltage to current. Coefficients c_1 and k are the scaling factors of the two DACs. As discussed previously, the two DACs are simple voltage/current switchers. Since the loop filter is implemented using G_mC, switch current DACs are designed. All the 1/s blocks are implemented as capacitors which can be used to integrate current to voltage. A latched comparator is used to implement the quantizer. In addition, the half clock cycle delay as shown in Figure 4.2 is realized inside the quantizer.

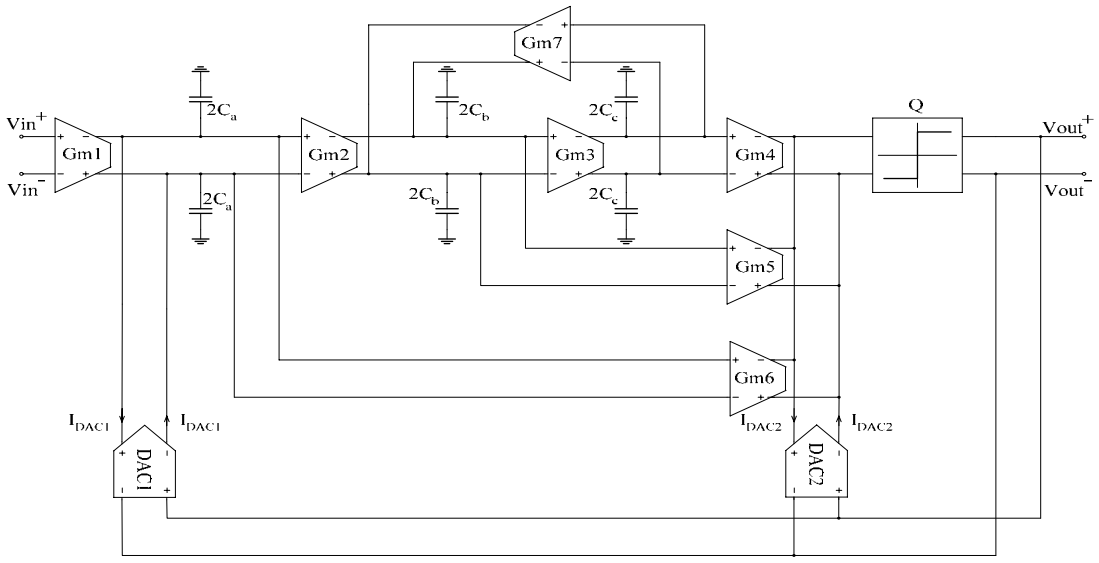

Figure 4.1 CT MOD3 Circuit Block Realization.

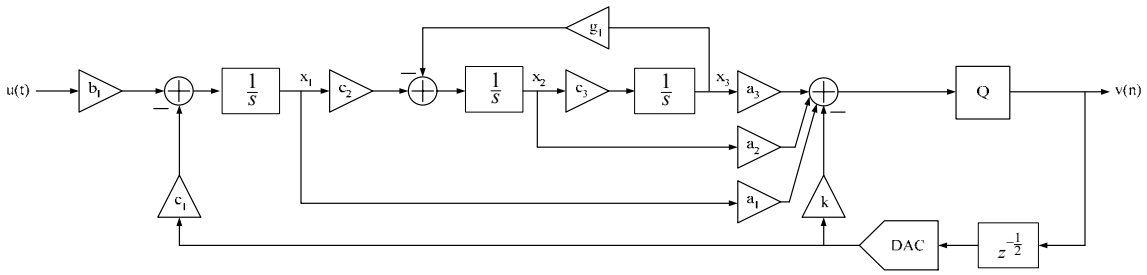

Figure 4.2 CT MOD3 with Feedforward Loop Filter.

For all the current outputs in transconductors and DACs, the plus sign indicates the output current is entering into the block and the minus sign indicates the output current is leaving from the block. Integration capacitors are split into two for stabilizing the CMFB.

Together with Figure 4.2, the following circuit parameters dependency can be shown:

$$b_1 f_s = \frac{G_{m1}}{C_a} \Rightarrow G_{m1} = b_1 \cdot f_s \cdot C_a \tag{4.1}$$

$$c_2 f_s = \frac{G_{m2}}{C_b} \Rightarrow G_{m2} = c_2 \cdot f_s \cdot C_b \tag{4.2}$$

$$g_1 f_s = \frac{G_{m7}}{C_b} \Rightarrow G_{m7} = g_1 \cdot f_s \cdot C_b \tag{4.3}$$

$$c_3 f_s = \frac{G_{m3}}{C_c} \Rightarrow G_{m3} = c_3 \cdot f_s \cdot C_c \tag{4.4}$$

$$a_1 : a_2 : a_3 = G_{m6} : G_{m5} : G_{m4} \tag{4.5}$$

$$V_{ref} = \frac{I_{DAC1}}{G_{m1}} \Rightarrow I_{DAC1} = G_{m1} \cdot V_{ref} \tag{4.6}$$

$$\frac{I_{DAC2}}{k} = \frac{I_{DAC1} \cdot \frac{1}{sC_a} \cdot G_{m6}}{c_1 \frac{f_s}{s} a_1} \Rightarrow I_{DAC2} = k \cdot \frac{G_{m6}}{a_1} \cdot V_{ref} \tag{4.7}$$

Therefore, all the transconductors, capacitors and DAC currents can be determined numerically. The absolute values of transconductance as well as capacitance are chosen based on device noise, capacitor matching and power consumption considerations. Derived specifications are shown in Table 4.1:

Table 4.1 Transconductor Specifications with $V_{ref} = 0.5V_p$.

	G_{m1}	G_{m2}	G_{m3}	G_{m4}	G_{m5}	G_{m6}	G_{m7}
$G_{m,norminal}$ (μA/V)	212	21.2	21.2	28	25.4	21.2	6.9
IM3 Difference @ -3dBFS @ 5MHz (dBc)	> 50	> 30	> 30	> 30	> 30	> 30	> 30
DC Gain (dB)	> 30	> 30	> 30	> 30	> 30	> 30	> 30
Input Referred Noise Power ($10^{-9}V^2$)	< 35.3	—	—	—	—	—	—

To make the circuit noise non-dominant in the first transconductor, the input referred noise power is set to be 3dB below the in-band quantization noise power with $1V_{p-p}$ full scale voltage. For the other transconductor blocks, their device noises are highly suppressed by the loop filter. Capacitor and DAC current specifications are shown in Table 4.2 and Table 4.3 respectively.

Table 4.2 Capacitor Values.

	C_a	C_b	C_c
Capacitance (pF)	3.55	0.35	0.71

Table 4.3 DAC Current Values.

	I_{DAC1}	I_{DAC2}
Current (μA)	106	1.80

4.2 Transconductor Design and Simulation

A transconductor with improved linearity is shown in Figure 4.3 and the components sizes of the input transconductor are listed in Table 4.4. The operation is as follows: since the input stage transistors M1 and M2 are working as source followers, the input signal of the transconductor, which is the voltage difference between V_{in}^{+} and V_{in}^{-}, will be buffered across the equivalent resistor formed by M11 – M14. The equivalent resistor is used to convert the input voltage into current. Therefore, a transconductor is realized with its transconductance equal to the inverse of the equivalent resistance formed by M11 – M14. The current is further mirrored to the output through current mirrors and converted into a differential form. Transistors M5 and M6 are used as negative feedback at the source of the input transistors in order to reduce the output impedance of the source followers. M9 and M10 sense the gate-source voltages of M5 and M6 and mirror the current to the output. M3 – M4 and M7 – M8 are cascode stages to increase the current mirror output impedance. The two capacitors C_c are used to compensate the negative feedback loop. All the current sources shown in the figure are implemented by wide-swing current sources.

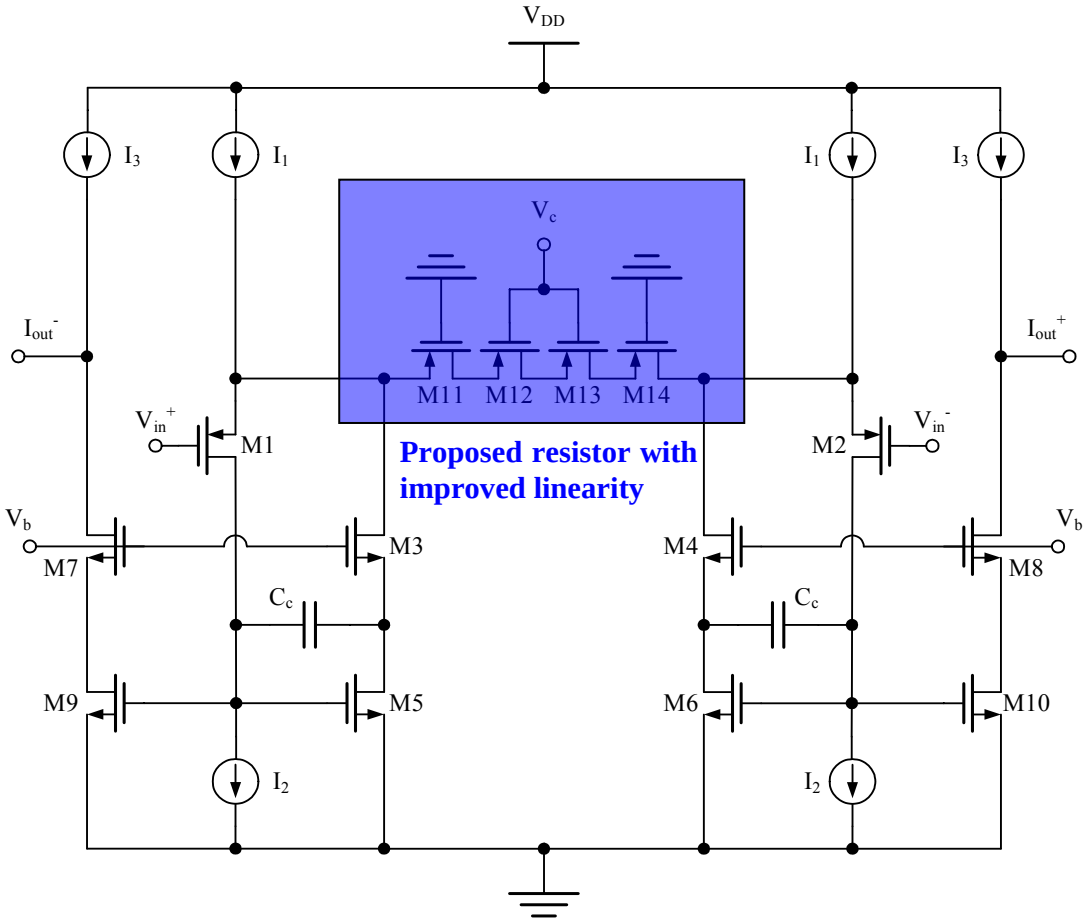

Figure 4.3 An Improved Transconductor using Series Transistors to Reduce Mobility Degradation.

Table 4.4 Components Sizes of Input Transconductor

Components	Size	Unit
M1, M2	120/0.8	μm/μm
M3, M4	16/0.18	μm/μm
M5, M6	32/0.5	μm/μm
M7, M8	16/0.18	μm/μm
M9, M10	32/0.5	μm/μm
M11 – M14	27/1	μm/μm
I1	240	μA
I2	80	μA
I3	160	μA
Cc	0.5	pF

In a more detailed analysis, it can be shown that transistors M3 – M6 are added to form two super source followers [58] in order to further reduce the output resistance. Here, M3 – M6 are also used to carry the signal current which is mirrored to the output by M7 – M10. It can be shown that the closed-loop output resistance of the super source follower is given by [58]:

$$R_{out} \approx \frac{g_{m3} r_{o3} r_{o5}}{g_{m5} \cdot g_{m3} r_{o3} r_{o5} \cdot g_{m1} r_{o1}} = \frac{1}{g_{m5} g_{m1} r_{o1}} \tag{4.8}$$

As the super source follower has a local negative feedback, a capacitor C_c is added to compensate the loop. Wide-swing current mirrors (M3 – M10) are employed to increase the current copy accuracy as well as the output resistance. Similarly, all the other current sources (I_1 – I_3) are also generated by wide-swing current mirrors. An advantage of this transconductor is that it can easily form multiple outputs (as a result, multiple transconductors) by simply including additional current mirrors, as long as all the formed transconductors share the same input [29]. In this project, the seven transconductors can

be eventually reduced to four main transconductors where three of them have two outputs. This approach generally saves power consumption as well as die area. About 30% reduction in terms of power consumption and die area is expected from transconductors by using this technique compared to using the same blocks without sharing the transconductance core.

In this thesis, a more linear equivalent resistor formed by M11 – M14 with reduced mobility degradation is proposed. The design in [29, 59] uses one transistor operating in triode as a resistor and the equivalent transconductance is equal to the inverse of the small-signal resistance of the triode transistor. In [29], the authors have assumed that the transistor used to converter voltage into current is operating in deep-triode and the V_{DS}^2 term is removed in the current equation, so that the small-signal resistance is given by:

$$r_{DS} = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)\left(V_{SG} - |V_{tp}|\right)} \tag{4.9}$$

However, as long as the transistor is in triode region and the input signal is differential, the drain current can be expressed as:

$$\begin{aligned} |i_D| &= \mu_p C_{ox}\left(\frac{W}{L}\right)\left[\left(v_{SG} - |V_{tp}|\right)\cdot v_{SD} - \frac{1}{2}v_{SD}^{\,2}\right] \\ &= \mu_p C_{ox}\left(\frac{W}{L}\right)\left[\left(V_{DC} + \frac{1}{2}v_{in} - V_G - |V_{tp}|\right)\cdot v_{in} - \frac{1}{2}v_{in}^{\,2}\right] \\ &= \mu_p C_{ox}\left(\frac{W}{L}\right)\left(V_{DC} - V_G - |V_{tp}|\right)\cdot v_{in} \end{aligned} \tag{4.10}$$

where V_{DC} is the DC drain-source voltage and v_{in} is the input voltage. Thus, the equivalent transconductance can be written as:

$$G_m = \mu_p C_{ox} \left(\frac{W}{L} \right) \left(V_{DC} - V_G - \left| V_{tp} \right| \right) \tag{4.11}$$

At large gate-source voltages, the high vertical electric field confines the charge carriers to a narrower region below the oxide-silicon interface, leading to more carrier scattering and hence lower mobility, which is generally referred as mobility degradation [60]. An empirical equation modeling this effect for PMOS is given by [60]:

$$\mu_{eff} = \frac{\mu_p}{1 + \theta \left(V_{SG} - \left| V_{tp} \right| \right)} \tag{4.12}$$

where μ_p is the zero-field mobility, θ is an empirical fitting parameter and $(V_{SG} - |V_{tp}|)$ is the overdrive voltage of the transistor.

As a result of mobility degradation, the effective transconductance becomes smaller than the zero-filed mobility as the overdrive voltage is non-zero. Moreover, since the overdrive voltage also varies with the input voltage, the transconductance also changes with the input voltage. This dependence of the transconductance on the input voltage will generate harmonics and thus degrade the overall linearity.

In order to reduce the effect of mobility degradation, four transistors (M11 – M14) are put in series. In this configuration, only one of the two transistors on the sides (M11 when input voltage is positive or M14 when input voltage is negative) suffers severely from mobility degradation due to the largest gate-source voltage. In other words, although there is still one transistor experiencing the same degree of mobility degradation as the original design, the effective transconductance value now depends on all the four transistors instead of only one, resulting in less susceptibility on the mobility degradation. In addition, the tuning voltage V_c is connected to only the gates of M12 and M13 which are shielded by the other transistors. The drawback is that the tuning range is reduced for the improved linearity. It should be noted that the body terminals of all the four PMOS have to be connected to V_{DD} since the source and drain terminals will exchange during operation. Therefore, they must share the same n-well.

Periodic Steady-State (PSS) and Periodic AC (PAC) simulations were performed with varying input voltage to extract the IM3 value of the four-transistor in series as well as the case of single transistor. As shown in Figure 4.4, the linearity of the output current of the series transistors (in blue) is about 20dB higher than that of the single transistor (in red). With the specified IM3 requirement (50dBc for -3dBFS peak input), the peak input voltage is limited to 200mV in the single transistor case while on the other hand, it can be extended to more than 500mV in the series transistors case, resulting in significantly increased input range.

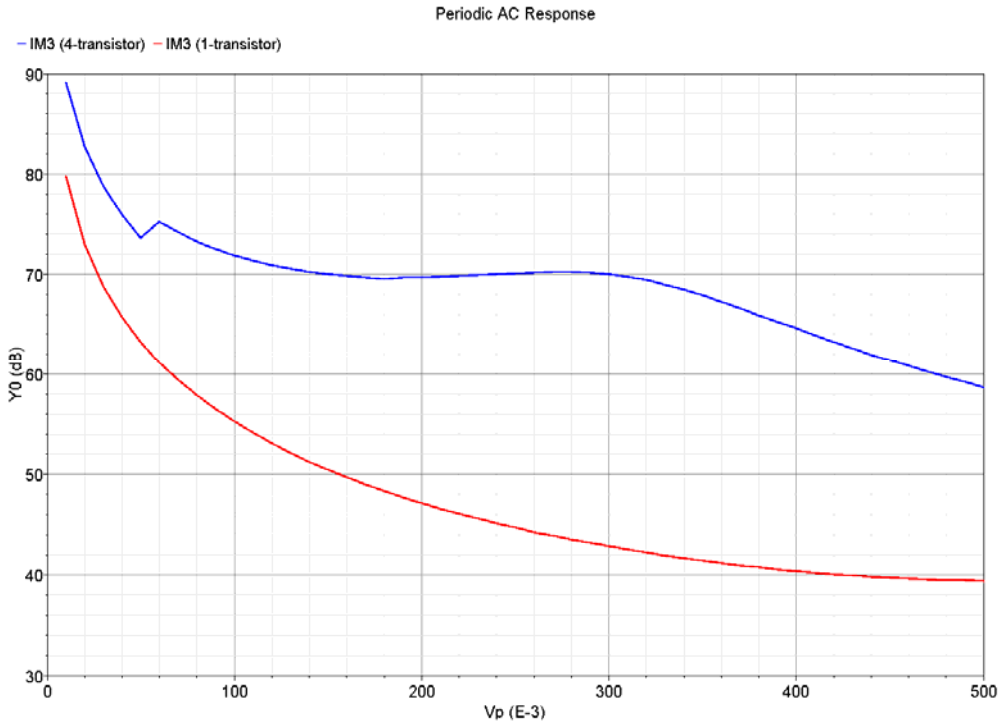

Figure 4.4 Improved Linearity of Series Transistors for G_{m1}.

PSS simulation was also performed on the transconductor block. The IM3 and transconductance simulation results of the first transconductor at 5MHz are shown in Figure 4.5 and Figure 4.6 respectively. In simulation, the load capacitor is chosen such that at 5MHz the voltage gain of the integrator is unity. This is because that the input and output swings of an integrator are designed to be in the same range. The integrator may get saturated with a smaller load capacitor (in other words, with a voltage gain higher than unity), resulting in harmonic distortion. This is unlikely to happen in the closed-loop system since the integrator output has already been limited through dynamic scaling in system level design. On the other hand, a larger load capacitor may unintentionally reduce the distortion at the output.

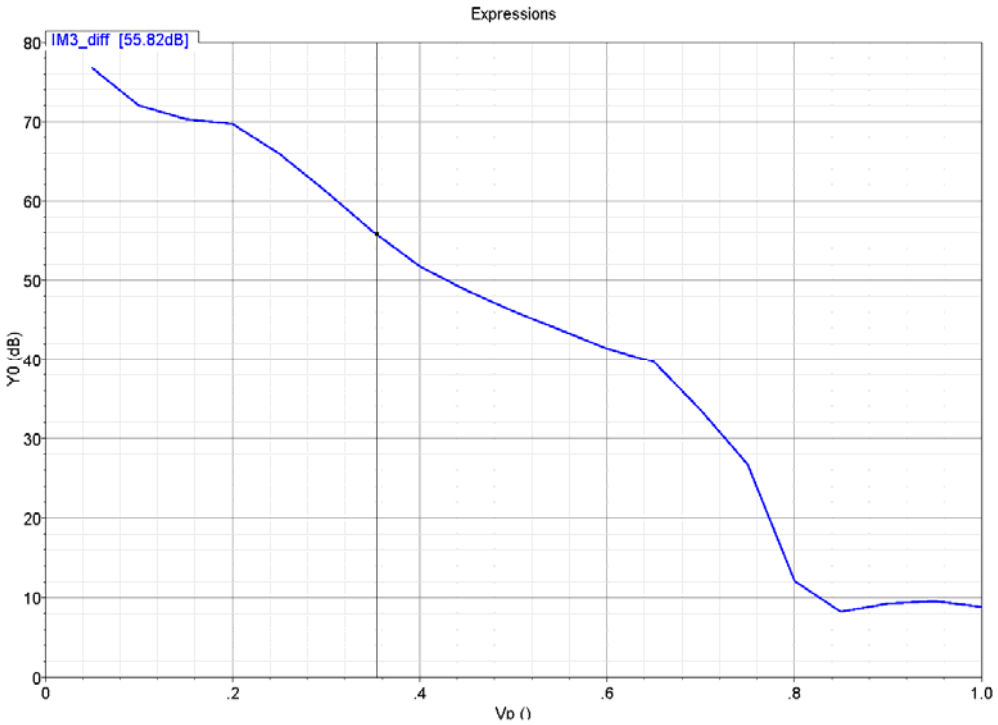

Figure 4.5 IM3 of G_{m1}.

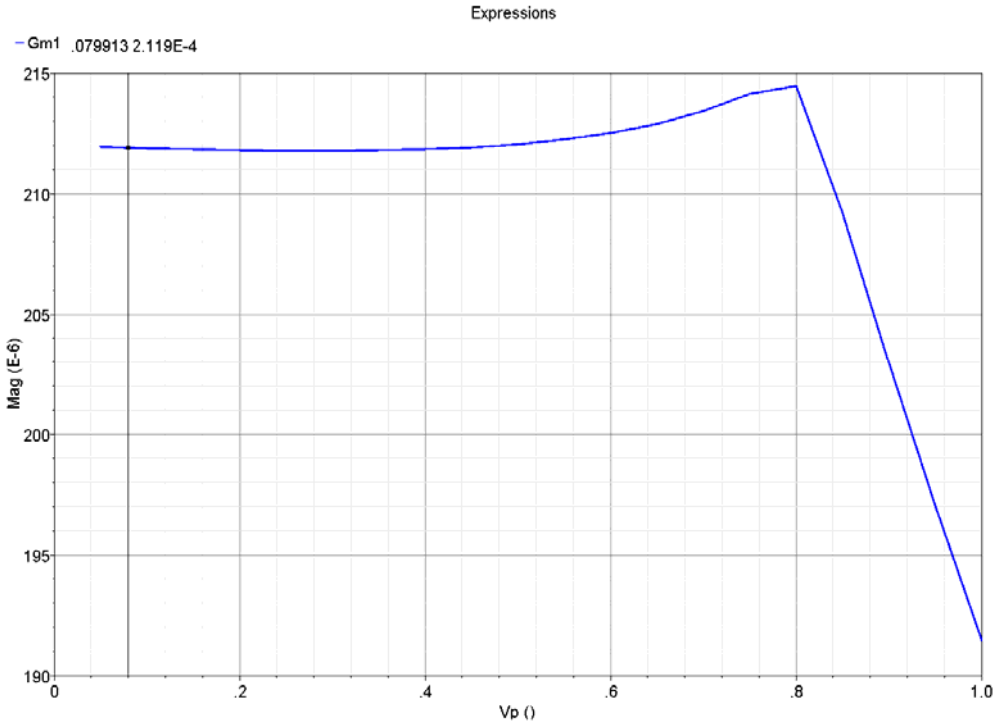

Figure 4.6 G_m of G_{m1}.

AC, noise and transient simulations were performed on the first integrator with the specified load capacitor (in Table 4.2) and the results are shown in Figure 4.7 to Figure 4.9 respectively. In the AC simulation as shown in Figure 4.7, it can be seen that the DC gain is 40dB which is 10dB higher than the required 30dB (Table 4.1). The simulated unity-gain bandwidth is 9.5MHz as designed value which is G_{m1}/C_a. In Figure 4.8, input noise power of the transconductor is integrated over the passband and the simulated noise power is 27.3e-9V^2 which is smaller than the required 35.3e-9V^2 (Table 4.1). The transient simulation with a sine wave input voltage is shown in Figure 4.9. The differential output current is plotted together with the input and it can be seen that the transconductor is stable and is able to convert a voltage into a current linearly.

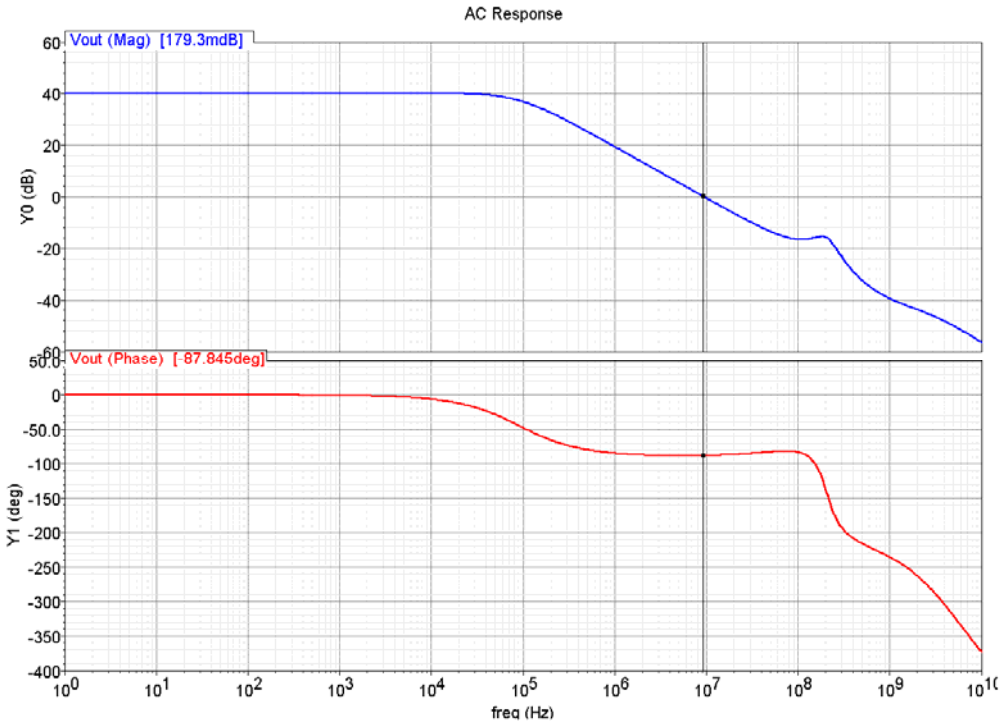

Figure 4.7 Integrator AC Simulation.

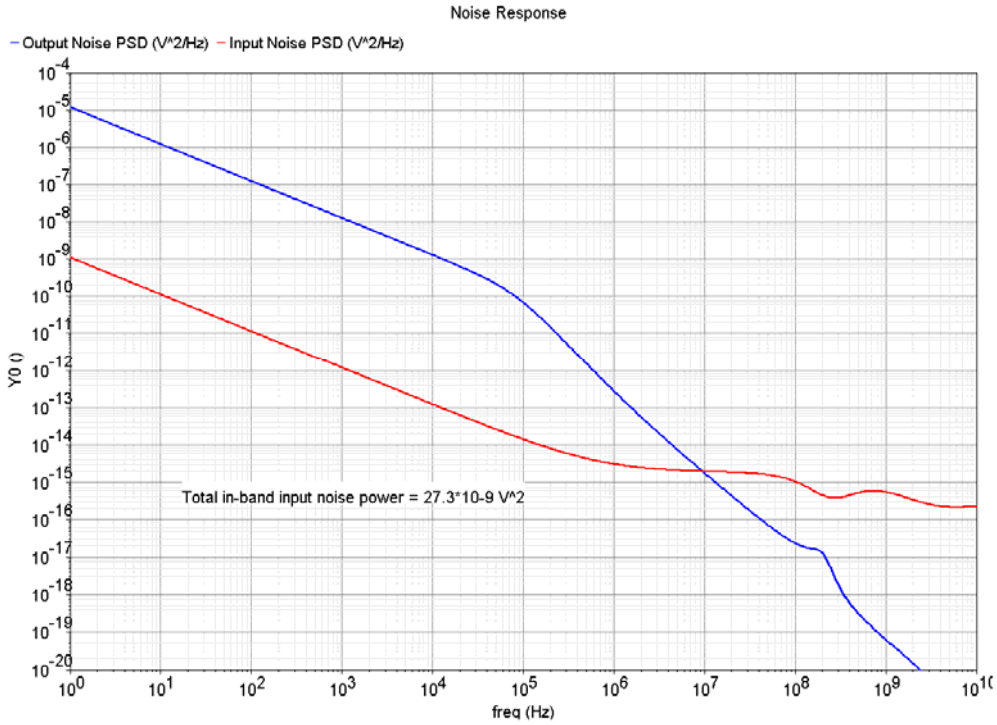

Figure 4.8 Integrator Noise Simulation.

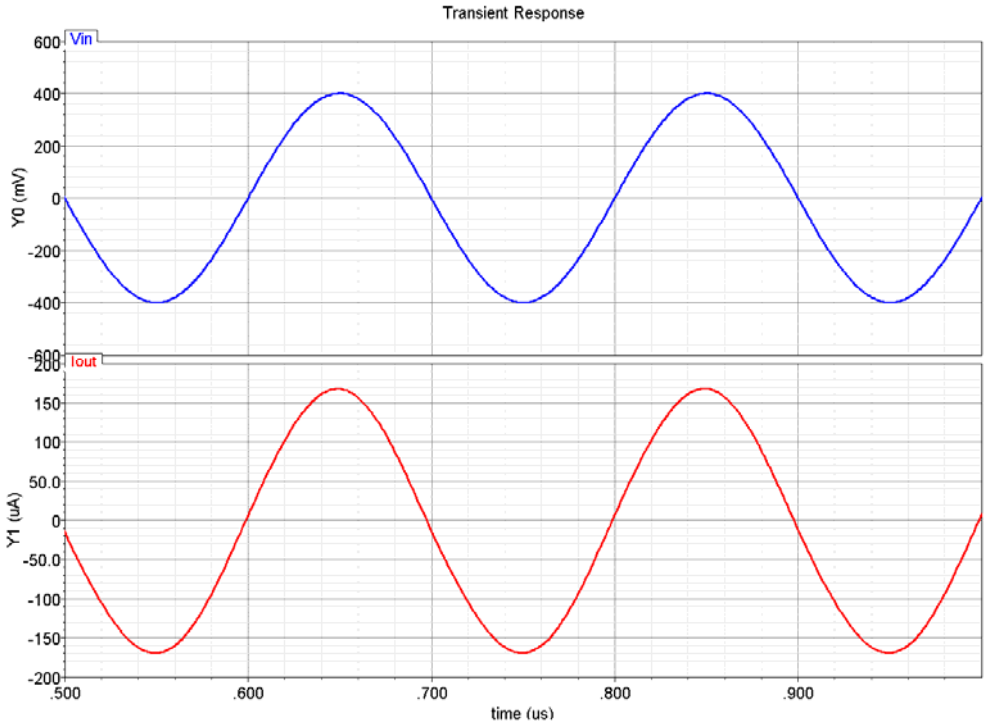

Figure 4.9 Transient Simulation with Output Current.

With the tuning voltage V_c varying from 0 to 0.4V ($V_{c,\ nominal}$ = 0.2V), the transconductance variations at $0.01V_{p\text{-}p,\ diff}$ and the IM3 variations at -3dBFS for all the transconductors are plotted in Figure 4.10 and Figure 4.11 respectively. It can be observed that all the transconductors can be tuned approximately from 70% to 120% of their nominal values. The IM3 also varies with the tuning voltage. Since the IM3 of the first transconductor is required to be below -50dBc, its tuning voltage can only be tuned between 0.1 to 0.25V, limiting its transconductance ranging from 200 to 235μA/V.

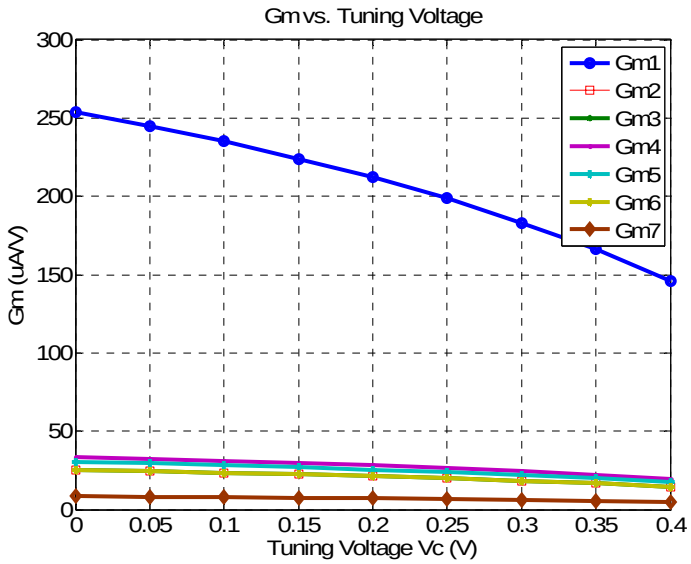

Figure 4.10 G_m vs. Tuning Voltage.

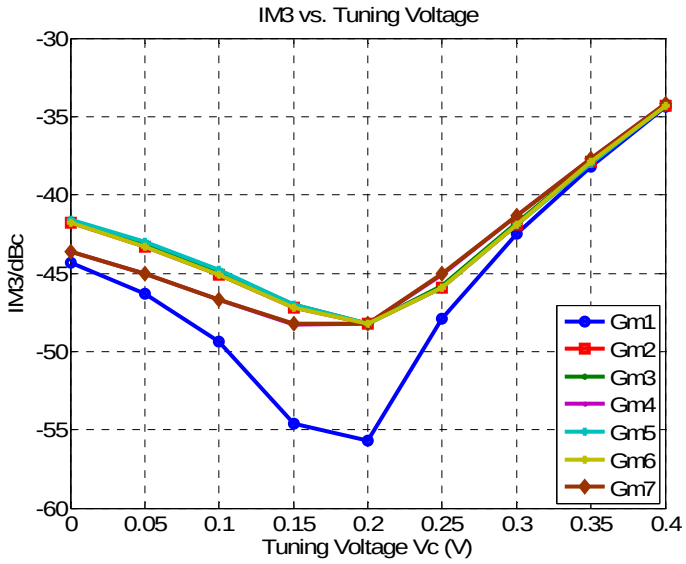

Figure 4.11 IM3 vs. Tuning Voltage.

Same simulations were also performed on the other transconductor blocks and the results are summarized in Table 4.5. The power consumption values of G_{m2} to G_{m4} also include that of G_{m5} to G_{m7}.

Table 4.5 Transconductor Simulation Summary after Merging.

	G_{m1}	G_{m2}	G_{m3}	G_{m4}	G_{m5}	G_{m6}	G_{m7}
$G_{m,norminal}$ (μA/V)	212	21.7	21.7	28.3	27.5	21.9	7.05
IM3 Difference @ -3dBFS @ 5MHz (dBc)	55.8	60.3	60.3	58.3	55.8	56.1	61.2
DC Gain (dB)	40.3	39.9	39.9	38.0	38.6	38.2	40.9
Input Referred Noise Power ($10^{-9}V^2$)	27.3	294.2	294.2	272.1	273.3	296.6	513.3
Power Consumption (mW)	1.48	0.36	0.37	0.37	—	—	—
Transconductance Tuning Range	94.3 – 110.8%	68.9 – 119.8%	68.9 – 119.8%	68.8 – 119.5%	69.0 – 119.6%	68.9 – 119.8%	69.0 – 119.6%
IM3 Variation with Tuning Voltage (dB)	-44.3 – -34.4	-41.8 – -34.3	-41.7 – -34.3	-43.6 – -34.2	-41.6 – -34.3	-41.8 – -34.3	-43.6 – -34.2

As mentioned previously, transconductors sharing the same inputs can eventually be merged together and only current mirrors are needed. Figure 4.12 shows the block diagram after merging.

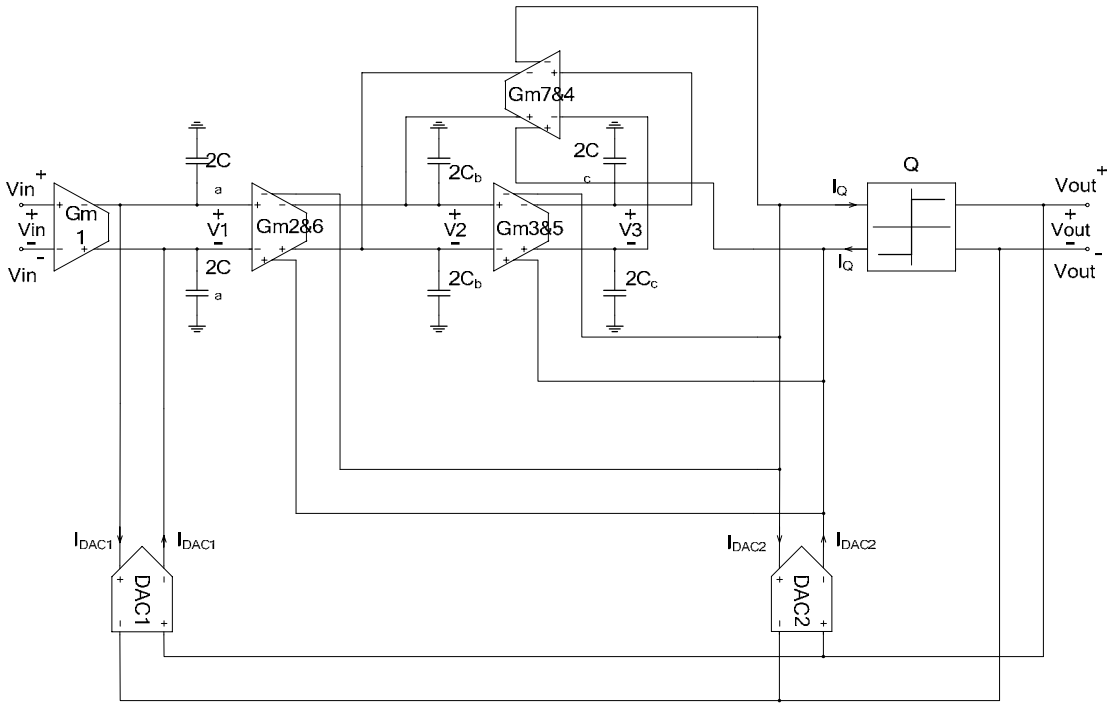

Figure 4.12 CT MOD3 Circuit Block Realization after Merging Transconductors.

4.3 Quantizer Design and Simulation

Since the output of the loop filter is current, a differential latched current comparator is used [61]. This comparator has the advantages of being simple since only 9 transistors are used and being high speed because it is operating in current mode. As shown in Figure 4.13, the comparator consists of one pair of cross-coupled inverters. The transistor sizes are shown in Table 4.6. The latched comparator is controlled by two non-overlapping clock phases which are generated by two digital NOR gates with delays [29].

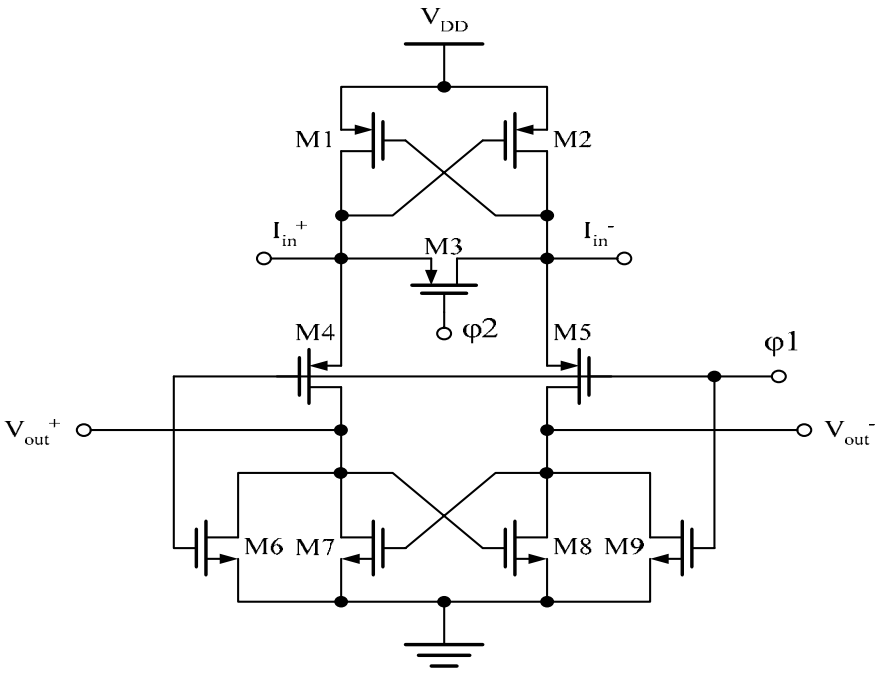

Figure 4.13 Latched Current Comparator.

Table 4.6 Components Sizes of Latched Current Comparator.

Components	Size	Unit
M1, M2	9/0.18	μm/μm
M3	3/0.18	μm/μm
M4, M5	3/0.18	μm/μm
M6, M9	1/0.18	μm/μm
M7, M8	3/0.18	μm/μm

The operation can be explained as follows: when clock φ_1 is high, the comparator is in reset mode and the input current flows through switch M3. Both output voltages are pulled to ground by M6 and M9. The final output after latches will hold previous states during this phase. Before M3 turns off, clock φ_1 goes low and the current difference starts to be amplified, reducing the regeneration time. Finally during φ_2, after M3 turns off, the

comparator enters into high gain regeneration mode and then differential input current will be converted and amplified to a differential output voltage. The polarity of the output voltage depends on the input current direction. In this design, if input current is flowing from I_{in}^{+} to I_{in}^{-}, the output voltage $(V_{out}^{+} - V_{out}^{-})$ will be positive. The output voltage will be further buffered by inverters to achieve full logic and latched by D flip-flops to generate the half clock cycle delay.

Usually, in order to obtain higher resolution and to minimize kickback noise, one or more preamplification stages are required in front of the latched comparator [29]. As shown in Figure 4.14, a current preamplifier with class-AB input stage is employed here [61] and the designed sizes are summarized in Table 4.7. Since the comparator resolution requirement is highly relaxed by the loop filter and the speed is a more critical design criteria, the preamplifier only provides a low gain of three. More importantly, the preamplifier prevents the kickback noise to enter into the output of the loop filter.

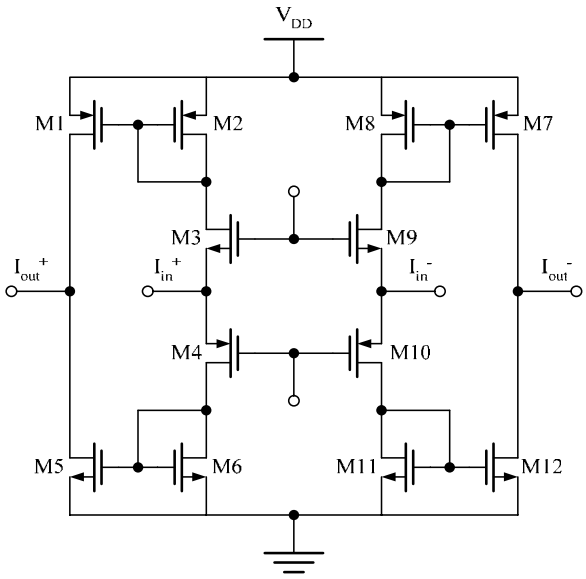

Figure 4.14 Current Preamplifier with Class-AB Input Stage.

Table 4.7 Components Sizes of Current Preamplifier

Components	Size	Unit
M1, M7	28.8/0.2	μm/μm
M2, M8	9.6/0.2	μm/μm
M3, M9	12.8/0.2	μm/μm
M4, M10	38.4/0.2	μm/μm
M5, M12	12/0.2	μm/μm
M6, M11	4/0.2	μm/μm

The latched comparator and the preamplifier was simulated with a differential current with amplitude of +/-20uA. As shown in Figure 4.15, at the end of phase φ_1, the comparator samples the input current. At the end of phase φ_2, the comparator outputs logic depending on the sign of the previous sampled input current.

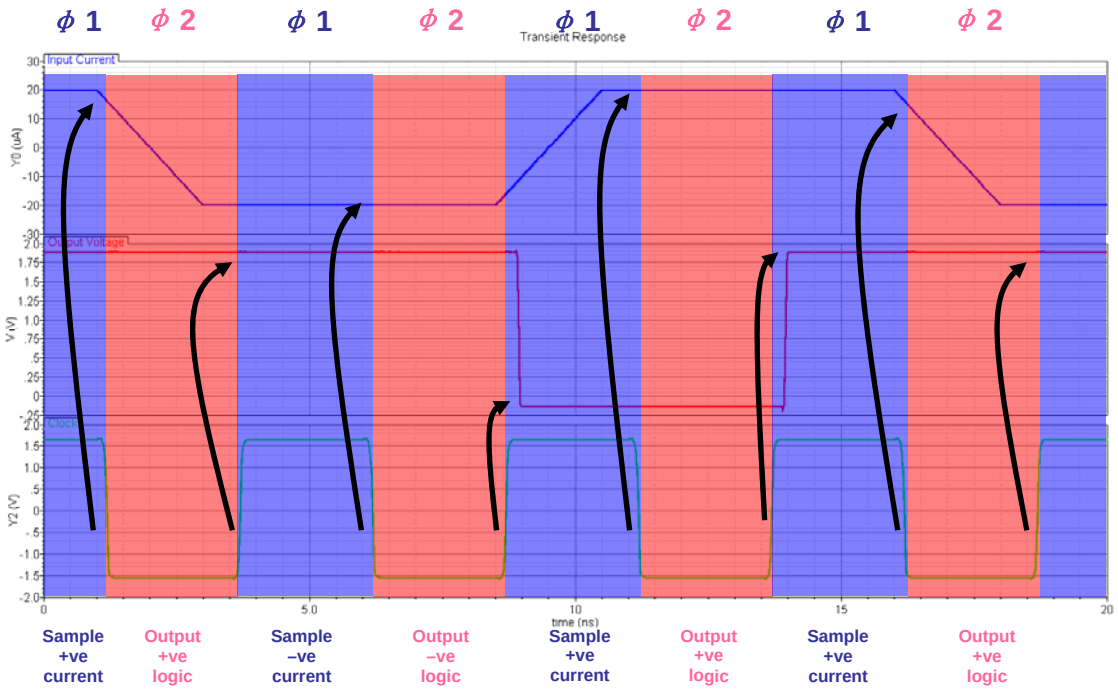

Figure 4.15 Comparator Output Voltage Response in Two Phases.

The latched comparator and the preamplifier was simulated with 1nA input current. The differential output voltage (before being buffered) is plotted in Figure 4.16 and it can be observed that the regeneration time for the output to restore well-defined digital logic levels is less than 0.28ns, which is much less than the required half clock cycle of 2.5ns.

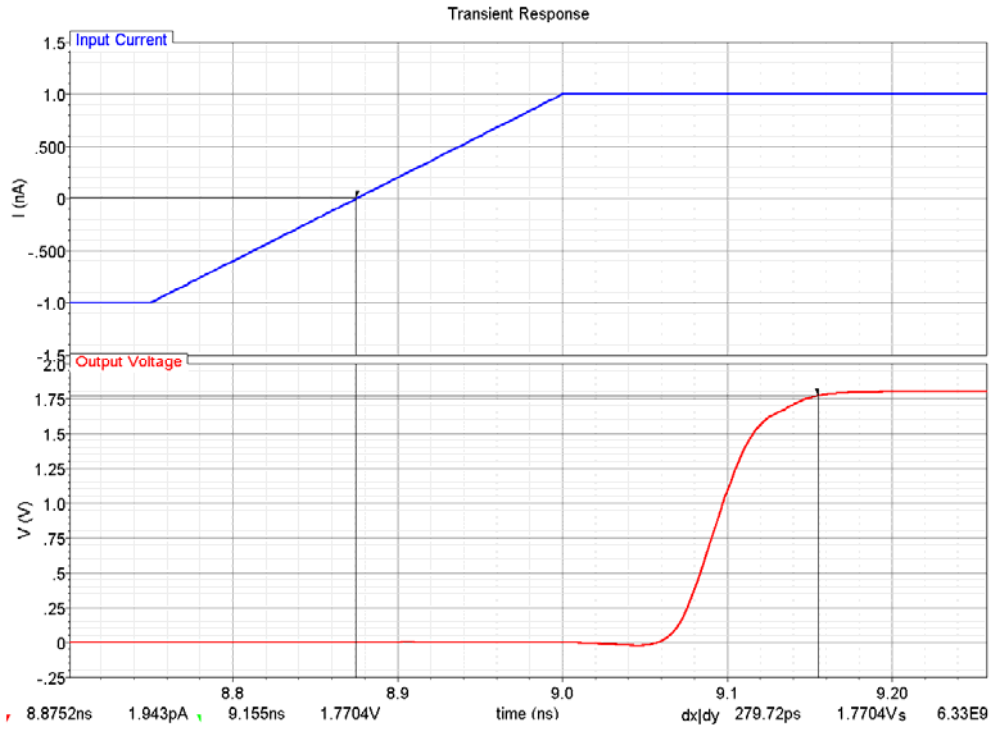

Figure 4.16 Comparator Output Voltage Response with 1nA Input Current.

4.4 Digital-to-Analog Converter Design and Simulation

The DAC is implemented based on a simple current steering structure as shown in Figure 4.17. The fundamental advantages of this DAC are its simple structure and high speed. The output current is either sourced to or sunk from the loop filter depending on the input sign. The current source is implemented by cascode structure to reduce the channel-length modulation effect. The output currents of the two DACs with magnitudes of 212uA and 3.6uA are shown in Figure 4.18. The components sizes of DAC1 and DAC2 are listed in Table 4.8 and Table 4.9 respectively.

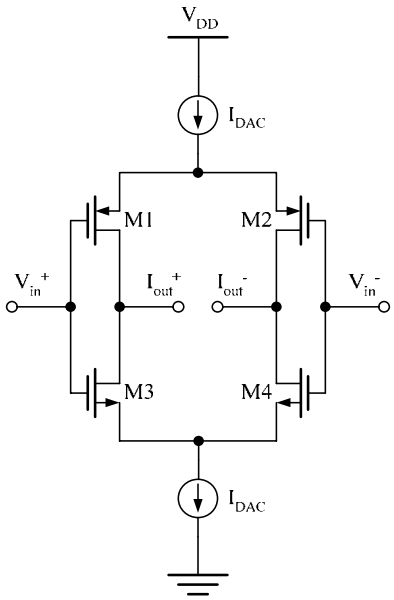

Figure 4.17 One-bit DAC.

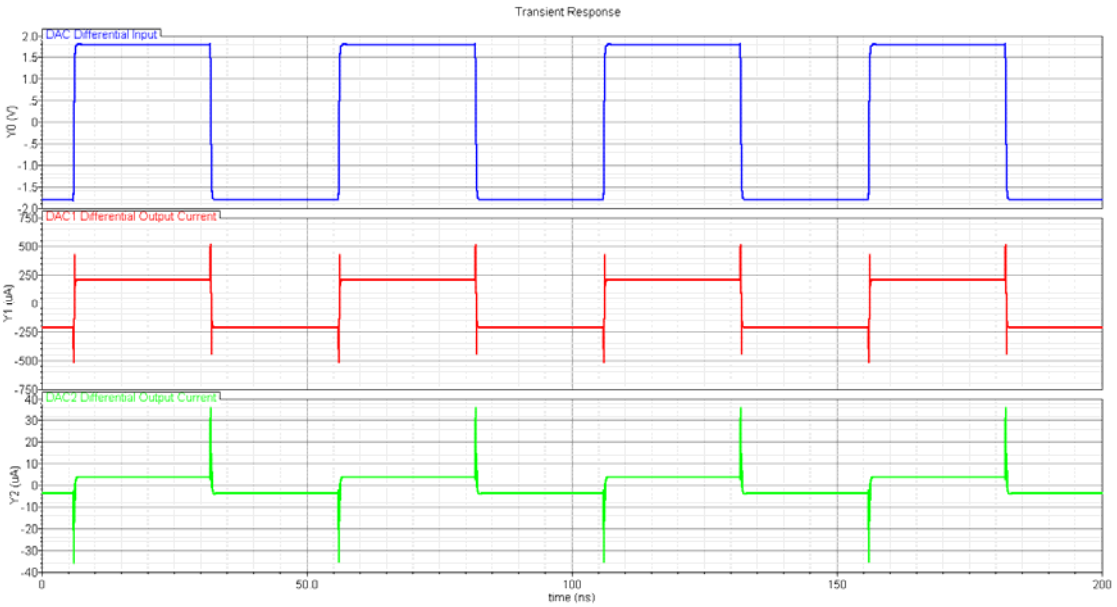

Figure 4.18 Output Differential Currents of DAC1 and DAC2.

Table 4.8 Components Sizes of DAC1

Components	Size	Unit

M1, M2	20/0.18	μm/μm
M3, M4	20/0.18	μm/μm
I_{DAC}	106	μA

Table 4.9 Components Sizes of DAC2

Components	Size	Unit
M1, M2	2/0.18	μm/μm
M3, M4	2/0.18	μm/μm
I_{DAC}	1.8	μA

4.5 Test Mode Implementation

The design consists of four transconductors, a current comparator, a single-bit current DAC, a biasing generator, an output buffer and a test multiplexer. In order to access every block and measure their performance, there are eight modes for testing individual block as well as system performance. When testing one particular block, other unused blocks are disabled. To save pin count, the input and output pins of the modulator are used in all the test modes and no additional dedicated test pin is needed. Three digital bits (B<2:0>) are used to control the test multiplexer. Transconductance tuning for all the transconductor blocks are also realized in the test mode.

Table 4.10 summarizes individual block activity in different test modes. Disable mode (000) is used to check whether there is any unexpected behavior such as high quiescent current. Enable mode (111) is the normal operating mode to measure system performance such as SNR. Biasing circuit is only disabled in the Disable mode. During the testing of transconductor blocks, the transconductor block which provides the CMFB for the transconductor under test is also enabled.

Table 4.10 Block Enabled/Disabled in Test Mode

B<2:0>	Mode	Biasing	Preamp + Quantizer	DAC	G_{m1}	G_{m2}	G_{m3}	G_{m4}
000	Disable	Dis	Dis	Dis	Dis	Dis	Dis	Dis
001	Quantizer	En	En	Dis	Dis	Dis	Dis	Dis
010	DAC	En	Dis	En	Dis	Dis	Dis	Dis
011	G_{m1}	En	Dis	Dis	En	En	Dis	Dis
100	G_{m2}	En	Dis	Dis	Dis	En	En	Dis
101	G_{m3}	En	Dis	Dis	Dis	Dis	En	En
110	G_{m4}	En	Dis	Dis	Dis	Dis	En	En
111	Enable	En	En	En	En	En	En	En

4.6 Overall System Design and Full Circuit Simulation

One quick way of checking the functionality of the implemented filter is to perform small-signal analysis on the filter. As shown in Figure 4.19, since the output of the loop filter is current, the AC output currents of the filter implemented by ideal blocks (in blue) and by circuit blocks (in red) are compared. The actual response deviates from the ideal one at low frequency due to the finite integrator gain and at high frequency due to parasitic poles and zeroes. For large signal, the filter performance is mainly limited by the nonlinearity of the integrators.

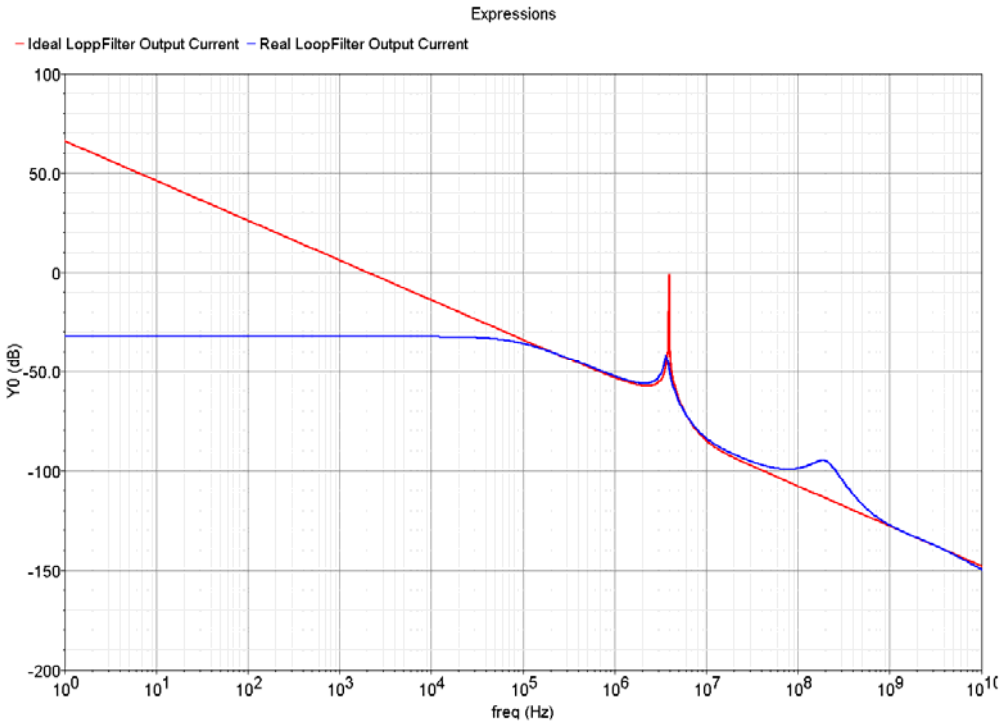

Figure 4.19 AC Response of Loop Filter $L_0(s)$.

Excess loop delay was simulated by taking the delay between the clock voltage and the DAC output current. As shown in Figure 4.20, the excess loop delay is around 0.26ns or 5.2% of one clock period.

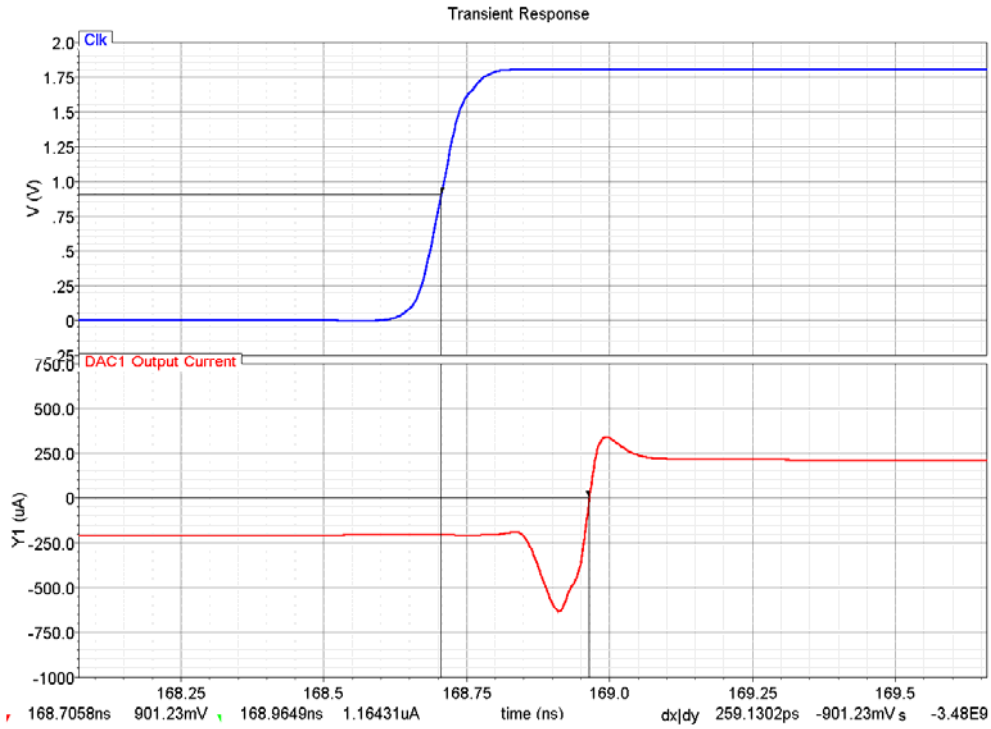

Figure 4.20 Excess Loop Delay.

Figure 4.21 shows one clip of the transient output of the DSM when input amplitude is -5dBFS. It can be observed that all the integrator outputs are at least 3dB below feedback reference. The modulator was simulated for 22.5μs while the first 2μs is used as the settling time for the circuit. The output bit stream was collected with sampling period of 5ns and processed in Matlab to generate the PSD and SNR. As in the system level simulation, a low frequency (bin 13) sinusoidal signal whose frequency is 634.765625kHz was used as input so that harmonic distortion up to seventh-order can be included.

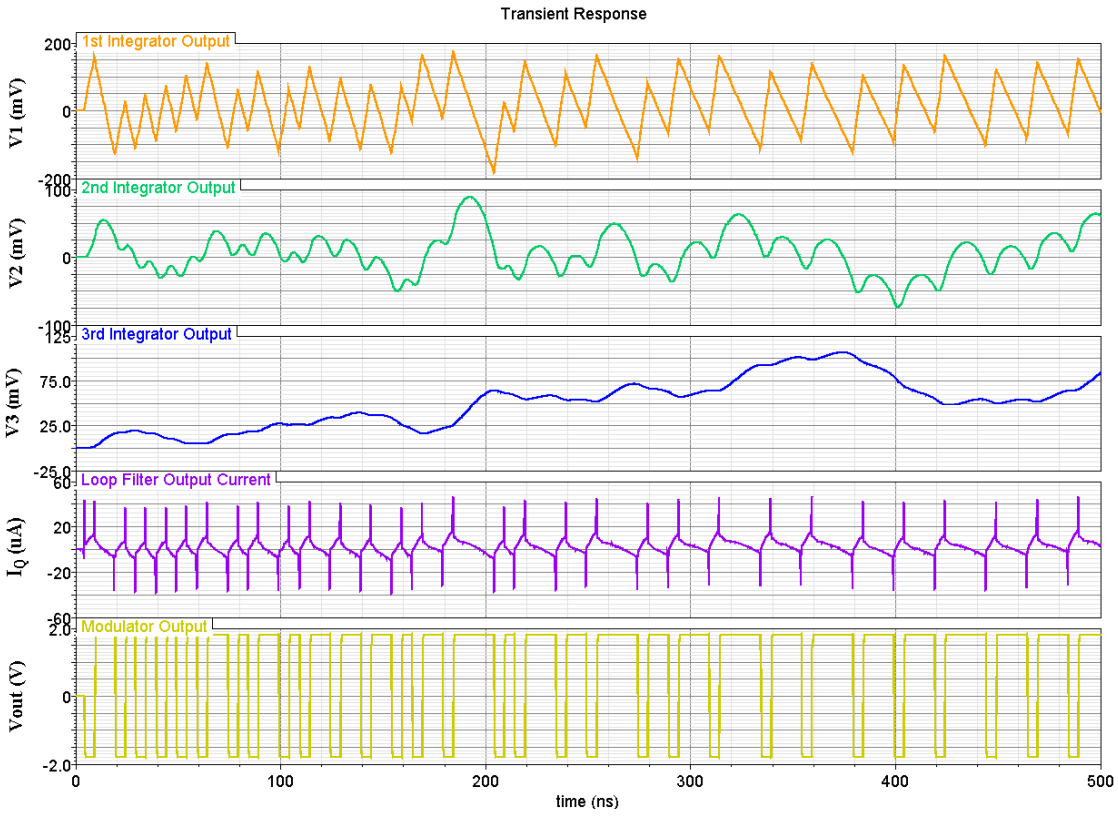

Figure 4.21 DSM Transient Simulation.

Process corner simulations were performed with slow-slow corner (NMOS slow/PMOS slow/Resistor high/Capacitor high) and fast-fast corner (NMOS fast/PMOS fast/Resistor low/Capacitor low). As shown in Figure 4.22, the typical corner simulation shows that the modulator can achieve peak SNDR of 54.1dB at -5dBFS and dynamic range of 59.6dB. The total power consumption is 4.20mW with 1.8V power supply. The FOM is 0.54pJ. The simulated performance is summarized in Table 4.11.

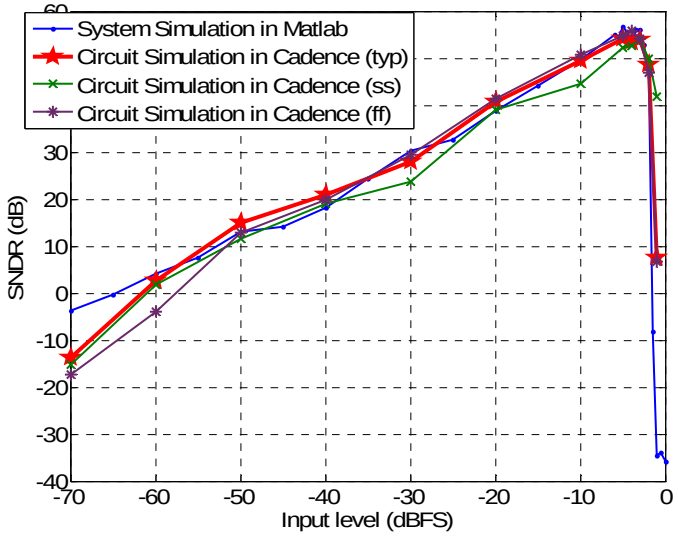

Figure 4.22 SNDR vs. Input Amplitude with Process Corner Simulation

Table 4.11 Simulated Performance Summary of the DSM with Low Frequency Input.

Dynamic Range	59.6dB
ENOB	9.6-bit
Peak SNR	54.1dB
MSA	-2dBFS
Power Consumption	Total: 4.20mW @ 1.8V
	Analog: 3.13mW
	Digital: 0.62mW
	Output buffer: 0.45mW
FOM	0.54pJ

Lastly, the performance of this work is compared with the published work listed in Table 2.4. Since the chips in bipolar process and BiCMOS process generally dissipate much more power with wide bandwidth, they are removed from the comparison. The comparison is summarized in Figure 4.23, which shows the FOM vs. bandwidth for the published works and the designed modulator with simulation. It can be seen that the

performance of this work is comparable to the others, especially for bandwidth wider than 5MHz, the FOM of the designed modulator is lower than most of them.

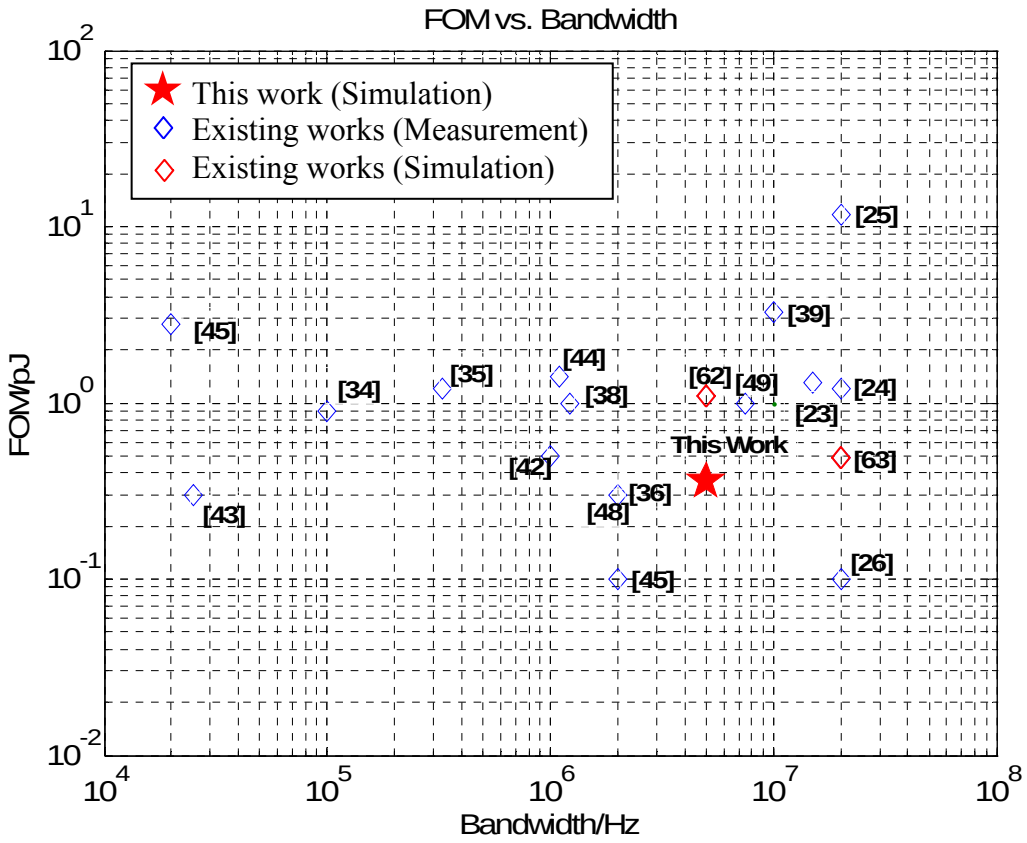

Figure 4.23 FOM vs. Bandwidth Existing Works (some are fabricated) and This Work.

The advantages and unique features of the proposed system among all the studied works are shown in Table 4.12.

Table 4.12 Advantages and Unique Features of the Proposed System

Application	This work is dedicated to ultrasound imaging.
Modulator order	Third-order is derived as the optimized order in wideband ultrasonic application.
Loop filter	A low power structure is realized by sharing several transconductors.
Transconductor	An improved linearity transconductor is proposed.

4.7 Layout Implementation

The layout of the design was implemented as shown in Figure 4.24. In order to isolate the analog circuitry from the switching digital circuits, three core power domains and two ESD power domains were implemented. There are 24 pads together with ESD protection circuits which are taken from an I/O library surrounding the core layout and each pad's purpose is summarized in Table 4.13. The core layout occupies 0.273 mm X 0.266 mm ≈ 0.073 mm^2 and the entire die (including pads) occupies 1.240 mm X 1.240 mm ≈ 1.54 mm^2.

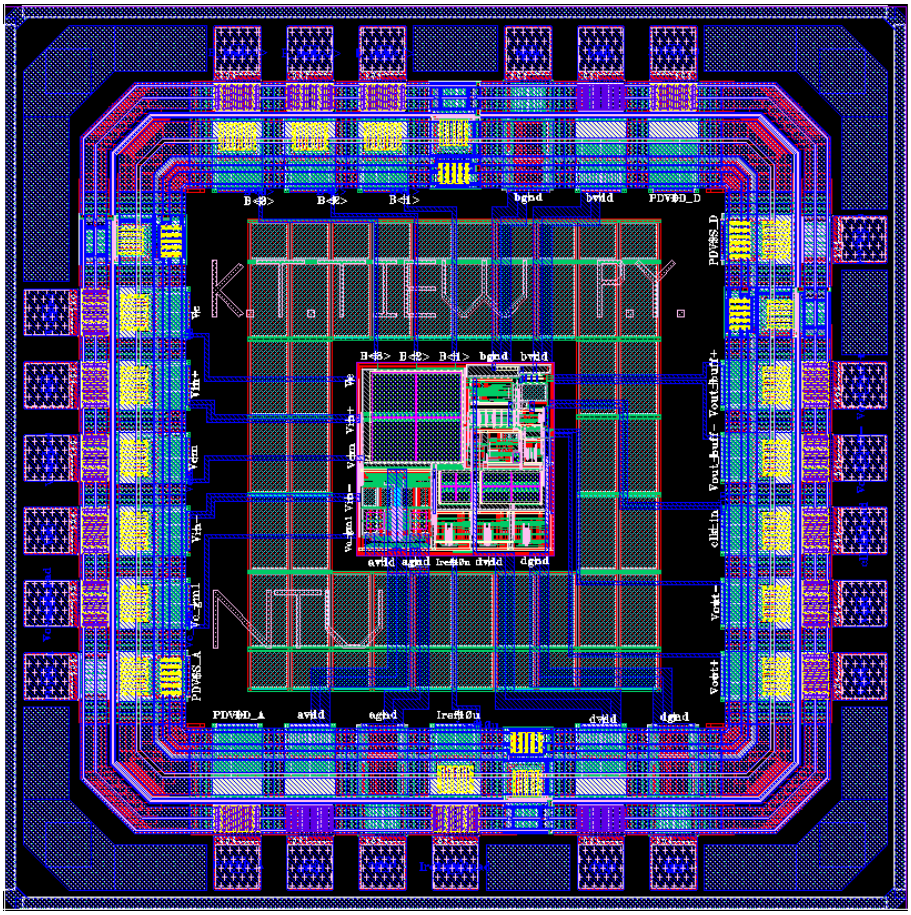

Figure 4.24 Layout of DSM.

Table 4.13 Pad Summary

Pin No.	Pad name	Pad Purpose	X-axis (um)	Y-axis (um)
1	PDVDD_A	ESD power (analog)	319.740	58.240
2	avdd	analog power	419.740	58.240
3	agnd	analog ground	519.740	58.240
4	Iref10u	reference current	619.740	58.240
5	dvdd	digital power	819.740	58.240
6	dgnd	digital ground	919.740	58.240
7	Vout+	test mux output +	1181.240	319.740
8	Vout–	test mux output –	1181.240	419.740
9	clk_in	reference clock	1181.240	519.740
10	Vout_buff–	buffer output –	1181.240	619.740
11	Vout_buff+	buffer output +	1181.240	719.740
12	PDVSS_D	ESD ground (digital)	1181.240	919.740
13	PDVDD_D	ESD power (digital)	919.740	1181.240
14	bvdd	buffer power	819.740	1181.240
15	bgnd	buffer ground	719.740	1181.240
16	B<1>	digital control bit <1>	519.740	1181.240
17	B<2>	digital control bit <2>	419.740	1181.240
18	B<3>	digital control bit <3>	319.740	1181.240
19	Vc	Gm tuning control	58.240	819.740
20	Vin+	test mux input +	58.240	719.740
21	Vcm	common mode voltage	58.240	619.740
22	Vin–	test mux input –	58.240	519.740
23	Vc_gm1	Gm1 tuning control	58.240	419.740
24	PDVSS_A	ESD ground (analog)	58.240	319.740

The core layout is shown in Figure 4.25, excluding pads and ESD protection. Block G_{m1} and integration capacitors C_a are placed on the left, where the input signal comes in. Blocks G_{m2}, G_{m3} and G_{m4} together with integration capacitors C_b and C_c are placed in sequence as in the schematic to allow the signal to flow smoother. The biasing block is placed at center since it supplies all the bias currents and voltages to other blocks. Block quantizer and block DAC are placed on the right side near the output signal. The sizes and areas occupied by various blocks are summarized in Table 4.14.

In order to prevent the switching noise to enter into the analog blocks, all the digital blocks such as clock generator and noisy blocks with switching activity such as quantizer and DAC are powered with different supply from the sensitive analog blocks. Power domains for various blocks are shown in Table 4.14.

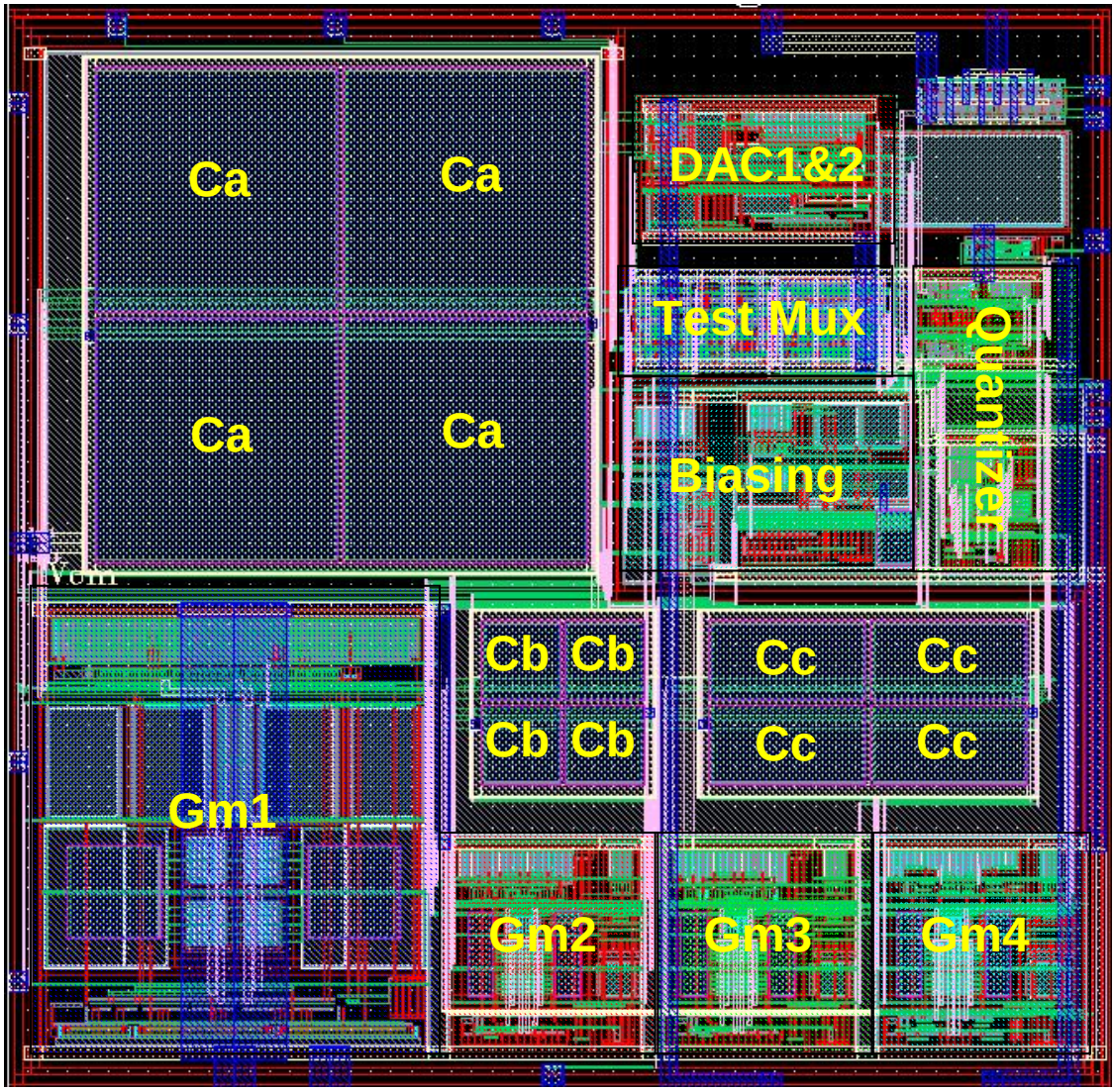

Figure 4.25 Core Layout.

Table 4.14 Layout Size and Power Domain of Various Blocks.

Block	Size (um x um)	Area (um^2)	Power Domain
G_{m1}	100 x 110	11000	Analog
G_{m2}	56 x 54	3024	Analog
G_{m3}	56 x 54	3024	Analog
G_{m4}	56 x 54	3024	Analog
C_a x 4	128 x 128	16384	N/A
C_b x 4	46 x 46	2116	N/A
C_c x 4	84 x 46	3864	N/A
DAC 1&2	64 x 36	2304	Digital
Quantizer	35 x 76	2660	Digital
Biasing	74 x 46	3404	Analog
Test Mux	64 x 24	1536	Digital

Chapter 5 Conclusions and Future Works

5.1 Conclusions

In this project, various aspects of delta-sigma modulator from system level synthesis to transistor level implementation have been reviewed and studied. Difference between discrete-time and continuous-time realization was highlighted and continuous-time modulator was chosen due to its relaxed speed requirement on the circuit. Nevertheless, continuous-time delta-sigma modulators have several drawbacks such as excess loop delay and clock jitter, which make them less popular than their counterparts. Moreover, poor device matching also makes them more sensitive to process variation. Therefore, continuous-time delta-sigma modulators are used in applications which require medium resolution and high speed, for example, a home ultrasound system.

A third-order continuous-time delta-sigma modulator was synthesized and simulated in Matlab. The modulator order and sampling frequency for optimum ultrasound signal processing was firstly determined. A discrete-time prototype was then created by using an existing toolbox and subsequently it was transformed into a continuous-time delta-sigma modulator. Extensive simulations were performed in order to ensure the stability. Various non-idealities simulations were also carried out and several important specifications for the circuit implementation were derived. After the modulator design was accomplished in system level, ultrasound signal was used to test the functionality of the modulator and a beamforming image was successfully generated with the designed

modulator. A reconfigurable modulator for dual-mode ultrasonic application was simulated and designed in system level.

The circuit blocks were implemented with CMOS 0.18μm process. The power supply used is 1.8V. Transconductors were identified as the most critical and most power hungry blocks. A transconductor with multiple outputs was employed to implement the integrator in order to reduce the power consumption and silicon area by sharing some transconductor blocks. The linearity of the transconductor was improved by reducing the effect of mobility degradation. Other circuit blocks including current input quantizer and DAC were also designed and simulated. A test multiplexer which provides eight test modes was implemented. Circuit simulations showed that with 5MHz signal bandwidth the designed modulator can achieve a dynamic range of 59.6dB, which is equivalent to 9.6-bit resolution, with 4.20mW power consumption under 1.8V supply.

5.2 Future Works

5.2.1 Implementation of Reconfigurable Modulator for Dual-Mode Ultrasonic Application

Compared to the low-pass modulator, a much higher resolution (18-bit) is required for the bandpass modulator in the CW application. A system level reconfigurable structure based on the low-pass DSM is proposed in this thesis and the transistor level implementation of the reconfigurable CT DSM could be valuable and challenging.

5.2.2 Fabricated Chip Measurement

The layout of this chip design was sent for fabrication. It would be useful to evaluate the measurement results against the circuit simulation as reported in this dissertation.

The Author's Publications

P. Song, K.-T. Tiew, Y. Lam, and L. M. Koh, "A CMOS 3.4 mW 200 MHz continuous-time delta-sigma modulator with 61.5 dB dynamic range and 5 MHz bandwidth for ultrasound application," presented at Circuits and Systems, 2007. MWSCAS 2007. 50th Midwest Symposium on, 2007.

P. Song, K.-T. Tiew, Y. Lam, and L. M. Koh, "A Reconfigurable Continuous-Time Delta-Sigma Modulator for Dual-Mode Ultrasonic Application," presented at Integrated Circuits, 2007. ISIC '07. International Symposium on, 2007.

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