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A BURST MODE OPTICAL RECEIVER FOR ETHERNET PASSIVE OPTICAL NETWORK

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Table of Content

Acknowledgments	i
Table of Content	iii
Abstract	vi
List of Figures	vii
List of Tables	x
Chapter 1	1
Introduction	1
1.1 Background	1
1.2 Motivation	5
1.3 Thesis Organization and Contribution	8
Chapter 2	11
Basics of Optical Communication.....	11
2.1 Optical Fiber.....	11
2.2 Photodiodes (Photodetectors).....	12
2.3 Data Modulation Schemes	15
2.4 Eye Diagram.....	17
2.5 BER (Bit Error Rate) and Noise.....	18
Chapter 3	21
Transimpedance Amplifier & Limiting Amplifier Theory	21
3.1 Introduction	21
3.2 TIA Design Considerations.....	22
3.2.1 Gain and Bandwidth.....	22
3.2.2 Sensitivity and Overload	24
3.2.3 Group delay.....	27
3.3 Basic Structures for TIAs.....	27
3.3.1 Common-source, Common-drain, and Common-gate TIAs.....	29
3.3.2 Current mirror TIAs	31
3.4 Advanced Structures of TIAs.....	32
3.4.1 RGC input TIAs	33
3.4.2 Hybrid TIAs	35
3.4.3 TIAs with inductors and inductive elements.....	35
3.4.4 TIAs with negative capacitance	37
3.4.5 AGC TIAs	38
3.4.6 Dual TIA core.....	40
3.5 Limiting Amplifier Design Considerations.....	42
3.5.1 Gain of LAs.....	43
3.5.2 DC Offset Cancellation.....	43
3.5.3 AC coupled and DC coupled LAs.....	46
3.5.4 LA circuit with reset.....	48
3.6 Basic Structure for LAs.....	50
3.6.1. LAs with shunt-peaking inductors or active inductors.....	50
3.6.2. Active Feedback LAs.....	51

3.6.3. LA with regulated cascode load.....	53
3.7 Advanced Structures for LAs.....	54
3.7.1 Feedback type LAs.....	54
3.7.2 Feedforward type LAs.....	57
3.7.3 LAs with internally created reset in a feedback configuration.....	60
3.8 Summary	63
Chapter 4.....	64
Design of a CMOS Burst Mode Optical Receiver with Novel Feedforward Created Reset.....	64
4.1 Introduction	64
4.2 Circuit Design Methodology.....	65
4.3 Individual Circuit Blocks	68
4.3.1 Transimpedance amplifier.....	68
4.3.2 Single-to-Differential circuit.....	71
4.3.3 Limiting Amplifiers with automatic DC offset cancellation.....	71
4.3.4 Peak detector with self-discharging function.....	73
4.3.5 Comparator.....	74
4.3.6 Buffer block.....	76
4.4 Simulation Results.....	77
4.5. Layout Design	80
4.5.1 Multiple guard rings.....	81
4.5.2 Separated V_{DD} , GND and bias block.....	82
4.5.3 New common centroid layout with interdigitated transistors	83
4.5.4 Multiple layers current path	85
4.6 Measurement.....	86
4.6.1 Test setup.....	87
4.6.2 Measurement results.....	89
4.7 Summary	93
Chapter 5.....	94
Design of a CMOS Burst Mode Optical Receiver with Automatic Gain Control & Novel Feedforward Created Reset	94
5.1 Introduction	94
5.2 Circuit Design Methodology.....	94
5.3 Individual Circuit Blocks	97
5.3.1 Differential RGC input transimpedance amplifier.....	97
5.3.2 Schmitt trigger.....	100
5.4 Simulation Results.....	101
5.5 Measurement.....	104
5.5.1 Test setup.....	105
5.5.2 Measurement results.....	105
5.6 Summary	110
Chapter 6.....	112
Conclusion and Recommendations	112
6.1 Research Work Highlights	112
6.2 Future Work	114
The Author's Publications.....	116

References 117

Abstract

The explosive growth of the internet demand high-speed data transmission due to the multimedia and telecommunication. To break the existing speed bottleneck with the traditional broadband solutions such as Digital Subscriber Line (DSL) and Community Antenna Television (CATV), Fiber-To-The-Home (FTTH) using optical fiber has been developed as a feasible solution for the Local Area Network (LAN). A popular implementation of the FTTH is the Ethernet Passive Optical Network (EPON) system.

Two versions of the circuit are designed to operate with 2.5 Gbps data for the burst mode optical receiver inside the Optical Line Terminal (OLT) in the EPON system. The second version of the circuit is an improved version of the first with an added automatic gain control block to increase the dynamic range.

The key idea in the two designs is to generate an internal *reset* signal based on the magnitude of the input signal in a feedforward configuration. A very fast response time of less than 10 ns including the reset creation time is achieved with a normal 0.18 μm CMOS technology. The novel architecture removes the bottleneck of response time in the receiver design, and makes optical receiver circuits operating with 40 Gbps burst mode data feasible with an internally created *reset* signal.

List of Figures

Figure 1.1: The world internet usage growth with reference to year 2000	1
Figure 1.2: The proportion of FTTH in broadband services in Japan	2
Figure 1.3: EPON system including ONUs and an OLT	4
Figure 1.4: (a) Transmitter inside an OLT and (b) receiver inside an OLT	5
Figure 2.1: One multimode Optical fiber with two optical signal paths	12
Figure 2.2: The structure of p-i-n photodiode	13
Figure 2.3: The structure of avalanche photodiode	14
Figure 2.4: The equivalent model for photodiode for use in simulation	14
Figure 2.5: Different modulation schemes: (a) NRZ, (b) RZ and (c) PAM-4	15
Figure 2.6: Continuous mode and burst mode data	17
Figure 2.7: Formation of an eye diagram	18
Figure 2.8: Noise distribution spectrum relating BER	19
Figure 3.1: Block diagram of a conventional optical receiver	21
Figure 3.2: Optical receiver TIA stage	23
Figure 3.3: BER vs. BW/Data_rate for NRZ data	24
Figure 3.4: Optical receiver TIA stage with noise analysis	25
Figure 3.5: BER vs. the optical power	26
Figure 3.6: (a) Low-impedance, High-impedance and (b) Transimpedance front-end ..	27
Figure 3.7: (a) Common-source, (b) Common-drain and (c) Common-gate TIAs	30
Figure 3.8: Current mirror TIA	32
Figure 3.9: RGC input TIA	33
Figure 3.10: A Pseudo Differential RGC input TIA	34
Figure 3.11: TIA with inductors to enhance the bandwidth	36
Figure 3.12: Lumped element models of an on-chip inductor	36
Figure 3.13: Active inductor to enhance the bandwidth	37
Figure 3.14: TIA with negative capacitance	38
Figure 3.15: Automatic Gain Control TIA	39
Figure 3.16: Resistor tree (a) transistor and fixed value resistor and (b) transistor acting as switches	40
Figure 3.17: (a) Dual TIA circuit and (b) Increased dynamic range	41
Figure 3.18: DC transfer function of (a) an LA and (b) an VGA	42
Figure 3.19: Asymmetrical DC levels at the final outputs	44
Figure 3.20: A continuous mode LA with DC offset cancellation circuit	45
Figure 3.21: (a) AC coupled LA and (b) Average power for the continuous mode and burst mode data	46
Figure 3.22: (a) AC coupled LA with hysteretic comparator and (b) waveforms at different nodes	47
Figure 3.23: DC coupled Limiting Amplifier for burst mode data	48
Figure 3.24: Reset signal with the burst mode data	49
Figure 3.25: LA (a) without peaking inductors and (b) with peaking inductors	51
Figure 3.26: Block diagram of an active feedback LA	52
Figure 3.27: Schematic diagram of an active feedback LA	52
Figure 3.28: A simplified LA with regulated cascode load	53

Figure 3.29: LA with DC offset compensation in a feedback configuration.....	55
Figure 3.30: Simplified Crain Limiting Amplifier.....	56
Figure 3.31: Top level detector circuit structure.....	56
Figure 3.32: (a) Burst mode optical receiver with a dynamic bias voltage and (b) Bias voltage creation based on the input data.....	58
Figure 3.33: Four-input-pin LA	58
Figure 3.34: (a) Feedforward optical receiver with a external <i>reset</i> and (b) waveforms at different nodes.....	59
Figure 3.35: Burst mode LA with internal <i>reset</i> in the feedback path.....	60
Figure 3.36: Reset-creation circuit (a) block diagram and (b) operating principle.....	61
Figure 3.37: Self Discharging Bottom level detector	62
Figure 4.1: Block diagram of the proposed burst mode optical receiver.....	65
Figure 4.2: Waveforms at different nodes in the circuit	66
Figure 4.3: Feedforward-reset creation operation.....	66
Figure 4.4: Feedforward created <i>reset</i> signal with low to high power burst	67
Figure 4.5: Feedforward created <i>reset</i> signal with high to low power burst	68
Figure 4.6: Schematic diagram of the regulated cascode input TIA.....	70
Figure 4.7: Schematic diagram of the S2D.....	71
Figure 4.8: Schematic diagram of an LA with automatic DC offset cancellation	72
Figure 4.9: Schematic diagram of the peak detector.....	74
Figure 4.10: Schematic diagram of the comparator.....	75
Figure 4.11: Schematic diagram of the buffer	76
Figure 4.12: Input referred noise spectrum.....	77
Figure 4.13: Transient response at optical input current of 12.8 μA peak-to-peak with 2^7 -1 random data and reset creation.....	78
Figure 4.14: Internally created <i>reset</i> with high power input followed by low power input	78
Figure 4.15: Internally created <i>reset</i> with low power input followed by high power input	79
Figure 4.16: The eye diagram at optical input current of 12.8 μA peak-to-peak using random data	79
Figure 4.17: The eye diagram at optical input current of 80 μA peak-to-peak using random data	80
Figure 4.18: Multiple guard rings to achieve isolations.....	81
Figure 4.19: Separated power planes on the chip	82
Figure 4.20: Separated bias circuit blocks on the chip	82
Figure 4.21: Conventional common centroid layout: (a) Cross-coupled pair pattern and (b) Interdigitate pattern	84
Figure 4.22: New interdigitate pattern in a stack manner	84
Figure 4.23: New interdigitate pattern in a cross-coupled pair manner.....	85
Figure 4.24: (a) Limited width for the metal and (b) current path in the metal layers in the cross section	86
Figure 4.25: Chip photograph with test probes.....	87
Figure 4.26: The overall measurement setup.....	87
Figure 4.27: The schematic diagram and the PCB view of the conversion circuit.....	88
Figure 4.28: The photo of the probe station.....	88

Figure 4.29: Outputs to verify the functionality of the <i>reset</i> signal.....	89
Figure 4.30: Outputs at the start of burst for the input current of 50 μA peak-to-peak	90
Figure 4.31: Outputs at the steady state of burst for the input current of 50 μA peak-to-peak	90
Figure 4.32: Outputs at the start of burst for the input current of 500 μA peak-to-peak ..	91
Figure 4.33: Outputs at the steady state of burst for the input current of 500 μA peak-to-peak	91
Figure 4.34: Integrated output noise using the standard deviation from the histogram ...	92
Figure 5.1: Block diagram of the proposed burst mode optical receiver.....	95
Figure 5.2: (a) Waveforms at different nodes in the circuit and (b) Feedforward-reset creation operation	95
Figure 5.3: Feedforward created <i>reset</i> and <i>Gain_ctl</i> signals with low to high power burst	96
Figure 5.4: Feedforward created <i>reset</i> and <i>Gain_ctl</i> signal with high to low power burst	97
Figure 5.5: Schematic diagram of differential regulated cascode input TIA.....	99
Figure 5.6: (a) Schematic diagram and (b) the transfer characteristics of the Schmitt trigger	100
Figure 5.7: Input referred noise spectrum.....	101
Figure 5.8: Transient response at optical input current of 12.8 μA using 2^7 -1 random data and reset creation	102
Figure 5.9: Internal <i>reset</i> and <i>Gain_ctl</i> signals with high power input followed by low power input.....	102
Figure 5.10: Internal <i>reset</i> and <i>Gain_ctl</i> signals with low power input followed by high power input.....	103
Figure 5.11: The eye diagram at optical input current of 12.8 μA peak-to-peak using random data	103
Figure 5.12: The eye diagram at optical input current of 600 μA peak-to-peak using random data	104
Figure 5.13: Chip photograph with test probes.....	104
Figure 5.14: Outputs to verify the functionality of the <i>reset</i> signal.....	106
Figure 5.15: Outputs at the start of burst for the input current of 25 μA peak-to-peak ..	106
Figure 5.16: Outputs at the steady state of burst for the input current of 25 μA peak-to-peak	107
Figure 5.17: Outputs at the start of burst for the input current of 500 μA peak-to-peak	107
Figure 5.18: Outputs at the steady state of burst for the input current of 500 μA peak-to-peak	108
Figure 5.19: Outputs at the start of burst for the input current of 1600 μA peak-to-peak	108
Figure 5.20: Outputs at the steady state of burst for the input current of 1600 μA peak-to-peak	109
Figure 5.21: Integrated output noise using the standard deviation from the histogram .	109

List of Tables

Table 1.1:	1000BASE-PX20-U receiver characteristics	6
Table 1.2:	10GBASE-L receiver characteristics	6
Table 1.3:	Desired receiver circuit specification	6
Table 1.4:	Allowable time to create the reset signal.....	8
Table 2.1:	2B/4B code table	16
Table 2.2:	Numerical relationship between Q and BER.....	20
Table 6.1:	Performance summary of the completed designs	114

Chapter 1

Introduction

1.1 Background

Data traffic is growing fast over the decades, especially in recent years. The number of internet users worldwide has also increased by 300% from the year 2000 to 2008 [1]. The continuous growth of internet traffic demands higher data transfer rates. However, the bottleneck of the speed-limiting factor lies in the first mile network in the Local Area Network (LAN) [2]. Ethernet is evolving in response to the demand for communication at higher speed.

Figure 1.1: The world internet usage growth with reference to year 2000

There are three widely deployed broadband solutions: Digital Subscriber Line (DSL), Community Antenna Television (CATV), and Fiber-To-The-Home (FTTH). The first two solutions are built using twisted pair line and hybrid fiber coax cable respectively, and they face speed-limiting problems as they are not originally designed for broadband services. With the rapidly increasing bandwidth requirements from services including video conference and high-speed internet, the first two solutions are no longer the best choices. The FTTH has been developed with the optical fiber and provides a good solution to enhance the speed beyond Giga-bit-per-second (Gbps) data rate. It dominates the growth in broadband services in Japan as suggested in Fig. 1.2 [3].

Figure 1.2: The proportion of FTTH in broadband services in Japan

One of the popular implementations of the FTTH is the Ethernet Passive Optical Network (EPON) system, as it provides promising options with several advantages such

as high speed, low cost, easy implementation and maintenance. A general EPON system covering 20 km range is shown in Fig. 1.3. It consists of several Optical Network Units (ONUs), an Optical Line Terminal (OLT), a passive optical splitter, and several optical fibers.

The EPON system has a star network configuration: one OLT is attached to several ONUs in a point to multiple-point network. The OLT and ONUs communicate through the optical fiber and the passive optical splitter, where two data paths exist: one is the upstream data path and the other is the downstream data path. The data in the two paths are multiplexed using two different optical wavelengths: 1.31 μm for the upstream data path and 1.49 μm for the downstream data path. For the downstream data path, the data is transmitted continuously from the OLT to the ONUs in a broadcasting mode, and each ONU will recognize its own data and receive it. On the other hand, for the upstream data path, there are multiple sources of data from different ONUs to be received by the only OLT. To avoid data collisions at the OLT, the data is arranged using the Time Division Multiple Access (TDMA) technique: each ONU is allocated a time slot to transmit data to the OLT, so the data from the different ONU will arrive at the OLT one at a time in burst mode. Because the distance from each ONU to the OLT varies, the data power level also varies, and this puts a challenging requirement on the optical receiver for the OLT: it has to have high sensitivity and wide dynamic range. To increase the channel efficiency, a short response time is required to handle the burst mode data.

Figure 1.3: EPON system including ONUs and an OLT

Both ONU and OLT have built-in transmitters and receivers to accommodate the 2-ways communications through the optical fiber. The block diagram of the OLT is as shown in Fig. 1.4. It consists of a transmitter indicated in Fig 1.4 (a) and a receiver indicated in Fig. 1.4 (b). The transmitter has two photodiodes: one is to generate optical signal and the other is to monitor the output optical signal magnitude through a power control circuit block in the analog front end. The data is re-timed through the Multiplexer, the re-timer, the Phase Lock loop (PLL), and the divider block. The re-timed data is sent to the laser driver to generate the optical signal. The receiver part has only one photodiode acting as the photodetector, Transimpedance Amplifier (TIA), Main Amplifier (MA), Clock and Data Recovery circuit (CDR), and Demultiplexer (DEMUX) block. The process in the receiver is a reverse process of that in the transmitter and the detailed analysis of the analog part is given in section 3.1.

Figure 1.4: (a) Transmitter inside an OLT and (b) receiver inside an OLT

1.2 Motivation

The Institute of Electrical and Electronics Engineers (IEEE) keeps on developing standards for EPON for data rates that are increasing rapidly over the years. For the bit rate of 1.25 Gbps and 10 Gbps, IEEE802.3 1000BASE-PX20-U and 10GBASE-L specifications are developed as shown in Table 1.1 and Table 1.2 [4]. Different specifications for the optical receiver are defined inside the tables such as Bit Error Rate (BER), receive sensitivity, maximum receive power, and response time. Based on the study of the two specifications, a target specification for 2.5 Gbps is proposed as shown in Table 1.3.

Table 1.1: 1000BASE-PX20-U receiver characteristics

Description	1000BASE-PX-U	Unit
Bit rates	1.25	Gbps
BER rate	10^{-12}	
Centre wavelength range	1260-1355	nm
Maximum receive power	-3	dBm
Receive sensitivity	-24	dBm
Response time	400	ns

Table 1.2: 10GBASE-L receiver characteristics

Description	10GBASE-L	Unit
Bit rates	10	Gbps
BER rate	10^{-12}	
Centre wavelength range	1260-1355	nm
Maximum receive power	0.5	dBm
Receive sensitivity	-14.4	dBm
Response time	51.2	ns

Table 1.3: Desired receiver circuit specification

Description	Mine	Unit
Bit rates	2.5	Gbps
BER rate	10^{-12}	
Centre wavelength range	1260-1355	nm
Maximum receive power	-1	dBm
Receive sensitivity	-21	dBm
Response time	10	ns

The Bit Error Rate (BER) is an ultimate requirement for optical receiver and will be further explained in section 2.5. It sets the sensitivity as well as the maximum receiver

power of the optical receiver. A high sensitivity is desired as the optical receiver can pick up a very low power signal, and discriminate the signal from the noise.

High dynamic range is required because the input signal varies in power due to the different dispersions in the fiber channel and different distances the signal travels. To boost the dynamic range, automatic gain control blocks are often adopted [5-12]. In addition, to achieve a broad bandwidth performance with relatively high gain, the use of regulated cascode input transimpedance amplifier (TIA) is explored in the burst mode optical receiver for EPON systems.

CMOS technologies are chosen in this project as they permit the integration of a huge amount of transistors. Furthermore, the deep-submicron CMOS process has similar high frequency performance as their bipolar counterpart. It is possible to achieve an integration of the high-speed analog circuit with the digital core onto one die at a considerably low cost.

Fast response, defined as within the first 512 bits of the data, is one of the top priorities in the design considerations for the burst mode optical receiver inside the OLT. The incoming data at the OLT is in the burst mode, so fast response will ensure a rapid establishment for the slicing level of the input data. An external *reset* signal would initialize all the biasing conditions inside the circuit as well as instantaneously storing the peaking values from the peak detector blocks. However, this will increase the system complexity with the addition of the external *reset* signal. Therefore, there is a design trend to remove this external *reset* signal by creating the *reset* signal internally from the dummy data at the very beginning of the input data packet. Existing architecture has been developed with an internally created reset signal in the feedback configuration, and a

response time of 100 ns has been achieved. However, when the data rate is increased from 1.25 Gbps to 10 Gbps upto 40 Gbps, the allowable time to create the reset signal, equivalent to 512 bits of data, is decreased from about 400 ns to 51.2 ns down to 12.8 ns respectively as shown in Table 1.4. On the other hand, the response time of existing architecture does not scale down proportionally with increased data rate, hence there is a strong need to propose new circuit architecture to reduce the response time to meet the demand for higher bit rate of 10 Gbps or even of 40 Gbps.

Table 1.4: Allowable time to create the reset signal

Bit rate (Gbps)	1.25	2.5	10	40
Equivalent time (ns)	400	204.8	51.2	12.8

1.3 Thesis Organization and Contribution

This thesis consists of six chapters:

Chapter 1 gives a basic introduction to the background of the work, followed by the motivation of this research. Next, an overview of the fiber optical communication system is presented in brief, followed by the organization of the thesis and contribution from this work as given at the end of the chapter.

Chapter 2 covers the basic of the optical communication. The objective of this chapter is to give the reader a detailed view of the components and methodologies adopted in EPON systems. The structures of the laser fiber and photodetector described in Chapter 1.1 are then studied. Next, the data modulation scheme and coding scheme in EPON systems are explained. Finally, the formation of the eye diagram and the relationship

between the BER and the noise are explored to evaluate the performance of optical receiver circuits presented in Chapter 4 and Chapter 5 qualitatively and quantitatively.

Chapter 3 presents the theory of the transimpedance amplifier and the limiting amplifier inside the burst mode optical receiver. A detailed literature review is also included for the state-of-the-art works. The design considerations of the Transimpedance Amplifier (TIA) are introduced, followed by a study of the basic structures of the TIA. To achieve the goal to boost the bandwidth, gain and other design considerations, advance structures for the TIA are presented and analyzed. After the TIA section, the design considerations for the LA are first presented, and the advanced structures of the LA are then analyzed and discussed, with the motivation to achieve fast response and other design considerations.

Chapter 4 describes a 2.5 Gbps burst mode optical receiver with a novel feedforward created reset for EPON Systems. By creating an internal *reset* signal in a feedforward configuration, the circuit fabricated in a 0.18 μm CMOS technology achieves a fast response time of less than 10 ns including the reset creation time. When measured with peak-to-peak input currents of 50 μA and 500 μA respectively, the total response time is less than 10 ns with a single-ended output swing of about 300 mV for both cases. The measured input referred noise is less than 0.79 μA_{rms} corresponding to a sensitivity current of 5.53 μA_{rms} . The chip occupies an area of 1500 $\mu\text{m} \times 650 \mu\text{m}$ and consumes 198 mW from a 1.8 V supply. This contribution designed totally in integrated circuit makes system design more flexible by having avoided the use of an external *reset* signal.

Chapter 5 presents a 2.5 Gbps burst mode optical receiver with automatic gain control and a novel feedforward created reset for EPON systems. It is an improved version of the

circuit in Chapter 4. An automatic gain control block is added to increase the dynamic range of the circuit. When measured with peak-to-peak input currents of 25 μA and 1600 μA respectively, the total response time is less than 10 ns with a single-ended output swing of about 300 mV. The measured input referred noise is less than 0.97 μA_{rms} corresponding to a sensitivity current of 6.79 μA_{rms} . The power consumption of the chip is 189 mW from a 1.8 V supply with an area of $1400 \mu\text{m} \times 550 \mu\text{m}$.

Chapter 6 covers the contributions of this thesis and suggestions for future research.

Chapter 2

Basics of Optical Communication

Optical transmitters, receivers and fibers are the three common modules inside the optical communication channel. The optical transmitter consists of a laser diode driven by a high performance laser driver circuit, whereas the optical receiver generally consists of a photodiode followed by an amplifying circuit. As for the optical fiber, it provides transmission paths for optical signals to travel. A simple structure of the optical fiber will be introduced. Different types of photodiodes will be further studied. In addition, an optical receiver will be presented at a system level. Different data modulation schemes will be introduced. The relationship between the noise and Bit Error Rate (BER) is investigated.

2.1 Optical Fiber

Optical fiber did not come to practical use until a scientific team at the Corning Glass Works first developed an optical fiber which has signal attenuation below 20dB/km at a low cost in 1970. The fiber core is surrounded by a cladding that has a lower refractive index compared with the core as shown in Fig. 2.1. Therefore the light would be confined in the fiber core by the internal reflection. Optical signals traveling in the optical fiber experience different types of dispersions: modal dispersion, chromatic dispersion, and polarization mode dispersion. An example of the modal dispersion is shown in a multimode fiber in Fig. 2.1. The optical signals have multimode (multi paths) to

propagate through the optical fiber with the same speed, hence the difference in the lengths of paths (fast and slow) causes the dispersion. Considering the effects from all other dispersions within the same optical fiber as well as the impacts of different optical fibers, the accumulated differences between received signals would be increased significantly. This is the reason for the challenging requirements for the optical receiver at the end user side such as the OLT of the EPON system.

Figure 2.1: One multimode Optical fiber with two optical signal paths

2.2 Photodiodes (Photodetectors)

The first device seen by the optical data coming from the optical fiber is the photodiode (photodetector). Therefore, its characteristics will have a great impact on the overall optical receiver performance. The photodiodes are generally divided into two categories: the p-i-n photodiode, and the avalanche photodiode.

The p-i-n photodiode has a simpler structure of the two. The structure of the p-i-n photodiode is shown in Fig. 2.2. It consists of three layers as indicated from the top to the bottom: the “p” region formed by p-doped material, the “i” region which is an intrinsic semiconductor material layer, and the “n” region formed by n-doped material. By reverse biasing the PN junction and depleting the intrinsic region, a strong electric field is established inside the intrinsic semiconductor material, where electron-hole pairs are created by photons to form photocurrent. The width of the intrinsic semiconductor material layer W , determined by the manufactory, controls a trade-off between the chance a photon is absorbed and the speed of the detector. The p-i-n is relatively low cost due to the simple structure but suffers from a slow response due to the drift component in the photocurrent.

Figure 2.2: The structure of p-i-n photodiode

The avalanche photodiode has a similar structure compared with the p-i-n photodiode as shown in Fig. 2.3. However, the avalanche photodiode has an additional multiplication layer, which will increase the number of electron-hole pairs significantly

through avalanche multiplication. Therefore the sensitivity of the avalanche photodiode is generally larger than that of the p-i-n photodiode.

Figure 2.3: The structure of avalanche photodiode

Generally, a photodiode could be modeled as a current source with a few circuit components for use in the circuit simulation as shown in Fig. 2.4 [13]. The capacitors and resistors are used to model the effect of parasitic capacitance and resistance of the photodiode, the bonding wires, and the non-ideal contacts.

Figure 2.4: The equivalent model for photodiode for use in simulation

2.3 Data Modulation Schemes

Three common data modulation schemes in the optical communication are the Non-Return-to-Zero (NRZ) format, the Return-to-Zero (RZ) format, and the Pulse Amplitude Modulation-4 (PAM-4) format as shown in Fig. 2.5.

Figure 2.5: Different modulation schemes: (a) NRZ, (b) RZ and (c) PAM-4

Two levels of digital signals are used to present bit “1” and “0” in the NRZ format and the duration of pulses presenting the bit occupies the entire bit period as shown in Fig. 2.5(a). RZ format also adopts two levels of digital signals but the duration of the pulses presenting the bit occupies only a fraction of the bit period as shown in Fig. 2.5 (b), so it requires wider bandwidth but lower signal-to-noise ratio compared with NRZ format. On the other hand, PAM-4 encodes two successive bits with one of four levels of digital signals, so it requires narrower bandwidth but higher signal-to-noise ratio as compared with NRZ format. As a result, NRZ format makes a compromise between the signal-to-noise ratio and the bandwidth.

Block coding is often used in EPON systems. A group of bits is replaced by another group of bits with two more bits to achieve a 50% of bit “1” density, so a DC balance is achieved. In addition, the maximum number of successive identical bits is also limited. Taking the 2B/4B code as an example, two more bits are added into the 2 bits to form a new 4-bit data as shown in Table 2.1, with the added bits underlined and in bold. Upon observation, it is seen that a 50% of bit “1” density is achieved. The 8B/10B code is widely used in EPON systems. For such coding, the original bits are grouped in 8 bits, with the first 5 bits encoded into a 6-bit group while the last 3 bits encoded into a 4-bit group.

Table 2.1: 2B/4B code table

2B group			4B group			
0	0		0	<u>1</u>	0	<u>1</u>
1	0		1	<u>0</u>	0	<u>1</u>
0	1		0	<u>1</u>	1	<u>0</u>
1	1		1	<u>0</u>	1	<u>0</u>

There are two transmission modes for the data in the optical communication. One is the continuous mode and the other is the burst mode. For continuous mode data, the bits are transmitted continuously and normally DC balanced, which is suitable for AC coupling. For burst mode data, the bits are transmitted burst by burst, and the DC level is not balanced, hence DC coupling is normally used.

Figure 2.6: Continuous mode and burst mode data

2.4 Eye Diagram

The eye diagram is an intuitive graphical way to present the integrity of electrical and optical communication signals. The quality of the signals (noise) can be predicted from the appearance of the eye diagram.

To form an eye diagram for NRZ data, the waveform is first cut into two-bit segments: half a bit on the left, a full bit in the center, and half a bit on the right. In all, there are eight distinct types of segments corresponding to the three-bit binary words: 000, 000, 001, 010, 011, 100, 101, 110, and 111, and an eye diagram is formed when all of them are superimposed as shown on the right hand side of Figure 2.7. The wider the eye opens, the higher the chance of a correct data received when the signal is sampled at the middle of the eye.

Figure 2.7: Formation of an eye diagram

2.5 BER (Bit Error Rate) and Noise

The relationship between the Bit Error Rate (BER) and noise is explored. The signal with the noise and the corresponding noise statistics is presented in Fig. 2.8: the signal has a peak-to-peak value V_s^{pp} while the noise has an rms value V_n^{rms} , and the noise is assumed to be Gaussian distributed. The BER is expressed in having the probability of “1”, $P(1)$, probability of “0”, $P(0)$, and the conditional probabilities of error $P(1 | 0)$ and $P(0 | 1)$ indicated by Equation (2.1).

$$BER = P(1|0) \cdot P(0) + P(0|1) \cdot P(1) \quad (2.1)$$

As seen from the Fig. 2.8, the probabilities of $P(1)$ and $P(0)$ are equal with a value of 0.5, and the conditional probabilities of error $P(1 | 0)$ and $P(0 | 1)$ are equal due to symmetry, the Equation (2.1) can be simplified to Equation (2.2) and Equation (2.3) as follows

$$BER = P(1|0) \cdot 0.5 + P(0|1) \cdot 0.5 \quad (2.2)$$

$$BER = P(1|0) \quad (2.3)$$

With the Q factor defined as the signal voltage V_s^{pp} over twice of the noise voltage V_n^{rms} in Equation (2.4), BER can be related to the noise through the Q factor.

$$BER = \frac{1}{\sqrt{2\pi}} \int_Q^\infty e^{-\frac{x^2}{2}} dx = \frac{1}{2} \operatorname{erfc} \left(\frac{Q}{\sqrt{2}} \right) \approx \frac{1}{\sqrt{2\pi}} \cdot \frac{\exp \left(-\frac{Q^2}{2} \right)}{Q}$$

$$\text{with } Q = \frac{V_s^{pp}}{2 \cdot V_n^{rms}} \quad (2.4)$$

Figure 2.8: Noise distribution spectrum relating BER

The numerical relationship between the Q factor and BER is given in Table 2.2. It is obvious that to achieve a BER of 10^{-12} , the Q factor is required to be 7 and this value is used throughout the thesis.

Table 2.2: Numerical relationship between Q and BER

Q	BER
3.090	1.00E-03
3.719	1.00E-04
4.265	1.00E-05
4.753	1.00E-06
5.199	1.00E-07
5.612	1.00E-08
5.998	1.00E-09
6.361	1.00E-10
6.706	1.00E-11
7.035	1.00E-12
7.349	1.00E-13
7.651	1.00E-14
7.942	1.00E-15

Chapter 3

Transimpedance Amplifier & Limiting Amplifier Theory

3.1 Introduction

A simplified block diagram of a general optical receiver for the analog front-end is shown in Fig. 3.1. Photocurrent generated from the photodiode is converted into a voltage signal by the Transimpedance Amplifier (TIA), and is further amplified by the Main Amplifier (MA). The MA usually employs the Variable Gain Amplifier (VGA) or the Limiting Amplifier (LA) (the LA is adopted in our design). Finally, the Clock and Data Recovery (CDR) circuit will extract the timing information for synchronous operation and enhance the circuit performance. Our design will focus on the TIA and LA.

Figure 3.1: Block diagram of a conventional optical receiver

Generally the voltage signal arriving at the input of the LA is a single-ended signal because of the unipolar nature of the light source. In most cases, it requires a single to differential conversion for the signal to be processed differentially in the later stages. To obtain an accurate bias voltage in the single-to-differential conversion, a dynamic bias voltage is essential especially for the burst mode data which varies in power from burst to burst.

3.2 TIA Design Considerations

The first block connecting from the photodiode with a large parasitic capacitance is the transimpedance amplifier. This is a crucial circuit block as it determines most if not all of the circuit performance parameters such as gain, bandwidth, and noise. The individual circuit design considerations will be discussed in details in the following sections.

3.2.1 Gain and Bandwidth

A conventional shunt-feedback transimpedance amplifier is shown in Fig. 3.2 [14-16]. The photodiode is connected to the input of a transimpedance amplifier, which has a feedback resistor R_f . The current from the photodiode flows into R_f , and the amplifier output responds in such a way that the input of the amplifier remains at virtual ground.

The gain and bandwidth of a transimpedance amplifier is given in Equation (3.1)-(3.3). The bandwidth ω_{BW} is determined by the gain of the amplifier, the feedback resistor R_f , and the total capacitance C_T , which includes the photodiode capacitance C_{diode} and input capacitance C_{inA} at the input of the transimpedance amplifier. In the early years, C_{inA} is comparable with C_{diode} . As the transistors are scaled down, C_{inA} is reduced rapidly and C_{diode} dominates the value of C_T .

Figure 3.2: Optical receiver TIA stage

$$Z_T = -R_f \cdot \frac{1}{1 + s \cdot \frac{R_f C_T}{A + 1}} \quad (3.1)$$

$$C_T = C_{diode} + C_{inA} \quad (3.2)$$

$$\omega_{BW} = \frac{A + 1}{R_f C_T} \quad (3.3)$$

There is a trade-off between the gain and the bandwidth of the transimpedance amplifier. It is desirable to increase the gain to enlarge the signal for a better signal detection ability but at the expense of sacrificing the bandwidth. A larger bandwidth will generally handle the signal with a faster bit rate. However, it would pick up much more high frequency noise if the bandwidth is much larger than the bit rate and hence reduce the Signal-to-Noise Ratio (SNR). On the other hand, if the bandwidth is too small as compared with the bit rate, signal distortion such as Inter-Symbol-Interference (ISI) will appear.

As a rule of thumb, there is an optimized bandwidth ω_{BW} for the receiver, which is about 2/3 of bit rate as a compromise between ISI and high frequency noise indicated by Equation (3.4), where B is the bit rate [17]. When the bandwidth is smaller than the 2/3 of the bit rate, the ISI effect will dominate the circuit performance, indicated by the left portion of the curve as shown in Fig. 3.3; when the bandwidth is bigger than the 2/3 of the bit rate, high frequency noise will dominate the circuit performance, indicated by the right portion of the curve.

$$\omega_{BW} \approx \frac{2}{3} \cdot B \quad (3.4)$$

Figure 3.3: BER vs. BW/Data_rate for NRZ data

3.2.2 Sensitivity and Overload

The input referred noise for the TIA as shown in Fig. 3.4 is determined by Equation (3.5), and the sensitivity of the optical receiver is determined by Equation (3.6)-(3.8). g_m is the transconductance of the input transistor, Q is the Q factor, ρ is the responsivity of

the photodiode, $P_sensitivity$ is the sensitivity power of the TIA, and $I_sensitivity$ is the sensitivity current of the TIA. An observation is made that, to achieve a low input referred noise, a small total capacitance or a big feedback resistor R_f is required. However, a big feedback resistor R_f will result in a narrower bandwidth. So there is a trade-off between the bandwidth and the input referred noise.

$$\overline{di_{equ,in}^2}(\omega) \approx \frac{8}{3} \cdot \frac{kT \cdot \omega^2 \cdot C_T^2}{g_m} + 4 \frac{kT}{R_f} \quad (3.5)$$

$$i_n^{rms} = \sqrt{\int_0^{>2 BW} i_{equ,in}^2 df} \quad (3.6)$$

$$P_sensitivity = 10 \cdot \log \left(\frac{Q \cdot i_n^{rms}}{\rho} \cdot 1000 \right) dBm \quad (3.7)$$

$$I_sensitivity = Q \cdot i_n^{rms} \quad (3.8)$$

Figure 3.4: Optical receiver TIA stage with noise analysis

The optimum values for the g_m , the input capacitance C_{inA} , and photodiode capacitance C_{diode} are intensively studied for the best noise performance. The input

capacitance C_{inA} must fall in a range comparable with C_{diode} as shown in Equation (3.9) [15, 16]. A further study suggests that a fixed ratio between C_{inA} and C_{diode} can be found for the best noise performance in [18].

$$0.2C_{diode} < C_{in} < 2C_{diode} \quad (3.9)$$

The performance of the TIA is characterized by plotting the BER as a function of the received power as shown in Fig. 3.5 [17]. When the input signal is too weak, the optical receiver fails to restore the data so the BER will become worse. On the other hand, when the input signal is too strong, the optical receiver is overloaded and the output is distorted, again the BER will become worse. For a given BER requirement, there will be two limits corresponding to the sensitivity and the overload of the optical receiver, and the difference of the two limits is the dynamic range.

Figure 3.5: BER vs. the optical power

3.2.3 Group delay

Another parameter to evaluate the TIA performance is the group delay, which is defined in Equation (3.10). ϕ is the phase of the TIA. To measure the phase linearity of the TIA, a common method is employed to find the variation of the group delay with frequency. A typical value for group delay variation $\Delta\tau$ is less than $\pm 10\%$ of the bit period for good phase linearity.

$$\tau(\omega) = -d\phi/d\omega \quad (3.10)$$

3.3 Basic Structures for TIAs

There are two other circuit topologies used in the analog front-end besides the transimpedance amplifier, namely, low-impedance front-end and high-impedance front-end as shown in Fig. 3.6(a) [19].

Figure 3.6: (a) Low-impedance, High-impedance and (b) Transimpedance front-end

Both the low-impedance and high-impedance front-ends have the same circuit structure: one pin of the photodiode is connected to the ground through a resistor while the other pin of the photodiode is connected to a bias voltage V_{bias} . When the photodiode current passes through the resistor, a voltage signal will be generated and taken as the output. The difference between the two front-ends is the value of the resistors. A typical value of the resistor is $50\ \Omega$ for the low-impedance front-end and $500\ \Omega$ for the high-impedance front-end. The low-impedance front-end has the best bandwidth performance among the three because of the small RC time constant at the output, but suffers from the weak signal detection ability because of the small value of the resistor R_1 . In addition, the equivalent thermal noise current is given in Equation (3.11), and yield a lower SNR (Signal to Noise Ratio) given in Equation (3.12) for the resistor R_1 with a smaller value. Increasing R_1 raises the output noise but also increase the gain, and the effect of latter is more significant than the former thus improving the SNR.

$$i_{n,rms} = \sqrt{\frac{4kT}{R_1}} \quad (3.11)$$

$$SNR = \frac{i_{in,rms}}{i_{n,rms}} = \frac{i_{in,rms}}{\sqrt{\frac{4kT}{R_1}}} = \frac{i_{in,rms} \cdot \sqrt{R_1}}{\sqrt{4kT}} \quad (3.12)$$

On the other hand, the high-impedance front-end has the best signal detection ability as well as a low input referred thermal noise current because of the high value of the resistor. However, it suffers from the narrow bandwidth caused by the large RC time constant at the output, and limited signal swing even if followed by an equalizer to enhance the bandwidth performance.

To overcome all the problems brought by the low-impedance and high-impedance front-ends, transimpedance front-end comes into place and makes a good comprise of the bandwidth and signal detection ability. The input resistance R_{in_TIA} for the transimpedance front-end is given in Equation (3.13), and is smaller than that of the other two front-ends by a factor of $A+1$, so the bandwidth performance of the transimpedance front-end is improved by a factor of $A+1$ as compared with the other two front-ends [17].

$$R_{in_TIA} = \frac{R_f}{A+1} \quad (3.13)$$

In addition, the transimpedance gain of all the three front-ends is determined by the value of R_f or R_L . In summary, transimpedance front-end gives a better bandwidth performance while sustaining the same gain performance.

Generally there are three basic types of transimpedance front-ends with the CMOS technology: the common-source, common-gate, and common-drain TIAs. In addition, some TIAs are implemented with the help of current mirrors [20]. The configurations and performance for these different structures will be further discussed in the following sections.

3.3.1 Common-source, Common-drain, and Common-gate TIAs

The circuit structures of the common-source, common-drain and common-gate TIAs are shown in Fig. 3.7 [21-25]. Common-source and common-drain TIAs are actually the circuit implementations in transistor level of the TIA circuit concept described in Fig. 3.2. The input current will go through the resistor R_f because of the high impedance of the input transistor. For the common-gate TIA, transistor M_1 acts as a current buffer. The bandwidths of the three are given in Equations (3.14), (3.15), and (3.16).

Figure 3.7: (a) Common-source, (b) Common-drain and (c) Common-gate TIAs

$$\omega_{BW-CS} = \frac{1 + g_{m1}R_1}{2\pi R_f [C_{pd} + C_{gs1} + (1 + g_{m1}R_1)(C_f + C_{gd1})]} \quad (3.14)$$

$$\omega_{BW-CD} = \frac{1 + g_{m2}R_2}{2\pi R_f [C_{pd} + C_{gd1} + (1 + g_{m2}R_2)C_f]} \quad (3.15)$$

$$\omega_{BW-CG} = \frac{1 + g_{m2}R_2}{2\pi R_f [C_{d1} + C_{gs2} + (1 + g_{m2}R_2)(C_f + C_{gd2})]} \quad (3.16)$$

$$C_{pd} \gg C_{gs1}, C_{gs2}, C_{gd1}, C_{d1}, C_f \quad (3.17)$$

$$1 + g_{m1}R_1 \approx 1 + g_{m2}R_2 \quad (3.18)$$

$$\begin{aligned} C_{pd} + C_{gs1} + (1 + g_{m1}R_1)(C_f + C_{gd1}) &= C_{pd} + C_{gs1} + (1 + g_{m1}R_1)C_{gd1} + (1 + g_{m1}R_1)C_f \\ &> C_{pd} + C_{gd1} + (1 + g_{m2}R_2)C_f \gg C_{d1} + C_{gs2} + (1 + g_{m2}R_2)(C_f + C_{gd2}) \end{aligned} \quad (3.19)$$

The photodiode capacitance C_{pd} has a value ranging from 0.1 pF to 1pF, and is much larger than the gate-source parasitic capacitance C_{gs1} , C_{gs2} , the gate-drain parasitic capacitance C_{gd1} , the parasitic capacitance C_{d1} at the drain of M_1 and the parasitic capacitance C_f over the feedback resistor R_f , which are usually dozens of fF as shown in Equation (3.17). Equation (3.18) holds as the transconductance $g_{m1} \approx g_{m2}$ and the

resistor $R_1 \approx R_2$. From Equation (3.17) and Equation (3.18), Equation (3.19) is derived. Therefore, the common-gate TIA has the best the bandwidth performance, and the common common-drain TIA have a slight better bandwidth performance than the common-source TIA.

3.3.2 Current mirror TIAs

Current mirrors can be used to build TIA as shown in Fig. 3.8 [20]. Similar to the common-gate front-end, the input resistance is approximately $\frac{1}{g_{m1}(1+A)}$ at low frequencies and $\frac{1}{g_{m1}}$ at high frequencies. Because of the low input resistance, the bandwidth is no longer determined by the input resistance, but determined by the feedback resistance and the loading capacitor at the output node. Thus the large photodiode parasitic capacitance will have little effect on the bandwidth performance in such case, and hence the current mirror type of TIA has a better bandwidth performance. However, the current mirror TIA has a few disadvantages. One of the disadvantages is that the input transistors-pair of the current mirror is connected directly to the input of the TIA, so it will introduce much more noise into the circuit as compared with other types of TIAs. Another disadvantage is its high DC power consumption because of the large DC current in the output branch.

Figure 3.8: Current mirror TIA

3.4 Advanced Structures of TIAs

To achieve better bandwidth, noise, transimpedance gain, dynamic range, and other circuit performances, different advanced structures of TIAs are proposed and studied. In the following sections, a Regulated Cascode (RGC) input TIA is discussed for its excellent bandwidth performance without reducing the transimpedance gain [26-30]. To reduce the parasitic capacitance between the photodiode and TIA, an integration of compound semiconductor detectors and silicon circuitry was explored [31-39]. Different ways to enhance the bandwidth performance with inductors or inductive elements were also experimented [13, 38, 40-50]. The inductors are realized using on-chip inductors, on-chip transformers, and active inductors. Some works are also done to generate negative impedance especially negative capacitance to further improve the bandwidth performance [51-55]. To enlarge the dynamic range, some topologies are introduced such as Automatic Gain Control and dual TIA core circuit [5-12, 56, 57].

3.4.1 RGC input TIAs

Since the TIA is the first stage of the analog front-end of an optical receiver, it is the most crucial block in determining the bandwidth and input referred noise. The conventional TIAs such as the common-source TIA have a trade-off between the bandwidth and transimpedance gain. The RGC input TIA in Fig. 3.9 has an improved bandwidth performance by isolating the large photodiode capacitor from the feedback resistor [27, 28, 30]. Compared with the common-gate TIA, the RGC input TIA has a smaller input resistance due to the local feedback loop which consists of transistor NMOS M_1 and M_B . The input resistance is given in Equation (3.20), which is smaller than that of the common-gate TIA by a factor of $(1 + g_{mB} R_B)$.

Figure 3.9: RGC input TIA

$$R_{in} \approx \frac{1}{g_{m1}(1 + g_{mB} R_B)} \quad (3.20)$$

The schematic diagram of a pseudo differential RGC input TIA is shown in Fig. 3.10. It consists of the RGC input stage formed by transistors M_1 and M_2 , and the second

voltage-gain stage with threshold-voltage loss compensation loads. The drain of NMOS M_5 can swing up to V_{DD} as the PMOS M_7 can operate at triode region to provide small signal resistance.

A pseudo differential RGC input TIA will have a better noise rejection performance because of its pseudo differential structure. The bandwidth of the circuit is given in Equation (3.21), and it is obvious that the large photodiode capacitance no longer dominates the bandwidth. In this manner the feedback resistor can be made a bit larger to enhance the noise performance while sustaining a relatively high bandwidth.

Figure 3.10: A Pseudo Differential RGC input TIA

$$\omega_{BW} = \frac{1}{2\pi R_f \left[\left(\frac{C_{d1} + C_{gs5}}{1 + \frac{g_{m5}}{g_{07}}} \right) + C_{gd5} \right]} \quad (3.21)$$

3.4.2 Hybrid TIAs

To reduce the parasitic capacitance between the photodiode and the TIA, and save the cost of assembling the external photodiode to the transimpedance amplifier, an integration of compound semiconductor photodiodes and the silicon TIA circuitry were experimented [31-39].

Traditionally, to obtain high-bandwidth receivers, high frequency technologies such as GaAs and SiGe are utilized for TIA circuit. The trend to reduce cost is by using the CMOS technology. As such, realization of the photodiode in the CMOS technology integrated together with the CMOS TIA circuit is studied [31, 39]. As the scale of the transistor decreases especially in the CMOS technology, the supply voltage also reduces. Charge pump techniques are therefore adopted to generate a photodiode bias voltage which is higher than the supply voltage. By employing a flip-chip technique, it is possible to bond the Quantum Well (QW) diodes arrays to the CMOS TIA circuit [58], hence saving excessive usage of silicon area.

3.4.3 TIAs with inductors and inductive elements

To further increase the bandwidth of the TIA, inductors and other inductive elements are used in the circuit. A simple diagram of the TIA utilizing an inductor or inductive element in a single-ended manner is shown in Fig. 3.11. This circuit structure can increase the bandwidth by a factor from 1 up to 1.85 due to the negative impedance

introduced by the inductor or inductive element [42]. The inductor can be implemented by on-chip inductors, on-chip transformers, active inductors, and even bonding wire in the package. On-chip inductors can be modeled as a lumped element model, which is often presented by a typical π -equivalent model as shown in Fig. 3.12. Inside this model, L is the total inductance produced by the metal winding and the mutual inductive coupling. R_L is the loss of the inductor, C_{oxide} is the capacitance between the inductor and the substrate, R_{Si} and C_{Si} are the parasitic resistance and capacitance to the substrate.

Figure 3.11: TIA with inductors to enhance the bandwidth

Figure 3.12: Lumped element models of an on-chip inductor

Active inductors are also adopted to save the large chip area occupied by the on-chip inductors, and its circuit implementation is shown in Fig. 3.13. It consists of a NMOS M_L and a resistor R_L connecting between the gate and the drain. The input impedance looking into the source of the NMOS M_L behaves as an inductive element and hence broadens the bandwidth with a small chip area.

Figure 3.13: Active inductor to enhance the bandwidth

3.4.4 TIAs with negative capacitance

To improve the bandwidth performance of the TIA, negative capacitance is extensively studied in [51, 52, 54, 55]. One approach to implement the negative capacitor is shown in Fig. 3.14. The input impedance looking into the drain of the NMOS transistor pair is given in Equation (3.22) [52, 59], and will be modeled as a negative capacitance $-C_a$ in series with a negative resistance $-(C_{gs}/C_a + 2)/g_m$ if the operating frequency is

far below f_T of the transistor. The negative capacitance will compensate the positive capacitance at the nodes of the circuit to improve the bandwidth performance.

$$Z_{in} = -\frac{1}{sC_a} \cdot \frac{g_m + s(C_{gs} + 2C_a)}{g_m - sC_{gs}} \quad (3.22)$$

Figure 3.14: TIA with negative capacitance

3.4.5 AGC TIAs

As the optical signal arriving at the photodiode varies its power due to different transmission paths, the TIA needs to be able to handle different input photocurrents with wide dynamic range. To increase the dynamic range of the TIA, Automatic Gain Control (AGC) block is developed [5-12, 51, 52, 54, 55]. Usually it is achieved by replacing the fixed feedback resistor with a variable feedback resistor illustrated by R_f as shown in Fig. 3.15. The operation mechanism of the AGC is that: the value of resistor R_f increases

when the input power is low, and reduces when the input power is high. Hence the dynamic range of the TIA circuit is extended.

Figure 3.15: Automatic Gain Control TIA

The variable feedback resistor can be implemented using a transistor operating in the triode region, which can be modeled as a voltage controlled resistor. An alternative way to realize the variable feedback resistor is a combination of transistors and fixed value resistors. Fig. 3.16(a) shows a fixed resistor R_{FIX} connected in series with a resistor R_{AGC} , which is connected to a transistor in parallel. A control voltage V_{control} is generated based on the magnitude of input photocurrent and applied at the gate of the transistor. A feedback capacitor C_{FB} is inserted into the network to introduce a zero and improve the bandwidth performance of the TIA circuit. An alternative method to build the resistive network is using transistors as switches, which are connected in series with the fixed

value resistors. A few of these are placed in parallel to achieve variable gain as shown in Fig. 3.16(b).

Figure 3.16: Resistor tree (a) transistor and fixed value resistor and (b) transistor acting as switches

3.4.6 Dual TIA core

With increased demand for wide dynamic range, a dual TIA core topology is proposed to extend the dynamic range of the TIA [56, 57]. It consists of two TIA front-ends as shown in Fig. 3.17(a): one is a high-gain mode TIA and the other is a low-gain mode TIA implemented by unequal feedback resistors. The high-gain mode TIA will have a better noise performance but with degraded overload performance, so an additional low-gain mode TIA is introduced to enhance dynamic range. The low-gain TIA will be activated

when the input power is high as shown in Fig. 3.17(b). The drawback of this structure is of course greater power consumption.

Figure 3.17: (a) Dual TIA circuit and (b) Increased dynamic range

Another type of the dual TIA core proposed in [57] has a similar structure as the one shown in Fig. 3.17(a). It features two TIA front-ends, with one of the TIA generating the average level of the input signal, and comparing it with the delayed version of the output from the other TIA, hence extracting the data information based on the comparison results.

3.5 Limiting Amplifier Design Considerations

The Limiting Amplifier (LA), which is one of the implementations of the Main Amplifier (MA) in Fig. 3.1, enlarges the signal from the Transimpedance Amplifier (TIA) to wider dynamic range, usually in several 100 mV peak-to-peak. An alternative implementation of an MA is the Variable Gain Amplifier (VGA). The DC transfer functions of the two are shown in Fig. 3.18. An LA has a linear transfer function within a small range for small input voltage, and the output will be clipped to a peak value when it is operated out of the small range as shown in Fig. 3.18(a). In contrast, the VGA has different linear transfer functions with different slopes based on the magnitude of the input data. When the magnitude of the input data increases, the overall gain will decrease as indicated by the curves from left to right in Fig. 3.18(b).

Figure 3.18: DC transfer function of (a) an LA and (b) an VGA

To some extent, an LA can be viewed as a VGA which has only one extremely large gain, hence only a small linear operating region is obtained while the output is saturated to two-peak values out of the linear operating region. Other than the gain, if the LA receives an asymmetrical data from the TIA, a DC level difference would be exhibited

between the two differential outputs of the LA unless a proper DC offset cancellation scheme is implemented. A normal AC coupled LA could remove the DC offset problem but will encounter problems with input burst mode data. In addition, a *reset* signal is required for such input burst mode data.

3.5.1 Gain of LAs

Because of the well known Gain-Bandwidth-Product (GBW) constrain [60], it is hard to achieve both the high gain and broad bandwidth in one single-stage amplifier. Conventionally the LA consists of several gain stages, and has an overall gain defined by Equation (3.23). ΔV_{Out} is the change of the output of the last gain stage, and ΔV_{in} is the change of the input of the first gain stage. Normally a few gain cells are adopted to achieve higher gain.

$$A = \frac{\Delta V_{Out}}{\Delta V_{in}} \quad (3.23)$$

3.5.2 DC Offset Cancellation

In most of the cases a single-ended photodiode is used in the optical receiver, and it results in a single-ended photodiode current, which will be further converted into a single-ended voltage signal after the TIA which in turn causes an asymmetry in the DC levels of the MA final outputs as shown in Fig. 3.19. Although differential and multiple-pin photodiodes are investigated in the optical receiver, the increased complexity of the overall structure raises the total cost of the optical receiver [58].

Figure 3.19: Asymmetrical DC levels at the final outputs

The asymmetrical DC levels at the final outputs will cause a significant reduction in the output dynamic swing, and limit the advantages brought by a differential configuration. Therefore it is desirable to eliminate this DC level offset.

For the continuous mode data, the DC level of the input data is fixed, so the DC level offset of the output can be easily removed by an offset control circuit in a feedback configuration as shown in Fig. 3.20 [46, 61]. Initially the two inputs are vertically offset against each other with different DC levels indicated by one solid *pulse* and one dotted *pulse*. The DC offset control circuit consists of two pairs of low-pass filters formed by simple RC networks, and an op-amp (OPA) used as a comparator connected in the feedback of the LAs. With the use of this DC offset control circuit, the differential outputs eventually share the same DC level after the cascading chain of limiting amplifiers.

Figure 3.20: A continuous mode LA with DC offset cancellation circuit

Usually the low-pass RC network will introduce a lower cutoff frequency in the overall transfer function, which is inversely proportional to the value of the resistor and the capacitor. To achieve a lower cutoff frequency, very large RC time constant is needed, so resistors and capacitors with large values are required. In silicon implementation, a large value resistor is realized by a MOS transistor instead of normal low resistive polysilicon resistor to save chip area [59]. However, due to the large value requirement for the capacitors, typically in terms of μF , the capacitors are realized using off-chip capacitors.

A drawback of this type of DC offset control circuit is the long settling time due to the large RC time constant, which makes it unsuitable to be used for the burst mode data which requires very fast response [62, 63]. So alternative approaches to eliminate the DC offset are studied and further explored in section 3.7.1 and section 3.7.2.

3.5.3 AC coupled and DC coupled LAs

After the TIA stage, the photocurrent signal is converted into a voltage signal and passed on to the next stage: the LA stage. There are two topologies connecting the two stages: one is the AC coupling and the other is the DC coupling.

For the DC-balanced continuous mode data as shown in Fig. 3.21 (b), it is easy to extract the average DC level of the signal, and use it as a bias voltage to be compared with the original signal as seen entering the limiting amplifier as shown in Fig. 3.21 (a). However, it is not suitable for the burst mode data as the average DC level varies and is not near the average of the maximum and minimum signal voltage excursion as the input data varies with power between different packets [17] .

Figure 3.21: (a) AC coupled LA and (b) Average power for the continuous mode and burst mode data

An exception to use the AC coupling for the burst mode data is to put a small coupling capacitor between the TIA and LA acting as a differentiator shown in Fig. 3.22 [64, 65]. The AC coupling will produce pulses with polarities depending on whether the data edges are rising or falling. To restore the original signal, the following LA is configured as a hysteretic comparator and functions as an integrator. However, it will introduce more high frequency noise into the circuit because of the high-pass function of the AC coupling and degrade the sensitivity performance.

Figure 3.22: (a) AC coupled LA with hysteretic comparator and (b) waveforms at different nodes

To avoid the problem brought by the AC coupling for burst mode data, the special DC coupled LA is widely used instead in the optical receiver [66-70]. A simplified block

diagram is shown in Fig. 3.23: compared with the AC coupling method, the coupling capacitor is removed, and a DC bias voltage block is included to generate a bias voltage from the input signal and compare it with the input signal at the input of the LA. In this manner, the input data is sliced accurately. The details of the circuit will be discussed in section 3.7.2.

Figure 3.23: DC coupled Limiting Amplifier for burst mode data

3.5.4 LA circuit with reset

The burst mode data come in packets, and arrive at the photodetector one by one with a guard time between them as shown in Fig. 3.24. For each packet of data, there is the preamble data (512 bits) at the very beginning of the data sequence acting as dummy data. When the DC coupled LA is adopted, the peak and bottom level detection function blocks are built into the circuit to detect the power level of the input data. However, the power level is different from one packet to another packet. Therefore the desired peak and bottom level values extracted by the circuit would be different from packet to packet. If a certain peak level value is pre-stored at a capacitor or any other charge holding

blocks, a smaller peak level value may not be detected correctly unless the pre-stored value is first removed by a discharging process.

In this case, a *reset* signal is required to trigger the discharging of the holding capacitors and hence reset the peak level detecting blocks. Some variations have been reported to provide an external *reset* signal in the system [68, 71, 72]. However, the addition of an external *reset* signal will increase the circuit complexity. To avoid the external *reset* signal, [73] has been reported with an internally created *reset* signal by utilizing the preamble data without affecting the primary data containing the real information. The details of the reset creation circuit structure will be discussed in section 3.7.3.

Figure 3.24: Reset signal with the burst mode data

3.6 Basic Structure for LAs

Over the decades, different types of LAs have been proposed and studied as they are the intermediate stage between the Transimpedance Amplifier (TIA) and the Clock and Data Recovery circuit (CDR). To increase the bandwidth performance, shunt-peaking inductors or inductive components are often adopted in the circuit as loads [43, 44, 46, 47, 49]. The second and third order active feedback techniques are also developed for the LA to broaden the bandwidth [59, 74, 75]. The elimination of on-chip inductors from the circuit reduces the chip size. Regulated cascode LA is proposed to enhance the bandwidth by isolating the load from the input transistor stage through the use of a regulated cascode stage.

3.6.1. LAs with shunt-peaking inductors or active inductors

Fig. 3.25 shows a single-stage Limiting Amplifier without and with shunt-peaking inductors. Resistor R_1 and R_2 have the same value and the rest of the circuit is symmetrical as seen in Fig. 3.25(a) [43, 44, 46]. A quick analysis reveals that the two outputs will be confined in a range between V_{DD} and $(V_{DD} - I_1 \cdot R_1)$ indicated by Equation (3.24) as implied by the word “Limiting” in the name “Limiting Amplifier”. Similar to a TIA, an LA can also make use of the inductors to increase its bandwidth as indicated in Fig. 3.25(b).

$$(V_{DD} - I_1 \cdot R_1) < V_{out1,2} < V_{DD} \quad (3.24)$$

Figure 3.25: LA (a) without peaking inductors and (b) with peaking inductors

3.6.2. Active Feedback LAs

On-chip inductors, however, occupy large chip area. The active feedback Limiting Amplifier is developed to explore the possibility to build inductorless circuits with an enhanced bandwidth performance [45, 74, 76]. The block diagram and schematic diagram of an active feedback LA are shown in Fig. 3.26 and Fig. 3.27. The Gain Bandwidth product (GBW) can be increased beyond the technology f_T by a factor equal to the ratio of f_T over one gain cell bandwidth f_{-3dB} as in Equation (3.25).

$$GBW = Gain \cdot \omega_{BW} = f_T \cdot \frac{f_T}{f_{-3dB}} \quad (3.25)$$

Figure 3.26: Block diagram of an active feedback LA

Figure 3.27: Schematic diagram of an active feedback LA

3.6.3. LA with regulated cascode load

To increase the bandwidth performance of the LA, a regulated cascode LA is used as depicted in Fig. 3.28 [47]. The two identical regulated cascode loads at the top of the circuit are isolated from the input source-coupled transistor pair M_5 and M_6 . Therefore the large capacitances caused by Miller effect at the gates of transistor pair M_5 and M_6 are removed from the circuit, so it will not deteriorate the signal bandwidth when the circuit is connected up. The dominant pole is at the drain of NMOS transistors M_1 and M_2 , so the signal bandwidth is increased. The input impedance is greatly reduced by the feedback loop formed by NMOS transistors M_1 and M_3 hence the nondominant pole is pushed to a higher frequency region to avoid any instability.

Figure 3.28: A simplified LA with regulated cascode load

3.7 Advanced Structures for LAs

Both the continuous mode LA and burst mode LA share some common design challenges such as the bandwidth which is discussed in the previous sections. However, the special features of the burst mode data put more challenging design requirements for the burst mode LA: the burst mode LA needs to have a quick DC offset cancellation loop, fast response with the input signal, and an internal *reset* signal to reduce the overall system design complexity. Over the years, different circuit topologies have been developed to meet these design requirements and will be further presented in the following sections [66-68, 71, 73, 77-79].

3.7.1 Feedback type LAs

An LA circuit utilizing peak detectors in a feedback configuration is proposed in [8] as shown in Fig. 3.29. The feedback loop is built to generate a voltage signal which is proportional to the magnitude of the input signal. The mechanism of the operation is explained as follows: the positive peak of the signal is captured by the peak detector, and subtracted by the difference amplifier with the negative peak captured by the negative peak detector. The result after subtraction is applied to the input of the comparator and compared with a reference voltage. The difference is integrated by an integrator and the final result is applied to the gain control block to adjust the gain. The overall circuit structure proposes the possibility to handle the data with varying power by including peak detectors in the feedback loop. However, this type of feedback amplifier suffers from a long settling time hence is not suitable for the burst mode LA, especially when the bit rate is fast.

Figure 3.29: LA with DC offset compensation in a feedback configuration

Taking the idea from the previous circuit [8], the inclusion of the peak detectors in the feedback loop is explored to create a new DC offset cancellation scheme as shown in Fig. 3.30 [77]. Instead of averaging the signal, the circuit adopts a differential configuration and compares the difference of the peak values from the differential signals after each gain cell in the Limiting Amplifier chain. The results after the comparison are sent to the Analog Mux and Select Logic block, where a digital selection logic output is instantaneously selected according to the input signal. A dynamic continuous voltage signal is produced from the integrator based on the digital select logic output. The settling time of the overall circuit can be reduced to the μs range, which is better than the conventional offset compensation circuit by three orders of magnitude. However, it could not meet the burst mode LA design requirement, which normally demands a settling time usually in the range of a few hundreds of ns or less.

Figure 3.30: Simplified Crain Limiting Amplifier

A conventional peak detector circuit is present in Fig. 3.31 [73, 80] , which consists of an operational amplifier, a diode-connected transistor, a level-holding capacitor, a transistor whose gate is controlled by a *reset* signal, and a source follower as a voltage buffer. The *reset* signal is used to initialize the hold level when each burst packet comes. Whether it performs a positive peak (top level) detection or negative peak (bottom level) detection is determined by the polarity of the diode formed by the transistor M_1 .

Figure 3.31: Top level detector circuit structure

3.7.2 Feedforward type LAs

Over the decades, lots of works have been investigated for LAs inside the burst mode optical receiver [67-69, 71, 81, 82]. Among these designs, [67, 68] introduce the concept of the feedforward Auto-Bias. Based on the method to extract the average level of the signal in the feedback path in [8] as shown in Fig. 3.29, the concept of the feedforward Auto-Bias method is proposed to extract the average level of the signal as the bias voltage in a feedforward configuration [67, 68]. The LA chain in the circuit consists of several identical cascaded gain cells. To illustrate the concept of the feedforward Auto-Bias, the block diagram of one of the gain cells is shown in Fig. 3.32(a). The gain cell consists of a top-hold and bottom-hold circuit, a resistive bridge, and a limiting amplifier. The positive peak of the input signal V_{top} is detected by the top-hold circuit and the negative peak of the input signal V_{bottom} is detected by the bottom-hold circuit. The exact centre value of the input signal V_{ref} is extracted from the resistive bridge even with the presence of a small offset voltage existing in the input signal as shown in Fig. 3.32(b). This voltage V_{ref} is set as the bias voltage for the auxiliary input of the Limiting Amplifier and compared with the input signal. In this manner, the optimum bias voltage for the burst mode data with different amplitudes can be generated instantaneously avoiding the need for any external and fixed bias voltage.

A different approach has been proposed in [71, 81] as shown in Fig. 3.33. The gain cell for this type of circuit consists of two peak detectors and a four-input-pin Limiting Amplifier. Instead of extracting the bias voltage based on the input signal directly, the peak values of the differential circuit are sampled and passed through a ramp amplifier

whose gain is fixed at 0.5. The outputs from the ramp amplifier and original differential signals are fed into the four-input Limiting Amplifier. The large DC offset voltage inside the differential signals can be cancelled off through this type of circuit implementation.

Figure 3.32: (a) Burst mode optical receiver with a dynamic bias voltage and (b) Bias voltage creation based on the input data

Figure 3.33: Four-input-pin LA

With the idea of the feedforward DC offset cancellation scheme discussed above, a new type of the burst mode optical receiver is presented in Fig. 3.34(a) [78]. A Single-to-Differential (S2D) block is inserted between the TIA and LA chain. The signal is single-ended at the node *A* as indicated by the waveform *A* in Fig. 3.34(b), and becomes differential at the node *B* after the S2D stage but with different DC levels indicated by the waveforms at node *B*. The LA chain developed in [71, 81] will eventually bring the DC levels of the two differential outputs close to each other as indicated by the waveform *C* and waveform *D*. A buffer block is provided to enable the circuit to drive 50 Ω resistive loads. An external *reset* signal is required to initialize the peak detectors inside the LA gain cells. The removal of the averaging circuit in Fig. 3.32(a) reduces the circuit response time significantly.

Figure 3.34: (a) Feedforward optical receiver with a external *reset* and (b) waveforms at different nodes

3.7.3 LAs with internally created reset in a feedback configuration

To reduce the system complexity by avoiding an external *reset* signal, an internal *reset* signal is created in a feedback configuration as shown in Fig. 3.35 [73, 79]. The feedback loop is established in this manner: it takes the voltage signals from the outputs of the LA chain, and passes them to a reset creation circuit. The reset creation circuit will create a *reset* signal based on the input signal's magnitude, and apply it to the LA chain. The LA chain will amplify the input signal just as conventional LAs, except that the last stage of the LA will switch its feedforward gain according to the state of the *reset* signal: when there is no data, the *reset* signal is off, and the feedforward gain is kept at a higher level compared with the normal operation level. This is to ensure strong signal detection ability so that the *reset* signal can be generated with weak data at the input. On the other hand, when the data is detected, the *reset* signal is set to low, and the feedforward gain is set to the normal operation level.

Figure 3.35: Burst mode LA with internal *reset* in the feedback path

Figure 3.36: Reset-creation circuit (a) block diagram and (b) operating principle

The block diagram and the operating principle of the reset creation circuit is shown in Fig. 3.36(a) and Fig. 3.36(b). It consists of two bottom level detectors with the self discharging function, two comparators, and some logic circuits. The outputs of the LA chain V_A and V_B are sampled by the bottom level detectors, and then the sampled results V_{A_bottom} and V_{B_bottom} are compared with reference voltages V_{ref1} and V_{ref2} which are externally provided. The reference voltages V_{ref1} and V_{ref2} are set to one quarter of the output signal magnitude V_0 above the most negative level of the output signal. When

incoming data arrives, the bottom level of the input signal V_{A_bottom} is detected by the bottom level detector and its waveform will cross the line presenting the reference voltage V_{ref1} . Therefore the polarity of the output of the comparator will be changed, and then a *reset* signal will be generated after a few logic gates internally.

The bottom level detector circuit with a self discharging function is shown in Fig. 3.37 [73, 79]. Compared with the peak level detector as shown in Fig. 3.32, the orientation of the diode connected transistor M_1 is reversed for the bottom level detector. In addition, the transistor whose gate is controlled by an external *reset* signal is replaced by a large value resistor R_1 , so that the charges stored in the holding capacitor C_1 will be discharged through the resistor R_1 during the no data period without any need for an external *reset* signal.

Figure 3.37: Self Discharging Bottom level detector

3.8 Summary

This chapter describes the theory of the transimpedance amplifier and the limiting amplifier.

The general design considerations of the TIA are first introduced, including the bandwidth performance, transimpedance gain, sensitivity, overload, and group delay. Basic circuit structures for the TIA are investigated and a comparison is done between different circuit structures based on the pros and cons. To achieve excellent circuit performance, advanced circuit structures for the TIA are reviewed and discussed. The Regulated Cascode input TIA, Hybrid TIA, inductive peaking, negative impedance, automatic gain control, and dual TIA core circuits are presented.

Then, in the following sections, the general design considerations for the LA are discussed. The gain, offset compensation, fast response for burst mode data, and reset creation are analyzed. Some basic circuit structures for LAs are presented, followed by a detailed study of advanced structures for LAs which are designed to meet requirements for the burst mode LAs.

Chapter 4

Design of a CMOS Burst Mode Optical Receiver with Novel Feedforward Created Reset

4.1 Introduction

With the increasing demand for fast response in burst mode communication, a feedforward configuration is adopted to generate the bias voltage for the single to differential amplifier [66-68, 78]. To reduce the system complexity by avoiding the use of an external *reset* signal, an internally created reset circuit is implemented in a feedback configuration [73, 79]. However, there is a limitation as described in [73, 79]: the *reset* signal needs to go through a long loop before it can be applied to the circuit, and the total response time is approximately 100 ns. To reduce the total response time significantly, a burst mode optical receiver with a novel feedforward created reset is proposed in this chapter to reduce the response time down to one tenth for the EPON systems.

The proposed design methodology of the optical receiver is first discussed in section 4.2, followed by the detailed analysis of individual blocks inside the circuit in section 4.3. The simulation results of the circuit are shown to give an indication of the circuit performance in section 4.4. The layout design of the circuit is studied in section 4.5. To solve the problems encountered in the layout design such as isolation and matching, different approaches have been proposed to ensure an excellent circuit performance. The measurement of the chip is discussed in section 4.6. The test setup is presented with the

testing PCB board included. The measurement is carried out on wafer with the use of a high-speed probe station. A brief summary is given in section 4.7.

4.2 Circuit Design Methodology

A block diagram of the burst mode optical receiver is proposed as shown in Fig. 4.1. It comprises a Regulated Cascode (RGC) input TIA, a Single-to-Differential amplifier stage (S2D), five stages of Limiting Amplifiers (LA) with an automatic DC offset cancellation function, a Buffer block and a feedforward Reset-creation Circuit.

The RGC input TIA is adopted at the first stage such that in connecting with the photodiode it can achieve both wide bandwidth and high transimpedance gain performance. After the RGC input TIA, the output signal is presented as waveform *A*, which is further amplified by S2D to obtain symmetric outputs but with different DC level presented as the curve *B* in Fig. 4.2. The five stages of LAs with an automatic DC offset cancellation function further amplify the signal and move the differential outputs to the same DC level stage-by-stage as depicted by the waveforms *C* and *D* [73, 79].

Figure 4.1: Block diagram of the proposed burst mode optical receiver

Figure 4.2: Waveforms at different nodes in the circuit

Figure 4.3: Feedforward-reset creation operation

The feedforward reset creation operation is shown graphically in Fig. 4.3 and implemented by two Peak Detectors (PDs) and one Comparator (CMP) as shown in Fig. 4.1. During the period with no incoming data, the *reset* signal is set to high. As data start to arrive, the peak detectors will lock to the positive peak of the S2D output waveforms. The difference between the outputs of the S2D will be compared by the comparator. When the difference is higher than the threshold value V_{th} , indicating that data is received at the input of the optical receiver, the *reset* signal will be set to low indicated by the waveform *F*. The threshold value V_{th} is set corresponding to one third of the minimum input current to ensure that the *reset* signal will be triggered at the minimum input current.

The PD is designed without an external *reset* signal by providing self-discharge paths. The circuit implementation of the PD is explained in details in section 4.3.4.

The *reset* signal is designed to follow the pattern according to the input data. When a low power burst followed by a high power burst is applied at the input as shown in Fig. 4.4, the circuit would generate nearly constant magnitude outputs during the *data on period*. The *reset* signal would be set to low when the input data appears and set to high when data disappears. On the other hand, when a high power burst followed by a low power burst is applied at the input of the circuit as shown in Fig. 4.5, the analysis is identical and the output and *reset* signal will follow the same pattern as the one discussed above. The settling time of the *reset* signal should be kept as short as possible to ensure fast response when data is on and off.

Figure 4.4: Feedforward created *reset* signal with low to high power burst

Figure 4.5: Feedforward created *reset* signal with high to low power burst

4.3 Individual Circuit Blocks

4.3.1 Transimpedance amplifier

The RGC input transimpedance amplifier is chosen as the core circuit in the TIA block in this work for a high-speed operation. As the first block connecting to the photodiode and the rest of the circuit, the TIA dominates the overall circuit performance. Because the large feedback resistor is isolated from the large parasitic capacitance of the photodiode, the RGC input TIA can obtain a broad bandwidth while sustaining a high transimpedance gain.

The proposed RGC input TIA as shown in Fig. 4.6 is a modification of the differential RGC input TIA in [28], and it differs from [28] mainly through the removal of the tail current source connected to the sources of transistors M_5 and M_6 . while providing a transimpedance gain of $57\text{dB}\Omega$, The -3 dB bandwidth ω_{BW} is given in Equation (4.1)

$$\omega_{BW} = \frac{1}{2\pi R_f \left[\left(\frac{C_{d1} + C_{gs5}}{1 + \frac{g_{m5}}{g_{o7}}} \right) + C_{gd5} \right]} \quad (4.1)$$

where C_{d1} is the drain capacitance of M_1 , C_{gs5} is the gate-source parasitic capacitance of M_5 , C_{gd5} is the gate-drain parasitic capacitance of M_5 , g_{m5} is the transconductance of M_5 , and g_{o7} is the output conductance of M_7 . $g_{m5} = 7.1mS$ and $g_{o7} = 5mS$, so $1 + \frac{g_{m5}}{g_{o7}} = 2.4$, $C_{d1} = 78fF$, $C_{gs5} = 25fF$, $C_{gd5} = 10fF$, and $R_f = 1.4K\Omega$, so $\omega_{BW} \approx 2.14GHz$.

The equivalent noise current spectral density is given in Equation (4.2),

$$\begin{aligned} \overline{I_{eq_noise}^2} &\approx 4kT\Gamma g_{m,Rf} + 4kT\Gamma(g_{m,I1} + g_{m,I2}) \\ &+ \frac{4kT\Gamma(g_{m2} + g_{m,I3}) \cdot \omega^2 \cdot (C_{in} + C_{gs2} + C_{sb1} + C_{d,I2})^2}{(g_{m2} + g_{o,I3})^2} \\ &+ \frac{4kT\Gamma(g_{m1} + g_{m,Rf} + g_{m,I1}) \cdot \omega^2 \cdot (C_{gs1} + C_{gd2})^2}{g_{m1}^2} \\ &+ \frac{4kT\Gamma(g_{m5} + g_{m7}) \cdot \omega^2 \cdot (C_{gs5} + C_{d1})^2}{g_{m5}^2} \end{aligned} \quad (4.2)$$

where k is the Boltzmann constant, T is the absolute temperature, Γ is the noise factor, $g_{m,Rf}$ is the effective transconductance of resistor R_f , $g_{m,I1}$, $g_{m,I2}$ and $g_{m,I3}$ are the transconductance of the transistors providing the bias current I_1 , I_2 and I_3 , g_{m1} , g_{m2} , g_{m5} and g_{m7} are the transconductance of M_1 , M_2 , M_5 and M_7 , C_{in} is the input parasitic capacitance, C_{sb1} is the source-bulk parasitic capacitance of M_1 , and $C_{d,I2}$ is the drain capacitance of the transistor M_2 providing the bias current I_2 .

As $C_{in} \approx 450 \text{ fF} \gg C_{gs1}, C_{gd2}, C_{gs5}, C_{d1}, C_{gs2}, C_{sb1}, C_{d,12}, \overline{I_{eq_noise}^2}$ is dominated by the first three items in the equation. With $k = 1.38 \cdot 10^{-23}$, $T = 300 \text{ K}$, $\Gamma = 1$ for $g_{m,Rf}$, $\Gamma = 2/3$ for $g_{m,I1}$ and $g_{m,I2}$, $g_{m,Rf} = 0.7 \text{ mS}$, $g_{m,I1} = 1.5 \text{ mS}$, $g_{m,I2} = 0.87 \text{ mS}$, $g_{m2} = 4.5 \text{ mS}$, $g_{m,I3} = 0.44 \text{ mS}$, $g_{o,I3} = 1 \text{ mS}$, $C_{in} \approx 450 \text{ fF}$, $C_{gs2} = 16 \text{ fF}$, $C_{sb1} = 1 \text{ fF}$ and $C_{d,12} = 5 \text{ fF}$, an integration over the bandwidth yields the input referred noise current equal to $0.287 \mu\text{A}$.

Figure 4.6: Schematic diagram of the regulated cascode input TIA

4.3.2 Single-to-Differential circuit

The schematic of the Single-to-Differential (S2D) circuit is shown in Fig. 4.7. It mainly consists of a differential NMOS transistors input pair, two loading resistors, and two source follower voltage buffers. The single-ended signal at node *A* is converted into differential signals with different DC levels at node *B*. The gain of the S2D is dominated by the resistors R_1 and R_2 as the output impedances looking into the drains of the NMOS transistors M_1 and M_2 are much larger than the resistors R_1 and R_2 . Two identical S2Ds are cascaded to provide a single to differential conversion as well as a single ended gain of 7.6dB.

Figure 4.7: Schematic diagram of the S2D

4.3.3 Limiting Amplifiers with automatic DC offset cancellation

An LA with automatic DC offset cancellation has a similar circuit structure in the feedforward path as the S2D block shown in Fig. 4.8. However, different from the S2D block, an LA has local feedback paths consisting of diodes D_1 and D_2 , level holding

capacitors C_1 and C_2 , and a transistor pair M_3 and M_4 . The diodes and level holding capacitors act as peak detectors to sample the peak values of the signals at the outputs of the LA. The gates of the transistor pair M_3 and M_4 are controlled by the sampled peak values stored in the level holding capacitors, and the signals at the drains of the transistors M_3 and M_4 will be pushed towards the same DC level because of the negative feedback. Due to the nature of the source followers formed by transistors M_5 and M_6 , the outputs of the LA will approximately have the same signal level following the gates of transistors M_5 and M_6 , and an automatic DC offset cancellation function is achieved in this configuration. A pair of NMOS transistors M_7 and M_8 , whose gates are controlled by a *reset* signal, is put in parallel with capacitors C_1 and C_2 acting as switches to charge and discharge the capacitors. Those transistors M_3 , M_4 , M_5 and M_6 , whose channel length width equal to $0.35\text{ }\mu\text{m}$, are transistors with a low threshold voltage of 0.2 V .

Figure 4.8: Schematic diagram of an LA with automatic DC offset cancellation

The overall voltage gain of the LA is given in Equation (4.3).

$$Gain = \frac{2 \cdot \alpha_5 \cdot g_{m1} \cdot R_1}{1 + \alpha_5 \cdot g_{m3} \cdot R_1} \approx \frac{2 \cdot g_{m1} \cdot R_1}{1 + g_{m3} \cdot R_1} = \frac{2 \cdot g_{m1}}{g_{m,R1} + g_{m3}} \quad (4.3)$$

where $\alpha_5 \approx 1$ is the gain of source follower formed by M_5 , g_{m1} is the transconductance of the transistor M_1 , and g_{m3} is the transconductance of the transistor M_3 . From equation (4.3), it is desirable to increase the overall voltage gain by increasing the ratio of the g_{m1} over the g_{m3} . However, the ability to achieve the automatic DC offset cancellation is dominated by g_{m3} . A big g_{m3} is required if the DC offset voltage before cancellation was large. So there is a trade-off between the overall voltage gain and the ability to achieve the automatic DC offset cancellation. In our design, $g_{m1} = 35mS$, $g_{m3} = 33.6mS$ and $g_{m,R1} = 10mS$, so $Gain \approx 4.1dB$. Five stages of LAs, with some gain variations due to different DC operating points, provide a total gain of 25.1 dB.

4.3.4 Peak detector with self-discharging function

The peak detector circuit is shown in Fig. 4.9. The main part of the circuit consists of a differential amplifier, a high value resistor R_1 , a level-hold capacitor C_1 , and a diode D_1 formed by the diode-connected transistor. The input signal is amplified by the differential amplifier, and then sampled and held the peak value by diode D_1 and capacitor C_1 . Due to the unity gain feedback loop through the source follower M_5 , the output voltage is equal to the positive peak of the input signal swing. One more identical follower M_6 is inserted at the output stage to obtain an output with higher driving capacity and less loading effect. A self-discharge path is provided by a high value resistor R_1 paralleled with C_1 during the no burst period.

To ensure that the *reset* signal is kept low during self-discharging in the PD during the *data on period*, the self-discharging time constant is designed to be at least 100 ns. On the other hand, the maximum number of consecutive identical bits is five for an 8B/10B coding in the EPON systems [4]. Each bit occupies 0.4 ns in time for a 2.5 Gbps data, so the maximum allocated time for the five consecutive identical bits “0” during the *data on period* is 2 ns, which is much less than the self-discharging time constant. Thus the *reset* signal will be kept low even if the consecutive identical bits “0” of maximum number have been detected during the *data on period*.

Figure 4.9: Schematic diagram of the peak detector

4.3.5 Comparator

The comparator block is shown in Fig. 4.10. It consists mainly of three stages: a pre-amplification stage, a decision circuit stage, and a post-amplification stage. The input signal is amplified by the pre-amplification stage to increase the overall sensitivity of the comparator over that of one single stage comparator. The inputs of the pre-amplification

stage are isolated from the decision circuit stage which has a positive feedback loop and generates unwanted switching noise (a.k.a. kickback noise). A decision will be made in the decision circuit stage based on the magnitudes of the signals arriving at the input of the pre-amplification stage, and the resultant output is sent to the post-amplification stage where a digital signal is generated. When a 3.5 mV signal is applied at the pre-amplification stage, corresponding to one third of the minimum input current, a 200 mV swing signal appears at the gate of the inverter formed by M_{15} and M_{16} , hence triggering the *reset* signal.

Figure 4.10: Schematic diagram of the comparator

There is no high impedance node inside the pre-amplification stage, so high speed is achieved at this stage. At the decision circuit stage, a positive feedback is formed by the cross-gate connection of NMOS transistors M_8 and M_9 to increase the gain of the decision circuit. A single to differential conversion is realized at the post-amplification stage.

4.3.6 Buffer block

The buffer block is a simple differential amplifier with a pair of NMOS source followers used to drive the following stage. The schematic diagram of the buffer block is shown in Fig. 4.11. The inductors L_1 and L_2 are included to model the effect of the bonding wire. The resistor pairs R_3 , R_4 and R_5 , R_6 provide differential-ended $50\ \Omega$ loads. The buffer block provides a gain of 8 dB.

Figure 4.11: Schematic diagram of the buffer

4.4 Simulation Results

The complete proposed burst mode optical receiver is simulated using the cadence spectre software. The input referred noise spectrum is plotted in Fig. 4.12 indicating a density of $11.46 \text{ pA}/\sqrt{\text{Hz}}$ at 1.75 GHz. A response time of 10 ns is demonstrated with a peak-to-peak current of $12.8 \text{ }\mu\text{A}$ including the reset creation time and data settling time as shown in Fig. 4.13. The *reset* signal functions correctly when two packets with different power levels and an alternative sequence are applied at the input of the optical receiver as shown in Fig. 4.14 and Fig. 4.15. The eye diagrams at different optical input current with a random data pattern are shown in Fig. 4.16 and Fig. 4.17. The peak-to-peak value of the eye is 335 mV and the width of the eye is 400 ps for 2.5 Gbps data. The widely opened eyes indicate a good performance for the analog front-end.

Figure 4.12: Input referred noise spectrum

Figure 4.13: Transient response at optical input current of 12.8 μA peak-to-peak with 2^7-1 random data and reset creation

Figure 4.14: Internally created *reset* with high power input followed by low power input

Figure 4.15: Internally created *reset* with low power input followed by high power input

Figure 4.16: The eye diagram at optical input current of 12.8 μA peak-to-peak using random data

Figure 4.17: The eye diagram at optical input current of $80\ \mu\text{A}$ peak-to-peak using random data

4.5. Layout Design

The ability to detect signals of very low power at the front-end of the chip and signals with large swing at the back-end of the chip put a challenge on the layout design. Noise picked up by the front-end of the circuit through the substrate may be treated as signals, and this degrades performance of the circuit. In addition, matching between circuit components is required to reduce errors caused by component mismatches [83]. The compact transistor size also limits the maximum current to be drawn from a narrow space if one single layer of metal was used. To solve these problems, different approaches have been adopted, such as multiple guard rings, separated V_{DD} , GND, and bias circuit blocks, interdigitate plus cross couple of crucial transistors, and multiple layers current path. These approaches will be explained and discussed in details in following sections.

4.5.1 Multiple guard rings

The substrate of the CMOS process usually has a lower resistance than other III-V compound semiconductor technologies, and so the chance of noise coupling through the substrate is relatively higher. To prevent the noise coupling between different circuit blocks through the substrate, multiple guard rings technique is utilized to achieve better isolation. Each circuit block is surrounded by a sequence of the guard rings with alternative types as shown in Fig. 4.18. The P type guard ring is formed by a close loop of the P well that is connected to GND, and the N type guard ring is formed by a close loop of the N well that is connected to V_{DD} . Block 1, Block 2, and Block 3 are isolated from each other due to the multiple guard rings. Any noise inside the blocks will be coupled to V_{DD} or GND, via the guard rings, which have the lowest impedance to V_{DD} and GND.

Figure 4.18: Multiple guard rings to achieve isolations

4.5.2 Separated V_{DD} , GND and bias block

To further reduce the noise coupling in the circuit, the power plane of the circuit is separated into two parts. Each part of the power plane will have its own V_{DD} and GND as shown in Fig. 4.19. Due to the presence of the large swing signal inside the circuit, especially at the LA stages, the switching noise may couple through the bias circuit to the front part of the chip. To prevent the noise coupling through the bias circuit, each circuit block will be biased with a separate bias circuit as shown in Fig. 4.20. This method sacrifices the power performance of the overall circuit, with additional bias circuit blocks, but it achieves better isolation between circuit blocks.

Figure 4.19: Separated power planes on the chip

Figure 4.20: Separated bias circuit blocks on the chip

4.5.3 New common centroid layout with interdigitated transistors

To obtain matching between two transistors, the common centroid layout usually employs the cross-coupled pair and the interdigitated patterns, which are depicted in Fig. 4.21(a) and Fig. 4.21(b) [83]. Transistors M_1 and M_2 are divided into four equal parts and arranged in a cross-coupled pair manner as shown in Fig. 4.21(a). The centroid of transistors M_1 and M_2 will overlap each other at the centre point O , as the name “common centroid” suggests, and the transistors M_1 and M_2 are matched. Matching could also be achieved when the fingers of the two transistors are properly interdigitated as shown in Fig. 4.21 (b). Two transistors M_1 and M_2 , whose gates are controlled by signals A and B , are merged as if only one single transistor existed (the gates controlled by the signal B are shaded). Both transistors share their sources (S) as common but they have individual drains (D). The advantages of such an arrangement are that the centroid of components from the two transistors overlap at the same point, and the two transistors are merged with each other. As a result, the transistor matching is more robust to any process variations. However, there is a drawback for this method: the two transistors have unequal number of drains, which will reduce the matching between the two transistors.

To enhance matching of the two transistors, new interdigitate patterns are proposed. The new patterns are classified into two categories: one is in a stack manner as shown in Fig. 4.22 and the other is in a cross-coupled pair manner as shown in Fig. 4.23. For the first type, the fingers of the two transistors are arranged in four rows, and their gates are controlled by signals A and B separately. They share common sources and have individual drains. The centroid of components overlap each other with the same number of drains. For the second type, the four rows are arranged in a cross-coupled pair manner.

The centroid remain at the centre with equal number of drains and sources. The first layer metal connecting the source or drain would need to be extended away from the active region in order to have more contacts or vias, whereas the second type has inherently more room for such extension of metal as compared with the first type and hence introduces lesser mismatches.

Figure 4.21: Conventional common centroid layout: (a) Cross-coupled pair pattern and (b)

Interdigitate pattern

Figure 4.22: New interdigitate pattern in a stack manner

Figure 4.23: New interdigitate pattern in a cross-coupled pair manner

4.5.4 Multiple layers current path

The small transistor size causes a compact size in the layout. For a single transistor as shown in Fig. 4.24(a), the maximum width allowed for one single layer metal connecting the drain or source of the transistor is limited, as indicated by W_1 . To remove the limit of the current brought by the narrow width W_1 , the multiple layers current path method is proposed. Five layers of metal are employed to allow more current to flow to the active regions as seen from the cross section view as shown in Fig. 4.24(b). The metal width is made to increase from the bottom layer, metal 1 to the top layer, metal 5. So eventually, metal 5 has a much wider width and is able to carry a larger amount of the current. The increase in metal width is accompanied by the increase in the number of vias as the current passing the vias are increased from the metal at bottom layer to the top layer metal.

Figure 4.24: (a) Limited width for the metal and (b) current path in the metal layers in the cross section

4.6 Measurement

The burst mode optical receiver is fabricated using the Chartered CSM018PDK 0.18 μm CMOS process. This process provides a double well process and MIM capacitors. The die occupies an area of $1500 \mu\text{m} \times 650 \mu\text{m}$. The chip photograph, with blocks highlighted, is shown in Fig. 4.25. The test setup and measured results will be presented in the following sections.

Figure 4.25: Chip photograph with test probes

4.6.1 Test setup

The chip was mounted on and tested using a high-speed probe station. The overall measurement setup is indicated in blocks as shown in Fig. 4.26. Non-Return-to-Zero (NRZ) test data at 2.5 Gbps with a 2^7-1 PRBS pattern, which was generated from the Anritsu MP1632A digital data analyzer, provided a reasonable approximation to 8B/10B encoded data used in the EPON systems. A test circuit, which was built on a PC Board to convert voltage signals into current signals, was placed between the MP1632 digital data analyzer and the high-speed probe station. An oscilloscope was connected to the high-speed probe station to measure the output signal, using the differential $50\ \Omega$ probes.

Figure 4.26: The overall measurement setup

The schematic diagram and the PCB view of the conversion circuit are shown in Fig. 4.27. The DC component of V_{in} is blocked by the $1\ \mu\text{F}$ capacitor and the AC component of V_{in} is divided by the $2\ \text{k}\Omega$ resistor to provide a current signal source. The input parasitic capacitance of the Device-Under-Test (DUT) is $250\ \text{fF}$. The photograph of the probe station is shown in Fig. 4.28.

Figure 4.27: The schematic diagram and the PCB view of the conversion circuit

Figure 4.28: The photo of the probe station

4.6.2 Measurement results

A sequence of bursts, at 1 μs length with 1 μs guard time, was generated from the MP1632A digital data analyzer, and applied to the input of the voltage-to-current conversion circuit. A single-ended output, taken from the conversion circuit, was applied to the input of the optical receiver, and the differential outputs of the optical receiver indicated a correct functionality of the *reset* signal as shown in Fig. 4.29. The transient responses taken at the outputs of the optical receiver at the start and at steady state for the peak-to-peak input currents of 50 μA and 500 μA are shown in Fig. 4.30, Fig. 4.31, Fig. 4.32, and Fig. 4.33 respectively. From the measured results, the total response time (including reset creation time and data settling time) is less than 10 ns with a single-ended output swing of about 300 mV. This is much shorter as compared with a response time of 50 ns as reported in [73, 79], which excludes the reset creation time which is approximately another 50 ns for a bit rate of 1.25 Gbps. A power consumption of 189 mW was measured with a 1.8 V supply.

Figure 4.29: Outputs to verify the functionality of the *reset* signal

Figure 4.30: Outputs at the start of burst for the input current of 50 μ A peak-to-peak

Figure 4.31: Outputs at the steady state of burst for the input current of 50 μ A peak-to-peak

Figure 4.32: Outputs at the start of burst for the input current of 500 μA peak-to-peak

Figure 4.33: Outputs at the steady state of burst for the input current of 500 μA peak-to-peak

Figure 4.34: Integrated output noise using the standard deviation from the histogram

The output noise was measured in accordance with the methodology proposed in [84] as shown in Fig. 4.34. After disabling the input current source, the measurement shows the standard deviation from the histogram with an output noise of 5 mV. The oscilloscope itself contributed a 1.5 mV noise. With an under-estimated transimpedance gain of 12 k Ω (600mV peak-to-peak differential output versus the 50 μ A peak-to-peak input), an integrated input referred noise can be estimated by Equation (4.4).

$$I_{in_noise} = \frac{2\sqrt{(5m)^2 - (1.5m)^2}}{12k} = 0.79 \mu A_{rms} \quad (4.4)$$

With the assumption of photodiode responsivity of 0.8 A/W and from Equation (3.7) and (3.8), a sensitivity current of 5.53 μ A_{rms} (11.06 μ A_{p-p}) and an optical sensitivity of -21.6 dBm are achieved.

4.7 Summary

In this chapter, a burst mode optical receiver with novel feedforward reset creation circuit is proposed. The system level design concept is presented and illustrated. Individual blocks of the optical receiver are studied and discussed. The simulation results are provided to give an indication on the performance of the optical receiver.

The layout design is critical to ensure an excellent circuit performance and different approaches have been implemented to solve problems such as mismatch between components and isolation between different blocks. A novel interdigitate pattern is proposed to achieve excellent matching between crucial transistors to reduce unwanted offset.

The test setup is established and a conversion circuit is realized in a PCB board. The measurement is carried out on a wafer using a high-speed probe station. The measurement results show a nearly constant output swing of about 300 mV with different input current signals yet with a power consumption of 198 mW. The input referred noise is smaller than 0.79 μA_{rms} , corresponding to a sensitivity current of 5.53 μA_{rms} . The total response time (including reset creation time and data settling time) is less than 10 ns with the peak-to-peak input current ranging from 50 μA to 500 μA , which is a significant reduction in time, and is more suitable for applications requiring fast response.

Chapter 5

Design of a CMOS Burst Mode Optical Receiver with Automatic Gain Control & Novel Feedforward Created Reset

5.1 Introduction

Due to the demand for the increasing dynamic range, a CMOS burst mode optical receiver with automatic gain control and a novel feedforward created reset is proposed. The methodology of the overall optical receiver is first presented in section 5.2. Individual blocks different from the design in chapter 4 are analyzed in section 5.3. The simulation results of the circuit are shown to give an indication of the circuit performance in section 5.4. A high-speed probe station is used in the measurement and the results are given in section 5.5. A brief summary is given in section 5.6.

5.2 Circuit Design Methodology

The block diagram of the burst mode optical receiver with automatic gain control and a novel feedforward created reset is shown in Fig. 5.1. It has a differential Regulated Cascode (RGC) input TIA, five stages of Limiting Amplifiers (LA) with an automatic DC offset control function, a buffer block, a feedforward reset creation circuit, and a Schmitt trigger.

Compared with the design in Chapter 4, the TIA and the S2D are replaced by one single-stage of differential TIA circuit [28]. A Schmitt trigger is employed to provide a gain control signal *Gain_ctl* to the TIA circuit. The rest of the circuit remains unchanged.

The waveforms at different nodes are shown in Fig. 5.2(a) and the Feedforward-reset creation operation is shown in Fig 5.2(b).

Figure 5.1: Block diagram of the proposed burst mode optical receiver

Figure 5.2: (a) Waveforms at different nodes in the circuit and (b) Feedforward-reset creation operation

The *reset* signal and the *Gain_ctl* signal are designed to follow the pattern of the input data. When a low power burst followed by a high power burst is applied at the input as shown in Fig. 5.3, the circuit would generate outputs of nearly constant magnitude during the *data on period*. The *reset* signal would be set to low when the input data appears and set to high when input data disappears. The *Gain_ctl* signal would be switched to low during the low power data burst to provide a high transimpedance gain. On the other hand, when a high power burst followed by a low power burst is applied at the input of the circuit as shown in Fig. 5.4, the output, the *reset*, and the *Gain_ctl* signals will have similar waveforms according to the input data. The settling time of the *reset* signal and the *Gain_ctl* signal should be kept as short as possible to ensure fast response.

Figure 5.3: Feedforward created *reset* and *Gain_ctl* signals with low to high power burst

Figure 5.4: Feedforward created *reset* and *Gain_ctl* signal with high to low power burst

5.3 Individual Circuit Blocks

5.3.1 Differential RGC input transimpedance amplifier

A differential Regulated Cascode (RGC) input TIA is deployed as the core circuit in the TIA block for high-speed operation. The RGC input TIA provides a low input impedance to achieve broad bandwidth even in the presence of large photodiode parasitic capacitance. The differential RGC input TIA is shown in Fig. 5.5 [28]. A feedback resistor R_f is replaced by a resistive network together with an active element to adjust the transimpedance gain of the TIA based on the magnitude of the input signal. The active element, transistor M_c is turned on and off by the control signal *Gain_ctl* and the TIA circuit is switched between the low gain and high gain mode. While providing a transimpedance gain between 53 dB Ω and 55 dB Ω , the -3 dB bandwidth ω_{BW} is given in Equation (5.1)

$$\omega_{BW} \approx \frac{1}{2\pi R_f \left[\left(\frac{C_{d1} + C_{gs5}}{1 + g_{m5}/g_{o7}} \right) + C_{gd5} \right]} \quad (5.1)$$

where C_{d1} is the drain capacitance of M_1 , C_{gs5} is the gate-source parasitic capacitance of M_5 , C_{gd5} is the gate-drain parasitic capacitance of M_5 , g_{m5} is the transconductance of M_5 , and g_{o7} is the output conductance of M_7 . $g_{m5} = 19mS$ and $g_{o7} = 3.6mS$, so $1 + g_{m5}/g_{o7} = 6.3$, $C_{d1} = 100fF$, $C_{gs5} = 56fF$, $C_{gd5} = 17fF$, and $R_f = 1.5K\Omega$, so $\omega_{BW} \approx 2.5GHz$.

The equivalent noise current spectral density is given in Equation (5.2),

$$\begin{aligned} \overline{I_{eq_noise}^2} \approx & 4kT\Gamma g_{m,Rf} + 4kT\Gamma(g_{m,I1} + g_{m,I2}) \\ & + \frac{4kT\Gamma(g_{m2} + g_{m,I3}) \cdot \omega^2 \cdot (C_{in} + C_{gs2} + C_{sb1} + C_{d,I2})^2}{(g_{m2} + g_{o,I3})^2} \\ & + \frac{4kT\Gamma(g_{m1} + g_{m,Rf} + g_{m,I1}) \cdot \omega^2 \cdot (C_{gs1} + C_{gd2})^2}{g_{m1}^2} \\ & + \frac{4kT\Gamma(g_{m5} + g_{m7}) \cdot \omega^2 \cdot (C_{gs5} + C_{d1})^2}{g_{m5}^2} \end{aligned} \quad (5.2)$$

where k is the Boltzmann constant, T is the absolute temperature, Γ is the noise factor, $g_{m,Rf}$ is the effective transconductance of resistor R_f , $g_{m,I1}$, $g_{m,I2}$ and $g_{m,I3}$ are the transconductances of the transistors providing the bias current I_1 , I_2 and I_3 , g_{m1} , g_{m2} , g_{m5} and g_{m7} are the transconductances of M_1 , M_2 , M_5 and M_7 , C_{in} is the input parasitic capacitance, C_{sb1} is the source-bulk parasitic capacitance of M_1 , and $C_{d,I2}$ is the drain capacitance of the transistor M_2 providing the bias current I_2 .

As $C_{in} \approx 450 \text{ fF} \gg C_{gs1}, C_{gd2}, C_{gs5}, C_{d1}, C_{gs2}, C_{sb1}, C_{d,I2}, \overline{I_{eq_noise}^2}$ is dominated by the first three items in the equation. With $k = 1.38 \cdot 10^{-23}$, $T = 300 \text{ K}$, $\Gamma = 1$ for $g_{m,Rf}$, $\Gamma = 2/3$ for $g_{m,I1}$ and $g_{m,I2}$, $g_{m,Rf} = 0.67 \text{ mS}$, $g_{m,I1} = 1.49 \text{ mS}$, $g_{m,I2} = 0.9 \text{ mS}$, $g_{m2} = 5.5 \text{ mS}$, $g_{m,I3} = 0.5 \text{ mS}$, $g_{o,I3} = 1 \text{ mS}$, $C_{in} \approx 450 \text{ fF}$, $C_{gs2} = 14 \text{ fF}$, $C_{sb1} = 1.8 \text{ fF}$ and $C_{d,I2} = 5.5 \text{ fF}$, an integration over the bandwidth yields the input referred noise current equal to $0.31 \mu\text{A}$.

Figure 5.5: Schematic diagram of differential regulated cascode input TIA

5.3.2 Schmitt trigger

The schematic of the Schmitt trigger circuit is shown in Fig. 5.6(a) and the hysteretic transfer characteristic is shown in Fig. 5.6(b). The hysteresis of the Schmitt trigger V_H is defined by Equation (5.3). The switching-point voltages V_{SPH} and V_{SPL} are determined by the W/L ratios of the transistors. This circuit will generate the *Gain_ctl* signal based on the magnitude of the input signal.

$$V_H = V_{SPH} - V_{SPL} \quad (5.3)$$

where $V_{SPH} = 1.06V$ and $V_{SPL} = 1.02V$, hence $V_H = 40mV$.

Figure 5.6: (a) Schematic diagram and (b) the transfer characteristics of the Schmitt trigger

5.4 Simulation Results

The simulation of the proposed burst mode optical receiver is accomplished using the cadence spectre software. An input referred noise spectrum with the density of $13.91 \text{ pA}/\sqrt{\text{Hz}}$ at 1.75 GHz is obtained as shown in Fig. 5.7. When a peak-to-peak current of $12.8 \text{ }\mu\text{A}$ is used as the input, the circuit demonstrates a response time of less than 10 ns including the reset creation time and data settling time as shown in Fig. 5.8. To test the functionality of the *reset* and *Gain_ctl* signals, two packets with different power levels and an alternative sequence are applied at the input of the optical receiver, and the simulation results are consistent with the design principle as shown in Fig. 5.9 and Fig. 5.10. When applying different optical currents with random data pattern at the input of the circuit, the eye diagrams are generated as shown in Fig. 5.11 and Fig. 5.12. The eye diagrams have an eye opening of 340 mV and the width of the eye is 400 ps for 2.5 Gbps data. A good performance for the analog front-end is indicated by the widely opened eyes.

Figure 5.7: Input referred noise spectrum

Figure 5.8: Transient response at optical input current of $12.8 \mu\text{A}$ using 2^7-1 random data and reset creation

Figure 5.9: Internal *reset* and *Gain_ctl* signals with high power input followed by low power input

Figure 5.10: Internal *reset* and *Gain_ctl* signals with low power input followed by high power input

Figure 5.11: The eye diagram at optical input current of 12.8 μA peak-to-peak using random data

Figure 5.12: The eye diagram at optical input current of 600 μA peak-to-peak using random data

5.5 Measurement

The optical receiver is fabricated using the Chartered CSM018IC1D 0.18 μm CMOS process. The die area is 1400 $\mu\text{m} \times 550 \mu\text{m}$. The chip photograph is shown in Fig. 5.13.

Figure 5.13: Chip photograph with test probes

5.5.1 Test setup

A high-speed probe station was utilized in the testing. The overall test setup is the same as that in Chapter 4 in Fig. 4.32. Anritsu MP1632A digital data analyzer provided Non-Return-to-Zero (NRZ) test data in voltage format at 2.5 Gbps with a 2^7-1 PRBS pattern, which gave a reasonable approximation to 8B/10B encoded data used in the EPON systems. A voltage-to-current conversion, which was realized with the circuit on the PCB, was connected between the MP1632 digital data analyzer and the chip. An oscilloscope, with differential 50 Ω probes, was used to measure the output signals extracted from the die through the high-speed probe station.

5.5.2 Measurement results

Similar to the proposed design in Chapter 4, the MP1632A digital data analyzer generated a sequence of bursts at 1 μ s length with 1 μ s guard time and applied them to the input of the voltage-to-current conversion circuit to verify the functionality of the *reset* signal. The output of the conversion circuit was applied at the input of the optical receiver in a single-ended way and the functionality of the *reset* signal was verified by the outputs of the optical receiver as shown in Fig. 5.14. The transient responses of the optical receiver at the start and at steady state were shown for the peak-to-peak input currents of 25 μ A, 500 μ A, and 1600 μ A as shown in Fig. 5.15, in Fig. 5.16, in Fig. 5.17, in Fig. 5.18, Fig. 5.19, and Fig. 5.20 respectively. A single-ended output swing of about 300 mV was measured with a total response time (including reset creation time and data settling time) of less than 10 ns, as compared with a response time of 50 ns as reported in [73, 79], which excludes the reset creation time which is approximately another 50 ns for a bit rate of 1.25 Gbps. The chip consumed 189 mW from a 1.8 V supply.

Figure 5.14: Outputs to verify the functionality of the *reset* signal

Figure 5.15: Outputs at the start of burst for the input current of 25 μ A peak-to-peak

Figure 5.16: Outputs at the steady state of burst for the input current of 25 μ A peak-to-peak

Figure 5.17: Outputs at the start of burst for the input current of 500 μ A peak-to-peak

Figure 5.18: Outputs at the steady state of burst for the input current of 500 μ A peak-to-peak

Figure 5.19: Outputs at the start of burst for the input current of 1600 μ A peak-to-peak

Figure 5.20: Outputs at the steady state of burst for the input current of 1600 μ A peak-to-peak

Figure 5.21: Integrated output noise using the standard deviation from the histogram

Similar to the method to extract the input referred noise, the output noise is measured in accordance with the methodology proposed in [84] with the standard deviation from

the histogram from an output noise of 6 mV as shown in Fig. 5.21. Taking into account a 1.5 mV noise contributed by the oscilloscope probe itself, and with an under-estimated transimpedance gain of 12 k Ω (600 mV peak-to-peak differential output versus the 50 μ A peak-to-peak input), an integrated input referred noise can be estimated by Equation (5.4)

$$I_{in_noise} = \frac{2\sqrt{(6m)^2 - (1.5m)^2}}{12k} = 0.97 \mu A_{rms} \quad (5.4)$$

With the assumption of a photodiode responsivity of 0.8 A/W and from Equation (3.7) and (3.8), we achieve a sensitivity current of 6.79 μA_{rms} (13.58 μA_{p-p}) and an optical sensitivity of -20.72 dBm.

5.6 Summary

In this chapter, a burst mode optical receiver with automatic gain control and a novel feedforward reset creation circuit is developed. The design concept is first discussed in system level and the comparison with the first design is then made. An automatic gain control function is included in the TIA circuit to increase the dynamic range of the circuit. Some of the building blocks different from the previous design are studied and discussed. The performance of the optical receiver is predicted by the simulation results.

A conversion circuit realized in a PCB board is included in the test setup to provide a voltage to current conversion from the signal generator to the chip under test. The measurement is carried out on wafer using a high-speed probe station. When measured with peak-to-peak input currents of 25 μ A, 500 μ A, and 1600 μ A respectively, the total

response time is less than 10 ns for all the three cases with a single-ended output swing of about 300 mV. This gives a significant reduction in time and is suitable for applications requiring fast response. The measured input referred noise is less than $0.97 \mu\text{A}_{\text{rms}}$ corresponding to a sensitivity current of $6.79 \mu\text{A}_{\text{rms}}$ ($13.58 \mu\text{A}_{\text{p-p}}$). The chip occupies an area of $1400 \mu\text{m} \times 550 \mu\text{m}$ and consumes 189 mW from a 1.8 V supply.

Chapter 6

Conclusion and Recommendations

6.1 Research Work Highlights

In this research work we explored the design of the optical communication systems and focused on the challenges of high-speed burst mode optical receiver.

First, we studied different broadband solutions for the explosive growth of internet and highlighted EPON systems as the best implementation. Furthermore, we reviewed the principles of today's high-speed optical communication system, and explained the theory relating the optical communication system reliability, i.e., the BER, to the circuit level characteristics, e.g., the circuit bandwidth, and the input referred noise.

Second, we discussed the building blocks inside the optical receiver, mainly the Transimpedance Amplifier (TIA) and the Limiting Amplifier (LA). The design theory and the state-of-the-art of the TIA and the LA are fully examined, especially for burst mode data communication.

Third, we have proposed a burst mode optical receiver with a novel feedforward created reset for EPON Systems. We have demonstrated that the circuit fabricated in a 0.18 μm CMOS technology reacted with a fast response time of less than 10 ns including the reset creation time. The circuit generates a single-ended output with about a 300 mV voltage swing with input peak-to-peak current ranging from 50 μA to 500 μA . The chip occupies an area of 1500 $\mu\text{m} \times 650 \mu\text{m}$ with a power consumption of 198 mW from a 1.8 V supply.

Finally, a burst mode optical receiver with automatic gain control and a novel feedforward created reset for EPON Systems was developed. With the added automatic gain control block, the circuit fabricated in a 0.18 μm CMOS technology achieves a fast response time of less than 10 ns including the reset creation time with improved dynamic range. The circuit generates a single-ended output with about a 300 mV voltage swing from having input peak-to-peak current ranging from 25 μA to 1600 μA . The chip occupies an area of 1400 $\mu\text{m} \times 550 \mu\text{m}$ with a power consumption of 189 mW from a 1.8 V supply. The performances of the two designs are summarized and compared with [47, 73] in Table 6.1. Compared with [73], a significant reduction in the response time is achieved. The response time of 10 ns makes burst mode optical receiver with internal reset signal feasible up to a bit rate of 40 Gbps. In addition, two external voltage references are required for the comparators in [73], which would require additional pins for the package resulting at a higher cost. The switches inside the last LA block [73] also increase the complexity of the circuit. The power consumption is greatly reduced in our designs. Compared with [85] operating with the continuous mode data with the same bit rate of 2.5 Gbps, the sensitivities of our designs are 2.7 dB and 3.6 dB better, and the response time is faster even with an internal reset while [85] is using an external reset.

Table 6.1: Performance summary of the completed designs

Description	Proposed design 1	Proposed design 2	[73]	[85]
Bit rate (Gbps)	2.5	2.5	1.25	2.5
Sensitivity (dBm)	-21.6	-20.7	-26.1	-18
Overload (dBm)	-5.05	0	-5.1	-
Dynamic range (dB)	16.55	20.7	21	-
Response time (ns)	10	10	100	50
Internal Reset	Yes	Yes	Yes	No
Output level (mV)	300	300	800	300
VDD (V)	1.8	1.8	3.3	1.8
Power consumption (mW)	198	189	528	122
Technology	0.18 μm pure CMOS	0.18 μm pure CMOS	0.18 μm mixed-mode CMOS	0.18 μm pure CMOS

6.2 Future Work

We have proposed new architecture for burst mode optical receiver inside the EPON system to achieve fast response, and built the circuit to meet the design goals.

One of possible directions includes building a Clock and Data Recovery (CDR) circuit after the LA blocks, so the overall optical receiver performance would be enhanced and system integration is achieved. Furthermore, it is possible to study the laser driver hence the transmitter block to build the whole optical transceiver.

Another possible direction would be study and development of a feedforward error correction circuit. This method would reduce the required Q factor, and hence achieve a better BER with the same input signal.

The Author's Publications

L. Duan and L. Siek, "Optimized Integrated Building Blocks for a Charge Pump Circuit," Hangzhou, IEEJ International Analog VLSI Workshop 2006.

L. Duan and L. Siek, "A 1.8 V, 2.5 Gbps Burst Mode Optical Receiver with Feedforward Created Reset for EPON System," in *International Symposium on Integrated Circuits*, ISIC, 2007, pp. 69-72.

L. Duan, L. Siek and W. M. Lim, "2.5 Gbps Burst Mode Optical Receiver with Novel Feedforward Created Reset," *Electronics Letters*, vol. 45, pp. 70-71. January 1, 2009.

L. Siek, L. Duan, and W. M. Lim, "2.5 Gbps Burst Mode Optical Receiver with Automatic Gain Control and Novel Feedforward Created Reset," *IEEE Transactions on Circuits and Systems I*, submitted.

References

- [1] <http://www.internetworldstats.com/stats.htm>.
- [2] G. Kramer, *Ethernet passive optical networks* 2005.
- [3] "Results of July 2007 Survey on "overall results of Japan's Communications Industry" (Prompt Report)," *Communication News*, vol. 14, November 9, 2007, Available:http://www.soumu.go.jp/joho_tsusin/eng/Statistics/pdf/070914_1.pdf.
- [4] IEEE standard 802.3-2005, "Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications", 2005.
- [5] H. Y. Hwang, J. C. Chien, T. Y. Chen, and L. H. Lu, "A CMOS Tunable Transimpedance Amplifier," *IEEE Microwave and Guided Wave Letters*, vol. 16, pp. 693-695, 2006.
- [6] H. Ikeda, T. Ohshima, M. Tsunotani, T. Ichioka, and T. Kimura, "An auto-gain control transimpedance amplifier with low noise and wide input dynamic range for 10-Gb/s optical communication systems," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1303-1308, 2001.
- [7] D. B. Yen Nguyen, Q. Le, Y.-H. Oh, H.-B. Le, and S.-G. Lee, "A high linearity, efficient bandwidth, and high stability transimpedance amplifier," in *The Midwest Symposium on Circuits and Systems, MWSCAS*, 2005, vol. 1, pp. 167-170.
- [8] D. M. Pietruszynski, J. M. Steininger, and E. J. Swanson, "A 50-Mbit/s CMOS monolithic optical receiver," *IEEE Journal of Solid-State Circuits*, vol. 23, pp. 1426-1433, 1988.

- [9] Q. Le, S.-G. Lee, H.-Y. Kang, and S.-H. Chang, "A CMOS Burst-Mode TIA with Step AGC and Selective Internally Created Reset for 1.25Gb/s EPON," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC*, 2007, pp. 50-51.
- [10] M. A. T. Sanduleanu and P. Manteman, "A low noise, wide dynamic range, transimpedance amplifier with automatic gain control for SDH/SONET (STM16/OC48) in a 30GHz f_T BiCMOS process," in *The European Solid-State Circuits Conference, ESSCIRC* 2001, pp. 190-193.
- [11] S. Yamashita, S. Ide, K. Mori, A. Hayakawa, N. Ueno, and K. Tanaka, "Novel cell-AGC technique for burst-mode CMOS preamplifier with wide dynamic range and high sensitivity for ATM-PON system," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 881-886, 2002.
- [12] S. Han, H.-S. Ko, T.-W. Yoo, and M.-S. Lee, "Transient characteristic of AGC loop in burst-mode transimpedance amplifier for EPON," in *Conference on Lasers and Electro-Optics, CLEO*, 2003, p. 147.
- [13] S. M. R. Hasan, "Design of a low-power 3.5-GHz broad-band CMOS transimpedance amplifier for optical transceivers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, pp. 1061-1072, 2005.
- [14] A. A. Abidi, "Gigahertz transresistance amplifiers in fine line NMOS," *IEEE Journal of Solid-State Circuits*, vol. 19, pp. 986-994, 1984.
- [15] A. A. Abidi, "On the noise optimum of gigahertz FET transimpedance amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 22, pp. 1207-1209, 1987.

- [16] A. A. Abidi, "On the choice of optimum FET size in wide-band transimpedance amplifiers," *Journal of Lightwave Technology*, vol. 6, pp. 64-66, 1988.
- [17] E. Sackinger, *Broadband circuits for optical fiber communication*, 2005.
- [18] M. Ingels and M. S. J. Steyaert, "A 1-Gb/s, 0.7 μ m CMOS optical receiver with full rail-to-rail output swing," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 971-977, 1999.
- [19] D. J. T. Heatley, *Design of analog-digital VLSI circuits for telecommunications and signal processing*, 1994.
- [20] Y. Fei, "Low-voltage CMOS current-mode preamplifier: analysis and design," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, pp. 26-39, 2006.
- [21] K. Manetakis, S. M. Park, A. Payne, S. Setty, A. Thanachayanont, and C. Toumazou, "Wideband CMOS analog cells for video and wireless communications," in *IEEE International Conference on Electronics, Circuits and Systems, ICECS*, 1996, pp. 227-230.
- [22] S. M. Park and C. Papavassiliou, "On the design of low-noise, giga-hertz bandwidth preamplifiers for optical receiver applications," in *IEEE International Conference on Electronics, Circuits and Systems, ICECS*, 1999, vol.2, pp. 785-788.
- [23] S. M. Park and C. Toumazou, "Gigahertz low noise CMOS transimpedance amplifier," in *IEEE International Symposium on Circuits and Systems, ISCAS*, 1997, vol.1, pp. 209-212.

- [24] S. M. Park and C. Toumazou, "Low noise current-mode CMOS transimpedance amplifier for giga-bit optical communication," in *IEEE International Symposium on Circuits and Systems, ISCAS*, 1998, vol.1, pp. 293-296.
- [25] C. Toumazou, and S. M. Park, "Wideband low noise CMOS transimpedance amplifier for gigaHertz operation," *Electronics Letters*, vol. 32, pp. 1194-1196, 1996.
- [26] S. M. Park and H.-J. Yoo, "2.5 Gbit/s CMOS transimpedance amplifier for optical communication applications," *Electronics Letters*, vol. 39, pp. 211-212, 2003.
- [27] S. M. Park and H.-J. Yoo, "1.25-Gb/s regulated cascode CMOS transimpedance amplifier for Gigabit Ethernet applications," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 112-121, 2004.
- [28] S. M. Park, L. Jaeseo, and H.-J. Yoo, "1-Gb/s 80-dB Ω fully differential CMOS transimpedance amplifier in multichip on oxide technology for optical interconnects," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 971-974, 2004.
- [29] S.-E. Kim, S.-J. Song, S. M. Park, and H.-J. Yoo, "CMOS optical receiver chipset for gigabit Ethernet applications," in *IEEE International Symposium on Circuits and Systems, ISCAS*, 2003, vol.1, pp. 29-32.
- [30] S. M. Park and C. Toumazou, "A packaged low-noise high-speed regulated cascode transimpedance amplifier using a 0.6 μ m N-well CMOS technology," in *The European Solid-State Circuits Conference, ESSCIRC 2000*, pp. 431-434.
- [31] C. Hermans and M. S. J. Steyaert, "A high-speed 850-nm optical receiver front-end in 0.18 μ m CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 1606-1614, 2006.

- [32] A. Jayakumar, M. S. Bustos, D. Cheskis, S. J. Pietrucha, M. Bonelli, S. Al-Kuran, and N. Scheinberg, "3-V MSM-TIA for Gigabit Ethernet," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1271-1275, 2000.
- [33] M. Lee, O. Vendier, M. A. Brooke, N. M. Jokerst, and R. P. Leavitt, "CMOS optical receiver with integrated InGaAs thin-film inverted MSM detector operating up to 250 Mbps," in *IEEE/LEOS Summer Topical Meetings: Advanced Applications of Lasers in Materials Processing/Broadband Optical Networks/Smart Pixels/Optical MEMs and Their Applications* 1996, pp. 17-19.
- [34] M. Lee, C. Camperi-Ginestet, M. A. Brooke, and N. M. Jokerst, "Silicon CMOS Optical Receiver Circuit With Integrated Compound Semiconductor Thin-film P-i-N Detector," in *IEEE/LEOS Summer Topical Meetings: Integrated Optoelectronics*, 1994, pp. 58-59.
- [35] T. Nakahara, H. Tsuda, K. Tateno, S. Matsuo, and T. Kurokawa, "Hybrid integration of GaAs pin-photodiodes with CMOS transimpedance amplifier circuits," *Electronics Letters*, vol. 34, pp. 1352-1353, 1998.
- [36] O. Vendier, M. Lee, N. M. Jokerst, M. Brooke, and R. P. Leavitt, "Integrated 200 Mbit/s receiver: silicon CMOS transimpedance amplifier with a thin film InGaAs photodetector," in *Conference on Lasers and Electro-Optics, CLEO*, 1996, pp. 402-403.
- [37] H. Zimmermann, R. Swoboda, and H. Zimmermann, "11Gb/s monolithically integrated silicon optical receiver for 850nm wavelength," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC*, 2006, pp. 904-911.

- [38] T. Yoon and B. Jalali, "Front-end CMOS chipset for fiber-based gigabit Ethernet," in *Symposium on VLSI Circuits, Digest of Technical Papers*, 1998, pp. 188-191.
- [39] W.-Z. Chen and S.-H. Huang, "A 2.5 Gbps CMOS Fully Integrated Optical Receiver with Lateral PIN Detector," in *IEEE Custom Integrated Circuits Conference, CICC*, 2007, pp. 293-296.
- [40] M. Kossel, C. Menolfi, T. Morf, M. Schmatz, and T. Toifl, "Wideband CMOS transimpedance amplifier," *Electronics Letters*, vol. 39, pp. 587-588, 2003.
- [41] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1368-1382, 2000.
- [42] S. S. Mohan, M. D. M. Hershenson, S. P. Boyd, and T. H. Lee, "Bandwidth extension in CMOS with optimized on-chip inductors," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 346-355, 2000.
- [43] E. Sackinger and W. C. Fischer, "A 3-GHz 32-dB CMOS limiting amplifier for SONET OC-48 receivers," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1884-1888, 2000.
- [44] A. Zolfaghari, A. Chan, and B. Razavi, "Stacked inductors and transformers in CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 620-628, 2001.
- [45] C.-T. Chan and O. T. C. Chen, "A 10 Gb/s CMOS optical receiver using modified regulated cascade scheme," in *The Midwest Symposium on Circuits and Systems, MWSCAS*, 2005, pp. 171-174.

- [46] W.-Z. Chen, Y.-L. Cheng, and D.-S. Lin, "A 1.8-V 10-Gb/s fully integrated CMOS optical receiver analog front-end," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 1388-1396, 2005.
- [47] W.-Z. Chen and C.-H. Lu, "Design and analysis of a 2.5-Gbps optical receiver analog front-end in a 0.35- μ m digital CMOS technology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, pp. 977-983, 2006.
- [48] W.-Z. Chen and Y.-L. Cheng, "A 1.8 V, 10 Gbps fully integrated CMOS optical receiver analog front end," in *The European Solid-State Circuits Conference, ESSCIRC 2004*, pp. 263-266.
- [49] W.-Z. Chen and W.-H. Chen, "Symmetric 3D passive components for RF ICs application," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Digest of Papers*, 2003, pp. 599-602.
- [50] J. Cao, M. Green, A. Momtaz, K. Vakilian, D. Chung, K.-C. Jen, M. Caresosa, X. Wang, W.-G. Tan, Y. Cai, L. Fujimori, and A. Hairapetian, "OC-192 transmitter and receiver in standard 0.18- μ m CMOS," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1768-1780, 2002.
- [51] C.-M. Tsai, "A 20mW 85dB Ω 1.25Gb/s CMOS transimpedance amplifier with photodiode capacitance cancellation," in *Symposium on VLSI Circuits, Digest of Technical Papers*, 2004, pp. 408-409.
- [52] C.-M. Tsai and W.-T. Chen, "A 40mW 3.5k Ω 3Gb/s CMOS Differential Transimpedance Amplifier Using Negative-Impedance Compensation," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC*, 2007, pp. 582-586.

- [53] Y. Kwisung, L. Dongmyung, H. Gunhee, S. M. Park, and W. S. Oh, "A 1.2V 5.2mW 40dB 2.5Gb/s Limiting Amplifier in 0.18 μ m CMOS Using Negative-Impedance Compensation," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC*, 2007, pp. 56-57.
- [54] C.-M. Tsai, "20 mW 1.25 Gbit/s CMOS transimpedance amplifier with 30 dB dynamic range," *Electronics Letters*, vol. 41, pp. 109-110, 2005.
- [55] C.-M. Tsai, and L.-R. Huang, "A 24mW 1.25Gb/s 13k Ω transimpedance amplifier using active compensation," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC*, 2006, pp. 894-903.
- [56] C.-C. Chen, C.-M. Tsai, D.-U. Li, and L.-R. Huang, "A 1.25 Gbps burst-mode receiver IC with extended dynamic range," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Digest of Papers*, 2005, pp. 625-628.
- [57] Y. Emori, Y. Akasaka, S. Namiki, and J.-W. Park, "Burst-mode optical receiver with two preamplifiers having different bandwidths," *Electronics Letters*, vol. 34, pp. 2146-2148, 1998.
- [58] C. Petri, S. Rocchi, and V. Vignoli, "High dynamic CMOS preamplifiers for QW diodes," *Electronics Letters*, vol. 34, pp. 877-878, 1998.
- [59] S. Galal and B. Razavi, "10-Gb/s limiting amplifier and laser/modulator driver in 0.18 μ m CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 2138-2146, 2003.
- [60] W. W. Hansen, "On maximum gain-band width product in amplifiers," *Journal of Applied Physics*, vol. 16, pp. 528-534, 1945.

- [61] A. K. Petersen, K. Kiziloglu, Y. Ty, F. J. Williams, and M. R. Sandor, "Front-end CMOS chipset for 10 Gb/s communication," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Digest of Papers*, 2002, pp. 93-96.
- [62] D. Guckenberger, J. D. Schaub, and K. T. Kornegay, "A DC-coupled low-power transimpedance amplifier architecture for Gb/s communication system applications," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Digest of Papers*, 2004, pp. 515-518.
- [63] Y. Ota, R. G. Swartz, and V. D. Archer, III, "DC-1 Gb/s burst-mode compatible receiver for optical bus applications," *Journal of Lightwave Technology*, vol. 10, pp. 244-249, 1992.
- [64] M. Nogawa, K. Nishimura, S. Kimura, T. Yoshida, T. Kawamura, M. Togashi, K. Kumozaki, and Y. Ohtomo, "A 10 Gb/s burst-mode CDR IC in 0.13 μ m CMOS," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC*, 2005, pp. 228-230.
- [65] M. Nogawa, Y. Ohtomo, S. Kimura, K. Nishimura, T. Kawamura, and M. Togashi, "A 10Gb/s burst-mode adaptive gain select limiting amplifier in 0.13 μ m CMOS," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC*, 2006, pp. 940-949.
- [66] M. Nakamura, N. Ishihara, and Y. Akazawa, "A 156-Mb/s CMOS optical receiver for burst-mode transmission," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1179-1187, 1998.
- [67] M. Nakamura, N. Ishihara, Y. Akazawa, and H. Kimura, "A wide-dynamic-range and extremely high-sensitivity CMOS optical receiver IC using feed-forward

- auto-bias adjustment," in *IEEE Custom Integrated Circuits Conference, CICC*, 1994, pp. 629-632.
- [68] M. Nakamura, N. Ishihara, Y. Akazawa, and H. Kimura, "An instantaneous response CMOS optical receiver IC with wide dynamic range and extremely high sensitivity using feed-forward auto-bias adjustment," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 991-997, 1995.
- [69] P. Ossieur, D. Verhulst, Y. Martens, C. Wei, J. Bauwelinck, Q. Xing-Zhi, and J. Vandewege, "A 1.25-Gb/s burst-mode receiver for GPON applications," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 1180-1189, 2005.
- [70] P. Ossieur, Y. C. Yi, J. Bauwelinck, X. Z. Qiu, J. Vandewege, and E. Gilon, "DC-coupled 1.25 Gbit/s burst-mode receiver with automatic offset compensation," *Electronics Letters*, vol. 40, pp. 447-448, 2004.
- [71] K. Nishimura, H. Kimura, M. Watanabe, T. Nagai, K. Nojima, K. Gomyo, M. Takata, M. Iwamoto, and H. Asano, "A 1.25-Gb/s CMOS burst-mode optical transceiver for ethernet PON system," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 1027-1034, 2005.
- [72] Y.-H. Oh, S.-G. Lee, Q. Le, H.-Y. Kang, and T.-W. Yoo, "A CMOS burst-mode optical transmitter for 1.25-Gb/s ethernet PON applications," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 52, pp. 780-783, 2005.
- [73] Q. Le, S.-G. Lee, Y.-H. Oh, H.-Y. Kang, and T.-W. Yoo, "A burst-mode receiver for 1.25-Gb/s ethernet PON with AGC and internally created reset signal," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 2379-2388, 2004.

- [74] H. Y. Huang, J. C. Chien, and L. H. Lu, "A 10-Gb/s Inductorless CMOS Limiting Amplifier With Third-Order Interleaving Active Feedback," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 1111-1120, 2007.
- [75] S. Galal and B. Razavi, "40Gb/s amplifier and ESD protection circuit in 0.18 μ m CMOS technology," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC*, 2004, vol.1, pp. 480-541.
- [76] C.-T. Chan and O. T. C. Chen, "Inductor-less 10Gb/s CMOS transimpedance amplifier using source-follower regulated cascode and double three-order active feedback," in *IEEE International Symposium on Circuits and Systems, ISCAS*, 2006, pp. 5487-5490.
- [77] E. A. Crain and M. H. Perrott, "A 3.125 Gb/s limit amplifier in CMOS with 42 dB gain and 1 μ s offset compensation," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 443-451, 2006.
- [78] M. Nakamura, Y. Imai, Y. Umeda, Jun Endo, and Y. Akatsu, "1.25-Gb/s burst-mode receiver ICs with quick response for PON systems," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 2680-2688, 2005.
- [79] Q. Le, S.-G. Lee, Y.-H. Oh, H.-Y. Kang, and T.-W. Yoo, "Burst-mode receiver for 1.25Gb/s Ethernet PON with AGC and internally created reset signal," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC*, 2004, vol.1, pp. 474-540.
- [80] J.-W. Seo, S. Han, S.-G. Lee, M.-S. Lee, and T. W. Yoo, "A 1.25 Gb/s high sensitive peak detector in optical burst-mode receiver using a 0.18 μ m CMOS

- technology," in *International Conference on Communication Technology Proceedings, ICCT*, 2003, vol.1, pp. 644-646.
- [81] K. Nishimura, H. Kimura, M. Watanabe, T. Nagai, K. Nojima, K. Gomyo, M. Takata, M. Iwamoto, and H. Asano, "A 1.25Gbit/s CMOS burst-mode optical transceiver for Ethernet PON system," in *Symposium on VLSI Circuits, Digest of Technical Papers*, 2004, pp. 414-417.
- [82] T. De Ridder, P. Ossieur, B. Baekelandt, C. Melange, J. Bauwelinck, C. Ford, X.-Z. Qiu, and J. Vandewege, "A 2.7V 9.8Gb/s Burst-Mode TIA with Fast Automatic Gain Locking and Coarse Threshold Extraction," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC*, 2008, pp. 220-221.
- [83] A. Hastings, *The art of analog layout* Pearson Prentice Hall, 2006.
- [84] C.-F. Liao and S.-I. Liu, "40 Gb/s Transimpedance-AGC Amplifier and CDR Circuit for Broadband Data Receivers in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 642-655, 2008.
- [85] W.-Z. Chen and R.-M. Gan, "A Single Chip 2.5 Gbps CMOS Burst Mode Optical Receiver," in *Symposium on VLSI Circuits (VLSI), Digest of Technical Papers*, 2006, pp. 120-121.