Poly(vinylidene fluoride-trifluoroethylene) ferroelectric polymer for non-volatile memory applications

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**POLY(VINYLDENE FLUORIDE –
TRIFLUOROETHYLENE) FERROELECTRIC POLYMER
FOR
NON-VOLATILE MEMORY APPLICATIONS**

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ABSTRACT

Ferroelectric copolymer, poly(Vinylidene fluoride – trifluorine ethylene) P(VDF-TrFE), has been investigated for the application in non-volatile memory. Thin films by spin-coating have been characterized for changes in surface morphology, crystalline structure and electrical properties induced by thermal annealing and corona poling. Topography of rod-like structure is correlated to the film semi-crystallinity which is strongly dependent on thermal annealing and can be modified into better order by corona poling. Measurements of dielectric properties below glass transition temperature lead to findings of free charge carrier concentration and interface charge density in the P(VDF-TrFE) film that are matched to devices formed by interfacing with semiconductor layer. Schottky contact is suggested to form at the ferroelectric and semiconductor interface which governs the behavior of the field effect transistor device. Organic ferroelectric field effect transistors (FeFET) are presented with investigation into mechanism of memory functionality, switch-on behavior as well as the anomalous observation of turn-on voltage shift and double polarization switching. While the voltage shift is resulted from fixed dipoles and trapped charges at the interface, the double switching is caused by field distribution due to potential difference between electrodes. Organic FeFET fabricated from complete solution process are also presented with various device structures, which lead to understandings in device performance control. Application of solution process for flexible devices which are examined in mechanically deformed states is shown with critical stress value being determined. A new method of stretching thin film attached to a plastic substrate is demonstrated to improve surface morphology and obtain comparable polarization properties at lower working temperature. Due to the smoother topography and good polarization, performance of the organic FeFET is enhanced with better drive current characteristics. Langmuir-Schaffer transfer method is employed for the formation of nanostructures of islands, mesas, wells and ultrathin films. Types and dimensions of the nanostructures are found to depend on annealing temperatures and surface amphiphilicity. Ultrathin ferroelectric film shows substantial and stable polarization switching which can be employed for low-voltage organic capacitor and FeFET devices.

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LIST OF ABBREVIATIONS

AC	Alternating current
AFM	Atomic force microscopy
Al	Aluminum
CV	Capacitance – voltage
DC	Direct current
DSC	Differential scanning calorimetry
FeFET	Ferroelectric field effect transistors
FET	Field effect transistors
FTIR	Fourier transform infra-red
FWHM	Full width half maximum
ITO	Indium-doped tin oxide
IV	Current – voltage
I_D - V_G	Drain current vs. gate voltage
I_G - V_G	Gate current vs. gate voltage
LB	Langmuir – Blodgett
LS	Langmuir – Schaefer
MEK	Methyl ethyl ketone
MFIS	Metal – ferroelectric – insulator – semiconductor
MFM	Metal – ferroelectric – metal
OFeFET	Organic ferroelectric field effect transistors
PEN	Polyethylene naphthalate
PET	Polyethylene terephthalate
PQT	Poly (3,3''-diakyl quaterthiophene)
PVDF	Poly(Vinylidene fluoride)
P(VDF-TrFE)	Poly(Vinylidene fluoride – trifluoroethylene)
PZT	Lead zirconium titanate
RAM	Random access memory
Si	Silicon
UV-vis	Ultraviolet to visible light range
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction

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Journals:

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4. C. A. Nguyen, P. S. Lee, and S. Mhaisalkar, "*Enhanced Ferroelectric Field Effect Transistor Characteristics with Strained Poly(Vinylidene fluoride–trifluoroethylene) Dielectric*" (under review).
5. C. A. Nguyen, P. S. Lee, and S. Mhaisalkar, "*Ultra-thin ferroelectric copolymer P(VDF-TrFE) films by Langmuir-Schaefer transfer for nanostructure formation and memory application*" (under review).
6. C. A. Nguyen, P. S. Lee, and S. Mhaisalkar, "*Effects of free charges in devices with ferroelectric polymer P(VDF-TrFE) and organic semiconductor interface*" (manuscript submitted).

Conference Proceedings:

1. C. A. Nguyen, and P. S. Lee, "*Capacitance-voltage measurement in memory devices using ferroelectric polymer*", proceedings of SPIE 6037, Dec 2005.
2. C. A. Nguyen, and P. S. Lee, "*Ferroelectric copolymer P(VDF-TrFE) as gate dielectric in organic field effect transistors for memory application devices*", NanoSingapore 2006 - IEEE Conference on Emerging Technologies, 179 (2006).

Patent:

1. C. A. Nguyen, P.S. Lee, and S. Mhaisalkar, "*Thin Films Subjected to Stretching and Annealing for Application in Printed Electronics*" (in preparation).

Chapter 1

INTRODUCTION

1.1 Background and Motivation

Since the first study of Rochelle salt by Valasek in 1920s, ferroelectric materials have attracted great attention for their unique properties and possible device applications [1]. They exhibit stable macroscopic polarization or net dipole that can be repeatably switched by an external electric field between equal-energy states of opposite polarization [2]. In general, ferroelectric materials can be both inorganic and organic. Inorganic materials include compound ceramics in which the most well-known is perovskite type, e.g. lead zirconium titanate (PZT), barium titanate etc. The organic counterparts consist of Poly(Vinylidene-fluoride) (PVDF) with copolymer family, Nylon, and some liquid crystals.

Deposition of ferroelectric materials in the form of thin film has been investigated for applications ranging from sensors, actuators, transducers, microelectro-mechanical systems (MEMS) and non-volatile memory devices. With a long history of research and establishments, new application of ferroelectric ceramic thin film for random access memory (RAM) technologies have been recently announced and produced by companies such as Hitachi Ltd., NEC Corporation, Ramtron International Corporation etc. [3]. This fully proves the applicability of ferroelectric materials in industrial manufacturing.

Ferroelectricity in organic materials has been only observed since the first discovery of piezoelectricity in PVDF by Kawai in 1969 [4]. However, their advantages have been quickly recognized including the ease of fabrication process (low energy and temperature), good conformation, smooth surface, robust mechanical and chemical properties, and much less toxicity etc. Although some properties of these materials (remanent polarization, fatigue strength, switching time etc.) are inferior due to semi-crystalline and less ordered structure as compared to ceramics, researches in properties and device applications have been intensive and well-accomplished. Other efforts have

also been put in tailoring chemical structure [5] for specific applications and designing of new device structures. With the invention and development of new organic semiconducting materials, fabrication of all-organic non-volatile memory devices, which are useful in simple circuits, is enabled by combining with the ferroelectric counterpart. These new types of electronic devices can be produced at cheaper cost and with simpler structure compared to current Silicon technology.

1.2 Objectives

This thesis aims to investigate the application of ferroelectric copolymers P(VDF-TrFE) for non-volatile memory devices by

- Examining the material properties and intrinsic characteristics of device (organic ferroelectric field effect transistors) operation
- Optimizing device fabrication with various techniques (e.g. solid-state, solution process), different substrate types (e.g. conventionally rigid, flexible plastic), and device architectures.
- Exploring new methods to enhance the properties of materials and device applications.

1.3 Summary of all chapters

Chapter 1 is shown with a brief introduction about the background, motivation and the objectives of the project. More detailed information relating to materials, device, performance etc. will be reviewed in Literature survey of Chapter 2. Technical data and analysis will be presented in Chapter 3 onwards. In Chapter 3 structure characterization and modification by corona poling of ferroelectric copolymer thin film will be shown. Chapter 4 presents study in the dielectric and polarization hysteresis properties of thin film metal-polymer-metal devices with varied signal frequency and measurement temperature to understand the effect of free charge carrier in ferroelectric film alone and its interface with an organic semiconductor. Device performance of organic ferroelectric

field effect transistor will be examined for memory functionality and switching behaviors in Chapter 5. The anomalous shifting of turn-on voltage and double polarization switching will also be studied. Chapter 6 will report a new method of optimizing the ferroelectric properties of the P(VDF-TrFE) copolymer thin film attached to plastic substrate at lower temperature by uniaxially stretching. Improved device performance of FeFET will also be discussed. Device fabrication by solution process for the realization of low-cost devices will be investigated in Chapter 7. Application of these devices in flexible conditions under effect of bending and tensile stress will also be reported. Fabrication of nano-size features of islands and wells as well as ultrathin films by Langmuir-Schaffer transfer methods. Application for FeFET devices will also be explored. Finally Chapter 9 will conclude the project and provide some further recommendations.

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Chapter 2

LITERATURE SURVEY

2.1 Theory of dielectric and ferroelectric polarization

The source of dielectric displacement $\mathbf{D}$ [1,2,3] is given by the density of free (conducting) charges ρ following Poisson equation: $\nabla \cdot \mathbf{D} = \rho_{free}$ (2.1)

The overall charge neutrality of matter in an external field is described by:

$$\mathbf{D} = \epsilon_0 \mathbf{E} + \mathbf{P} \quad (2.2)$$

The vacuum contribution caused by externally applied electric field is represented by the term $\epsilon_0 \mathbf{E}$, and the electrical polarization of matter in the system is described by $\mathbf{P}$. This relation is independent of nature of polarization which could be pyroelectric, piezoelectric or dielectric polarization (by an external electric field). For a pure dielectric response of matter, polarization is proportional to electric field in linear approximation by

$$\mathbf{P} = \epsilon_0 \chi_e \mathbf{E} \quad \text{hence} \quad \mathbf{D} = \epsilon_0 \mathbf{E} + \epsilon_0 \chi_e \mathbf{E} = \epsilon_0 \epsilon_r \mathbf{E} \quad (2.3)$$

Dielectric susceptibility χ_e is related to relative permittivity ϵ_r by $\chi_e = (\epsilon_r - 1)$. However this linearity is only valid for small fields and non-ferroelectric materials. In the case of ferroelectric materials, dielectric properties are strongly non-linear that leads to sub-loops of hysteresis as shown in Figure 2.1 [4].

Figure 2.1 – DC bias dependence of dielectric constant of (a) dielectric and (b) ferroelectric material under strong AC field potential (adopted from [4]).

In general there are five different mechanisms of polarization which can contribute to dielectric response [4] e.g.

- (a) **Electronic polarization** exists in all dielectrics. It is based on displacement of negatively charged electron shell against positively charged core.
- (b) **Ionic polarization** is observed in ionic crystals and describes the displacement of positive and negative sub-lattices under an applied field.
- (c) **Orientation polarization** describes the alignment of permanent dipoles. At ambient temperatures, all dipole moments usually have statistical distribution of their directions. An electric field generates a preferred direction for dipoles, while thermal movement of atoms perturbs this alignment.
- (d) **Space charge polarization** could exist in dielectric materials which show spatial inhomogeneities of charge carrier densities. Space charge polarization effects are not only of importance in semiconductor field-effect devices, they also occur in ceramics with electrically conducting grains and insulating grain boundaries (so-called Maxwell-Wagner polarization).
- (e) **Interfacial polarization at domain wall regions** plays a decisive role in ferroelectric materials and contributes to the overall dielectric response. The motion of a domain wall that separates regions of different oriented polarization takes place by the fact that favored oriented domains with respect to applied field tends to grow.

An ideal ferroelectric single crystal shows $P(E)$ behavior as depicted in Figure 2.2(a). Non-ferroelectric dielectric ionic and electronic polarization contributions are clearly linear horizontal lines and orientation polarization is manifested by spontaneous polarization P_s . To reverse the polarization, an electric field with amplitude $E > E_c$ is required. In opposite to single crystal ferroelectric, poly-domain possesses a smaller remnant polarization P_r than P_s due to back-switching even for opposite fields. In this case P_s can be estimated by extrapolation to $E = 0$. To obtain hysteresis curve (full line) a voltage combining of DC (polygonal step) and AC field (triangular shape) is applied to a thin film sample with DC ramping from zero to a value that saturation polarization is

reached (point A). Voltage is then reversed direction ($A \rightarrow B$), value of polarization is preserved due to unchanged alignment of permanent dipoles corresponding to field direction during the first step. However, only value of $P_r (\leq P_s)$ is obtained at zero fields because of back-switching and relaxation behavior of ionic and electronic dielectric. If voltage is further reversed to opposite direction ($B \rightarrow C$), poly-domain of permanent dipoles starts switching to the new field direction provided that applied field is greater than coercive field of each domain. Polarization reduces to zero at point C or coercive field value E_c of the sample, indicating that all permanent dipoles have been switched to 180° domains for which sum of polarization vector is zero. An applied voltage higher than E_c will rotate dipoles to new opposite direction and to saturation (point D). Reversing process ($D \rightarrow E \rightarrow F \rightarrow A$) is explained similarly as above.

Figure 2.2 – (a) Ferroelectric hysteresis of single crystal (dash line) and polycrystalline sample (full line), (b) Correlation of polarization-voltage, capacitance-voltage, and current-voltage of ferroelectric thin film (adopted from [5]).

Figure 2.2 (b) gives a better differentiation between switching and non-switching components of polarization mechanism by observing correlation of polarization (PV), capacitance (CV) and current (IV) simultaneously. It is clear that for pure switching case, during saturation and as $E \rightarrow 0$, polarization is unchanged, capacitance and current are zero. Yet in the other case, ionic and electronic polarization appears in pre-existing capacitance and reduction of polarization (dielectric relaxation). These polarizations

always exist in materials as described above however they may also come from defects of trapping charges or interface mismatch of film and electrodes.

2.2 P(VDF-TrFE) thin film

The study and application of ferroelectric polymers date back to around 1969 with the discovery of piezoelectricity in PVDF by Kawai [6]. Properties of ferroelectric polymers – mainly PVDF and its copolymer [8] and odd nylons [10] have been reviewed by Furukawa [8], Lovinger [9], Esayan et al [10], and Wang et al [7].

Figure 2.3 – Conformation and crystalline forms of PVDF (adopted from [3]).

As showed in Figure 2.3, PVDF is a non-conjugated linear fluorinated hydrocarbon with a dipole moment pointing roughly from fluorine to hydrogen on each monomer. It has been found that PVDF material is semicrystalline of which there are three most common conformations e.g. all-trans ($TTTT$), alternating left-right trans-gauche ($TGT\bar{G}$), and helical (TGTG) or ($T\bar{G}T\bar{G}$). All three conformations form straight cylindrical chains that crystallize in a quasi-hexagonal packing. The all-trans ($TTTT$) crystallite has orthorhombic $m2m$ structure with chains along the crystal c-axis and dipoles align

approximately along the crystal b-axis. This so-called “ β -phase” (or form I) is polar and uniaxial ferroelectric, as polarization can be repetitively switched between opposite but energetically equivalent directions along 2-fold b-axis. The paraelectric phase or “ α -phase” (form II) is composed of chains with alternating trans-gauche ($TGT\bar{G}$) conformation packing with no macroscopic polarization. The last helical conformation is regarded as “ γ -phase” (form III) with certain amount of ferroelectricity but may be only metastable.

PVDF had also been copolymerized, in random sequence, with trifluoroethylene (TrFE) $[-(\text{CHF}-\text{CF}_2)-]$ and tetrafluoroethylene (TeFE) $[-(\text{CF}_2-\text{CF}_2)-]$. The reversed monomers (unavoidably introduced from synthesis) and TrFE or TeFE units function as defects, tending to lower ferroelectric transition temperatures. Figure 2.4 shows phase transition diagram of copolymer P(VDF-TrFE). The copolymers also have slightly larger unit cell and smaller average dipole moment than pure PVDF, owing to replacement of some of hydrogen atoms by larger fluorines [3].

Figure 2.4 – Phase transition diagram for various compositions VDF and molecular structure of copolymer (adopted from [11]).

Thin film samples prepared by solvent-casting and spin-coating methods are polymorphous, containing amorphous materials and lamellar crystallites, often with more

than one phase. The needle-shaped crystallites tend to form radial spherulite balls [7], where crystalline regions are strained by the dangling and looped chain segments and embedding amorphous materials. The relative proportion of amorphous and crystalline phase strongly depends on thermal, mechanical, and electrical treatments of samples, making it difficult to identify equilibrium features associated with ferroelectricity. PVDF essentially does not crystallize from the melt and crystallizes only poorly from solution. Film sample must be treated mechanically by stretching to align polymer chains and electrically to align polarization axes of the crystallites. Mechanical and electrical alignment results in macroscopic piezoelectric behavior, though the samples still contain about 50% amorphous content and the crystallites are incompletely oriented [7,8,9]. However copolymer P(VDF-TrFE) crystallizes readily from the melt and can be stretched and electrically polarized to over 90% crystallinity [7,9,12]. Recently, refined treatments significantly are shown to improve crystallization of copolymer films, apparently eliminating amorphous phase to produce single-crystalline phase [13,14].

For application of thin film devices, Wang et al [7] discussed a wide variety of methods, including: film extrusion (e.g. slot-die casting of single sheets and multi-sheets, blown (bubble) films, thermal lamination) and solvents casting. Some of the orientation techniques were also recommended such as uniaxial/biaxial stretching, oven stretching, roll drafting, compression rolling, chill wheel extrusion and orientation, tentering. However most of the methods of film formation and orientation (except for solvent casting) are only applicable for stand-alone film devices which do not require supporting substrate. For microelectronic device application, there is always requirement for integration of materials into electrical circuit to electrically operate as one. Therefore, thin film prepared from solution is the most suitable method.

Raw materials of copolymers, usually in powder or pellet form, are dissolved in polar solvents as acetone, dimethylformamide (DMF), dimethylacetamide (DMA), dimethylsulfoxide (DMSO), hexamethylphosphoric triamide (HMPA), and methyl ethyl ketone (MEK). It has been found that dipole moment of solvent also affects the formation of crystalline phase in thin film as well as absorption of water or moisture during

processing [15]. Solution, after being prepared by mechanical or ultrasonic stirring and optional heating at a certain concentration, is then directly applied to substrate and thin film is formed either by self-evaporation of solvent (solution casting) or enhanced evaporation by spinning of substrate (spin-coating). Comparing to solution casting, spin-coating gives better control of film thickness, uniformity and surface morphology. Film thickness can be controlled by spinning speed, ramping rate, solution concentration and dispensing volume. Xia et al investigated thickness dependence of P(VDF-TrFE) spin-coating film on polarization switching. The result was found that thin films of thickness below 100 nm had large reduction of remnant polarization and increment of switching time [20]. However further investigation of polarization switching of below 100nm P(VDF-TrFE) film showed that the drastic remnant reduction is possibly due to the usage of Aluminum electrode which may react to form a thin oxide layer at the interface. The use of PEDOT:PSS as electrode has been proven to suppress this reduction due to better wetting and adhesion between organic layers [39]. Spin-coated film is subsequently refined through post-annealing and electrical poling to improve ferroelectric properties.

Another method that has been recently investigated for accurate deposition of monolayer of ferroelectric polymer is Langmuir-Blodgett (LB) film transfer. An amphiphilic molecule is dispersed on the surface of a liquid subphase and compressed laterally into a dense film of one molecule thickness – one monolayer. This film can then be transferred to substrate by very slow dipping substrate into the solution. Thicker film can be built-up by repeated dipping. Although VDF-TrFE molecules are not good amphiphiles, it has been reported excellent ferroelectric films can be produced with polarization hysteresis measured by pyroelectric current and clear ferroelectric-paraelectric phase transition [3].

As found out by Furukawa [8], annealing of thin copolymer film at temperature below melting point enhances crystallization in which more ferroelectric phase is formed as presented in Figure 2.4. Therefore, range of interest for annealing temperature is from 130 to 145°C. Result of crystallization improvement can be observed through X-ray diffraction, electron diffraction microscopy, Fourier transformed Infra-red and Raman spectroscopy [16]. A typical wide angle XRD spectrum is presented in Figure 2.5.

Characteristic diffraction peaks for crystalline phase recognition are observed in range from 17° to 21° , with paraelectric phase (diffracted from (110) planes) at around 18.2° - 18.4° and the ferroelectric counterpart (diffracted from (200) planes) at 19.6° - 19.8° . Quantification of peak intensity allows determination of phase composition in sample.

Figure 2.5 – XRD spectrum of P(VDF-TrFE) thin film showing coexistence of paraelectric and ferroelectric phase (adopted from [17]).

Several methods have been discussed above to enhance the ferroelectric phase however refinement by mechanical means are only suitable for stand-alone film. To enable refinement of film on substrate, electrical field is utilized due to response of dipoles to field direction. An original method of electrical poling is to create a pair of metal electrodes that sandwich copolymer film and a voltage is correspondingly applied to the electrodes depending on the preferred orientation. This has been used in several cases of single gate for capacitor [18, 19] or double metal gate in FET devices [19]. However there are always issues of interface between polymer film and electrode which results defects or trapped charges that diminish film quality. A new method has been proposed for poling using a corona discharge source [21, 22] or plasma source [23]. Phase transformation from paraelectric to ferroelectric can be observed from the increment of ferroelectric XRD intensity peak compared to that of paraelectric ones.

2.3 Organic semiconducting materials for low cost application

Metallic-like electronic conduction was first discovered and reported in organic material (all trans polyacetylene) in 1977 [24]. The conduction mechanism is enabled by conjugated bonding system of the carbon backbone in which there is an alternation of

single and double bonds. The discovery has been proven to be scientifically important for the development of wide range of applications and new interdisciplinary research areas of chemistry and physics. The impressive fast-pacing progress in this field can be observed from a tremendous quantity of research data and available information that deepen the knowledge and inspire new practical applications [25-29].

In terms of processing methods, organic semiconducting materials are divided into two types of fabrication: by vacuum evaporation and by solution deposition. Thermal evaporation in low vacuum is applicable for chemical of low molecular weight, so-called "small-molecules" e.g. pentacene, hexathiophene (and derivatives) etc. Device fabrications from these materials possess good properties due to high quality crystalline thin films that can be obtained by slow evaporation [25]. However their applications are limited by the stringent conditions of depositing process. For the method by solution, device fabrication is made simple by usage of diluted solution in normal ambient environment with spin-coating or drop-casting process. This allows the amount of materials and the overall cost of products to be drastically reduced. Some of these materials include polyaniline (PANI), poly(3,4-ethylenedioxythiophene):poly(styrene sulfonic acid) (PEDOT:PSS), polythiophene derivatives (P3HT, PQT) etc. [26,27]. Based on either method, good quality thin film of semiconducting materials can be obtained suitable for electronic device application [25,29].

2.4 Ferroelectric capacitors and field effect transistors

Capacitor and field effect transistor (FET) are elements in integrated circuit of memory devices especially for non-volatile random memory access (RAM). Circuit designs have been using as 1T-1C, 1T-2C, or 2T-2C (T-transistor, C-capacitor). With integration of ferroelectric thin film into stacking gate of FET, which makes the gate become polarizable, usage of capacitor can be reduced. Compared to the capacitor-type FeRAM, ferroelectric gate FET devices allow non-destructive reading operation as well as smaller cell size. However the incorporation of ferroelectric materials into the stacking dielectric

layer of the transistor may pose some serious problem to the operation of the device. Some of the well-known issues of ferroelectric device are depolarization field and retention problem due to leakage current. While solving these problems in the FeFET device may require to compromise certain of performance properties (e.g. usage of buffer layer to reduce gate leakage which also changes the gate dielectric value), using capacitor-type or mixed capacitor-transistor type device enable the problems to be remedied separately. For organic FeRAM, besides the advantages mentioned above the usage of FeFET device is more preferable as it helps to simplify the device fabrication in which the organic semiconductors can be critically degraded through various steps of patterning. Incorporating of ferroelectric and semiconductor to the same location ensures the limitation of patterning steps and preserve the integrity of the conducting materials. Moreover as compared to the transistor – capacitor type, the operating speed of the cell is limited by the capacitance charging/discharging rate and the RC component of the organic semiconductor circuit, which subsequently affects the turning on/off of drain current. Therefore, the usage of stacking ferroelectric layer into the insulator can also improve the operating speed of the whole transistor device ($\sim 500 \mu\text{s}$ [33]).

Figure 2.6 – MFIS capacitor structure and CV characteristic data (adopted from [18]).

Figure 2.7 – Structure and IV characteristic of ferroelectric FET based on Silicon technology (adopted from [31]).

Capacitor devices can come in two structures e.g. ferroelectric polymer film sandwiched between two metal electrodes (MFM) and stack of metal-ferroelectric-insulator-seiniconductor (MFIS). While an MFM capacitor exhibits a "butter-fly" CV curve which is useful for understanding electrical transition processes, an MFIS shows a CV curve with areas of accumulation, depletion and inversion. Analysis of MFIS capacitance curve enables us to examine ON/OFF stage by capacitance amplitude difference and voltage memory window of device. Figure 2.6 shows structure of MFIS device and its CV data. As voltage applied to top gate changes it sweeping direction, turn-on voltage of capacitor also shifts accordingly that creates a memory window. It is also noted that shifting of turn-on voltage only occurs as applied voltage must be higher than a certain value, which well agrees with switching of dipoles when a field higher than coercive filed is applied.

Figure 2.8 – Organic ferroelectric thin film transistor using MEH-PPV as semiconducting channel (adopted from [33]).

FET is the most important device of an integrated circuit. By making the transistor gate polarizable, FET can also show memory characteristic through shifting of device turn-on voltage. Several researchers have been reported on application of P(VDF-TrFE) in FET in both conventional Silicon and new organic semiconducting material technology. Figure 2.7 showcases application in Silicon technology in which P(VDF-TrFE) is used as memory layer with backing insulator layer [31]. Advantages of this process include low drive voltage, high current intensity and ON/OFF ratio ($\sim 10^7$) however the main drawback is the complication and difficulties of integration process. Yamauchi reported seven-step process for making of this device [31] yet some steps are not fully compatible for polymer processing due to high temperature (sputtering), chemical attack (etching) etc.

As a result, research in this field has been diverted to new direction since the invention of organic semiconducting materials [30]. Ideas of fabricating all organic ferroelectric FET have been proceeded into real devices with reasonable results for memory function [32,33]. Figure 2.8 shows the design and performance of bottom gate organic thin film transistor using Poly[2-methoxy,5-(2'-ethyl-hexyloxy)-*p*-phenylenevinylene] (MEH-PPV) [33]. The operating mechanism is observed to be similar to the normal transistor behavior. P-type materials is usually used for transistor due to better hole mobility which is resulted from hopping mechanism of charge transfer though devices with n-type materials have also been demonstrated [33].

2.5 Application of thin film

2.5.1 Non-volatile memory

The hybrid ferroelectric field effect device is the current choice for commercial ferroelectric memory made with PZT and similar perovskite ferroelectrics [34, 35]. By optimizing film fabrication and post-treatment, it is able to decrease coercive field and switching time for ferroelectric polymer devices. This is more promising with the fast-switching behavior observed from ultrathin LB film [3].

2.5.2 Wide-Band Imaging

Deposition of ferroelectric polymer thin films is inexpensive and can directly be deposited on integrated charge sensing array and covered with counter-electrodes and an absorbing coating [3]. With proper coatings it should be possible to make an array sensitive to wavelengths ranging from microwave to X-ray region. This enables usage of polymer film in low price pyroelectric detectors and imaging systems.

2.5.3 Piezoelectric transducer, actuator and sensors

PVDF is now widely used in electrochemical actuators, switches, strain gauge, accelerometers, and acoustic transducers for ultrasound and sonar [36]. Recently electron radiation studies demonstrate conversion of P(VDF-TrFE) from ferroelectrics to relaxors, producing strain of several percentages that creates new application area for the copolymer [37, 38].

2.5.4 Capacitors and Energy storage

By utilizing the same method of electron radiation, it has been shown that dielectric constant increased five fold and stabilization of this value over wide temperature range for P(VDF-TrFE) [37, 38]. This allows high charge capacitors and high energy storage capacity device to be made from the copolymer. A multilayer capacitor made from these films can revolutionize portable power, lightening many mechanical and electronic devices that use heavy capacitors or batteries.

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Chapter 3

CHARACTERIZATION OF P(VDF-TrFE) THIN FILM AND STRUCTURAL CHANGES BY HEAT TREATMENT AND ELECTRICAL POLING

3.1 Introduction

Though the characteristics of surface morphology and crystallization of ferroelectric copolymer have been under intensive studies over the last few decades, the main results have been focused on the mechanisms of crystalline formation and transformation among the known phases e.g. α , β , γ [1,2,3]. These findings and understandings however provide broadly useful fundamentals in explaining the physical properties of P(VDF-TrFE) in the aspect of real applications [4,5]. In most of the cases, the studies used either thick films (> 20 μm) prepared by mechanical methods (pressing, extruding) or very thin film (< 50 nm) by solution cast. Due to the good crystallinity of the thick films, it helps to obtain the findings without the interference of the amorphous phase [6]. As for the very thin films, it allows the property characterization down to single crystalline domains [7]. For films with thickness in the middle range of 0.1-10 μm , they are probably more useful in practical applications due to lower driving voltage and better mechanical strength.

While thick ferroelectric polymer films are usually used as stand-alone part in many applications, thin film is an essential functional layer in multi-layered devices. Characteristics of poled films supported by a substrate are hence of great interest as structural changes by poling are constrained by the film-substrate adhesion. Furthermore, in multilayered functional films, surface morphology of the poled films is also important in understanding the interfacial formation and functional interactions within the multilayered structure. One such example is the application of P(VDF-TrFE) thin films in organic non-volatile memory devices in which the ferroelectric copolymer layer is deposited on a substrate surface and forms direct interfacial contact with an organic semiconducting film [4]. Such devices hold a great promise of realizing low-cost non-volatile memory devices that could be either used in all plastic electronic-applications [4] or could potentially be integrated with Si devices [8].

In this chapter, changes in surface morphologies and crystalline structure of thin P(VDF-TrFE) film are examined to obtain the optimized condition for fabricating good quality film for device applications in subsequent chapters. It will also focus on the usage of corona poling method to understand the crystallizing of copolymer film that affects crystallinity, surface morphology and chemistry.

3.2 Experimental

Filtered P(VDF-TrFE) (70-30 mol%) solution in MEK of 30 mg/cc concentration was used for spin-coating thin films of 330-400 nm thickness depending on substrate materials. Different types of substrates (e.g. ITO-glass, aluminum-coated glass, bare glass, and Silicon wafer) were used and cleaned using three-step process of acetone, methanol and deionized water in an ultrasonic bath.

Due to low boiling point of MEK solvent, the spin-coated films were usually dried in the oven for 10 minutes at ambient temperature before annealing. For inert gas annealing, Nitrogen was used to fill in the chamber at pressure of 0.5 bar and maintained throughout the process. For vacuum annealing, a base pressure of 10^{-4} torr was reached before the ramping-up was started. The final pressure of 7×10^{-6} torr was also maintained throughout the process. All samples were annealed for 2 hours with the ramping rate as shown in Table 3.1

Table 3.1 – Details of annealing process

Annealing	Ramp-up/down	Holding time	Pressure
Nitrogen gas	10°C/min	2 hours	–0.5 bar
Vacuum	1°C/min	2 hours	7×10^{-6} torr

Surface morphology of samples was examined by Atomic force microscopy (AFM) (Digital Instrument Dimension 3100). Film crystalline structure was characterized using CuK α source X-Ray Diffractionmeter (XRD) of Rigaku with vertical goniometer and

Bruker AXS D8 DISCOVER with 2-dimensional (2D) general area diffraction detector system. The incident angle was kept at $0.5\text{--}1^\circ$ and scans were done in theta-2theta mode. Absorption spectra were measured by Ocean Optics USB4000 spectrometer using reflectance mode in the wavelength range from 200-850nm. Blank ITO-glass was initially scanned at the glass surface to serve as reference. X-ray photoelectron spectra were recorded with PHI 5600 spectrometer using $\text{MgK}\alpha$ (1253.6 eV) source at base pressure of 3.5×10^{-9} torr. The measurement was performed with non-monochromatic resolution and at pass energy of 23.5 eV. High frequency capacitance – voltage (CV) data were obtained from HP4284 LCR meter, operating at 1 MHz, 15 mV amplitude and forward/reversed voltage sweeping.

Figure 3.1 – Corona poling set-up.

For the study of corona-poling, filtered copolymer solution was spin-coated on the glass side of ITO-glass substrates. Some samples were pre-annealed in N_2 gas as described. They were then poled at either room temperature (25°C) or elevated temperature (hot-poled) (145°C) as listed in Table 3.3. The corona poling set-up was completely enclosed by a heating chamber (dashed enclosure in Figure 3.1) which controlled the poling temperature. For hot-poling (samples 1 and 4), the corona charge was maintained as the temperature was cooled from poling temperature of 145°C to room temperature (25°C). Room temperature samples were kept under the field for the same duration of two hours. The corona field was kept in constant voltage mode and the current in the circuit was

monitored. The metal-polymer-metal capacitor devices were fabricated by thermal evaporation of gold electrodes onto the P(VDF-TrFE) film using a shadow mask.

Table 3.2 – Details of experimental poling samples

Sample	Annealing	Poling
(1)	YES	+6 kV at 145°C in ambient
(2)	YES	+6 kV at 25°C in ambient
(3)	YES	NO
(4)	NO	+6 kV at 145°C in ambient
(5)	NO	+6 kV at 25°C in ambient
(6)	NO	NO

3.3 Results and Discussion

3.3.1 Crystalline structure of P(VDF-TrFE) thin film

DSC measurement for bulk P(VDF-TrFE) materials in pellet form is shown in Figure 3.2. The data clearly indicate crystalline structure of the copolymer with sharp melting and recrystallization peak at 152°C and 138°C, respectively. The crystalline copolymer exhibits the Curie transition (ferroelectric ↔ paraelectric) at around 100°C during heating and 50-70°C during cooling. The observed data are characteristically consistent with previous reports [1,2,3].

Insignificant crystallinity is observed in thin P(VDF-TrFE) film prepared from spin-coating on Si-wafer substrate, but obvious crystallization is obtained after annealing in N₂ ambient near the melting point (–140°C) as shown in Figure 3.2. Due to small thickness, only strong peak appears in 18-20° range. The 33° peak is found to belong to crystalline Si. The inset of Figure 3.3 shows the resolution of the strong peak that is actually a doublet of 18.9° and 19.3° peak. The broadening at bottom of the doublet and the lacking of other diffracting planes confirm the semi-crystallinity of the annealed P(VDF-TrFE) thin film. The doublet is suggested to result from the coexistence of para- and

ferroelectric phase [11]. The peak at smaller angle is obtained from the diffracting (110) plane of the alternating trans-gauche (TGTG) packing while the other is from the (200) plan of all trans (TTTT) packing. Calculation from DSC data for annealed sample at 140°C yield the highest value of 80% for crystallinity that agrees with previous reports [1]. From Bragg's law, ($\lambda=2d\sin\theta$), the d-spacing is estimated to be 0.47 nm and 0.46 nm for (110) and (200) diffracting plane, respectively.

Figure 3.2 – Differential scanning calorimetric data of P(VDF-TrFE) copolymer.

Figure 3.3 – Crystalline structure of P(VDF-TrFE) thin film on Si substrate. The inset shows the resolution of the strongest peak.

Crystalline structure of thin films spin-coated on different substrates was examined. Structural data for film on Si-wafer and ITO-glass are compared and show similar crystallization (diffracting planes and d-spacing). The data, however, has broad hump indicating more of amorphous phase in film prepared on ITO substrate. The increment of the amorphous intensity is suggested to result from the irregularities of ITO surface (surface roughness –1-10 nm) which forms more regions of disordered polymer chains at the substrate-polymer interface as compared to the smoother surface of Si-wafer (roughness –0.2 nm).

Figure 3.4 – Crystalline structure of P(VDF-TrFE) thin film on Silicon and ITO substrate. The inset shows XRD data of the ITO-glass substrate alone.

3.3.2 Structural changes by heat treatment conditions

As the polymer chains are packed into better-ordered and close-packed all-trans and trans-gauche phase, the doublet observed in Figure 3.3 and 3.4 merge into a broad single peak corresponding to $d = 0.47$ nm as seen in Figure 3.5 and 3.6. The crystallites also show similar characteristics as the samples were annealed in different environments of inert gas and vacuum. The higher diffracting intensity of film annealed in vacuum was possibly resulted from the lower ramping rates as shown in Table 1, which allowed the polymer chains to reorient and grow into more packed and well-ordered crystallites.

Based on the singlet profile, average size of crystalline lamellae is estimated by Scherer's equation [9],

$$t = \frac{a}{B \cos \theta}$$

with B is the FWHM of the diffracting peak. The value is computed to be ~ 10 nm, for both annealing environments, which agrees with previously reported lamellar size of P(VDF-TrFE) copolymer [11,14].

Figure 3.5 – Crystalline structure of P(VDF-TrFE) as annealed at 140°C in different environments.

Figure 3.6 shows the diffracting data for samples annealed at different temperatures in N₂ environment. It can be seen that annealing below the copolymer's melting point T_m strongly enhanced the crystallization as compared to the same process above T_m . It has been well postulated for two different crystallization process in P(VDF-TrFE) for these two temperature regions of annealing [10]. As annealed below T_m , the polymer chains still largely remain in solid state and tend to grow into crystalline domain while being parallel to substrate surface. In contrary, the polymer chains become more mobile as annealed above T_m , hence they reorient with the folding in perpendicular direction to substrate surface. These lead to different types of surface morphology and polarization properties that will be examined in the later parts.

Figure 3.6 – Crystalline structure of P(VDF-TrFE) thin film as annealed at different temperatures in Nitrogen ambient.

3.3.3 Surface morphology of spin-coated P(VDF-TrFE) film

Figure 3.7 – Surface morphology of P(VDF-TrFE) thin film spin-coated and annealed at various temperatures. Below panel shows the 3D topographical images of the corresponding above pictures.

Figure 3.7 shows the typical surface morphology of P(VDF-TrFE) thin film as spin-coated and after annealing in Nitrogen. Without annealing, the film surface appears featureless with pinholes. This is consistent with the mostly amorphous phase in the non-annealed sample. After annealing grain formation is observed for both temperatures below and above T_g , yet the samples appear with different topography. For film annealed at 140°C mainly long rod-like grains are formed while grains with much smaller size and round shape present in film annealed at 160°C. As mentioned above, different crystallization processes were expected for each annealing temperature. Using 3-D topographical image, the rod-like grains can be distinctively seen as vertical walls growing out of sample surface and intercepting each other to create deep valleys. The smaller grains by 160°C-annealing seem to be more broadened hence providing continuous surface covering. This can be affirmed by the surface roughness values as shown in Table 3.3 which indicate much rougher surface for 140°C-annealed film,

Table 3.3 - Surface roughness of film morphology as shown in Figure 3.8

Annealed at	Surface roughness	Grain size distribution
140°C	–15-20 nm	Rod-shape: 600nm (L) / 80nm (W)
160°C	–3-7 nm	Round/Oblong shape: <200nm

The behaviors of each grain type are in agreement with two crystalline grain forms of P(VDF-TrFE) copolymer e.g. "edge-on" crystal and "flat-on" crystal obtained after annealing below and above T_g , respectively [10,12]. In the case of "edge-on" crystals, the polymer chains lie parallel to substrate surface and fold into thin lamellas (–10 nm thick) which closely pack along the rod length. As the dipole vectors are nearly perpendicular to the backbone chains, this packing configuration leads to overall vertically dipolar alignment hence allows better polarization response to the applied field across the film thickness. On the other hand, the "flat-on" crystals are formed from the polymer chains folding in normal direction to the substrate which makes the dipolar vector almost in the same plane with the surface. Therefore it is expected that annealed films above T_m show less response to the applied field hence possess inferior polarization

properties. Nevertheless, the less rough surface with more coverage of the grains by this annealing method seems to be more suitable to application of multilayer devices of electronic application as compared to the irregular surface of lower temperature annealing. This feature will be further explored in Chapter 6.

Figure 3.8 – Surface morphology of P(VDF-TrFE) thin film spin-coated on different substrates and annealed at 140°C.

Similar surface morphology of characteristic rod-like grain is observed as the copolymer is spin-coated on different types of substrates and after annealing at 140°C as presented in Figure 3.8. In spite of the resemblance, certain features appear differently depending on the surface characteristic. More closely packing of the rod grains is seen for film on Si-wafer while the rod grain is less well-defined for films on Al-coated and bare glass as compared to ITO-coated substrate. The close-packed grains are possibly resulted from the lowest surface roughness (0.2 nm) of Si-wafer that lead to better crystallization at the interface and in the bulk of the film, which is also depicted by XRD measurement. For the cases of Al-coated and bare glass substrate, the irregularity of the rod grains likely

indicates presence of disordered regions besides the crystalline grains on the top surface as compared to mostly crystalline rods for film on ITO-substrate.

3.3.4 *Structural changes by corona poling at various heating conditions*

Figure 3.9 – 2D diffraction patterns of different poled samples.

Figure 3.9 and 3.10 show the diffraction patterns and the integrated intensity from the patterns of all six samples. As the 2D-detector was used, diffraction data are no longer limited to measurement only in the diffractometer plane. Instead as a larger portion of the diffraction rings can be recorded, it could provide more information on the crystal orientation related to the forming of crystalline grains. From Figure 3.9, thermal-treated samples (1, 2, 3 & 4) show typical crystalline structure with the appearance of bright arc patterns. The arcs, which were formed by the intersection of the diffracting cones and the 2D-detector moving in the **diffractometer** plane, indicate polycrystalline structure of the copolymer film [13]. For samples without thermal-treatment (5 & 6), low intensity arcs were observed from the patterns that show low crystallinity, probably of short-range order, in a predominantly amorphous matrix. A preferred crystalline orientation can also be seen from the annealed & hot-poled sample-1 with the appearance of a distinctively bright band at center of the arc; whereas a uniform arc indicating a lack of texture is observed in the non-annealed but hot-poled sample-4. The brighter color of the arcs (as seen from the intensity chart) also suggests higher crystallinity in sample 1 & 4 as

compared to sample 2 & 3. As evident from the 2-D X-ray data (Figure 3.10), all the annealed samples (1-3) show good crystallinity whereas the hot-poling seems to induce high texture (sample 1) and improved crystallinity (sample 4).

From the integrated intensity data (shown in Figure 3.10), only one dominant crystalline peak was observed in all the samples. The d-spacing is nearly constant for all samples at $4.47 \pm 0.01 \text{ \AA}$ indicates the packing of polymer chains is not affected by the interaction of thermal treatment (annealing or heating during hot-poling) and poling field. Lamellar crystal sizes, determined from the Scherrer equation [9], are in the range of 10 to 10.7 nm, also in agreement with previously reported data [14].

Figure 3.10 – Crystalline structure of poled samples obtained from integrating of 2D diffraction images of Figure 3.10 (a) samples with pre-annealing & (b) samples without pre-annealing.

The XRD intensity reveals that room-temperature poling does not have any effects on film crystallinity by comparing results between sample 2 & 3 as well as between sample 5 & 6. In both cases, it is probable that the restriction of polymer chains in the solid state was much stronger compared to the field strength. Prior to hot-poling, sample 1 should have a semi-crystalline structure similar to sample-3 due to pre-annealing, while sample-4 would mainly contain the amorphous phase similar to sample-4. From Figure 3.9 and results from the above calculations, it is evident that after hot-poling, samples 1 and 4 both possess similar crystalline characteristics.

Figure 3.11 – Surface morphology of differently poled samples.

AFM studies display a preferential orientation of grains for hot-poled sample 1 (Figure 3.11) while AFM image of room temperature-poled sample 2 shows similar characteristics as that of sample 3, with randomly oriented grains. It is estimated that the orientation of the grains in sample 1 is nearly perpendicular to the direction of the poling electrode wire; hence folding polymer chains are nearly parallel to the poling wire. Similar orderly rearrangement of $P(VDF-TrFE)$ rod-like crystals has been previously reported [15]. Hence, hot-poling process can be similarly used to obtain ordered structure of semicrystalline ferroelectric thin films without invasive contact to the sample surface. Corona poling effects were also examined in amorphous films (samples 4 and 5). While sample 4 exhibits high crystallinity but randomly oriented grains with smaller size, sample 5 had similar crystallinity and surface morphology as sample 6. The morphology of samples 2 and 5 could be anticipated since the required energy for the polymer chains in solid state to become mobile is much larger than that provided by the corona field alone at low temperatures.

A characteristic rod-like grain structure or edge-on crystal is observed in AFM images of the annealed sample-3 (Figure 3.11). Each rod-grain has a length of ~600 nm and consists of a multi-slab thickness of ~60 nm. This is about two-times longer and slightly thicker compared with other reports [10,16]; possibly due to the higher annealing temperatures used in this study that leads to the growth of larger grains. For the hot-poled sample 4, smaller rod-like grains were observed with average sizes of 200 nm long and 50 nm thick. The formation of these small and random grains in sample 4 is attributed to thermal activation from the hot-poling process leading to crystalline structure as observed by XRD (Figure 3.9 and 3.10 (b)).

The difference of crystal sizes between sample 1, 3 and 4 is attributed to the interaction of different thermal conditions and the presence of the poling field. During annealing, polymer chains were disentangled from the amorphous regions and folded into crystalline lamellae through gliding motion. However in the presence of corona charges created by the poling field, dipolar moments were anchored at the top surface thus hindering the motion and rearrangement of the chains. This opposite effect, therefore, limited the crystal sizes and prevented orientation of rod-like grains. For sample 1, crystalline grains had been formed during the annealing step (similar to sample 3) which led to a stronger response to the subsequently applied poling field at elevated temperature and resulted in formation of longer grains possibly by joining of preexisting grains.

To further confirm the organized structure in the hot poled samples, UV-vis absorption spectra were obtained (Figure 3.12), with the strongest absorption occurring in the 350-400 nm range. The existence of the absorption peak in W-vis spectra of P (VDF-TrFE) copolymer can be viewed under the effects of electron donation into σ^* orbitals of the C-F bond [17,18]. Pre-annealed and hot-poled sample 1 and hot-poled sample 4 show the highest absorbance intensity and exhibit a shift of absorption peak to longer wavelengths (bathochromic). We attribute the increased absorption to the enhanced crystallinity due to heat treatments. In the pre-annealed and hot poled sample 1 and the hot poled sample 4, more ferroelectric phase was formed after poling hence more F-pairs were aligned on the same side of the polymer chain. This would eventually lead to easier excitation and

donation of electrons from n_p orbitals of F-atoms to anti-bonding orbitals σ^* of C-F bond by the excitation light.

Figure 3.12 – UV-vis absorption spectra of poled samples.

The bathochromic shift has been seen in polymer-dye films subjected to elevated temperature corona poling [19] and is explained based on electrochromism in which large electrostatic charges induced by corona fields accumulating near the sample surface. For the reported polymer-dye system, the bathochromic **shift** was seen to disappear after 10 days due to slow depletion of charges [19]. The shifts in our experiment were found to be unchanged upon retesting after 60 days. This is attributable to the longer retention of injected charges by semicrystalline structures of the copolymer film that consists of crystalline phases embedded in an amorphous matrix. During the poling process, **ferroelectric** dipoles were aligned according to the field direction, which was accompanied by a simultaneous charge injecting into the film surface to compensate for the potential built up by the dipole moment. The injected charges could reside in the amorphous phase or at the crystalline-amorphous interface regions (refer to Chapter 4) for a long time due to stability of the polarization dipoles.

High frequency (1 MHz) capacitance measurement (CV) was used to characterize the changes in dielectric properties of the poled film. Measurements performed on a **metal-**polymer-metal capacitor device (Figure 3.13) display butterfly-shaped hysteresis

behavior, characteristic of ferroelectric materials, for samples subjected to annealing treatments (samples 1, 2, and 3); whereas, samples not subjected to annealing (samples 4, 5 and 6) failed to give stable data due to high conductivity (More discussions on the capacitance hysteresis and related properties can be found in Chapter 4). It is believed that the high conductivity was caused by the porosity of the amorphous phase which led to **diffusion** of gold during thermal evaporation of the top electrode. Hot-poled and annealed samples showed the largest capacitance, the increment being attributed to ferroelectric phase formation in hot-poled samples, contributed by significant dipolar alignment and injected charges for compensation. As opposed to hot-poled sample 1, the capacitance values of room-temp poled sample-2 showed a drastic reduction in capacitance after just one day of storage. This reduction in capacitance suggests that room-temperature corona poling had only led to charge accumulation on the sample surface, leading to a slow discharging effect upon the removal of the external field.

Figure 3.13 – Capacitance-voltage hysteresis curves of samples measured after poling and after relaxing times.

Characterizations by XPS (Figure 3.14) indicate four different C-states exist in C1s deconvoluted spectra e.g. 282.22 eV–organic contaminants, 284.82 eV–saturated

hydrocarbon CH_2 , 287.51 eV– CFH , and 289.79 eV– CF_2 . While the positions of CH_2 and CF_2 peak have been well determined, the CFH component was determined by comparing its shift from CF_2 and correlated to the characteristics of poly(trifluoroethylene) as reported in [20]. Spectra of F1s also clearly revealed two states of F-atoms in the copolymer namely 684.75 eV – CFH and 687.06 eV – CF_2 due to differences in the bonding environment. Scans in O1s region showed similar spectra for all six samples and was attributed to the presence of organic traces in the analysis chamber. Summary of peak positions of C1s and F1s is shown in Table 3.4 after charge compensation using the equipment reference C1s peak.

Figure 3.14 – XPS spectra of core C1s and F1s measured from surface of P(VDF-TrFE) poled samples.

A clear trend of peak shifting in the spectra of both C and F atoms is evident in Figure 3.14 and Table 3.4. Samples 1 and 4 show similar C1s and F1s binding energies, which indicate the similar atomic binding states, hence a similar process of chain folding and reorientation during poling at elevated temperature. After hot poling, the environment of the atoms shows to be unaffected by pre-existing crystalline/amorphous structure or joining of rod-like grains. Room-temperature poling is seen to have more pronounced effects to the pre-annealed samples compared to the non-annealed one, by comparing sample 2 and 5. We suggest this is related to the formation of polarizable α -phase (α_p) in the semicrystalline sample. It has been reported that electret poling of crystalline PVDF

film under similar conditions (field of 1500 kV/cm at 24°C for 3 hours) led to new formation of α_p phase without any changes to α and β phase observed at (110, 200) diffraction [21]. This observation also explains the identical XRD data obtained for samples 2 and 3.

Table 3.4 – Summary of binding energy (eV) values for components of C1s and F1s

Sample	(1)	(2)	(3)	(4)	(5)	(6)
$\underline{\text{CF}}_2$	290.35	290.47	289.61	290.31	289.31	289.68
$\underline{\text{CFH}}$	288.25	288.33	287.60	288.26	287.36	287.40
$\underline{\text{CF}}_2$	687.31	687.37	686.62	687.36	686.57	686.95
$\underline{\text{CFH}}$	685.07	684.97	684.44	684.76	684.35	684.64

Figure 3.15 – Compositions of different chemical group as calculated from the XPS data in Figure 3.14.

Figure 3.15 shows the compositions of C1s components and the ratio of hydrocarbon $\underline{\text{CH}}_2$ to fluorine-bonding carbons ($\underline{\text{CF}}_2+\underline{\text{CFH}}$) in all six samples. The data shows clear differences in the effect of poling samples of semicrystalline and amorphous structure. Annealed samples displayed an overall increment of fluorine-bonded carbons bonding against hydro carbon bonds. Hot-poled sample (1) is seen to have the highest percentage

of (CF_2+CFH) component suggesting that the applied positive corona poling induced the re-location of more Fluorine atoms containing higher electron density towards the top surface of the copolymer film sample. This indicates a change in chemistry on the top surface of the films; the compatibility of which with subsequent multilayer may need to be considered to ensure optimal device integrity and functionality.

3.3 Conclusion

Surface morphological and crystalline structural characteristics of thin P(VDF-TrFE) films have been examined for an optimized condition to be rendered in device application. Thin films of high crystallinity are obtained through annealing below melting point for sufficient time and possess unique surface morphology of rod-like grains independent of substrate surfaces. The film crystallinity is generally unaffected by substrate types, however, can be improved with better surface flatness. As good crystallization is specifically required for polarization properties, the appearance of the rod-like grains that intercept each other and cause surface roughness is unavoidable. Using corona poling method it can be shown that the formation of crystalline grains as well as their organization can be obtained by combining sufficient poling voltages and annealing conditions. Other effects by poling can also be acquired such as retention of capacitance that raises dielectric constant, changes in absorption properties that shows more ordering and tendency to increase negative surface charges by more Fluorine components. Understanding these changes helps to facilitate different applications or the engineering of multi-layer devices.

3.4 Reference

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Chapter 4

STUDY ON POLARIZATION AND ELECTRICAL PROPERTIES OF P(VDF-TrFE) THIN FILM AND THEIR EFFECTS IN DEVICE OPERATION

4.1 Introduction

Due to its good dielectric properties and ease of solution processing, ferroelectric copolymer P(VDF-TrFE) has been employed for various electrical devices e.g. diodes, transistors, varied capacitors [1,2,3]. For copolymers with superior polarization properties (with more than 70 %VDF), they can also be used for ferroelectric field effect transistors for non-volatile memory application [1]. Because of semicrystalline structure of solution formed films, the polarization switching process is accompanied by a complicated compensation of charges [4,5]. Generally it has been postulated of three general mechanisms that involve the appearance of charges – dipolar switching in ferroelectric phase, charge injection in amorphous phase and the Maxwell-Wagner interface charges [6]. So far these processes have been investigated by using poling with temperature either heating to Curie point or cooling to glass transition [6,7,8,9]. While the heating method usually points out to the relaxation caused by ferroelectric-paraelectric phase transition that observes a steep increment of dielectric constant, the cooling process is used to suppress the molecular rotation and then probe for the dipole-independent components. So far most of the reports have been focused in the heating method and limited information of the cooling one is available for P(VDF-TrFE) copolymer.

In terms of device operation, the understanding of the free charge carrier behavior is important due to its contribution to leakage current that degrades device characteristics. For capacitors, the leakage leads to suppression of capacitance over shorter period. In the case of transistors where ferroelectric copolymer is used as dielectric layer, leakage current is more serious when higher applied voltage is required and causes high OFF-state current. By identifying the right source and mechanism of the leakage current it will provide ways to improve device performance.

In this chapter, polarization and dielectric properties of P(VDF-TrFE) copolymer will be investigated. Sources of free charge carriers which exist in ferroelectric copolymer will be examined for capacitor and diode devices. A mechanism of charge transportation will be proposed to corroborate with the observed data.

4.2 Experimental

Thin P(VDF-TrFE) film was prepared by spin-coating from filtered solution of 30 mg/cc in MEK. ITO glass was used as substrate and ultrasonically cleaned by acetone, methanol and deionized water. Films of 320-360 nm thickness were annealed in Nitrogen gas for 2 hours as described in Chapter 3. Gold (99.9% purity) electrode (1 mm diameter) was formed by thermal evaporation through round-shape shadow mask for metal-polymer-metal capacitor device. For Schottky diodes, 50 nm thick pentacene was evaporated in $\sim 10^{-7}$ torr vacuum at rate of 0.1-0.2 Å/s on top of P(VDF-TrFE) film. It was then followed by deposition of gold electrode of 500 x 500 μm^2 size.

Polarization hysteresis was measured by Radiant Ferroelectric tester using triangular signals of various frequencies in ambient condition. Low temperature measurement was done in Lakeshore Cryogenic probe station with temperature cooling by liquid Nitrogen and at vacuum of $\sim 10^{-6}$ torr. Testing temperatures were maintained by counter-effect heating of thermal sources. Capacitance and conductance measurement were obtained by HP4284 and HP4980 LCR meter with AC amplitude of 50 mV. Current-voltage measurement was done with Keithley4200 Semiconductor analyzer. All the measurements were performed by applying the active voltage to the ITO electrode with respects to the gold electrode.

4.3 Results and Discussion

4.3.1 Polarization and dielectric properties of *P(VDF-TrFE)* thin film

Figure 4.1 – Polarization hysteresis of *P(VDF-TrFE)* copolymer with different %VDF (a) 57-43 mol% (1.5 μm thick film) (b) 70-30 mol% (1.2 μm thick film). Inset shows M-P-M device structure.

Typical saturated polarization curves of *P(VDF-TrFE)* thin film with various %VDF are shown in Figure 4.1. It can be seen that higher percentage of VDF component results in higher remnant polarization P_R and lower coercive field E_C e.g. $|6| \mu\text{C}/\text{cm}^2$, $\sim|60| \text{MV}/\text{m}$ for 57 mol% and $|8| \mu\text{C}/\text{cm}^2$, $\sim|50| \text{MV}/\text{m}$ for 70 mol% similar to previous reports [10]. This can be explained from the lower crystallinity of the 57 %mol film in which the applied field is reduced due to dropping across the majority of amorphous regions [10]. Lower crystallinity also leads to less ferroelectric phase formation, hence smaller remnant values. Figure 4.2 shows the dielectric properties of copolymer thin films. Overall, both of the copolymers have high dielectric constant that is suitable and useful as dielectric layer in field effect transistors. In contrary to polarization, dielectric constant of copolymer with 57 mol% VDF is higher especially in the low frequency range. This hence indicates a strong correlation between the crystalline-amorphous phase ratio in the prepared thin film and the electrical properties. The higher dielectric constant should be resulted from the higher percentage of amorphous phase in low %VDF copolymer as determined in previous reports. The disordered or amorphous phase in ferroelectric

polymers possibly including some short-range ordered regions and the interface regions of different phases can contribute to charge metastable accumulation during bias application. Besides, the existence of higher %TrFE also likely increases more electronegative components due to high percentage of F atoms. These few mechanisms eventually lead to higher dielectric susceptance in lower %VDF copolymer,

Figure 4.2 – Dielectric properties of P(VDF-TrFE) thin films of various %VDF (■ & □ – 57-43 mol%, ● & ○ – 70-30 mol%).

Figure 4.3 – Displacement current profile of 320 nm-thick P(VDF-TrFE) 70-30 mol% film sample.

Figure 4.3 shows the displacement current profile of 320 nm-thick P(VDF-TrFE) 70-30 mol% film with the same device structure as shown in Figure 4.1. The observed peaks are resulted from dipolar switching by the applied sweeping bias [11]. The broadening of the baseline indicates the dipole reorientation occurs over wide range of applied voltage. This

tallies the semi-crystallinity of the thin film sample and also suggests various sizes of ferroelectric domains in P(VDF-TrFE) film. In terms of device application, it can be seen that the leakage is mainly due to the displacement current. As a result, beside stable and permanent polarizability the P(VDF-TrFE) thin film also exhibits good dielectric and insulating properties.

4.3.2 Changes of capacitance and conductance against frequency and temperature

Figure 4.4 – Capacitance and conductance vs. temperature and frequency of P(VDF-TrFE) 70-30 mol% thin film. Inset of C-T data shows capacitance hysteresis at 1 kHz against temperatures.

Figure 4.4 shows the behavior of capacitance and conductance in P(VDF-TrFE) 70-30 mol% thin film with various conditions of temperatures (C-T, G-T) and frequencies (V-f, G-f). In the C-T data, capacitance drops gradually with temperature before the glass transition (T_G -233 K) [12]. Further below T_G , capacitance is independent of both temperature and frequency as shown in the C-f data. This hence suggests that dipolar rotation depends on thermal energy contribution as seen by the absence of "butter-fly"

shape hysteresis of the C-V curve in the inset of C-T graph. The reduction of capacitance with increased frequency also indicates dynamic resistance of dipolar reorientation against very fast applied signals. Using a reported method to extract the non-dispersive capacitance of ferroelectric thin film which is independent of frequency [13], the non-dispersive values of P(VDF-TrFE) film are shown in Figure 4.5(a). The presented curve shows a combined behavior of both phases with the monotonous increment above 243 K being affected by the crystalline phase and the hump at lower temperature resulted from the dominance of the amorphous phase [14]. The obtained data are in good agreement with the reported overall changes in dielectric constants of separated crystalline and amorphous phase of P(VDF-TrFE) copolymer.

Figure 4.5 – (a) Non-dispersive capacitance with inset showing the method to extract capacitance values and (b) equivalent imaginary dielectric constant ($\epsilon'' \sim G_p/\omega$) against temperatures.

In terms of conductance data (Figure 4.4(b)), trend of gradual decrement can also be found against temperatures. Furthermore, the G-T data exhibits evolution of peaks at T_G for low frequency measurement (1-10 kHz) and shifting of peaks to higher temperature ($\sim 273 \text{ K}$) at frequencies greater than 10 kHz. This behavior can be better viewed in the graph of equivalent imaginary dielectric constant G_p/ω vs. T shown in Figure 4.5(b). It is hence correlated to a-relaxation of the polymer chains with the low-temperature peak corresponding to amorphous phase (a,) and the higher one to crystalline phase (a,) similar to previous observation for PVDF homopolymer [7]. On the other hand, the conductance values are seen drastically varied with frequencies (linear relationship in log-log graph). The behavior above and below T_G possibly share similar mechanism due

to the same tangent while deviation is seen for data in the transition region ($T_G \sim 233K$). As the conductance measurement mainly relates to how the charge carrier moves in the copolymer film, it provides detailed information of dielectric behavior of P(VDF-TrFE) film especially when the capacitance is seen under the effects of both amorphous as crystalline. Detailed analysis of conductance data will be discussed in the followed part.

4.3.3 Relationship of polarization and capacitance hysteresis - Correlation of reversible and irreversible polarization

Hysteresis behaviors of capacitance and polarization of P(VDF-TrFE) thin film device are shown in Figure 4.6. Higher frequency mainly lowers the overall capacitance values and slightly reduces peak voltages. It, nevertheless, substantially increases the coercive voltages in P-E curves. While the increased coercive field is possibly due to limited response of dipolar rotation at high speed and the domain wall movement, the consistence of spontaneous and remnant polarization is of great interest [16]. The slanting slope from spontaneous to remnant value indicates polarization loss between the bias applied state and zero voltage or reversible polarization [15,16]. The remnant polarization is hence so-called irreversible which simultaneously exists with the reversible counterpart. The coexistence of these two polarization types can be seen from the displacement charge in dielectric materials as followed. The overall charge neutrality of matter under the application of an external field is described by:

$$\vec{D} = \epsilon_0 \vec{E} + \vec{P} \quad (1)$$

with D is dielectric displacement, which is equal to the surface charge on the metal plates, P is the electrical polarization in the dielectric film, E is the external applied field and ϵ_0 is the vacuum permittivity. The displacement D is controlled by both of the amplitude and direction of the applied field as well as the internal polarization of the dielectric layer. For ferroelectric thin film, the electrical polarization at the measurement frequency range (< 1 MHz) mainly consists of two types e.g. dipoles and free charge carrier. Therefore the dielectric displacement in equation (1) can be rearranged as followed:

$$\vec{D} = \epsilon_0 \vec{E} + \vec{P}_{dipole} + \vec{P}_{charge} = \epsilon_0 \vec{E} + \epsilon_0 \chi_e \vec{E} + \vec{P}_{dipole} = \epsilon_r \vec{E} + \vec{P}_{dipole} \quad (2)$$

with $\vec{P}_{charge} = \epsilon_o \chi_e \vec{E}$, which behaves as dielectric material, $\epsilon_r = \epsilon_o(1 + \chi_e)$ is dielectric constant of the ferroelectric copolymer, and χ_e is susceptibility. Overall the displacement charge of equation (2) describes the two simultaneous processes recorded from both capacitance and polarization hysteresis.

Figure 4.6 – (a) Capacitance and (b) polarization hysteresis of P(VDF-TrFE) 70-30 mol% film device.

Figure 4.7 – Comparison of polarization and capacitance measured in small signal method. Inset shows the C-V curve measured at 100 Hz.

Using small-signal method [16] in which a sinusoidal AC signal of various frequency and small amplitude is superimposed on constant DC voltage, the amount of free charges in the ferroelectric capacitor can be obtained from both bias accumulation and induction by dipolar orientation. Figure 4.7(a) presents polarization hysteresis measured at 100 Hz using the standard Sawyer-Tower circuit compared to the small signal measurement. It can be seen that the slope of $P_{\text{small_signal}}$ curve is in good match to the tangent of

polarization loss from spontaneous to remnant value. As mentioned above, this loss is caused by the reversible charges which cannot be retained during the absence of the applied bias. Furthermore, comparison of $P_{\text{small-signal}}$ curve to the integration of "butterfly" shape CV curve measured at the same frequency shows excellent matching between them. Therefore the subsequent extraction of free charge carriers is based on the C-V sweeping measurements.

4.3.4 Study of free charge carriers in P(VDF-TrFE) thin film

Figure 4.8 – Log(I)-V graph of P(VDF-TrFE) film measured at 211 K with inset showing the linear I-V curve.

As shown in Figure 4.4(b) and 4.5(b), the conductance of P(VDF-TrFE) film exhibits two peaks e.g. below T_G at low frequencies and above T_G at high frequencies. While the later one is possibly caused by lagging of dipolar switching against the applied signal, the former occurs when polymer chains are frozen presents true dielectric behavior of the copolymer film. This can be observed with almost unchanged dielectric constant (capacitance value) for temperatures below 223 K shown in the inset of Figure 4.4(a). As temperature is decreased further below T_G , the reduction in capacitance values indicates the existence of charges in the system purely depends on thermal activation, which is strongly supported by the constant capacitance against frequency and temperature (Figure 4.4(c)). It, therefore, can be seen that the reversible polarization P_R (discussed above) should be a part of the compensating charges in semicrystalline ferroelectric film, and besides P_R there is another type of free charge carriers that results in the measured

capacitance as well as the leakage current recorded below T_G as shown in Figure 4.8. A weak rectifying behavior with hysteresis characteristic can be seen from the linear scale I-V curve. It has been shown that the Fermi level of Langmuir-Blodgett transferred P(VDF-TrFE) film lies near to its conduction edge which makes the copolymer as wide band gap n-type semiconductor [25]. The weakly observed rectified current, hence, possibly indicates weak Schottky contact type in the ITO-P(VDF-TrFE)-Au device.

Based on this, surface state density N_{ss} and series resistance R_s of the device are determined at 1 MHz for temperatures below T_G by assuming the device to be equivalent to a circuit of various components [17] as followed:

$$\text{Series resistance} \quad R_s = \frac{G_m}{G_m^2 + (\omega C_m)^2} \quad (3)$$

$$\text{Surface state density} \quad N_{ss} = \frac{2}{qA} \frac{(G_m / \omega)_{\max}}{[G_m / (\omega C_{eq})^2 + (1 - C_m / C_{eq})^2]} \quad (4)$$

$$\text{with} \quad C_{eq} = C_m \left[1 + \left(\frac{G_m}{\omega C_m} \right)^2 \right] = \frac{\epsilon_{eq} \epsilon_o A}{d_{eq}} \quad (5)$$

Figure 4.9 – Calculated series resistance and surface state density of ITO-P(VDF-TrFE)-Au capacitor device (a) at different applied voltages & (b) at different frequencies.

The calculated data are shown in Figure 4.9. It can be seen that the series resistance and surface state density are reversed of each other. While series resistance shows a steep rise near T_G , surface state density profile is almost linear against temperature. The opposite behavior of these two quantities further indicates the dominance of the free charge

carriers below T_G regime especially in the absence of polarization switching and compensation. As shown in Figure 4.4(d) the conductance-frequency curve at T_G (-233 K) exhibits a different characteristic compared to others. A constant conductivity is obtained towards low frequency range indicating dominant DC conductance. As a result the imaginary part of dielectric constant (equivalent to G/ω) shows a loss peak against the frequency as presented in Figure 4.10. The surface state at T_G is hence estimated from the relaxation peak as followed.

Figure 4.10 – Equivalent imaginary part of dielectric constant measured at T_G .

The quantity G_p indicated in Figure 4.10 is the corrected value for conductance and given by,

$$G_p = \frac{G_m}{\left(\frac{G_m}{\omega C_{eq}}\right)^2 + \left(1 - \frac{C_m}{C_{eq}}\right)^2} \quad (6)$$

Due to the relaxation peak (determined to be at 1 kHz), the G_p/ω curve must satisfy the relationship [18]

$$\frac{G_p}{\omega} = \frac{qAD_{ii}}{2\omega\tau} \ln[1 + (\omega\tau)^2] \quad (7)$$

The peak maximum is hence determined by $\frac{d(G_p/\omega)}{d[\ln(\omega\tau)]} = 0$ which yields $\omega\tau = 1.98$.

As a result, the surface state density at T_G is calculated by

$$D_{ii} = \frac{(G_p/\omega)_{\max}}{0.402qA} = 2.97 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2} \quad (8)$$

Comparing this value to 1 KHz curve in Figure 4.9(b) shows a reasonable fit in which the surface state density is drastically reduced in the glass transition regime due to the fluctuation of transition behavior at different locations of various domain sizes or crystallinity. Following Fuoss approach [19,20] the activation energy of the relaxation process is estimated around 0.067-0.097 eV which is slightly higher than reported values for PVDF homopolymer (0.02-0.05 eV). The difference can be explained from the presence of TrFE that changes the electronegativity of the copolymer and crystallization characteristics as well as the rigidity of the TrFE molecular chains.

Using the data shown in Figure 4.4(d), the conductance curve $\log(\sigma)$ - $\log(f)$ below T_G is seen in good fit to linear line described by:

$$\sigma(\omega) = A\omega^s \Leftrightarrow \log \sigma(\omega) = \log A + s \log \omega \quad (9)$$

with ω being frequency in rad/s and the exponent “s” found to be slightly superlinear which is agreed with the mechanism of correlated barrier hopping with non-random distribution of asymmetric barrier height [21,22,23]. The estimated s value (~ 1.00523) is different from the reported value of PVDF [7]. This, hence, possibly indicates two asymmetric polarization states in which one is more favored resulting in a slightly larger value of coercive voltage observed in the transfer characteristic of a ferroelectric field effect transistor (Chapter 5). A schematic presentation of the suggested mechanism is shown in Figure 4.11. The maximum barrier height indicated by the scheme is related to s value as $s = 1 + a$, and $a = k_B T / W_M$ from which the value of W_M is estimated to be 3.84 eV. This value is in the same order of band gap value, 3.2 eV, reported for 5 monolayer of P(VDF-TrFE) film prepared by Langmuir-Blodgett method [2].

Figure 4.11 – Schematic presentation of energy level in correlated barrier hopping with non-random distribution of asymmetric barrier height (adopted from [21]).

The density of states near the Fermi level $N(E_F)$ in the P(VDF-TrFE) thin film can be estimated from the AC conductivity by using the relationship [7,24] given as

$$\sigma(\omega) = \frac{\pi [eN(E_F)]^2 \omega}{3 \alpha^5 [\ln \omega \tau_o]^4} k_B T \tag{10}$$

with e is the electronic charge, k_B is Boltzmann constant ($k_B = 1.38066 \times 10^{-23}$ J/K = 8.617385×10^{-5} eV/K), τ_o is time factor (assumed to be 10^{-13} s), and a is the radius of the carrier wave function. The calculated data are shown in Table 4.1 for three different values of a . These values are around one order smaller than the ones reported for PVDF [7]. This is possibly explained by the n-type semiconducting characteristic that has been determined for P(VDF-TrFE) [2,25]. Because the Fermi level is nearer to the conduction band, the distribution of density of states around this energy level is hence lesser. As seen from Figure 4.11 these energy states likely exist at levels much below the conduction band and the hopping transport only initiates and takes place from bottom of the wells which at maximum is about 3.84 eV from the conducting level.

Table 4.1 – Estimated values of density of states at Fermi level for P(VDF-TrFE) film using equation (10)

T (K)	f (Hz)	$\sigma(\omega)$ (S)	$N(E_F)$ (eV ⁻¹ cm ⁻³)		
			$\alpha = 1 \text{ \AA}$	$\alpha = 2 \text{ \AA}$	$\alpha = 4 \text{ \AA}$
190	10^6	1.55×10^{-5}	$1.53 \times 10^{+16}$	$8.63 \times 10^{+16}$	$4.88 \times 10^{+17}$
	10^5	6.80×10^{-7}	$1.37 \times 10^{+16}$	$7.73 \times 10^{+16}$	$4.37 \times 10^{+17}$
	10^4	6.23×10^{-8}	$1.70 \times 10^{+16}$	$9.59 \times 10^{+16}$	$5.42 \times 10^{+17}$
	10^3	6.93×10^{-9}	$2.25 \times 10^{+16}$	$1.27 \times 10^{+17}$	$7.20 \times 10^{+17}$
298	10^6	1.36×10^{-4}	$4.42 \times 10^{+16}$	$2.50 \times 10^{+17}$	$1.41 \times 10^{+18}$
	10^5	1.41×10^{-5}	$6.06 \times 10^{+16}$	$3.43 \times 10^{+17}$	$1.94 \times 10^{+18}$
	10^4	1.19×10^{-6}	$7.22 \times 10^{+16}$	$4.08 \times 10^{+17}$	$2.31 \times 10^{+18}$
	10^3	7.88×10^{-8}	$7.40 \times 10^{+16}$	$4.18 \times 10^{+17}$	$2.37 \times 10^{+18}$
	10^2	4.45×10^{-9}	$6.83 \times 10^{+16}$	$3.86 \times 10^{+17}$	$2.19 \times 10^{+18}$

4.3.4 Study of electrical properties of *P(VDF-TrFE)* – Pentacene interface

Figure 4.12 shows cyclic sweeping I-V curve for ITO-P(VDF-TrFE)-Pentacene-Au device with the drive voltage applied to the ITO gate. The data clearly indicates rectifying behavior during accumulation state of pentacene hence Schottky contact has been formed between P(VDF-TrFE) and pentacene agreed with previous reports [2] as Ohmic contact is formed at Pentacene-Au interface [26]. A threshold voltage of -11 V determined from the linear graph is resulted from the non-rectifying or contact resistance probably between ITO and ferroelectric copolymer. The rising current during the positive voltage application is due to leakage across the bulk of pentacene and P(VDF-TrFE) film. It will be seen in the later chapters that gate current profile of transistor device is similar to one in Figure 4.12. The absence of the displacement current peak is, however, possibly due to the high magnitudes of rectifying current.

Figure 4.12 – Current – voltage data of ITO-P(VDF-TrFE)-Pentacene-Au device. Inset show semi log curve.

Capacitance and conductance data at various frequencies are shown in Figure 4.13. The expected capacitance of the P(VDF-TrFE) layer here (dielectric constant of 13) is 65.4 pF and that of the pentacene layer is 265.5 pF (using dielectric constant of 6). So the measured capacitance at accumulation is matched to that of the insulator layer while at full depletion the expected capacitance (of both insulator and semiconductor) is 52.5 pF which is of same order to the measured value (49 pF). The bistability of two threshold voltages in capacitance curves results in a fixed ΔV_T window that governs that memory functionality as investigated in the subsequent chapters. The conductance data follows

similar hysteresis of capacitance and exhibits peaks at flat-band voltages e.g. -10 and +11.7 V. The charge carrier concentration in pentacene layer is evaluated from the slope of the depletion regions that is given by [26],

$$N_{\text{free-carrier}} = \frac{2}{q\epsilon_o\epsilon_{st}A[d(1/C^2)/dV]} \quad (11)$$

with ϵ_{st} being static dielectric constant of P(VDF-TrFE) layer. Equation 11 was only applied for the sweeping cycle from accumulation to depletion as shown in Fig. 4.13 which shows a more stable polarization switching. The calculated data are shown in Table 4.2. It can be seen that the free charge carriers yield values greater than $2 \times 10^{17} \text{ cm}^{-3}$ which is quite similar to the density of states around Fermi level in P(VDF-TrFE) film taking average radius of carrier wave function of $2 \text{ \AA}^{-1}$.

Figure 4.13 – Capacitance and conductance vs. voltage data of device shown in Figure 4.12.

Figure 4.14 – Capacitance and conductance vs. frequency. Inset show $G(\omega)/\omega$ vs. ω curve.

The change of capacitance and conductance against frequencies are also measured and shown in Figure 4.14. Applying the same method described above (equation (8)), the $G(\omega)/\omega$ vs. ω shows a peak profile as in the inset of Figure 4.14. The interface state density is then calculated from the peak value and extracted from different frequencies as indicated in Table 4.2. Comparing to Figure 4.9(b) the surface state density in P(VDF-TrFE) film is slightly higher than interface states found for the ferroelectric copolymer-pentacene interface yet both are in the same order. As a result from the density of charge carriers and interface states there can be seen a good matching of values in both of dielectric and semiconductor layer. The interface state density is further investigated to reveal its distribution in the semiconductor band. Figure 4.15 shows that the interface states have the tendency to increase at locations farther away from the valence band of pentacene. This is hence corresponded to n-type characteristics of P(VDF-TrFE) [2,25] for which negative mobile charges can be removed from available states in pentacene and transfer to P(VDF-TrFE) by transporting through the states near conduction band of the ferroelectric copolymer. A proposed schematic diagram of this process is presented in Figure 4.16. These findings conclude the probability of charge injection and movement between P(VDF-TrFE) and pentacene layer which facilitates better understanding of some of the phenomena in transistor device described in Chapter 5.

Figure 4.15 – Interface state density distribution at energy levels against valence band of pentacene calculated from C-V and G-V data.

Table 4.2 – Calculated values for free charge carrier concentration and interface state in ITO-P(VDF-TrFE)-Pentacene-Au device followed equation (11) and (8), respectively

Frequency (Hz)	N_A (cm^{-3})	D_{it} ($\text{eV}^{-1}\text{cm}^{-2}$)
10^4	2.77×10^{17}	1.76×10^{12}
10^3	2.15×10^{17}	1.69×10^{12}
500	2.78×10^{17}	1.29×10^{12}
200	2.71×10^{17}	1.42×10^{12}

Figure 4.16 – Proposed energy diagram for contact formation in ITO-P(VDF-TrFE)-Pentacene-Au device. Energy levels of P(VDF-TrFE) are adapted from [26].

4.4 Conclusion

Dielectric and polarization properties of P(VDF-TrFE) were investigated. The correlation between polarization remnant and coercive values with dielectric constants of copolymers of various VDF compositions is mainly dependent on chemical variation and crystallinity of the samples. Overall the dielectric constant drops at high frequencies due to slower response of dipoles. Combining results at low (polarization hysteresis) and high (capacitance hysteresis) frequency, the "butterfly-shape" response is found to emulate the reversible polarization which consists of compensation charges in amorphous phase and interfacial regions. Measurement at temperatures below T_G shows that part of the compensation charges exists in "free-carrier" state which can respond to applied voltage independently from dipole switching. The carrier density is found to be in the order of 10^{17} cm^{-3} and their transportation through the bulk ferroelectric polymer is possibly

governed by carrier hopping mechanism with non-random distribution of asymmetric barrier heights.

Measurements of Schottky diode made from P(VDF-TrFE)-Pentacene contact lead to similar value of interface state density in both Pentacene and P(VDF-TrFE) layer. Further examination reveals increased interface state distribution at energy levels away from the valence band of pentacene. This hence corroborates to the suggested transport mechanism in which negative charges can be removed from valence band of pentacene and injected into gap-states in P(VDF-TrFE). The existence of positive holes in pentacene by this mechanism is directly observed by transistor behavior in the subsequent chapters. Based on the findings a schematic energy diagram is proposed for the formation of heterogeneous contact between P(VDF-TrFE) and pentacene semiconductor.

4.5 Reference

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Chapter 5

ORGANIC FERROELECTRIC FIELD EFFECT TRANSISTORS AND STUDY OF PERFORMANCE BEHAVIORS

5.1 Introduction

Ferroelectric copolymers [1] have been recently studied for the application in non-volatile memory for organic electronics [2-6]. The memory functionalities are resulted from the polarizability of dipoles in the organic layer that serves as the gate insulator in the field effect transistors. Two of the polymers which have been reported as gate dielectrics in ferroelectric transistors are Poly(vinylidene fluoride-trifluoroethylene), P(VDF-TrFE), and Nylon poly(m-xylylene adipamide), MXD6. While PVDF copolymers are usually in semi-crystalline form with dipolar vectors perpendicular to the main polymer chain [1], MXD6 has been reported for ferroelectric-like properties but in amorphous state [6]. Transistor devices with spin-coated thin film of both materials have shown good memory functionalities of high ON/OFF ratio at zero gate voltage, long current retention time and high programming cycles [2-6].

Containing substantial amount of F atoms, PVDF copolymer has been known to have dipole vectors perpendicular to the substrate surface when the thin film is grown on a conducting surface [7]. The memory function is obtained by the manipulation of surface conductivity in the semiconductor layer due to the ferroelectric remnant polarization. It is realized by the existence of two turn-on (or threshold) voltages of opposite signs, and hence a hysteresis of drain current in the transfer characteristic curve. As the coercive voltages of the ferroelectric film (voltages at which polarization reversal occurs) have equal amplitude, the above-mention magnitude of turn-on voltages are ideally expected to be similar. Gate insulators modified with self assembled monolayers (SAM) have recently been reported to exhibit positive turn on voltage shift during transistor sweeping between OFF to ON state due to the nonswitchable dipole's field [8,9] and interfacial trapped charges [10]. This suggests that organic transistors using insulating PVDF

copolymer films are likely to exhibit similar behavior during switching which is critical in memory operation and has not been previously addressed.

Most of the reported devices were fabricated with a common gate structure that creates overlapping regions between gate and source/drain electrodes [2-6]. These regions of polymer-metal sandwiching make perfect capacitors for polarization switching. As a result, the source-drain bias (V_{SD}) is always applied at much smaller amplitude than the gate-source bias (V_{GS}) so that the potential difference from gate to source (V_{GS}) and drain (V_{GD}) is minimal. Polarization switching will then be similar throughout the bulk dielectric. When V_{SD} increases to reach channel pinch-off regime of the transistor, the difference of V_{GS} and V_{GD} is equal to V_{SD} value. As gate bias is swept, V_{GS} and V_{GD} will overcome the ferroelectric coercive fields and switch the dipoles at two different gate biases for each forward and reversed sweeping cycle. This will result in "double switching" by the gate-source and gate-drain sandwiching regions which eventually leads to degradation in OFF state behavior.

This chapter will examine the fabrication of FeFET using P(VDF-TrFE) copolymer as gate insulator with pentacene as semiconductor and the characterization of device operation and performance. The occurrence and effects of the positive turn-on voltage shift and the "double-switching" polarization to device performance will be investigated.

5.2 Experimental

Indium doped tin oxide (ITO) glass slides were cleaned by standard process (acetone, methanol, deionized water) in ultrasonic bath and blown dry with Nitrogen gas. Copolymer P(VDF-TrFE) solution was filtered using pore size of 0.45 μm and spin-coated onto the ITO substrates to form 1 ± 0.2 μm thick film measured by Surface Profiler. The samples were annealed in Nitrogen ambient at 140°C for 2 hours to enhance the film crystallinity [11] and adhesion to the ITO surface. Gold electrodes (1.5 mm diameter) were deposited by thermal evaporation onto the film to form metal-ferroelectric-metal

(MFM) capacitors. Hysteric polarization was measured from the MFM device using a Radiant Ferroelectric tester HVS6000 with high voltage options and subjecting the devices to a triangular signal frequency of 2 Hz. The dielectric constant was extracted from capacitance measured from the same device by using HP4284 LCR Analyzer at 1 MHz, 15 mV AC amplitude and zero DC voltage. Pentacene (Sigma Aldrich) was purified by temperature gradient sublimation in vacuum at 10^{-3} torr and then deposited by thermal evaporation onto the copolymer film. Pentacene evaporation was done at 5×10^{-5} Pa vacuum and rate of 0.1-0.2 Å/s to obtain 60-80 nm thick film. Pure gold (99.99%) was evaporated in 9×10^{-5} Pa vacuum through shadow mask to form top contacts for source and drain. Electrical measurement of transistors was performed using either Keithley2400 Sourcemeters with N₂ glove-box or Keithley4200 Semiconductor analyzer with vacuum chamber. The transfer characteristics (I_D - V_G) of the transistors were done by sweeping the gate voltage from positive value corresponding to the depletion state of the pentacene transistor (OFF state) to the negative value – accumulation state (ON state), and reversed to show the current hysteresis.

5.3 Results and Discussion

5.3.1 Ferroelectric field effect transistor with organic small molecule semiconductor

Bottom-gate FeFET device is shown as inset of Fig. 5.1(a) with the corresponding I_D - V_D curve. The device was observed to operate in accumulation mode of p-type transistor, in which holes are the hopping charge carriers. The copolymer layer is also seen to operate as an excellent gate dielectric layer. The mobility of the device (μ_{FE}) is determined to be 0.05 cm²/Vs in the saturated regime following the equation:

$$I_{D,sat} = \frac{W}{2L} C_{FE} \mu_{FE} (V_G - V_T)^2 \quad (1)$$

The capacitance C_{FE} of the dielectric P(VDF-TrFE) 57-43 mol% was measured to be 15.7 nF/cm² and dielectric constant ϵ is calculated to be 17. Recently, there have been a few reports from Naber et al. describing the ferroelectric transistor using similar P(VDF-

TrFE) copolymer but with higher composition of VDF component, e.g. 65 mol% VDF [2-4]. It is interesting to note that the copolymer with higher VDF composition possesses a higher value of remnant polarization (74 mC/cm^2) but of a lower dielectric constant (calculated to be 13) than the one used in this study ($\epsilon = 17$). The difference in the remnant value is due to the different amount of dipoles while higher dielectric constant of the copolymer in this case is due to the higher composition of Fluorine atoms from the trifluoroethylene groups in the gate dielectric as discussed in Chapter 4.

Figure 5.1 – Transistor characteristics of ferroelectric field effect transistor (channel W/L: 500:150 $\mu\text{m}/\mu\text{m}$) (a) I_D - V_D , inset shows device structure and (b) I_D - V_G , inset shows square root of I_D vs. V_G curve of the OFF-ON half cycle.

Figure 5.1(b) shows the transfer characteristic of the same device. The I_D - V_G curve is obtained by the cyclic sweeping of gate bias from positive – OFF state to negative – ON state. By subjecting the gate to positive voltage sweeping (+45V to 0V), the transistor is effective in OFF-state due to p-type semiconducting characteristic of pentacene. At the same time, positive voltage also orients the dipoles to upward direction, or pointing away from the bottom-gate. As voltage polarity switches at 0 V to negative values, the accumulation mode takes place in the pentacene layer as well as the reversing of dipoles in the P(VDF-TrFE) layer to downward direction (towards the bottom-gate). When gate voltage reaches -45 V, most of the dipolar domains with local coercive field E_C less than 45 V are switched to downward direction. As the bias is reversed in the second half cycle, the dipoles are undisturbed since the voltage polarity is not changed (from -40 to 0 V). However the apparent field at the gate is actually higher because it consists of the field of

the applied DC voltage and the electric field resulted **from** the dipolar direction. As a result, the measured drain current (I_D) is much higher than the one collected during the first half. A difference of 2 orders in current amplitude can be obtained at zero gate voltage as shown in Figure 5.1(b). This difference is **useful** for the application in non-volatile memory devices as it can represent ON ("1") and OFF ("0") states.

Figure 5.2 – Surface morphology of pentacene layer of different thicknesses as grown on (a) Si-wafer and (b) & (c) P(VDF-TrFE) layer.

The charge transport is well-known to depend on the quality of the deposited semiconductor layer which is reflected by the surface grain size and the crystalline structure [12]. It is hence useful to examine these characteristics for the evaporated pentacene on P(VDF-TrFE) layer that will help to explain the observed transistor behavior. Figure 5.2 and 5.3 present the data obtained **from** pentacene films of different thicknesses on copolymer surface as compared to the reference film on Si-wafer. The reference film shows a characteristic dendritic grain formation ($\sim 1 \mu\text{m}$ in size) which has been observed from slow evaporating rate process [12]. Due to the rod-like grain

topography of P(VDF-TrFE) (as being characterized in Chapter 3), the pentacene layer grows following this surface morphology if the thickness is kept to 45 nm. As the film thickness is increased to 80 nm, the pentacene layer can fully cover the P(VDF-TrFE) surface and create an uniform distribution of grain. In spite of the difference in coverage, the grain size of the thin and thick pentacene film is nearly identical (~200 nm). It is therefore seen that pentacene growth critically depends on the surface roughness of the substrate, which forms larger grains on smooth surface due to limited nucleation centers and better order at the first few monolayers. On the other hand smaller grains grow on irregular surface, which subsequently provides more nucleating centers at the inter-grain boundaries. Moreover it is most likely that the room-temperature growth had provided little room for the merging of the small grains.

Figure 5.3 – XRD crystalline structure of the pentacene layers as shown in Figure 5.2.

The crystalline structure of the pentacene films are examined in Figure 5.3. It is clear that from the well-developed dendritic grains, the reference film is better crystallized with up to 4th order diffracting plane being observed. As for films on P(VDF-TrFE) layer, crystallinity is only obtained in 80 nm-thick film with mainly first two diffracting planes. The peak positions are also found to increase slightly indicating the crystallization had developed into bulk form. The strong peak in the 45 nm-thick film is without doubt from

the P(VDF-TrFE) diffraction. It is interesting that the appearance of amorphous phase (raising curve of the baselines) is similar for both pentacene samples which is again likely resulted from the P(VDF-TrFE) layer as oppose to the reference film. The poor crystallinity and coverage of the 45 nm film are accounted for the non-functionality of devices fabricated with such thin pentacene film. The thicker film (60-80 nm) ensures device function, yet the small pentacene grain size had led to low mobility ($-0.05 \text{ cm}^2/\text{Vs}$) of charge transport in the semiconducting layer. One of the possible explanations is the scattering of charges at the grain boundaries as shown in Figure 5.2 [12].

Figure 5.4 – Characteristic of FeFET device with sweeping voltage applied up to saturation of polarization.

From the investigation of polarization in Chapter 4, it can be seen that a voltage of double the magnitude of coercive field is at least required to obtain saturating polarization in the P(VDF-TrFE) film. Figure 5.4 shows the characteristics of such operation including the transfer characteristic and leakage profile. As the polarization is saturated, the drain current retention is nearly unchanged at 0 V gate during the ON state and maintained until the positive coercive bias is reached. The dipolar switching can be observed from the peaks of gate current I_G at $|80| \text{ V}$ (corresponding to $|50| \text{ MV/m}$). It can also be seen that with the sufficiently thick dielectric layer ($-1.6 \text{ }\mu\text{m}$), the leakage is subtle (-1 nA) and mainly due to the displacement current. Figure 5.4 also depicts two anomalous phenomena observed in both drain and gate currents of the device that can affect the performance of memory functionality. First, it was seen that after a first few cycles of gate voltage sweeping, the turn-on voltage V_{to} is shifting toward a consistent positive

value. This basically does not change the device functions but reduce the ON/OFF ratio by increasing the OFF state current at zero gate bias. The second phenomenon is observed from the gate current appearing with multiple peaks. The pair of peaks at $|80|$ V is due polarization switching in the channel while the others are caused by switching in the overlapping regions of source/drain and gate electrodes. These phenomena are investigated in details in the later sections of this chapter.

Figure 5.5 Memory functionality of the FeFET device (a) ON-current retention after device fully written & (b) “switch-on” response by various pulsed voltages $V_G = -100$ V (c) programming time of drain current against pulse width.

The Fe-FET devices are examined for memory functionality with data shown in Figure 5.5 (a), (b), and (c) respectively. Varied pulse-width voltages were applied to gate electrode as indicated and the drain currents were measured with equipment capture-time of 1 μ s. The device is seen to well respond to the pulse width down to 1 ms similar to the reported device prepared with MEH-PPV and measured in N_2 ambient of which the fastest responding time is 0.5 ms [2]. The current retention can be maintained above 80% for more than 10^4 s duration. Figure 5.5 (c) shows the device response to the programming time (pulse-width) extracted from (b). As compared to previous report [2],

this response is more gradual than one of device made with MEH-PPV. It can be seen that response to ON and OFF state is essentially dependent on the density of charges and their responding speed in the channel of the semiconducting layer. The charge density here is rather low, $3 \times 10^{17} \text{ cm}^{-3}$, for pentacene [13]. This and possible degradation of semiconductor molecules under applied bias (e.g. carrier doping by deep traps) affect the stability of ON and OFF state and limit the device working speed.

Figure 5.6 – Characteristics of FeFET device using Al_2O_3 - TiO_2 and P(VDF-TrFE) as composite dielectric (a) I_D - V_G & (b) I_D - V_D .

To examine the possibility of reducing operation voltage by using thinner P(VDF-TrFE) film and reduce the leaking gate current, high quality oxide dielectric layer of 220 nm-thick Al_2O_3 - TiO_2 (ATO, $C/A = 60\text{-}70 \text{ nF/cm}^2$) was used together with 320 nm-thick copolymer. The composite dielectric allows the transistor to work in saturation mode by applying gate voltage of -40 V of which the coercive voltages of the P(VDF-TrFE) film are about $|20| \text{ V}$. Figure 5.6 shows good behavior of field effect with low leakage (I_D - V_D curve) yet a narrow drain current hysteresis was recorded (I_D - V_G curve). The narrow hysteresis was unchanged even as the applied gate voltage was increased up to $|60| \text{ V}$ or in the saturation mode $V_D = V_G = -40 \text{ V}$. Since the polarization hysteresis of a 320 nm-thick film was measured to be similar as the 1 μm -thick sample, the observed behavior is believed to be related to the separation between the copolymer layer and the gate electrode. As the dipolar switching involves the compensation of charges, the ATO layer hence behave as a blocking layer that hinders the enter and exit of charges between the electrode and the P(VDF-TrFE) as described in details in Chapter 4. Following the

analysis by Black et al, the compensation of polarization in this case was only up to 0.45 (as by C_{Fe}/C_o) [21]. Especially, the charge amount induced at -40 V gate bias was only $0.8 \mu\text{C}/\text{cm}^2$ ($Q_o = Q_{Fe}$) which was one-order smaller than the remnant polarization $-8 \mu\text{C}/\text{cm}^2$ of the used P(VDF-TrFE) film. It is believed that this device was under the effects of two processes such as the depolarization by the ATO capacitor and negative charge trapping at the interface (described in the next section). As a result, the turn-on voltage was critically shifted to the right and only a negligible drain current retention was observed as gate bias was swept from negative to positive.

5.3.2 Study of turn-on voltage shift in FeFET using P(VDF-TrFE) as gate dielectric

Polarization hysteresis of 1.2 μm -thick P(VDF-TrFE) (57-43 mol%) film is presented in Figure 5.7(a). The remnant polarization is $|6| \mu\text{C}/\text{cm}^2$ and the coercive voltage is $|70| \text{ V}$ (-15831 MV/m). The highest reported remnant value for this copolymer is $|7| \mu\text{C}/\text{cm}^2$ and the coercive field is generally $|50| \text{ MV/m}$ [14] for samples that had been thermally and mechanically treated to obtain a higher order structure. Using the reported value ($|50| \text{ MV/m}$), the corresponding coercive voltage of the copolymer film in this work should have a value of $|60| \text{ V}$, which is smaller than the measured value. The difference is likely due to voltage drop across very thin interfacial layers between the copolymer and the metal electrodes.

From Figure 5.7(a), a difference of $2 \mu\text{C}/\text{cm}^2$ between remnant polarization (P_R) and the spontaneous polarization (P_S) is observed, which results in the non-square shape of the P-E curve. Bolten et al. ascribed the loss polarization to a reversible process that exists concurrently with the irreversible polarization in thin film samples [16]. It has been also well recognized that local charge compensation of polarization is necessary to maintain the matter neutrality [17]. There are three types of contribution to the polarization properties of semicrystalline PVDF homopolymers, namely permanent polarization of dipoles in crystalline phase, frozen-in polarization in the amorphous state and the Maxwell–Wagner amorphous-crystalline interfacial polarization [18]. It has clearly linked the loss polarization observed in the P-E curve to the electrical properties of the

amorphous state and the interfacial states. The compensating charges to the dipolar polarization in these two states can, hence, be treated as trapped charge existing in the gate dielectric layer of the transistor device. The trapped charges are either created or released during the voltage sweeping at the transistor gate. As a result, interpretation of ferroelectric transistor's operation would require the understanding of the electrical behaviors not only from the dipolar polarization but also the trapped charges due to charge compensation.

Figure 5.7 – Characteristics of FeFET device showing (a) the polarization hysteresis of the P(VDF-TrFE) dielectric layer and (b) the shift of V_{t0} during the OFF-ON cycle.

The transfer characteristics (I_D - V_G) in the linear regime were obtained by sweeping the gate bias to values higher than the copolymer's coercive voltages as shown in Figure 5.7(b). The device was measured in nitrogen ambient inside a dark glove box to minimize the degradation of pentacene due to effect of air and moisture during bias stressing time. Before the transfer characteristic measurement, a voltage of +100V was applied to program the device to OFF state. The gate bias was then swept from +100V to -100V and back, with a constant drain voltage of -30V. The I_D - V_G curve shows a current hysteresis following a clockwise direction which is consistent with the hysteretic data reported in [Ref.2-4,6]. It indicates the current retention behavior is due to the dipolar polarization by the ferroelectric dielectric rather than charge trapping mechanism. In the current hysteresis which is caused by charge trapping, the hysteresis would be observed in the opposite manner in which the drain current in the reversed sweeping is smaller than that

of the first sweeping for the same gate voltage with the same gate voltage looping direction [19,20].

A significantly positive shift of turn-on voltage V_{to} , which is the gate voltage at which the drain current starts to increase exponentially, can be observed in the first sweeping cycle (+100 V to -100 V). In previous reports [Ref.2-5], the devices were shown to switch on by negative gate biases. While the negative turn-on voltage shows the complete operation in accumulation mode of the device, the observed positive V_{to} in this study implicates a possibly critical charge trapping mechanism [7,8]. Because of the positive shift of V_{to} in the first sweeping cycle, the ratio of On/Off current at 0V zero gate bias has deteriorated as observed (less than two-order difference).

In terms of p-type FET devices, a positive turn-on voltage is usually associated with device working in depletion mode. In this experiment, before the I_D - V_G curve was taken, gate voltage of +100V was applied to keep the device in OFF state. This voltage ensured all the dipoles aligned into the direction (pointing up, away from the gate) that would not accumulate holes in the pentacene layer. The device was then measured from OFF to ON state by sweeping gate voltage from +100V to -100V. If the pentacene layer is free from hole accumulations, a negative gate voltage higher than the coercive field (around -60V) is expected to switch the polarization and turn the device on similar to Ref. [2]. The large positive turn-on voltage V_{to} observed in I_D - V_G graph of Figure 5.7(b) clearly indicated significant hole accumulation (p-doping) in the pentacene layer. As the device was characterized in inert and dark ambient, it is therefore reasonable to believe that the P(VDF-TrFE) layer has a significant negative surface potential which is sufficient to induce hole accumulation in pentacene channel even during the OFF state of the device (e.g. gate voltage gradually drops from +100V to zero).

Similarly observed V_{to} shifts (or I_D - V_G behavior) have been investigated for pentacene transistor devices with self-assembled monolayer (SAM) of similar chemical functional groups on thermal oxides used as gate dielectric [8,9]. A large positive shift in turn-on voltage of about +60 V for device modified with 1H,1H,2H,2H-Perfluorooctyl

trichlorosilane having the highest number of F atoms in the functional end-group was recorded. By reducing the number of atoms but still keeping F in the functional group, a positive V_{to} shift was still observable at near +50 V in the case of Trichloro(3,3,3-trifluoropropyl)silane [8]. This was attributed to the effect of the SAM's dipole field and the increasing of trap states in the interfacial layer next to gate insulator. By applying their proposed model to the transfer curve in our experiment, the mobile charge carrier density induced by the surface dipoles of P(VDF-TrFE) layer is estimated to be $2.45 \times 10^{12} \text{ cm}^{-2}$, corresponding to a charge amount of $0.39 \text{ } \mu\text{C}/\text{cm}^2$. The total trap states are deduced from the threshold voltage above the turn-on voltage to be $1.47 \times 10^{12} \text{ cm}^{-2}$, or equivalent charge amount of $0.24 \text{ } \mu\text{C}/\text{cm}^2$. The results are surprisingly in good agreement with findings from Ref. [8] as well as from simulation model in Ref. [9]. Direct measurement on the top surface of a (PVDF-TrFE) film (20 to 50 nm thick on graphite substrate) also resulted in a negative potential of -40 mV [15]. The negative surface field can induce accumulation in the gate channel even without gate bias application. This explains the high drain current obtained during the device OFF state.

It is noted that combination of the above findings can only yield up to carrier charge of $0.63 \text{ } \mu\text{C}/\text{cm}^2$ in the channel. Using the model by Miller and McWhorter [18] with adjustments for device operating in accumulation mode, it had been found that the remnant value of the surface charge density yielded up to a quarter of the remnant polarization charge [2]. For the remnant polarization of $6 \text{ } \mu\text{C}/\text{cm}^2$ for the copolymer film in this case, the remnant surface charge density by the dipolar polarization could yield up to $1.5 \text{ } \mu\text{C}/\text{cm}^2$ that is about two-fold larger than the estimated total charge density of $0.63 \text{ } \mu\text{C}/\text{cm}^2$. Therefore, as the device is switched to OFF state, the total dipole field should be sufficient to compensate for all the defects described above and shift the turn-on voltage back to the negative value corresponding to negative coercive field. Another possible charge trapping mechanism caused by surface roughness of the gate insulator is also considered. The surface roughness R_{ms} of the P(VDF-TrFE) layer in this work was measured by Atomic Force Microscopy to be 15 nm, which falls within the range for semicrystalline copolymer thin film. Positive threshold voltage has previously been observed for organic transistor with rough gate dielectric layer (RMS up to 10 nm) but

the magnitude was small ($V_t \approx +2$ V) and did not depend on the dielectric roughness values [23]. The combination of the mentioned mechanisms, hence, cannot fully account for such a large turn-on voltage shift that has been observed.

For a complete explanation for the large positive V_{to} shift, compensating charge injection into P(VDF-TrFE) layer during switching due to different potentials at gate and drain electrode is examined. The right axis of Figure 5.7(b) shows the gate current profile of the same device which was recorded concurrently as the drain current was measured. The large value of the gate current (up to 1.75×10^{-7} A) obtained only during the ON state of the device is due to the leakage current through the semiconductor during accumulation. This occurred as the pentacene layer was not patterned that possibly created leaking paths between gate and source/drain electrodes. Apart from the current due to leaky paths, gate current in a ferroelectric transistor could also originate from the polarization reversal, e.g. displacement current (appears as peaks in I_G curve Figure 5.7 (b)). This contributes to the non-zero gate current during the device OFF state.

At the start of gate voltage sweeping (+100V, OFF to ON state), gate and drain current closely mimic each other showing a sudden drop from the initial value. At the beginning of this sweeping, the relative potential difference between the gate and drain was largest and the positive current spike at the gate indicates negative charges were injected to the P(VDF-TrFE) layer to compensate for the polarization buildup at the start of the sweeping cycle. It has been reported that the Fermi level located at a position much nearer to the unoccupied conduction band for an ultra-thin P(VDF-TrFE) film likely favors electron injection or removal from the film [15,24]. As PVDF copolymer is a wide band-gap insulator, the injected electrons were unlikely to be conducted to the positive ITO electrode but rather remained trapped at region near to the interface with pentacene. Combining the negative compensating trapped charges with the possible effects of dipole field and trap states discussed above, these defects could result in a gate field that overcome the reducing applied positive field and turn the transistor on at positive gate voltage. As gate voltage crossed zero and the device reached complete accumulation state, the trapped charges were released as the gate voltage now (-100 V) was more

negative compared to the drain voltage (-30 V). No charge trapping should occur during accumulation and as gate voltage returned to zero because of the existence of holes in the pentacene region near the interface. The drop of drain current from accumulation at -100 V to zero gate voltage is related to the release of non-switchable charges in the semicrystalline P(VDF-TrFE) film which is similar to the polarization (Figure 5.7(a)).

To observe the control of V_{to} shift, I_D - V_G curve measurements were done on a device ($L=100$ pm, $W=2000$ pm) after it was subjected to different positive pulsing gate voltages at fixed source-drain voltage $V_{DS} = -5$ V (Figure 5.8(a)). The transfer characteristic was measured right after the application of pulsing voltages and started from gate voltage of 0 V. It can be clearly seen that V_{to} (as determined by extrapolating from current value at 0 V gate) was strongly dependent on the magnitude of positive voltage applied at the gate. Different pulse durations (up to 60 seconds) at each voltage showed little effects on the V_{to} shift (Figure 5.8(c)). This indicates the negative charge trapping process in the P(VDF-TrFE) layer is a long and irreversible process. The relationship of I_D and V_{DS} shown in equation (2) was used to estimate the remnant charge density (σ) in the transistor device (linear regime was assumed as the device had been turned on due to the V_{to} shift). The results calculated from current values obtained by sweeping-up direction in Figure 5.8(a) are shown in Table 5.1.

$$I_D = \mu \frac{W}{L} \sigma |V_{DS}| \quad (2)$$

As discussed above, the effective remnant polarization by the P(VDF-TrFE) layer is about $1.5 \mu\text{C}/\text{cm}^2$, or corresponding to a surface charge density of $9.4 \times 10^{12} \text{ cm}^{-2}$. From Table 1, it can be seen that the charge trapping upon the application of a positive pulse voltage is much higher than the surface charge amount resulted by the remnant polarization. The amount of the excessive trapped charges in the copolymer dielectric layer is believed to result from the buildup of ferroelectric polarization which is contributed from the conductivity in the P(VDF-TrFE) layer [25]. This process was observed to occur at much slower speed as compared to the fast ferroelectric polarization (in microseconds range) and involved compensation charges in the non-ferroelectric (amorphous and paraelectric) phase in the semicrystalline thin film.

Table 5.1 – Summary of trapping charge values calculated from curves in Figure 5.8(a)

	I_D ($V_G = 0V$) (A)	σ_{trap} (cm^{-2})
Reference curve (no pulsing)	8.38×10^{-9}	5.25×10^{12}
Pulse 50V	6.61×10^{-8}	4.13×10^{13}
Pulse 80V	1.49×10^{-7}	9.38×10^{13}

Figure 5.8 – Characteristics of FeFET under pulsed gate voltages showing the effect of trapping charges to the V_{th} shift (a) & (c) I_D - V_G , (b) I_D -time.

To confirm the presence of negative trapped charges, time domain measurement was applied to the same device as shown in Figure 5.8(b). Positive pulse voltage of different amplitudes was applied to the gate for 100 seconds followed by a fixed -60V pulse to measure the behavior of the drain current. As discussed above, the application of a positive bias to the gate leads to different surface charge densities in the channel caused by the trapped charges in the P(VDF-TrFE) layer. By applying a negative voltage to the gate right after the pulse, partial amount of the negative charges should be detrapped [26]. As this occurred, the decaying hole population in the channel would led to the decrement

of drain voltage in the same manner. One may argue about the presence of the dipoles in the P(VDF-TrFE) layer that pointed towards the gate to enhance accumulation of holes in the pentacene channel. However, the results in Table 5.1 show a much higher concentration of trapped charges as compared to the accumulated charges by the dipoles. This, hence, indicates a more dominant effect of trapped charges. Another time-domain experiment using negative voltage pulses and followed by $V_G = -60V$ (Figure 5.8(b)) showed no changes observed in the drain current after the pulse period. This agrees with the consistency of the I_D - V_G curve swept from ON to OFF direction and evidently supports the negative charges trapping during the OFF to ON sweeping cycle.

5.3.3 Study of double polarization switching in FeFET - Comparison between common-gate and pattern-gate device

To understand different types of polarization switching, the polarization hysteresis was first measured with potential applied to vertical and horizontal direction using a common bottom-gate device structure as shown in inset of Figure 5.9. Biases were applied to either source or drain electrode and the ITO gate in the "vertical" measurement and to both source and drain electrodes with floating gate in the "horizontal" measurement.

Figure 5.9 – Polarization hysteresis of "horizontal" and "vertical" measurement. Inset shows hysteresis curves for different electrode and channel dimensions: L-length, W-width and electrode structure for hysteresis measurement. Bias was applied to bottom ITO and one of gold electrodes for "vertical" test, and to both gold electrodes for "horizontal" test.

Figure 5.9 shows the saturated polarization hysteresis for both of the "vertical" and "horizontal" measurement. The "vertical" data are consistent with the reported values for P(VDF-TrFE) (70-30 mol%) copolymer with coercive field of $\sim|50|$ MV/m and remnant polarization of $\sim|10|$ $\mu\text{C}/\text{cm}^2$ [14]. The "horizontal" measurement data show similar coercive values while the remnant values are about 60% of the "vertical" ones. The similar coercive values indicate the polarization switching in both cases has the same characteristics with bulk polymer. Based on these observations, it is concluded that the tested device should behave as two identical capacitors in back-to-back series connection during the "horizontal" measurement. As a result the measured remnant polarization was almost half of the bulk value. To further confirm, the "horizontal" measurement was done on devices with various electrode and channel dimensions (inset of Figure 5.9). The obtained coercive and remnant data are independent of the separating gap lengths or widths. Hence, this confirms the possibility of polarization switching caused by varied bias between source and drain electrodes in transistor device.

To examine this phenomenon in transistor operation, 80 nm-thick pentacene was used as semiconductor layer with channel length and width of 1000 μm and 100 μm , respectively. The transistor was characterized in a dark vacuum chamber. The I_D - V_G measurement was done by cyclically sweeping the gate bias while keeping constant drain potential with respect to the source. Figure 5.10 show I_D - V_G and I_G - V_G data for the ferroelectric transistor measured at three drain voltages (V_{SD}). There are two switching current profiles existing in the I_G - V_G curve observed as current peaks. The one with two peaks locating at ± 80 V is caused by the vertical potential between gate and source electrode (V_{GS} switching) and independent of V_{SD} . The other two peaks shifted to more negative bias accordingly to the increased V_{SD} , which was caused by the anomalous polarization switching resulting from the gate-drain potential difference V_{GD} with a dependence on the magnitude of V_{SD} (V_{GD} switching). The current peaks' values are shown in Table 5.2. The relationship of V_{SD} , V_{GS} , and V_{GD} can be generalized as:

$$V_{GD} = |V_{GS}| + V_{SD}, \text{ with } \begin{cases} V_{GS} < 0, \text{ for positive-to-negative switching} \\ V_{GS} > 0, \text{ for negative-to-positive switching} \end{cases}$$

Figure 5.10 – Electrical characterization I_D - V_G & I_G - V_G of common bottom gate Fe-FET device with 1.6 μm thick P(VDF-TrFE) dielectric layer. Arrows show the direction of drain current hysteresis.

Table 5.2 – Tabulated switching current peaks for data shown in Figure 5.10

Source-drain bias V_{SD}	Switching peaks by V_{GS}	Switching peaks by V_{GD}
-10 V	-80 V / +80 V	-88 V / +70 V
-30 V	-80 V / +78 V	-106 V / +48 V
-50 V	-80 V / +75V	-126 V / +26 V

Figure 5.1 1 shows plots of equipotential contours determined in the P(VDF-TrFE) layer sandwiched by gate and source/drain electrodes under various fields applied at gate. The data of this simulation were obtained from a collaborated project for which the author would like to acknowledge Professor Haibin Su and Nathaniel Ng (NTU). The results were attained by solving Maxwell equation (Gauss law) using finite difference method [27]. In considering only the distribution of electric field in the dielectric layer, polarization and charge density terms were ignored. The simulated biases are relatively scaled to the real testing voltages. The potentials are kept constant at source ($V_S = 0$) and drain ($V_D = -0.5$ or -0.1). As the gate is operative with bias reaching -1 (ON state) or $+1$ (OFF state), the contour density is distributed more densely at the region under the source or the drain respectively in the case of $V_D = -0.5$. For the case that V_{DS} is much smaller than V_{GS} ($V_D = -0.1$), the contour density is almost uniform in the dielectric layer during the operative stages of sweeping gate bias. This agrees with our experiment data (in Table 5.2) for the order of V_{GS} and V_{GD} switching in the negative and positive sweeping

cycle as discussed above. It is also seen that as gate bias approaches 0 and switches its polarity, the contour density is only redistributed below the drain electrode. Hence this likely caused the earlier switching to the opposite polarization of the region between gate-drain and reduced the accumulation of charges in the channel, which led to reduction in I_D retention.

Figure 5.11 – Plots of equipotential contours calculated for transistor electrode structure as shown in Figure 5.9.

To remove the anomalous V_{GD} switching, bottom patterned gate device was fabricated as shown in Figure 5.12(a). Patterned gold gate was formed by thermal evaporation through a shadow mask on cleaned glass substrate. The overlapping between gate-drain electrodes is minimized by keeping the gate and channel gap of same dimensions and aligning the gate electrode edges to those of source and drain. Similar I_D - V_G tests were applied to the device. The data presented in Figure 5.12(b) clearly show the removal of the shifting V_{GD} switching peaks in the gate current I_G - V_G profile as well as in the OFF state of I_D - V_G current. The maintenance of hysteresis and direction of drain current indicates the polarization switching mainly establishes in the channel region. The device performance

is improved with the good I_D retention as well as a more constant and low leakage current during OFF state.

Figure 5.12 – (a) **Optical** micrograph of patterned gate Fe-FET device. (b) I_D - V_G characteristic of the shown device. Arrows show hysteresis direction. Inset shows I_G - V_G data. (c) I_D - V_G characteristics of device with 10% overlapping between gate and **source/drain** electrodes. Inset shows I_G - V_G data.

Figure 5.12(c) show the I_D - V_G data for a device with the Au-gate electrode having 10% area overlapping with the source and drain electrodes. The device was measured similarly to one in (b) which also exhibits the horizontal polarization switching and behaves in the same manner. Based on this, it is concluded that the anomalous switching is not

originated by the difference in amphiphilicity of ITO and Au surface but purely due to the switching in the overlapping regions.

5.4 Conclusion

Ferroelectric field effect transistors have been demonstrated using small molecule semiconductor which allows the investigation of device operation characteristics and effect of device structure to performance. Memory functionality from clockwise hysteresis of drain current by sweeping of gate voltage is resulted by dipolar polarization of the ferroelectric copolymer. Due to the irregular surface of semicrystalline rod-like grains, formation of the semiconductor layer critically affects device performance. Sufficiently thick semiconducting layer is required to completely cover the copolymer dielectric to result transistor behavior. The gate voltage application needs to be higher than coercive field of the ferroelectric film to attain saturating and stable transistor characteristics. The memory retention is found up to 80 % for more than 10^4 seconds period and the response time can reach to 0.1 ms.

Large positive turn-on voltage shifts were observed as gate bias was swept from OFF to ON state. Investigation of current retention against time showed a transient behavior of drain current both when the gate voltage is applied and removed. Accumulation of mobile holes in the pentacene channel during the application of positive gate voltage was determined to account for the shift. Deep trapping and slow detrapping process in both dielectric layer and semiconducting layer were attributed to the transient behavior of drain current. Analysis combining properties of the copolymer insulator layer and transfer characteristic of transistor during OFF to ON state sweeping explained the observed phenomena by employing three mechanisms: 1. The dipole field caused by strong electronegativity of Fluorine atoms leading to a negative surface potential, 2. The interfacial charge traps between a polar dielectric and an organic semiconductor which possibly results the broadening of the Gaussian distributed transport state, 3. The

injection of negative charges from drain to the insulator region near the dielectric-semiconductor interface.

Two different types of polarization switching in an organic ferroelectric field effect transistor using bottom common gate has been studied. One is resulted from biases between gate and source that contribute to drain current hysteresis, while the other is caused by potential difference between gate and drain that closely follows drain voltages. Field distribution in the ferroelectric layer with regards to the potential differences at the electrodes is directly responsible to the sequential polarization switching, which leads to unstable high OFF leakage current hence resulting in uncontrollable OFF state of the memory device. Reduction of electrode overlapping to minimize the gate-drain polarization switching can result in improved device performance, which is applicable to integrated non-volatile memory devices.

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Chapter 6

STUDY OF STRUCTURE AND PROPERTIES OF STRETCHED P(VDF-TrFE) FILM ATTACHED TO A FLEXIBLE SUBSTRATE

6.1 Introduction

To increase the crystallinity and ferroelectric properties of PVDF and copolymer, different methods have been employed including: mechanical stretching, thermal annealing, and electrical poling [1,2,3,4]. Out of these methods, mechanical stretching (uniaxial/biaxial) has been usually applied to pure PVDF copolymer in which the process is accompanied by high working temperature. Due to flexibility of polymer, stretching up to plastic deformation is the most efficient method to yield high film crystallinity as the polymer chains can be reorganized along the stress direction. However, the working film must be sustainable by itself which requires sufficient thicknesses (at least of 15 μm). For thin ferroelectric polymer films which are used for electronic device application, much smaller thickness (less than 5 μm) is required for low power consumption. Ferroelectric properties of these thin films hence cannot be improved by mechanical methods.

To overcome this obstacle, Trifluoroethylene (TrFE) is added to PVDF polymer resulting in the usual random block-copolymer P(VDF-TrFE). The copolymers with various compositions were shown to crystallize into high percentage of ferroelectric phase that only requires annealing process [4]. The annealing is done at temperatures above the Curie point and below the melting point for sufficient duration. The best properties obtained from this process are the highest remnant polarization of 10 $\mu\text{C}/\text{cm}^2$ and coercitivity of 50 MV/m [1,4,5]. As a result, annealing and possibly accompanied by electrical poling is the most suitable method to obtain high quality crystalline ferroelectric film for device application as discussed in Chapter 3. One of the drawbacks of this procedure is the resulted surface morphology of the working film (refer to Chapter 3). Due to the high crystallinity (up to 80%), the film topography appears with random oriented rod-like grains which intercept each other resulting in irregularity of vertical walls and deep valleys. The surface roughness and non-uniformity are the main

hindrances to the performance of the electrical device as a whole (refer to Chapter 5). So far the topic of top surface quality has been of great interest especially in multilayer devices (refer to Chapter 3).

In this chapter, it will be shown that by attaching the thin P(VDF-TrFE) film to a flexible substrate the whole sample can be modified by means of mechanical stretching. In the company of low temperature annealing process, ferroelectric properties similar to that at high temperature annealing can be obtained. The surface morphology can be greatly improved with a different type of crystalline grain being formed. These enhancements lead to the improved performance of non-volatile memory device.

6.2 Experimental

Polyethylene terephthalate (PET) (110 μm thick) with laminated Aluminum electrode (100 nm thick) was used as substrate in all experiment. Film properties are shown in Table 6.1. The substrates were cut into suitable sizes and cleaned with acetone, methanol and deionized water. P(VDF-TrFE) (70-30 mol%) solution (concentration of 50 mg/cc) was filtered through 1 μm pore size and spin-coated on the substrate. The samples were then kept in vacuum oven at 40°C for 1 hour to remove the excess solvent.

Table 6.1 – Properties of PET substrate and P(VDF-TrFE) copolymer

	PET	P(VDF-TrFE)
Tensile modulus	2-4 GPa	1.1 GPa
Volume resistivity	$>10^{14} \Omega\cdot\text{cm}$	$>10^{14} \Omega\cdot\text{cm}$
Thermal expansion coefficient	$20-80 \times 10^{-6} \text{K}^{-1}$	$100 \times 10^{-6} \text{K}^{-1}$
Elongation at break	60-165%	400%
Upper working temperature	115-170°C	110°C

Stretching of samples was done in *situ* using Instron Microforce tester with 2 kN load which allows accurate application of strains and monitoring of the corresponding stresses. Annealing of samples was performed simultaneously with stretching. The chamber was preheated to a defined temperature before samples were loaded onto holder and kept for 30 minutes to stabilize the environment temperature. This eliminates the effects of

thermal expansion and prevents any annealing effects before stretching taking place. Once the preset temperature maintained constant, the stretching was begun at rate of 50 N/min. When the required strain (elongation percentage) was reached, samples were kept stretched and heated for 1 hour. After that, the chamber was allowed to naturally cool down to ambient temperature while samples were still stretched.

Changes in crystallinity and molecular configuration were investigated by FTIR (PerkinElmer). Surface morphology of the stretched film was obtained from AFM in non-contact mode. Sheet resistance of the Al electrodes with various applied strain was measured using 4-point resistant probe (Table 6.2). Polarization hysteresis was measured from metal-ferroelectric-metal (MFM) device by thermally evaporating gold through shadow mask onto the copolymer surface. For FeFET, pentacene was evaporated as described in Chapter 5 followed by source/drain electrodes formation. The devices were then characterized in dark vacuum chamber using Keithley semiconductor analyzer.

6.3 Results and Discussion

6.3.1 Mechanical behavior of stretched samples

Mechanical performance of a bare Al-PET film is presented in Figure 6.1 under the application of 100% elongation (strain). The data shows that the lamination of the Al electrode (100 nm thick) does not change the mechanical properties of the PET film (Table 6.1). The highest strain of 100% is well in the working limit of the PET substrate and also does not cause rupture of the Al-electrode as examined under microscope. Nevertheless the applied strain slightly increases the surface resistivity of the Aluminum as shown in Table 6.2. The maximum elongation that can be applied to the PET film is less than 200% which is far less than the process used to orient the PVDF or copolymer film (–400%) [1,3,4]. As a result, stretching of sample up to 100% strain at room temperature is not expected to induce sufficient crystallization and formation of ferroelectric phase. To solve this problem, additional annealing is applied simultaneously with the stretching to increase the nucleation and growth of ferroelectric domains. It will

be showed that by combining stretching and annealing of sample both the strain and temperature used can be greatly reduced as compared to the use of single process.

Figure 6.1 – Mechanical properties of bare Al-coated PET substrate as stretched to 100% strain at room temperature 25°C.

Table 6.2 – Changes in film resistance with applied strains

% Strain	Average Resistance (Ohms per square)	Fractional change in resistance ($\Delta R/R$) (%)
0	1.367	0.000
100	10.934	6.999

Figure 6.2 – Mechanical behavior of stretched samples at various temperatures.

Figure 6.2 examines the mechanical behaviors of samples consisting of Al-coated PET plastic substrate with spin-coated P(VDF-TrFE) layer. Combined effects of stretching and annealing are compared to the reference behavior as shown in Figure 6.1. It can be

seen that at room temperature the sample follows the behavior of the Al-PET substrate with elastic region up to 4% strain and linearly flat plastic region. As temperature increased to 50°C, the elasticity only follows the substrate up to 3% then the sample exhibits exponential increment of stress in the plastic region. Similar behavior is observed at 70°C but with higher stress generated during plastic deformation. The plasticity dominates the sample stretched at 120°C with the elastic region almost disappearing. It is also seen that the stress value in the elastic-plastic transition region decreases as temperature is raised. This indicates the increment of polymer chain mobility possibly in both PET substrate and P(VDF-TrFE) thin film that leads to more easily glide along elongating direction hence reduces stiffness.

6.3.2 Effects of stretching to crystalline structures and phases

The crystalline structure and molecular group configuration are examined by FTIR spectra for all the samples. Figure 6.3 presents the changes caused by annealing of standard process at 140°C in 2 hours for reference P(VDF-TrFE)-coated Al-PET sample. As sample was annealed at 140°C, the drastic reduction of viscosity allowed polymer chains to glide along and reorganize into high-order regions of paraelectric phase. Due to the presence of TrFE groups, the head-tail interaction between F and H atoms was reduced which directly led to more β -phase formation by annealing [4,5].

Overall it can be seen that most of the absorption bands become sharper and increases in intensity after annealing. In details, the 1400 cm^{-1} band is most sensitive to the ordering of the crystallization of P(VDF-TrFE) copolymer that it appears with the sharpest rise [6,7]. Two sharp peaks 883 and 850 cm^{-1} relates to the ordered phase of *all trans* and *trans-gauche* sequence, respectively. However it has also been shown that there is possible overlapping of bands from similar polymer chain sequences but in the disorder phase. In particular, the increment of 1286 cm^{-1} band relates to both crystallinity and trans sequence of more than 4 monomers, hence its changes help to predict if a sample possibly exhibits polarization switching. The broad band with peak at 1173 cm^{-1} also links to the formation of ordering phase and especially when accompanied by the sharp

rise of 1400cm^{-1} band. However, as being observed later, the increasing of 1173 cm^{-1} band does not require thermal treatment as shown in Figure 6.4(a) which possibly indicates the formation of trans-gauche chain sequence in both order and disorder phase. As a result, the change in 1400 and 1286cm^{-1} band is used to compare the crystallinity and ferroelectric phase transformation, respectively, particularly for sample exhibiting long-range order.

Figure 6.3 – FTIR spectra showing the effects of annealing on crystallinity and phases of P(VDF-TrFE) film spin-coated on Al-PET substrate.

Figure 6.4(a) presents the spectra of samples stretched to 50% strain at room temperature (RT) and 70°C . The P(VDF-TrFE) film crystallinity from 1400 cm^{-1} band is found to be similar for both stretch samples and the one annealed at 140°C . For sample stretched at room temperature, the magnitudes of the 1400 and 1173 cm^{-1} band are slightly reduced while the 1286 cm^{-1} band is seen unchanged as compared to the non-annealed sample. As mentioned above, this indicates the reorganization of polymer chains along the stress direction into ordered trans-gauche sequence yet without the transformation to ferroelectric phase. It hence emphasizes the need of thermal activation for phase transformation in P(VDF-TrFE) film.

In the case of sample simultaneously stretched and annealed (70°C), the viscosity was rather high but the polymer chains still glided along the stress direction and reorganize

into order domains which can be seen from similar crystallization behavior shown in 1400 cm^{-1} band. Yet because of the low temperature, nucleation and growth of β -phase (or transformation from para to ferroelectric phase) was limited as seen by the smaller magnitude of 1286 cm^{-1} peak of 50%-70°C sample. Another evidence of the incomplete reordering of polymer chains is the slight increment of the 1243 cm^{-1} band. From these comparisons, it can be seen that standard annealing process allows the polymer chains to sufficiently reorganize into order phase of lowest free energy and converse from paraelectric to ferroelectric phase due to reduced head-to-tail defects. Mechanical stretching is recognized in aligning the molecular chains along the stress direction by plastic extension. However the extend of this alignment strongly depends on the viscosity of polymer chains which is governed by working temperature. Furthermore, as samples were stretched from the as-spun state, reorganization of chains mainly occurs in amorphous or disorder phase [8].

Figure 6.4 – FTIR spectra of stretched samples at different strains and temperatures as compared to reference sample.

Figure 6.4(b) examines samples processed at 70°C with one fully annealed at 140°C for 2 hours before being elongated to 25% length, and the other stretched from as-spun state up to breaking of the PET substrate (at 75% strain) without delaminating the P(VDF-TrFE) film. For the pre-annealed sample, stretching and elongating of chains should occur in amorphous regions first before taking place in the crystallites. Yet this stretching is

limited by the stronger interchain interactions and random orientation of crystalline phase (as seen from AFM surface morphology in Figure 6.6(a)) which absorbs most of the applied energy. If the strain is sufficiently high, the interchain bonding in crystalline phase is broken. When temperature is cooled down the polymer chains are unable to resume the favorable packing position attained during annealing step. This leads to reduction in crystallinity as being seen with smaller intensity of 1400 cm^{-1} band in Figure 6.4(b).

If the strain is excessively applied to the as-spun sample till breaking point (75% elongation before breaking) at 70°C , both crystallinity and phase transformation are obtained. Nevertheless only part of the applied stretching energy is consumed in plastic deformation. Once the sample yields to the necking region right before the breaking point, most of the energy is absorbed in chain resistance to glide further [8]. As yielding takes place at high strain values and only at certain locations on sample that are prone to necking, the strain distribution over the sample is not uniform. At locations exhibiting high strain application, relaxation of polymer chains possibly occurs during cooling duration. Due to severe deformation of necking polymer chains are unable to reorganize to long-range order packing regions and relax to amorphous phase with certain short-range order. The strong 1286 cm^{-1} band is hence possibly resulted from chains of short *trans* sequence. This results to overall lower crystallinity as seen in Figure 6.4(b).

Figure 6.5 shows the comparison of different samples stretched at 70°C . It can be seen that the most favorable condition is the application of 50% strain as good crystallinity and ferroelectric phase transformation are obtained. Sample stretched at 70% elongation and 70°C has similar characteristics as one stretched to breaking point i.e. strong 1286 cm^{-1} but weak 1400 cm^{-1} band. Especially, necking was also observed in 70%-strain sample. It is hence suggested that relaxation of molecular chains to short-range order region also dominated during cooling. From the data, it is then expected sample stretched to 50% elongation at 70°C will exhibit strongest polarization properties.

Figure 6.5 FTIR spectra of variously stretched samples at 70°C.

Assuming that the IR absorption only follows the Lambert-Beer law, the A_α (of alpha phase) and A_β (of beta phase) absorbance, respectively, are given by [7]

$$A_\alpha = \log \frac{I_\alpha^o}{I_\alpha} = K_\alpha C X_\alpha L \qquad A_\beta = \log \frac{I_\beta^o}{I_\beta} = K_\beta C X_\beta L$$

for a sample of thickness L , and an average total monomer concentration C (0.0305 mol/cm^3). In the above equation, I^o and I are the incident and transmitted transmission intensity respectively. The A_α and A_β values were determined by ratio of I^o and I which is the transformation percentage. The amount of phase formed was compared by calculating the relative beta phase formation for samples with long-range order. With K_α and K_β having values of 6.1×10^4 and $7.7 \times 10^4 \text{ cm}^2/\text{mol}$ respectively, the relative fraction of beta phase F_β can be expressed as [7]:

$$F_\beta = \frac{X_\beta}{X_\alpha + X_\beta} = \frac{A_\beta}{\left(\frac{K_\beta}{K_\alpha}\right) A_\alpha + A_\beta} = \frac{A_\beta}{1.26 A_\alpha + A_\beta}$$

Table 6.3 – Summary of F_β values for various strain values at different temperatures

Strain	Temperature (°C)	F_β
0%	140	0.43
25%	120	0.51
50%	70	0.48

From Table 6.3, the β -fraction (F_β) of a standard annealed (140°C , 2 hours) sample yields up to 30%. As sample is stretched to $\frac{1}{4}$ of the original length at 120°C , the fraction

slightly increases compared to that of the reference. It can be seen that at annealing temperatures near melting point the applied strain enhanced the ordering of the polymer chains that resulted to higher fraction of β -phase for shorter duration (30 minutes as compared to 2 hours in the standard process). Based on this, working temperature can be reduced further to 70°C by raising the strain to 50% which results in compatible value of beta phase fraction. The F_β will be shown to be in good agreement with the polarization properties in the later section.

6.3.3 Surface morphology of stretched P(VDF-TrFE) films

Surface morphology of annealed and stretched sample is shown in Figure 6.6. After standard annealing process P(VDF-TrFE) film crystallizes with rod-like grain structure on the top surface as described in Chapter 3. This hence indicates the substrate flexibility does not affect the crystallization and reorganization of the polymer chains during annealing. Figure 6.6(b) presents a completely different topography of the sample stretched to 25% strain at 120°C. The new morphology appears as flat grains which are close-packed and stacked in groups together. The surface roughness RMS is much improved and measured to be 4.5 nm comparing to that of annealed sample of 15.4 nm. It is hence expected to promote the uniform growth and also helps to reduce the thickness of the semiconducting layer using the stretched samples.

As indicated by FTIR spectra, the crystallinity of film stretched at 70°C can be improved mainly due to the tensile stress. It is therefore expected to have similar flat grain morphology for stretched films at this lower temperature. Topographical images of various stretched samples are shown in Figure 6.7. At the lowest strain of 25%, the flat grain formation starts to take place. As the applied strain increases to 50% the grain topography becomes smoother and closer in packing. It can also be seen that the grain formation is in the vertical direction of the image which is almost perpendicular the stretching direction. As discussed in Chapter 3 and from previous reports [9], the polymer chains have been found to fold across the long-axis of the rod grain in semi-crystalline film. As a result, the formation of flat grains seen here should be similar to rod-like grains

but the growth evolves in the planar short-axis (stretching direction) to expand the width rather than developing out of the surface to form vertically steep wall.

Figure 6.6 – Surface morphology of (a) an annealed sample (140°C, 2 hours) and (b) sample stretched to 25% strain at 120°C for 30 minutes.

In general the density of the flat grain increases with higher strains and is accompanied by small reduction of surface roughness. The decreased roughness is suggested to result from the better coverage of the flat grains as well as the disappearance of the granular feature seen in the lower strain case. Nevertheless once higher grain packing is attained with higher strain (70% and near yielding) surface roughness drastically increases as shown in Figure 6.7. As discussed above, up to necking point at high strain the hardening of polymer chains took place which prevents them from further gliding. Furthermore, during annealing time relaxation occurs that alters the ordered phase to regions of **short-range** order mixed with disordered phase. This consequently leads to more irregular topography and exacerbates the surface roughness.

Figure 6.7 – Surface morphology of various stretched samples at 70°C
(a) 25% (RMS = 7.74 nm), (b) 50% (RMS = 5.66 nm), (c) 70% (RMS = 13.08 nm).

6.3.4 Polarization properties of stretched film

Figure 6.8 – Polarization hysteresis of reference sample (P(VDF-TrFE) on Al-PET substrate, annealed at 140°C for 2 hours).

Polarization hysteresis of a reference sample is shown in Figure 6.8 indicating standard ferroelectric behavior for P(VDF-TrFE) film on flexible substrate. The presented data show polarization saturated at 150 MV/m which is three times of the coercive field similarly described in Chapter 4. The remnant polarization is about $|10| \mu\text{C}/\text{cm}^2$ corresponding to the strongest increment of 1286 cm^{-1} band of FTIR spectrum (Figure 6.3). In the bias range of $\sim |100| \text{ V}$ for transistors, the hysteresis is seen to approach the saturating state hence the condition of fabricating the ferroelectric film on flexible substrate here is **efficient** for memory device.

Figure 6.9 – Saturating polarization hysteresis of samples stretched to (a) 25% and (b) 50% at various temperatures.

Figure 6.10 – Saturating polarization hysteresis of samples stretched to various % elongations at 70°C.

Figure 6.9 and 6.10 present the hysteresis data for samples stretched to 25% and 50 % strain, respectively, at various temperatures. It can be seen that the polarization switching is strongly dependent on temperature. As samples were stretched to lower strain level (25%) it requires the working temperature to be above the Curie point ($T_C = 100^\circ\text{C}$, Figure 3.2) for a complete transformation into ferroelectric phase as compared to reference annealed sample. At temperatures below T_C , the remnant polarizations yields to half of the maximum value of $10 \mu\text{C}/\text{cm}^2$ while the coercive fields are slightly larger than 50 MV/m as seen in Figure 6.10. The similarity in the coercitivity and the slope resulting to reversible polarization P_R (discussed in Chapter 4) for samples stretched above and below T_C indicates the resemblance of chain reorganizing by elongation in all

the samples and up to 50% strain. It also emphasizes again the role of working temperature in ferroelectric-paraelectric phase transformation.

6.3.5 Application of stretched substrates to flexible organic Fe-FET

Figure 6.11 – Surface morphology of pentacene layer thermally evaporated on the stretched P(VDF-TrFE) surface.

Figure 6.12 – Electrical characteristics of FeFET device fabricated on substrate stretched at 120°C and 25% elongation ($W/L = 2000:100$, mobility = $0.085 \text{ cm}^2/\text{Vs}$) (a) I_D - V_D & (b) I_D - V_G with inset showing I_G - V_G .

Surface morphology of the pentacene layer thermally evaporated on P(VDF-TrFE) film stretched at 120°C to 25% elongation is presented in Figure 6.1 1. The pentacene grains are shown to be densely packed and have average diameter of nearly 200 nm. The 3-D topology shows the grains grow separately into vertical direction which may limit the size and leads to lower transistor performance. Figure 6.12 shows the electrical

characteristics of device ($W/L = 2000:100$) fabricated on substrate stretched to 25% elongation at 120°C. Due to the drastic reduction of surface roughness of P(VDF-TrFE) film (RMS = 4.5 nm, Figure 6.6), the pentacene growth was attained with better quality allowing the film thickness to be reduced to around 50 nm. The mobility is much improved up to 0.085 cm²/Vs, about doubling of the value obtained for device on standard annealing P(VDF-TrFE) film with 80 nm-thick pentacene layer. This improvement is likely resulted from less scattering of charge carriers at regions near dielectric – semiconductor interface and at the grain boundaries due to larger size.

The drain current hysteresis in Figure 6.12(b) is consistent with polarization switching mechanism of P(VDF-TrFE) in FeFET device as described in Chapter 5. The leakage is however found to be 2-3 times higher than that of devices with annealed films of similar thickness. From Figure 6.6(b), it can be observed that topology of the stretched film is still uneven in spite of the lower roughness. The flat grains are seen to stack against each other leading to high unfinished surface area at grain boundary. The leakage current from the inset of Figure 6.12(b) critically increases in the accumulation mode of transistor which is similar to the device with standard annealed P(VDF-TrFE) film as discussed in Chapter 5. Due to the appearance of more edges of the flat grains in P(VDF-TrFE) (Figure 6.6(b)), the leakage current flowing vertically from gate to source electrode could follow the defects along these grain boundaries. Comparing to the case of annealed film where leaking-prone locations are mainly due to the interception of vertical grains resulting deep valleys or pin-holes, the defects here are likely due to the high area density of boundary which can be reduced by growth of large flat grains.

Performance of current retention and response to various gate pulse widths are shown in Figure 6.13. Similar to device reported in Chapter 5, the shortest pulse the device responds to is about 1 ms. It can be seen that the gate pulse can result to reaction in transistor device down to 100 μs. The absence of permanent increased drain current indicates the inactivity of dipole rotation that is the limit of switching speed of P(VDF-TrFE) of 900 nm thick film. It has been reported the fastest switching speed of P(VDF-TrFE) film at 300 μs at field of 100 MV/m [10]. Figure 6.13(b) presents the retention of

device followed 1 s writing pulse the current level is well maintained up to 5000 s with the ON/OFF ratio extrapolated to more than 10^4 s for 2-order difference similar to previous report [11].

Figure 6.13 – Performance of drain current retention for device stretched at 120°C to 25% elongation and measured with $V_D = -10$ V (a) response against gate pulse width & (b) retention after 1 s pulse.

Figure 6.14 – Different drain current configurations against stretching direction indicated by arrows (a) current parallel to stress & (b) current perpendicular to stress.

Figure 6.15 – Comparison of current configuration against stretching direction for different channel dimensions (W-width, L-length, with unit in μm).

With the whole sample being uniaxially stretched, the reorganization and alignment of P(VDF-TrFE) chains are expected to follow the stress direction. As transistor device is usually fabricated with highly unequal channel length and width dimension, the dependence of device performance due to relative direction between stress and current flow (as shown in Figure 6.14) is examined. Figure 6.15 shows the compared hysteresis of drain current for devices of different dimensions. In all cases, the current retention (I_D at 0V) is almost similar during the ON to OFF sweeping cycle. For the smallest channel (1000:100), the turn-on voltage (V_{to}) in the perpendicular current case behaves better than that of the parallel case which leads lower I_{OFF} current and hence larger ON/OFF ratio. However as the channel dimensions are increased, especially length, I_D - V_G curves of the parallel and perpendicular current approximately resemble each other. It is hence suggested that the shift of V_{to} and small change of current amplitude purely be experimental variations and device characteristics are uniquely independent of stretching direction.

Figure 6.16 – Surface morphology of pentacene film evaporated on stretched P(VDF-TrFE) sample stretched at (a) 25%, (b) 50% (mobility μ), and (c) 70% at 70°C.

As discussed above, same quality and characteristics of stretched P(VDF-TrFE) film can be obtained at working temperature lowered to 70°C and strain raised to above 25%. Figure 6.16 shows series of AFM images for pentacene layers deposited on variously stretched P(VDF-TrFE) films. Similar to pentacene layer evaporated on sample stretched at 120°C to 25% elongation, grains in round shape are found on pentacene layer deposited on sample stretched at same strain but lower temperature 70°C. On the other hand, pentacene grains on 50%-strain sample are seen in elongated shape which likely follows the orientation of grain structure of the beneath P(VDF-TrFE) layer. Overall the grain size for these two samples is in range 100 to above 200 nm size which indicates enhancement **from** smooth morphology of flat grains structure of P(VDF-TrFE) layer. In contrary, due to high surface roughness of 70%-strain sample the pentacene layer grows into smaller and disordered grains which look similar to that on annealed copolymer film (Chapter 5).

FeFET performances of variously stretched P(VDF-TrFE) films are shown in Figure 6.17 for perpendicular and parallel current – stress configurations. It can be seen that the current hysteresis tallies with the polarization properties (Figure 6.11(a)). Due to smaller remnant polarization, current retention in 25%-stretched device is less than the others leading to narrower hysteresis loop. Furthermore, as the dielectric constant is dependent in ferroelectricity (refer to Chapter 4), less crystalline and ferroelectric phase in 25% strain sample results to lower dielectric constant hence smaller drive current. Comparing 50% and 70% strain sample the OFF to ON cycle's current resemble each other. Yet the

70% sample has slightly lower current retention during ON to OFF cycle. This also agrees with the above FTIR trend in which the extend of crystalline phase in 70% strain sample is smaller than that of the 50% one due to hardening and relaxing of polymer chains in the regions of necking which hinders the reorganization and lead to short-range order phase.

Figure 6.17 – Transistor performance of devices fabricated on substrates stretched to various % elongations at 70°C.

6.4 Conclusion

Uniaxial stretching method has been applied to **P(VDF-TrFE)** thin film attached to a flexible PET substrate to improve surface morphology and polarization properties of ferroelectric polymer. By combining stretching to plastic deformation and annealing above the Curie temperature, the surface roughness can be drastically reduced. As annealing temperature is decreased below the Curie point, crystallization and phase transformation to ferroelectric phase are greatly influenced by effect of the applied strain. Stretching of sample to higher elongation till necking occurs (70%), however, results in hardening of polymer chains and leads to formation of short-range order regions only. The hindrance of molecular chain movement by hardening effects also results in non-uniform topography that greatly increases the surface roughness. The reduction of roughness greatly enhances the growth of pentacene layer on top of stretched film for the **FeFET** device. Charge carrier mobility is hence improved than the annealed copolymer

film device and memory functionality is obtained by current hysteresis with comparable characteristics.

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Chapter 7

SOLUTION PROCESSED ORGANIC FERROELECTRIC FIELD EFFECT TRANSISTOR–APPLICATION OF NON-VOLATILE MEMORY DEVICE ON FLEXIBLE SUBSTRATE

7.1 Introduction

Since the discovery of organic semiconducting materials it has been of great interests in both scientific understandings of new materials and practical aspects of real-life device applications. From their chemical structures, there are usually two types e.g. small molecules and polymeric molecules. While small molecular semiconductors offers comparable charge transport properties to amorphous silicon due to their good crystallinity and well defined structure, the polymeric counterpart is often deemed as potential low-cost alternatives to the mainstream amorphous silicon technology. These materials can be tailored so that they can be processed in solution-form which will allow devices to be fabricated in large volumes, areas and by cheaper methods such as spin-coating, ink-jet printing or screen printing. One of the shortcomings is, however, the stability of the materials in ambient conditions during normal or testing periods. Recently, a new semiconducting polymer, regioregular Poly (3,3'-diakyl quaterthiophene) - PQT (shown below), has been introduced as one that exhibits excellent solution processability as well as ability to self-organize through intermolecular side-chain interactions. Due to its substitution of long alkyl chains the π - π interactions along the main chains are stabilized gives the molecules good sustainability in normal ambient conditions [1,2,3].

Owing to its solution-process, transistor devices can be simply fabricated with different structures. Moreover, due to the flexibility of polymeric materials the devices can be subjected to more realistic testing conditions. This hence leads to realization of so-called

mechanically flexible devices that can be bent, rolled, folded or mildly deformed which are more suitable to everyday applications.

In this chapter, different ways of device fabrication using solution-processing PQT semiconductor will be explored. Flexible organic FeFET device will be demonstrated on plastic substrate for which behaviors of working devices will be characterized under deformed conditions.

7.2 Experimental

All of the used substrates e.g. ITO glass, Aluminum-coated plastic, and glass slides with patterned gold electrodes were cleaned by acetone, methanol and deionized water in ultrasonic bath. The patterned gate substrates were fabricated by thermal evaporation of gold through shadow mask resulting in electrode area similar to the channel area defined by the source-drain shadow mask. P(VDF-TrFE) films of 1-2 μm thickness were formed by spin-coating from filtered solution of 50-100 mg/cc concentration. The polymer films were then annealed in Nitrogen ambient at 140°C for 2 hours to enhance crystallinity. Semiconductor PQT solution was agitated in ultrasonic bath and filtered through 1 μm pore size before being spin-coated onto P(VDF-TrFE) surface at 1000 rpm for two minutes. This resulted in a 40 nm-thick semiconducting film. The samples were annealed again in vacuum (~ 1 mbar) at 140°C for 30 minutes to let PQT nanoparticles crystallize [3]. Source-drain electrodes were formed by gold evaporation through shadow masks. For device with patterned gate electrodes, the edges of source-drain electrodes were aligned to match to those of the gate to prevent overlapping regions as described in Chapter 5. The transistor devices were characterized in normal ambient (23°C, 60-70% relative humidity) using Keithley 4200 Semiconductor analyzer. The bending tests of flexible samples were done by tightly pasting the samples onto the curved surface of a test tube with determined diameter.

7.3 Results and Discussion

7.3.1 Solution-processed ferroelectric FET using PQT

Electrical characteristics and device structure of an organic FeFET device fabricated from solution process using PQT as semiconductor are shown in Figure 7.1. The usage of such thick P(VDF-TrFE) film (~ 2 pm) is to prevent the gate leakage which is caused by possible penetration of PQT solution though the semi-crystalline structure of the ferroelectric copolymer. The transfer characteristic exhibits clockwise-direction hysteresis of drain current similar to devices with pentacene in Chapter 5. Moreover, the device here is also observed with a drastic shift of turn-on voltage V_{TO} as described in 5.3.2. Using the described method [4], the charge densities caused by the traps and fixed interfacial dipoles are calculated to be 0.63 and 0.53 $\mu\text{C}/\text{cm}^2$. As compared to the pentacene devices, the V_{TO} shift is more dominated by the fixed interfacial dipoles, it can be seen here that the traps contribute more charges to the final shift. This is probably the characteristic of solution process that requires special attention for improvement. Although all the used solutions had been filtered through suitable pore size and the solvent dichlorobenzene of PQT solution had been tested and confirmed not to dissolve the P(VDF-TrFE) copolymer, traces of liquid solvent might have been still remained in the interface between the dielectric and semiconductor film after spin-coating which could not be totally removed during annealing process. Besides, during spin-coating P(VDF-TrFE) polymer chain at the top might have also swollen when in the contact with dichlorobenzene and lost some of crystallinity after the process finished. This created more disordered regions in the ferroelectric copolymer layer and the subsequent PQT film grew on top. It has been shown that disorders in both dielectric and semiconductor are the most possible sources of electronic traps that degrade the device behavior. From the saturation drain current in I_D - V_D curve, charge carrier mobility across the semiconductor channel is calculated by

$$I_{D,sat} = \frac{W}{2L} C_{FE} \mu_{FE} (V_G - V_T)^2$$

The value obtained is 0.065 cm^2/Vs (refer to Table 7.1) which is comparable to similar device structure but using self-assembled HMDS-modified SiO_2 dielectric [2]. The good

mobility value obtained here is attributed to the high dielectric constant ($\epsilon = 13$) of P(VDF-TrFE) and the significant immiscibility between the formed film and the subsequent one.

Figure 7.1 – Electrical characteristics of solution-processed FeFET device using PQT and 2 μm thick ferroelectric copolymer film with device structure shown on top.

To investigate the effects of PQT solution in contact with the P(VDF-TrFE) surface, a thin (50 nm thick) Poly(methyl methacrylate) (PMMA) is used as a capping layer for the dielectric film. It has been well known of using such thin capping layers of lower dielectric constant (~ 2.2 for PMMA) to improve the performance of the organic field effect transistors [5,6]. Figure 7.2 shows a series of AFM pictures of P(VDF-TrFE) films alone with PQT layer on top as compared to sample with PMMA capping layer and its form PQT film. It can be seen that with the ferroelectric copolymer alone, the surface is rough with the semicrystalline structure of rod-like grain as characterized in Chapter 3. Deposition of 40 nm thick PQT film on top is seen to result in slightly smoother surface as indicated by the surface roughness values in Table 7.1. It is also interesting to see that in spite of resembling the same surface feature of P(VDF-TrFE) the PQT layer can still well function as a semiconductor in comparison with 45 nm thick Pentacene that is grown onto similar P(VDF-TrFE) surface and does not lead to any FET device behavior. This is possibly due to the microcrystalline size of PQT is much limited and smaller than that of

Pentacene. PQT microcrystals have been found to grow into lamellae of 10-15 nm size in optimized condition [3]. As a result, the tiny grains are more likely to form on all over the dielectric surface and come in contact with each other to create conduction paths for charge carriers.

Figure 7.2 – Surface morphology of P(VDF-TrFE) film with or without PMMA capping layer and the corresponded PQT film on top (a) P(VDF-TrFE) film and (b) PQT on top, (c) P(VDF-TrFE) film with PMMA and (d) PQT on top.

As discussed above, due to the contact of P(VDF-TrFE) film with the PQT solution, more disordered regions are likely to form at the semiconductor-ferroelectric interface. It has also been shown that there is strong charge scattering effect occurring in the channel regions when high-k dielectric materials are used [5,7]. As a result a capping layer separating the dielectric and semiconductor is favored to prevent these effects. When the 50 nm thick PMMA capping layer is used, surface energy of the dielectric film is seen to increase as indicated by reduction in the contact angle before annealing. After annealing to enhance the P(VDF-TrFE) crystallinity, the surface energy approaches similar value of

the ferroelectric film alone but the surface roughness is reduced. These factors lead to much smoother surface of the spin-coated PQT film. The increment of surface energy by PMMA capping layer (before annealing) due to the presence of oxygen bonding indicates a full coverage of P(VDF-TrFE) surface, yet its reduction after annealing suggests a strong dependence of surface energy in roughness rather than chemical composition. Moreover, AFM morphology shows rather different surface topography which consists of smaller and denser grains leading to a small reduction in roughness (Figure 7.2 & Table 7.1). Figure 7.3 examines the electrical performance of transistor with the PMMA-capping layer. It can be seen , however, that the device behavior exactly follows the one without the capping film with slightly reduced ON/OFF ratio as well as carrier mobility (Table 7.2). The reduction of ON/OFF ratio is caused by the blocking of compensating charges between the ferroelectric and semiconductor leading to smaller polarization as described in Chapter 4. The drop in mobility likely links to the reduction of overall accumulating capacitance as PMMA ($\epsilon = 2.2$) has much small dielectric constant compared to P(VDF-TrFE).

Figure 7.3 – Electrical characteristics of device with PMMA capping layer on top of the P(VDF-TrFE) film.

Table 7.1 – Topographical properties of P(VDF-TrFE) films with capping PMMA layer

Dielectric	Contact angle (°)		Surface roughness (nm)	
	Bef. annealing	Aft. annealing	Dielectric	Semiconductor on top
P(VDF-TrFE)	78.3	78.4	18.7	17.4
P(VDF-TrFE) with PMMA	63.6	77.5	15.8	11.7

To remove the overlapping areas between gate and source/drain electrodes and enhance device performance, a patterned gate electrode structure is used as shown in Figure 7.4. As discussed in Chapter 5, the overlapping regions lead to the double polarization switching and their removal also helps to minimize the effects of V_{to} shifts which results in larger ON/OFF ratio at zero gate voltage. In terms of device integration, usage of patterned gate is also more practical especially in reducing dielectric breakdown. The electrical characteristic of such device are shown in Figure 7.4. It can be seen that thinner ($\sim 1\ \mu\text{m}$) P(VDF-TrFE) film can be used as penetration of PQT solution is less severe through smaller effective gate area that allows operating voltage to greatly decrease. The device electrical performance can be further improved by using a thin layer ($\sim 40\ \text{nm}$) of poly(methyl silsesquioxane), PMSSQ, to promote the growth of PQT layer [2]. Data shown in Figure 7.5 of this device indicates much more desirable transistor behavior including higher drive current, more stable drain current in saturation regime, near-zero turn-on voltage, and higher mobility of charge carrier (Table 7.2). The obtained mobility value and turn-on behavior are as comparable to reported devices fabricated on thermal oxide with modified self-assembled molecules [2].

In all previous devices the memory ON/OFF ratio is strongly dependent in the deposition of semiconductor materials on top of P(VDF-TrFE) film with the factors limiting the memory functionality including gate leakage, position of turn-on voltage and OFF state current. It is hence suggested that if the P(VDF-TrFE) is formed independently from the semiconductor layer these limited factors can be overcome. Figure 7.6 presents top patterned gate device structures in which the P(VDF-TrFE) film is formed on top of the PQT layer which also helps to protect the semiconductor from degradation. The transfer characteristics show great improvement in terms of memory ratio which is resulted from

low OFF-state current and negative-shifted turn-on voltage. Data summarized in Table 7.2 indicates the highest memory performance with acceptable carrier mobility obtained from this device structure.

Figure 7.4 – Electrical-characteristics of bottom patterned gate with top source-drain electrodes. Device structures (side view – left and top view – right) are shown together.

While leakage current and ON/OFF ratio have been always examined (as shown in the insets of transfer characteristic graphs) for all the devices, stable write/read/erase operations have not been satisfactorily observed. In general, it was found that the gate leakage current mainly depended on the quality of spin-coated P(VDF-TrFE) films regardless of gate types (common vs. patterned) and the capping layers, PMMA or PMSSQ. In terms of stable operation, one of the factors believed to exacerbate the degradation of PQT was the low-quality interface between P(VDF-TrFE) and PQT even with capping layers and other was possibly the high humidity (>70%) of the laboratory environment. It was also observed that during the write/erase test (in ambient) the bottom-gate devices were degraded faster and mainly due to the organic semiconductor as the saturated drain current value kept dropping after every pulse applied. Based on these observations, it was decided that the comparison of the pulse test for writing/erasing would not accurately indicate the true device performance in ambient yet the stability of retention would be more suitable for performance comparison. It had been found that

bottom-patterned gate devices had overall higher current retention ($I_{ON}/I_{OFF} > 80\%$) upon removal of gate bias as compared to -60% of common gate devices. This difference was believed due to the lowered parasitic RC components in the patterned device which resulted in less current loss. In terms of maintaining stability of current retention, top-patterned gate devices with reversed ferroelectric insulator – organic semiconductor stack possessed better retention over time as compared to bottom-patterned ones. A drop of 20% of current level from the initial value (upon gate-bias removal) was recorded at 10^4 s for the top gate while the reduction of a bottom-patterned device was about 30-40%. This hence emphasizes the protecting role of the P(VDF-TrFE) film to the semiconductor layer in the reversed stack which helped to improve the stable memory retention behavior. Therefore, based on the available data it is believed that top gate device should be the best structure for operation in normal ambient conditions.

Figure 7.5 – Electrical characteristics of bottom patterned gate device with pMSSQ capping layer on top of P(VDF-TrFE) layer.

Figure 7.6 – Electrical characteristics of top patterned gate with bottom source drain electrodes.

Table 7.2 – Summary of mobility and ON/OFF ratio of different device types

Type of electrode	Mobility (cm ² /Vs)	ON/OFF ratio
ITO	0.065	10 ³
ITO with PMMA	0.05	5x10 ²
Bottom patterned Au	0.035	1.5x10 ³
Bottom patterned Au with PMSSQ	0.08	<10 ²
Top patterned Au	0.009	6.1x10 ³

7.3.2 *Solution-process ferroelectric FET on plastic substrate for flexible application*

The possibility of using simple solution process with polymeric semiconductor for organic FeFET presents a great opportunity for fabrication of low-cost devices which can be used in flexible applications. This is further supported by the independence of polarization properties of P(VDF-TrFE) against the mechanically deformed conditions. Figure 7.7 shows polarization hysteresis obtained from measurement of tensile bending test as demonstrated by the inset. For substrate (thickness ~10 μm) that is slightly “harder” Polyethylene naphthalate (PEN, tensile modulus ~200 MPa), polarization

properties are nearly unchanged as the applied tensile strains vary from 0.022 to 1.1%. This is possibly caused by the energy absorption is much more in the substrate as compared to the ferroelectric film hence the polarization switching is unaffected by the strain application. On the other the hand for Polyethylene terephthalate (PET, tensile modulus –80 MPa) substrate, there is reduction of remnant polarization with increased values of strain. It is possible that energy absorption during bending has stronger effect in the ferroelectric copolymer film which restricts the dipoles in certain regions to reorient with the field hence reduces net dipolar polarization.

Figure 7.7 – Polarization property behaviors under mechanical bending test (a) sample on Al-PEN and (b) sample on Al-PET substrate

Figure 7.8 presents the electrical data of FeFET devices fabricated on Al-PET substrate and obtained from measurement in normal ambient. It can be seen that the device behavior is not affected by oxygen doping in the semiconductor which results in stable operation [8,9]. Various testing conditions with the sample differently bent are shown in Figure 7.9 and 7.10. It can be seen that below 0.8% tensile strain the samples performs independently of the applied strains. The drain current is also found to be unchanged by

the relative direction of channel dimensions against the applied strain direction. This is possibly resulted from the random distribution of PQT microcrystals. The critical strain where the device lose its field effect transistor behavior was determined around 0.8% as indicated by Figure 7.10(a). Nevertheless it is suggested that this behavior is caused by the strained effects to the PQT layer rather than the ferroelectric copolymer as it has been shown that polarization can be obtained up to 1.1% strain. Furthermore, with much higher applied drain and gate voltages, certain hysteresis behavior can still be obtained from the device transfer characteristic.

Figure 7.8 – Electrical characteristics of FeFET device fabricated on PET substrate.

Figure 7.9 – Device performance under tensile strain test conditions at (a) various strains (with drain current parallel to strain) and (b) at strain of 0.4% with drain current path parallel and perpendicular to strain direction.

Figure 7.10 – Device behavior at tensile strain of 0.73%.

7.4 Conclusion

Organic FeFET devices have been fabricated by simple solution-process using polymeric semiconductor. Owing to process versatility, different device structures can be formed with controlled operation behaviors. It can be shown that by forming the ferroelectric copolymer layer independent of the semiconducting layer desirable current hysteresis can be obtained as well as device stability. Devices on flexible substrate which operate in mechanically deformed conditions have also been demonstrated. Up to critical strain of 0.8% the devices work independently of tensile strain amplitudes and the relative current path and strain direction. The non-volatility of memory functions is predicted to be unaffected up to strain of 1.1%. These findings hence enable the realization of ferroelectric non-volatile memory in practical and low-cost applications.

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Chapter 8

STUDY OF P(VDF-TrFE) NANOSTRUCTURES AND ULTRATHIN FILMS FORMED BY LANGMUIR-SCHAEFER TRANSFERRED METHOD AND THEIR APPLICATIONS IN NON-VOLATILE MEMORY

8.1 Introduction

Through the capabilities of chemical synthesis almost without limitations and better understandings of surface properties, it has recently been much of interest to fabricate high quality films of organic materials at extremely small thickness. These ultrathin (<100 Å) films are of high expectation to be useful in the newly developed organic electronics for applications ranging from sensors, detectors to circuit component of memory, display devices [1,2]. Besides traditional methods using thermal or molecular beam evaporation, electro-deposition etc. the attention has been turned to solution process because of its simplicity and low cost. One of the most popular methods is the self-assembly of organic molecules onto surfaces by either chemical or physical adsorption [3]. This method allows precise deposition of materials at required locations and thickness control. However the structural order of the film requires the corresponding order from the substrate surface that limits its usage. Another method which has been proved to be versatile and become well-understood is the transfer of Langmuir-Blodgett (LB) film [1,4,5]. It has the advantages of using low-concentration solution and independence of substrate surface. The LB film is formed by compressing the dissolved molecules into the required layer and transferring it onto a designated surface. Figure 8.1 (a) and (b) display various states of the molecule floating on top of the subphase and being compressed by the moving barriers. The ordered molecular layer is then simply transferred onto a substrate vertically (LB) or horizontally (Langmuir-Schaefer, LS).

Forming and transferring the LS films of P(VDF-TrFE) copolymer have been intensively performed by Ducharme et al [7]. Using a single monolayer film on a highly ordered pyrolytic graphite (HOPG) substrate, different properties and characteristic of P(VDF-TrFE) have been observed at polymer chain level including intrinsic switching

polarization, optical and energy band etc. [7]. They have also demonstrated the application of LS-transferred P(VDF-TrFE) for non-volatile memory using hybrid device with Si-technology [8]. As one of the unique features of the ultrathin polymer film that is strongly under influence of surface tension and interaction with substrate, it has been showed that the LB-transfer copolymer can be transformed into nanostructures of mesas or wells [9]. These new findings are proven to be practically useful improvements for memory application in terms of device density and performance. However the demonstration of non-volatile memory behavior has been so far limited, hence limiting the real applicability of the ultrathin P(VDF-TrFE).

Figure 8.1 – Formation of monolayer on substrate surface from the subphase-air interface by vertical transferring (adopted from [6]).

In this chapter, the usage of LS-transferred P(VDF-TrFE) layers will be examined for the formation of different nanostructures under the effect of temperatures and surface conditions. The good quality ultrathin films prepared from the same method will be investigated for the demonstration of non-volatile memory based on the organic electronic technology. The device operation mechanism will be identified and the performance will be examined for further improvements.

8.2 Experimental

P(VDF-TrFE) (70-30 mol%) copolymer pellets were dissolved in MEK at concentration of 0.1 mg/cc. The solution was then filtered by using 0.2 μm pore-size Teflon filter and promptly used for deposition to maintain a consistent concentration. N-doped Silicon wafer was used as transfer substrates. Wafer substrates of 2x2 cm^2 dimensions were cleaned with Piranha solution ($1\text{H}_2\text{O}_2 : 2\text{H}_2\text{SO}_4$), SC2 solution ($1\text{NH}_4\text{OH} : 1\text{HCl} : 10\text{H}_2\text{O}$), followed by Acetone, Methanol and DI water and blow-dried by N_2 gas. This is then followed by surface treatment using O_2 plasma and/or trichloro octyl silane (OTS) self assembling as summarized in Table 8.1.

Table 8.1 – Surface treatment scheme of wafer substrates prior to L-S transfer

Type of treatment	Processing conditions
Reference samples - A	Substrate cleaning without further treatment.
O_2 -plasma treated - B	Substrate cleaning followed by 2-minute O_2 -plasma.
OTS-treated - C	Substrate cleaning followed by self assembling of OTS-8 at 60°C . The 0.1 M OTS-8 solution was prepared by mixing 1 g OTS-8 molecules to 40ml toluene. Substrates were submerged in the solution for 15 minutes at 60°C and rinsed with toluene followed by N_2 blow-drying.
O_2 -plasma treated followed by OTS - D	Substrates treated using O_2 -plasma as in B and followed by OTS treatment as in C.

LS-transfer was done using Langmuir KSV5000 trough as schematically shown in Figure 8.2. Ultra-purified water with resistivity of $18.2 \text{ M}\Omega\cdot\text{cm}$ was used as subphase medium. The copolymer solution was manually spread onto the subphase surface between the two automatically moving barriers with surface pressure measured by the Wilhelmy plate. The monolayers were manually transferred onto a substrate in horizontal manner at 25°C and surface pressure of 5 mN/m . Thickness of 1.8 nm has been reported for each of the transferred monolayer at this pressure [10].

Figure 8.2 – LS trough for compressing monolayer at subphase surface (adopted from [6]).

From DSC data of spin-coated P(VDF-TrFE) thin film (Figure 3.1), the copolymer exhibits the ferroelectric-paraelectric (F-P) transition at 80-120°C and melting region at 145-170°C in the heating direction, while P-F transition is at 50-75°C and recrystallization region at 120-142°C in the cooling direction. Based on these observations, the transferred films were annealed at three different temperatures of 100, 120 and 140°C in ambient condition using slow-ramping oven (rate of 1°C/min). Film crystallinity was determined by Rigaku CuK α X-ray diffractometer (XRD) (40KV, 30mA) with an incident angle of 0.5° and step of 0.02. The surface morphology was characterized using Atomic Force Microscopy (AFM).

Polarization switching was examined using Piezoforce microscopy (PFM) with Si conductive tip. The closed circuit of the PFM equipment was made through the contact from the conductive tip to the LS-film surface and the back of the Si-wafer substrate using Silver paste to reduce contact resistance. The scanning parameters are shown in Figure 8.7. The metal-ferroelectric-semiconductor (MFS) capacitor devices were fabricated by thermal evaporation of gold (99.9% purity) through a shadow mask onto annealed samples. The electrodes in circular shape have diameter of 300 μm . The leakage current was measured by Keithley 4200 analyzer and capacitance data was obtained by using HP4284 LCR meter. The AC signal was of 50 mV amplitude and 1 MHz frequency. The ferroelectric field effect (Fe-FET) was fabricated using Si-wafer with 5 nm thermal oxide as substrate. The transistor was formed by evaporation of pentacene on top of the transferred samples in vacuum (5×10^{-7} torr) at 1-2 $\text{\AA}/\text{s}$ rate. It was then followed by evaporation of gold electrodes for source and drain through shadow mask.

8.3 Results and Discussions

8.3.1 Formation of nanostructures by different annealing temperatures

Figure 8.3 shows AFM images of the LS films of 1-5 ML after annealed at 120°C. The nano-islands could only be formed in 1 ML film with feature thickness of 12 ± 2 nm and diameter of 120 ± 20 nm. Up to 3 ML, separated islands join together to form a percolating network with similar thickness. The 5 ML film shows a complementary structure of the islands with nano-wells of similar sizes. Figure 8.3 also shows the diffraction data of the annealed films indicating high crystallinity of the nanostructures was obtained with increased number of monolayers.

Figure 8.3 – AFM images of nano-islands (1-ML film), nanomesas (2-4-ML film) and nano-wells (5-ML film) obtained from LS transferred film after annealed at 120°C with crystalline diffracting data of the transferred films after annealed.

As the films were annealed at 120°C, the polymer chains only underwent phase transformation (F-P) and mainly remained in the solid state as shown by the DSC data (Figure 3.1). Therefore it has been suggested that plastic flow of copolymer chains in the

crystalline paraelectric phase is the main forming mechanism of the nanostructures [9]. However, surface morphologies and annealing temperatures appear to play an important role in controlling feature types and sizes. This can be observed from the spontaneous formation of the nanostructures and the weak thickness-dependence on numbers of monolayers. Further calculations also showed that the driving force for the feature evolution involves elastic energy, interface energy, and internal energy density per unit surface area [11].

Figure 8.4 – LS-transferred films after **annealed** at 140°C with XRD data after annealed.

AFM images and XRD data of the LS-transferred films after annealed at 140°C are shown in Figure 4. Nano-islands were formed in 1-ML film with a thickness of 14 ± 2 nm and diameter of 2-3 times larger as compared to the 120°C-annealed samples. The oblong-structures were also observed in the 2, 3 and 4 ML film with larger sizes. However nano-wells were not obtained in the 5 or 6 ML film. We believe the larger feature sizes in 1 to 4 ML films were resulted from pattern-coarsening due to higher interface energy. Because of higher annealing temperature (near to the melting point),

mobility of copolymer chains was drastically increased leading to rising interfacial energy and reducing elasticity.

The absence of nano-wells in the 6 ML film can be explained from the onset of lamellar grain formation. From the XRD data of the two annealing temperatures, the evolution of crystallinity is different for films with increased monolayers. In the case of 120°C, the 4 and 6 ML film have similar crystalline structure possibly resulted from the connecting oblong-structure. The 6 ML film's crystallinity is much higher than the 4-ML as annealed at 140°C, which probably indicates the difference in crystallization process. It should be noted that annealing at 140°C is a common method to enhance the crystallinity in spin-coated P(VDF-TrFE) films in which fully developed rod-like grain structure with lamellas of folding polymer chains is observed [12]. This is further supported by the higher crystallinity of 8 ML film after 140°C annealed (Figure 8.4).

Figure 8.5 – LS-transferred films after annealed at 100°C with XRD data after annealed.

For films annealed at 100°C (Figure 8.5), where both of ferro- and paraelectric phase coexist, no separated islands or oblong-structures were observed but only closely packed

areas. In this case, it is expected that the thermal energy was mainly consumed for the phase transition rather than in the pattern separation. Therefore, the interplay between pattern coarsening and refining did not take place to form the nanostructures. It was also observed that 100°C annealing could still result in crystallization in the LS films. The evolution of crystallization has similarities as the case of 120°C annealing in which the crystallinity is identical at the onset of nano-well formation (4 and 6 ML film).

8.3.2 Effects of surface treatment on the nanostructure formation

Figure 8.6 – AFM images of IML films deposited at the same conditions after annealed at 120°C on (a) reference (A), (b) plasma-cleaned (B), (c) OTS-treated (C), and (d) plasma-cleaned and OTS-treated (D) Si wafer.

Figure 8.6 shows AFM images of 1 ML films on surfaces with different treatments (Table 8.1). The contact angle data are presented in Table 8.2. The plasma-cleaned substrate (B) is more hydrophilic as compared to the reference (A) while the OTS-treated

ones (C & D) are more hydrophobic. Substrate (D) is slightly more hydrophobic than (C) as the OTS molecules were better self-assembled on the plasma-cleaned substrate due to higher number of non-terminated Si bonds available. It was observed that more continuous film was transferred onto the hydrophilic surface of substrate-B. It is likely due to the surface roughening by plasma that increased the wetting as the monolayer was transferred. In the case of OTS-treatment, patchy films were obtained after transferring.

Table 8.2 – Tabulated surface contact angle values for the various treated substrates

Ref – Si (A)	Plasma cleaned (B)	OTS-treated (C)	Plasma-cleaned and OTS-treated (D)
25.27°	7.72°	99.6°	111°

It can be seen that surface conditions drastically affected the nanostmcture formation (Figure 8.6) illustrated using 1 ML films. As compared to the nano-islands formed on substrate-A, well-developed nanomesas were seen on substrate-B. As explained above, due to the hydrophilicity and surface roughness at the interface between substrate and the transferred film, there is a strong driving force by the interface energy that resulted in pattern coarsening to minimize the interfacial area. As a consequence, percolating nanomesa was formed even in 1 ML film.

In contrary, substrate-C & -D were observed with scattered nanomesas of larger widths. Tiny polymer wires were also found bridging between nanomesas on sample-C & -D. After OTS-treatment, substrate surface was smoothened and became more hydrophobic due to the alkaline end-group of OTS molecules. This led to bad wetting of the water-subphase on the surface and resulted in patchy deposition. On the other hand, this also indicates weaker adhesion between polymer molecules and OTS-surface. Consequently, elasticity dominated the nanostmcture evolution leading to pattern refining to minimize elastic energy. The appearance of tiny bridges shows the evidence of moving polymer molecular chains to form larger domains by elasticity. The increasing existence of polymer bridges in sample-C as compared to -D tallies with the higher surface tension of substrate-D which facilitates easier movement of polymer chains.

8.3.3 Polarization switching and capacitance hysteresis for application in non-volatile memory

Figure 8.7 – Piezoforce microscopy (PFM) measurement of 10-ML film on Si-wafer (a) AFM topographical image, (b) d_{33} coefficient image, (c) phase image. The dot-box and dash-box in (b) corresponding to the scanning area and voltage in the text box. The contrast differences in the two boxes of (b) and (c) correspond to various dipolar orientations.

Polarization switching of the LS-transfer film was examined in a 10-ML sample on Si-wafer after annealed at 120°C for 1 hour in air ambient by combining AFM and PFM method. The data of this experiment were obtained from a collaborated project for which the author would like to acknowledge Professors Chen Lang and Wang Junling for their important recommendations and assistance in measurements. The topographical image shows a partial formation of rod-like grain and surrounded by which is believed to be disordered regions. The scanned data for d_{33} coefficient and phase difference are shown in Figure 8.7 (b) and (c). The experiment was performed in two steps – $6 \times 6 \mu\text{m}^2$ (dotted

box) scan with +10 V that registered "down" dipoles (point towards substrate) appearing as dark contrast, and $2 \times 2 \mu\text{m}^2$ scan (dashed box) that reversed the polarization to "up" dipoles (pointing away from substrate) appearing as bright contrast in Figure 8.7 (c). The bright contrast in the dashed box of Figure 8.7 (b) indicates the strong response of dipolar vectors which could only be resulted from the orientation switching as compared to the outer areas where the polarization was not disturbed. As mentioned the presence of the disordered regions surrounding the crystalline rod-grain did not contribute to the measurement hence appearing unchanged in contrast. These evidences clearly indicate the polarization switching similar to bulk material in an 18 nm-thick film especially observed at the well-defined crystalline regions,

Non-volatile memory application was examined using MFS structure with the same dielectric layer of 10 ML. Figure 8.8(a) shows the leakage current profile which is reasonably low for device application with the inset showing the typical diode behavior indicating Schottky contact. It can be seen the current is asymmetric across the y-axis but has the minimum value at 0 V. The asymmetric shape is caused by different barrier heights at P(VDF-TrFE)/Au and P(VDF-TrFE)/Si interfaces. With potential applied at the bottom electrode to the Silicon substrate, higher current obtained by positive biases means the apparent barrier height of electron injection at the top electrode (Au) is small than that at bottom one (Si). The minimum current at 0 V indicates the absence of charge trapping near the interfacial regions hence the memory function is mainly resulted from the switching polarization of the P(VDF-TrFE) dipoles as explained by the capacitance hysteresis below.

Figure 8.8(b) presents the hysteresis capacitance data obtaining by different sweeping voltages with the first curve (-5V to +2V) as reference curve. As voltage was swept in the reversed direction (+2V to -5V, red curve), a capacitance hysteresis was obtained by the shifting of flat-band voltage of 0.7 V to the negative potential. This can be explained from the direction of dipole vectors. The positive bias (+2V) at the top metal electrode caused the dipole pointing down towards the Si substrate and led to accumulation in the Si. As the voltage was swept to negative bias (-5V), the field across the device must

overcome the dipolar coercive field to revert the dipole direction. As a result the charges were accumulated in the Si until coercive field was reached and led to depletion as displayed in the insets of Figure 8.8(b). The charge accumulation and depletion in the Si can be treated as ON and OFF state, respectively, for the non-volatile memory. An estimation of the coercive field for this device including voltage of $|1|$ V over thickness of 18 nm yields a value of $|56|$ MV/m which agrees with previously report [13].

Figure 8.8 – Electrical characteristics of MFS device with 10 ML thick P(VDF-TrFE) film (a) leakage current profile in semilog graph. The insets shows the normal IV curve and device structure. (b) capacitance-voltage curve. The two insets show the mechanism of memory retention.

Furthermore, Figure 8.8(b) also displays variability of flat-band voltage shift or memory window of the device with the application of different voltage amplitudes. When the "writing" voltage was increased to +4 V, the window memory could be extended up to 1.3 V (green curve). To bring the device back to the original state, an "erasing" voltage was applied at -6 V (blue curve). To obtain the data in the device a small "reading" voltage should be used e.g. -0.5 V without destroying the data, which will result in a capacitance hysteresis of up to 50 pF for +4 V "writing" voltage. This hence proves the versatility and applicability of thin ferroelectric polymer for low voltage non-volatile memory application.

From Figure 8.8, it can be seen that the device exhibits high current leakage during the accumulation state of the Si-wafer substrate, which caused the instability of capacitance values. Similar conductance hysteresis is also observed in both measurements by DC and

AC voltage as shown in Figure 8.9. As the shape of the conductance curve can be described by the rectifying behavior of Si-wafer in forward mode, the hysteresis is resulted from the displacement current due to polarization switching. As the coercive voltage for 10 ML thick P(VDF-TrFE) layer is estimated to be around 1 V, the sinusoidal signal (10^3 Hz, 50 mV amplitude) used in the dynamic measurement does not disturb the polarization switching. The resemblance between the two measurements indicates strong influence of charges in the Si-wafer that causes the instability of capacitance during the accumulation.

Figure 8.9 – Comparison of conductance data obtained by DC and AC voltage measurement.

In order to improve the device stability the semiconducting layer is replaced with Pentacene which is an organic p-type semiconductor with lower free charge carrier concentration ($\sim 3 \times 10^{17} \text{ cm}^{-3}$ [14]) and the n-type Si-wafer acting as an electrode. The electrical characteristics and dielectric properties versus frequency are shown in Figure 8.10 and 8.11, respectively. The capacitance hysteresis can be clearly observed with the magnitude increasing with higher voltage application (Figure 8.10 (b)). The increased leakage can still be seen yet during the depletion region of pentacene which leads to weak inversion behavior in the CV curve measured at 10^3 Hz. From the data at various frequencies, the inversion is seen to occur strongly at lower frequencies ($< 10^4$ Hz) and is accompanied by the increasing capacitance in accumulation. This increment of charges is likely due to the non-reversible polarization which can only respond at low frequencies and originates from the amorphous phase as described in Chapter 4. Considering the

unvaried small values of conductance in both of accumulation and inversion regions at low frequencies, the inverting capacitance is hence resulted from the drastic removal of holes in pentacene. It should be noted that the work function of gold is nearly matched to the HOMO of pentacene hence it is unlikely for electron injection from gold to pentacene in the formation of the inversion.

Figure 8.10 – Electrical characteristics of MFS capacitor device using Pentacene as semiconductor layer and Si-wafer as gate (a) leakage current profile with inset showing device structure and linear graph (b) capacitance-voltage hysteresis curves.

Based on the consistency of charge accumulation and the hysteresis of flat band voltage shift in the semiconducting pentacene layer, ferroelectric field effect transistor (FeFET) is examined for memory behavior. Figure 8.12 presents the electrical characteristic of a FeFET device with 20 ML P(VDF-TrFE) as the dielectric layer. From the $I_D V_D$ curve, it can be seen that the device properly operates in the field effect regime. Moreover a hysteresis is also recognized in the $I_D V_G$ curve which yields to I_{ON}/I_{OFF} ratio of 10^3 at $V_G = 0$ V and $V_D = -4$ V. One of the intriguing features is the observation of the polarization switching peak in the gate current profile. It therefore confirms the expected memory operation in the device. However due to surface roughness of the transferred film (~ 22 nm for 20 ML film), the charge mobility in the evaporated pentacene layer is drastically affected, estimated to be 0.001 - 0.004 cm^2/Vs in the saturation regime for the device shown in Figure 8.12.

Figure 8.11 – Capacitance and conductance properties of the MFS device shown in Figure 8.10 (a) Capacitance – voltage, (b) Conductance – voltage. Both graphs have similar color legend.

Figure 8.12 – Electrical characteristic of FeFET using 20 ML P(VDF-TrFE) film as dielectric layer (a) I_D - V_D , (b) I_D - V_G .

To improve device stability, a blocking layer using thin 5 nm SiO_2 was inserted between the P(VDF-TrFE) dielectric and the Si-gate, the transferred layer was reduced to 10 ML thickness. The reducing number of transferred layer was also found to lower the surface roughness (–12 nm for 10 ML layer). From the surface treatment data (Figure 8.6) transistor devices on normally and plasma cleaned wafer substrates are examined due to better coverage of the dielectric films (Figure 8.13). Charge mobility values of these two devices are calculated from saturation regime to be around $0.003 \text{ cm}^2/\text{Vs}$. This similar mobility value in spite of better surface roughness is likely caused by the reduction of the equivalent dielectric constant of the P(VDF-TrFE)- SiO_2 stack as compared to the 20 ML copolymer layer.

Figure 8.13 – Surface morphology of 10 ML – LS transferred film on (a) normally cleaned and (b) plasma cleaned Si-wafer.

Figure 8.14 – Surface morphology of evaporated pentacene layer on top of 10 ML-LS transferred P(VDF-TrFE) film on (a) normally clean and (b) plasma cleaned Si wafer.

Transfer characteristics (shown in Figure 8.15) indicate similar operation behavior in both devices consistent with the similar surface morphology of pentacene layer (Figure 8.14). Yet higher retention current at 0 V gate voltage and better OFF-state current for the normally cleaned reference device was found. As switching current peaks can be seen from the insets of both graphs at around $V_G = |5|$ V, sweeping gate voltage of $|15|$ V is hence sufficient to induce saturated polarization in the ferroelectric layer. This is consistent for the reference device as the drain current can be retained at zero gate voltage while the plasma-cleaned device exhibits a great loss in current retention. It is possibly resulted from the effects of plasma-cleaning. As the substrate was subjected to plasma, the ion bombardments partially removed the topmost oxygen from Si-bond indicated by increased **hydrophilicity**. This makes the surface susceptible to trapping of mobile charges during the transfer of a first few layers. The existence of trapped charges therefore caused the non-switching polarization (discussed in Chapter 4) which induced

higher drain current during strong accumulation but did not retain the current as gate voltage drop to 0 V. These mobile charges are also possible cause of the increasing OFF current due to inversion in the pentacene layer as having been examined earlier.

Figure 8.15 – Transfer characteristic of FeFET device on (a) normally cleaned Si-wafer (b) plasma cleaned Si-wafer.

Figure 8.16 shows the operational behavior of a FeFET device being subjected to pulsing gate voltages of different widths. Despite the transfer characteristic consistently exhibits large ON/OFF ratio at zero gate, the drain current (of the same device in Figure 8.15 (a)) shows fast decaying behavior and little retention even after 10 second pulse gate voltage. Same behavior was observed for the plasma-cleaned device. One of the likely explanations was due to the dissipation of the non-switching charge in the LS layer as the voltage was removed. Another possibility is the contribution from trapping defects in the pentacene layer. The small size grain of the pentacene layer (Figure 8.14) could lead to a large amount of trapping defects. During the pulsing accumulation, the pentacene layer was filled with holes in the region near the oxide interface and any trapped holes could be compensated from the bulk. However the hole-compensation diminished as the off cycle was reached hence the amount of free charge carriers dropped subsequently.

Figure 8.16 – Current retention measured at $V_D = -4$ V of device shown in Figure 8.15(a) after pulse gate voltage for (a) 10 sec, (b) 1 sec.

8.4 Conclusion

It has been demonstrated for the application of the Langmuir-Schaefer transfer method to fabricate various nanostructures and ultrathin films. For nanostructures e.g. islands, mesas, and wells, types and sizes are strongly affected by annealing temperatures especially in the plastic flow range e.g. below melting point. The forming mechanism is mainly dependent on the competition among the copolymer coherent strength, the substrate surface energies and the interfacial energy. Treatments of substrate surface also show important role on nanostructure formation and possibly affects the quality of ultrathin films. Change in amphiphilicity of surface is found to mainly affect the transport

of the copolymer chain during constant annealing temperature hence leads to different coverage even in 1 ML film. The non-volatile memory was examined with different devices e.g. capacitors and field effect transistors. Different states of data storing and erasing can be demonstrated with programming voltage less than 10 V. The mechanism of instability in the devices is identified and improved using organic semiconductor layer. FeFET devices are fabricated with good ON/OFF ratio in the transfer characteristic. However certain limitation is also recognized in the operating process when pulse voltage is applied to the device. This hence requires further investigation into device performance to fully recognize the capability of the material and the method. Overall the LS-transfer method offers the advantages of simple processing conditions and small volume of consumed material. The ferroelectric LS-transferred films are proven to be versatile and applicable for device application that requires low operation voltages.

8.5 Reference

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Chapter 9

CONCLUSION AND RECOMMENDATIONS

Fabrication of non-volatile memory device using ferroelectric field effect transistor structure has been demonstrated with the combination of organic ferroelectric, P(VDF-TrFE), and semiconducting materials, Pentacene and Poly(3,3''-dialkyl thiophene).

Characteristics of spin-coated P(VDF-TrFE) thin film have been fully characterized for surface morphology, crystalline structure and electrical properties. These characteristics can be enhanced by thermal annealing which results in rod-like grain topography, semi-crystallinity and good polarization hysteresis. They can also be modified by the application of corona poling methods by which better order of the topography and structure as well as higher dielectric constant and changes in surface chemistry can be obtained.

Thin film devices of metal-polymer-metal have been examined to understand the processes involved in polarization and capacitance hysteresis. Two types of polarization e.g. irreversible and reversible are determined from the hysteresis. The first one is caused by dipolar switching while the second is related to free charge carriers which exist due to trapping in the amorphous phase and compensating of dipole charges. The free charges are characterized below glass transition temperature yielding values of volume and interface density that match to those in device which ferroelectric layer in contact with the semiconductor. This leads to suggestion of Schottky contact being formed at the ferroelectric-semiconductor interface that governs that electrical behavior of the field effect transistor. A schematic band diagram is also proposed for the Schottky contact formation.

Organic ferroelectric field effect transistors have been fabricated and characterized for non-volatile memory functionality. Non-volatile memory behavior is observed and fully explained from clockwise hysteresis of drain current. Time measurement indicates the current retention by dipolar polarization can stretch over long time and switching speed is

up to 1 millisecond. Anomalous behaviors from transistor operation e.g. turn-on voltage shift and double polarization switching are also reported. The causes of voltage shift are determined to be the combination of the charge injection from semiconductor to ferroelectric as well as fixed dipoles and trapped charges at the interface. The injection mechanism is supported from findings in Chapter 4. Double polarization switching is resulted from the field distribution of potential difference between electrodes in the dielectric layer and is minimized by removing the overlapping regions of source/drain and gate electrodes.

A new method to obtain improved surface morphology and comparable polarization properties but at lower temperature is proposed for thin P(VDF-TrFE) film attached to a plastic substrate. The film sample is stretched to plastic deformation at temperature below the Curie point which results in formation of flat crystalline grain hence leads to drastic reduction in surface roughness. Combination of temperature and tensile strain ensures crystallization to take place through molecular chain reordering which gives rise to similar polarization as annealing. The improvement of surface morphology promotes the electrical characteristic of the organic FeFET built on top. Examination of non-volatile memory performance also shows enhancement in terms of memory window and ON/OFF ratios.

Organic FeFET fabricated by solution process for dielectric and semiconductor are presented. Various device structures are examined which enables the understandings of the correlation between the ferroelectric and semiconductor layers to device operation. Application of solution process using polymeric semiconductor allows fabrication of flexible devices on plastic substrates which possess high degree of mechanical versatility. Deformed devices in terms of bending are examined to showing unvaried characteristic in normal ambient conditions up to critical strain value depending on the semiconductor layer.

Langmuir-Schaefer transfer method has been explored to form different nanostructures of separated islands, mesas, and wells as well as ultrathin film. Annealing temperatures and

surface amphiphilicity are determined as two important factors that affect the dimensions and types of nanostructure through the interplaying of coherent strength surface and interface energy. Substantial polarization switching is observed for ultrathin film which enables the fabrication of memory devices operating at low voltages. Non-volatile memory behaviors have been demonstrated for both ferroelectric capacitors and transistors which show clear potential and substantial rooms for further improvements.

Overall, the obtained results and analysis are believed to fulfill the project objectives. Different insights of non-volatile memory based on ferroelectric materials have been examined for better understandings of materials properties, device fabrication and operation as well as exploration of new methods for further improvements. Nevertheless, there are still plenty rooms for improvements as suggested in the followed recommendations:

- Further property improvements of P(VDF-TrFE) film by stretching method:*** it has been shown in Chapter 6 that stretching ferroelectric copolymer film is promising to improve both polarization properties and surface morphology at lower thermal budget which are important for thin film organic devices. The limitations are, however, the strength of the supporting plastic substrate as well as the constrained substrate size for stretching to be effective. To obtain better properties of P(VDF-TrFE), the film should be stretched to higher ratio which means an independence from substrate. One of the ideas is to stretch the ferroelectric polymer film alone to the required thickness by possible pulling force in rolling process then attach the stretched film to a plastic substrate by laminating. The devised scheme hence removes the substrate-dependence and provides nearly unlimited sample size.
- ***Increasing switching time of P(VDF-TrFE) by improving the conduction of compensating charges:*** the dipolar switching time is dependent on how fast the compensating charge dissipation is in the amorphous phase and from the crystalline-amorphous interface of the ferroelectric copolymer. By enhancing the paths for the charges to be conducted away, it is likely helps to enhance the reorientation of the

dipoles. One of the possibilities is to include the conductive materials into the sample. It, however, requires the choosing of the suitable conductive materials and good control of composition as the insulation of the ferroelectric film must not be compromised to ensure the operation of the FeFET device.

- ***Application of P(VDF-TrFE) nano-islands to improve the switching time of device:*** it has been shown that the switching of dipoles goes through process of nucleation and domain growth that involves in movement of interface boundaries. By reducing the size of the domains but still maintain good crystallinity as obtained by the nano-island structure in Chapter 8, it is possible to reduce the process of grain boundary movement which can lead to decrement of switching time. Demonstration of FeFET device in the same Chapter shows the working principle but the performance is limited by the irregular surface formed by the separated nano-island. For the realization of this application, it hence requires the finding of suitable materials for capping layer which protects the nano-islands as well as design of a new FeFET device architecture in which the nano-islands should be formed on top of the semiconductor layer,