Design, modeling and characterization of on-chip transformer for silicon RFIC

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Design, Modeling And Characterization Of On-Chip Transformer For Silicon RFIC

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Abstract

On-chip inductors play a crucial role in radio frequency integrated circuits (RFICs). For gigahertz circuitry, these components are usually realized using bond-wires or planar metal traces that route in the spiral or symmetrical configuration. In recent years, demand for multiple inductors in each RFIC application has driven the development of on-chip transformers. In fact, the physical isolation property of the transformers has already facilitated the integration of many large functional blocks (impedance matching, low-noise feedback, differential-to-single-ended conversion) into the silicon wafer. Furthermore, they permit a large range of inductances to be realized. However, these transformers possess a drawback of smaller quality-factor (Q) values with various loss mechanisms and are more difficult to model.

In this dissertation, a scalable model has been developed for the proposed stacked-transformer lumped-element circuit. It is subsequently extended to a geometry-based scalable model that is suitable for performance optimization. A total number of 48 stacked transformers have been designed and fabricated for model development and verification. The scalable model is evaluated to have an error of $< 7\%$ as compared to the silicon measurement results. Five challenges have been identified based on two most-commonly used transformer designs, Interleaved and Stacked transformer designs.

To circumvent these five challenges, 2 conceptual designs are developed and patented. They are the Symmetrical (Sym) & Fully Symmetrical Transformer (FST) designs and the High Effective Turn-ratio (HETR) design. The Sym and FST designs provide solutions to low electrical coupling limitation and asymmetry nature of monolithic transformer designs. With the proposed patented interdigitization technique for the transformer windings, an identical inductors pair with higher individual coil self-resonant frequency (from $f_{SRF(Staked)} = 7.5GHz$ to $f_{SRF(Sym)} = 9.3GHz$) is achieved. On top of that, these

proposed designs can achieve $> 50\%$ reduction in the silicon estate area, based on the comparison between the states-of-the-arts transformer designs with similar performance parameters. The symmetricity and performance enhancement are further silicon verified using a differential 2-stage PA circuit and a differential LNA design. Both the proposed designs are able to produce comparable gain with significant physical area reduction.

The second patented design demonstrates the ability to achieve extremely high unit inductance value ever reported on silicon. The inductance ratio between the primary and secondary winding presented in this dissertation exceeds 30 with minimum area consumption. The proposed inductance synthesizer is able to yield $< 3\%$ of matching error over a wide range of inductance value, based on the proposed equations.

All the silicon data reported in this work are based on Chartered Semiconductor Manufacturing's 0.18 and $0.13\mu\text{m}$ RFCMOS technology node.

Chapter 1

Introduction

1.1 Motivation

The system-on-chip (SoC) radio frequency (RF) integrated circuit has recently emerged as an attractive candidate to satisfy the rapidly growing wireless and wired communication applications. Traditionally, RFICs have been mostly used in military applications and have been fabricated in expensive GaAs and silicon bipolar technologies. However, the quest for low cost solutions in the commercial market has driven a desire to implement RFICs in standard CMOS technology.

The advantages of integrating radio frequency circuits on Silicon are compelling. The fewer the external components, the smaller the size of the circuit board thus, smaller power consumption. On top of that, the use of Silicon based technologies has further reduced the cost on system integration as Silicon are abundant as compared to the III - V compound elements. (e.g. GaAs.) These advantages are especially significant in the rapidly expanding personal communication services market where low-cost, portability and long battery life are essential. Therefore, the emphasis on the reliability and the cost of the RF integrated circuits (RFICs) become the drivers in recent RF circuit designs.

Unlike digital CMOS circuits, the performance of many RF and AMS (Analog Mix Signal) circuits are mainly determined by the performance of passive elements. Voltage and temperature coefficients are key parameters for capacitors and resistors. Also,

capacitors and resistors are used in AMS circuits such as analog-to-digital and digital-to-analog converters that have clock frequencies below 0.8 GHz. Among the common RF and AMS circuit elements, transistors, diodes, capacitors and resistors are easily integrated on chip, the credits have to go to the research done that scaled the technology substantially in the past decades [1]. In fact, the sub-micron CMOS technologies now exhibit promising performance for radio frequency applications just lying in low GHz regime (such as 900 MHz of global system for mobile communication (GSM) system, 1.8 GHz of digital communication system (DCS) system and 2.4 GHz for both Bluetooth technology and WIFI (802.11b/g)) that makes them ideal for commercial applications. However, the showstopper that limits the scaling of RF design is the on-chip inductors/transformers. Of all major RF designs in the narrowband front-end system requires at least one inductor/transformer, mainly for frequency selection. These designs include low-noise amplifiers (LNAs), oscillators, filters, baluns, matching networks and mixers [2]-[8]. Thus, inductors and transformers account for a large fraction of the area (and cost) of RFICs [8]-[19].

Most people understand what are a monolithic inductor and its functions but less knowledge has been unveiled for the monolithic transformer. In recent years, on-chip transformers have become more profound in high frequency applications. This is mainly because many RFIC designers started to integrate transformer blocks with VCO, PAs etc [3]-[6]. Majority of the work done has shown enhancement in circuit performance compared to that of a non-transformer integrated design. In general, the key advantage of using a transformer is the ability to reduce the large silicon area consumption by as high as 50%. This reduction has become a figure-of-merit, as silicon area is a limiting factor in current and future RFIC designs.

A microstrip line is the simplest on-chip element for monolithic implementation of an inductor. Interwinding or overlapping of the microstrip inductors to magnetically coupled independent conductors results in a simple monolithic transformer [13].

Commonly, there are two main types of transformer structure, interleaved and stacked transformer, that are widely used in two different transformer modes (i.e. flux-linkage (FL) and transmission line transformer (TLT) mode [20] (please refer to Fig. 1.1(a) and (b))). Many RFIC designs such as VCO, LNA, and mixer prefer a fully differential architecture in order to suppress common-mode noise. In these circuits, one fully symmetrical passive component can be adopted to replace two asymmetric ones in the differential paths so as to save chip area and cost. Most importantly, by means of the miniaturized symmetric architecture, the effective inductance can be increased by inherent mutual coupling. Usually, the flux linkage transformer is limited to lower frequency applications by its inherent distributed winding capacitance. Thus, the TLT mode is introduced for higher frequency applications. In fact, the TLT mode design requires a pair of fully symmetrical coils. The ideal way of constructing the TLT, using transmission lines, is often too bulky for high inductance applications. The area needed to build a pair of high inductance transmission lines is too large. Therefore, an alternative solution comprised of monolithic transformers has been introduced to realize an on-chip TLT by trading off the bandwidth as compared to the conventional transmission line design. The detail literature review of these two kinds of transformer modes can be found in Chapter 2.5 of this dissertation.

Figure 1.1: (a) Flux linkage transformer mode (b) Transmission Line Transformer mode

Unfortunately, semi-conducting silicon substrate produces substrate loss effect and drastically degrades the performance of Si-based components at microwave frequency

range. Consequently, the past decades has seen increased research activities in the design and optimization of the inductor/transformer. These researches aim to improve the Q factor and the transmission loss of the on-chip inductor/transformer. Some successful techniques in achieving larger Q value include patterned ground shield [21],[22] and Micro-Machined IC [23]-[25]. It is also reported separately in [26] and [27] that high-Q (>100) factor can be achieved by reducing substrate, ohmic and magnetically induced losses through active circuitry.

Besides engineering on the design of the inductor/transformer, modeling is another direction that centered on the development of field solvers to predict the behavior of on-chip inductors and transformers. While accurate, these field solvers are time consuming, computationally intensive and require experience on the part of the user. These field solvers also do not provide any insight into the engineering trade-offs involved in the design of these on-chip inductors and transformers. Although the better field solvers are excellent for verification, they are inconvenient at the initial design and optimization stages.

To facilitate the design of RF circuits, significant work has been done on modeling on-chip inductors/transformers using lumped circuit models [10]-[19]. These SPICE-based lumped models are attractive as they can be easily incorporated into a standard circuit design environment (such as Cadence, ADS, etc.). Furthermore, most of the parasitic capacitance and resistances in these models have simple, physically intuitive, analytical expressions. However, these models are usually over simplified as they tend to focus on the two ports equivalent lumped circuit. This modeling technique has limited perspective (where two of its ports are terminated to ground or reference plane) and does not offer port selectivity to the designers.

A simple, accurate lumped elements model has been developed in this work that based on geometries parameters for the multi-ports on-chip stacked transformer. Subsequently,

the central idea of the geometries based expressions serves as a benchmark in the development of a scalable model for the multi-ports on-chip stacked transformer across various dimensions in 0.18 μm technology node. On top of that, we also develop ingenious designs that provide solutions to challenges in silicon-based transformer designs. The work presented in this thesis forms a basis for using lumped circuit models to facilitate the design and optimization of the inductors/transformer circuits.

1.2 Objectives

The objectives of this project are summarized as follows:

- To characterize the silicon-based stacked transformer.
- To develop simple, accurate lumped elements model for the silicon-based stacked transformer.
- To study and understand the various loss mechanisms that the existing transformer designs are facing.
- To develop a fully symmetrical transformer design that is suitable for high frequency differential applications.
- To develop an accurate geometry based model for the novel fully symmetrical transformer design.
- To demonstrate that the fully symmetrical transformer design is value added in circuit applications.
- To develop an extremely high turn ratio transformer design that occupy minimum silicon area.

1.3 Outline

Chapter 2 reviews the current state-of-the-art on the two commonly used designs of the on-chip transformers. After presenting the existing designs, it elaborates on a popular lumped circuit model for both designs and highlights the characteristics of the two on-chip transformer designs. Some well known applications for the transformer will be presented and follows by the introduction of the two common types of transformer configuration (single-ended and differential driven). Lastly, the Transmission Line Transformer will be reviewed in detail that includes its origins and the fundamental principle of the design.

Chapter 3 presents the proposed lumped equivalent circuit for stacked transformer structure. Firstly, the model used to predict the on-chip inductor studied and spin off to the full 4-port circuit model with semi-empirical derivation based on geometry parameters. The modified R_S formulas are implemented accurately to predict the series resistance of the stacked transformer.

Subsequently, a scalable model is created based on a wide range of device dimension and presented in Chapter 4. All these expressions are compared to measurement results. The new expressions show high degree of accuracy that makes them ideal for circuit design and optimization. Finally, the problems and challenges faced in the silicon-based transformer structures are investigated.

Chapter 5 proposed a novel way of inter-coil-crossing method in achieving a symmetrical transformer that provides solutions to four challenges described in Chapter 4. At first, a symmetrical design that can achieve close to 1:1 monolithic transformer is presented. It is conceptualized around the half-turn inter-coil-crossing technique. The performance of the symmetrical design are fabricated and tested based on single-ended and differential mode configuration with the existing transformer design. Subsequently, the design evolved into a fully symmetrical (True 1:1) design. It is derived by sub-segment

the half-turn into quadrant. A fully symmetrically (physically, electrically and magnetically) is achieved and the novel routing are described in detail, pictorially. Following, an accurate lumped equivalent circuit model is proposed with the geometries based expressions that demonstrate good agreement with the extracted data. Lastly, additional layout optimization technique is included, which targets to provide extra flexibility to the designers. The Power Amplifier and Low-Noise Amplifier circuits using the proposed structure are compared against the circuit using the conventional stacked transformer to demonstrate the credibility of the new design, while utilizing small silicon area.

In chapter 6, a CMOS transformer that produces high inductance ratio ($L_{Sec}/L_{Pri} > 30$) with excellent area efficiency is presented. This technique uses an electrical all-round coupling effect of a conductor A (Primary Coil), having large effective width, and a densely routed conductor B (Secondary Coil). Thus, a high turn ratio monolithic transformer, using minimum die size, is realizable on silicon. The coil having the dense routing can also be doubled up as a monolithic RF choke on silicon. In this work, area efficiency is compared between various types of existing transformer structures. Finally, the novel routing method introduces a high degree of inductance selectivity to the designers.

Chapter 7 summarizes the major contributions of this thesis and suggests areas that merit further work.

Chapter 2

Literature Review

Transformers have been in RF circuits since the early days of telegraph. The transformer is primarily designed to couple alternating current from one winding to the other without a significant loss of power, and impedance levels between the windings are transformed in the process. In addition, direct current is isolated by the transformer, allowing the windings to be biased at different potentials. Fig. 2.1 illustrates the schematic topology of a standard transformer.

A microstrip line is the simplest on-chip element for monolithic implementation of a transmission line inductor, and the strip is normally wound into a spiral to reduce on-chip area of the device. In early days, by placing two microstrip lines in close proximity, it produces performance that resembles the transformer [28]. This was followed by a circuit demonstration of a monolithic transformer in a push-pull amplifier, and later, transmitter and image-reject mixer circuits fabricated in gallium-arsenide (GaAs) IC technology by

Figure 2.1: The standard transformer schematic topology.

Podell [29] and [30]. The first analysis on monolithic transformers was published by [31], who compared simulation and experimental measurement for a monolithic spiral transformer and a transformer balun. Boulouard *et.al* proposed an alternate topology and analysis technique for monolithic microwave integrated circuit spiral transformers, which was also verified experimentally [32]. Rabjohn subsequently demonstrates the square spiral transformers on alumina and GaAs substrates, and developed circuit simulation tools based on the extraction of a lumped element model for the transformer [33]. This technique was later extended to the analysis of silicon based planar structures by John [10] and [34]. There are many past examples of monolithic transformers fabricated in silicon IC technology for use in RF circuits, such as preamplifiers [2], [8]-[35], oscillators [3]-[5], [36]-[37], mixers [38]-[40], and power amplifiers [6] and [41].

From Fig. 2.1, the magnetic flux produced by current flowing into the primary coil (Left-hand coil) induces a current in the secondary coil (Right-hand coil) that flows out of the secondary terminal that produces a positive voltage across a load connected at the terminal. The main electrical parameters of interest to a circuit designer are the transformer turns ratio ($n = N_S/N_P$) and the magnetic mutual coupling coefficient (k), which is derived from the mutual inductance (M). The expression for the current and voltage transformations between windings is shown in (Eq. 2.1).

$$n = \frac{V_S}{V_P} = \frac{i_P}{i_S} = \sqrt{\frac{L_S}{L_P}} \quad (\text{Eq. 2.1})$$

The mutual inductance (M), is mathematically related to the self inductances, L_P and L_S , by the mutual coupling coefficient (k) as shown in (Eq. 2.2).

$$k = \frac{M}{\sqrt{L_P \cdot L_S}} \quad (\text{Eq. 2.2})$$

In general, $|k|$ has value ≤ 1 as transformer is a passive device that does not generate/produce power. Typically, an ideal loss-less transformer (off-chip with ferro-magnetic

core) is able to yield $|k| = 1$. This is to say that the magnetic field from the primary coil is coupled 100% over to the secondary coil. However, the monolithic transformers will exhibit $|k|$ ranges from 0.3 - 0.9, depending on the type of transformer structure. This lossy phenomenon is attributed to the absent of the ferro-magnetic coupling medium between the two coils. In addition to reducing k , practical monolithic transformers suffer from several inherit parasitic parameters. A transformer may be configured as a three or four terminal device. Furthermore, one or more terminals may be connected to incremental ground. The self inductances, series resistances and mutual inductances are independent of the configuration of the transformer. However, some of the capacitive elements may be shorted out. This situation is attributed to that a spiral inductor being used as either a single or dual terminal device. The self-inductance of a given winding is the inductance measured at the transformer terminals with all other windings open-circuited.

The phase of the voltage induced at the secondary of the transformer depends upon the choice of the reference terminal. For an ac signal source with the output and ground applied between the primary terminals 1 and 2, there is minimal phase shift of the signal at the secondary if the load is connected to the terminal 3 (with grounded). This is the non-inverting connection. In the inverting connection, terminal 3 is grounded and terminal 4 is connected to the load so that the secondary output is anti-phased to the signal applied to the primary coil. The non-inverting and inverting transformer configurations are depicted in Figs. 2.2 and 2.3, respectively.

2.1 Ideal Transformer Model

The ideal transformer circuit models are shown in Fig. 2.4 to Fig. 2.6. Synthesis of a model directly from the circuit equations for magnetic coupling between current loops results in the direct-form model shown in Fig. 2.4 Inductance L_P and L_S model the self-inductances of the primary and secondary coils. Mutual coupling between the coils

Figure 2.2: The transformer configured in non-inverting topology.

Figure 2.3: The transformer configured in inverting topology.

Figure 2.4: The direct form circuit model of the ideal transformer.

Figure 2.5: The dual-source circuit model of the ideal transformer.

is modeled by the dependent current sources, which can weight by parameters M_{12} and M_{21} .

By applying the Thevenin's Theorem, the dependent current source on the secondary side gives the dual-source model shown in Fig. 2.5. In this equivalent circuit, the transformer turns ratio n is an explicit parameter. Current flowing through magnetizing inductance $k_m L_P$ gives rise to voltage v_P , which controls the dependent voltage source on the secondary side. The actual terminal voltage is modified by current flow through leakage inductances L_{KP} and L_{KS} placed in series with the primary and secondary windings. The model shown in Fig. 2.5 has the leakage inductance partitioned equally between windings, as the mutual inductance is shown in (Eq. 2.3).

$$M^2 = (L_P - L_{KP})(L_S - L_{KS}) \quad (\text{Eq. 2.3})$$

Figure 2.6: The T-section circuit model of the ideal transformer.

Fig. 2.6 shows the T-section circuit model of the ideal transformer. It uses three inductors to model the mutual coupling between windings. This model simplifies hand analysis of circuits incorporating transformers however it is only valid for ac signals because there must be isolation of dc current flow between the primary and secondary loops in a physical transformer.

2.2 Monolithic Transformer

In this section, the parasitic elements that contribute losses to the model will be reviewed. One potential source of significant parasitic is the material around or on which the inductor is fabricated. Monolithic transformer is built on top of the semiconductor substrate with oxide-based material as the surrounding elements also constitutes to imperfect coupling. All magnetic core materials exhibit loss of at least two types. *Hysteresis loss* arises from the inelasticity of magnetic domain walls. To support magnetic state changes, these walls must move. The energy lost per magnetic state transition is usually well modeled as constant for an excitation of fixed amplitude, so the total power dissipation owing to this mechanism is approximately proportional to frequency. Thus, the inclusion of a frequency-dependent resistance in shunt with the primary winding of the model is necessary. *Eddy current loss* affects transformers as much as it degrades monolithic inductors. Currents may be induced in any nearby conductor, including electrically conductive core materials, adjacent windings, and conductive substrates. Because

the induced voltage is proportional to frequency, eddy current losses are proportional to the square of frequency. In addition to the loss terms, there is also energy storage in the electric field surroundings and suffusing the windings. Hence, a high-frequency model must also include capacitances to account for this additional energy storage mechanism. Further complications arise when attempting to model behavior at frequencies where the dimensions of the transformer are not very small relative to the wavelength. In those cases, a simple lumped description of the transformer will be insufficient. Lastly, these materials suffer severe non-linearity at high frequency and all parameters are generally functions of temperature as well. These factors, contribute to the incompatibility of most magnetic materials with standard CMOS processes, which explains the non-existence of such materials for commercial integrated circuits. The most crucial implication of the other losses is that the various parasitic limit both the frequency response and efficiency. The magnetizing inductance shorts out the primary of the ideal transformer at DC, providing isolation, while the winding capacitances perform a similar disservice at high frequencies. This creates an avenue for the energy to loss or leak that degrades the performance drastically.

2.2.1 Monolithic Modeling

The modeling of on-chip inductors can be classified into three major groups [42]. In decreasing order of complexity, they are:

1. Field solvers
2. Segmented circuit models
3. Compact, scalable, lumped circuit models

The following subsections will examine these approaches.

2.2.1.1 Field Solvers

The most accurate approach to modeling any distributed electrical system is to solve Maxwell's equations subject to boundary conditions. There are several renowned Electromagnetic (*EM*) tools that are available in the market that compute the Maxwell's equations numerically. This tools can be generally classified into full 3D EM tools, which includes 3D input drawing (High Frequency Structural Simulator (*HFSS*) [44] and Computer Simulation Technology (*CST* [45]), and quasi-state or planar EM tools (Momentums [46], Designer [47]). Although accurate, these simulators are slow and are computationally intensive, both in memory and time. Since these simulators require both the lateral and vertical geometries (3D) to be specified, considerable experience is also required on the part of the user in setting up the simulation. Thus, full field solvers implementation is not a practical option in the industry. Custom field solvers are introduced to increase the simulation speeds by ignoring retardation effects so that magneto-static and electrostatic approximations can be used to solve the field matrices quickly (example: Analysis and Simulation of Spiral Inductors and Transformers for ICs (*ASITIC*) [48]). Even though the custom field solvers are proven to be faster than the full field solvers, it is still not widely used in the industry. The most fundamental reason for the showstopper is the changes in the standard design flow. The custom field solver requires interface between the model and the circuit simulator (such as SPICE) and the only solution is the introduction of new libraries for each process. This step is usually tedious and time consuming. Thus, implementing the custom solvers will have to trade-off its product scalability and the time-to-market. Another disadvantage is that several iterations (each involving the transfer of simulation data from the field solver to the circuit simulator) may be required to achieve the optimum design. Furthermore, this approach offers no design insight about engineering trade-offs. Thus field solvers are best suited for verification rather than design and optimization.

2.2.1.2 Segmented circuit models

A simpler approach that uses separated lumped π models for each segment of the winding. Each segment contains the conductor's self inductance, series resistance and the associated capacitances. A dependent current source is used to account for the mutual inductance between segments. The values of the resistances and capacitances are determined from parasitic components that are frequency dependents. The self and mutual inductances are commonly computed using the approach outlined by Greenhouse [43]. Although simpler than a field solver, the segmented model is very bulky and complicated. Even though that it can be integrated into a circuit simulator environment, the degree of complexity in the circuit model could easily outshine the advantage and reduces the speed of the circuit simulation significantly. Furthermore, the model complexity is directly proportional to the turn ratio of the device, which makes circuit optimization impossible.

2.2.1.3 Compact, scalable, lumped circuit models

Lastly, these models are different from segmented circuit models as it simplifies the distributive system using *equivalent* π circuit with the inductance and series resistance in the series branch and the substrate capacitances and the substrate parasitic in the shunt branches. Due to the simplicity, this model losses its accuracy at high frequencies. Nevertheless, these models exhibit sufficient accuracy up to the self-resonant frequency of the spiral, which is the frequency range of interest as it represents the region where the windings remain inductive. The speed, convenience and compactness of these lumped models make them ideal candidates for use in circuit design and optimization.

2.2.2 Layout

Unlike ideal transformer, the efficiency of the monolithic transformer is also proportional to the layout of the designs. By changing the width, length, thickness and distance be-

tween the conductors, various performance parameters can be optimized for different applications. In general, the parasitic components (resistance, inductance and capacitance) of the transformer are related to the physical length of each winding. By inter-leaving or over-layering (also known as stacking) metal traces, to maximize the length of the conductor causes the device in-built parasitic components to increase. This increment provides enhancement to the mutual inductance at the expense of increased interwinding capacitance and series resistance. The magnetic coupling coefficient k is determined by the mutual and self-inductances, which depends primarily upon the width and spacing of the metal traces and the substrate thickness [43].

Many of the techniques that have been applied to optimization of monolithic spiral inductors are also applicable to the transformer [49]-[50]. Although uniform width and spacing of the metal traces is typically used, non-uniform width and spacing usually offers some performance enhancement and flexibility [51] and [52].

From literature, monolithic transformers can be categorized into the following two main types based upon their layout patterns.

2.2.2.1 Interleaved Transformer Design

The design for the interleaved transformer can be traced back to 1981 by Shibata. The Shibata coupler is constructed from two parallel conductors that are interwound. Its primarily working mechanism is the edge coupling of the magnetic field between windings. The primary and secondary terminals lie in the same plane. One disadvantage of Shibata's design is that the total length of primary and secondary windings is not equal because the windings are asymmetric. In 1989, the interleaved transformer made its first appearance that is known as Frlan-style transformer after its inventor (Frlan) [31]. This design provides solution to the inherent asymmetry of the Shibata coupler, which ensures that the electrical characteristics of the primary and secondary are somewhat similar when they are having the same number of turns. Another advantage of

Figure 2.7: The top view of the Interleaved transformer illustrating the difference in the inner diameter.

this design is that the transformer terminals are on opposite sides of the physical layout that facilitates connections to other circuitry. Although the asymmetry of the Shibata coupler has been minimized but the physical length is still not identical as shown in Fig. 2.7. This can be explained through the difference in the inner diameter of the primary coil and the secondary coil as one of the primary coil has its inner diameter $Width + Spacing$ larger than the secondary coil, where $ID_{pri} > ID_{sec}$. This difference in the physical length shown in Fig. 2.7 might not be a major issue in low frequency applications but in *Gigahertz* frequency applications, this asymmetry property will result in degradation of circuit performance as the inductance value gets smaller.

This type of transformer design requires at least 3 metallization layers as 2 underpasses are needed to facilitate the routing (see Fig. 2.8 and Fig. 2.9).

In fact, the main conductors of the interleaved design are using the top-most metal layers in the process flow that experiences a better resistive distribution. It is illustrated in Fig. 2.10, which is the current density (J) plot of the design.

Figure 2.8: The 3D view of the Interleaved transformer.

Figure 2.9: The cross-sectional view of the Interleaved transformer that reveal the 2 underpasses requirement.

Figure 2.10: The Current Density distribution of the Interleaved Transformer design.

Fig. 2.10 shows that the current density is distributed evenly across the entire design, less the region nearer to the inner diameter of the design. The regime that found to occur current density peaking can be attributed to the current crowding effect. In general, current density will determines the conductor resistivity hence an evenly distributed conductor will result in a lower resistance. This theory can be further justified with (Eq. 2.4) as the top-most metal is also usually the thickest metal layers in the process flow (larger *thickness*).

$$R_{DC} = \frac{\rho \times Length}{Width \times thickness} \quad (\text{Eq. 2.4})$$

The impedance plot in Fig. 2.11 shows the effect of even current distribution and thick metal layers, where both coils have small parasitic series resistance. Since R_{DC} is also a function of length thus resulting in the inequality of the series resistance between the two coils ($Length_{Pri} < Length_{Sec}$).

Generally, a transformer is more often used in two-port configuration, unless the device is needed for differential applications. Also, modeling a two terminals transformer is much easier than a full four terminals transformer [53]. But this simplification makes

Figure 2.11: The input impedance (real term) of the Interleaved Transformer design.

the model less physical and un-scalable. This can be attributed to the facts that some of the electrical effects (i.e. coupling capacitance, substrate resistance, and etc) are neglected. Thus, El-Gharniti *et. al* has proposed the full multiple ports Interleaved transformer model as shown in Fig. 2.12 [15]. Similarly, Gao *et. al* has demonstrated a six terminals Interleaved transformer that has two additional center-tap terminals, based on EM simulation [18].

2.2.2.2 Stacked Transformer Design

As wafer fabrication technology advanced, multiple conductor layers can be used to build an overlay or broadside coupled transformer. This implementation was first described by Finlay for spiral inductors [54] and [55]. The Finlay-type winding, or lately known as Stacked design, utilizes both edge and broadside magnetic coupling to reduce the overall area required in the physical layout. Flux linkages between the conductor layers

Figure 2.12: The multiple ports Interleaved transformer model.

Figure 2.13: The top view of the Stacked transformer showing identical inner diameter.

are improved as the inter-metal dielectric is thinned. Generally, the dielectric separation between layers is in sub $1\text{-}\mu\text{m}$ regime that results in high coupling coefficient ($k \approx 0.9$). From the layout perspective, the Stacked transformer design shown in Fig. 2.13 is symmetric as the physical length of the two windings are identical.

Even though the windings shown in the figure are identical, they are implemented on different metal layers causing asymmetry in the electrical response of the transformer. Part of this asymmetry arises from the difference in thickness between metal layers in most VLSI interconnect schemes, which results in unequal resistances between the two coils as shown in (Eq. 2.4). (i.e. the top metal layers with thicker conductor will have lower series resistance as compared to the lower metal layers) The difference in thickness can be better explained pictorially in Fig. 2.14 and Fig. 2.15, where the primary coil is fabricated using the top layer (thick) and the secondary is built on the lower conductor layer (thin).

Also, the upper conductor is electrically shielded from the conductive substrate by the lower conductor, and hence the parasitic capacitances to the conductive substrate differ for each winding. In addition, there is a large parallel-plate component to the

Figure 2.14: The 3D view of the Stacked transformer.

Figure 2.15: The cross-sectional view of the Stacked transformer.

capacitance between windings due to the overlapping of metal layers, which limits the frequency response (f_{SRF}). However, the effects can be mitigated by increasing the distance between the two windings (*thickness*) as shown Fig. 2.15 ($h_{Pri-Sec}$). These performance impairments are balanced by a savings in chip area when the windings are stacked vertically. It is expected that the current trend in silicon technologies toward thicker and lower permittivity inter-metal dielectrics and more layers of interconnect metal will result in improved performance from stacked winding transformers in future.

Similar to the interleaved transformer, the current density distribution field plot is shown in Fig. 2.16. It shows that the primary coil (top-most layer) exhibits even distribution of current as compared to the secondary coil (bottom layer). The non-uniform current density causes the secondary coil to have large parasitic series resistance (see Fig. 2.17), which degrades the performance (i.e. Q -factor).

The model of a stacked transformer is proposed in [16] as shown in Fig. 2.18. The model represents a tradeoff between the classical lumped topologies that is obtained by applying a π -network to both the coils and distributed models [56]. Up to date, the traditional proposed model are derived using simplified π -network topology that does not fully modeled the skin and substrate effects [57] hence, it can hardly be used to model the monolithic transformer at relatively high frequencies. On the other hand, distributed networks model reflects the real physical nature of the device. But in order to model the full parasitic effects of the stacked transformer, the complexity and the needs for massive computing power make the model unrealistic for the industrial applications.

The performance and characteristic of the two transformers can be summarized in Table. 2.1.

The Stacked design is clearly the winner in term of area utilization and coupling coefficient. However, its thin secondary metal layer and the high electrical coupling between the two windings cause the Stacked to lose out in its average Q -factor and

Figure 2.16: The Current Density distribution of the Stacked Transformer design.

Figure 2.17: The impedance plot (real term) of the Stacked Transformer design.

Figure 2.18: The proposed lumped model for stacked transformer by Biondi *et. al.*

Table 2.1: Performance overview for Interleaved and Stacked Transformer

Design	Silicon Area	Q_{avg} $(\frac{Q_{Pri}+Q_{Sec}}{2})$	Unit Ind (nH/m)	k (Coupling Coeff.)	Symmetry	f_{SRF}
Interleaved	B	G	B	B	B	G
Stacked	G	B	G	G	G	B

G - Good and B - Bad

its self resonant frequency (f_{SRF}). In fact, the Ultra-wide band (UWB) and the wider band applications do not need the transformer's Q -factor to be extremely high. To be exact, these applications require the Q -factor to be small so as to achieve the flat band characteristic. More circuit implementations for the transformers will be illustrated in the following section.

2.3 Transformer applications

Basically, transformers are commonly used in the following four different areas.

- *Impedance matching*: Depending on the number of windings, the transformer has the property to change the impedance of the primary or secondary when measuring from the opposite port [58]. It is usually implemented to link one building block to the other while achieving maximum power transfer.
- *Balun*: Balanced to unbalanced conversion based on the magnetic coupling of a balanced or differential inductor and a single inductor [59],[60]. Baluns are mainly used for differential circuits [61], which withstand common noise and even harmonics. Especially, monolithic baluns are necessary for push-pull power amplifiers that are either class B or class D [62],[63]. The class B power amplifiers can achieve higher efficiency and linearity against conventional class AB power amplifiers.
- *DC isolation*: physical isolation of the primary and secondary coil [64].
- *Replacement for Inductors*: In realizing the same effective inductance, the transformer takes advantage of its mutual coupling between the two windings and thus occupies less

die area and less shunt capacitance as compared to two isolated inductors (i.e. each winding of the transformer requires shorter metal length that translates to reduction of parasitic components as smaller inductance is needed). Theoretically, reduce in the parasitic components will improves the overall device's performance significantly. As reported by Zhou *et. al.* [8], the transformer outshines the equivalent inductors by 45% in quality factor and 12% in self-resonant frequency. Another advantage of a transformer is that its ability to provide common-mode rejection in fully differential applications. This credit can be awarded to the symmetrical property of the transformer. The substrate noise coupling through parasitic oxide capacitances appears as a common-mode signal to the transformer, which leads to higher substrate noise rejection. [8] also demonstrates a fully differential LC tuned LNA @ 900 MHz.

2.4 Differential *vs* Single-ended

It is well known that a differentially driven winding produces a higher quality factor (Q) as compared to a single-ended source [13] and [25]. Fig. 2.19 shows a simplified equivalent lumped circuit model that represents the electrical behavior at any given frequency.

The value of $Z_{single-ended}$ is given in (Eq. 2.5).

$$Z_{single-ended} = \frac{Z_A \times Z_B}{Z_A + Z_B} \quad (\text{Eq. 2.5})$$

For single-ended excitation, Port 2 (right hand port of Fig. 2.19) is grounded and the equivalent circuit is connected as a one-part. The input impedance at Port 1 is expressed as $Z_{Single-ended}$, which becomes a parallel combination of the two impedances (Z_A : the winding series inductance and series resistance, Z_B : substrate parasitic capacitance and parallel resistance).

Figure 2.19: The simple lumped element model for a monolithic winding driven in single-ended mode.

As for a differential excitation, where the signal is applied across the two terminals, the input impedance $Z_{differential}$ is a parallel effect of Z_A and $2 Z_B$ as shown in Fig. 2.20.

Note that the impedance of the substrate parasitic in the differential case has doubled the value for the single-ended excitation. Therefore, at lower frequencies, the input impedance in either the shunt or the differential connections is approximately the same. However, as the frequency increases, these parasitic of the lumped elements that are driven differentially will have higher impedance at a given frequency. This can be expressed by (Eq. 2.6), the input impedance of the differentially driven lumped element circuit.

$$Z_{differential} = \frac{Z_A \times 2Z_B}{Z_A + 2Z_B} \quad (\text{Eq. 2.6})$$

This phenomenon reduces the real part and increases the reactive component of the input impedance. Therefore, the Q factor is improved in differential excitation and a wider operating bandwidth is realized for no extra cost in processing.

Figure 2.20: The simple lumped element model for a monolithic winding driven differentially.

2.5 Transmission Line Transformer

The detailed study of the conventional transformer shows that the conventional transformer has limited operating bandwidth, attributing to the winding capacitance and leakage inductance. In this section, the *Transmission Line Transformer (TLT)* will be discussed, which suffer less losses and suitable for higher frequencies applications.

The first TLT was reported in 1944 and 1959 by Guanella [65] and Ruthroff [66] in two publications, respectively. Both transformers are distinguished from their classic counterparts by having a DC low resistance path from the input to the output and for inducing zero net flux in the transformer core material. This property reduces the hysteresis losses that determine the upper frequency of operation for many practical transformers.

The basic Guanella's configuration is shown in Fig. 2.21. This kind of configuration is generally classified as *Balun* in literature. However, the design is not quite a *Balun*

Figure 2.21: The basic configuration of the Guanella 1:1 balun.

as it does not set the output common-mode voltage (AC). Whatever is connected to the output determines the common-mode voltage. In the circuit of Fig. 2.21, grounding the center-tap of the output load resistor will cause the overall circuits to behave as a *balun*.

Broadband operation is enabled by exploiting the transmission line nature of the windings making up the primary and secondary. The Guanella's design uses the transmission lines property for the windings that provides solution to the bandwidth limitation caused by the winding capacitance. If the characteristic impedance of the line equals that of the load will maximized the bandwidth. The upper frequency range is therefore extended by two mechanisms: absorption of reactive parasitic into transmission line constants and the reduction of hysteresis loss by keeping the core flux small.

The latter property is appreciated by considering when the upper (primary) coil in Fig. 2.21 is driven by an input voltage. The input current that flows in response causes a voltage to be induced in the secondary. Because of the $1:1$ turns ratio, the winding voltages are the same and so are the currents. However, the primary and secondary currents flow in opposite directions, so the net magnetic flux they induce in the core is ideally zero. As a consequence, hysteresis-based core losses are correspondingly small. In many practical realizations of the Guanella transformer, dielectric loss dominates over other core loss sources. The main selection criteria for the transformer core material are

Figure 2.22: The Guanella 1:1 balun as common-mode choke.

low hysteresis and conductive losses, but dielectric loss is particularly important in cores for TLT.

This TLT configuration is capable of rejecting common-mode signals over a wide bandwidth, where it is commonly known as common-mode choke in Fig. 2.22. It is valuable because the common-mode rejection provided by the TLT greatly relaxes the requirement of common-mode rejection (*CMR*) of the subsequent circuits. Example: common-mode chokes for the front-end vertical amplifiers of oscilloscopes between the input connectors and the front ends of the amplifiers.

Fig. 2.22 illustrates that a ground loop causes the internal and external grounds to be at different AC potentials. Assuming that the internal ground is at zero potential and a small AC signal (v_I) is the voltage at the external ground. The voltage difference between the two nodes causes the same voltage to be induced across the top winding. With the help of the common-mode choke, the induced voltage is cancelled that results in a *clean* V_{in} .

On the other hand, the Ruthroff configurations are different that exhibits much inferior bandwidth. In Fig. 2.23, the configuration has an unbalanced input and output. An applied voltage across the lower winding causes the same voltage to be induced in the upper winding. The series connection of the two windings causes the output voltage to

Figure 2.23: The Ruthroff 1:4 transformer configuration.

double, resulting in a 1:4 impedance transformation. This configuration is also known as bootstrapped connection attributed to its series-aided voltage boost.

As compared to the Guanella's configuration, the Ruthroff's configuration has lower bandwidth. This is caused by the summation of the applied voltage with one having an inherent delay along the winding. The delay produces a fundamental upper frequency limit. This delay will not result in drastic transformer performance deviation so long the delay is shorter than a period of the signal. The direct solution to mitigate this issue is to shorten the lines to improve the upper frequency limit, but the lower frequency limit is somehow compromised as the shortening causes a reduction in the common-mode inductance.

2.6 Technology Node

In this project, there is an extensively involvement in CMOS process flow that are based on Chartered Semiconductor Manufacturing's $0.18\mu\text{m}$ and $0.13\mu\text{m}$ technology node. These two nodes are chosen because they are matured and are widely used in

the industry. Furthermore, it is common that the technology node that are suitable for RF implementations are usually two generation nodes behind the leading technology node. Although these two technologies are renowned, there are substantial differences between these two nodes. In this section, the two technology nodes are illustrated and analyzed in detail. The two niche technology nodes will also be introduced to be in-lined with ITRS roadmap [1] as 65 and 45 nm nodes will be expected to be the next promising process for future RF CMOS.

2.6.1 0.18 μm Process

This process has been in the market for a decade but its still stay competitive with the other technology nodes as it is cheaper and reliable to manufacture, especially for RF CMOS applications. The process has six metallization layers as shown in Fig. 2.24

Where IMD is Inter Metal Dielectric and ILD is Inter Layer Dielectric. The metal stack parameters are tabulated in Table. 2.2. In this technology node, the metal does not has high conductivity (4.1×10^7 S/m) as the metallization layers are formed using $Al - Cu$, this is to provide good metal stack with good mechanical strength and the present of Aluminum prevents Electro-migration.

Table 2.2: 0.18 μm metal stack parameters

Layer	Silicon
M1	0.55 μm
M2	0.55 μm
M3	0.55 μm
M4	0.55 μm
M5	0.55 μm
TM	2.56 μm

2.6.2 0.13 μm Process

A few years younger in age, this technology node has been introduced to the industrial as the 0.18 μm technology node has too high metal traces resistance and high trace capaci-

Figure 2.24: The Chartered's 0.18μm process stack.

Figure 2.25: The Chartered's 0.13μm process stack.

tance caused by the high k value of the inter metal dielectric, especially in large circuit. This 0.13μm technology is completely different from the older 0.18μm node. The most fundamental different is easily distinguish in Fig. 2.25, the back-end metal stack has *eight* layers that is 2 more layers as compared to 0.18μm process.

The metal conductivity is also improved because of the pure *Cu* material used for metal 1 - 7 and a slight mixture of *Al* for the top metal. The average conductivity for the copper scheme is 5.2×10^7 S/m, which is much higher than the *Al - Cu* scheme. In this new copper scheme, the top layer that is the most commonly used is able to yield lower

resistance as expressed in (Eq. 2.4). The back-end metal stack parameters are shown in Table. 2.3.

Table 2.3: 0.13 μm metal stack parameters

Layer	Silicon
M1	0.465 μm
M2	0.465 μm
M3	0.465 μm
M4	0.465 μm
M5	0.465 μm
M6	0.465 μm
M7	0.465 μm
TM	3.030 μm

Because of the larger distance away from the substrate, the induce eddy current and parallel plate capacitance is reduced largely. This advantage also result in higher self resonant frequency and higher Q -factor. However, every pro will come with cons. In this newer process, Cu being smaller in atomic size and mass is vulnerable to Electro-migration. On top of that, a porous Inter-metal dielectric (to reduce the k value of the dielectric ≈ 3.0) induces reliability issue as the stack mechanical strength is greatly compromised and its Temperature Dependent Dielectric Breakdown (TDDB) is degraded.

2.6.3 65 nm and 45 nm Process

As the niche technologies are usually confidential to the foundry thus a generic process will be revealed in this section. Generally, the more advance technologies will have more metallization layers as shown in Fig. 2.26, a ten metal layers stack for 65nm process. This is to fulfill the requirement of ULSI and VLSI, where more transistors will be integrated into a single chip area. With more circuits incorporated, more metal lines will be needed for interconnects so the needs for more metal layers is essential. However, from the RF CMOS perspective VLSI is usually over-killed. Comparing with digital circuits, RF

CMOS do not require the circuits to be densely packed hence the foundry will offers additional packages that use less metallization for RF CMOS applications.

The metals stack parameters are shown in Table. 2.4. The average metal traces thickness for 65nm process has been reduced by $> 30\%$ as compared to $0.13\mu\text{m}$. Additional thicker top metal (M9) are included to increase the flexibility on circuit routing.

Table 2.4: 65nm metal stack parameters

Layer	Silicon
M1	$0.135\mu\text{m}$
M2	$0.175\mu\text{m}$
M3	$0.175\mu\text{m}$
M4	$0.175\mu\text{m}$
M5	$0.175\mu\text{m}$
M6	$0.175\mu\text{m}$
M7	$0.350\mu\text{m}$
M8	$0.570\mu\text{m}$
M9	$3.000\mu\text{m}$
TM	$1.323\mu\text{m}$

The generic 45nm process is so complex that none of the foundry has their process similar to the others. In this node, the metal scheme is expected to be having > 12 metallization layers. Overall, the downsizing of technology node is expected to increase the performance of RF CMOS (in terms of parallel plate capacitance and series resistance). However, the complexity of the device's process flow (especially in its lithography process) and the difficulty in mask making causes the manufacturing expenditure to increase exponentially. Thus, having the nano-scale technology node to be the mainstream manufacturing for RF CMOS is still uncertain at this point, but this will certainly be the trend in the future.

Modeling across technology nodes becomes complicated and tedious with scaling down of device feature size. Passive elements such as inductors and transformers are often used in RFCMOS circuits to provide good isolation and enhance circuit performance.

Figure 2.26: The Chartered's 65nm process stack.

Therefore, their requirements on Q-factor and inductance value become important. These requirements will usually translate into some combinations of device geometry parameters such as width, spacing, and inner and outer diameters of the passive device. Fortunately, these combinations tend not to fall near the minimum design rule requirements of the advanced node.

Luckily, the shrinking of the device's pitch size does not pose a challenge in modeling of backend passive elements as compared with active devices. But changes in the backend materials and properties could still introduce many uncertainties and unknowns to the model. For example, as the technology node is scaled down, the inter-metal capacitance has to be reduced so as to minimize the RC delay along the metal traces. In addition, pores are created in the inter-metal dielectric to reduce its relative permittivity. This porous effect does not stay constant or linear across technologies, which makes the model un-scalable across all technology nodes.

Besides the inter-metal dielectric, metal resistance also increases with the advancement of process technology. This is due to the fact that more metal layers are desired to facilitate a more complex circuit design. As a result, thinner metals are used as shown in Tables 2.2, 2.3, and 2.4.

Even though these uncertainties and unknown parameters impede the modeling process to some extent during a technology node migration, it is not a serious problem in advanced technology node modeling. In fact, many foundries have taken sufficient measures to circumvent these issues. Moreover, up-to-date material specifications are often made available for modelers' reference. However, the available specifications might not be accurate enough as most of the parameters are extracted based on simulations. In general, when migrating from one technology node to another, modelers will perform a silicon-based verification before qualifying the models.

2.7 Temperature effect

Lastly, temperature effect is an important design consideration that needs to be addressed particularly in deep sub-micrometer integrated circuits. Any changes in the device performance - due to a temperature fluctuation - might result in a circuit malfunction. However, in this thesis, the main research focus is on the creation and development of new accurate models for on-chip inductors/transformers. Nevertheless, the computation of temperature dependency elements in the model files has already been incorporated into all the SPICE or compatible simulator tools, which is governed by the temperature coefficients ($Tc1$ and $Tc2$) as shown in Eq. 2.7. For the sake of completeness, the temperature dependency of the inductors/transformers is included in the model files of the revised thesis as shown in Eq. 2.7

$$R = R_0 * (1 + Tc1(T - T_0) + Tc2(T - T_0)^2) \quad (\text{Eq. 2.7})$$

Where R_0 is the resistance at reference temperature, T_0 is the reference temperature (25 °C) and T is the temperature at which the property is measured.

As we have seen in the earlier part of this chapter, Inductors/Transformers are fundamentally *long* metal lines that introduce resistance. These built-in resistances are also visualized in the respective equivalent lumped-element models as resistors. These temperature dependent elements/parameters cause the Q-factor to decrease with increasing temperature up to a certain frequency and to increase with increasing temperature after the frequency (≈ 2 GHz). Specifically, the two primary mechanisms in controlling Q-factor over temperature are the coil metal layers and substrate resistivity. The winding metallization, which is in series with the inductance, has a positive temperature coefficient. It increases the resistance and hence decreases the Q-factor of the inductor. In addition, the power loss in the inductor increases with the temperature.

```

rs2 (6 2) resistor r=ind_rs1
ls2 (5 6) inductor l=ind_ls1
rp2 (62 2) resistor r=ind_rp1
lp2 (6 62) inductor l=ind_lp1
cox1 (1 10) capacitor c=ind_cox1
rsub1 (10 3) resistor r=ind_rsub1

```

Figure 2.27: The model sample without temperature option.

The substrate resistivity, which is in parallel with the inductance, also has a positive temperature coefficient. But it decreases the power loss in the substrate with increasing temperature. This is because the current is shunted away from the substrate and hence more current will flow into the spiral with increasing substrate resistance. As a result, the Q-factor of the inductor will increase.[67]. The variation of Q-factor with temperature below a certain frequency is said to be dominated by the temperature coefficient of resistance (TCR) of the metallization (Q-factor decreases with increasing temperature), while above this frequency, the variation of Q-factor with temperature is reversed (Q-factor increases with increasing temperature), indicating that the substrate TCR dominates at higher frequencies [68].

The implementation of the temperature dependency has become very straight-forward as majority of the SPICE tools have built-in functions to do the computation of Eq. 2.7. The temperature coefficient (Tc1) can be easily obtained from the foundry's Electrical Parameters (EP) specs. The Tc1 typically has a value ranged from 0.1×10^{-3} to 5×10^{-3} , depending largely on the material properties. As for the other coefficient (Tc2), it is meant for fine model fitting with measurement and it can be extracted through measurement. After obtaining the coefficient values, the modeler can input them into the respectively model files as shown in Fig. 2.27 and 2.28, depicting raw model sample without temperature option and a model sample with incorporated temperature option, respectively.

```
+ ind_tc1=3.8e-3 ind_tc2=1.5e-5 ind_tsub1=1e-4 ind_tsub2=2.5e-5
rs2 (6 2) resistor r=ind_rs1 tc1=ind_tc1 tc2=ind_tc2
ls2 (5 6) inductor l=ind_ls1
rp2 (62 2) resistor r=ind_rp1 tc1=ind_tc1 tc2=ind_tc2
lp2 (6 62) inductor l=ind_lp1
cox1 (1 10) capacitor c=ind_cox1
rsub1 (10 3) resistor r=ind_rsub1 tc1=ind_tsub1 tc2=ind_tsub2
```

Figure 2.28: The model sample with temperature option.

Besides the resistance, the variation in extracted inductance with temperature is observed to be very small over the entire frequency range. Beyond the self resonance frequency, the extracted inductance falls off rapidly. This nonphysical behavior also defines the limitations of the compact lumped element model for frequencies above its self-resonance.

Chapter 3

Modeling of Stacked Transformer

Existing literatures reported for the stacked transformer design is either modeled based on the EM (Electromagnetic) simulator [26],[27] or the model reported is based on simplified two ports configuration [16],[69]. Whereas the 4-port stacked transformer model using analytical equations for various RLC components has not been established. In this session, a novel analytical model for the stacked transformer that is suitable for circuit simulation and design optimization is presented. In the latter section of this chapter, a geometries based scalable lumped circuit model for the Stacked Transformer is developed. This model accounts for the scalability of the device's physical dimension (i.e. Width, Turns, Diameter, etc.).

3.1 Equivalent Circuit Model for Spiral Stacked Transformer [70]

Fig. 3.1 shows the 4-port circular-shaped spiral stacked transformer structure, which has been reported to be able to achieve extremely high-Q value [26],[27]. It consists of two identical circular spiral metallization layers overlapping each other. The structure is fabricated using a $0.18\mu\text{m}$ CMOS based 6-metallization layers process. The port orientation is laid-out such that none of the ports is directly underneath or above the other. Fig. 3.2a shows the open pad structure (i.e. without the stacked transformer in the middle)

Figure 3.1: Spiral Stacked Transformer Layout and Port Orientation.

that will be used as a reference for de-embedding measurements. The layout of both open and actual structure (see Fig. 3.2b) follows the G-S-G coplanar waveguide pad configuration. The measured data based on PLTS are then exported as touchstone files for evaluation. An EDA tool (Advance Design System, ADS) is used to compute the various complex functions. The de-embedded measurements are done using the conventional admittance subtraction techniques [71],[72]. The results are collected in the form of a 4x4 S-parameter matrix.

In a RF circuit, the on-chip stacked transformer always comes with some unwanted parasitic elements from the neighbors as shown in Fig. 3.3. Fig. 3.4 shows the equivalent circuit of the stacked transformer created from a modified 9-elements spiral inductor model. In order to model the stacked transformer accurately, a coupling capacitance, C_{center} , is inserted (between the top and bottom metallization layer) to distribute the series resistance and inductance evenly. The additional components of C_{pp1+ox} , C_{pp2+ox}

Figure 3.2: (a)Open structure, (b)Actual layout structure.

Figure 3.3: Distribution of the Series Inductance and Resistance

and C_{center} are used to describe the coupling effect between the top inductor (primary coil) and the bottom inductor (secondary coil).

Based on the metal interconnect length from Table 3.1 and the 4-port design shown in Fig. 3.1, the overlapping surface area between the top and bottom coil is approximately 80%. Therefore, the coupling component, C_{center} , is estimated to be about 80% of the total overlapping capacitance, $C_{overlap}$, as shown in (Eq. 3.1).

Figure 3.4: Model structure of the stacked Transformer

Table 3.1: Stacked Transformer Dimension

Coil	Width (μm)	Length (μm)	Thickness (μm)	Inner Dia (μm)	a (@100MHz)	b (@100MHz)	Turn
Top	6	2039	2	75	2.32	13.6	5.5
Bottom	6	1640	0.54	81	2.32	13.6	4.5

$$C_{Center} = 0.8 \times C_{overlap} \quad (\text{Eq. 3.1})$$

The total overlapping capacitance can be calculated using (Eq. 3.2).

$$C_{overlap}(F) = \frac{\varepsilon_0 \varepsilon_r \times L_{GML} \times W}{d} \quad (\text{Eq. 3.2})$$

where the ε_0 is absolute permittivity, ε_r is relative permittivity of the dielectric, L_{GML} is the geometry (physical) length of the winding, W is the winding width and d is the dielectric thickness. Using the top metallization layer as a primary coil, the overlapping capacitance value is expected to be smaller as the thick dielectric (d) offers less parasitic effect from the substrate. In addition, the bottom inductor produces an electric field that interacts with the top inductor. This complicates the extraction of the S-parameter matrix and makes the 4-port modeling inaccurate.

However, if the structure is configured in an isolation mode, the extraction and modeling can be accurately performed on the coil of interest. The isolation mode is achieved by leaving the coil (i.e. not of interest) floating or unconnected. The example illustrated in Fig. 3.5 shows that the coil of interest is the top inductor, leaving the bottom inductor floating at high impedance. In this case, the C_{pp1+ox} and C_{pp2+ox} are connected in series with C_{OX3} and C_{OX4} , resulting in C_1 and C_2 , which are expressed in (Eq. 3.3).

$$\begin{aligned} C_1 &= \frac{C_{pp1+ox} \times C_{OX3}}{C_{pp1+ox} + C_{OX3}} \\ C_2 &= \frac{C_{pp2+ox} \times C_{OX4}}{C_{pp2+ox} + C_{OX4}} \end{aligned} \quad (\text{Eq. 3.3})$$

From Fig. 3.1 and Table 3.1, it can be computed that approximately 80% of the top inductor overlaps with the bottom inductor. Hence the coupling component C_{center} is estimated to be 80% of $C_{overlap}$ as shown in (Eq. 3.1).

Figure 3.5: Model structure in Isolation mode

Using the C_{pp1+ox} and C_{pp2+ox} in (Eq. 3.3) is able to model the remaining 20% overlap capacitance (in parallel with the substrate parasitic capacitance, C_{sub1} and C_{sub2}) as shown in (Eq. 3.4).

$$\begin{aligned}
 C_{pp1+OX} &= (0.1 \times C_{overlap}) // C_{sub1} \\
 &= (0.1 \times C_{overlap}) + C_{sub1} \text{ Where } C_{sub1} = C_{sub3} \\
 C_{pp2+OX} &= (0.1 \times C_{overlap}) // C_{sub2} \\
 &= (0.1 \times C_{overlap}) + C_{sub2} \text{ Where } C_{sub2} = C_{sub4}
 \end{aligned}
 \tag{Eq. 3.4}$$

The notation of $C_{sub1}=C_{sub2}=C_{sub3}=C_{sub4}$ is used because the top and bottom inductor are integrated on the same substrate material. The substrate capacitors, $C_{substrate}$, and resistors, $R_{substrate}$ are expressed in (Eq. 3.5) [73].

$$\begin{aligned}
 C_{sub3} &= C_{sub4} = \frac{1}{2} (L_{GML} W \times C_{substrate}) \\
 R_{sub3} &= R_{sub4} = \frac{2}{(L_{GML} W \times G_{substrate})}
 \end{aligned}
 \tag{Eq. 3.5}$$

Where $C_{substrate}$ is substrate capacitance (per unit area) and $G_{substrate}$ is substrate conductance (per unit area).

The series inductance (L_S) of a stacked transformer includes both the self and mutual inductance of the circular spiral metal coil. The value is computed using (Eq. 3.6) [11].

$$\begin{aligned} L_S &= \frac{\mu N^2 d_{avg} g_1}{2} \times \left(\ln\left(\frac{g_2}{\vartheta}\right) + g_3 \vartheta + g_4 \vartheta^2 \right) \\ d_{avg} &= \frac{OD + ID}{2} \\ \vartheta &= \frac{OD - ID}{OD + ID} \end{aligned} \quad (\text{Eq. 3.6})$$

μ is the absolute permeability, N is the number of turns of the structure, d_{avg} defines the average diameter of the structure (μm), OD is the structure outer diameter (μm), ID is the structure inner diameter (μm) and g_1 to g_4 are coefficients from [11].

Note that (Eq. 3.6) is only applicable when the metal spacing is much less than the metal width [11]. The series resistance, R_S , based on DC conditions is determined by (Eq. 3.7).

$$R_S = \frac{\rho_{Al-Cu} L_{GML}}{W \times t} \quad (\text{Eq. 3.7})$$

$$R_{S1} = R_{S2} = 0.5 \times R_S$$

whereby ρ_{Al-Cu} denotes the Aluminum-Copper resistivity.

At high frequency, the depth of current (vs. the thickness of metal coil, skin-depth effect) is comparable to or even smaller than the cross-sectional dimensions of the coil. In addition, the proximity effect of the magnetic field from the nearby conductors causes the modeling using the conventional 9-elements structure inaccurate [74]. Therefore, a more robust stacked transformer model with additional frequency independent components to account for these effects [75] must be considered. As a result, a resistor (R_{f1}), is added to model the skin-depth and the proximity effect as shown in Fig. 3.6 [76]. R_{f1} is connected in parallel with the series components, L_{S1B} and R_{S1} , to model the frequency

Figure 3.6: Skin and proximity effect

dependency. The expressions to describe the series resistors and inductors as well as R_{f1} are shown in (Eq. 3.8) - (Eq. 3.10) [76].

$$\begin{aligned}\omega_{crit} &= \frac{3.1}{\mu} \times \frac{P}{W^2} \times R_{sheet} \\ R_{sheet} &= \frac{\rho_{Al-Cu}}{t} \\ m_r &= \frac{240}{N^{1.23}}\end{aligned}\tag{Eq. 3.8}$$

$$\frac{0.315 \times R_S^2}{(m_r \omega_{crit}^2 L_S^2) n_r^2} + \frac{(\varepsilon_0 \varepsilon_r L_{GML}^2)}{(6 C_{OX} L_S c^2) n_r} - 1 = 0\tag{Eq. 3.9}$$

$$\begin{aligned}k_r &= \sqrt{\frac{0.315}{m_r}} \times \left(\frac{R_S}{\omega_{crit} L_S} \right) \times n_r \\ R_{f1} = R_{f2} &= \left(1 + \frac{1}{n_r} \right) \times \frac{R_S}{2} \\ L_{S1A} &= \left(1 - \frac{3.57 k_r}{n_r^{1.5}} \right) \times \frac{L_S}{2}\end{aligned}\tag{Eq. 3.10}$$

ω_{crit} , n_r , k_r and m_r are coefficients cited from [76].

By solving the (Eq. 3.8) and taking the positive root from (Eq. 3.9), the ratio (n_r) can

Figure 3.7: Modified structure considering Skin effect and Eddy Current Loss

be determined. Thus, the components, L_{S1A} and R_{f1} , can be calculated using (Eq. 3.10) [76].

By incorporating resistors (R_{S1} , R_{S2} , R_{f1} and R_{f2}) and inductors (L_{S1A} , L_{S1B} , L_{S2A} and L_{S2B}) to the equivalent circuit as shown in Fig. 3.7, the losses from the skin-depth and proximity effect can be accurately predicted.

Since the (Eq. 3.8) - (Eq. 3.10) are only capable to describe the mathematical separation of the series inductance, the summation of L_{S1A} and L_{S1B} should not exceed the calculated L_{S1} , which represents half of the L_S calculated by (Eq. 3.6). Based on Cao's work [76], further modification to determine L_{S1B} as shown in (Eq. 3.11) is necessary. The data analysis shows that the proximity effect [76] between L_{S1A} and L_{S1B} is small ($K_{proximity} \approx 0.0001$). It also has proven that the inductor (L_S) is only mathematically divided into L_{S1A} and L_{S1B} , which physically do not introduce any magnetic coupling effect. Thus, it is straightforward to create a more comprehensive model with fewer components, and the remaining components inherent from the bottom inductor can be computed using the conventional 2-port inductor equations cited in [73].

Table 3.2: Process parameters for 0.18 μm technology node

Parameter	Value
Silicon Substrate Resistivity (ρ_{Si})	10 $\Omega\text{-cm}$
Silicon Substrate Thickness	150 μm
Silicon dielectric constant	11.7
Silicon Oxide dielectric constant	3.9
Al-Cu Resistivity	2.439 $\mu\Omega\text{-cm}$
h (Top)	8.05 μm
h (Bottom)	2.29 μm
P	150 μm
g_1 (Eq. 3.6)	1 [11]
g_2 (Eq. 3.6)	2.46 [11]
g_3 (Eq. 3.6)	0 [11]
g_4 (Eq. 3.6)	0.2 [11]

$$L_{S1B} = \frac{L_S}{2} - L_{S1A} \quad (\text{Eq. 3.11})$$

3.1.1 Result and Discussion

The layout of the circular-shaped spiral stacked transformer follows the recommended interconnect dimensions from Table 3.1. And the process parameters for 0.18 μm technology node is shown in Table 3.2. For silicon verification, the stacked transformer has been simulated using the electromagnetic solver (HFSS) before fabrication. The electrical measurements have been carried out at 27°C and frequencies between 100 MHz to 15 GHz. All the PLTS measurements are extracted from the probe station using Short-Open-Load-Through (SOLT) calibration. The data are then exported out to ADS as touchstone files (s4p) for model simulation and evaluation.

To compare the proposed model, the PLTS measurement and the EM solver results, the individual port reflection coefficient (S(1,1), S(2,2), S(3,3) and S(4,4)) are shown in Fig. 3.8 - (3.11). For the PLTS measurements and the EM solver results, the series resistance and inductance are extracted at 100 MHz based on (Eq. 3.12) and (Eq. 3.13).

CHAPTER 3. MODELING OF STACKED TRANSFORMER

Figure 3.8: Port 1 reflection coefficient ($S(1,1)$)

Figure 3.9: Port 2 reflection coefficient ($S(2,2)$)

Figure 3.10: Port 3 reflection coefficient ($S(3,3)$)

Figure 3.11: Port 4 reflection coefficient ($S(4,4)$)

$$L_{S_extracted} = \frac{lm[(Y(1,1))^{-1}]}{\omega} \quad (\text{Eq. 3.12})$$

$$R_{S_extracted} = \text{Real}(Y(i,i))_{i=1,3}^{-1} \quad (\text{Eq. 3.13})$$

So far, the stacked transformer model is able to explain the increasing trend of the S-parameters by (Eq. 3.7) where R_S is modeled using the conventional DC method. However, there is still a significant discrepancy between the predicted and the measured result at frequencies less than 2 GHz as shown in Fig. 3.8 - 3.11. The difference is particularly obvious for port 3 (S33) and port 4 (S44) as illustrated in Fig. 3.10 and 3.11, hence an understanding of (Eq. 3.7) is necessary. After investigating the procedure on S-parameter extraction from the PLTS measurements and the EM solver results, the studies show that all the extracted data are based on the initial frequency at 100 MHz. In fact, the (Eq. 3.7) uses DC conditions to calculate the R_S value in predicting the frequency dependence causes a significant inaccuracy in computing the series resistor value. As a result, the model based on DC measurements is not correctly predicting the various S-parameters of the stacked transformer. Mihaela's work [77] suggests that the series resistor depends strongly on the frequency as shown in (Eq. 3.14).

$$\begin{aligned} \delta &= \sqrt{\frac{\rho_{Al-Cu}}{\pi \times freq \times \mu}} \\ t_{eff} &= \delta \left(1 - e^{-\frac{t}{\delta}}\right) \\ R_{S1} &= \frac{\rho_{Al-Cu} \times L_{GML}}{W \times t_{eff}} \end{aligned} \quad (\text{Eq. 3.14})$$

Therefore, the effect of the series resistances (R_{S1} & R_{S2}) losses at low frequency must be taken into consideration when computing the S-parameters.

Since the statistical variance is quite significant for the back-end-of-line (BEOL) processes, an exponential term with parameters (a and b) is introduced into (Eq. 3.14) to account for the variation as shown in (Eq. 3.15).

$$R_{S1} = \frac{\rho_{Al-Cu} \times L_{GML}}{W \times t_{eff}} \times \left(1 + e^{\frac{a-h}{b}}\right) \quad (\text{Eq. 3.15})$$

whereby h is the vertical separation between the conducting inductor and its underneath substrate.

By equating the PLTS measurements to the mathematical solutions in (Eq. 3.15), the frequency dependent R_S value is derived as shown in (Eq. 3.16).

$$R_{S_extracted} = R_{S1} = \frac{\rho_{Al-Cu} \times L_{GML}}{W \times t_{eff}} \times \left(1 + e^{\frac{a-h}{b}}\right) \quad (\text{Eq. 3.16})$$

Using the touchstone file (s4p) from PLTS, the simulation and extrapolation are successfully performed with ADS at frequencies between 10 to 200 MHz . Subsequently, (Eq. 3.16) is re-arranged to facilitate the computation of a and b as shown in (Eq. 3.17).

$$a = b \times \ln \left(\frac{R_{S_extracted} \times W \times t_{eff}}{\rho_{Al-Cu} \times L_{GML}} - 1 \right) + h \quad (\text{Eq. 3.17})$$

Based on (Eq. 3.17), a set of simultaneous equations has been setup to satisfy the conditions for the top and bottom coil. The values of a and b are plotted in Fig. 3.12. The calculated S-parameters using the modified R_S from (Eq. 3.15) are shown in Fig. 3.8 to Fig. 3.11. An excellent correlation is observed with an error of $< 10\%$ between the modified R_S and the measured data.

To demonstrate the robustness of (Eq. 3.15) for different type of stacked transformer, the silicon verification has been carried out subsequently using a $0.18\mu m$ process to fabricate an octagonal-shaped symmetrical based stacked transformer as shown in Fig. 3.13. The resistance of this stacked transformer is measured at an initial frequency of 50 MHz . To maintain the accuracy of (Eq. 3.15), the exponential parameters (a and b) are extracted at the same measured frequency. At the initial frequency, different set of a and b is used to ensure that the computed and the extracted value are close. The result

Figure 3.12: Empirical Value for a & b

Table 3.3: Verification of the Symmetrical Stacked transformer using (Eq. 3.15)

Coil	Width (μm)	Length (μm)	Turn	a (@50MHz)	b (@50MHz)	$R_{S_extracted}$ (Ω)	R_{S1} (Ω)
Top	6	1810	4	1.743	12.387	3.978	4.167
Bottom	6	1810	4	1.743	12.387	23.679	24.540

based on (Eq. 3.15) in Table 3.3 has demonstrated excellent correlation of $< 10\%$ on the octagonal-shaped stacked transformer.

The coupling coefficient, K , for the top inductor to the bottom inductor is extracted using (Eq. 3.18).

$$k = \sqrt{\frac{\text{imag}(Z_{12}) \times \text{imag}(Z_{21})}{\text{imag}(Z_{11}) \times \text{imag}(Z_{22})}} \quad (\text{Eq. 3.18})$$

All the components from the modified model are then optimized using ADS and recorded as optimized values in Table 3.4. Since the stacked transformer requires only minimum tuning, the predicted values are able to match the optimized values very well.

Figure 3.13: Octagonal symmetrical stacked transformer

Furthermore, the comparison between the measured and predicted input impedance for the primary coil has been carried out. The methodology to extract the input impedance is shown in (Eq. 3.19).

$$Zin_i = (Y_{(i,i)})^{-1} \Big|_{i=1 \rightarrow 2} \quad (\text{Eq. 3.19})$$

An excellent fit between the measured and the predicted impedance values for the primary coil is illustrated in Fig. 3.14 and Fig. 3.15.

To verify that the proposed model is applicable for stacked transformer with various sizes, a series of spiral stacked transformers with different number of turns are fabricated, measured and modeled as shown in Fig. 3.16. The Q values for the primary coil of the spiral stacked transformer are extracted as described in (Eq. 3.20) [13] and [73].

$$Q = \frac{\text{Im}(Y_{11}^{-1})}{\text{Real}(Y_{11}^{-1})} \quad (\text{Eq. 3.20})$$

To be consistent, the chosen a and b value at 100 MHz as shown in Fig. 3.12 for all the new spiral stacked transformers are the same as the firstly discuss stacked transformer.

Table 3.4: Circular Spiral Stacked transformer parameters

	Calculated	Measured	Optimized
L_S (Top) (nH)	4.3425	4.244	4.25
L_S (Bottom) (nH)	3.1239	3.502	3.5
L_{S1A} (nH)	1.16375	-	1.125
L_{S1B} (nH)	1.0075	-	1
L_{S2A} (nH)	0.87475	-	0.95
L_{S2B} (nH)	0.6872	-	0.8
R_{S1} (Ω)	3.823	3.815	3.81
R_{S2} (Ω)	12.645	12.655	12.6
C_{center} (fF)	65	-	80
C_{ox3} (fF)	145	-	145
C_{ox4} (fF)	145	-	145
C_{pp1+ox} (fF)	11.5	-	15
C_{pp2+ox} (fF)	11.5	-	15
C_{sub3} (fF)	3.5	-	3.5
C_{sub4} (fF)	3.5	-	3.5
R_{sub3} (Ω)	762.195	-	762.2
R_{sub4} (Ω)	762.195	-	762.2
R_{f1} (Ω)	142.55	-	146
R_{f2} (Ω)	429.56	-	435
K	-	0.7	0.7

Figure 3.14: Port-1 (Z_{in1}) Input impedance

Figure 3.15: Port-2 (Z_{in2}) Input impedance

Figure 3.16: Spiral stacked transformers (a) 2.5 turns, (b) 3.5 turns, (c) 4.5 turns, (d) 5.5 turns

Figure 3.17: Two port Q of the spiral stacked transformers with varies turns ratio

This is made possible by selecting the initial frequency for PLTS measurement at 100 MHz. A very good fit of $\sim 10\%$ error is observed for the 2 port Q comparison between the predicted and the measured data for different stacked transformers as shown in Fig.3.17.

3.1.2 Stacked Transformer in High-Q Application

The concept of using the proposed stacked transformer model to design a high-Q active inductor has been evaluated. The ideal block level experimental setup of the high-Q inductor application, using stacked transformer, is shown in Fig. 3.18 [78]. This setup is solely based on ideal components found in the ADS library so as to demonstrate the accuracy between the stacked transformer's measured silicon data vs. model simulation. The changes of Port 1 input impedance are observed by varying the phase of the voltage applied on Port 3. An increase of the mutual inductance also has been observed, however, the increment on the mutual inductance alone would not able to improve the quality

Figure 3.18: High-Q experimental Setup

factor of the stacked transformer. Hence, a variable gain amplifier is inserted into the circuit design to amplify the signal before feeding it into the secondary coil (Port 3 & 4).

The variable gain amplifier is fixed at 17.5 dB and the phase shifter is at 67° . At the same time, the directional coupler introduces a -20 dB gain before the variable gain amplifier [78].

The Q value of the active inductor is then extracted in touchstone file format (s4p). Fig. 3.19 shows the exponential increasing trend of Q value for frequency between 1.5 and 2.6 GHz. The proposed model can be concluded to be able to predict the experimental data very well.

A novel stacked transformer lumped circuit model is presented and described in depth. In addition, a modified equivalent circuit is proposed to model this stacked transformer. Both the skin-depth effect and the substrate eddy current have been considered for the frequency dependent stacked transformer. A modified equation explaining the frequency dependent enables a more accurate calculation of the series resistance than the conventional DC method. The proposed equation shows excellent correlation for a wide range of stacked transformer with various types and sizes. In summary, this novel stacked transformer model together with the modified R_S equations, are analytically efficient and can be used to optimize the high-Q on-chip active inductor for RF applications.

Figure 3.19: Q value of Stacked transformer in High-Q setup (1.5 GHz to 2.6 GHz)

Chapter 4

Geometry-Based Scalable Model for Stacked Transformer

In Chapter 3, a novel stacked transformer model with a set of semi-empirical formulas has been presented. However, the practical stacked transformer's compact model scalability depends heavily on the layout geometries, which includes *Substrate - Metal separation*, *Width* (W), *Inner Diameter* (D_{in}), *Number of Turns* (n), *Metal Thickness* and *Metal - Metal separation*. Therefore, a set of geometry-based scalable expressions to be developed using the model shown in Chapter 3. All expressions presented in this Chapter are derived based on Chartered's $0.18\mu\text{m}$ Industrial Compatible (*IC*) process. It is built from a range of geometry parameters, namely *Width* from 5 to $15\mu\text{m}$, *Inner Diameter* (D_{in}) from 60 - $150\mu\text{m}$, and number of turns (n) from 1 to 7. In total, there are 48 stacked transformers been fabricated in this set of matrix. Besides, additional de-embedding structures are fabricated to minimize measurement errors.

The model development presented in this chapter is based on the octagonal shape stacked transformer design. The reason for this selection is largely due to the fact that a circular design creates many DRC errors that could possibly cause manufacturing issues as the technology node shrinks. Intuitively, a polygonal shape (octagonal - eight sided with 45° angles) symmetrical stacked transformer is chosen so as to obtain a result close to a circular design while maintaining zero DRC violation. To justify this theory, a

Figure 4.1: a): Circular symmetrical inductor design. b): Octagonal symmetrical inductor design.

simple experiment is carried out using a circular symmetrical inductor vs. an octagonal symmetrical inductor as shown in Fig. 4.1. Both designs are based on $0.13\mu\text{m}$ -CMOS technology node based on identical inductance value. i.e, $N = 2$, Circular Inner diameter ($D_{in_{CIR}}$) = $100\mu\text{m}$, Octagonal Inner diameter ($D_{in_{OCT}}$) = $95\mu\text{m}$, Width = $15\mu\text{m}$ and Spacing = $3\mu\text{m}$. They are simulated using HFSS with a calibrated Chartered's $0.13\mu\text{m}$ -CMOS technology backend deck profile from Chartered.

The Q-factor, Inductance, and Series resistance plots of the comparison are shown in Fig. 4.2 and 4.3. This simple experiment demonstrates that the octagonal symmetrical inductor can achieve approximately the same results as that of a circular symmetrical inductor, with no DRC violation.

4.1 Stacked Transformers Analysis

The performances of the stacked transformers are analyzed to examine their geometry dependency. Some of the 48 transformers' micrograph are shown in Fig. 4.4, Fig. 4.5, Fig. 4.6 and Fig. 4.7 based on their number of turns.

In Fig. 4.8, the self-resonant frequencies of the primary and secondary coils are plotted verse the inductance value. This demonstrates that the self resonant frequency of the

Figure 4.2: The Q-factor and Inductance comparison plot.

Figure 4.3: The Inductor's series resistance comparison plot.

Figure 4.4: The 1-turn stacked transformer micrographs.

Figure 4.5: The 3-turn stacked transformer micrographs.

Figure 4.6: The 5-turn stacked transformer micrographs.

Figure 4.7: The 7-turn stacked transformer micrographs.

Figure 4.8: The self-resonant frequency and individual inductance relationship.

monolithic transformer has close relationship with its inductance value at low frequency. With reference to the data presented in Chapter 3, the secondary coil's substrate parasitic capacitances are transferred to the primary coil wholesomely that resonates both coils around the same frequency. This is possible only when both coils having the same inductance value and high magnetic coupling coefficient (k) thus, this phenomenon can only be found in stacked transformers. From this finding, the self-resonant frequency is also found to be dependent of the parasitic capacitance of the device substrate.

Fig. 4.9 - Fig. 4.11 show the magnetic coupling coefficient with respect to the device sizes for the selected metal width. The figures demonstrate that magnetic coupling increases as the area of the coils gets larger.

Similarly, the figures also show that with a given outer diameter, higher value of k can be attained for a smaller inner diameter. This feature is important when the selection of a higher inductance stacked transformer is required. For example, in Fig. 4.10: for a

Figure 4.9: The magnetic coupling (k) vs. Outer Diameter with the width fixed at $5 \mu m$.

Figure 4.10: The magnetic coupling (k) vs. Outer Diameter with the width fixed at $10 \mu m$.

Figure 4.11: The magnetic coupling (k) vs Outer Diameter with the width fixed at $15\mu m$.

given $D_{out} = 180\mu m$, the stacked transformer with $D_{in} = 70\mu m$ has a higher magnetic coupling than the stacked transformer with $D_{in} = 130\mu m$. Thus, it can be summarized that the magnetic coupling of the stacked transformers can be enhanced with the increase in the D_{out}/D_{in} ratio.

Although the use of smaller D_{in} can yield a higher magnetic coupling (with the use of more turns), there are several trade-offs needed to be taken into consideration. With higher turn ratio, the overall conductor length will be increased, leading to an increase in the series resistance and parasitic substrate capacitance. These increments induce more energy dissipation, which degrades the device performance. This effect can be best expressed with the well-known Q -factor equation shown in (Eq. 4.1).

$$Q = 2 \times \pi \times \frac{\text{Net Magnetic Energy Stored}}{\text{Energy Dissipated per Cycle}} \quad (\text{Eq. 4.1})$$

As the energy dissipation increase, the overall device's Q -factor will decrease.

4.2 Lumped Element Model

The proposed lumped element model for the scalable design is depicted in Chapter 3, Fig. 3.4. It represents a novel design that consists of the classical π -network on both the primary and secondary coils with modified ladder series impedance. It also models the electrical coupling from the main branches to the substrate (substrate capacitance) and branch to branch coupling (coils capacitance). This model is chosen because it is relatively easier to manage and it contains physical insight from the layout perspective. On the other hand, although a distributed network reflects the full physical behavior of the device but achieving a full scalability is near impossible and the cost for the computation increased as the device gets larger.

The layout configuration used in this geometry-based scalable model is standardized to be the symmetrical stacked-transformer design as shown in Fig. 3.13. There is a difference in the layout configuration as compared to spiral layout shown in Fig. 3.16. The difference can be easily identified by tracing the simulated current direction. Generally, there is an obvious physical difference between the two designs, which is the port locality. In the symmetrical design, the ports of the same coil are located on the same plane naturally; however, the spiral design would require an additional via to surface the bottom port to the same level. The simulated current flow direction for the symmetry stacked transformer shown in Fig. 4.12 illustrates the symmetrical property of the design.

The symmetrical stacked transformer design is proven to be user friendly at the expense of higher series resistance caused by the increase in the number of vias. From modeling point of view, the symmetrical stacked transformer has better predictability as compared to the spiral stacked transformer design. The assumption in most of the spiral stacked transformer to simplify the capacitance at the coil-underpass overlap (see Fig. 4.13) is responsible for the inefficiency. This is particularly serious as the width of the device gets larger. The other factor that is in favor of the symmetrical stacked transformer

Figure 4.12: The simulated current flow direction in the stacked transformer design.

design is the violation of the design rule in the circular spiral stacked transformer design. A circular spiral can easily generate tenths of thousands of DRC (design rule check) violation on acute angle. No doubt, the use of the square spiral stacked transformer design could resolve the DRC errors but its right-angle corners largely increase the coil series resistance (due to the current crowding effect), which degrades the device performance significantly. As shown in the earlier part of this chapter, octagonal shape is the most efficient layout configuration.

In the proposed model, the overall inductance of the primary and secondary coils, L_{Pri} and L_{Sec} , are computed using the current sheet expression presented by Mohan *et. al* [11] (Eq. 3.6). Where g_1, g_2, g_3 and g_4 takes the values of 1, 2.46, 0 and 0.2.

With the effect of both the skin and proximity, the current density in the conductor at a given frequency tends to crowd toward its outer surface. This phenomenon causes the series resistance to be dependent of frequency; and makes it difficult to model using physics-based expressions. This is especially important in a transformer as close proximity is one of the fundamental principles [79] - [82]. Most reported models are based

Figure 4.13: The top-view of the spiral stacked transformer design that demonstrates the overlap capacitance assumption.

on either empirical monomial, or frequency-dependent fitting for the parasitic series resistance value. The low frequency resistance value is one of the key components in the scalable lumped model design flow as it forms the initial resistive response of the model. Thus, an accurate expression that has the ability to model this component is needed. In Chapter 3, the proposed series resistive expression (Eq. 3.15) that accounts for the process statistical variances is evolved from the well-known frequency-dependent resistance calculation (Eq. 3.14) [77]. In a scalable model development, process statistical variances have to be incorporated into the expression as a form of error percentile as different processes will sustain different set of process variations. Moreover, from the experimental extraction of 48 stacked transformers, which were based on Chartered's $0.18\mu\text{m}$ industrial compatible process, the dependency of the additional process variance correction term $(1 - e^{-\frac{t}{\delta}})$ is found to be weak. In fact, this initial resistance value is heavily dependent on the metal sheet resistance (ρ_{Al-Cu}). Although majority of the works reported in the literature have simplified the problem by assuming that the sheet resistance for all the

metal layers remains constant throughout all geometry, this assumption does not hold in RF CMOS process. Therefore, the modified conventional sheet resistance equation is employed in this proposed model with the focus placed on the metal sheet resistance adjustment for the thick top-most metal layer ($\rho_{018IB-thick}$) and thin lower metal layers ($\rho_{018IB-thin}$) as shown in (Eq. 4.2).

$$\begin{aligned} R_{Pri} &= \frac{\rho_{018IB-thick} \times L_{GML}}{W \times t} \\ R_{Sec} &= \frac{\rho_{018IB-thin} \times L_{GML}}{W \times t} \end{aligned} \quad (\text{Eq. 4.2})$$

where the adjusted $\rho_{018IB-thick}$ and $\rho_{018IB-thin}$ have the values of 4.500 and 20.021 $\mu\Omega - cm$. This calibration of the sheet resistance with the experimental data will be able to capture the process systematic errors on the documented sheet resistance. In comparison with the sheet resistance found in Chapter 3, the adjusted sheet resistance values are found to be higher, which can be attributed to the different 0.18 μ process that is used in fabricating the set of stacked transformer matrix reported in this Chapter. It is built on the industrial compatible (IC) that has thinner (lower t value) metal layers as compared to the Chartered's baseline (CB) process demonstrated in Chapter 3.

To account for the skin effect into the scalable model, the proposed ladder network calculation for the series resistance and inductance are modified as show in (Eq. 4.3) [18]. It consists of 2 empirical coefficients for each coil, K_{Rp} and K_{Lp} that simplifies the model, while maintain high degree of accuracy.

$$\begin{aligned} R_{ser-pri-a,b} &= K_{Rp} \times R_{par-pri-a,b}, \\ L_{pri-a-2,pri-b-2} &= K_{Lp} \times L_{pri-a-1,pri-b-1}, \\ R_{par-pri-a} &= R_{par-pri-b} = (1 + (1/K_{Rp})) \times R_{DC}/2, \\ L_{pri-a-1} &= L_{pri-b-1} \\ &= L_{DC}/[2 + 2K_{Lp} \times (1 + K_{Rp})^{-2}] \end{aligned} \quad (\text{Eq. 4.3})$$

These semi-empirical coefficients K_{Rp} , K_{Rs} , K_{Lp} and K_{Ls} are held constant in this work, $K_{Rp}=0.96$, $K_{Rs}=0.884$ and $K_{Lp} = K_{Ls}=0.27$.

In the stacked transformer, the magnetic flux that couples from one coil to the other depends on the geometrical parameters of the routing as shown in Fig. 4.9 - Fig. 4.11. Indeed, the magnetic coupling coefficient of the investigated transformers can vary from 0.4 to 0.97, depending on the device dimensions. Thus, the geometry dependence for this parameter was taken into consideration in this proposed lumped element model. Several works in literature have reported the use of a constant coupling coefficient value for model simplicity that leads to an error range of as large as $\pm 13\%$ [16]. The dependence of the magnetic coupling coefficient (k) on the layout of the coils was taken into account using the several proposed layout related parameters. These parameters are average diameter (D_{avg}), fill factor (ϑ) and effective width ratio ($W_{eff-ratio}$) as expressed in (Eq. 4.4).

$$\begin{aligned} D_{avg} &= \frac{OD + ID}{2} \\ \vartheta &= \frac{OD - ID}{OD + ID} \\ W_{eff-ratio} &= \frac{D_{diff}}{2 \times N \times W} \\ D_{diff} &= OD - ID \end{aligned} \tag{Eq. 4.4}$$

The proposed magnetic coupling coefficient for the scalable model is

$$k = x_1 - \frac{x_2}{D_{avg}} - x_3 \times W_{eff-ratio} + x_4 \times N - x_5 \times \vartheta \tag{Eq. 4.5}$$

where x_1, x_2, x_3, x_4 and x_5 are coefficients determined by least-square-fitting to the measured data. Their values were 1.069, 2.150, 0.218, 0.031 and 0.143, respectively.

The accuracy of (Eq. 4.5) is demonstrated in Fig. 4.14 and Fig. 4.15 that compare the measured and model simulated S21 and the magnetic coupling coefficients of the stacked transformer ($D_{in} = 110\mu\text{m}$, $\text{Width} = 10\mu\text{m}$ and $\text{Turn} = 3$) from the test matrix. The magnetic coupling coefficient shown in Fig. 4.15 is extracted using (Eq. 4.6).

Figure 4.14: The S21 verification using (Eq. 4.5) on stacked transformer with $D_{in} = 110\mu\text{m}$, Width = $10\mu\text{m}$ and Turn = 3.

$$k = \sqrt{\frac{\text{imag}(Z_{12}) \times \text{imag}(Z_{21})}{\text{imag}(Z_{11}) \times \text{imag}(Z_{22})}} \quad (\text{Eq. 4.6})$$

The results show a good agreement with an average error of $< 2\%$ with respect to the measurement data.

The inter-coils electrical coupling (capacitance) is the other key parameter that is related to the device layout dimension. In the stacked transformer model proposed earlier, this effect is distributed evenly across the whole device into two main branches. They are namely the center capacitance (C_{center}) and the parallel port-to-port capacitance ($C_{pp1,2+ox}$) as reported in Chapter 3. However, the reported model trade-offs its accuracy for simplicity as it does not account for the crossed port-to-port coupling ($C_{cross-pp1,2+ox}$). This component is a crucial element, especially in symmetry stacked transformer (see Fig. 4.12) as the winding inter-crosses one another to create the symmetricity effect. Hence, an additional branch is included into Fig. 3.7 and illustrated in Fig. 4.16.

Figure 4.15: The magnetic coupling (k) verification using (Eq. 4.5) on stacked transformer with $D_{in} = 110\mu\text{m}$, $\text{Width} = 10\mu\text{m}$ and $\text{Turn} = 3$.

Figure 4.16: The geometries scalable stacked transformer model.

Since all the capacitances are determined based on the distribution of the overall overlapping capacitance (the percentage of the overall overlapping surface area - $C_{overall}$). Thus, the derivation of the $C_{overall}$ is the most fundamental approach to the electrical coupling in the device, as shown in (Eq. 4.7).

$$C_{overall} = \frac{\varepsilon \times Area}{d_{plate-plate}} [\sigma_1 + \sigma_2 \times \ln(W_{eff-ratio}) + \sigma_3 \times \ln(\rho)] \quad (\text{Eq. 4.7})$$

$$Area = 2 \times \tan 22.5^\circ (OD^2 - ID^2)$$

where $d_{plate-plate}$ is the physical plate-to-plate separation (primary to secondary plane) that has the value of $2.15\mu\text{m}$, ε is the oxide dielectric constant and $Area$ is the area of plate-to-plate overlap of the stacked transformer. Also, σ_1 , σ_2 , and σ_3 are coefficients that account for the geometry dependency that have the value of 0.966, 0.229, and 0.119, respectively. Similar to the distribution effect reported in Chapter 3, the 3 branches of capacitances get its value as follows: $C_{pp1,2+ox} = 0.1 \times C_{overall}$, $C_{cross-pp1,2+ox} = 0.04 \times C_{overall}$ and $C_{center} = 0.72 \times C_{overall}$.

The electric losses of the silicon substrate are proportional to its conductivity and working frequency. There are 3 different signal propagation modes for the metal on silicon substrate as determined by the conductivity as well as the working frequency. Silicon substrate will act as a dielectric layer if it is highly resistive. At very high frequency the silicon substrate will act like a metal layer. Moderate working frequency, where most commercial frequencies lie, will lead to a propagation mode that falls in between the above-mentioned two modes. This intermittent mode is also known as *slowwave mode* [83]. Each mode has a corresponding equivalent circuit model, which leads to different types of substrate configuration. In most of the modeling reports in the literature, silicon substrate is only modeled as a dielectric layer using RC network [73], [76] and [82]. However, this type of modeling method is only applicable to relatively high resistive substrate at low frequency. For moderate and high conductivity or moderate resistive at

high frequency, the substrate skin effect needs to be considered. Hence, Huo *et.al.* [84] has consolidated a set of substrate expressions that takes into account the substrate skin effect using the effective thickness and effective dielectric constant reported by Schneider [85]. This set of effective substrate parameters are shown in (Eq. 4.8).

$$\begin{aligned}\varepsilon_{eff} &= \frac{1 + \varepsilon_{sil}}{2} + \frac{\varepsilon_{sil} - 1}{2} \left(1 + \frac{10 \times t}{W}\right)^{-0.5} \\ d_{eff} &= \frac{W}{2 \times \pi} \times \ln \left(\frac{8 \times t}{W} + \frac{4 \times W}{t}\right)\end{aligned}\tag{Eq. 4.8}$$

In this work, the stacked transformer has a slightly different working substrate principle that leads to the need to modify the substrate capacitances. It is found that the substrate capacitances has a strong relationship with the device effective width ($W_{eff-ratio}$) as show in (Eq. 4.9).

$$C_{sub} = \frac{\varepsilon \times \varepsilon_{eff} \times Area}{2 \times d_{eff} \times W_{eff-ratio}}\tag{Eq. 4.9}$$

4.3 Experimental Validation

The geometrical scalability of the model and its accuracy up to the transformer self-resonant frequency are demonstrated by comparing with the measurements show in Fig. 4.17 - Fig. 4.26. All the measurement and simulation are presented based on two-port topology (port 2 and 4 are connected to ground) for better pictorial illustration of the result as a four-port results does not carried much performance information. A wide range of layout geometries are covered and 5 selected stacked transformers with different dimension are depicted in Fig. 4.17 - Fig. 4.26 as a function of frequency that demonstrates the accuracy of the model up to its resonant frequency.

To demonstrate the capabilities of the proposed model, some of the key components that are the foundation of the model are tabulated and show in Table. 4.1. It shows that

Figure 4.17: The a) S11 and b) S22 smith plot of the stacked transformer model simulation vs measurement with $D_{in} = 70\mu\text{m}$, Width = $8\mu\text{m}$ and Turns = 2.

Figure 4.18: The S21 dB plot of the stacked transformer model simulation vs measurement with $D_{in} = 70\mu\text{m}$, Width = $8\mu\text{m}$ and Turns = 2.

Figure 4.19: The a) S11 and b) S22 smith plot of the stacked transformer model simulation vs measurement with $D_{in} = 90\mu\text{m}$, Width = $15\mu\text{m}$ and Turns = 3.

Figure 4.20: The S21 dB plot of the stacked transformer model simulation vs measurement with $D_{in} = 90\mu\text{m}$, Width = $15\mu\text{m}$ and Turns = 3.

Figure 4.21: The a) S11 and b) S22 smith plot of the stacked transformer model simulation vs measurement with $D_{in} = 100\mu\text{m}$, Width = $5\mu\text{m}$ and Turns = 5.

Figure 4.22: The S21 dB plot of the stacked transformer model simulation vs measurement with $D_{in} = 100\mu\text{m}$, Width = $5\mu\text{m}$ and Turns = 5.

Figure 4.23: The a) S11 and b) S22 smith plot of the stacked transformer model simulation vs measurement with $D_{in} = 120\mu\text{m}$, $\text{Width} = 15\mu\text{m}$ and $\text{Turns} = 7$.

Figure 4.24: The S21 dB plot of the stacked transformer model simulation vs measurement with $D_{in} = 120\mu\text{m}$, $\text{Width} = 15\mu\text{m}$ and $\text{Turns} = 7$.

Figure 4.25: The a) S11 and b) S22 smith plot of the stacked transformer model simulation vs measurement with $D_{in} = 150\mu\text{m}$, Width = $10\mu\text{m}$ and Turns = 4.

Figure 4.26: The S21 dB plot of the stacked transformer model simulation vs measurement with $D_{in} = 150\mu\text{m}$, Width = $10\mu\text{m}$ and Turns = 4.

Table 4.1: List of low frequency Inductance and Resistance values of the transformer model and its measured result

Din (μm)	Width (μm)	Turn (N)	L_{Pri-m} (nH)	L_{Sec-m} (nH)	L_{sim} (nH)	R_{Pri-m} (Ω)	R_{Sec-m} (Ω)	$R_{Pri-sim}$ (Ω)	$R_{Sec-sim}$ (Ω)
60	5	3	1.00	1.09	1.03	2.98	13.06	2.83	12.60
60	5	5	2.81	2.89	2.88	5.96	25.86	5.65	25.10
60	5	7	5.81	5.78	5.91	9.39	41.74	9.21	41.06
80	5	3	1.37	1.46	1.42	3.46	16.08	3.53	15.70
80	5	5	3.69	3.77	3.80	6.73	30.86	6.82	30.32
80	5	7	7.50	7.30	7.58	10.47	48.79	10.82	48.36
100	5	3	1.75	1.83	1.82	3.94	19.15	4.21	18.89
100	5	5	4.67	4.70	4.78	7.56	36.00	7.98	35.56
100	5	7	9.28	9.00	9.29	11.62	55.93	12.51	55.58
70	10	3	1.17	1.23	1.20	1.78	8.28	1.85	8.24
70	10	5	3.46	3.49	3.52	3.66	17.01	3.84	17.11
70	10	7	7.54	7.41	7.52	5.95	28.42	6.39	28.75
110	10	3	1.86	1.92	1.91	2.26	11.35	2.55	11.42
110	10	5	5.17	5.16	5.20	4.47	22.12	5.01	22.33
110	10	7	10.80	10.48	10.67	7.09	35.58	7.99	35.92
150	10	2	1.24	1.29	1.27	1.66	9.01	2.02	8.97
150	10	4	4.56	4.54	4.60	3.96	20.49	4.20	20.38
150	10	6	10.40	10.00	10.28	6.72	34.67	7.32	35.06
90	15	3	1.48	1.51	1.53	1.48	7.21	1.64	7.31
90	15	5	4.33	4.56	4.61	3.07	15.02	3.22	15.31
90	15	7	10.10	9.87	9.94	5.04	25.32	5.39	25.83
120	15	3	1.95	2.06	2.06	1.72	8.74	1.99	8.86
120	15	5	5.78	5.77	5.86	3.47	17.59	3.86	17.92
120	15	7	12.80	12.30	12.21	5.61	28.89	6.02	29.40

the model simulated values based on the above reported equations yielded accurate data as compared to the measurement result.

In summary, the error terms are plotted for the most common figure-of-merits based on the set of 48 stacked transformer matrix as illustrated in Fig. 4.27 - Fig. 4.29. In general, the critical parameters of the scalable stacked transformer could be predicted within 7% tolerance, where majority of the values fall $< 3\%$ error.

The effect of layout parameters on the performance of monolithic stacked transformers was investigated through on-wafer experimental measurements of several structures based

Figure 4.27: The magnetic coupling coefficient (k) error term of the stacked transformer with respect to measurement and model comparison.

Figure 4.28: The primary coil's low frequency resistance error term of the stacked transformer with respect to measurement and model comparison.

Figure 4.29: The primary coil's low frequency resistance error term of the stacked transformer with respect to measurement and model comparison.

on Chartered Semiconductor Manufacturing's $0.18\mu\text{m}$ Industrial Compatible process. It demonstrates the fact that increase of the transformer silicon area can be used to enhance the magnetic coupling coefficient with an expense of large substrate electrical coupling, which degrades the self-resonant frequency. The proposed scalable lumped element circuit and its closed-form expressions have also proven to be able to produce $< 7\%$ error based on measurement verification of the S-parameters, coil inductance, coil resistance, magnetic coupling coefficient.

4.4 Challenges

Based on the literature review in Chapter 2 and stacked transformer investigation in the previous sections, five major challenges for the monolithic transformer have been identified.

1. It is well known that a stacked transformer is capable of producing a high magnetic

coupling coefficient, up to 0.95. However, this high coupling coefficient comes with a price of large device area, which means large inductance with low working frequency. For a moderate inductance application, the highest k ever reported is < 0.7 . An ideal transformer that bears a k value of 1 is able to have its signal transferred from one coil to the other with zero losses. In monolithic application, the use of lossy substrate makes the k value impossible to be ideal. Thus, it is identified as one of the challenges in the current and future transformer design.

2. With reference to Challenge No. 1, the transmission loss (also known as S21 in two-port configuration) of the transformer is also a key challenge ahead. As process improved into smaller feature size and lower operating voltage, the transmission loss becomes particularly crucial. Even though an excellent monolithic transformer that has the best performance parameters could only attain a transmission losses of 5 dB, which will still attenuated/degraded the signal that is passed through this block. So the development to uncover the methods to improve the transmission loss is always the on-going research focus in RFIC.

3. Generally, the self-resonant frequency of the on-chip inductor is much smaller as compared to off-chip inductor, due to the conductive/lossy substrate that increased the shunt parasitic capacitance. Moreover, the use of two microstrip lines configured as a transformer increases the internal electrical coupling that drives the self-resonant frequencies into an even lower regime. Several backend methods (i.e. Micro-machined substrate, bond wire, etc.) have been introduced to provide solution to wideband applications. However, these methods are normally very expensive and lack of repeatability.

4. Challenges No. 1 to 3 are mainly focusing on the circuit performance. And in the current and future RFIC, designers are given a constricted design floor that does not enable too much flexibility. In low and moderate operating frequency applications (i.e. GSM, WiFi), the inductance value needed for these frequencies selection are usually very

big. Some of these circuits have its inductors occupying more than 90 % of its entire chip area. The other application that potentially needs high inductance value is the impedance matching network. In practice, the turn ratio of the transformer in impedance matching application is restricted to a value not more than 1:10. One of the showstopper for this restriction is the huge silicon area consumption for transformer with turn ratio larger than 1:10. Therefore, the need for a transformer that occupies a smaller silicon area is desired.

5. The state-of-the-art transformer normally have the unit inductance value reported to be $< 0.2 \text{ pH}/\mu\text{m}^2$. Together with Challenge No. 4, it demonstrates that the need for a high unit inductance transformer with respect to its silicon area has to be developed. It must also be able to provide large turn ratio range that gives RFIC designers maximum flexibility.

Chapter 5

Symmetrical Transformer Design

Up to date, majority of the design in [8]-[6] had shown enhancement in circuit performance than that of a non-transformer integrated design. The monolithic transformer has the ability to reduce the silicon area consumption (stacked design can achieve up to 50%), has demonstrated excellent area efficiency. This reduction has become a figure-of-merit, as silicon area is a limiting factor in current and future RFIC design.

Some general circuit applications for a symmetrical device are shown in Fig. 5.1. In [86], Kluge *et.al.* has highlighted that a symmetric differential inductor is proven to be better in suppressing common-mode signals instead of two single-ended inductors. However, using conventional differential inductor, it does not have true symmetry property. The coupling coefficient is low and the area consumption is usually very high for large inductance applications. Thus, a symmetrical transformer connected as a differential inductor is one of the solutions to this limitation.

The need for a symmetrical transformer extends to unconventional circuits as well. Such as LC-VCO [87]. In [87], it requires an electrically symmetrical structure to form the parallel LC-tank that yields identical inductance and resistance values.

Commonly, there are two main types of monolithic transformer configurations that are (i.e. interleaved and stacked) widely used in two kinds of differential orientation (i.e. Flux-linkage (FL) and transmission line transformer (TLT) orientation). The flux-linkage

Figure 5.1: Fully symmetrical (1:1) transformer used as a (a) drain & input differential inductor pairs in simple differential LNA design [88] and (b) input stage of the system as differential broadband transformer in TLT configuration

transformer is usually limited to lower frequency applications by its inherent distributed winding capacitance. Thus, the latter TLT is introduced for higher frequency applications. Ideally, a 1:1 TLT transformer requires a pair of identical coils that is not achievable with the current monolithic transformer design. It is well known that the real world monolithic transformers (interwinding or overlapping of the coils) have problems such as the different finite metal line resistances on various backend layers, unmatched finite inductances between the primary and secondary coils and imperfect power losses, especially with lossy silicon substrate. In general, monolithic implementation of a 1: n transformer is proven to be relatively simpler than a 1:1 transformer [13]. With the challenge identified, Lee *et.al* has proposed a new type of transformer structure that demonstrates a nearly 1:1 ratio design [89]. However, the area of the design proposed by Lee *et. al.* is not completely efficient as additional silicon area is needed to facilitate the interconnection.

5.1 An Area Efficient Symmetrical Monolithic Transformer using Inter-coil-crossing Method [90]

A novel method that produces an area efficient, close to ideal 1:1 monolithic transformer is proposed and compared with the existing stacked transformer structure in this part of the work. The proposed design demonstrates higher self-resonant frequency with excellent area efficiency.

5.1.1 Proposed Transformer Design

The fundamental concept of this design is derived by combining the two existing transformer configurations; stacked and interleaved. This is realized using several metallization layers for interconnects overpasses, and underpasses [91]. Inevitably, the impedance of the two coils is expected to be similar as they are physically equalized through the inter-coil-crossing. The 3D view of the proposed transformer design is depicted in Fig. 5.2, where the proposed structure is classified into two segments along the Y'-Y'' axis. Each half will experience a switching from top layer to the bottom layer, same goes for the bottom layer as shown in the cross-sectional view of the proposed design. The inter-coil routing of the design can be better described by isolating one winding from the design. Fig. 5.3 shows the primary winding of the proposed design. The winding has an equal amount of metallization layers from various metal schemes, while maintaining the same physical length and number of turns, irrespective of the layers. In general, Fig. 5.2 can be summarized into an effective four-turn transformer with each coil having four half-turns of the top and bottom layers.

In the conventional transformer design, the mutual coupling is *laterally* or *vertically* unidirectional for interleaved [18] or stacked design [70], respectively. However, as shown in the cross-sectional view of Fig. 5.3, in the proposed transformer design, a bi-directional mutual coupling can be achieved. i.e., P1 is vertically coupled with S1 and horizontally

Figure 5.2: The 3D view of the proposed transformer design with cross-sectional view along X'-X'' axis.

Figure 5.3: The proposed design's primary winding that demonstrates the novel inter-coil-crossing using multiple metallization layers.

coupled with S2. The routing of the layers must also ensure that at any time the current does not travel in opposite direction within the same coil. This is crucial as the reverse current produces a negative self-inductance effect that will substantially reduce the overall coil inductance. The proposed transformer's unique way of inter-coil-crossing requires six metallization layers. TM and TM-4 are the layers forming the main coil, whereby TM-1, TM-2, TM-3 and TM-5 are used to form underpasses for this design. TM is the topmost metal layer and TM-5 is the bottom-most layer.

5.1.2 Results And Discussion

In this work, octagonal shape inductors has been taken as standard for evaluation. Recently, the differential circuits have become popular as they can better suppress common mode noise. Therefore, the TLT orientation with wider bandwidth has been selected to be the benchmark for all differential comparison in this work. The measurement data are obtained using Agilent E8364B Performance Network Analyzer (PNA) and Physical Layer Test System (PLTS) on Cascade S300 probe station. G-S-G-S-G type of Infinity probes with 100 μm pitch are carefully calibrated using SOLR (short, open, load, reciprocal thru) on Impedance Standard Substrate (ISS: 129-239) so as to ensure no measurement errors are brought over to the device data. The measured data are subsequently de-embedded using simple four port de-embedding techniques as expressed in equation (Eq. 5.1).

$$\begin{aligned}
[Y_{less-open}] &= [Y_{DUT}] - [Y_{open}], \\
[Y_{short-open}] &= [Y_{short}] - [Y_{open}], \\
[Z_{final}] &= [Z_{less-open}] - I \cdot [Z_{short-open}] + \begin{bmatrix} a & 0 & 0 & 0 \\ 0 & a & 0 & 0 \\ 0 & 0 & b & 0 \\ 0 & 0 & 0 & b \end{bmatrix}
\end{aligned} \tag{Eq. 5.1}$$

$I = \text{unit matrix}$

$$\begin{aligned}
a &= \frac{Z_{12(short)} + Z_{21(short)}}{2}, \\
b &= \frac{Z_{34(short)} + Z_{43(short)}}{2}
\end{aligned}$$

Y_{DUT} is the admittance of the DUT, Y_{open} the admittance of the open structure, Y_{short} is the admittance of the short structure, Z_{short} is the impedance of the short structure. All the admittance/impedance in equation (Eq. 5.1) is derived from the measured S-parameters. The final Z_{final} is converted back to S-parameter for performance evaluation. i.e. S_{final} The de-embedded single-ended coil inductances are then extracted based on the configuration shown in Fig. 5.4(a). Next, the single-ended to differential mode conversion is performed based on the standard single-to-differential mode conversion equations for TLT comparison, using configuration shown in Fig. 5.4(b). The design parameters for the proposed structure are as follows: Number of turns (N) = 4, Width (W) = 6 μm , Inner Diameter (ID) = 100 μm , Turn spacing (s) = 2 μm , Silicon Area = 228.28 μm^2 , Silicon thickness (h_{sil}) = 150 μm , Top Metal thickness (T_{TM}) = 3.03 μm , Metal 1-5 thickness (T_{TM-1} to T_{TM-5}) = 0.465 μm and Inter-metal oxide thickness = 0.42 μm . Among the various existing transformer configurations such as stacked, vertical coupled and Interleaved, lateral coupled, the stacked design is chosen to be the suitable candidate because it occupies the same amount of silicon area as the proposed design (228.28 μm^2). The extracted individual coil Inductance, differential quality factor (Qd), and differential S21 (S_{d21}) between the two transformers are extracted and shown in Figs. 5.4(a) and (b), together with the corresponding extraction technique. The experimental

and EM-simulated S_{d21} (dB) and Q_d are plotted in Fig. 5.4(b). These two parameters are considered the most fundamental requirements in transformer design. In Fig. 5.4(b), the proposed transformer is able to attain a comparable transmission power with $|S_{d21}|$ ranging from 0.7 dB to 3.3 dB at lower frequency band (50 MHz - 2.45 GHz). At 2.45 GHz, the proposed design demonstrates 0.3 dB enhancement in $|S_{d21}|$ as compared to stacked design. Concurrently, the stacked design has its S_{d21} roll-off faster than that of the proposed design as frequency moves beyond 6 GHz. In summary, the proposed design has also demonstrated a higher differential self-resonant frequency. The $f_{d_SRF(Stacked)} = 8$ GHz for stacked design and the $f_{d_SRF(Sym)} = 10.35$ GHz for proposed design. This improvement in the f_{SRF} is attributed to the larger separation of the windings' vertical plate-to-plate distance. As shown in the cross-sectional view of Fig. 5.2, $h_{stacked}$ (metal f-f) $<$ h_{sym} (metal f-f) results in a smaller overall winding capacitance. The stacked transformer is formed using layer TM and TM-2 (Fig. 5.4(a)) whereas the proposed design uses layer TM and TM-4.

The $Q_{d_{peak}}$ of the stacked design demonstrates a slightly higher value compared to the proposed design (Fig. 5.4(b)). This phenomenon can be attributed to the increase in the overall effective coil resistance of the proposed design that is due to the mixture of thick (TM) and thin (TM-4) metal layers within the same winding. Nevertheless, design optimization can still be incorporated into the proposed design to further enhance its performance with no additional manufacturing cost. This is achieved by via-connecting multiple thin lower metal layers (i.e. TM-2 + TM-3 + TM-4), the overall effective coil resistance will be reduced, improving the quality factor of the device.

Figure 5.4: (a) The individual coil inductance plot of the stacked and the proposed transformer designs together with the 3D and the cross-sectional view of the stacked design. (b) The differential Q and S_{d21} plots of the stacked and the proposed transformer designs.

5.2 A Fully Symmetrical Monolithic Transformer [92]

The design proposed in Chapter 5.1 can be further modified to improve the symmetry of the device by sub-dividing each half of the Symmetrical Transformer design into quadrant. Two novel monolithic fully symmetrical transformer designs are proposed and compared with the existing transformer structures[92]. The first proposed fully symmetrical (FS) design demonstrates better performance in terms of area efficiency, self-resonant frequency, and symmetry. Equivalent circuit model that shows good agreement to the measured novel transformer is also reported in this work using accurate geometries-based equations. The trade-off option between the self-resonant frequency and S21 and k are introduced in the second proposed FS design, offering more flexibility to RFIC designers.

Figure 5.5: 3D view of the FST1 and $0.13\mu\text{m}$ silicon die photo.

5.2.1 Description

The first proposed fully symmetrical transformer (FST1) has its primary and secondary coils inter-crossed, equalizing the physical aspect of the two windings [91]. The concept of the design is based on using several metallization layers as interconnects to achieve inter-coil crossing. Thus, the impedance looking into the two windings are expected to be identical. The 3D view of the FST1 is depicted in Fig. 5.5 together with its silicon die photo.

The structure consists of four segments. Each quadrant will experience a switching from top layer to the corresponding bottom layer. The fully symmetrical property of the design can be illustrated by virtually separating the two coils from their inter-crossing as shown in Fig. 5.6(a). Each coil will be experiencing equal amount of various metallization

Figure 5.6: (a) Virtual separation of the primary and secondary coil that depicts the fully symmetrical property of the FST1. (b) layers description of the FST1 based on one of the coils

layers, while maintaining the same physical length (number of turns, irrespective of the layers). For example, Fig. 5.6 demonstrates a four turn transformer design with each coil having eight quadrants of both the top and bottom layers. It is clearly visible that the two coils are in fact identical. They are integrated with 180 degree difference in the port orientation.

In the conventional transformer design, the mutual coupling is *unidirectional*, either laterally or vertically. However, in the FST1, a *multi-directional* mutual coupling can be achieved. Fig. 5.7 illustrates this process using the cross sectional view of the proposed design along X'-X'' axis. Quadrant s6 is not limited to vertical coupling provided by

Figure 5.7: Cross sectional view of the FST1 along $X'-X''$ as shown in Fig.5.5.

quadrant p5, it has quadrant p9 and p13 contributing the lateral coupling. Thus, the mutual coupling of the FST1 is expected to improve. The routing of the design must also ensure the current travels only in one direction within the same coil. This is crucial, as the reverse current will result in negative self-inductance effect that substantially reduces the overall coil inductance.

The proposed transformer's novel way of inter-coil crossing method, requires six metallization layers as shown in Fig. 5.6(b). By expanding the 3D view of the design shown in Fig. 5.8, it reveals the detailed via mapping of the FST1. The vertical deck of the metal layers is illustrated in Fig. 5.9. TM and TM-4 are the layers forming the turns quadrant, whereby TM-1, TM-2, TM-3 and TM-5 are used to form underpasses and overpasses for this design. Similarly, TM denotes the topmost metal layer and TM-5 is the bottom-most layer.

5.2.2 Equivalent Lumped Circuit Model

Generally, a simple two-port lumped circuit element is sufficient to model all multi-port devices as one or more ports will be grounded in most practical circuit applications. However, for this fully symmetrical device, the model with independently driven terminals

Figure 5.8: 3D exploration view of the FST1 with detail vias mapping.

Figure 5.9: The vertical metallization profile of the FST1 design.

is much more appropriate in showing the credibility of the differential mode applications. Fig. 5.10 illustrates the proposed equivalent lumped circuit model for the novel design. The electrical model of this design is relatively simpler as compared to the conventional transformer. This is because both winding are identical, requiring only single branch solutions. The proposed design's turns are described by ideal inductors together with resistors in a ladder network as suggested in [12] and [93]. The magnetic coupling coefficient are modeled in terms of k . The port-to-port capacitive effects from various nodes are captured with $C_{pp,P2-3}$, $C_{pp,P1-4}$, $C_{pp,P1-sec_ctr}$, $C_{pp,P2-pri_ctr}$, $C_{pp,P3-sec_ctr}$ and $C_{pp,P4-pri_ctr}$. Whereas $C_{ox,P1}$ to $C_{ox,P4}$ models the parasitic capacitance of the device to the silicon substrate. The entire substrate network (silicon area beneath the device) is separated into six blocks of C_{sub} and R_{sub} to better model the distribution effect of the lossy substrate.

5.2.2.1 Series Inductance and Resistance

Extensive effort has been reported in finding an accurate analytical expression for the self-inductance. In this work, a well-known formula suggested by Prof Thomas H.Lee's group [11] is used as shown in (Eq. 5.2)

$$L_{DC} = \frac{\mu \times n^2 \times d_{avg} \times c_1}{2} \left(\ln \left(\frac{c_2}{\delta} \right) + c_3 \times \delta + c_4 \times \delta^2 \right),$$

$$d_{avg} = \frac{OD + ID}{2},$$

$$\delta = \frac{OD - ID}{OD + ID}$$
(Eq. 5.2)

where coefficient c_1 to c_4 has the value of 1, 2.29, 0 and 0.19 respectively. The OD and ID correspond to the outer and inner diameter of the structure.

The series resistance computation is expressed in (Eq. 5.3). This formula consists of two main parts, the resistance contributed by the metallization layers and the vias. The huge amount of vias utilization in this design demands a necessity to include via resistance

Figure 5.10: The equivalent lumped circuit model for the proposed design.

Table 5.1: Technology parameters for 0.13 μm process

Parameter	Value
Silicon resistivity	10 $\Omega\text{-cm}$
Silicon thickness (h_{sil})	150 μm
Silicon dielectric constant	11.9
Top Metal thickness (T_{TM})	3.03 μm
Metal 1-5 thickness (T_M)	0.465 μm
Metal sheet resistivity (ρ_{metal})	26.55 $\text{m}\Omega\text{-}\mu\text{m}$
Inter-metal oxide thickness	0.42 μm
Eff. Inter-metal dielectric constant	4.2
Eff. Via sheet resistance (ρ_{via})	90 $\text{m}\Omega/\mu\text{m}$
Metal Vert. plate-plate separation ($h_{(metal-f-f)}$)	3.038 μm
Top Metal - Silicon distance ($h_{(TM-Sil)}$)	6.595 μm
Metal 2 - Silicon distance ($h_{(TM-4-Sil)}$)	1.593 μm

in the ohmic calculation. The technology parameters of the Chartered Semiconductor Manufacturing's 0.13 μm process are summarized in Table 5.1.

$$\begin{aligned}
R_{DC} = & \rho_{metal} \times \frac{l_{length}}{2(w_{width} \times t_{TM_thickness})} + \\
& \rho_{metal} \times \frac{l_{length}}{2(w_{width} \times t_{TM-4_thickness})} + \\
& \rho_{via} \times t_{via_height}
\end{aligned} \tag{Eq. 5.3}$$

Fig. 5.10 shows two series L-R branches to model the skin and proximity effects. An analytical equation is suggested in [93]. However, for SPICE simplicity, Gao *et. al.* has reported using a semi-empirical equation to compute the ladder elements shown in (Eq. 5.4) [12].

$$\begin{aligned}
R_{ser-pri-a,b} &= K_{Rp} \times R_{par-pri-a,b}, \\
L_{pri-a-2,pri-b-2} &= K_{Lp} \times L_{pri-a-1,pri-b-1}, \\
R_{par-pri-a} &= R_{par-pri-b} = (1 + (1/K_{Rp})) \times R_{DC}/2, \\
L_{pri-a-1} &= L_{pri-b-1} \\
&= L_{DC}/[2 + 2K_{Lp} \times (1 + K_{Rp})^{-2}]
\end{aligned} \tag{Eq. 5.4}$$

The semi-empirical coefficients K_{Rp} and K_{Lp} are held constant for this work, e.g., $K_{Rp}=1.1$ and $K_{Lp}=0.3$.

The k term indicates the strength of the magnetic coupling between the primary and secondary coils. The use of SiO_x as the isolation median instead of Ferro-magnetic material results in finite magnetic losses. The relationship between the k factor and the fabrication parameters can be rather complicated. Alternatively, [15] and [16] proposed a closed-form k expression based on the layout parameters. However, those suggested equations are based on unilateral coupling that underestimate the capability of this novel design. Therefore, a semi-empirical geometries-based equation proposed by Mohan *et. al.*, expressing the k term as a function of the layout offset is applied in this work [17]. The d_s suggested are modified to take into account the vertical separation between the primary and secondary coil as shown in (Eq. 5.5).

$$k = 0.9 - \left(\frac{d_s}{d_{avg}} \right) \quad (\text{Eq. 5.5})$$

where $d_s = \sqrt{(\Delta x)^2 + (\Delta y)^2 + (\Delta h)^2}$. In this proposed design Δx and Δy are zero as the two windings does not offset in x and y axis. Thus, it can be simplified as $d_s = \Delta h$.

5.2.2.2 Parasitic capacitances

Beneath the device's lowest metal, there is a series of oxide layers before the silicon-oxide interface. This is described as a parasitic capacitance in the lumped circuit model. For a passive device, the coplanar dimensions are much larger than the oxide thickness. Hence, the oxide capacitance is proportional to the total area occupied by the device (Eq. 5.6).

$$Area = 8 \times \tan 22.5^\circ \left(\left(\frac{OD}{2} \right)^2 - \left(\frac{ID}{2} \right)^2 \right), \quad (\text{Eq. 5.6})$$

$$C_{ox-pri,ox-sec} = \frac{\varepsilon_0 \times \varepsilon_r \times Area}{2 \times t_{TM-4-Sil}} \quad (\text{Eq. 5.7})$$

Figure 5.11: Cross sectional view of the fully symmetrical transformer showing multi-directional electrical coupling.

Fig. 5.5 shows that $\sim 80\%$ of the trace is part of the main octagonal block. Therefore, the distribution of the oxide capacitance can be expressed as $C_{ox,P1} = C_{ox,P3} = C_{ox,P2} = C_{ox,P3} = 0.1 \times C_{ox-pri}$. Whereas $C_{ox-ctr-1} = C_{ox-ctr-2} = 0.8 \times C_{ox-pri}$.

The C_{PP} and C_{center} modeling in this design is slightly different from the conventional transformer. The proposed design's electrical capacitive coupling from one winding to another involves both the vertical and lateral axes as shown in Fig. 5.11.

The total vertical overlapping and horizontal length is geometrically computed by

$$\begin{aligned}
 l_{vertical} &= 8 \times \tan(22.5^\circ) \times \\
 &\quad \left(\sum_{i=1}^{i=N} ID + (2 \times i - 1) \times W + 2 \times (i - 1) \cdot S \right), \\
 l_{horizontal} &= 8 \times \tan(22.5^\circ) \times \\
 &\quad \left(\sum_{i=1}^{i=N} ID + 2 \times i \times W + \frac{(2 \times i - 1) \times S}{2} \right)
 \end{aligned} \tag{Eq. 5.8}$$

Subsequently, the overall port-oxide-port capacitance can be derived by substituting the length into the general capacitance equation (Eq. 3.2). The overall port-oxide-port capacitance is distributed across the lumped circuit model with minimum fitting coefficient. i.e. $C_{pp,P1-2} = C_{pp,P3-4} = 0.1 \times C_{pp-overall}$, $C_{center} = 0.2 \times C_{pp-overall}$ and $C_{pp,P2-3} = C_{pp,P1-4} = 0.3 \times C_{pp-overall}$.

The components $C_{pp,P1-sec_ctr}$, $C_{pp,P2-pri_ctr}$, $C_{pp,P3-sec_ctr}$ and $C_{pp,P4-pri_ctr}$ are introduced to model the inter-quadrants electrical coupling. However, the derivation is rather complicated. Therefore, an optimization process has been performed on these components using Agilent Advanced Design System (ADS) to identify its value. In order to lower the dynamic range for optimization, all these capacitance are set to be equal since this is a fully symmetrical design.

5.2.2.3 Substrate network

The capacitance C_{sub} models the parasitic capacitive effect between the device and the substrate. The area equation based on device's layout parameters (Eq. 5.6) is calculated using (Eq. 5.9).

$$C_{sub} = \frac{2 \times \varepsilon_0 \times \varepsilon_r \times Area}{h_{sil}} \quad (\text{Eq. 5.9})$$

For the ohmic losses in the substrate, [19] suggested an analytical layout parameter-based equation.

$$R_{sub} = \frac{1}{\pi \times \sigma_{sub} \times l_{mean}} \times \ln \left[2 \times \coth \left(\frac{\pi \times (W_{dev} + 6 \times h_{TM-4} - S_{il} + T_M)}{8 \times h_{sil}} \right) \right] \quad (\text{Eq. 5.10})$$

where $W_{dev} = (OD - ID)/2$, which represent the complete width of the coil. And $l_{mean} = 8 \times \tan(22.5^\circ) \times d_{avg}$ that is the mean perimeter of the device. All the component values are optimized using ADS optimization tools as shown in Table 5.2. The variation of the optimization is kept to be $< 1\%$ so as to maintain the credibility of all the proposed semi-empirical equations.

For consistency, the model is verified using the exact measurement setup in Chapter 5.1: Agilent E8364B PNA Network Analyzer and Physical Layer Test System (PLTS) on Cascade S300 probe station. G-S-G-S-G type of Infinity probes (pitch 100 μm) are carefully calibrated using SOLR (short, open, load, reciprocal thru) on Impedance Standard

Table 5.2: Components value for the proposed design

Component	Measured value	Computed value	Optimized value
L_{DC-pri}	2.933 nH	2.999 nH	2.999 nH
L_{DC-sec}	2.933 nH	2.999 nH	2.999 nH
R_{DC-pri}	10.074 Ω	9.907 Ω	9.907 Ω
R_{DC-sec}	10.074 Ω	9.907 Ω	9.907 Ω
$C_{pp-overall}$	-	349.23 fF	350 fF
C_{ox-pri}	-	176.69 fF	176.69 fF
C_{sub}	-	18.156 fF	18 fF
R_{sub}	-	522.78 Ω	530 Ω
$C_{pp,P1-secctr}$	-	-	3 fF
k	0.86	0.86	0.86

Substrate (ISS:129-239) so as to ensure no measurement errors are brought over to the device data. Additional calibration data are plotted in Fig. 5.12 and 5.13 that show the transmission and reflection power of the *through* structure with 2 ps delay found in the ISS. The results has demonstrated that the calibration is well performed with minimum transmission loss (≈ 0 dB, refer to Fig. 5.12) and excellent noise floor (< -60 dB, refer to Fig. 5.13).

Good agreement between the modeled and measured parameters (S-parameters and Figure-of-merits) of the device has been achieved. Details measurement techniques and extraction procedure are depicted in Fig. 5.14.

5.2.3 Existing Transformer Design

The existing transformer designs are studied in this section prior to their performance evaluation. Fig. 5.15(a-c) illustrate the interleaved, stacked and differential inductor configurations, respectively. Each figure comes with the silicon die photo based on Chartered Semiconductor Manufacturing's $0.13\mu\text{m}$ process. In this work, all the configurations will be standardized to octagonal shape. The closest approximation to a circle is an octagon, which does not violate any design rule.

Figure 5.12: Transmission power of the 2 ps delay through line.

Figure 5.13: Reflection power of the 2 ps delay through line.

Figure 5.14: Flowchart of the measurement and extraction process.

Figure 5.15: 3D view of the (a)interleave transformer, (b)stacked transformer and (c)differential inductor configuration with their respective $0.13\mu\text{m}$ silicon die photo.

Figure 5.16: The inductance plot of the various transformer configurations.

5.2.4 Silicon Area efficiency

To conduct a study on the area efficiency of various configurations, the inductance has been identified as a reference figure-of-merit (Eq. 5.11). All the designs are drawn to achieve individual coil inductance of $\sim 3\text{-}3.5\text{ nH}$ as displayed in Fig. 5.16. The geometry parameters are tabulated in Table 5.3 with the silicon area normalized to the smallest device size (stacked and fully symmetrical design).

$$L_p = \frac{\text{imag}(1/Y_{11})}{2 \times \pi \times f} \quad (\text{Eq. 5.11})$$

Table 5.3 demonstrates that the interleaved and differential inductor occupied more than twice the silicon area as compared to the stacked or the fully symmetrical transformer. Therefore, in order to perform a fair evaluation, these transformers with the smallest silicon area are chosen to be the suitable candidates.

Table 5.3: Layout parameters of the various transformers

Design	ID (μm)	W (μm)	N	OD (μm)	$Area$ (μm^2)	$Norm$ $Area$
Interleaved	100	6	4	238	469.25	2.06
Stacked	100	6	4	160	228.28	1
Differential	100	15	6	310	796.12	3.49
Fully symmetrical	100	6	4	160	228.28	1

5.2.5 Stacked VS Fully symmetrical

Stacked and fully symmetrical transformer with the same silicon area of $228.28 \mu m^2$ have been tested. The quality factor, inductance, coupling coefficient, and S21 between the two transformers are compared and discussed in the following subsection. The proposed equivalent lumped circuit model is also tested against the measured silicon data to demonstrate the ability to achieve good agreement.

5.2.6 Results and Discussion

5.2.6.1 Q-factor and Self-resonant frequency

The individual Q-factors illustrated in Fig. 5.17 is extracted from (Eq. 5.12). During this extraction, the coil of no interest will be isolated (unconnected) so as not to affect the extracted data. i.e. while extracting for Q_{pri} , device's terminal P1 and P3 will be connected to Port 1 and Port 2 leaving terminal P2 and P4 unconnected; the same method applies for Q_{sec} extraction (refer to Fig. 5.14).

$$Q_{pri,sec} = \frac{imag(1/Y_{11})}{real(1/Y_{11})} \quad (\text{Eq. 5.12})$$

The outcome for the FST1, in term of Q-factor, does not show any advantage as compared to the primary (topmost) coil of the stacked transformer, it does exhibit excellent symmetry between the two windings. In fact, the resulting lower individual Q-factor for the proposed transformer is due to the mixture of multiple thick and thin metal quadrants. Thinner metal layers (t) has higher ohmic losses as shown in (Eq. 5.13).

Figure 5.17: The quality factor plot of the stacked and FST1 design.

$$R = \rho \times \frac{\text{length}}{\text{width} \times \text{thickness}} \quad (\text{Eq. 5.13})$$

For the same reason, the stacked transformer's secondary winding demonstrates a much lower quality factor of <4 . The data has clearly shown that the stacked's primary winding is able to achieve high quality factor, its secondary winding exhibits a much poorer asymmetrical performance. This asymmetry will cause degradation in the circuit performance, especially for a differentially driven design. Majority of the practical RF circuits require inductors / transformers to have a higher Q-factor, but there are certain parts of the circuit that do not really require high Q-factor. i.e. see Fig. 5.1(a) [88] - the drain inductors and source inductors can be replaced by fully symmetrical transformer configured as differential inductors as this portion of the design demands the device to be fully symmetrical instead of having higher Q-factor.

Nonetheless, it is still plausible to mitigate the low Q-factor drawback faced by the proposed design using physical layout optimization. The top metal is having a thickness of $3.03\mu\text{m}$ that is more than six times thicker than the lower layers ($0.465\mu\text{m}$). By increasing the thickness of the bottom layer that is formed by via-connected multiple layers of lower metal, the effective real term of the coil's impedance $\text{real}(1/Y_{11})$ will decrease. To justify this argument, simulation has been performed using Ansoft HFSS (High Frequency Structure Simulator). The HFSS simulation profile is calibrated to the Chartered's $0.13\mu\text{m}$ technology so as to ensure that the results obtained are credible. The calibrated HFSS has demonstrated an excellent matching on the comparison of the simulated ordinary FST1 design (FS - 1 X $0.465\mu\text{m}$ metal layer thickness) and the stacked design with its measured silicon data as shown in Fig. 5.18. The 3D view of the FST1 design with via-connected 3 lower metal layer is illustrated in Fig. 5.19. In Fig. 5.18, the HFSS simulation demonstrates that with the increase of the effective thickness of the lower metal layers, a higher quality factor can be achieved. The inductance plot shown in Fig. 5.20 illustrates that the Q improvement technique does not affect the DC inductance value of the device. In contrast, the self-resonant frequency of the individual coil has dropped. This reduction is attributed to the shortening of the distance between the two coils, which increases the distributed winding capacitance. (i.e. $h_{\text{before}} > h_{\text{after}}$ as displayed in Fig. 5.19). On top of that, Danesh *et. al.* has also suggested that a microstrip winding driven differentially gives a higher quality factor and broader bandwidth than a single-ended terminal [25].

The individual self resonant frequency (f_{SRF}) demonstrated by the FST1 design shows a significant improvement as compared to the stacked transformer depicted in Figs. 5.16 and 5.17. i.e. the stacked transformer's $f_{SRF} = 7.5\text{ GHz}$ and the FST1 design's $f_{SRF} = 9.5\text{ GHz}$, this increment in f_{SRF} can be attributed to the larger separation of the winding's vertical plate-to-plate distance ($h_{(\text{metal-f-f})}$). The stacked transformer is formed using TM and TM-2 whereas the new design uses TM and TM-4 layers. The increment in the separation causes an decrease in capacitance, which translates to higher f_{SRF} .

Figure 5.18: The quality factor plot of the ordinary FST1 design, stacked design and the FST1 design with via-connected 3 lower metal layer, together with the respective HFSS simulation result.

Figure 5.19: The 3D view of the FST1 design with via-connected 3 lower metal layer.

Figure 5.20: The inductance plot of the ordinary FST1 design, stacked design and the FST1 design with via-connected 3 lower metal layer, together with their respective HFSS simulation result.

In order to model the individual self resonant frequency (f_{SRF}) of the proposed design, a modification to Zhou *et. al.*'s differential self resonant frequency equation in [8] is used as shown in (Eq. 5.14). The individual self resonant frequency is extracted with the coil of no interest un-connected. This is to isolate the mutual coupling effect that causes the individual coil inductance to change. (Example: while extracting primary coil, the secondary coil is unconnected) Based on the novel inter-coil crossing method, the oxide height of each proposed winding is not constant throughout. Thus, an average oxide height (refer to (Eq. 5.15)) is needed to determine the effective oxide capacitance (C_{ox-avg}) using (Eq. 5.9).

$$f_{SRF} = \frac{1}{2 \times \pi \sqrt{L \times C_{ox-avg}}} \left(1 - \frac{R_{DC}^2 \times C_{ox-avg}}{L} \right)^{0.5}, \quad (\text{Eq. 5.14})$$

$$h_{ox-avg} = \frac{h_{TM-Sil} + h_{TM-4-Sil}}{2} \quad (\text{Eq. 5.15})$$

Based on (Eq. 5.14), the computed $f_{SRF-model}$ is 9.483 GHz and the extracted $f_{SRF-meas}$ is 9.5 GHz (see Fig. 5.17). It can be concluded that the equation is able to predict the self resonant frequency of the proposed design with less than 0.2% error.

5.2.6.2 S21 and Coupling coefficient (k)

Lastly, the most critical figure-of-merits, S21 - transmission gain and k , are addressed. Both transformers are connected in a two-port configuration to evaluate the ability to transfer power (S21) and its magnetic strength (k) from one winding to another. The schematic connection of the transformers is shown in the S21 and k extraction block of Fig. 5.14. The magnetic coupling coefficient is extracted using (Eq. 5.16). Both the S21 (dB) and k are plotted in Fig. 5.21.

$$k = \sqrt{\frac{\text{imag}(Z_{12}) \times \text{imag}(Z_{21})}{\text{imag}(Z_{11}) \times \text{imag}(Z_{22})}} \quad (\text{Eq. 5.16})$$

Figure 5.21: The S_{21} and coupling coefficient (k) plot of the stacked and FST1 designs.

These two parameters are considered the most fundamental requirements in transformer design. In Fig. 5.21, the FST1 is able to attain the same comparable transmission power as the stacked transformer, having $S_{21} < 5$ dB. However, the FST1 shows a slight improvement in the k value as compared to the stacked transformer. i.e. the stacked transformer has $k = 0.82$ and the FST1 has $k = 0.86$. The enhancement demonstrated by the novel inter-coil crossing method is not drastic as it does not allow the coils to have maximum overlapping surface area (which is needed to facilitate the quadrants crossing shown in Fig. 5.6). Nevertheless, the comparison with the stacked transformer that has the highest k value (having the largest coil overlapping surface area) ever reported demonstrates that although the proposed design does not geometrically favor its k value, it is still able to attain a comparable value with slight improvement. The above finding has proven that this unique way of connecting the coils is both electrically and magnetically effective.

5.2.6.3 Differentially driven TLT mode

In this subsection, the proposed and the stacked designs are tested in differentially driven TLT mode shown in Fig. 1.1(b). The differential data can be extracted using PLTS (as touchstone (.s2p) file) or standard single-ended to differential mode conversion method (Eq. 5.17).

$$\begin{aligned}
S_{D11} &= 0.5 \times (S_{11} - S_{21} + S_{12} - S_{22}), \\
S_{D12} &= 0.5 \times (S_{13} - S_{23} + S_{14} - S_{24}), \\
S_{D21} &= 0.5 \times (S_{31} - S_{41} + S_{32} - S_{42}), \\
S_{D22} &= 0.5 \times (S_{33} - S_{43} + S_{34} - S_{44})
\end{aligned} \tag{Eq. 5.17}$$

The differential performance (Q_d and S_{d21}) are taken using (Eq. 5.12) and plotted in Fig. 5.22. The result has shown that the proposed design is suitable for higher frequency band applications as compared to the stacked design. Based on Fig. 5.22, it shows that the stacked design's differential S_{21} rolls-off rapidly after 5 GHz and reaches its self resonant point at ≈ 8 GHz. On the other hand, the proposed design is able to attain a more gradual roll-off in its transmission loss (S_{d21}) with its self resonant frequency at 10 GHz. This is to say that the proposed design is able to achieve 2 GHz more operating frequency than the stacked design, at no additional cost. Looking into the differential Q performance plot (see Fig. 5.22), it has proven that the symmetry is an important aspect in differential application. The single-ended quality factor of the stacked's primary coil (refer to Fig. 5.17) has been reduced by its asymmetric secondary coil; Thus the stacked design has experienced a lower differential Q value shown in Fig. 5.22. On the other hand, the proposed design (with a fully symmetrical structure) has further boosted the differential Q value comparable to that of the stacked design. In general, the proposed design is expected to perform even better with a higher individual coil's Q value. This can be achieved based on the discussion in section 5.2.6.1 - (Q-factor and Self-resonant frequency).

Figure 5.22: Differential Q and S_{21} of the stacked and FST1 design in TLT mode.

5.2.6.4 Enhancement to the proposed design

The FST1 shows improvement in k value, f_{SRF} and better area efficiency. However, the transmission power (S_{21}) illustrated in Fig. 5.21 is only able to achieve a similar value to that of the stacked transformer. It is because the proposed design's primary and secondary coil vertical plate-to-plate distance has become further apart. This physical implementation reduces the electrical coupling capability. To demonstrate the ability to achieve higher transmission gain, the FST1 design has been enhanced by shifting the lower metal quadrants from TM-4 to TM-1 as shown in Fig. 5.23, the 3D view of the second proposed design (FST2). The vertical profile of the second proposed design is depicted in Fig. 5.24.

Fig. 5.23(a) and (c) present the narrowing of the inter-coil plate-to-plate distance. Fig. 5.23(b) shows the re-routed traces from the lower metal layer (TM-4) to the higher one (TM-1).

The performance parameters of the FST2 design are plotted in Fig. 5.25. It has

Figure 5.23: 3D view of the FST2 design using the top two metal layers to enhance the transmission power.

Figure 5.24: Cross sectional view of the second proposed transformer design using the top two metal layers to enhance the transmission power.

demonstrated improvement in terms of the transmission gain, up to a frequency band of 4 GHz. In Fig. 5.25, at 2 GHz, the S_{21} of the first design is -4.4 dB and the second design has a S_{21} of -3.29 dB. The high frequency response of the S_{21} starts to roll off rapidly after 4 GHz. This phenomenon is caused by the intensive electrical coupling within the coils that induced high leakage in high frequency applications. Concurrently, the plot also displays an increase in the k value. It has rose from $k_{1st} = 0.86$ to $k_{2nd} = 0.9$.

There is a trade-off point for this enhancement technique. The increase in the electrical capacitive effect results in a reduction of the individual coil self-resonant frequency (f_{SRF}) as reveal in Fig. 5.26. The FST2 design's f_{SRF} drops from 9.5 GHz, for the FST1 design, to 5.5 GHz. This is caused by the large distributed shunt capacitance that dominates the oxide-substrate capacitance.

Figure 5.25: The measured S_{21} and coupling coefficient (k) plot of the FST1 and FST2 designs.

Figure 5.26: The measured inductance of the FST1 and FST2 designs reflecting the drop in the f_{SRF} .

5.2.7 Fully Symmetrical Transformer Circuit Applications

This section demonstrates the following two circuit applications (Differential PA and LNA) where the proposed fully symmetrical transformer (FST) is used as differential inductors. These designs are able to produce comparable results and have achieved the best area efficiency ever reported using Chrt's $0.13 \mu\text{m}$ process.

5.2.7.1 A 2.45 GHz Power Amplifier Using Fully Symmetrical Transformer

For a consistent comparison, both power amplifier designs will be based on the same transistors geometry that is optimized to the same power gain of 14.9 dB. The transistors properties are displayed in Table 5.4. Fig. 5.27 shows the differential PA circuit using conventional inductor pair (from the Chartered's $0.13 \mu\text{m}$ Process Design Kit), which has a higher Q-factor of 10 (see Fig. 5.28). The total silicon area needed for 2 inductors is $566 \mu\text{m} \times 270 \mu\text{m}$.

Table 5.4: The Chartered's $0.13 \mu\text{m}$ transistors properties for the Two-stage Power Amplifiers

Transistor	No. of Finger(s)	Channel Length (μm)	Channel Width (μm)
M_{N1-4}	8	0.13	4
M_{N5-8}	12	0.13	4

Fig. 5.30 depicts the schematic drawing of the differential PA circuit using fully symmetrical transformer (FST) replacing the differential inductor. It shows that the Q-factor and the silicon area of the FST are 4.3 and $160 \mu\text{m} \times 188 \mu\text{m}$, respectively in Fig. 5.31 and 5.32.

The results for the above power amplifiers are as shown in the following Table 5.5.

The transmission gain of the two PA designs is plotted in the Fig. 5.33, showing that both of the designs having the similar performance.

The micrograph for the FST integrate power amplifier using G-S-G-S-G infinity probe is shown in Fig. 5.34

Figure 5.27: A two-stage Power Amplifier schematic using conventional two inductors as the differential inductor pair at the drain terminal.

Figure 5.28: The Quality factor of the Chrt's $0.13 \mu\text{m}$ Inductor.

Figure 5.29: The layout of two Chrt's $0.13 \mu\text{m}$ Inductors as drain differential inductor pair as shown in Fig. 5.27.

Figure 5.30: The schematic of the same Power Amplifier as shown in Fig. 5.27 with the Fully Symmetrical Transformer replacing the differential inductor pair.

Figure 5.31: The Quality factor of the Chrt's $0.13 \mu\text{m}$ Fully Symmetrical Transformer.

Figure 5.32: The layout of the Fully Symmetrical Transformer configured as drain differential inductor pair (refer to Fig. 5.30).

Figure 5.33: Transmission gain of the two PA designs shown in Fig. 5.27 and Fig. 5.30.

Figure 5.34: The micrograph of the FST integrated power amplifier design.

Table 5.5: Power amplifiers parameters and basing conditions

Design	RF Power (In)	Power (Out)	Power Gain	I_{DC}
Inductors	-14 dBm	0.821 dBm	14.821 dB	6.693 mA
FST*	-14 dBm	0.972 dBm	14.972 dB	6.108 mA

$$V_{gg1}(H) = V_{gg2}(H) = 1.2V, V_{gg1}(L) = V_{gg2}(L) = 0.5V$$

$$V_{DD1} = V_{DD2} = 1.2V$$

*Fully Symmetrical Transformer

In summary, the power amplifier with FST replacing the drain inductors is capable in reducing the total silicon area consumption by 5 times, while having the same amount power gain. On top of this advantage, the FST integrated PA design is able to reduce the overall power consumption as shown in the I_{DC} of Table 5.5. This can be attributed to the fully symmetrical property of the drain replacement, FST, as it suppress the common-mode signals much better than that of the two single-ended inductors.

5.2.7.2 Differential Low Noise Amplifier Using Fully Symmetrical Transformer

With the promising data obtained from the fabricated power amplifiers, the FST is implemented into the differential Low Noise Amplifier (LNA) as compared to the conventional two inductors design. This LNA design cascades M_{N3} and M_{N4} at the drain of M_{N1} and M_{N2} is to reduce the interaction of the tuned output with the tuned input and also to reduce the effect of M_{N1} and M_{N2} 's C_{gd} . The total node capacitance at the drain of M_{N3} and M_{N4} resonates with the inductance both to increase gain at the center frequency and simultaneously to provide an additional level of highly desirable bandpass filtering. The input and output resonances are commonly (and arbitrarily) set equal to each other but, if desired, can be offset from each other to yield a flatter and broader response. M_{N5} and M_{N6} essentially forms a current mirror with M_{N1} and M_{N2} , and the width are some fraction of M_{N1} and M_{N2} 's width to minimize the power overhead of the bias circuit. These differential LNA designs consists of six transistors with same properties as shown in Table 5.6 that are optimized for a gain of 15 dB @ 2.4 GHz.

Table 5.6: The Chartered's 0.13 μm transistors properties for the Differential Low Noise Amplifier

Transistor	No. of Finger(s)	Channel Length (μm)	Channel Width (μm)
M_{N1-2}	8	0.13	4
M_{N3-4}	12	0.13	4
M_{N5-6}	8	0.13	2

Figure 5.35: A Differential Low Noise Amplifier using conventional two inductors as the differential inductor pair at the drain terminal.

Fig. 5.35 shows the schematic drawing of a simple differential LNA design using two inductors at the M_{N3} and M_{N4} 's drain terminals. The S21 and NF of the LNA (Inductors based design) are shown in Fig. 5.36.

Similarly, the FST LNA design and its performance are illustrated in Fig. 5.37 and Fig. 5.38.

The results for the above LNAs are tabulated in the following Table 5.7.

Table 5.7: LNAs parameters and basing conditions

Design	NFmin @ 2.4GHz	S21 @ 2.4GHz	V_{DD1}	I_{DC}
Inductors	1.657 dB	15.022 dB	1.2 V	4.81 mA
FST*	1.742 dB	15.007 dB	1.2 V	4.80 mA

*Fully Symmetrical Transformer

Figure 5.36: The performance of the differential LNA with conventional drain inductors.

Figure 5.37: A Differential Low Noise Amplifier using conventional two inductors as the differential inductor pair at the drain terminal.

In general, the finding shows that the circuit performance of replacing the drain inductors with the FST is able to achieve similar NF. On the other hand, the FST implementation is able to achieve $> 50\%$ of the silicon area reduction as the passive inductors account for majority of the silicon estate area. In this section, the low Q -factor property of the FST has proven that it does not degrade the circuit performance. However, the compact structure of the FST greatly reduces the silicon area and the mutual inductance between the two coils of the FST also helps in the area reduction as larger inductance could be achieved with smaller silicon area. This is particularly important because one of the critical current market niches is the downsizing for all electronics products. Therefore, it is believed that this area efficient FST will be a good alternative to the conventional inductors in RFIC designs.

Figure 5.38: The performance of the differential LNA with FST.

Chapter 6

An High Effective Turn Ratio Monolithic Transformer

The needs for high inductive devices have been identified in tuned amplifiers and mixers with high intermediate frequencies (IFs). In these applications, high equivalent parallel resistance is required to achieve high conversion gain. The equivalent parallel resistance is governed by the product of Q -factor and inductance value ($R_p = Q * \omega L$), the Q -factor of the on-chip inductor is generally not > 10 . Thus, maximizing the inductance value is a common practice for high conversion gain design. Alireza's group has proposed a technique to create high inductance inductor and transformer [14]. However, the unit inductance ($H/\mu m^2$) of the reported transformer design is not as efficient as its inductor design. This is because the primary winding is inserted in-between the secondary winding, which degrades the secondary coil's intensive self-inductance effect.

A novel monolithic high turn ratio transformer is proposed in this portion of the dissertation. The proposed design demonstrates excellent performance in terms of area efficiency, coil impedance and inductance ratio. The design is able to achieve a large dynamic range of inductance ratio (as high as > 30), through simple design manipulation. This dedicated option offers high degree of selectivity that is important for customized RFIC designs. Detail description of the proposed design and the performance comparison between various transformers are addressed in the following sub-sections.

6.1 High Effective Turn Ratio Transformer Description

The proposed high turn ratio transformer has its concept evolved from a bundle cable as shown in Fig. 6.1. The primary coil of the proposed design forms the external conductor (A) that encloses the internal conductor (secondary coil, B) entirely. This enclosure method is expected to enhance the electrical coupling factor significantly. The proposed structure consists of two main components (i.e. Primary and Secondary) as depicted in Fig. 6.2.

Figure 6.1: The concept of the proposed HETR transformer design.

The primary component employs the inter-coil connection (ICC) that aims to reduce the winding effective inductance and resistance value. The design is not restricted by the number of ICCs used. (i.e. this proposed design uses 16 ICCs but the designer can opt to increase the number of ICCs to further lower the coil resistance or reduce the number of

Figure 6.2: 3D View of the proposed HETR transformer design.

ICCs for simplicity.) In fact, a coil with physically wide width is an ideal implementation for this concept. However, the large metal layer coverage will translate to manufacturing Chemical Mechanical Polishing (CMP) dishing issue. This is particularly crucial, as the process problem will result in poor yielding and poor device's reliability. With the use of ICC, the process problem can be addressed by keeping a distance (turn spacing) in-between the coil that is filled with SiO_2 . In Fig. 6.3b), the cross-sectional view of the proposed primary component demonstrates the best resemble of the all-round coupling concept. For the secondary component, Fig. 6.4 is extracted and expanded from Fig. 6.2 for a better pictorial explanation.

Fig. 6.4a) demonstrates a systematic way of routing that creates an intensive self-inductance effect. Instead of the conventional way of routing multiple turns per layer, the proposed technique routes the design using multiple layers per turn. For this technique to work, the proposed design must fulfill the condition that the direction of the current flow does not travel in opposite direction within the secondary component as

Figure 6.3: a) isolated primary component of the proposed HETR design and the b) Cross-sectional view of the primary component.

illustrated by the dotted line in Fig. 6.4a). This is critical, as any reverse current will result in negative self-inductance effect that substantially reduces the overall inductance. Based on this unique routing method, the degree of inductance selectivity has also been enhanced. This is because any of the intermittent segment(s) can be removed, customizing to designers needs. (i.e In Fig. 6.4b), segment 1-6 can be selectively removed for inductance optimization, without disturbing the physical structure) Together with the inner diameter (ID) and the conductor width (W) parameters, this proposed design can perform a large dynamic optimization range.

Fig. 6.5 shows the die photo of the proposed transformer design based on Chartered Semiconductor Manufacturing's $0.13\mu m$ technology node.

Figure 6.4: Expanded 3D view of the a) isolated secondary component of the proposed HETR design and the b) Cross-sectional view of the secondary component.

6.2 Result and Discussion

The following measurement and simulation data are obtained using Agilent E8364B PNA Network Analyzer, Physical Layer Test System (PLTS) and Ansoft High Frequency Structural Simulator (HFSS).

6.2.1 Inductance and Inductance ratio

The existing transformer designs are studied in this section to demonstrate that the proposed design is able to yield an excellent area efficiency, for a specific area (160 by $160 \mu m^2$). Fig. 6.6 illustrates the die photos of the a) stacked and b) interleaved transformer configurations. Alireza's design has been constructed using EM simulator (HFSS), which are calibrated to 0.13μ technology node, for comparison as shown in

Figure 6.5: The die photo of the proposed HETR transformer design.

Figure 6.6: The die photo of the a) Stacked and b) Interleaved configuration.

Fig. 6.7. In this work, all the configurations will be standardized to octagonal shape. From the manufacturer's point of view, octagonal shape is a polygonal shape that is of a form closest to a circle, which does not validate any design rule. The inductance of the respectively design is extracted (Eq. 6.1) and tabulated in Table 6.1.

$$L_p = \frac{\text{imag}(1/Y_{11})}{2 * \pi * f} \quad (\text{Eq. 6.1})$$

Figure 6.7: The 3D view of Alireza's design.

Table 6.1: Largest inductance of the various transformer design

Design	Inductance (nH)	Unit Inductance ($H/\mu m^2$)
Stacked Transformer	3.295	$0.1287p$
Interleaved Transformer	0.91	$0.0355p$
Alireza's Design	7.25	$0.2832p$
Proposed HETR Transformer	8.07	$0.3152p$

Figure 6.8: The inductance plot of the proposed HETR transformer design.

In the last column of Table 6.1, the inductance per unit silicon area shows that the proposed design has the best area efficiency among the 4 structures. Certainly, this design can be doubled up as a monolithic RF choke implementation.

6.2.2 Inductance of the proposed design

The inductance plot of the proposed design's primary and secondary coil is shown in Fig. 6.8. The inductance ratio for this proposed design is $L_{\text{Sec}}/L_{\text{Pri}} = 33.625$. In fact, the true formula for the turn ratio is (Eq. 6.2). Thus, the effective turn ratio of the proposed design should be $\sqrt{33.625} = 5.8$.

$$\text{Turn Ratio} = \sqrt{\frac{L_{\text{sec}}}{L_{\text{pri}}}} \quad (\text{Eq. 6.2})$$

6.2.3 Impedance of the proposed design

The real impedance plot of the proposed transformer is extracted from (Eq. 6.3) and illustrated in Fig. 6.9. The ICCs described in Fig. 6.2 has widened the overall conductor width of the primary coil. The inter-layers (vias) that aids in forming the hollow primary component (Fig. 6.3b)) have also increased the effective thickness of the coil. Based on the simplest sheet resistance formula (Eq. 6.4), the increment in the effective conductor width and thickness, reduces the parasitic resistance significantly. As a result, the measured series resistances of the primary coil shown in Fig. 6.9 display a much smaller value than the secondary coil.

Based on the Table 6.2, the main contributor to the parasitic resistance for the secondary coil is layer 2 to layer 5 (i.e. TM-4 to TM-1), which has the thinnest dimension. With this knowledge, the designers can remove any undesirable segment(s) (reducing the overall *length* of the conductor in (Eq. 6.4) to optimize the device's parasitic resistance to his requirement. The measured impedance ratio of the high turn ratio transformer is $\sqrt{|Z_{\text{sec}}|/|Z_{\text{pri}}|} = 60.177$.

$$Z = \text{real}(1/Y_{11}) \quad (\text{Eq. 6.3})$$

$$R = \rho * \frac{\text{length}}{\text{width} * \text{thickness}} \quad (\text{Eq. 6.4})$$

Table 6.2: The back-end vertical metallization profile of the 0.13 μm technology node

Layers	Thickness (μm)
Top Metal	3.03
Top Via	0.6
Metal 2-5	0.465
Via 1-4	0.42
Metal 1	0.34

Figure 6.9: The real term of the input impedance of the proposed HETR transformer.

6.2.4 Individual coil Q -factor

On the other hand, the drawback of the secondary coil high parasitic resistance value is the degradation of the quality factor as depicted in Fig. 6.10. The reported individual Q -factor plot is extracted based on (Eq. 6.5). The measured peak Q -factors are $9.05@1.5GHz$ and $2.15@1.7GHz$ for primary and secondary coil, respectively.

$$Q = \frac{\text{imag}(1/Y_{11})}{\text{real}(1/Y_{11})} \quad (\text{Eq. 6.5})$$

6.2.5 Coupling Coefficient (k)

The magnetic coupling coefficient (k) of the HETR design is extracted using (Eq. 6.6) under 2-port configuration shown in Fig. 6.11.

$$k = \sqrt{\frac{\text{imag}(Z_{12}) * \text{imag}(Z_{21})}{\text{imag}(Z_{11}) * \text{imag}(Z_{22})}} \quad (\text{Eq. 6.6})$$

Figure 6.10: The Q -factor plot of the proposed transformer design.

Figure 6.11: The 2-port schematic drawing of the transformer design.

Figure 6.12: The k -plot of the proposed transformer design.

The extracted k -plot is shown in Fig. 6.12. The k value at low frequency is ≈ 0.67 that is considered relatively high for a high turn ratio transformer design. In order to realize a transformer with $k = 1$, Ferro-magnetic material (i.e. Iron, Nickel, etc.) is required to minimize magnetic losses. In this work, the low k -value is attributed to the SiO_2 base isolation layer that surrounds the two conductors. However replacing the SiO_2 layers with the Ferro-magnetic material will not resolve the problem. In fact, it will result in process integration issues such as etching/trenching non-uniformity, unpredictable silicide formation and substantial defect density) Although fabricating an ideal $k = 1$ on-chip transformer is not feasible using standard foundry processes, a cost-free close to ideal ($k \approx 1$) highly efficient monolithic transformer has been reported in Chapter 5 by the authors.

6.2.6 Performance comparison between Alireza's design and HETR design

To ensure that the proposed HETR transformer is efficient, a comparison between the proposed design and the design that best resemble (Alireza's design) the proposed structure has to be studied. Based on the simulation structure setup shown in Fig. 6.7, the device performance for the two designs (Alireza and HETR) are tested and compared in the following sub-section.

6.2.6.1 Inductance

The inductance of Alireza's design are extracted using similar equation as the HETR design (Eq. 6.1) and shown in Fig. 6.13. In order to fulfill the high inductive secondary coil inductance, the lowest value achievable by the Alireza's primary coil inductance is $0.32nH$. This value is 54.59% larger than the proposed HETR design, which results in a smaller effective turn ratio. ($\sqrt{22.656} = 4.76$) The constriction that limits the lowest value of the primary inductance is the large inner core diameter ($100\mu m$). This value is needed to achieve $\approx 8nH$ for the secondary coil inductance.

However, based on the Fig. 6.13, Alireza's design demonstrates a higher self-resonant frequency as compared to the proposed HETR design. (i.e. Alireza's primary coil f_{SRF} is at 5.5 GHz and proposed HETR is at 4.8 GHz.) The smaller self-resonant frequency of the proposed HETR transformer can be attributed to the increment of the overall coil-to-coil electrical coupling surface area (cause by the all round coupling effect). This increment can be translated to the increase of the device winding capacitance.

6.2.6.2 Q -factor

The comparisons of the Individual coil Q -factor are illustrated in Fig. 6.14 and Fig. 6.15.

In Fig. 6.14, the proposed MT design yields a better Q -factor than the Alireza's design. This effect can be analyzed as the low series parasitic resistance for the MT's

Figure 6.13: The inductance plot of the Alireza transformer design.

Figure 6.14: The Q -factor plot of the Primary Coil for the MT and Alireza's transformer design.

Figure 6.15: The Q -factor plot of the Secondary Coil for the MT and Alireza's transformer design.

primary coil, with the help of *ICCs*. Comparatively, the Alireza's design does not have mediums that help to achieve high effective width that is inversely proportional to the parasitic resistance. In contrast, the Secondary coil's Q -factor plot shown in Fig. 6.15 demonstrates that the MT's Q -factor is more inferior as compared to Alireza's design. This can be explained with the extensive involvement of the vias from various metal layers.

6.3 Inductance Synthesizer

The inductance ratio proposed in this work offers a large optimization range. To further enhance the significance of this work, an *Inductance Synthesizer* that is compatible with most of the SPICE simulators is proposed here.

6.3.1 Inductance Calculation

Up to date extensive effort has been spent in finding an accurate analytical expression for the self-inductance. In this work, a well-known formula suggested by Prof Thomas H.Lee's group [11] has been modified as shown in (Eq. 6.7). This modification takes into account the unconventional routing method proposed in this design. The number of turns (N) for this design is not equal to the number of physical winding, as compared to that shown in [11]. This is because the routing is spanned in both lateral and transverse axes. Therefore, N_{phys} is introduced to describe this phenomenon:

$$\begin{aligned}
 L_{Comp} &= \frac{\mu \times N_{phys}^2 \times D_{avg} \times c_1}{2} \left(\ln \left(\frac{c_2}{\rho} \right) + (c_3 \times \rho^2) \right), \\
 D_{avg} &= \frac{OD + ID}{2}, \\
 \rho &= \frac{OD - ID}{OD + ID}, \\
 OD &= ID + 2 \times NW + 2 \times S(N - 1), \\
 N_{phys} &= v \times \chi \times 3(N - 1)
 \end{aligned} \tag{Eq. 6.7}$$

where N is the turn of the secondary coil based on planar perspective and S is the spacing between the coils that is fixed at $2 \mu\text{m}$ for this implementation. D_{avg} is the average diameter, OD is the outer diameter and ID is the inner diameter of the design. c_1 , c_2 and c_3 are geometry constants that are kept at 1.09, 2.29 and 0.19, respectively. χ is a variable created to describe the multi-layer per turn routing that is discussed in the previous section, it takes a value of 3 for the initial condition. And in this work, χ is limited to a maximum value of 3, implying that these expressions are based on three vertical metal stack layers. Please see Fig. 6.4; Where each pair formed by metallization layers 1 & 4, 2 & 5 and 3 & 6. v is the numerical representation of the distance that does not contribute to the self-inductance of the coil. It can be translated to $\approx 10\%$ of the winding that is used to realize the underpasses and overpasses so v is held at a constant of 0.9.

6.3.2 Synthesis Procedure

The synthesis procedure is as follows:

- (i) User defines the desired inductance value (L_{des}).
- (ii) Assume $W = W_{min} = 6\mu m$, $N = N_{min} = 1$, $S = 2\mu m$, $ID = ID_{min} = 100\mu m$.
- (iii) The L_{Comp} is computed based on (Eq. 6.7).
- (iv) The computed L_{Comp} is compared with L_{des} to determine the error term (Eq. 6.8).

$$err = \frac{L_{des} - L_{Comp}}{L_{des}} \times 100\% \quad (\text{Eq. 6.8})$$

Go to step v.), if $err > 5\%$,

Go to step vi), if $err \leq |5|\%$.

- (v) For $err > 30\%$, increase N with steps of 1,
 For $7\% < err \leq 30\%$, increase ID with steps of $10\mu m$,
 For $5\% < err \leq 7\%$, increase W with steps of $1\mu m$,
 *For $-30\% < err < -20\%$, decrease χ with steps of 1,
 (*After decreasing χ , reset W to the initial value.)
 Update the N, ID and W values and go to step 3).
- (vi) Iteration is terminated and the geometry variables N, ID, χ , and W are output for layout generation.

The flow chart of the synthesis procedure is illustrated in Fig. 6.16.

The Inductance Synthesizer kit is generally highly compatible across different technology nodes. This is because there are no process-based parameters in the synthesizing equations and also in the synthesizing flow chart (Please refer to Eq. 6.7 and Fig. 6.16).

Figure 6.16: The flow chart of the HETR Inductance Synthesis procedure.

Table 6.3: HETR Synthesis table based on (Eq. 6.7)

S/N	L_{des}	L_{Comp}	err	N	χ	ID	W	CS view ¹ <div> <div>Primary Coil</div> <div>Secondary Coil</div> </div>
1.	8.0 nH	7.942 nH	0.72%	2	3	100 μm	6 μm	
2.	12.3 nH	12.0 nH	2.46%	3	1	120 μm	7 μm	
3.	15.7 nH	15.66 nH	0.25%	3	2	120 μm	8 μm	
4.	20.0 nH	20.04 nH	-0.22%	4	1	100 μm	9 μm	
5.	21.5 nH	21.499 nH	0.007%	4	1	110 μm	6 μm	
6.	33.8 nH	33.76 nH	0.132%	4	3	120 μm	6 μm	
7.	55.0 nH	54.61 nH	0.701%	6	2	100 μm	8 μm	

¹ CS - Cross-sectional view of the HETR transformer at γ plane shown in Fig. 6.17.

However, depending on the materials used, devices' design and layout geometries, some parameters such as dielectric permittivity ϵ_r , metal resistivity ρ and metal conductivity σ , metal-to-metal spacing and metal thickness must be changed according to the process and design rules requirements. Nevertheless, these changes do not affect the equation formation and engine developed in this thesis.

6.3.3 Synthesis Examples

Based on the above procedure, a set of examples are tested using the flow chart shown in Fig. 6.16. The synthesis table is generated using a dynamic range of possible inductance values (Table 6.3). The geometry notations of the HETR transformer are displayed in Fig. 6.17.

Figure 6.17: The HETR transformer parameters for Table 6.3.

The synthesis data in Table 6.3 has demonstrated the excellent correlation between the desired inductance and the computed value. To increase the confidence level of

Figure 6.18: The HFSS 3D view of the 3 selected structures from Table 6.3

the synthesizer, three structures are chosen from Table 6.3 for HFSS simulation, based on calibrated Chartered's $0.13\mu\text{m}$ profile. The 3D views of these three structures are depicted in Fig. 6.18 as well.

The results show that the dimensions generated from the synthesizer are able to achieve less than 2% deviation from the desired inductance value as described in Table 6.4.

In summary, an area-efficient high turn ratio transformer has been developed. Based on the area comparison with the existing transformers, this new design is able to achieve higher inductance per unit silicon area. Thus, manufacturing a monolithic RF choke using minimum area is hereby feasible. The conceptual features of the design have been

Table 6.4: Comparison of the desired inductance L_{des} and the simulation inductance L_{sim} for the 3 selected structures

Design	L_{des}	L_{sim}	Deviation
1.	8.0 nH	8.02 nH	0.25%
5.	21.5 nH	21.58 nH	0.37%
7.	55.0 nH	54.23 nH	1.4%

investigated and confirmed with the measured silicon data. It can be concluded that a high inductance and impedance ratio transformer have been realized on silicon. A set of expressions for the inductance value has been introduced to describe the unique routing method of the proposed design. In addition, the novel transformer configuration has also offered a wider inductance optimization range. This has been proven by the proposed synthesizer that yields less than 3% error for a wide range of inductance value, based on the proposed equations.

Chapter 7

Conclusions

In this thesis, the design and modeling of the on-chip transformers are thoroughly carried out. This chapter summarizes the major contributions of this work and identifies the areas that merit future study.

7.1 Major Contributions of the Thesis

Chapter 3

For the stacked inductor a novel model configuration that is based on RLC elements is presented. The proposed model can predict the stacked inductor behaviour based on a 4-port circuit design with semi-empirical derivation. The modified R_S formulae are implemented accurately to predict the series resistance of the stacked inductor. The verification has been carried out using a mature technology process ($0.18\mu\text{m}$) to fabricate stacked inductors with various sizes and types. The predicted and measured S-parameter results show excellent correlation in terms of performance for frequencies up to 15 GHz . A high-Q on chip active inductor is demonstrated using a multiple-turns stacked inductor.

Chapter 4

The effect of the layout parameters on the performance of monolithic stacked transformers is investigated through on-wafer measurement of several structures based on Chartered

Semiconductor Manufacturing's 0.18 μ m Industrial Compatible process. A fully scalable model based on geometric parameters is developed. It demonstrates that the increase of the transformer silicon area can be used to enhance the magnetic coupling coefficient at the expense of large substrate electrical coupling, which degrades the self-resonant frequency. The proposed scalable lumped-element circuit and its closed-form expressions have also proven to be able to produce $< 7\%$ error compared to the measured values of the S-parameters, coil inductance, coil resistance, and magnetic coupling coefficient.

Chapter 5

Novel on-chip transformer configurations that give nearly identical inductor pairs, higher individual coil self-resonant frequency, and good area efficiency are presented. This technique involves the unique way of interdigitizing the transformer's primary and secondary coil using multiple metallization layers. A symmetrical transformer configuration with minimum die size (close to 100%) is demonstrated. Thus, an area efficient 1:1 transformer with higher self-resonant frequency (from $f_{SRF(Stacked)} = 7.5GHz$ to $f_{SRF(Sym)} = 9.3GHz$) has been realized for high frequency CMOS applications. Of all the existing transformer structures reported, the stacked design has been selected for performance comparison (i.e. Single-ended and differential Quality factor, self-resonant frequency, coupling coefficient, input impedance, and inductance) with the proposed symmetrical design. The designs have been silicon proven on a 2-stage PA and LNA designs. The designs with the proposed transformer are able to reduce the silicon area by more than 50% as compared to the ones with the inductor pair with similar performance parameters. The method presented is fully compatible with standard CMOS foundry processes.

Chapter 6

Finally, a novel way of manufacturing an on-chip transformer that produces high inductance ratio ($L_{Sec}/L_{Pri} > 30$) with excellent area efficiency is presented. This technique

uses an electrical coupling effect of a conductor A (Primary Coil), having large effective width, and a densely routed conductor B (Secondary Coil). Thus, a high turn ratio monolithic transformer, using minimum die size, is realizable on silicon. The coil having the dense routing can also be doubled up as a monolithic RF choke on silicon. The area efficiency of the design is also compared between various type of existing transformer structures (i.e. Interleaved and Stacked transformer), based on the unit inductance. In addition, the novel transformer configuration has also offered a wider inductance optimization range. This has been proven by the proposed synthesizer that yields less than 3% error for a wide range of inductance value, based on the proposed equations.

7.2 Future Work

This section identifies the topics covered in this thesis which merit more detailed study.

7.2.1 Optimized Compact Scalable Model for *FST* and *MT* designs in the leading edge node

As discussed in Chapter 5 and 6, the transformer model is only valid for a limited frequency range because of the complexity of the E- and H- field effects in the high frequency regime. As the technology advances, the Back-End-of-Line (BEOL) scheme increases significantly [1]. For example, the backend metallization layers for the 65nm technology node can have as many as twelve layers. From layout perspective, the increase in the available layers improves the flexibility of implementing these two patented monolithic designs. However, the modeling work for this implementation increases tremendously as the density of the multi-directional coupling is doubled, or even tripled. The issue of this complicated coupling needs to be addressed so as to derive the compact scalable model equations for the leading edge node. In general, to optimize the model, massive amount of silicon data is required. But it is rather time consuming and expensive to

secure the huge silicon estate area, especially for the leading edge node. On top of that, the unveiling of the model equations would also require in-depth study of the device field patterns and the structural configurations.

7.2.2 Design of the on-chip transformer for large signal applications

Ideally the transformer has only the transformation property, so it doesn't have any losses, or power limitations. Its bandwidth may seem to be infinite. However, in reality, the practical components have limited efficiency and bandwidth; and it can behave in a non-linear fashion. In conventional small-signal applications, the transformer can be treated as two individual windings coupled together with a frequency-dependent coefficient (k). The circulating electrical eddy currents induced by the magnetic fields will result in waste, heating up the transformer core. Secondly, the permeability of the silicon-based dielectric is complex at the frequencies of interest; therefore, additional power will be dissipated. The first effect is more important with low frequency power transformers. The inherent parasitic capacitances limit the upper bandwidth of operation and also reduce the transformer isolation capability. The inductance of the primary winding also limits the low frequency operation of the transformer. For small signal operation, the dielectric will not be saturated, but the transformer's performance will be limited by the low winding impedance. For large signal operation, the dielectric will saturate; and the inductance will change during the course of a voltage cycle. This causes non-linear behavior that can lead to catastrophic transformer failure. Hence, the need for a novel design of on-chip transformer from process engineering must be explored and developed. This is crucial for the realization of SoC applications with high power RF integration.

7.3 Summary

This dissertation has contributed to a better understanding of on-chip transformers. This work has provided two novel transformer designs (*FST* and *MT*), accurate geometry-based expressions for the stacked transformer, novel models for the stacked transformer, and engineering insight. All of these have significantly contributed to the design and optimization process of the monolithic transformer circuits.

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Author's Publications

1. C. C. Lim, K. S. Yeo, C. Y. Tan, K. W. Chew, J. G. Ma, M. A. Do, and L. Chan, "Equivalent circuit model of a stacked inductor for high-Q on-chip RF applications," *IEEE Proc. Circuits, Devices and Syst.*, Vol. 153, Issue 6, pp. 525–532, Dec. 2006.
2. C. C. Lim, K. S. Yeo, K. W. Chew, S. F. Lim, C. C. Boon, Qiu-ping, M. A. Do and L. Chan, "High Self-resonant and Area Efficient Monolithic Transformer using Novel Inter-coil-crossing structure for Silicon RFIC," *IEEE Electron Devices Letter*, Vol. 10 Issue 12.
3. C. C. Lim, K. W. Chew, K. S. Yeo, S. F. Lim, M. A. Do and L. Chan, "Integrated Transformer," U.S. Patent Applicat. filed no. 11/750,341, May 18, 2007. U.S. Patent Granted no. 7,570,144, August 4, 2009.
4. C. C. Lim, K. S. Yeo, K. W. Chew, C. Alper, J. Gu, S. F. Lim, C. C. Boon and M. A. Do, "Fully Symmetrical Monolithic Transformer (True 1:1) For Silicon RFIC," *IEEE Trans. Microw. Theory Tech.*, Vol. 56, No. 10, pp. 2301 – 2311, Oct. 2008.
5. C. C. Lim, K. W. Chew, K. S. Yeo, S. F. Lim, M. A. Do and L. Chan, "Effective High Turn Ratio Transformer," U.S. Patent Applicat. 11/779,892, July 19, 2007. Pending patent filing.
6. C. C. Lim, K. S. Yeo, K. W. Chew, S. F. Lim, C. C. Boon, Qiu-ping, M. A. Do and L. Chan, "An Area Efficient High Turn Ratio Monolithic Transformer For Silicon RFIC," *IEEE Radio Frequency Integrated Circuits Symp., RFIC 2008*, June 2008.

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