Physical analysis on ultrathin gate dielectric breakdown using TEM

Tang, Lei Jun

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Physical Analysis on Ultrathin Gate Dielectric Breakdown Using TEM

Tang Lei Jun

School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
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Summary

With the continuous shrinking of devices down to the nano-size regime, the thickness of gate dielectric in small size MOSFETs has unavoidably been reduced down to less than 20Å. A high gate leakage current and the intrinsic breakdown of gate dielectric are two major issues in MOSFET reliability.

(Soft breakdown) SBD was discovered when the dielectric layer has been scaled down to less than 50 Å. A high leakage current can be observed as dielectric breakdown occurs in a device, and the occurrence of dielectric breakdown will degrade the performance of a device. Different from soft breakdown, hard breakdown (HBD) will cause a device to experience a catastrophic failure. Undoubtedly, the failure mechanisms of gate dielectric breakdown are one of the most important research topics in MOSFET reliability.

In the past decades, the study of gate dielectric breakdown had been based on the changes in electrical characteristics. However, as shown in this study the changes in physical structure of a device that experiences dielectric breakdown has been proven to play an important role in understanding the breakdown event.

After M.K. Radhakrishnan *et al.* ^[16] first reported the discovery of gate dielectric breakdown induced physical damages in 33 Å small size transistors, a series of research works have been further carried out.

In this project, the mechanism of Dielectric Breakdown Induced Epitaxy (DBIE) growth and its effects on the performance of a small size transistor have been further studied. In this research, we focus on studying the dielectric breakdown of 20 Å SiO_xN_y gate dielectric transistors since this gate dielectric technology has been widely used in the current technology node. In the first part, we analyzed the relationship between the electrical characteristics and physical damage of BD

devices. Three regions of breakdown, which are correlated with different types of microstructural damage that may occur during the evolution of dielectric breakdown, have been proposed. Transmission electron microscopy (TEM) results clearly show that dielectric breakdown in 20 Å SiO_xN_y gate dielectric transistors is associated with DBIEs. This also confirms the earlier findings that DBIE acts as one of the dominant factors in dielectric breakdown. Moreover, a successive constant voltage stressing (SCVS) has been developed in this project. Based on the TEM results, the impacts of DBIE growth and percolation path dilation have been differentiated. On the other hand, the evolution of BD location has been clearly observed in the SCVS method. It is believed that the effects of BD location act as one of the crucial factors in determining the performance of post-BD devices.

In the second part, the mechanism of DBIE growth has been described. Pyramid-like DBIE, which can be observed in most of the HBD cases, have been confirmed by TEM analysis. We also study the relationship between the BD transient and DBIE growth. Generally, the BD transient can be categorized into two different phases. The effect of DBIE on the performance of a device is dependent on the BD location. The post-BD I-V characteristics of the small size transistors may partially remain transistor-like even the poly-Si gate and the Si substrate is physically and electrically shorted by a DBIE. The polarity dependence of DBIE has been observed in both n/p MOSFETs.

Finally, we provide a sequence of dielectric hard breakdown induced microstructural damage in small size transistors. As HBD occurs, different kinds of microstructural damage, such as DBIE growth, the migration of silicide from the silicided gate and the source/drain regions (DBIM), as well as open-contact phenomenon, can be directly observed by using TEM. It was found that all the microstructural damage are highly related to the compliance current limit and BD location. This finding is useful in future circuit design.

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Chapter 1

Introduction

1.1 Introduction

This chapter provides a brief introduction to the gate dielectric breakdown (BD) study in SiO₂ base material. It covers the dominant BD theories, the motivation of the scope of the work. Finally, the general layout and organization of this thesis will be presented.

1.2 Background

SiO₂ has high resistivity ($\sim 10^{15} \Omega \text{ cm}$), excellent dielectric strength ($\sim 1 \times 10^7 \text{ V/cm}$), a large band gap (9 eV), high melting point (1713 °C) and a native, low defect density interface with Si ($\sim 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$). These properties of SiO₂ are in large part responsible for enabling the microelectronics revolution. The Si/SiO₂ interface, which forms the heart of the modern MOSFET and the building block of the integrated circuit, is arguably the world's most economically and technologically important materials interface^[1].

Aggressive scaling in microelectronics to achieve higher performance and circuit density necessitates the thinning of the SiO₂ gate dielectric. This thinning is necessary to maintain the MOSFET gate capacitance such that there is adequate drive current for proper circuit operation. Two of the most critical factors that may limit the future scaling of the thickness of SiO₂ are the gate leakage current and the intrinsic reliability of the film. The possible gate leakage has been suggested to be

between $1\text{A}/\text{cm}^2$ to $10\text{A}/\text{cm}^2$ ^[2-3]. This corresponds to an oxide thickness between $\sim 12\text{ \AA}$ to $\sim 15\text{ \AA}$ ^[3]. Ultrathin oxide dielectric breakdown shows new BD failure mechanisms compared with thick oxide. M. Depas *et al.* ^[4] reported the soft breakdown (SBD) phenomenon in less than 5nm thin gate oxide. The SBD phenomenon was explained by a decrease of the applied power during the stressing for thinner oxides, so that the thermal effects are avoided during the breakdown of the ultrathin oxide capacitor.

Based on the reports in the literature, people believe that the intrinsic dielectric breakdown can be considered as a three-stage process. First is the wear out phase, then the breakdown event itself, eventually followed by a third phase of thermal damage due to the dissipation of the energy stored in the MOS capacitor. In the presence of such a thermal damage, the event is commonly referred to as hard breakdown (HBD). In some cases, however, such thermal damage is not present and the breakdown in this case is referred to as soft breakdown. But most of researchers have agreed that soft breakdown and hard breakdown have same original triggering source, and the only difference is the energy dissipation process ^[5].

Many breakdown models have been proposed to explain the root cause of dielectric breakdown, but none of them is able to explain all the experimental data. The E model ^[6-8] was the first model proposed for dielectric breakdown. C.H. Chen ^[9-10] proposed that breakdown is function of $1/E$ instead of E . Lifetime extrapolations based on the linear E and the reciprocal $1/E$ models show large discrepancies at the lower electric field region. Both models are indistinguishable for electric fields above $9\text{MV}/\text{cm}$ for the field acceleration values and the argument is continued until now. Some other workers have tried to link the E and $1/E$ models in one complete model that separates by the field energy in the dielectric ^[11-13]. For bond strengths $< 3\text{eV}$, the bond breakage rate is generally dominated by field-enhanced thermal processes which can be described by the E model. For bond strengths $> 3\text{eV}$, the bond breakage must be hole catalyzed by current-induced hole injection and

capture^[13].

1.3 Motivation

The microstructural nature of the defects induced by gate oxide BD is still unclear. In addition, the physical analysis of the failure mechanism of Gate oxide BD is always a challenge. SBD is found to be the dominant failure mechanism for oxide with thickness less than 50Å^[14-15]. Normally, the physical analysis of the SBD failure and its associated damage are not realizable as the physical failure defects of SBD cannot be easily located and identified. Most of the breakdown phenomena are studied from the electrical point of view. Recently, Radhakrishnan *et al.*^[16] and Pey *et al.*^[17] reported that a dielectric-breakdown-induced epitaxy (DBIE) in the vicinity of gate area is associated with ultrathin gate oxide breakdown. The physical analysis results show that the DBIE is highly localized and its location is dependent on the stressing voltage polarity regardless of the compliance current and hardness of the breakdown. The suggested driving force behind the DBIE formation is thermal electromigration effect^[16-17]. It is also reported that DBIE formation is the one of the major concerns for the reliability of ultrathin gate oxide^[18]. Hence, the project aims to study the structural property of DBIE and its impact on transistor degradation during gate oxide BD.

1.4 Objective

The project involves the physical analysis of breakdown phenomenon in ultrathin SiO₂ gate dielectric using TEM and electron-energy-loss spectroscopy (EELS). Based on the physical structure analysis results obtained from single small size transistor, we aim to develop a model to explain the gate dielectric breakdown mechanism in small size transistors. Other objectives are:

- (a) To study the microstructural damage associated with Gate oxide BD under constant voltage stress (CVS) and perform systematic analysis on the physical structural change associated with breakdown hardness.

- (b) To study the impact of breakdown hardness and location on the transistor performance.
- (c) To perform TEM analysis on Gate oxide BD in small size p/n MOSFETs stressed under both inversion and accumulation in CVS mode.

1.5 Thesis Organization

This thesis is organized into 7 chapters.

Chapter 2 concentrates on literature review and summarizes the common breakdown models, breakdown induced microstructural damage, SBD and HBD effect on the performance of MOSFETs.

Chapter 3 describes the details of the experimental set-up and sample preparation. Transmission Electron Microscopy (TEM) and Electron Energy Loss Mapping working theory are briefly described.

Chapter 4 reports the BD characteristics in small size transistors. The transistor physical structural changes associated with different hardness are described in this chapter.

Chapter 5 discusses the DBIE growth mechanism and its relationship with BD location, transient and the impact on the post-BD I-V performance.

Chapter 6 describes the physical analysis on the microstructural damage of HBD devices.

Chapter 7 concludes the thesis and provides some recommendations.

Chapter 2

Literature Review

2.1 Introduction

This chapter provides an overall view of gate dielectric breakdown. A few dominant dielectric breakdown mechanisms, SBD and HBD, and different analysis methods are also discussed.

2.2 Gate oxide intrinsic breakdown Model

2.2.1 Anode hole injection model (AHI)

Anode hole injection model (AHI) was first proposed by Chen *et al.* in 1986^[9]. As shown in Fig. 2.1, a positive current at substrate is measured when the NMOSFET is stressed with a positive gate voltage, while source and drain are grounded. During acceleration electrical stressing, electrons tunnel from the cathode to anode via Fowler-Nordheim(F-N) tunneling for thick oxide dielectric layer^[19]. A positive current can be measured at the substrate. The substrate current density has the similar oxide field dependence as the F-N current density. But this substrate current is not parallel with the F-N current. The widely accepted explanation given by D.J. DiMaria *et al.*^[20], reported that the F-N tunneling electron exists at the silicon substrate/SiO₂ interface, it gives up its energy through impact ionization. Not all the F-N tunneling electrons are able to make their way to the anode. For those electrons that successfully reach the anode, they will transfer their energy (E_{gain}) to a deep valence band electron, causing a hole being injected from anode into the gate oxide.

Fig. 2.3: Schematic showing the Anode-hole injection mechanism. ^[21]

When the hole fluence reaches the cathode, it is measured as a positive substrate current J_p .

The hole current density can be related to the electron current density, J_n , as follows

$$J_p = \alpha(E_{ox}) J_n \quad \text{----- Eqn. (2.1)}$$

where $\alpha(E_{ox})$ is the field dependent hole generation efficiency. In the anode hole injection model, α is the holes percentage that follows back to the cathode. α is found to be constant in constant voltage stress ^[22], and slightly increased in constant current stress. An approximate equivalent relation to Eqn. (2.1) can hold for the integrated values of J_p and J_n , hole influence, Q_p , and the electron influence, Q_n .

$$Q_p = \alpha(E_{ox}) Q_n \quad \text{----- Eqn. (2.2)}$$

A critical $Q_{p,crit}$ value was observed by Chen *et al.* ^[9], which triggers gate oxide breakdown and has been verified by other research groups ^[7,23]. The value of $Q_{p,crit}$ was determined to be approximately $0.1C/cm^2$ and was independent of stress

conditions ^[9]. But the value of $Q_{p,crit}$ decreased for decreasing the oxide thickness ^[24]. It exhibited a temperature dependence ^[25] and was not constant under low electron injection conditions for substrate hot hole injection experiments ^[26].

In ultrathin SiO_2 , the direct tunneling proportional to the applied gate voltage is the major consideration of tunneling electrons ^[27]. The process of hole injection and subsequent trapping need the input electrons energy to be greater than 7eV ^[23,28]. This is too high carrier energy to accept anode-hole-injection model at low circuit operating voltage condition. So minority ionization of hole ^[29-30] in p-type anode material or lightly doped inverted n-type material, that would allow hole injection at low voltage, was proposed. Nicollian ^[15] also reported that bulk defect generation is significantly increased and Q_{bd} decreased for devices with lightly doped n^+ polysilicon gate electrodes in low gate voltage condition. The devices were biased to invert the polysilicon anode resulting in mechanisms that favor the injection of hole at the poly-Si/ SiO_2 interface. The holes could be injected through or over the oxide energy barrier.

2.2.2 Thermochemical Model

Thermochemical model or the E-model is the only oxide breakdown model that allows the breakdown lifetime to be predicted from the measurable quantities. The E refers to the electric field across the oxide. This applied electric field interacts with the weak Si-O-Si bonds associated with oxygen vacancies in the amorphous SiO_2 film.

Defects are generated throughout the gate oxide by the electric field that eventually breaks the weak bond and creates a permanent defects or traps ^[31-32]. These defects accumulated with time to arrive at a critical density, which triggered a sudden loss of dielectric properties. A surge of current produces a large localized rise in temperature leading to permanent structural damage in the silicon-oxide film. Fig. 2.2 shows the creation of a hole trap.

Fig. 2.4: (a) A silicon dioxide (SiO_2) network. (b) Precursor to bond breakage. (c) Hole-trap creation. ^[32]

So the thermochemical model was hypothesized based on an electric field driven defect process. When the logarithm of the time-to-failure was plotted against applied electric field, a straight line was observed, i.e., $t_{\text{BD}} \sim \exp(-\gamma E)$, where E is the electric field and γ is the electric field acceleration factor. The acceleration parameters for the electric field and temperature could be extracted from the model allowing extrapolation of oxide lifetime from accelerated stress conditions. Fig. 2.3 plots the lifetime extrapolations based on the linear E and the reciprocal $1/E$ models. Both of models give a good fit to the data for high electric fields. The long time-to-failure experimental result approximates logarithm ^[33-35].

Fig. 2.3: Lifetime extrapolations based on the liner E and reciprocal 1/E models illustrating very large discrepancies at the lower electric fields. Both models are indistinguishable for electric field above 9MV/cm for the field acceleration values. [36]

2.2.3 Anode Hydrogen Release Model @ AHR Model

Eric *et al.* proposed ^[37] that hole traps can be induced by AHI, but the hole trapping does not result in oxide breakdown. Another possible mechanism for silicon dioxide breakdown may associate with hole traps. Hydrogen released by stress is one possible mechanism ^[23,38]. Anode hydrogen release model is involving the release of atomic hydrogen form at the anode by energetic tunneling electrons ^[39-40]. Hydrogen atom can terminate the dangling bond at Si/SiO₂ interface and electrically passivate the defects. Thus, hydrogen plasma exposure creates many Si-OH and Si-H groups in oxide. Hydrogen in the oxide might cause oxide degradation by depassivating by non-elastic collision to hot electron and generating electron traps. This model postulated that electrons with sufficient energy tunnel through the gate oxide potential and reached the anode. These energetic electrons release hydrogen

(H) from the anode/gate oxide interface. The threshold voltage is approximately 5V^[39]. The process has been shown to continue at voltages as low as 1.2V^[23,41]. The released hydrogen diffuses through the gate oxide and generates electron traps in the gate oxide as shown in Fig. 2.4.

Fig. 2.4: Hot electron induced Hydrogen release mechanism.^[23]

2.3 Gate oxide soft breakdown and hard breakdown

It is generally believed that the intrinsic dielectric breakdown can be considered as a three stages process. First is the wear out phase, then the breakdown event itself, eventually followed by a third phase of thermal damage due to the dissipation of the energy stored in the MOS capacitor. In presence of such a thermal damage, the event is commonly referred to as hard breakdown. In some cases, however, such damage is not present and the breakdown in this case is referred to as soft breakdown. During scaling down of voltage, relevant reports show that ultrathin gate dielectric suffers only soft breakdown instead of hard breakdown^[42].

2.3.1 Soft breakdown

Aggressive scaling in microelectronics to achieve higher performance and circuit

density necessitates the thinning of SiO₂ gate dielectric. This thinning is necessary to maintain the MOSFET gate capacitance such that there is adequate drive current for proper circuit operation. Two of the most critical factors that may limit the future scaling of the thickness of SiO₂ are the gate leakage current and the intrinsic reliability of the film.

Soft breakdown is one of the new failure mechanisms associated with gate oxide thinning process that was first reported by Okada *et al.* ^[43] in 1994 and later by M. Depas *et. al* ^[4] in 1996 for gate oxide less 5nm. As they mentioned “the soft breakdown phenomenon corresponds to an anomalous increase of the stress induced leakage current and the occurrence of fluctuation in the current”. The soft breakdown phenomenon is explained by the decrease of the applied power during the stress for thinner oxides, so that thermal effects are avoided during the breakdown of the ultrathin oxide capacitor. Different stress voltages, temperatures, device structures and stress methodologies have been widely studied to describe the SBD mechanism ^[44-50].

The common explanation of the post breakdown conductance of BD devices has been linked with multiple traps assisted with electron tunneling mechanism in the localized small area. Lee *et al.* ^[51] proposed that SBD takes place when the injected electrons travel in the oxide conduction band ballistically causing a localized physical damage in the vicinity of the anode interface. The damaged region was then modeled as a resistance in series with a trapezoidal potential barrier of reduced thickness ^[51]. No significant variations in MOSFET I_d-V_g characteristics can be observed after SBD and therefore, for some applications, soft breakdown does not necessarily imply device failure ^[52].

Other physical models for soft breakdown include quantum point conduction model ^[53-54], variable range hopping of carrier ^[55] and percolation conductance path model ^[56-59].

2.3.1.1 Quantum Point Contact Model

In quantum point contact model (QPC), the breakdown path is modeled as a quantum wire for SBD and HBD as shown in Fig. 2.5.

Fig. 2.5: Quantized energy in point-contact model (a) SBD and (b) HBD. ^[53]

In QPC model, the conduction has formed after BD. The momentum in the direction perpendicular to propagation is quantized. SBD takes place through a potential barrier defined by $\Phi = V(E) = E_0(0) - E_F$, where $E_0(0)$ is the ground 1D subband and E_F is the Fermi level in the SBD path.

The post breakdown curve is define by

$$I = 4q/\alpha h \exp(-\alpha\Phi) \sinh[\alpha * q/2(V-V_0)] \quad \text{----- Eqn.(2.3)}$$

where h being the Planck's constant, q the electron charge, Φ is the barrier height, and the shape parameter α is related to the second derivative of $E_0(Z)$ at $Z=0$, i.e. to the change of the constriction area near the narrowest point of the SBD path.

This model has a good SBD I-V curves fitness. It points out that small variation of Φ and α will lead to exponential change in the current. Point contact model uses a common picture to explain the main features of SBD, and even for HBD.

2.3.1.2 Variable Range Hopping Model

Variable range hopping (VRH) model is a model for explanation the conduction mechanism of the "B-mode" stress induced leakage current (B-SILC), which was reported by Okada *et al.* in 1997^[55]. In ultrathin silicon dioxides, under the electrical stressing, the B-mode shift suddenly occurs at a local spot to induce the B-SILC. B-SILC shows a large leakage current fluctuation during constant voltage stressing. In the VRH conduction, the temperature dependence of the current is expressed as

$$I(T) = A \exp(-BT^{-1/4}), \quad B = 2.06(\alpha^3 K_B N)^{-1/4} \quad \text{----- Eqn.(2.4)}$$

where I is the current, T is the temperature, K_B is the Boltzmann's constant, A is a constant, and α is the decay length of the localized states.

Okada *et al.* reported that for device under stressing, the number of available localized states dynamically changed^[55]. As carriers exist at the localized states, it results in current fluctuation. These traps sites and interface states induced by stress provide useful information to the clarification of the degradation and breakdown mechanisms of silicon dioxides. The model fits the temperature dependence.

2.3.1.3 Percolation Model

In 1998, Houssa *et al.* ^[56] used a percolation model to explain gate oxide soft breakdown. As he mentioned, soft breakdown is related to a critical number of electron traps in the SiO₂ layer and at the Si/SiO₂ interface that form a percolation cluster between the electrodes of the stressed capacitor. Degraeve *et al.* ^[57-58] first reported a computer simulation of percolation approach to study breakdown in ultrathin SiO₂ layer. Later work by J.H. Stathis ^[59], who used computer simulation to link percolation model with statistic analysis (Weibull Distribution), made a completed explanation for this model.

Fig. 2.6: Schematic of a percolation model for gate oxide breakdown. ^[59]

In percolation model hypothesis, defects are objects with finite size and randomly generated in the oxide bulk. When overlapping of defects lead the formation of a conductive path, breakdown occurred. The thinner the gate oxide, the lower defect density required for breakdown to form. Weibull shape parameter (β) is experimentally observed to decrease as the oxide thickness is decreased. The experimental data show that β became small when the N_{BD} is (defect density) reduced. For gate oxide thinner than 3nm, β approaches to 1. This means only one defect can cause the breakdown ^[58-59]. Fig. 2.6 shows a schematic of a percolation path induced breakdown.

K.L. Pey *et al.* ^[18,87] expanded the percolation mode to link it with the BD local microstructural damages. It is also reported that BD induced Si epitaxy grows from the transistor cathode to the anode. In addition DBIE could be a domination effect for SBD evolution to HBD.

2.3.2 Hard breakdown

Unlike soft breakdown just created one or few leakage paths in a particular MOS dielectric layer, hard breakdown is a catastrophic damage caused by a huge thermal dissipation at breakdown time. Suñe *et al.* used a quantum point contact mechanism ^[53,54] to explain the post soft breakdown current that shows exponential characteristic and fits the power law $I=aV^b$. Hard breakdown has a linear current – voltage relationship. Lambardo *et al.* ^[60] linked hard breakdown with breakdown transient time and store energy in the breakdown capacitor. Some other groups have also related hard breakdown with store energy dissipation. They concluded that larger capacitor size is easier to cause hard breakdown ^[61-63]. M. A. Alam *et al.* ^[42] reported that the store energy has slight effect to breakdown level. They performed experiments on a large capacitor connected in series with small devices and found that the breakdowns were not much different. But most of researchers have agreed that soft breakdown and hard breakdown have same origin, and the difference is the energy dissipation process ^[63]. They also demonstrated that there is a critical energy requirement that differentiates soft breakdown and hard breakdown ^[60]. When hard breakdown occurred, the local temperature can be above the Si melting point ^[64]. If high electric field is kept, the hard breakdown location can propagate with the sound velocity from the starting point ^[64]. Lombardo reported that the breakdown transient was about few nanoseconds for 35nm gate oxide and ten of nanoseconds for 5.6nm gate oxide. The energy dissipation in BD is a strong function of BD transient. The post-BD measurement found that faster transient has larger damage ^[64]. Further analysis indicated that the BD transient is also dependent on stress voltage. Higher stress voltage on a same gate oxide thickness device leads to faster

transient. ^[65] TEM has been used to physically analyze the post breakdown microstructural change ^[64]. Abnormal epitaxial Si has been found at gate oxide breakdown dielectrics. Same post-BD phenomenon has also reported by K.L. Pey *et al.* in sub-micro nMOSFETs devices ^[16-17].

2.4 Post-BD transistor performance

As shown in the previous sections, both SBD and HBD affect the device characteristic but the damage level is different. This section concentrates on the BD effect on small transistor instead of large capacitor that has been widely used in the study of stress induced defect generation mechanism. Crupi *et al.* ^[66] studied the SBD current in ultrathin oxide device. They found that if SBD happened in large areas, the gate current is stable and independent of SBD. But for smaller area, the gate current decreases and becomes less stable. So the gate current after breakdown is area dependent. N. Yang *et al.* further reported ^[67] that the transistor source/drain extension to gate overlap regions have strong effect on the device performance in terms of both gate tunneling currents and oxide reliability. As reported, when breakdown happens at the extension area, the off-state power consumption is higher. At the same time, for smaller device structure, the breakdown has higher chance to happen at the extension area. Stress polarity also affects the breakdown hardness. In CMOS circuit, NMOS stress under positive voltage condition has the maximum damage level ^[68]. F. Crupi *et al.* have also reported similar findings ^[69]. A method as shown in Eqn.(2.6) that uses the current change after the breakdown in the source and drain was developed to locate the breakdown location.

$$S = \Delta I_d / (\Delta I_d + \Delta I_s) \quad \text{-----Eqn.(2.6)}$$

where ΔI_d is the changing current measured at drain side and ΔI_s is at the source side for a negative V_g and $V_s = V_d = V_{sub} = 0V$. Under these conditions, electrons are

injected through the breakdown path from the gate. Parameter S is uniquely related to the relative position of the breakdown position x and can be used to compare the relative position of two breakdowns.

Another interesting point of the transistor BD is that hard breakdown does not necessarily correspond to circuit failure ^[70]. Kaczer *et al.* plotted the breakdown location changes with post-BD leakage curve and confirmed that breakdown is very much location dependence ^[71]. The post-BD model and effect on post-IV curve are shown in Fig. 2.7.

Fig. 2.7: Post breakdown measurement on $L=0.2\mu\text{m}$ nFETs with hard breakdown location changed from drain to source. ^[71]

2.5 Physical analysis of gate oxide breakdown

Besides studying the electrical characteristics of breakdown devices, physical analysis have been used to study gate oxide breakdown. Transmission electron microscopy ^[65,72], photoemission microscope (PEM) ^[71,73] and conductive-atomic-force Microscopy (C-AFM) ^[74] have been reported to analyze the breakdown in gate dielectric layer. M. Porti *et al.* used ^[75] C-AFM to stress gate

oxide at nanoscale. Experiments on bare oxides show that, although BD is triggered at one point, it electrically propagates to neighbor regions. The area of breakdown is strongly affected by BD hardness and stress circuitry. The topographic information given is the advantage of the C-AFM stress method. It opens a new alternative for the study of the impact of BD on device and at circuit level.

Another method that is widely used in analyzing dielectric breakdown phenomenon is PEM. When stress induced BD in dielectric layer, a hot spot can be identified by PEM. More than one small hot spot has been proposed in big capacitor ^[76]. Electrical result on a stressed big capacitor indicated multiple SBDs in the ultrathin dielectric layer before a HBD final occurred ^[16]. The results also indicated SBD may not be the same source for HBD. But S. Bruyère *et al.* reported that using PEM analysis, a unique BD spot evolution was found to be the ultrathin dielectric breakdown mechanism ^[77].

B. Kaczer reported that the position of the breakdown spot can be independently determined from emission microscope images for $L=10\mu\text{m}$ transistors ^[71]. The PEM information directly supports Eqn. (2.6), which is important to study the effect of the breakdown location on the transistor performance.

TEM could be used in the study of dielectric BD induced microstructural damages. Lombardo *et al.* showed that Si epitaxial islands were found from 35nm thick dielectric breakdown capacitor. This is clearly indicative of a local melting produced by large power dissipated through the MOS stack. The substrate as the epitaxial growth template has emerged through the oxide up to the poly-Si surface ^[65]. At the same time, a large amount of threading dislocations has been found on the Si substrate. In addition, TEM plan-view images on 5.6nm thick dielectric capacitor showed that the breakdown has caused oxide melting. The damages aligned along the line of breakdown propagation ^[64]. Similar result has reported by Satoshi *et al.*, in transistor BD study case ^[78]. Based on the report, for a breakdown

field of 7-15MV/cm, twin planes and anode interface roughening were found in the surface region of the Si substrate. The presence of twins indicates that a Si substrate is locally molten during dielectric breakdown. These results are well explained by a local thermal breakdown model of intrinsic oxides BD.

Ti-silicide migration associated in small size transistor dielectric breakdown was first reported by M. K. Radhakrishnan *et al.* ^[16]. C.H. Tung *et al.* further reported that a “hillock” type epitaxial Si spot with size ranging from 2-100nm associated with the gate oxide breakdown failure is always found in the vicinity of the gate oxide and its formation strongly depends on the stress polarity ^[79]. The epitaxy always grows from the device cathode to anode. The size differences in dielectric breakdown induced epitaxy in small size n- and p-MOSFET are also studied by TEM ^[80].

2.6. Comparison between Constant voltage stress and constant current stress (CCS) in ultrathin gate dielectric BD

Gate oxide reliability is usually monitored with highly accelerated electrical stress. Constant voltage stress and constant current stress are the most widely used in the past decades.

When the gate oxide thickness continuous to scale, many research works have concentrated on using constant voltage stress instead of constant current stress ^[81-83]. Since thick gate dielectric has a unique relationship between the FN current density and oxide field, the charge-to-breakdown should be measured using CCS. For ultrathin oxide (<5nm), however the injected electron travel ballistically through the oxide without interacting with the SiO₂ lattice. This can be either F-N tunneling ($T_{ox} \sim 5\text{nm}-3.5\text{nm}$) or direct tunneling ($T_{ox} < 3.5\text{nm}$) ^[81]. Therefore, the electron energy at the anode is determined by the voltage difference between the cathode and the anode which corresponds to the applied gate voltage. The defect generation rate

depends only on the gate voltage, independent of substrate or gate doping ^[82].

2.7 Summary

Dielectric breakdown in the gate dielectrics of MOSFETs is a major failure issue in Si-based circuit. Regardless of soft or hard breakdown, it degrades the device and circuit performance. Several breakdown models have been used to study the gate dielectric breakdown phenomena. However none of the model is robust enough to explain all the experimental data. Gate oxide breakdown is a very complex phenomenon that needs a combination of models. Physical analysis on gate oxide breakdown is able to provide new insights. But it is also a challenge to directly analyze the device breakdown using physical analysis, especially in SBD.

Chapter 3

Experimental Setup

3.1 Introduction

In order to reveal the physical characteristics of gate oxide BD in small size transistors, TEM has been used to perform the study. This chapter describes the details of the electrical stressing method, focus ion beam (FIB) sample preparation and TEM analysis.

3.2 Electrical stress

In our experimental work, n/p MOSFETs with gate oxide thickness from 16 Å to 33 Å, fabricated with standard 0.18µm and 0.13µm CMOS technologies have been used for the study.

(a) Test wafer –C

(b) Test wafer -G

Fig. 3.1: MOSFETs used in experiments (a) single transistors connected with common ground (b) insulated single transistor structure.

Two types of test patterns, single small size transistors connected with common ground (wafer-C) and isolated single small size transistor (wafer-G), were used. The test structures are shown in Fig. 3.1(a) and (b) respectively. In order to facilitate TEM analysis, the transistors width has been limited to 0.2-0.3 μm . In this case, the final TEM membranes will have high probability of containing the BD defects for analysis.

The small size transistors were stressed by constant current stress and constant voltage stress methods. HP 4156C parameter analyzer and CASCADE low leakage probe station were used to measure and record all the electrical data. Fig. 3.2 shows the schematic of the experimental setup.

In CCS method, various stressing current densities were employed on the gate of a single transistor. The stress was immediately terminated after observing a first drop in the gate voltage. Some samples were selected for TEM analysis.

Fig. 3.2: Schematic of the experimental setup, this configuration is for stressing MOSFET under CCS in inversion mode.

As described in Chapter 2, CVS is preferred for stressing ultrathin gate oxides. In

our work, CVS was used for most of the electrical stress. In CVS method, positive or negative stress voltage was applied to the gate while the source, drain and substrate electrodes were grounded. The stress voltage is dependent on the gate dielectric thickness. Before stressing any new gate oxide, voltage ramp test was used to randomly stress several transistors in the wafer of interest. The breakdown voltage, as described in Ref. 84, has been used to determine the final stressing voltage for CVS.

Based on the experimental data, a 3.8V was selected for 20Å gate oxide dielectric to obtain a reasonable BD time and electric field (15MV/cm)^[72]. Using the similar approach, 5.1V, 4.4V and 3.4V were used for 33Å, 25Å and 16Å gate oxide, respectively^[85].

Each small size transistor was stressed at 100°C under high stress voltage in inversion or accumulation mode with a specific current compliance setting. When the gate leakage current hits the compliance current limitation, the stressing was stopped immediately. Some BD samples were selected for TEM analysis.

It is believed that the progressive BD is the dominant BD mode under operating condition in CMOS circuits^[99]. Another stressing method, successive constant voltage stress (SCVS), has been developed to study the BD induced physical damages in small size transistors. In SCVS, after each BD, the compliance current limit was relaxed to a next higher level. The post-BD transistor I-V characteristics were measured at nominal operating condition. Based on the post-IV curves, some BD transistors were selected for TEM analysis.

3.3 Sample preparation by Focus Ion Beam (FIB) method

For HRTEM analysis, the thickness of specimens needs to be less than 1000Å. In view of the very small device size and very specific BD location, only FIB technique can meet this sample preparation requirement.

FIB is a powerful equipment that has been widely used in semiconductor area and material science study. In FIB, Ga^+ ions are accelerated by a 30KV voltage. These heavy ions sputter material away from its original stack. The Ga^+ ions can also be focused and controlled very well by electric and magnetic fields in the ion beam column.

Two FIB sample preparation methods were used in the specimen preparation process. One of the methods is called pre-thin FIB sample preparation, which needs a mechanical polishing to thin the specimen down to less 30 μm . The transistor of interest is located in the middle of the thin membrane. After that, the specimen is mounted onto a copper ring to enhance the sample mechanical integrity. Then the specimen is fixed on a specific FIB sample holder. FIB is used to further thin the specimen to the location of interest from both sides of the membrane.

Lift-off sample preparation method is now a common method used for TEM sample preparation. This method uses FIB to thin the specimen from both sides of the location of interest without mechanical polishing. Fig. 3.3 shows a sequence of images of a lift-off FIB sample thinning method.

In Wafer C, the transistor structure was covered by a thick of passivation layer that needs FIB to mill it away before the real cutting (See Fig. 3.3(b)). For Wafer G, the transistor structure can be directly seen in the FIB (See Fig. 3.3(a)), Figs. 3.3(c) and (d) show a small size transistor gate was protected by depositing a layer of Pt, and then FIB milling from both sides of the gate. When the FIB milling approached the area of interest, the specimen membrane was isolated from the specimen stack by FIB cutting both sides and bottom of the membrane. The gate structure can be clearly seen in the FIB images shown in Fig. 3.3 (e) and (f). Finally, the sample membrane was picked up from the milled hole and mounted it to a copper mesh that has a very thin layer of carbon film to hold the TEM specimen.

Fig. 3.3: FIB sample preparation process. (a) FIB image of a wafer-G single transistor, (b) FIB image of a wafer-C single transistor. FIB milling has exposed the top passivation layer. (c) Pt deposition to protect the area of interest. (d) FIB thins the sample to the required thickness, and lifts it for TEM analysis. (e) FIB cross-sectional image of a transistor of wafer-G. (f) FIB cross-sectional image of a transistor of wafer-C.

3.4 TEM analysis and GIF element mapping

3.4.1 TEM image

Transmission Electron Microscopy uses transmission electrons (200KeV) to provide useful information. When a uniform electron beams incidents on an electron transparent sample, after suffering elastic and inelastic scattering, the incident electrons can transmit from the bottom side of the sample. The elastic transmission beams include the materials information that has been projected on the

screen by showing as the different contrast. At the same time, due to inelastic scattering, other useful information such as electron energy loss spectrum (EELS) can be obtained. TEM has been widely used in material science, engineering, and biological science.

Fig. 3.4: A Philips CM 200FEG TEM was used in the project.

Interface such as SiO_2/Si has been extensively studied by high resolution TEM. In this project, small size MOSFET gate dielectric BD has been analyzed by a Philips CM 200FEG TEM. Fig. 3.4 shows the instrument employed. The HRTEM liner resolution is $1.4\text{\AA}$ that is smaller than the two silicon atoms distance along the $\langle 111 \rangle$ direction ($3.135\text{\AA}$). Using the Philips TEM, the analysis of the gate oxide BD device structure can be obtained at atomic level. Thus direct and clear microstructural information of small size MOSFETs after gate oxide BD can be obtained. Because the HRTEM analysis needs the sample thickness less than one thousand angstroms, only very small dimension transistors i.e. $3.0\text{-}8.0 \times 10^{-10}\text{cm}^2$, can be used.

3.4.2 GIF element mapping

Gatan Image Filter (GIF) is one of important attachments that can be used to enhance TEM capability. Special designed filter is used to split and project

transmission energy beam based on different elements. In the GIF image, interest elements have been highlighted that constitutes a map. This analysis method is based on the energy loss of TEM incident electron beam through the material. The gate oxide breakdown MOSFETs has been analyzed to identify the chemical changes, such as oxygen, cobalt and titanium etc., associated with the gate dielectric breakdown event.

3.5 Simulation

In order to support the experimental results, computer simulation was also carried out using TSUPREM4 and MEDICI. The TSUPREM4 simulator was used to setup a $0.13\mu\text{m}$ MOSFET with a $20\text{\AA}$ gate oxide. The gate oxide BD induced defects were modeled based on the physical defects revealed by TEM^[88]. MEDICI was employed to simulate the I-V characteristics before and after gate oxide BD. In addition, finite element analysis with ANSYS has been used to simulate the thermal profiles of gate oxide BD MOSFETs during BD transient. In the analysis, a “heat source” is defined in the gate oxide to simulate the joule heating generated by percolation path during gate oxide BD. The details of the model can be found in Ref. 89 and 90.

3.6 Summary

Gate oxide thickness range from $33\text{\AA}$ to $16\text{\AA}$ was used for our project. This range of gate oxide covers a few generations of CMOS devices. CVS and CCS stressing methods were used for stressing the pMOSFETs and the nMOSFETs with different gate widths and lengths. FIB sample preparation method is a crucial step for precision TEM sample preparation for gate oxide BD study. High-resolution TEM analysis provides very clear structural information that is useful to the physical analysis of the BD transistors.

Chapter 4

Breakdown Characteristics in Small Size MOSFETs

4.1 Introduction

Constant voltage stress (CVS) is widely used in gate dielectric breakdown study. Recently, the physical analysis of microstructural changes in ultrathin gate oxide breakdown has been emphasized ^[16,79]. It has been reported that dielectric-breakdown-induced epitaxy is one of the major microstructural changes that occurs during the evolution of dielectric breakdown ^[18]. In this chapter, the electrical data collected by stressing p/nMOSFETs with CVS and successive CVS have been reported. The evolution of BD hardness with relaxation in the compliance current limits has been analyzed. Microstructural changes that occur during the evolution of dielectric breakdown have been studied with the aid of TEM. From this study, the post-BD electrical characteristics have been linked to the microstructural changes associated with BD event in the stressed transistors. Since K.L. Pey *et al.* reported that the BD location is an important factor in governing the evolution of dielectric breakdown ^[91], the BD location has also been calculated and studied.

4.2 Ultrathin gate dielectric BD characteristics during CVS

4.2.1 The behavior of BD leakage current during CVS

In order to study the leakage current during CVS, about 100 p/n MOSFETs were stressed under different stressing voltages and compliance current limits. Fig. 4.1 shows a typical evolution of gate leakage current in small size nMOSFETs with n^+

poly-Si gate, 20Å oxynitride gate dielectric and p⁻ Si substrate. Note that the devices were stressed under inversion mode with different stressing voltages.

Fig. 4.1: Evolution of gate leakage current in small size nMOSFETs ($0.3 \times 0.13 \mu\text{m}^2$) stressed with CVS (3.5 V – 4.0 V) in inversion mode.

According to Fig. 4.1, the behavior of gate leakage current is a strong function of stressing voltages. The stress induced leakage current (SILC) is obviously increasing with the stressing time, and time-to-BD is shorter for a higher stressing voltage (4.0 V). However, the increment in SILC at a lower stressing voltage (3.5 V) is relatively small. Traps generated by stressing voltages are believed to contribute the increment in SILC ^[101,102]. It can be observed that the gate leakage current instantly reaches the compliance current limits during the BD event. This implies that the BD transient for nMOSFETs that are stressed in inversion mode is very short under high stressing voltages. The post-BD measurements confirmed that these MOSFETs were all suffered SBD.

(a)

(b)

Fig. 4.2: The evolution of gate leakage current in n/p MOSFETs stressed with CVS under a stressing voltage of 3.8 V. All the post-BD MOSFETs are suffered SBD. The insert graphs show the BD transients for each of BD event. (a) nMOSFET stressed in accumulation mode (-3.8V) (b) pMOSFET stressed in inversion mode (-3.8V).

Fig. 4.2 Cont.: (c) pMOSFET stressed in accumulation mode (3.8V).

Fig. 4.2 shows the evolution of gate leakage current in n/p MOSFETs with 20Å gate oxide stressed with CVS under a stressing voltage of 3.8 V in both inversion and accumulation mode. We can observe that nMOSFETs and pMOSFETs consist of different breakdown transient.

Figs. 4.1 and 4.2(a) clearly show that in SBD, the gate leakage current in nMOSFETs always instantly reached the compliance current limits. On the other hand, pMOSFETs consist of a relatively slow BD transient for a same stressing condition as in nMOSFETs.

Fig. 4.3: The evolution of leakage currents (I_g , I_d , I_s and I_{sub}) in a nMOSFET stressed with CVS in inversion mode under a stressing voltage of 3.8V. (a) Evolution of leakage currents (I_g , I_d , I_s and I_{sub}) during the stressing. (b) The BD transient takes place instantly, and most of the BD currents are constituted by the source and drain currents.

Fig. 4.3 shows the evolution of leakage currents (I_g , I_d , I_s and I_{sub}) in a SBD nMOSFET stressed with CVS in inversion mode under a stressing voltage of 3.8 V. Based on Fig. 4.3, the BD transient is very short, which is similar to the curves shown in Fig. 4.1. Most of the BD currents are constituted by the source and drain currents. The substrate current is about one order of magnitude lower than the gate leakage current.

During the BD transient, the effective resistance is a dominant factor in affecting the occurrence of microstructural changes in stressed transistors^[91]. Lombardo *et al.*^[97] reported that by connecting a 500Ω external resistance to a gate terminal, the fast BD current runaway phenomenon disappeared. The channel resistance is an important factor in affecting the overall effective resistance that will give a different BD transient ($\tau=RC$). In nMOSFETs, during the evolution of dielectric breakdown, most of the BD currents are constituted by the source and drain. Hence, the post-BD characteristics of the transistors are much related with the channel resistances.

For nMOSFETs that are stressed in inversion mode, they possess the lowest channel resistances. F. Crupi *et al.* ^[69] reported that more catastrophic failures were observed in nMOSFETs stressed in inversion mode. The relationship between the microstructural damage in the BD transistors and the channel resistances will be discussed in detail in the next chapter. Based on the ratio of leakage current I_s to I_d , the breakdown location in a failed transistor can be roughly estimated by the calculation the equation $S=I_d/(I_s+I_d)$.

Fig. 4.4 shows the SBD behavior of a pMOSFET stressed in inversion mode. Compared with nMOSFET (Fig. 4.3), a higher substrate current has been observed in the BD transient. Figs. 4.2(b) and (c) indicate that the SBD in pMOSFETs always shows a slow BD transient. A higher substrate current may play an important role in forming a slow BD transient.

Fig. 4.4: The evolution of leakage currents (I_g , I_d , I_s and I_{sub}) in a SBD pMOSFET stressed with CVS in inversion mode under a stressing voltage of -3.8V. (a) Evolution of leakage currents (I_g , I_d , I_s and I_{sub}) during the stressing. (b) A high substrate current is observed during the BD.

Due to the difference in substrate currents in n/p MOSFETs, SBD gate leakage current versus substrate current has been plotted (see Fig. 4.5). The results clearly

show that a higher substrate current is associated with SBD event in pMOSFETs.

(a)

(b)

Fig. 4.5: Ratio of BD induced gate leakage current versus substrate current in SBD n/pMOSFETs. (a) Wafer-G with 20Å gate oxide MOSFETs was stressed with CVS under a stressing voltage of 3.8 V. The compliance current limits were kept at 10μA to 120μA. (b) Wafer C with 20Å gate oxide MOSFETs was stressed with CVS under a stressing voltage of 3.8 V. The compliance current limits were kept at 100nA to 150μA.

In pMOSFETs, since a large amount of gate leakage current flows into the substrate, the substrate resistance should be included into the calculation of the overall effective resistances. As the substrate acts as a higher-resistance conducting path for the gate leakage current, its involvement in the BD path can increase the overall effective resistance.

One of the possible reasons for which the substrate currents in n/pMOSFETs are different is due to the electron wind effect on the different dopant type of the substrate. The substrate of pMOSFET is n^- type, which can supply and absorb electron winds during the BD transient^[104]. But the occurrence of this phenomenon is quite unfavorable in nMOSFETs with the p^- substrate.

From the experimental results, longer BD transient in pMOSFETs are believed to be due to this high substrate current. Lombardo reported that BD transient is a very important parameter to determine the hardness of device breakdown^[64]. The longer the BD transient time, the more unlikely the microstructure damage will occur. The experimental data also confirmed that in the moderate compliance current limits (10 μ A to 150 μ A), pMOSFETs have a lower percentage of HBD, which is also agreed by Lombardo's transient study^[97].

4.2.2 Post-BD I-V characteristics

Once dielectric breakdown occurs in a MOSFET, pMOSFET and nMOSFET show the same impact that the gate leakage current increases with the relaxation in the compliance current limits.

Fig. 4.6 shows the BD induced gate leakage current of a nMOSFET, which was measured after successive CVS. Note that BD induced gate leakage currents increase with the relaxation in the compliance current limits. Before the occurrence of dielectric breakdown, SILC will cause a slight increase in the gate leakage current. SILC is caused by the generation of traps within the dielectric layer and

gate interface; while a BD induced gate leakage current is due to the formation of a permanent percolation path within the dielectric layer. The effect of SILC and very small gate oxide BD on the device channel driving capability degradation can be seen in the Fig. 4.7.

Fig. 4.6: The post-BD gate leakage currents of a nMOSFET increase with different compliance current limits. The dimension of the nMOSFET is $0.3 \times 0.13 \mu\text{m}^2$ and the stressing voltage is 3.8 V.

Fig. 4.7: The post- BD I_d - V_d characteristics of the nMOSFET shown in Fig. 4.6. The I-V curves include pre-BD case, the case after stressing for 2000s, as well as the cases at different compliance current limits.

The effect of SILC is a universal to the whole gate area, in which it will cause obvious drain current degradation. Dielectric breakdown is a localized effect. For dielectric breakdown that occurs at low compliance current limit, degradation on the performance of the stressed MOSFET is not so obvious.

In a widely accepted BD model ^[70], a permanent leakage path is formed in the gate dielectric layer. The leakage path will remain dilating with a constant stressing. Followed by the continuously increase in the gate leakage currents, catastrophic failure will take place in the stressed transistors.

Under a normal working condition, the channel currents of a MOSFET that experiences SBD will be modified by the gate leakage current. When the dielectric breakdown is severe, the gate leakage current from the gate will become higher at the same gate voltage (assuming the voltage across the gate oxide will not change after the dielectric breakdown occurs). As shown in Fig. 4.7, a large negative drain current has been found when the BD occurred at a higher compliance current limit (200 μ A). More drain current is thus needed to compensate this gate leakage current. Drain current can be roughly estimated by $I_{d0} - V_g / (R_{perc} + R_{poly} + R_{channel-d})$, where I_{d0} is the transistor channel current driven by the gate and drain voltages. R_{poly} and $R_{channel-d}$ are the poly-Si resistance and the channel resistance between the BD point and the drain side, which remains nearly unchanged for SBD, respectively. The leakage path resistance (R_{perc}) in the gate oxide is changing with different breakdown hardness. Based on the measurement value, the post-BD effective gate resistance (R_g) is a strong function of the R_{perc} that could be used to distinguish the degree of damage in dielectric breakdown. It can be used as a critical parameter ^[71] to differentiate the BD hardness.

4.3 Categorization of breakdown in CVS

4.3.1 Analysis of the BD hardness using post-BD gate resistance

Fig. 4.8 shows the post-BD effective gate resistance R_g for nMOSFETs that were stressed with CVS in inversion mode. R_g was measured after each BD. The post-BD R_g covers a wide range of the compliance current limits. The hardness of the BD nMOSFETs covers SBD to HBD. Based on the values of R_g , three breakdown regions can be easily distinguished in according to the values of R_g .

Fig. 4.8: The post-BD effective gate resistance R_g of devices experienced only one breakdown versus the compliance current limits. These devices are stressed with CVS in inversion mode.

In Region I, breakdown was limited by low compliance current limits from 100nA to 1 μ A. The post-BD gate leakage currents are about 10-100 times higher than that of pre-BD nMOSFETs. Typically, R_g is above $10^7 \Omega$. In this region, the gate leakage current in the dielectric layer is sustained and maintained in the percolation path ^[92]. No HBD is found in this region.

In Region II, the experimental data show that the compliance current limits cover a wider range from 10 μ A to 150 μ A. In this region, the post-BD characteristics can be

very different for a given stressing condition. From Fig. 4.8, the hard breakdown and soft breakdown can occur at the same compliance current limit (based on the post-BD R_g ^[71] for which the post-BD R_g for HBD < 30K Ω .) A clear post-BD resistance gap between 30k Ω to 100k Ω can be observed on the conventional CVS experiment. The reason for the SBD and HBD co-existing on the same stressing condition is not very clear. We believe that the sufficiently high BD current induced DBIE formation ^[18] at a suitable condition plays a very important role in causing this difference. DBIE is an electron-thermal migration phenomenon associated with high thermal effects ^[87]. Details will be discussed in the later sections.

The experimental results indicate that during the HBD, most of the BD currents flow towards either the drain or source. As BD occurred at the corner of a MOSFET under CVS, the effective BD resistance is lower that leads to a shorter BD transient ($\tau=RC$) than BD at a channel center (See detailed discussion in later chapter). Hence, the local BD current density associated with this BD transient for a given stressing condition is higher. A severe thermal damage will take place and it is hard to balance in the BD transistor. Hence, corner SBD+DBIE in ultrathin gate oxide is rare. MOSFETs corner BD is one suspect for observing the post-BD resistance gap in Region II.

For MOSFETs suffered HBD, the substrate currents are obviously lower and the ratio of substrate current to the gate leakage current during the HBD is shown in Fig. 4.9. Compared with the results shown in Fig. 4.5, MOSFETs has smaller substrate/gate current ratio. From Fig. 4.9, the ratio of substrate current and gate leakage current is 2-3 orders of magnitude smaller than that of SBD. It is believed that in HBD DBIE shorts the two electrodes ^[91], leading to a lower Si-substrate current.

Fig. 4.9: Substrate current versus gate leakage current in HBD MOSFETs. HBD occurred in 20Å gate oxide small size MOSFETs that were stressed with CVS under a stressing voltage of 3.8 V. The compliance current limits were kept at 10µA to 400µA.

In Fig. 4.9, the ratio of the substrate current to the gate leakage current for pMOSFETs is smaller than that for nMOSFETs. BD associated microstructural damage in the BD MOSFETs substrate are believed to be severe. This is because a low-resistive gate to source or drain leakage path has been generated during the BD. One example is a pMOSFET HBD shown in Fig. 4.10. A DBIE between the poly-Si gate and Si substrate can be clearly observed. At the same time, the Si substrate and poly-Si gate in the center of the transistor channel have also been damaged. A very low substrate current in this HBD pMOSFET was contributed by the microstructural damage during the BD.

Fig. 4.10: TEM micrograph of a HBD pMOSFET, stressed in accumulation mode with a compliance current limit of $50\mu\text{A}$. A DBIE is indicated by the dotted circle.

For Region III, due to very high current density, BD always associates with high thermal effect. Similar microstructural damage in the BD MOSFETs dominate the post-BD I-V characteristics. In this region, soft breakdown is hardly seen. When the compliance current is larger than $250\mu\text{A}$, no soft breakdown can be observed.

4.3.2 Structural analysis of BD in Regions I, II and III

In the previous section, we discussed the BD hardness based on the post-BD effective gate resistance values. Three regions have been defined. We also mentioned that in Regions II and III, DBIE plays a very important role in determining the post-BD characteristics of small size MOSFETs. In this section, we use TEM to correlate the physical analysis results with the post-BD effective resistance.

Soft breakdown without DBIE

In Region I, we found that TEM analysis does not reveal any BD related microstructural changes. Fig. 4.11 shows a TEM micrograph of a failed device with

the post-BD R_g value around $9 \times 10^7 \Omega$. The HRTEM image in Fig. 4.11(c) shows that the SiO_2 and Si interface is clearly distinguished. Houssa *et al.* reported ^[94] that the percolation path in the dielectric layer is temperature dependent. The gate leakage current increases with increasing temperature. The percolation path will be dynamically evolved during a breakdown transient. At the initiation of a SBD, the BD current flowing through the percolation path interacts with the scattering centers and heats up the leakage path, and a positive feed back current-temperature loop ensures a higher density current is pumped into the percolation path resulting in enhancement in the temperature as long as the stress voltage is maintained. But the compliance current limit cuts off the BD current at low level and retards the current-temperature positive feedback enhancement loop. So nMOSFETs BD in Region I only have the percolation path formed in the gate dielectric layer.

Fig. 4.11: TEM images of a failed nMOSFET with the compliance current limit of $1 \mu\text{A}$. The dimension of this nMOSFET is $L=0.3 \mu\text{m}$ and $W=0.15 \mu\text{m}$. The post-BD effective gate resistance is around $9.78 \times 10^7 \Omega$.

In Region I, breakdown associated thermal effect is less due the very low compliance current setting. The BD devices have maintained relatively good post-BD IV characteristics. An example of post-BD IV characteristics is shown in Fig. 4.7.

Soft breakdown with DBIE

In Region II, SBD in gate oxide causes the post-BD effective gate resistance in the range of 10^5 - $10^6 \Omega$. In this region, the BD induced microstructural change can be observed in the vicinity of the BD spot. Fig. 4.12 shows two typical examples. The BD result shown in Fig. 4.12(b) is situated near the corner of the transistor channel, while BD shown in Fig. 4.12(a) is situated at the center of the transistor channel.

Fig. 4.12: TEM images of SBD at different locations in two nMOSFETs (a) BD situated near the center of the transistor channel. The post-BD R_g is around $7.8 \times 10^5 \Omega$. (b) BD situated near the corner of the transistor channel. The post-BD R_g is around $2.6 \times 10^5 \Omega$.

From the HRTEM micrographs shown in Fig. 4.12, we can see DBIE occurred in both BD devices. On the same understanding from the percolation dynamic model, the current-temperature loop is higher than Region I due to the higher compliance current limit. When SBD with current-temperature feedback is sufficiently strong to trigger the microstructural damage, DBIE starts to grow. DBIE growth is believed to consume the system free energy of the BD system. If the DBIE growth dominates and the current density is capped at certain level, this will eventually lead to a metastable equilibrium. As a result, SBD with DBIE will occur.

Hard breakdown with DBIE

If the BD current density is very high, more energy will be generated and discharge into the structure of the small size MOSFET. In Region III and Region II for HBD, DBIE will grow and presumably has punched through the gate dielectric layer, leading to the occurrence of thermal runaway and catastrophic failure in the MOSFET. After HBD, the MOSFET loses its transistor-like characteristics, and shows resistance-like post-BD characteristics as shown in Fig. 4.13(b).

(a)

(b)

Fig. 4.13: HBD induced DBIE in a 20Å gate oxide nMOSFET. (a) DBIE has been found at the corner of the poly-Si gate, and causes direct short between the gate and substrate. The post-BD gate resistance is 5kΩ. (b) The post-BD V_d - I_d curve shows that the nMOSFET possesses resistor-like post-BD characteristics.

From the TEM image shown in Fig. 4.13(a), a DBIE can be clearly seen near the edge of the poly-Si corner. The size of DBIE is around 10nm, which shorts the poly-Si electrode to the substrate, leading to a resistor-like post-BD IV characteristic of the MOSFET. This HBD is named as Type I hard breakdown, in which DBIE has formed in the vicinity of breakdown location. The remaining part of the device structure is still intact. The I_{sd} - V_{sd} measurement by swapping the source and drain terminal shows the transistor-like behavior, i.e. asymmetry in the post-BD I-V characteristics of the device^[103].

B.Kaczer *et al.*^[73] reported that digital circuits could still function even some transistors have suffered HBD. We suspect the one-sided hard breakdown described in Fig. 4.13 is responsible for the reported phenomenon in Ref. 73.

As the BD caused the gate voltage loses control on the entire transistor channel, this HBD is treated as Type II hard breakdown. In Type II hard breakdown, channel short associated with gate oxide BD in the MOSFETs has occurred. Silicide compounds from the source, drain and gate have migrated from their original location to the BD location, which we term as DBIM (device breakdown induce migration)^[17]. This is the worse case gate oxide BD in MOSFETs. Fig. 4.14 shows an example of Type II HBD. As shown in Fig. 4.14(c), both I_{sd} - V_{sd} and I_{ds} - V_{ds} curves show a liner-like response. In particular, the drain/source current at 1.5V is much higher than original channel current. Based on the BD MOSFET microstructure shown in Fig. 4.14(a), more severe microstructural damage are observed in the MOSFET with Type II HBD. Elemental cobalt mapping by GIF in Fig. 4.14(b) shows that the gate silicide has migrated from the source/drain and gate to the BD spot. In this case, coupled with dopant redistribution^[96], the DBIM material shorts the transistor channel, leading to the I-V curves seen in Fig. 4.14(c).

Fig. 4.14: HBD induced DBIE and DBIM in a small size nMOSFET. (a) HBD DBIE occurred at the corner of the poly-Si gate. (b) Elemental Co mapping of (a) by GIF shows that the cobalt from the gate and S/D has moved towards the BD location. (c) V_d - I_d curves show a channel short.

4.4 SCVS against CVS in ultrathin gate dielectric BD

4.4.1 Characteristics of SCVS stressed MOSFETs

As discussed in the previous sections, we know that the HBD and SBD can co-exist for a given stress compliance current condition. The uncontrolled thermal effect causes a distinctive post-BD effective gate resistance difference with missing R_g

between $30\text{K}\Omega$ and $100\text{K}\Omega$, as shown in the Fig. 4.8. In order to more systematically analyze the BD phenomenon in MOSFETs in relation to the physical damage and post breakdown I-V characteristics, another stress method, known as SCVS, has been developed. In Fig. 4.15, the R_g values corresponding to gate oxide BD at various stressing compliance currents were measured after each relaxation of the compliance current limit to a higher value. In our experiments, we found that the leakage current surged to the compliance limit each time as it was being relaxed. The R_g values in Fig. 4.15 indicate that the SCVS can also lead to hard breakdown, but the final breakdown current is much larger than that of a single CVS. A band of continuously decreasing R_g with increasing leakage can be clearly seen and defined from the graph. Hence SCVS can be used to control the breakdown hardness.

Fig. 4.15: Post-BD effective gate resistance values (R_g) measured from nMOSFETs stressed with successive constant voltage stress (SCVS) method.

The actual reason for decreasing R_g with increasing compliance current limit in SCVS is not fully understood. One possible explanation is due to a well-controlled thermal effect in this kind of stressing method. The incremental relaxation of compliance current limits to a next higher value in SCVS leads to a more controlled BD spot evolution. The discontinuously evolved BD spot will degrade the fast

transient effect. The gate oxide punch-through by the DBIE growth is limited due to insufficient thermal energy.

Under SCVS method, since the evolution of SBD to HBD can be well controlled, thus no discontinuity in the post-BD effective gate resistance R_g values (Figs. 4.8 and 4.15) is seen. As we mentioned, BD degradation involves the initial percolation path dilation and DBIE growth. In CVS, it is relatively hard to differentiate the impact of these two parameters. However in SCVS, we can further understand their effects on MOSFETs degradation.

Fig. 4.16: HRTEM micrographs of the nMOSFETs failed during SCVS in inversion mode in Region II, as discussed in Fig. 4.8. (a) BD without DBIE. The post-BD R_g is $\sim 50\text{k}\Omega$ with a stress compliance current of $500\mu\text{A}$. (b) BD with a small DBIE at the channel corner. The post-BD R_g is $\sim 30\text{k}\Omega$, with a stress compliance of $380\mu\text{A}$.

Fig. 4.16 shows HRTEM micrographs of the two same size nMOSFETs stressed with SCVS and BD in Region II, with a final stressing compliance current limit of $380\mu\text{A}$ and $500\mu\text{A}$ respectively. It can be seen from Fig. 4.16(a) that the first nMOSFET shows no visible DBIE associated with BD. The other MOSFET shows DBIE formation in the LDD region of the channel during BD evolution (see Fig.

4.16(b)). The DBIE is HBD-like and obvious gate dielectric thinning has been found in the sample shown in Fig. 4.16(b).

Fig. 4.17 shows the pre- and post-BD I-V characteristics of both the small size transistors seen in Fig. 4.16. We can see that both samples show a relative large negative value (which is much greater than the direct tunneling leakage) I_d at $V_d = 0V$. It has been also observed that the negative value of I_d at $V_d = 0V$ is more for the MOSFET having DBIE, even though the MOSFET without DBIE was stressed to the final BD with a higher compliance current value.

Fig. 4.17: Pre- and post-BD I-V characteristics of nMOSFETs shown in Fig. 4.16. The I-V of the nMOSFET with DBIE has more degraded post-BD I-V characteristics.

The peak value of the transconductance of MOSFETs stressed under SCVS shown in Fig. 4.16 is plotted in Fig. 4.18. A steeper slope in the degradation of the transconductance peak between $250\mu A$ and $350\mu A$ can be seen for the nMOSFET having DBIE. It indicates that the DBIE formation has higher impact on the degradation of transconductance, which is directly related to carrier mobility and transistor capacitor degradation.

Fig. 4.18: Relationship between the transconductance and compliance current limits. A drastic drop in the transconductance is observed for the nMOSFET with DBIE.

The post-BD gate leakage current versus stress compliance current shown in Fig. 4.19 shows that the I_g/I_{com} ratio is stable for the MOSFET without DBIE. But there is a drastic increase in the I_g/I_{com} ratio for the MOSFET having DBIE (see Fig. 4.19). The results demonstrate that the DBIE growth, which leads to dielectric layer thinning, has more impact on the performance of a MOSFET during the BD transient.

If the BD induced percolation path dilation is a dominant factor in deciding the post breakdown characteristic, higher stress leakage current can be tolerated. If this effective conductor-like percolation path is wide enough after dilation, HBD can occur without the formation of DBIE. Our TEM results also support this phenomenon. For thinner gate dielectric layer, the critical trap density necessary in forming a new percolation path is less ^[56-57]. It is believed that less thermal budget is needed to form a wide leakage path in thinner dielectric layer, and the DBIE does not have proper condition to form. As a result the probability for the formation of

DBIE in the very thin gate dielectrics is very low. The final BD effect in nominal operating conditions may close to the results represent for MOSFETs stressed under SCVS.

Fig. 4.19: Increase in the post-BD gate leakage current against stress compliance current limit for nMOSFETs as shown in Fig. 4.16. The curves clearly indicate that once DBIE occurs, the gate leakage increases drastically.

On the other hand, the presence DBIE growth is still important, because it can still happen in ultrathin gate dielectric layer, resulting in gate dielectric thinning and finally leading to an early failure. Compared with SBD without DBIE, it is observed that SBD + DBIE always results in large impact on the performance of MOSFETs [87].

4.4.2 Comparison between CVS and SCVS

Based on both conventional constant voltage stress and successive constant voltage stress, a comparative study on understanding the BD mechanism can be made.

It has been established that, when the BD is very soft (i.e. Region I), gate dielectric

percolation path forms and dilation is the dominant factor for the failure mechanism.

If breakdown hardness is further increased (i.e. Region II) by relaxing the compliance current limit, DBIE can be formed due to a high thermal effect caused by the flow of higher current density into the vicinity of the BD spot. So in region II, both percolation path dilation and DBIE formation are responsible for the degradation in the transistor performance and are the two major factors in determining the BD hardness in Region II.

In SCVS stressing method, in the post-BD effective gate resistances is continuous in Region II (Fig. 4.15). This is due to the presence of a well-controlled joule heating during the BD event by progressively relaxing the compliance current limit successively. In this way, it provides a continuous and more controlled BD evolution. It is found that, if there is no obvious dielectric thinning due to the DBIE formation during BD transient, the final breakdown leakage current for HBD will be much larger. On the other hand, if DBIE growth during BD event results in substantial gate dielectric thinning it accelerates device degradation. When the DBIE growth is fast enough to punch through the gate dielectric layer, then HBD will occur. It also supports that DBIE growth is the factor responsible for the co-existence of SBD and HBD in the same compliance current (Region II) in the CVS mode (see Fig. 4.8).

Based on the study, it is also established that DBIE formation during the BD transient plays an important role in the evolution of SBD to HBD. This is especially important if the thermal effect cannot be preciously controlled during the BD transient. DBIE formation is found directly related to the release of thermal energy during the BD transient. It increases with stressing compliance current and decreases with stress voltage^[97] for the same dielectric thickness. It is predicted that for thinner gate oxide operating at nominal voltage, the chance to form DBIE is still possible, but it will be much less. This may explain that fast HBD (i.e. non

progressive-like at nominal voltage) is much less likely to happen in ultrathin gate oxide MOSFETs.

4.5 BD location evolution

BD location has been found to be an important factor affecting the BD behavior and post-BD I-V characteristics^[91]. The BD location in a BD gate oxide can be calculated using the equation $\Delta I_d / (\Delta I_d + \Delta I_s)$ ^[71], where ΔI_d and ΔI_s are the measured post-BD leakage currents increment in the source and drain respectively. The relationship between the breakdown location and stress compliance current is plotting in Fig. 4.20.

Fig. 4.20: BD locations for various compliance current limits. The MOSFETs were stressed under CVS and SCVS. (a) BD locations in low compliance current limits. The distribution is random along the transistor channel. (b) BD locations in high compliance current limits. Most of MOSFETs, the BD has evolved to the edge of the transistor edge.

MOSFETs were stressed either by CVS or SCVS for various compliance current ranges. The breakdown location has different distribution characteristics depending

on the compliance current limit. In the low to middle compliance current condition (100nA-100 μ A), the breakdown locations are random and located along the device channel. But in high compliance currents condition (>150 μ A), the final leakage path in most of the small size MOSFETs is near the edge of the transistor channel. A possible mechanism is that the breakdown leakage path evolves from the initial BD point to nearer to the corner of the channel^[87]. But this phenomenon is hard to be distinguished and differentiated under single CVS since the BD evolution is a very fast, especially for high compliance currents. The SCVS has been used to study the breakdown location change with the relaxation in the breakdown current.

Fig. 4.21: The evolution of BD locations in gate oxide=20Å MOSFETs stressed under SCVS with $V_{g\text{stress}}=3.8\text{V}$ in inversion mode. (a) The dimension of the MOSFETs is $W=0.3\mu\text{m}$ and $L=0.13\mu\text{m}$. (b) The dimension of devices is $W=0.3\mu\text{m}$ and $L=0.3\mu\text{m}$.

Figs. 4.21 (a) and (b) show the BD location for different MOSFETs stressed with SCVS. In Fig. 4.21(a), for small L , i.e. $0.3\times 0.13\mu\text{m}^2$ ($W\times L$), the initial breakdown location shown is randomly distributed along the MOSFETs channel, but they evolved slowly or suddenly to the poly-Si corner while the breakdown current increased. However, for the high compliance current limits, the final BD is always situated near one side of the channel, in which the results agree well with those in

Fig. 4.20. M. Houssa *et al.* ^[94] reported that the BD induced charges could further increase the percolation path. Due to the asymmetry in the breakdown leakage path between the breakdown spot and the S/D regions, the associated effective channel resistances dominated by R_{gs} and R_{gd} are different. As the BD leakage increases, a larger current is resulted in the lower R_{gs}/R_{gd} side. Thus it is believed that a more favorable condition is developed on the higher current side, leading to possible more rapid dilation of the percolation path, and formation and growth of DBIE on the lower R_{gs}/R_{gd} side ^[87].

From Fig. 4.21, the sudden change in BD location is also seen in one of the MOSFET. We suspect that a new BD has taken place. Thus multiple BDs are still possible in a same small size transistor, but it is very rare.

On the other hand, in longer channel devices ($0.3 \times 0.3 \mu\text{m}^2$) shown in Fig. 4.21(b), the final leakage path does not evolve much even at high compliance current limits. Based on the geometrical dependence of gate oxide breakdown evolution studied, Y. Sun ^[89] reported that the localized joule heating generated by the percolation path takes longer time to induce DBIE formation for longer L , which may explain the less evolution phenomenon seen in longer transistor. In view of the continuous shrinking of the dimension of devices, the evolution of BD location in short-channel MOSFETs is an important BD mechanism for reliability study.

Another important conclusion that can be derived from this BD location analysis is the relation between the BD transient and location evolution. As we see, HBD or harder BD always takes place near the device corner. However, if the initial BD point is close to the center of the channel, it needs longer time to evolve from the center to the edge. Eventually, this leads to a longer transient time. Same BD compliance current may have a different impact to the hardness of BD MOSFETs, as we shown in Fig. 4.8. The BD transient and location will be discussed in detail in the next chapter.

4.6 Conclusion

Based on the above physical and electrical analysis, we show that there are three distinctive regions i.e. SBD, SBD+DBIE and HBD+DBIE during the BD event in ultrathin gate dielectric. Different BD hardness is in these regions which result in different microstructural damage in the small size transistors stressed. The physical i.e. TEM and electrical results show that the dielectric percolation path dilation and DBIE growth affect the post-BD performance of small size MOSFETs. At the same time, we found that the breakdown location is an important parameter in studying the final post-BD transistor performance.

Chapter 5

DBIE formation and its effect on transistor performance

5.1 Introduction

In the pervious chapter, we reported the microstructural damage in the gate channel associated with gate oxide breakdown, especially for high compliance current stressing. DBIE is one of the most important phenomena occurred during breakdown event. The formation of DBIE and its effects on the device performance will be reported in this chapter.

5.2 DBIE formation mechanism

DBIE plays a major role in the evolution of SBD to HBD during a BD event and the results have been reported in the previous chapter. The size and shape of the DBIE are strongly dependent on the breakdown induced thermal effect. Fig. 5.1 shows a schematic of the DBIE growth mechanism during a BD event.

When a MOSFET suffers a breakdown, a permanent percolation path formed in the dielectric layer. The effective diameter of the percolation path (t_{per}) is a strong function of the BD current during the breakdown transient. Higher current can generate wider percolation path^[55]. At the same time, the localized heat generation is also associated with the breakdown current. This heat source is believed to generate huge thermal effects in the vicinity of breakdown path that is strongly dependent on the BD power (w), which is determined by the percolation path resistivity and BD current density ($w=j^2\rho$). At a favorable condition, DBIE can grow from the cathode to the anode due to thermal-electro migration effect^[79].

Fig. 5.1: Schematics showing the possible effects of oxide deformation caused by the growth of DBIE on gate oxide failures. (a) Localized oxide “thinning” occurs when the gate oxide thickness at DIBE point $t_{1ox} < t_{ox}$, which favors more percolation paths formation in its vicinity. (b) A proposed progression of the growth of the DBIE during a SBD where $t_1 < t_2 < t_3$. HBD will occur if the DBIE from the cathode grows to an extent that it shorts the anode. [18]

Fig. 5.1(a) shows schematics of one of the proposed model for the DBIE formation based on the percolation model [57]. When a high density of BD current is passing through the initial percolation path, dynamics joule heating effect [92] has been generated in the vicinity of percolation path. When the localized temperature approaches the Si melting point (1415°C), the Si-Si bonds start to break. Si atom dislodgment occurs mainly near the BD location. It is believed that Si broken bond occurs at both cathode and anode side.

These dislodged Si are “migrated” by an electronmingation-like electron wind from

the stressed MOSFET cathode side to the anode side. However, due to the presence of the gate oxide, the migrated Si atoms on the cathode side are “piled” up at the entrance of the percolation path. Coupled with the presence of a very high and localized temperature at both electrodes of the percolation path, the Si substrate/SiO₂ cathode interface and the SiO₂/poly-Si anode interface are expected to move in the same direction, but the extent of the movement of the anode interface will be smaller. Thus this mechanism makes the localized gate oxide thinner than elsewhere.

Fig. 5.1(b) shows the schematic of the dynamic growth of the DBIE during a BD event, where $t_1 < t_2 < t_3$ are the progressive effects of BD with respect to the initial time of BD. Catastrophic failure i.e. HBD will occur if the DBIE from the cathode side grows to an extent that it punches through the gate oxide, making a direct short to the anode.

We reported that two competing BD mechanisms, i.e. DBIE growth and percolation path dilation, take place simultaneously during the BD event in the previous chapter. With the scaling down of gate oxide thickness, defects in the gate oxide can generate a wider percolation path easily [56-57]. As the thermal effect is a strong function of the BD current density (j^2) and percolation path resistance (R_{perc}), the faster dilation of the percolation path results in a decrease in the BD localized heat generation in the vicinity of the percolation path. Thus DBIE has less possibility to form in very thin gate oxide. The experimental results confirmed that SBD has less DBIE in 16Å gate oxide MOSFETs, but HBD is still associated with thermal runaway and the formation of DBIE [18].

In CVS, besides the stress compliance current effect on the DBIE growth, the BD location, BD transient and device geometry are important factors in nucleating a DBIE.

5.3 Effective of breakdown location on DBIE

In BD MOSFETs stressed under SCVS method, we found that the effective BD locations are evolved during the successive relaxation in the gate leakage compliance current limit. The high leakage paths always evolve towards the small size transistor corner as the I_{com} relaxes. In this section, we analyze the DBIE type and its relation with the BD location.

In one of the designed experiments, we floated the drain terminal and connected the source and substrate of a small size nMOSFET to a ground while applied a stress voltage to the gate. This asymmetric stressing condition (or called one-sided stress) forces the BD current to flow towards the one side of the stressing MOSFET. The purpose of this experiment is to enhance BD at the corner of the poly-Si gate to study the relation of DBIE growth with the BD leakage current and location. As we have previously discussed these two parameters are important to for the formation of a DBIE in small size transistors.

Fig. 5.2: (a) TEM micrograph of a HBD small size transistor under one-sided stress. (b) TEM micrographs of a HBD small size transistor stressed using CVS. The insert shows a high magnification TEM of DBIE.

Fig. 5.2 shows the TEM micrographs of two HBD small size transistors. One transistor is a HBD with the one-sided stress described above (Fig. 5.2(a)), and the other is a HBD during a CVS (Fig. 5.2(b)). In both cases, the respective DBIEs near the gate corner are apparent and grown from the Si substrate into the poly-Si gate. The experimental results also found that, the HBD cases are easily occurred in the asymmetric stress, as compared to the conventional CVS for a same stressing condition. The post-BD microstructural damage is similar in both stressing condition. The corner-DBIE is typically sharp with an apparent peak, similar to a pyramid. This kind of DBIE is defined as Type I DBIE.

Fig. 5.3: (a) Low and (b) high magnification TEM micrographs of a SBD nMOSFET with $33\text{\AA}$ gate oxide stressed in inversion mode with a current compliance at 100nA .

In contrast to the DBIE in Fig. 5.2, the DBIE shown in Fig. 5.3 occurred near the center of the channel. The shape of such DBIE is rounded and smooth with no apparent apex. Such DBIE is termed as Type II DBIE. This kind of BD induced DBIE does not cause a catastrophic fail i.e. HBD in transistor.

Based on the localize thermal-electron migration effects ^[79], DBIE is thermally

driven and induced by a sudden surge in the highly localized current through the percolation conduction path within the gate oxide. One model for the gate oxide breakdown conduction is shown in Fig. 5.4.

If the breakdown site of the gate oxide is nearer the center of the channel as shown in Fig. 5.4(a), R_{ch1} and R_{ch2} will be similar and the breakdown current will be determined by the total effective resistance $R_1 = (R_{parasitic} + R_{poly} + R_{perc} + R_{ch1} \text{ (or } R_{ch2})/2 + R_{LDD}/2)$, where $R_{parasitic}$ is the total parasitic resistance and R_{perc} is the resistance of the percolation conduction path^[98], respectively. In this case, we assume that $R_{sub} \gg (R_{ch2} + R_{LDD})/2$ which is valid for our transistor architecture. If the breakdown happens near the edge of the poly-Si gate as shown in Fig. 5.4(b), the total effective resistance will be $R_2 = (R_{parasitic} + R_{poly} + R_{perc} + R_{eff,ch} + R_{LDD})$, where $R_{eff,ch}$ is dominated by the much lower R_{ch2} (i.e. $R_{eff,ch} \approx R_{ch2}$) since $R_{ch2} \ll R_{ch1}$. Due to this asymmetry in the conduction channel resistance upon breakdown, much higher current (which equals to the externally applied voltage, V , divided by the total effective resistance (R_1 or R_2), i.e. V/R) is expected to flow through the percolation conduction path via R_{ch2} as shown in Fig. 5.4(b) since $R_2 < R_1$ and $R_{LDD} < (R_{ch1} + R_{ch2})/2$. If V , R_{poly} , R_{LDD} , $R_{parasitic}$ and the instantaneous R_{perc} are assumed to be the same for both cases under the same stress conditions upon gate oxide breakdown, effectively more localized joule heating is expected for cases where the breakdown site is nearer to the poly-Si gate edge. As higher current density surges through the breakdown location, much higher joule heating (proportional to J^2R) can be expected. These conditions greatly favor the fast-growth of the DBIE^[18]. If the rate of change of the total effective resistance associated with the dilation of the percolation path during the transient does not change faster than the DBIE growth rate, DBIE growth will dominate. And it not only punches through the gate oxide resulting in HBD^[18], but also forms a shape that resembles to pyramid as shown in Fig. 5.2. This is Type I DBIE.

Fig. 5.4: Schematics showing the effective resistance dependence on the gate oxide breakdown location in the transistor channel for nMOSFETs stressed in inversion mode. (a) Gate oxide breakdown happens near the center of the channel. (b) Gate oxide breakdown happens near the edge of the poly-Si gate. ^[91]

In the case of Type II DBIE, due to the lower induced current density (higher parasitic resistivity) and thus less joule heating near the breakdown site, Si atoms do not migrate as fast as the case in Type I DBIE towards the percolation path. As a result, the dynamic R_{perc} does not change rapidly, due to a lower localized temperature increase as compared to that of Type I DBIE. Hence the DBIE growth is gradual and gentle. This means that the DBIE growth rate is slower for gate oxide

breakdown site nearer to the center of the channel, resulting in rounded and smooth DBIE morphology. In this case, the final appearance of Type II DBIE is expected to be less prominent as shown in Fig. 5.3. More importantly, Type II DBIE is less likely to lead to HBD. The physical analysis of Type I and II DBIE agrees well with the effective post-breakdown gate resistance, R_g , as a function of breakdown position in the MOSFET channel reported by Degraeve *et al.* [99] and Kaczer *et al.* [73]. R_g has been shown to be much higher for gate oxide breakdown in the channel and drops significantly when the gate oxide breakdown occurs between the gate and the S/D extension.

From the above discussion, it is concluded that catastrophic damage (DBIE) taken place at the edge of gate is important to small size transistor BD as the gate dimension now shrinks to sub 100nm regime.

5.4 DBIE formation in relation to BD transient

BD transient is another important phenomenon in study of small size transistor BD, because it represents the amount of energy release. The relation of DBIE formation with BD transient is studied in this section.

Fig. 5.5 shows an example of progressive BD transient arrested in a 20Å gate oxide nMOSFET stressed at 4V. Two distinctive phases could be identified in this transient curve. The first part of the transient is a noisy and progressive process, which is typically of the order of milliseconds, in agreement with ref. 100. In the second part of the transient, the gate current jumps to mA level in a time of the order of 1μs, limited by the bandwidth of the amplifier [97]. Since the different BD transient phases exist, the correspondence microstructural damage in the small size transistor are studied.

Fig. 5.5: BD transient in submicron nMOSFETs ($0.3 \times 0.3 \mu\text{m}^2$) stress under CVS in inversion at 4V gate voltage. Note that after an initial phase of progressive BD (Phase I), a fast BD runaway takes place (Phase II).^[92]

Fig. 5.6 shows the TEM results of a BD transistor stressed under CVS without current limitation. In this sample, a huge leakage current surged into the BD transistor and reached the second phase of the transient curve after gate oxide BD. The results are similar to the BD transient shown in Fig. 5.5. Type I DBIE has been found on the edge of the poly-Si gate that supports the presence of Phase II BD transient is a thermal runaway process. It also supports that DBIE is always seen after device suffered the faster BD transient (Phase II). This agrees with our previous discussion that Type I DBIE grows very rapidly during the thermal runaway, and shorts the electrodes of the transistor, leading to HBD.

Fig. 5.6: Low (a) and high (b) magnification of TEM images show a 20Å gate oxide BD nMOSFET stressed in 4V inversion mode without compliance current. In this case, Phase II of the BD transient shown in Fig. 5.5 was observed in the transient.

This runaway in Phase II in the BD transient is a strong function of the transistor size. And it is strongly dependent on the geometry of the transistor ^[97]. Fig. 5.7 shows the BD transient results of different transistor sizes. In Fig. 5.7(a), it is clearly seen that the larger transistor has a longer Phase I BD transient, i.e. a progressive increased the BD current. In Fig. 5.7(b), as the lengths of transistors are 100μm, no Phase II BD transient can be observed in the similar stress condition and time window. This indicates that longer channel devices take longer time to reach HBD compared with short channel devices. As we described in the previous section, the BD leakage path near the gate corner is critical in the formation of a type I DBIE that explains the size dependence on BD transient characteristic. During gate oxide BD, the longer the transistor channel length is, the less chance of corner BD and higher the effective resistance during the BD will be ^[97]. The BD transient is a function of this BD effective resistance ($\tau=RC$) that has been confirmed by this BD transient studied.

Fig. 5.7: BD transient in different transistor sizes. (a) $0.2 \times 0.15 \mu\text{m}^2$ to $0.3 \times 0.3 \mu\text{m}^2$ nMOSFETs stressed in inversion mode at 3.9V. (b) BD transient of $100 \mu\text{m}$ gate length nMOSFETs in inversion mode at 4V.

In Phase I of gate oxide BD transient, it is assumed the percolation path evolves dynamically^[92]. The temperature dependence of the leakage current in a percolation cluster forms a positive current-temperature feedback loop with the dangling bands and defects increase in the gate oxide film. If this electro-thermal effect is sufficient, Si atoms of the Si substrate and poly-Si in the vicinity of the percolation path will be dislodged. Si atoms pile up at the Si/SiO₂ interface and form a DBIE hillock, i.e. SBD with DBIE.

Fig. 5.8 (b) shows a BD transistor that contains multiple small DBIEs formed in the channel, but the gate oxide is still retained. In the transient curve (Fig. 5.8(a)), we can see that the leakage current is still progressively increasing and did not reach the Phase II of BD transient. The BD current has been limited by a compliance current setting of $100 \mu\text{A}$. The results further demonstrate that DBIE that has already formed during the progressive increase in the BD current (Phase I). When the DBIE punches through the gate oxide layer, a fast current runaway will take place (Phase II).

Fig. 5.8: (a) Gate leakage current with time of a small size nMOSFET ($0.3 \times 0.15 \mu\text{m}^2$) captured during BD event until the gate leakage current reaches the compliance current limit of $100 \mu\text{A}$.^[95] (b) TEM micrograph shows multiple DBIEs in the channel during the progressive BD transient.

5.5 Effect of breakdown location on post-BD I-V characteristics

Based on the above discussion, we know that DBIE is a phenomenon associated with small size transistor BD. In this section, we will continue the discussion about the effect of the location of DBIE on the post-BD I-V characteristics.

5.5.1 DBIE near poly-Si gate edge

Fig. 5.9(a) shows the $I_{\text{ds}}-V_{\text{ds}}$ characteristic of a $20 \text{ \AA}$ gate oxide nMOSFET stressed in accumulation mode under SCVS with a compliance current limit of 2.5 mA . The post-BD I_{ds} curves are almost linearly increasing with the drain voltage increase, i.e. resistance-like characteristics. The TEM micrograph of this BD small size transistor is shown in Figs. 5.9(c) and (d). We can see that an abnormal DBIE near the drain edge of the poly-Si gate. On the drain side, the Si substrate has shorted with the poly-Si gate. Hence no more saturation current can be formed in the transistor channel with increasing drain voltage. The TEM micrographs correspond well with

the resistance-like characteristics of the post-BD transistor i.e. due to DBIE formation near the poly-Si edge.

(a)

(b)

Fig. 5.9: Electrical characteristics of a 20Å gate oxide small size nMOSFET stressed under SCVS in accumulation mode with a compliance current of 2.5mA. (a) I_{ds} - V_{ds} curves. (b) I_{sd} - V_{sd} curves

Fig. 5.9 Cont: (c) and (d) TEM micrographs show a DBIE nucleation bump near the drain side of the transistor.

The post-BD effective gate resistances with respect to source and drain show very different values. The post-BD R_g at $V_g=1.5V$ while $V_s=V_d=0V$ is $2.7K\Omega$, which is in agreement with the reported data for HBD.^[71] Furthermore, the pos-BD R_{dg} value is $2.97K\Omega$ while the R_{sg} is $31.7K\Omega$. Fig. 5.9(b) shows the $I_{sd}-V_{sd}$ curves of the same transistor measured in a reverse configuration (i.e. the source and drain are swapped) exhibit transistor-like characteristics for all the V_g values studied. The transistor can partially retain its transistor-like performance even the gate and substrate are shorted to each other. TSUPREME4 has been used to simulate the post-BD device characteristics. The model used a doped Si like filament^[73] to simulate DBIE within gate oxide.^[88] Fig. 5.10 shows the post-BD curves of a 4nm highly doped Si filament situated near the transistor corner. The simulation results confirm that the asymmetric $I_{ds}-V_{ds}$ curves can be obtained in HBD with a DBIE grown near one side of the transistor.

Fig. 5.10: The TSUPREM4 simulated I_{ds} - V_{ds} characteristics with a 4nm doped Si filament situated at the poly-Si gate corner. ^[88] (a) and (b) show asymmetric I-V characteristics of the post-BD transistor. (a) Linear-like I-V curves (b) transistor-like I-V curves.

5.5.2 DBIE near poly-Si gate center

Figs. 5.11(a) and (b) show the I_{ds} - V_{ds} characteristics of another 20Å gate oxide nMOSFET failed with a compliance current of 10μA stressed in voltage-ramp method. The post-BD I-V characteristics have degraded in the saturation current in both drain current measurement configurations (i.e. reversing drain and source for various V_g). But both measurement configurations show transistor-like characteristics.

(a)

(b)

Fig. 5.11: (a) and (b) electrical characteristics of a 20Å gate oxide small size nMOSFET stressed under voltage ramp with a compliance current of 10μA. (a) I_{ds} - V_{ds} curves (b) I_{sd} - V_{sd} curves.

Fig. 5.11 Cont: (c) TEM micrograph shows a DBIE nucleation bump near the channel center of the transistor (d) HRTEM micrograph shows the DBIE is an epitaxy from the Si substrate to the poly-Si gate.

The TEM micrograph shows that gate oxide rupture happened near the center of the transistor channel (Figs. 5.11(c) and (d)). The HRTEM image indicates that DBIE has punched through the gate oxide, resulting in a “direct” short between the Si substrate and poly-Si electrodes. Based on the above analysis, even a “direct” short takes place in the small size transistor gate, the remaining area is still able to form a channel. Because the DBIE is not situated on top of LDD region, the transistor-like post-BD I-V characteristics for the BD MOSFET can still be seen. In this sample, R_g is $5.8\text{K}\Omega$ while the R_{gs} and R_{gd} are $14.6\text{K}\Omega$ and $9.8\text{K}\Omega$ respectively.

B. Kaczer *et al.* ^[71] reported that if the R_g is $< 30\text{K}\Omega$, the device suffered HBD. Our physical and electrical results show that even though R_g is less than $10\text{k}\Omega$, the transistor can still obtain a transistor-like I-V characteristic unless the DBIE is located very near the channel corner.

Fig. 5.12 shows the TSUPREME4 simulation results of a center DBIE BD. The simulation curves show symmetric characteristics in the post-BD device.

Fig. 5.12: TSUPREM4 simulated I_{ds} - V_{ds} characteristics with a 4nm doped Si filament situate near the poly-Si gate center. ^[88] (a) and (b) show a symmetrical I-V characteristic of the post-BD transistor.

After studying the two cases in the two previous sections, we can understand the DBIE effect on the post-BD I-V characteristics of a gate oxide BD small size transistor. The DBIE location is an important factor to determine the post-BD device performance. The impact of DBIE in BD transistor on circuit level functionality is still unclear.

5.6 Polarity dependent DBIE in MOSFETs

C. H. Tung *et al.* ^[79] has reported the polarity dependent DBIE in 25Å and 33Å BD devices. This phenomenon has been studied in thinner gate dielectric MOSFETs. 20Å gate oxide nMOSFETs were stressed in accumulation mode with various stressing compliance currents.

Figs. 5.13 (a) and (b) show the TEM micrographs of an nMOSFET stressed in accumulation mode using SCVS.

Fig. 5.13: TEM micrograph of a 20Å small size nMOSFET stressed under SCVS with final compliance current of 800μA. (a) Low magnification TEM image of a BD transistor. The BD location is close to one side of the device channel. (b) HRTEM image shows gate oxide thinning by a DBIE from the poly-Si gate to the Si substrate.

(a)

(b)

The HRTEM micrograph shown in Fig. 5.13(b) clearly indicates a localized gate oxide thinning due to the DBIE formation. According to the DBIE growth model, ^[18] a high leakage current running/surging through the breakdown path triggers DBIE, leading to the epitaxy nucleation. Because the nMOSFET was stressed in accumulation mode, an electromigration-like electron wind was introduced by a high-density leakage current from the poly-Si gate to the Si substrate.

In order to further analyze the polarity dependent DBIE on MOSFETs, pMOSFETs were stressed with inversion and accumulation mode. One example of pMOSFET BD induced microstructural damaged is shown in Fig. 5.14. The TEM results

indicate that the pMOSFETs BD can induce similar microstructural damage at the channel. The polarity dependent DBIE is also valid in pMOSFETs after gate oxide BD. The TEM images in Fig. 5.14 show that the DBIE has pushed gate oxide together into the Si substrate.

Fig. 5.14: (a) Low and (b) high TEM micrographs of a 20Å gate oxide small size pMOSFET stressed under CVS in inversion mode (-3.8V) with a compliance current of $100\mu\text{A}$. DBIE has grown from the poly-Si gate into the Si substrate. The dimension of the transistor is same as the nMOSFET ($0.3 \times 0.13\mu\text{m}^2$) shown in Fig. 4.12.

DBIE in pMOSFETs are almost half of the dimension as compared to that in nMOSFETs^[80]. From the DBIE point of view pMOSFETs should have better reliability as compared to nMOSFETs. In the analysis of pMOSFETs, it was found that the BD induces a high substrate current in transistor during the SBD transient. (See detailed analysis in chapter 4) In SBD, the effect of the high substrate current in pMOSFETs and coherent microstructural damage is still not very clear.

5.7 Conclusion

DBIE is a universal defect associated with the gate dielectric BD. Two types of BD transients have been observed. One is a slow transient and the other is a fast transient. In the slow BD transient, both DBIE growth and dielectric conductive path dilation affect the gate oxide BD hardness. In fast transient, thermal runaway with DBIE shorting the cathode and anode leads to a HBD. DBIE growth is also a strong function of the BD location. SBD and HBD show different types of DBIE on the BD MOSFETs. BD location can also affect the final post-BD IV curve. Even direct short occurs in the transistor channel, the transistor is still functional. Finally, polarity dependence of DBIE is still seen in both 20Å gate oxide p/n MOSFETs.

Chapter 6

Gate dielectric hard breakdown (HBD) induced microstructural damage in MOSFETs

6.1 Introduction

Numerous failure mechanisms associated with hard breakdowns in ultrathin gate oxides were physically studied by high resolution TEM. Migration of silicide from silicided gate and source/drain regions, abnormal growth of dielectric-breakdown-induce-Si epitaxy^[79], poly-Si gate melt-down and recrystallization, severe damage in Si substrate and total epitaxy of poly-Si gate and Si substrate of the entire transistor are among the common microstructural damage observed in MOSFETs after hard breakdowns in gate oxides. The type of catastrophic failures and its degree of damage are found to be strongly dependent on the allowable current density and total resistance of the breakdown path during the breakdown transient. The physical analysis data from TEM analysis allow us to establish the sequence of the physical damage associated with the gate oxide HBD in transistors.

6.2 Hard breakdown induced microstructural defects

6.2.1 HBD DBIE

As discussed in the previous sections, one of the consequences of gate oxide hard breakdown induced defect is the formation of Si hillock^[17] that is commonly

termed as dielectric-breakdown-induced-epitaxy, i.e. DBIE. As the hillock is epitaxy in nature and always occurs on the cathode of the stressed electrodes, the defect is also termed as polarity-dependent DBIE ^[79]. DBIE can grow rapidly and even propagate if the high voltage stress is maintained ^[92]. As a result, due to the presence of a huge mechanical stress at the DBIE/gate oxide and gate oxide/Si interfaces, the ultrathin gate oxide will eventually give way and rupture, leading to a HBD. This effectively creates an electrical short between the two stressed electrodes as the DBIE is epitaxial and “partially” doped in nature.

Fig. 6.1: TEM micrograph of a transistor ($W \times L = 0.3 \mu\text{m} \times 0.13 \mu\text{m}$) failed with HBD. The TEM results were obtained along the gate width direction. (a) A DBIE is clearly seen near the center of the transistor width direction. (b) High resolution TEM micrograph of (a) showing Si epitaxy formed on the Si substrate.

Fig. 6.1 shows TEM results cross section along its width direction from a HBD transistor. The DBIE location is near the center of the transistor width. The $I_d/(I_d + I_s)$ calculation indicates that the ratio is 0.82 that is closed to the device drain side along the length direction. Based on the TEM analysis, the DBIE damage size is estimated to be around 10-20% of the total transistor area.

It is worth mentioning that in the vicinity of the DBIE, substrate defects have been observed. An example is shown in Fig. 6.6. The detail will be discussed in a later section.

A thermal simulation was carried out by ANSYS to simulate the effect of a “heat source” in a $20\text{\AA}$ gate dielectric layer^[90]. From the simulation result in Fig. 6.2, the thermal gradient profile clearly shows that the heat generated from the “heat source” was dissipated to the surrounding area, leading to a rise of the surrounding temperature near the breakdown spot. After 500ns, the whole structure is heated up to a same temperature of 1384K. When the heating time is $350\mu\text{s}$, the heat center has arrived 1751K, which is beyond the Si melting temperature. Base on the previous chapter, we knew that the BD thermal effect generated a positive feedback loop with the breakdown current. If the stress condition i.e. $V_g \text{ stress}=4\text{V}$ for a $20\text{\AA}$ gate oxide is maintained, the leakage current can increase drastically in millisecond before a thermal damage runaway.

Fig. 6.2: Temperature evolution of a small size transistor structure in a “heat source” in the gate dielectric layer. The simulation results show the relationship between the transient times with the accumulated joule heating at the “heat source”. The results clearly show the local temperature increased from 635K in the first 100nS to 1751K when the transient time prolong to 350μS. ^[90]

6.2.2 Dielectric-breakdown-induced-migration (DBIM)

Once the gate oxide is ruptured by the presence of a DBIE, it may subsequently trigger several other severe microstructural damage. One of the important observations of the gate oxide breakdown related mechanism is the migration of the silicide materials from the neighboring Co/Ti-silicided Si areas. An example of such failure defects is shown in Fig. 6.3. The TEM results show that the DBIM phenomenon does not depend on the stress polarity. However, it is a strong function of the gate oxide breakdown location along the channel. In Fig. 6.3, DBIM occurs after the transistor exhibited a HBD-like failure. It is clear that Ti compound shown in the elemental map does not just migrate from both the Ti-silicided source and drain (i.e. the cathode side), it also migrates down from the Ti-silicide formed on top of the small size poly-Si electrode (i.e. anode side).

Similar results were observed for CCS (constant current stress) samples and Co-silicide technology, as shown in Fig. 6.4

Fig. 6.3: (a) TEM micrograph of gate oxide HBD damage in a 33 Å gate oxide of a Ti-silicided 0.18 μm nMOSFET for a current compliance set at 10 μA . (b) Elemental map of Ti of the region shown in (a).

From the thermodynamic and kinetics perspective, this is possible provided the “sink” of the migration is at a very high temperature than its surrounding. Tung *et al.* [79] has postulated that joule heating effects via the percolation non-linear network of the gate oxide breakdown path is so significant that the temperature in its vicinity can be even higher than the melting point of Si [65,70]. Hence, the thermal gradient between the Ti-silicide and the gate oxide breakdown site can be very steep that the HBD DBIE becomes an effective sink of the migrated Co/Ti compound that “segregates and diffuses” rapidly along the Si/oxide interface of the channel and poly-Si/liner oxide of the spacer sidewalls.

Fig. 6.4: Elemental map of Co obtained from a $0.20 \times 0.30 \mu\text{m}^2$ $20\text{\AA}$ gate oxide nMOSFET stressed in CCS in inversion mode. The stress fluence was kept at $500 \times 10^3 \text{A/cm}^2$.

It is believed that in DBIM, besides the extraordinary thermal gradient between the Ti/Co-silicided regions and the heat spot (i.e. the percolation path within the gate oxide), the high current density near the surrounding of the breakdown spot plays an important role in some secondary mechanisms. This includes mechanism similar to the thermal electromigration in which the silicide atoms from the cathode end are electrically driven and diffuse via the Si/oxide interfaces that have substantial dangling bonds. This secondary effect gives rise to a slightly enhanced migration of silicide from the cathode side. For example, as shown in Fig. 6.5, in nMOSFETs stressed in inversion mode, DBIM is slightly more pronounced from the source/drain deep junction as compared to those migrating from the poly-Si top.

Another possible mechanism is the presence of point defects created in the Si substrate (for nMOSFET stressed in inversion mode) due to the formation of DBIE. Since the point defects serve as an effective migration site, their presence in the cathode side as shown in Fig. 6.6 could serve as another driving force for more silicide migration in the cathode side.

Fig. 6.5: TEM electron energy loss spectrometry elemental mapping image of Co showing DBIM of Co compound from the silicided source and drain and poly-Si towards the HBD DBIE. This nMOSFET was CVS in inversion mode with a $400\mu\text{A}$ compliance current setting. More DBIM can be seen from the source/drain areas that are the cathode.

Fig. 6.6: HRTEM lattice image showing Si epitaxial growth at the breakdown point and its associated substrate damage regions in the Si substrate (marked by arrows) in nMOSFET. The SBD transistor was stressed with CVS with $1\mu\text{A}$ compliance current. The arrows indicate possible crystal defects such as vacancies in the Si substrate.

6.2.3 Melt-down and regrowth of silicided poly-Si gate

If the breakdown current is not controlled either by the presence of parasitic resistance such as external resistance or current compliance, due to the presence of the “doped”-DBIE ^[17] at the ruptured gate oxide region, the effective resistance between the stress electrodes will reduce dramatically. This further reinforces the magnitude of the maximum allowable stress current ^[92]. The chain reactions will likely result into a thermal runaway situation. Due to the fact that the initial temperature at the DBIE site is already extremely high, the localized temperature due to the presence of a much larger current density will be greatly enhanced within the very tiny poly-Si structure. Under this circumstance, other heat generation mechanisms such as thermionic emission phenomenon ^[65,70] could happen.

Fig. 6.7: Co-silicided poly-Si gate melt-down in a 20Å gate oxide nMOSFET stressed at 3.8V in inversion mode with a current compliance of 50 μ A. The melting is so severe that CoSi₂ has intermixed with the poly-Si materials.

Fig. 6.8: Poly-Si gate melt-down in a 33Å gate oxide nMOSFET stressed in inversion mode with a current compliance of 1mA. In this case, the original TiSi₂ on top of the poly-Si is totally absent.

Due to the poorer thermal conduction in the poly-Si gate, severe melt-down in the poly-Si lines always take place ahead of melt-down in the Si channel as well as source/drain deep junctions even though the melting point of poly-Si and Si(100) substrate is similar. Fig. 6.7 shows an example. In most cases, the destructive process is severe enough that the poly-Si melts and intermixes with the Co/Ti-silicide as shown in Fig. 6.8. In these cases, the localized temperature is expected to be close to or exceeded the undoped Si melting point of about 1415 °C. It is obvious that upon cooling down, the intermixed compound has regrown into a mixture consisting of Si and Co.

6.2.4 Damage in Si Substrate

Subsequent to the melt-down and regrowth of silicide and poly-Si mixture in the gate area, microstructural damage can possibly occur in the Si substrate even though much thermal energy generated at the breakdown spot can be readily conducted away via the high thermal conductivity Si substrate and the W-plugs of the source/drain contacts. Fig. 6.9 gives an example of an nMOSFET showing severe Si substrate damage after

failing with HBD in inversion mode. The following critical observations can be made in this case.

- 1.) The origin of the breakdown spot was traced to be located near the edge of the poly-Si line. This is similar to the DBIE seen in Fig. 6.1, which is the triggering point of the very massive multiple microstructural damage.
- 2.) DBIM and melt-down of the Co-silicided poly-Si lines had occurred. The intermix of the melt-down formed a mixed compound.
- 3.) New damage have occurred in the Si substrate and extended towards the right side of the breakdown spot. Hence, the damage in the Si substrate does not just confine to the area beneath the initial HBD DBIE site (see Fig. 6.9) at the breakdown spot near the gate corner, but it has propagated all the way into the gate channel regions.

Despite that a dramatic thermal event has occurred in the Si(100) substrate and poly-Si structure, the ultrathin gate materials of the unruptured gate oxide regions remain very much intact. As a result, the gate oxide effectively separates the re-grown poly-Si gate and the Si substrate damage. The highly strained ultrathin gate oxide sandwiched by the newly formed structures is expected to experience tremendous mechanical stress at its two interfaces after the deformation.

Fig. 6.9: TEM micrograph of a 20 Å gate-oxide nMOSFET stressed at 3.8V with a compliance current of 50 μ A. (a) The initial HDB DBIE near the poly-Si edge is shown by the circle. (b) HRTEM micrograph of the circle location. (c) DBIM and poly-Si gate melt-down were observed.

Fig. 6.10: TEM micrograph of (a) a 33Å gate oxide Ti-silicide nMOSFET stressed at 5.1V in inversion mode with a compliance current of 10μA, and (b) a 25Å gate oxide Co-silicide nMOSFET stressed at 4.4V in inversion with a compliance current of 1μA. The substrate damage is delineated by the dotted lines.

Fig. 6.10 shows a few more examples, showing severe Si damage, regardless of the silicide, gate oxide thickness and CMOS technology. These results illustrate that microstructural damage in the Si substrate can still be triggered by the ruptured gate oxide even the compliance current is not sufficiently high as compared to all the previous cases discussed. As shown in Fig. 6.11, similar phenomenon is consistently found in pMOSFET stress in accumulation mode.

Fig. 6.11: (a) TEM micrograph of a 20Å gate oxide pMOSFET stressed at 3.8V in accumulation mode with a compliance current of 1mA. (b) Elemental map of Co of (a). The entire channel and poly-Si gate were melted and mixed with DBIM Co compound. The heat generated by the breakdown is so pronounced that both source and drain regions have been electrically short either by DBIM and/or shorting of the source/drain regions. It is interesting that the TEM micrograph reveals that the gate oxide in most areas is still intact.

6.2.5 Recrystallization of Entire Transistor

The next level of physical damage associated with the gate oxide HBD is a massive gate oxide rupture besides the original DBIE. The entire process is so destructive that none of the original materials or structures such as the silicided poly-Si, gate oxide and channel Si can be distinguished or recognized after the breakdown event. Using the undamaged Si substrate as the precursor for the growth, upon cooling down of the intermixed material, a complete recrystallization of the entire poly-Si structure and the neighboring source/drain deep junctions, including the channel areas directly beneath the gate oxide, is realized. As shown in Fig. 6.12, the growth process is expected to take

via the original gate oxide BD spot. The TEM micrograph clearly demonstrates that the localized temperature in the vicinity of the breakdown spot is so high that it not only melts the poly-Si, Si ($T_m = 1415\text{ }^{\circ}\text{C}$) and CoSi_2 ($T_m = 1326\text{ }^{\circ}\text{C}$), but also the SiO_2 gate ($T_m = 1600\text{ }^{\circ}\text{C}$), that has a melting point substantially higher than its surrounding materials. However, in our experiments, this happens only when the compliance current setting is very high or unlimited.

Fig. 6.12: Total epitaxy of poly-Si gate with Si substrate. The compliance current is 100 mA. The gate oxide was 33 Å.

6.2.6 Implosion

The phenomenon of implosion has been rarely observed in a few TEM samples after gate oxide stressed failures. This could be one of the worst structural damage induced by CVS. As seen in Fig. 6.13, the poly-Si gate and its surrounding dielectrics have evaporated, leading to the formation of a void that can be readily seen in the neighborhood of the tinny transistor. In this particular sample, the test was carried out on a long serpentine (i.e. snake-like) structure. Thus the gate oxide area is much larger than other samples.

Fig. 6.13: Implosion is found after narrow transistor failed with accelerated voltage stress in the gate oxide. In this particular case, the sample was a snake-like test structure.

6.2.7 Other Transistor Related Structural Damage (W Plug Burnt-out)

Once all the possible structural damage associated with the transistor structure due to the thermal effects of gate oxide breakdown have accomplished, the next most vulnerable location(s) to suffer physical damage would be the device structures that have very high parasitic resistance and current *density*. This includes the interface between the W-plug contact and the poly-Si or source/drain active areas.

Fig. 6.14 shows an example of an evaporation of the W-plug in one of the source/drain contacts after the small size transistor has suffered HBD in the gate oxide. Even though W has a very high melting pointing of 3410 °C, it is evident that part of W materials in the plug has been melted/reacted. This is possible since the total effective resistance between the cathode and anode upon severe gate oxide rupture would be reduced dramatically. As a result, the effective current flowing along the breakdown path is expected to be extraordinary high. Based on the post breakdown I-V measurements,

these current values can be in the order of milli-amperes as compared to a few hundreds of nano-amperes to a few micro-amperes for SBD cases. For advance CMOS technology, the dimension of the W-plug is in the range of 130nm to 200nm. Hence, a substantial amount of joule heating is expected in the W-plug itself once the breakdown current surges to a very high value of the order of milli-amperes. It is not unreasonable to expect that the localized temperature in the plug goes beyond the W melting point of 3410 °C, resulting in partial evaporation of the W-filled contact plug. However, it is worth to note that not all HBD will eventually result in a W-plug destruction.

Fig. 6.14: TEM micrograph of a 20 Å gate-oxide nMOSFET stressed at 3.8V with a compliance current of 100 μA. The W-plug has already burnt-out.

Fig. 6.15 clearly shows that W materials in one of the contacts part of its connecting top copper metallization had melted intermixed and re-grown. As shown in Fig. 6.15, the thermal mismatch is so large the newly formed W and Cu compound broke away from the copper metallization of Metal 1. The absence of the contact hole in the interlayer dielectric SiO₂ is attributed to the solidification of the melted SiO₂ in the surrounding of the heated plug. This provides another evidence that the localized temperature has exceeded that of the tungsten melting point.

Fig. 6.15: TEM micrographs of an HBD in a 20Å gate oxide nMOSFET stressed in CVS at 3.9V. (a) The W and Cu materials of the left plug and top metallization have melted and recrystallized. (b) The copper in Metal 1 directly above the plug has disconnected.

Under favorable conditions, the localized heating, either from the percolation path or W plug or both, may have to be dissipated mainly through the Si substrate. This can happen if the metallization connections to the source/drain or and poly-Si are broken. Our recent finite element simulation results show that the source/drain contacts are in fact very effective heat sinks during the gate oxide breakdown transient. Fig. 6.16(a) confirms the hypothesis. Since the Metal 1 copper lines are disconnected, the Si substrate becomes the dominant path for the heat dissipation. It is believed that in this particular case, most of the heat energy during the later stage of breakdown was channeled into the Si substrate. The semicircle dark contrast directly below the failed small size transistor clearly demonstrates the thermal contours of the heat dissipation. In this rare examples, the post I-V characteristics reinforces that the substrate current sank all the gate leakage current while the current in the source/drain remained almost zero, i.e. broken connections.

Fig. 6.16: (a) TEM micrograph of a 20Å gate oxide nMOSFET stressed in CVS at 3.9V with no compliance current setting. (b) ANSYS simulation result shows that the MOSFET structure temperature can reach 3814K after the “heat source” is kept for 10ms+10μs^[89].

The analysis simulation result in Fig. 6.16(b) shows that the temperature contours in the second part of the transient thermal analysis, which makes use of the results at 10ms as the initial condition for HBD and applies a constant heat generation rate of $5 \times 10^{18} \text{ J/s.m}^3$ at the heat source^[90]. The final temperature can reach 3814K that is very close to the W melting point. The simulation result correlates well with the experimental result shown in Fig. 6.16(a).

6.2.8 “Explosion-like” Contact Failure

In an equally severe situation, the high temperature in the W-plug not only fuses at the weak point and melts the W materials, but the developed pressure is so great that it forces part of the unconnected plug materials to move as shown in Fig. 6.17. In this example, as the W-plug breaks nearer to the Si contact, it is expected that the lower

portion of the plug, which is smaller in size and easier to move as compared to the upper one, to move downward towards to the Si substrate. This extrusion process can be further accelerated if the Si substrate is already in molten phase upon absorbing much of the heat released from the plug since the surrounding SiO_2 of the inter-layer dielectric is a very poor thermal conductor. In Fig. 6.17, the disappearance of the seam formed during the CVD W process in the middle of the W-plug further supports that the broken W-plug has been melted and recrystallized during the melting process.

Fig. 6.17: TEM micrograph of a 20 Å gate-oxide nMOSFET stressed at 3.8V with a compliance current of 100 μA . The open in the W-plug is clearly seen. Noted that the dark patches in the Cu metals and near the W-plug areas are the FIB induced contamination artifacts.

On the other hand, much generated heat within the W-plugs will be conducted away through the top Al/Cu metallization and its silicided Si substrate. In this case, it is not surprised to understand the temperature gradient between the W-plug itself and the neighboring Si substrate is huge that W materials will preferentially migrate towards the Si active areas and reacts with Si to form compound. In view of the presence of the large thermal gradient for W migration and high localized Si

temperature, the thermodynamic reaction is greatly enhanced and accelerated. In addition, the participation of local electrical driving force in the formation of the W-silicide cannot be ruled out as well.

6.3 Model for Microstructural Damage of gate oxides HBD

The structural damage associated with HBD in gate oxide of very small size transistors can be summarized as shown in Fig. 6.18. The severity of each of the microstructural damage in MOSFETs is strongly dependent on the localized current *density* and resistance of the damaged site. Once the non-linear time-dependent percolation network in the gate oxide is diminished by HBD DBIE, the next structural damage will likely happen at an area in which the thermal effects are the most pronounced and dominant. The primary deciding factor is the localized current density and the resistance. Other secondary factors include the geometry and its surrounding materials, and the electrical driving force. Each of these factors plays a significant role in determining the next possible physical damage.

In summary, the sequence of events upon HBD in ultrathin gate oxide would be as follows:

- 1.) Formation of abnormally huge DBIE at the breakdown site. This DBIE ruptures the gate oxide;
- 2.) DBIM of the silicide material towards the “heat sink” with its center located somewhere near at the original HDB DBIE;
- 3.) Silicided poly-Si melt-down and regrowth. This happens if the localized temperature is above about 1300 °C and somewhere near 1400 °C; Severe damage in the Si substrate. This happens if the localized temperature is between 1400 °C and 1600 °C;

- 4.) Severe damage in the Si substrate. This happens if the localized temperature is between 1400 °C and 1600 °C;
- 5.) Further massive rupture of the gate oxide from the original breakdown spot and melting down of the entire transistor structure including the SiO₂ gate. The expected localized temperature is more than 1600 °C. The end result is the recrystallization of the melted intermix upon cooling;
- 6.) Implosion of the tiny transistor; and/or
- 7.) Severe damage in the W-plug contact.

Fig. 6.18: Sequence of structural damage associated with HBD in ultrathin gate oxide.

The results are summarized in Fig. 6.18. It is obvious even though not all defects can be seen upon HBD, but on the other hand, multiple microstructural damage in tiny sub-quarter micron Si devices are quite common if the compliance current setting in the constant voltage stress is not limited or is not set appropriately.

6.4 Conclusion

Based on TEM results, it is suggested that the HBD triggered microstructural damage in MOSFETs are strongly dependent on two parameters: 1) the localized current density and 2) the resistance of the leakage path. The sequence of the physical damage can be ascertained and described by Fig. 6.18. If an ESD-like protection system such as with the introduction of a high external resistor can be incorporated into the gate oxide breakdown path and limit the current flow at the initial stage of the gate oxide breakdown before the completion of the breakdown transient ^[18,92], it is possible to safeguard the gate oxide integrity, thus improving its reliability as well as leading to a more robust circuit.

Chapter 7

Conclusion and Recommendation

7.1 Conclusion

Ultrathin gate dielectric breakdown is one of the key reliability issues that affect the circuit function. Hence study of the breakdown induced physical structure change can provide more insights and knowledge to better understand breakdown phenomenon clearly. Based on the TEM results, it has been shown that the BD triggered DBIE growth plays an important role in the evolution of SBD to HBD during a BD event. The DBIE growth is a strong function of two parameters: 1) the localized current density and 2) the effective resistance of the leakage path.

In all of the stress modes studied, inversion mode stress causes the most severe damages in the stressed nMOSFETs. We suspect that the lowest effective resistance during the BD generates a suitable condition for DBIE growth that is the main root cause of the observed results. On other hand, based on the BD characteristics in pMOSFETs and nMOSFETs, for a given leakage, compliance current limit in SBD, it is found that the pMOSFET BD transient is always longer for the BD transistors. The higher substrate current during the pMOSFETs BD may play an important role in resulting in the lower HBD rate for a giving stressing condition.

In the physical study of nMOSFETs BD under inversion stressing mode, we classified the post-BD nMOSFETs into three regions, namely SBD, SBD+DBIE and HBD+DBIE. These three regions are attributed to the different microstructural damages seen by TEM in the BD nMOSFETs. In the initial phase, as the stressing compliance current limit is very low, percolation path dilation is believed to

contribute to the post-BD leakage current increment. The DBIE starts to grow with increasing compliance current limits, leading to a thinner Gox at the BD spot and an evolution of SBD to HBD in the stressed MOSFE. This phenomenon has been consistently observed for Gox in the range of 16Å to 33Å.

SCVS stress method has been proposed and applied in our BD study. SCVS has been found to be effective in differentiating the effect on DBIE and dielectric percolation path dilation. It is found that DBIE growth and dielectric conductive path dilation are complementary factors during a BD event. As the dielectric layer becomes thinner and thinner, the percolation path needs fewer defects to initiate. We thus expect that DBIE formation in the initial stage of very thin Gox BD event will be rare, which has been confirmed by our experimental results for thinner in the range of 20Å and 16Å.

From the BD transistor and TEM analysis, it has been shown that the BD location is an important factor in the formation of different types of DBIE. The poly-Si gate edge BD is always associated with higher thermal damages for a given stressing condition. This is because of a lower effective BD resistance through the source/drain, leading to a faster BD transient.

The BD location is also important in determining the post-BD MOSFETs characteristics. If a DBIE is formed at the MOSFET channel center, the post-BD transistor maintained a transistor-like characteristic on both drain current configuration measurements (swapping the applied voltage from drain and source). On the other hand, in Type I HBD, TEM analysis has confirmed that a DBIE has physically shorted the gate and substrate near the LDD region, causing the gate loose control towards the BD side. But, the post-BD I-V curves measured by swapping the S/D electrodes still showed transistor-like characteristics. This result indicates that various BD locations in narrow transistors have different strong

effects on the post-BD electrical performance. In Type II HBD, the MOSFET source/drain have been shorted together that is the worse case of narrow transistor HBD.

Finally, we studied the microstructural damages in HBD narrow MOSFETs. During HBD, migration of silicide from silicided gate and source/drain regions, abnormal growth of dielectric-breakdown-induce-Si epitaxy, poly-Si gate melt-down and recrystallization, severe damage in Si substrate and total epitaxy of poly-Si gate and Si substrate of the entire transistor are among the common microstructural damages observed in MOSFETs. The sequence of the physical damages has been ascertained and modeled.

7.2 Recommendations

1. For TEM analysis of BD nMOSFET stressed in inversion mode, DBIEs grow from the Si substrate to the poly-Si gate are correlated with BD hardness. Similar growth DBIEs have also been found in accumulation mode stress. However, the detailed study of DBIE in accumulation mode has not been carried out. The relationship between DBIE and stress method can be further investigated.
2. pMOSFET BD has not been studied as extensive as the nMOSFET BD. The slow transient in pMOSFETs is an interesting topic, which needs further analysis.
3. It is also found that BD can induce dopant redistribution. Dopant redistribution could be very important because fast dopant redistribution into the transistors channel can affect the performance of MOSFETs drastically. In order to study the dopant redistribution, further TEM and SCM analysis are needed. The main challenge is how to prepare a suitable sample.

4. Gox BD is found to strongly dependent on the allowable current density and total resistance of the breakdown path during the breakdown transient. If an ESD-like protection system can be incorporated into the critical gate device that limits the current flow at the initial stage of the Gox breakdown, it is possible to safeguard the gate oxide integrity, thus improve its reliability, leading to a more robust circuit.

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Appendix

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