Design of liquid-crystal-on-silicon and organic light-emitting device microdisplays

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2006

Tan, S. C. (2006). Design of liquid-crystal-on-silicon and organic light-emitting device microdisplays. Master's thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/3389>

<https://doi.org/10.32657/10356/3389>

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**DESIGN OF LIQUID-CRYSTAL-ON-SILICON
AND
ORGANIC LIGHT-EMITTING DEVICE
MICRODISPLAYS**

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School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Master of Engineering

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Statement of Originality

I hereby certify that the content of this thesis is the result of work done by me and has not been submitted for a higher degree to any other University or Institution.

21 MAR 2003

Date

TAN SOO CHIANG

Acknowledgements

I would like to express my sincere gratitude to my supervisor, Assistant Professor Sun Xiaowei, for his constant support, encouragement and patient guidance throughout my candidature. His insightful comments and suggestions are invaluable towards the completion of this work.

I would like to thank Mrs. Leong-Tan Min Lin, Mrs. Seow-Guee Geok Lian and Mr. Tsoi Mun Keong, Richard for their kind assistances in administration and support in EDA.

Finally I would like to thank my parents for their continual support throughout my studies.

Summary

Building display on silicon has been explored for its advantages of low power, high resolution and low cost of manufacturing. Using silicon allows complex and high-density circuits to be build on the same substrate as the display itself, eliminating off-chip interconnects to realize a Display-on-Chip (DOC). In addition, dense layout rules of CMOS processes allow pixels to be placed very close together. Regardless of reflective (Liquid-Crystal-on-Silicon (LCoS)) or emissive (organic light-emitting device (OLED)) displays, the aperture ratio typically of greater than 90% is attainable for most CMOS processes.

For Liquid-Crystal-on-Silicon microdisplay studied in this work, low power and frame-at-a-time are the main focuses. Common voltage (VCOM) modulation together with a new pre-compensation scheme and a simple pixel buffer were designed to realize a low working voltage (3.3V) for both the electronics and LC with frame-at-a-time refresh. Frame inversion was adopted as it gave better performance in microdisplay against crosstalks due to fringe electric field effect. Low power digital-to-analog converters with integrated Gamma correction using C-2C architecture were adopted in the design. A rail-to-rail op-amp in each column driver was designed to provide the drive for charging the storage element in each pixel cell. In addition, these op-amps also provide the pre-compensation network for the elimination of voltage offsets and non-linearity of the in-pixel buffers.

OLED is the hottest topic in recent years. OLED-on-Silicon is a strong candidate for microdisplay due to its attractive features of self-emissive, high luminescence efficiency and wide viewing angle. OLED is a current-driven device, requiring accurate current control to achieve good display uniformity.

Using silicon as backplane has a great advantage because CMOS circuits can provide reliable performance with very good linearity down to very low current levels. In this work, the OLED-on-Silicon microdisplay was designed with a common anode configuration. Namely, the designed OLED has an inverted structure in which the top metal of the silicon backplane acts as the cathode for the OLED. This arrangement also facilitates the use of low voltage supply for the display electronics.

In the design, a current mode digital-to-analog converter (DAC) was used to drive the pixel array. The DAC features current steering cells with improved noise performance. For the pixel design, a Lightly-Doped Drain (LDD) transistor was used to provide protection from the high voltage of the OLED for the low voltage driver circuit.

With the general design methodologies developed for the silicon backplane, a LCoS and an OLED-on-Silicon microdisplays were designed with QVGA resolution. The LCoS and OLED-on-Silicon microdisplays were fabricated on a 0.6 μ m process at XFAB, an external silicon foundry. The interfaces for the microdisplays consist of a 4-bit data input, a horizontal synchronization signal and a vertical synchronization signal. In addition, for the LCoS microdisplay, five external connections were provided for fine-tuning of Gamma correction.

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Chapter 1. Introduction

1.1 Motivation

The Cathode Ray Tube (CRT) has been the dominant display technology for many years, while Flat Panel Display (FPD) technologies, especially Liquid Crystal Display (LCD), have just emerged over the past decade and have been increasingly employed in many areas for information display. While LCD is predominantly used in portable applications such as notebook computers, it is slowly replacing CRT in many applications like desktop monitors and small-size to mid-size televisions [1]. This is because LCD is thin, flat and light, non-radiative and consumes less power. With the development of information technology, high-resolution displays that are portable or wearable are highly demanded. This need has enabled the development of miniature displays called microdisplays [2]. This type of displays is very versatile, and it can be used in projection displays such as rear-projection televisions and front-projection video projectors, or direct-view displays such as head-mounted displays, viewfinders and wearable computers. The scope of the thesis is to design such microdisplays.

The mainstream of microdisplays is to build microdisplay on silicon substrate directly, namely, Liquid-Crystal-on-Silicon (LCoS). LCoS provides a very economical solution for display systems due to the availability of CMOS technology. Unlike conventional thin-film-transistor (TFT) technology of amorphous or polycrystalline silicon, the superior performance of the CMOS process allows high-density integration of electronics and the display on a single chip, realizing a Display-On-Chip (DOC). Data drivers, data converters and

voltage/current references that are previously located off-chip in conventional displays are now being integrated on the same chip as the display, thereby eliminating interconnections and simplifying applications of the device in display systems. Low power and low voltage are the added advantages of migration to CMOS processes.

Development tools and libraries with proven designs of standard analog (e.g. operational amplifiers) and digital (e.g. logic gates) building blocks for CMOS circuits are readily available. The performance of a design can be verified even before the device is fabricated with the help of these advance CAD tools. A highly working device can be obtained from a single development cycle, reducing time and cost wasted on repeated design cycles.

LCoS microdisplays have been studied for around ten years. Commercial deployments in projectors, head-mounted displays and desktop displays have been realized. Microdisplays are starting to appear in consumer products such as viewfinders for digital cameras [3]. More applications are expected both in direct-view and projection displays.

The motivation for designing a new LCoS is towards low voltage and low power design. Current designs keep relatively high operating voltage for driving of the liquid crystal (LC) despite having built the display electronics with a low voltage design. Inefficiency in power consumption arises due to the need to supply two different voltages for the electronics and the driving of LC. The new LCoS design will attempt to realize a single, low voltage supply display.

Organic Light-Emitting Devices (OLED) has emerged as a potential candidate for flat panel display application. OLED has many attractive properties such as high luminous efficiency, low drive voltage, wide viewing angle and fast

response. Fabrication of OLED makes use of relatively simple processes, such as thermal evaporation and spin-coating, which are already well developed in the CMOS industry. As self-emitting devices, OLED proves to be much more power efficient than the non-emissive LCD. In addition, possible use of cheap materials like plastics, as substrate and low processing temperature have placed OLED in the spot light as an emerging technology for FPD.

Several research and commercial bodies have successfully built working prototypes based on OLED which showed very attractive features. While TFT based backplanes for OLED have been widely studied and published in literatures, reports on silicon-based backplanes remain rare. To date, only few publications described the display electronics related to the integration of OLED with silicon. Two well-known works are the commercially available device from eMagin [4] and a binary controlled OLED-on-silicon microdisplay from IBM [5]. A very recent paper presented at the IEEE Solid-State Circuits Conference in February 2002 described various circuit techniques developed at eMagin for their OLED-on-Silicon microdisplay [6].

1.2 Objectives

The main objective of this research is to develop the design methodology of silicon backplane for LCoS and OLED-on-Silicon. Another objective is to design and build prototypes based on the methodology developed. The designed prototype has a resolution of 320 x 240 (QVGA) for both LCoS and OLED-on-Silicon. The display accepts 4-bit digital data and is capable of displaying 16 levels of gray. Besides the 4-bit digital data, there are three control signals: a pixel

clock, a line (horizontal) synchronization signal, and a frame (vertical) synchronization signal.

The completed designs will be fabricated on a commercially available CMOS process. Circuit designs are to be verified using simulations with foundry supplied devices' models and layout will be done with foundry supplied design rules.

For the LCoS microdisplay, a single voltage supply operation for logic and LC driving will be developed. Improvement to the illumination duty ratio will be developed to increase the efficiency of the display system. Improvement to image flickers will be also studied.

For the OLED-on-Silicon microdisplay, efficient current mode DAC will be developed. Pixel designs that improve the uniformity of the image will be developed. The final design will operate from a low 3.3V supply voltage.

1.3 Major Contributions

The major contribution of this research is in developing the generic design methodology and in the designing and fabrication of the two backplanes for LCoS and OLED-on-silicon. In the design process, several new designs were introduced and implemented.

For the LCoS microdisplay, a new pre-compensation scheme has been developed to facilitate frame-at-a-time refresh operation. VCOM modulation and rail-to-rail in-pixel buffer allowed the full utilization of the logic supply voltage to switch the LC cell. The marriage of VCOM modulation and the pre-compensation in-pixel buffer scheme enables a 3.3V LCoS display to be achieved. This is

believed to be the first analog gray scale LCoS display to operate with such low voltage.

The proposed LCoS microdisplay design also improves light efficiency by using frame-at-a-time refresh to obtain higher duty ratio. As a result, flickering and color breaking problems will be greatly prohibited.

For the OLED-on-Silicon microdisplay, the entire design is performed using a low voltage 3.3V supply for the device. Current mode DAC with good linearity and simple architecture is developed. A pixel design that is process invariant is proposed to improve the uniformity of the displayed image.

1.4 Organizations of the Chapters

The motivations, objectives and major contributions of the research are presented in the first chapter. Subsequently, overviews of silicon backplane, LC and OLED are presented in Chapter 2. A brief description of the operating principles and research advances of the various technologies are included in this chapter.

The basic addressing operation for the microdisplays is introduced in Chapter 3. The timing relationship between the interfacing signals, and the sequence of addressing the display is explained. The design of the low power D flip-flop (DFF) is also covered in this chapter.

The design of the LCoS microdisplay is presented in Chapter 4. New developments such as the pre-compensation scheme and in-pixel buffer are presented. DAC with gamma correction feature, column operational amplifiers and bandgap reference are also described in this chapter. The frame-at-a-time refresh operation is explained in detail and the timing relationship for the operation is also

covered. At the end of the chapter, a simulation result based on a scaled down 4x4 matrix display is used to explain the working principles and performance of the completed design.

The design of the OLED-on-Silicon microdisplay is presented in Chapter 5. Analog circuits of the OLED-on-Silicon including the pixel and the DAC are discussed in detail with simulations results. At the end of the chapter, a scaled down 4x4 matrix microdisplay is used to present the results and performance of the completed design.

Finally conclusion for this thesis is presented in Chapter 6. Recommendations for further research works are also presented in this chapter.

1.5 Note on Schematic Figures in this Thesis

In this thesis, N-well CMOS processes are used. The N-channel transistors have fixed body connection to the common P-type substrate while the P-channel transistors reside in N-wells and have to be properly biased to ensure correct operation. For reading simplicity, the body connections of the P-channel transistors in the figures were not shown. For P-channel transistors used for switching operations as in digital logic circuits and transmission gates, the body connections were tied to the highest potential (V_{DD}) in the circuit. For P-channel transistors used in analog circuits like op-amps and voltage/current references, the body terminals were connected to the source terminals of the transistors.

Chapter 2. Liquid Crystal and Organic Light-Emitting Devices Based Microdisplays Built on Silicon

2.1 Silicon Backplane for Microdisplays

Silicon microdisplay has been a hot topic in recent years. Building displays on silicon substrate harnesses the full advantage of mature CMOS processes to produce high-quality, high information content devices. Complex circuitry and peripheral drivers can be integrated onto a single chip, providing a system-on-chip solution for display system.

Single crystal silicon CMOS has been the mainstream technology in integrated circuits due to the mature technology and stable, predictable performance that it can offer. The feature size of transistors has been shrunk well into deep sub-micron dimensions through years of continuous development, yielding higher packing density and faster circuit performance.

Single crystal silicon has more than three orders of magnitude higher electron mobility than amorphous silicon (a-Si). In addition, low resistivity interconnects and small die size reduce the R-C delays on the chip. Therefore higher performance electronics can be built on silicon. Availability of other integrated devices such as resistors, capacitors and bipolar devices allows various circuits to be housed on the same substrate, eliminating the need for off-chip interconnects to external drivers.

CMOS processes that are suitable for microdisplay applications must have at least three layers of metals. This is due to the physical constraint of the row, the

column and the pixel electrode. The first two metal layers will be used for the orthogonal layout of row and column interconnects, while the third metal layer is used as the pixel electrode. Although the polysilicon layer may be used for interconnect, the large die area of the microdisplay makes the resistance of the polysilicon too high for proper operation as interconnect. A few extra layers of metals would be advantageous to simplify routing but may not be necessary, depending on the complexity of the design.

The compact layout rules of the CMOS processes allow very fine pixel. Pixel dimensions of less than $10\mu\text{m}$ and high aperture ratio of greater than 90% are readily attainable for most processes.

In adopting CMOS processes for microdisplay applications, it is important to consider the effect of light induced electron-hole pairs. As the die will be exposed to light without any opaque encapsulation as in the case of normal integrated circuit packaging, special care has to be taken to avoid any circuit malfunction due to light-induced carriers. Fig. 2.1 shows the cross-section of a silicon backplane for microdisplay. An intermediate metal layer is used as a light shield to minimize the amount of light reaching the active devices. In addition, dynamic logic circuits that are sensitive to charge fluctuations are not suitable to be used in microdisplay designs.

Fig. 2.1. Cross-section of a CMOS backplane for microdisplay

In this work, a $0.6\mu\text{m}$ N-well, triple metal and double poly process from XFAB was adopted. This process offers a high resistivity polysilicon layer and

inter-poly capacitor as options. In addition, a Lightly Doped Drain (LDD) NMOS is available for high voltage application.

2.2 Liquid-Crystal-on-Silicon

Liquid crystal display (LCD) is a non-emissive display that works by modulating light passing through LC. Most LCDs modulate the polarization of light and need polarizers to function. Other LCD types (e.g. polymer-dispersed liquid LC, cholesteric LC and guest-host display) work by scattering or absorbing the light to modulate intensity.

The basic structure of a cross polarizers transmissive LC cell is shown in Fig. 2.2. The LC is sandwiched between two layers of glasses. A transparent thin film of conducting material, usually Indium-Tin Oxide (ITO), is fabricated by sputtering or some other suitable methods on each of these layers of glasses. These films form the two electrodes of the LC cell. Alignment layers (usually polyimide which is rubbed to set up the director of LC) are then fabricated ITO to set up the twist in the LC cell with a prescribed pre-tilt angle. In the absence of an electric field, the LC is in equilibrium state with minimum free energy. The LC can be visualized as a spiral staircase.

The operation of a normally white transmissive twisted nematic (TN) LC cell is as follows: light entering the LC cell is linearly polarized by the polarizer. In the absence of electric field, the LC cell changes the polarization of the light by 90° , the same as the LC twist angle. The analyzer, placed orthogonally to the front polarizer at the other end of the cell, allows light to pass through to yield a bright state. When a high enough electric field is applied to the cell, almost all LC molecules are aligned to the field and the polarization of light passing through the

cell is preserved. The analyzer blocks the light as the polarization is perpendicular to the polarization of the analyzer. This yields a dark state. Gray scales are generated at intermediate voltages applied on the LC.

Fig. 2.2. Basic structure of twisted nematic (TN) LC cell

In reflective LC cell, only one polarizer is needed to perform the function of polarizing and analyzing [7]. Fig. 2.3 shows the structure of such a cell. In this setup, the polarizer behaves like two parallel polarizers. The main advantages of this structure are the savings of one polarizer and brighter display. This structure is also suitable for LCoS application as the topmost metal of the CMOS backplane can be used as the mirror.

Fig. 2.3. Basic structure of reflective LC cell

Fig 2.4 shows the structure of a typical LCoS cell. The structure can be distinctly separated into two portions based on the fabrication. The first portion is the silicon backplane where the fabrication is entirely based on conventional CMOS process. This portion houses the display electronics. An extra Chemical-Mechanical Polishing (CMP) process can be adopted to obtain higher reflectivity.

Fig. 2.4. Typical LCoS cell

The second portion consists of the LC cells fabrication. In this portion, the LC cell is formed by adding a top ITO-coated glass with an alignment layer to the silicon backplane. Prior to this, an alignment layer is coated and photo-aligned on the silicon surface. Photo-alignment is a crucial process for LCoS, as the yield of rubbed LCoS is only around 30% [8].

Usually, full color display on LCD is obtained by fabricating color filters on top of the pixel cell. However, in LCoS, the fabrication of filters is difficult due to the small dimensions. As a result, the field sequential technique [9] is employed to obtain full color display from a monochrome display panel. The concept of field

sequential color is to display red, green and blue color frames sequentially. The human eye integrates the frames temporally to see a color image. The display device is required to operate at a very high speed for sequential color display. In order for the human eye to see a stable, flicker-free image, the composite frame refreshing rate must be higher than 60Hz. Since each composite frame is made up of three primary color frames, the actual frame rate required is 180Hz. This translates to a pixel clock rate of 142 MHz for a XGA (1024 x 768) display. With advance high-speed CMOS processes ($< 0.25\mu\text{m}$) available nowadays, this speed is easily attainable. Increasing the degree of data driver's parallelism can lower the frequency to a more manageable level for slower processes (sub $0.35\mu\text{m}$ processes).

There are two ways to obtain gray scales on LCoS: analog and digital. The former attains gray scales by accurate control of voltages applied across the LC cell to manipulate the polarization of reflected light. This is the method of interest in this work and will be discussed in detail in Chapters 4. The latter uses either temporal or spatial methods to display gray scale. Usually fast ferroelectric LC is used in this type of display [10, 11, 12].

LCoS has been studied for more than ten years [13]. In fact several companies have put LCoS into mass production. Some large OEMs have integrated LCoS into projection displays, near-to-eye displays and viewfinders in cameras. The low power operation for LCoS makes it a very attractive candidate in portable or wearable equipment like viewfinders for cameras [14], where it has seen tremendous growth in demand in the market.

2.3 OLED Microdisplay

OLED has been attracting very wide attention since its introduction by Tang & VanSlyke in 1987 [15]. The advantages of OLED include wide viewing angle, lightweight, low power, fast response time and high contrast. OLEDs operate on the principle of converting electrical energy into light, a phenomenon known as electroluminescence. An OLED cell consists of organic layers sandwiched between two electrodes. When voltage is applied to the cell, electrons and holes injected from the electrodes recombine in the organic layer to emit light.

Fig. 2.5. Basic structure typical OLED

The basic structure of an OLED is shown in Fig. 2.5. Electrons are injected into the electron transport material from a low work function cathode, such as Lithium (Li), Calcium (Ca) or composites such as Magnesium Silver (MgAg) to increase the effectiveness of electron injection [16]. Holes are injected from a high work function anode. Usually the anode is made of Indium Tin Oxide, which is typically deposited by sputtering. ITO is commonly used in the fabrication of liquid crystal display panels. The electrons and holes recombine at the interface between the hole transport layer and the emitting layer to produce light. Balanced electron and hole injection is crucial for OLED with high efficiency.

OLED can be broadly divided into small molecule and polymer types. Both types are widely studied and improvements have been reported regularly. Either of

the two types of OLED can be used for microdisplay. The choice of material does not affect the design of the backplane for the microdisplay.

Many works have been done to enhance the light emitting efficiency and lowering the operating voltage of the OLED. Inserting buffer layers between the cathode and the electron transport layer has been shown to be effective by incorporating a cathode buffer layer, the electron injection efficiency can be greatly improved and the OLED can operate at a lower voltage. Buffer materials that are proven to be effective include lithium fluoride (LiF) [17, 18], and diamond-like carbon (DLC) film [19]. Meanwhile insertion of anode buffer layers like LiF [20] and metallophthalocyanines (MPcs) [21] have also been shown to be effective in lowering operating voltages. A popular technique to improve hole injection is by spin coating PEDOT:PSS [22], a conducting polymer, between ITO and the hole transport layer. Other enhancements include using CuPc as electron transport [23], P-doped silicon for anode [24]. Recently, Huang et. al. reported a structure using P-doped and N-doped transport layers with appropriate blocking layers similar to a *pin* diode structure found in inorganic LEDs [25]. The results showed very high brightness at low voltages.

There are several methods to obtain full color display from OLED [26]. One of them is to use different emitting layers for the three primary colors [27]. However this method is problematic in that the three color-emitting layers have to be deposited. Inkjet printing seems to be a very promising technology for fabricating color polymer OLED without patterning of the pixels. The other methods are: filtering of white OLED with RGB color filters [28], down conversion of blue OLED [29], microcavity filtered OLED [30] and color-tunable OLED [31].

An OLED can be built onto a CMOS backplane quite easily with a little modification to the standard structure [32, 33]. As emitted light has to come from the ITO anode side, an inverted structure of the OLED would be unavoidable for OLED-on-Silicon. Fig. 2.6 shows the OLED-on-silicon with inverted OLED structure. In this figure, the topmost metal layer of the silicon backplane acts as the electron injecting cathode. An emitting layer of Alq_3 is deposited on top of the cathode first, followed by the hole transport layer. Finally the device is capped by an ITO layer that acts as the hole injecting anode. This inverted structure favors a common anode configuration of the pixel array. The cathode, being the metal layer in a CMOS process, can be patterned easily using standard processing steps. The subsequent organic layers only require a uniform coating to form the OLED structure. Since no patterning is required for the organic layers, processing steps are very much simplified.

Fig. 2.6. Basic structure of OLED-on-Silicon microdisplay

As mentioned in preceding paragraphs, additional layers may be inserted to improve the efficiency of the OLED. Buffer layers like LiF can be easily incorporated in the fabrication process. One problem associated with this inverted structure is the need to deposit ITO on top of the organic stack. It has been reported that sputtered ITO damages the organic layers in the process and the OLED showed little or no emission. Possible solutions include insertion of buffer

layers (e.g. CuPc) to protect the organic emitting layer, alternative deposition techniques to deposit ITO and replacement of ITO with other suitable anode materials.

Constructing the OLED using an inverted structure has another advantage besides better optical coupling. As the OLED array is common anode connected, a current sink is used to drive the OLED instead of a current source. This allows the display electronics to operate with a low voltage supply while the OLED supply can be high. This is illustrated in Fig. 2.7. The only requirement for the output device connected to the cathode of the OLED is to withstand the high voltage when the OLED is in the OFF state. (In the ON state, most of the voltage drop is on the OLED; therefore the output devices do not experience a high voltage between drain and gate). A CMOS process with Lightly-Doped Drain (LDD) transistors is well suited in this case for a low voltage display electronics and high voltage device drivers.

Fig. 2.7. Low voltage display electronic for OLED driving

OLED-on-Silicon is relatively new although OLED has been widely studied in recent years. Limited literature can be found on OLED-on-silicon and the design of the display electronics. To date, only two publications can be found

on this topic. One comes from IBM [34] which describe a digital mode display (on & off only) with memory using SRAM cells and another with limited circuit design details from eMagin describing a full color, OLED-on-Silicon microdisplay [6, 35,36].

Chapter 3. Addressing in Microdisplay

The addressing circuit of a display has the role of controlling the manner by which the image data is transferred into the pixel array. The scheme of addressing depends on the complexity and size of the display, and may be divided into three types. The first, direct addressing, connects each portion (or pixel) of a display directly to the driving electronics. This scheme is only applicable to display with limited number of segments or pixels such as the seven segments digit display. Obviously, direct addressing is not suitable for high-information content displays. The second type, passive matrix addressing, provides a more versatile addressing by connecting to rows and columns of a display. The pixels are activated row by row with low duty cycles. This type of addressing is limited to small pixel array as the duty cycle of the driving signal decreases with increasing pixel count.

For high resolution displays, the active matrix addressing is preferred. In the active matrix addressing scheme, there is a switch in each pixel to control the pixel data. Each pixel contains a storage element which could hold the pixel data with certain retention ratio. The active matrix addressing is obviously the right choice for microdisplays, which takes the full advantage of silicon CMOS technology.

3.1 Line-at-a-time Refresh

The digital driver designs are essentially the same for the LCoS and the OLED-on-Silicon microdisplays to perform the line-at-a-time refresh operation.

For LCoS, additional control logics are needed to perform the frame-at-a-time refresh operation. The details for LCoS’s frame-at-a-time refresh will be presented in Chapter 4.

In active matrix addressing, each pixel contains an access transistor connecting the pixel to the data line. Fig. 3.1 shows the schematic of a simple pixel circuit. This pixel is used to form the display by placing it in an array depending on the resolution required. Fig. 3.2 shows an $M \times N$ pixel array, where M is the number of columns and N is the number of rows.

Fig. 3.1. Simple pixel circuit for active matrix addressing

Typically, video data is progressively scanned. The image is scanned in a left to right, top to bottom sequence. As such, it is natural to assign the row lines as the access control signal for the switching transistor of each pixel and the column as the data line. In order to program the pixels of each line in a short time, each column has a dedicated driver to deliver the desired voltage or current to the pixel. A digital data buffer normally holds the data stable for the entire line period for the DAC in the column driver to perform the conversion and to drive the column line.

Fig. 3.2. Pixel array consisting of M x N pixels

Fig. 3.3. Block diagram of microdisplay

A block diagram of the microdisplay is shown in Fig. 3.3. The basic digital video signals that are supplied externally are the video data (four bits as in the design), the horizontal synchronization signal, vertical synchronization signal and the pixel clock. The timing relationship of the input signals is shown in Fig. 3.4.

Fig. 3.4. Timing relationship of input signals

A simplified 8x8 pixel array is shown in Fig. 3.5. This block diagram will be used to explain the operation of the addressing. First, the incoming four bits data will be transferred into the shift register by the pixel clock. The shift register performs the role of a serial-to-parallel converter. The shift register starts shifting the data from left to right on the rising edge of the horizontal synchronization signal. By the end of one horizontal line period, the shift register would have been filled with the data for the entire row. On the next rising edge of the horizontal synchronization signal, the entire row of data is transferred into the data buffer. The shift register will then continue to load the next row of data.

The data buffer will hold the data steady for one horizontal line period. During this period, digital-to-analog conversion is performed and the converted outputs will be programmed into the pixels. The pixels are activated by the row

scanner at the start of the horizontal period. The pixels remain connected to the column lines until the end of a horizontal period where the row scanner deactivates the present row and proceed to activate the next row of pixels.

Fig. 3.5. Block diagram of simplified 8 x 8 microdisplay

This data loading, conversion and programming sequence is repeated until the entire pixel array is updated with the image data. The operation is called line-at-a-time refresh as the data is programmed onto the pixel array a line at a time.

Fig. 3.6 and 3.7 show the timings for the shifting of digital data and scanning of the rows respectively. In Fig. 3.6, the data is transferred serially into the shift register on the rising edge of the pixel clock. On the rising edge of the horizontal sync signal, the data in the shift register is transferred in parallel to the data buffer. The data buffer will hold the data steady for one complete horizontal period.

Fig. 3.6. Timing relationship of shift register and data buffer

Fig. 3.7. Timing relationship of row scanner

Fig. 3.7 shows the timing diagram of the row scanner. In the figure, row E is a dummy signal that does not activate any pixel row. Row E is needed to create the first pulse in the row scanner that will be propagated down the rows. The reason for this arrangement is because the data buffer does not contain any valid data in the beginning of a frame. The data in the buffer is only valid on the second rising edge of HSYNC after the VSYNC signal.

The input to the first element in the row scanner (row E) is VSYNC. The row scanner is initiated by clocking VSYNC into the first element on the rising edge of HSYNC, as shown in Fig. 3.7. Subsequently the pulse is passed onto the next element on the next rising edge of HSYNC. This sequence activates the pixel array row by row. In the design, a reset operation is omitted in the row scanner in order to simplify the circuit design. Instead, the reset operation is achieved by cycling the row scanner through one frame of operation. Therefore the first frame upon initial operation may not show the correct image. But this may not be observable by our eyes, as it lasts only a few milliseconds.

The addressing circuit is based on the D-type flip-flop. The shift register, data buffer and the row scanner are built by the same D-type flip-flop. In microdisplay applications, dynamic logics are not suitable due to the presence of light-induced carriers. This is because the silicon die will be exposed to strong light, as the die is the display itself. Fig. 3.8 shows a simple example of a dynamic CMOS Domino logic circuit and its operation. The circuit operates in two phases. The first phase is the pre-charge phase. The clock input is grounded and the output node will be charged to VDD , as shown in Fig. 3.8(a). In the second (evaluation) phase, the node is either discharged (Fig. 3.8(b)) or isolated (Fig. 3.8(c)) depending on the inputs. In the third case of an isolated output node, the reliability of the logic will be questionable due to the change in charge by the light-induced carrier. Therefore, dynamic logic circuits are not suitable in microdisplay application, as the integrity of the logics cannot be ensured.

Fig. 3.8. Dynamic Domino logic circuit, a)precharge phase, b) precharged node connected to ground, c) precharged node isolated

Static logic circuits do not suffer from the effect of light-induced carrier because there is always a path to either one of the power supply rails in static circuit. Fig. 3.9 shows a static inverter where the output is either connected to ground (Fig. 3.9(a)) or VDD (Fig. 3.9(b)). Any light-induced carriers will flow into either one of the supply rails, thus preventing any alteration of logic states.

Fig. 3.9. Static CMOS inverter, a) output pull to VDD , b) output grounded

3.2 D-type Flip-Flop

The design adopted for the D-type flip-flop is of the transmission gate type (TG-DFF). The TG-DFF is a fully static, master-slave flip-flop formed by cascading two identical latches. The schematic for the latch element is shown in Fig. 3.10. The TG-DFF has the advantage of low clock to output latency, but has the drawback of high clock loading due to the large number of transmission gates present in the circuit, as investigated by Reference 37.

Fig. 3.10. Schematic of transmission gate type latch

Fig. 3.11. Operation of TG base latch, a) holding phase, b) program phase

Fig. 3.11 shows the operation of the latch. In Fig. 3.11(a), the ‘enable’ (refer to Fig. 3.10) signal is grounded. The input transmission gate is switched off. The feedback path in the latch is connected and the latch is in the hold state. In Fig. 3.11(b), the ‘enable’ signal is high and the transmission gate is switched on, delivering the input to the latch. The feedback path is disconnected and the input logic is programmed into the latch.

Cascading the latches in series realizes a D flip-flop, as shown in Fig. 3.12. It is obvious in the figure that the clock loading is high due to the large number of pass-gates in the circuit.

Fig. 3.12. TG D flip-flop form by cascading two latches

The effect of high clock loading can be reduced by gating the clock with an exclusive OR function of the input and output of the TG-DFF. Fig. 3.13 shows the configuration for gating the input clock. The rationale for doing this is that if the output is the same as the input, then there is no need for the circuit to change state. Hence the clock is terminated at the NAND gate and the load is greatly reduced. The power savings (or penalty) of the gated DFF depends greatly on the switching activity (1/total number of rows). The addition of the gating circuit introduces

extra overheads in power dissipation. Fig. 3.14 shows the simulation results of the power dissipation as a function of the switching activity. The simulation showed that power saving is achieved only when the switching activity is lower than 24%. The power saving increases as the switching activity is reduced.

Fig. 3.13. Gated clock TG-DFF

Fig. 3.14. Simulated power savings of gated TG-DFF over non-gated TG-DFF

For the microdisplay with QVGA resolution, the switching activity for the row scanner is less than 0.42%. Therefore a remarkable amount of power can be saved if the clock of the row scanner is gated.

As for the shift register, the gated-clock scheme is not used because naturally, the image data does not guarantee a low switching activity input.

In this chapter, the addressing of the microdisplays was discussed. The focus was on line-at-a-time addressing, which will be employed in both LCoS and OLED-on-Silicon microdisplays. The timings relationship is important for the proper operation of the display. The power consumption of a display depends greatly on the design of the logic circuits. A TG based DFF was presented and simulation was carried out to verify the power savings for gated DFFs.

Chapter 4. Liquid-Crystal-on-Silicon

Power consumption of a LCD is a great concern especially in portable equipment like personal digital assistants (PDA) and camera viewfinders. A low power display is highly desired for extending battery life in this type of equipment. In transmissive LCD, the backlight system consumes the most power, while in reflective LCD, the ambient light source external to the display provides the illumination and therefore no extra power is needed to drive a lamp for illumination. For reflective type display, the bulk of the power consumption comes from data driving. The driving method in the LCD depends greatly on the type of material, inversion schemes and refreshing methods employed.

This chapter will discuss the design of various circuit blocks essential for the microdisplay. Low voltage and low power will be the main emphasis in the design. Basic factors affecting the performance of a LC display will be presented first, followed by addressing and refreshing schemes.

A novel refreshing method, which combines frame-at-a-time refresh and VCOM modulation, was conceptually developed and possible implementations were proposed. The design of DAC with integrated gamma correction was presented together with an inversion scheme for reference voltages in the negative frame operation. Analog building blocks of op-amp with rail-to-rail capability and precision voltage reference were presented with simulation results. Finally a scaled down version of the microdisplay was used to show the workability and performance of the proposed refreshing scheme and building blocks.

4.1 LC Operating Voltage

The advantages of a low LC operating voltage are: firstly it lowers the power consumption directly associated with the driving of the LC cells; secondly, it allows a cheaper, low voltage driving electronics to be used for the display.

For a normally white display, the minimum voltage at which the dark state occurs determines the maximum operating voltage, while the white state voltage defines the maximum operating voltage for a normally black display. The operating voltage is determined by several factors, from LC material, pre-tilt and twist angles to usage of compensating films.

Fig 4.1 illustrates a typical Reflectance-versus-Voltage Curve (RVC) for a normally white, reflective mode LC. A threshold voltage, which is needed to overcome the intermolecular forces before the twisted molecules start to rotate, exists in the RVC, and is determined by two factors, the dielectric anisotropy ($\Delta\epsilon$) and the elastic constant (K_{11}), as shown in the following equation [38],

$$V_{TH_LC} = \pi \left(\frac{K_{11}}{\epsilon_0 \cdot \Delta\epsilon} \right)^{\frac{1}{2}} \quad (4.1)$$

Fig. 4.1. Typical reflectance-vs-voltage curve (RVC) for normally white mode LC

An example of LC mixture (ZLI-4792) with $K_{11} = 6.4 \times 10^{-12} \text{N}$, $\Delta\epsilon = 5.2$ will yield a threshold voltage of about 1.17V. The operating voltage for the LC starts from the threshold voltage since the LC does not response below the threshold. This characteristic will be exploited to design a low voltage display that is one of the foci of this work.

For a well-designed LC cell, a low voltage CMOS process is sufficient for the driving electronics of the display. For example, by keeping the LC working voltage below 5V, a normal 5V process can be used for the backplane design. If there is a requirement for a higher voltage, then additional process steps has to be added to provide high voltage transistors. These extra steps raise the cost of processing the silicon backplane.

4.2 Inversion Methods

In LCD, there is a need to apply alternating voltage to the LC cell in order to prevent charge accumulation. If the charge is allowed to build up, the display will eventually fail due to electric field shielding.

Fig. 4.2. Polarity inversion methods: a) conventional method, b) VCOM modulation

The charge neutralization is achieved by applying the driving voltage in two phases. In the first phase, a positive potential is applied to the LC cells and in the second phase, an equal and opposite potential is applied for the same duration

to cancel the charge accumulated in the cell. The voltage polarity reversal is normally obtained by fixing the common cathode voltage (VCOM) at a midway voltage ($VDD/2$) between the supply voltage (VDD) and ground. In this way, a positive potential is presented across the LC cell when the applied voltage is between $VDD/2$ and VDD , while a negative potential is achieved when the applied voltage is between GND and $VDD/2$. In this method, the supply voltage needed for the display will be twice the operating voltage of the LC.

The polarity of the applied voltage can also be inverted by changing the voltage of the common cathode. This method is called VCOM modulation [39]. In this method, instead of fixing VCOM at a midpoint voltage between the supply rails, the common cathode is switched from ground (GND) to the supply voltage (VDD). A negative potential is achieved when VCOM is at VDD and a lower voltage is applied on the other plate of the LC. This scheme allows a lower supply voltage to be used for the display - half of that in the previous method. Since power is proportional to the square of the supply voltage, remarkable power savings can be achieved. Fig. 4.2 shows the polarity inversion for the two mentioned methods.

The voltage inversion can be applied to the display in four schemes: dot inversion, column inversion, row inversion and frame inversion. In dot inversion, polarity inversion is applied to every other pixel, as shown in Fig. 4.3(a). In column inversion, every other column of pixels is inverted; while in row inversion, every other row of pixels is inverted, as shown in Fig. 4.3(b) and Fig. 4.3(c). In frame inversion, the pixels are inverted every other frame, as shown in Fig. 4.3(d).

In the normal method of polarity reversal by fixing VCOM at a mid-voltage between the supply rails, the common cathode is always fabricated as a

single un-patterned layer regardless of inversion scheme. However, in the case of VCOM modulation, the fabrication of the common cathode may require patterning for some of the schemes. In dot inversion, the common cathode has to be patterned in a checkerboard fashion, where every alternate pixel is connected. This type of connection is impossible with a single layer of conductor. In column inversion and row inversion, the common cathode has to be patterned in vertical and horizontal strips respectively.

Fig. 4.3. Inversion schemes, a) dot inversion, b) column inversion, c) row inversion, d) frame inversion

The patterning of common cathode is undesirable because additional process steps will add to the cost of the manufacturing process. In the last method of frame inversion, there is no need to pattern the common cathode as the whole of the common cathode can be switched to achieve VCOM modulation. Therefore it is desirable to select the frame inversion scheme when VCOM modulation is used. Furthermore, it has been shown that frame inversion is the most suitable inversion method for microdisplay [40, 41]. This is because the pixel is very fine in

microdisplay ($10\mu\text{m} - 100\mu\text{m}$ square); fringe electrical field effect is strong enough to cause undesirable artifacts.

4.3 Refreshing Methods

Fig. 4.4. Simple pixel circuit for typical active matrix LCD

Fig 4.4 shows a simple pixel cell in a typical LCD. The access transistor acts as a switch and controls access to the capacitor that acts as a storage element in the cell. During the refresh operation, the transistor is turned on and the storage capacitor is connected to the column driver. The desired voltage, which modulates the LC cell to present gray scale, will be programmed onto the storage capacitor. Then the access transistor will be turned off and the storage capacitor holds the voltage representing the gray. The charge stored in this capacitor will leak with time and the voltage on the capacitor will be changed. Once the voltage changes, the pixel no longer present the correct gray scale. As a result, the storage capacitor has to be reprogrammed again before the voltage drops to an unacceptable level. This defines the minimum refresh rate of the display.

The refresh operation is normally carried out in a line-at-a-time manner, where a single row on the pixel array is activated at any time by turning on the

access transistors. Each pixel on the activated row is connected to a column driver that will program the required voltage into the storage capacitor. A horizontal line period is needed for the programming operation to complete. Subsequently, the next row of pixels in the array is activated while the present row is deactivated. The activation, programming and deactivation actions are repeated until the entire pixel array has been completely updated with the image data.

The line-at-a-time refresh operation contributes to flickers because of the scanning motion. If the whole image can be refreshed in a single instance, the perceived flickers will be significantly lowered due to the absence of the scanning motion. And since the image is stable for a longer time in frame-at-a-time refresh, the contrast and brightness of the image is also improved significantly. In order to achieve this frame-at-a-time refresh effect, frame buffers is needed to store the entire image before it is transferred to all pixels [42].

Fig. 4.5. Schematic of pixel with in-pixel buffer for frame buffering

Fig. 4.5 shows a pixel design with an in-pixel buffer, an intermediate storage capacitor and an isolation switch (transfer transistor) in addition to the usual access transistor and (final) storage capacitor. The intermediate storage capacitor serves the function of frame buffering by holding the image data while

the line refresh operation is in progress. The transfer transistor acts as a switch to isolate the intermediate storage capacitor from the final storage capacitor. When the entire frame of data has been written into the frame buffers, the final storage capacitors are connected to the in-pixel buffers through the transfer transistors, activated by a global signal. Voltage in the frame buffer is replicated onto the final storage capacitor by the in-pixel buffer. In this way, the image appears on the display in a single instance, instead of one line at a time. The frame buffer also allows the present image to be viewed while the next frame is being loaded in the background, therefore the time that the image is stable and viewable is significantly longer than that of the line-at-a-time refresh. This frame-at-a-time refresh is especially attractive for field sequential color application. [43]

The in-pixel buffer has to be compact to fit within the area available for a pixel. Previous works [44, 45] describe circuits which perform the function. However, these circuits suffer from charge redistribution, voltage offset or require discharge phases which increase complexity of the design.

In this chapter, a new pre-compensation scheme is proposed. The pre-compensation scheme circumvents the mentioned problems by adopting a correction arrangement in the column driver to compensate for any offset or non-linearity introduced by the in-pixel buffer. With this scheme, the design of the in-pixel buffer circuit is very much relaxed, since any offset or non-linearity is pre-compensated in the column driver and the buffer will always deliver the correct voltage to the final storage capacitor.

Fig. 4.6. Pre-compensation setup in column driver with in-pixel buffer

In this new scheme, an operational amplifier is included in the column driver. Fig. 4.6 shows the configuration of the operational amplifier circuit where an identical in-pixel buffer has been included in the feedback path. By the feedback loop action of the operational amplifier, the output voltage of the in-pixel buffer is always equal to the reference input at the positive terminal of the operational amplifier. The voltage at the input of the in-pixel buffer is adjusted to provide the match. This voltage is programmed onto the intermediate storage capacitors during the line-at-a-time refresh operation. On the activation of the global refresh signal, the in-pixel buffers will charge the final storage capacitors to the correct reference values.

Fig. 4.7. Push-pull driver as in-pixel buffer

Fig 4.7 shows an in-pixel buffer in the form of a push-pull buffer. The output characteristic is shown in Fig. 4.8. This design offers a very compact layout, with only two transistors and the push-pull buffer has excellent driving capability. The major drawback of this design is the non rail-to-rail output swing, as shown in Fig. 4.8, which makes it unsuitable for low voltage design. Fig 4.9 shows a variation in which the supply to the buffer can be shut off to reduce power dissipation.

Fig. 4.8. Output characteristic of push-pull buffer

Fig. 4.9. Modified configuration with push-pull buffer for low power operation

The output swing of the buffer can be improved by adopting a source follower design. Fig 4.10 shows a PMOS version where the output swings from V_{thp} to VDD , while Fig. 4.11 shows a NMOS version where the output swings from GND to $(VDD - V_{thn})$. Both the active load can be shut off to conserve power by pulling the gate bias to GND and VDD for the NMOS and PMOS respectively.

It should be noted that the threshold voltage of the transistor is not constant if the transistor is not residing in a well. In the case of a N-well process, the NMOS transistor suffers body effect and the threshold voltage increases with increasing source-to-body potential. Therefore it is more advantageous to use the PMOS source follower in such a process. The transfer characteristics of PMOS and NMOS buffers are shown in Fig 4.12 and Fig. 4.13 respectively. The difference between the input and output voltages for the NMOS follower varies throughout the operating range.

Fig. 4.10. PMOS source follower as in-pixel buffer

Fig. 4.11. NMOS source follower as in-pixel buffer

Fig. 4.12. Output characteristic of PMOS source follower for a N-well process

Fig. 4.13. Output characteristic of NMOS source follower for a N-well process

The RVC shown previously in Fig 4.1 reveals a threshold voltage at which the liquid crystal cell starts to response. This property of the LC is exploited in the next buffer design to enable the maximum utilization of the supply voltage. The circuit configuration is shown in Fig. 4.14. In this design, the buffer has two active load transistors which are activated accordingly in each frame. In the positive frame (with VCOM grounded), the PMOS load is activated by biasing the gate with a voltage which corresponds to the reference current, while the NMOS load is grounded to deactivate it. The buffer now operates from V_{thp} to VDD which covers the operating range of the LC. The LC threshold is dependent on several factors which can be optimized so that the threshold falls within the output range of the buffer. In the negative frame, the NMOS load is activated while the PMOS load is deactivated and the buffer swings from GND to $(VDD-V_{thn})$. The same bias is

applied to the buffer in the op-amp feedback loop to provide the compensated voltage to be stored on the intermediate storage capacitor.

Fig. 4.14. Novel wide swing buffer as in-pixel buffer

The simulated output characteristic of the buffer is shown in Fig. 4.15. The separate bias arrangement for the PMOS and NMOS loads creates a pseudo rail-to-rail operation for driving the LC. In this way, the entire range of the voltage supply can be utilized to drive the LC.

Fig. 4.15. Output characteristic of wide swing buffer

4.4 Gamma Correction

The LC’s reflectance response is nonlinear with respect to the voltage applied to the cell. In order to obtain a good gray scale that is required for accurate color display, gamma correction is needed to compensate for the nonlinear reflectance-voltage response.

The RVC shown in Fig 4.16 is of a typical reflective LC mode. The gamma correction is to be incorporated into the digital-to-analog converter. By defining several reference points on the curve and interpolate linearly between the points, a piece-wise linear curve is obtained which matches closely to the RVC. The result is shown in Fig 4.16. In this figure, the reference voltages are set at the 2%, 20%,

50%, 80% and 98% reflectance on the RVC. For a 4-bit gray scale display, each pair of these references will be interpolated to obtain four linear voltages in between them. From these five references, 16 distinct voltages corresponding to 16 gray scales can be obtained. The use of five reference voltages to provide four piece-wise segments provides good matching to the actual RVC. For higher degree of accuracy, more segments can be used. Similarly, for more gray scales, more points can be interpolated between the segments or more segments can be defined.

Fig. 4.16. Gamma correction references on the RVC

The selection of the reference voltages discussed in this section is based on a floating reference design. The first and the last reference voltage can be fixed to the supply rails (*GND* and *VDD*) to reduce the number of references to three. The floating reference arrangement provides a more flexible design to alter the fitting of the RVC. In addition, the operating voltage range of the LC can be reduced to facilitate low voltage operation. In Fig. 4.16, the first and last references are fixed at about 0.9 V and 3.1 V respectively. This arrangement enables the display to work rail-to-rail at a low supply voltage of 3.3V.

The interpolation of voltage levels in between the references can be achieved by a DAC. Alternatively, it can be achieved by resistor strings to provide all the voltage levels. Fig. 4.17 shows such a setup. Reference 46 proposed a low power resistor string by optimizing the values of the resistors in the string.

Fig. 4.17. Resistor string for gamma correction references

The light modulating function of the LC cell is wavelength dependent, therefore independent RVC exist for each of the three primary colors. In a single LCD, field sequential color application, it is necessary to change the reference points to provide the corresponding RVC for that color. Reference 40 had

demonstrated such a system to dynamically change the reference voltages for the gamma correction.

4.5 Color Display Using Field Sequential Color Technique

Display systems using single monochrome panel for full color display generally rely on field sequential color technique [47,48]. In this technique, every composite color frame is made up of red (R), green (G) and blue (B) sub-frames, which are displayed sequentially. The human eye integrates the RGB sub-frames to form a color image. High refresh rate is essential to produce a flicker-free and stable display. The illumination sources usually consist of light-emitting diodes (LED) for miniature displays or arc lamp with rotating color wheels for projection displays.

The illumination period for a field sequential color display is very short. The illumination source is only lighted up after the refresh operation has completed for a frame. Fig. 4.18 shows the timing relationship for the field sequential color operation. In this figure, the illumination period is made to coincide with the vertical flyback period that is typically found in analog video signal. This arrangement enables the maximum usage of available time, and was demonstrated in Reference 49. However the lighting period is extremely short. Due to the low duty ratio of the illumination phase, the light source had to be driven with a very high intensity pulse in order to maintain the brightness and contrast of the display. Also the refresh rate has to be high to avoid color-breaking problem.

Fig. 4.18. Timing relationship for field sequential color operation

In order to overcome the low duty ratio, a technique called scrolling color is being used in some display systems [50]. In this technique, the light source is filtered by a specially created color wheel. The color wheel is made such that the illumination on the display panel appears sequentially on a line-by-line basis. By synchronizing the illumination to the line refresh frequency, a very high duty ratio for the illumination can be attained. It was reported in Reference 51 that an illumination duty ratio as high as 95% could be obtained. Fig. 4.19 shows the timing diagram for a scrolling color illumination.

Fig. 4.19. Timing relationship for field sequential color operation using scrolling color illumination

Although the duty ratio is high for the scrolling color illumination technique, the need for precise synchronization of the illumination sequence to the line refresh operation poses difficulty in implementation. In addition, such a technique is not suitable for miniature display systems due to the large physical size of the scrolling light source.

The frame-at-a-time refresh can improve the illumination duty ratio very significantly with normal illumination. Fig. 4.20 shows the timing diagram of the field sequential color operation for a frame-at-a-time refresh display system. Due to the short refresh time which can be made to coincide with the vertical flyback period and restricted to the LC response time, the illumination duty ratio can reach 90%. For this implementation, the light source can be a simple LED.

Fig. 4.20. Timing relationship for field sequential color operation with frame-at-a-time refresh

4.6 Silicon Backplane for LCoS Microdisplay

The backplane for the LCoS was designed with the objectives of achieving low power and low voltage. As presented in preceding section, this can be achieved with a combination of frame-at-a-time refresh and VCOM modulation. The full range of supply voltage can be used with the proposed novel rail-to-rail in-pixel buffer.

Fig. 4.21. Timing relationship for second phase of frame-at-a-time refresh operation

The basic line-at-a-time refresh operation that was discussed in Chapter 3 is the first phase operation required for performing the frame-at-a-time refresh. Fig. 4.21 shows the timing diagram for the second phase operation where the frame transfer takes place. The global refresh (GR) signal is in phase with the vertical synchronization signal (VSYNC). The VSYNC signal also triggers the change of VCOM.

Fig. 4.22. Schematic of pixel design for LCOS microdisplay

Fig. 4.22 shows a schematic of the pixel design used for the LCoS microdisplay. As shown in the figure, the capacitors were implemented using MOS transistors because they offer the highest capacitance per unit area as compared to the other types of capacitors (inter-poly capacitors and inter-metal capacitors) in the process. Although this type of capacitor exhibits a non-linear voltage dependent characteristic, the application in this case ensures proper operation by driving the voltage and the capacitance with the in-pixel buffer until a stabilized operating point is obtained. The access transistor and the transfer transistor were replaced with transmission gates to eliminate threshold voltage drops.

Fig. 4.23 shows the detail of the in-pixel buffer with bias control. A frame control signal determines the bias to be generated for a specific frame. When the frame control is “HIGH”, it represents a positive (P) frame and the bias for the

PMOS load is generated and delivered to the buffer. The NMOS bias is grounded to deactivate the NMOS load. When the frame control is “LOW”, it represents a negative (N) frame and the bias for the NMOS load is generated. The PMOS bias is pulled to V_{DD} to deactivate the PMOS load. The activation of the load bias coincides with the VSYNC signal to ensure that the in-pixel buffer is only active when frame transfer is needed. At other times, the in-pixel buffer is disabled to reduce power dissipation.

Fig. 4.23. Bias control for in-pixel buffer

The same in-pixel buffer is inserted in the feedback loop of the column op-amp with the same bias control. Fig. 4.24 shows the column op-amp with the in-pixel buffer. The bias control section is shown in the figure as well. The bias is set according to the particular frame that the refresh operation is carried out. Fig. 4.25 shows the timing diagram for the bias control. In this diagram, the “op-amp frame” signal shows one horizontal period delay because in the line-at-a-time refresh

operation, the data is always delayed by one horizontal period to accommodate the serial-to-parallel conversion of the input data.

Fig. 4.24. Column op-amp with in-pixel buffer as feedback element

Fig. 4.25. Timing relationship for bias control

4.7 Digital-to-Analog Converters with Gamma Correction

In order to integrate the gamma correction feature into the DAC, the DAC was separated into two parts. The first part consists of a network of switches that select the appropriate range of voltages for correct gamma correction. The second part consists of a C-2C DAC [52] that will divide the selected range of voltages into equal levels linearly based on the input digital code. The C-2C DAC is adopted because of the low power feature. Other resistor based and current-scaling based structures require constant flow of current during operation, whereas the capacitor-based DAC only charges or discharges in the switching phase. In addition, the C-2C structure allows easy implementation of the gamma correction

function. The structure of the DAC with integrated gamma correction is shown in Fig. 4.26.

Fig. 4.26. Structure of DAC with built-in gamma correction

In order to provide reference voltages for both the positive and negative frames, the reference inputs are buffered with difference amplifiers as shown in Fig 4.27. In the positive frame, the difference amplifier acts as a unity gain buffer, while in the negative frame, the difference amplifier subtracts the reference voltages from VDD to provide the inverted references.

Fig. 4.27. Difference amplifier for providing voltage references

The selector is implemented using transmission gate which eliminates transistors' threshold voltage drop across the input and output terminals. Dummy

switches are inserted to compensate for the finite voltage drop across the switches. The two most significant bits are used to select the appropriate voltages from the five supplied reference voltages. Fig. 4.28 shows the schematic of such a selector.

Fig. 4.28. Schematic of voltage selector

The main requirements for the DAC are compact and low power. In a QVGA display, there are 320 of such DACs needed and the power and area consumption will be significantly high if the design is not compact and low power.

The C-2C structured DAC consumes very little power because the only power dissipation comes from charging and discharging of the capacitors. The inter-poly capacitors available from a double-poly CMOS process offer low leakage and good linearity. The switches used are similar to the selector's transmission gates as shown in Fig. 4.28. This switch configuration with complementary pair reduces the charge redistribution. The effect of charge redistribution caused by switching is also minimized by optimizing capacitances.

An important feature of the C-2C structure is the number of capacitors needed increases linearly with the number of bits. The number of capacitors needed for a N-bits DAC is given by the following equation:

$$\text{total no. of caps.} = (N - 1) \cdot (C + 2C) + (2 \times C) \quad (4.2)$$

For a two bits DAC, the capacitors needed are one $2C$ and three C , and for a six bits DAC, the total number of capacitors needed are five $2C$ and seven C . Therefore the number of capacitors increase linearly with the number of bits. This feature makes it easy for future modifications of design to include higher order DAC. This is contrary to most DAC structures like the resistor string type where the components increase exponentially with higher number of data bits.

The basic operation of the C-2C DAC is illustrated in Fig 4.29. This figure shows a simplified architecture with a single reference, V_{ref} . By applying superposition theorem and considering only one bit at a time, the output voltage can be determined. Fig. 4.30(a) shows the equivalent circuit with LSB switch $b0$ connected to V_{ref} and switch $b1$ connected to GND . The voltage at the output node is given by:

$$V_{out} = \frac{1}{4} \cdot V_{ref} \quad (4.3)$$

Fig 4.30(b) shows the equivalent circuit with switch $b1$ connected to V_{ref} and switch $b0$ connected to GND . The voltage at the output node is given by:

$$V_{out} = \frac{1}{2} \cdot V_{ref} \quad (4.4)$$

Fig. 4.29. Structure of a 2-bit C-2C DAC

Fig. 4.30. Equivalent circuit of DAC when, a) switch b_0 is closed and b_1 is opened,
b) switch b_0 is opened and b_1 is closed

The C-2C DAC is sensitive to residual charges in the capacitors and therefore a reset operation is needed to discharge the capacitors prior to a conversion.

4.8 Rail-to-rail Input and Output Op-amp

In the design of the microdisplay, a compact and low voltage design is required. Rail-to-rail operation is necessary to make full utilization of the power supply. A compact rail-to-rail op-amp from Reference [53] is adopted with some modifications to suit the microdisplay application.

The op-amp can be split into two parts for design consideration. The first part is the input stage and the second part is the output stage. In order to achieve rail-to-rail input, the following requirements must be met for the input stage:

1. To reach the negative supply rail, PMOS transistors must be used while keeping the drain voltages close to the ground.
2. To reach the positive supply rail, NMOS transistor must be used while keeping the drain voltages close to the supply voltage.

Fig 4.31 shows an op-amp circuit with the rail-to-rail input. The PMOS transistors are active for input range from ground to the positive supply minus the gate-source voltage $|V_{GS}|$ and the saturation voltage $|V_{DSsat}|$ of the tail current source, while the NMOS transistors are active from the positive supply down to the sum of V_{GS} and V_{DSsat} above ground.

Fig. 4.31. Input stage of rail-to-rail op-amp

The gain of this input stage varies over the common mode input range due to the different level of activation of the transistors at different common mode voltage. The value of the transconductance of this input stage can be divided into three ranges, as shown in Fig. 4.32.

Fig. 4.32. Value of transconductance (g_m) of the input stage

Although there are methods to maintain a constant gain over the entire range of common mode input, it is not necessary in this application. The op-amp in this design works only in DC mode; the AC distortion and performance is not of much consideration in this case although the gain does affect the settling time and offsets of the op-amp. However these effects are negligible in designing driving circuit for LCoS.

The output stage of the op-amp is shown in Fig. 4.33. This stage consists of the current summing circuit for the input stage and a Class AB output stage capable of rail-to-rail voltage swing. The biasing circuit for the Class AB stage is integrated into the current summing circuit, comprising of M7-M10 and M11-M14. The bias voltages $V1$ - $V2$ and currents $I1$ - $I2$ are global sources that provide biases for all the op-amps in the microdisplay. The total number of transistors needed for each op-amp is only 20. The output driver is formed by M19 and M20,

configured in a Class AB inverting buffer. The final compact op-amp schematic used in the design is shown in Fig. 4.34.

Fig. 4.33. Output stage of op-amp with class AB bias control

The bode plot of the opamp is shown in Fig. 4.35. The op-amp performance is satisfactory with an open loop gain of 76.9 dB at a load of 1pF and 1M Ω . The gain margin is 11 dB and the phase margin is 45°.

Fig. 4.36 shows the simulated gain of the op-amp at three different common mode input voltages of 0.5V, 1.65V and 2.8V. As mentioned earlier, the gain is varying due to the shift in gain of the input stage. It can be seen that the lowest gain of the op-amp at low input voltage is still high at 56 dB, which still yield tolerable error voltage.

Fig. 4.37 shows the step response of the op-amp when configured as a unity buffer with a 1pF load. Results for input of 0.1V, 0.875V, 1.65V, 2.425V

and 3.2V are shown. From the figure, the performance of the buffer is satisfactory. The output of the op-amp is stable and settles quickly to the input voltage.

Fig. 4.34. Complete schematic of compact op-amp

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Fig. 4.35. Bode plot of op-amp

Fig. 4.36. Gain of op-amp at different common mode input voltages

Fig. 4.37. Various step responses of the op-amp with 1pF load

4.9 Bandgap Reference

A bandgap reference provides the biases needed for the op-amp. The bandgap reference circuit is shown in Fig 4.38. The circuit consists of two parts: the current proportional to absolute temperature (*PTAT*) circuit and the V_{BE} circuit. The *PTAT* circuit generates a current that is proportional to the absolute temperature and the V_{BE} circuit generates a current derived from a base-emitter junction of a bipolar transistor. The currents are scaled so that the sum of the currents are temperature and supply independent. This current mode architecture is commonly used in low voltage reference design. The relationships between the currents are shown in the following equations.

$$I_{out} = I_{PTAT} + I_{VBE} \tag{4.5}$$

$$\frac{\partial I_{out}}{\partial T} = \frac{\partial I_{PTAT}}{\partial T} + \frac{\partial I_{VBE}}{\partial T} = 0 \tag{4.6}$$

Fig. 4.38. Schematic of bandgap reference

In both circuits the current conveyor [54] is used. The PMOS current mirror (M3 & M4) in the conveyor replicates the current flowing through the left branch (I_x) in the right branch (I_y). The NMOS transistor pair (M5 & M6) transfers the input voltage on the right (V_y) to the output on the left (V_x). With this circuit, V_{BE} is applied across the resistor ($R3$) in the V_{BE} circuit to generate a current with negative temperature coefficient, shown in Eq. 4.7 and Eq. 4.8. In the *IPTAT* circuit, a cross-coupled NMOS pair (M7 & M8) is added to improve the supply rejection ratio. The current conveyor creates the difference between the two V_{BE} ($\Delta V_{BE} = V_{BE1} - V_{BE2}$) and the voltage difference is applied across the resistor ($R2$) to generate a current with positive temperature coefficient, shown in Eq. 4.9 and Eq. 4.10. The two currents are summed to obtain a temperature and supply independent current.

$$I_{VBE} = \frac{V_{BE3}}{R3} \quad (4.7)$$

$$\frac{\partial I_{VBE}}{\partial T} \approx \frac{1}{R3} \cdot (-2mV) \text{ \{-ve temp coefficient\}} \quad (4.8)$$

$$I_{PTAT} = \frac{V_T \ln 4}{R2} \quad (4.9)$$

$$\frac{\partial I_{PTAT}}{\partial T} \approx \frac{\ln 4}{R2} \cdot \left(\frac{k}{q} \right) \text{ \{+ve temp coefficient\}} \quad (4.10)$$

A start-up circuit formed by M1, M2 and R1 ensures that the bandgap reference operates properly. Initially, when no current flows through M3, M2 does not source any current as well, as the gates of M2 and M3 are connected. No voltage is developed across R1 and therefore M1 is turned on, pulling current from the gate of M3 and starting up the *IPTAT* circuit. Once the circuit is started, M2 mirrors the current and a high voltage is developed across R1 to shut off M1.

Fig. 4.39. Layout and cross-sectional view of PNP bipolar transistor in N-well process

Fig. 4.39 shows the layout and cross-sectional view of the vertical PNP transistor that is available from the N-well process. The emitter is formed using the P+ diffusion and the base of the transistor is formed using the N-well. The P-substrate forms the collector for the transistor and is permanently committed to ground.

Fig. 4.40 shows the simulated output current of the bandgap reference at three temperatures of 10°C, 30°C and 50°C. The output current is very accurate and stable from 3.3V to 5V. Fig. 4.41 shows a closed up view on the simulated output.

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Fig. 4.40. Bandgap reference at temperature of 10°C, 30°C and 50°C

Fig. 4.41. Closed up view of bandgap reference

4.10 Design and Fabrication by XFAB 0.6 μ m Process

The design methods, circuits and architectures described in preceding sections were used to realize a LCoS microdisplay based on XFAB 0.6 μ m process. The final microdisplay has a resolution of 320 x 240 (QVGA) with 4-bit gray scales. The microdisplay operates with a single 3.3V supply. The pixel size is 35 μ m by 35 μ m. Based on the design rules supplied by XFAB, a 91% aperture ratio was achieved for this design.

A scaled down version with 4x4 matrix of the microdisplay was created to simulate the operation of the microdisplay. A complete microdisplay is too big and not suitable for simulation. The reference voltages incorporating Gamma correction used in the simulation is shown in Fig. 4.42. The block diagram for the microdisplay is shown in Fig. 4.43.

Fig. 4.42. Gamma correction curve and reference voltages used for the simulation

The simulation results for various nodes in the microdisplay are shown in Figs. 4.44 – 4.49. These monitored nodes are labeled from A to F in Fig. 4.43. Fig. 4.44 shows the input signals at node A. Fig. 4.45 shows the outputs of the row

scanners at node B. Fig. 4.46 shows the outputs of the DACs at node C. Fig. 4.47 shows the outputs of the column drivers at node D. Fig. 4.48 and Fig. 4.49 show the voltages at the intermediate storage capacitors (node E) and final storage capacitors (node F) respectively. The numbers on Fig. 4.46 to Fig. 4.49 correspond to the pixel number shown in Fig. 4. 43.

From the simulation results, the good performance of the microdisplay can be verified. In Fig. 4.46, the outputs of the converted analog voltages for the sixteen different levels are shown. These voltages are pre-compensated by the column op-amps and the outputs are shown in Fig. 4.47. These voltages were shifted by the offsets of the in-pixel buffers, and programmed using line-at-a-time refresh method into the intermediate storage capacitors. The voltages on these intermediate storage capacitors are shown in Fig. 4.48. Finally, the voltages on the final storage capacitors are shown in Fig. 4.49. The comparison between Fig. 4.46 and Fig. 4.49 shows that the desired voltages corresponding to the digital inputs have been transferred correctly onto the final storage capacitors. The result in Fig. 4.49 also shows that in the frame-at-a-time refresh, the image signal is quite stable throughout the frame period for the simulated 4x4 matrix.

Fig. 4.43. Block diagram of simplified 4 x 4 LCOS microdisplay

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Fig. 4.44. Timing relationship of input signals (point A)

Fig. 4.45. Simulated output of row scanner (point B)

Fig. 4.46. Simulated output of DAC (point C)

Fig. 4.47. Simulated output of pre-compensated voltages (point D)

Fig. 4.48. Simulated voltage at intermediate storage capacitors (point E)

Fig. 4.49. Simulated voltage at final storage capacitors (point F)

4.11 Test Result of LCoS Microdisplay

The fabricated backplane LCoS microdisplay was further processed to integrate the LC cells. Shown in Fig. 4.50 is the completed LCoS microdisplay was packaged using Chip-On-Board (COB) technology.

Fig. 4.50. Photograph of packaged LCoS microdisplay

Fig. 4.51. Die photograph of LCoS microdisplay (top left corner of die)

Fig. 4.51 shows the top left corner of the microdisplay. In this figure, the main circuit components (bandgap reference, row scanner, DFF, DAC, op-amps and pixels) can be clearly seen. Close-up view of the various circuits can be seen in the following figures (Fig. 4.52 to Fig. 4.54).

Fig. 4.52. Close-up view of bandgap reference

Fig. 4.53. Close-up view of rail-to-rail op-amp

Fig. 4.54. Close-up view DAC with gamma correction

For testing of the row scanner, a pulse was injected at the input (VSYNC). This pulse was propagated through the row scanner by clocking the HSYNC signal. Fig. 4.55 shows a measured waveform of the output with a VSYNC input. The input VSYNC pulse was propagated through the row scanner and the output of the last element was measured through an inverter. An inspection of the output had shown that the row scanner was operating properly. In Fig. 4.56, the input signal was changed to an arbitrary pattern. The output was an exact inverted replica with a frame period delay.

Fig. 4.55. Measured waveform of row scanner output (VSYNC input)

Fig. 4.56. Measured waveform of row scanner output (arbitrary pattern input)

As for the visual inspection, complete result was unavailable at the time of writing. However initial test showed promising results. Gray scale was observed when the input data varied from minimum (Fig. 4.57(a)) to maximum values (Fig. 4.57(c)), indicating that the DAC, op-amp and in-pixel buffer were working properly. However the pattern on the display cannot be controlled and differs from

chip to chip. A possible cause could be damage induced during the fabrication of the LC cells. Further tests will be carried out when fabricated samples are available.

Fig. 4.57. Gray scale display on LCoS microdisplay
(The figure is reproduced in color in the Appendix)

Electrical measurement was performed on the pixels of three other different panels. The results are shown in Fig. 4.58, Fig. 4.59, Fig. 4.60 and Fig. 4.61. For the first two samples, the input data was switched between all '1's and all '0's for alternate frames. Measurement from Sample 1 shows that the pixel voltage is very noisy at high voltage. For Sample 2, the pixel voltage is stuck at two distinct levels for input of all '1's and all '0's respectively. Fig. 4.60 and Fig. 4.61 shows measurements from the third sample. For the Sample 3, the input data was varied from minimum to maximum in four steps. As seen in Fig. 4.60, four distinct voltage levels were observed, indicating that the correct operation of the DAC. However, it was observed that the voltage was held steady for only the global refresh period, indicating possible damage to the final storage capacitor. The cause for this damage could be attributed to the breakdown of the gate of the

MOS capacitor due to electrostatic discharge. Fig. 4.61 shows a close-up view of the pixel voltage measurement before the electrostatic discharge happened.

Fig. 4.58. Measured waveform of pixel voltage (Sample 1)

Fig. 4.59. Measured waveform of pixel voltage (Sample 2)

Fig. 4.60. Measured waveform of pixel voltage at 4 distinct DAC output levels (Sample 3)

Fig. 4.61. Close-up view of pixel voltage (Sample 3)

In this chapter, the basics of LCoS design were presented with emphasis on low voltage and low power designs. A pre-compensation scheme in the column driver and a pseudo rail-to-rail buffer to achieve frame-at-a-time refresh were presented. Several in-pixel buffers were introduced and the performances were explained with simulation results. The operation and timing controls for frame

buffering were also discussed. Analog building blocks like the DAC, op-amp and bandgap reference were described and the performance of these blocks were verified by simulations. Finally a scaled down version microdisplay with a 4x4 matrix was simulated and the results showed satisfactory performance of the proposed scheme and circuits.

Chapter 5. OLED-on-Silicon

Conventionally OLED is fabricated on glass substrate, and prototypes have shown remarkable performances that surpass LCD [55]. Microdisplays of the OLED type using silicon as backplane offer the advantages of both CMOS and OLED technologies. Low voltage and power, high resolution and excellent contrast ratio are some of the many properties that OLED-on-silicon microdisplays can offer.

This chapter deals with the design of the driver circuitry essential for building a backplane for OLED-on-Silicon microdisplay. Simulation results of both individual sections and scaled down version of the microdisplay have been presented.

5.1 Current versus Voltage Characteristic of OLED

The structure of a conventional OLED is shown in Fig. 5.1. Electrons and holes are injected from the metal cathode and ITO anode respectively. Electroluminescence (EL) is generated by radiative recombination of these carriers near the interface between the two transport layers. The device current versus voltage characteristic had been well documented by previous works [56].

Fig. 5.1. Basic OLED structure

Under low voltage forward biased condition, the device current is proportional to the applied voltage ($I \propto V$), indicating ohmic behavior. At forward voltage higher than the turn-on potential, the current-voltage relationship is described by $I \propto V^{m+1}$, where m vary from 6 to 10, indicating trap-charge-limited conduction [57]. Fig. 5.2 shows an illustration of the forward biased current versus voltage characteristic of a typical OLED.

Fig. 5.2. Forward biased current vs voltage characteristic of OLED

The EL intensity of the OLED is in direct proportion to the applied current density, as shown in Fig. 5.3. The EL intensity is linear with current density over three orders of magnitude [58].

Fig. 5.3. Linear dependence of output optical power on current density of OLED

Gray scale in OLED displays can be achieved in three ways. The first is an analog method whereby the magnitude of the voltage or current of the OLED is controlled directly. As the OLED experienced high power-law ($I \propto V^{m+1}$) increase in the current after the turn-on voltage, accurate gray scale by voltage control is difficult to achieved. On the other hand, the EL intensity of the OLED varies linearly with the current density. Therefore the output intensity of the OLED can be accurately control by programming the current driving the device.

The second way of obtaining gray scale is by pulse width modulation (PWM) whereby the illumination duration of the OLED is controlled. This PWM method of gray scale is more consistent because the OLED operates in either entire “on” or “off” states, eliminating any effect of threshold voltage or other process variations. However this method requires a frame memory which would increase the cost of the system [59].

The third way of obtaining gray scale is spatial modulation. In this method, multiple sub-pixels are grouped together to form a pixel. By switching on the numbers of sub-pixels corresponding to the digital input, gray scale is obtained. This method has the disadvantage of higher pixel count as sub-pixels are grouped to form pixel elements.

The analog method of obtaining gray scale is used in this work. Since CMOS technology is used for the backplane, analog circuits with excellent performance can be expected. Accurate current control is attainable which allows very good uniformity for the OLED display.

5.2 OLED Pixel Cell Design

The OLED may be driven with a simple two-transistor circuit as shown in Fig. 5.4. The access transistor is turned on when a pixel is addressed and voltage is stored onto the storage capacitor. The transconductance transistor acts as a voltage-to-current converter and converts the stored voltage to a current as shown in Eq. 5.1. The stored voltage will have to be high enough to keep the transistor in saturation so that the output behaves close to an ideal current sink with high output impedance to provide steady current for driving the OLED.

The driving of OLED with this method suffers from luminescence variations due to errors in input voltage because of the square-law characteristic of transistors. Eq. 5.1 can also be rewritten as Eq. 5.2, in which variations due to process are reflected. In the equation, ΔK are the transistor gain factor variations due to non-uniform gate oxide thickness. Δw and Δl are geometrical variations caused by misalignment and ΔV_{THN} is the threshold voltage variations. As a result, displays with this pixel structure cannot offer good pixel-to-pixel uniformity.

Fig. 5.4. Simple two transistors pixel cell for OLED displays

$$I_D = \frac{1}{2} \cdot K_n \cdot \frac{W}{L} \cdot (V_{GS} - V_{THN})^2 \cdot (1 + \lambda \cdot V_{DS}) \quad (5.1)$$

$$I_D = \frac{1}{2} \cdot [K_n + \Delta K] \cdot \frac{W + \Delta w}{L + \Delta l} \cdot (V_{GS} - [V_{THN} + \Delta V_{THN}])^2 \quad (5.2)$$

In order to have good uniformity on the display, a four-transistor pixel cell design is usually adopted in OLED pixel design. Fig. 5.5 shows a schematic of such a circuit. The circuit is similar to the current copier cell that is commonly used in analog current mode circuit [60]. In this design, the same transistor is used for both programming and driving operation, thereby eliminating any mismatch.

Fig. 5.5. Four transistors pixel cell for OLED displays

The circuit consists of a transistor which acts as a transconductance amplifier to convert the input voltage to output current, a storage capacitor implemented with the gate of a NMOS (for higher capacitance per unit area) and three transistors for switching.

The circuit operates in two phases. Fig. 5.6 shows the waveform for the current programming operation of the pixel. The operation of the circuit is as follows:

- a. At t_1 , the row select signal is activated to start the programming phase.
- b. Input transistors are turned on while the output transistor is turned off. The transconductance transistor's gate is connected to the drain.

- c. The voltage of the storage capacitor, V_c , is adjusted to sustain the reference current flow in the channel of the transconductance transistor.
- d. At t_2 , row select signal goes low and input transistors are switched off. The output transistor switches on and now output current is sink from the OLED. This is the driving phase of operation.
- e. Current sink will remain constant as long as the gate voltage remains the same.
- f. Pixel cell has to be re-programmed by t_3 before the output current drops to an unacceptable level, caused by the voltage droop at the storage capacitor.

Fig. 5.6. Driving waveform for current programming

In the programming operation of the pixel cell, the signal that drives the output switch lags the row select signal by a gate delay. This delay is important for proper operation of the pixel cell. This is because the gate-drain connection must be broken before the output is connected to the transconductance transistor to avoid disturbing the voltage programmed onto the storage capacitor.

The gate-source voltage of the transistor controls the output current, as shown in Eq. 5.3. The aspect ratio, threshold voltage and drain current appear as independent variables in the equation. The programming of the gate-source voltage is accomplished by shorting the gate-drain terminals to force the desired current through the transistor. The gate node will be charged to the voltage required to sustain the current through the cell. In this way the programming of the cell is self-calibrating; any device mismatch will not affect the performance as the gate voltage is calibrated to supply the output current.

$$V_{GS} = V_{THN} + \sqrt{\frac{2 \cdot I_D}{K_N \cdot \left(\frac{W}{L}\right)}} \quad (5.3)$$

Although the current copier cell is self-calibrating, it still suffers from the following problems, as shown in Fig. 5.6.

- ◆ Charge redistribution due to switching of transistors
- ◆ Gate voltage droop due to charge leakage
- ◆ Channel length modulation due to different drain-source voltage, V_{DS} , during programming and driving

Many literatures have reported ways to overcome the above-mentioned problems [61, 62]. However in the microdisplay, the pixel size limits the area available for the layout of the current copier circuit, making circuits with large devices count not suitable. As a result, the basic circuit with a little modification is used for the OLED pixel. In order to minimize errors, the transistors in the cell are carefully designed.

Using minimal size transistors can reduce the first problem of charge redistribution due to the switching transistors. The charge redistribution of the switches is caused by partial injection of the accumulated charge in the channel

into the storage capacitor during the switching of the transistor. The amount of charge accumulated in the channel depends on the voltage applied on the gate and the channel area. The gate voltage is fixed by the switching logic and thus cannot be easily changed. Minimum size transistors are used for the switch to minimize the channel area.

The charges from the switching transistor channel, ΔQ , injects into the storage capacitor and result in a change in the gate voltage, ΔV_g , which manifest itself as a change in current, ΔI , at the output. The mathematical relation is shown in the formulae below.

Initially, the gate voltage with initial charge Q_{ini} and storage capacitance $C_{storage}$,

$$V_g = \frac{Q_{ini}}{C_{storage}} \quad (5.4)$$

Due to charge injection, ΔQ_{switch} ,

$$\Delta V_g = \frac{\Delta Q_{ini}}{C_{storage}} \quad (5.5)$$

The error in output current can be shown as follows:

$$I_{D1} = \frac{1}{2} \cdot K_N \cdot \frac{W}{L} \cdot (V_{GS} - V_{THN})^2 \quad \{\text{before charge injection}\} \quad (5.6)$$

$$I_{D2} = \frac{1}{2} \cdot K_N \cdot \frac{W}{L} \cdot ([V_{GS} + \Delta V_g] - V_{THN})^2 \quad \{\text{after}\} \quad (5.7)$$

$$\begin{aligned} \Delta I &= I_{D2} - I_{D1} \\ &= \frac{1}{2} \cdot K_N \cdot \frac{W}{L} \cdot (2 \cdot \Delta V_g \cdot V_{GS} - 2 \cdot \Delta V_g \cdot V_{THN} + \Delta V_g^2) \\ &= \frac{1}{2} \cdot K_N \cdot \frac{W}{L} \cdot (V_{GS} - V_{THN}) \cdot 2 \cdot \Delta V_g \end{aligned} \quad (5.8)$$

The ΔVg^2 term in the equation can be ignored when V_{GS} and $V_{THN} \gg \Delta Vg$. The equation reduces to the following:

$$\Delta I = \sqrt{2 \cdot K_N \cdot \frac{W}{L} \cdot I_D} \cdot \Delta Vg \quad (5.9)$$

in which the first term on the right hand side happens to be the same as g_m , the small signal transconductance of the transistor.

From the above equations, the error in the output current can be reduced in two ways: the first is to select a small aspect ratio to reduce the transconductance g_m , and the second is to use a larger storage capacitor to reduce ΔVg . Eq. 5.9 also shows that the transconductance g_m is proportional to $\sqrt{I_D}$. Therefore the error is amplified by a larger gain at high drain current.

The maximum capacitance that can be used is restricted by available space in the pixel, and therefore error reduction is limited. Minimizing the aspect ratio method is used instead to reduce the error to an acceptable level.

The second problem of gate voltage droop is caused by charge leakage, which is due to current leakage through the capacitor, the gate of the transconductance transistor and the source of the switching transistor. The first two components are less significant than the last. Using the smallest size for the switches minimizes the leakage through the source of the switching transistor. Another way of reducing the leakage is to reduce the voltage across the drain and the bulk of the switching transistor. A cross section of the switching transistor is shown in Fig. 5.7(a). The leakage current is proportional to the reverse bias voltage across the PN junction formed by the drain and the bulk of the transistor. If the bulk can be connected to the source, then the leakage due to the reverse biased junction can be minimized. Fig. 5.7(b) shows a NMOS in a P-well process with

the source and bulk connected. For NMOS on a P-substrate, this arrangement is not possible, as the bulk would have been committed to the ground.

Fig. 5.7. Cross-section of NMOS transistor, a) N-well process, b) P-well process

The third problem of channel length modulation effect is reduced by the introduction of the LDD_MOS transistor. This transistor serves two functions. Firstly it is used to connect the current copier cell to the cathode of the OLED and secondly, it is used to buffer the high voltage stress from the high external OLED voltage supply. With this transistor in place, the drain voltage of the transconductance transistor can be held at V_{GS} by biasing the gate of the LDD_MOS at $(V_{GS(transconductance transistor)} + V_{GS(LDD_MOS)})$ in the driving phase. This will force the drain in both phases to roughly the same voltage. In the programming phase, the drain is connected to the gate whose voltage is determined by the reference current. The difference in drain voltages in the two phases is restricted to a limited range and channel modulation effect is reduced. In addition, long channel length reduces the effect of channel length modulation as well.

The final circuit design for the pixel cell is shown in Fig. 5.8. In this figure, the transistor that switches the current sink to the output is replaced with a LDD_MOS. This is due to the high voltage drive needed for the OLED, typically 15 V, which will result in high stress at the drain. Hot carriers injection may degrade or destroy the transistor if the stress is not reduced. Due to the lightly

doped region, the resistance presented by the lightly doped region is high, creating a voltage drop when current flows. The drop in voltage reduces the available driving voltage for the OLED. Therefore it is desirable to use a wide channel for the LDD_MOS. The maximum size of the LDD_MOS is limited by the available space in each pixel.

Fig. 5.8. Schematic of pixel cell

It should be noted that only NMOS could be used for switching of the output because of the higher voltage of the OLED supply. If a PMOS is used instead, the logic voltage on the gate will be lower than the source voltage and thus is not sufficiently high to switch off the transistor completely.

The minimum output voltage at the MOS switch is shown in Eq. 5.10. In the equation, V_{Logic} is the switching voltage of the logic, V_{GS} and $V_{DS(sat)}$ are the gate-source voltage and drain-source voltage of the LDD_MOS respectively and $I_{out} \cdot R_{LDD}$ is the voltage drop due to the lightly-doped region of the drain.

$$V_{out} = V_{Logic} - V_{GS} + V_{DS(sat)} + I_{out} \cdot R_{LDD} \quad (5.10)$$

It can be seen that a lower logic 'high' voltage improves the voltage drive available for the OLED. The drive can be improved by lowering the gate voltage of the switch as shown in Fig. 5.9. In this figure, the gate voltage of the switch is lowered by a threshold voltage by inserting a diode-connected transistor in the inverter that drive the gate. This arrangement is suitable for higher logic voltage of 5V, while it may not be necessary for lower logic voltage of 3.3V or 2.5V.

Fig. 5.9. Schematic showing lowering of gate drive voltage for output transistor

5.3 Charging of Storage Capacitor

The charging of the storage capacitor can be examined with a simple circuit as shown in Fig. 5.10. The charging operation can be classified into three regions, as shown in Fig. 5.11.

Fig. 5.10. Gate-drain connected transistor for analysis of charging operation

Fig. 5.11. Regions of operation for the charging process

In region I, the transistor is in the cut off region and a negligible drain current flows. The full reference current charges up the storage capacitor linearly, and the voltage of the capacitor is given by:

$$V_{C1} = \frac{1}{C} \cdot (I_{ref} \cdot t_1) \quad (5.11)$$

In the second region, the transistor enters the subthreshold conduction region and the drain current is given by Eq. 5.12 [63].

$$I_{D_SUB} = k_x \cdot \frac{W}{L} \cdot e^{V_{GS}/nV_T} \cdot (1 - e^{-V_{DS}/V_T}) \quad (5.12)$$

where k_x and n are dependent on process parameters, V_T is the thermal voltage and $\frac{W}{L}$ is the aspect ratio of the transistor.

Part of the reference current, I_{ref} , is diverted into the drain as the subthreshold current flow. As the gate voltage increases, the subthreshold current also rises, reducing the amount of current charging up the gate voltage. This slows down the charging process.

The dependency of the gate voltage on the subthreshold current is shown in the following equation.

$$\begin{aligned} V_{C2} = V_{GS} &= \frac{1}{C} \int_{t_1}^{t_2} (I_{ref} - I_{D_SUB}) dt \\ &= \frac{1}{C} \int_{t_1}^{t_2} \left(I_{ref} - \left[k_x \cdot \frac{W}{L} \cdot e^{V_{GS}/nV_T} \cdot (1 - e^{-V_{DS}/V_T}) \right] \right) dt \end{aligned} \quad (5.13)$$

In the third region, the transistor operates in the saturation region and Eq. 5.14 gives the drain current.

$$I_{D_SAT} = \frac{1}{2} \cdot K_N \cdot \frac{W}{L} \cdot (V_{GS} - V_{THN})^2 \quad (5.14)$$

Where K_N is the N-channel transconductance parameter.

Similarly, the relationship between the drain current and the gate voltage can be written below.

$$\begin{aligned}
 V_{C3} = V_{GS} &= \frac{1}{C} \int_{t_2}^{\infty} (I_{ref} - I_{D_SAT}) dt \\
 &= \frac{1}{C} \int_{t_2}^{\infty} \left(I_{ref} - \left[\frac{1}{2} \cdot K_N \cdot \frac{W}{L} \cdot (V_{GS} - V_{THN})^2 \right] \right) dt
 \end{aligned} \tag{5.15}$$

The simulation result of the charging of the storage capacitor voltage is shown in Fig. 5.12. The capacitor is initially discharged and the reference current is set to 10 μ A. The sudden rise in charging current in the initial portion is due to switching of a transistor that is used to connect the gate to the drain in the simulation.

Fig. 5.12. Simulated result of charging operation

The time required to charge the capacitor also depends on the size of the capacitor, C , and the aspect ratio, $\frac{W}{L}$, of the transistor. The effect of different capacitor size is shown in Fig. 5.13. For this simulation, the aspect ratio was fixed at $80\mu\text{m}/1.6\mu\text{m}$.

From the simulated result, it can be seen that a small capacitance allows the desired output current to be reach in a shorter time. This is to be expected as the voltage on a smaller capacitance rises faster with the same charging current.

Fig. 5.13. Simulated results of different storage capacitor value

Fig. 5.14. Simulated results of using different aspect ratio for transistor

The charging of the storage capacitor is also affected by the aspect ratio of the transistor. In the case of a high aspect ratio, there exists an overshoot in the output current, as shown in Fig. 5.14. This is due to the large gain of the transistor. It is also affected by the subthreshold region which is shortened by the high aspect ratio.

From the two simulation results, it can be observed that the charging of the gate voltage of the current copier cell can be considered a second order feedback system at low capacitance or high aspect ratio. The block diagram of the feedback system is shown in Fig. 5.15. The gate-drain junction of the transistor provides the negative feedback.

Fig. 5.15. Block diagram of feedback system

5.4 Current Mode Digital-to-Analog Converter

Fig. 5.16. Block diagram of a column driver

Fig. 5.16 shows the block diagram of the column driver consisting of the shift register, data buffer and the DAC, with the flow of data shown on the figure with arrows indicating the directions. The shift register performs the serial to parallel conversion for the incoming video data. The data of the particular column is transferred to the data buffer on the rising edge of the horizontal synchronizing signal after a complete row of data has been loaded into the shift register. The data

buffer will hold the data stable for one horizontal period while the DAC converts the data to analog current levels which will be programmed into the pixel.

In this section, the design of the DAC will be discussed in detail. In view of the relationship between the current and output luminescence of the OLED, it is more advantageous to perform the digital-to-analog conversion in current mode to control the output luminescence more accurately. The binary weighted current scaling DAC offers a simple design that is suitable for integration into the microdisplay. This type of DAC is more compact as compared to resistor based or capacitor based type for the required resolution, as the area needed to implement passive components for the other two types is very large. The structure of this DAC is well documented in common textbooks, and a basic 4-bit binary weighted current scaling DAC is shown in Fig. 5.17.

Fig. 5.17. Basic structure of 4-bit binary weighted current scaling DAC

The converter performs the conversion by switching current sources of one, two, four and eight times the reference current to the output according to the data input. Sixteen different levels of current sources will be available from the 4-bit DAC, from zero to fifteen times the reference current.

In the design implementation, multiple unit of the NMOS current mirrors form the current sources. There will be fifteen such unit current sources which are

grouped into parallels of one, two, four and eight units according to the weightage of the current source. The switches are implemented with NMOS transistors and these transistors introduce current spikes when they switch. This is due to the charge redistribution of the accumulated charge in the channels of the transistors. The current spikes create noise and degrade the performance of the DAC. To overcome the problem, a current steering structure is used to improve the DAC. Fig. 5.18 shows the structure of a current steering cell. The structure consists of a tail current sink, a switching transistor and a fixed bias transistor. The principle of the operation is based on the steering of the current into either path of the switch transistor and the fixed bias transistor. Since the fixed bias transistor is not switched, no charge redistribution will occur in that path and the noise is minimal. Fig. 5.19 and Fig. 5.20 show the output waveform at the switching and non-switching nodes respectively. Note the significant improvement of the noise current spikes in the latter figure.

Fig. 5.18. Structure of current steering cell

Fig. 5.19. Simulated output waveform at the switching node

Fig. 5.20. Simulated output waveform at the non-switching node

The fixed bias transistor also serves the purpose of acting as a buffer for the current source. The result is similar to a cascode current mirror with improved current matching for the current source. Since the transistor is biased at a voltage of V_{bias2} , the drain of the current source will be strapped at $(V_{bias2} - V_{THN})$, essentially eliminating channel modulation effect on the current source.

Fig. 5.21. Partial circuit implementation for 4-bit DAC

Fig. 5.21 shows the partial circuit implementation of the DAC. The current is summed at the non-switching node of the transistors and this current is mirrored to the output. Note that the input data has to be complimented to get the right corresponding converted values at the output.

A wide swing cascode design is used for the current mirror to enable the design to work for a low voltage supply. In this case, the wide swing mirror consumes only one gate-source voltage as compared to two gate-source voltages for a normal cascode current mirror. The schematic of the two mirrors is shown in Fig. 5.22.

Fig. 5.22. Schematic of a wide swing and normal cascode mirror

The minimum voltage supply required for the DAC is determined as follows:

$$VDD_{\min} = V_{Bias2} - V_{GS2} + V_{DS2} + V_{SG_mirror} \quad (5.16)$$

For a typical CMOS process, the voltage required can be below 3.3V with V_{bias2} fixed at $2 \times V_{GS1}$.

The DAC can be easily adopted for higher number of data bits by stacking the basic circuit. Fig. 5.23 shows a 8-bit DAC made up of two 4-bit basic DACs. The two DACs are biased by two different reference current. The higher order DAC is biased with a reference that is sixteen times larger than the first DAC. This arrangement extends the resolution of the DAC without consuming too much silicon area.

Fig. 5.23. Structure of 8-bit DAC formed by stacking two 4-bit DAC

5.5 Design and Fabrication by XFAB 0.6 μ m Process

The design methods, circuit and architectures described in previous sections were carried on a XFAB 0.6 μ m process. The final microdisplay design has a resolution of 320 x 240 (QVGA) with 4-bit gray scale. The microdisplay will operate with a 3.3V logic supply and an external OLED supply of up to 15V.

The display is designed to operate up to a current density of 1000mA/cm². Since the microdisplay has to display 16 shades of gray, the minimum current density is 62.5 mA/cm². With a pixel size of 35 μ m by 35 μ m for the 0.6 μ m process, the current in the cell range from 766nA to 11.49 μ A.

For the pixel design, an aspect ratio of 4 μ m/10 μ m is chosen for the transconductance NMOS, which limits the error to a very small value. The change of voltage at the storage capacitor for the smallest reference current of 766nA is

shown in Fig. 5.24. The charge injection caused a voltage change of 1.627mV, which was converted to an error of 5.9nA, which amounts to only 0.77% of error. Fig. 5.25 shows the results for the largest reference current of 11.49μA. The error in gate voltage was 2mV and the resultant error in output current was 52.1nA which accounted to 0.45% of the reference. The current sink for the OLED at 16 different current levels is shown in Fig. 5.26. The $V_{DS(SAT)}$ for the transconductance NMOS transistor shown in Fig. 5.8 is given by the following equation.

$$V_{DS(SAT)} = \sqrt{\frac{2 \cdot I_D}{K_n \left(\frac{W}{L}\right)}} \tag{5.17}$$

The $V_{DS(SAT)}$ for the transistor are 0.179 V and 0.714 V for the minimum and maximum current respectively.

The available voltage swing for the OLED was calculated with Eq. 5.10. The parameters for the LDD_MOS are shown in Table 1.

Parameter	Typical Value
Threshold voltage, V_{th0}	0.82 V
Max V_{DS}	15 V
On resistance	19 kΩ μm

Table 1. Parameters of LDD_MOS

For a 3.3V logic, the minimum output voltage is about 2.25V. Therefore, with an external high voltage supply of 15V for the OLED, the available voltage for the OLED operation is 12.75V.

Fig. 5.24. Simulation result showing charge injection at storage node (reference = 766nA)

Fig. 5.25. Simulation result showing charge injection at storage node (reference = 11.49µA)

Fig. 5.26. Simulated output current levels for OLED driving

In order to have good matching and replication of the current sources in the DAC, a moderately large NMOS ($W/L = 4\mu\text{m}/4\mu\text{m}$) was used for the current sources, labeled as transistor M_A in Fig. 5.21. The switching transistors, M_B , are wide channel devices with aspect ratio of $10\mu\text{m}/0.6\mu\text{m}$ to facilitate switching. The cascode NMOS, M_C , was set to a moderate size of $4\mu\text{m}/1\mu\text{m}$.

The size of the wide swing mirror PMOS (M_E) and the cascoding PMOS (M_D) were $4\mu\text{m}/4\mu\text{m}$ and $4\mu\text{m}/1\mu\text{m}$ respectively.

$$V_{GS(source)} = V_{THN} + \sqrt{\frac{2 \cdot I_D}{K_N \left(\frac{W}{L}\right)_{source}}} = 0.83V \quad (5.18)$$

$$\Delta V_{cascode} = V_{THN} + \sqrt{\frac{2 \cdot I_D}{K_N \left(\frac{W}{L}\right)_{cascode}}} = 56.5mV \quad (5.19)$$

$$V_{SG(mirror)} = V_{THP} + \sqrt{\frac{2 \cdot I_D}{K_P \left(\frac{W}{L}\right)_{mirror}}} = 1.58V \quad (5.20)$$

Eq.5.18 shows the gate-source voltage for the current source. The drain-source voltage of the current source was forced to be the same by the cascading NMOS, M_C . Eq. 5.19 shows the drain-source saturation voltage for the cascode NMOS, M_C and Eq. 5.20 shows the gate-source voltage of the PMOS, M_E mirror. From the equations, it can be verified that the transistors are operating in the saturation region, with the total voltage of 2.47V, which is well within the supply range.

A scaled down version of the microdisplay was created for the simulation to show the operation of the microdisplay. A complete microdisplay is too big and not suitable for presentation in this thesis. Fig. 5.27 shows a block diagram of a microdisplay with 4 x 4 pixel array. The simulation results at various points of the microdisplay is presented labeled 'A', 'B' and 'C' on Fig. 5.27. 'A' shows the input signals, as shown in Fig. 5.28. Fig. 5.29 shows the output current at the four DACs at point 'B'. The curves are labeled 0 through 15, which correspond to the pixel number as shown in Fig. 5.27. In this figure, the currents were measured at the drain nodes of the output transistor in the DACs, therefore the simulation results showed negative currents. The simulation results show that the performance of the DAC is excellent with regards to accuracy and settling time (340ns).

Fig. 5.30 shows the output current at the pixels at point 'C'. The numbers on the curves correspond to the pixels in the array as numbered in Fig. 5.27. The result shows that the output currents at the pixels were maintained at a steady level throughout the frame period. The figure shows sixteen distinct levels, corresponding to the digital data inputs.

Fig. 5.27. Block diagram of 4 x 4 OLED microdisplay

Fig. 5.28. Waveforms of input signals

Fig. 5.29. Simulated output waveform of DAC

Fig. 5.30. Simulated output waveform at the pixels

5.6 Prototyping on AMI 1.5μm Process

A 8x8 pixel microdisplay was designed and fabricated as a prototype on AMI 1.5μm process. 5 V digital drivers were used in the design. The design was laid out using Cadence tools and fabricated through MOSIS multi-project wafer service.

The OLED based microdisplay cannot be packaged in a conventional chip carrier like the PLCC because the microdisplay requires post-processing steps to fabricate the organic layers on the die. A die attached in a recessed cavity (Fig. 5.31) makes the post-fabrication difficult. Therefore the microdisplay was packaged using Chip-on-Board (COB) technology, as shown in Fig. 5.32.

Fig. 5.31. Bonding with conventional package

Fig. 5.32. Bonding using Chip-on-Board (COB) technology

To prepare the PCB pads for wire bonding, the copper pads were first plated with 150-200 mils of nickel. Subsequently a 5-15 mils of malleable gold was plated over the nickel. The bonding pads had to be placed, as much as possible, in line with the die pads [64]. The PCB design is shown in Fig 5.33. The die was attached to a Printed Circuit Board (PCB) using thermal conductive paste. A plated through-hole beneath the die conducts heat from the die to the bottom layer where a large copper plate was placed for efficient heat dissipation. Aluminum wire was used for wire bonding between the die pads and the gold/nickel plated PCB pads. Epoxy resin was then used to encapsulate the bonding wire to prevent damages to the wire in subsequent processing. Subsequent organic material will be evaporated onto the die surface to form the OLEDs. Fig. 5.34 shows a packaged microdisplay.

Fig. 5.33. PCB design for COB packaging

In Fig. 5.35, the die photograph of the prototype was shown. The layouts of the various components were clearly marked with an enlarged view of the pixel layout.

Fig. 5.34. Final packaged microdisplay

Fig. 5.35. Die photograph of AMI 1.5μm prototype

5.7 Silicon Backplane Test Result and OLED Fabrication

The fabricated prototype from AMI 1.5 μ m process was tested for the active matrix addressing circuit. The tests were carried out by sending a pulse input and propagating it through the row scanner (or shift register in the columns) and reading the output of the last element. The output at the last element was a similar signal to the input pulse which was delay by the number of element in the row scanner (or shift register). These results verified that the digital circuits were in good working condition.

As for the visual tests, due to the difficulty in fabricating inverted OLED structure, tests and measurements were not possible at the time of writing. There had been a trial to fabricate the OLED layers, however the trial did not yield a working device, possibly due to damages to organic layers by ITO sputtering.

The prototypes from the XFAB 0.6 μ m process has not been processed to fabricate the organic layers due to the same fabrication difficulty. As the active addressing circuit bears the same design as the LCoS microdisplay, the digital circuits would be functional as tested in the LCoS microdisplay. The die photographs of the prototype are shown in the following figures.

Fig. 5.36. Die photograph of the XFAB OLED prototype (top left corner of die)

Fig. 5.37. Die photograph of the XFAB OLED prototype (DAC)

Currently, OLED fabrication technology has been advancing rapidly due to the market demand. In the near future, fabricating inverted OLED structure will be possible. Tests on the designed OLED microdisplay will be carried out as soon as fabrication is possible within the research group or external source is available.

Fig. 5.38. Die photograph of the XFAB OLED prototype (DFF)

In this chapter, various building blocks essential to the OLED-on-silicon microdisplay were presented. The pixel cell design and working principles have been discussed in details. The charging dynamics of the pixel cell was also presented with detailed simulation results. The current mode DAC, an important block in the microdisplay that determine the output linearity of the display, was presented both in design and simulations. The entire microdisplay was simulated using a scaled down version to show the workability and the performance. Finally the packaging design of a prototype was described.

Chapter 6. Conclusions and Recommendations for Future Works

In this work, research was focused on developing the generic design methodology for design of the silicon backplane for microdisplays. The main emphasis was on low voltage and low power design. Two types of displays, LCoS and OLED-on-Silicon were designed and fabricated in a commercial foundry. This chapter concludes the works in this thesis on LCoS and OLED-on-Silicon microdisplay. Recommendations for future works are presented at the end of this chapter.

6.1 LCoS Microdisplay

In the LCoS microdisplay design, VCOM modulation, a method that switches the VCOM between VDD and GND to provide frame inversion, is adopted to reduce the operating voltage of the display. With this method, the required operating voltage is half that of conventional frame inversion method, therefore providing tremendous power savings.

For the refreshing of display, the frame-at-a-time scheme is achieved by inserting frame buffers into the pixel array. In the context of field sequential color display, the ability to refresh the entire image instantly offers superior performances over typical line refreshing. The improvement comes from the significant increase in image brightness and contrast. This is because the frame-at-a-time refresh method only requires a short period for the transfer of data from the intermediate storage node to the final storage node. As a result, the image is stable

over almost the whole frame period. This contributes to a high illumination duty ratio that improves the efficiency of the display system greatly. Image flickers and color breaking problems were also greatly relieved with frame-at-a-time refreshing.

A new pre-compensation scheme was developed for incorporation of frame buffer into the display. The novelty of this scheme is that more compact buffer design can be used for the in-pixel buffer, regardless of non-linearity and offsets that the buffer might introduce. As a result, even a simple push-pull buffer configured with two transistors can be adopted in the in-pixel buffer design.

In order to make full utilization of the voltage supply for driving of LC, a new buffer design was developed. This design provided a pseudo rail-to-rail output by selectively biasing the buffer with the appropriate voltage for a specific frame. The threshold property of LC was exploited to realize the rail-to-rail operation. By fixing the operating voltage of the LC to fall within the range of the buffer, a single, low voltage design was obtained.

To provide the pre-compensation function in the column driver, a rail-to-rail op-amp was adopted in the design. The op-amp is biased by an on-chip bandgap reference. The op-amp also provide high driving capability for charging the pixel's storage capacitor faster.

Gamma correction is indispensable in LCD design to provide accurate gray scale suitable for full color application. In this work, the gamma correction function was integrated into the DAC. Fine adjustment for the Gamma correction was achieved through five external voltage references. With these five references, a piece-wise linear fitting of the ideal correction curve was achieved with good accuracy. The voltages were buffered by difference amplifiers which provided

unity gain in the positive frame. In the negative frame, the difference amplifiers provided negative voltages (with respect to V_{DD}) by subtracting the reference voltages from the supply, V_{DD} . This arrangement allows a single set of reference to be used for both the positive frame and negative frame, thereby reducing the number of external reference inputs. A 2-bit selector was used to select the appropriate range of reference voltages for the next digital-to-analog conversion stage. The C-2C DAC architecture which features low power and consumes little silicon area was chosen for this design.

6.2 OLED-on-Silicon Microdisplay

In the OLED-on-Silicon microdisplay, the drivers for the pixels were designed based on a common anode connected pixel array. The common anode connection arose from the inverted OLED structure. This type of structure is fabricated starting from the cathode, and has a common anode as the capping layer. With a common anode pixel array, the voltage supply to the OLED pixel array can be different from the driving electronics. Therefore a high voltage is used for the OLED while a low voltage is used for the electronics.

Programming of current into the pixel cell was achieved by making use of the self calibrating property of a gate-drain connected transistor to cancel parameters variations. As a result the overall uniformity of the display was improved significantly. The programming of the pixel is distinctly separated into three regions: cutoff region, subthreshold region and saturation region. The optimization of storage capacitor size and the transconductance of the transistor is important in programming of the pixel cell.

In order to operate with a high voltage for driving of the OLED, a transistor with lightly doped drain was used as an output switch for each pixel. The switch buffers the circuit from high voltage stresses, thus allows the utilization of low voltage devices for the rest of the circuit.

A current mode DAC was used to convert digital input data into analog currents. The binary weighted current DAC was used in this design. A current steering cell was used to perform the switching so that current spikes in the output were minimized. As a result, a relatively noise-free DAC was obtained. A simple method of extending the resolution of the DAC was also proposed. This proposal makes use of stacked DACs with different references to keep the size of the converter small. The reference for the DAC is supplied externally, thus allows fine adjustment of the step size of the DAC.

6.3 Recommendations for Future Works

CMOS technology is gearing towards sub-100nm range for higher performance and packing density. However, this trend is not favorable for analog based circuits as the decreasing transistor size makes it difficult to attain reliable performance. Therefore, possibilities of using a full digital design for backplane of microdisplay may be explored to take advantage of the technology advancement.

Adopting a full digital design for backplane has an important advantage of having memory capability. With present analog design, the storage capacitor cell in the pixel exhibits limited memory retention due to charge leakage. With digital design, the memory element can hold the data for as long as power to the display is available. This feature can help to realize an addressable display. The motivation for developing an addressable display is that it can offer ultra low power

consumption. In such a display, only the pixels that have a change of content will be updated, while the rest are not activated, thus offering tremendous power savings. This feature is especially attractive in applications where the displayed image experiences little change, as in the case of digital watch or a computer monitor used for office applications like word processing.

For further improvement in LCoS design, the goal is in lowering the power consumption. One possible way is through the use of charge recycling techniques. In such techniques, power consumption is minimized by storing charge on a tank capacitor and reusing this charge to program the pixel. New methodology should be developed to perform the charge recycling efficiently on the microdisplay, preferably without resorting to external tank capacitors.

The op-amp is an important circuit used in the column driver for LCoS microdisplay. In order to optimize the efficiency of power consumption, lower power op-amp should be developed. The foci of the new development should be on low power, wide swing and compactness.

For further improvement in OLED-on-Silicon microdisplay, better pixel driving circuit can be explored. Charge redistribution problem can possibly be further reduced by better circuit topology or switching techniques.

Driving OLED with a fully digital backplane can offer several advantages over the analog way. First, memory can be incorporated in the display with excellent memory retention ratio. The fact that OLED does not need AC driving increases the attractiveness of a memory-backplane.

From a system point of view, efficient setup for viewing the microdisplays should be developed. For the OLED-on-Silicon, the setup may be a simple magnifying optics for direct-view application. As for the LCoS microdisplay, the

Chapter 6. Conclusions and Recommendations for Future Works

design for projection displays would require an elaborate study to ensure efficient use of illumination. For color sequential display application, the challenge is to reduce color breaking that is an inherent problem for this type of display.

For conclusion, it is much desirable to develop microdisplay with low power consumption and high light throughput, in order to build high quality display system with a low price tag.

References

- [1] H. Kitahara, E. Colgan and K. Schleupen, "Technology trend of large size and high resolution direct-view TFT LCD", *SID Digest*, pp. 1108-1111, 2000.
- [2] I. Underwood, "VLSI design and fabrication for Liquid-Crystal-on-Silicon", *IEE Seminar on Microdisplay and Smart Pixel Technologies*, pp.7/1-7/6, 2000.
- [3] http://www.displaytech.com/downloads/pr_Minolta.pdf
- [4] <http://www.emagin.com>
- [5] W. E. Howard and O. F. Prache, "Microdisplays based upon organic light-emitting diodes", *IBM Journal of Research & Development*, Vol. 45, No.1, 2001.
- [6] H. Lin, E. Naviasky, J. Ebner, W. Evans, P. Farrell, M. Hufford, G. Levy, D. Wheeler, B. Allison and O. Prache, "An 852x600 pixel OLED-on-Silicon color microdisplay chip using CMOS sub-threshold-voltage-scaling current driver", *IEEE Solid-State Circuits Conference 2002*, Vol. 1, pp. 426-437, 2002.
- [7] F. H. Yu, J. Chen, S. T. Tang and H. S. Kwok, "New Reflective Liquid Crystal Display Modes", *Proceedings of the Fourth Asian Symposium on Information Display*, pp. 207-210, 1997
- [8] H. Seiberle, O. Muller, G. Marck and M. Schadt, "Photoalignment of LCoS LCDs", *Journal of the SID*, Vol. 10, No. 1, pp. 31-35, 2002.
- [9] R. V. Kieronski, *U.S. Patent H1320*, 1994
- [10] L. Banks, "High performance ferroelectric LC microdisplay", *Proceedings of the 5th Asian Symposium on Information Display*, pp. 333-337, 1999
- [11] M. A. Handschy, D. Banas, H. Chase, J. Cunningham, R. Malzbender, M. R. Meadows and D. Ward, "Miniature FLC/CMOS color sequential display systems", *Journal of the SID*, Vol. 5, No. 1, pp. 27-30, 1997.
- [12] A. Graham, J. R. Hughes, J. C. Jones, M. F. Lewis, D. G. McDonnell, A. J. Slaney and R. L. Vizard, "Colour and greyscale in ferroelectric liquid crystal displays", *IEE Colloquium on Novel Display Technologies*, pp. 5/1-5/6, 1995.

References

-
- [13] I. Underwood, D. G. Vass, I. D. Rankin, D. C. Burns, A. O'Hara and J. Gourlay, "A novel technology for highly compact displays", *IEE Colloquium on Novel Display Technologies*, pp. 6/1-6/4, 1995.
 - [14] P. O'Donnell and A. Doi, "Microdisplays in Digital Cameras", *Information Display*, Vol. 17, No. 12, pp. 16-19, 2001.
 - [15] C. W. Tang and S. A. VanSlyke, "Organic electroluminescent diodes", *Applied Physics Letters*, Vol. 51, pp. 913-915, 1987.
 - [16] L. S. Hung, "Recent progress in organic light-emitting diodes", *6th International Conference on Solid-State and Integrated-Circuit Technology*, Vol. 2, pp. 1228-1233, 2001
 - [17] L. S. Hung, C. W. Tang, M. G. Mason, P. Raychaudhuri, and J. Madathil, "Application of an ultrathin LiF/Al bilayer in organic surface-emitting diodes", *Applied Physics Letters*, Vol. 78, No. 4, pp. 544-546, 2001.
 - [18] G. E. Jabbour, B. Kippelen, N. R. Armstrong and N. Peyghambarian, "Aluminum based cathode structure for enhanced electron injection in electroluminescent organic devices", *Applied Physics Letters*, Vol. 73, No. 9, pp. 1185-1187, 1998.
 - [19] K. Lmimouni, C. Legrand, C. Dufour, and A. Chapoton, "Diamond-like carbon films as electron-injection layer in organic light emitting diodes", *Applied Physics Letters*, Vol. 78, No. 17, pp. 2437-2439, 2001.
 - [20] Y. Zhao, S. Y. Liu and J. Y. Hou, "Effect of LiF buffer layer on the performance of organic electroluminescent devices", *Thin Solid Films*, Vol. 397, pp. 208-210, 2001.
 - [21] L. Zhu, H. Tang, Y. Harima, Y. Kunugi, K. Yamashita, J. Ohsita and A. Kunai, "A relationship between driving voltage and the highest occupied molecular orbital level of hole-transporting metallophthalocyanine layer for organic electroluminescence devices", *Thin Solid Films*, Vol. 396, pp 213-218, 2001
 - [22] A. J. Makinen, I. G. Hill, R. Shashidhar, N. Nikolov and Z. H. Kafafi, "Hole injection barriers at polymer anodes/small molecule interfaces", *Applied Physics Letters*, Vol. 79, No. 5, pp. 557-559, 2001.
 - [23] L. S. Hung and M. G. Mason, "Voltages reduction in organic light-emitting diodes", *Applied Physics Letters*, Vol. 78, No. 23, pp. 3732-3734, 2001.

References

-
- [24] X. Zhou, J. He, L. S. Liao, M. Lu, Z. H. Xiong, X. M. Ding, and X. Y. Hou, "Enhanced hole injection in a bilayer vacuum-deposited organic light-emitting device using a p-typed doped anode", *Applied Physics Letters*, Vol. 74, No. 4, pp. 609-611, 2000.
 - [25] J. Huang, M. Pfeiffer, A. Werner, J. Blochwitz and K. Leo, "Low voltage organic electroluminescent devices using pin structure", *Applied Physics Letters*, Vol. 80, No. 1, pp. 139-141, 2002.
 - [26] P. E. Burrows, G. Gu, V. Bulovic, Z. Shen, S. R. Forrest and M. E. Thompson, "Achieving Full-color Organic Light-emitting Devices for Lightweight, Flat-Panel Displays", *IEEE Transactions on Electron Devices*, Vol. 44, No 8, pp. 1188-1203, 1997.
 - [27] C. C. Wu, J. C. Sturm and R. A. Register, "Integrated three-color organic light-emitting devices", *Applied Physics Letters*, Vol. 69, No. 21, pp. 3117-3119, 1996.
 - [28] C. W. Ko and Y. T. Tao, "Bright white organic light-emitting diode", *Applied Physics Letters*, Vol. 79, No. 25, pp. 4234-4236, 2001
 - [29] C. W. Tang, D. J. Williams and J. C. Chang, "Organic electroluminescent multicolor image display device", *U.S. Patent 5 294 870*, 1994
 - [30] N. Takada, T. Tsutsui and S. Saito, "Control of emission characteristic in organic thin-film electroluminescent diodes using an optical-microcavity structure", *Applied Physics Letters*, Vol. 63, No. 15, pp. 2032-2034, 1993.
 - [31] P. E. Burrows, S. R. Forrest, S. P. Sibley and M. E. Thompson, "Color tunable organic light-emitting devices", *Applied Physics Letters*, Vol 69, No. 20, pp. 2959-2961, 1996.
 - [32] L. M. H. Heinrich, J. Müller, U. Hilleringmann, K. F. Goser, A. Holmes, D. H. Hwang and R. Stern, "CMOS-compatible organic light-emitting diodes", *IEEE transactions on Electronic Devices*, Vol. 44, No 8, pp.1249-1252, 1997
 - [33] D. L. Mathine, H. S. Woo, W. He, T. W. Kim, B. Kippelen and N. Peyghambarian, "Heterogeneously integrated organic light-emitting diodes with complementary metal-oxide-silicon circuitry", *Applied Physics Letters*, Vol. 76, No. 26, pp. 3849-3851, 2001.
 - [34] J. Sanford and E. Schlig, "Direct view active matrix VGA OLED-on-crystalline-silicon display", *SID Digest*, pp. 376-379, 2001.

References

- [35] G. W. Jones, "Active matrix OLED microdisplays", *SID Digest*, pp. 134-137, 2001.
- [36] O. Prache, "Full color SVGA+ OLED on silicon microdisplay", *SID Digest*, pp. 514-517, 2001.
- [37] D. Markovic, B. Nikolic and R. W. Broderson, "Analysis and design of low-energy flip-flops", *International Symposium on Low Power Electronic and Design 2001*, pp. 52-55, 2001.
- [38] S. T. Wu and D. K. Yang, *Reflective Liquid Crystal Displays*, Chicester, New York, Wiley, 2001
- [39] O. K. Kwon, B. D. Choi and Y. C. Sung, "An ultra-low-power driving method for AM-LCD", *International Display Workshop 2001*, pp. 1595-1598, 2001
- [40] H. C. Huang, D. D. Huang and J. Chen, "Optical modeling of small pixels in reflective mixed-mode twisted nematic cells", *SID Digest*, pp. 742-745, 1999.
- [41] M. Lu and K. H. Yang, "Reflective nematic LC devices for LCOS application", *Conference Record of the 20th International Display Research Conference*, pp. 1-7, 2000
- [42] S. Lee, C. Mao and K. M. Johnson, "A novel frame-buffering circuit for liquid crystal on silicon microdisplay", *Lasers and Electro-Optics Society Annual Meeting 2000*, Vol. 1, pp 121-122, 2000.
- [43] P. W. Cheng, H. C. Huang and H. S. Kwok, "Fast Prototyping Of Video Interface Controller For AMLCD System", *Proceedings of the Fourth Asian Symposium on Information Display*, pp. 195-198, 1997.
- [44] S. E. Shields, *U.S. Patent 4,870,396*, 1989.
- [45] D. Mcknight, *WO Patent 98/27540*, 1997.
- [46] K. Meinstein, C. Ludden, M. Hagge and S. Carruth, "A high-speed 6-bit TFT-LCD driver for COG application", *SID Digest*, pp. 261-264, 1995
- [47] X. W. Sun, S. C. Tan, J. Y. Lin, S. Q. Zhang, M. S. Tse, H. C. Huang, P. W. Cheng, and H. S. Kwok, "Development of a XGA color sequential liquid-crystal-on-silicon reflective microdisplay", *Conference Record of the 20th International Display Research Conference*, pp. 427-430, 2000.

References

-
- [48] F. Yamada, H. Nakamura, Y. Sakaguchi and Y. Taira, "Sequential-color LCD based on OCB with an LED backlight", *Journal of the SID*, Vol. 10, No. 1, pp. 81-85, 2002.
 - [49] S. C. Tan, J. Y. Lin, X. W. Sun, H. C. Huang, P. W. Cheng and H. S. Kwok, "Design of an interface controller for color sequential liquid-crystal-on-silicon microdisplay", *Proceedings of the Sixth Asian Symposium on Information Display*, pp. 42-45, 2000.
 - [50] D. S. Dewald, "Sequential color recapture and dynamic filter: A method of scrolling color", *SID Digest*, pp. 1076-1079, 2001
 - [51] M. L. Jepsen, M. J. Ammer, M. Bolotski, J. J. Drolet, A. Gupta, Y. Lai, D. Huffman, H. Shi and C. Vieri, "0.9" SXGA liquid crystal on silicon panel with 450Hz field rate", *Microdisplay 2001*, pp. 106-109, 2001
 - [52] S. W. Lee, H. J. Chung and C. H. Han, "C-2C digital-to-analogue converter on insulator", *Electronics Letters*, Vol. 35, No. 15, pp. 1242-1243, 1999.
 - [53] J. H. Huijsing, R. Hogervorst and K. Langen, "Low-power low-voltage VLSI operational amplifier cells", *IEEE Transactions on Circuits and Systems I*, Vol. 42, No. 11, pp. 841-852, 1995.
 - [54] C. Toumazou, F. Lidgey and D. Haigh, *Analogue IC design: The current-mode approach*, London: Peter Peregrinus Ltd., 1990.
 - [55] G. Rajeswaran, M. Itoh, M. Boroson, S. Barry, T. K. Hatwar and K. B. Kahen, K. Yoneda, R. Yokoyama, T. Yamada, N. Komiya, H. Kanno and H. Takahashi, "Active matrix low temperature Poly-Si TFT/OLED full color displays : development status", *SID Digest*, pp. 974-977, 2000.
 - [56] P. E Burrows, Z. Shen, V. Bulovic, D. M. McCarty, S. R. Forrest, J. A. Cronin and M. E. Thompson, "Relation between electroluminescence and current transport in organic heterojunction light-emitting devices", *Journal of Applied Physics*, Vol. 79, pp. 7991-8006, 1996.
 - [57] G. Gu and Stephen R. Forrest, "Design of Flat-Panel Displays Based on Organic Light-Emitting Devices", *IEEE Journal of Selected Topics in Quantum Electronics*, Vol. 4, No 1, pp. 83-98, 1998.
 - [58] J. Kido and T. Matsumoto, "Bright organic electroluminescent devices having a metal-doped electron injecting layer", *Applied Physics Letters*, Vol. 73, No. 20, pp. 2866-2868, 1998.

References

- [59] A. Yumoto, A. Mitsuru, H. Hasegawa and M. Sekiya, "Pixel-driving methods for large-sized Poly-Si AM-OLED displays", *International Display Workshop '01*, pp. 1395-1398, 2001
- [60] S. J. Daubert and D. Vallancourt, "Operation and analysis of current copier circuits", *Circuits, Devices and Systems, IEE Proceedings G*, Vol. 137, Issue 2, pp. 109-115, 1990.
- [61] C. Wang, M. O. Ahmad, M. N. S. Swamy and A. Azelmad, "Low switching-noise current copier", *Canadian Conference on Electrical and Computer Engineering 2000*, Vol 2, pp. 802-805, 2000.
- [62] T. Loliger and W. Guggenbuhl, "Cascode circuits for switched current copier", *Proceedings of the 40th Midwest Symposium on Circuits and Systems 1997*, Vol. 1, pp. 256-259, 1997.
- [63] P. Gray and R. Meyer, Analysis and design of analog integrated circuits, 3rd edition, *John Wiley & Sons Inc.*, pp. 76-78.
- [64] <http://www.pacemicroinc.com/guide.html>

Author's Publications

1. S. C. Tan and X. W. Sun, "Compact in-pixel buffer for frame buffering in LCoS ", *Microdisplay 2002*, pp. 57-60, Sep 2002.
2. S. C. Tan and X. W. Sun, "Design and analysis of OLED pixel with noiseless switching", *Proceeding of the 7th Asian Symposium on Information Display*, pp. 299-303, Sep 2002.
3. S. C. Tan and X. W. Sun, "Low power CMOS level shifters by bootstrapping technique", *Electronics Letter*, Vol. 38, No. 14, pp. 876-878, Aug 2002.
4. S. C. Tan and X. W. Sun, "Generic design of silicon backplane for LCoS microdisplays", *SID Digest 2002*, pp. 200-203, May 2002.
5. S. C. Tan and X. W. Sun, "Designing of circuit building blocks for OLED-on-Silicon microdisplays", *SID Digest 2002*, pp. 980-983, May 2002.
6. S. C. Tan, J. Y. Lin, X. W. Sun, H. C. Huang, P. W. Cheng and H. S. Kwok, "Design of an interface controller for color sequential liquid-crystal-on-silicon microdisplay", *Proceeding of the 6th Asian Symposium on Information Display*, pp. 42-45, Oct 2000.
7. X.W. Sun, S.C. Tan, J.Y. Lin, S.Q. Zhang, M.S. Tse, H.C. Huang, P.W. Cheng, and H.S. Kwok, "Development of a XGA color sequential liquid-crystal-on-silicon reflective microdisplay", *Conference Record of the 20th International Display Research Conference*, pp. 427-430, Sept 2000

Appendix

Gray scale display on LCoS microdisplay