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DEVELOPMENT OF ADVANCED PWM INVERTER WITH SOFT SWITCHING TECHNIQUE FOR BRUSHLESS DC MOTOR VARIABLE SPEED DRIVES SYSTEMS

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Contents

Summary

Permanent magnet brushless DC motor (BDCM) has been widely used in industrial applications because of its low inertia, fast response, high power density, high reliability and less maintenance. It exhibits the operating characteristics of a conventional commutated DC permanent magnet motor but eliminates the mechanical commutator and brushes. Hence many problems associated with brushes are eliminated such as radio-frequency (RF) interfenrence and sparking which is the potential source of ignition in inflammable atmosphere. BDCM is usually supplied by a hard-switching PWM inverter. However switching power losses increase with the increasing of switching frequency. In order to reduce the switching power losses, many soft switching inverters have been designed. Unfortunately, there are many drawbacks, such as high device voltage stress, large DC link voltage ripple, discrete pulse modulation, complex control scheme and so on. On the other hand, the majority of soft-switching inverters proposed in the recent decades have been aimed at the induction motor drive applications. So research on novel topologies of soft-switching inverter and special control circuit for BDCM drive systems is very important.

Soft switching operation of power inverter has attracted much attention in recent decades. In electric motor drive applications, soft-switching inverters are usually classified in three categories, namely resonant pole inverters, resonant DC link inverters and resonant AC link inverters. Resonant AC link inverter is not suitable to BDCM drives. Resonant DC link inverter and resonant pole inverter are all applicable to BDCM. In medium power applications, the resonant DC link concept offered a practical and reliable way to reduce commutation losses and to eliminate individual snubbers. Resonant pole inverter has the disadvantage containing more number of additional components than that of resonant DC link inverter, however there is no conduction path auxiliary switches and its normal operation is totally the same as hard switching inverter. In this thesis, two novel topologies of resonant DC link inverter and resonant pole inverter for BDCM drive system are proposed. These inverters possess the advantage of low switching power loss, low inductor power loss, low DC link voltage ripple, small device voltage stress, simple control scheme, eliminating a stiff DC link capacitor bank that is center-tapped.

The main idea of fuzzy logic control is to use the control ability of human being which includes experience and intuition so the nature of the controller has adaptive characteristics that can achieve robust response to a system with uncertainty, parameter variation, and load disturbance. PI controller has the advantage of fast response especially in motor starting but it will introduce overshoot and oscillation. The fuzzy logic controller can solve these problems while it is slower response than that of PI controller. To utilize the advantages of both PI and fuzzy logic controllers to provide better response than any one controller only, one hybrid controller with fuzzy logic and PI will be introduced in this thesis.

A variable speed electric drive system is normally controlled by a speed/current double closed-loop control system. In conventional control system, during starting, the current reaches its maximum value quickly which contributes to the fast response of the system as the motor runs with maximum acceleration. When the motor reaches the desired speed, the current can not be reduced to its steady state value immediately; it needs time to settle. Normally overshoot and oscillation are inevitable, settling time are multiple that of the starting time. If current reaches its maximum value immediately during starting and when the motor reaches desired speed, the current skips to its steady state value at the same time and the motor runs at the desired speed, the starting time is shortest and the settling time is only the starting time. If the motor reaches desired speed while the current can only skip to around the steady state value, there is oscillation too, but the oscillation is smaller than that of conventional control system and the settling time can be reduced greatly, too. To achieve fast starting, the key is to determine (predict) the steady state reference current (SSRC) during starting. An artificial neural network (ANN) is a computational network, consisting of a number of interconnected processing units (neurons), which is able to learn and represent the unknown dependency relationship between a set of input variables and a set of output variables of a system. By selecting the training patterns (acceleration, speed, current, DC link voltage, reference speed) which cover all conditions (i.e. various DC link voltage, various load, various moment of inertia, various reference speed) to train the neural network, the neural network is then possible to predict the SSRC according to the acceleration, speed, current, DC link voltage, reference speed of the drive system, although the predicted value may be not very accurate. Conventional controller combined with this technique holds the advantages of fast response, little overshoot, little oscillation, robust and so on.

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List of Abbreviations

ABEL	Advanced Boolean Equation Language
ACRDCLI	Actively Clamped Resonant DC Link Inverter
ADC	Analog to Digital Converter
AND	And logical gate
ANN	Artificial Neural Network
ARCPI	Auxiliary Resonant Commutated Pole Inverter
BDCM	Brushless DC Motor
CK	Synchronous Pulse between BDCM Commutation Circuit and Control Circuit
CPLD	Complex Programmer Logical Device
CSI	Current Source Inverter
DSP	Digital Signal Processor
E^2PROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electro Magnetic Compatibility
EMF	Electromotive Force
EMI	Electro Magnetic Interference
GAL	Gate Array Logic
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
IPM	Intelligent Power Module
JEDEC	Joint Electron Device Engineering Council
LED	Light-emitting Diode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MRC	Multi-element Resonant Converter
NB	Negative big
NM	Negative medium
NOT	Not logical gate
NS	Negative small
OR	Or logical gate
PB	Positive big

PI	Proportional Integral
PM	Positive medium
PRC	Parallel-Resonant Converter
PS	Positive small
PWM	Pulse Width Modulation
PM	Permanent Magnet
QEP	Quadrature Encoder Pulse
QRDCLI	Quasi Resonant DC Link Inverter
QPRDCLI	Quasi Parallel Resonant DC Link Inverter
QRC	Quasi-Resonant Converter
RAM	Random-access Memory
RDCLI	Resonant DC Link Inverter
RF	Radio frequency
RPI	Resonant Pole Inverter
SCI	Serial Communications Interface
SMPS	Switching Mode Power Supply
SPRC	Series-Parallel Resonant Converter
SRC	Series-Resonant Converter
SRM	Switch Reluctance Motor
SSRC	Steady State Reference Current
SSRS	Steady State Reference Speed
SVCRDCLI	Source Voltage Clamped Resonant DC Link Inverter
TG	Tachometer generator
UPS	Uninterruptible power supply
VSI	Voltage Source Inverter
Z	Zero
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ZVT	Zero Voltage Transition

List of Principle Symbols

a	Transformer turn ratio 1: n
$a_1(n) \sim a_5(n)$	Input of the neural network
a_1A_1, a_2A_2	Coil in BDCM
act	conventional controller active signal
$A_\omega(s)$	The transfer function of speed loop
B	Viscous friction coefficient
$b_1(n)$, $b_2(n)$, $b_3(n)$	Input of the neural network
B_g	Air gap flux density
C_{bs}	Bootstrap capacitor
C_c	Clamping capacitance in ACRDCL inverter
C_r	Resonant capacitance
$C_{r1} \sim C_{r6}$	Snubber capacitor
C_{ra}, C_{rb}, C_{rc}	Snubber capacitor
$D_1 \sim D_6$	Build in freewheeling diode of main switches in an inverter
D_a, D_b	Auxiliary diode in QPRDCL inverter I
	Build in freewheeling diode of auxiliary switch S_a and S_b
D_{bs}	Bootstrap diode
D_{cl}	Clamping diode
D_{fp}, D_r	Auxiliary diode in special design RPI
D_L	Build in freewheeling diode of auxiliary switch S_L
E	Back EMF of BDCM
e	Speed error in controller
$\tilde{e}$	Speed error fuzzy variable
$\tilde{\dot{e}}$	Acceleration error fuzzy variable
e_1, e_2	Speed error membership function boundary
$\dot{e}_1$, $\dot{e}_2$	Acceleration error membership function boundary
e, e_a, e_b, e_c	Instantaneous phase back EMF of BDCM
e_{a1}, e_{a2}	Instantaneous phase back EMF of coil a_1A_1 and a_2A_2
e_h, e_l	Speed error threshold

e_i	Current error
e_{pu}	Normalized speed error
$\dot{e}_{pu}$	Normalized acceleration error
$H_i(s)$	The transfer function of current loop
$G_1 \sim G_6$	The output of Monostable flip-flop $M_1 \sim M_6$
$G_i(s)$	current controller
$G_{S1} \sim G_{S6}$	Gate signal for main switches $S_1 \sim S_6$
G_{Sa}, G_{Sb}, G_{Sc}	Gate signal for auxiliary switches S_a, S_b, S_c
I_0	Equivalent load current during resonant
I_{0max}	Maximum load current
i, i_a, i_b, i_c	Instantaneous phase current of BDCM
i^*	Reference current
I_{avg}	Average value of i_{sum}
I_{boost}	Preset current threshold in ARCP inverter
i_{cr}	Coarse reference current
i_{cs}^*	Coarse steady state reference current
$i_{cs}(n)$	Coarse steady state reference current calculated in one sample period
i_{DL}	Current of freewheeling diode D_L
I_{offset}	Current offset
i_{Lr}	Current of resonant inductor
i_{Lrs}	Secondary winding current
i_{Lra}, i_{Lrb}, i_{Lrc}	Current of resonant inductor L_{ra}, L_{rb} and L_{rc}
$i_{Lr\text{-}m}$	Peak value of resonant inductor current
I_{Lr0}, I_{Lr1}, I_{Lr2}	Preset inductor current level
I_M	Current of load
I_{PR}	Peak reverse recovery current of freewheeling diode
I_{PT}	Turning on peak current of power semiconductor switch
I_R	Rated phase current
$i_{S1} \sim i_{S6}$	Current of main switch $S_1 \sim S_6$
i_{SL}	Current of auxiliary switch S_L
i_{sum}	Absolute sum of phase currents
i_s^*	Steady state reference current
J	Moment of inertia

k	Armature constant $4N_{ph}/\pi$
k_c	Clamping factor in ACRDCL inverter
K_C	Equivalent gain of the inverter for BDCM
K_i	The gain of current sensor
K_{si}	The gain of current controller
$K_{s\omega}$	The gain of speed controller
K_ω	The gain of speed sensor
l	Rotor axial length
L, L_a, L_b, L_c	BDCM phase inductance
L_{eq}	Equivalent inductance (L-M)/2
L_{l1}	Primary winding leakage inductance
L_{l2}	Secondary winding leakage inductance
L_r	Resonant inductance
L_{ra}, L_{rb}, L_{rc}	Branch resonant inductance in resonant pole inverter
M	Mutual inductance of BDCM
$M_1 \sim M_6$	Monostable flip-flop
N_1	The turn number of full-pitch coils in BDCM
net_j^1	The input of the j^{th} node in the 1st hidden layer
net_k^2	The input of the k^{th} node in the 2nd hidden layer
net_1^3	The input of only neuron in the ouput layer
N_{ph}	Number of turns in series per phase
p	Derivational operator d/dt
P	Power
r_1	Rotor radius
R, R_a, R_b, R_c	BDCM phase resistance
R_{eq}	Equivalent resistance R/2
R_{LR}	Resistance of resonant inductor
$S_1 \sim S_6$	Main switches in an inverter
S_a, S_b, S_c	Auxiliary switch
S_c	Clamp switch in ACRDCL inverter
sel	Controller selection signal
S_h	Upper switch in a phaseleg
S_l	Lower switch in a phaseleg

S_L	Auxiliary switch in main conduction path
S_r	Auxiliary switch in resonant DC link inverter
T, T_e	Electromagnetic torque of BDCM
T_L	Load torque
t_{on}	Turn on time of a switch
t_{off}	Turn off time of a switch
T_r	Resonant period
T_w	DC link voltage rising transition time
u_1, u_2, u_3	Fuzzy controller output membership function boundary
u_{Cr}	Voltage of resonant capacitor
u_{S6}	Voltage drop of main switch S_6
v, v_a, v_b, v_c	Instantaneous phase voltage of BDCM
v_{bs}	Bootstrap capacitor voltage
$v_{Cr1} \sim v_{Cr6}$	Snubber capacitor voltage
v_{dc}	DC link voltage
v_o	Output voltage
V_{FT}	Conduction voltage drop of power semiconductor switch
V_{FD}	Conduction voltage drop of freewheeling diode
V_R	Rated voltage
V_S	Voltage of DC power supplies
w_{ji}^1	The weight between the j^{th} node in the 1st hidden layer and the i^{th} node in the input layer
w_{kj}^2	The weight between the k^{th} node in the 2nd hidden layer and the j^{th} node in the 1st hidden layer
w_{1k}^3	The weight between the k^{th} node in the 2nd hidden layer and the only one neuron in the output layer
$x_1(n) \sim x_5(n)$	Input of the neural network
y_j^1	The output of the j^{th} node in the 1st hidden layer
y_k^2	The output of the k^{th} node in the 2nd hidden layer
y_1^3	The output of only neuron in the ouput layer
α	Momentum gain
τ	Resonant circuit time constant
τ_e	Electrical time constant

τ_{em}	Electromechanical time constant
τ_m	Mechanical time constant
τ_{si}	The integral time constant
$\tau_{s\omega}$	The integral time constant of speed controller
ω_{cs}	Critical frequency
$\dot{\omega}_{\max}$	Possible maximum acceleration
ω_r	Natural angular resonance frequency
ω_r^* , ω^*	Reference speed
$\dot{\omega}_r$	Motor acceleration
ω_R	Rated rotor speed
θ_r	Rotor position
ϕ	Flux
φ_{cs}	Phase margin
ψ_1, ψ_2	Flux linkage
$\psi_{1\max}$	Maximum flux linkage
δ	PWM duty
$\Delta t_1 \sim \Delta t_8$	Duration of the operation mode 1 ~ 8 in soft-switching inverter
ΔT_a, ΔT_b, ΔT_d	Pulse width of auxiliary switch control signal
ΔT_1, ΔT_2, ΔT_3	Pulse width of auxiliary switch control signal
Δu	Crisp incremental command
$\Delta\tilde{u}$	Incremental command fuzzy variable
Δw	Pulse width of Hall signal
$\Delta\delta$	Incremental PI current control output
$\mu(.)$	Membership function
η	Learning rate of the neural network

Chapter 1 Introduction

1.1 Background

Permanent magnet (PM) brushless DC motor (BDCM) [78, 81] has been widely used in industrial applications because of its low inertia, fast response, high power density, high reliability and less maintenance. It exhibits the operating characteristics of a conventional DC motor but eliminates the mechanical commutator and brushes. The stator structure is similar to that of a polyphase AC induction motor but with PM mounted on the rotor for excitation. This has the advantage of eliminating the use of commutator and brushes which are present in conventinal DC motor. Hence many problems associated with brushes are eliminated such as radio-frequency (RF) interfenrence and sparking which is the potential source of ignition in inflammable atmosphere. The brushless configuration provides more cross sectional area for armature windings and produces greater torque and higher efficiency with the absence of brush friction. This also allows reduction of the motor length to provide greater torque/inertia ratio.

BDCM is usually supplied by a hard-switching Pulse-width-modulation (PWM) inverter. The performance of an inverter is dependent on the switching frequency as it determines the value and size of the reactive components in the inverter. Thus, high frequency operation of the inverter is desired. However, operation at high frequency results in higher switching power losses and higher switching stresses caused by the circuit parasitics (stray inductance, junction capacitance). In order to reduce the switching power losses, many soft switching inverters have been designed. Unfortunately, there are many drawbacks, such as high device voltage stress, large DC link voltage ripple, discrete pulse modulation, complex control scheme and so on. On the other hand, the majority of soft-switching inverters proposed in recent decades have been aimed at the induction motor drive applications. [98. 99, 101] So research on the novel topology of soft-switching inverter and special control circuit for BDCM drive systems is very important.

1.2 Conventional Voltage Source Inverter

DC-to-AC converters are known as inverters [63]. The function of the inverter is to change a DC input voltage to a symmetrical AC output voltage of desired magnitude and frequency. With the improvement of power semiconductor switches such as insulated gate bipolar transistors (IGBTs), metal oxide- semiconductor field effect transistors (MOSFETs), intelligent power module (IPM), conventional voltage source inverter (VSI) are widely used in industrial applications, e.g. variable speed AC motor drives, induction heating, standby power supplies, uninterruptible power supplies (UPS). In small to medium power ranges, the VSI is superior than current source inverter (CSI) in smaller size, lower power losses and higher efficiency. The construction of a conventional voltage source three-phase inverter is shown in Fig. 1-1. There is diode bridge rectifier connected to AC power supplies, electrolytic capacitor as filter component, six power semiconductor switches inverter (including build-in freewheeling diodes, snubber circuit), gate driver circuit and controller. The current, speed and/or position feedback signal of the motor is usually fed to the controller.

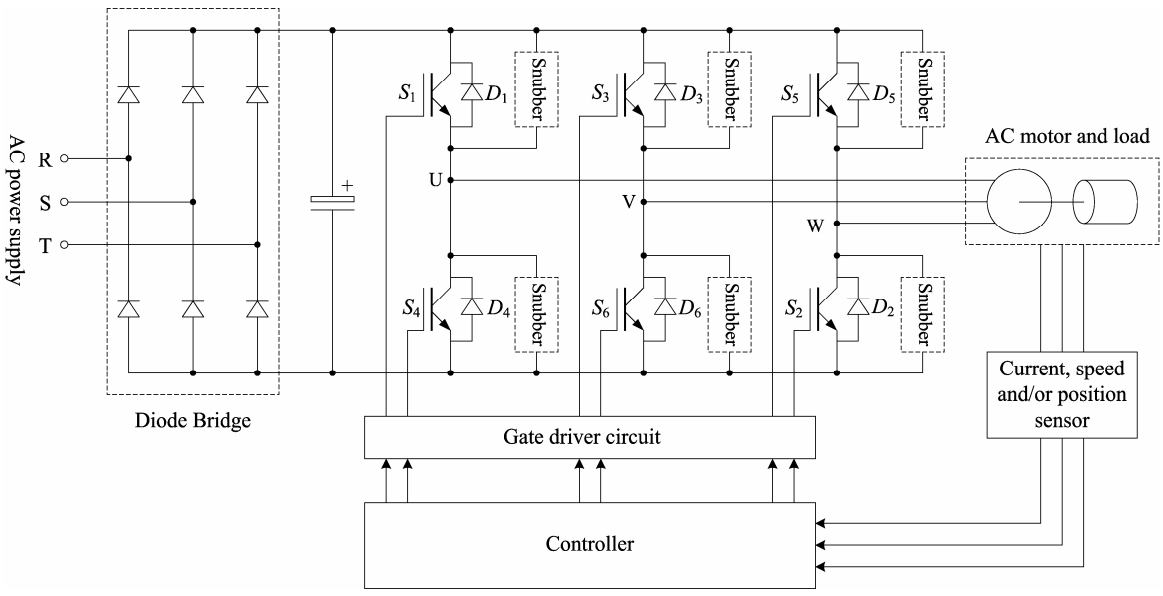


Fig. 1-1. The construction of conventional voltage source three-phase inverter

Power semiconductor switches have non-zero turn-on and turn-off times and thus there is a finite time during the transitions wherein the switches are carrying a significant current while a large voltage is applied across it. This results in large energy dissipation. This energy loss increases with the increasing of switching frequency. The typical voltage and

current waveforms during one cycle of a power semiconductor switch and freewheeling diode are shown in Fig. 1-2 (linear for convenient). Suppose the load current flows through one lower freewheeling diode (e.g. D_4) of the inverter before t_1, one upper power semiconductor switch (e.g. S_1) turned on at t_1. During t_1 and t_2 load current is shifted from freewheeling diode (D_4) to power semiconductor switch (S_1), but there is significant reverse recovery current before the freewheeling diode can block reverse voltage. The reverse recovery current also flows through power semiconductor switch (S_1), so the switching device current is the sum of reverse recovery current and load current. The voltage drop of power semiconductor switch is the same as that of DC link V_S before t_2 (actually it is the sum of DC link voltage V_S and forward voltage drop of freewheeling diode V_{FD} which is relatively small and can be neglected), thus the power loss of the switching device is high during t_1 and t_2 (i.e. high turning on power loss). Similarly there are significant switching power losses of the freewheeling diode during t_2 and t_3.

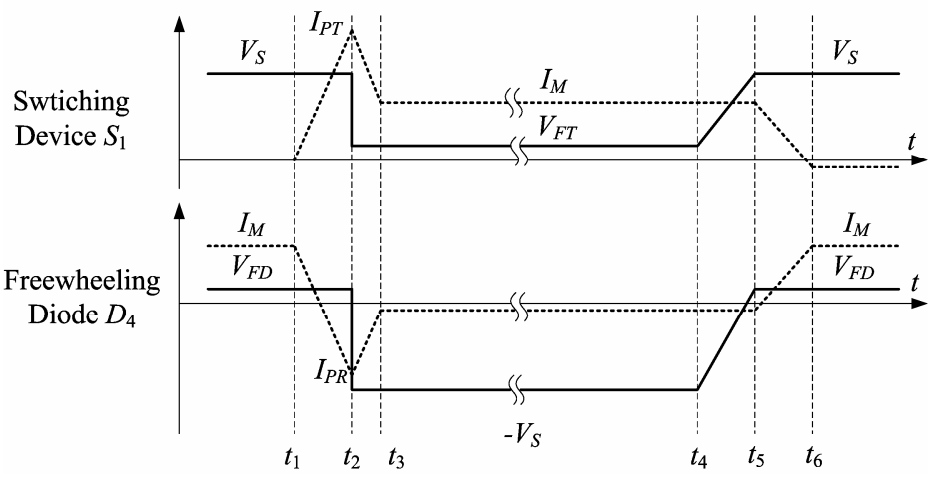


Fig. 1-2. The voltage and current waveforms of power semiconductor switch and freewheeling diode

V_S	Voltage of DC power supplies
V_{FT}	Conduction voltage drop of power semiconductor switch
V_{FD}	Conduction voltage drop of freewheeling diode
I_M	Current of load
I_{PR}	Peak reverse recovery current of freewheeling diode
I_{PT}	Turning on peak current of power semiconductor switch

Then the power semiconductor switch (S_1) is turned off at t_4. Load current is shifted from switching device to freewheeling diode (D_4). The voltage drop of power semiconductor switch rises from conduction voltage drop (several volts) to that of DC link before t_5. From t_5 and t_6 the switching device current decays to zero, but the voltage drop of power

semiconductor switch is the same as that of DC link, so the power loss of the switching device is high during t_4 and t_6 (i.e. high turning off power loss).

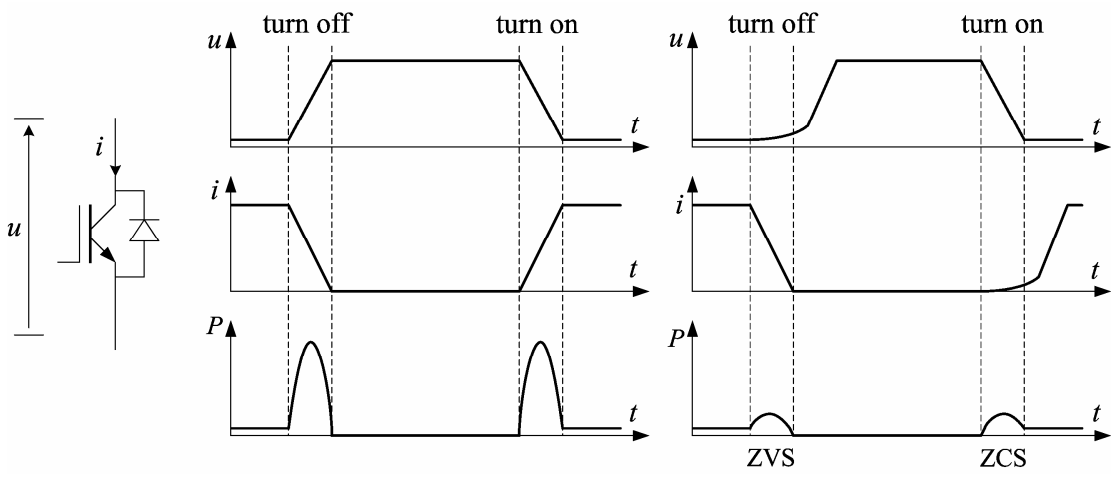
Turning on and turning off power losses are called switching power losses. It is well known that with higher switching frequency, the size of electromagnetic energy storage components like filter inductors and capacitors can be reduced significantly. The performance of the inverter is improved and the output current is more smooth. However the switching power loss increases significantly while the conduction power loss is almost the same. Thus, the total power loss increases significantly. For an IGBT in normal work condition, when the switching frequency is higher than 10kHz, the switching power losses is greater than conduction power losses. The switching power loss is primary for the higher switching frequency inverters.

Besides high power loss, the conventional hard switching has also the following drawbacks [63]:

- Second breakdown: there is turning off current spike for inductive load or turning on voltage spike for capacitive load with hard switching inverter, which can produce excessive localized hot spots to damage power semiconductor switch.
- Severe EMI: In hard switching inverter high *dv*/*dt* and *di*/*dt* induce voltage and current oscillations in parasitic capacitors and inductors during switching transitions. These oscillations result in higher peak current and voltage in the power switches and thus the switching power losses increase. These oscillations can also produce severe EMI which can interfere with other parts of the circuit or surrounding electronic equipment.
- Increase of power semiconductor switch presses: In order to decrease *dv/dt* and *di/dt*, snubber circuit is obligatory, but the snubber can not reduce power losses while it will increase current press on the power semiconductor switches.
- Noise: When the switching frequency is within audio spectrum, it may produce severe acoustic noise.

1.3 Introduction to Soft-switching Inverter

Soft switching has been proven to be an effective means of reducing switching losses and for attaining higher overall efficiencies. Various soft-switching techniques have been developed in recent decades. Soft-switching techniques force the switch voltage or current to zero before the device switching, thus avoiding current and voltage overlap during the switching transition. It can be achieved by either zero-voltage switching (ZVS) or zero-current switching (ZCS). ZVS consists of turning on/off the switches while the voltage across them is zero. ZCS consists of turning on/off the switches when the current through them is zero.



(a) Hard switching (b) Soft switching

Fig. 1-3. Comparison of hard switching with soft switching

ZVS or ZCS can be accomplished by adding small undamped LC networks at strategic places in the inverter circuit and gating the power semiconductor switches on and off at the right opportunities. With soft-switching technology much demerit related to the hard switching can be reduced: reduction of switching power loss, risk of second breakdown, noise and eliminate snubber circuit. Lowering the inverter's overall losses can also make it possible to reduce its size by using smaller cooling apparatus. The switching waveforms in the conventional hard switching inverter and soft switching inverter are shown in Fig. 1-3. From the figure we can see that overlap of voltage drop and current of the soft-switching inverter is reduced, so the switching power loss can be reduced. ZCS turn on and ZVS turn off are similar to that of Fig. 1-3(b).

Soft switching technique was first introduced in DC/DC converter from the beginning of 1980s, such as Quasi-Resonant Converter (QRC) [25, 45, 46], Series Resonant Converter (SRC) [7, 83], Parallel Resonant Converter (PRC) [2, 93], Series-Parallel Resonant Converter (SPRC) [3, 69, 84], Multi-element Resonant Converter (MRC) [1, 35, 77, 94]. In 1986, D.M. Divan introduced soft switching technique in DC/AC inverter. In electric motor drive applications, soft-switching inverters are usually classified in three categories, namely resonant DC link inverters (RDCLI), resonant pole inverters (RPI) and resonant AC link inverters [6, 58].

1) Resonant DC Link Inverter

The structure of a resonant DC link inverter [17] is shown in Fig. 1-4. LC resonant circuit was added between DC power supply and 6-switches inverter. All power semiconductor switches' snubber circuit can be eliminated. Resonance occurs periodically or at controlled instant to make DC link voltage reach zero temporarily during which the power semiconductor switches at the output section could be switched on or off under ZVS condition.

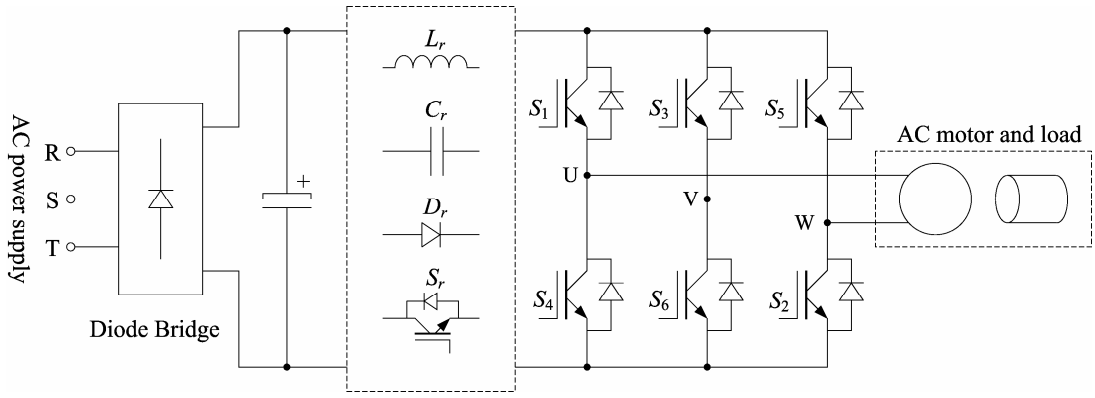


Fig. 1-4. The structure of resonant DC link inverter

2) Resonant Pole Inverter

The structure of a resonant pole inverter [18] is shown in Fig. 1-5. There is a so-called resonant pole that comprises a resonant inductor and a pair of resonant capacitors at each phase leg. These capacitors are directly connected in parallel with the main switches in order to achieve ZVS. In contrast to resonant DC link inverters, no resonance is produced

at the DC link. Instead of that, the resonant transitions occur separately at each resonant pole, only when the switches in the output stage need to be commutated. The DC link voltage remains unaffected during the resonant transitions. Therefore, the main switches in the inverter phase legs can be commutated totally independent from each other and we can choose the commutation instant freely. One of the disadvantages of the resonant pole inverter is that relatively more auxiliary switches are needed than that of resonant DC link inverter.

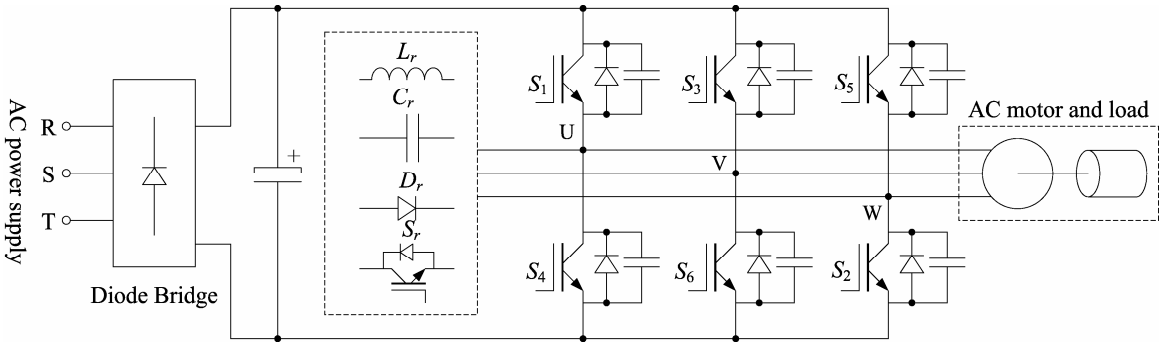


Fig. 1-5. The structure of resonant pole inverter

3) Resonant AC Link Inverter

The structure of the resonant AC link inverter [58] is similar to the resonant DC link inverter. The resonant tank in the AC link produces a high-frequency alternating voltage or a high-frequency alternating current. The switches of both the source-side and the load-side inverters are turned on and off when the voltage or the current in the AC link passes through zero, minimizing the switching losses.

1.4 Controller

Fuzzy logic, or fuzzy set theory, was first presented by Zadeh [53]. The main idea of fuzzy logic control [26, 48, 53] is to use the control ability of human being which includes experience and intuition, so the nature of the controller has adaptive characteristics that can achieve robust response to a system with uncertainty, parameter variation, and load disturbance. PI controller has the advantage of fast response especially in motor starting, but it will introduce overshoot and oscillation. The fuzzy logic controller can solve these problems while it is slower response than that of PI controller.

To utilize the advantages of both PI and fuzzy logic controllers to provide better response than any one controller only, a hybrid controller with fuzzy logic and PI will be introduced in this thesis.

A variable speed electric drive system is normally controlled by a speed/current double closed-loop controller. In conventional control system, during starting, the current reaches its maximum value quickly which contributes to the fast response of the system as the motor runs with maximum acceleration. When the motor reaches the desired speed, the current can not be reduced to its steady state value immediately; it needs time to settle. Normally overshoot and oscillation are inevitable, settling time is multiple that of the starting time. If current reaches its maximum value immediately during starting and when the motor reaches desired speed, the current skips to its steady state value at the same time and the motor runs at the desired speed, the starting time is shortest and the settling time is only the starting time. If the motor reaches desired speed while the current can only skip to around the steady state value, there is oscillation too, but the oscillation is smaller than that of conventional control system and the settling time can be reduced greatly, too.

To achieve fast starting, the key is to determine (predict) the steady state reference current during starting. An artificial neural network (ANN) [5, 10, 15] is a computational network, consisting of a number of interconnected processing units (neurons), which is able to learn and represent the unknown dependency relationship between a set of input variables and a set of output variables of a system. By selecting the training patterns (acceleration, speed, current, DC link voltage, reference speed) which cover all conditions (i.e. various DC link voltage, various load, various moment of inertia, various reference speed) to train the neural network, the neural network is then possible to predict the SSRC according to the acceleration, speed, current, DC link voltage, reference speed of the drive system, although the predicted value may be not very accurate.

1.5 Objectives and Major Contributions

The objectives of this research work are as follows:

- To conduct a literature survey on soft-switching inverter and find possible topology which is applicable to BDCM drive system;
- To survey the current close-loop controller for variable speed drive system and offer new solutions to improve the performance of the system.

The major contributions are:

- Find a transformer based resonant DC link inverter which can generate DC link voltage notches during chopping switches commutation to guarantee all switches working in zero voltage switching condition. The inverter has the advantages: all switches work under soft-switching condition; voltage stress on all the switches would be not greater than DC supply voltage; only one DC link voltage notch is needed during one PWM cycle, and the switching frequency of the auxiliary switches would not higher than PWM frequency; *dv*/*dt* and *di*/*dt* are reduced significantly to reduce EMI, does not need center taped DC link capacitor; simple auxiliary switches control scheme and so on.

- Propose a novel resonant pole inverter, which is special to brushless DC motor drive system. The inverter possesses the advantages: low switching power loss; low inductor power loss; all switches work under soft-switching condition; voltage stress on all the switches would be not greater than DC supply voltage; The normal operation of the inverter is entirely the same as hard switching inverter; simple auxiliary switches control scheme; *dv*/*dt* and *di*/*dt* are reduced significantly to reduce EMI and so on.

- A hybrid controller for the PM BDCM drive system is proposed which holds the advantages of both PI controller and fuzzy controller, i.e. fast response, little overshoot, little oscillation, robust to system parameters variation, stability and so on.

- Propose a steady state reference current (SSRC) prediction technique based on neural network for PM BDCM drive system. Conventional controller combines with this technique can improve system response speed, reduce overshoot and oscillation.

1.6 Organization of this thesis

This thesis comprises the brief describing the operation principle of BDCM, literature review of resonant DC link inverter and resonant pole inverter, analysis of proposed novel resonant DC link inverter and resonant pole inverter for BDCM drive system. Simulation and experiment are also proposed to verify the analysis. This thesis also proposes a fuzzy and PI hybrid controller that holds the advantages of PI and fuzzy logic controller. Then steady state reference current (SSRC) prediction technique will be introduced, Conventional controller with this technique holds the advantages of fast response, little overshoot, robust and so on. There are seven chapters in this thesis, the first chapter is the introduction of research work which contains background, overview of soft-switching inverter and major contribution of this thesis. The main contents are presented in Chapter 2, 3, 4, 5 and 6, respectively.

In Chapter 2, the operation principle of BDCM will be introduced first, the controller of the BDCM will be briefly described, then one novel method to reduce torque ripple will be proposed.

In Chapter 3, known resonant DC link inverter topologies will be reviewed, then a transformer based resonant DC link inverter for BDCM drive system will be proposed. The operation principle and control scheme of the inverter are analyzed. Simulation and experimental results are proposed to verify the theoretical analysis.

In Chapter 4, literature review of resonant pole inverter will be proposed first, then a special design resonant pole inverter for BDCM drive system will be offered. The operation principle of the inverter is analyzed. Simulation and experimental results are proposed to verify the theoretical analysis.

In Chapter 5, a hybrid controller for the PM BDCM drive system which holds the advantages of both PI and fuzzy logic controller will be proposed. The design of the controller will be described in detail. Experimental results are given to verify the feasibility of the controller.

In Chapter 6, a steady state reference current (SSRC) prediction technique based on neural network for PM BDCM drive system will be proposed. The SSRC prediction technique is described in detail. Hardware implementation and experimental results are proposed.

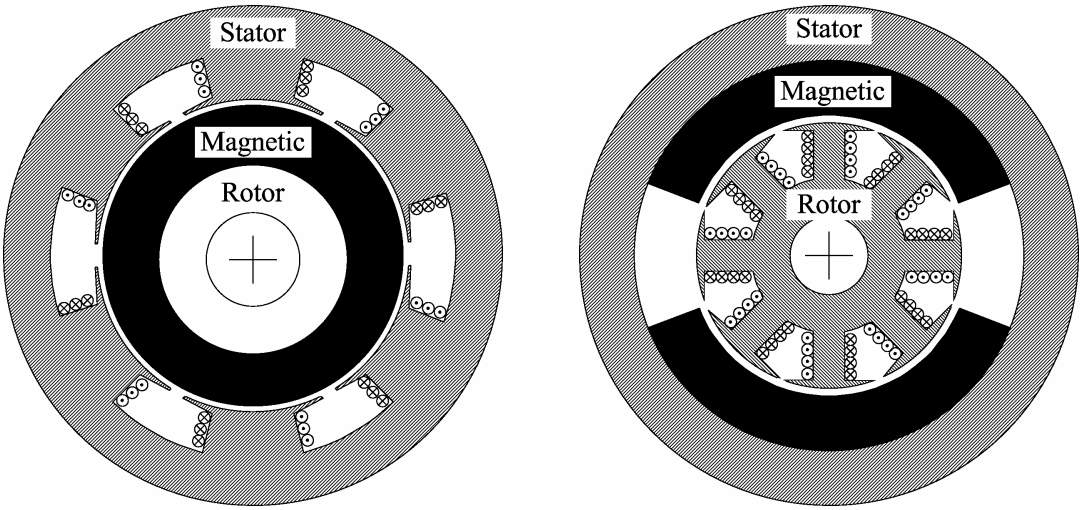
Finally, a summary of the research work and some suggestions for further developments are given in chapter 7.

Chapter 2 Brushless DC Motor

The earliest prototype of a brushless DC motor (BDCM) was built up in 1962 when T.G. Wilson and P.H. Trickey made a "DC Machine with Solid State Commutation". It was subsequently developed as a high torque, high response drive for specialty applications such as tape and disk drives for computers, robotics and positioning systems, and in aircraft. With the advent of powerful permanent magnetic materials and power semiconductor switches in the early to mid 1980s, the ability to build a high power BDCM became reality. Today, almost all of the major motor manufacturers make BDCM in at least some horsepower sizes and makes BDCM from 1/2 to 500 hp as a complete product line.

2.1 Operation Principle

The structure of BDCM [78, 81] is shown in its most usual form in Fig. 2-1 alongside the PM DC commutator motor. The stator structure is similar to that of a polyphase AC induction motor. The function of the magnet is the same in both the BDCM and the DC commutator motor. In both cases the air gap flux is fixed by the magnet and little affected by armature current. BDCM works on the same principle as DC commutator motor but the motor is built "inside out" with the fields (which are permanent magnets) on the motor rotor and the "armature" on the outside. The fields magnets and the "armature" stays stationary. The action of the commutator (which no longer needs to exist since the winding is now stationary) is implemented by a shaft encoder and a controller. The shaft encoder (which is mostly a Hall sensor) is to sense the magnetic position of the fields on the shaft. The controller determines which winding(s) should be active according magnetic position to produce maximum torque. In this way the motor and controller act in the same way as a DC commutator motor without the brushes. The controller is made up of an inverter which is similar in topology to the inverter used in induction motor drives if the BDCM has three phases.



(a) BDCM (b) PM DC commutator motor

Fig. 2-1. The structure of brushless DC motor and PM DC commutator motor [78]

The most obvious advantage of the brushless configuration is the removal of the brushes. Brush maintenance is no longer required, and many problems associated with brushes are eliminated. For example, brushes tend to produce RFI (radio-frequency interference) and the sparking associated with them is a potential source of ignition in inflammable atmospheres. The absence of commutator and brush reduces the motor length. This is useful not only as a simple space saving, but also as a reduction in the length between bearings. So that for a given stack length the lateral stiffness of the rotor is greater, permitting higher speeds or a longer active length/diameter ratio. This is important in servo-type drives where a high torque/inertia ratio is required. The removal of the commutator reduces the inertia still further. Another advantage of the brushless configuration is that the stator is outside and more cross-sectional area is thus available for the windings. At the same time the conduction of heat through the frame is improved. Generally an increase in the electric loading is possible providing a greater specific torque.

The basic torque and back EMF equations of the BDCM are quite simple and resemble those of the DC commutator motor. A simple "concept machine" is shown in Fig. 2-2(a). The two-pole magnet has a pole arc of 180 degrees. The air gap flux-density waveform is ideally a square wave as shown in Fig. 2-2(b). In practice, fringing causes the corners to be somewhat rounded. The coordinate axes have been chosen so that the centre of a north pole of the magnet is aligned with the x-axis, i.e. at θ=0. The stator has 12 slots and a three-phase winding. Thus there are two slots per pole per phase. Each phase winding

consists of two adjacent full-pitch coils of N_1 turns each, whose axes are displaced from one another by 30 degrees. The winding is a single-layer, and any slot contains N_1 conductors from only one phase winding. Consider the flux-linkage ψ_1 of coil a_1A_1 as the rotor rotates which is shown in Fig. 2-2(c). The flux-linkage varies linearly with rotor position because the air gap flux-density set up by the magnet is constant over each pole-pitch of the rotor. Maximum positive flux-linkage occurs at 0° and negative flux-linkage at 180°. By integrating the flux-density around the air gap, the maximum flux-linkage of the coil can be found as

$$\psi_{1\max} = N_1 \int B(\theta) r_1 d\theta \cdot l = N_1 B_g \pi r_1 l \tag{2-1}$$

Where B_g is the air gap flux-density, r_1 is the rotor radius, l is the rotor axial length. The variation with θ as the rotor rotates from 0 to 180° is given by

$$\psi_1(\theta) = \left[1 - \frac{\theta}{\pi/2}\right] \psi_{1\max} \tag{2-2}$$

The back EMF induced in coil a_1A_1 is given by

$$e_1 = -\frac{d\psi_1}{dt} = -\frac{d\psi_1}{d\theta}\frac{d\theta}{dt} = -\omega\frac{d\psi_1}{d\theta} = 2N_1 B_g l r_1 \omega \tag{2-3}$$

This represents the magnitude of the square-wave back EMF. The back EMF e_{a1} induced by coil a_1A_1 is shown in Fig. 2-2(d). The back EMF e_{a2} induced in the second coil a_2A_2 is identical, but retarded in phase by 30°, which is shown in Fig. 2-2(e). If the two coils are connected in series, the total phase back EMF e_a is the sum of the two separate coil back EMF, which is shown in Fig. 2-2(f). The basic effect of distributing the winding into two coils is to produce a stepped back EMF waveform. In practice, fringing causes its corners to be rounded, as shown by the dotted lines. Then the back EMF waveform has the "trapezoidal" shape that is characteristic of the BDCM. With 180° magnet arcs and two slots per pole per phase, the flat top of this waveform is ideally 150° wide, but in practice the fringing field reduces this to a somewhat smaller value, possibly as little as 120°. The magnitude of the flat-topped phase back EMF e is given by

$$e = 2N_{ph} B_g l r_1 \omega \tag{2-4}$$

Where N_{ph} is the number of turns in series per phase.

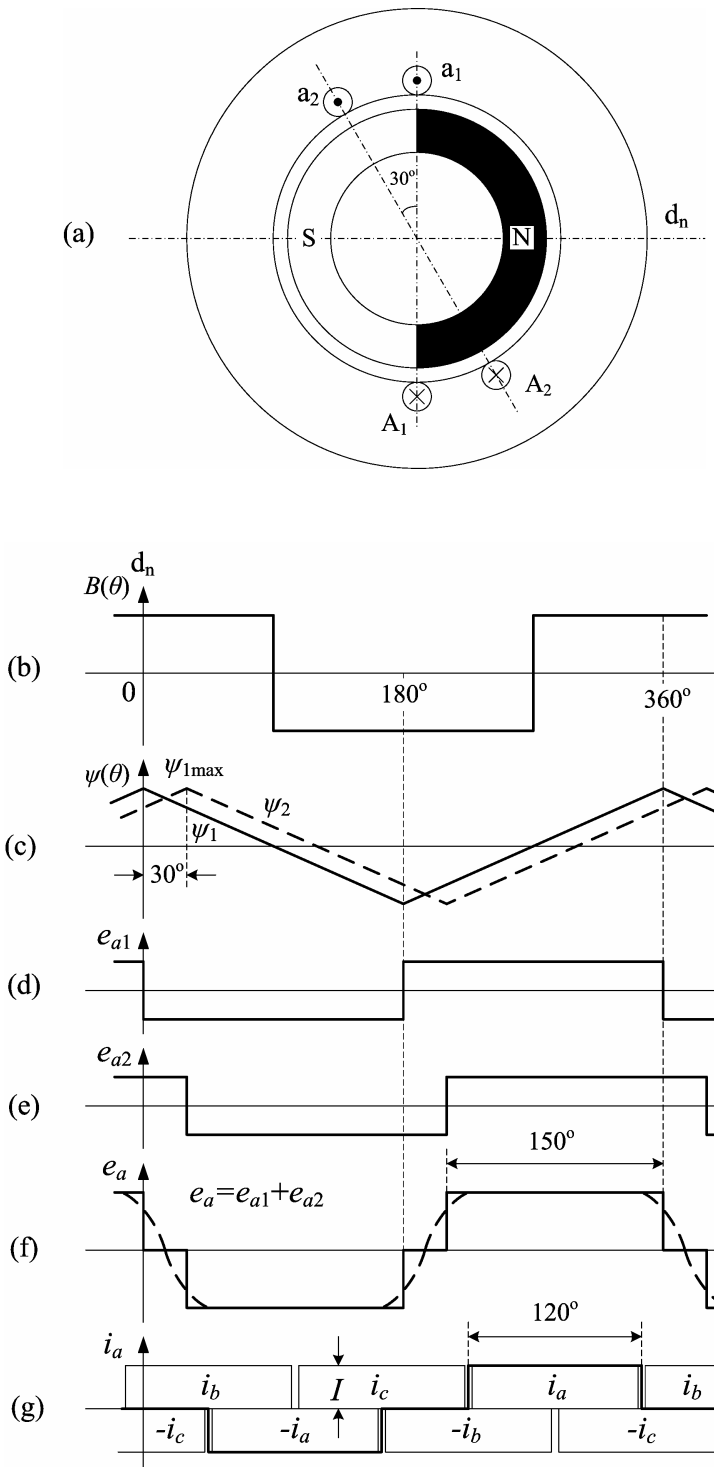


Fig. 2-2. BDCM with ideal waveforms of flux-density, back EMF and current [78], (a) Motor showing two coils of one phase, (b) Magnet flux-density around the air gap. (c) Flux-linkage of coils 1 and 2 as the rotor rotates, (d) Back EMF waveform of coil 1. (e) Back EMF waveform of coil 2. (f) Back EMF waveform of phase a. (g) Ideal phase current waveforms.

An ideal rectangular waveform of phase current with pulse width 120 electrical degrees and magnitude I is shown in Fig. 2-2(g). If the phase windings are star-connected, at any

time there are just two phases conducting. During any 120° interval of phase current the instantaneous power being converted from electrical to mechanical is

$$P = \omega T_e = 2eI \tag{2-5}$$

The '2' in this equation arises from the fact that two phases are conducting. Using the expression derived above for the back EMF, the electromagnetic torque is given by

$$T_e = 4N_{ph}B_g l r_1 I \tag{2-6}$$

This equation is valid for any number of pole-pairs. The similarity between the brushless motor and the commutator motor can now be seen. Writing $E=2e$ to represent the combined back EMF of two phases in series, the back EMF and torque equations can be written in the form

$$E = k\phi\omega \qquad \text{and} \qquad T = k\phi I \tag{2-7}$$

Where $k = 4N_{ph}/\pi$ and $\phi = B_g r_1 \pi l$. k is the "armature constant" and ϕ is the flux. These equations for back EMF and torque are similar to those of the DC commutator motor; only the form of the constant k is different. It is clear that with ideal wave shapes and with perfect commutation, these equations are true at all instants of time. The electronic commutation of the inverter switches has thus assumed the function of the mechanical commutator in the DC commutator motor, to give a pure DC machine with constant, ripple-free torque. In practice, of course, none of the ideal conditions can be perfectly realized. The main result of this is to introduce ripple torque, but the basic relationships of the back EMF proportional to speed and the torque proportional to current remain unchanged.

2.2 Controller

2.2.1 Controller

The structure of simplest controller for BDCM drive is shown in Fig. 2-3 [78]. The rotor position is sensed by a Hall-effect sensor, a slotted optical disk or some other transducer,

providing signals as represented in Table 2-1. These signals are decoded by combinatorial logic to provide the firing signals for 120º conduction on each of the three phases.

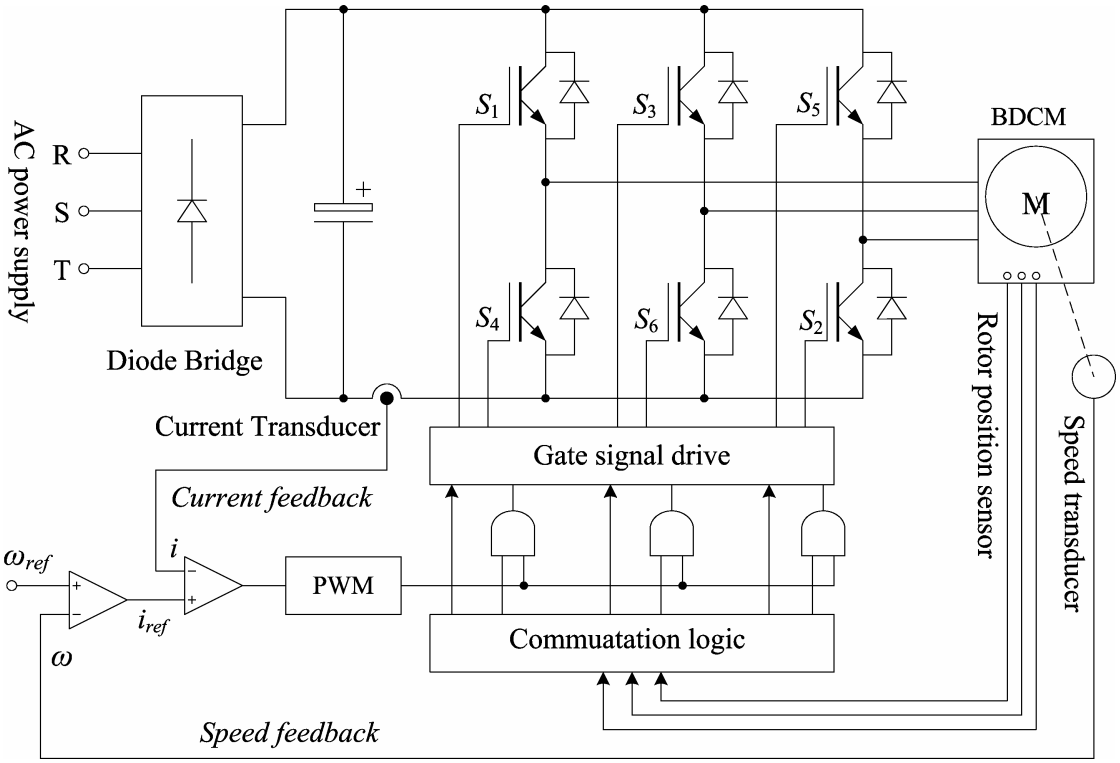


Fig. 2-3. The structure of controller for BDCM drive

Table 2-1 Commutation logic of BDCM

(180º Magnet-Star winding, 120º square-wave phase currents BDCM)

Direction	Position	Hall signal			Switching state					
		A	B	C	S_1	S_4	S_3	S_6	S_5	S_2
Forward	0º - 60º	1	0	0	1	0	0	0	0	1
	60º - 120º	1	0	1	1	0	0	1	0	0
	120º - 180º	0	0	1	0	0	0	1	1	0
	180º - 240º	0	1	1	0	1	0	0	1	0
	240º - 300º	0	1	0	0	1	1	0	0	0
	300º - 360º	1	1	0	0	0	1	0	0	1
Reverse	0º - 60º	1	0	0	0	1	0	0	1	0
	300º - 360º	1	1	0	0	0	0	1	1	0
	240º - 300º	0	1	0	1	0	0	1	0	0
	180º - 240º	0	1	1	1	0	0	0	0	1
	120º - 180	0	0	1	0	0	1	0	0	1
	60º - 120º	1	0	1	0	1	1	0	0	0

The basic forward control loop is voltage control, implemented by PWM (voltage reference signal compared with triangular wave). The PWM is applied only to the lower phaseleg power semiconductor switches. This not only reduces the current ripple but also avoids the need for wide bandwidth in the level-shifting circuit that feeds the upper phaseleg power semiconductor switches. From a control point of view, the BDCM is similar to the DC commutator motor, as the simple torque and voltage equations shown. Consequently it is possible to implement current (torque) feedback and speed feedback in the same way as for the DC motor.

Sometimes the instantaneous current in the BDCM is regulated in each phase by a hysteresis-type regulator that maintains the current within adjustable limits. This is called "current mode" control and several algorithms are possible to control the switching.

The commutation logic and the three AND gates in Fig. 2-3 can be implemented by GAL programmable logical device. With Advanced Boolean Equation Language (ABEL) [70, 91] and commutation logic table (Table 2-1), the source file can be written (Appendix A). Then the source file is compiled into Joint Electron Device Engineering Council (JEDEC) standard file. The JED file is written to the GAL chip 16V8 using programmer and the commutation logic IC for BDCM is thus created.

2.2.2 Speed sensor

Speed feedback signal can be obtained from a tachometer-generator, optical encoder, resolver or derived from rotor position sensor. A tachometer generator is a generator (DC or AC generator) with its shaft mounted on the object which can develop a voltage proportional to the object speed. The generator has low moment of inertia and small electromagnetism time constant.

An optical encoder [40] consists of a rotating disk, a light source, and a photodetector (light sensor). The disk, which is mounted on the rotating shaft, has coded patterns of opaque and transparent sectors. As the disk rotates, these patterns interrupt the light emitted onto the photodetector, generating a digital or pulse signal output. Traditionally, two very different types of encoders exist in automation: Incremental and Absolute. The

two types vary greatly in their design and in the type of interface electronics typically used to read the encoder. Applications determine which type of encoder is required to satisfy a particular system requirement. Incremental encoders are most commonly used due to their low cost and simple application. Quadrature encoders are the most common incremental style and widely used in all forms of automation. This type of encoder has two channels, which output digital square waves proportional to the number of windows on the optical code disk. The quadrature encoders signals are shown in Fig. 2-4. The quadrature name comes from the fact the two channels are phase shifted by 90˚ to each other; the offset phasing relationship reverses between the two signals for opposite direction of encoder shaft rotation. By observing the phase sequence between the two digital output channels, a controller can determine the direction of shaft rotation. Additionally, Incremental square waves are counted by a controller to determine shaft position, velocity and/or acceleration. A third channel with a once per rotation signal is often found on incremental encoders and is commonly called the index or reference pulse. This signal is typically used to mark a particular location in a system's rotation that corresponds to a known mechanical location often called a home position.

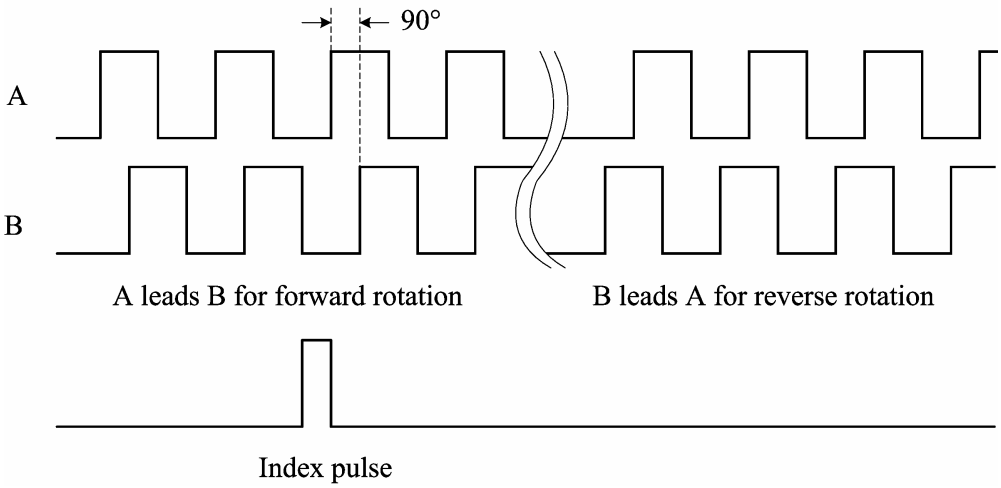


Fig. 2-4. Quadrature encoder signals

The drawback to an incremental encoder in a control system is that if the controller's counter loses power or miscounts, the system must be cycled back to a known location, such as an index location, before restarting. Normally an absolute encoder is used instead of an incremental encoder in order to overcome this problem. Absolute encoders provide position information in a very different manner. The noticeable difference is with the disk

pattern and sensing system. The absolute encoder disk is made up of several tracks with alternating light and opaque segments, which correspond with several tracks of photo detectors to form a distinct multi-bit word. The final result for the absolute encoders is a unique multi-bit word defining a unique shaft location. A 4-bit absolute encoder disk is shown in Fig. 2-5, the number of each position is also marked. Motion control systems using absolute feedback do not require a restart sequence in case of losing power, they simply read the encoder output word and determine the exact absolute shaft position.

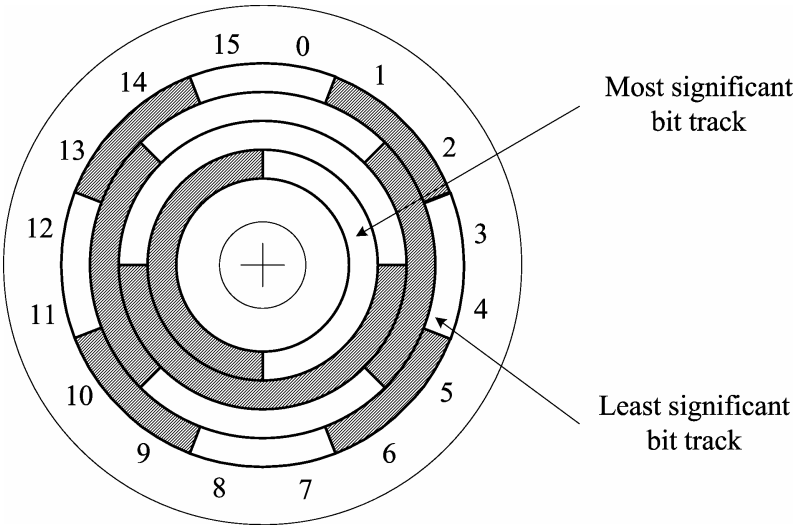


Fig. 2-5. A 4-bit absolute encoder disk

A resolver is a position sensor or transducer which measures the instantaneous angular position of the rotating shaft to which it is attached. Resolvers are typically built like small motors with a rotor (mounted on the object shaft), and a stator (stationary part) which produces the output signals. The word resolver is a generic term for such devices derived from the fact that at they resolve the rotor mechanical angle into orthogonal or Cartesian (x and y) components. From a geometric perspective, the relationship between the rotor angle and its x and y components is that of a right triangle. Then all resolvers produce signals proportional to the sine and cosine of their rotor angle. To get the rotor angle, a resolver-to-digital converter is required which performs two basic functions: demodulation of the resolver format signals to remove the carrier, and angle determination to provide a digital representation of the rotor angle. Since every angle has a unique combination of sine and cosine values, a resolver provides absolute position information within one revolution (360°) of its rotor. This absolute (as opposed to

incremental) position capability is one of the resolver's main advantages over incremental encoders.

If the rotor position of a BDCM is sensed by a Hall-effect sensor and no critical speed is required, the speed signal can be obtained by measuring the width of three Hall signals to reduce cost as shown in Fig. 2-6. We can get 60^o electrical angle width square wave Q from three Hall signals marked A, B, C which are with 120^o electrical angle shift. The width of the pulse Δw can be obtained by detecting both edges of the wave via a timer which can be easily implemented by any microprocessor. The motor speed ω_r is inversely proportional to the width Δw.

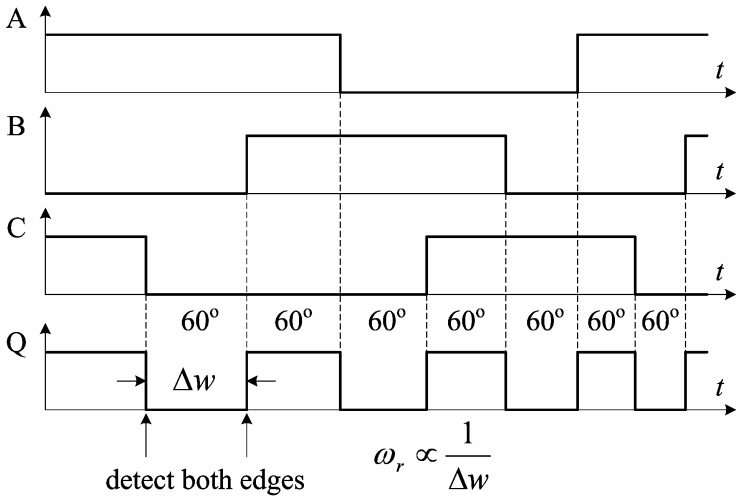
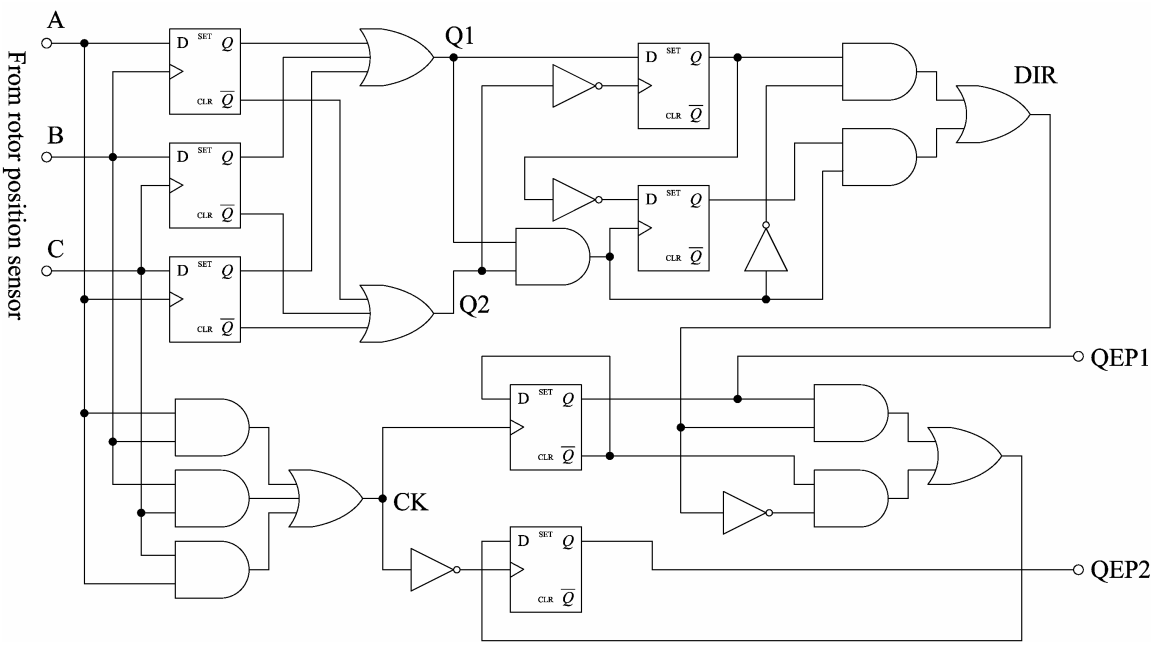
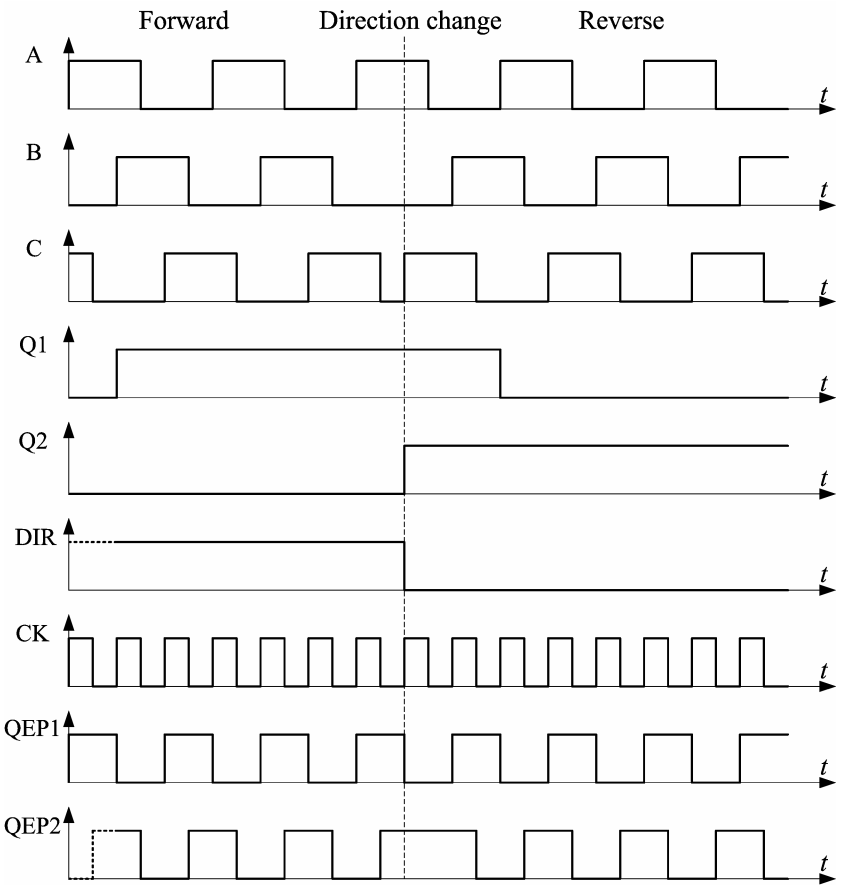


Fig. 2-6. Hall signal for speed measurement

Quadrature Encoder Pulse (QEP) is a standard digital speed or position signal and can feed into many devices (e.g. TMS320C24x DSP has QEP receive circuit). In high speed BDCM, the QEP can be derived from rotor position. The converter circuit and interesting waveforms are shown in Fig. 2-7. Where Hall signals marked A, B, C are the inputs and QEP1 and QEP2 are the outputs. Some microprocessors have digital counter and can accept DIR and CK signal, thus the converter circuit can be simpler. The circuit can be implemented by Complex Programmer Logical Device (CPLD) and only occupy partial resource of the chip. The circuit can also be implemented by one GAL 16V8 IC and four dual D flip-flop IC (e.g. 74LS74) (Appendix B).



(a) Converting Hall signal to QEP circuit



(b) Key waveforms

Fig. 2-7. Circuit for deriving QEP from Hall signal and waveforms

2.2.3 Gate drive for IGBT

In general, there will be level-shifting circuits to buffer the outputs of the logic circuit and provide the drive to the power semiconductor switches. Fig. 2-8 shows the gate driver circuit for a single IGBT. The input buffer state is made up of hex inverter buffer 74LS06 and a current limiting resistor. A Photocoupler gate driver, TLP250, is used to implement the gate drive circuit. This gate driver provides a peak output current of 1.5A. This current capability is good enough to drive the IGBT being used. It also isolates the input signal from the output so that common mode noise is reduced. An IGBT needs a voltage in +15V ~ +20V to turn-on and –5V ~ -10V to turn-off. The input to the gate driver is only 5V. To get the required output voltage and reduce the number of isolated DC power supply, a +7V Zener diode is used to get the required negative turn off voltage. Thus the driver circuit can provide +17V for turn on and –7V for turn off with only single +24V output DC power supply.

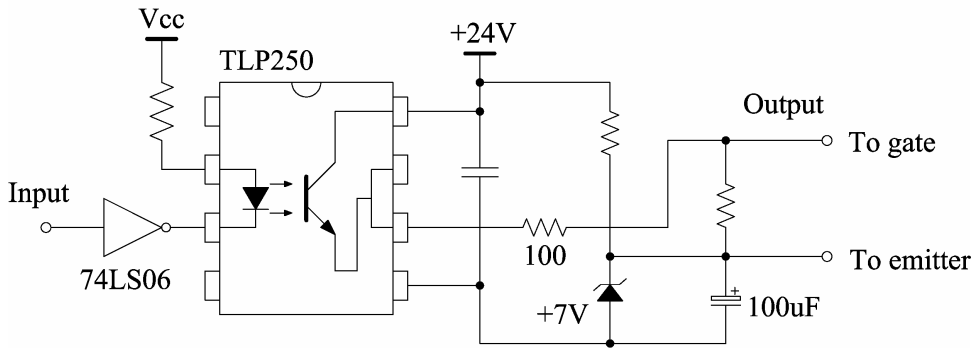


Fig. 2-8. Gate driver circuit for IGBT

For inverters, the emitters of three lower main switches are commonly connected together, the gate driver for these switches can use one common output DC power supply. However, the emitters of three upper main switches have no common nodes, the gate driver for one upper main switch should use one individual output DC power supply. Thus four isolated DC power supplies are needed for gate driver of 6 main switches. If soft switching is adopted and auxiliary switches is added, more isolated DC power supplies is required. All the DC power supplies for gate driver and control circuit can be built up by switching mode power supply (SMPS). The drive board for the inverter is introduced in Appendix C in detail.

To save the number of output DC power supply, bootstrap circuit can be adopted. The bootstrap circuit [42] is proposed by International Rectifier company and adopted in gate driver, such as IR2110, IR2113. This method has the advantage of only one insulated DC power supply is needed for 6 switches gate driver in a three-phase full bridge inverter, but has some limitations, such as duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The Gate driver circuit for two switches in one phase leg with bootstrap supply is shown in Fig. 2-9. The bootstrap circuit is formed by a bootstrap diode D_{bs} and bootstrap capacitor C_{bs}. The bootstrap capacitor voltage v_{bs} (the voltage difference between the v_{hb} and v_{hl} pins on the IC TLP250) provides the supply to the high side driver circuitry of the gate driver IC TLP250. This supply needs to be in the range of 17 - 27V (normally the turn on voltage for an IGBT is 10 ~ 20V) to ensure that the gate driver IC can fully enhance the IGBT S_h being driven. This v_{bs} supply voltage is a floating supply that sits on top of the DC link.

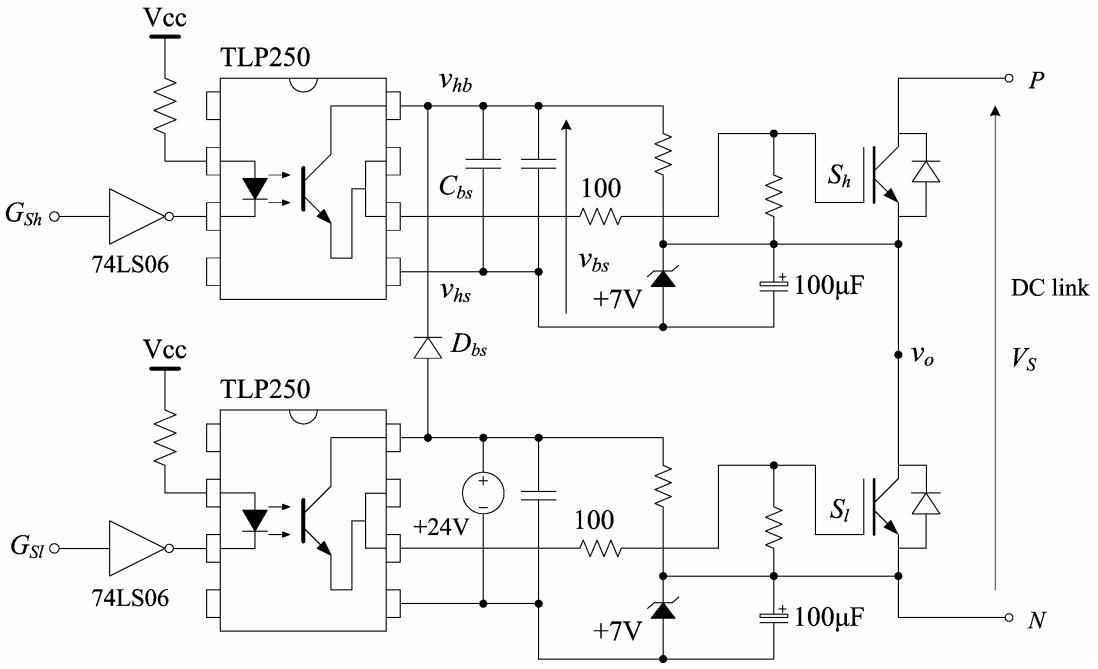


Fig. 2-9. Gate driver circuit for two switches in one phase leg with bootstrap supply

The operation of the circuit is as follows. When v_o is pulled down to ground (turn on lower switch S_l), the bootstrap capacitor C_{bs} is charged through the bootstrap diode D_{bs} from the +24V supply, thus providing a supply to v_{bs}. To reduce leakage current of bootstrap capacitor, it is always better to use a non-electrolytic capacitor. The bootstrap capacitor C_{bs} is charged only when v_o is pulled down to ground. Therefore the turn on

time for the lower switch S_l should be sufficient to ensure the full charging of bootstrap capacitor C_{bs}. The bootstrap diode D_{bs} needs to be able to block the full DC link voltage, which is seen when the upper switch S_h is turned on. It must be a fast recovery device to minimize the amount of charge fed back from the bootstrap capacitor into the +24V supply, and similarly the high temperature reverse leakage current would be important if the capacitor has to store charge for long periods of time.

The gate driver with bootstrap supply can be applied to the inverter directly where the upper switches and the lower switches are turned on alternately, such as inverter for induction motor, induction heating, standby power supplies and so on. When the gate signal is minor modified, the gate driver can be also applied to the inverter for BDCM. The PWM signal is applied to the upper phaseleg switches other than lower phaseleg switches in conventional inverter.

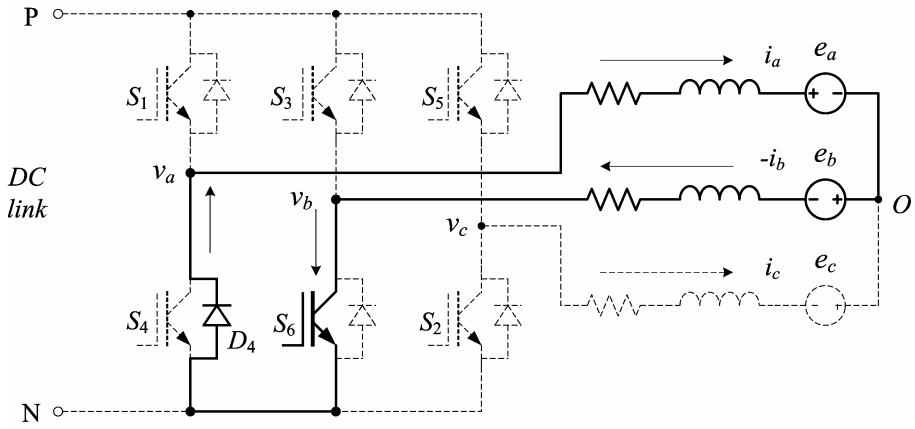


Fig. 2-10. Freewheeling path when switch S_1 is turned off

Suppose PWM signal is applied to the upper switch S_1 and the lower switch S_6 is turned on. During freewheeling, phase current i_a flows through the freewheeling diode D_4 as shown in Fig. 2-10. The phase voltage v_a is clamped to the ground and the bootstrap capacitor for the gate driver circuit of the upper switch S_1 can be charged. During phase current commutation, if the switching state is changed from one lower switch to another lower switch, there is no problem as the gate driver circuit for the lower switch is not supplied by bootstrap capacitor. During phase current commutation, if the switching state is changed from one upper switch to another upper switch, e.g. turn off S_1 and turn on S_5, before turning on the upper switch S_5, the lower switch S_2 should be turned on for a short

time beforehand to charge the bootstrap capacitor for the gate driver circuit of the switch S_5, which will not affect the operation of BDCM as the time of turning on the switch S_2 is very short and the phase current i_c will not increase much due to bulk motor inductance.

2.3 12-switches Inverter to Reduce Torque Ripple

In relation to the commutation of the inverter, the back EMF is essentially at its full value when the outgoing phase is commutated, and this back EMF is in such a direction as to drive the current down and assist in the commutation. On the other hand, the back EMF is of equal value in the incoming phase and is in such a direction as to oppose the current build-up. This is the primary reason for the current ripple. So the BDCM drive system with conventional three phase full wave inverter has the demerit of current ripple during commutation and the torque ripple of is also high. Many methods to reduce torque ripple has been proposed [12, 79, 95], but these methods show limited effectiveness in practical applications due to motor parameter sensitivity and dissatisfactory performance over wide speed range. In this section, one 12-switches inverter for BDCM will be introduced [99], which can commutate the phase current more freely and reduce the torque ripple.

2.3.1 Commutation process with conventional inverter

Assumption the rotor reluctance of BDCM is constant independent rotor position θ_r and only the fundamental components of the flux linkages contributed by the permanent magnet are considered. Then the mathematical model of the BDCM can be expressed as [67]

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} L & M & M \\ M & L & M \\ M & M & L \end{bmatrix} p \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \tag{2-8}$$

Where R is the phase resistance, L is phase inductance, M is the mutual inductance, v is the phase voltage, i is the phase current, e is the phase back EMF, p is the derivational operator $\frac{d}{dt}$.

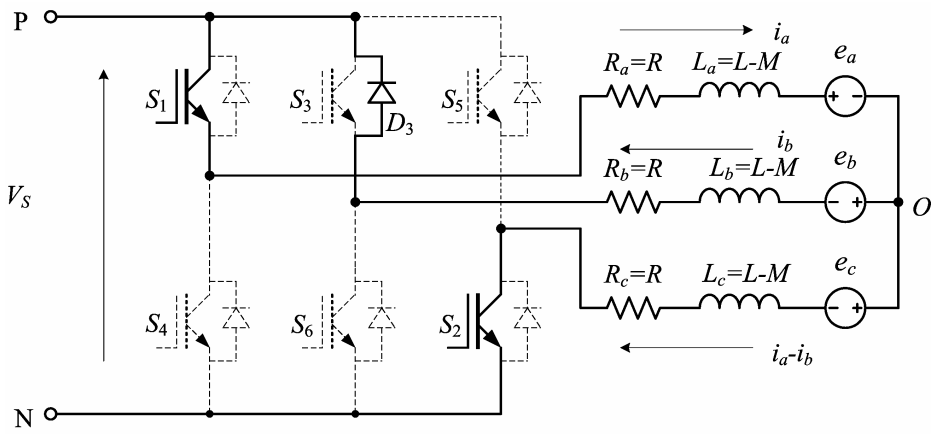


Fig. 2-11. Equivalent circuit during commutation

For Y-connected BDCM with conventional three-phase full wave inverter, Equation (2-8) can be changed to

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} L-M & 0 & 0 \\ 0 & L-M & 0 \\ 0 & 0 & L-M \end{bmatrix} p \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \quad (2\text{-}9)$$

$$T_e = (e_a i_a + e_b i_b + e_c i_c)/\omega_r \quad (2\text{-}10)$$

So the equivalent circuit of the BDCM drive system during commutation can be simplified as Fig. 2-11 (Assume commutation from +A-B => +A-C, "+" means current flow from the positive pole of supply, "-" means current flow to the negative pole).

Neglecting the voltage drop across switches and diodes, the governed voltage and current equation can be obtained

$$\begin{cases} V_S = i_a R_a + L_a \dfrac{di_a}{dt} + e_a + e_c + L_c \dfrac{d(i_a - i_b)}{dt} + (i_a - i_b) R_c \\ i_a R_a + L_a \dfrac{di_a}{dt} + e_a + e_b + L_b \dfrac{di_b}{dt} + i_b R_b = 0 \end{cases} \quad (2\text{-}11)$$

Where $R_a = R_b = R_c = R$, $L_a = L_b = L_c = L - M$, $e_a = e_b = e_c = e$. V_S is DC power supply voltage. For approximate solution, assume the circuit has reached the steady state before commutation, we have the equation as conventional DC motor,

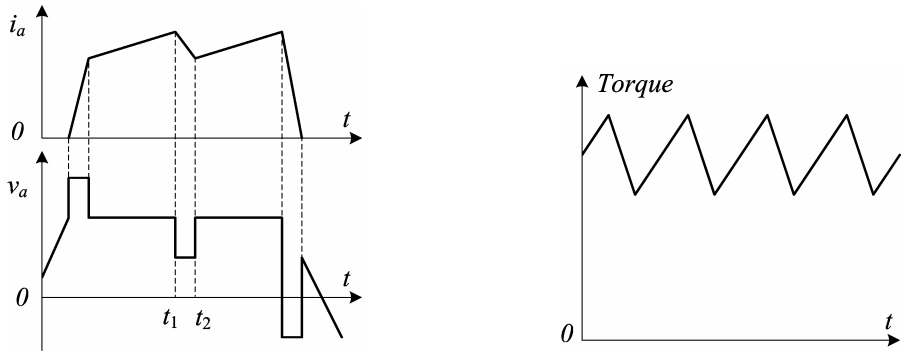
$$V_S = 2IR + 2e \quad (2\text{-}12)$$

With the initial value $i_{a0+} = I, \quad i_{b0+} = I$ (I is the current of DC link) and Equation (2-12) solve the Equation (2-11) obtain

$$\begin{cases} i_a = \left(\frac{4}{3}I - \frac{V_S}{3R}\right) + \left(\frac{V_S}{3R} - \frac{1}{3}I\right)e^{-\frac{R}{L-M}t} \\ i_b = \left(\frac{2}{3}I - \frac{2V_S}{3R}\right) + \left(\frac{2V_S}{3R} + \frac{1}{3}I\right)e^{-\frac{R}{L-M}t} \end{cases} \tag{2-13}$$

The phase voltage during commutation can be obtained from Equation (2-12)

$$\begin{cases} v_a = v_b = v_{PO} = \frac{V_S}{6} + \frac{1}{3}IR \\ v_c = v_{ON} = \frac{5V_S}{6} - \frac{1}{3}IR \end{cases} \tag{2-14}$$



(a) Phase A current and voltage (b) Torque

Fig. 2-12. Waveforms of phase current, phase voltage and torque with conventional inverter

Thus we can sketch the waveform of current and voltage of phase A as Fig. 2-12(a) and waveform of torque as Fig. 2-12(b). From the figure we can see that the current ripple of phase A is the cause by commutation, the phase voltage is decreased between t_1 and t_2. Maintaining the uncommutation phase voltage to be constant, the current ripple can be eliminated, and the torque ripple can be reduced. For this purpose, half wave inverter can be used, such as conventional half-wave inverter, Miller inverter, Buck-fronted inverter and C-dump inverter [49]. But the efficiency of the motor is low with these inverters for there is only one winding conducting at the same time. So the 12-switches inverter is introduced.

2.3.2 Commutation process with 12-switches inverter

The topology of the inverter is shown in Fig. 2-13. It consists of 3 single-phase inverters and the three armatures of the motor connect to them respectively. Thus phase current can be controlled independently and not affected by other phase commutation procedure.

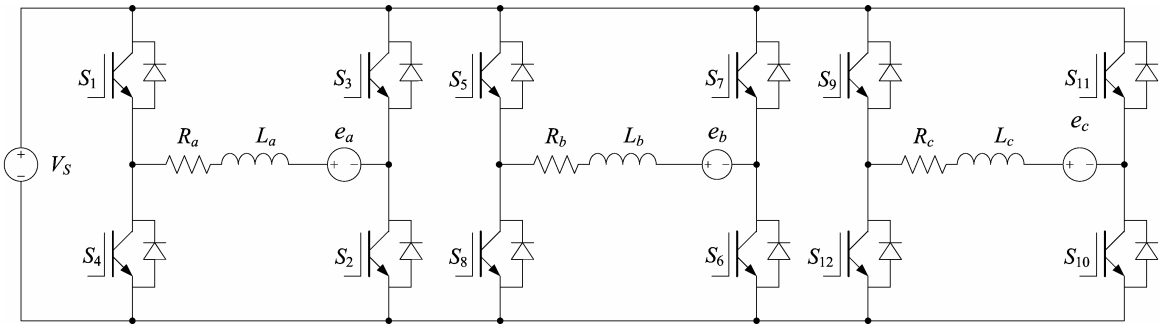


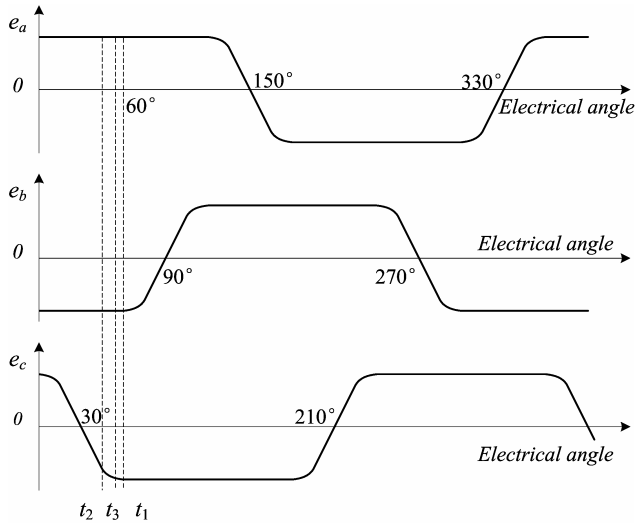
Fig. 2-13. The topology of 12-switches inverter

Also assume phase current commutates from +A-B => +A-C (turn off S_7, S_8; turn on S_{11}, S_{12}). With the 12-switches inverter, two independently governed voltage and current equations of the phase B, C can be obtained (current of phase A is not affected by commutation)

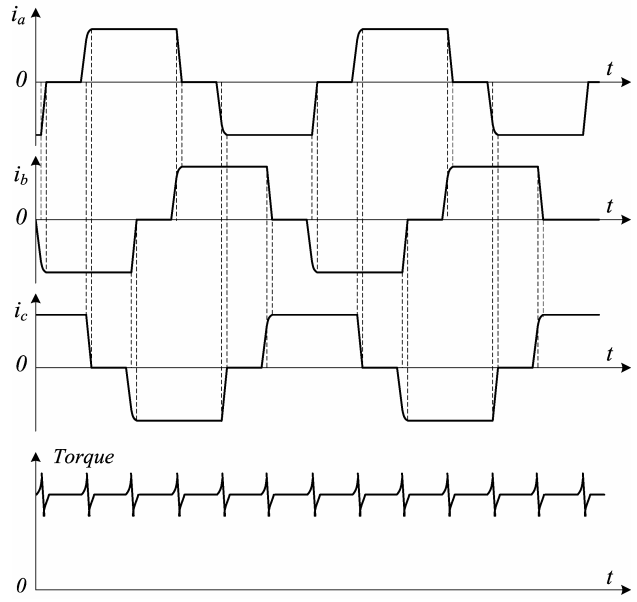
$$\begin{cases} V_S = R_b i_b + L_b \dfrac{di_b}{dt} + e_b \\ -V_S = R_c i_c + L_c \dfrac{di_c}{dt} + e_c \end{cases} \tag{2-15}$$

For trapezoidal back EMF BDCM, the waveform of the back EMF is shown in Fig. 2-14(a). If the commutation occurs at time t_1, with the initial condition $i_{b0+} = -I$, $i_{c0+} = 0$ and $e_b \approx e_c = -(V_S - IR)$ solve the equation, obtain

$$\begin{cases} i_b = \dfrac{2V_S}{R} - I + \dfrac{2V_S}{R} e^{-\frac{R}{L-M}t} \\ i_c = I(1 - e^{-\frac{R}{L-M}t}) \end{cases} \tag{2-16}$$



(a) Back EMF of trapezoidal BDCM



(b) Phase current and torque

Fig. 2-14. Waveforms of back EMF, phase current and torque with 12-switches inverter

i_b can reduce to zero very quickly, but the i_c increases very slowly. In order to shorten the commutation process, S_{11}, S_{12} are turned on at t_2, S_7, S_8 are turned off at t_3, then i_c can increases more quickly. As the back EMF Vs time (or electrical degree) is a continuous function, there exists an instant t_2 that i_c can reach the steady value at t_1. So the phase current is smoother, and the torque of the motor is reduced [as shown in Fig. 2-14(b)].

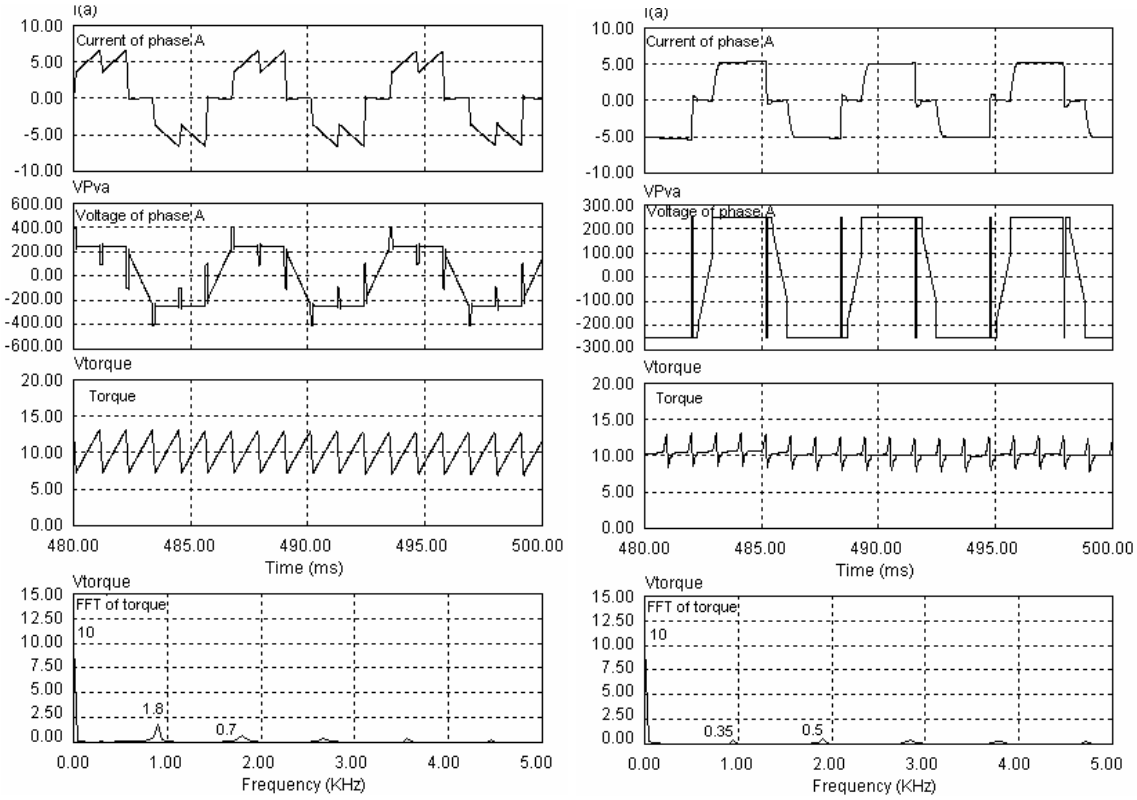
The 12-switches inverter not only reduces the torque ripple significantly, includes the merit of the conventional three phase full wave inverter and half wave inverter, but also has other merit as follows:

- For a given supply voltage, the current flows through one winding only other than two windings in conventional inverter, so it can offer twice phase current and torque. The supply only needs to get over back EMF of one phase, so the speed of the motor also doubled.
- For a given motor speed, it only requires half supply voltage, so the voltage stress of switching device is reduced half. It is easier to select required device and the price of two low voltage stress devices is lower than that of one high voltage stress device. The insulation class requirement can be also reduced.
- The inverter is applicable to other motors such as induction motor, synchronous motor, and no deadbeat time is required.
- The phase current can be controlled more flexible.

2.3.3 Simulation and experimental results

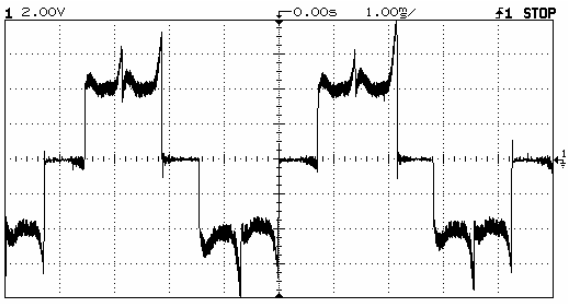
The simulation results of phase current, phase voltage, torque and FFT of torque in conventional three-phase full wave inverter and 12-switches inverter are shown in Fig. 2-15. The waveforms in Fig. 2-15(a) are with conventional three-phase full wave inverter, and supply voltage is 500V; waveforms in figure 2-15(b) are with 12-switches inverter, and supply voltage is 250V. From the simulation result we can see that average torque in the two inverter is almost the same, the first order of torque harmonics is much less in 12-switches inverter than that of in conventional inverter, so the torque ripple with 12-switches reduces significantly, the magnitude of phase current and torque with the two inverters is the same, the speed is also same, but the supply voltage of former is twice as that of later.

In order to verify the theoretical analysis and simulation results, two inverters are built up to compare the performance of the 12-switches inverter and conventional three-phase inverter. A customized 2.2kW BDCM with all stator windings terminal connected externally is introduced in this experiment. The shaft of the motor is clutched to variable load with torque probe. The phase current and torque waveforms in the two inverters are shown in Fig. 2-16. From the figure we can see that the phase current in 12-switches inverter is not affected by the commutation of other phase and the torque has less ripple than that of three-phase inverter.

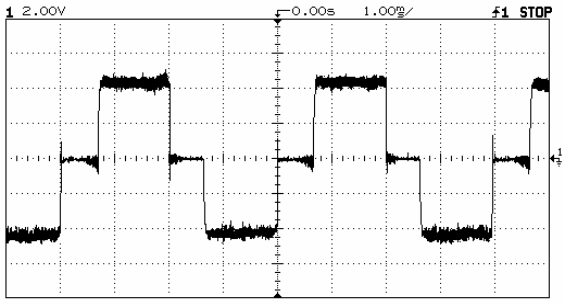


(a) (b)

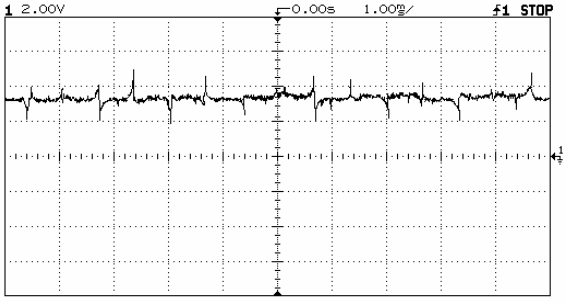
Fig. 2-15. Simulation result of conventional inverter versus that of 12-switches inverter, (a) Waveforms in conventional three-phase full wave inverter (b) Waveforms in 12-swtiches inverter



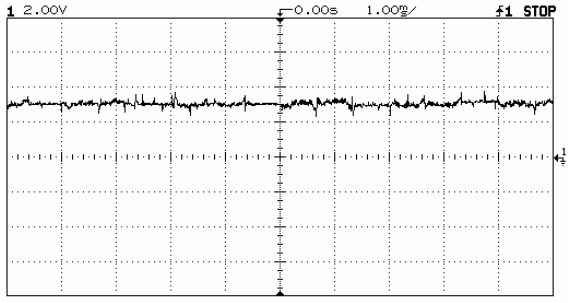
(a) Phase current in conventional inverter (5A/div)



(b) Phase current in 12-switches inverter (5A/div)



(c) Torque in conventional inverter (5N.m/div)



(d) Torque in 12-switches inverter (5N.m/div)

Fig. 2-16. Experimental result of conventional inverter versus12-switches inverter

2.4 Summary

The operation principle of the brushless DC motor is introduced first. Then the controller for BDCM drive system is described. Commutation logic table is proposed, speed sensor is introduced and two methods to get speed signal from Hall sensor are illustrated, gate driver circuit for IGBT is introduced and bootstrap supply is applicable to gate driver circuit to save the number of insulated DC power supply.

A novel 12-switches inverter for BDCM is proposed to reduce the torque ripple of BDCM. With the inverter, for a given voltage of supply, torque and speed of the motor are doubled. For a given speed of the motor, the voltage stress of switching device is reduced half, the insulation class requirement can be also reduced. The inverter is also applicable to induction motor.

Chapter 3 Resonant DC Link Inverter

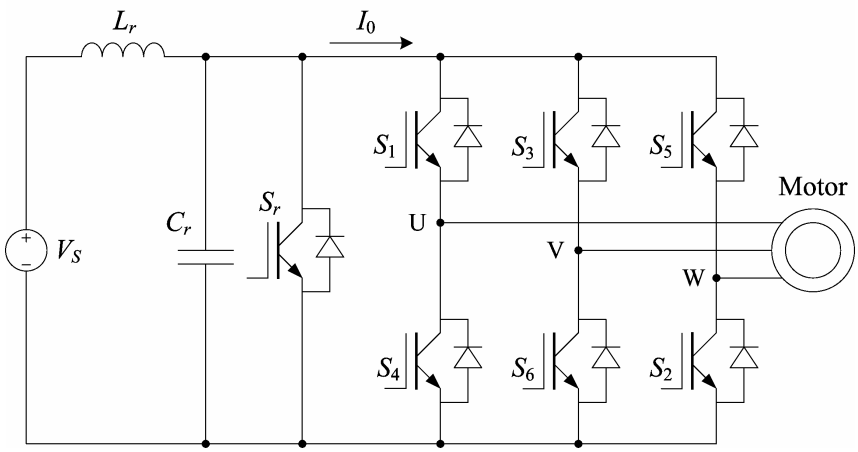
The structure of the resonant DC link inverter has been introduced in Chapter 1. An LC resonant circuit was added between DC power supply and 6-switches inverter. All power semiconductor switches' snubber circuit can be eliminated. Resonance occurs periodically or at controlled instant to make DC link voltage reach zero temporarily during which the power semiconductor switches at the output section could be switched on or off with ZVS condition. In this chapter, details will be proposed. Literature review will be given first, then a novel topology will be proposed, the operation principle and control scheme of the novel inverter are analyzed. Simulation and experimental results are proposed to verify the theoretical analysis.

3.1 Literature Review

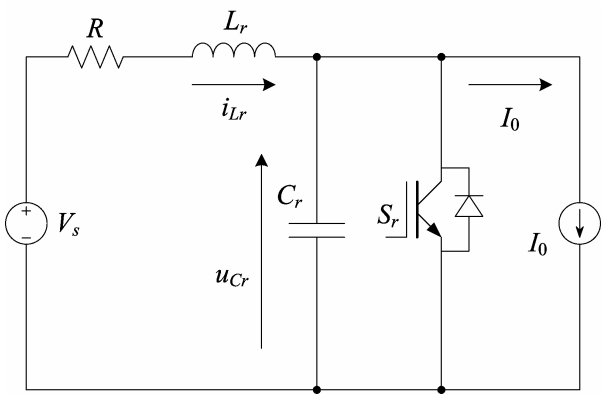
3.1.1 Prototype of resonant DC link inverter

D. M. Divan is the first scholar to introduce resonant DC link inverter (RDCLI) [17, 51]. The topology of the inverter and its equivalent circuit is shown in Fig. 3-1. The full bridge three-phase inverter and load can be modelled by a current source, based on the assumption that the load has a high inductance and that the load current varies slowly with respect to the DC link frequency. Analysis of the circuit operation can begin by assuming that switch S_r remains open and the DC link components are ideally lossless. Under these conditions, if the supply voltage is suddenly applied to the resonant tank, the voltage across the resonant capacitor C_r will oscillate sinusoidally between zero and twice the DC supply voltage. The DC link voltage would then exhibit periodically zero voltage opportunities during which the power semiconductor switches at the output section could be switched on or off with low switching losses. However, if the resonant tank is not lossless, the DC link voltage will never return to zero. The switch S_r is then included in the circuit to ensure that the resonant DC link voltage will always return to zero in order to produce a sustained DC link pulsation. Furthermore, switch S_r also ensures that the DC

link voltage will remain at zero for a finite time interval, in order to provide enough time for commutation of the main output switches.



(a) Resonant DC link inverter



(b) Equivalent circuit

Fig. 3-1. Topology of resonant DC link inverter and its equivalent circuit

If S_r is kept closed while the supply voltage is applied, the current in the resonant inductor L_r will build up linearly. S_r should then be held closed until the magnetic energy stored in L_r is enough to compensate for the losses in the resonant tank, define the corresponding current as I_{Lr0}. During the resonant, the circuit is governed by the equation

$$\begin{cases} L_r \dfrac{di_{Lr}}{dt} + i_{Lr} R + u_{Cr} = V_S \\ C_r \dfrac{du_{Cr}}{dt} = i_{Lr} + I_0 \end{cases} \tag{3-1}$$

With initial condition $i_{Lr}(0) = I_{Lr0}$, $u_{Cr}(0) = 0$, solve the equation, get

$$\begin{cases} u_{Cr} = (V_S - I_0 R) + e^{-\frac{t}{\tau}}(I_0 R - V_S)\cos\omega t + \\ \qquad e^{-\frac{t}{\tau}}\left[\frac{1}{\omega\tau}(V_S - \frac{R}{2}(I_{Lr0} + I_0)) + \omega L_r (I_{Lr0} - I_0)\right]\sin\omega t \\ i_{Lr} = I_0 + e^{-\frac{t}{\tau}}(I_{Lr0} - I_0)\cos\omega t - e^{-\frac{t}{\tau}}\left[\frac{2V_S - R(I_{Lr0} + I_0)}{\omega L_r}\right]\sin\omega t \end{cases} \quad (3\text{-}2)$$

Where $\tau = \frac{2L_r}{R}$, $\omega_r = \frac{1}{\sqrt{L_r C_r}}$, $\omega = \sqrt{\omega_r^2 - \frac{1}{\tau^2}}$. When neglecting inductor resistance R=0, Equation (3-2) can be simplified into

$$\begin{cases} u_{Cr} = V_S(1 - \cos\omega_r t) + \omega_r L_r (I_{Lr0} - I_0)\sin\omega_r t \\ i_{Lr} = I_0 + \frac{V_S}{\omega_r L_r}\sin\omega_r t + (I_{Lr0} - I_0)\cos\omega_r t \end{cases} \quad (3\text{-}3)$$

When $I_{Lr0} = I_0$, Equation (3-3) can be simplified into

$$\begin{cases} u_{Cr} = V_S(1 - \cos\omega_r t) \\ i_{Lr} = I_0 + \frac{V_S}{\omega_r L_r}\sin\omega_r t \end{cases} \quad (3\text{-}4)$$

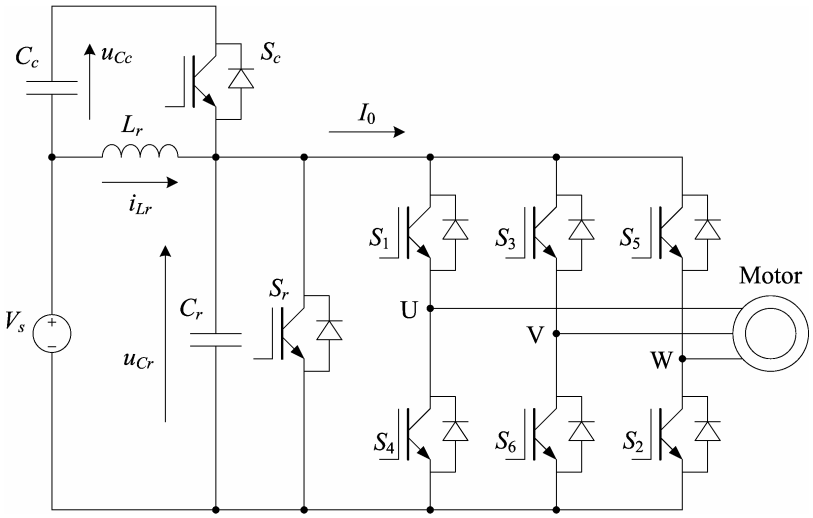
From Equation (3-4) we can see that if the DC link components are ideally lossless, and the charged resonant inductor current $i_{Lr}(0)$ is greater than I_{Lr0}, u_{Cr} will oscillate sinusoidally between zero and twice the DC supply voltage. The average value of resonant inductor current is I_{Lr0}. But actually it is impossible that the DC link components are lossless, $i_{Lr}(0)$ must greater than I_{Lr0}, then peak u_{Cr} will greater than twice the DC power supply voltage.

If the output section of the resonant DC link inverter is composed by half-bridge inverter legs, the function of switch S_r can be executed by the output switches themselves. In this case, S_r can be eliminated from the circuit. The inverter circuit will be therefore very simple, having only two additional passive elements in comparison to a hard switched inverter. No additional power semiconductor switch is required. However, due to the pulsed DC link voltage, only discrete pulse modulation techniques can be used for output control. Furthermore, the higher voltage stress on the power semiconductor switches at

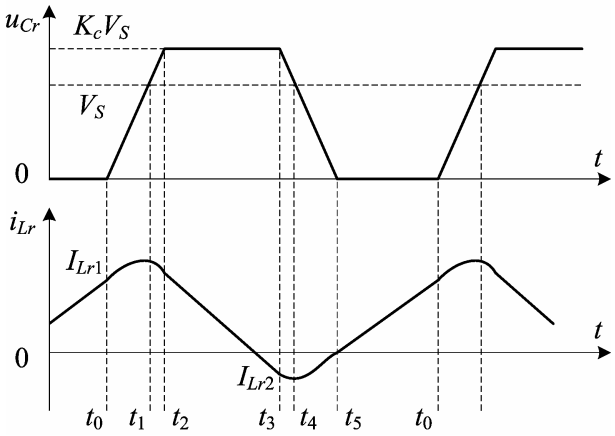
the output section, in excess of double of the supply voltage, represents a major drawback of this topology.

3.1.2 Improved resonant DC link inverter

Several alternative topologies which limit the peak voltage stress have been proposed to solve this problem. So far, one of successful topologies is the Actively Clamped Resonant DC Link Inverter (ACRDCLI) [19, 20, 23, 32, 33, 80].



(a) The topology of ACRDCLI



(b) Key waveforms of the inverter

Fig. 3-2. The topology of ACRDCLI and key waveforms

The topology of the ACRDCLI and key waveforms are shown in Fig. 3-2. It is obtained by augmenting the RDCLI with a clamping loop around the resonant inductor L_r. This

clamping loop is composed of the clamping capacitor C_c and the clamp switch S_c, with its associated anti-parallel connected diode.

Circuit operation of the ACRDCLI is very similar to that of the RDCLI mentioned in 2.1. The clamping capacitor C_c is charged to a preset voltage $(k_c\text{-}1)V_s$ where k_cV_s is the clamping voltage.

(i) Firstly switch S_r is turned on, the current through L_r (i_{Lr}) rises linearly. When the current reaches a preset current level I_{Lr1} (enough energy is stored in L_r to ensure that a full resonant cycle will be completed), switch S_r is turned off and resonant begins.

(ii) i_{Lr} is pumped into the resonant capacitor C_r, and the voltage across C_r (u_{Cr}) starts to rise towards its natural peak. When u_{Cr} reaches clamping voltage, the clamp diode across S_c begins to conduct, diverting the current from the resonant capacitor into the clamp capacitor.

(iii) While the clamp diode is conducting, switch S_c can be turned on, under zero voltage conditions and with low switching losses. S_c is kept on until the current in the C_c (equal to i_{Lr}) reverses and reaches a preset current level I_{Lr2}, at which S_c is turned off.

(iv) Immediately after turn-off of S_c, the inverted current which was flowing in the clamping circuit will be transferred back to C_r, causing the DC link voltage to oscillate toward zero. When u_{Cr} reaches zero, the anti-parallel diode of S_r will conduct and then a new cycle can be initiated.

The turn-off current reference I_{Lr2} is supplied by a control loop which regulates the voltage across the clamping capacitor. If C_c is large enough, the voltage across it will exhibit only a small change during one clamping cycle. However, the control loop must ensure that the excess charge injected into C_c at the beginning of each clamping cycle is returned to the main circuit in finite time, with the objective of maintaining the long-term charge balance in C_c, thus keeping the clamp voltage stable.

The clamping factor k_c should be chosen according to the supply voltage and to the voltage rating of the power semiconductor switches employed. For example, with industry-standard power modules rated at 1200V and with a rectified AC voltage equal to 600V, a clamping factor of approximately 1.5 would be a good choice, yielding a maximum voltage stress of 900V. The clamp switch S_c, as well as the shunt switch S_r, are turned off with low switching losses, under zero voltage conditions. This is achieved by the presence of the resonant capacitor C_r across the DC link, which slows down the voltage rise at the terminals of both switches when they cut off the current. The intervals where the DC link voltage is zero are used for lossless commutation of the output main switches.

It can be known from the analysis of literature [20] that when the k_c is smaller than 2, the frequency of the resonant circuit will be reduced with the reduction of k_c. When k_c = 1, the frequency is equal zero which means that the clamping circuit is no use any more. So the device voltage stress is still high. On the other hand, it is required to keep the voltage of clamping capacitor stable and there is need to measure the current of resonant inductor which is difficult to implement. Moreover the output of the inverter contains subharmonic components which are difficult to be filtered out, and in some cases, cannot be accepted.

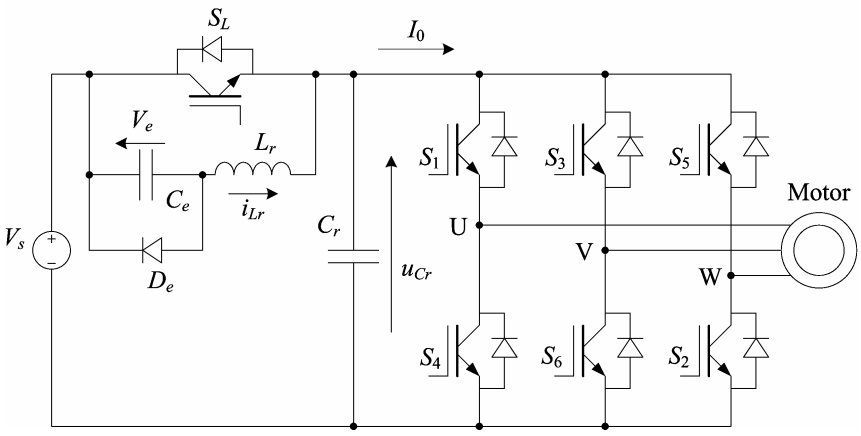


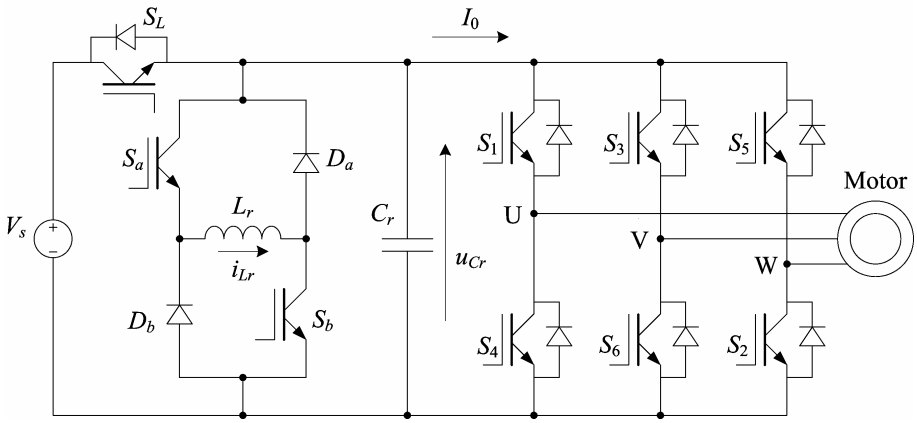
Fig. 3-3. The topology of SVCRDCLI

Source Voltage Clamped Resonant DC Link Inverter (SVCRDCLI) is another improved RDCLI that can limit the peak voltage stress [32, 33]. The construction of the inverter is shown in Fig. 3-3. The circuit only uses one auxiliary switch to clamp the DC link voltage to the same level as that of DC power supply. The zero voltage of DC link can be kept for

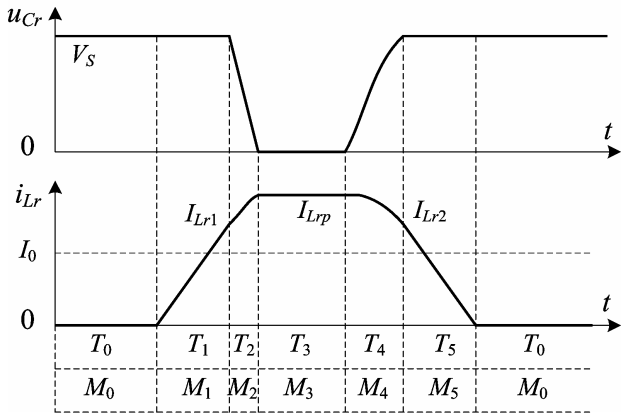
a short interval to guarantee the main switches of inverter switch under ZVS condition. However the circuit needs to preset four current levels to control the resonant circuit. The auxiliary switches should be turned on/off at the instant when the inductor current equal to the preset value which is hard to implement. The control scheme is very complex.

3.1.3 Quasi resonant DC link inverter

All above inverters have the disadvantage of considerable inductor power losses as there is always current flow through resonant inductor. In order to solve this problem, quasi resonant DC link inverter (QRDCLI) [14, 27, 36, 43, 52, 54, 87, 92, 102] is introduced. The resonant inductor can be removed from the main conduction path and paralleled with inverter section. The resonant only occurs at the interval when the main switches of inverter need to switch. No current flows through resonant inductor in regular time.



(a) The topology of QPRDCLI I



(b) Key waveforms of the inverter

Fig. 3-4. The topology of QPRDCLI I and its key waveforms

One quasi parallel resonant DC link inverter (QPRDCLI) [14, 87] is introduced by Jung G. Cho. The topology of the inverter is depicted in Fig. 3-4(a). It consists of three auxiliary switches, two power diodes and LC resonant components. The resonant inductor is connected at the center of H-bridge instead of main conduction path and forms a parallel resonant circuit with resonant capacitor. The operation of the inverter can be divided into six operational modes and the related waveforms are shown in Fig. 3-4(b).

- Mode 0 (S_L: on, S_a, S_b: off) The switch S_L conducts load current and the voltage of DC link is the same as that of DC power supply. It operates the same as conventional hard switching inverter.

- Mode 1 (S_L: on, S_a, S_b: on) When the switching is needed, the switches S_a and S_b are turned on with zero current conditions and the inductor current i_{Lr} is increased linearly to a preset reference value I_{Lr1}, while the capacitor voltage u_{Cr} is kept with DC power supply voltage V_S.

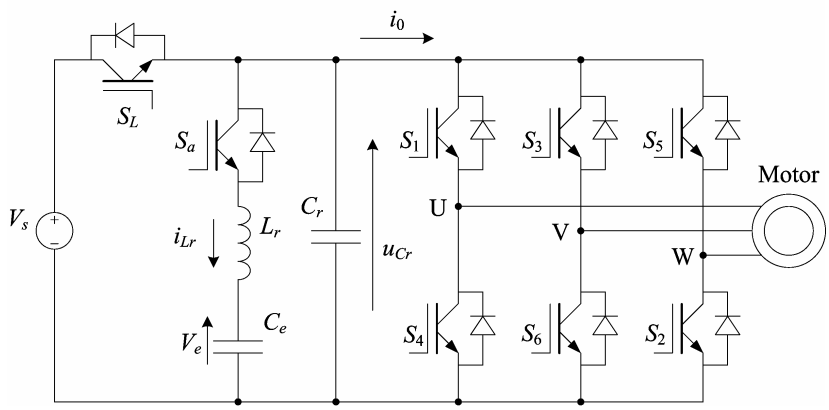
- Mode 2 (S_L: off, S_a, S_b: on) The switch S_L is turned off with zero voltage condition and resonance starts between L_r and C_r. The capacitor voltage u_{Cr} is decreased sinusoidally to zero.

- Mode 3 (S_L: off, S_a, S_b: on) The resonant capacitor voltage u_{Cr} is kept zero while the inductor current freewheels through paths of S_a - D_a and S_b - D_b. This zero DC link voltage period provides ZVS condition to the main switches of the inverter.

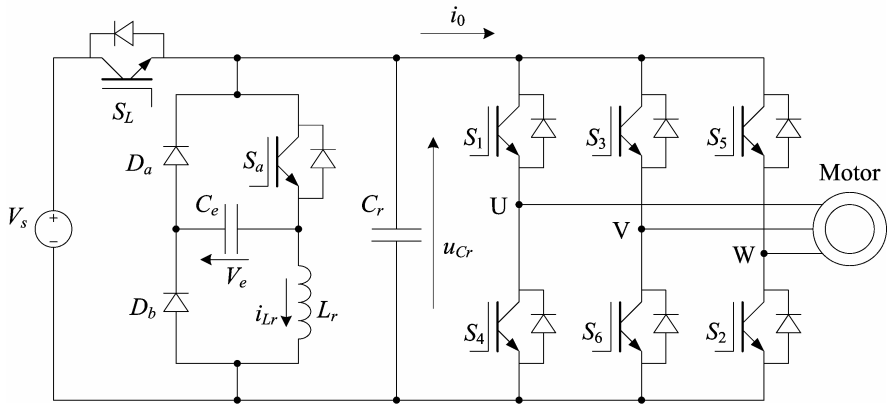
- Mode 4 (S_L: off, S_a, S_b: off) When the switching of inverter devices is completed, the switches S_a and S_b are turned off with ZVS condition. Then the path of inductor current is shifted to D_a, D_b and C_r, thus u_{Cr} is increased sinusoidally until u_{Cr} becomes V_S.

- Mode 5 (S_L: on, S_a, S_b: off) When u_{Cr} is increased slightly over V_S, the antiparallel diode connected in S_L is turned on with zero voltage condition. Then the DC link voltage u_{Cr} is clamped by supply voltage and the remaining energy in the resonant inductor is returned to supply. i_{Lr} is linearly decreased from I_{Lr2} to zero and the diodes D_a and D_b are turned off with ZCS condition.

From the analysis we can see that the advantages of the inverter are obvious: all the main switches, auxiliary switches and power diodes work under ZVS or ZCS condition, inductor power loss reduces significantly. The demerit of the topology is that: measuring inductor current is still necessary and too many auxiliary devices (three switches and two diodes) are required.



(a) The topology of QPRDCLI II



(b) The topology of QPRDCLI III

Fig. 3-5. The topology of QPRDCLI II and III

Another two QPRDCLIs [43, 54, 92] are shown in Fig. 3-5. The operation principle of these inverters is similar to the inverter I. They reduce the number of power device and possess the merit of as inverter I. But the inverters do not overcome the demerit of the needs of measuring inductor current. The resonant period of inverter III is a little long that would cause the failure of ZVS.

Applying zero voltage transition of DC/DC converter to DC/AC inverters, DC-rail parallel resonant zero voltage transition (ZVT) voltage source inverters [11, 29, 37, 50, 62]

are proposed, they are either having not all switches and diodes work under soft-switching condition or they require a stiff DC link capacitor bank that is center taped to accomplish commutation. The center voltage of DC link is susceptible to drift that may affect the operation of the resonant circuit. In addition they require two ZVT every PWM cycle, which would worsen the output voltage and limit the switch frequency of the inverter.

3.2 Transformer Based Resonant DC Link Inverter

3.2.1 The structure of the transformer based resonant DC link inverter

The majority of soft-switching inverters proposed in the recent years have been aimed at the induction motor drive applications. So it is necessary to research on the novel topology of soft-switching inverter and special control circuit for BDCM drive systems. This section proposes a resonant DC link inverter based on transformer for BDCM drive system to solve the problems mentioned above. The inverter possesses the advantage of low switching power loss, low inductor power loss, low DC link voltage ripple, small device voltage stress and simple control scheme.

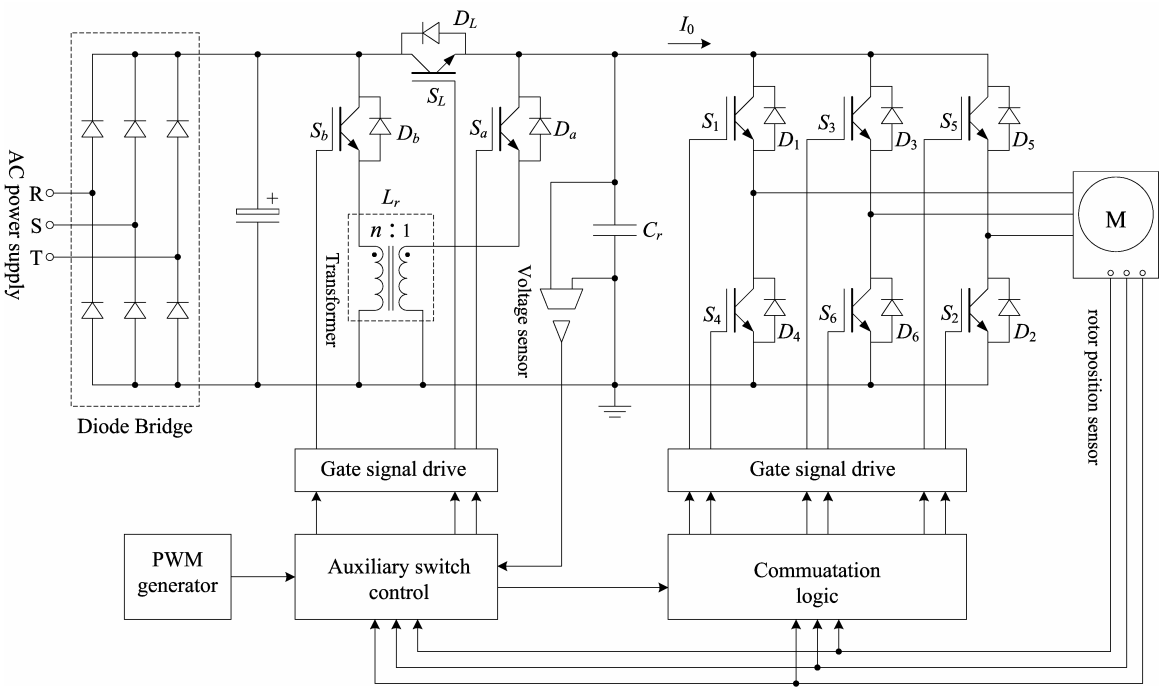


Fig. 3-6. The structure of the resonant DC link inverter for BDCM drive system

The structure of the transformer based resonant DC link inverter is shown in Fig. 3-6. The system contains an uncontrolled rectifier, a resonant circuit, a conventional three-phase inverter and control circuit. The resonant circuit consists of three auxiliary switches (S_L, S_a, S_b) and corresponding built in freewheeling diode (D_L, D_a, D_b), one transformer with turn ratio 1: n and one resonant capacitor. All auxiliary switches work under ZVS or zero current switching (ZCS) condition. It generates voltage notches of the DC link to guarantee the main switches (S_1-S_6) of the inverter operating in ZVS condition.

3.2.2 Resonant circuit

The resonant circuit consists of three auxiliary switches, one transformer and one resonant capacitor. The auxiliary switches are controlled at certain instant to obtain the resonance between transformer and capacitor. Thus, the DC link voltage reaches zero temporarily (voltage notch) and the main switches of the inverter get ZVS condition for commutation. Since the resonant process is very short, the load current can be assumed constant. The equivalent circuit of the inverter is shown in Fig. 3-7. Where V_S is the DC power supply voltage, I_0 is the load current. The corresponding waveforms of the auxiliary switches gate signal, PWM signal, resonant capacitor voltage (u_{Cr}) (i.e. DC link voltage), the transformer primary winding current (i_{Lr}) and current of switch S_L (i_{SL}) are illustrated in Fig. 3-8. The DC link voltage is reduced to zero and then rises to supply voltage again is called one zero voltage transition (ZVT) process or one DC link voltage notch. The operation of the ZVT process in one PWM cycle can be divided into 8 modes.

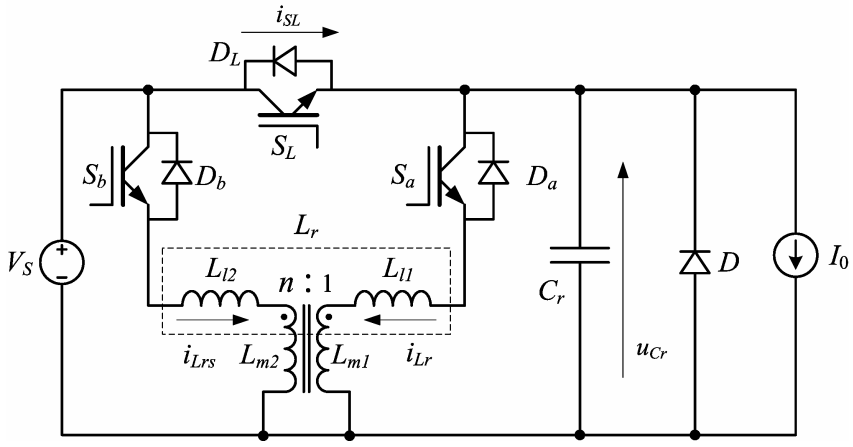


Fig. 3-7. The equivalent circuit of the inverter

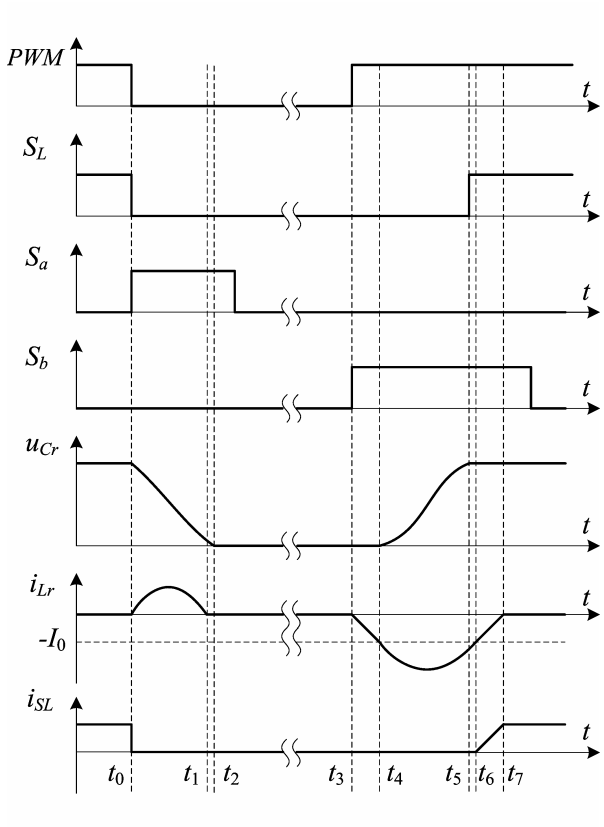


Fig. 3-8. Key waveforms of the equivalent circuit

Mode 0 (shown in Fig. 3-9) $0 < t < t_0$. Its operation is the same as conventional inverter. Current flows from DC power supply through S_L to the load. The voltage across resonant capacitor C_r (u_{Cr}) is equal to the supply voltage (V_S). The auxiliary switches S_a and S_b are turned off.

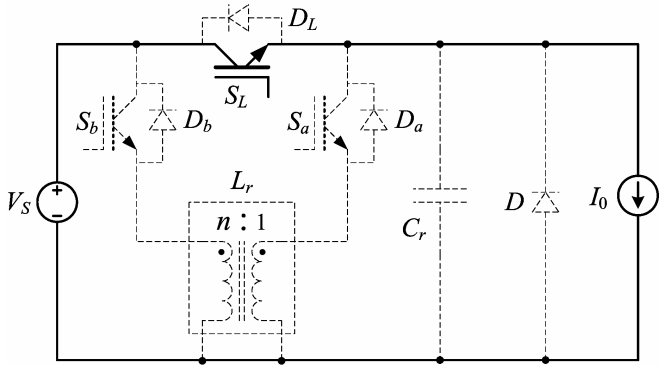


Fig. 3-9. Equivalent circuit of mode 0

Mode 1 (shown in Fig. 3-10) $t_0 < t < t_1$. When it is the instant for phase current commutation or PWM signal is flopped from high to low, auxiliary switch S_a is turned on with ZCS (as the i_{Lr} can not change suddenly due to the transformer inductance) and

switch S_L is turned off with ZVS (as the u_{Cr} can not change suddenly due to resonant capacitor C_r) at the same time. The transformer primary winding current i_{Lr} begins to increase and the secondary winding current i_{Lrs} also begins to build up through diode D_b to DC link at $t = t_0$. The terminal voltages of primary and secondary windings of the transformer are DC link voltage u_{Cr} and supply voltage V_S respectively. Capacitor C_r resonates with transformer, the DC link voltage u_{Cr} is decreased. Neglecting the resistances of windings, using the transformer equivalent circuit (referred to the primary side) [66], the transformer current i_{Lr}, i_{Lrs} and DC link voltage u_{Cr} obey the equation:

$$\begin{cases} u_{Cr}(t) = L_{l1}\dfrac{di_{Lr}(t)}{dt} + a^2 L_{l2}\dfrac{d[i_{Lrs}(t)/a]}{dt} + aV_S \\ i_{Lr}(t) + I_0 + C_r\dfrac{du_{Cr}(t)}{dt} = 0 \end{cases} \tag{3-5}$$

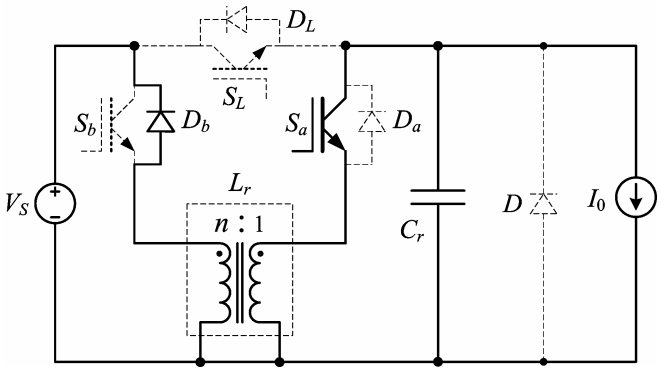


Fig. 3-10. Equivalent circuit of mode 1

Where L_{l1} and L_{l2} are the primary and secondary winding leakage inductance respectively, a is the transformer turn ratio 1: n. The transformer has a high magnetizing inductance. We can assume that $i_{Lrs} = i_{Lr}/n$, with initial condition $u_{cr}(0) = V_S$, $i_{Lr}(0) = 0$, solve the Equation (3-5), get (Deduction proposed in Appendix D)

$$\begin{cases} u_{Cr}(t) = \dfrac{(n-1)V_S}{n}\cos(\omega_r t) - I_0\sqrt{\dfrac{L_r}{C_r}}\sin(\omega_r t) + \dfrac{V_S}{n} \\ i_{Lr}(t) = I_0\cos(\omega_r t) - I_0 + \dfrac{(n-1)V_S}{n}\sqrt{\dfrac{C_r}{L_r}}\sin(\omega_r t) \end{cases} \tag{3-6}$$

Where $L_r = L_{l1} + L_{l2}/n^2$ is the equivalent inductance of the transformer, $\omega_r = \sqrt{1/L_r C_r}$ is the natural angular resonance frequency. Rewrite the Equation (3-6) get

$$\begin{cases} u_{Cr}(t) = K\cos(\omega_r t + \alpha) + \dfrac{V_S}{n} \\ i_{Lr}(t) = K\sqrt{\dfrac{C_r}{L_r}}\sin(\omega_r t + \alpha) - I_0 \end{cases} \tag{3-7}$$

Where $K = \sqrt{\dfrac{(n-1)^2 V_S^2}{n^2} + \dfrac{I_0^2 L_r}{C_r}}$, $\alpha = \arctan\left(\dfrac{nI_0}{(n-1)V_S}\sqrt{\dfrac{L_r}{C_r}}\right)$. n is a number which is slightly less than 2 (the selection of such a number will be explained late), i_{Lr} will decay to zero faster than u_{Cr}. Let $i_{Lr}(t) = 0$, the duration of the resonance can be determined:

$$\Delta t_1 = t_1 - t_0 = \frac{\pi - \alpha}{\omega_r} \tag{3-8}$$

When i_{Lr} is reduced to zero, auxiliary switch S_a can be turned off with ZCS condition. At $t = t_1$, the corresponding DC link voltage u_{Cr} is

$$u_{Cr}(t_1) = \frac{2-n}{n}V_S \tag{3-9}$$

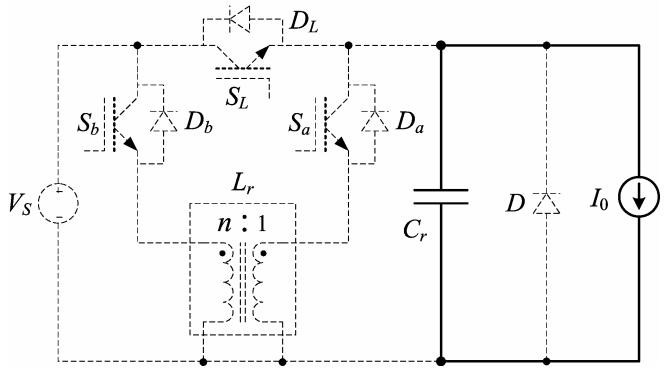


Fig. 3-11. Equivalent circuit of mode 2

Mode 2 (shown in Fig. 3-11) $t_1 < t < t_2$. When the transformer current is reduced to zero, the resonant capacitor is discharged through load from initial condition as Equation (3-9). The interval of this mode can be determined by:

$$\Delta t_2 = t_2 - t_1 = \frac{C_r V_S (2-n)}{nI_0} \tag{3-10}$$

As it has been mentioned that n is a number which is slightly less than 2, the interval is normally very short.

Mode 3 (shown in Fig. 3-12) $t_2 < t < t_3$. The DC link voltage (u_{Cr}) is zero. The main switches of the inverter can now be either turned on or turned off under ZVS condition during this mode. Load current flows through the freewheeling diode D.

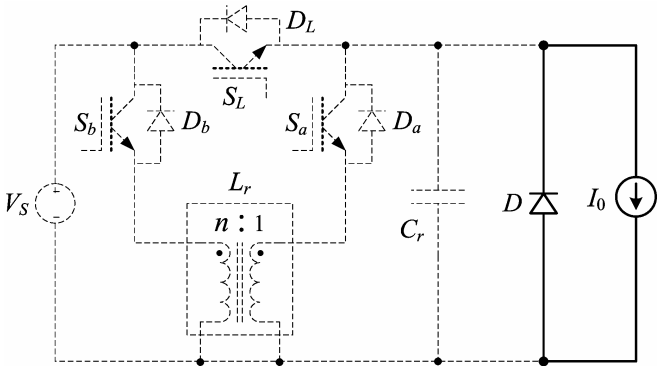


Fig. 3-12. Equivalent circuit of mode 3

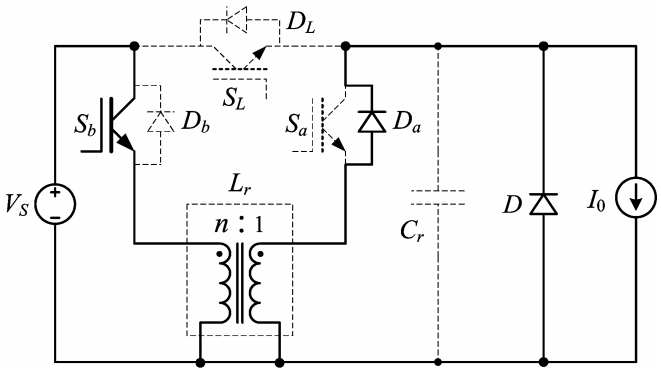


Fig. 3-13. Equivalent circuit of mode 4

Mode 4 (shown in Fig. 3-13) $t_3 < t < t_4$. As the main switches have turned on or turned off, auxiliary switch S_b is turned on with ZCS (as the i_{Lrs} can not change suddenly due to the transformer inductance) and the transformer secondary current i_{Lrs} starts to build up linearly. The transformer primary current i_{Lr} also begins to conduct through diode D_a to the load. The current in the freewheeling diode D begins to fall linearly. The load current is slowly diverted from the freewheeling diodes to the resonant circuit. DC link voltage u_{Cr} is still equal to zero before the transformer primary current is greater than load current.

The terminal voltages of transformer primary and secondary windings are zero and DC power supply voltage V_S respectively. Redefine the initial time, we obtain

$$0 = L_{l1}\frac{di_{Lr}(t)}{dt} + a^2 L_{l2}\frac{d[i_{Lrs}(t)/a]}{dt} + aV_S \tag{3-11}$$

Since the transformer current $i_{Lrs} = i_{Lr}/n$ as in mode 1, rewrite the Equation (3-11) as

$$\frac{di_{Lr}}{dt} = -\frac{V_S}{nL_r} \tag{3-12}$$

The transformer primary current i_{Lr} is reversed linearly from zero, the mode is end when $i_{Lr} = -I_0$, the interval of this mode can be determined:

$$\Delta t_4 = t_4 - t_3 = \frac{nL_r I_0}{V_S} \tag{3-13}$$

At t_4, i_{Lr} equals the negative load current $-I_0$ and the current through the diode D becomes zero. Thus the freewheeling diode turns off under ZCS condition, the diode reverse recovery problems are reduced.

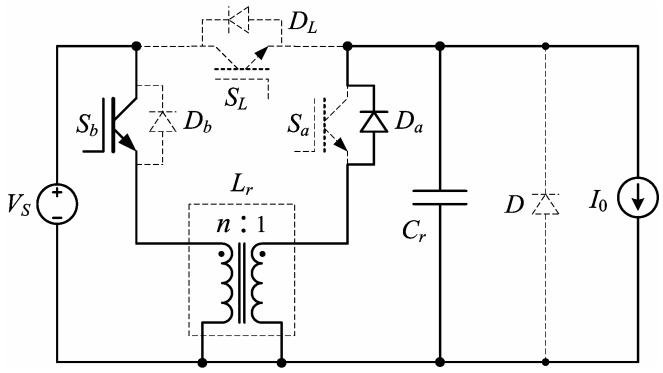


Fig. 3-14. Equivalent circuit of mode 5

Mode 5 (shown in Fig. 3-14) $t_4 < t < t_5$. Absolute value of i_{Lr} is increased continuously from I_0 and u_{Cr} is increased from zero when the freewheeling diode D is turned off. Redefine the initial time, we can get the same equation as Equation (3-5). The initial condition is $u_{Cr}(0) = 0$, $i_{Lr}(0) = -I_0$, neglecting the inductor resistance, solveing the equation, we get (Deduction proposed in Appendix D)

$$\begin{cases} u_{Cr}(t) = -\dfrac{V_S}{n}\cos(\omega_r t) + \dfrac{V_S}{n} \\ i_{Lr}(t) = -I_0 - \dfrac{V_S}{n}\sqrt{\dfrac{C_r}{L_r}}\sin(\omega_r t) \end{cases} \tag{3-14}$$

When

$$\Delta t_5 = t_5 - t_4 = \frac{1}{\omega_r}\arccos(1-n) \tag{3-15}$$

$u_{Cr} = V_S$, auxiliary switch S_L is turned on with ZVS (due to C_r). The interval is independent from load current. At $t = t_5$, the corresponding transformer primary current i_{Lr} is

$$i_{Lr}(t_5) = -I_0 - V_S\sqrt{\frac{(2-n)C_r}{nL_r}} \tag{3-16}$$

The peak value of the transformer primary current can be also determined:

$$i_{Lr-m} = \left| -I_0 - \frac{V_S}{n}\sqrt{\frac{C_r}{L_r}} \right| = I_0 + \frac{V_S}{n}\sqrt{\frac{C_r}{L_r}} \tag{3-17}$$

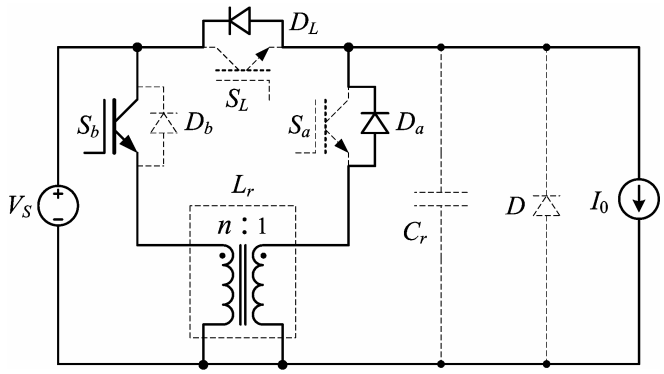


Fig. 3-15. Equivalent circuit of mode 6

Mode 6 (shown in Fig. 3-15) $t_5 < t < t_6$. Both the terminal voltages of primary and secondary windings are equal to supply voltage V_S after auxiliary switch S_L is turned on. Redefine the initial time, we obtain

$$V_S = L_{l1}\frac{di_{Lr}(t)}{dt} + a^2 L_{l2}\frac{d[i_{Lrs}(t)/a]}{dt} + aV_S \tag{3-18}$$

Since the transformer current $i_{Lrs} = i_{Lr}/n$ as in mode 1, rewrite the Equation (3-18) as:

$$\frac{di_{Lr}}{dt} = \frac{(n-1)V_S}{nL_r} \tag{3-19}$$

The transformer primary current i_{Lr} decays linearly, the mode is end when $i_{Lr} = -I_0$ again. With initial condition Equation (3-16), the interval of this mode can be determined:

$$\Delta t_6 = t_6 - t_5 = \frac{\sqrt{n(2-n)L_r C_r}}{n-1} \tag{3-20}$$

The interval is also independent from load current. As it has mentioned that n is a number which is slightly less than 2, the interval is also very short.

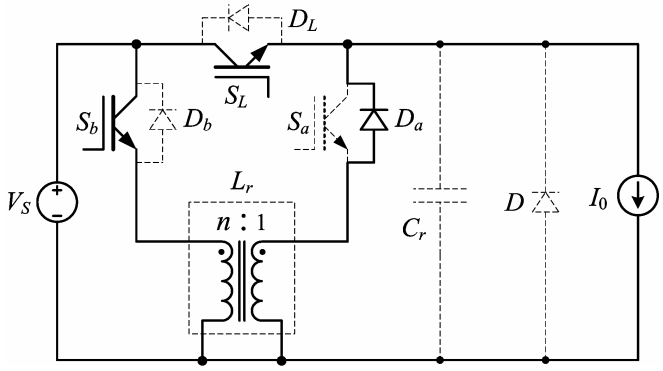


Fig. 3-16. Equivalent circuit of mode 7

Mode 7 (shown in Fig. 3-16) $t_6 < t < t_7$. The transformer primary winding current i_{Lr} decays linearly from negative load current $-I_0$ to zero. Partial load current flows through the switch S_L. The sum current flowing through switch S_L and transformer is equal to the load current I_0. Redefine the initial time, the transformer winding current obeys the Equation (3-19) with the initial condition $i_{Lr}(0) = -I_0$. The interval of this mode is:

$$\Delta t_7 = t_7 - t_6 = \frac{nL_r I_0}{(n-1)V_S} \tag{3-21}$$

Then auxiliary switch S_b can be also turned off with ZCS condition after i_{Lr} decays to zero (at any time after t_7).

3.2.3 Design consideration

It is assumed that the inductance of BDCM is much higher than transformer leakage inductance. From the analysis presented previously, the design considerations can be summarized as follows:

- Determine the value of resonant capacitor C_r, and the parameter of transformer.
- Select the main switches and auxiliary switches.
- Design the gate signal for the auxiliary switches.

The transformer turn ratio (1:n) can be determined ahead. From Equation (3-15) n must satisfy:

$$n < 2 \tag{3-22}$$

On the other hand, from Equations (3-9) and (3-10) it is expected that n is as close 2 as possible so that the duration of mode 2 would be not very long and u_{Cr} would be small enough at the end of mode 1. Normally, n can be selected at the range 1.7~ 1.9. The equivalent inductance of the transformer $L_r = L_{l1} + L_{l2}/n^2$ is inversely proportional to the rising rate of switch current when turn on the auxiliary switches. It means that the equivalent inductance L_r should be big enough to limit the rising rate of the switch current to work in ZCS condition. The selection of L_r can be referenced from the rule depicted in [19].

$$L_r \geq 4t_{on}V_S / I_{0\max} \tag{3-23}$$

Where t_{on} is the turn on time of switch S_a, I_{0max} is the maximum load current. The resonant capacitance C_r is inversely proportional to the rising rate of switch voltage drop when turn off the switch S_L. It means that the capacitance is as high as possible to limit the rising rate of the voltage to work in ZVS condition. The selection of the resonant capacitor can be determined as

$$C_r \geq 4t_{off} I_{0\max} / V_S \tag{3-24}$$

Where t_{off} is the turn off time of switch S_L. However, as the capacitance increases, more energy is stored on it, the peak value of transformer current will be also high. The peak value of i_{Lr} should be limited to twice peak load current. From Equation (3-17) we obtain

$$\sqrt{\frac{C_r}{L_r}} \le \frac{nI_{0\max}}{V_S} \tag{3-25}$$

The DC link voltage rising transition time is expressed as

$$T_w = \Delta t_4 + \Delta t_5 = \frac{nL_r I_0}{V_S} + \sqrt{L_r C_r}\arccos(1-n) \tag{3-26}$$

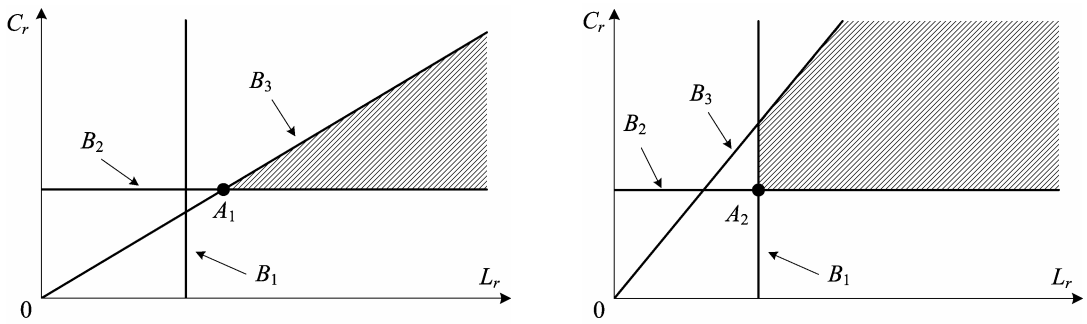
For high switching frequency, T_w should be as short as possible. Select the equivalent inductance L_r and resonant capacitance C_r to satisfy the Inequalities (3-23) - (3-25), L_r and C_r should be as small as possible. L_r and C_r selection area is illustrated in Fig. 3-17 to determine their values, the valid area is shadowed, where B_1 - B_3 is boundary which is defined according to Inequalities (3-24) - (3-26):

$$B_1: \quad L_r = 4t_{on}V_S / I_{0\max} \tag{3-27}$$

$$B_2: \quad C_r = 4t_{off}I_{0\max} / V_S \tag{3-28}$$

$$B_3: \quad \sqrt{\frac{C_r}{L_r}} = \frac{nI_{0\max}}{V_S} \tag{3-29}$$

If boundary B_3 intersects B_1 first as shown in Fig. 3-17(a), the value of L_r and C_r in the intersection of B_3 and B_2 (i.e. A_1) can be selected. Otherwise, the value of L_r and C_r in the intersection A_2 is selected as shown in Fig. 3-17(b).



(a) Case 1: B_3 intersects B_1 first (b) Case 2: B_3 intersects B_2 first

Fig. 3-17. L_r and C_r selection area

Main switches $S_{1\text{-}6}$ work under ZVS condition, the voltage stress is equal to the DC power supply voltage V_S. The device current rate can be load current. Auxiliary switch S_L works under ZVS condition, its voltage and current stress is the same as main switches. Auxiliary switches $S_{a,b}$ work under ZCS or ZVS condition, the voltage stress is also equal to the DC power supply V_S. The peak current flowing through them is limited to double maximum load current. As the auxiliary switches $S_{a,b}$ carry the peak current only during switch transitions, they can be rated lower continuous current rating.

The design of gate signal for auxiliary switches can be referenced to Fig. 3-8. The trailing edge of the gate signal for auxiliary switch S_L is the same as that of PWM, the leading edge is determined by the output of DC link voltage sensor. The gate signal for auxiliary switch S_a is a positive pulse with leading edge the same as PWM trailing edge, its width ΔT_a should be greater than Δt_1. From Equation (3-8), Δt_1 is maximum when the load current is zero. So ΔT_a can be a fixed value determined by:

$$\Delta T_a > \Delta t_1\big|_{\max} = \frac{\pi}{\omega_r} = \pi\sqrt{L_r C_r} \tag{3-30}$$

The gate signal for auxiliary switch S_b is also a pulse with leading edge the same as that of PWM, its width ΔT_b should be longer than $t_7 - t_3$ (i.e. $\Delta t_4 + \Delta t_5 + \Delta t_6 + \Delta t_7$). ΔT_b can be determined from Equation (3-13), (3-15), (3-20), (3-21) that:

$$\Delta T_b > \sum_{i=4}^{7} \Delta t_i\big|_{\max} = \frac{n^2 L_r I_{0\max}}{(n-1)V_S} + \sqrt{L_r C_r}\left[\arccos(1-n) + \frac{\sqrt{n(2-n)}}{n-1}\right] \tag{3-31}$$

3.2.5 Control scheme

When the duty of PWM is 100%, i.e. full duty cycle, the main switches of the inverter work under the commutation frequency. When it is the instant to commutate the phase current of the BDCM, we control the auxiliary switches S_a, S_b, S_L and resonant occurs between transformer L_r and capacitor C_r. The DC link voltage reach zero temporarily, thus ZVS condition of the main switches is obtained. When the duty of PWM is less than 100%, the auxiliary switch S_L works as chop. The main switches of the inverter do not

switch within a PWM cycle when the phase current needs not commutate. It has the benefit of reducing phase current drop during the PWM is off. The phase current is commutated during the DC link voltage becomes zero. There is only one DC link voltage notch per PWM cycle. It is very important especially for very low or very high duty of PWM. Otherwise the interval between two voltage notches is very short or even overlapped which will limit the tuning range.

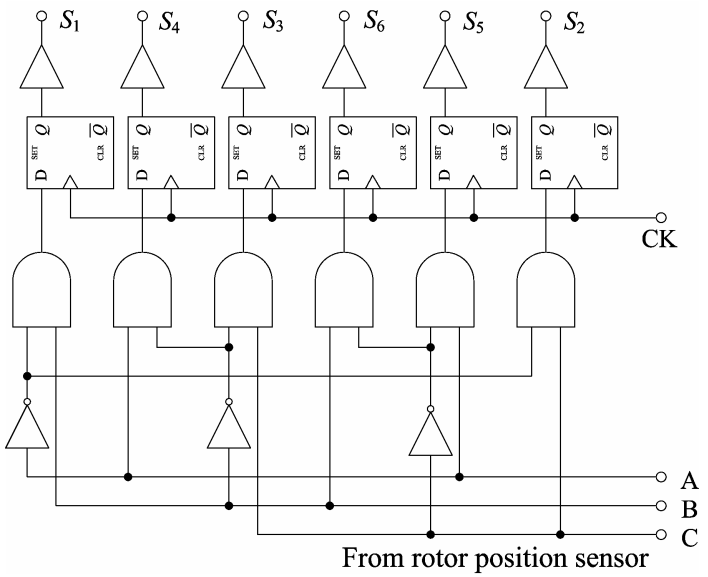


Fig. 3-18. Commutation logical circuit for main switches

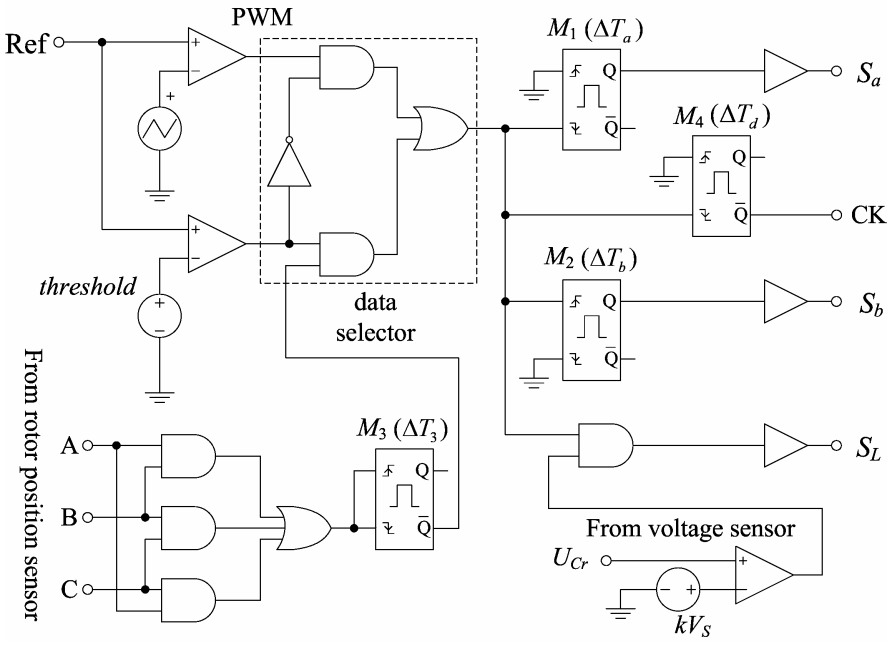


Fig. 3-19. Control circuit for the auxiliary switches

The commutation logical circuit of the system is shown in Fig. 3-18. It is similar to conventional BDCM commutation logical circuit except adding six D flip-flops to the output. Thus the gate signal of the main switches is controlled by the synchronous pulse CK that will be mentioned late and the commutation can be synchronized with auxiliary switches control circuit (shown in Fig. 3-19). The operation of the inverter can be divided into PWM operation and full duty cycle operation.

A. Full duty cycle operation

When the duty of PWM is 100%, i.e. full duty cycle, the whole ZVT process (mode1 – mode7) occurs when the phase current commutation is on going. The monostable flip-flop M_3 will generate one narrow negative pulse. The width of the pulse ΔT_3 is determined by $\Delta t_1 + \Delta t_2 + T_c'$, where T_c' is a constant consider the turn on/off time of main switches. If n is close 2, Δt_2 would be very short or u_{Cr} would be small enough at the end of mode1, ΔT_3 can be determined by:

$$\Delta T_3 = \Delta t_1\big|_{\max} + T_c = \pi\sqrt{L_r C_r} + T_c \tag{3-32}$$

Where T_c is a constant which is greater than T_c'. The data selector makes the output of monostable flip-flop M_3 active. The monostable flip-flop M_1 generates a positive pulse when the trailing edge of M_3 negative pulse is coming. The pulse is the gate signal for auxiliary switch S_a and its width is ΔT_a which is determined by Inequality (3-30). The gate signal for switch S_L is flopped to low at the same time. Then mode 1 begins and the DC link voltage is reduced to zero. Synchronous pulse CK is also generated by a monostable flip-flop M_4, the pulse width ΔT_d should be greater than maximum Δt_1 (i.e. $\pi\sqrt{L_r C_r}$). If the D flip-flops are rising edge active, then CK is connected to the negative output of the M_4, otherwise connected to the positive output. Thus the active edge of pulse CK is within mode3 when the voltage of DC link is zero and the main switches of the inverter get ZVS condition. The monostable flip-flop M_2 generates a positive pulse when the leading edge of M_3 negative pulse is coming. The pulse width of M_2 is ΔT_b that is determined by Inequality (3-31). Then mode 4-7 occurs, the DC link voltage is increased to that of supply again. The leading edge of the gate signal for switch S_L is

determined by DC link voltage sensor signal. In a word in full cycle operation when the phase current commutation is on going, the resonant circuit generates a DC link voltage notch to let main switches of the inverter switch under ZVS condition.

B. PWM operation

In this operation, the data selector makes PWM signal active. The auxiliary switch S_L works as chop, but the main switches of the inverter do not turn on or turn off within a single PWM cycle when the phase current needs not commutate. The load current is commutated during the DC link voltage becomes zero. (As the PWM cycle is very short, it does not affect the operation of the motor).

- When PWM signal is flopped down, mode 1 begins, pulse signal for switch S_a is generated by M_1 and gate signal for switch S_L is dropped to low. However the voltage of DC link does not increase until PWM signal is flipped up. Pulse CK is also generated by M_4 to let active edge of CK locate in mode 3.

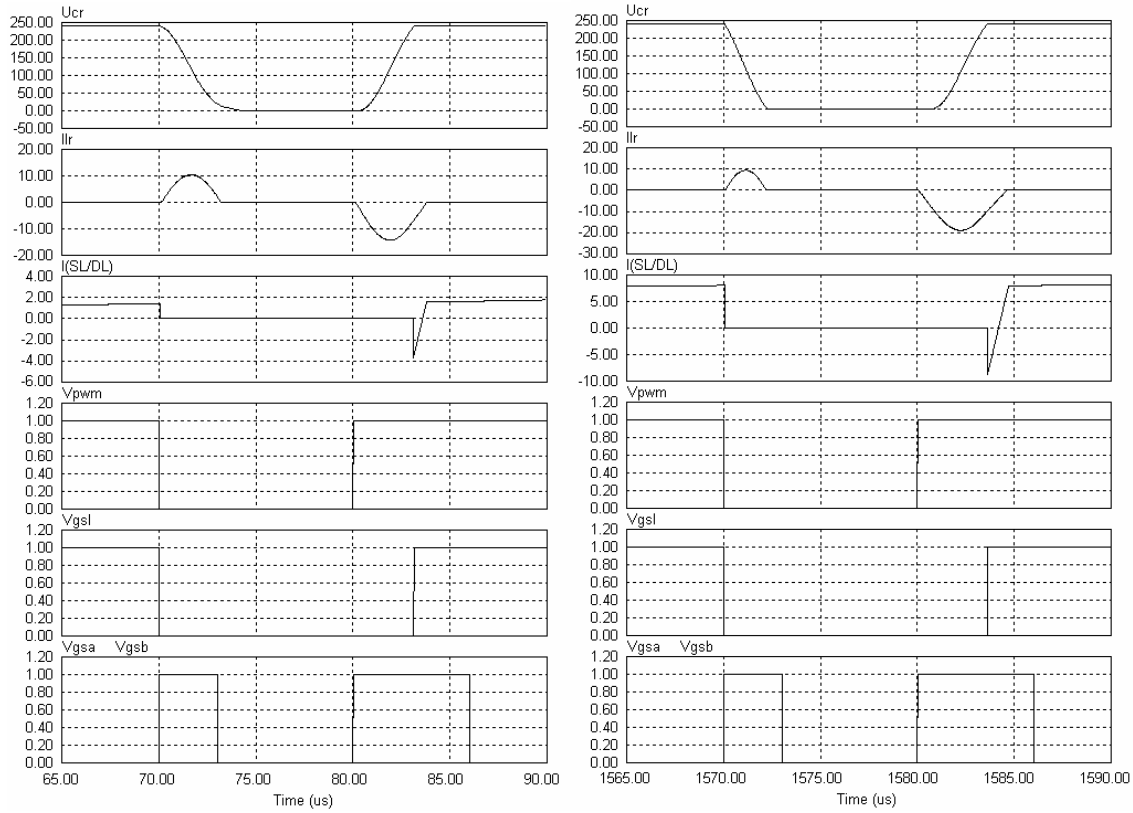
- When PWM signal is flipped up, mode 4 begins, pulse signal for switch S_b is generated at the moment. Then when the voltage of the DC link is increased to supply voltage V_S, the gate signal for switch S_L is flipped to high level.

Thus, only one ZVT occurs per PWM cycle: mode 1,2 for PWM turning off, mode 4,5,6,7 for PWM turning on. And the switching frequency would be not greater than PWM frequency.

3.2.5 Simulation and experiment

The proposed system is verified by simulation software PSim. The DC power supply voltage V_S is 240V, the maximum load current is 12A. The transformer turn ratio is 1: 1.8, the leakage inductances of the primary secondary windings are selected as 4μH and 12.96μH respectively. So the equivalent transformer inductance L_r is about 8μH. The resonant capacitance C_r is 0.1μF. Switch $S_{a,b}$ gate signal width ΔT_a and ΔT_b are set to be 3μs and 6μs respectively. The narrow negative pulse width ΔT_3 in full duty cycle is set to be 4.5μs, the delay time for synchronous pulse CK ΔT_d is set to be 3.5μs. The frequency

of the PWM is 20kHz. Waveforms of DC link voltage u_{Cr}, transformer primary winding current i_{Lr}, switch S_L and diode D_L current i_{SL}/i_{DL}, PWM, auxiliary switch gate signal under low and high load current are shown in Fig. 3-20. The figure shows that the inverter worked well under various load currents.



(a) Under low load current (I_0 = 2A) (b) Under high load current (I_0 = 8A)

Fig. 3-20. Waveforms of u_{Cr}, i_{Lr}, i_{SL}/i_{DL}, PWM, auxiliary switches gate signal under various load current

In order to verify the theoretical analysis and simulation results. The proposed soft switching inverter was tested on an experimental prototype. The DC link voltage is 240V, the switching frequency is 20kHz. Select 50A/1200V BSM 35 GB 120 DN2 dual IGBT module as main inverter switches S_1-S_6 and auxiliary switch S_L, another switch in the same module of S_L can be adopted as auxiliary switch S_a, 30A/600V IMBH30D-060 IGBT as auxiliary switch S_b. With datasheets of these switches and Equation (3-22) ~ (3-25), the value of capacitance and the parameter of transformer can be determined. A polyester capacitor of 0.1μF, 1000V was adopted as DC link resonant capacitor C_r. A high magnetizing inductance transformer with turn ratio 1:1.8 was employed in the experiment. The equivalent inductance is about 8μH under short circuit test [66]. The switching frequency is 20 kHz. The monostable flip-flop is set up by IC 74LS123,

variable resistor and capacitor. The logical gate can be replaced by programmable logical device to reduce the number of IC. ΔT_a, ΔT_b, ΔT_3 and ΔT_d are set to be 3μs, 6μs, 4.5μs and 3.5μs respectively.

From Fig. 3-19 it is required to measure the DC link voltage to generate the gate signal for auxiliary switch S_L, which can be implemented by a voltage sensor. The voltage sensor should be a high performance sensor with little delay and little distortion which may be high price. As it is only needed to know whether DC link voltage reaches DC supply voltage, auxiliary switch S_L gate signal generator can be built up as Fig. 3-21 with cheap parts. The DC link voltage is measured and compared in power stage then it is fed the AND logic gate by a Photocoupler. Detail is introduced in the Appendix E auxiliary drive board for resonant DC link inverter.

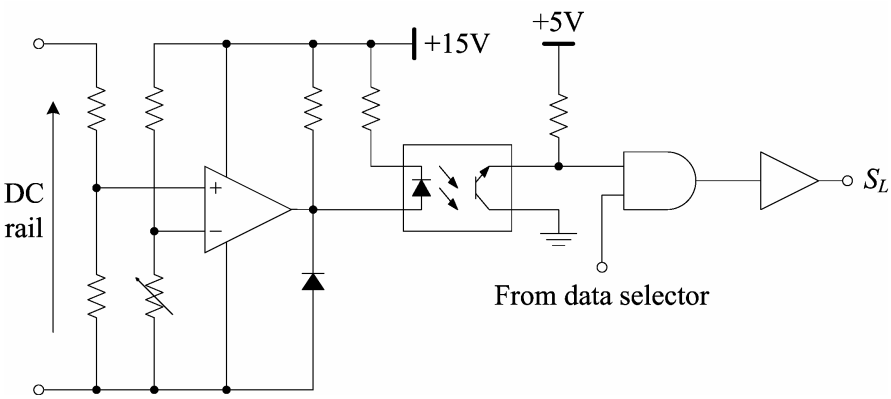
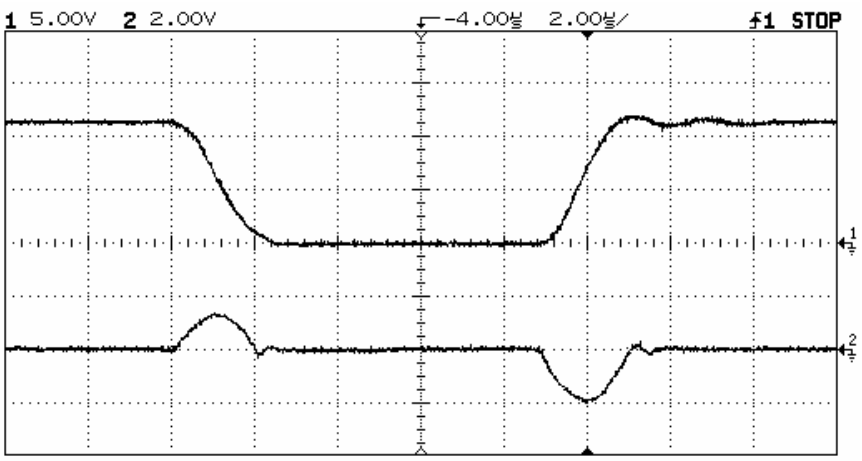
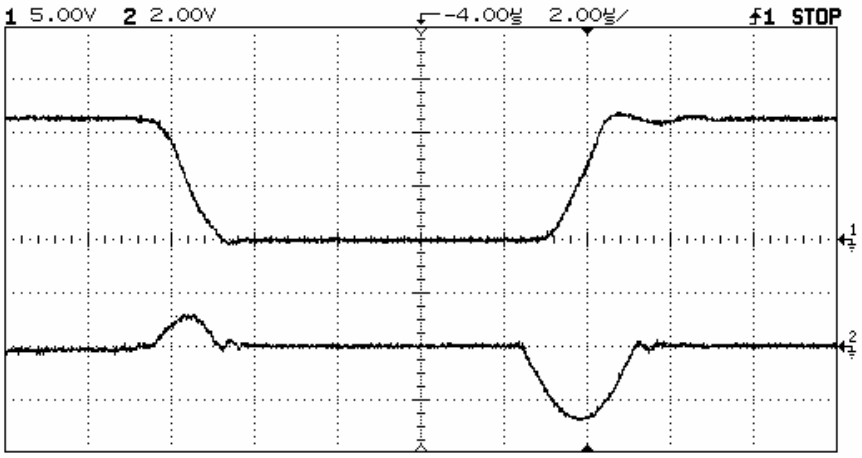


Fig. 3-21. Auxiliary switch S_L gate signal generator

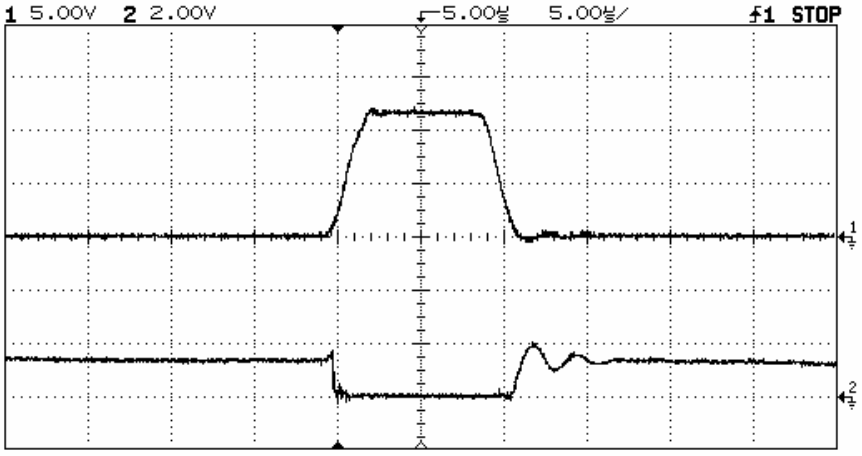
The system is tested in light and heavy load. The waveforms resonant DC link voltage u_{Cr} and transformer primary winding current i_{Lr} in low and high load currents are shown in Fig. 3-22(a) and Fig. 3-22(b) respectively. The transformer based resonant DC link inverter works well under various load currents. The waveforms of auxiliary switch S_L voltage u_{SL} and its current i_{SL} are shown in Fig. 3-22(c). There is little overlap between the switch S_L voltage and its current during the switching under soft switching condition, so the switching power losses are low. The waveforms of resonant DC link voltage u_{Cr} and synchronous signal CK are shown in Fig. 3-22(d), which the main switches can switch under ZVS condition during commutation. The phase current of BDCM is shown in Fig. 3-22(e). The design of the system is successful.



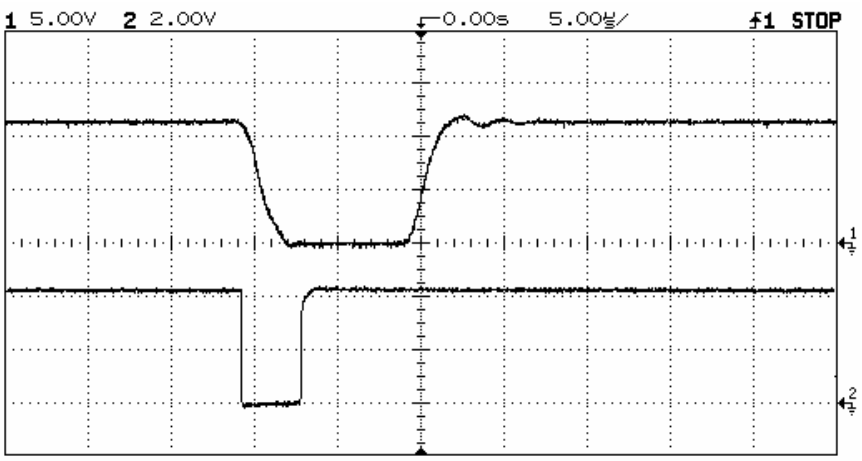
(a) u_{cr} and i_{Lr} under low load current (100V/div, 10A/div)



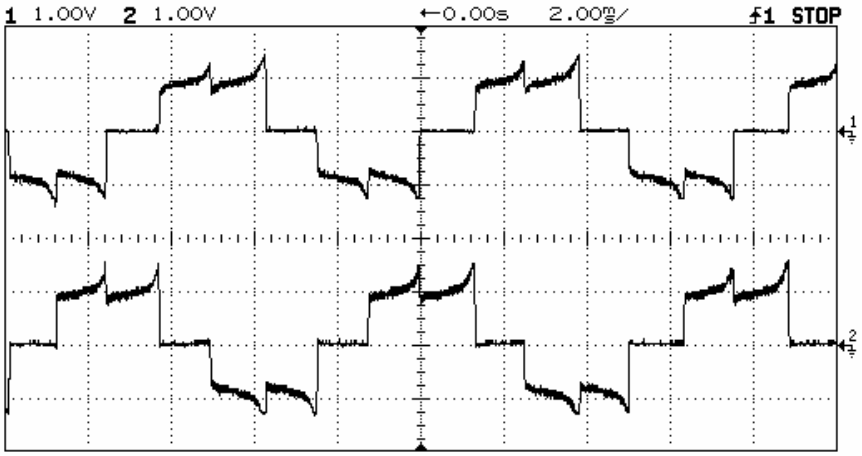
(b) u_{cr} and i_{Lr} under high load current (100V/div, 10A/div)



(c) Switch S_L voltage and current (100V/div, 10A/div)



(d) u_{cr} and synchronous signal CK (100V/div)



(e) Phase current of BDCM (5A/div)

Fig. 3-22. Experiment results

3.3 Summary

Known resonant DC link inverters have been reviewed first. A transformer based resonant DC link inverter for BDCM drive system, capable of controlling zero voltage notch instant and width is presented. Its principle of operation was explained. The simulation results are also given. All the relevant experimental waveforms were captured to verify the theory analysis and simulation. The following observations were made:

- All switches work under soft-switching condition, so their power losses are small.
- Voltage stress on all the switches would be not greater than DC Supply voltage.

- Only one DC link voltage notch is needed during one PWM cycle, and the switching frequency of the auxiliary switches would not higher than PWM frequency.
- Simple auxiliary switches control scheme.
- Freewheeling diodes turned off under zero current condition and this greatly reduced the reverse recovery problem of the diodes.
- *dv/dt* and *di/dt* are reduced significantly, so EMI is reduced.
- Soft switching results in considerably less noise as the switching frequency can be high to outside the audio spectrum.
- The topology also applicable to induction motor drive system.

Chapter 4 Resonant Pole Inverter

The structure of the resonant pole inverter (RPI) has been introduced in Chapter 1. The family of resonant pole inverter is characterized by the presence of a so-called resonant pole that comprises a resonant inductor and a pair of resonant capacitors at each phase leg. These capacitors are directly connected in parallel with the main switches in order to achieve zero-voltage switching. In this chapter, details will be proposed. Literature review will be given first, then a novel topology will be proposed, the operation principle of the inverter is analyzed. Simulation and experimental results are proposed to verify the theoretical analysis.

4.1 Literature Review

In contrast to resonant DC link inverters, no resonance is produced at the DC link in resonant pole inverters. Instead of that, the resonant transitions occur separately at each resonant pole, only when the switches in the output stage need to be commutated. The DC link voltage remains unaffected during the resonant transitions. Therefore, the main switches in the inverter phase legs can be commutated totally independent from each other and choice the commutation instant freely.

4.1.1. Auxiliary resonant commutated pole inverter

Resonant pole inverter is first proposed by D.M. Divan [18]. One of successful resonant pole inverter is auxiliary resonant commutated pole inverter (ARCPI) [41, 59, 71, 89, 90, 96]. An equivalent circuit of one phase ARCPI is shown in Fig. 4-1. Each main switch (S_1 and S_2) is closely paralleled by a snubber capacitor (C_{r1} and C_{r2}) to obtain ZVS turn-off conditions. Auxiliary switches (S_a and S_b) are placed in series with the resonant inductor L_r, and operate under zero current switching conditions. L_a is load inductor, i_a is load current. The DC link capacitor is center-tapped as the zero point.

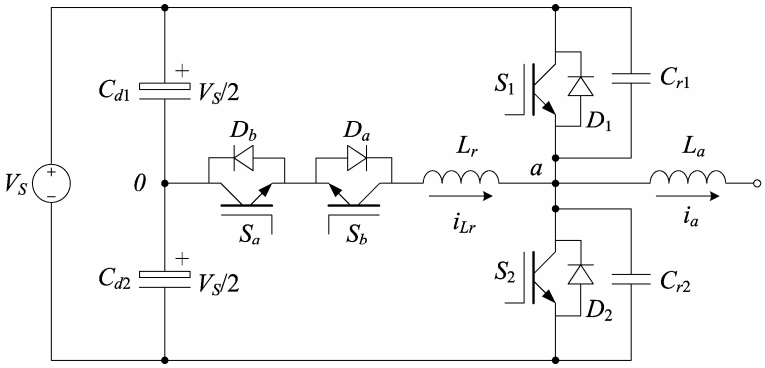


Fig. 4-1. The equivalent circuit of one phase ARCPI

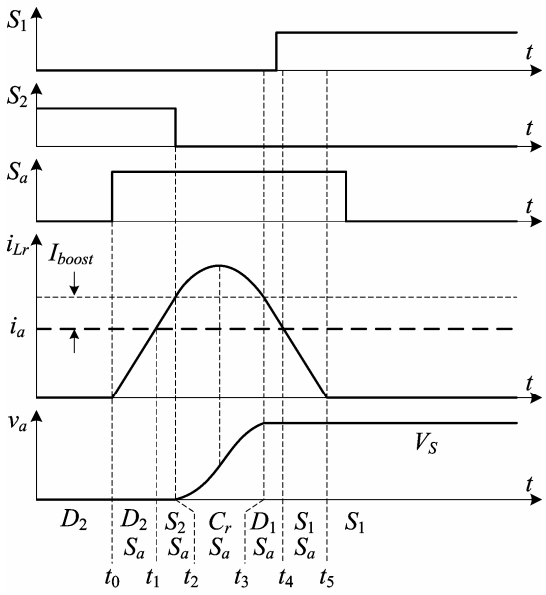


Fig. 4-2. The key waveform of ARCPI during S_2 -> S_1

As load inductance L_a is much larger than resonant inductance L_r, the load current i_a can be assumed constant in switching transition. For convenient discussion, assume load current $i_a > 0$, main switch S_1 is turned off and S_2 is turned on. Then during the switching transition of turning off the main switch S_2 and turning on S_1, the waveforms of main switches $S_1$and S_2 and auxiliary switch S_a gate signal, resonant inductor current i_{Lr}, phase voltage v_a are illustrated in Fig. 4-2. The operation of the switching transition can be divided into 7 modes.

Mode 0 ($t < t_0$): As the load current $i_a > 0$, main switch S_1 is turned off, load current flows through freewheeling diode D_2. Snubber capacitor C_{r1} voltage v_{Cr1} is DC supply voltage V_S, phase voltage v_a is zero.

Mode 1 ($t_0 < t < t_1$): At t_0, the auxiliary switch S_a is turned on (ZCS turned on due to resonant inductor L_r), resonant inductor current i_{Lr} increases linearly at a rate of $V_S / 2L_r$. When i_{Lr} reaches load current i_a, freewheeling diode D_2 is turned off self.

Mode 2 ($t_1 < t < t_2$): Resonant inductor current i_{Lr} still increases linearly, main switch S_2 carries partial resonant inductor current i_{Lr}. When i_{Lr} exceeds load current i_a at a preset threshold I_{boost}, main switch S_2 is turned off (ZVS turned off due to snubber capacitor C_{r2}). Phase voltage v_a is still zero.

Mode 3 ($t_2 < t < t_3$): Resonance occurs between resonant inductor L_r and snubber capacitors Cr_1 and C_{r2}. Phase voltage v_a rises sinusoidal, snubber capacitor C_{r1} voltage v_{Cr1} decays. The peak current in the auxiliary circuit will reach

$$i_{Lr-m} = i_a + I_{boost} + \frac{V_S}{2\sqrt{L_r / C_r}} \tag{4-1}$$

Where C_r is capacitance of snubber capacitor C_{r2}.

Mode 4 ($t_3 < t < t_4$): Phase voltage v_a reaches DC supply voltage, snubber capacitor C_{r1} voltage v_{Cr1} is zero, freewheeling diode D_1 begins to conduct, main switch S_1 can get ZVS turn on condition in this mode. Resonant inductor current i_{Lr} decreases linearly, but it is still greater than load current i_a.

Mode 5 ($t_4 < t < t_5$): Resonant inductor current i_{Lr} decreases linearly to zero and it is less than load current i_a, the load current transfers into main switch S_1.

Mode 6 ($t_5 < t < t_6$): Main switch S_1 carries load current, auxiliary switch S_a can be turned off ZCS.

The total duration of the commutation sequence can be estimated by

$$T_c = \frac{2L_r(i_a + I_{boost})}{V_S} + \pi\sqrt{L_r C_r} \tag{4-2}$$

The operation principle of switching transition from S_1 to S_2 is similar except turning on auxiliary switch S_b. When load current $i_a < 0$, the operation can be also described. The inverter is able to achieve real PWM control but it requires a stiff DC link capacitor bank that is center taped to accomplish commutation. The center voltage of DC link is susceptible to drift that may affect the operation of the resonant circuit. The inverter also needs to control current threshold I_{boost} which increases the control implementation complexity.

4.1.2 Y-configured auxiliary resonant snubber inverter

To eliminate the center taped stiff DC link capacitor bank, a Y-configured auxiliary resonant snubber inverter [56] is proposed, its structure is shown in Fig. 4-3. Each phase leg has an added resonant branch with an auxiliary switch and a resonant inductor. This topology requires one additional auxiliary switch for each phase, but the size of the auxiliary switch can be much smaller than that of the main switches because of low duty cycle. Depending on the switching frequency and the inductor design, typical size of the auxiliary switch is about one-tenth of the main switch.

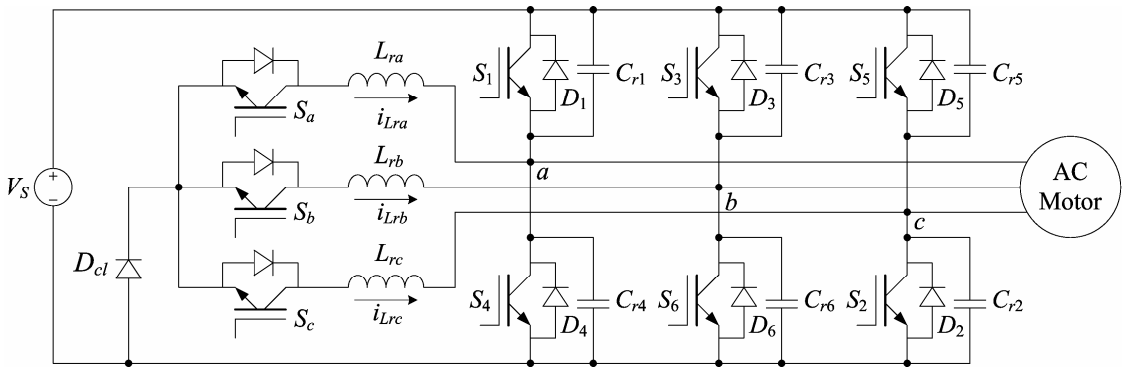


Fig. 4-3. The structure of Y-configured auxiliary resonant snubber inverter

The operation of the resonant snubber inverter is to produce zero voltage across the device using the resonant branch. For example, if the phase current is flowing through D_3, D_4 and D_5 which are anti-paralleled with S_3, S_4 and S_5, in order to turn on switch S_1 at zero voltage, we can turn on S_b and S_c to create a current path through $S_3//S_5$, (L_{rb} S_b)//(L_{rc}, S_c), S_a, L_{ra} and S_4. The supply voltage is now fully charging through this current path, and the inductor current is linearly increased. When the current in inductor L_{ra} is higher than

the load current in phase-A, we can turn off S_4 to form a resonance that charges and discharges snubber capacitors C_{r1} and C_{r4}. After the resonance, the voltage across C_{r1} tends to be negative which will be clamped to zero by the anti-paralleled diode D_1 so that main switch S_1 can be turned on at ZVS condition. The same procedure can also be applied to the other phases.

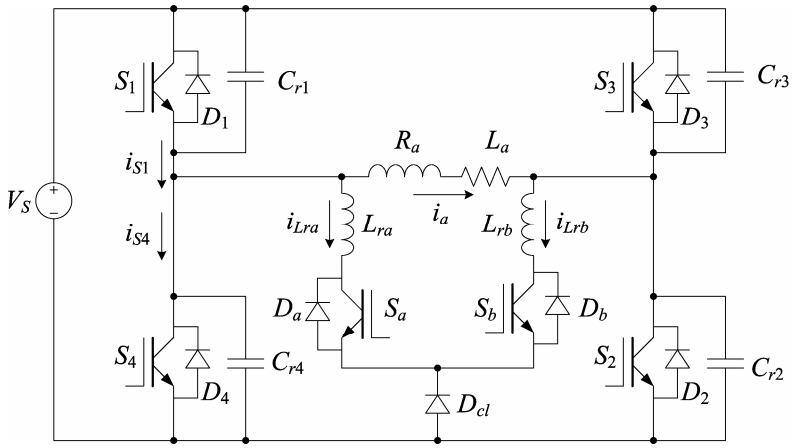


Fig. 4-4. The single phase version of auxiliary resonant snubber inverter

For single-phase applications, the proposed soft-switching inverter circuit can be configured in Fig. 4-4. This circuit consists of four main switches S_1, S_2, S_3 and S_4, and their corresponding anti-paralleled diodes D_1, D_2, D_3 and D_4. The resonant circuit consists of two resonant inductors L_{ra} and L_{rb}, two auxiliary switches S_a and S_b, and snubber capacitors C_{r1}, C_{r2}, C_{r3} and C_{r4}. These capacitors allow the main switches to turn off at ZVS condition. The inverter output is a resistor-inductor load, i.e., R_a and L_a. Typically the load inductance is much higher than the resonant inductance.

For an initially positive load current, turning off S_1 and S_2 will divert the load current to freewheeling diodes D_3 and D_4, and thus S_3 and S_4 can be turned on at ZVS condition without the need of auxiliary resonant circuit operation. If main switch S_1 and S_2 are turned on directly, the corresponding snubber capacitors discharge surge current will also flow through the switch S_1 and S_2 thus the switches may face the risk of second breakdown. The energy stored in snubber capacitors must be discharged ahead. The key waveforms of operating modes for turning on main switches S_1 and S_2 at the positive load current are illustrated in Fig. 4-5. These waveforms are main switch S_1 and S_4 and auxiliary switch S_b gate signal, resonant inductor current i_{Lr2}, main switch S_1 and S_4

branch current i_{S1} and i_{S4} (include corresponding diode current as indicated in Fig. 4-4), snubber capacitor C_{r1} voltage v_{Cr1}. The operation can be divided into 6 modes.

Mode 0 ($t_0 < t < t_1$): This is the initial condition that a positive load current is free-wheeling through D_3 and D_4 while S_3 and S_4 remain turn-on.

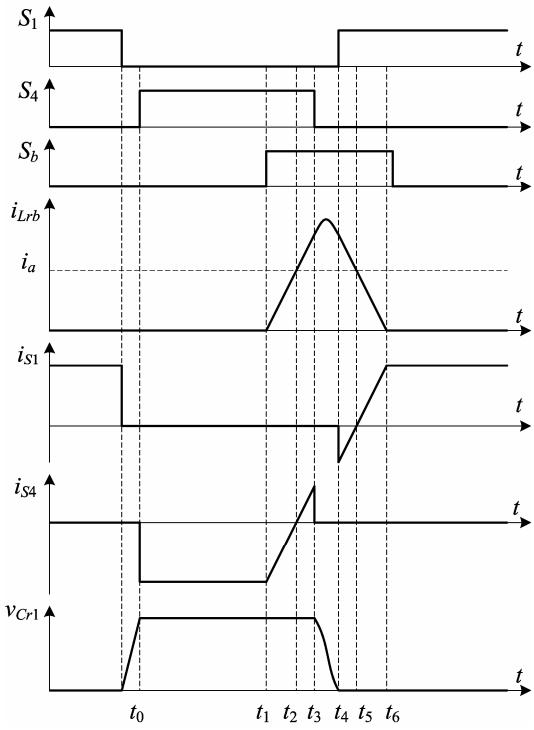


Fig. 4-5. The key waveform of auxiliary resonant snubber inverter

Mode 1 ($t_1 < t < t_2$): At t_1, turn on the auxiliary switch S_b. The resonant inductor current i_{Lrb} is built up linearly. The current in switches S_3 and S_4 gradually reduces to zero at t_2 when the resonant inductor current i_{Lrb} reaches the load current i_a.

Mode 2 ($t_2 < t < t_3$): The inductor current i_{Lrb} exceeds the load current at t_2 and the main switches S_3 and S_4 can be turned off after t_2 with ZVS condition due to snubber capacitors C_{r3} and C_{r4}.

Mode 3 ($t_3 < t < t_4$): The resonant capacitors conduct at t_3 after turning off devices S_3 and S_4, capacitors C_{r3} and C_{r4} are charged to full DC link voltage V_S, and C_{r1} and C_{r2} are discharged to zero voltage at t_4.

Mode 4 ($t_4 < t < t_5$): The resonant current starts decreasing, and the load current is diverted to diodes D_1 and D_4. Switches S_1 and S_4 can now be turned on at the zero-voltage condition. At t_5 the resonant current equals the load current, and the diode current is diverted to the switch.

Mode 5 ($t_5 < t < t_6$): The resonant current keeps decreasing, and the current of main switch S_1 and S_2 increase linearly. At t_6 the resonant current drops to zero, and the resonant switch S_b can be turned off at ZCS condition.

This topology has the advantages of simple structure and simple control scheme. There will be over-voltage across the auxiliary switch if the center point of the Y-connection resonant branch is floating. The voltage across the auxiliary switch will exceed the supply voltage which can cause over-voltage failure. One way of preventing over-voltage is to add a clamping diode D_{cl} between the center point and ground. There will be circulating current in the off phase when the main inverter circuit conducts current in two of the three phases. The off phase may have a circulating current because the load voltage is unknown and current can flow into this phase through the antiparallel diode. This case occurs mainly in BDCM drives where only two phases conduct at a time, and the back EMF tends to circulate current through resonant branches which are in off-state.

4.1.3 Delta-configured auxiliary resonant snubber inverter

To avoid over-voltage in auxiliary switches, a delta (Δ) configured resonant snubber inverter [38, 39] is proposed as shown in Fig. 4-6. The proposed inverter has auxiliary resonant branches connected between the different phase-leg outputs to avoid a floating point voltage which may cause over-voltage failure of the auxiliary switches. Instead of using an anti-paralleled diode to allow resonant current to flow in the reverse direction as in the Y-configured version, the resonant branch in the Δ-configured version uses a diode to block the negative voltage. Each auxiliary branch consists of a resonant inductor and a reverse blocking auxiliary switch.

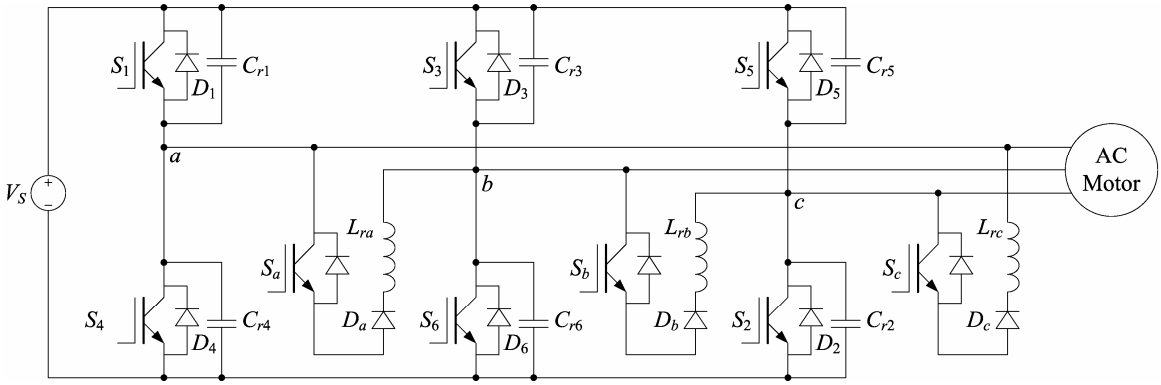


Fig. 4-6. The structure of Δ-configured resonant snubber inverter

The operation principle of Δ-configured version is similar to that of Y-configured version. For the three-phase operation, the unidirectional auxiliary switches allow the resonant current to flow only from phase *a* to *b*, *b* to *c* and *c* to *a*. For reverse resonant currents, i.e. from *b* to *a*, *c* to *b* and *a* to *c*, two auxiliary switches are turned on simultaneously. For example, to obtain a resonant current from b to a, turn on auxiliary switches S_b and S_c. This type of switching requires complicated logic circuit design and additional turn-on duty of the auxiliary switches. An alternative approach is to add a reverse conducting switch-diode pair in each branch to simplify the logic design and to reduce the conduction duty of the auxiliary switches. Fig. 4-7 shows the Δ-configured resonant snubber circuit with bidirectional auxiliary switches in resonant branch. However the inverter requires too many auxiliary switches.

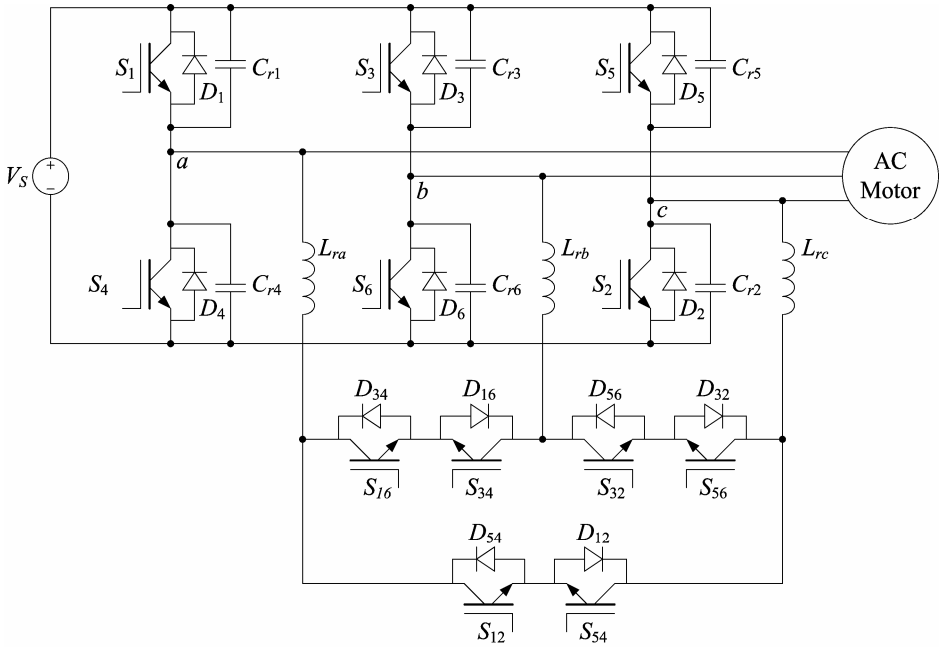


Fig. 4-7. The structure of resonant snubber inverter with bidirectional auxiliary switches

4.1.4 Zero voltage transition resonant pole inverter

To avoid the requirement of too many auxiliary switches, a zero voltage transition (ZVT) resonant pole inverter [16, 86] is introduced. The structure of the inverter is shown in Fig. 4-8.

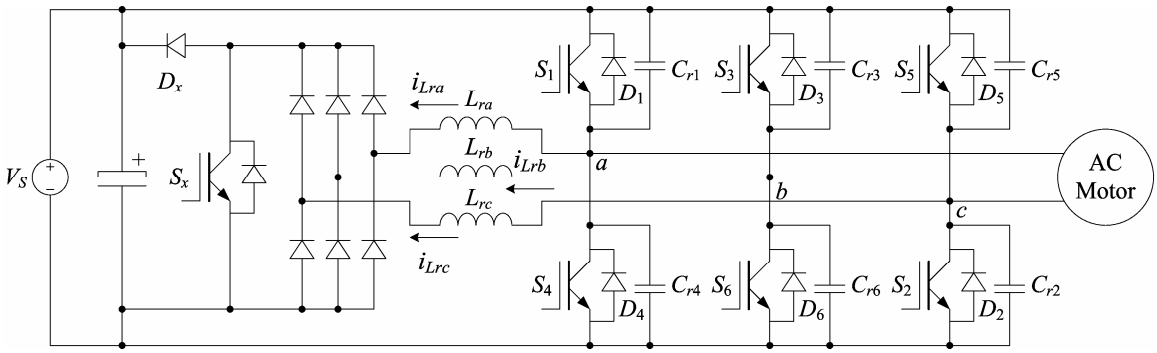


Fig. 4-8. The structure of the ZVT resonant pole inverter

To describe the operation principle, assume phase current i_a is positive, i_b and i_c are negative, main switches S_3, S_4 and S_5 are closed, phase currents are flowing through freewheeling diodes D_3, D_4 and D_5. The goal is to turn off main switches S_3, S_4 and S_5 and turn on S_1, S_2 and S_6, the phase currents are diverted to main switches, while achieving ZVS for all the switches and diodes involved in the transition. The transition can be divided into three phases: charging phase, resonant phase, discharging phase.

Charging phase: At the beginning, the auxiliary switch S_x is closed, the currents through resonant inductors i_{Lra}, i_{Lrb} and i_{Lrc} start to build up linearly from zero, gradually diverting the currents form freewheeling diodes D_3, D_4 and D_5 to the resonant circuit. When resonant inductor currents exceed the corresponding phase currents, freewheeling diodes D_3, D_4 and D_5 are turned off self with ZCS condition, which eliminates the diode reverse recovery problems. The charging stage is continued until there is enough energy stored in the auxiliary inductors to charge/discharge the snubber capacitors.

Resonant phase: After the resonant inductors L_a, L_b, and L_c have been charged, main switches S_3, S_4 and S_5 are turned off with ZVS condition due to snubber capacitors, resonant phase starts. The energy stored in the auxiliary inductors is used to charge /

discharge the snubber capacitors, swinging the phase voltage between the two DC rails. This provides ZVS turn-on conditions for the main switches S_1, S_2 and S_6.

Discharging phase: Turning on main switches S_1, S_2 and S_6 results in reversal of voltages at the resonant circuit, the energy stored in the resonant inductors is returned to the DC side, the resonant inductor currents are decays linearly. Then the auxiliary switch S_x can be turned off with ZCS condition.

The advantages of the ZVT resonant pole inverter are that it only require one auxiliary switch, and the control scheme is relative simple. However, the switching frequency of auxiliary switch is much higher than that applying to the main switches, thus it will limit the switching frequency of the inverter. Furthermore the three resonant branches of the inverter work together and will be affected each other.

4.2 Special Design Resonant Pole Inverter for BDCM

The resonant pole inverters mentioned previously are primarily applied in induction motor drive applications. They are usually required to change the switching state of two switches at the same time to obtain resonant path. It is not suitable to BDCM drive system as only one switch is needed to change the switching state in a single PWM cycle. In some topology, e.g. Y-configured auxiliary resonant snubber inverter, there will be circulating current in the off phase when the main inverter circuit conducts current in two of the three phases. The off phase may have a circulating current because the load voltage is unknown and the back EMF tends to circulate current through resonant branches which are at off-state. BDCM drive is just this case. So it is necessary to develop novel topology of soft-switching inverter and special control circuit for BDCM drive systems.

4.2.1 Topology of the resonant pole inverter

A typical controller for BDCM drive system has been introduced in Chapter 2 as shown in Fig. 2-3. The PWM is applied only to the lower switches. This not only reduces the current ripple but also avoids the need for wide bandwidth in the level-shifting circuit that feeds the upper switches. The switching frequency of three upper switches (S_1, S_3, S_5)

(typical several hundred Hz) is different from that of the three lower switches (S_4, S_6, S_2) (typical tens of kHz) in an inverter for BDCM drive system. So it is not important that the three upper switches work under soft switching condition. The switching power losses can be reduced significantly and the auxiliary circuit would be simpler if only three lower switches work under soft switching condition. Thus a specially designed resonant pole inverter [98] for BDCM drive system is introduced for this purpose which is easy to apply in industry. In addition, this inverter possesses the following advantages: low switching power losses, low inductor power losses, low switching noise and simple control scheme. The structure of the proposed inverter is shown in Fig. 4-9.

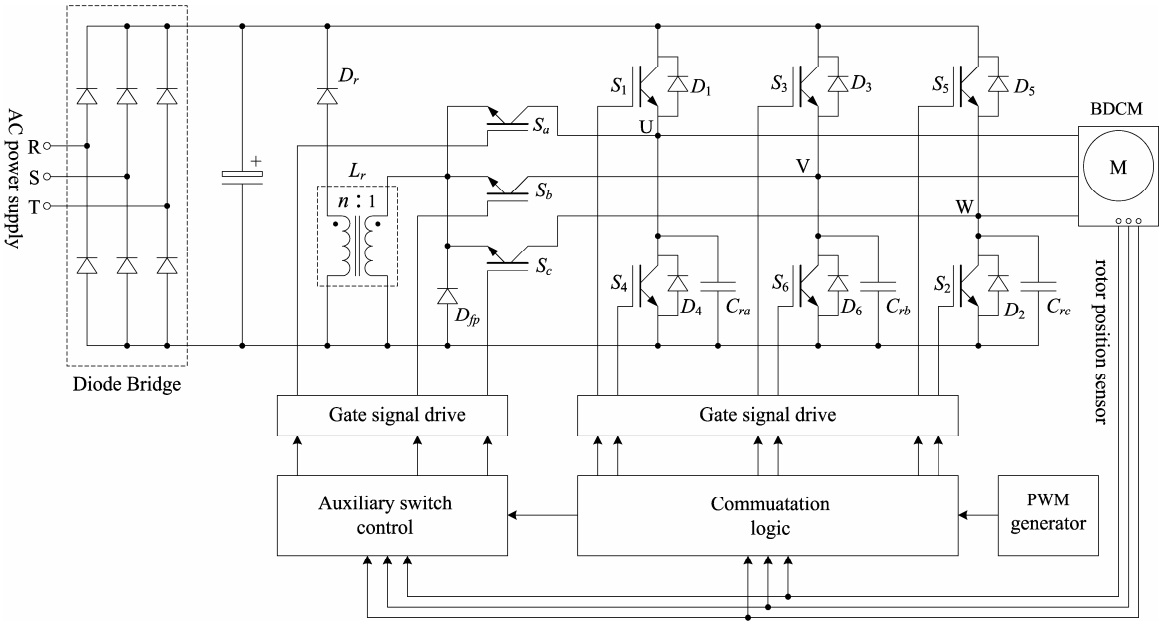


Fig. 4-9. The resonant pole inverter for BDCM drive system

The system contains a diode bridge rectifier, a resonant circuit, a conventional three-phase inverter and control circuitry. The resonant circuit consists of three auxiliary switches (S_a, S_b, S_c), one transformer with turn ratio 1: n and two diodes D_{fp}, D_r. Diode D_{fp} is connected in parallel to the primary winding of the transformer, diode D_r is serially connected with secondary winding across the DC link. There is one snubber capacitor connected in parallel to each lower switch of phase leg. The snubber capacitor resonates with the primary winding of the transformer. The emitters of the three auxiliary switches are connected together. So the gate drive of these auxiliary switches can use one common output DC power supply.

In a whole PWM cycle, the three lower switches (S_4, S_6, S_2) can be turned off in ZVS condition as the snubber capacitors (C_{ra}, C_{rb}, C_{rc},) can slow down the voltage rise rate. The turn-off power losses can be reduced and turn off voltage spike is eliminated. Before turning on the lower switch, the corresponding auxiliary switch (S_a, S_b, S_c) must be turned on ahead. The snubber capacitor is then discharged and the lower switches get ZVS condition. During phase current commutation, the switching state is changed from one lower switch to another, e.g. turn off S_6 and turn on S_2 S_6 can be turned off directly in ZVS condition, turning on auxiliary switch S_c to discharge the snubber capacitor C_{rc} then switch S_2 can get ZVS condition. During phase current commutation, if the switching state is changed from one upper switch to another upper switch, the operation is the same as hard switching inverter as the switching power losses of the upper switches is much smaller than that of lower switches.

4.2.2 Operation principle

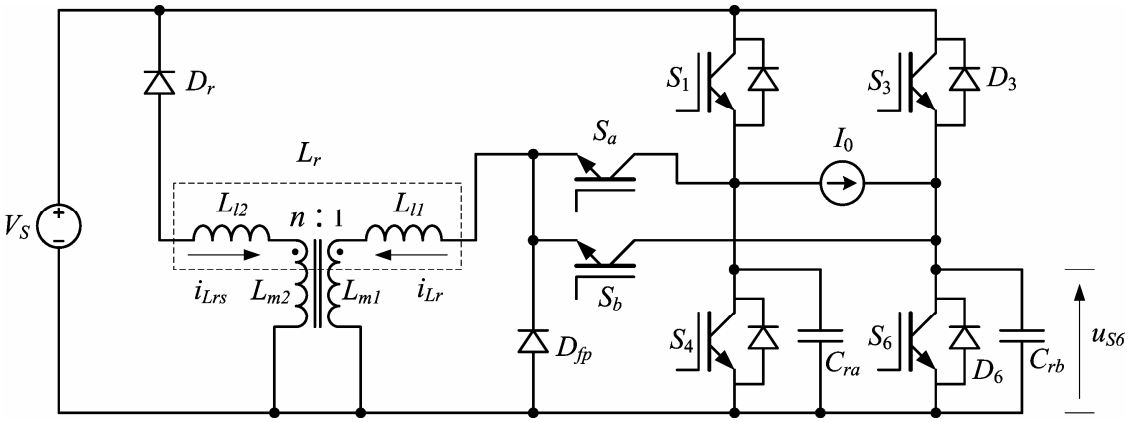


Fig. 4-10. The equivalent circuit

For convenience in describing the operation principle, we investigate the period while the switch S_1 is always turned on, switch S_6 works under PWM frequency and other main inverter switches are turned off. Since the resonant transition is very short, the load current can be assumed constant. The equivalent circuit is shown in Fig. 4-10. Where V_S is the DC link voltage, i_{Lr} is the transformer primary winding current, u_{S6} is the voltage drop across the switch S_6 (i.e. snubber capacitor C_{rb} voltage), I_0 is the load current. The waveforms of the switches (S_6, S_b) gate signal, PWM signal, main switch S_6 voltage drop (u_{S6}) and the transformer primary winding current (i_{Lr}) are illustrated in Fig. 4-11, details

will be explained following. According the interesting instant t_0-t_6, the operation of one switching cycle can be divided into 7 modes.

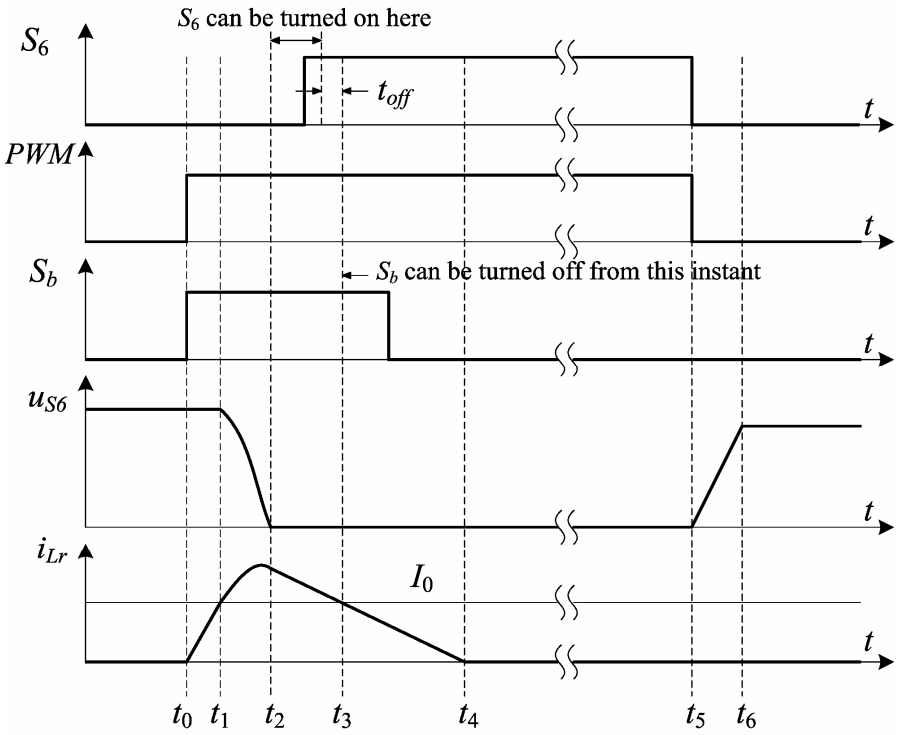


Fig. 4-11. Key waveforms of the equivalent circuit

Mode 0 (shown in Fig. 4-12) $0 < t < t_0$: After the lower switch S_6 is turned off, load current flows through upper freewheeling diode D_3, the voltage drop u_{S6} (i.e. snubber capacitor C_{rb} voltage) across the switch S_6 is the same as DC link voltage. The auxiliary resonant circuit does not operate.

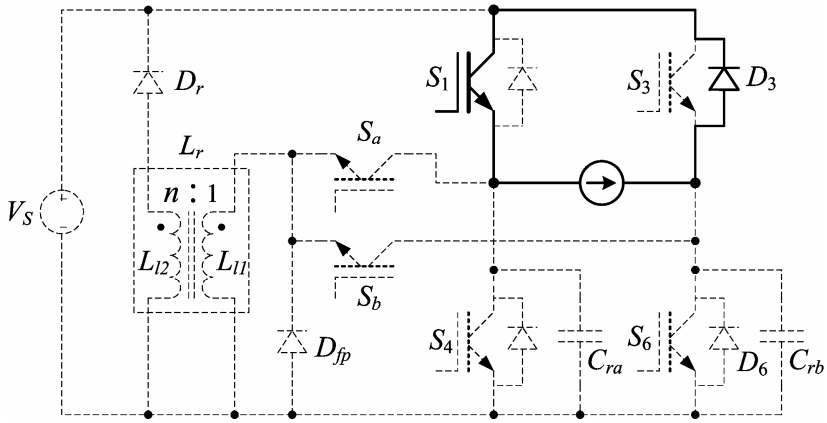


Fig. 4-12. Equivalent circuit of mode 0

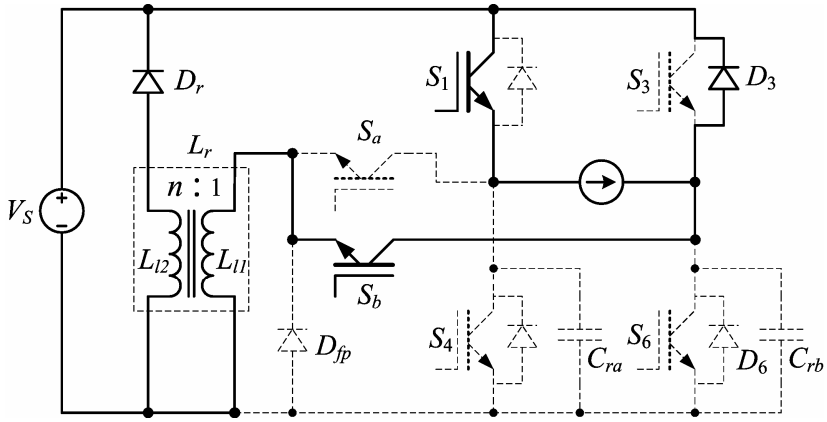


Fig. 4-13. Equivalent circuit of mode 1

Mode 1 (shown in Fig. 4-13) $t_0 < t < t_1$: If the switch S_6 is turned on directly, the capacitor discharge surge current will also flow through switch S_6 thus the switch S_6 may face the risk of second breakdown. The energy stored in snubber capacitor must be discharged ahead. Thus the auxiliary switch S_b is turned on (ZCS turn on as the i_{Lr} can't change suddenly due to the transformer inductance). The transformer primary winding current i_{Lr} begins to increase, the current flowing through freewheeling diode D_3 decays. The secondary winding current i_{Lrs} also begins to conduct through diode D_r to DC link. Both the terminal voltages of the primary and secondary windings are equal to DC link voltage V_S. Neglecting the resistances of the windings, using the transformer equivalent circuit (referred to the primary side) [72], we can get the equation:

$$V_S = L_{l1}\frac{di_{Lr}(t)}{dt} + a^2 L_{l2}\frac{d[i_{Lrs}(t)/a]}{dt} + aV_S \tag{4-3}$$

Where L_{l1} and L_{l2} are the primary and secondary winding leakage inductance respectively, a is the transformer turn ratio 1: n. The transformer has a high magnetizing inductance. We can assume that $i_{Lrs} = i_{Lr}/n$, and rewrite (1) as:

$$\frac{di_{Lr}}{dt} = \frac{(n-1)V_S}{n\left(L_{l1} + \frac{1}{n^2}L_{l2}\right)} = \frac{(n-1)V_S}{nL_r} \tag{4-4}$$

Where L_r is the equivalent inductance of the transformer $L_{l1} + L_{l2}/n^2$. The transformer primary winding current i_{Lr} increases linearly, the mode is ended when $i_{Lr} = I_0$. The interval of this mode can be determined by

$$\Delta t_1 = t_1 - t_0 = \frac{nL_r I_0}{(n-1)V_S} \tag{4-5}$$

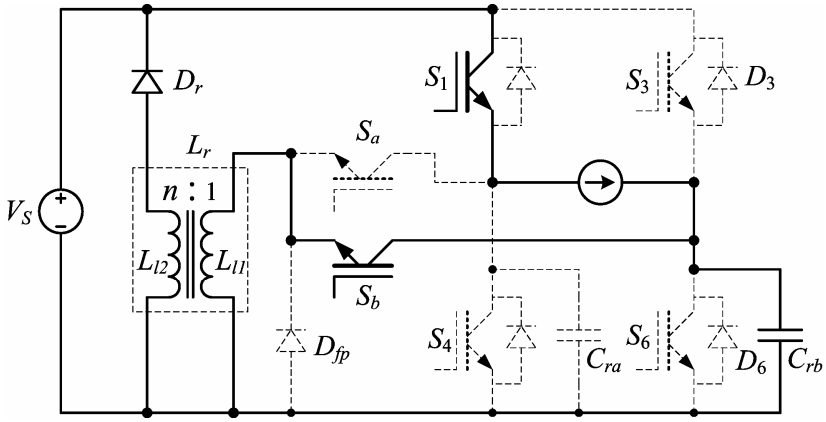


Fig. 4-14. Equivalent circuit of mode 2

Mode 2 (shown in Fig. 4-14) $t_1 < t < t_2$: At $t = t_1$, all load current flows through the transformer primary winding, freewheeling diode D_3 is turned off in ZCS condition. The freewheeling diode reverse recovery problems is reduced greatly. The snubber capacitor C_{rb} resonates with transformer, voltage drop u_{S6} across switch S_6 decays. Redefine the initial time, the transformer current i_{Lr}, i_{Lrs} and capacitor voltage u_{S6} obey the equation:

$$\begin{cases} u_{S6}(t) = L_{l1}\dfrac{di_{Lr}(t)}{dt} + a^2 L_{l2}\dfrac{d[i_{Lrs}(t)/a]}{dt} + aV_S \\ -C_r\dfrac{du_{S6}(t)}{dt} = i_{Lr}(t) - I_0 \end{cases} \tag{4-6}$$

Where C_r is the capacitance of snubber capacitor C_{rb}. The transformer current $i_{Lrs} = i_{Lr}/n$ as in mode 1, with initial conditions $u_{S6}(0) = V_S$, $i_{Lr}(0) = I_0$, the solution of (4) is

$$\begin{cases} u_{S6}(t) = \dfrac{(n-1)V_S}{n}\cos(\omega_r t) + \dfrac{V_S}{n} \\ i_{Lr}(t) = I_0 + \dfrac{(n-1)V_S}{n}\sqrt{\dfrac{C_r}{L_r}}\sin(\omega_r t) \end{cases} \tag{4-7}$$

Where $\omega_r = \sqrt{\dfrac{1}{L_r C_r}}$. Let $u_{Cr}(t) = 0$, and get the duration of the resonance:

$$\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_r}\arccos\left(-\frac{1}{n-1}\right) \tag{4-8}$$

The interval is independent from load current. At $t = t_2$, the corresponding transformer primary current i_{Lr} is

$$i_{Lr}(t_2) = I_0 + V_S\sqrt{\frac{(n-2)C_r}{nL_r}} \tag{4-9}$$

The peak value of the transformer primary current can be also determined:

$$i_{Lr-m} = I_0 + \frac{(n-1)V_S}{n}\sqrt{\frac{C_r}{L_r}} \tag{4-10}$$

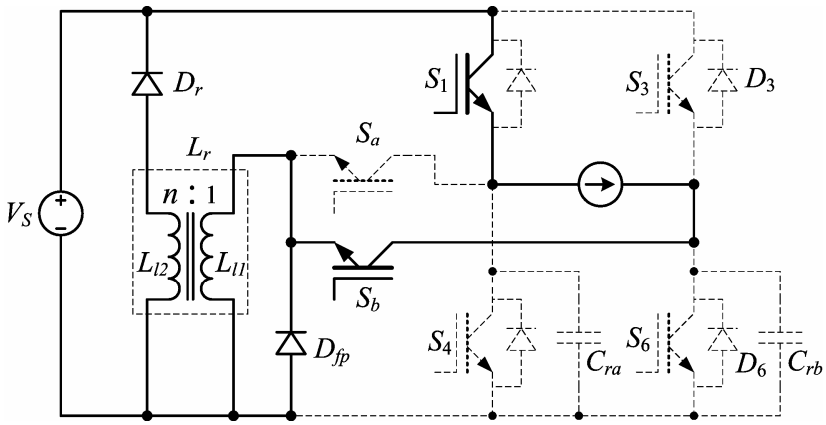


Fig. 4-15. Equivalent circuit of mode 3

Mode 3 (shown in Fig. 4-15) $t_2 < t < t_3$: When the capacitor voltage u_{S6} reaches zero at $t = t_2$, the freewheeling diode D_{fp} begins to conduct. The current flowing through auxiliary switch S_b is load current I_0. The sum current flowing through switch S_b and diode D_{fp} is transformer primary winding current i_{Lr}. The transformer primary voltage is zero and the secondary voltage is V_S. Redefine the initial time, we obtain

$$0 = L_{l1}\frac{di_{Lr}(t)}{dt} + a^2 L_{l2}\frac{d[i_{Lrs}(t)/a]}{dt} + aV_S \tag{4-11}$$

Since the transformer current $i_{Lrs} = i_{Lr}/n$ as in mode 1, we deduce (9)

$$\frac{di_{Lr}}{dt} = -\frac{V_S}{nL_r} \tag{4-12}$$

The transformer primary current i_{Lr} decays linearly, the mode is ended when $i_{Lr} = I_0$. With initial condition given by (7), the interval of this mode can be determined:

$$\Delta t_3 = t_3 - t_2 = \sqrt{n(n-2)L_r C_r} \tag{4-13}$$

The interval is also independent from load current. During this mode, switch S_6 is turned on in ZVS condition.

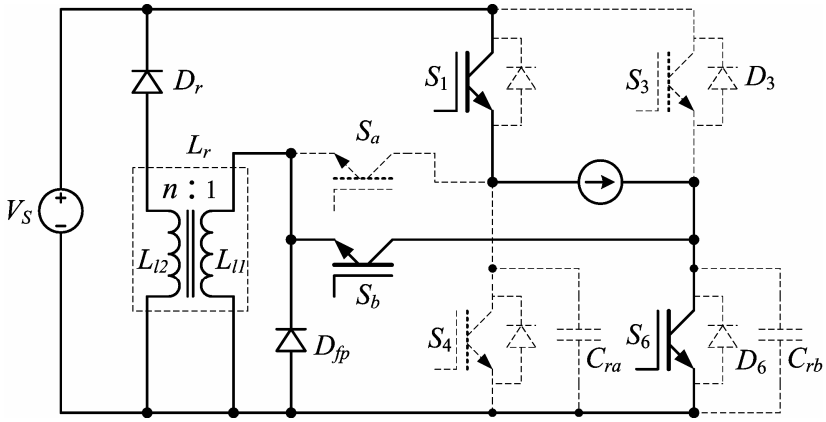


Fig. 4-16. Equivalent circuit of mode 4

Mode 4 (shown in Fig. 4-16) $t_3 < t < t_4$: The transformer primary winding current i_{Lr} decays linearly from load current I_0 to zero. Partial load current flows through the main switch S_6. The sum current flowing through switch S_6 and S_b is equal to the load current I_0. The sum current flowing through switch S_b and diode D_{fp} is transformer primary winding current i_{Lr}. Redefine the initial time, the transformer winding current obeys the Equation (4-12) with the initial condition $i_{Lr}(0) = I_0$. The interval of this mode is:

$$\Delta t_4 = t_4 - t_3 = \frac{nL_r I_0}{V_S} \tag{4-14}$$

The auxiliary switch S_b can be turned off in ZVS condition. In this case, after switch S_b is turned off, the transformer primary winding current i_{Lr} flows through freewheeling diode D_{fp}. The auxiliary switch S_b can be also turned off in ZVS and zero-current-switching (ZCS) condition after i_{Lr} decays to zero.

Mode 5 (shown in Fig. 4-17) $t_4 < t < t_5$: The transformer primary winding current decays to zero and the resonant circuit idles. This state is similar to the same operation state as

conventional hard switching inverter. The load current flows from DC link through two switches S_1 and S_6, and the motor.

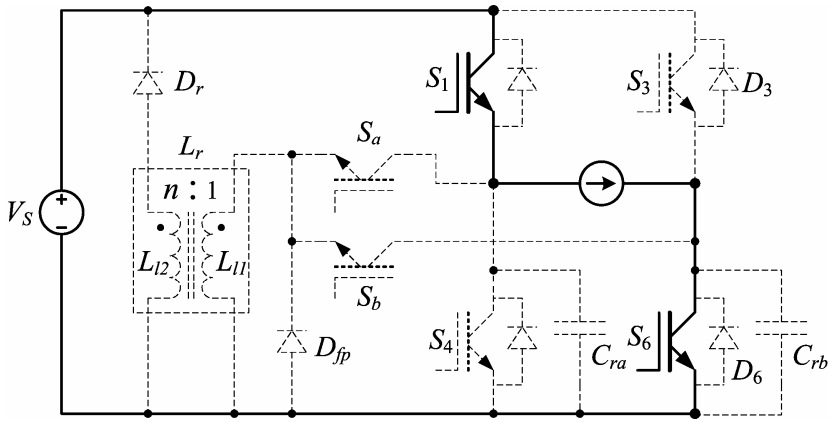


Fig. 4-17. Equivalent circuit of mode 5

Mode 6 (shown in Fig. 4-18) $t_5 < t < t_6$: The main inverter switch S_6 is turned off directly and resonant circuit does not work. The snubber capacitor C_{rb} can slow down the rise rate of u_{S6}, the main switch S_6 operates in ZVS condition. The duration of the mode is:

$$\Delta t_6 = t_6 - t_5 = \frac{C_r V_S}{I_0} \tag{4-15}$$

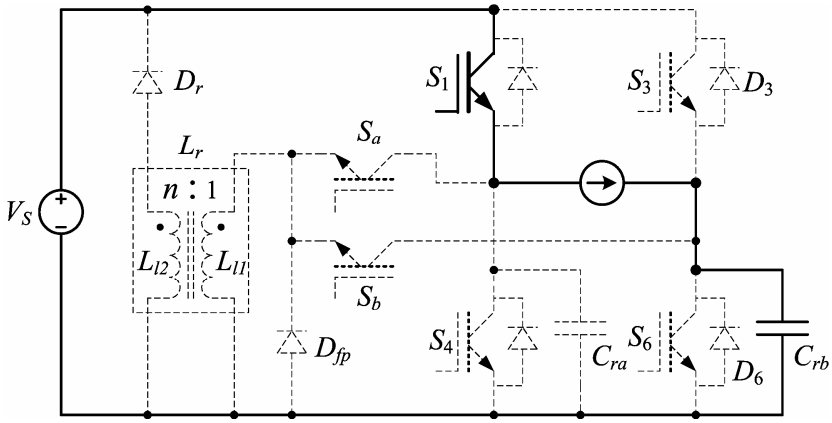


Fig. 4-18. Equivalent circuit of mode 6

The next period starts from mode 0 again, but the load current flows through freewheeling diode D_3. During phase current commutation, the switching state is changed from one lower switch to another (e.g. turn off S_6 and turn on S_2), S_6 can be turned off directly in ZVS condition (similar to mode 6), turning on auxiliary switch S_c to discharge

the snubber capacitor C_{rc} then switch S_2 can get ZVS condition (similar to mode 1 – mode 4).

4.2.3 Design considerations

It is assumed that the inductance of BDCM is much higher than the transformer leakage inductance. From the analysis presented previously, the design considerations can be summarized as follows:

- Determine the value of snubber capacitor C_r, and the parameter of transformer.
- Select the main and auxiliary switches.
- Design the control circuitry for the main and auxiliary switches.

The transformer turn ratio (1:n) can be determined ahead. From Equation (4-8) n must satisfy:

$$n > 2 \tag{4-16}$$

On the other hand, from Equation (4-14) the transformer primary winding current i_{Lr} will take a long time to decay to zero if n is too big. So n must be a moderate number. The equivalent inductance of the transformer $L_r = L_{l1} + L_{l2}/n^2$ is inversely proportional to the rise rate of the switch current when turning on the auxiliary switches. It means that the equivalent inductance L_r should be big enough to limit the rising rate of the switch current to work in ZCS condition. The selection of L_r can be referenced from the rule depicted in [19].

$$L_r \approx 4t_{on}V_S / I_{0\max} \tag{4-17}$$

Where t_{on} is the turn on time of an IGBT, I_{0max} is the maximum load current. The snubber capacitance C_r is inversely proportional to the rise rate of the switch voltage drop when turning off the lower main inverter switches. It means that the capacitance is as high as possible to limit the rising rate of the voltage to work in ZVS condition. The selection of the snubber capacitor can be determined as

$$C_r \approx 4t_{off} I_{0\max} / V_S \tag{4-18}$$

Where t_{off} is the turn off time of an IGBT. However, as the capacitance increases, more energy is stored in it. This energy should be discharged when the lower main inverter switches are turned on. With high capacitance, the peak value of transformer current will be also high. The peak value of i_{Lr} should be restricted to twice that of maximum load current. From (4-10) we obtain

$$\sqrt{\frac{C_r}{L_r}} \le \frac{nI_{0\max}}{(n-1)V_S} \tag{4-19}$$

Three lower switches of inverter (i.e. S_4, S_6, S_2) are turned on during mode 3 (i.e. lag rising edge of PWM at the time range $\Delta t_1 + \Delta t_2$ ~ $\Delta t_1 + \Delta t_2 + \Delta t_3$). In order to turn on these switches at a fixed time (say ΔT_1) lagging rising edge of PWM under various load current for control convenient, the condition should be satisfied:

$$\left(\Delta t_1 + \Delta t_2 + \Delta t_3\right)\Big|_{I_0=0} > \left(\Delta t_1 + \Delta t_2\right)\Big|_{I_0=I_{0\max}} + t_{off} \tag{4-20}$$

Substitute Equations (4-5), (4-8) and (4-13) into Equation (4-20),

$$\sqrt{n(n-2)L_r C_r} > \frac{nL_r I_{0\max}}{(n-1)V_S} + t_{off} \tag{4-21}$$

The whole switching transition time is expressed as

$$\begin{aligned} T_w &= \Delta t_1 + \Delta t_2 + \Delta t_3 + \Delta t_4 \\ &= \frac{nL_r I_0}{(n-1)V_S} + \sqrt{L_r C_r}\left[\arccos\left(-\frac{1}{n-1}\right) + \sqrt{n(n-2)}\right] \end{aligned} \tag{4-22}$$

For high switching frequencies, T_w should be as short as possible. Select the equivalent inductance L_r and snubber capacitance C_r to satisfy the Equations (4-16) - (4-21), L_r and C_r should be as small as possible.

As the transformer operates at high frequency (20kHz), the magnetic core material can be ferrite. The design of the transformer needs the parameters of form factor, frequency, the input/output voltage, input/output maximum current, ambient temperature. From Fig. 4-

11, the transformer current can be simplified as triangular waveforms, then the form factor can be determined as $2/\sqrt{3}$. Ambient temperature is dependent of application field. Other parameters can be obtained from the previous section. The transformer only carries current during the transition of turning on a switch in one cycle, so the winding can be of smaller diameter.

Main switches $S_{1\text{-}6}$ work under ZVS condition, the voltage stress is equal to the DC link voltage V_S. The device current rate can be load current. Auxiliary switches $S_{a\text{-}c}$ work under ZCS or ZVS condition, and the voltage stress is also equal to the DC link voltage V_S. The peak current flowing through them is limited to double maximum load current. As the auxiliary switches $S_{a\text{-}c}$ carry the peak current only during switch transitions, they can be rated at lower continuous current rating. The additional cost will be not too much.

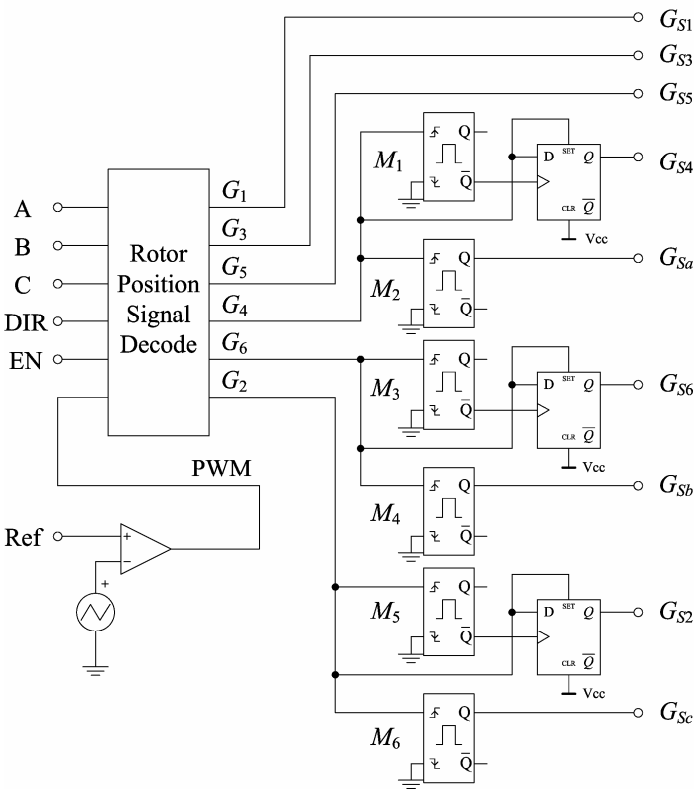


Fig. 4-19. Gate signal generator circuit

Gate signal generator circuit is shown in Fig. 4-19. Rotor position signal decode module produces the typical gate signal of the main switches. The inputs of the module are rotor position signals, rotating direction of the motor, “Enable” signal and PWM pulse-train.

The rotor position signals are three square-waves with phase shift in 120°. "Enable" signal is used to disable all outputs in case of emergency (e.g. over current, over voltage, over heat). PWM signal is the output of comparator comparing the reference voltage signal with triangular wave. The reference voltage signal is the output of speed controller. Speed controller is a processor (single chip computer or digital signal processor) and the PWM signal can be produced by software. The outputs (G_1 - G_6) of the module are the gate signals applied to the main inverter switches. The outputs $G_{1,3,5}$ are the required gate signals for three upper main inverter switches.

The gate signals of three lower main inverter switches and auxiliary switches can be deduced from the outputs $G_{4,6,2}$ as shown in Fig. 4-20. The trailing edge of the gate signals for three lower main inverter switches $G_{S4,6,2}$ is the same as that of $G_{4,6,2}$, the leading edge of $G_{S4,6,2}$ lags $G_{4,6,2}$ for a small time ΔT_1. The gate signals for auxiliary switches $G_{Sa,b,c}$ have a fixed pulse width (ΔT_2) with the leading edge same as that of $G_{4,6,2}$. In Fig. 4-19, the gate signals $G_{Sa,b,c}$ are the outputs of monostable flip-flops $M_{2,4,6}$ with the inputs $G_{4,6,2}$. The three monostable flip-flops $M_{2,4,6}$ have the same pulse width ΔT_2. The gate signals $G_{S4,6,2}$ are combined by the negative outputs of monostable flip-flops $M_{1,3,5}$ and $G_{4,6,2}$. The combining logical controller can be implemented by a D flip-flop with "preset" and "clear" terminals. The three monostable flip-flops $M_{2,4,6}$ have the same pulse width ΔT_1.

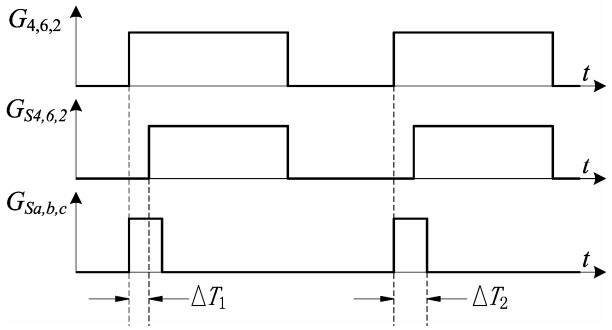


Fig. 4-20. Gate signals $G_{S4,6,2}$ and $G_{Sa,b,c}$ from $G_{4,6,2}$

Determination of the pulse widths of ΔT_1 and ΔT_2 is referenced from theoretical analysis in section 4.2.2. In order to get ZVS condition of the main inverter switches under various load currents, the lag time ΔT_1 should satisfy:

$$\left(\Delta t_1 + \Delta t_2\right)\Big|_{I_0=I_{0\max}} < \Delta T_1 < \left(\Delta t_1 + \Delta t_2 + \Delta t_3\right)\Big|_{I_0=0} - t_{off} \tag{4-23}$$

In order to get soft switching condition of the auxiliary switches, pulse width ΔT_2 needs only satisfy:

$$\Delta T_2 > \left(\Delta t_1 + \Delta t_2 + \Delta t_3\right)\Big|_{I_0=I_{0\max}} \tag{4-24}$$

4.2.4 Simulation and experimental results

The proposed topology is verified by simulation software PSim. The DC link voltage V_S is 300V, the maximum load current is 25A. The parameters of the resonant circuit were determined from Equations (4-16) - (4-22). The transformer turn ratio is 1: 4, the leakage inductances of the primary secondary windings are 6μH and 24μH respectively. So the equivalent transformer inductance L_r is 7.5μH. The resonant capacitance C_r is 0.047μF. Then $\Delta t_1 + \Delta t_2$ and $\Delta t_1 + \Delta t_2 + \Delta t_3$ can be determined under various load current I_0 as shown in Fig. 4-21. Considering the turn off time of a switch lagging time ΔT_1 and pulse width ΔT_2 are set to 2.1μs and 5μs respectively. The frequency of the PWM is 20 kHz. Waveforms of transformer primary winding current i_{Lr}, switch S_6 voltage drop u_{S6}, PWM, main switch S_6 and auxiliary switch S_b gate signal under low and high load current are shown in Fig. 4-22. The figure shows that the inverter worked well under various load currents.

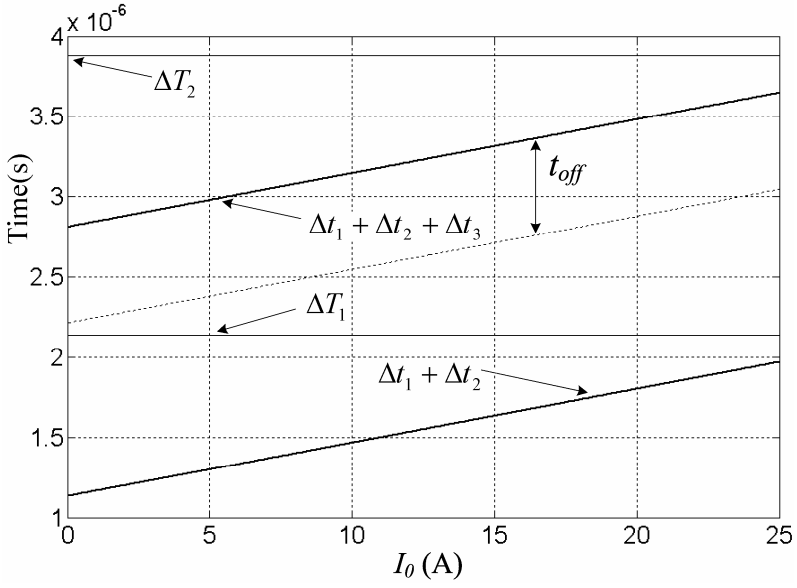
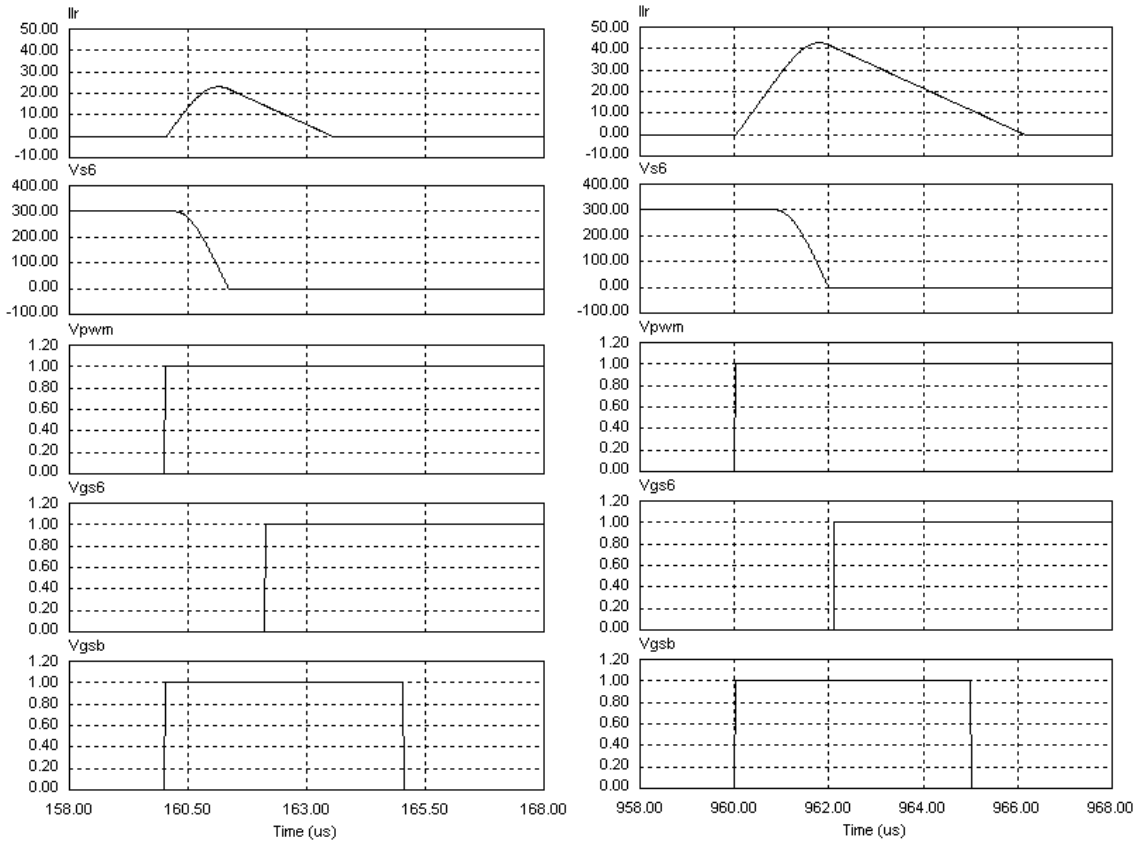


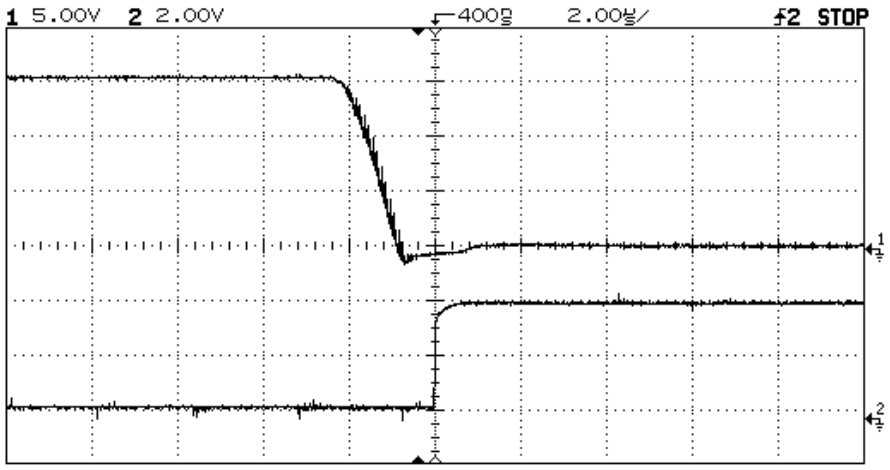
Fig. 4-21. Boundary of ΔT_1 and ΔT_2 under various load current I_0



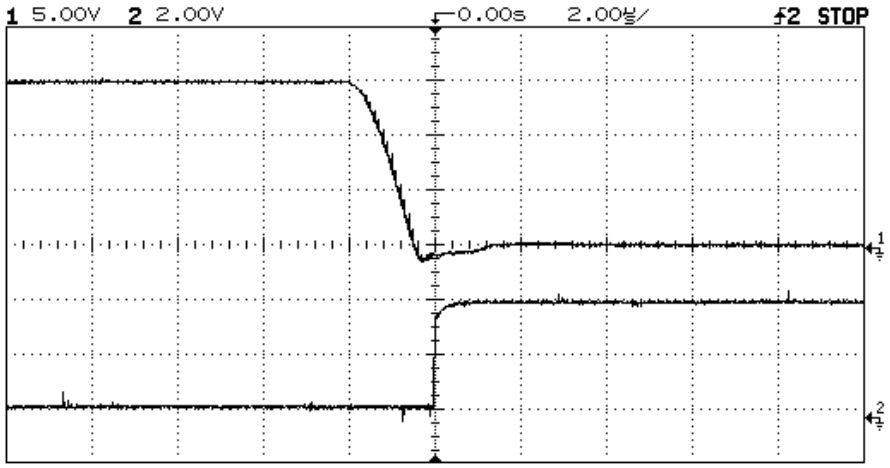
(a) Under low load current (I_0 = 5A) (b) Under high load current (I_0 = 25A)

Fig. 4-22. Simulation waveforms of i_{Lr}, u_{S6}, PWM, S_6 and S_b gate signal under various load current

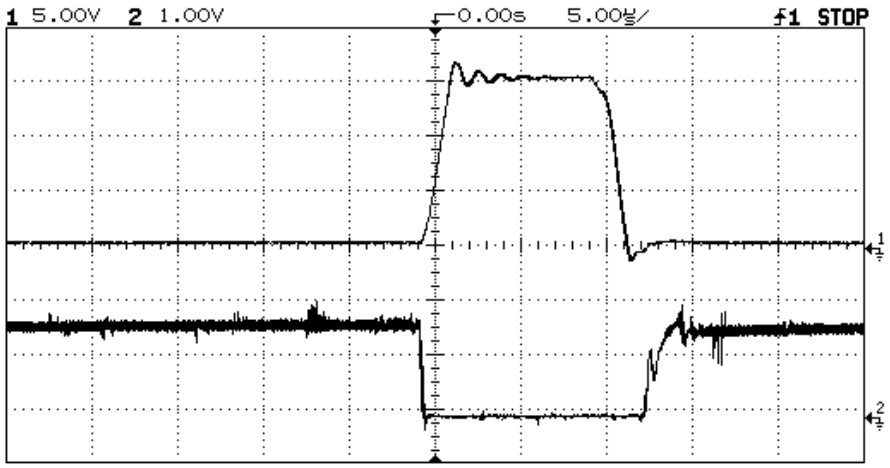
In order to verify the theoretical analysis and simulation results, the inverter was tested by experiment. The DC link voltage is 300V, the switching frequency is 20kHz. Select 50A/1200V BSM 35 GB 120 DN2 dual IGBT module as main inverter switches, 30A/600V IMBH30D-060 IGBT as auxiliary switches. With datasheets of these switches and Equation (4-16) – (4-22), the value of inductance and capacitance can be determined. Three polyester capacitors of 47nF/630V were adopted as snubber capacitor C_r for three lower switches of the inverter. A high magnetizing inductance transformer with turn ratio 1:4 was employed in the experiment. 52 turns wires with size AWG 15 are selected as primary winding, 208 turns wires with size AWG 20 are selected as secondary winding. The equivalent inductance is about 7μH. The switching frequency is 20 kHz. The rotor position signal decode module is implemented by a 20 leads gate array logic (GAL) IC GAL16V8. The monostable flip-flop is set up by IC 74LS123, variable resistor and capacitor. With Equations (4-23) and (4-24), lag time ΔT_1 and pulse width ΔT_2 are determined to be 2.5μs and 5μs respectively.



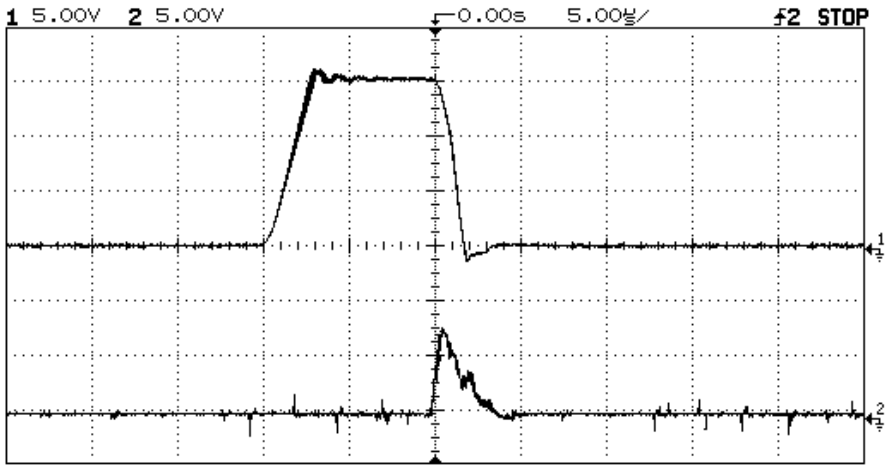
(a) Switch S_6 voltage u_{S6} (top) and its gate signal (bottom) under low load current (100V/div)



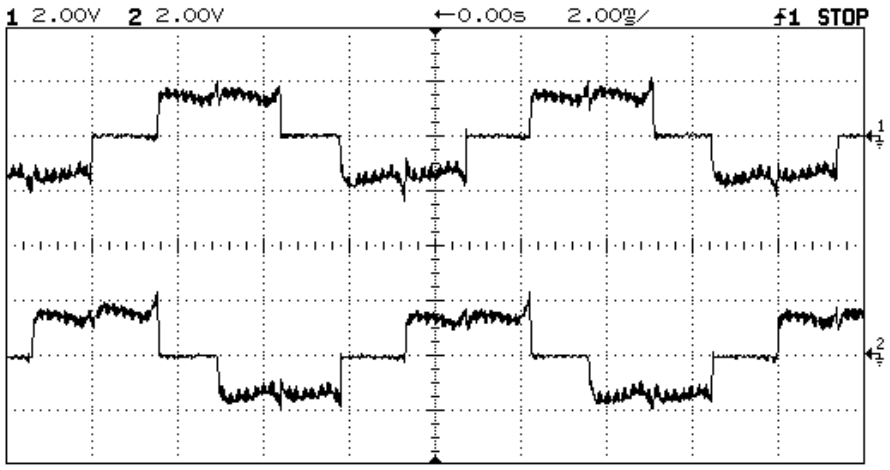
(b) Switch S_6 voltage u_{S6} (top) and its gate signal (bottom) under high load current (100V/div)



(c) Switch S_6 voltage u_{S6} (top) and its current i_{S6} (bottom) (100V/div, 5A/div)



(d) Switch S_6 voltage u_{S6} (top) and transformer current i_{Lr} (bottom) (100V/div, 25A/div)



(e) The waveforms of phase current (10A/div)

Fig. 4-23. Experiment waveforms

The system is tested in light load and full load currents. The waveforms of the voltage across main inverter switch u_{S6} and its gate signal in low and high load currents are shown in Fig. 4-23(a) and Fig. 4-23(b) respectively. All the voltage signals measured by a differential probe with a gain of 20. For voltage waveform, 5.00V/div = 100V/div. The waveforms of u_{S6} and its current i_{S6} are shown in Fig. 4-23(c), *dv/dt* and *di/dt* are reduced significantly. The waveforms of u_{S6} and transformer primary winding current i_{Lr} are shown in Fig. 4-23(d). The phase current is shown in Fig. 4-23(e). It can be seen that the resonant pole inverter works well under various load currents, and there is little overlap between the voltage and current waveforms during the switching under soft switching condition, so the switching power losses is low. The efficiency of hard switching and soft

switching under rated speed and various load torque (p.u.) is shown in Fig. 4-24. The efficiency improves with soft switching inverter. The design of the system is successful.

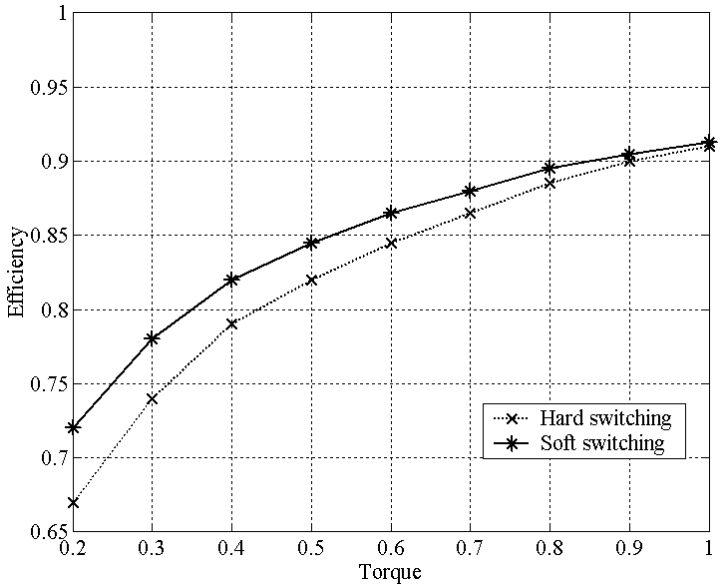


Fig. 4-24. Efficiency of hard switching and soft switching under various load torque (p.u.)

4.3 Summary

Known resonant pole inverters have been reviewed firstly. A specially designed resonant pole inverter dedicated for BDCM drive system is presented. Its principle of operation is explained. Selection of the required transformer parameter, snubber capacitors is given. The main inverter switches and auxiliary switches gate signal generation methods are also illustrated. Determination of the corresponding pulse width is given. The inverter operation is also verified by the results of simulation and experiment. The following observations were made:

- All the high switching frequency switches (three lower main switches and auxiliary switches) work under soft-switching condition.
- Voltage stress on all the switches is low that is not greater than DC Supply voltage.
- Very simple auxiliary switches control scheme.
- Freewheeling diodes turned off under zero current condition and this greatly reduced the reverse recovery problem of the diodes.

- The normal operation of the inverter is entirely the same as hard switching inverter.
- *dv/dt* and *di/dt* are reduced significantly, so EMI is reduced.
- As the switching frequency is as high as 20 kHz, the switching acoustic noise can be eliminated.

Chapter 5 Fuzzy and PI Hybrid Control

PI controller has the advantage of fast response especially in motor starting but it will introduce overshoot and oscillation. The fuzzy logic controller can solve these problems and is robust to the system parameters variation while it has slower response than that of PI controller. A hybrid controller for the PM BDCM drive system is proposed in this chapter which holds the advantages of both PI and fuzzy logic controller. In case of large speed error, PI controller is active; in case of small speed error, fuzzy logic controller is applied. Experimental results are given to verify the feasibility of the controller.

5.1 Introduction

Fuzzy logic, or fuzzy set theory, was first presented by Zadeh [53]. The main idea of fuzzy logic control is to use the control ability of human being which includes experience and intuition so the nature of the controller has adaptive characteristics that can achieve robust response to a system with uncertainty, parameter variation, and load disturbance. The fuzzy logic control [9, 26, 28, 48] has been broadly used in ill-defined, nonlinear, or imprecise systems and no accurate mathematical model of the complete system is required. In the area of the electrical drive system, fuzzy logic controllers have been applied to switched reluctance motors [8, 31], induction motors [57], brushless DC motors [76] and so on.

PI controller has the advantage of fast response especially in motor starting but it will introduce overshoot and oscillation. The fuzzy logic controller can solve these problems while it has slower response than that of PI controller. To utilize the advantages of both PI and fuzzy logic controllers to provide better response than any one controller only, hybrid controller with fuzzy logic and PI has been introduced in many fields and achieve good performance. Un-Chul Moon proposed hybrid PI and fuzzy controller for TV glass furnace temperature control [82] to overcome the complex and nonlinear of glass melting furnace. Yen-Shin Lai also introduced this hybrid controller for direct torque control

induction motor drives [97] which reduces the steady state error as compared with PI-type fuzzy logic controller, while keeping the merits of PI-type FLC. Onat M. proposed fuzzy plus integral control of the effluent turbidity in direct filtration [65] which successfully compensates the disturbances such as the filter flow rate and the influent turbidity that directly affect the effluent turbidity.

Rubaai A. proposed a hybrid fuzzy and PI controller for PM BDCM drive system which is effective and simple to design [76]. However it is a single closed-loop controller without current loop which will be slow response in motor starting and sensitive to load disturbance. Moreover the load current may exceed allowed maximum value which will be harmful to the motor. This chapter introduces a hybrid fuzzy and adaptive PI controller with current/speed double closed-loop for PM BDCM drive system. It has the advantages of fast response, little overshoot, robust, stability and so on. It has also the advantage of easy to be implemented and the algorithm, flowing chart of the software will be offered in this chapter. The structure of the control system is shown in Fig. 5-1. It includes outer speed loop, inner current loop, drive system, sensor and user interface (to set reference speed and other parameter). The outer speed loop comprises two controllers: PI controller and fuzzy logic controller. In case of large speed error PI controller is active, in case of small speed error fuzzy logic controller is applied. The inner current loop is made up of a conventional PI controller. The drive system includes rectifier, inverter, motor and mechanical load.

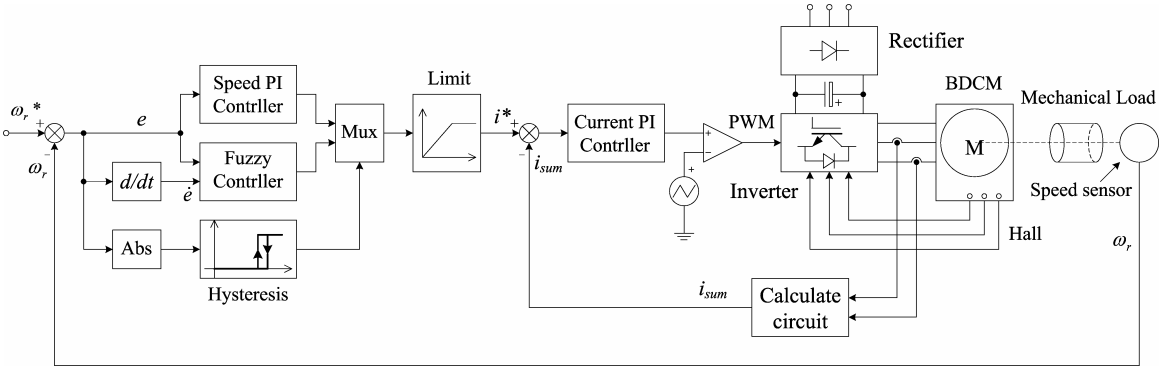


Fig. 5-1. The structure of control system

5.2 Model of Drive System

The drive system comprises rectifier, inverter, motor and mechanical load. The rectifier is a three-phase diode bridge. The inverter can be hard switching inverter or soft switching inverter. The soft-switching inverters have been introduced in Chapter 3 and Chapter 4. Assumption the rotor reluctance of PM BDCM is constant independent rotor position θ_r and only the fundamental components of the flux linkages contributed by the permanent magnet are considered. Then the mathematical model of the three phase Y connected PM BDCM can be expressed as [67]

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} L-M & 0 & 0 \\ 0 & L-M & 0 \\ 0 & 0 & L-M \end{bmatrix} p \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \quad (5\text{-}1)$$

$$T_e = (e_a i_a + e_b i_b + e_c i_c)/\omega_r \quad (5\text{-}2)$$

Where R is the phase resistance, L is phase inductance, M is the mutual inductance, $v_{a,\,b,\,c}$ is the phase voltage, $i_{a,\,b,\,c}$ is the phase current, e is the phase back EMF, p is the derivational operator $\frac{d}{dt}$, ω_r is the rotor speed, and T_e is electromagnetic torque.

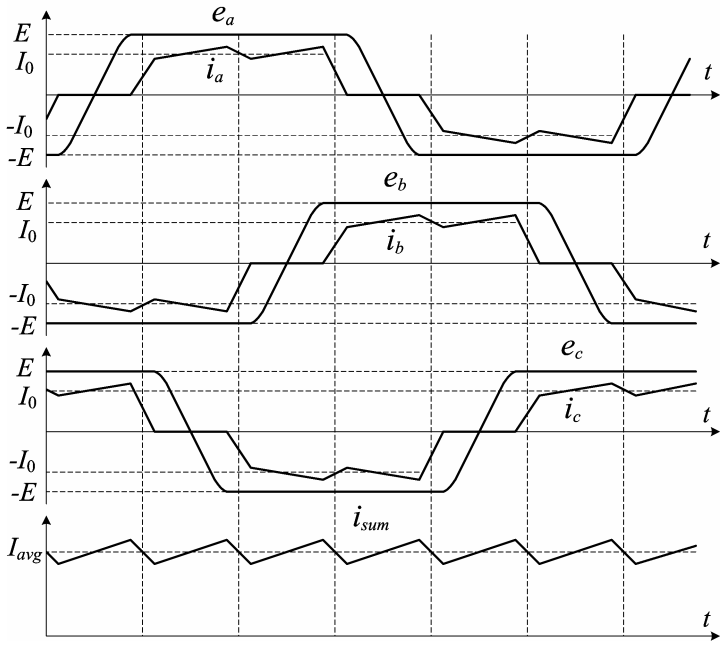


Fig. 5-2. The waveforms of back EMF and phase currents

For three-phase Y connected trapezoidal back EMF PM BDCM, two phases are active at all time, phase currents commutation happens every 60 electrical degrees. Normal waveforms of back EMF, phase currents are shown in Fig. 5-2. The sum of absolute phase currents i_{sum} is also shown in the figure. I_{avg} is the average value of i_{sum}. The maximum phase back EMF E is expressed as:

$$E = K\phi\omega_r \tag{5-3}$$

Where ϕ is flux per pole produced by the permanent magnetic, K is a constant for a given motor which is related to the number of poles, conductors in the armature, parallel paths in the armature circuit. Details have been described in Chapter 2. When the phase currents are active, it is beyond the flat top part of back EMF. Then from Equations (5-2) and (5-3), the electromagnetic torque is in the form:

$$T_e = K\phi\, i_{sum} \tag{5-4}$$

From Equation (5-1), we can also get

$$v = R_{eq} i_{sum} + L_{eq} \frac{di_{sum}}{dt} + K\phi\omega_r \tag{5-5}$$

Where R_{eq} is the equivalent resistance $R_{eq} \approx R/2$, L_{eq} is the equivalent inductance $L_{eq} \approx (L-M)/2$, v is the equivalent terminal voltage $v = \delta V_S$, V_S is the inverter DC link voltage (DC power supply voltage), δ is the duty of PWM. The Equations (5-4) and (5-5) are similar to that of conventional DC motor. For three-phase Y connected PM BDCM, the two active phases are connected in serial, we can not control their current separately, but we can change inverter average voltage to control the sum of absolute phase current i_{sum}. Thus we can design the controller for PM BDCM according the design formula for commutated DC motor.

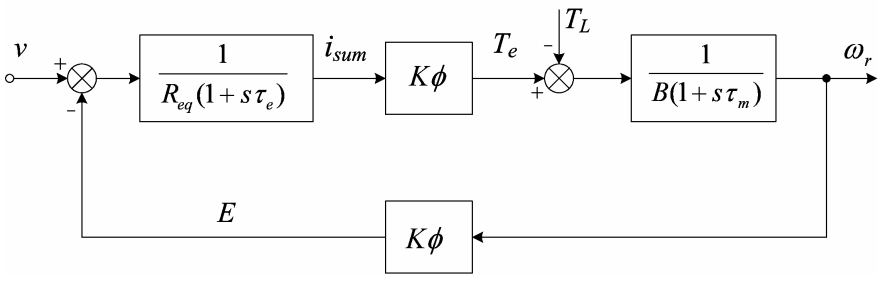


Fig. 5-3. The block diagram of the PM BDCM

The motion equation of the drive system is describe as

$$J\frac{d\omega_r}{dt} = T_e - B\omega_r - T_L \tag{5-6}$$

Where J is the moment inertia of motor and load, B is the viscous friction coefficient which is generally small and can be neglected, T_L is the load torque. Then the block diagram of PM BDCM can be got from Equations (5-3) ~ (5-6) as shown in Fig. 5-3, where τ_e is electrical time constant L_{eq}/R_{eq}, τ_m is mechanical time constant J/B.

5.3 Current Controller

The inner current loop of the controller is a PI controller. The design of the current loop controller can be referred from the textbook [34]. The output of the current controller is PWM duty δ for the inverter, the average voltage for motor is proportional to the duty δ, when switching frequency is high enough the inverter can be considered as one amplifier, it has the gain of K_C which is proportional to DC link voltage. The current loop for PM BDCM is shown in Fig. 5-4. Where K_{si} is the gain of current controller, τ_{si} is the integral time constant, K_i is the gain of current sensor, τ_{em} is electromechanical time constant $JR/(K\phi)^2$. The current controller is expressed as

$$G_i(s) = \frac{K_{si}(1+s\tau_{si})}{s\tau_{si}} \tag{5-7}$$

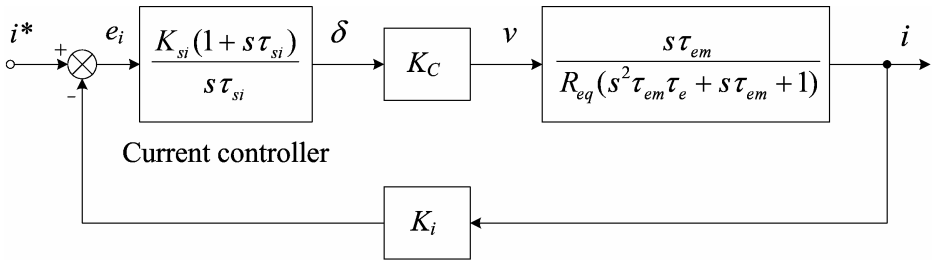


Fig. 5-4. The current loop for the PM BDCM

Consider current loop is much faster than that of speed loop, when $\omega^2\tau_{em}\tau_e >> 1$, the right block of Fig. 5-4 can be simplified as

$$\frac{s\tau_{em}}{R_{eq}(s^2\tau_{em}\tau_e + s\tau_{em} + 1)} \approx \frac{s\tau_{em}}{R_{eq}(s^2\tau_{em}\tau_e + s\tau_{em})} = \frac{1}{R_{eq}(1 + s\tau_e)} \tag{5-8}$$

Select the integral time constant τ_{si} to be equal to the electrical time constant τ_e i.e. $\tau_{si} = \tau_e$, then simpler current loop can be obtained as shown in Fig. 5-5.

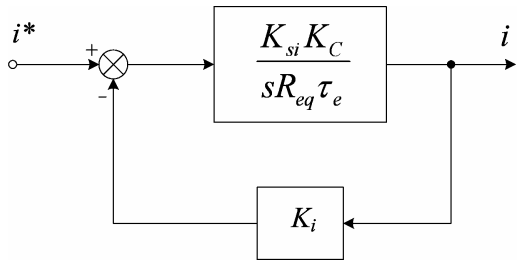


Fig. 5-5. The simplified current loop for the PM BDCM

For given critical frequency ω_{ci}, the gain of current controller K_{si} can be determined:

$$K_{si} = \frac{\omega_{ci}\tau_e R_{eq}}{K_C K_i} \tag{5-9}$$

The close loop transfer function can be also determined:

$$H_i(s) = \frac{1}{K_i(1 + s/\omega_{ci})} \tag{5-10}$$

The current loop is always stable as the phase will never cross –180°. Normally the current controller will not be saturated, a limit in the output of the controller is not needed. In case of saturation, the PWM duty δ is 1 and the motor runs with full DC link voltage. In digital control system, the sum of absolute phase currents i_{sum} can be obtained by two current sensors via analog digital converter (ADC), then calculate the third phase current and sum of absolute phase currents i_{sum}. In analog control system, i_{sum} can be obtained by two current sensor and analog operating circuit. In order to reduce sensors and save cost, only one single DC current sensor with saturation compensator during commutation is applicable [44].

In time domain, incremental PI control can be also obtained

$$\Delta\delta = K_{si}\Delta e_i + \frac{K_{si}}{\tau_{si}} e_i \tag{5-11}$$

After continuous time controller is designed, it can be approximated using a digital controller. This design method has the advantages of simple and tools readily available. However there are approximation errors and no guarantee on stability & performance after digital implementation. The digital controller can be designed direct in z-plane. First get the z-transform of plant consider the sample and zero order holder. Then select sample time of inner current loop T according electrical time constant τ_e and select integrate time constant τ_{si} to balance system steady state and transient performance. Lastly the gain of the controller can be determined by root-locus in z-plane.

5.4 Speed Controller

5.4.1 PI controller for the speed loop

The design of PI controller for the speed loop can be also referred from textbook. The current loop of the system is expressed as (5-10). The speed loop for the PM BDCM with PI controller is shown in Fig. 5-6. Where $K_{s\omega}$ is the gain of speed controller, $\tau_{s\omega}$ is the integral time constant, K_ω is the gain of speed sensor. The output of the speed controller is the reference current i^* for current controller. The motor has a limited allowed maximum phase current, so one limit (or saturation) is needed to protect motor. The open loop transfer function of the speed loop is:

$$A_\omega(s) = \frac{K_{s\omega}(1+s\tau_{s\omega})\cdot K\phi\cdot K_\omega}{s\tau_{s\omega}BK_i(1+s/\omega_{ci})(1+s\tau_m)} \tag{5-12}$$

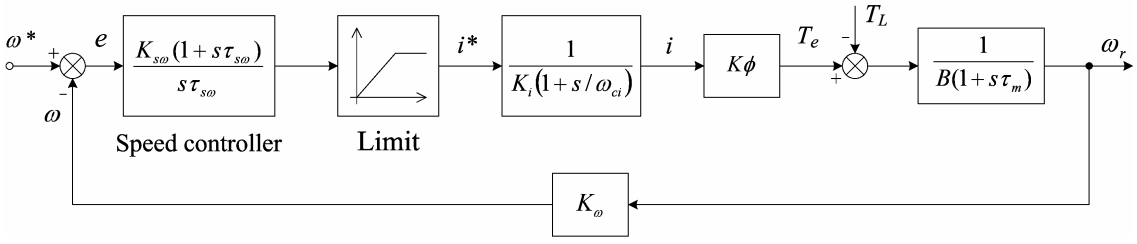


Fig. 5-6. The speed loop for the PM BDCM

The critical frequency of speed loop ω_{cs} should be at least five times smaller than that of current ω_{ci}. With the required critical frequency ω_{cs} and phase margin φ_{cs}, the speed controller parameter $K_{s\omega}$ and $\tau_{s\omega}$ can be determined from open loop transfer function (5-12). As the PI controller is active in case of large error, speed controller parameter $K_{s\omega}$ and $\tau_{s\omega}$ can be selected most for fast response. Overshoot and oscillation will be alleviated by fuzzy controller.

5.4.2 Fuzzy logic controller for the speed loop

PI controller has the advantage of fast response especially during the starting of a motor when the speed error is large and the phase current will reaches maximum rapidly, then the motor can start with maximum acceleration. At the same time the speed controller is saturated and it will not retreat from saturation until the speed error is negative, thus overshoot is inevitable. On the other hand, the response of the controller is conflict with overshoot. When the response of the controller is fast then the overshoot is large. When the overshoot is small, the settling time is long. The PID controller can retreat from saturation beforehand to eliminate overshoot, however, the differential part of the controller is sensitive to disturbance, and the settling time is longer than PI controller. In order to solve these problems, fuzzy logic controller is introduced.

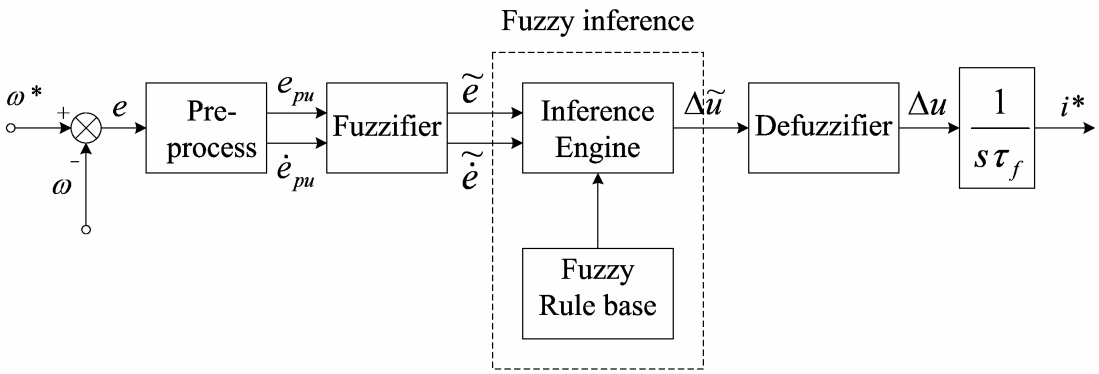


Fig. 5-7. The structure of fuzzy logic controller

The main idea of fuzzy logic control is to use the control ability of human being which includes experience and intuition of experts. It is one of the useful control techniques for uncertain and ill-defined nonlinear systems. Control actions of a fuzzy controller are

described by some linguistic rules. This property makes the control algorithm easy to understand. Heuristic fuzzy controllers incorporate the experience or knowledge into rules. Before the motor will reach desired speed, the controller will reduce the command signal to avoid overshoot. The structure of fuzzy logic controller for PM BDCM is shown in Fig. 5-7.

The input of the fuzzy logic controller is speed error and acceleration error (the differential of speed error). The output of the controller is command increment. The pre-process is used to calculate normalized speed error e_{pu} and acceleration error $\dot{e}_{pu}$, so it is convenient to determine parameter of the fuzzifier. The pre-process can be expressed by:

$$\begin{cases} e = \omega^* - \omega \\ e_{pu} = e / \omega_n \\ \dot{e}_{pu} = de_{pu} / dt \end{cases} \tag{5-13}$$

Where ω_n is the rated motor speed. Then the crisp inputs e_{pu} and $\dot{e}_{pu}$ should be mapped into fuzzy variables $\tilde{e}$ and $\tilde{\dot{e}}$. This process is called fuzzification, the corresponding module is called fuzzifier. A fuzzy variable has linguistic values, for example, LOW, MEDIUM, HIGH which may be defined through triangle, trapezoidal or bell shape membership functions with gradual variation. Triangle shape membership function is introduced here. The membership functions of fuzzy variables $\tilde{e}$ and $\tilde{\dot{e}}$ are shown in Fig. 5-8. Where linguistic value Z, PS, PB, NS and NB means zero, positive small, positive big, negative small and negative big respectively. The membership functions of $\tilde{e}$ and $\tilde{\dot{e}}$ are expressed as:

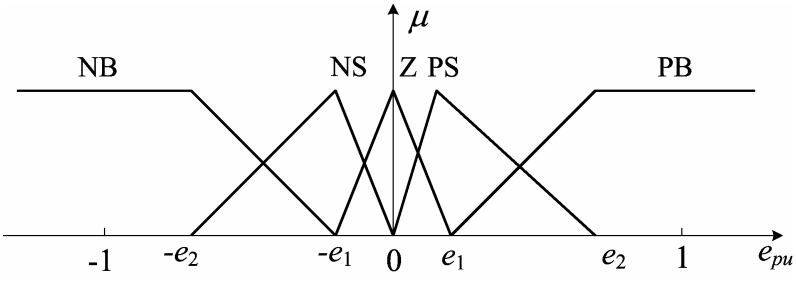
$$\mu_{NB}(e_{pu}) = \begin{cases} 1 & e_{pu} \le -e_2 \\ \dfrac{e_1 + e_{pu}}{e_1 - e_2} & -e_2 < e_{pu} < -e_1 \\ 0 & otherwise \end{cases}$$

$$\mu_{NS}(e_{pu}) = \begin{cases} \dfrac{e_2 + e_{pu}}{e_2 - e_1} & -e_2 < e_{pu} < -e_1 \\ \dfrac{e_{pu}}{e_1} & -e_1 < e_{pu} < 0 \\ 0 & otherwise \end{cases}$$

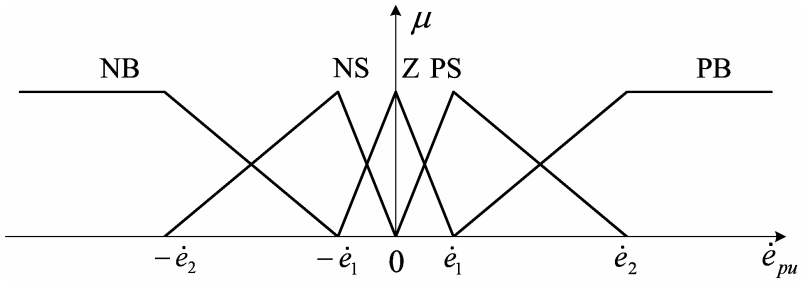
(5-14)

……

$$\mu_{PB}(\dot{e}_{pu}) = \begin{cases} 1 & \dot{e}_{pu} \geq \dot{e}_2 \\ \dfrac{\dot{e}_{pu} - \dot{e}_1}{\dot{e}_2 - \dot{e}_1} & \dot{e}_1 < \dot{e}_{pu} < \dot{e}_2 \\ 0 & otherwise \end{cases}$$



(a) Speed error $\tilde{e}$ membership function



(b) Acceleration error $\tilde{\dot{e}}$ membership function

Fig. 5-8. Membership function of fuzzy input variable

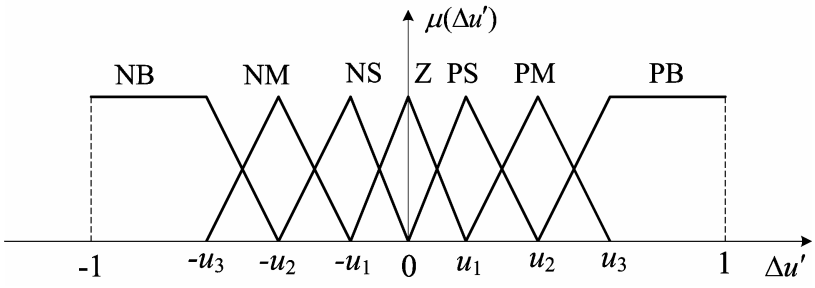


Fig. 5-9. Membership function of fuzzy output variable $\Delta\tilde{u}$

The boundary e_1, e_2, $\dot{e}_1$ and $\dot{e}_2$ can be determined according to the experience and trial in simulation and no rigorous values are required. As the crisp inputs e_{pu} and $\dot{e}_{pu}$ are per unit value, the boundary e_1, e_2, $\dot{e}_1$ and $\dot{e}_2$ can be fixed values. There are also some

methods to determine the membership function, such as: three-phase method, the incremental method, multiphase fuzzy statistical method, absolute comparison method, set-valued statistical iteration method and so on [26].

Table 5-1. The fuzzy rule base

$\tilde{e}$ \ $\dot{\tilde{e}}$	NB	NS	Z	PS	PB
NB	NB	NB	NM	NS	Z
NS	NB	NM	NS	Z	PS
Z	NM	NS	Z	PS	PM
PS	NS	Z	PS	PM	PB
PB	Z	PS	PM	PB	PB

It has mentioned that the fuzzy rule base comes from the experience of experts. The input signals to the controller that the experts can observe are the speed error ($\tilde{e}$) and the change rate of speed error ($\dot{\tilde{e}}$). The output of the experts is to alter the control signal and determines how much the control signal should be altered ($\Delta\tilde{u}$). Then the fuzzy rule base can be deduced as shown on Table 5-1. The output of fuzzy inference is the command (control signal) increment $\Delta\tilde{u}$. Its values is NB, NM, NS, Z, PS, PM and PB. NM means negative medium, PM means positive medium, other values are the same as former. The membership of $\Delta\tilde{u}$ is shown in Fig. 5-9. The boundary u_1, u_2 and u_3 can be also determined according to the experience and trial in simulation. There are $5 \times 5 = 25$ rules, i.e.:

$$\begin{aligned}
&\text{Rule 1:} && \text{IF } \tilde{e} = \text{NB AND } \dot{\tilde{e}} = \text{NB THEN } \Delta\tilde{u} = \text{NB} \\
&&& \cdots\cdots \\
&\text{Rule 5:} && \text{IF } \tilde{e} = \text{PB AND } \dot{\tilde{e}} = \text{NB THEN } \Delta\tilde{u} = \text{Z} \\
&&& \cdots\cdots \\
&\text{Rule 25:} && \text{IF } \tilde{e} = \text{PB AND } \dot{\tilde{e}} = \text{PB THEN } \Delta\tilde{u} = \text{PB}
\end{aligned} \tag{5-15}$$

Rule 1 suggests that when the real speed is greatly more than reference speed ($\tilde{e}$ = NB) while motor speed is still increase greatly ($\dot{\tilde{e}}$ = NB), the control signal should be reduced greatly ($\Delta\tilde{u}$ = NB). Rule 5 suggests that when the real speed is greatly more than

reference speed ($\tilde{e}$ = NB) while motor speed is decreased greatly ($\tilde{\dot{e}}$ = PB), the motor speed is approaching to the reference speed with maximum deceleration, the current control signal is perfect, we need not change it ($\Delta\tilde{u}$ = Z). Other rules can be also interpreted.

Fuzzy inference engine is used to combine the IF-THEN rules and obtain the conclusion for the consequent. Use Mamdami implication [10] for each IF_THEN rule, the output membership of the linguistic value can be got:

$$\begin{aligned}
&\text{Rule 1:} && \mu_{NB1}(\Delta u') = \min\{\mu_{NB}(e_{pu}),\quad \mu_{NB}(\dot{e}_{pu})\} \\
&\text{Rule 2:} && \mu_{NB2}(\Delta u') = \min\{\mu_{NS}(e_{pu}),\quad \mu_{NB}(\dot{e}_{pu})\} \\
&\qquad\cdots\cdots \\
&\text{Rule 25:} && \mu_{PB25}(\Delta u') = \min\{\mu_{PB}(e_{pu}),\quad \mu_{PB}(\dot{e}_{pu})\}
\end{aligned} \tag{5-16}$$

From Table 5-1 we can find that different rules may conclude same linguistic value, e.g. rule 1, 2, 6 get the same linguistic value NB. Then we can set the maximum one as the final membership, e.g. for NB, have

$$\mu_{NB}(\Delta u') = \max\{\mu_{NB1}(\Delta u'), \mu_{NB2}(\Delta u'), \mu_{NB6}(\Delta u')\} \tag{5-17}$$

Thus the fuzzy output obtain:

$$\Delta\tilde{u} = \frac{\mu_{NB}(\Delta u')}{NB} + \frac{\mu_{NM}(\Delta u')}{NM} + \frac{\mu_{NS}(\Delta u')}{NS} + \frac{\mu_{Z}(\Delta u')}{Z} + \frac{\mu_{PS}(\Delta u')}{PS} + \frac{\mu_{PM}(\Delta u')}{PM} + \frac{\mu_{PB}(\Delta u')}{PB} \tag{5-18}$$

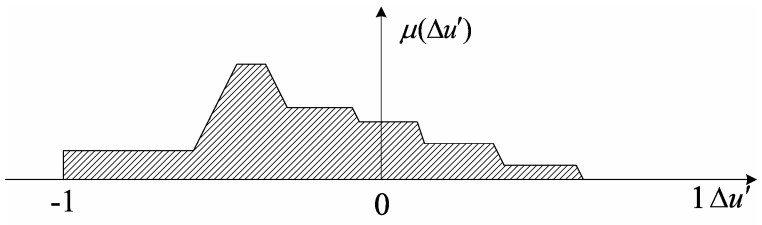


Fig. 5-10. Output of fuzzy controller $\Delta\tilde{u}$

The output of the inference engine is fuzzy variable in the form as shown in Fig. 5-10. The fuzzy logic controller must convert its internal fuzzy variable into crisp value so that the actual system can use the command signal. This conversion is called defuzzification.

One of the commonly used methods for defuzzification is center of area (COA) method. COA method is to get the centroid of each membership function for each output linguistic value. Then the crisp output command increment Δu is expressed as:

$$\Delta u = \frac{\int_{-1}^{1} \mu(\Delta u')\Delta u' d\Delta u'}{\int_{-1}^{1} \mu(\Delta u') d\Delta u'} \tag{5-19}$$

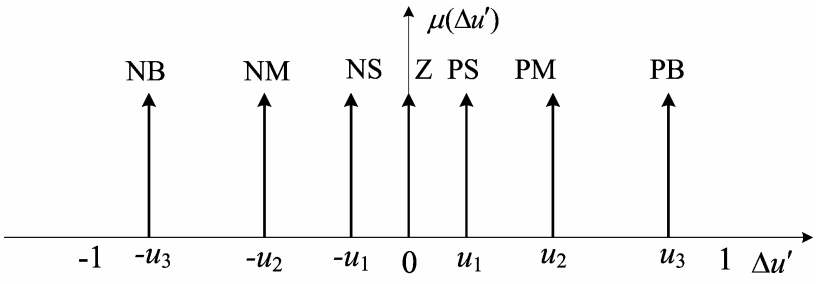


Fig. 5-11. Output variable $\Delta\tilde{u}$ membership function with crisp value

To simplify the defuzzification, the membership function of output variable $\Delta\tilde{u}$ can be crisp value [97] as shown in Fig. 5-11. Then defuzzification is simplified as:

$$\Delta u = \frac{\sum_{i=1}^{7} \mu_i(\Delta u')\Delta u_i'}{\sum_{i=1}^{7} \mu_i(\Delta u')} = \frac{u_1[\mu_{PS}(\Delta u') - \mu_{NS}(\Delta u')] + u_2[\mu_{PM}(\Delta u') - \mu_{NM}(\Delta u')] + u_3[\mu_{PB}(\Delta u') - \mu_{NB}(\Delta u')]}{\mu_{NB}(\Delta u') + \mu_{NM}(\Delta u') + \mu_{NS}(\Delta u') + \mu_Z(\Delta u') + \mu_{PS}(\Delta u') + \mu_{PM}(\Delta u') + \mu_{PB}(\Delta u')} \tag{5-20}$$

Integrating the command increment, the reference current i^* is obtained (Fig. 5-7), where τ_f is integration time constant. The value of τ_f is determined by the response speed, load current. For fuzzy logic control, it is hard to obtain analytical equation of τ_f. It can only be obtained by trial and experience. However, a wide range of τ_f is applicable to the control system.

5.4.3 Switching controller

The objective of the hybrid controller is to utilize the advantages of the PI and fuzzy controllers to provide better response than one controller only. The combined speed

controller is shown in Fig. 5-12. The controller selection signal *sel* is determined by absolute speed error $|e|$ with hysteresis:

$$sel(n)=\begin{cases}0 & |e|\le e_l \\ 0 & e_l<|e|\le e_h \quad sel(n-1)=1 \\ 1 & otherwise\end{cases} \tag{5-21}$$

Thresholds e_l and e_h (with $e_h > e_l$) can be determined by user, a wide range of e_l and e_h can be selected. When the *sel* is "1", speed error is big, switch *K* is turned on, multiplexer MUX selects $K_{s\omega}e/\tau_{s\omega}$ to the integrator, thus PI controller is active; when the *sel* is "0", speed error is small, switch *K* is turned off, MUX selects fuzzy controller output command increment Δu to the integrator, thus fuzzy controller is active. Fuzzy logic controller and PI controller can use the same integrator. When the controller is switched between PI controller and fuzzy logic controller, the step command signal is $K_{s\omega}e$, i.e. when the controller is switched from fuzzy to PI, command signal will step up $K_{s\omega}e$, vice versus. During the motor starting, PI controller will be saturated soon, when the controller is switched from PI to fuzzy logic controller, the step down command signal $K_{s\omega}e$ will help the controller to retreat from saturation to avoid overshoot. When the controller is required from fuzzy logic to PI, it means that the motor speed is deviated from reference speed and the controller should increase command signal greatly, the step up command signal $K_{s\omega}e$ just does it.

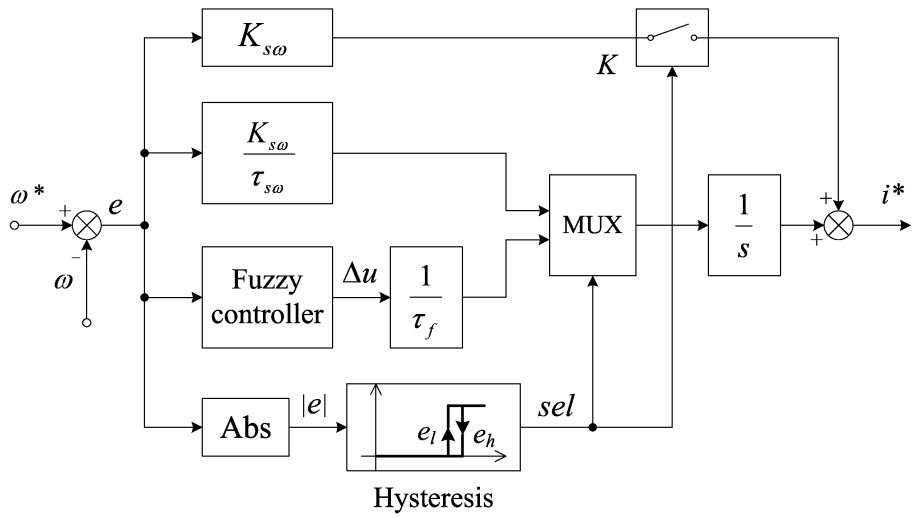


Fig. 5-12. Switching speed controller

5.5 Implementation and Experimental Results

5.5.1 Structure of the experimental system

The structure of PM BDCM drive system for experiment is illustrated in Fig. 5-13 which comprises: diode bridge rectifier, three phase full wave inverter, motor, digital signal processor (DSP), user interface, sensor, commutation logic circuit and gate drive. The motor is a 3.3 hp 3000 rpm three-phase PM BDCM. The BDCM is equipped with a Hall-effect sensor and an incremental optical encoder. The Hall-effect sensor indicates which of the three phases of the motor should be excited as the motor runs. The optical incremental encoder with resolution of 512 pulses/revolution is used to give speed feedback. The optical encoder has been introduced in Chapter 2, Section 2.2.2. As only speed feedback is needed, no index pulse is required.

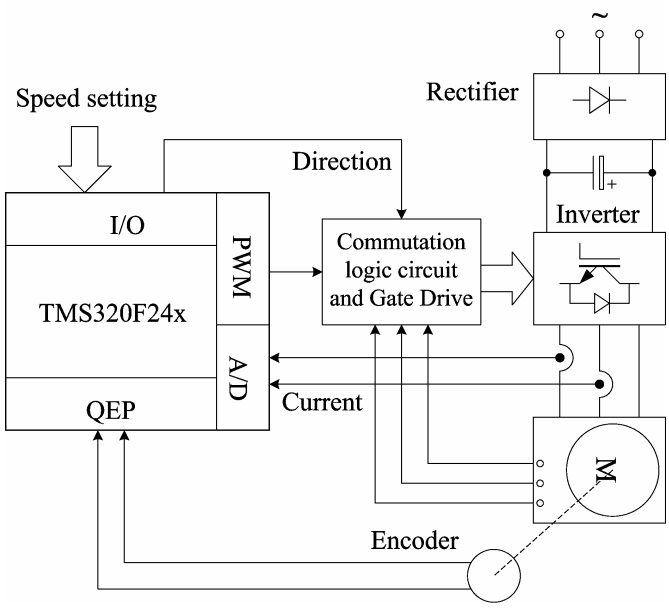


Fig. 5-13. Structure of the experimental system

The control algorithm is implemented by software and executed by the DSP. The control software is written and loaded into the DSP using a PC. User interface is one key panel and LED display to set the reference speed. User interface can be also implemented by PC software which communicates with DSP via serial communication RS-232. The inputs to the commutation logic circuit are the three Hall sensor signals, the direction of desired rotation and PWM. The commutation logic circuit determines which switches should be turned on. The output of the commutation logic circuit is gate signals which

feed the power semiconductor switches of the inverter via gate driver circuit. The commutation logic circuit and gate driver circuit have been described in Chapter 2.

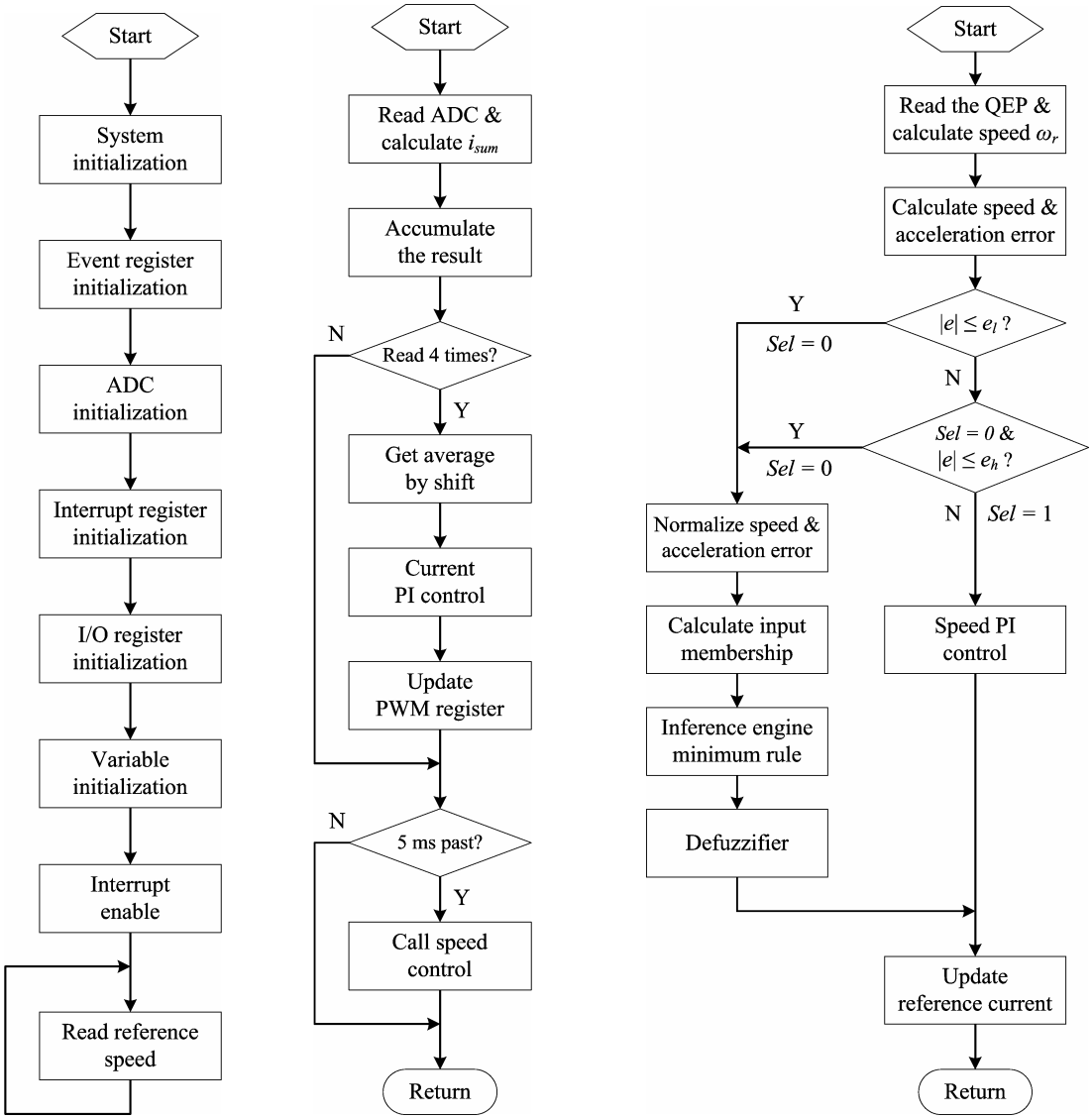
The DSP used in the controller is TMS320F2407 which is special designed for power electronics and electric drive. The on-chip memory system includes 16k words (16bits) program flash E^2PROM, 544 words data/program dual access RAM. The chip also comprises dual 10 bits 16 channel ADCs, serial communication interface (SCI), event manager, digital I/O and other modules. The event manager includes PWM channels, quadrature encoder pulse (QEP) circuit, capture unit, timer and so on. As PWM signal can be generated by the DSP, triangular wave generator and comparator are not required any more. The output of the incremental optical encoder can feed the QEP of the DSP directly. Capture unit can detect both edge of a square wave and measure its width. Dual on-chip ADC can accept two current sensor signals. Only one DC path current sensor is also applicable to reduce cost and to be set up conveniently [1]. The DSP can also accept reference speed signal from other processor via SCI.

5.5.2 Software introduction

The control algorithm is implemented by software and executed by the DSP. The flowchart of the software is shown in Fig. 5-14 which includes main routine, timer T1 interrupt service routine and speed control subroutine.

The flowchart of main routine is shown in Fig. 5-14(a). System initialization is executed first which includes system and output clock setting, sign extension mode setting, overflow mode settings and watchdog setting. In event register initialization, timer, PWM unit, event interrupt register, capture unit will be set. The period of timer T1 will be set to be 50μs, the timer also acts as time base of PWM unit, thus the switching frequency is 20kHz. Timer T2 and T3 are cascaded into a 32-bit timer for QEP circuit to measure the motor speed. There are four capture units in the DSP, capture 1 and capture 2 are combined as QEP circuit. The DSP comprises dual 10 bits 16 channel ADCs. As there are only two phase currents should be measured by ADC, one phase current is allocated one ADC to simplify the software. The ADCs are also set to be started by timer T1 event, thus the phase current is measured every 50μs (The conversion time for ADC is about 6μs).

Timer T1 period interrupt is enabled, the event interrupt is belong to interrupt 2 which should be also enabled, the corresponding register is set. Shared I/O registers are also set to read reference speed. Interrupt is enabled after all the initialization is complete. Then the main routine read the reference speed all the time, the main routine will be paused if the interrupt service routine is being executed.



(a) Main routine (b) Timer T1 interrupt routine (c) Speed control subroutine

Fig. 5-14. Flowchart of software

The flowchart of timer T1 interrupt service routine is shown in Fig. 5-14(b). The routine can read two phase currents from ADC data register, then calculate i_{sum} as

$$i_{sum} = \left|i_a - I_{offset}\right| + \left|i_b - I_{offset}\right| + \left|2I_{offset} - i_a - i_b\right| \tag{5-22}$$

Where I_{offset} is current offset. As the ADC in DSP can only accept positive voltage signal (0~5V), phase current i_a and i_b are added I_{offset} first to satisfy the ADC. The winding of the motor is Y-configured, phase current i_c can be calculated from i_a and i_b. To alleviate the measure noise, i_{sum} is averaged every four data. Division by 4 can be replaced by right shift 2 bits. Incremental PI regulation for current will be executed every 200μs. Incremental PI algorithm has the advantages of avoiding error accumulation and less memory is needed. The output of the current PI controller is duty cycle δ of PWM. The sample period of speed controller is 5ms, thus speed control subroutine is called every 100 times of timer T1 interrupt.

The flowchart of speed control subroutine is shown in Fig. 5-14(c). In the subroutine, the count in the cascaded 32-bit timer of T2 and T3 is read first to calculate the current speed ω_r. Then the speed error e and derivative of the speed error $\dot{e}$ are also determined. The controller selection signal *sel* can be determined from speed error according to Equation (5-21). When the *sel* is 0, fuzzy logic controller is selected, otherwise PI controller is selected. In fuzzy logic controller, speed error e and its derivative $\dot{e}$ are normalized first to get their per unit value e_{pu} and $\dot{e}_{pu}$. Then the membership of input will be determined. From the figure of membership function (Fig. 5-8) we can see that there are only two linguistic values are nonzero at most for each input. One algorithm to obtain membership of speed error can be:

```
Define variables Eind1 and Eind2 to save nonzero linguistic name
for speed error;                    /* 0 -- NB  1 -- NS  2 – Z  3 -- PS  4 -- PB */

Define variables Emb1 & Emb2 to save possible nonzero speed error
membership and initial with zero;          /* member2 may be zero */

Store absolute value of speed error to variable absError;

if (absError < e1)                         /* e1 is the boundary
{
     Eind1 = 3; Eind2 = 2;                 /* PS and Z are nonzero value */
     Emb1 = absError / e1;                 /* calculate membership */
     Emb2 = 1 – Emb1;
}
else
```

```
{
      Eind1 = 4; Eind2 = 3;            /* PB and PS are possible nonzero value */
      if (absError < e2)                     /* e2 is also the boundary
      {
            Emb1 = (absError - e1) / (e2 - e1);
            Emb2 = 1 - Emb1;                 /* calculate membership */
      }
      else
      {
            Emb1 = 1; Emb2 = 0;              /* PB is maximum, PS is zero */
      }
}

if (speed error < 0)
{
      /* PB -> NB, PS -> NS, Z has no changed */
      Eind1 = 4 - Eind1;  Eind2 = 4- Eind2;
}
```

The algorithm to determined membership of acceleration error is similar to that of speed error. This algorithm has less CPU load, the variables defined in the algorithm are also convenient for inference. As there are only two linguistic values are nonzero at most for each input, only four rules at most will be invoked as shown in Table 5-1 and contribute to the output. One algorithm of inference with Mamdami implication can be:

```
/* Variables to save nonzero linguistic name for acceleration error is dEind1 and dEind2, Variables
to save nonzero membership for acceleration error is dEmb1 and dEmb2. */
Define array Omb[7] to save output membership & initial with zero;

index = (Eind1 left shift 3 bits) + dEind1; /* index = Eind1 × 8 + dEind1 */
ptr = RuleTable[index];
Omb[ptr] = min(Emb1, dEmb1);

index = (Eind1 left shift 3 bits) + dEind2; /* index = Eind1 × 8 + dEind2 */
ptr = RuleTable[index];
if (Omb[ptr] <= min(Emb1, dEmb2))
{
      Omb[ptr] = min(Emb1, dEmb2);             /* Maximum value */
}
```

```
. . . . . .
/* The same for group (Eind2, Emb2, dEind1, dEmb1) and (Eind2, Emb2, dEind2, dEmb2) */

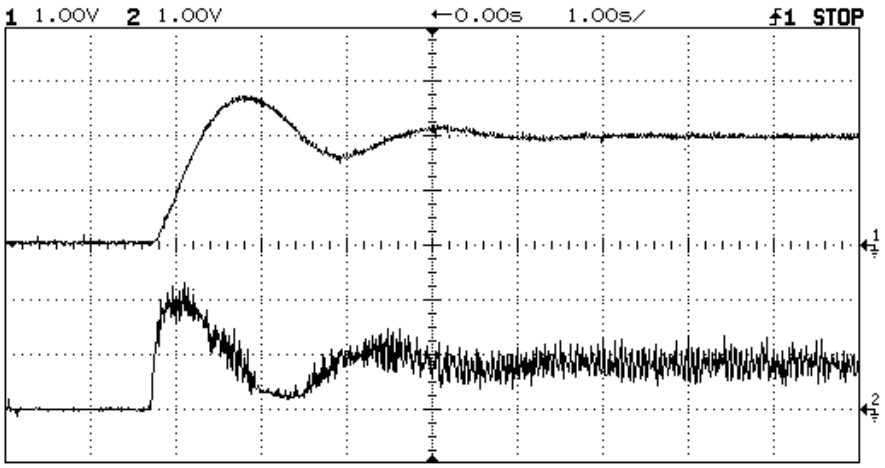
RuleTable
/* Output linguistic 0 - NB, 1 - NM, 2 - NS, 3 - Z, 4 - PS, 5 - PM, 6 – PB, 0FFH is padding */
    0       0       1       2       3       0FFH    0FFH    0FFH
    0       1       2       3       4       0FFH    0FFH    0FFH
    1       2       3       4       5       0FFH    0FFH    0FFH
    2       3       4       5       6       0FFH    0FFH    0FFH
    3       4       5       6       6       0FFH    0FFH    0FFH
```

This algorithm has also less CPU load. Then with Equation (5-20), command increment Δu can be obtained. Lastly the subroutine updates the reference current. Detail can be referenced from source code in Appendix G.

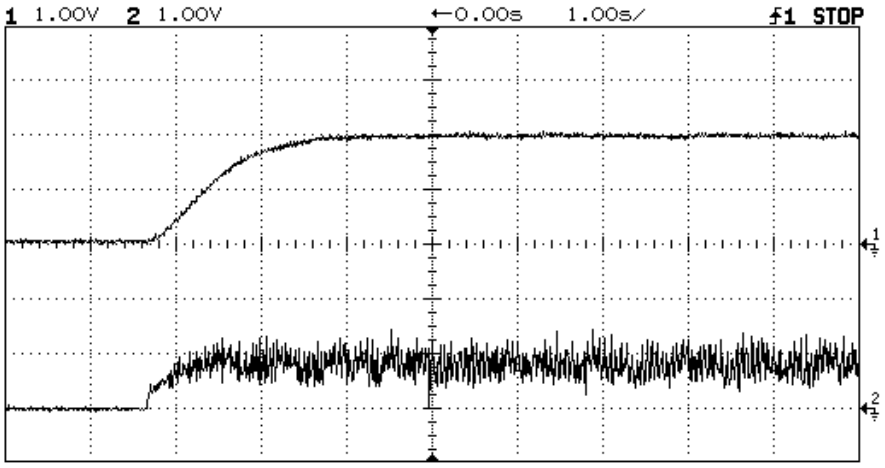
5.5.3 Experimental results

The switching frequency is 20 kHz. The phase current is sampled every 50μs, the speed is measured every 5ms. The integration time constant for fuzzy controller τ_f is 3.5ms, threshold for switching controller e_l and e_h is 15% ω_n and 20% ω_n respectively. The boundary of the membership function of the fuzzy variable e_1, e_2, $\dot{e}_1$, $\dot{e}_2$, u_1, u_2 and u_3 is 0.1, 0.3, 0.5, 1.8, 0.1, 0.3 and 0.6 respectively. The parameter of the PI speed controller $K_{s\omega}$ and $\tau_{s\omega}$ is 15 and 28.7ms respectively, the parameter PI current controller K_{si} and τ_{si} is 2.2 and 3.075ms respectively. The experimental waveforms are shown in Fig. 5-15. The top waveform of each capture figure is motor speed with scale 1000 rpm/div. The bottom waveform is DC link current with scale 5A/div. Step speed response with PI controller only, fuzzy controller only, hybrid controller and corresponding DC link current are shown in Fig. 5-15(a), 5-15(b) and 5-15(c) respectively. From these figures we can see that the PI controller is faster response than that of fuzzy controller while there is overshoot and oscillation in PI controller. There is little overshoot and oscillation with fuzzy logic controller. Speed response of PI controller and fuzzy logic controller with impulse load torque are shown in Fig. 5-15(d) and 5-15(e) respectively. Speed response of PI controller and fuzzy logic controller with step load torque are shown in Fig. 5-15(f)

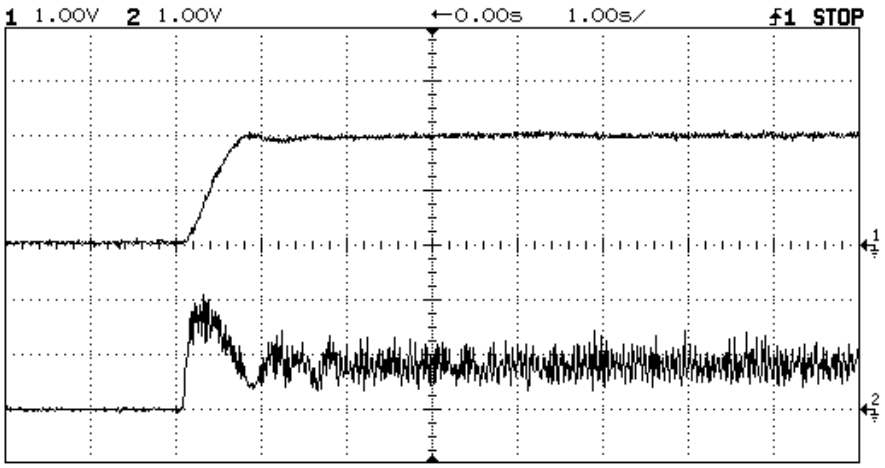
and 5-15(g) respectively. Fuzzy logic controller is more robust than that of PI controller, hybrid controller holds the advantages of the two controllers.



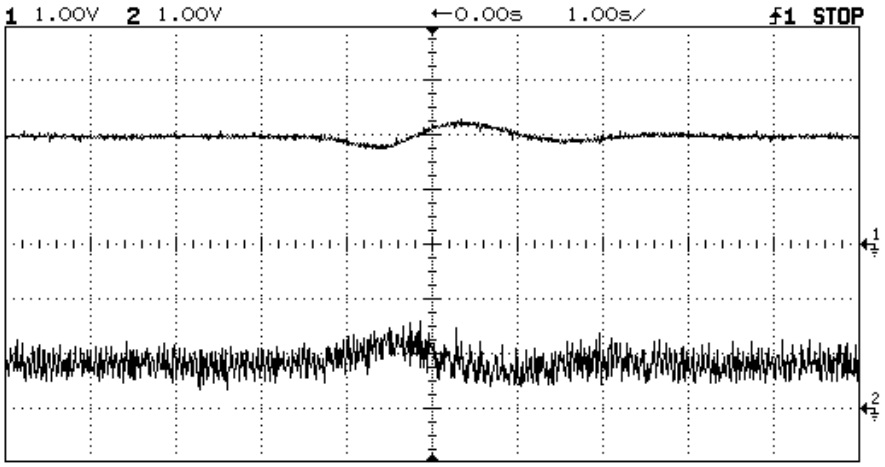
(a) Step speed response with PI controller only and DC link current



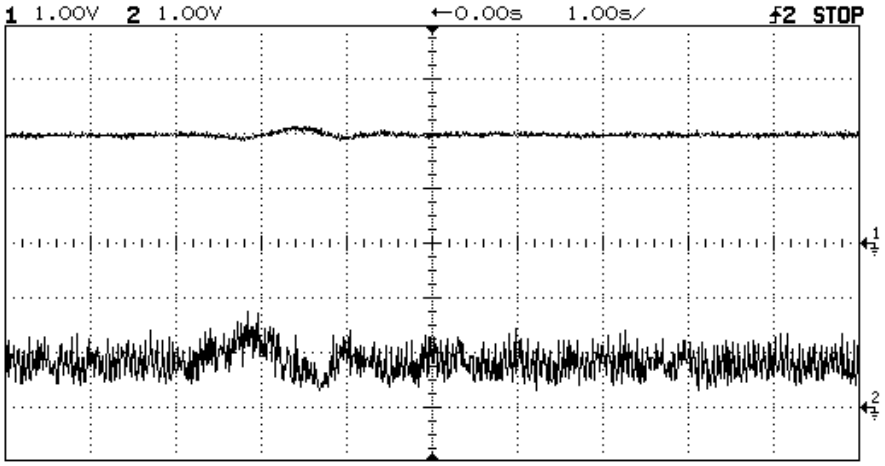
(b) Step speed response with fuzzy controller only and DC link current



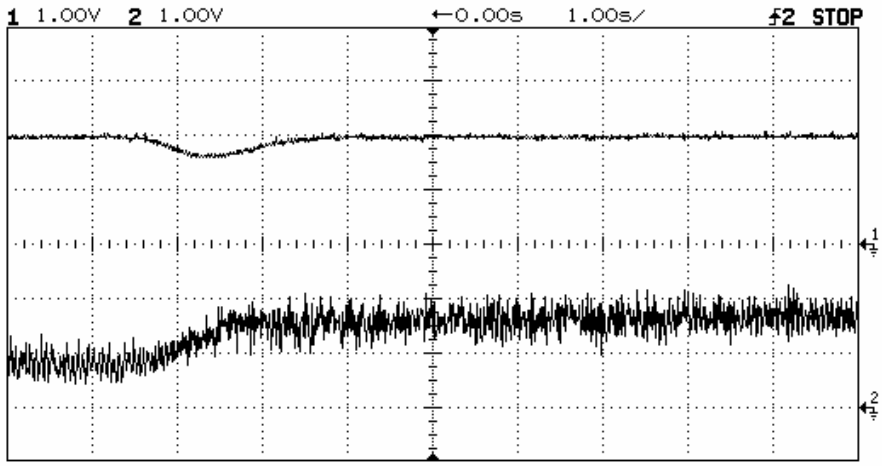
(c) Step speed response with hybrid controller and DC link current



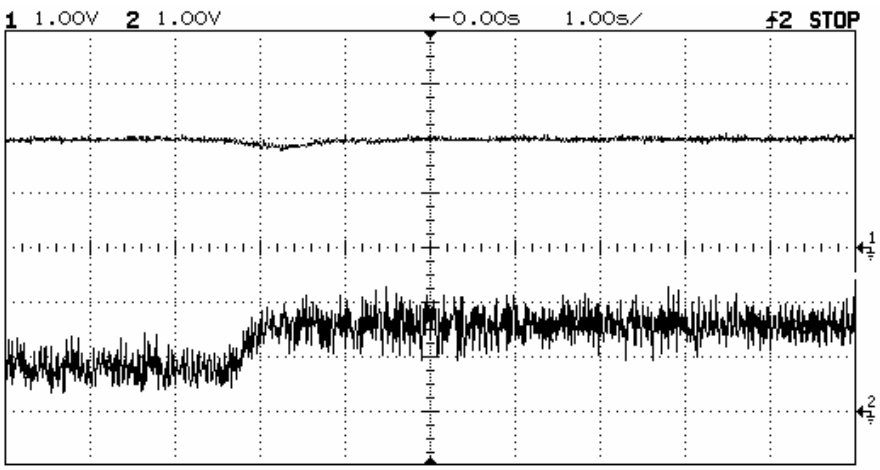
(d) Speed response of PI controller with impulse load torque and DC link current



(e) Speed response of fuzzy controller with impulse load torque and DC link current



(f) Speed response of PI controller with step load torque and DC link current



(g) Speed response of fuzzy controller with step load torque and DC link current

Fig. 5-15. Experimental waveforms of speed response and DC link current under PI controller only, fuzzy controller only and hybrid controller

5.6 Summary

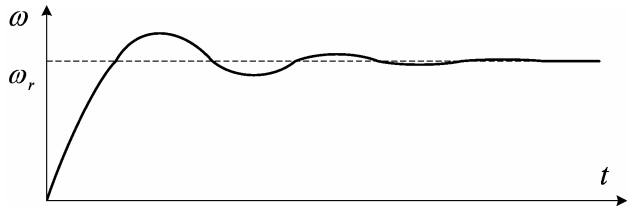
A hybrid controller for the PM BDCM drive system is proposed which holds the advantages of both PI controller and fuzzy controller, i.e. fast response, little overshoot, little oscillation, robust to system parameters variation, stability and so on. The design of the controller is proposed. Hardware implementation is described. Experimental results are illustrated. The design of the controller is successful.

Chapter 6 SSRC Prediction Technique

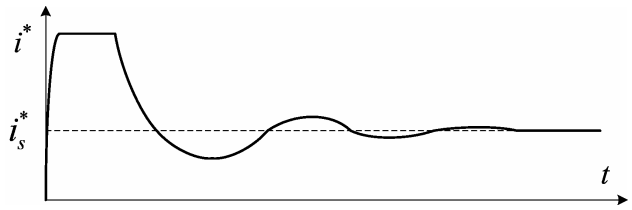
This chapter proposed a Steady State Reference Current (SSRC) prediction technique based on neural network for PM BDCM drive system. Conventional controller that combines this technique holds the advantages of fast response, little overshoot, robust and so on. The prediction technique is described in detail. Hardware implementation and software flowchart are proposed and experimental results are illustrated. The drive system is tested under PI controller and fuzzy controller. The performance is improved greatly.

6.1 Introduction

A variable speed DC (or brushless DC) motor drive system is normally controlled by a speed/current double closed-loop controller. Typical speed and current curve of the drive system is shown in Fig. 6-1. Where ω_r is reference speed, i_s^* is Steady State Reference Current (SSRC). During starting, the current (torque) reaches its maximum value quickly, which contributes to the fast response of the system as the motor runs with maximum acceleration. When the motor reaches desired speed, the current can not be reduced to its steady state value immediately. Normally it is still at maximum value and needs time to settle. Normally, speed overshoot and oscillation are inevitable, and the settling time is as long as multiple the starting time. Ideal speed and current curve are shown in Fig. 6-2. Current reaches its maximum value immediately during starting. When the motor reaches desired speed, the current can skip to its steady state value at the same time and the motor runs at the desired speed. Thus the settling time is shortest as it is only the starting time. Of course, it is hard to achieve ideal starting, however we can try to approach it. Near ideal speed and current curve is shown in Fig. 6-3. When the motor reaches desired speed while the current can not skip to the exact steady state value i_s^* and it can only skips to around the steady state value, there is oscillation too, but the oscillation is smaller than that of conventional control system and the settling time can be reduced greatly, too.

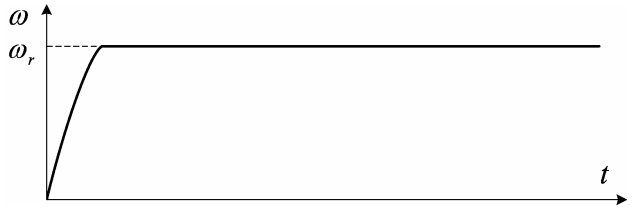


(a) Speed

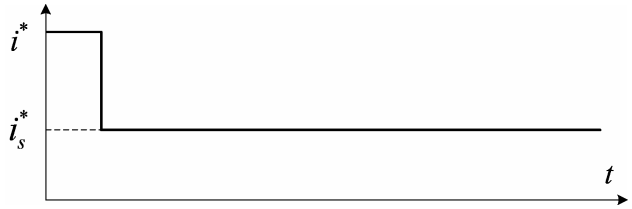


(b) Current

Fig. 6-1. Typical speed and current curve of a DC motor drive system

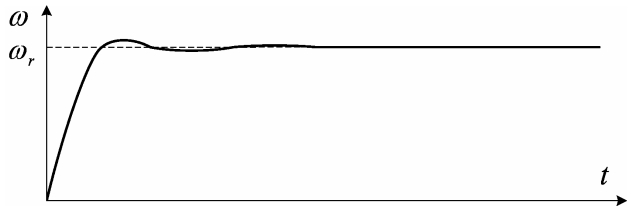


(a) Speed

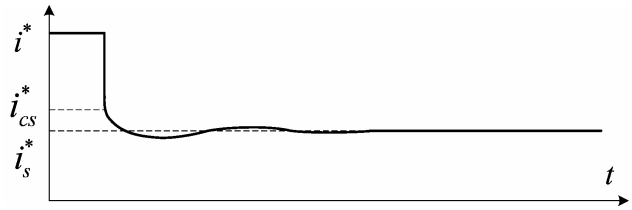


(b) Current

Fig. 6-2. Ideal speed and current curve of a DC motor drive system



(a) Speed



(b) Current

Fig. 6-3. Near ideal speed and current curve of a DC motor drive system

So the key is to determine (predict) the SSRC during starting. An artificial neural network (ANN) [4, 5, 10, 15] is a computational network, consisting of a number of interconnected processing units (neurons), which is able to learn and represent the unknown dependency relationship between a set of input variables and a set of output variables of a system. By selecting the training patterns (acceleration, speed, current, DC link voltage, reference speed) which cover all conditions (i.e. various DC link voltage, various load, various moment of inertia, various reference speed) to train the neural network, the neural network is able to predict the SSRC according to the acceleration, speed, current, DC link voltage, reference speed of the drive system, although the predicted value may be not very accurate.

6.2 The Structure of the System

This chapter introduces a SSRC prediction technique based on neural network for PM BDCM drive system. Conventional controller with this technique holds the advantages of fast response, little overshoot, robust and so on. Short settling time is very important for frequent run/stop drives, e.g. lift, lathe, electric actuator and so on. The structure of the control system is shown in Fig. 6-4. It includes outer speed loop, inner current loop, drive system, sensor and user interface (to set reference speed and other parameter). The outer speed loop comprises conventional controller, SSRC estimator, coarse reference current i_{cr} generator. In case of large speed error the reference current is maximum or minimum current, depending on the polarity of the speed error. When the speed error e is small enough, the reference current skips from extremum to coarse value i_{cs}^{*} which is determined by SSRC estimator. Then the conventional controller is active to fine adjust reference current and control the motor speed to the desired value. The coarse reference current generator is used to determine coarse reference current and active conventional controller according to the speed error e. The expression of the coarse reference current i_{cr} will be proposed later. The conventional controller can be incremental PI controller, fuzzy logic controller or other controller. The inner current loop is a conventional PI controller. The drive system includes rectifier, inverter, motor and mechanical load.

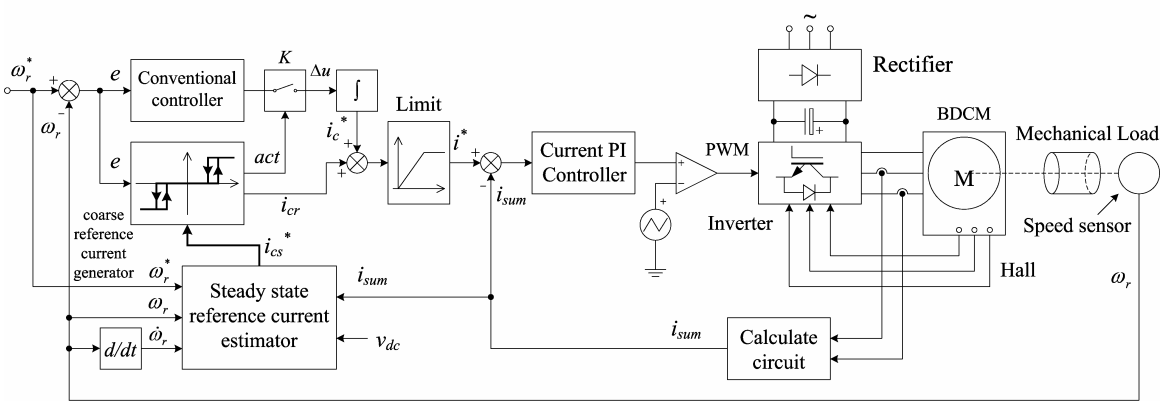


Fig. 6-4. The structure of the control system

PI controller for the current loop, PI and fuzzy logic controller for the speed loop has been introduced in the Chapter 5. SSRC estimator will be described in next section. Coarse reference current generator will be introduced here.

The coarse reference current generator is used to determine coarse reference current and active conventional controller according to the speed error e. The conventional controller active signal act is

$$act(n)=\begin{cases}1 & |e|\le e_l\\ 1 & e_l<|e|\le e_h \quad act(n-1)=1\\ 0 & otherwise\end{cases} \tag{6-14}$$

The coarse reference current i_{cr} is

$$i_{cr}=\begin{cases}I_{\max} & e<0 \quad act(n)=0\\ I_{\min} & e>0 \quad act(n)=0\\ i_{cs}^{*} & act(n)=1\end{cases} \tag{6-15}$$

Thresholds e_l and e_h (with $e_h > e_l$) can be determined by simulation. $I_{\max}$ is allowed continuous maximum current. $I_{\min}$ is minimum current, it maybe a negative value for reverse current braking, otherwise it is zero. i_{cs}^{*} is coarse SSRC which is determined by SSRC estimator. During starting, the absolute of speed error $|e|$ is big, coarse reference current i_{cr} is maximum current $I_{\max}$, and conventional controller is not active. When $|e|$ decreases to smaller than e_l, conventional controller is active and coarse reference current

i_{cr} is i_{cs}^*. After the conventional controller is active, it would not be stopped unless $|e|$ is larger than e_h again.

SSRC estimator will calculate $i_{cs}(n)$ for every sample period. The output for coarse reference current generator i_{cs}^* can be calculated from recent $i_{cs}(n-i)$ with weight; the more recent the value, the larger the weight. For convenient execution in micro-processor, one expression of the calculation can be

$$i_{cs}^* = \frac{1}{P}\sum_{i=0}^{P-1}\sum_{j=0}^{2^i-1}\frac{1}{2^i} i_{cs}\left[n-(2^i+j-1)\right] \tag{6-16}$$

Where P is a natural number. When P is power of 2, all the division operations in Equation (16) can be replaced by right shifting which is fast instruction in micro-processor. For example, if $P = 2^2 = 4$, then current and 14 previous i_{cs} will be calculated, all the divisors are power of 2.

$$\begin{aligned} i_{cs}^* = \frac{1}{4}\Bigg\{ & i_{cs}(n) + \frac{i_{cs}(n-1)+i_{cs}(n-2)}{2} \\ & + \frac{i_{cs}(n-3)+\cdots+i_{cs}(n-6)}{4} + \frac{i_{cs}(n-7)+\cdots+i_{cs}(n-14)}{8}\Bigg\} \end{aligned} \tag{6-17}$$

If P is not power of 2, only one division should be executed.

6.3 Steady State Reference Current Estimator

6.3.1 The architecture of the SSRC estimator

The architecture of SSRC estimator is shown in Fig. 6-5 which is a feed-forward neural network with sigmoid activation function. The neural network comprises input layer, two hidden layers, output layer. The number of input and output nodes corresponds to the number of network inputs and desired outputs, respectively.

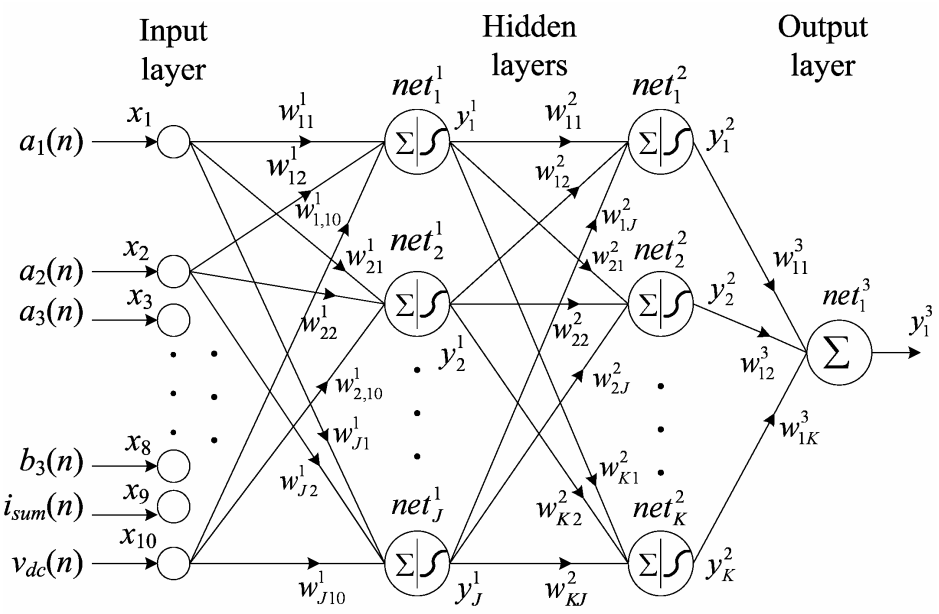


Fig. 6-5. The architecture of SSRC estimator

From Equations (5-4) and (5-6) in Chapter 5 we can get

$$\dot{\omega}_r J + \omega_r B + T_L = K\phi i_{sum} \tag{6-18}$$

Where $\dot{\omega}_r$, ω_r and i_{sum} can be measured from system. For *N* samples, we have

$$\begin{bmatrix} \dot{\omega}_r(n) & \omega_r(n) & 1 \\ \dot{\omega}_r(n-1) & \omega_r(n-1) & 1 \\ \cdots & \cdots & \cdots \\ \dot{\omega}_r(n-N+1) & \omega_r(n-N+1) & 1 \end{bmatrix} \begin{bmatrix} J \\ B \\ T_L \end{bmatrix} = K\phi \begin{bmatrix} i_{sum}(n) \\ i_{sum}(n-1) \\ \cdots \\ i_{sum}(n-N+1) \end{bmatrix} \tag{6-19}$$

When *N*>3, Equation (6-19) has no accurate solution, but we can get the least squares solution by left multiply coefficient matrix

$$\begin{bmatrix} \sum_{i=0}^{N-1}\dot{\omega}_r^2(n-i) & \sum_{i=0}^{N-1}\dot{\omega}_r(n-i)\omega_r(n-i) & \sum_{i=0}^{N-1}\dot{\omega}_r(n-i) \\ \sum_{i=0}^{N-1}\dot{\omega}_r(n-i)\omega_r(n-i) & \sum_{i=0}^{N-1}\omega_r^2(n-i) & \sum_{i=0}^{N-1}\omega_r(n-i) \\ \sum_{i=0}^{N-1}\dot{\omega}_r(n-i) & \sum_{i=0}^{N-1}\omega_r(n-i) & 1 \end{bmatrix} \begin{bmatrix} J \\ B \\ T_L \end{bmatrix} = K\phi \begin{bmatrix} \sum_{i=0}^{N-1}\dot{\omega}_r(n-i)i_{sum}(n-i) \\ \sum_{i=0}^{N-1}\omega_r(n-i)i_{sum}(n-i) \\ \sum_{i=0}^{N-1}i_{sum}(n-i) \end{bmatrix} \tag{6-20}$$

Define the coefficient as

$$x_1(n) = a_1(n) = \sum_{i=0}^{N-1} \dot{\omega}_r^2(n-i) \tag{6-21}$$

$$x_2(n) = a_2(n) = \sum_{i=0}^{N-1} \omega_r^2(n-i) \tag{6-22}$$

$$x_3(n) = a_3(n) = \sum_{i=0}^{N-1} \dot{\omega}_r(n-i)\omega_r(n-i) \tag{6-23}$$

$$x_4(n) = a_4(n) = \sum_{i=0}^{N-1} \dot{\omega}_r(n-i) \tag{6-24}$$

$$x_5(n) = a_5(n) = \sum_{i=0}^{N-1} \omega_r(n-i) \tag{6-25}$$

$$x_6(n) = b_1(n) = \sum_{i=0}^{N-1} \dot{\omega}_r(n-i) i_{sum}(n-i) \tag{6-26}$$

$$x_7(n) = b_2(n) = \sum_{i=0}^{N-1} \omega_r(n-i) i_{sum}(n-i) \tag{6-27}$$

$$x_8(n) = b_3(n) = \sum_{i=0}^{N-1} i_{sum}(n-i) \tag{6-28}$$

And Equation (5-20) is simplified as

$$\begin{bmatrix} a_1(n) & a_3(n) & a_4(n) \\ a_3(n) & a_2(n) & a_5(n) \\ a_4(n) & a_5(n) & 1 \end{bmatrix} \begin{bmatrix} J \\ B \\ T_L \end{bmatrix} = K\phi \begin{bmatrix} b_1(n) \\ b_2(n) \\ b_3(n) \end{bmatrix} \tag{6-29}$$

In steady state, reference current (output torque) is related to ω_r, B, T_L, thus reference rotor speed ω_r^*, $a_1(n)$, $a_2(n)$, $a_3(n)$, $a_4(n)$, $a_5(n)$, $b_1(n)$, $b_2(n)$ and $b_3(n)$ are selected as input for the neural network. DC link voltage $v_{dc}(n)$ will affect the phase commutation in brushless DC motor, it is another factor to affect SSRC, so $v_{dc}(n)$ is also one input for the neural network. The input data also implicate speed error e and acceleration error $\dot{e}$. Neural network requires that its input and output data should be normalized to have the same order of magnitude. If the input data are not of the same order of magnitude, some input may appear to be more significant than they actually do. The training algorithm has to compensate for order-of-magnitude differences by adjusting the network weights, which is not very effective in some training algorithms such as back propagation algorithm. In addition, typical activation functions, such as a sigmoid function, or a

hyperbolic tangent function, cannot distinguish between two large values, because both yield identical threshold output values of 1.0. Normalize input data can be.

$$\omega_r(n) = \omega_r(n) / \omega_R \tag{6-30}$$

$$\dot{\omega}_r(n) = \dot{\omega}_r(n) / \dot{\omega}_{\max} \tag{6-31}$$

$$i_{sum}(n) = i_{sum}(n) / 2I_R \tag{6-32}$$

$$\omega_r^* = \omega_r^* / \omega_R \tag{6-33}$$

$$v_{dc}(n) = v_{dc}(n) / V_R \tag{6-34}$$

Where ω_R is rated rotor speed, I_R is rated phase current, V_R is rated voltage, $\dot{\omega}_{\max}$ is possible maximum acceleration.

The choice of the number of hidden layers and the nodes in each hidden layer depends on the network application. In general, adding a second hidden layer improves the network prediction capability due to the nonlinear separability property of the network. Although using a single hidden layer is sufficient for solving many functional approximation problems, some problems may be easier to solve with a two hidden layer configuration [5]. So two hidden layers network is employed here. The number of neurons was chosen on a trial-and-error basis. The activation function of neurons in the hidden layers is sigmoid function, as

$$f(x) = \frac{1}{1+e^{-x}} \tag{6-35}$$

For the j^{th} node in the 1st hidden layer, the input net_j^1 (j = 1, 2, …, J) (J is the number of neurons in the 1st hidden layer) and output y_j^1 of the neuron are represented, respectively, as

$$net_j^1(n) = \sum_{i=1}^{10} w_{ji}^1(n) x_i(n) \tag{6-36}$$

$$y_j^1(n) = f(net_j^1(n)) = \frac{1}{1+e^{-net_j^1(n)}} \tag{6-37}$$

Where w_{ji}^1 is the weight between the j^{th} node in the 1st hidden layer and the i^{th} node in the input layer. For the k^{th} node in the 2nd hidden layer, the input net_k^2 (k = 1, 2, …, K) (K is the number of neurons in the 2nd hidden layer) and output y_k^2 of the neuron are represented, respectively, as

$$net_k^2(n) = \sum_{j=1}^{J} w_{kj}^2(n) net_j^1(n) \tag{6-38}$$

$$y_k^2(n) = f(net_k^2(n)) = \frac{1}{1+e^{-net_k^2(n)}} \tag{6-39}$$

Where w_{kj}^2 is the weight between the k^{th} node in the 2nd hidden layer and the j^{th} node in the 1st hidden layer. There is only one neuron in the output layer, the activation function is linear function. The input net_1^3 and output y_1^3 of the neuron are represented as

$$y_1^3(n) = net_1^3(n) = \sum_{k=1}^{K} w_{1k}^3(n) net_k^2(n) \tag{6-40}$$

Where w_{1k}^3 is the weight between the k^{th} node in the 2nd hidden layer and the only one neuron in the output layer. The output of the neuron y_1^3 is just the coarse SSRC $i_{cs}(n)$ mentioned formerly.

6.3.2 Training the neural network

Back propagation (BP) algorithm [4, 5, 10, 15, 85] is one of the most popular algorithms for training a network due to its success from both simplicity and applicability viewpoints. The algorithm consists of two phases: Training phase and recall phase. In the training phase, first, the weights of the network are randomly initialized. Then, the output of the network is calculated and compared to the desired value. The error of the network is calculated and used to adjust the weights of the output layer. In a similar fashion, the network error is also propagated backward and used to update the weights of the previous layers. There are two different methods of updating the weights. In the first method, weights are updated for each of the input patterns using an iteration method. In the second method, an overall error for all the input output patterns of training sets is calculated. In

other words, either each of the input patterns or all of the patterns together can be used for updating the weights. First method of updating weights will be adopted here. The training phase will be terminated when the error is less than the minimum set value provided by the designer. One of the disadvantages of back propagation algorithm is that the training phase is very time consuming. If the training is implemented off-line by a PC, the time consumption is not important. During the recall phase, the network with the final weights resulting from the training process is employed. Therefore, for every input pattern in this phase, the output will be calculated using both linear calculation and nonlinear activation functions. The process provides a very fast response of the network in the recall phase, which is one of its important advantages and it can be executed by a fixed-point micro-processor.

To describe the back propagation algorithm, first the energy function E is defined as

$$E = \frac{1}{2}\left[i_s^* - y_1^3(n)\right]^2 \tag{6-41}$$

Where i_s^* is the desired SSRC. Minimizing energy function leads to a sequence of updating weight which starting from output layer, then backward. The weights of the interconnections between the two adjacent layers can be updated based on the following formula

$$w(n+1) = w(n) - \eta \frac{\partial E}{\partial w(n)} \tag{6-42}$$

Where η is learning rate of the network, $\partial E / \partial w(n)$ is the local gradient. Between the output layer and the second hidden layer, for weight $w_{1k}^3(n)$ the local gradient descent of energy function can be obtained from Equations (6-40) and (6-41)

$$\frac{\partial E}{\partial w_{1k}^3(n)} = \left[i_s^* - y_1^3(n)\right]\frac{\partial y_1^3(n)}{\partial w_{1k}^3(n)} = y_k^2(n)\left[i_s^* - y_1^3(n)\right] \tag{6-43}$$

The derivative of activation function (6-35) is

$$f'(x) = f(x)[1 - f(x)] \tag{6-44}$$

Then between the second hidden layer and the first hidden layer, for weight $w_{kj}^2(n)$, to get the local gradient of energy function, apply chain-rule

$$\frac{\partial E}{\partial w_{kj}^2(n)} = \frac{\partial E}{\partial y_1^3(n)} \cdot \frac{\partial y_1^3(n)}{\partial y_k^2(n)} \cdot \frac{\partial y_k^2(n)}{\partial net_k^2(n)} \cdot \frac{\partial net_k^2(n)}{\partial w_{kj}^2(n)} \tag{6-45}$$

From Equations (6-38) ~ (6-40), (6-41) and (6-44) obtain

$$\frac{\partial E}{\partial w_{kj}^2(n)} = \left[i_s^* - y_1^3(n)\right] w_{1k}^3(n)\, y_k^2(n)\left[1 - y_k^2(n)\right] y_j^1(n) \tag{6-46}$$

Between the first hidden layer and the input layer, for weight $w_{ji}^1(n)$ similarly apply chain-rule

$$\frac{\partial E}{\partial w_{ji}^1(n)} = \frac{\partial E}{\partial y_1^3(n)} \sum_{k=1}^{K} \frac{\partial y_1^3(n)}{\partial y_k^2(n)} \cdot \frac{\partial y_k^2(n)}{\partial net_k^2(n)} \cdot \frac{\partial net_k^2(n)}{\partial y_j^1(n)} \cdot \frac{\partial y_j^1(n)}{\partial net_j^1(n)} \cdot \frac{\partial net_j^1(n)}{\partial w_{ji}^1(n)} \tag{6-47}$$

From Equations (6-36) ~ (6-40), (6-41) and (6-44) the local gradient of energy function is obtained

$$\frac{\partial E}{\partial w_{ji}^1(n)} = \left[i_s^* - y_1^3(n)\right] y_j^1(n)\left[1 - y_j^1(n)\right] x_i(n) \sum_{k=1}^{K} w_{1k}^3(n)\, y_k^2(n)\left[1 - y_k^2(n)\right] w_{kj}^2(n) \tag{6-48}$$

Another problem of back propagation algorithm is local minima. One suggested solution is momentum technique[68] which includes addition of first and second moments to the learning phase. In such an approach, the network memorizes its previous adjustment, and, therefore it will escape the local minima. A new term can be added to Equation (6-42)

$$w(n+1) = w(n) - \eta \frac{\partial E}{\partial w(n)} + \alpha \Delta w(n) \tag{6-49}$$

Where α is the momentum gain, $\Delta w(n)$ is the weight change in the previous iteration.

An important factor is that the training set should be comprehensive and cover all the practical areas of applications of the network. Therefore, the proper selection of the training sets is critical to the good performance of the network. For brushless DC motor drive system, SSRC is determined for given DC link voltage, reference speed, load torque,

moment of inertia. So the selected L sets will cover variable DC link voltage, load, reference speed, moment of inertia. For one set, measure and record DC link voltage and reference speed first, then run the motor with conventional controller and acquire $M + N$ samples of acceleration $\dot{\omega}_r$, speed ω_r and current i_{sum}, lastly record the desired SSRC i_s^*. These data can be combined to M training patterns for neural network. So there are totally LM training patterns. The pattern selection order to train the neural network is: first pattern of set 1, then first pattern of set 2, …, first pattern of set L, second pattern of set 1, …, second pattern of set L, …, last pattern (M^{th}) of set 1, …, last pattern of set L. If the error is not small enough, train the neural network again with these patterns at the same order again.

6.4 Implementation and Experimental Results

6.4.1 Structure of the experimental system

The structure of PM BDCM drive system for experiment is illustrated in Fig. 6-6 which comprises: diode bridge rectifier, three phase full wave inverter, motor, digital signal processor (DSP), user interface, sensor, commutation logic circuit and gate drive. The motor is a 3.3 hp 3000 rpm 4 pole-pairs three-phase PM BDCM. The BDCM is equipped with a Hall-effect sensor and a tachometer generator (TG). The Hall-effect sensor indicates which windings of the motor should be excited as the motor runs. The tachometer generator is used to give speed feedback. The advantage of adopting a tachometer generator is to get high measured precision in case of low speed and high sampling frequency. The acceleration $\dot{\omega}_r$ is obtained from speed ω_r by an analog differentiator. User interface is one key panel and LED display to set the reference speed. User interface can be also implemented by PC software which communicates with DSP via serial communication RS-232. The inputs to the commutation logic circuit are the three Hall sensor signals, the direction of desired rotation and PWM. The commutation logic circuit determines which switches should be turned on. The output of the commutation logic circuit is gate signals which feed the power semiconductor switches of the inverter via gate driver circuit. The commutation logic circuit and gate driver circuit have been described in Chapter 2.

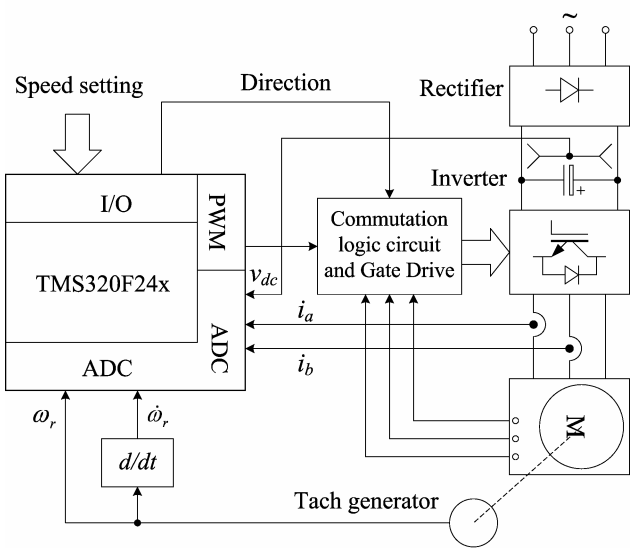


Fig. 6-6. Structure of the experimental system

The DSP used in the system is TMS320F2407 which is specially designed for power electronics and electric drive. The chip comprises dual 10 bits 16 channel ADCs, serial communication interface (SCI), event manager, digital I/O and other modules. The conversion time for each ADC unit is approximately 6μs, DC link voltage v_{dc}, the phase current i_a speed ω_r can be converted by ADC1, the phase current i_b and acceleration $\dot{\omega}_r$ can be converted by ADC2. The event manager includes PWM channels, quadrature encoder pulse (QEP) circuit, capture unit, timer and so on. As PWM signal can be generated by the DSP, triangular wave generator and comparator are not needed any more. SSRC estimator is also operated by the DSP, activation function (6-35) can be implemented by table and interpolation for fast execution.

6.4.2 Software introduction

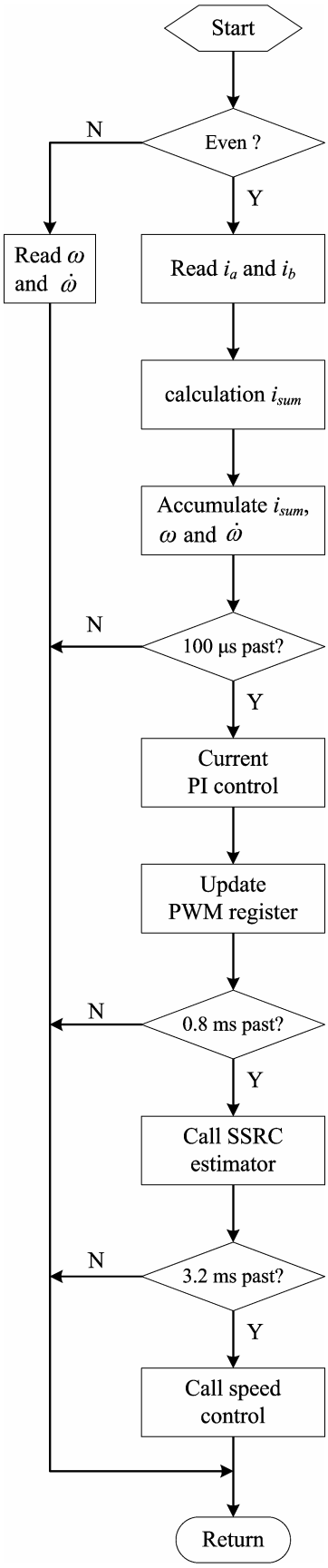
Conventional control software is modified to acquire data for training neural network in SSRC estimator. To simplify software, only two phase currents i_a and i_b, speed ω_r and acceleration $\dot{\omega}_r$ are converted by ADCs, DC link voltage is recorded by hand. The period of timer T1 will be set to be 25μs and the period interrupt of timer T1 is enabled. The period of timer T2 will be set to be 50μs and be selected as the time base for PWM unit, the switching frequency is 20 kHz. Phase current i_a and speed ω_r are converted by ADC1 alternately when timer T1 interrupt occurs, Phase current i_b and acceleration $\dot{\omega}_r$ are

converted by ADC2 alternately when timer T1 interrupt occurs. Thus phase currents i_a and i_b can be converted at the same time and speed ω_r and acceleration $\dot{\omega}_r$ can be converted at the same time, too. Every 16 samples are averaged to get $\dot{\omega}_r(n)$, $\omega_r(n)$ and $i_{sum}(n)$. For each set, DSP saves $\dot{\omega}_r(n)$, $\omega_r(n)$ and $i_{sum}(n)$ in the DSP memory during starting. Then these data are uploaded to a PC, the PC selects $M + N$ of them to build up M training patterns for neural network by Equations (6-21) ~ (6-28). The reference current in steady state is also recorded as the desired output i_s^* of neural network. Then the neural network can be trained to get ultimate weights.

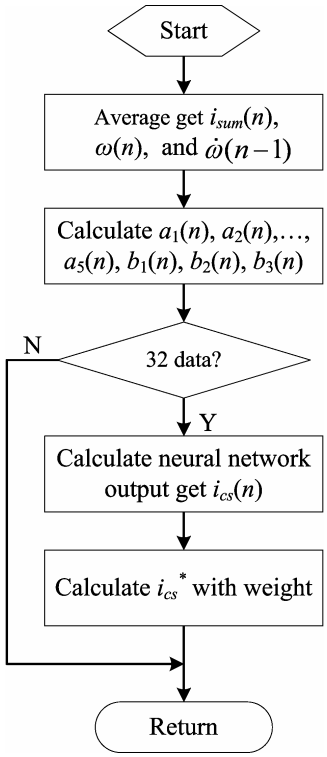
With trained neural network, the control software with SSRC prediction technique can be developed. The flowchart of the software is shown in Fig. 6-7 which includes timer T1 interrupt service routine, SSRC prediction routine and speed control subroutine.

The flowchart of main routine is similar to Fig. 5-14(a) except that there are more than two variables that should be converted by ADCs, no QEP is needed any more. The period of timer T1 is also set to be 25μs and T2 is also set to be 50μs. Timer T2 is also selected as the time base for PWM unit and the switching frequency is 20k Hz. The ADCs are also set to be started by timer T1 event. Thus two phase currents i_a and i_b, speed ω_r and acceleration $\dot{\omega}_r$ can be sampled every PWM period.

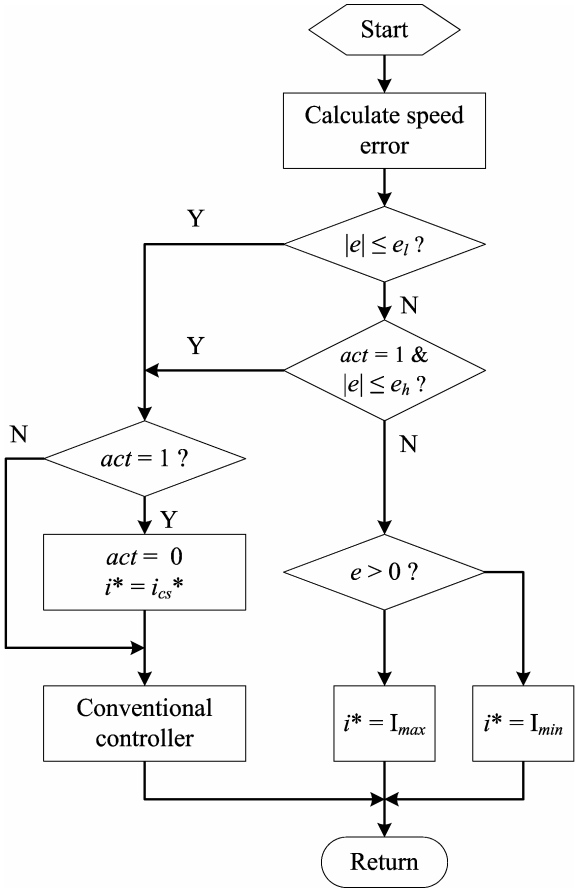
The flowchart of timer T1 interrupt service routine is shown in Fig. 6-7(a). Phase current i_a and speed ω_r are also converted by ADC1 alternately, and phase current i_b and acceleration $\dot{\omega}_r$ are also converted by ADC2 alternately. If the timer T1 interrupt number is odd, the routine reads speed ω_r and acceleration $\dot{\omega}_r$ from ADC1 and ADC2 respectively. If the interrupt number is even, the routine reads phase currents i_a and i_b from ADC1 and ADC2 respectively. Then i_{sum} can be also calculated as Equation (5-23). i_{sum} should be accumulated for current PI control every 100 μs (i.e. two PWM period). Speed ω_r, acceleration $\dot{\omega}_r$ and i_{sum} should be also accumulated to get average every 0.8 ms for being built up neural network input data. SSRC estimator is also called every 0.8 ms. The sample period of speed controller is 3.2 ms, thus speed control subroutine is called every 64 times of timer T1 interrupt. The input of speed controller is latest averaged speed (and acceleration).



(a) Timer T1 interrupt routine



(b) SSRC prediction subroutine



(c) Speed control subroutine

Fig. 6-7. Flowchart of software

The flowchart of SSRC estimator is shown in Fig. 6-7(b). In the subroutine, the DSP get the average of the 16 samples of acquired data to obtain $\omega_r(n)$, $\dot{\omega}_r(n)$ and $i_{sum}(n)$. Current and 15 former data are used to built up neural network input $a_1(n)$, $a_1(n)$, … , $a_5(n)$, $b_1(n)$, $b_2(n)$ and $b_3(n)$ according to the Equation (6-21) ~ (6-28). To save CPU cycle, these Equations are modified as:

$$x_1(n) = a_1(n) = a_1(n-1) + \dot{\omega}_r^2(n) - \dot{\omega}_r^2(n-N) \tag{6-50}$$

$$x_2(n) = a_2(n) = a_2(n-1) + \omega_r^2(n) - \omega_r^2(n-N) \tag{6-51}$$

$$x_3(n) = a_3(n) = a_3(n-1) + \dot{\omega}_r(n)\omega_r(n) - \dot{\omega}_r(n-N)\omega_r(n-N) \tag{6-52}$$

$$x_4(n) = a_4(n) = a_4(n-1) + \dot{\omega}_r(n) - \dot{\omega}_r(n-N) \tag{6-53}$$

$$x_5(n) = a_5(n) = a_5(n-1) + \omega_r(n) - \omega_r(n-N) \tag{6-54}$$

$$x_6(n) = b_1(n) = b_1(n-1) + \dot{\omega}_r(n)i_{sum}(n) - \dot{\omega}_r(n-N)i_{sum}(n-N) \tag{6-55}$$

$$x_7(n) = b_2(n) = b_2(n-1) + \omega_r(n)i_{sum}(n) - \omega_r(n-N)i_{sum}(n-N) \tag{6-56}$$

$$x_8(n) = b_3(n) = b_3(n-1) + i_{sum}(n) - i_{sum}(n-N) \tag{6-57}$$

To save multiply instruction, $\dot{\omega}_r^2(n-i)$, $\omega_r^2(n-i)$, $\dot{\omega}_r(n-i)\omega_r(n-i)$, $\dot{\omega}_r(n-i)i_{sum}(n-i)$ and $\omega_r(n-i)i_{sum}(n-i)$ (i = 0, … , N) are also saved in DSP memory. The output of the neural network $i_{cs}(n)$ can be calculated with input $x_1(n)$ ~ $x_8(n)$. Then coarse reference current i_{cs}^* can be get according Equation (6-16).

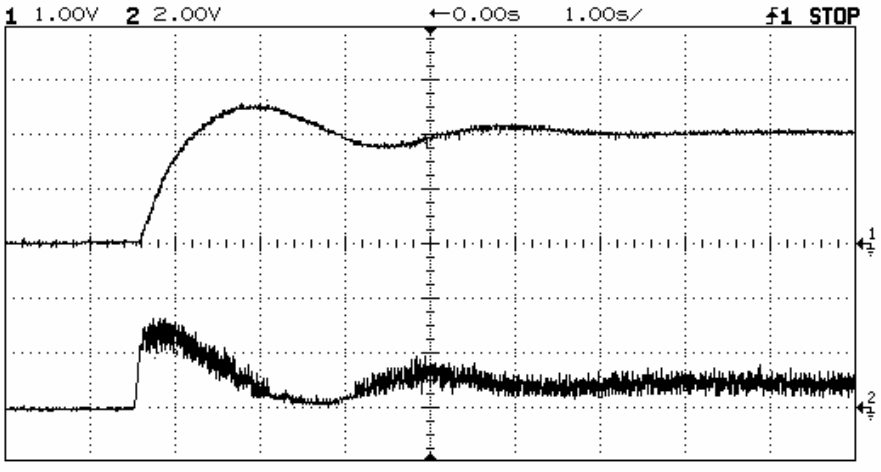
The flowchart of speed control subroutine is shown in Fig. 6-7(c). In the subroutine, the conventional controller active signal $act(n)$ is determined according speed error and previous $act(n\text{-}1)$ according Equation (6-14). When the act is 1, conventional controller is active, otherwise reference current i^* is set as extremum value. When the act is jumped from 1 to 0, reference current i^* skips from extremum value to coarse reference current i_{cs}^*.

6.4.3 Experimental results

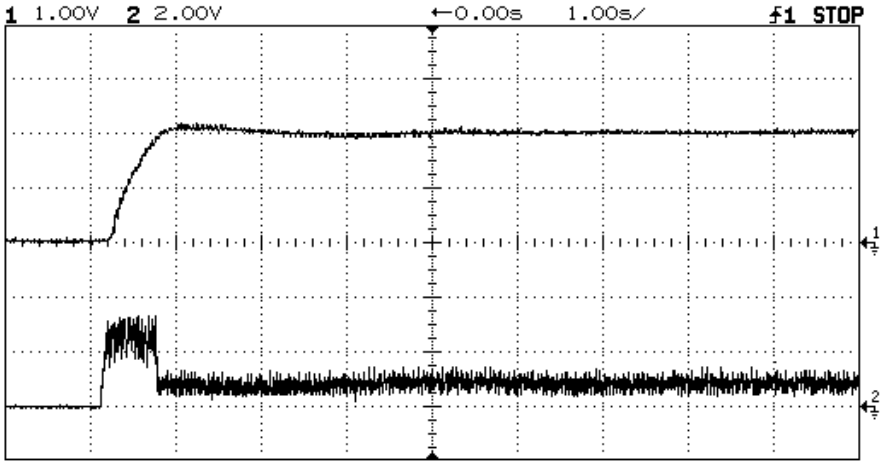
The switching frequency is 20 kHz. The phase current is sampled every 50μs, the speed is also measured every 50μs. SSRC estimator executes every 0.8ms. There are 16 current and speed samples each period. These samples are averaged to get $\dot{\omega}_r(n)$, $\omega_r(n)$ and

$i_{sum}(n)$. These data are used to build up input data for neural network by Equations (6-21) ~ (6-28) with former N-1 samples. The sample period for inner current loop is 100μs (two switching periods). The sample period for outer speed loop is 3.2ms (four SSRC estimator sample period). Threshold for coarse reference current generator e_l and e_h is 5% ω_n and 15% ω_n respectively. The parameter of the PI speed controller $K_{s\omega}$ and $\tau_{s\omega}$ is 15 and 28.7ms respectively, the parameter PI current controller K_{si} and τ_{si} is 2.2 and 3.075ms respectively. The data number N for calculating neural network training pattern is 32, the pattern number M in each set is 200, the set number L is 32. The neuron number in the first hidden layer is 24, the neuron number in the second hidden layer is 16. The drive system is tested under PI controller and fuzzy controller respectively.

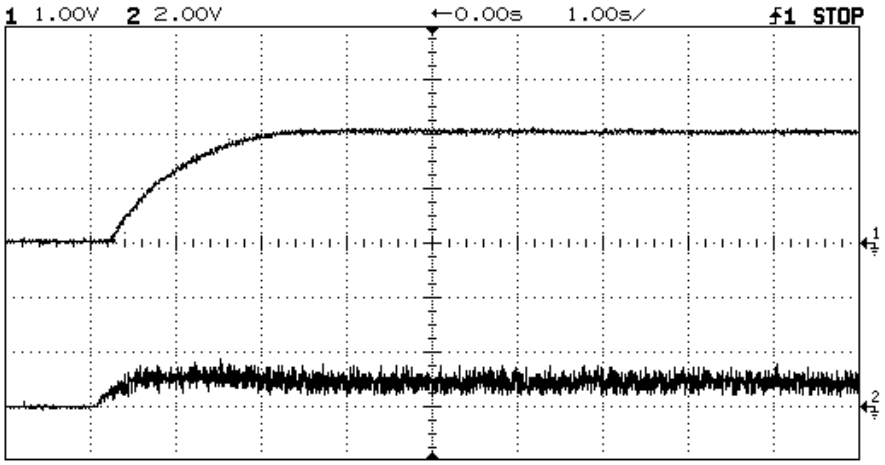
The experimental waveforms are shown in Fig. 6-8. The top waveform of each captured figure is motor speed with scale 1000 rpm/div. The bottom waveform is DC link current with scale 5A/div. Time scale is 1 s/div. Speed response during starting under PI controller with and without SSRC prediction technique and corresponding DC link current are shown in Fig. 6-8(a) and 6-8(b) respectively. Speed response under fuzzy logic controller for various reference speed and various loads with and without SSRC prediction technique are shown in Fig. 6-8(c) ~ 6-8(g) respectively. Speed response with load torque impulse is shown in Fig. 6-8(h). Step up and step down speed response is shown in Fig. 6-8(i) and 6-8(j) respectively. From these figures we can see that the conventional controller combined with SSRC prediction technique has the advantage of little overshoot, little oscillation, fast response, robust and so on. The performance is improved greatly.



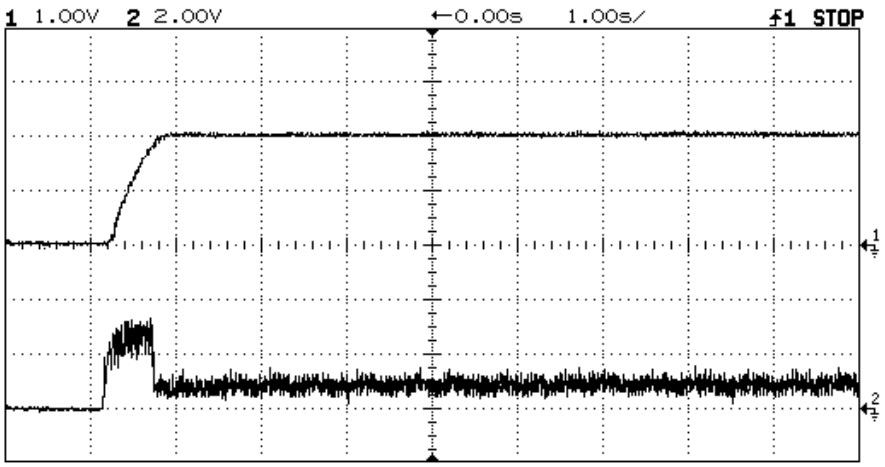
(a) PID control without SSRC prediction technique (ω_r^* = 2000rpm, starting)



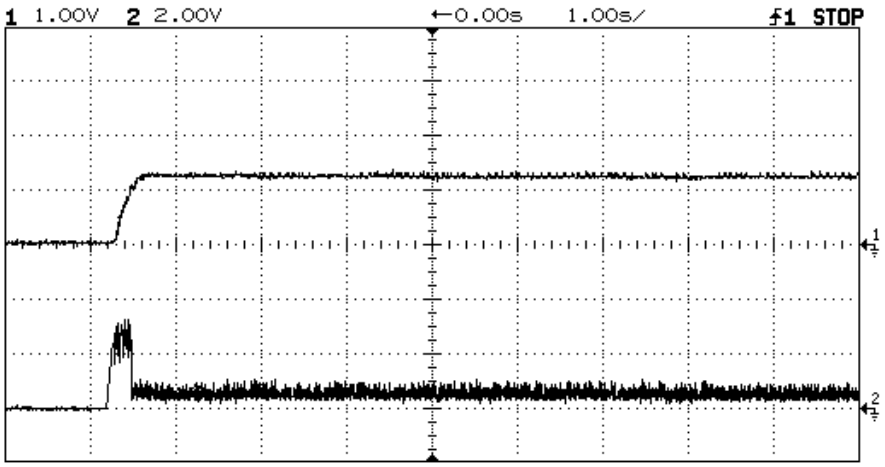
(b) PID control with SSRC prediction technique (ω_r^* = 2000rpm, starting)



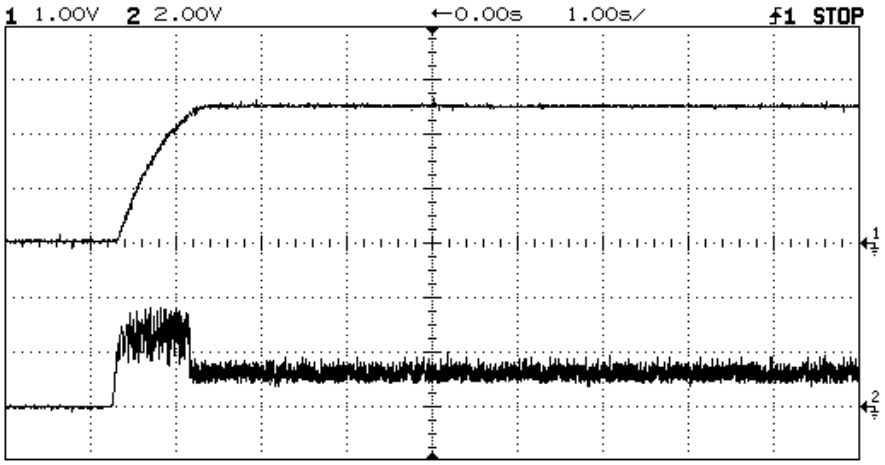
(c) Fuzzy control without SSRC prediction technique (ω_r^* = 2000rpm, starting)



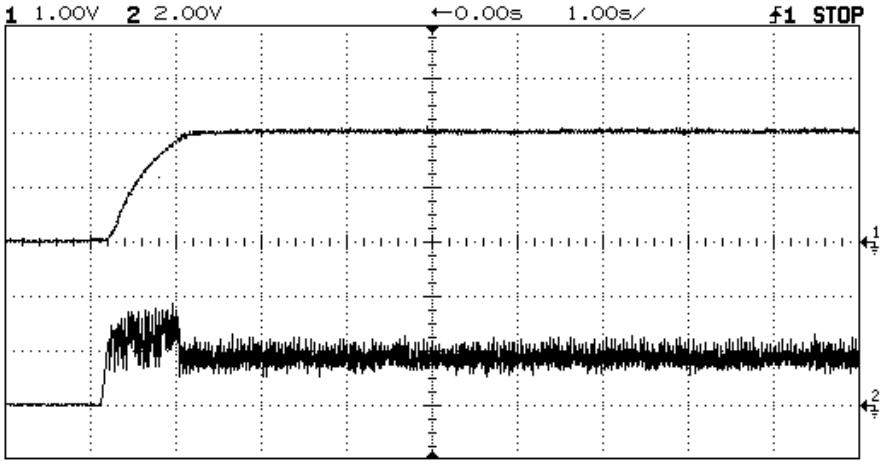
(d) Fuzzy control with SSRC prediction technique (ω_r^* = 2000rpm, starting)



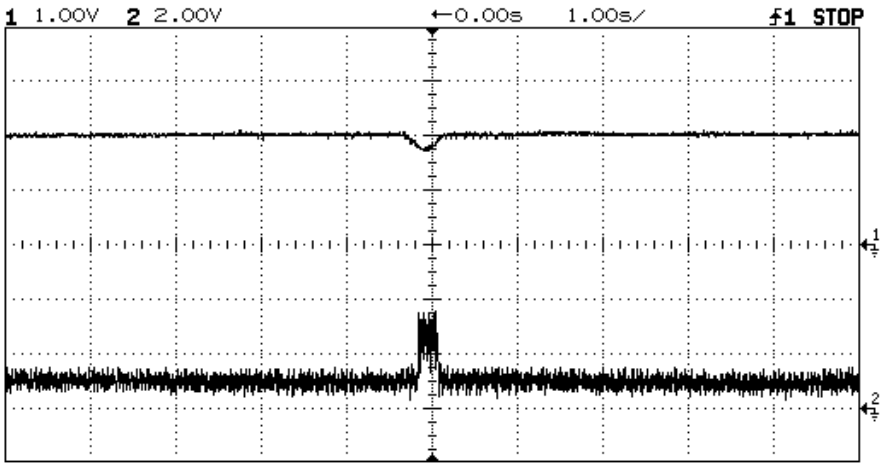
(e) Fuzzy control with SSRC prediction technique (ω_r^* = 1250rpm, starting)



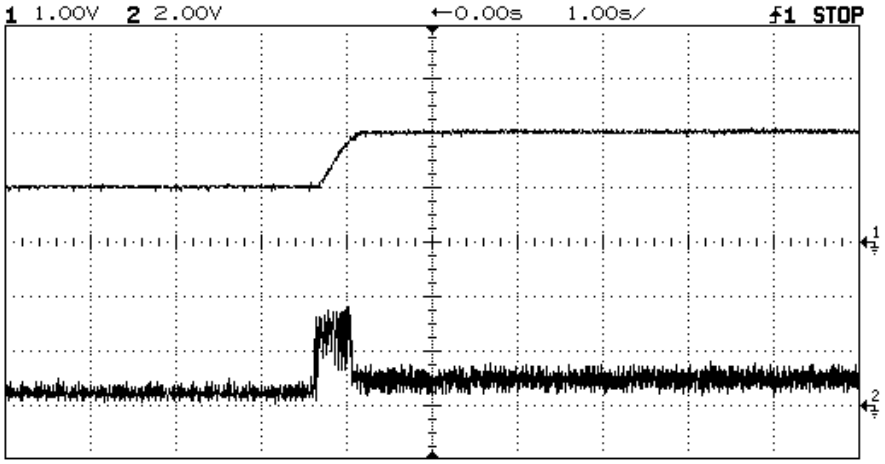
(f) Fuzzy control with SSRC prediction technique (ω_r^* = 2500rpm, starting)



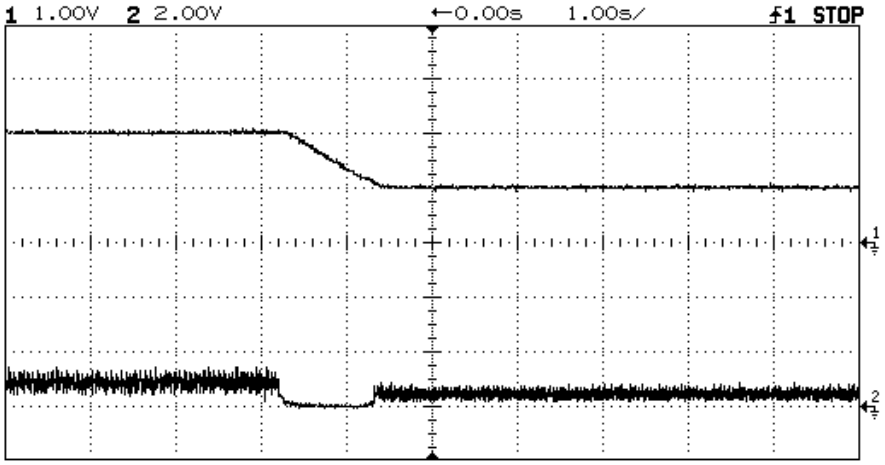
(g) Fuzzy control with SSRC prediction technique (ω_r^* = 2000rpm, starting, heavy load)



(h) Fuzzy control with SSRC prediction technique (ω_r^* = 2000rpm, load torque impulse)



(i) Fuzzy control with SSRC prediction technique (ω_r^* step up from 1000rpm to 2000 rpm)



(j) Fuzzy control with SSRC prediction technique (ω_r^* step down from 2000rpm to 1000 rpm)

Fig. 6-8. Experimental waveforms of speed response and DC link current under PI and fuzzy control with or without SSRC prediction technique

6.5 Summary

A SSRC prediction technique based on neural network for PM BDCM drive system is proposed. Conventional controller with this technique holds the advantages of fast response, little overshoot, little oscillation, robust and so on. The design of the conventional controller is introduced. The prediction technique is described in detail. Hardware implementation and software flowchart are described and experimental results are illustrated. The drive system is tested under PI controller and fuzzy controller. The performance is improved greatly. The result of this investigation will be very useful for industrial applications.

Chapter 7 Conclusion and Recommendation

7.1 Conclusion

The background of the research work is introduced firstly and the concept of the soft-switching is introduced. Then operation principle of the brushless DC motor is introduced. The controller for BDCM drive system is described. Commutation logic table is proposed, speed sensor is introduced and two methods to get speed signal from Hall sensor are illustrated, gate driver circuit for IGBT is introduced and bootstrap supply is applicable to gate driver circuit to save the number of insulated DC power supply. A novel 12-switches inverter for BDCM is proposed to reduce the torque ripple of BDCM. With the inverter, for a given voltage of supply, torque and speed of the motor are doubled. For a given speed of the motor, the voltage stress of switching device is reduced by half, the insulation class requirement can be also reduced. The inverter is also applicable to induction motor.

Then known resonant DC link inverters have been reviewed. A transformer based resonant DC link inverter for BDCM drive system, capable of controlling zero voltage notch instant and width is presented. Its principle of operation was explained. The simulation results are also given. All the relevant experimental waveforms were captured to verify the theory and simulation. The following observations were made:

- All switches work under soft-switching condition, so their power losses are small.
- Voltage stress on all the switches would be not greater than DC Supply voltage.
- Only one DC link voltage notch is needed during one PWM cycle, and the switching frequency of the auxiliary switches would not be higher than PWM frequency.
- Simple auxiliary switches control scheme.
- Freewheeling diodes turned off under zero current condition and this greatly reduced the reverse recovery problem of the diodes.

- *dv/dt* and *di/dt* are reduced significantly, so EMI is reduced.
- Soft switching results in considerably less noise as the switching frequency can be high to beyond the audio spectrum.
- The topology also applicable to induction motor drive system.

Known resonant pole inverters have been reviewed. A special designed resonant pole inverter dedicated for BDCM drive system is presented. Its principle of operation is explained. Selection of the required transformer parameter, snubber capacitors is given. The main inverter switches and auxiliary switches gate signal generation method are also illustrated. Determination of the corresponding pulse width is given. The inverter operation is also verified by the results of simulation and experiment. The following observations were made:

- All the high switching frequency switches (three lower main switches and auxiliary switches) work under soft-switching condition.
- Voltage stress on all the switches is low that is not greater than DC Supply voltage.
- Very simple auxiliary switches control scheme.
- Freewheeling diodes turned off under zero current condition and this greatly reduced the reverse recovery problem of the diodes.
- The normal operation of the inverter is entirely the same as hard switching inverter.
- *dv/dt* and *di/dt* are reduced significantly, so EMI is reduced.
- As the switching frequency is as high as 20 kHz, the switching acoustic noise can be eliminated.

In a resonant DC link inverter with little link voltage ripple, usually there is a main conduction path switch which will increase conduction power losses. In case of induction motor (or other three phase AC load) application, there is a DC link voltage notch if any main inverter switch changes state, thus unchanging phase will be affected. In a resonant pole inverter, there are no extra conduction power losses and the DC link voltage is kept constant while relative more auxiliary devices are required than that of resonant DC link inverter. General speaking, the performance of resonant pole inverter is a little higher

than that of resonant DC link inverter. For BDCM drive system, in case of compact inverter is required, resonant DC link inverter is recommended. If requiring more auxiliary device is acceptable, resonant pole can be adopted.

A hybrid controller for the PM BDCM drive system is proposed which holds the advantages of both PI controller and fuzzy controller, i.e. fast response, little overshoot, little oscillation, robust to system parameters variation, stability and so on. The design of the controller is proposed. Hardware implementation is described and software flowchart is illustrated. Experimental results are presented. The design of the controller is successful.

A SSRC prediction technique based on neural network for PM BDCM drive system is proposed. Conventional controller with this technique holds the advantages of fast response, little overshoot, little oscillation, robust and so on. The design of the conventional controller is introduced. The prediction technique is described in detail. Hardware implementation and software flowchart is proposed and experimental results are illustrated. The drive system is tested under PI controller and fuzzy controller. The performance is improved greatly. The result of this investigation will be very useful for industrial applications.

The reference current in conventional controllers (such as the controller presented in Chapter 5) is continuous. Although these controllers can greatly improve the performance of the system, they can not further shorter the rise time and settling time. The controller combined with SSRC technique, the reference current is discontinuous. Current can reach its maximum value immediately during starting which gets shorter rising time; when the motor reaches desired speed, the current is changed to its steady state value at the same time and the motor runs at the desired speed, then settling time can be further reduced. It can get the shortest rise time and settling time in theory.

7.2 Recommendation

The laboratorial resonant DC link inverter and resonant pole inverter, used in this thesis, are only prototypes. Although it could explain some fundamental laws of the topology, higher power and higher voltage inverter seems more preferable for practical applications.

Protection and Reliability are other factors that should be considered for practical applications. More research work can be focused on current source inverter with soft-switching technique for BDCM, soft-switching inverter for switch reluctance motor (SRM) and 12-switches inverter for induction motor application.

The SSRC technique proposed in this thesis is based on off-line training neural network, on-line training neural network can be also further studied. Doing some experiment on the application of BDCM drive system such as Electrical Vehicle would be very attractive if there is chance.

Author's Publications

[1] Z.Y. Pan and F.L. Luo, "Novel Soft-switching Inverter for Brushless DC Motor Variable Speed Drive System", *IEEE Trans. Power Electron.*, Vol. 19, No. 2, pp. 280-288, Mar. 2004.

[2] Z.Y. Pan and F.L. Luo, "Novel Resonant Pole Inverter for Brushless DC Motor Drive System", *IEEE Trans. Power Electron.*, Vol. 20, No. 1, pp. 173-181, Jan. 2005.

[3] Z.Y. Pan and F.L. Luo, "Transformer Based Resonant DC link Inverter for Brushless DC Motor Drive System", *IEEE Trans. Power Electron*, Vol. 20, No. 4, pp. 939-947, Jul. 2005.

[4] Z.Y. Pan and F. L. Luo, "Steady State Reference Current Prediction Technique for Brushless DC Motor Drive System", *IEE Proc. Electric Power Appl.*, Vol. 152, No. 6, pp. 1585-1594, Nov. 2005.

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Appendix

A. The ABEL Source Code for Commutation Logical Circuit

The ABEL source file for BDCM commutation logical circuit can be written as follows:

```
"Filename: Commut.abl

MODULE  COMMUTATE
TITLE   'Commutate logical circuit IC for BDCM,'
ICCOMMU     DEVICE 'P16V8S';

"INPUT PIN
A, B, C             PIN 1,2,3;
PWM, DIR, EN        PIN 4,5,6;

"OUTPUT PIN
PWM1, PWM3, PWM5    PIN 19,18,17;
PWM4, PWM6, PWM2    PIN 16,15,14;

EQUATIONS
PWM1 = EN & !A & B & DIR         #  EN & !B & A & !DIR;
PWM3 = EN & !B & C & DIR         #  EN & !C & B & !DIR;
PWM5 = EN & !C & A & DIR         #  EN & !A & C & !DIR;
PWM4 = EN & !B & A & DIR & PWM   #  EN & !A & B & !DIR & PWM;
PWM6 = EN & !C & B & DIR & PWM   #  EN & !B & C & !DIR & PWM;
PWM2 = EN & !A & C & DIR & PWM   #  EN & !C & A & !DIR & PWM;

TEST_VECTORS
([A, B, C, PWM,EN,DIR]->[PWM1,PWM3,PWM5,PWM4,PWM6,PWM2])
 [1, 1, 1, 1,  1, 1]  ->[0,   0,   0,   0,   0,   0];
 [0, 0, 0, 1,  1, 1]  ->[0,   0,   0,   0,   0,   0];
 [1, 0, 1, 1,  0, 1]  ->[0,   0,   0,   0,   0,   0];
 [0, 1, 0, 1,  1, 1]  ->[1,   0,   0,   0,   1,   0];
 [0, 0, 1, 0,  1, 1]  ->[0,   1,   0,   0,   0,   0];
 [0, 1, 1, 1,  1, 0]  ->[0,   0,   1,   1,   0,   0];

END COMMUTATE
```

B. Implementation of QEP Generator Circuit

The schematic circuit which adds some definition of input and output ports for GAL PLD from Fig. 4-4a is shown in Fig. A-1. All the logic GATE in the schematic circuit can be implemented by only one GAL16V8 IC. The definition of input and output ports name and ABEL logical equation can be written as follows:

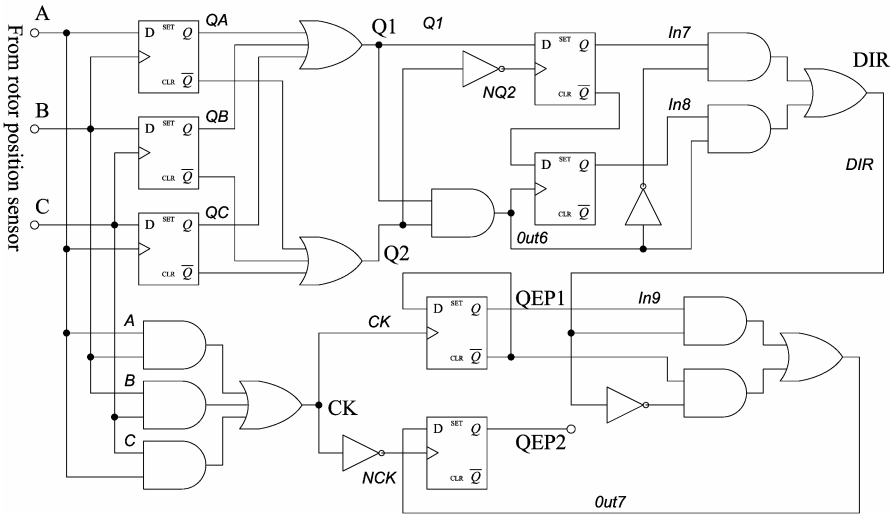

Fig. A-1. Schematic circuit

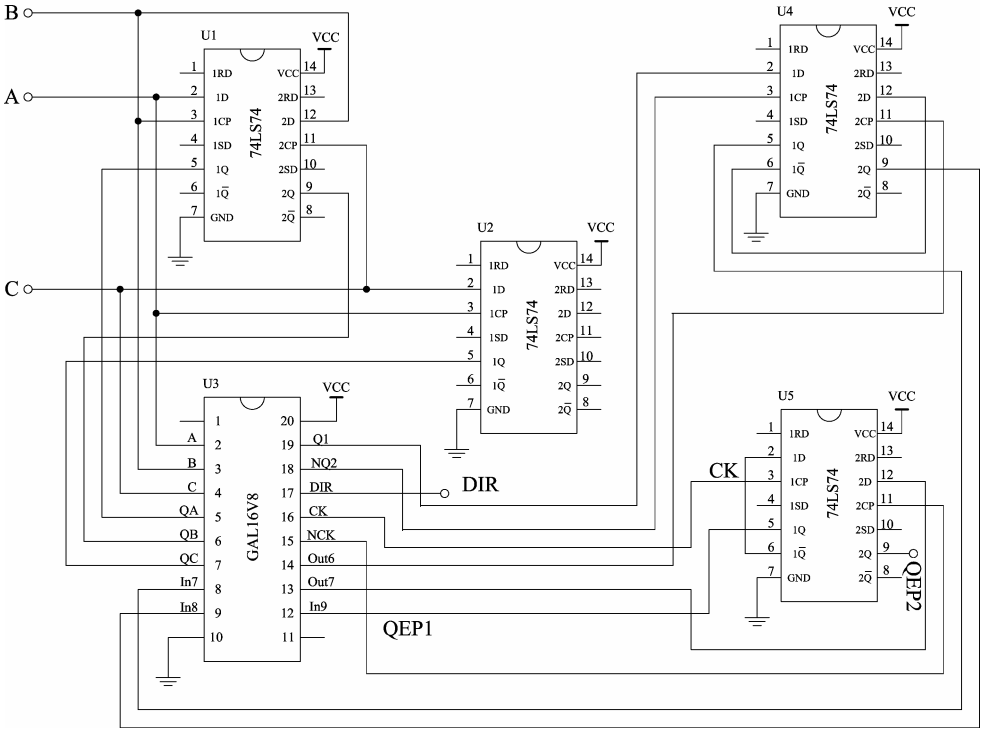

Fig. A-2. Implementation circuit

```
Input:      A, B, C, QA, QB, QC, In7, In8, In9;
Output:     Q1, NQ2, DIR, CK, NCK, Out6, Out7;
Equation:
            Q1   = QA # QB # QC;
            NQ2  = QA & QB & QC;
            CK   = A & B # B & C # C& A;
            NCK  = !CK;
            Out6 = !NQ2 & Q1;
            DIR  = In7 & !Out6 # In8 & Out6;
            Out7 = In9 & DIR # !In9 & !DIR;
```

The implementation circuit for QEP generator is shown in Fig. A-2.

C. Main Drive Board for the Inverter

The main drive board for the inverter provides gate driver for the main switches and brake switch of the inverter, isolated DC power supply for gate driver and control circuit. Its schematic circuit diagram is shown in Fig. A-4. Detail of the IC board in this figure is shown in Fig. A-3.

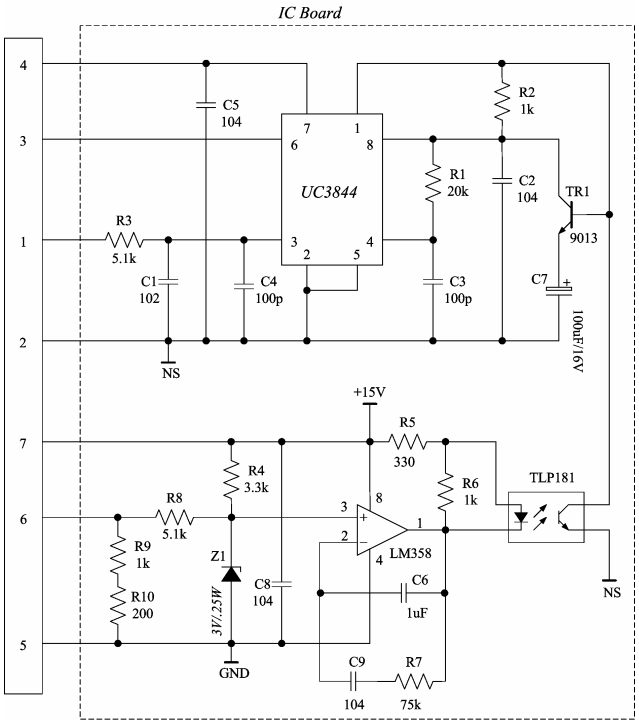

Fig. A-3. Detail of the IC board in the main drive board

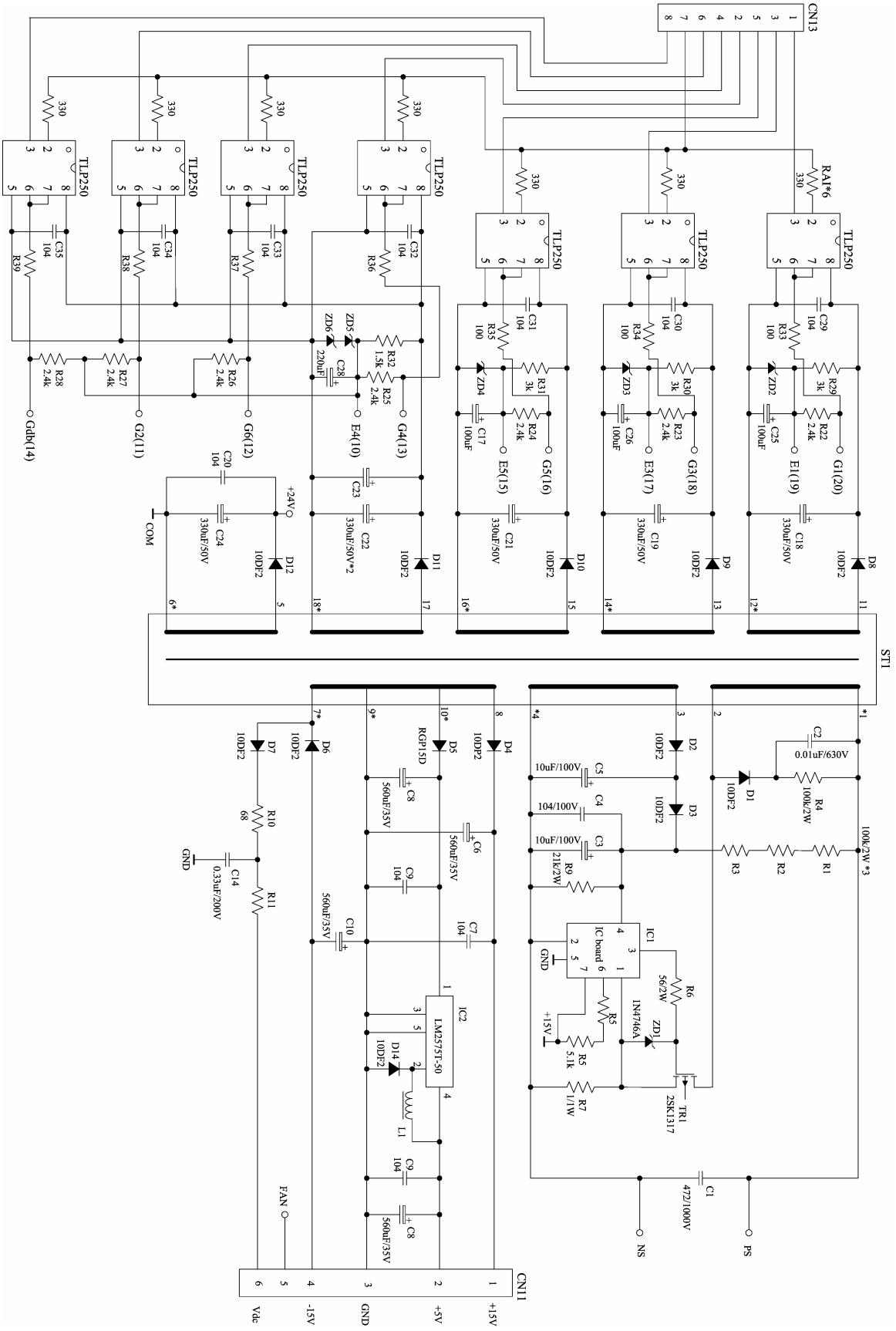

Fig. A-4. Main drive board for the inverter

D. Solution of the Equation 3-5

Solve the Equation (3-5):

$$\begin{cases} u_{Cr}(t) = L_{l1}\dfrac{di_{Lr}(t)}{dt} + a^2 L_{l2}\dfrac{d[i_{Lrs}(t)/a]}{dt} + aV_S \\ i_{Lr}(t) + I_0 + C_r\dfrac{du_{Cr}(t)}{dt} = 0 \end{cases} \tag{3-5}$$

With initial condition $u_{Cr}(0) = V_S$, $\quad i_{Lr}(0) = 0$

Solution:

Rewrite the equation $L_r = L_{l1} + L_{l2}/n^2$

$$\begin{cases} u_{Cr}(t) = \left(L_{l1} + \dfrac{1}{n^2}L_{l2}\right)\dfrac{di_{Lr}(t)}{dt} + \dfrac{V_S}{n} \\ i_{Lr}(t) + I_0 + C_r\dfrac{du_{Cr}(t)}{dt} = 0 \end{cases}$$

$$\begin{cases} u_{Cr}(t) = L_r\dfrac{di_{Lr}(t)}{dt} + \dfrac{V_S}{n} \\ i_{Lr}(t) = -I_0 - C_r\dfrac{du_{Cr}(t)}{dt} \end{cases}$$

Laplace transform of the above equation get

$$\begin{cases} U_{Cr}(s) - \dfrac{V_S}{ns} = L_r s I_{Lr}(s) \\ I_{Lr}(s) = -\dfrac{I_0}{s} - C_r\left[sU_{Cr}(s) - V_S\right] \end{cases}$$

$$U_{Cr}(s) - \frac{V_S}{ns} = L_r s\left[-\frac{I_0}{s} - C_r sU_{Cr}(s) + C_r V_S\right]$$

$$L_r C_r s^2 U_{Cr}(s) + U_{Cr}(s) = sL_r C_r V_S + \frac{V_S}{ns} - L_r I_0$$

$$U_{Cr}(s) = \frac{sL_r C_r V_S + \dfrac{V_S}{ns} - L_r I_0}{L_r C_r s^2 + 1} = \frac{sV_S + \dfrac{V_S}{nL_r C_r s} - \dfrac{I_0}{C_r}}{s^2 + \dfrac{1}{L_r C_r}}$$

$$= \frac{sV_S + \frac{V_S}{ns}\left(s^2 + \frac{1}{L_r C_r}\right) - \frac{sV_S}{n} - \frac{I_0}{C_r}}{s^2 + \frac{1}{L_r C_r}} = \frac{\frac{n-1}{n} sV_S - \frac{I_0}{C_r}}{s^2 + \frac{1}{L_r C_r}} + \frac{V_S}{ns}$$

$$u_{Cr}(t) = \frac{(n-1)V_S}{n}\cos(\omega_r t) - I_0\sqrt{\frac{L_r}{C_r}}\sin(\omega_r t) + \frac{V_S}{n}$$

$$I_{Lr}(s) = -\frac{I_0}{s} + C_r V_S - C_r s U_{Cr}(s)$$

$$I_{Lr}(s) = -\frac{I_0}{s} + C_r V_S - \frac{s^2 L_r C_r C_r V_S + \frac{C_r V_S}{n} - sL_r C_r I_0}{L_r C_r s^2 + 1}$$

$$= -\frac{I_0}{s} + \frac{s^2 L_r C_r C_r V_S + C_r V_S - s^2 L_r C_r C_r V_S - C_r V_S / n + sL_r C_r I_0}{L_r C_r s^2 + 1}$$

$$= -\frac{I_0}{s} + \frac{\frac{n-1}{n} C_r V_S + sL_r C_r I_0}{L_r C_r s^2 + 1} = -\frac{I_0}{s} + \frac{\frac{(n-1)V_S}{nL_r} + sI_0}{s^2 + \frac{1}{L_r C_r}}$$

$$i_{Lr}(t) = I_0\cos(\omega_r t) - I_0 + \frac{(n-1)V_S}{n}\sqrt{\frac{C_r}{L_r}}\sin(\omega_r t)$$

Solve the same equation:

$$\begin{cases} u_{Cr}(t) = L_{l1}\dfrac{di_{Lr}(t)}{dt} + a^2 L_{l2}\dfrac{d[i_{Lrs}(t)/a]}{dt} + aV_S \\ i_{Lr}(t) + I_0 + C_r\dfrac{du_{Cr}(t)}{dt} = 0 \end{cases} \tag{3-5}$$

With initial condition $u_{Cr}(0) = 0, \quad i_{Lr}(0) = -I_0$, (in mode 5)

Solution:

Rewrite the equation

$$\begin{cases} u_{Cr}(t) = L_r\dfrac{di_{Lr}(t)}{dt} + \dfrac{V_S}{n} \\ i_{Lr}(t) = -I_0 - C_r\dfrac{du_{Cr}(t)}{dt} \end{cases}$$

Laplace transform of the above equation get

$$\begin{cases} U_{Cr}(s) - \dfrac{V_S}{ns} = L_r\left[sI_{Lr}(s) + I_0\right] \\ I_{Lr}(s) = -\dfrac{I_0}{s} - C_r s U_{Cr}(s) \end{cases}$$

$$U_{Cr}(s) - \frac{V_S}{ns} = L_r s\left[-\frac{I_0}{s} - C_r s U_{Cr}(s)\right] + L_r I_0$$

$$L_r C_r s^2 U_{Cr}(s) + U_{Cr}(s) = \frac{V_S}{ns}$$

$$U_{Cr}(s) = \frac{\dfrac{V_S}{ns}}{L_r C_r s^2 + 1} = \frac{\dfrac{V_S}{nL_r C_r s}}{s^2 + \dfrac{1}{L_r C_r}}$$

$$= \frac{\dfrac{V_S}{ns}\left(s^2 + \dfrac{1}{L_r C_r}\right) - \dfrac{sV_S}{n}}{s^2 + \dfrac{1}{L_r C_r}} = \frac{-\dfrac{sV_S}{n}}{s^2 + \dfrac{1}{L_r C_r}} + \frac{V_S}{ns}$$

$$u_{Cr}(t) = -\frac{V_S}{n}\cos(\omega_r t) + \frac{V_S}{n}$$

$$I_{Lr}(s) = -\frac{I_0}{s} - C_r s U_{Cr}(s)$$

$$I_{Lr}(s) = -\frac{I_0}{s} - \frac{\dfrac{C_r V_S}{n}}{L_r C_r s^2 + 1} = -\frac{I_0}{s} - \frac{\dfrac{V_S}{nL_r}}{s^2 + \dfrac{1}{L_r C_r}}$$

$$i_{Lr}(t) = -I_0 - \frac{V_S}{n}\sqrt{\frac{C_r}{L_r}}\sin(\omega_r t)$$

E. Auxiliary Drive Board for Resonant DC Link Inverter

Auxiliary drive board for resonant DC link inverter provides gate driver for auxiliary switches, measure and compare DC link voltage to generate gate signal for auxiliary switch S_L. Its schematic circuit diagram is shown in Fig. A-5.

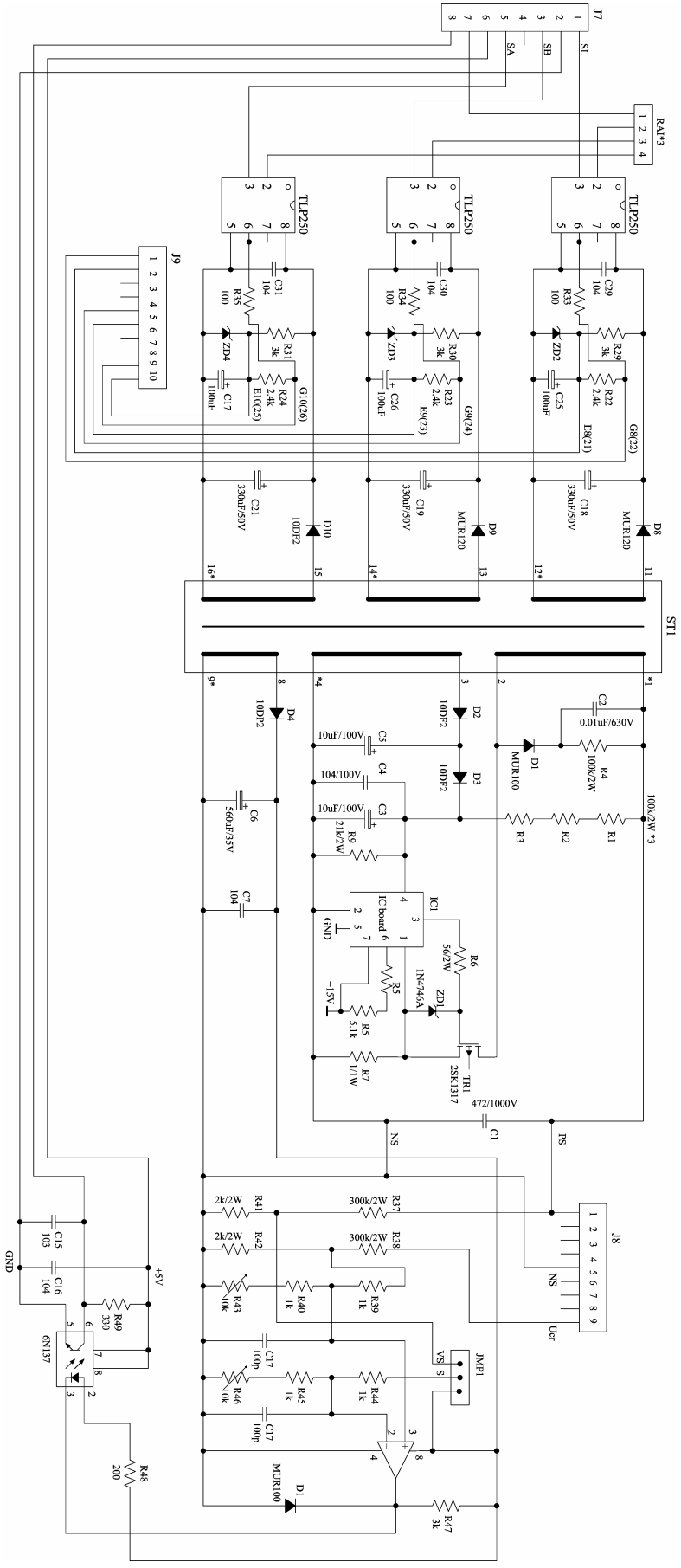

Fig. A-5. Auxiliary drive board for resonant Dc link inverter

F. Solution of the Equation 4-6

Solve the Equation (3-5):

$$\begin{cases} u_{S6}(t) = L_{l1}\dfrac{di_{Lr}(t)}{dt} + a^2 L_{l2}\dfrac{d[i_{Lrs}(t)/a]}{dt} + aV_S \\ -C_r\dfrac{du_{S6}(t)}{dt} = i_{Lr}(t) - I_0 \end{cases} \tag{4-6}$$

With initial condition $u_{S6}(0) = V_S$, $i_{Lr}(0) = I_0$

Solution:

Rewrite the equation $L_r = L_{l1} + L_{l2}/n^2$

$$\begin{cases} u_{S6}(t) = \left(L_{l1} + \dfrac{1}{n^2}L_{l2}\right)\dfrac{di_{Lr}(t)}{dt} + \dfrac{V_S}{n} \\ i_{Lr}(t) + C_r\dfrac{du_{S6}(t)}{dt} = I_0 \end{cases}$$

$$\begin{cases} u_{S6}(t) = L_r\dfrac{di_{Lr}(t)}{dt} + \dfrac{V_S}{n} \\ i_{Lr}(t) = I_0 - C_r\dfrac{du_{S6}(t)}{dt} \end{cases}$$

Laplace transform of the above equation get

$$\begin{cases} U_{S6}(s) - \dfrac{V_S}{ns} = L_r\left[sI_{Lr}(s) - I_0\right] \\ I_{Lr}(s) = \dfrac{I_0}{s} - C_r\left[sU_{S6}(s) - V_S\right] \end{cases}$$

$$U_{S6}(s) - \frac{V_S}{ns} = L_r s\left[\frac{I_0}{s} - C_r sU_{S6}(s) + C_r V_S\right] - L_r I_0$$

$$L_r C_r s^2 U_{S6}(s) + U_{S6}(s) = sL_r C_r V_S + \frac{V_S}{ns}$$

$$U_{S6}(s) = \frac{sL_r C_r V_S + \dfrac{V_S}{ns}}{L_r C_r s^2 + 1} = \frac{sV_S + \dfrac{V_S}{nL_r C_r s}}{s^2 + \dfrac{1}{L_r C_r}}$$

$$= \frac{sV_S + \dfrac{V_S}{ns}\left(s^2 + \dfrac{1}{L_r C_r}\right) - \dfrac{sV_S}{n}}{s^2 + \dfrac{1}{L_r C_r}} = \frac{\dfrac{n-1}{n}sV_S}{s^2 + \dfrac{1}{L_r C_r}} + \frac{V_S}{ns}$$

$$u_{S6}(t) = \frac{(n-1)V_S}{n}\cos(\omega_r t) + \frac{V_S}{n}$$

$$I_{Lr}(s) = \frac{I_0}{s} + C_r V_S - C_r s U_{S6}(s)$$

$$I_{Lr}(s) = \frac{I_0}{s} + C_r V_S - \frac{s^2 L_r C_r C_r V_S + \frac{C_r V_S}{n}}{L_r C_r s^2 + 1}$$

$$= -\frac{I_0}{s} + \frac{s^2 L_r C_r C_r V_S + C_r V_S - s^2 L_r C_r C_r V_S - C_r V_S / n}{L_r C_r s^2 + 1}$$

$$= \frac{I_0}{s} + \frac{\frac{n-1}{n} C_r V_S}{L_r C_r s^2 + 1} = \frac{I_0}{s} + \frac{\frac{(n-1)V_S}{nL_r}}{s^2 + \frac{1}{L_r C_r}}$$

$$i_{Lr}(t) = I_0 + \frac{(n-1)V_S}{n}\sqrt{\frac{C_r}{L_r}}\sin(\omega_r t)$$

G. Source Code of the Hybrid Controller

Source code of the hybrid controller is in the following:

```
;*********************************************************************
; File Name:     Hybrid.asm
; Target System: TMS320F24x Evaluation Board
;
; Description:   This program is use to control a bruhless DC
;                motor drive system with speed current double close
;                loop feed back control system, the speed controller
;                is a hybrid controller with conventional PI controller
;                and fuzzy logic controller.
;
; Author:        Pan Zhiyang
; Organize:      Electric Power Research Lab,
;                School of Electrical & Electronics Engineering,
;                Nanyang Technological University, Singapore
;
; Version:       1.00
;*********************************************************************
                .include    x24x.h
                .def        _c_int0

;-----------------------------------------
;Speed regulator coefficients setting
;-----------------------------------------
KPw             .set    15                  ; P for speed controller
KIw             .set    8                   ; I for speed controller

KPi             .set    5                   ; P for current controller
KIi             .set    3                   ; I for current controller

;-----------------------------------------
;Speed and current limitation
;-----------------------------------------
MaxCurrent      .set    2000
```

```
;-----------------------------------------
;Fuzzy membership function boundary
;-----------------------------------------
E1              .set    030H
E2              .set    090H
MAX_E           .set    060H

dE1             .set    030H
dE2             .set    090H
MAX_dE          .set    060H

;---------------------------------------------------------------------
; Variable Declarations for on chip RAM Blocks
;---------------------------------------------------------------------
                .bss    GPR0,1              ; General purpose register.
                .bss    LED_STATUS,1        ; LED Status Register
                .bss    COMP,1              ; Duty cycle
                .bss    Idc,1               ; Line current
                .bss    Idc_ref,1           ; Current reference
                .bss    SPEED_REF,1         ; Speed reference
                .bss    SPEED_COUNT,1       ; Speed loop count
                .bss    Current_Sample_No,1 ; Speed sample number
                .bss    Direction,1         ; The direction of the motor
                .bss    Speed,1             ; The speed of the motor
                .bss    SpeedSum,1          ; The sum of speed every 8 times
                .bss    CurrentSum,1        ; The sum of current every 4 times
                .bss    CurError,1          ; Current speed error
                .bss    PreError,1          ; Previous speed error
                .bss    dError,1            ; Differential of speed error
                .bss    PreCodeH            ; Previous count in QEP
                .bss    PreCodeL            ; Previous count in QEP
                .bss    Sel                 ; Controller selection
                .bss    temp,1
                .bss    temp1,1
                .bss    temp2,1
                .bss    stack,6             ; Context save stack

;---------------------------------------------------------------------
; Vector address declarations
;---------------------------------------------------------------------
                .sect   ".vectors"

RSVECT          B       START               ; Reset Vector
INT1            B       PHANTOM             ; Interrupt Level 1
INT2            B       T1_INT              ; Interrupt Level 2
INT3            B       PHANTOM             ; Interrupt Level 3
INT4            B       PHANTOM             ; Interrupt Level 4
INT5            B       PHANTOM             ; Interrupt Level 5
INT6            B       PHANTOM             ; Interrupt Level 6
RESERVED        B       PHANTOM             ; Reserved
SW_INT8         B       PHANTOM             ; User S/W Interrupt
SW_INT9         B       PHANTOM             ; User S/W Interrupt
SW_INT10        B       PHANTOM             ; User S/W Interrupt
SW_INT11        B       PHANTOM             ; User S/W Interrupt
SW_INT12        B       PHANTOM             ; User S/W Interrupt
SW_INT13        B       PHANTOM             ; User S/W Interrupt
SW_INT14        B       PHANTOM             ; User S/W Interrupt
SW_INT15        B       PHANTOM             ; User S/W Interrupt
SW_INT16        B       PHANTOM             ; User S/W Interrupt
TRAP            B       PHANTOM             ; Trap vector
NMINT           B       PHANTOM             ; Non-maskable Interrupt
EMU_TRAP        B       PHANTOM             ; Emulator Trap
SW_INT20        B       PHANTOM             ; User S/W Interrupt
SW_INT21        B       PHANTOM             ; User S/W Interrupt
SW_INT22        B       PHANTOM             ; User S/W Interrupt
SW_INT23        B       PHANTOM             ; User S/W Interrupt

;=====================================================================
; M A I N   C O D E  - starts here
; Description:  Read reference speed
; Input:        IOPB
; Output:       SPEED_REF
;=====================================================================

                .text
_c_int0:
                NOP
```

```
START:
                CALL    SYSINIT
                CALL    EV_INIT
                CLRC    INTM                ; Enable interrupt

LOOP
                NOP
                POINT_PF2
                LACC    PBDATDIR            ; IOPB, read reference speed
                AND     #0FFH
                SFL                         ; Times 2
                POINT_PG0
                SACL    SPEED_REF
                B       LOOP

;=====================================================================
; I S R  -      T1_INT
; Description:  Responsible for T1 general purpose timer T1 period
;               interrupt, regulate the current loop every 4 times.
;               regulate the speed loop each 100 times
;=====================================================================
T1_INT
                ;save status registers
                MAR     *,AR1
                SST     #1, *+              ; save ST1
                SST     #0, *               ; save ST0

                POINT_EV
                SPLK    #0ffffh,IFRA
                POINT_PF1
                LACC    SYSIVR
                LACC    ADCTRL2
                AND     #0C0h
                BZ      NO_CURRENT_SIGNAL

                LACC    ADCFIFO1,10         ; Read ADC 1, phase current A
                POINT_PG0
                SACH    temp
                LACC    temp
                SUB     #200h               ; Minus Ioffset
                SACL    temp                ; ia
                POINT_PF1
                LACC    ADCFIFO2,10         ; Read ADC 2, phase current B
                POINT_PG0
                SACH    temp1
                LACC    temp1
                SUB     #200h               ; Minus Ioffset
                SACL    temp1               ; ib
                NEG                         ; -ib
                SUB     temp                ; ic = -ia - ib
                ABS                         ; |ic|
                SACL    temp2
                LACC    temp
                ABS                         ; |ia|
                ADD     temp2               ; |ia| + |ic|
                SACL    temp

                LACC    temp1
                ABS                         ; |ib|
                ADD     temp                ; |ia| + |ib| + |ic|
                ADD     CurrentSum          ; Accumulate
                SACL    CurrentSum

                LACC    Current_Sample_No
                ADD     #1
                SACL    Current_Sample_No
                AND     #4
                BZ      NO_CURRENT_REG
                LACC    CurrentSum          ; Read current 4 times
                SACL    Idc                 ; The value of Isum
                                            ; Not need to divid 4
                SPLK    #0, CurrentSum
                SPLK    #0, Current_Sample_No

                LACC    Idc_ref             ; Current PI control
                SUB     Idc
                MAR     *,AR2
```

```
                LAR     AR2,#0328h
                SACL    *+
                SUB     *+
                SACL    *
                LT      *-
                MPY     #KPi
                LTP     *-
                MPY     #KIi
                LTD     *
                ADD     COMP
                SACL    COMP                    ; duty

                BLZ     NEG_CURRENT             ; duty < 0;
                SUB     #4000
                BLZ     RESTORE_CMPR            ; 0 < duty < 4000
                SPLK    #4000,COMP              ; duty > 4000, 4000 => duty
                B       RESTORE_CMPR
NEG_CURRENT
                BGZ     RESTORE_CMPR
                SPLK    #0,COMP                 ; duty <0, 0 => duty

RESTORE_CMPR
                LACC    COMP
                SFR                             ; divide 8
                SFR                             ; 4000 / 8 = 500
                SFR
                POINT_EV
                SACL    CMPR1                   ; Update PWM

NO_CURRENT_REG
                POINT_PG0
                LACC    SPEED_COUNT
                ADD     #1
                SACL    SPEED_COUNT

                SUB     #100                    ; 50us * 100 = 5ms
                BLZ     NO_SPEED_REG
                CALL    SPEED_REG
                SPLK    #0, SPEED_COUNT
NO_SPEED_REG

                ;restore status registers
                MAR     *, AR1                  ; make stack pointer active
                LST     #0, *-                  ; load ST0
                LST     #1, *                   ; load ST1
                CLRC    INTM
                RET

;=====================================================================
; S R   -       SYSINIT
; Description:  Initial the system parameter
;=====================================================================
SYSINIT:
                SETC    INTM                    ; Disable interrupts
                CLRC    SXM                     ; Clear Sign Extension Mode
                CLRC    OVM                     ; Reset Overflow Mode
                CLRC    CNF                     ; Config Block B0 to Data mem
                CLRC    XF

                LAR     AR1,#stack              ; Init context save stack pointer

                POINT_PF1                       ; DP for addresses 7000h-707Fh
                SPLK    #00BBh,CKCR1            ; CLKIN(OSC)=10MHz,CPUCLK=20MHz
                SPLK    #00C3h,CKCR0            ; CLKMD=PLL Enable,SYSCLK=CPUCLK/2
                SPLK    #40C0h,SYSCR            ; CLKOUT=CPUCLK

                SPLK    #006Fh, WDCR            ; Disable WD if VCCP=5V (JP5 in pos. 2-3)
                KICK_DOG                        ; Reset Watchdog

                SPLK    #0h,GPR0                ; Set wait state generator for:
                OUT     GPR0,WSGR               ; Program Space, 0 wait states
                                                ; Data Space, 0 wait states
                                                ; I/O Space, 0 wait states
                ;I/O setting p11-11
                POINT_PF2
                SPLK    #000fh, OCRA
                SPLK    #0076h, OCRB
```

```
                SPLK    #0, PBDATDIR        ; Configured as input

                LAR     AR2,#310h           ; Parameter for fuzzy control
                MAR     *,AR2
                SPLK    #0FFB0H,*+          ; -U3 --- -50H
                SPLK    #0FFD0H,*+          ; -U2 --- -30H
                SPLK    #0FFF0H,*+          ; -U1 --- -10H
                SPLK    #00030H,*+          ;  U1 ---  30H
                SPLK    #00010H,*+          ;  U2 ---  10H
                SPLK    #00050H,*           ;  U3 ---  50H

                LAR     AR2,#0320h          ; Parameter for speed PI control
                SPLK    #029H,*+
                SPLK    #029H,*+
                SPLK    #0,*

                LAR     AR2,#0328h          ; Parameter for current PI control
                SPLK    #029H,*+
                SPLK    #029H,*+
                SPLK    #0,*

                SPM     0                   ; No shift of PREG output
                RET

;=====================================================================
; S R   -       SYSINIT
; Description:  Initial the event management and ADC parameter
;=====================================================================
EV_INIT:
                POINT_EV
                ZAC
                SACL    T1CON               ; Clear register first
                SACL    T1PER
                SACL    T1CNT
                SACL    T1CMP
                SACL    T2CON
                SACL    T2PER
                SACL    T2CNT
                SACL    T2CMP
                SACL    T3CON
                SACL    T3PER
                SACL    T3CNT
                SACL    T3CMP
                SACL    COMCON
                SACL    DBTCON
                SACL    ACTR
                SACL    SACTR
                SACL    CMPR1
                SACL    CMPR2
                SACL    CMPR3
                SACL    SCMPR1
                SACL    SCMPR2
                SACL    SCMPR3
                SACL    CAPCON
                SPLK    #00ffh, CAPFIFO
                LACC    FIFO1
                LACC    FIFO2
                LACC    FIFO3

                ;PWM Unit setting
                SPLK    #0500,T1PER         ; 500 * 100ns = 50us
                SPLK    #0000h,T1CNT
                SPLK    #0FFDh,ACTR         ; Only use PWM1 output
                SPLK    #00000,CMPR1
                SPLK    #00000,CMPR2
                SPLK    #00000,CMPR3
                SPLK    #8287h,COMCON
                SPLK    #8287h,COMCON
                SPLK    #2800h,T1CON        ; Input clock prescaler = 1
                SPLK    #2840h,T1CON
                SPLK    #1830h,T2CON        ; Casecade to a 32-bit timer
                SPLK    #1870h,T2CON        ; Directional up/down count mode
                SPLK    #2820h,T3CON        ; Casecade to a 32-bit timer
                SPLK    #2860h,T3CON
                SPLK    #0E0F0h,CAPCON      ; Set capture 1,2 as QEP
                SPLK    #0FFh,CAPFIFO       ; Clear status register
                SPLK    #0100h,GPTCON       ; Start ADC by GP timer 1 event
```

```
                                        ; Setting of period interrupt flag

                ;Core Mask Setting
                POINT_PG0
                LACC    #02h            ; Unmask INT2 (Timer)
                SACL    IMR
                SPLK    #0ffffh,IFR

                ;EV Mask Setting, Vector & Flag reset p11-46
                POINT_EV
                SPLK    #0ffffh,IFRA    ; Clear event interrupt flag
                SPLK    #0ffffh,IFRB
                SPLK    #0ffffh,IFRC
                SPLK    #80h,IMRA       ; GP timer 1 period interrupt
                SPLK    #0,IMRB
                SPLK    #0,IMRC         ; Only no capture interrupt
                LACC    EVIVRA
                LACC    EVIVRB
                LACC    EVIVRC

                ;ADC Unit setting p3-8
                POINT_PF1
                SPLK    #0403h,ADCTRL2
                SPLK    #0385Ah,ADCTRL1 ; ADCIN0 and ADCIN8

                POINT_PG0               ; Variables initial
                ZAC
                SACL    SPEED_REF
                SACL    PreCode
                SACL    Idc_ref
                SACL    COMP
                SACL    SPEED_COUNT
                SACL    Direction
                SACL    SpeedSum
                SACL    CurrentSum
                SACL    Speed
                SACL    Current_Sample_No
                SACL    PreCodeH
                SACL    PreCodeL
                SACL    CurError        ; Current speed error
                SACL    PreError        ; Previous speed error
                SACL    dError          ; Differential of speed error
                SPLK    #1, Sel

                        RET

;=====================================================================
; S R   -       SPEED_REG
; Description:  Regulate the speed loop subrountine.
;
; Fuzzifier of input data
;
; Membership function of speed error
;
;    NB        NS     Z     PS      PB
;  _______             |           _______
;         \    /\    /|\    /\    /
;          \  /  \  / | \  /  \  /
;           \/    \/  |  \/    \/
;           /\    /\  |  /\    /\
;          /  \  /  \ | /  \  /  \
;         /    \/    \|/    \/    \
;  -------------------+---------------------->
;       -E2   -E1     0     E1    E2
;
; Membership function of differential speed error
;
;    NB        NS     Z     PS      PB
;  _______             |           _______
;         \    /\    /|\    /\    /
;          \  /  \  / | \  /  \  /
;           \/    \/  |  \/    \/
;           /\    /\  |  /\    /\
;          /  \  /  \ | /  \  /  \
;         /    \/    \|/    \/    \
;  -------------------+---------------------->
;      -dE2   -dE1    0    dE1    dE2
```

```
;
; Membership function of output
;
;         NB      NM      NS      Z     PS      PM      PB
;                                 |
;         ^       ^       ^       |      ^       ^       ^
;         |       |       |       |      |       |       |
;         |       |       |       |      |       |       |
;         |       |       |       |      |       |       |
;         |       |       |       |      |       |       |
;  ---------------------------+---------------------------->
;        -U3     -U2     -U1     0      U1      U2      U3
;=====================================================================

SPEED_REG
                KICK_DOG
                MAR     *,AR2
                LAR     AR2,#0330h
                POINT_EV
                LACC    T2CNT
                SACL    *+
                LACC    T3CNT, 16
                POINT_PG0
                SACH    *-
                LACL    *                   ; Read 32-bit timer
                SUB     PreCodeL
                SUBB    PreCodeL
                ABS
                SACL    Speed               ; Speed calculate
                LACC    *+
                SACL    PreCodeL
                LACC    *+
                SACL    PreCodeH            ; Save current count for next calculation

                SETC    SXM
                LACC    SPEED_REF
                SUB     Speed               ; Speed error calculation
                SACL    CurError
                SUB     PreError
                SACL    dError,5

                LACC    CurError
                ABS
                SUB     #75
                BLZ     FuzzyControl        ; |e| < el

                LACC    Sel
                BNZ     PI_CONTROL          ; Current controller is PI
                LACC    CurError
                ABS
                SUB     #100
                BLZ     FuzzyControl        ; |e| < eh & Sel = 0

PI_CONTROL
                LACC    CurError            ; Speed PI control
                MAR     *,AR2
                LAR     AR2,#0320h
                SACL    *+
                SUB     *+
                SACL    *
                LT      *-
                MPY     #KPw
                LTP     *-
                MPY     #KIw
                LTD     *
                ADD     Idc_ref
                SACL    Idc_ref
                B       LIM_REG

FuzzyControl
                SPLK    #0, Sel

                ; Initialization
                LAR     AR2,#308h
                MAR     *,AR2
                ZAC
```

```
                ; For speed error
                ; 300H, 301H  membership function index 1 & 2
                ; 0 -- NB   1 -- NS   2 -- Z
                ; 3 -- PS   4 -- PB
                ; 302H, 303H  membership 1 & 2

                ; For differential speed error NB, NS, Z, PS, PB
                ; 304H, 305H  membership function index 1 & 2
                ; 306H, 307H  membership 1 & 2

                ; For output membership NB, NM, NS, Z, PS, PM, PB
                SACL    *+                  ; NB  --  308H
                SACL    *+                  ; NM  --  309H
                SACL    *+                  ; NS  --  30AH
                SACL    *+                  ; Z   --  30BH
                SACL    *+                  ; PS  --  30CH
                SACL    *+                  ; PM  --  30DH
                SACL    *                   ; PB  --  30EH

                ; Fuzzification
                LAR     AR2,#300h
                LACC    CurError
                ABS
                SUB     #E1
                BGZ     PS_PB_E
                SPLK    #3,*+               ; PS
                SPLK    #2,*+               ; Z
                LACC    CurError
                ABS
                SFL                         ; x 2
                SACL    *+                  ; Membership of PS
                SUB     #MAX_E
                ABS
                SACL    *                   ; Membership of Z
                B       SYMBOL_E
PS_PB_E:
                LACC    CurError
                ABS
                SUB     #E2
                BGZ     PB_E
                SPLK    #4,*+               ; PB
                SPLK    #3,*+               ; PS
                LACC    CurError
                ABS
                SUB     #E1
                SACL    *+                  ; Membership of PB
                SUB     #MAX_E
                ABS
                SACL    *                   ; Membership of PS
                B       SYMBOL_E
PB_E:
                SPLK    #4,*+               ; PB
                SPLK    #3,*+               ; PS
                SPLK    #MAX_E,*+           ; PB
                SPLK    #0,*                ; PS
SYMBOL_E
                LACC    CurError
                BGZ     Ffuzi_dE            ; Symmetry of negative
                LAR     AR2, #300h
                LACC    #4
                SUB     *                   ; Change the membership index
                SACL    *+
                LACC    #4
                SUB     *
                SACL    *

Ffuzi_dE
                LAR     AR2, #304h
                LACC    dError
                ABS
                SUB     #dE1
                BGZ     PS_PB_dE
                SPLK    #3,*+               ; PS
                SPLK    #2,*+               ; Z
                LACC    dError
                ABS
                SFL                         ; x 2
```

```
                SACL    *+                  ; Membership of PS
                SUB     #MAX_dE
                ABS
                SACL    *                   ; Membership of Z
                B       SYMBOL_dE
PS_PB_dE:
                LACC    dError
                ABS
                SUB     #dE2
                BGZ     PB_dE
                SPLK    #4,*+               ; PB
                SPLK    #3,*+               ; PS
                LACC    dError
                ABS
                SUB     #dE1
                SACL    *+                  ; Membership of PB
                SUB     #MAX_dE
                ABS
                SACL    *                   ; Membership of PS
                B       SYMBOL_dE
PB_dE:
                SPLK    #4,*+               ; PB
                SPLK    #3,*+               ; PS
                SPLK    #MAX_dE,*+          ; PB
                SPLK    #0,*                ; PS
SYMBOL_dE
                LACC    dError
                BGZ     Inference           ; Symmetry of negative
                LAR     AR2, #304h
                LACC    #4
                SUB     *                   ; Change the membership index
                SACL    *+
                LACC    #4
                SUB     *
                SACL    *

Inference:
                LAR     AR0,#2
                LAR     AR2,#0304h
                LAR     AR3,#0300h
                LACC    *0+,3,AR3
                ADD     *0+,AR2             ; (304)*8+(300) => ACC
                ADD     #RuleTable
                TBLR    temp                ; Get index of output u
                LACC    #308H
                ADD     temp
                SACL    temp
                LAR     AR4,temp

                LACC    *,AR3               ; Inference engine, minimum rule
                SACL    temp
                SUB     *
                BLZ     Get_306
                LACC    *
                B       UpdateU
Get_306:
                LACC    temp
UpdateU:
                MAR     *,AR4
                SACL    *,AR2

                LAR     AR2,#0305h
                LAR     AR3,#0300h
                LACC    *0+,3,AR3
                ADD     *0+,AR2             ; (305)*8+(300) => ACC
                ADD     #RuleTable
                TBLR    temp                ; Get index of output u
                LACC    #308H
                ADD     temp
                SACL    temp
                LAR     AR4,temp

                LACC    *,AR3               ; Inference engine, minimum rule
                SACL    temp
                SUB     *
                BLZ     Get_307
                LACC    *
```

```
                B       UpdateU2
Get_307:
                LACC    temp
UpdateU2:
                SACL    temp
                MAR     *,AR4
                SUB     *
                BLZ     NextRule3
                LACC    temp
                SACL    *,AR2

NextRule3:
                LAR     AR2,#0304h
                LAR     AR3,#0301h
                LACC    *0+,3,AR3
                ADD     *0+,AR2             ; (304)*8+(301) => ACC
                ADD     #RuleTable
                TBLR    temp                ; Get index of output u
                LACC    #308H
                ADD     temp
                SACL    temp
                LAR     AR4,temp

                LACC    *,AR3               ; Inference engine, minimum rule
                SACL    temp
                SUB     *
                BLZ     Get_306_2
                LACC    *
                B       UpdateU3
Get_306_2:
                LACC    temp
UpdateU3:
                SACL    temp
                MAR     *,AR4
                SUB     *
                BLZ     NextRule4
                LACC    temp
                SACL    *,AR2

NextRule4:
                LAR     AR2,#0305h
                LAR     AR3,#0301h
                LACC    *0+,3,AR3
                ADD     *0+,AR2             ; (305)*8+(301) => ACC
                ADD     #RuleTable
                TBLR    temp                ; Get index of output u
                LACC    #308H
                ADD     temp
                SACL    temp
                LAR     AR4,temp

                LACC    *,AR3               ; Inference engine, minimum rule
                SACL    temp
                SUB     *
                BLZ     Get_307_2
                LACC    *
                B       UpdateU4
Get_307_2:
                LACC    temp
UpdateU4:
                SACL    temp
                MAR     *,AR4
                SUB     *
                BLZ     Defuzzifier
                LACC    temp
                SACL    *,AR2

Defuzzifier:
                MAR     *,AR2
                LAR     AR2,#0308h
                LAR     AR3,#0310h
                LACC    *+
                ADD     *+                  ; Sum of membership
                ADD     *+
                ADD     *+
                ADD     *+
                ADD     *+
```

```
                ADD     *
                SACL    temp

                LAR     AR2,#0308h          ; Sum of membership * boundary
                ZAC
                LT      *+,AR3
                MPY     *+,AR2
                LT      *+,AR3
                MPYA    *+,AR2
                LT      *0+,AR3             ; Skip Z
                MPYA    *+,AR2
                LT      *+,AR3
                MPYA    *+,AR2
                LT      *+,AR3
                MPYA    *+,AR2
                LT      *+,AR3
                MPYA    *+,AR2
                APAC                        ; Add the previous product to ACC

                SFR
                SACL    temp1
                ABS
                RPT     #15
                SUBC    temp                ; Division
                AND     #0FFFFH
                BIT     temp1,0
                BCND    UpdateIdc,NTC
                NEG
UpdateIdc:
                ADD     Idc_ref
                SACL    Idc_ref

LIM_REG
                ;reference current limitation
                BGZ     CURRENT_LIM
                SPLK    #0,Idc_ref              ; Minimum zero
                B       RESOTRE_IREF

CURRENT_LIM
                SUB     #MaxCurrent             ; Limit the reference current
                BLZ     RESOTRE_IREF
                SPLK    #MaxCurrent, Idc_ref

RESOTRE_IREF
                LACC    CurError
                SACL    PreError
                LACC    Idc_ref

                SPLK    #0,SPEED_COUNT          ; Reset Speed loop timer
                CLRC    SXM
                RET

;=====================================================================
; I S R  -      PHANTOM
; Description:  Dummy ISR, used to trap spurious interrupts.
;=====================================================================
PHANTOM
                KICK_DOG                    ;Resets WD counter
                B       PHANTOM

;=====================================================================
; Rule table
; dE\E    NB   NS   Z    PS   PB
;         |    |    |    |    |
;  NB  -  NB   NB   NM   NS   Z
;  NS  -  NB   NM   NS   Z    PS
;  Z   -  NM   NS   Z    PS   PM
;  PS  -  NS   Z    PS   PM   PB
;  PB  -  Z    PS   PM   PB   PB
;
;=====================================================================
RuleTable   .word               0           ; Line 1
            .word               0
            .word               1
            .word               2
            .word               3
            .word               0FFH        ; Padding
```

```
.word               0FFH
.word               0FFH
.word               0           ; Line 2
.word               1
.word               2
.word               3
.word               4
.word               0FFH        ; Padding
.word               0FFH
.word               0FFH
.word               1           ; Line 3
.word               2
.word               3
.word               4
.word               5
.word               0FFH        ; Padding
.word               0FFH
.word               0FFH
.word               2           ; Line 4
.word               3
.word               4
.word               5
.word               6
.word               0FFH        ; Padding
.word               0FFH
.word               0FFH
.word               3           ; Line 5
.word               4
.word               5
.word               6
.word               6
.word               0FFH        ; Padding
.word               0FFH
.word               0FFH
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H Novel Soft-Switching Inverter for Brushless DC Motor Variable Speed Drive System

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Novel Soft-Switching Inverter for Brushless DC Motor Variable Speed Drive System

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***Abstract*—Brushless dc motor has been widely used in industrial applications because of its low inertia, fast response, high power density, high reliability and maintenance-free. It is usually supplied by a hard-switching PWM inverter, which normally has low efficiency since the power losses across the switching devices are high. In order to reduce the losses, many soft switching inverters have been designed. Unfortunately, there are many drawbacks, such as high device voltage stress, large dc link voltage ripple, complex control scheme and so on. This paper introduces a novel soft-switching inverter which generates notches of the dc bus voltage becomes to zero during chopping switches commutation to guarantee all switches working in zero voltage state. The result of this investigation will be very useful for industrial applications.**

***Index Terms*—Brushless dc motor (BDCM), resonant dc link, soft switching, 12-switches inverter.**

I. Introduction

BRUSHLESS dc motor (BDCM) has been widely used in industrial applications because of its high power density, low inertia, fast response, high reliability and therefore maintenance-free. It is usually supplied by a hard-switching PWM inverter, which normally has low efficiency since the power losses across the switching devices are high. In order to reduce the losses, many soft switching inverters have been designed.

Soft switching operation of power inverter has attracted much attention in recent decade. In medium power applications, the resonant dc link concept [1] offered a first practical and reliable way to reduce commutation losses and to eliminate individual snubbers. Thus it allows high operating frequencies and improved efficiency. The inverter is quite simple to get the zero voltage switching (ZVS) condition of the six main inverter switches only by adding one auxiliary switch. However, the inverter has the drawbacks of high voltage stress of the switches, high voltage ripple of the dc link, discrete pulse modulation (DPM) other than PWM control. In order to overcome the drawback of high voltage stress of the switches, actively clamped resonant dc link inverter was introduced [2]. The control scheme of the inverter is too complex and the output contains subharmonic which, in some cases, cannot be accepted.

In order to generate notches of the dc link at controllable instants, several quasiparallel resonant schemes were proposed [3]–[5]. As a dwell time is generally required after every notch, severe interferences occur, mainly in multiphase inverters, appreciably worsening the modulation quality. A novel dc-rail parallel resonant zero voltage transition (ZVT) voltage source inverter [6] is introduced, it overcome many drawbacks mentioned above. However it requires two ZVT per PWM cycle, it would worsen the output and limit the switching frequency of the inverter.

The conventional three phase full wave inverter has the demerit of current ripple during commutation, thus the torque ripple of BDCM is high. Some authors [7]–[9] proposed some method to reduce torque ripple, but these methods show limited effectiveness in practical applications due to motor parameter sensitivity and dissatisfactory performance over wide speed range.

The paper proposed a novel resonant dc link inverter for BDCM. The topology of the soft-switching inverter is shown in Fig. 1. The system contains an uncontrolled rectifier, a resonant circuit, a 12-swtiches inverter and control circuit. The resonant circuit consists of three auxiliary switches (one IGBT S_L and two fast switching thyristors S_a, S_b), one resonant inductor and one resonant capacitor. All auxiliary switches work under ZVS or zero current switching (ZCS) condition. It can generate voltage notches of the dc link at controllable instants and width so that the main inverter switches $(S_1 - S_{12})$ of the inverter can get ZVS condition. The conventional quasiresonant procedure is divided into two half procedure for PWM operation. It has the merit of low voltage ripple of the dc link, low voltage stress of the switches and simple control schemes. In order to reduce torque ripple, the 12-switches inverter is introduced. The inverter comprises three single-phase inverters, and the three motor windings are connected to the three single-phase inverters respectively. The 12-switches inverter has other merit for motor drives not only for BDCM, but also for other ac motor such as induction motor, synchronous motor. Although the inverter requires more switching devices, for a given torque and speed, the voltage stress of the switches can reduce half, thus the total cost of the switching device would not increase. While the price of switching device has decreased significantly especially for medium and low power application and the cost of switches has lower proportion of the drive system. The control circuit contains speed controller, commutation logical circuit of the BDCM, auxiliary switches control circuit and gate signal drive.

II. Resonant Circuit

The resonant circuit consists of three auxiliary switches, one resonant inductor and one resonant capacitor. The auxiliary switches are controlled at certain instant to obtain the resonance between inductor and capacitor. Thus the dc link voltage

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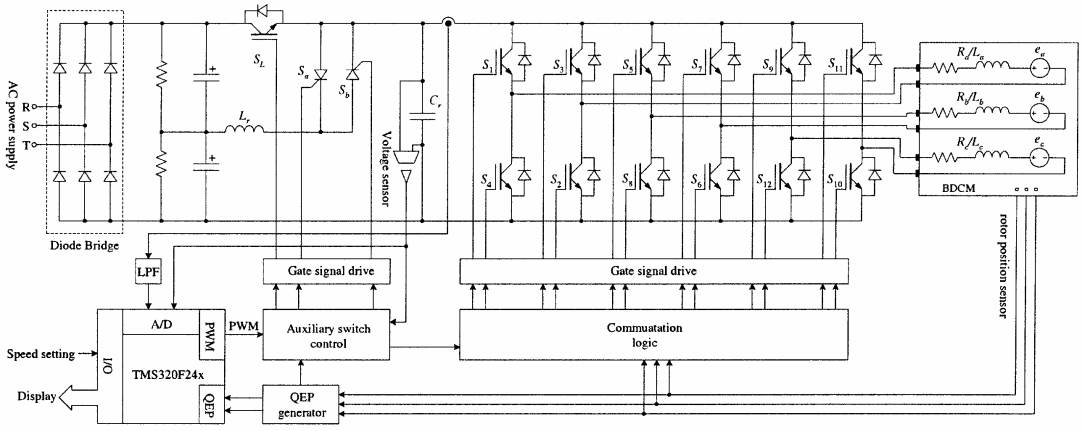

Fig. 1. Topology of soft-switching inverter for BDCM drive system.

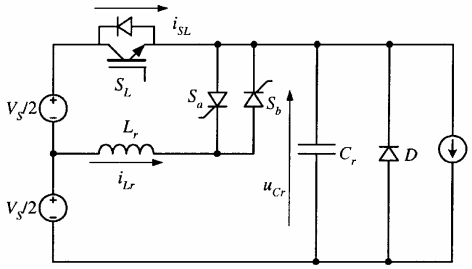

Fig. 2. Equivalent circuit.

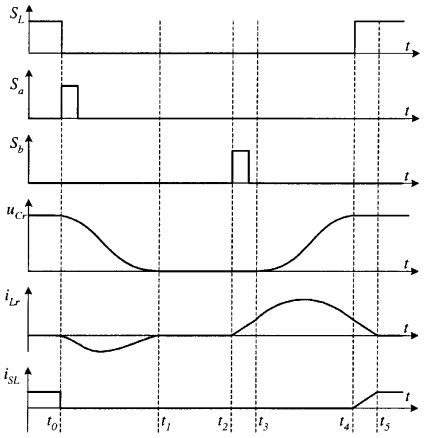

Fig. 3. Waveforms of simplified circuit.

reaches zero temporarily (voltage notch) and the main switches of the inverter get ZVS condition.

A. Operation Principle of the Resonant Circuit

Since the resonant procedure is very short, the load current can be assumed constant. The equivalent circuit is shown in Fig. 2. The corresponding waveforms of gate signal of auxiliary switches, resonant capacitor voltage (u_{Cr}), inductor current (i_{Lr}) and current of switch $S_L(i_{SL})$ are illustrated in Fig. 3. The dc link voltage reduce to zero and then rise to dc supply voltage again is called one zero voltage transition process or one dc link voltage notch, shortened for ZVT. The operation of the ZVT process can be divided into six modes.

Mode 0 [shown in Fig. 4(a)] $0 < t < t_0$. Its operation is the same as conventional inverter. Current flows from dc power supply through S_L to the load. The voltage across C_r (u_{Cr}) is equal to the supply voltage (V_S). The auxiliary switches S_a and S_b are in off state.

Mode 1 [shown in Fig. 4(b)] $t_0 < t < t_1$. When it is the instant for phase current commutation or PWM signal is flopped from "1" to "0," thyristor S_a is fired (ZCS turn on due to L_r) and IGBT S_L is turned off (ZVS turn off due to C_r) at the same time. Capacitor C_r resonates with inductor L_r, the voltage across capacitor C_r is decreased. Redefine the initial time we have the equation

$$\begin{cases} u_{Cr}(t) + R_{Lr} i_{Lr}(t) + L_r \frac{di_{Lr}(t)}{dt} = \frac{V_S}{2} \\ I_0 - i_{Lr}(t) + C_r \frac{du_{cr}(t)}{dt} = 0 \end{cases} \tag{1}$$

where R_{Lr} is the resistance of inductor L_r, I_0 is load current, V_S is the dc power supply voltage, with initial condition $u_{cr}(0) = V_S$, $i_{Lr}(0) = 0$, solve the (1), we get

$$\begin{cases} u_{Cr}(t) = \left(\frac{V_S}{2} - R_{Lr} I_0\right) + \left(\frac{V_S}{2} - R_{Lr} I_0\right) e^{-\frac{t}{\tau}} \cos(\omega t) + \frac{1}{L_r C_r \omega} \\ \qquad \times e^{-\frac{t}{\tau}} \left(\frac{1}{4} R_{Lr} C_r V_S - L_r I_0 + \frac{1}{2} R_{Lr}^2 C_r I_0\right) \sin(\omega t) \\ i_{Lr}(t) = I_0 - I_0 e^{-\frac{t}{\tau}} \cos(\omega t) - \frac{V_S + R_{Lr} I_0}{2 L_r \omega} e^{-\frac{t}{\tau}} \sin(\omega t) \end{cases} \tag{2}$$

where

$$\tau = \frac{2L_r}{R_{Lr}}, \quad \omega = \sqrt{\frac{1}{L_r C_r} - \frac{1}{\tau^2}}.$$

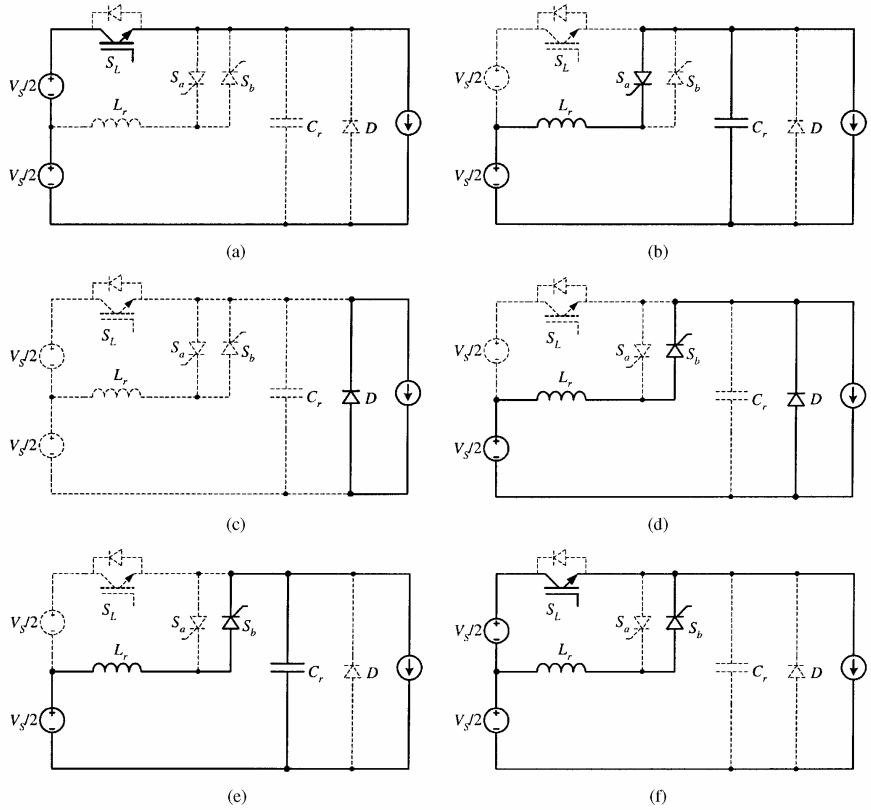

Fig. 4. Operation mode of the zero voltage transition. (a) Mode 0. (b) Mode 1. (c) Mode 2. (d) Mode 3. (e) Mode 4. (f) Mode 5.

As the resonant frequency is very high (several hundred kHz), $\omega L_r \gg R_{Lr}$, resonant inductor resistance R_{Lr} can be neglected. Then (2) can be simplified as

$$\begin{cases} u_{Cr}(t) = \frac{V_S}{2} + K\cos(\omega_r t + \alpha) \\ i_{Lr}(t) = I_0 - K\sqrt{\frac{C_r}{L_r}}\sin(\omega_r t + \alpha) \end{cases} \tag{3}$$

where

$$K = \sqrt{\frac{V_S^2}{4} + \frac{I_0^2 L_r}{C_r}}, \quad \omega_r = \sqrt{\frac{1}{L_r C_r}}, \quad \alpha = tg^{-1}\left(\frac{2I_0}{V_S}\sqrt{\frac{L_r}{C_r}}\right).$$

Let $u_{cr}(t) = 0$, we get

$$\Delta T_1 = t_1 - t_0 = \frac{\pi - 2\alpha}{\omega_r} \tag{4}$$

$i_{Lr}(t_1)$ is zero at the same time. Then the thyristor S_a is self turned-off.

Mode 2 [shown in Fig. 4(c)] $t_1 < t < t_2$. None of auxiliary switches is fired and the voltage of dc link (u_{cr}) is zero. The main switches of the inverter can be either turned on or turned off under ZVS condition during the interval. Load current flows through the freewheeling diode D.

Mode 3 [shown in Fig. 4(d)] $t_2 < t < t_3$. As the main switches have turned on or turned off, thyristor S_b is fired (ZCS turn on due to L_r) and i_{Lr} starts to build up linearly in the auxiliary branch. The current in the freewheeling diode D begins to fall linearly. The load current is slowly diverted from the freewheeling diodes to the resonant branch. But u_{Cr} is still equal to zero. We have

$$\Delta T_2 = t_3 - t_2 = \frac{2I_0 L_r}{V_S}. \tag{5}$$

At t_3, i_{Lr} equals the load current I_0 and the current through the diode becomes zero. Thus the freewheeling diode turns off under zero-current condition.

Mode 4 [shown in Fig. 4(e)] $t_3 < t < t_4$. i_{Lr} is increased continuously from I_0 and u_{Cr} is increased from zero when the freewheeling diode D is turned off. Redefine the initial time, we can get the same equation as (1). But the initial condition is $u_{Cr}(0) = 0$, $i_{Lr}(0) = I_0$, neglect the inductor resistance, solve the equation, we get

$$\begin{cases} u_{Cr}(t) = \frac{V_S}{2}[1 - \cos(\omega_r t)] \\ i_{Lr}(t) = I_0 + \frac{V_S}{2}\sqrt{\frac{C_r}{L_r}}\sin(\omega_r t) \end{cases} \tag{6}$$

when

$$\Delta T = t_4 - t_3 = \frac{\pi}{\omega_r} \tag{7}$$

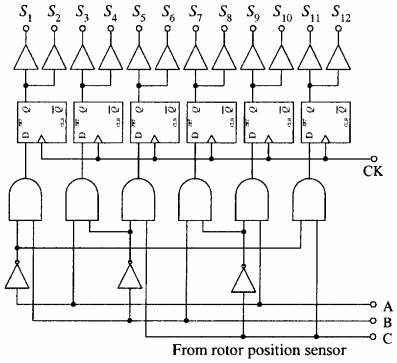

Fig. 5. Commutation logical circuit for main switches.

$u_{Cr} = V_S$, IGBT S_L is fired (ZVS turn on), $i_{Lr} = I_0$ again. The peak inductor current can be derived from (6), that

$$i_{Lr-m} = I_0 + \frac{V_S}{2}\sqrt{\frac{C_r}{L_r}}. \tag{8}$$

Mode 5 [shown in Fig. 4(f)] $t_4 < t < t_5$. When the dc link voltage is equal to the supply voltage, auxiliary switch S_L is turn on (ZVS turned on due to C_r). i_{lr} is decreased linear from I_0 to zero at t_5 and the thyristor S_b is self turned off.

Then go back to mode 0 again. The operation principle of the other procedure is the same as conventional inverter.

B. Commutation Logical Circuit and Control Circuit for Auxiliary Switches

When the duty of PWM is 100%, i.e. full duty cycle, the main switches of inverter work under the commutation frequency. When it is the instant to commutate the phase current of the BDCM, we control the auxiliary switches S_a, S_b, S_L and resonant occur between L_r and C_r. The voltage of dc link reach zero temporarily, thus ZVS condition of the main switches is obtained. When the duty of PWM is less than 100%, the auxiliary switch S_L works as a chop. The main switches of the inverter do not switch within a PWM cycle when the phase current needs not commutate. It has the benefit of reducing phase current drop during the PWM is off. The phase current is commutated during the dc link voltage becomes zero. So there is only one dc link voltage notch per PWM cycle. It is very important especially for very low or very high duty of PWM. Otherwise the interval between two voltage notches is very short even overlapped which will limit the tuning range.

The commutation logical circuit of the system is shown in Fig. 5. It is similar to conventional BDCM commutation logical circuit except adding six D flip-flops to the output. Thus the gate signal of the main switches is controlled by pulse CK that will be mentioned late. The operation of the inverter can be divided into full duty cycle operation and PWM operation.

1) Full Duty Cycle Operation: When the duty of PWM is 100%, i.e. full duty cycle, the whole ZVT process (mode 0–mode 5) occurs when the phase current commutation is on going. The control scheme for the auxiliary switches in this operation is illustrated in Fig. 6(a). When mode 1 begins, pulse signal for thyristor S_a is generated by a monostable flip-flop

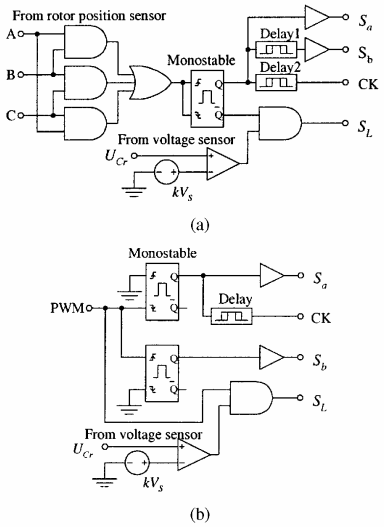

Fig. 6. Control scheme for the auxiliary switches: (a) in full duty cycle operation and (b) in PWM operation.

and gate signal for IGBT S_L is dropped to low level (i.e., turn off the S_L) at the same time. Then, pulse signal for thyristor S_b and pulse CK can be obtained after two short delays (delay1 and delay2 respectively). Obviously delay1 is longer than delay2. Pulse CK is generated during mode 2 when the voltage of dc link is zero and the main switches of the inverter get ZVS condition. Then modes 3,4,5 occur, the voltage of dc link is increased to that of supply again.

2) PWM Operation: In this operation the auxiliary switch S_L works as chop, but the main switches of the inverter do not turn on or turn off within a PWM cycle when the phase current needs not commutate. The load current is commutated during the dc link voltage becomes to zero, i.e. when PWM signal is "0" (As the PWM cycle is very short, it does not affect the operation of the motor). The control scheme for the auxiliary switches in PWM operation is illustrated in Fig. 6(b).

- When PWM signal is flopped from "1" to "0 ," mode 1 begins, pulse signal for thyristor S_a is generated and gate signal for IGBT S_L is dropped to low level. But the voltage of dc link does not increase until PWM signal is flipped from "0" to "1." Pulse CK is generated during mode 2.
- When PWM signal is flipped from "0" to "1," mode 3 begins, pulse signal for thyristor S_b is generated at the moment (mode 3). Then when the voltage of the dc link is increased to supply voltage V_S, the gate signal for IGBT S_L is flipped to high level (Modes 4 and 5).

Thus, only one ZVT occurs per PWM cycle: mode 1,2 for PWM turned off, modes 3,4,5 for PWM turned on. And the switching frequency would be not greater than PWM frequency.

III. Operation Principle of the 12-Switches Inverter

A. Commutation Process With Conventional Inverter

Assumption the rotor reluctance of BDCM is constant independent rotor position θ_r and only the fundamental components of the flux linkages contributed by the permanent magnet are

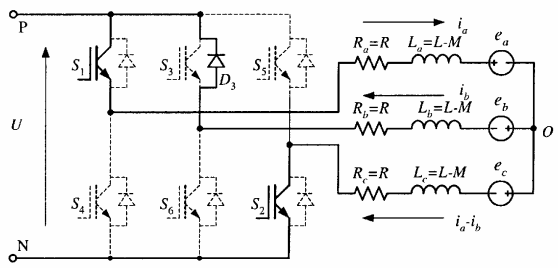

Fig. 7. Equivalent circuit during commutation.

considered. Then the mathematical model of the BDCM can be expressed as [10]

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} L & M & M \\ M & L & M \\ M & M & L \end{bmatrix} p \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \tag{9}$$

where R is the phase resistance, L is phase inductance, M is the mutual inductance, v is the phase voltage, i is the phase current, e is the phase back EMF, and p is the derivational operator (d/dt).

For Y-connected BDCM with conventional three-phase full wave inverter, the (9) can be changed to

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} L-M & 0 & 0 \\ 0 & L-M & 0 \\ 0 & 0 & L-M \end{bmatrix} \times p \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \tag{10}$$

$$T_e = \frac{(e_a i_a + e_b i_b + e_c i_c)}{\omega_r} \tag{11}$$

so the equivalent circuit of the BDCM drive system during commutation can be simplified as Fig. 7 (Assume commutation from $+\mathrm{A}-\mathrm{B} => +\mathrm{A}-\mathrm{C}$, "+" means current flow from the positive pole of supply, "−" means current flow to the negative pole).

Neglect the voltage drop across switches and diodes, the governed voltage and current equation can be obtained [11]

$$\begin{cases} U = i_a R_a + L_a \frac{di_a}{dt} + e_a + e_c + L_c \frac{d(i_a - i_b)}{dt} + (i_a - i_b) R_c \\ i_a R_a + L_a \frac{di_a}{dt} + e_a + e_b + L_b \frac{di_b}{dt} + i_b R_b = 0 \end{cases} \tag{12}$$

where $R_a = R_b = R_c = R$, $L_a = L_b = L_c = L - M$, $e_a = e_b = e_c = e$. For approximate solution, assume the circuithas reached the steady state before commutation, we have the equation as conventional dc motor

$$U = 2IR + 2e. \tag{13}$$

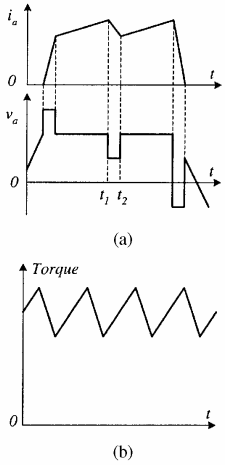

Fig. 8. Waveforms of phase current, phase voltage and torque with conventional inverter. (a) Phase A current and voltage. (b) Torque.

With the initial value $i_{a0+} = I$, $i_{b0+} = I$ (I is the current of dc link) and (13) solve the (12) obtain

$$\begin{cases} i_a = \left(\frac{4}{3}I - \frac{U}{3R}\right) + \left(\frac{U}{3R} - \frac{1}{3}I\right) e^{-\frac{R}{L-M}t} \\ i_b = \left(\frac{2}{3}I - \frac{2U}{3R}\right) + \left(\frac{2U}{3R} + \frac{1}{3}I\right) e^{-\frac{R}{L-M}t} \end{cases}. \tag{14}$$

The phase voltage during commutation can be obtained from (13)

$$\begin{cases} v_a = v_b = v_{PO} = \frac{U}{6} + \frac{1}{3}IR \\ v_c = v_{ON} = \frac{5U}{6} - \frac{1}{3}IR. \end{cases} \tag{15}$$

Thus we can sketch the waveform of current and voltage of phase A as Fig. 8(a) and waveform of torque as Fig. 8(b). From the figure we can see that the current ripple of phase A is the cause of commutation, the phase voltage is decreased between t_1 and t_2. Maintaining the uncommutation phase voltage to be constant, the current ripple can be eliminated, and the torque ripple can be reduced. For this purpose, half wave inverter can be used, such as conventional half-wave inverter, Miller inverter, Buck-fronted inverter and C-dump inverter [12]. But the efficiency of the motor is low with these inverters for there is only one winding conduct at the same time. So the 12-switches inverter is introduced.

B. Commutation Process With 12-Switches Inverter

The topology of the inverter is shown in Fig. 9. It consists of three single-phase inverters and the three armatures of the motor connect to them respectively. Thus phase current can be controlled independently and not affected by other phase commutation procedure.

Also assume phase current commutates from $+\mathrm{A}-\mathrm{B} => +\mathrm{A}-\mathrm{C}$ (turn off S_7, S_8; turn on S_{11}, S_{12}). With the 12-switches inverter, two independent governed voltage and current equations of the phase B,C can be obtained (current of phase A is not affected by commutation)

$$\begin{cases} U = R_b i_b + L_b \frac{di_b}{dt} + e_b \\ -U = R_c i_c + L_c \frac{di_c}{dt} + e_c. \end{cases} \tag{16}$$

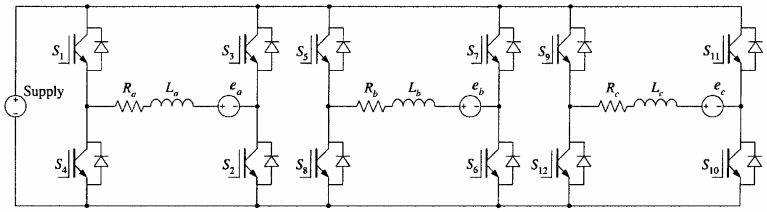

Fig. 9. Topology of 12-switches inverter.

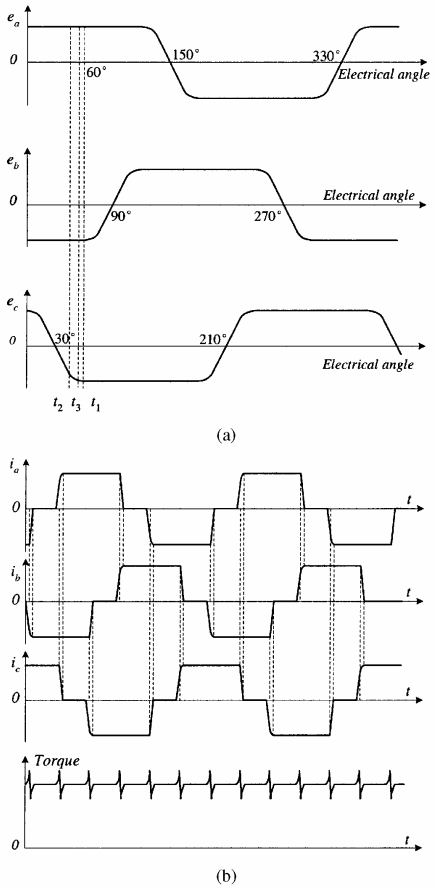

Fig. 10. Waveforms of back EMF, phase current and torque with 12-switches inverter. (a) Back EMF of trapezoidal BDCM. (b) Phase current and torque.

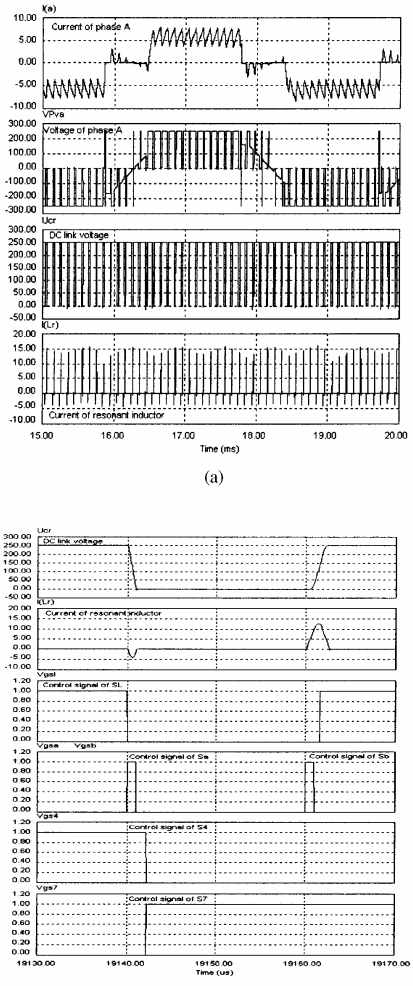

Fig. 11. Simulation result of the soft switching inverter with PWM. (a) Waveforms of i_a, v_a, u_{Cr}, i_{Lr}. (b) Zoom in waveforms of u_{Cr}, i_{Lr} and switches gate signal.

For trapezoidal BDCM, the waveform of the back EMF is shown in Fig. 10(a). If the commutation occurs at time t_1, with the initial condition $i_{b0+} = -I$, $i_{c0+} = 0$, $e_b \approx e_c = -(U - IR)$, solve the equation, obtain

$$\begin{cases} i_b = \frac{2U}{R} - I + \frac{2U}{R} e^{-\frac{R}{L-M}t} \\ i_c = I\left(1 - e^{-\frac{R}{L-M}t}\right). \end{cases} \tag{17}$$

i_b can reduce to zero very quickly, but the i_c increases very slowly. In order to shorten the commutation procedure, S11, S12 are turned on at t_2, S7, S8 are turned off at t_3, then i_c can increase quicker. As the back EMF Vs time (or electrical degree) is a continuous function, there exists an instant t_2 that i_c can reach the steady value at t_1. So the phase current is smoother, and the motor torque is reduced [as shown in Fig. 10(b)].

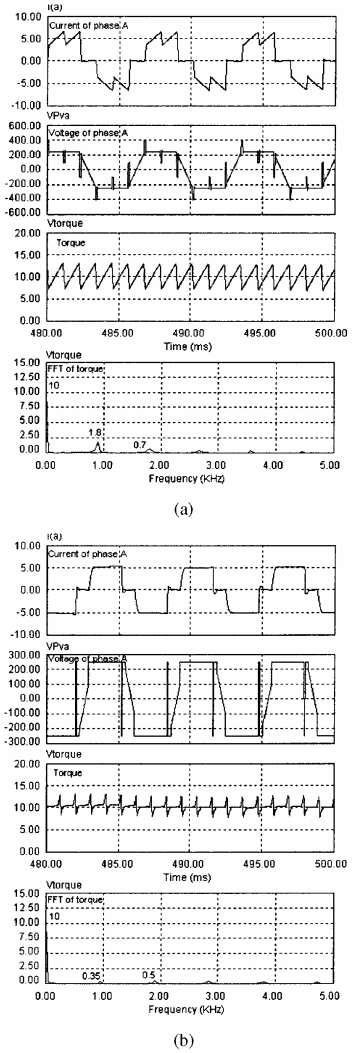

Fig. 12. Simulation result of conventional inverter versus 12-switches inverter. (a) Waveforms in conventional three-phase full wave inverter. (b) Waveforms in 12-swtiches inverter.

The 12-switches inverter not only reduces the torque ripple significantly, includes the merit of the conventional three phase full wave inverter and half wave inverter, but has other merit as follows.

- For a given supply voltage, the current flows through one winding only other than two windings in conventional inverter, so it can offer twice phase current and torque. The supply only needs to get over back EMF of one phase, so the speed of the motor is also doubled.
- For a given motor speed, it only requires half supply voltage, so the voltage stress of switching device is reduced half. It is easier to select required device and the price of two low voltage stress devices is lower than that of one high voltage stress device. The insulation class requirement can be also reduced.

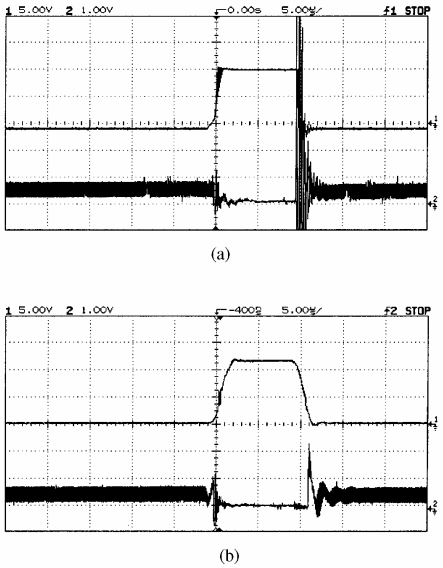

Fig. 13. Voltage and current waveforms of switch S_L in hard switching and soft switching inverter. (a) Switch voltage and current with hard switching (10 A/div). (b) switch voltage and current with soft switching (10 A/div).

- The inverter is applicable to other motors such as induction motor, synchronous motor, and no deadbeat time is required.
- The phase current can be controlled more flexible.

IV. Simulation and Experiment Result

The simulation results of soft-switching inverter with PWM operation by Psim is shown in Fig. 11. The waveforms of phase current (i_a), phase voltage (v_a), dc link voltage (u_{Cr}) and resonant inductor current (i_{Lr}) are shown in Fig. 11(a). The zoom in waveforms of dc link voltage, resonant inductor current and switches gate signal are shown in Fig. 11(b). The dc link voltage is 250 V, the switching frequency is 10 kHz, the resonant inductor is 10 μH, the resonant capacitance is 0.047 μF. From the zoom in waveforms we can see that the simulation results matches the theoretical analysis in Section II, the switch S_4 is turned off and switch S_7 is turned on during the dc link voltage is zero.

The simulation results of phase current, phase voltage, torque and FFT of torque in conventional three-phase full wave inverter and 12-switches inverter are also shown in Fig. 12. The waveforms in Fig. 12(a) are with conventional three-phase full wave inverter, and supply voltage is 500 V; waveforms in Fig. 12(b) are with 12-switches inverter, and supply voltage is 250 V. From the simulation results we can see that average torques in the two inverters are almost the same, the first order of torque harmonics is much less in 12-switches inverter than that of in conventional inverter, so the torque ripple with 12-switches reduces significantly. The magnitude of phase current and torque with the two inverters is the same, the speed is also same, but the supply voltage of former is twice as that of later.

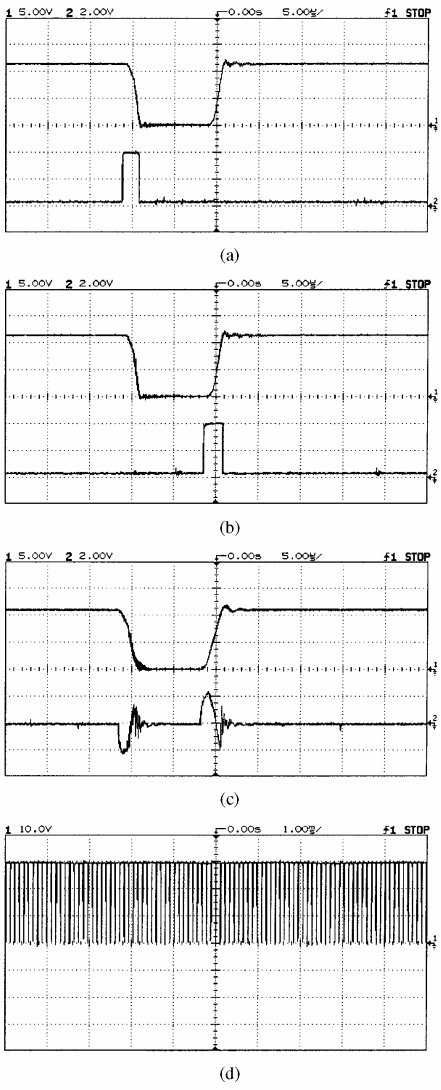

Fig. 14. Key experiment waveforms of the soft switching inverter: (a) u_{cr} and S_a gate signal, (b) u_{cr} and S_b gate signal, (c) u_{cr} and i_{Lr}, and (d) u_{cr} (Zoom out).

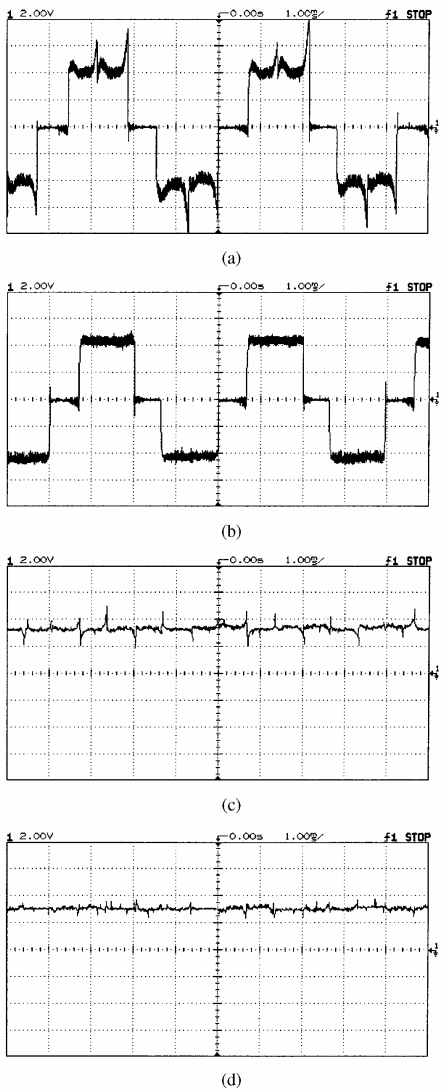

Fig. 15. Experimental result of conventional inverter versus 12-switches inverter. (a) Phase current in conventional inverter (5 A/div). (b) Phase current in 12-switches inverter (5 A/div). (c) Torque in conventional inverter (5 N.m/div). (d) Torque in 12-switches inverter (5 N.m/div).

In order to verify the theoretical analysis and simulation results. The proposed soft switching inverter was tested on an experimental prototype. A polyester capacitor of 47 nF, 1500 V was adopted as dc link resonant capacitor C_r. The resonant inductor was of 6 μH/30 A with ferrite core. The design of the auxiliary switches control circuit was referenced from Fig. 6. The waveforms of voltage across switch and current under hard switching and soft switching are shown in Fig. 13. All the voltage signals come from differential probe, and there is a gain of 20. For voltage waveform, 5.00 V/div in oscilloscope represents 100 V/div, which is the same for Fig. 14. It can be seen that there is a considerable overlap between the voltage and current waveforms during the switching under hard switching. The overlap is much less with soft switching and the switching power loss is smaller. A serial of key waveforms with soft switching inverter is shown in Fig. 14. The default scale is: dc link voltage: 100 V/div, current: 20 A/div. The default switching frequency is 10 kHz. The dc link voltage is fixed to 240 V. These experimental waveforms are coincident with the simulation waveforms in Fig. 11.

Two inverters are set up to compare the performance of the 12-switches inverter and conventional three-phase inverter. A customizing 2.2 kW customizing BDCM with all stator windings terminal connected external is introduced in this experiment. The shaft of the motor is clutched to variable load with torque probe. The phase current and torque waveforms in the two inverters are shown in Fig. 15. From the figure we can see

that the phase current in 12-switches inverter is not affected by the commutation of other phase and torque is less ripple than that of three-phase inverter [13]–[15].

V. Conclusion

A novel soft switching inverter for BDCM variable speed drives systems is proposed. Operation principles, analysis and simulation experiment result are also illustrated.

1) All switches work under soft-switching condition, so their power losses are small. Only one dc link voltage notch is needed for every PWM cycle. Simple auxiliary switches control scheme.
2) Torque ripple of motor is reduced significantly. For a given voltage of supply, torque and speed of the motor are doubled. For a given speed of the motor, the voltage stress of switching device is reduced half, the insulation class requirement can be also reduced. The inverter is also applicable to induction motor.

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I Novel Resonant Pole Inverter for Brushless DC Motor Drive System

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Novel Resonant Pole Inverter for Brushless DC Motor Drive System

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***Abstract*—The brushless dc motor (BDCM) has been widely used in industrial applications because of its low inertia, fast response, high power density, high reliability, and maintenance-free reputation. It is usually supplied by a hard-switching pulse width modulation inverter, which normally displays relative low efficiency since the power losses across the switching devices are high. In order to reduce the losses, many soft switching inverters have been designed. However, these inverters have such disadvantages as high device voltage stress, large dc link voltage ripple, discrete pulse modulation, and complex control scheme. This paper introduces a novel resonant pole inverter, which is unique to a BDCM drive system, and is easy to implement. The inverter possesses the advantages of low switching power loss, low inductor power loss, low device voltage stress, and simple control scheme. The operation principle of the inverter is analyzed. Simulation and experimental results are proposed to verify the theoretical analysis.**

***Index Terms*—Brushless dc motor (BDCM), resonant pole inverter, soft switching, zero-current-switching (ZCS), zero-voltage switching (ZVS).**

I. Introduction

THE brushless dc motor (BDCM) has been widely used in industrial applications because of its low inertia, fast response, high power density, high reliability, and maintenance-free reputation. It exhibits the operating characteristics of a conventional commutated dc permanent magnet motor but eliminates the mechanical commutators and brushes. Hence, many problems associated with brushes are eliminated, such as radio-frequency interfenrence and sparking which is the potential source of ignition in inflammable atmosphere. It is usually supplied by a hard-switching pulse width modulation (PWM) inverter, which normally has relative low efficiency since the power losses across the switching devices are high. The high dv/dt and di/dt will result in severe electromagnetic interference (EMI) and severe problems with the reverse recovery of the freewheeling diodes, especially in high switching frequency. As the switching frequency of the hard switching is not very high when the switching frequency is within audio spectrum, it may produce severe acoustic noise. Furthermore, there is "turning off current spike" for inductive load or "turning on voltage spike" for capacitive load with a hard switching inverter, which can produce excessive localized hot spots to damage power semiconductor switches. In order to solve these problems, many soft switching inverters have been designed.

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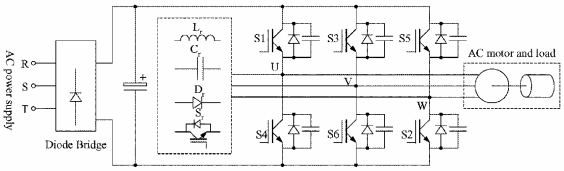

Fig. 1. Resonant pole inverter.

Soft switching operation of the power inverter has attracted much attention in the recent decades. In electric motor drive applications, soft-switching inverters are usually classified into three categories, namely, resonant pole inverter, resonant dc link inverter, and resonant ac link inverter [1]. Resonant ac link inverter is not suitable to BDCM drivers. Resonant dc link inverter [2], [3] has disadvantages such as high voltage stress of the switches, high dc link voltage ripple, and large resonant inductor power losses. It is with discrete pulse modulation (DPM) control that it is hard to achieve real PWM control and will result in sub-harmonics. Several quasiparallel resonant dc link inverters were designed to solve these problems, but these inverters require an additional main conduction path switch, which will increase the conduction power losses of the inverter [4], [5]. Other problems with the resonant dc link are such that whichever phase is needed to commutate, the dc link voltage is reduced to zero temporarily, which will affect the operation of other phases.

The structure of the resonant pole inverter [6]–[11] is shown in Fig. 1. Each resonant pole comprises a resonant inductor and a pair of resonant capacitors at each phase leg. These capacitors are directly connected in parallel to the main inverter switches in order to achieve zero-voltage switching (ZVS) condition. In contrast to the resonant dc link inverter, the dc link voltage remains unaffected during the resonant transitions. The resonant transitions occur separately at each resonant pole when the corresponding main inverter switch needs switching. Therefore, the main switches in the inverter phase legs can switch independently from each other and choose the commutation instant freely. Moreover, there is no additional main conduction path switch. Thus, the normal operation of the resonant pole inverter is entirely the same as that of the conventional hard switching inverter.

The auxiliary resonant commutated pole (ARCP) inverter [6] and the ordinary resonant snubber inverter [7] provide a ZVS condition without increasing the device voltage and current stress. These inverters are able to achieve real PWM control. However, they require a stiff dc link capacitor bank that is center-taped to accomplish commutation. The center voltage of dc link is susceptible to drift that may affect the operation of the resonant circuit. The resonant transition inverter [8], [9]

only uses one auxiliary switch, whose switching frequency is much higher than that applying to the main switches. Thus, it will limit the switching frequency of the inverter. Furthermore, the three resonant branches of the inverter work together and will be affected by each other. A Y-configured resonant snubber inverter [10] has a floating neutral voltage that may cause overvoltage failure of the auxiliary switches. A delta (Δ) configured resonant snubber inverter [11] avoids the floating neutral voltage and is suitable for multiphase operation without circulating currents between the off-state branch and its corresponding output load. However, the inverter requires three inductors and six auxiliary switches.

Moreover, resonant pole inverters have been applied in induction motor drive applications. They are usually required to change two phase switch states at the same time to obtain a resonant path. It is not suitable for a BDCM drive system as only one switch is needed to change the switching state in a PWM cycle. The switching frequency of three upper switches (S_1, S_3, S_5) is different than that of three lower switches (S_4, S_6, S_2) in an inverter for a BDCM drive system. All the switches have the same switching frequency in a conventional inverter for induction motor applications. Therefore, it is necessary to develop a novel topology of soft-switching inverter and special control circuit for BDCM drive systems. This paper proposes a special designed resonant pole inverter that is suitable for BDCM drive systems and is easy to apply in industry. In addition, this inverter possesses the following advantages: low switching power losses, low inductor power losses, low switching noise, and simple control scheme.

II. Topology of the Resonant Pole Inverter

A typical controller for BDCM drive system [12] is shown in Fig. 2. The rotor position can be sensed by a Hall-effect sensor or a slotted optical disk, providing three square-waves with phase shift in 120°. These signals are decoded by a combinatorial logic to provide the firing signals for 120° conduction on each of the three phases. The basic forward control loop is voltage control implemented by PWM (voltage reference signal compare with triangular wave or generated by microprocessor). The PWM is applied only to the lower switches. This not only reduces the current ripple but also avoids the need for wide bandwidth in the level-shifting circuit that feeds the upper switches. The three upper switches work under commutation frequency (typical several hundred Hz) and the three lower switches work under PWM frequency (typical tens of kHz). So it is not important that the three upper switches work under soft switching condition. The switching power losses can be reduced significantly and the auxiliary circuit would be simpler if only three lower switches work under soft switching condition. Thus a special design resonant pole inverter for BDCM drive system is introduced for this purpose. The structure of the proposed inverter is shown in Fig. 3.

The system contains a diode bridge rectifier, a resonant circuit, a conventional three-phase inverter, and control circuitry. The resonant circuit consists of three auxiliary switches (S_a, S_b, S_c), one transformer with turn ratio $1 : n$, and two diodes D_{fp}, D_r. Diode D_{fp} is connected in parallel to the primary winding of the transformer, diode D_r is serially connected with secondary winding across the dc link. There is one snubber capacitor connected in parallel to each lower switch of phase leg. The snubber capacitor resonates with the primary winding

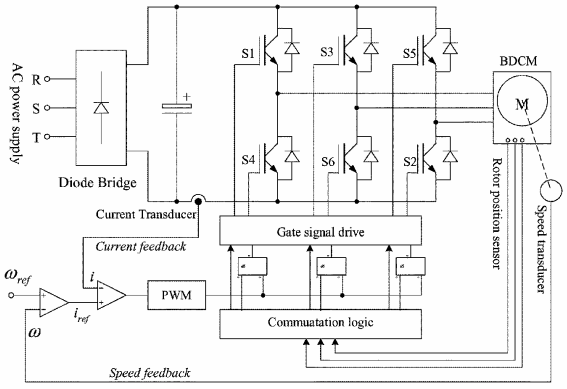

Fig. 2. Typical controller for BDCM drive system.

of the transformer. The emitters of the three auxiliary switches are connected together. Thus, the gate drive of these auxiliary switches can use one common output dc power supply.

In a whole PWM cycle, the three lower switches (S_4, S_6, S_2) can be turned off in the ZVS condition as the snubber capacitors (C_{ra}, C_{rb}, C_{rc}) can slow down the voltage rise rate. The turn-off power losses can be reduced and the turn off voltage spike is eliminated. Before turning on the lower switch, the corresponding auxiliary switch (S_a, S_b, S_c) must be turned on ahead. The snubber capacitor is then discharged and the lower switches get the ZVS condition. During phase current commutation, the switching state is changed from one lower switch to another, e.g., turn off S_6 and turn on S_2, S_6 can be turned off directly in the ZVS condition, turning on auxiliary switch S_c to discharge the snubber capacitor C_{rc} then switch S_2 can get the ZVS condition. During phase current commutation, if the switching state is changed from one upper switch to another upper switch, the operation is the same as that of the hard switching inverter, as the switching power losses of the upper switches is much smaller than that of the lower switches.

III. Operation Principle

For convenience sake, to describe the operation principle, we investigate the period of time when the switch S_1 is always turned on, when switch S_6 works under PWM frequency, and when other main inverter switches are tuned off. Since the resonant transition is very short, it can be assumed that the load current is constant. The equivalent circuit is shown in Fig. 4. Where V_S is the dc link voltage, i_{Lr} is the transformer primary winding current, u_{S6} is the voltage drop across the switch S_6 (i.e., snubber capacitor C_{rb} voltage), and I_0 is the load current. The waveforms of the switches (S_6, S_b) gate signal, PWM signal, main switch S_6 voltage drop (u_{S6}), and the transformer primary winding current (i_{Lr}) are illustrated in Fig. 5, and details will be explained as follows. Accordingly, the instant t_0–t_6, the operation of one switching cycle can be divided into seven modes.

Mode 0 [Shown in Fig. 6(a)] $0 < t < t_0$*:* After the lower switch S_6 is turned off, load current flows through the upper freewheeling diode D_3, the voltage drop u_{S6} (i.e., snubber capacitor C_{rb} voltage) across the switch S_6 is the same as that

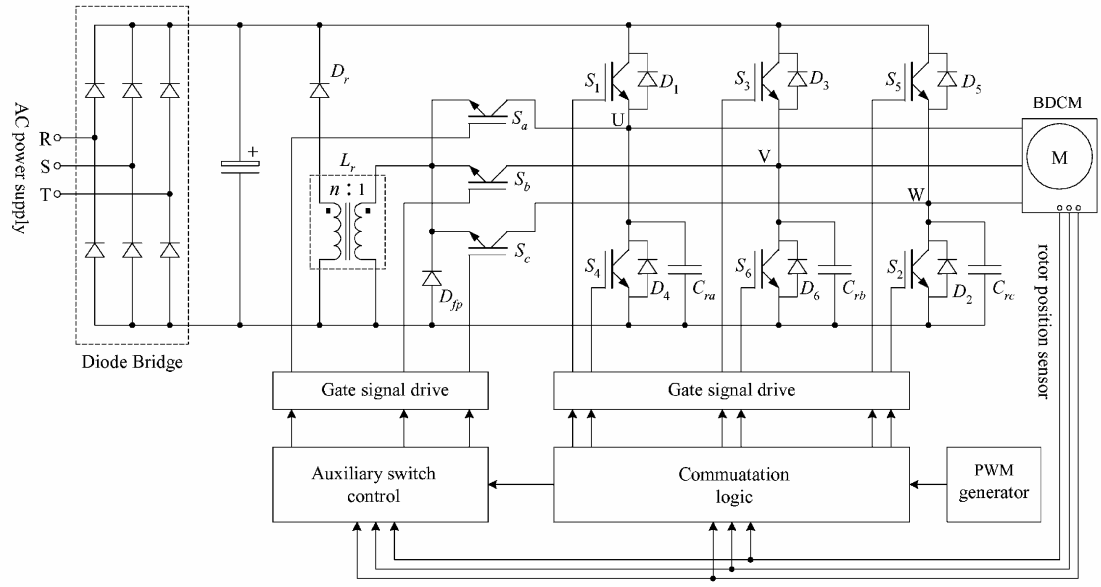

Fig. 3. Structure of the resonant pole inverter for BDCM drive system.

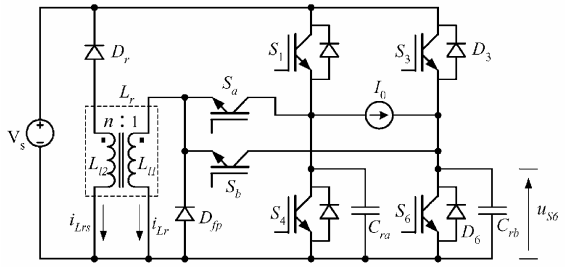

Fig. 4. Equivalent circuit.

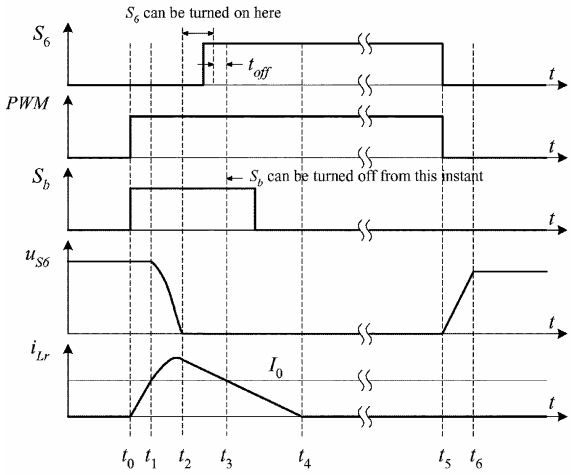

Fig. 5. Key waveforms of the equivalent circuit.

of the dc link voltage. The auxiliary resonant circuit does not operate.

Mode 1 [Shown in Fig. 6(b)] $t_0 < t < t_1$: If the switch S_6 is turned on directly, the capacitor discharge surge current will also flow through switch S_6, thus, switch S_6 may face the risk of second breakdown. The energy stored in the snubber capacitor must be discharged ahead of time. Thus, auxiliary switch S_b is turned on (ZCS turn on as the i_{Lr} cannot change suddenly due to the transformer inductance). As the transformer primary winding current i_{Lr} begins to increase, the current flowing through the freewheeling diode D_3 decays. The secondary winding current i_{Lrs} also begins to conduct through diode D_r to the dc link. Both of the terminal voltages of the primary and secondary windings are equal to the dc link voltage V_S. By neglecting the resistances of the windings and using the transformer equivalent circuit (referred to the primary side) [13], we get

$$V_S = L_{l1}\frac{di_{Lr}(t)}{dt} + a^2 L_{l2}\frac{d[i_{Lrs}(t)/a]}{dt} + aV_S \qquad (1)$$

where L_{l1} and L_{l2} are the primary and secondary winding leakage inductance, respectively, a is the transformer turn ratio $1:n$. The transformer has a high magnetizing inductance. We can assume that $i_{Lrs} = i_{Lr}/n$, and rewrite (1) as

$$\frac{di_{Lr}}{dt} = \frac{(n-1)V_S}{n\left(L_{l1} + \frac{1}{n^2}L_{l2}\right)} = \frac{(n-1)V_S}{nL_r} \qquad (2)$$

where L_r is the equivalent inductance of the transformer $L_{l1} + L_{l2}/n^2$. The transformer primary winding current i_{Lr} increases linearly and the mode is ended when $i_{Lr} = I_0$. The interval of this mode can be determined by

$$\Delta t_1 = t_1 - t_0 = \frac{nL_r I_0}{(n-1)V_S}. \qquad (3)$$

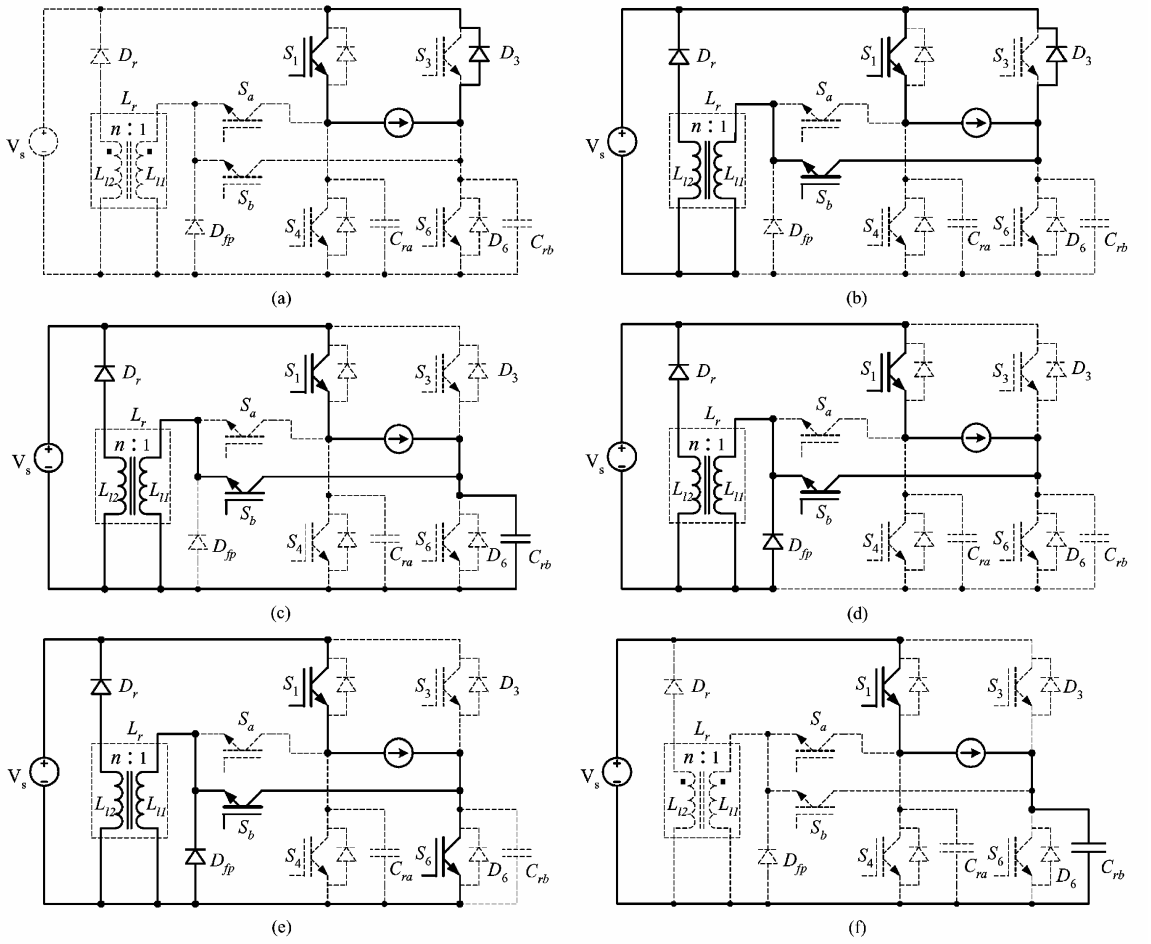

Fig. 6. Operation modes of the resonant pole inverter. (a) Mode 0. (b) Mode 1. (c) Mode 2. (d) Mode 3. (e) Mode 4. (f) Mode 6.

Mode 2 [Shown in Fig. 6(c)] $t_1 < t < t_2$: At $t = t_1$, all load current flows through the transformer primary winding, the freewheeling diode D_3 is turned off in the ZCS condition. The freewheeling diode reverse recovery problems are reduced greatly. The snubber capacitor C_{rb} resonates with the transformer, and the voltage drop u_{S6} across switch S_6 decays. By redefining the initial time, the transformer current i_{Lr}, i_{Lrs} and capacitor voltage u_{S6} obey the equation

$$\begin{cases} u_{S6}(t) = L_{l1}\dfrac{di_{Lr}(t)}{dt} + a^2 L_{l2}\dfrac{d[i_{Lrs}(t)/a]}{dt} + aV_S \\ -C_r\dfrac{du_{S6}(t)}{dt} = i_{Lr}(t) - I_0 \end{cases} \tag{4}$$

where C_r is the capacitance of snubber capacitor C_{rb}. The transformer current $i_{Lrs} = i_{Lr}/n$, as in mode 1, with initial conditions $u_{S6}(0) = V_S, i_{Lr}(0) = I_0$, then the solution of (4) is

$$\begin{cases} u_{S6}(t) = \dfrac{(n-1)V_S}{n}\cos(\omega_r t) + \dfrac{V_S}{n} \\ i_{Lr}(t) = I_0 + \dfrac{(n-1)V_S}{n}\sqrt{\dfrac{C_r}{L_r}}\sin(\omega_r t) \end{cases} \tag{5}$$

where $\omega_r = \sqrt{(1/(L_r C_r))}$. Let $u_{Cr}(t) = 0$, which gets the duration of the resonance

$$\Delta t_2 = t_2 - t_1 = \frac{1}{\omega_r}\arccos\left(-\frac{1}{n-1}\right). \tag{6}$$

The interval is independent from the load current. At $t = t_2$, the corresponding transformer primary current i_{Lr} is

$$i_{Lr}(t_2) = I_0 + V_S\sqrt{\frac{(n-2)C_r}{nL_r}}. \tag{7}$$

The peak value of the transformer primary current can also be determined

$$i_{Lr-m} = I_0 + \frac{(n-1)V_S}{n}\sqrt{\frac{C_r}{L_r}}. \tag{8}$$

Mode 3 [Shown in Fig. 6(d)] $t_2 < t < t_3$: When the capacitor voltage u_{S6} reaches zero at $t = t_2$, the freewheeling diode D_{fp} begins to conduct. The current flowing through auxiliary switch S_b is the load current I_0. The sum current flowing through switch S_b and diode D_{fp} is the transformer primary

winding current i_{Lr}. The transformer primary voltage is zero and the secondary voltage is V_S. By redefining the initial time, we obtain

$$0 = L_{l1}\frac{di_{Lr}(t)}{dt} + a^2 L_{l2}\frac{d[i_{Lrs}(t)/a]}{dt} + aV_S. \tag{9}$$

Since the transformer current $i_{Lrs} = i_{Lr}/n$ as in Mode 1, we deduce (9)

$$\frac{di_{Lr}}{dt} = -\frac{V_S}{nL_r}. \tag{10}$$

The transformer primary current i_{Lr} decays linearly, the mode is ended while $i_{Lr} = I_0$. With the initial condition given by (7), the interval of this mode can be determined by

$$\Delta t_3 = t_3 - t_2 = \sqrt{n(n-2)L_r C_r}. \tag{11}$$

The interval is also independent from the load current. During this mode, switch S_6 is turned on in ZVS condition.

Mode 4 [Shown in Fig. 6(e)] $t_3 < t < t_4$*:* The transformer primary winding current i_{Lr} decays linearly from load current I_0 to zero. Partial load current flows through the main switch S_6. The sum current flowing through switch S_6 and S_b is equal to the load current I_0. The sum current flowing through switch S_b and diode D_{fp} is the transformer primary winding current i_{Lr}. By redefining the initial time, the transformer winding current obeys (10) with the initial condition $i_{Lr}(0) = I_0$. The interval of this mode is

$$\Delta t_4 = t_4 - t_3 = \frac{nL_r I_0}{V_S}. \tag{12}$$

The auxiliary switch S_b can be turned off in ZVS condition. In this case, after switch S_b is turned off, the transformer primary winding current i_{Lr} flows through the freewheeling diode D_{fp}. The auxiliary switch S_b can be also turned off in ZVS and zero-current-switching (ZCS) condition after i_{Lr} decays to zero.

Mode 5 $t_4 < t < t_5$*:* The transformer primary winding current decays to zero and the resonant circuit idles. This state is likely the same operational state as the conventional hard switching inverter. The load current flows from dc link through the two switches S_1 and S_6, and the motor.

Mode 6 [Shown in Fig. 6(f)] $t_5 < t < t_6$*:* The main inverter switch S_6 is turned directly off and the resonant circuit does not work. The snubber capacitor C_{rb} can slow down the rise rate of u_{S6}, while the main switch S_6 operates in ZVS condition. The duration of the mode is

$$\Delta t_7 = t_7 - t_6 = \frac{C_r V_S}{I_0}. \tag{13}$$

The next period starts from mode 0 again, but the load current flows through freewheeling diode D_3. During phase current commutation, the switching state is changed from one lower switch to another (e.g., turn off S_6 and turn on S_2), S_6 can be turned off directly in ZVS condition (similar to Mode 6), turning on auxiliary switch S_c to discharge the snubber capacitor C_{rc}, then switch S_2 can get ZVS condition (similar to Modes 1–4).

IV. Design Considerations

It is assumed that the inductance of BDCM is much higher than the transformer leakage inductance. From the previous analysis, the design considerations can be summarized as follows:

1) determine the value of snubber capacitor C_r, and the parameter of transformer;
2) select the main and auxiliary switches;
3) design the control circuitry for the main and auxiliary switches.

The turn ratio $(1 : n)$ of the transformer can be determined ahead. From (6) n must satisfy

$$n > 2. \tag{14}$$

On the other hand, from (12) the transformer primary winding current i_{Lr} will take a long time to decay to zero if n is too big. So n must be a moderate number. The equivalent inductance of the transformer $L_r = L_{l1} + L_{l2}/n^2$ is inversely proportional to the rise rate of the switch current when turn on the auxiliary switches. It means that the equivalent inductance L_r should be big enough to limit the rising rate of the switch current to work in ZCS condition. The selection of L_r can be referenced from the rule depicted in [14]

$$L_r \approx 4t_{\text{on}}V_S/I_{0\,\max} \tag{15}$$

where t_{on} is the turn on time of an IGBT, $I_{0\,\max}$ is the maximum load current. The snubber capacitance C_r is inversely proportional to the rise rate of the switch voltage drop when turning off the lower main inverter switches. It means that the capacitance is as high as possible to limit the rising rate of the voltage to work in ZVS condition. The selection of the snubber capacitor can be determined as

$$C_r \approx 4t_{\text{off}}I_{0\,\max}/V_S \tag{16}$$

where t_{off} is the turn off time of an IGBT. However, as the capacitance increases, more energy is stored on it. This energy should be discharged when the lower main inverter switches are turned on. With high capacitance, the peak value of the transformer current will be also high. The peak value of i_{Lr} should be restricted to twice that of the maximum load current. From (8), we obtain

$$\sqrt{\frac{C_r}{L_r}} \le \frac{nI_{0\,\max}}{(n-1)V_S}. \tag{17}$$

Three lower switches of the inverter (i.e., S_4, S_6, S_2) are turned on during Mode 3 (i.e., lag rising edge of PWM at the time range $\Delta t_1 + \Delta t_2 \sim \Delta t_1 + \Delta t_2 + \Delta t_3$). In order to turn on these switches at a fixed time (say ΔT_1) lagging rising edge of PWM under various load current for control convenient, the condition should be satisfied

$$(\Delta t_1 + \Delta t_2 + \Delta t_3)|_{I_0=0} > (\Delta t_1 + \Delta t_2)|_{I_0=I_{0\,\max}} + t_{\text{off}}. \tag{18}$$

Substitute (3), (6), and (11) into (18)

$$\sqrt{n(n-2)L_rC_r} > \frac{nL_rI_{0\max}}{(n-1)V_S} + t_{\text{off}}. \tag{19}$$

The whole switching transition time is expressed as

$$\begin{aligned} T_w &= \Delta t_1 + \Delta t_2 + \Delta t_3 + \Delta t_4 \\ &= \frac{nL_rI_0}{(n-1)V_S} + \sqrt{L_rC_r} \\ &\quad \times \left[\arccos\left(-\frac{1}{n-1}\right) + \sqrt{n(n-2)}\right]. \end{aligned} \tag{20}$$

For high switching frequencies, T_w should be as short as possible. Select the equivalent inductance L_r and snubber capacitance C_r to satisfy (14)–(19), and L_r and C_r should be as small as possible.

As the transformer operates at high frequency (20 kHz), the magnetic core material can be ferrite. The design of the transformer needs the parameters of form factor, frequency, the input/output voltage, input/output maximum current, and ambient temperature. From Fig. 2, the transformer current can be simplified as triangle waveforms, then the form factor can be determined as $2/\sqrt{3}$. Ambient temperature is dependent on the application field. Other parameters can be obtained from the previous section. The transformer only carries current during the transition of turning on a switch in one cycle, so the winding can be a smaller diameter one.

Main switches S_{1-6} work under ZVS condition, therefore the voltage stress is equal to the dc link voltage V_S. The device current rate can be load current. Auxiliary switches S_{a-c} work under the ZCS or ZVS condition, while the voltage stress is also equal to the dc link voltage V_S. The peak current flowing through them is limited to double maximum load current. As the auxiliary switches S_{a-c} carry the peak current only during switch transitions, they can be rated with a lower continuous current rating. The additional cost will not be too much.

The gate signal generator circuit is shown in Fig. 7. The rotor position signal decode module produces the typical gate signal of the main switches. The inputs of the module are rotor position signals, rotating direction of the motor, which "enable" the signal and PWM pulse-train. The rotor position signals are three square-waves with a phase shift in 120°. The "enable" signal is used to disable all outputs in case of emergency (e.g., over current, over voltage, and over heat). The PWM signal is the output of comparator, comparing the reference voltage signal with the triangular wave. The reference voltage signal is the output of the speed controller. The speed controller is a processor (single chip computer or digital signal processor) and the PWM signal can be produced by software. The outputs (G_1–G_6) of the module are the gate signals applying to the main inverter switches. The outputs $G_{1,3,5}$ are the required gate signals for three upper main inverter switches.

The gate signals of three lower main inverter switches and auxiliary switches can be deduced from the outputs $G_{4,6,2}$ as shown in Fig. 8. The trailing edge of the gate signals for three lower main inverter switches $G_{S4,6,2}$ is the same as that of $G_{4,6,2}$, the leading edge of $G_{S4,6,2}$ lags $G_{4,6,2}$ for a short time ΔT_1. The gate signals for auxiliary switches $G_{Sa,b,c}$ have a fixed pulse width (ΔT_2) with the leading edge, the same as that of $G_{4,6,2}$. In Fig. 7, the gate signals $G_{Sa,b,c}$ are the outputs of

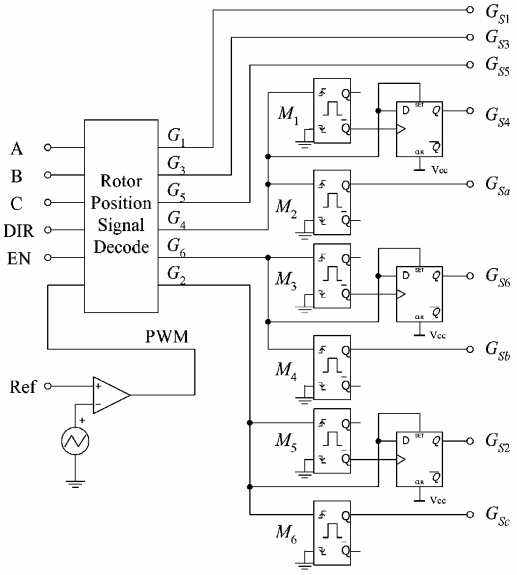

Fig. 7. Gate signal generator circuit.

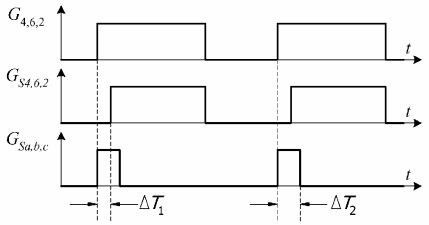

Fig. 8. Gate signals $G_{S4,6,2}$ and $G_{Sa,b,c}$ from $G_{4,6,2}$.

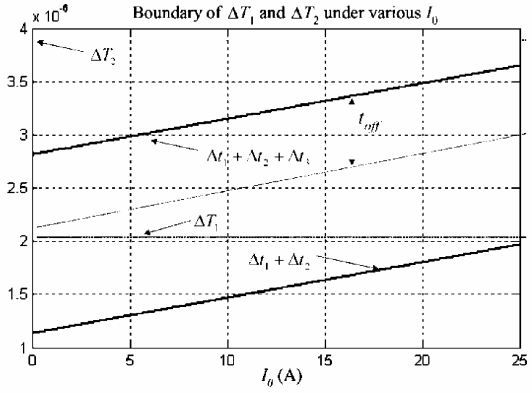

Fig. 9. Boundary of ΔT_1 and ΔT_2 under various load current I_0.

monostable flip-flops $M_{2,4,6}$ with the inputs $G_{4,6,2}$. The three monostable flip-flops $M_{2,4,6}$ have the same pulse width ΔT_2. The gate signals $G_{S4,6,2}$ are combined by the negative outputs of monostable flip-flops $M_{1,3,5}$ and $G_{4,6,2}$. The combining logical controller can be implemented by a D flip-flop with "preset"

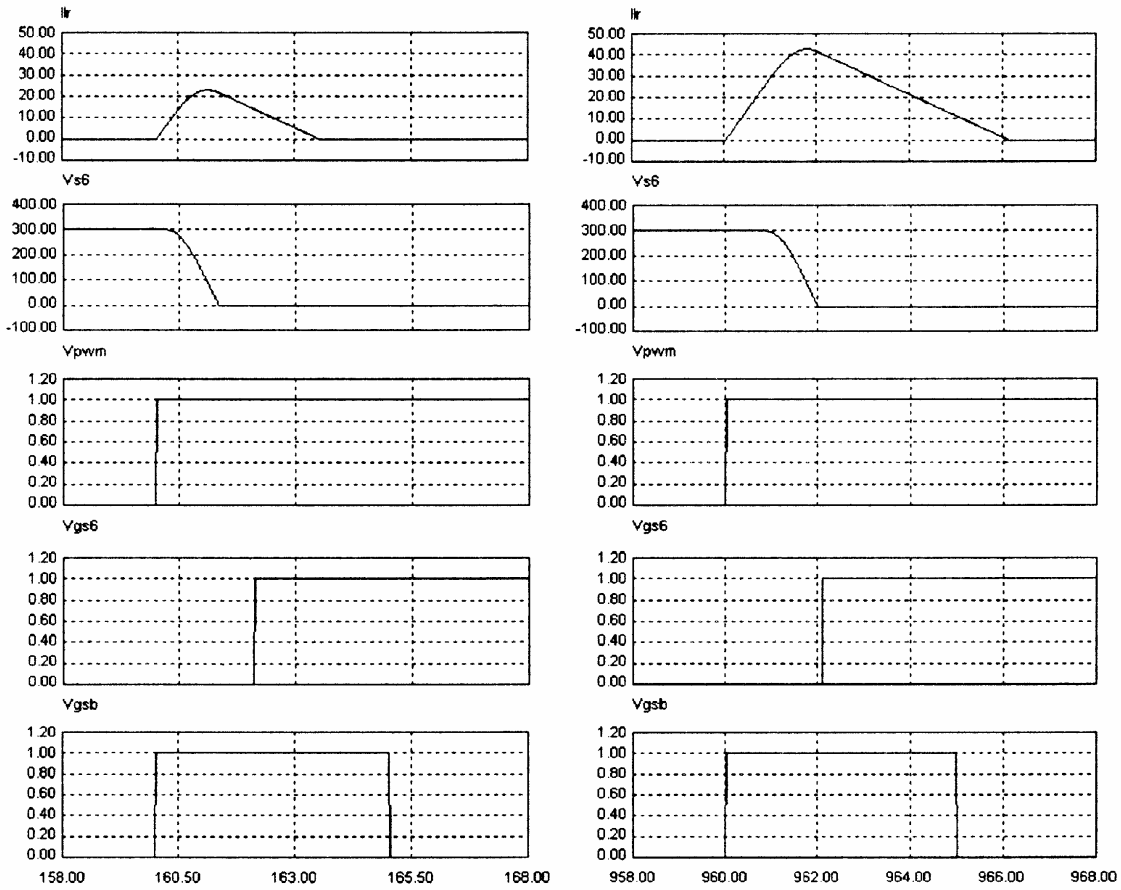

Fig. 10. Simulation waveforms of i_{Lr}, u_{S6}, PWM, S_6 and S_b gate signal under various load current (a) under low load current ($I_0 = 5$ A) and (b) under high load current ($I_0 = 25$ A).

and "clear" terminals. The three monostable flip-flops $M_{2,4,6}$ have the same pulse width ΔT_1.

Determination of the pulse widths of ΔT_1 and ΔT_2 is referenced from theoretical analysis in Section III. In order to get the ZVS condition of the main inverter switches under various load currents, the lag time ΔT_1 should satisfy

$$(\Delta t_1 + \Delta t_2)|_{I_0=I_{0\max}} < \Delta T_1 < (\Delta t_1 + \Delta t_2 + \Delta t_3)|_{I_0=0} - t_{\text{off}}. \tag{21}$$

In order to get a soft switching condition of the auxiliary switches, pulse width ΔT_2 need only satisfy

$$\Delta T_2 > (\Delta t_1 + \Delta t_2 + \Delta t_3)|_{I_0=I_{0\max}}. \tag{22}$$

V. Simulation and Experimental Results

The proposed topology is verified by software simulation PSim. The dc link voltage V_S is 300 V, and the maximum load current is 25 A. The parameters of the resonant circuit were determined from (14)–(20). The transformer turn ratio is 1:4, and the leakage inductances of the primary secondary windings are 6 μH and 24 μH, respectively. Therefore, the equivalent transformer inductance L_r is 7.5 μH. The resonant capacitance C_r is 0.047 μF. Then, $\Delta t_1 + \Delta t_2$ and $\Delta t_1 + \Delta t_2 + \Delta t_3$ can be determined under various load current I_0 as shown in Fig. 9, considering the turn off time of a switch lagging time ΔT_1 and pulse width ΔT_2 are set to 2.1 μs and 5 μs, respectively. The frequency of the PWM is 20 kHz. Waveforms of transformer primary winding current i_{Lr}, switch S_6 voltage drop u_{S6}, PWM, main switch S_6, and auxiliary switch S_b, the gate signal under low and high load current is shown in Fig. 10. The figure shows that the inverter worked well under various load currents.

In order to verify the theoretical analysis and simulation results, the inverter was tested by experiment. The test conditions are

1) dc link voltage: 300 V;
2) power of the BDCM: 3.3 hp;
3) rated phase current: 10.8 A;
4) switching frequency: 20 kHz.

Select 50 A/1200 V BSM 35 GB 120 DN2 dual IGBT module as main inverter switches, and 30 A/600 V IMBH30D-060 IGBT as auxiliary switches. With datasheets of these switches

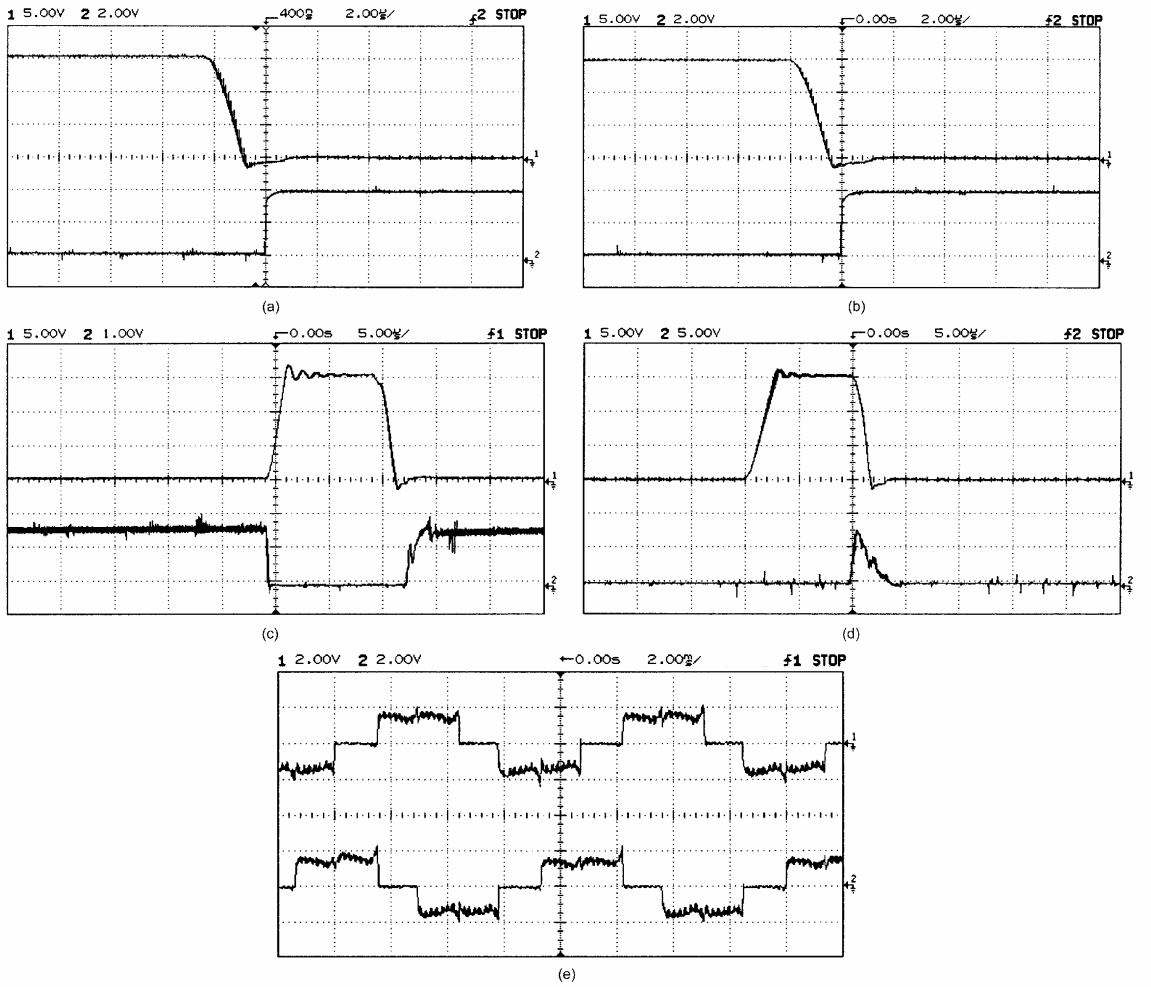

Fig. 11. Experiment waveforms. (a) Switch S_6 voltage u_{S6} (top) and its gate signal (bottom) under low load current (100 V/div). (b) Switch S_6 voltage u_{S6} (top) and its gate signal (bottom) under high load current (100 V/div). (c) Switch S_6 voltage u_{S6} (top) and its current i_{S6} (bottom) (100 V/div, 5 A/div). (d) Switch S_6 voltage u_{S6} (top) and transformer current i_{Lr} (bottom) (100 V/div, 25 A/div). (e) Waveforms of phase current (10 A/div).

and (14)–(20), the value of inductance and capacitance can be determined. Three polyester capacitors of 47 nF/630 V were adopted as snubber capacitor C_r for three lower switches of the inverter. A high magnetizing inductance transformer with the turn ratio 1:4 was employed in the experiment. 52 turns wires with size AWG 15 are selected as primary winding, and 208 turns wires with size AWG 20 are selected as secondary winding. The equivalent inductance is about 7 μH. The switching frequency is 20 kHz. The rotor position signal decode module is implemented by a 20 leads gate array logic (GAL) IC GAL16V8. The monostable flip-flop is set up by IC 74LS123, variable resistor, and capacitor. With (21) and (22), lag time ΔT_1 and pulse width ΔT_2 are determined to be 2.5 μs and 5 μs, respectively.

The system is tested in light load and full load currents. The voltage waveforms across the main inverter switch u_{S6} and its gate signal in low and high load currents are shown in Fig. 11(a) and (b), respectively. All the voltage signals measured by a differential probe with a gain of 20. For voltage waveform, 5.00 V/div=100 V/div. The waveforms of u_{S6} and it's current i_{S6} are shown in Fig. 11(c), and dv/dt and di/dt are reduced significantly. The waveforms of u_{S6} and transformer primary winding current i_{Lr} are shown in Fig. 11(d). The phase current is shown in Fig. 11(e). It can be seen that the resonant pole inverter works well under various load currents, and there is little overlap between the voltage and current waveforms during the switching under soft switching condition, therefore, the switching power losses is low. The efficiency of hard switching and soft switching under rated speed and various load torque (p.u.) is shown in Fig. 12. The efficiency improves with the soft switching inverter. Therefore, the design of the system is successful.

VI. Conclusion

A specially designed resonant pole inverter dedicated for BDCM drive system is presented. Its principle of operation

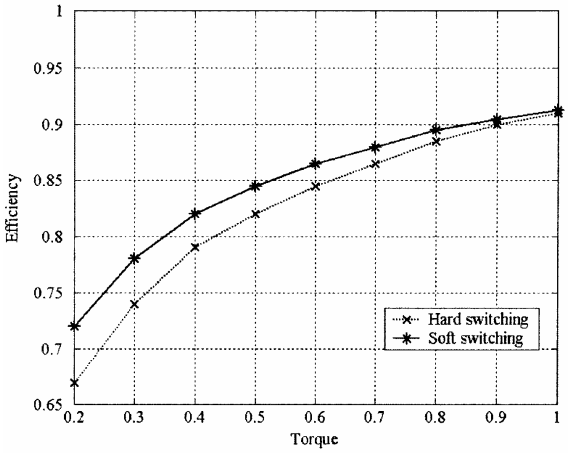

Fig. 12. Efficiency of hard switching and soft switching under various load torque (p.u.).

is explained. Selection of the required transformer parameter and snubber capacitors is given. The main inverter switches and auxiliary switches gate signal generation method is also illustrated. Determination of the corresponding pulse width is given. The inverter operation is also verified by the results of the simulation and experiment. The following observations were made.

1) All the high switching frequency switches (three lower main switches and auxiliary switches) work under soft-switching condition.
2) Voltage stress on all the switches is so low that it is not greater than the dc supply voltage.
3) Very simple auxiliary switches control scheme.
4) Freewheeling diodes turned off under zero current condition greatly reduced the reverse recovery problem of the diodes.
5) The normal operation of the inverter is entirely the same as that of the hard switching inverter.
6) dv/dt and di/dt are reduced significantly, so that EMI is reduced.
7) As the switching frequency is as high as 20 kHz, the switching acoustic noise can be eliminated.

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Transformer Based Resonant DC Link Inverter for Brushless DC Motor Drive System

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***Abstract*—Brushless dc motor has been widely used in industrial applications because of its low inertia, fast response, high power density, high reliability and maintenance-free. It is usually supplied by a hard-switching pulse-width modulation inverter, which is normally relative low efficiency since the switching power losses across the switching devices are high. In order to reduce the losses, a lot of soft switching inverters have been designed. Unfortunately, there are many drawbacks, such as high device voltage stress, large dc link voltage ripple, complex control scheme and so on. This paper introduces a soft-switching inverter based on transformer which can generate dc link voltage notches during chopping switches commutation to guarantee all switches working in zero voltage switching condition. The operation principle and control scheme of the inverter are analyzed. Simulation and experimental results are proposed to verify the theoretical analysis.**

***Index Terms*—Brushless dc motor (BDCM), resonant dc link inverter, soft switching, zero-current-switching (ZCS), zero-voltage switching (ZVS).**

I. Introduction

BRUSHLESS dc motor (BDCM) has been widely used in industrial applications because of its low inertia, fast response, high power density, high reliability and maintenance-free. It exhibits the operating characteristics of a conventional commutated dc permanent magnet motor but eliminates the mechanical commutators and brushes. Hence, many problems associated with brushes are eliminated. These problems are radio-frequency interfenrence and sparking which is the potential source of ignition in inflammable atmosphere. It is usually supplied by a hard-switching PWM inverter, which is normally relative low efficiency since the switching power losses across the switching devices are high. In order to reduce the losses, many soft switching inverters have been designed.

Soft switching operation of power inverter has attracted much attention in recent decades. In electric motor drive applications, soft-switching inverters are usually classified into three categories, namely resonant pole inverters, resonant dc link inverters, and resonant ac link inverters [1]–[3]. Resonant pole inverter has the disadvantage containing a considerably large number of additional components, in comparison to other hard- and soft-switching inverter topologies. Resonant ac link inverter is not suitable to BDCM drivers.

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In medium power applications, the resonant dc link concept [4] offered a first practical and reliable way to reduce commutation losses and to eliminate individual snubbers. Thus, it allows high operating frequency and improves efficiency. The six main switches of the inverter is quite simple to get the zero voltage switching (ZVS) condition only by adding one auxiliary switch. However, the inverter has the drawbacks of high voltage stress of the switches, high dc link voltage ripple. It is with discrete pulse modulation (DPM) control that is hard to achieve real PWM control and will result in sub-harmonics. Furthermore, the inductor power losses of the inverter are also considerable as the inductor always conducts. To overcome the drawback of high voltage stress across the switches, actively clamped resonant dc link inverter was introduced [5]–[8]. The control scheme of the inverter is too complex and the output also contains subharmonic. In addition, these inverters still did not overcome the drawback of high inductor power losses.

In order to generate voltage notches of the dc link at controllable instants and reduce the power losses of the inductor, several quasi-parallel resonant schemes were proposed [9]–[11]. As a dwell time is generally required after every notch, severe interferences occur, mainly in multiphase inverters, appreciably worsening the modulation quality. A novel dc-rail parallel resonant zero voltage transition (ZVT) voltage source inverter [12] is introduced, it overcome many drawbacks mentioned above. However, it requires a stiff dc link capacitor bank that is center taped to accomplish commutation. The center voltage of dc link is susceptible to drift that may affect the operation of the resonant circuit. In addition it requires two ZVT per PWM cycle, it would worsen the output voltage and limit the switch frequency of the inverter.

On the other hand, the majority of soft-switching inverters proposed in the recent years have been aimed at the induction motor drive applications. So it is necessary to research on the novel topology of soft-switching inverter and special control circuit for BDCM drive systems. This paper proposed a resonant dc link inverter based on transformer for BDCM drive system to solve the problems mentioned former. The inverter possesses the advantages of low switching power loss, low inductor power loss, low dc link voltage ripple, small device voltage stress and simple control scheme. The structure of the soft-switching inverter is shown in Fig. 1. The system contains a diode bridge rectifier, a resonant circuit, a conventional three-phase inverter and control circuit. The resonant circuit consists of three auxiliary switches (S_L, S_a, S_b) and corresponding built in freewheeling diode (D_L, D_a, D_b), one transformer with turn ratio 1: n and one resonant capacitor. All auxiliary switches work under ZVS or zero current switching (ZCS) condition. It generates voltage notches of the dc link to guarantee the main switches ($S_1 - S_6$) of the inverter operating in ZVS condition.

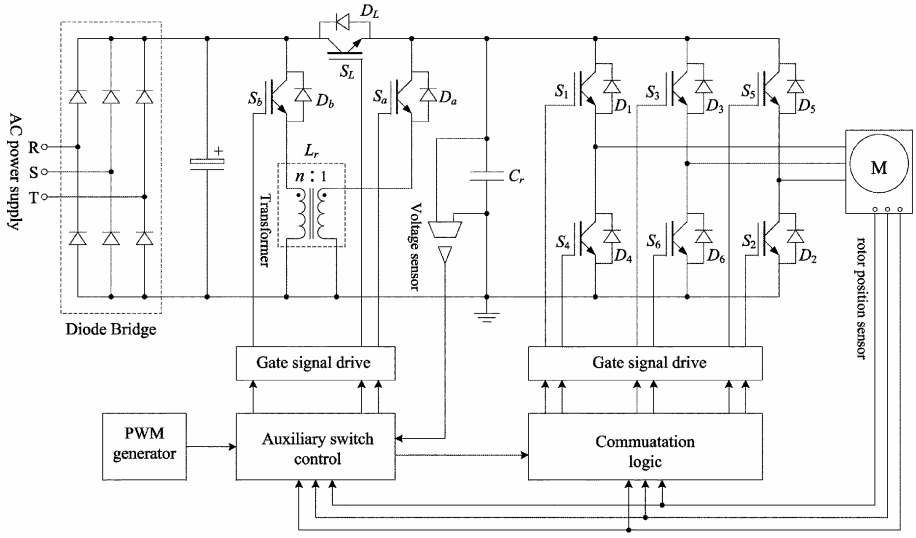

Fig. 1. Structure of the resonant dc link inverter for BDCM drive system.

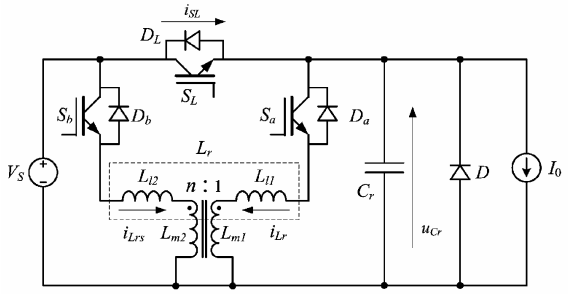

Fig. 2. Equivalent circuit of the inverter.

II. Resonant Circuit

The resonant circuit consists of three auxiliary switches, one transformer and one resonant capacitor. The auxiliary switches are controlled at certain instant to obtain the resonance between transformer and capacitor. Thus, the dc link voltage reaches zero temporarily (voltage notch) and the main switches of the inverter get ZVS condition for commutation. Since the resonant process is very short, the load current can be assumed constant. The equivalent circuit of the inverter is shown in Fig. 2. Where V_S is the dc power supply voltage, I_0 is the load current. The corresponding waveforms of the auxiliary switches gate signal, PWM signal, resonant capacitor voltage (u_{Cr}) (i.e., dc link voltage), the transformer primary winding current (i_{Lr}) and current of switch $S_L(i_{SL})$ are illustrated in Fig. 3. The dc link voltage is reduced to zero and then rises to supply voltage again is called one zero voltage transition (ZVT) process or one dc link voltage notch. The operation of the ZVT process in one PWM cycle can be divided into eight modes.

Mode 0 [Shown in Fig. 4(a)] $0 < t < t_0$*:* Its operation is the same as conventional inverter. Current flows from dc power supply through S_L to the load. The voltage across resonant capacitor $C_r(u_{Cr})$ is equal to the supply voltage (V_S). The auxiliary switches S_a and S_b are turned off.

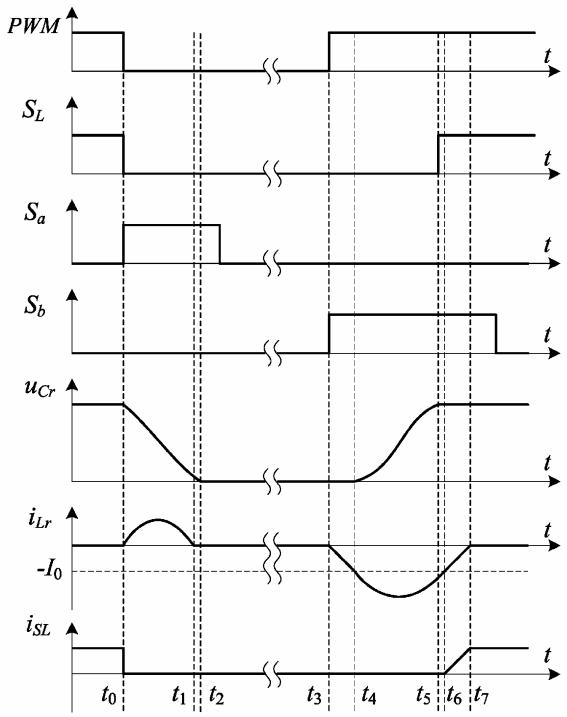

Fig. 3. Key waveforms of the equivalent circuit.

Mode 1 [Shown in Fig. 4(b)] $t_0 < t < t_1$*:* When it is the instant for phase current commutation or PWM signal is flopped from high to low, auxiliary switch S_a is turned on with ZCS (as the i_{Lr} can not change suddenly due to the transformer inductance) and switch S_L is turned off with ZVS (as the u_{Cr} can not change suddenly due to resonant capacitor C_r) at the same time. The transformer primary winding current i_{Lr} begins to increase and the secondary winding current i_{Lrs} also begins to build up

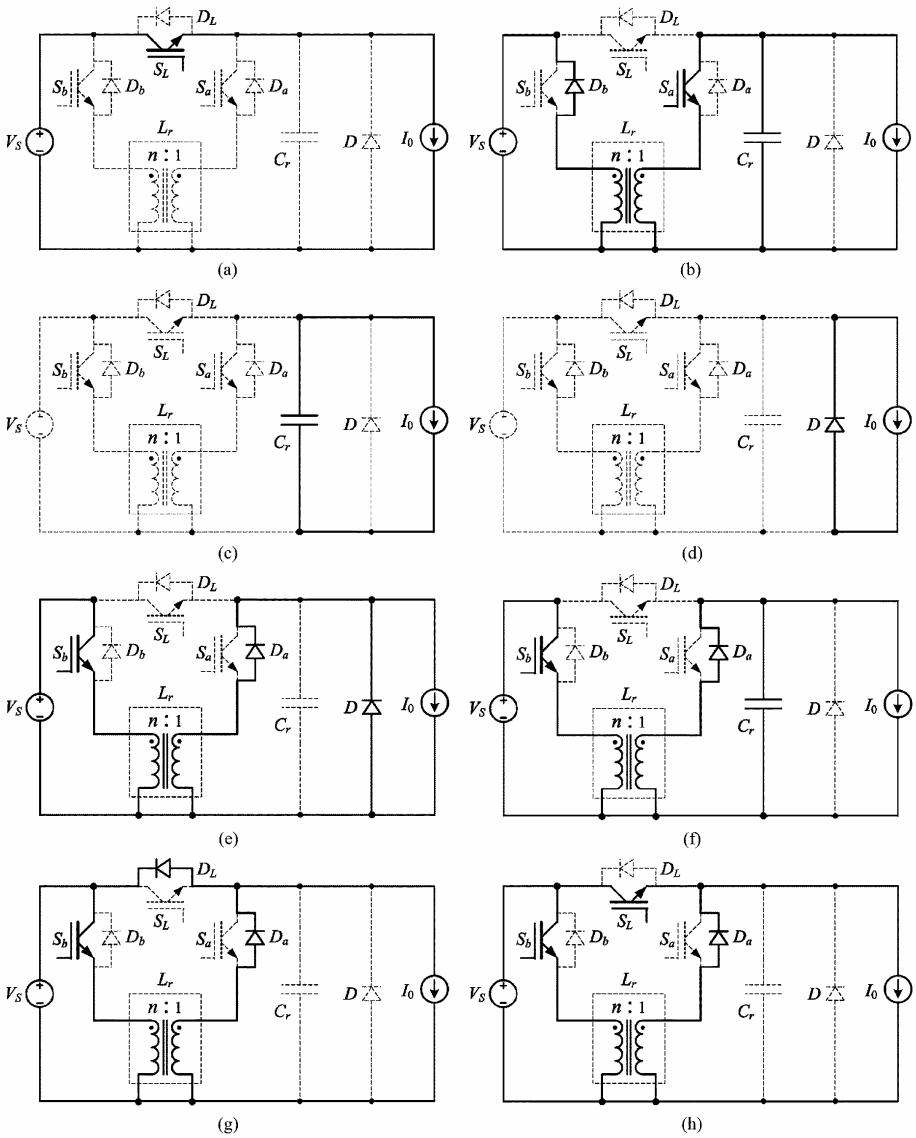

Fig. 4. Operation mode of the resonant dc link inverter: (a) Mode 0, (b) Mode 1, (c) Mode 2, (d) Mode 3, (e) Mode 4, (f) Mode 5, (g) Mode 6, and (h) Mode 7.

through diode D_b to dc link. The terminal voltages of primary and secondary windings of the transformer are dc link voltage u_{Cr} and supply voltage V_S respectively. Capacitor C_r resonates with transformer, the dc link voltage u_{Cr} is decreased. Neglecting the resistances of windings, using the transformer equivalent circuit (referred to the primary side) [13], the transformer current i_{Lr}, i_{Lrs} and dc link voltage u_{Cr} obey the equation

$$\begin{cases} u_{Cr}(t) = L_{l1}\frac{di_{Lr}(t)}{dt} + a^2 L_{l2}\frac{d\left[\frac{i_{Lrs}(t)}{a}\right]}{dt} + aV_S \\ i_{Lr}(t) + I_0 + C_r\frac{du_{Cr}(t)}{dt} = 0 \end{cases} \quad (1)$$

where L_{l1} and L_{l2} are the primary and secondary winding leakage inductance, respectively, a is the transformer turn ratio $1:n$. The transformer has a high magnetizing inductance. We can assume that $i_{Lrs} = i_{Lr}/n$, with initial condition $u_{cr}(0) = V_S$, $i_{Lr}(0) = 0$, solve the (1), get

$$\begin{cases} u_{Cr}(t) = \frac{(n-1)V_S}{n}\cos(\omega_r t) - I_0\sqrt{\frac{L_r}{C_r}}\sin(\omega_r t) + \frac{V_S}{n} \\ i_{Lr}(t) = I_0\cos(\omega_r t) - I_0 + \frac{(n-1)V_S}{n}\sqrt{\frac{C_r}{L_r}}\sin(\omega_r t) \end{cases} \quad (2)$$

where $L_r = L_{l1} + L_{l2}/n^2$ is the equivalent inductance of the transformer, $\omega_r = \sqrt{1/L_r C_r}$ is the natural angular resonance frequency. Rewrite the (2) get

$$\begin{cases} u_{Cr}(t) = K\cos(\omega_r t + \alpha) + \frac{V_S}{n} \\ i_{Lr}(t) = K\sqrt{\frac{C_r}{L_r}}\sin(\omega_r t + \alpha) - I_0 \end{cases} \quad (3)$$

where $K = \sqrt{((n-1)^2V_S^2/n^2) + (I_0^2L_r/C_r)}$, $\alpha = \arctan((nI_0/(n-1)V_S)\sqrt{L_r/C_r})$. n is a number which is slightly less than 2 (the selection of such a number will be explained late), i_{Lr} will decay to zero faster than u_{Cr}. Let $i_{Lr}(t) = 0$, the duration of the resonance can be determined

$$\Delta t_1 = t_1 - t_0 = \frac{\pi - \alpha}{\omega_r}. \tag{4}$$

When i_{Lr} is reduced to zero, auxiliary switch S_a can be turned off with ZCS condition. At $t = t_1$, the corresponding dc link voltage u_{Cr} is

$$u_{Cr}(t_1) = \frac{2-n}{n}V_S. \tag{5}$$

Mode 2 [Shown in Fig. 4(c)] $t_1 < t < t_2$*:* When the transformer current is reduced to zero, the resonant capacitor is discharged through load from initial condition as (5). The interval of this mode can be determined by

$$\Delta t_2 = t_2 - t_1 = \frac{C_rV_S(2-n)}{nI_0}. \tag{6}$$

As it has mentioned that n is a number which is slightly less than 2, the interval is normally very short.

Mode 3 [Shown in Fig. 4(d)] $t_2 < t < t_3$*:* The dc link voltage (u_{Cr}) is zero. The main switches of the inverter can now be either turned on or turned off under ZVS condition during this mode. Load current flows through the freewheeling diode D.

Mode 4 [Shown in Fig. 4(e)] $t_3 < t < t_4$*:* As the main switches have turned on or turned off, auxiliary switch S_b is turned on with ZCS (as the i_{Lrs} can not change suddenly due to the transformer inductance) and the transformer secondary current i_{Lrs} starts to build up linearly. The transformer primary current i_{Lr} also begins to conduct through diode D_a to the load. The current in the freewheeling diode D begins to fall linearly. The load current is slowly diverted from the freewheeling diodes to the resonant circuit. dc link voltage u_{Cr} is still equal to zero before the transformer primary current is greater than load current. The terminal voltages of transformer primary and secondary windings are zero and dc power supply voltage V_S respectively. Redefine the initial time, we obtain

$$0 = L_{l1}\frac{di_{Lr}(t)}{dt} + a^2L_{l2}\frac{d\left[\frac{i_{Lrs}(t)}{a}\right]}{dt} + aV_S. \tag{7}$$

Since the transformer current $i_{Lrs} = i_{Lr}/n$ as in mode 1, rewrite the (7) as

$$\frac{di_{Lr}}{dt} = -\frac{V_S}{nL_r}. \tag{8}$$

The transformer primary current i_{Lr} is increased reverse linearly from zero, the mode is end when $i_{Lr} = -I_0$, the interval of this mode can be determined

$$\Delta t_4 = t_4 - t_3 = \frac{nL_rI_0}{V_S}. \tag{9}$$

At t_4, i_{Lr} equals the negative load current $-I_0$ and the current through the diode D becomes zero. Thus the freewheeling diode turns off under ZCS condition, the diode reverse recovery problems are reduced.

Mode 5 [Shown in Fig. 4(f)] $t_4 < t < t_5$*:* Absolute value of i_{Lr} is increased continuously from I_0 and u_{Cr} is increased from zero when the freewheeling diode D is turned off. Redefine the initial time, we can get the same equation as (1). The initial condition is $u_{Cr}(0) = 0$, $i_{Lr}(0) = -I_0$, neglect the inductor resistance, solve the equation, we get

$$\begin{cases} u_{Cr}(t) = -\frac{V_S}{n}\cos(\omega_r t) + \frac{V_S}{n} \\ i_{Lr}(t) = -I_0 - \frac{V_S}{n}\sqrt{\frac{C_r}{L_r}}\sin(\omega_r t) \end{cases}. \tag{10}$$

When

$$\Delta t_5 = t_5 - t_4 = \frac{1}{\omega_r}\arccos(1-n). \tag{11}$$

$u_{Cr} = V_S$, auxiliary switch S_L is turned on with ZVS (due to C_r). The interval is independent from load current. At $t = t_5$, the corresponding transformer primary current i_{Lr} is

$$i_{Lr}(t_5) = -I_0 - V_S\sqrt{\frac{(2-n)C_r}{nL_r}}. \tag{12}$$

The peak value of the transformer primary current can be also determined

$$i_{Lr-m} = \left|-I_0 - \frac{V_S}{n}\sqrt{\frac{C_r}{L_r}}\right| = I_0 + \frac{V_S}{n}\sqrt{\frac{C_r}{L_r}}. \tag{13}$$

Mode 6 [Shown in Fig. 4(g)] $t_5 < t < t_6$*:* Both the terminal voltages of primary and secondary windings are equal to supply voltage V_S after auxiliary switch S_L is turned on. Redefine the initial time, we obtain

$$V_S = L_{l1}\frac{di_{Lr}(t)}{dt} + a^2L_{l2}\frac{d\left[\frac{i_{Lrs}(t)}{a}\right]}{dt} + aV_S. \tag{14}$$

Since the transformer current $i_{Lrs} = i_{Lr}/n$ as in mode 1, rewrite the (14) as

$$\frac{di_{Lr}}{dt} = \frac{(n-1)V_S}{nL_r}. \tag{15}$$

The transformer primary current i_{Lr} decays linearly, the mode is end when $i_{Lr} = -I_0$ again. With initial condition (12), the interval of this mode can be determined

$$\Delta t_6 = t_6 - t_5 = \frac{\sqrt{n(2-n)L_rC_r}}{n-1}. \tag{16}$$

The interval is also independent from load current. As it has mentioned that n is a number which is slightly less than 2, the interval is also very short.

Mode 7 [Shown in Fig. 4(h)] $t_6 < t < t_7$*:* The transformer primary winding current i_{Lr} decays linearly from negative load current $-I_0$ to zero. Partial load current flows through the switch S_L. The sum current flowing through switch S_L and transformer

is equal to the load current I_0. Redefine the initial time, the transformer winding current obeys the (15) with the initial condition $i_{Lr}(0) = -I_0$. The interval of this mode is

$$\Delta t_7 = t_7 - t_6 = \frac{nL_rI_0}{(n-1)V_S}. \tag{17}$$

Then auxiliary switch S_b can be also turned off with ZCS condition after i_{Lr} decays to zero (at any time after t_7).

III. Design Consideration

It is assumed that the inductance of BDCM is much higher than transformer leakage inductance. From the analysis presented previously, the design considerations can be summarized as follows.

1) Determine the value of resonant capacitor C_r, and the parameter of transformer.
2) Select of the main switches and auxiliary switches.
3) Design the gate signal for the auxiliary switches.

The turn ratio $(1 : n)$ of the transformer can be determined ahead. From (11) n must satisfy

$$n < 2. \tag{18}$$

On the other hand, from (5) and (6) it is expected that n is as close 2 as possible so that the duration of mode 2 would be not very long and u_{Cr} would be small enough at the end of mode1. Normally, n can be selected at the range 1.7–1.9. The equivalent inductance of the transformer $L_r = L_{l1} + L_{l2}/n^2$ is inversely proportional to the rising rate of switch current when turn on the auxiliary switches. It means that the equivalent inductance L_r should be big enough to limit the rising rate of the switch current to work in ZCS condition. The selection of L_r can be referenced from the rule depicted in [14].

$$L_r \geq \frac{4t_{\text{on}}V_S}{I_{0\,\max}} \tag{19}$$

where t_{on} is the turn on time of switch S_a, I_{0max} is the maximum load current. The resonant capacitance C_r is inversely proportional to the rising rate of switch voltage drop when turn off the switch S_L. It means that the capacitance is as high as possible to limit the rising rate of the voltage to work in ZVS condition. The selection of the resonant capacitor can be determined as

$$C_r \geq \frac{4t_{\text{off}}I_{0\,\max}}{V_S} \tag{20}$$

where t_{off} is the turn off time of switch S_L. However, as the capacitance increases, more energy is stored on it, the peak value of transformer current will be also high. The peak value of i_{Lr} should be limited to twice peak load current. From (13) we obtain

$$\sqrt{\frac{C_r}{L_r}} \leq \frac{nI_{0\,\max}}{V_S}. \tag{21}$$

The dc link voltage rising transition time is expressed as

$$T_w = \Delta t_4 + \Delta t_5 = \frac{nL_rI_0}{V_S} + \sqrt{L_rC_r}\arccos(1-n). \tag{22}$$

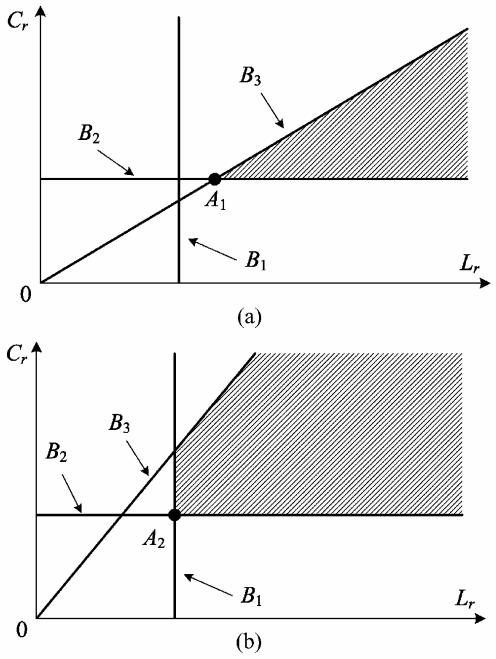

Fig. 5. L_r and C_r selection area: (a) Case 1: B_3 intersects B_1 first and (b) Case 2: B_3 intersects B_2 first.

For high switching frequency, T_w should be as short as possible. Select the equivalent inductance L_r and resonant capacitance C_r to satisfy the Inequalities (18)–(21), L_r and C_r should be as small as possible. L_r and C_r selection area is illustrated in Fig. 5 to determine their values, the valid area is shadowed, where $B_1 - B_3$ is boundary which is defined according Inequalities (18)–(21)

$$B_1 : L_r = \frac{4t_{\text{on}}V_S}{I_{0\,\max}} \tag{23}$$

$$B_2 : C_r = \frac{4t_{\text{off}}I_{0\,\max}}{V_S} \tag{24}$$

$$B_3 : \sqrt{\frac{C_r}{L_r}} = \frac{nI_{0\,\max}}{V_S}. \tag{25}$$

If boundary B_3 intersects B_1 first as shown in Fig. 5(a), the value of L_r and C_r in the intersection of B_3 and B_2 (i.e., A_1) can be selected. Otherwise, the value of L_r and C_r in the intersection A_2 is selected as shown in Fig. 5(b).

Main switches S_{1-6} work under ZVS condition, the voltage stress is equal to the dc power supply voltage V_S. The device current rate can be load current. Auxiliary switch S_L works under ZVS condition, its voltage and current stress is the same as main switches. Auxiliary switches $S_{a,b}$ work under ZCS or ZVS condition, the voltage stress is also equal to the dc power supply voltage V_S. The peak current flowing through them is limited to double maximum load current. As the auxiliary switches $S_{a,b}$ carry the peak current only during switch transitions, they can be rated lower continuous current rating.

The design of gate signal for auxiliary switches can be referenced from Fig. 3. The trailing edge of the gate signal for auxiliary switch S_L is the same as that of PWM, the leading edge is determined by the output of dc link voltage sensor. The gate signal for auxiliary switch S_a is a positive pulse with leading edge the same as PWM trailing edge, its width ΔT_a should be greater than Δt_1. From (4), Δt_1 is maximum when the load current is zero. So ΔT_a can be a fixed value determined by

$$\Delta T_a > \Delta t_1|_{\max} = \frac{\pi}{\omega_r} = \pi\sqrt{L_r C_r}. \tag{26}$$

The gate signal for auxiliary switch S_b is also a pulse with leading edge the same as that of PWM, its width ΔT_b should be longer than $t_7 - t_3$ (i.e., $\Delta t_4 + \Delta t_5 + \Delta t_6 + \Delta t_7$). ΔT_b can be determined from (9), (11), (16), and (17) that:

$$\begin{aligned}\Delta T_b &> \sum_{i=4}^{7} \Delta t_i|_{\max} \\ &= \frac{n^2 L_r I_{0\max}}{(n-1)V_S} + \sqrt{L_r C_r} \\ &\quad \times \left[\arccos(1-n) + \frac{\sqrt{n(2-n)}}{n-1}\right].\end{aligned} \tag{27}$$

IV. Control Scheme

When the duty of PWM is 100%, i.e., full duty cycle, the main switches of the inverter work under the commutation frequency. When it is the instant to commutate the phase current of the BDCM, we control the auxiliary switches S_a, S_b, S_L, and resonant occurs between transformer L_r and capacitor C_r. The dc link voltage reach zero temporarily, thus ZVS condition of the main switches is obtained. When the duty of PWM is less than 100%, the auxiliary switch S_L works as chop. The main switches of the inverter do not switch within a PWM cycle when the phase current needs not commutate. It has the benefit of reducing phase current drop during the PWM is off. The phase current is commutated during the dc link voltage becomes zero. There is only one dc link voltage notch per PWM cycle. It is very important especially for very low or very high duty of PWM. Otherwise the interval between two voltage notches is very short even overlapped which will limit the tuning range.

The commutation logical circuit of the system is shown in Fig. 6. It is similar to conventional BDCM commutation logical circuit except adding six D flip-flops to the output. Thus the gate signal of the main switches is controlled by the synchronous pulse CK that will be mentioned late and the commutation can be synchronized with auxiliary switches control circuit (shown in Fig. 7). The operation of the inverter can be divided into PWM operation and full duty cycle operation.

A. Full Duty Cycle Operation

When the duty of PWM is 100%, i.e., full duty cycle, the whole ZVT process (mode1 – mode7) occurs when the phase current commutation is on going. The monostable flip-flop M_3 will generate one narrow negative pulse. The width of the pulse

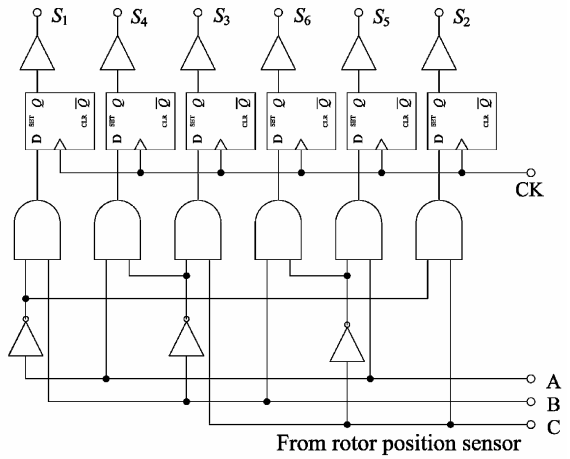

Fig. 6. Commutation logical circuit for the main switches.

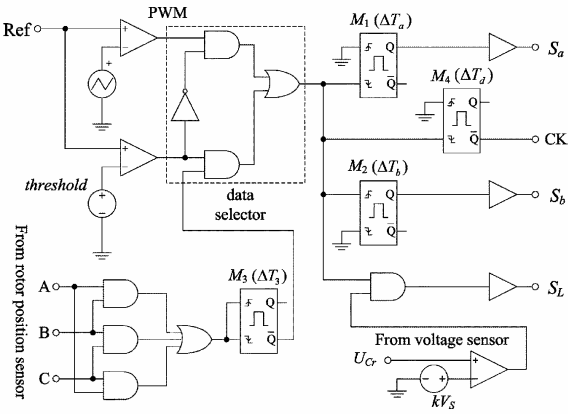

Fig. 7. Control circuit for the auxiliary switches.

ΔT_3 is determined by $\Delta t_1 + \Delta t_2 + T_c'$, where T_c' is a constant consider the turn on/off time of main switches. If n is close 2, Δt_2 would be very short or u_{Cr} would be small enough at the end of mode1, ΔT_3 can be determined by

$$\Delta T_3 = \Delta t_1|_{\max} + T_c = \pi\sqrt{L_r C_r} + T_c \tag{28}$$

where T_c is a constant which is greater than T_c'. The data selector makes the output of monostable flip-flop M_3 active. The monostable flip-flop M_1 generates a positive pulse when the trailing edge of M_3 negative pulse is coming. The pulse is the gate signal for auxiliary switch S_a and its width is ΔT_a which is determined by Inequality (26). The gate signal for switch S_L is flopped to low at the same time. Then mode 1 begins and the dc link voltage is reduced to zero. Synchronous pulse CK is also generated by a monostable flip-flop M_4, the pulsewidth ΔT_d should be greater than maximum Δt_1 (i.e., $\pi\sqrt{L_r C_r}$). If the D flip-flops are rising edge active, then CK is connected to the negative output of the M_4, otherwise connected to the positive output. Thus the active edge of pulse CK is within mode3

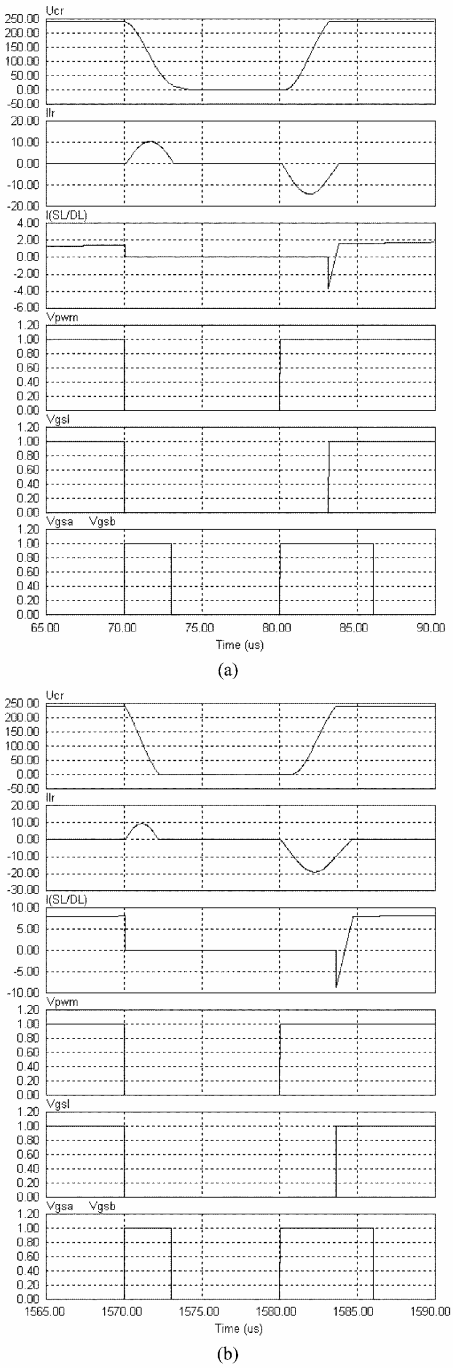

Fig. 8. Waveforms of u_{Cr}, i_{Lr}, i_{SL}/i_{DL}, PWM, auxiliary switches gate signal under various load current: (a) under low load current ($I_0 = 2A$) and (b) under high load current ($I_0 = 8A$).

when the voltage of dc link is zero and the main switches of the inverter get ZVS condition. The monostable flip-flop M_2 generates a positive pulse when the leading edge of M_3 negative pulse is coming. The pulsewidth of M_2 is ΔT_b that is determined by Inequality (27). Then mode 4–7 occurs, the dc link voltage is increased to that of supply again. The leading edge of the gate signal for switch S_L is determined by dc link voltage sensor signal. In a word in full cycle operation when the phase current commutation is on going, the resonant circuit generates a dc link voltage notch to let main switches of the inverter switch under ZVS condition.

B. PWM Operation

In this operation, the data selector makes PWM signal active. The auxiliary switch S_L works as a chop, but the main switches of the inverter do not turn on or turn off within a single PWM cycle when the phase current needs not commutate. The load current is commutated during the dc link voltage becomes zero. (As the PWM cycle is very short, it does not affect the operation of the motor).

1) When PWM signal is flopped down, mode 1 begins, pulse signal for switch S_a is generated by M_1 and gate signal for switch S_L is dropped to low. However the voltage of dc link does not increase until PWM signal is flipped up. Pulse CK is also generated by M_4 to let active edge of CK locate in mode 3.
2) When PWM signal is flipped up, mode 4 begins, pulse signal for switch S_b is generated at the moment. Then when the voltage of the dc link is increased to supply voltage V_S, the gate signal for switch S_L is flipped to high level.

Thus, only one ZVT occurs per PWM cycle: mode 1,2 for PWM turning off, mode 4,5,6,7 for PWM turning on. And the switching frequency would be not greater than PWM frequency.

V. Simulation and Experiment

The proposed system is verified by simulation software PSim. The dc power supply voltage V_S is 240 V, the maximum load current is 12 A. The transformer turn ratio is 1: 1.8, the leakage inductances of the primary secondary windings are selected as 4 μH and 12.96 μH respectively. So the equivalent transformer inductance L_r is about 8 μH. The resonant capacitance C_r is 0.1 μF. Switch $S_{a,b}$ gate signal width ΔT_a and ΔT_b are set to be 3 μs and 6 μs respectively. The narrow negative pulsewidth ΔT_3 in full duty cycle is set to be 4.5 μs, the delay time for synchronous pulse CK ΔT_d is set to be 3.5 μs. The frequency of the PWM is 20 kHz. Waveforms of dc link voltage u_{Cr}, transformer primary winding current i_{Lr}, switch S_L and diode D_L current i_{SL}/i_{DL}, PWM, auxiliary switch gate signal under low and high load current are shown in Fig. 8. The figure shows that the inverter worked well under various load currents.

In order to verify the theoretical analysis and simulation results. The proposed soft switching inverter was tested on an experimental prototype. The dc link voltage is 240 V, rated phase current is 10.8 A, the switching frequency is 20 kHz. Select 50 A/1200 V BSM 35 GB 120 DN2 dual IGBT module as main inverter switches $S_1 - S_6$ and auxiliary switch S_L, another switch in the same module of S_L can be adopted as auxiliary switch S_a, 30 A/600 V IMBH30D-060 IGBT as auxiliary switch S_b. With datasheets of these switches and (18)–(21), the

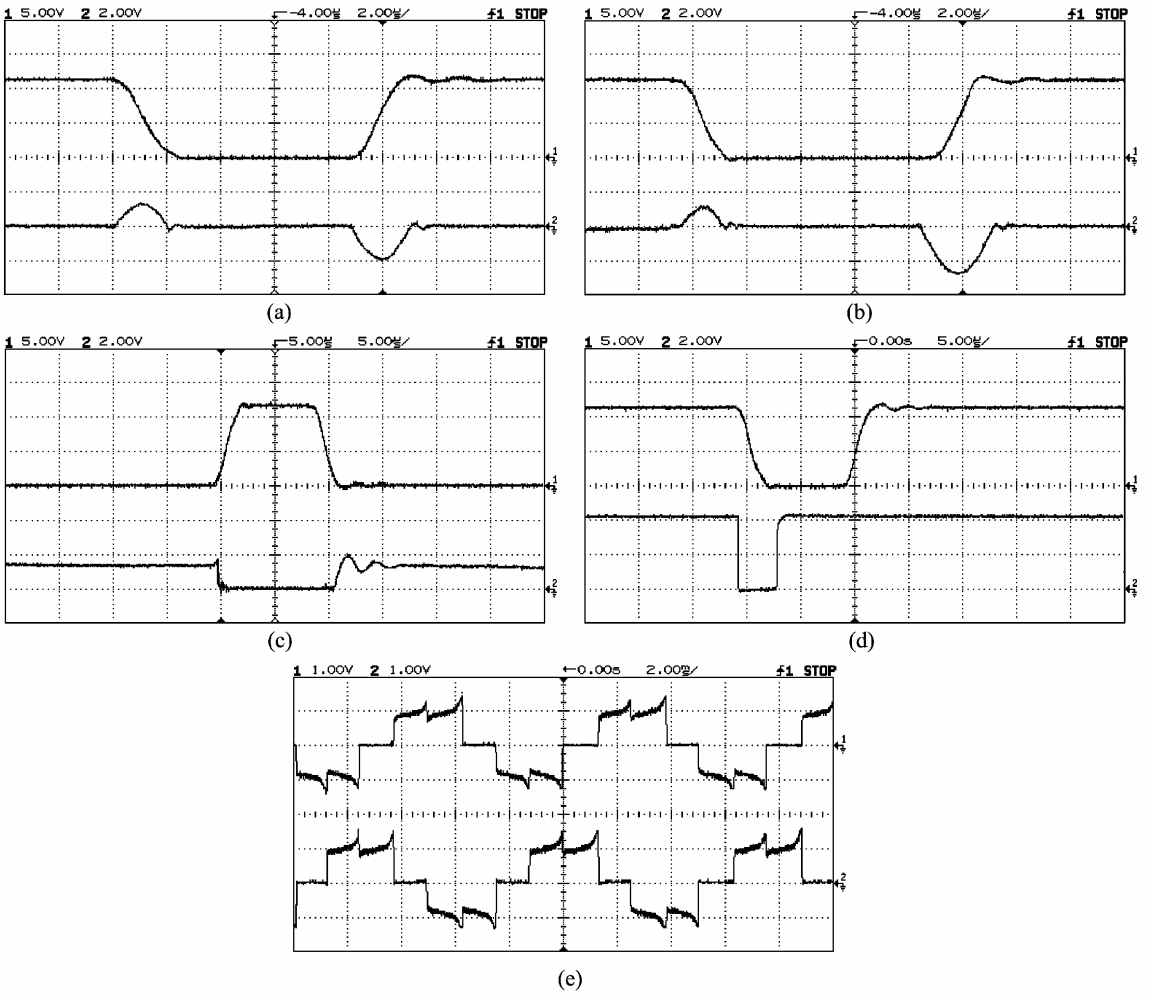

Fig. 9. Experiment waveforms: (a) the dc link voltage u_{cr} (top) and transformer current i_{Lr} (bottom) under low load current (100 V/div, 10 A/div), (b) the dc link voltage u_{cr} (top) and transformer current i_{Lr} (bottom) under high load current (100 V/div, 10 A/div), (c) switch S_L voltage (top) and current (bottom) (100 V/div, 10 A/div), (d) the dc link voltage u_{cr} (top) and synchronous signal CK (bottom) (100 V/div), and (e) phase current of BDCM (5 A/div).

value of capacitance and the parameter of transformer can be determined. A polyester capacitor of 0.1 μF, 1000 V was adopted as dc link resonant capacitor C_r. A high magnetizing inductance transformer with turn ratio 1:1.8 was employed in the experiment. The equivalent inductance is about 8 μH under short circuit test [13]. The switching frequency is 20 kHz. The monostable flip-flop is set up by IC 74LS123, variable resistor and capacitor. The logical gate can be replaced by programmable logical device to reduce the number of IC. ΔT_a, ΔT_b, ΔT_3, and ΔT_d are set to be 3 μs, 6 μs, 4.5 μs, and 3.5 μs respectively.

The system is tested in light and heavy load. The waveforms dc link voltage u_{Cr} and transformer primary winding current i_{Lr} in low and high load currents are shown in Fig. 9(a) and (b), respectively. The transformer based resonant dc link inverter works well under various load currents. The waveforms of auxiliary switch S_L voltage u_{SL} and its current i_{SL} are shown in Fig. 9(c). There is little overlap between the switch S_L voltage and its current during the switching under soft switching condition, so the switching power losses are low. The waveforms of resonant dc link voltage u_{Cr} and synchronous signal CK are shown in Fig. 9(d), which the main switches can switch under ZVS condition during commutation. The phase current of BDCM is shown in Fig. 9(e). The design of the system is successful.

VI. Conclusion

A transformer based resonant dc link inverter for BDCM drive system, capable of controlling zero voltage notch instant and width is presented. Its principle of operation was explained. The simulation results are also given. All the relevant experimental waveforms were captured to verify the theory analyze and simulation. The following observations were made.

1) All switches work under soft-switching condition, so their power losses are small.

2) Voltage stress on all the switches would be not greater than dc Supply voltage.
3) Only one dc link voltage notch is needed during one PWM cycle, and the switching frequency of the auxiliary switches would not higher than PWM frequency.
4) Simple auxiliary switches control scheme.
5) Freewheeling diodes turned off under zero current condition and this greatly reduced the reverse recovery problem of the diodes.
6) dv/dt and di/dt are reduced significantly, so EMI is reduced.
7) Soft switching results in considerably less noise as the switching frequency can be high to outside the audio spectrum.
8) The topology also applicable to induction motor drive system.

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