Fault control paralleled DC-DC converters and
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communication strategy decentralized control
paralleled inverters

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**Fault Control for Paralleled DC-DC Converters and
Novel Common Mode Current Based
Communication Strategy for Decentralized Control
of Paralleled Inverters**

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School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

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SUMMARY

The technology advancement over the years has demanded a highly reliable and good quality of electricity from the power utilities and independent power producer (IPP) companies. As much as precaution and care were taken by the utilities and IPP companies, the power quality issues are still unavoidable. These indispensable problems call for the need of power quality mitigation equipment to be aggressively developed recently. As the dependency on these equipment to ensure high quality of power has increased each day, the reliability of these equipment has also draw much attention because of its vulnerability is at stake. Hence, the research to enhance the reliability of those equipment is intense. One of the well-known ways to achieve higher reliability is by paralleling two or more units of equipment together. This is because the paralleled system has wide advantages over single unit equipment. Advantages include increase of power capability, high reliability, enhanced availability from the fault tolerance with $N+1$ modules and ease of maintenance with redundancy implementation. This thesis explores and investigates the paralleling of power supply modules, with the aim to achieve decentralized control scheme that assured reliability, flexibility, reduces power ratings of each module, and to overcome the limitation in centralized control scheme as well as conventional droop method. New approaches are developed and verified experimentally, including method to communicate information wirelessly, smooth ride-through during fault, synchronization as well as near-perfect equal current sharing. The performance of these techniques are quantified and dynamically analyzed. Three DC-DC buck converters with 5Vdc/1A output and three single-phase DC-AC inverters with 110V_{rms}/550VA 60Hz are constructed to verify the approaches developed in this thesis. The research findings are very promising with full marketable potential for the industrial.

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LIST OF SYMBOLS

i_{com} : Common-mode current

i_{diff} : Differential-mode current

i_L : Inductor current

L_{com} : Common-mode choke

L_{diff} : Filter inductor

R_{int} : Inductor's internal resistance

V_{in} : Input voltage

VR : Voltage regulators

V_{ref} : Reference voltage

$$\alpha = K_0 K_1 L \left(M \left(\frac{1}{N} - 1 \right) - 1 \right)$$

$$\beta = \frac{K_0 K_1 L M}{N}$$

$$\gamma = -\frac{K_0 K_1 L K_2 C}{N}$$

$$\hat{\lambda} = K_0 K_1 L$$

$$\Psi = \hat{\lambda} (1 + M)$$

$\delta \varepsilon_j$: An external source of disturbance for j -th module

ζ : Damping ratio

ω_n : Natural frequency

LIST OF ABBREVIATIONS

AC	: Alternating Current
ADC	: Analog-to-digital converter
AM	: Amplitude modulation
BPF	: Band-pass-filter
DAC	: Digital-to-analog converter
DC	: Direct Current
DSP	: Digital-signal-processor
DVR	: Dynamic voltage restorers
EMI	: Electromagnetic interference
ESR	: Equivalent series resistance
FM	: Frequency modulation
IEC	: International Electrotechnical Commission
IEEE	: Institute of Electrical and Electronics Engineers, Inc.
KCL	: Kirchhoff Current Law
kVA	: Apparent Power in 1,000
KVL	: Kirchhoff Voltage Law
LHP	: Left-half of s -plane
LPF	: Low-pass filter
M	: Current sharing controller
MOSFET	: Metal-Oxide-Semiconductor Field-Effect Transistor
MRAC	: Model reference adaptive control
MVA	: Apparent Power in 1,000,000
N	: Number of paralleled modules
PI	: Proportional-integral
PID	: Proportional-integral-derivative

List of Abbreviations

PLL	: Phase-locked-loop
PQ	: Power Quality
PWM	: Pulse-width-modulation
RLC	: Resistor-inductor-capacitor
SEMI	: Semiconductor Equipment and Materials International
TVSS	: Transient voltage surge suppressor
UPS	: Uninterruptible power supply
US	: United States
USD	: US Dollars

Chapter 1 INTRODUCTION

1.1 BACKGROUND

One of the major concerns in recent years for the power industries, that has significant impact on the economy, is the power quality (PQ) problem. According to IEEE Standard 1159-1995 [1], the term power quality refers to a wide variety of electromagnetic phenomena that characterize the voltage and current at a given time and at a given location on the power system. The general classification of the power quality phenomena [1] can be found in Appendix 1.

These power quality phenomena have become an increasingly important issue and problem due to the proliferation of critical and sensitive electrical and electronic equipment used in the industries, commercial buildings as well as within the home; such as computers, medical equipment, satellite systems, telecommunication equipment and others. The cost associated with the effect of power quality problem can be tremendous and can range from a couple hundred dollars to upwards of a million dollars [2-5]. This is due to repair or replacement of appliances, product losses, production losses and cleanup, which depend on the size and types of problem. According to [4], the actual net value of the damages caused by short interruptions and voltage sags in US was estimated to be about USD 1.8 million. Moreover, [2] reports that an automaker in US estimated about USD 10 million a year of total losses from momentary power glitches at all its plants.

To alleviate the effects of power quality problems and to improve the performance of these sensitive equipment, one of the ways is to install additional protective equipment closer to the critical loads. There are a wide variety of protective devices available from several manufacturers in the market. Equipment that are commonly implemented to enhance electrical system against PQ problems include uninterruptible power supply (UPS), dynamic voltage restorers (DVR), transient voltage surge suppressor (TVSS), harmonics filters, shielded isolation transformers, voltage regulators (VR), power line conditioners, motor generator sets, electromagnetic interference (EMI) filter and others. Each of these protective devices has different set of problem solving function that can be used in wide variety of applications. To avoid adverse interactions, the solutions must be compatible with both the load and the power source.

Due to the intense of PQ issue around there world, international organizations began to involve in providing guidelines, establish standards and code of practice to define and address these issues of power quality. Those organizations include the Institute of Electrical and Electronics Engineers, Inc (IEEE), International Electrotechnical Commission (IEC), Semiconductor Equipment and Materials International (SEMI) and other local authorities. These documents and standards that are prepared by these diverse organizations, including voluntary consensus standards are briefly recorded in Appendix 2 for reference.

1.2 RESEARCH MOTIVATION

As the growing concerns over power quality issues in the international communities are intensifying over the decades, especially the manufacturing industries and commercial customers, more protective equipment are invented to tackle those

problems in recent years too. A commonly applied solution to power quality problems is to install interface protective equipment between supplied power and sensitive loads, besides modifying the plant power systems. The success of reliable and continuous operation of these sensitive electronic equipment depends solely on these protective devices in those cases. Therefore, the reliability of the protective equipment must be increased as well in order not to jeopardize the sensitive equipment by its own malfunction components.

One of the ways to increase the reliability of these equipment is through paralleling technique, as illustrated in [6-7]. This paralleling architecture will also help to increase the system flexibility and reduce cost compared to a single unit high power rating system. This issue will be discussed in the following sessions.

1.2.1 RELIABILITY

The availability and aftermath failure of the components will determine the overall system reliability. In order to achieve high system reliability, the exploitation of redundancy architecture should be incorporated into the system. Due to the degree of redundancy introduced by the paralleled or distributed system, the system reliability is increased enormously. This feature is not present in the single unit system [8-9] because of the potential of single-point failure. When one of the modules fails in the paralleled system, the rest of the modules will help to supply the remaining load requirement. However, single system does not feature these benefits.

On the contrary, if one of the paralleled modules fails to function, the system reliability could be at risk. This is because the system performance at that moment of fault

is shaped by the behavior of the faulty module. In addition, the performance of the remaining healthy modules in the system also determines its effectiveness and reliability. All these performances are taken into consideration before the faulty module is being excluded from the system. During this faulty period, all kind of incident and phenomena could occur that might post more damage to the system than increasing the system reliability because of its component uncertainty. Therefore, the understanding of the system's transient during fault is crucial in order to propose any mitigation solution to ensure that the system is reliable and able to withstand all kinds of conditions. This motivates the investigation of transient behavior of paralleled modules when one of its modules malfunctioned.

1.2.2 FLEXIBILITY

The flexibility of expanding the system can be done easily when the system is constructed in parallel. This is because the paralleling architecture allow the users to adjust the number of modules to be paralleled as required in order to maintain the optimum operating condition [8-10].

Besides, any defect module can be removed easily without much disturbances, transients or stress to the overall system. This can be done provided a proper controller is designed to handle such situations in the paralleled system. The ease of replacement or maintenance is also benefited from this architecture. This too further motivates the research of hot swapping in the paralleled system. In recap, adding and removing of any modules could be easily realized in the paralleled system compare to single unit system.

1.2.3 POWER RATING, COST BENEFITS AND THERMAL MANAGEMENT

When configuring the system using more modules than the minimum load required, power rating for each module can be reduced while maintaining the required power. To understand this quantitatively, consider a general hospital that required a three phase 1MVA ‘double-conversion’ [11] UPS with backup time of at least 3 hours in order to ensure continuous operation of the life support equipment in case of prolong outage. Instead of having to specially customize the production of a UPS to meet the required high power rating, it can be paralleled with smaller units of UPS, such as paralleling 4 units of 300kVA or 5 units of 200kVA, depending on the economics of the UPS rating from various manufacturers.

Furthermore, it is easier to obtain standard products with smaller rating from any manufacturer compared to customize high power ratings. This is because the process of customization is unremarkably time consuming and also relatively expensive due to the manufacturing cost compare to smaller standard rating, which is more economical in high volume. Hence, the economics of mass production for standard product compared to customize products can reduce the costs.

The second area of cost benefit in exploiting paralleling technique is in the cost of thermal management. This is because by distributing the heat sources, the paralleled system can take the advantage of heatsink area much more effectively than a single high power module, which permits the use of lower-cost cooling technology. This can be realized by having the total power or heat distributed among the modules evenly, thus eliminating the single point source of heat generated by the single module. This, in turn,

could simplify the design of heatsink and also reduce the cost of the thermal management system [9].

In recap, all the previous discussions argue compellingly that the paralleling architecture should be pursued aggressively to further improve the system reliability and flexibility.

1.3 OBJECTIVES

This research further investigates and explores the design of paralleling technique for power modules with the aim of achieving improvements in performance, reliability and flexibility over existing techniques. This thesis has three objectives in that direction, which are outlined as follows.

- i. To present the fundamental of paralleling technique in order to comprehend its advantages.

This thesis focuses on the paralleling of power modules rather than investigating the physics and performances of paralleling components as illustrated in [12-14]. Several paralleling techniques will be presented in this thesis. Ultimately, there are only two main control topologies that can be deduced from those paralleling techniques. They are the centralized and decentralized control. The comparison between both topologies is discussed extensively in order to apprehend the superiority of each technique over the other.

- ii. To study the stability and transient analysis of paralleling technique for power modules in order to further explore other opportunities to enhance system reliability.

Since stability analysis is a crucial issue prior to any control system design, this thesis will present a generic stability analysis of the paralleled power modules. Furthermore, the transient analysis for the paralleled system with faulty module is also developed so that proper compensation techniques can be adopted to minimize the effects of it and thus, further improve the system reliability.

- iii. To explore and develop alternate decentralized controller technique to enhance the flexibility features.

As the number of module increases, the centralized control becomes unattractive compared with decentralized control. Nevertheless, the conventional decentralized control has several limitations and hence, new control strategy is developed to overcome those limitations and improve the performances. In order to realize the potential advantages of this strategy, a three UPS prototype system is developed at a reasonable power rating of 1kVA each to evaluate the design approach. The control strategy was tested for voltage command synchronization and near perfect equal current sharing among paralleled power modules.

1.4 CONTRIBUTIONS

This research comprehensively deals with paralleling of power modules, focusing on DC-DC converter initially and DC-AC inverter for the remaining of the thesis. The contributions of this thesis are summarized as follows.

1. A detailed paralleled buck converter stability analysis based on state variable technique was carried out in order to investigate any possibility of having an unstable system when paralleling technique is implemented.

2. A transient analysis and stability study of a paralleled system when one of the modules failed during the operation was conducted in order to enhance system reliability. This fault transient analysis is carried out by using the superposition principle and a compensation strategy is proposed to minimize the effect of the fault transient on the output of the paralleled power modules. The stability analysis for all the conditions (i.e. before the fault, during compensation and after fault clearance) was conducted to ensure smooth transitions during each phase. A prototype system consisting three DC-DC buck converter units was developed to attest the analysis performed and also the proposed compensations. The experimental waveforms and results obtained demonstrate the effectiveness of the proposed compensation strategy.

3. A novel communication strategy among paralleled multi-inverters was developed and experimentally verified for its feasibility and usability. This communication strategy utilizes the common-mode current, which is inherent in paralleled multi-inverters, to transmit signals throughout the paralleled modules. With this strategy, any signal or information can be transmitted and/or received throughout the paralleled modules via existing wires and thus eliminating additional communication cable. This enhances the decentralized control technique compared to the centralized controller, by avoiding single point failure in the controller itself. In order to comprehend this communication strategy, voltage command synchronization of paralleled multi-inverters is implemented. Such synchronization is important and necessary in a paralleled system in order to ensure that all output voltages are synchronized in frequency, phase and amplitude.

This avoids large circulating currents flowing among the inverters that will otherwise decrease system capability by forcing the components to operate beyond their rated current value. A prototype of paralleling three units of inverter is constructed to verify the proposed strategy. Experimental results and waveforms obtained affirm the conducted analysis and strategy.

4. Further investigation into issues in the decentralized controller for paralleled multi-inverters, such as near perfect equal current sharing and synchronization of voltage command, were carried out in order to enhance the decentralized control strategy. Mitigation solutions to these issues were proposed and experimentally verified on a prototype of three paralleled inverters.
5. Hotswapping feature in the paralleled power modules is added into this architecture in order to improve its flexibility and increase its modularity. With this feature added, it is desired that any module can be plug-in or plug-out without much difficulty and with minimum transient involved. Hence, several issues involved during hotswap are investigated and several techniques are proposed to minimize the transient during plug-in transition.

1.5 THESIS ORGANIZATION

This thesis is divided into seven chapters, including this introductory chapter. Chapter 2 presents an overview of paralleling techniques, which can be categorized into two main control methods, i.e. the centralized and decentralized control. The advantages and disadvantages for both methods will be discussed extensively in this chapter too. This chapter also illustrates the controller design of a simple buck converter, which is

eventually expanded into two extra units via paralleling. The simple controller design for paralleled power modules is verified experimentally in a prototype with the paralleling of two-buck converters.

Chapter 3 further analyzes the stability of the paralleled power modules in general. It is shown in this chapter that the stability analysis for paralleled power modules can be analyzed separately via common-mode and differential-mode stability analysis. In addition, the stability analysis for the droop method, which represents the decentralized control method, will be illustrated too in this chapter.

The transient analysis based on the superposition principle during fault is presented in Chapter 4. Likewise, the proposed compensation technique during one module failure is presented in this chapter. The controller used in this study was developed in Chapter 2. All the analysis and compensation proposed are verified experimentally on a prototype of paralleling three-buck converters with a centralized controller. The simulation and experimental results confirmed the effectiveness of the proposed compensation and also the affirmed the analysis performed.

Chapters 5 and 6 focused on paralleling of multi-inverters in the decentralized control method. A novel communication strategy for decentralized control of paralleled multi-inverters is presented in Chapter 5. This strategy utilizes the inherent common-mode current in the paralleled multi-inverters system as a signal to transmit information to each individual module. In order to apprehend this strategy, voltage command synchronization is implemented with this method. The proposed communication strategy

is tested on a prototype of three-paralleled single-phase inverters. The experimental results obtained coincide with the simulation results and analysis performed.

Chapter 6 further investigates the design issues in the decentralized control of paralleled multi-inverters. Those issues investigated include the synchronization of voltage command, near perfect equal current sharing among paralleled modules, the effect of parameter deviation in the paralleled system and hotswapping of modules. Several recommendations were provided in order to enhance the paralleled multi-inverters. All the mitigation solutions to ensure near-perfect equal current sharing were tested on the prototype developed for multi-inverters. The experimental results affirmed the effectiveness of the proposed mitigation solutions towards the current sharing issue. Furthermore, in order to enhance the flexibility and modularity of the paralleled multi-inverters, issues in hotswapping of the modules are also investigated. A transientless hotplug-in technique is proposed to ensure smooth plug-in transition.

Eventually, Chapter 7 concludes this thesis with the summary of the topic covered and some recommendations for further research.

Chapter 2 PARALLELING TECHNIQUES FOR PARALLELED POWER MODULES

2.1 INTRODUCTION

One of the important properties in the paralleling of power modules is that all the paralleled modules share their current stably and evenly. Near-perfect equal current sharing characteristic is important for the main two reasons of the reliability and output dynamics of the paralleled power modules. The reliability of the paralleled system tends to be reduced in the absence of a good current sharing controller. This is because if some of the modules continuously operate under heavy load compared with the others due to lack of equal current sharing, the failure rate of those overloaded modules can strongly impact the overall system reliability. On the other hand, the output dynamics of the paralleled power modules is very much affected and shaped by the current-sharing behaviour. Therefore, the current-sharing controller design should also address this issue as part of its system design in order to optimize the output dynamics of the paralleled system. This chapter will investigate on the paralleling techniques previously proposed and designed, which are available in the literature. The aim of this chapter is also to categorize all the existing paralleling methods into two main categories, i.e. the centralized and decentralized control method.

2.2 PARALLELING TECHNIQUES IN POWER MODULES

The current-sharing behaviour in the paralleled system is largely dependent upon the controller style of each module. There are many types of current-sharing controller

proposed and designed over the past two decades [6-10,15-40]. All these current-sharing controllers have some similarity in the way they communicate and control among the paralleled modules in order to ensure that the proposed current sharing style is implemented.

Unlike [19], which classified the paralleling methods based on the current sharing operating mechanism, the categorization done in this thesis for the current sharing methods is simplified by focusing on the manner the information is processed, controlled and shared across the paralleled modules. Sharing of information can be implemented either by having additional interconnected communication wire or using the existing connection. Any paralleled system having additional interconnected communication wire/cable or having some form of global control will be termed as a centralized control scheme in this thesis. This term *centralized* is chosen because it represents the nature of this paralleling technique where there exists a certain information center that processes and redistributes the current sharing reference among the paralleled modules via a commonly shared bus/cable.

The decentralized control scheme, on the other hand, is defined as any paralleled system that communicate via existing connection without having additional wire/cable or global control. This scheme is also known as wireless technique [40] or distributed scheme [8] in literatures. Nevertheless, the term *decentralized* is used in this thesis to avoid confusion and also because it represents the manner where the shared information is being processed separately without having a centralized unit in the paralleling architecture. In this scheme, each module has its own governed controller that can receive or transmit

information without depending upon any global or supervisory controller. The detail of each defined paralleling technique will be further illustrated in the following subsections.

2.2.1 CENTRALIZED CONTROL SCHEME

The main component in centralized control scheme category is that it has commonly-shared bus and also a supervisory control unit that monitors the whole system performance and parameters, as shown in Figure 2.1. Those parameter monitored can be the output voltage, total output current or individual current, depending on the desired current-sharing controller's style. The commonly implemented styles of current sharing are democratic or average scheme [15,16,18,25,36,37] and master-slave scheme [7,15-18,31,35].

Figure 2.1. Block diagram of N paralleled power modules with centralized control scheme.

The term democratic or average scheme itself illustrates that all the currents in the paralleled modules are shared evenly. This scheme basically either sum up all the currents produced by each module or obtains it from load current and divides it by the number of paralleled modules to provide the reference $I_{Average}$, as shown in Figure 2.2. The

centralized controller will ensure that all the paralleled modules generate near-perfect equal current sharing by feeding back the current sharing error information into each module's controller. All the modules used in this scheme have similar power ratings.

Figure 2.2. Democratic or average scheme for N paralleled power modules.

The master-slave scheme, on the other hand, has usually one 'master' module and several 'slave' modules as shown in Figure 2.3. The purpose of this scheme is to utilize the different power ratings in each module to generate output current relative to its rating. The highest relative output current, which is relative to its rating, will automatically become the 'master' and the other modules are regulated to relative output currents slightly lower than that of the master module.

Figure 2.3. Master-slave scheme for N paralleled power modules.

2.2.2 DECENTRALIZED CONTROL SCHEME

Unlike centralized control scheme, each converter in decentralized control scheme has individual current sharing controller that gather information from other converters and process it to produce near-perfect equal current sharing among converters. Furthermore, there is no interconnected communication cable among the paralleled modules. This is because the required information for current sharing is obtained from each module internally. Despite numerous publications on decentralized control scheme, most of the proposed schemes are basically developed based on the renowned conventional decentralized control scheme of droop method [20-23,32-34,39,40] except for the frequency-based [27] and switching-ripple-based current sharing technique [28]. Both schemes that are developed in [27] and [28] use a frequency that was generated internally to achieve current sharing among converter cells, and they require neither additional interconnection among cells nor rely on any droop characteristic.

On the contrary, the concept of droop method in this paralleling architecture is based on the distributed power system droop scheme. The droop method employed in this

paralleling of power modules relies upon the internal (output) and/or externally added resistance (physically or electronically) of the paralleled modules to maintain a relatively equal current distribution among the modules. This scheme can be artlessly described as an ‘open-loop’ current sharing technique that requires no wire interconnections among the control circuits of paralleled converters, as shown in Figure. 2.4.

Figure 2.4. Droop method for N paralleled power modules.

It can be briefly illustrated as shown in Figure 2.5. In the first scenario, both power modules have same droop resistances, i.e. $R_1=R_2$ and their outputs are not matched initially as shown in Figure 2.5(b), where the voltage outputs are labeled as V_1 and V_2 respectively. The corresponding output current for each module is I_1 and I_2 respectively. The current and voltage drop across the load R_L is I_o and V_o . It is clearly shown in Figure 2.5(b) that the current sharing error in this scenario is large due to mismatch output voltage at no load condition.

In the second scenario, the load resistance (R_L) as well as the droop resistance (R_1, R_2) remained unchanged but with modification on the output voltage at no load conditions. The output voltages in this scenario are closely matched at no load condition, as labeled in Figure 2.5(b) as V'_1 and V'_2 . The load voltage will ‘droop’ as the load current goes from

zero to full load (I_o). As a result of this matching, it improved the current sharing of I'_1 and I'_2 . Thus, for a perfect current sharing, both the output voltages at no load condition as well as the droop resistance must be identical, and these conditions are practically impossible.

In the third scenario, the output voltage mismatch and load (R_L) remained as shown in Figure 2.5(c), but with higher droop resistance of R'_1 and R'_2 compare to R_1 and R_2 , i.e. $R' > R$. This causes the load regulation characteristic slope to be steeper than in the first scenario. Consequently, with this change in droop resistance, current sharing is improved as shown in Figure 2.5(c), where the large current sharing error of I_1 and I_2 is reduced to I'_1 and I'_2 . However, the load voltage regulation at this juncture was sacrificed while supplying the same load current due to the load regulation characteristic slope. Therefore, a trade-off must be made between the current sharing and the load voltage regulation performance in applying the droop method for paralleling of power modules.

2.3 CENTRALIZED CONTROLLER VS. DECENTRALIZED CONTROLLER

Despite various claims regarding each approach's superiority compare with the others in the publication, there are limitations in all approaches. Thus, this section will address the advantages and limitation in both control schemes.

Figure 2.5. Droop current sharing method: (a) block diagram of paralleled two power modules; (b) effect of output voltage mismatch; (c) load regulation characteristic.

2.3.1 ISSUES IN CENTRALIZED CONTROL SCHEME

In the centralized control scheme, the system reliability depends exclusively on the existence of a supervisory control unit and the communication cable among modules. If the supervisory control unit fails, the whole system will breakdown because the current sharing control command property for each paralleled module is lost. When this occurs, each module will generate its own ‘false’ current sharing reference that could jeopardize the output load. Moreover, if the communication cable is broken, the paralleled modules will not be able to receive or share the current information. This too will provide a ‘false’ current sharing reference to each module. Thus, the system reliability is at stake if either the supervisory control unit fails or a communication cable is broken. One of the ways to overcome this limitation is to duplicate the communication cable and control units via redundancy.

Furthermore, the inherent flexibility features of paralleling architecture will also be limited and reduced tremendously due to the limitation of communication cable as well as supervisory control input/output interface. This is because any expansion or removal of module requires restructuring of the communication cable and also reconstructing of the supervisory control unit so that all the modules are able to receive and transmit accurate information with the correct number of paralleled modules. Therefore, this centralized control scheme is usually pre-specified and designed according to the predefined usability, which is not flexible in nature for future expansion or reduction.

The other concerned issues in the centralized control scheme are the performance and reliability in the paralleled system during module failure. This is because when one of the paralleled modules fails, it can influence the others by contributing faulty current

information to the other modules. Unless it has good supervisory control unit to govern and isolate this fault, the system reliability will be at stake due to uncontrolled output current during fault. Hence, a reliable paralleled system should incorporate ‘fault-proof’ techniques to minimize the effects of the faulty module. This remains unexplored and will be dealt with by a proposed compensation strategy during fault in this thesis.

On the other hand, there are numerous advantages in this centralized control scheme. One of the main advantages in this scheme over decentralized control is that it ensures near-perfect current distribution according to the controller type without the disadvantages of the droop method, such as degraded output voltage regulation and/or trimming of voltage references as illustrated in Section 2.2.2. Moreover, this scheme can integrate all kinds of control schemes to enhance the system transient respond and also to regulate its output power, as shown in various publication [7,15-19,25,26,29-31,35-37]. The objectives of each published control method remain the same, i.e. to improve current sharing, enhance system dynamics response and increase output performance. In recap, the ‘ideal’ centralized control scheme should incorporate the previously mentioned objectives as well as a ‘fault-proof’ strategy in order to enhance system reliability.

2.3.2 ISSUES IN DECENTRALIZED CONTROL SCHEME

This method is the most desirable scheme in the paralleling architecture because of its higher reliability and at the meantime its ability in ensuring acceptable current sharing among paralleled converters. This is because each module uses only locally measured variables for its own controller. If one of the converters fails, the remaining ‘survival’ modules will absorb and share the rest of the load among them, without having to depend on the corrupted current sharing information. Furthermore, any expansion or module

removal in the paralleled system can be performed with ease without any limitation of a communication cable. Thus, the flexibility and reliability of the paralleled system is conserved in this decentralized control scheme.

However, the well-known technique of droop method employed, under this scheme, has wide limitation due to its inherent droop characteristic [20-23,32-34,40] such as static trade-off between power sharing and voltage regulation, limited transient response and improper sharing of harmonic currents [34]. This is because in order to implement the droop method, interface impedance (Z), as shown in Figure 2.4, is incorporated between the paralleled modules and thus limits the module performances. The commonly used interfaces are either a physical or virtual resistor in a paralleled DC-DC converter and an inductive reactance for the paralleled inverters. The limitation due to this interface is further explained analytically in Section 3.3.

Besides the current sharing issue, synchronization of paralleled power module is the next important issue in this scheme, especially for paralleling of inverters. Synchronization is important and necessary in paralleled inverters in order to ensure that all output voltages are synchronized in frequency, phase and amplitude [7,32-41]. This avoids large circulating currents flowing among the inverters that will otherwise decrease system capability by forcing the components to operate beyond their rated current value.

Therefore, in order to achieve high modularity and good reliability as well as fast transient response and good voltage regulation, a decentralized control scheme without the inherent drawbacks of the droop method is desirable. These desired features are developed and incorporated in the proposed decentralized controller scheme in Chapter 5.

2.4 BUCK CONTROLLER DESIGN ARCHITECTURE

This section will illustrate the design of the basic buck configuration that will be used in this thesis. A single buck converter with two-state feedback will be implemented initially and eventually it will be paralleled with two or more individual units to verify the effectiveness of the proposed techniques. All evaluation of proposed techniques throughout the whole research will be based on this buck configuration paralleled power module.

The basic schematic of the buck converter is shown in Figure 2.6. In continuous conduction mode, the inductor current (i_L) will maintain above zero at all times during operation. In order to simplify the buck converter circuit, one assumes that the input voltage (V_{in}) and the switch (Q) will constantly generate sufficient voltage to maintain a constant output voltage to the load (V_C). This assumption is based on the premise that the output filter capacitor is large enough to maintain the output voltage for duration of a period. Hence, the simplified circuit is shown in Figure 2.7, which only consists of a voltage source (V_{PWM}) that represents a constant averaged supply and the remaining resistor-inductor-capacitor (RLC) circuit at the load. It is assumed in this study, that the capacitor does not have an equivalent series resistance (ESR) and the inductor has internal resistance (R_{int}). The triggering signal to control the switching of Q is obtained from a pulse-width-modulation (PWM) signal. Further information regarding various control methods of a single buck converter can be found in [42].

Figure 2.6. Schematic diagram of a buck converter.

Figure 2.7. Simplified schematic diagram of a buck converter.

Applying Kirchhoff Voltage Law (KVL) and Current Law (KCL), the corresponding equation derived from Figure 2.7 is as shown in (2.1) and (2.2).

$$\tilde{V}_{PWM} = \tilde{V}_L + \tilde{V}_C \quad (2.1)$$

$$\tilde{i}_L = \tilde{i}_C + \tilde{i}_{Load} \quad (2.2)$$

where $\tilde{V}_L = L \frac{d\tilde{i}_L}{dt} + R_{int} \tilde{i}_L$ and $\tilde{V}_C = \frac{1}{C} \int \tilde{i}_C dt$, and $\tilde{x}$ represents an instantaneous value with x as its Laplace Transform.

Taking the Laplace Transform for V_L and V_C , (2.1) can be written as (2.3).

$$V_{PWM} = Ls i_L + R_{int} i_L + \frac{1}{Cs} i_C \quad (2.3)$$

By substituting $V_{Load} = V_C$ and $i_{Load} = \frac{V_{Load}}{R_{Load}}$ into (2.2), it can be further written as (2.4).

$$i_L = i_C + \frac{V_C}{R_{Load}} \quad (2.4)$$

From (2.3) and (2.4), the equivalent state variable diagram for a buck converter can be drawn as shown in Figure 2.8. Neglecting the dynamics of the switching PWM signals, the averaged PWM subsystem can be represented crudely as a zero-order hold of duration

K_O , where K_O is equal to the duration of the PWM's period, $\left(K_O = \frac{1}{T_{PWM}}\right)$. The

bandwidth of this first order lag is $\frac{1}{K_O}$ in rads^{-1} or $\frac{1}{2\pi K_O}$ in Hertz. Thus, the first order lag can be expressed as (2.5).

$$\frac{1}{1 + \frac{s}{K_O}} \quad (2.5)$$

Figure 2.8 shows that the system model consists of two integrators and two controllable states, viz. V_C and i_L . Since both states are readily measured by sensors, conventional feedback method is applicable.

In general, a good control of the inner loop is achieved before the outer loop, as shown in Figure 2.9. In this case, the inner and outer loops are current and voltage loops respectively. The decoupling loop is deployed to further enhance the disturbance rejection of the controlled plant for the capacitor voltage. The reason for not apply feedforward cancellation for the negative feedback of R_{int} is because the required gain value R_{int} is not

easily matched. This is due to resistor tolerance that ranges from 2-20%. Hence, the decoupling of R_{int} is not taken into consideration in this study but its effects will be studied in the following section.

Figure 2.8. Equivalent state variable block diagram of a buck converter.

Figure 2.9. Two states feedback controller design for buck converter.

The controllers K_I and K_2 are series compensators for the control loops, and their values are given in (2.6) and (2.7) respectively.

$$K_1 = K_1' \tilde{L} \quad (2.6)$$

$$K_2 = K_2' \tilde{C} \quad (2.7)$$

The curled notation for parameters $\tilde{L}$ and $\tilde{C}$ indicates the estimated values of inductor L and C respectively. K_1' and K_2' will be defined in the following Subsection 2.4.1. The stability of this system will be analytically discussed in Chapter 3 for both single and paralleled power modules.

To simplify the design of this buck converter, a proportional controller for the democratic current sharing scheme is employed in the first part of this thesis. This controller has the current sharing characteristic of a centralized control scheme. In other words, each converter will have an individual proposed controller to ensure near-perfect equal current sharing among converters and also a shared bus to transmit current sharing information. The main objective of this proposed controller is to ensure near perfect equal current sharing and system stability.

2.4.1 IMPLEMENTATION APPROACH

To illustrate the design of the current sharing controller, a system with two similar buck converters ($N = 2$) is shown in Figure 2.10. In this system, it is assumed that the structures of the plants as well as the controllers are identical for each converter module. Thus, the controllers (M, K_1, K_2) for each module has identical values, where $\tilde{L}$ and $\tilde{C}$ are the rated value (i.e. excluding the variation errors). In order to simulate a practical condition, the inductors (L_1 and L_2) will have a variation of about 20% from the rated value, and also its corresponding internal resistances (R_{int1} and R_{int2}), varies about 20% from each other. This circuit has the following components value:

- Input voltage (V_{in}): 10V
- Output voltage (V_{out}) = Reference voltage (V_{ref}): 5V

- Rated output current for each converter (I_L): 1A
- Duty ratio (D): 0.5
- Switching frequency (f_s): 25kHz
- Inductor with internal resistance:
 - $L_1 = 0.940\text{mH}$, $R_{int1} = 0.58\Omega$
 - $L_2 = 0.900\text{mH}$, $R_{int2} = 0.62\Omega$
- Capacitor (C): 470 μF
- Output load (R_{Load}): 5 Ω

Figure 2.10. Control block diagram of paralleled two buck converters.

2.4.1.1 DESIGN OF CONTROLLERS K_I AND K_2

The switching frequency f_s in the circuit is represented by K_O . The controller K_I is selected as described in (2.6). As mentioned in [43], the overall gain crossover frequency should not be close to the switching frequency to avoid amplification of the ripple voltage.

Hence, the recommended practical value for selecting the crossover frequency is (2.8), which is 20 percent of the switching frequency; and K'_2 is selected as (2.9).

$$f_{xo} = \frac{f_s}{5} \quad (2.8)$$

where f_{xo} = crossover frequency and f_s = switching frequency.

$$K'_2 = \frac{K_o}{5} \quad (2.9)$$

On the other hand, the desired relationship between K'_1 and K'_2 is such that the system response is overdamped. Since the paralleled converters are formed by two individual buck converters, the selection of K'_1 and K'_2 will be based on single buck converter design. Based on Figure 2.9 and with the following assumptions, the state variables of the system can be expressed as (2.10) and (2.11). The assumptions are:

- Equation (2.5) is approximately unity due to high K_o and also during steady state, the output of K_1 is equal to V_{PWM} .
- R_{int} is very small and negligible in this case.
- i_{Load} is considered as an external disturbance injection into the system.

$$sV_c = \frac{1}{C} i_c \quad (2.10)$$

$$\begin{aligned} si_L &= \frac{1}{L} (K'_1 L) (-i_L + K'_2 C (V_{ref} - V_c)) \\ i_L &= \frac{K'_1 K'_2 C}{(s + K'_1)} (V_{ref} - V_c) \end{aligned} \quad (2.11)$$

Substitute (2.10) and (2.11) into $i_c = i_L - i_{Load}$ yield (2.12).

$$V_C = \frac{K_1' K_2'}{s^2 + K_1' s + K_1' K_2'} V_{ref} - \frac{(s + K_1')}{s^2 + K_1' s + K_1' K_2'} \frac{1}{C} i_{Load} \quad (2.12)$$

Thus, the respective transfer functions of the system are shown in (2.13) and (2.14).

$$\left. \frac{V_C}{V_{ref}} \right|_{i_{Load}=0} = \frac{K_1' K_2'}{s^2 + K_1' s + K_1' K_2'} \quad (2.13)$$

$$\left. \frac{V_C}{i_{Load}} \right|_{V_{ref}=0} = - \frac{(s + K_1')}{s^2 + K_1' s + K_1' K_2'} \frac{1}{C} \quad (2.14)$$

Generally, a second order system transient response will be determined by two quantities, which are called the natural frequency (ω_n) and damping ratio (ζ) as shown in (2.15) for a second order transfer function.

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2.15)$$

Furthermore, in this design, it is desirable to have the system with critically damped response without an overshoot. Hence, the damping ratio of the system should have the value of 1 ($\zeta=1$). Therefore, the system dynamics can be obtained by equating (2.13) and (2.15), as shown in (2.16)-(2.17).

$$\omega_n = \sqrt{K_1' K_2'} \quad (2.16)$$

$$2\zeta\omega_n = K_1' \quad (2.17)$$

Finally, the criteria for critically damped system response can be found by substituting $\zeta=1$ and (2.16) into (2.17), as shown in (2.18).

$$\begin{aligned} 2\sqrt{K_1' K_2'} &= K_1' \\ 4K_1' K_2' &= K_1'^2 \\ 4K_2' &= K_1' \end{aligned} \quad (2.18)$$

Therefore, from (2.9) and (2.18), the desired relationship of K_1' and K_O can be equated as (2.19).

$$K_1' = \frac{4K_O}{5} \quad (2.19)$$

However, (2.18) and (2.20) is selected for this study in order to ensure that the system is overdamped and also it is below the recommended crossover frequency as mentioned earlier.

$$K_1' = \frac{K_O}{5} \quad (2.20)$$

2.4.1.2 DESIGN OF CONTROLLER M

The controller M is design after both the controllers K_1 and K_2 have been identified. The controller M is chosen as a proportional controller. The reason for not having other types of controller is that the other controllers, such as proportional-integral (PI) controller, will introduce additional integrator into the system, which directly increases the system matrix and introduces extra poles into the system. Such problem is described in [15-16] where M is a proportional-integral-derivative (PID) controller.

Before the gain value for controller M is identified, the effects of M towards the current sharing properties in steady state should be investigated in order to apprehend the need of the current sharing loop. The diagram that focus on the current sharing loop for system with $N = 2$, is shown in Figure 2.11.

Figure 2.11. Current sharing controller block diagram.

Figure 2.12. Equivalent representations for current sharing loop.

In steady state, it is assumed that V_{PWM} is equal to output of K_I and hence the PWM subsystem will be neglected in this analysis. Figure 2.11 can be further represented as shown in Figure 2.12, where the negative feedback of inductor current (i_L) is incorporated with the internal resistance (R_{int}).

The individual inductor currents from Figure 2.12 can be written as (2.21) and (2.22).

$$i_{L1} = \frac{K_1}{L_1 s} \left(i^* + M(i_{ref} - i_{L1}) - \left(1 + \frac{R_{int1}}{K_1} \right) i_{L1} \right) \quad (2.21)$$

$$i_{L2} = \frac{K_1}{L_2 s} \left(i^* + M(i_{ref} - i_{L2}) - \left(1 + \frac{R_{int2}}{K_1} \right) i_{L2} \right) \quad (2.22)$$

However, at steady state with DC currents, $\frac{di_{Lj}}{dt} = 0$ and hence (2.21) and (2.22) can be further reduced to (2.23) and (2.24) respectively.

$$0 = i^* + M i_{ref} - \left(1 + \frac{R_{int1}}{K_1} + M \right) i_{L1} \quad (2.23)$$

$$0 = i^* + M i_{ref} - \left(1 + \frac{R_{int2}}{K_1} + M \right) i_{L2} \quad (2.24)$$

The current sharing error in steady state can be found by subtracting (2.23) with (2.24), as shown in (2.25).

$$\Delta i \left(1 + \frac{R_{int2}}{K_1} + M \right) = \frac{\Delta R}{K_1} i_{L1} \quad (2.25)$$

where $\Delta i = i_{L1} - i_{L2}$ and $\Delta R = R_{int1} - R_{int2}$.

Since $K_I \gg R_{int2}$, it is assumed that $\frac{K_I}{R_{int2}} + 1 \cong \frac{K_I}{R_{int2}}$. Therefore, substituting the assumption into (2.25), the ratio of current sharing error with respect to i_{L1} can be written as (2.26).

$$\frac{\Delta i}{i_{L1}} \cong \frac{\Delta R}{R_{int2}} \left(\frac{1}{(1+M) \frac{K_I}{R_{int2}}} \right) \quad (2.26)$$

Equation (2.26) clearly spells out that in order to reduce the steady state error in current sharing (Δi), the following parameters could be modified.

- i. Reduce ΔR .
- ii. Increase controller gain value of K_I .
- iii. Increase controller gain value of M .

However, among the three parameters, only the controller gain M could be utilized in order to reduce the steady state error in this case. This is because additional resistor could not eliminate the effects of ΔR as every resistor has its equivalent tolerance that ranges from 2-20%. Moreover, there is a limitation to the controller gain of K_I , whose choice is described in (2.18)-(2.20). Thus, the only remaining component that is available in this case is controller gain of M . The limitation on the magnitude of controller gain M will be discussed in Chapter 3. Nevertheless, $M = 20$ is chosen in this study so that the steady state current sharing error is about 0.001A, as calculated based on (2.26) and the system parameters given earlier in Section 2.4.1. The aim of that selection is to reduce Δi in steady state.

2.4.2 SIMULATION RESULTS

To demonstrate the effectiveness of controller M in the current sharing, an additional 1Ω resistor is included in series with inductor L_2 to amplify ΔR in (2.26). System response without controller M (i.e. $M=0$) are shown for output voltage (V_c) and individual currents (i_{L1} and i_{L2}) through simulation in Figure 2.13 and Figure 2.14 respectively. The parameters required in the simulation are the plant information as described earlier in Section 2.4.1 and controllers' information which are obtained from (2.6), (2.7), (2.18), (2.20) with $M = 20$. To verify that the crossover frequency is as required in (2.9), the system Bode plot is shown in Figure 2.15.

Figure 2.13. Starting output voltage without controller M .

Figure 2.14. Starting output inductor currents (i_{L1} and i_{L2}) without controller M . Figure 2.15 Bode plot system without controller M .

Figure 2.14 reveals that there is a steady state error in current sharing without controller M , where $i_{L1} = 0.4816\text{A}$ and $i_{L2} = 0.4655\text{A}$, although the total current is closed to the rated value, i.e. $i_{total} = 1\text{A}$. This appears after the 0.8ms mark in Figure 2.14 and is not obvious in the figure due to the vertical scale chosen to include the initial current transient. Figure 2.15 shows that the crossover frequency is 1.19 kHz, which is below the minimum requirement of 5 kHz, i.e. one fifth of switching frequency.

When controller M is included into the system, the current sharing error is reduced as compared with the system without it, as shown in Figure 2.16 and Figure 2.17 for voltage and individual currents, respectively. Again, to ensure that the requirement (2.9) has not been violated the system Bode plot with controller M is given in Figure 2.18.

Figure 2.16. Starting output voltage with controller M .

Figure 2.17. Starting output currents (i_{L1} and i_{L2}) with controller M for two buck converters.

Figure 2.18 Bode plot for system with controller M .

Figure 2.17 demonstrates the effectiveness of controller M in reducing the error in current sharing among the converters (see the currents after the 0.8ms mark). The steady state value for each inductor current is $i_{L1} = 0.4735\text{A}$, and $i_{L2} = 0.4736\text{A}$. Moreover, Figure 2.18 shows that the controller M does not contribute to any change in the system crossover frequency. Although there is small steady state error of about 0.3V in output voltage, this can be reduced by feedforwarding the load disturbance into the system in between controllers K_1 and K_2 . Nonetheless, the main focus in this analysis is to demonstrate the effectiveness of controller M in ensuring the near-perfect equal current sharing among converters.

2.4.3 HARDWARE IMPLEMENTATION

The realization of the current sharing controller's effectiveness can be demonstrated by hardware implementation. The system shown in Figure 2.10 with $N = 2$ is implemented in the laboratory setting by using a combination of subtracting, summing and inverting operational amplifiers in the circuit. The schematic diagram of the whole circuit is shown in Figure 2.19.

Figure 2.19. Schematic diagram of current sharing controller for two buck converters.

2.4.4 EXPERIMENTAL RESULTS

The following Figures 2.20 and 2.21 are the output voltage and current waveforms respectively for the first buck converter without paralleling. Figures 2.22 and 2.23 are the second buck converter's output voltage and current waveforms respectively. From Figures 2.21 and 2.23, the inductor current for each converter, #1 and #2, is about 0.9A and 1A respectively.

Figure 2.20. The starting output voltage V_{C1} (Ch2: 1V/div) for buck converter #1 (Time: 5ms/div) when it was power-up (oscilloscope triggering time at about 20ms), without parallel to converter #2.

Figure 2.21. The starting output inductor current I_{L1} (Ch1: 0.4A/div) for buck converter #1 (Time: 5ms/div) when it was power-up (oscilloscope triggering time at about 20ms), without parallel to converter #2.

Figure 2.22. The starting output voltage V_{C2} (Ch2: 1V/div) for buck converter #2 (Time: 5ms/div) when it was power up (oscilloscope triggering time at about 15ms), without parallel to converter #1.

Figure 2.23. The starting output inductor current i_{L2} (Ch1: 0.4A/div) for buck converter #2 (Time: 5ms/div) when it was power-up (oscilloscope triggering time at about 15ms), without parallel to converter #1

The following Figures 2.24 and 2.25 are the voltage and current waveforms respectively for the paralleled converters without current-sharing controller ($M=0$). Figure 2.25 distinctly shows that both converters are sharing unevenly the load of 1A.

Figure 2.24. The starting output voltages of converter #1 [Ch1: V_{C1} (1V/div)] and converter #2 [Ch2: V_{C2} (1V/div)] when it was power-up (oscilloscope triggering time at about 20ms), in the paralleled configuration *without* current sharing controller ($M=0$) (Time: 5ms/div).

Figure 2.25. The starting output currents of converter #1 [Ch1: i_{L1} (0.4A/div)] and converter #2 [Ch2: i_{L2} (0.4A/div)] when it was power-up (oscilloscope triggering time at about 20ms), in the paralleled configuration *without* current sharing controller ($M=0$) (Time: 5ms/div)

Although each converter share the same voltage as shown in Figure 2.24, Figure 2.25 clearly shows that there is error in current sharing when two converters are paralleled together. Inductor current converter #2 is slightly higher than converter #1 in steady state. Moreover, the total current of the same load is shared among the converters, where each converter #1 and #2 is generating about 0.5A and 0.6A, respectively.

In order to reduce this error, a current sharing controller M for each converter is incorporated into the paralleled system. The following figures demonstrate the

effectiveness of controller M in reducing the error in current sharing. The output voltages are shared equally among themselves as shown in Figure 2.26. In addition, the inductor currents for both converters, as shown in Figure 2.27, are sharing near-perfectly the load current, where $i_{L1} \cong i_{L2} \cong 0.5$ A.

Figure 2.26. The starting output voltages of converter #1 [Ch1: V_{C1} (1V/div)] and converter #2 [Ch2: V_{C2} (1V/div)] when it was power-up (oscilloscope triggering time at about 15ms), in the paralleled configuration *with* current sharing controller (Time: 5ms/div).

Figure 2.27. The starting output currents of converter #1 [Ch1: i_{L1} (0.2A/div)] and converter #2 [Ch2: i_{L2} (0.2A/div)] when it was power-up (oscilloscope triggering time at about 20ms), in the paralleled configuration *with* current sharing controller (Time: 5ms/div).

2.5 DISCUSSION AND CONCLUSION

Based on the previous experimental result as shown in Figure 2.25, it is shown that the system without current sharing controller is not able to share their current equally. In the long run, each converter might age differently caused by an uneven distribution of stresses. Moreover, there is a possibility of having one converter operating at its maximum rated value, whereas the others are operating at a lower capacity or even not in operation. When this occurs, the tendency of the overworked converter to deteriorate and fail is higher than for the rest. Moreover, the sudden failure of that particular converter

could also disturb the current sharing among the remaining converters and this might eventually jeopardize the system stability. Hence, near-perfect equal current is desirable.

In recap, the current sharing methodologies and its categorization is presented in this chapter. The design of a simple buck converter controller is also illustrated. The paralleling of two buck converters with an analysis of the effect of current sharing controller M on the current error is given in this chapter. The hardware implementation as well as the simulation and experimental results attest the feasibility of paralleling two or more converters with a simple current sharing controller and with achievable near-perfect current sharing.

In general, a high controller gain M as shown in (2.26) leads to better current sharing but could lead to possible instability in the paralleled system. There is thus a need to examine the stability of the paralleled system in general, and in particular on any effect the magnitude of M has on the stability. This study will be presented in Chapter 3.

Chapter 3 STABILITY ANALYSIS AND DYNAMICS OF PARALLELED POWER MODULES

3.1 INTRODUCTION

The first step towards designing a good controller is to study the stability of the overall system in order to ensure that it has all the stable properties. The stability analysis of the paralleled power modules is more complicated and has been tackled less often, while the analysis and design techniques for ensuring stable operation of a single converter have been discussed extensively in the literature [15]. As a result, most systems are typically designed by relying heavily on expensive prototyping and testing or extensive simulation.

A general framework of stability analysis for paralleled power modules using state-variable technique is employed in this thesis. This stability study demonstrates analytically that the complete stability of a paralleled power module depends on the stability of both the differential-mode and common-mode properties. The differential-mode property in this case is affected by the current-sharing loop, which are being controlled individually by the current-sharing controller loop. On the other hand, the common mode property is dependent on output and load impedances and the number of modules; being independent of the current sharing loops.

The general framework of stability analysis for paralleled power modules will be analytically illustrated in Section 3.2, including the description of both differential-mode and common-mode stability analysis. The DC-DC buck converter operating at continuous

conduction mode, as designed in Section 2.4, is used as the basic module in this stability analysis of paralleled power modules. Section 3.3 analyzes the stability of the droop method and also illustrates the effect of the interfaced impedance towards the dynamics of the system. Finally, the conclusion and discussion of this chapter will be presented in Section 3.4.

3.2 DYNAMICS AND STABILITY ANALYSIS OF A PARALLELED SYSTEM WITH AND WITHOUT CURRENT-SHARING CONTROLLERS

The dynamics and stability analysis is done here on the system with N -paralleled power modules as shown in Figure 3.1. The proportional gain of current-sharing controller M in Figure 3.1 represents a generic controller for three different schemes, viz. the democratic, master-slave and without current sharing controller scheme (i.e. $M=0$). The democratic current sharing scheme is realized when the entire modules' current-sharing controllers M have same gain, i.e. $M_1 = M_j = M_N$. On contrary, the master-slave scheme can be obtained by making the first current-sharing controller gain greater than the other modules, $M_1 > M_{j \neq 1}$, where $j = 2, \dots, N$. Finally, Figure 3.1 can represent the paralleling of power modules without current-sharing controllers by having a null controller gain M ($M_1 = M_j = M_N = 0$) for all the modules.

Figure 3.1. N -paralleled power modules with ϵ representing parameter deviations, and

$$M_1 = M_J = M_N = M.$$

In a realistic system, parameter deviations exist for each module. These parameter deviations can cause the output current of each module to deviate from the desired shared value. These parameter deviations are modeled in this analysis as disturbances to the modules' output current. This effect is represented as an external source of disturbance, $\delta \epsilon_j$, as shown in Figure 3.1. In addition, the current-sharing controllers M in this analysis are assumed to have same gain, i.e. $M_1 = M_J = M_N = M$.

The focus of this study is on the democratic current sharing scheme, where the final state equation will be simplified. The case of different current-sharing controllers M will not be considered due to the coupling of the current states which results in a more

complex system. This slight variation in current-sharing controllers M , however, can be dealt with by the approximation of the error injection $\delta\epsilon_j$ into the system.

The complete state vector for the paralleled system in Figure 3.1, comprises signals at the output of each integrator ($\frac{1}{s}$). Hence, the state vector for N paralleled power modules has for state variables $V_{P1}, \dots, V_{PJ}, \dots, V_{PN}, i_{L1}, \dots, i_{LJ}, \dots, i_{LN}$, and V_C . The total number of state variables for this N -paralleled power module is $2N+1$. Based on Figure 3.1, the inductor current for power module #1 (i_{L1}), output of PWM (V_{P1}) and output voltage (V_C) can be derived as (3.1)-(3.3) respectively.

$$i_{L1} = \frac{1}{Ls} (\delta\epsilon_1 + V_{P1}) \quad (3.27)$$

$$V_{P1} = \frac{K_o}{s} \left(K_1 \left(M \left(\frac{I}{N} - i_{L1} \right) + \frac{K_2}{N} (V_{ref} - V_c) - i_{L1} \right) - V_{P1} \right) \quad (3.28)$$

$$V_c = \frac{I}{Cs} \quad (3.29)$$

From (3.1)-(3.3) and Figure 3.1, the state equation for N -paralleled power modules can be represented in a state-space form of (3.4).

$$\dot{x} = Ax + Bu \quad (3.30)$$

where respective value of $A, B, \dot{x}, x, u$ is defined in (3.5).

$$\begin{aligned}
\begin{bmatrix} \dot{V}_{P1} \\ \vdots \\ \dot{V}_{PN} \\ \dot{i}_{L1} \\ \vdots \\ \dot{i}_{LN} \\ \dot{V}_C \end{bmatrix} &= \begin{bmatrix} -K_0 & 0 & \cdots & 0 & \alpha & \beta & \cdots & \beta & \gamma \\ 0 & \ddots & & \vdots & \beta & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & 0 & \vdots & & \ddots & \beta & \vdots \\ 0 & \cdots & 0 & -K_0 & \beta & \cdots & \beta & \alpha & \gamma \\ \frac{1}{L} & 0 & \cdots & 0 & 0 & \cdots & \cdots & 0 & 0 \\ 0 & \ddots & & \vdots & \vdots & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & 0 & \vdots & & \ddots & \vdots & \vdots \\ 0 & \cdots & 0 & \frac{1}{L} & 0 & \cdots & \cdots & 0 & 0 \\ 0 & \cdots & \cdots & 0 & \frac{1}{C} & \cdots & \cdots & \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} V_{P1} \\ \vdots \\ V_{PN} \\ i_{L1} \\ \vdots \\ i_{LN} \\ V_C \end{bmatrix} \\
&+ \begin{bmatrix} 0 & \cdots & \cdots & 0 & -\gamma \\ \vdots & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & \vdots & \vdots \\ 0 & \cdots & \cdots & 0 & -\gamma \\ \frac{1}{L} & 0 & \cdots & 0 & 0 \\ 0 & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & 0 & \vdots \\ 0 & \cdots & \cdots & \frac{1}{L} & 0 \\ 0 & \cdots & \cdots & 0 & 0 \end{bmatrix} \begin{bmatrix} \delta \mathcal{E}_1 \\ \vdots \\ \vdots \\ \delta \mathcal{E}_N \\ V_{ref} \end{bmatrix}
\end{aligned} \tag{3.31}$$

where

$$\begin{aligned}
\alpha &= K_0 K_1 L \left(M \left(\frac{1}{N} - 1 \right) - 1 \right) \\
\beta &= \frac{K_0 K_1 L M}{N} \\
\gamma &= -\frac{K_0 K_1 L K_2 C}{N}
\end{aligned}$$

From (3.5), it is not obvious that the stability of the paralleled power modules is dependent on common-mode and differential-mode properties. In order to illustrate those properties, the paralleled system will be represented with different state variables by vector transformation. Notwithstanding, the transfer function and system eigenvalues

remain the same even though a new set of state variables is adopted. Hence, the new state

vector has the following new state variables, i.e. $V_{PJ} - \frac{\sum V_{Pi}}{N}$, $i_{LJ} - \frac{I}{N}$, $\sum V_{Pi}$, I and V_C .

The state equation transformation of (3.4) will be briefly illustrated. Let $x = Pz$, where P = transformation matrix and z = new state vector. Substitute it into (3.4) gives (3.6).

$$P\dot{z} = APz + Bu \quad (3.32)$$

By multiplying both sides of (3.6) with the inverse of P , the equivalent system representation for (3.4) using the new state vector z is (3.7).

$$\dot{z} = P^{-1}APz + P^{-1}Bu \quad (3.33)$$

The transformation matrix P can be deduced as (3.10), and the inverse of P is (3.11) by substituting the old state vector of (3.8) and new state vector of (3.9) into $x = Pz$.

$$x^T = [V_{P1} \quad \cdots \quad V_{PN} \quad i_{L1} \quad \cdots \quad i_{LN} \quad V_C] \quad (3.34)$$

$$z^T = \left[V_{P1} - \frac{\sum V_{Pi}}{N} \quad \cdots \quad V_{P(N-1)} - \frac{\sum V_{Pi}}{N} \quad i_{L1} - \frac{I}{N} \quad \cdots \quad i_{L(N-1)} - \frac{I}{N} \quad \sum V_{Pi} \quad I \quad V_C \right] \quad (3.35)$$

$$P = \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 & 0 & \cdots & \cdots & 0 & 0 & \frac{1}{N} & 0 & 0 \\ 0 & \ddots & & \vdots & \vdots & \vdots & \ddots & & \vdots & \vdots & \vdots & \vdots & \vdots \\ \vdots & & \ddots & 0 & \vdots & \vdots & & \ddots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & 1 & 0 & 0 & \cdots & \cdots & 0 & 0 & \frac{1}{N} & 0 & 0 \\ -1 & \cdots & \cdots & -1 & 0 & 0 & \cdots & \cdots & 0 & 0 & \frac{1}{N} & 0 & 0 \\ 0 & \cdots & \cdots & 0 & 1 & 0 & \cdots & \cdots & 0 & 0 & 0 & \frac{1}{N} & 0 \\ 0 & \cdots & \cdots & 0 & 0 & 1 & 0 & \cdots & 0 & 0 & 0 & \frac{1}{N} & 0 \\ \vdots & \ddots & & \vdots & \vdots & 0 & \ddots & & \vdots & \vdots & \vdots & \vdots & \vdots \\ \vdots & & \ddots & \vdots & \vdots & \vdots & & \ddots & 0 & \vdots & \vdots & \vdots & \vdots \\ 0 & \cdots & \cdots & 0 & 0 & 0 & \cdots & 0 & 1 & 0 & 0 & \frac{1}{N} & 0 \\ 0 & \cdots & \cdots & 0 & 0 & 0 & \cdots & \cdots & 0 & 1 & 0 & \frac{1}{N} & 0 \\ 0 & \cdots & \cdots & 0 & -1 & -1 & \cdots & \cdots & -1 & -1 & 0 & \frac{1}{N} & 0 \\ 0 & \cdots & \cdots & 0 & 0 & 0 & \cdots & \cdots & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \quad (3.36)$$

$$P^{-1} = \begin{bmatrix} 1 - \frac{1}{N} & -\frac{1}{N} & \cdots & -\frac{1}{N} & -\frac{1}{N} & 0 & \cdots & \cdots & 0 & 0 & 0 \\ -\frac{1}{N} & \ddots & & \vdots & \vdots & \vdots & \ddots & & \vdots & \vdots & \vdots \\ \vdots & & \ddots & -\frac{1}{N} & \vdots & \vdots & & \ddots & \vdots & \vdots & \vdots \\ -\frac{1}{N} & \cdots & -\frac{1}{N} & 1 - \frac{1}{N} & -\frac{1}{N} & 0 & \cdots & \cdots & 0 & 0 & 0 \\ 0 & \cdots & \cdots & 0 & 0 & 1 - \frac{1}{N} & -\frac{1}{N} & \cdots & -\frac{1}{N} & -\frac{1}{N} & 0 \\ \vdots & \ddots & & \vdots & \vdots & -\frac{1}{N} & \ddots & & \vdots & \vdots & \vdots \\ \vdots & & \ddots & \vdots & \vdots & \vdots & & \ddots & -\frac{1}{N} & \vdots & \vdots \\ 0 & \cdots & \cdots & 0 & 0 & -\frac{1}{N} & \cdots & -\frac{1}{N} & 1 - \frac{1}{N} & -\frac{1}{N} & 0 \\ 1 & \cdots & \cdots & 1 & 1 & 0 & \cdots & \cdots & 0 & 0 & 0 \\ 0 & \cdots & \cdots & 0 & 0 & 1 & \cdots & \cdots & 1 & 1 & 0 \\ 0 & \cdots & \cdots & 0 & 0 & 0 & \cdots & \cdots & 0 & 0 & 1 \end{bmatrix} \quad (3.37)$$

The new system matrix $P^{-1}AP$ and input matrix $P^{-1}B$ are deduced as (3.12) and (3.13) respectively by substituting (3.10) and (3.11) into (3.7).

$$P^{-1}AP = \begin{bmatrix} -K_0 & 0 & \cdots & 0 & -\Psi & 0 & \cdots & 0 & 0 & 0 & 0 \\ 0 & \ddots & & \vdots & 0 & \ddots & & \vdots & \vdots & \vdots & \vdots \\ \vdots & & \ddots & 0 & \vdots & & \ddots & 0 & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & -K_0 & 0 & \cdots & 0 & -\Psi & 0 & 0 & 0 \\ \frac{1}{L} & 0 & \cdots & 0 & 0 & \cdots & \cdots & 0 & 0 & 0 & 0 \\ 0 & \ddots & & \vdots & \vdots & \ddots & & \vdots & \vdots & \vdots & \vdots \\ \vdots & & \ddots & 0 & \vdots & & \ddots & \vdots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & \frac{1}{L} & 0 & \cdots & \cdots & 0 & 0 & 0 & 0 \\ 0 & \cdots & \cdots & 0 & 0 & \cdots & \cdots & 0 & -K_0 & -\tilde{\lambda} & -\tilde{\lambda}K_2C \\ 0 & \cdots & \cdots & 0 & 0 & \cdots & \cdots & 0 & \frac{1}{L} & 0 & 0 \\ 0 & \cdots & \cdots & 0 & 0 & \cdots & \cdots & 0 & 0 & \frac{1}{C} & 0 \end{bmatrix} \quad (3.38)$$

where $\Psi = \tilde{\lambda}(1+M)$ and $\tilde{\lambda} = K_0K_1L$.

$$P^{-1}B = \begin{bmatrix} 0 & \cdots & \cdots & 0 & 0 & 0 \\ \vdots & \ddots & & \vdots & \vdots & \vdots \\ \vdots & & \ddots & \vdots & \vdots & \vdots \\ 0 & \cdots & \cdots & 0 & 0 & 0 \\ 1 - \frac{1}{N} & -\frac{1}{N} & \cdots & -\frac{1}{N} & -\frac{1}{N} & 0 \\ -\frac{1}{N} & \ddots & & \vdots & \vdots & \vdots \\ \vdots & & \ddots & -\frac{1}{N} & \vdots & \vdots \\ -\frac{1}{N} & \cdots & -\frac{1}{N} & 1 - \frac{1}{N} & -\frac{1}{N} & 0 \\ 0 & \cdots & \cdots & 0 & 0 & K_0K_1LK_2C \\ \frac{1}{L} & \cdots & \cdots & \frac{1}{L} & \frac{1}{L} & 0 \\ 0 & \cdots & \cdots & 0 & 0 & 0 \end{bmatrix} \quad (3.39)$$

By rearranging the states of the new state vector z , (3.14), through grouping the states of the module together, a modified system matrix (3.15) is obtained.

$$z^T = \left[\overbrace{V_{P1} - \frac{\sum V_{Pi}}{N} \quad i_{L1} - \frac{I}{N}}^{\text{Module 1}} \quad \cdots \quad \overbrace{V_{P(N-1)} - \frac{\sum V_{Pi}}{N} \quad i_{L(N-1)} - \frac{I}{N}}^{\text{Module N-1}} \quad \sum V_{Pi} \quad I \quad V_C \right] \quad (3.40)$$

$$\begin{bmatrix} \boxed{\begin{matrix} -K_0 & -\Psi \\ \frac{1}{L} & 0 \end{matrix}} & & & & & \\ & \boxed{\begin{matrix} -K_0 & -\Psi \\ \frac{1}{L} & 0 \end{matrix}} & & & & 0 \\ & & \boxed{\begin{matrix} -K_0 & -\Psi \\ \frac{1}{L} & 0 \end{matrix}} & & & \\ & & & \boxed{\begin{matrix} -K_0 & -\Psi \\ \frac{1}{L} & 0 \end{matrix}} & & \\ & & & & \boxed{\begin{matrix} -K_0 & -\Psi \\ \frac{1}{L} & 0 \end{matrix}} & \\ & 0 & & & & \begin{matrix} -K_0 & -\lambda & -\lambda K_2 C \\ \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{C} & 0 \end{matrix} \end{bmatrix} \quad (3.41)$$

Based on the system matrix in (3.15), it clearly reveals that only the ‘diagonal’ component matrices have variable quantities and the ‘off-diagonal’ components from those matrices are zero. This unveils the properties of common-mode and differential-mode in the system matrix. The last three components in the state vector are states common to all the paralleled power modules and the last 3x3 sub-matrix in (3.15) gives the common-mode properties for the system. On contrary, the remaining $2N-2$ vector

components in (3.14) comprises differential state variables $(V_{PJ} - \frac{\sum V_{Pi}}{N}, i_{LJ} - \frac{I}{N})$ of each module. The sub-matrix involving the differential states for each module and also decoupled one from another as shown in (3.15) as well as from the common-mode sub-matrix. Therefore, the stability analysis of the paralleled power modules can be segregated into two properties, i.e. by analyzing the common-mode and differential-mode stability analysis independently.

3.2.1 ANALYSIS OF COMMON-MODE PROPERTIES

The common-mode properties shown in (3.16) are extracted from (3.15). The stability of this time-invariant state-space common-mode property of the N -paralleled power modules can be determined by investigating the characteristic polynomial for the system matrix in (3.16). This characteristic polynomial can be found by taking the determinant of $\lambda(s) = |sI - A|$, as shown in (3.17). A basic fact from linear algebra is that the determinant of a matrix is equal to the product of its eigenvalues. Moreover, these eigenvalues determine the major characteristic of both the input-output and initial condition responses of the system. Hence, the common-mode stability can be determined by analyzing these eigenvalues in the characteristic equation (3.17) of system matrix in (3.16).

$$\begin{bmatrix} \dot{\sum V_{Pi}} \\ \dot{i} \\ \dot{V_C} \end{bmatrix} = \begin{bmatrix} -K_0 & -\lambda & -\lambda K_2 C \\ \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} \sum V_{Pi} \\ I \\ V_C \end{bmatrix} + \begin{bmatrix} 0 & \cdots & 0 & \lambda K_2 C \\ \frac{1}{L} & \cdots & \frac{1}{L} & 0 \\ 0 & \cdots & 0 & 0 \end{bmatrix} \begin{bmatrix} \delta \epsilon_1 \\ \vdots \\ \delta \epsilon_N \\ V_{ref} \end{bmatrix} \quad (3.42)$$

$$\begin{aligned}
 \det(sI - A) &= \begin{vmatrix} s + K_0 & K_0 K_1 L & K_0 K_1 L K_2 C \\ -\frac{1}{L} & s & 0 \\ 0 & -\frac{1}{C} & s \end{vmatrix} \\
 &= s^3 + K_0 s^2 + K_0 K_1 s + K_0 K_1 K_2
 \end{aligned} \tag{3.43}$$

Since the eigenvalues in (3.17) are not clearly revealed, the *Routh-Hurwitz* stability criterion [49] is employed to determine whether there are any unstable roots in the polynomial equation without actually solving it. According to this criterion, the information about absolute stability can be obtained directly from the coefficients of the characteristic equation. The criterion states that ‘if any of the coefficients are zero or negative in the presence of at least one positive coefficient, there is a root or roots that are imaginary or that have positive real parts’, and thus the system is not stable. In addition, it also states that ‘the number of roots of an equation with positive real parts is equal to the number of changes in sign of the coefficients of the second column of the *Routh-table*’. It should be noted that the exact values of the terms in the second column need not be known; instead only the signs are needed. The necessary and sufficient condition to ensure that all roots of an equation lie in the left-half of s -plane (LHP) is that all the coefficients of that equation should be positive and all terms in the second column of the *Routh-table* have positive signs. Therefore, the stability constraints in the third order polynomial of (3.17) can be obtained by using *Routh’s* stability criterion, where the coefficients in (3.17) are tabulated in the *Routh-table* as shown in Table 3.1.

Table 3.1. Routh-table of equation (3.17).

S^3	1	K_0K_1	0
S^2	K_0	$K_0K_1K_2$	0
S^1	$-\frac{\begin{vmatrix} 1 & K_0K_1 \\ K_0 & K_0K_1K_2 \end{vmatrix}}{K_0} = K_1(K_0 - K_2)$	0	0
S^0	$-\frac{\begin{vmatrix} K_0 & K_0K_1K_2 \\ K_1(K_0 - K_2) & 0 \end{vmatrix}}{K_1(K_0 - K_2)} = K_0K_1K_2$	0	0

By employing the *Routh-Hurwitz* stability criterion, the common-mode part of the N -paralleled power modules system is stable provided that the second column elements in Table 3.1 are greater than zero. Hence, the stability limits for this system will be $K_0 > K_2$ as computed in (3.18), and $K_0 > 0$, $K_0K_1K_2 > 0$ as inspected from Table 3.1.

$$\begin{aligned}
 K_1(K_0 - K_2) &> 0 \\
 K_0 - K_2 &> 0 \\
 K_0 &> K_2
 \end{aligned} \tag{3.44}$$

Therefore the common-mode properties of the voltage loop controller gain K_2 should be less than the switching frequency dependent gain K_0 and the current loop controller gain K_1 should have positive values in order to ensure stable operation of common-mode subsystem in the N -paralleled power modules. It should also be noted that the current sharing controller gain M has no influence on the properties of the common-mode system as it is not presented in (3.16).

3.2.2 DIFFERENTIAL-MODE DYNAMICS AND STABILITY ANALYSIS

The differential-mode property of J -th power module that is shown in (3.19) is extracted from (3.15). The determinant of differential-mode properties for N -paralleled power modules can be deduced as (3.20). The stability constraints of these differential-mode properties can be derived from Table 3.2 by utilizing the *Routh-Hurwitz* stability criterion and tabulating the coefficients of (3.20) into the *Routh-table*.

$$\begin{aligned}
 \begin{bmatrix} \dot{V}_{PJ} - \frac{\sum V_{Pi}}{N} \\ \dot{i}_{LJ} - \frac{I}{N} \end{bmatrix} &= \begin{bmatrix} -K_0 & -K_0 K_1 L(1+M) \\ \frac{1}{L} & 0 \end{bmatrix} \begin{bmatrix} V_{PJ} - \frac{\sum V_{Pi}}{N} \\ i_{LJ} - \frac{I}{N} \end{bmatrix} \\
 &+ \begin{bmatrix} 0 & \dots & \dots & \dots & \dots & \dots & \dots & 0 \\ -\frac{1}{N} & \dots & -\frac{1}{N} & 1 - \frac{1}{N} & -\frac{1}{N} & \dots & -\frac{1}{N} & 0 \end{bmatrix} \begin{bmatrix} \delta \mathcal{E}_1 \\ \vdots \\ \delta \mathcal{E}_{J-1} \\ \delta \mathcal{E}_J \\ \delta \mathcal{E}_{J+1} \\ \vdots \\ \delta \mathcal{E}_N \\ V_{ref} \end{bmatrix} \quad (3.45)
 \end{aligned}$$

$$\det(sI - A_{(N-1) \times (N-1)}) = \begin{vmatrix} s + K_0 & \Psi & & & \\ -\frac{1}{L} & s & & & 0 \\ & & \ddots & & \\ & & & s + K_0 & \Psi \\ & & & -\frac{1}{L} & s \\ & & & & \ddots \\ 0 & & & & & s + K_0 & \Psi \\ & & & & & -\frac{1}{L} & s \end{vmatrix} \quad (3.46)$$

$$= (s^2 + K_0 s + K_0 K_1 (1 + M))^{(N-1)}$$

Table 3.2. Routh-table of equation (3.20).

s^2	1	$K_0 K_1 (1 + M)$
s^1	K_0	0
s^0	$-\frac{\begin{vmatrix} 1 & K_0 K_1 (1 + M) \\ K_0 & 0 \end{vmatrix}}{K_0} = K_0 K_1 (1 + M)$	0

By reapplying the *Routh-Hurwitz* stability criterion on differential-mode subsystem, the stability constraints can be deduced as $K_0 > 0$ and $K_0 K_1 (1 + M) > 0$. Further simplification of condition $K_0 K_1 (1 + M) > 0$ yields (3.21).

$$\begin{aligned} K_0 K_1 (1 + M) &> 0 \\ \Rightarrow 1 + M &> 0 \\ \Rightarrow M &> -1 \end{aligned} \quad (3.47)$$

Hence, for the differential-mode subsystem, the switching frequency dependent gain K_0 must be greater than zero and the current-sharing controller gain M must be greater than -1 in order to ensure that the current-sharing of N -paralleled power modules is stable. This stability result (3.21) will be illustrated by simulation using various gains of current-sharing controller M in the following subsections.

Furthermore, by equating (3.20) with a general second order system's characteristic equation of $s^2 + 2\zeta\omega_n s + \omega_n^2 = 0$, the transient response for the differential-mode subsystem can be obtained using (3.22), where ω_n = undamped natural frequency and ζ = damping ratio. Hence, with proper selection of damping ratio in (3.22), the dynamics of the current sharing loop can be determined, i.e. underdamped, critically damped or overdamped response.

$$\begin{aligned} s^2 + K_0 s + K_0 K_1 (1 + M) &= s^2 + 2\zeta\omega_n s + \omega_n^2 \\ \omega_n &= \sqrt{K_0 K_1 (1 + M)} \\ \zeta &= \frac{1}{2} \sqrt{\frac{K_0}{K_1 (1 + M)}} \end{aligned} \quad (3.48)$$

3.2.2.1 CURRENT-SHARING CONTROLLER $M = -1$

If $M = -1$, the characteristic equation for differential-mode properties has the poles at $s_1 = 0$ and $s_2 = -K_0$, as deduced in (3.23). The pole at $s = 0$ denotes that the system is marginally stable, where the states of a transient neither decay, nor increase from its initial value. On the contrary, the second pole has a negative real root at $s = -K_0$ that will cause the system to decay exponentially at the rate of $e^{-K_0 t}$ (asymptotically stable). Note that K_0 represents the switching frequency in this model.

$$\begin{aligned}
s^2 + K_0 s + K_0 K_1 (1 + M) &= 0 \\
\text{if } M &= -1 \\
s^2 + K_0 s &= 0 \\
s_1 &= 0 \text{ and } s_2 = -K_0
\end{aligned} \tag{3.49}$$

3.2.2.2 CURRENT-SHARING CONTROLLER $M = 0$

The case $M = 0$ represents a paralleled system without current-sharing controller and thus, the current-sharing loops do not exist in Figure 3.1. In this case, (3.20) simply becomes a second order system with the characteristic equation of $s^2 + K_0 s + K_0 K_1$, which has a total

of $(N-1)$ poles at $s_{1,2} = \frac{-K_0 \pm \sqrt{K_0^2 - 4K_0 K_1}}{2}$, damping ratio of $\zeta = \frac{1}{2} \sqrt{\frac{K_0}{K_1}}$ and its natural

frequency at $\omega_n = \sqrt{K_0 K_1}$.

3.2.3 SIMULATION RESULTS WITH DIFFERENT CURRENT-SHARING CONTROLLER GAIN VALUES

The simulation results in this section are produced to verify the analysis shown in preceding sections. Three paralleled DC-DC power modules are simulated using different current-sharing control M gain values as described in Section 3.2.2. Those gains are $M = 0$ (without current-sharing controller), $M = -1$ (marginally stable system) and $M < -1$ (unstable system). The parameters used for these power modules are listed in Section 2.4.1 except for the inductance for each converter as shown in Table 3.3. The paralleling structure for this simulation is based on Figure 3.1, where $N = 3$ in this case.

Table 3.3. Line inductance for individual converter.

DC-DC converter	Inductance (L)	External Disturbance ($\delta\epsilon$)
<i>First converter</i>	<i>1.9 mH</i>	<i>0.01</i>
<i>Second converter</i>	<i>2.1 mH</i>	<i>0.0001</i>
<i>Third converter</i>	<i>2.5 mH</i>	<i>0.001</i>

3.2.3.1 CURRENT-SHARING CONTROLLER $M = 0$

Based on the simulation parameters, the system poles for the common-mode and differential-mode subsystems are shown in (3.24). The simulation results for output voltage, individual currents and total current are shown in Figures 3.2 – 3.4 respectively.

Figure 3.3 demonstrates that individual converters are not able to share the current evenly without the current-sharing controller M . As analyzed previously, the damping ratio in

this case is $\zeta = \frac{1}{2}\sqrt{\frac{K_0}{K_1}} = 1.12$, which denotes an impulse response for $\zeta > 1$. The

undamped natural frequency for differential-mode is $\omega_n = \sqrt{K_0 K_1} = 11.18 \times 10^3 \text{ rad s}^{-1}$.

Common-mode poles:

$$\begin{aligned}
 s^3 + K_0 s^2 + K_0 K_1 s + K_0 K_1 K_2 &= 0 \\
 s_1 &= -1.8790 \times 10^4 \\
 s_2 &= -0.1954 \times 10^4 \\
 s_3 &= -0.4256 \times 10^4
 \end{aligned} \tag{3.50}$$

Differential-mode poles:

$$\begin{aligned}
 s^2 + K_0 s + K_0 K_1 &= 0 \\
 s_{4,5} &= -0.6910 \times 10^4 \\
 s_{6,7} &= -1.8090 \times 10^4
 \end{aligned}$$

Figure 3.2. Output voltage of three paralleled DC-DC converters when $M = 0$.

Figure 3.3. Individual currents of three paralleled DC-DC converters when $M = 0$.

Solid line: Converter #1, Semi-dotted-line: Converter #2, Dotted line: Converter #3.

Figure 3.4. Total current of three paralleled DC-DC converters when $M = 0$.

3.2.3.2 CURRENT-SHARING CONTROLLER $M = -I$

The system poles in this case are shown in (3.25). As mentioned in Section 3.2.1, M should not affect any common-mode property. Note that the common-mode poles remain unchanged when M varies, as illustrated in both equations of (3.24) and (3.25). The transient responses are shown in Figures 3.5 – 3.7 for output voltage, individual converter currents and total current correspondingly.

Common-mode poles:

$$s^3 + K_0 s^2 + K_0 K_1 s + K_0 K_1 K_2 = 0$$

$$s_1 = -1.8790 \times 10^4$$

$$s_2 = -0.1954 \times 10^4$$

$$s_3 = -0.4256 \times 10^4 \quad (3.51)$$

Differential-mode poles:

$$s^2 + K_0 s = 0$$

$$s_{4,5} = 0$$

$$s_{6,7} = -2.5 \times 10^4$$

Figure 3.5. Output voltage of three paralleled DC-DC converters when $M = -1$.

Figure 3.6. Individual currents of three paralleled DC-DC converters when $M = -1$.

Solid line: Converter #1, Semi-dotted-line: Converter #2, Dotted line: Converter #3.

Figure 3.7. Total current of three paralleled DC-DC converters when $M = -1$.

Like previous gain when $M = 0$, the individual converters are not able to share the current evenly when $M = -1$ because half of the poles for differential-mode subsystem are located at the origin (0,0) of the s -plane. Hence, the errors in current sharing neither converge nor diverge in this case.

3.2.3.3 CURRENT-SHARING CONTROLLER $M < -1$

In this example, $M = -1.01$ is chosen to illustrate the characteristic of an unstable differential-mode subsystem. The system poles are deduced as (3.26). Likewise, the common-mode poles remain unchanged when M varies. The simulated transient response for output voltage, individual currents and total current are shown in Figures 3.8 – 3.10 respectively. The instability in differential-mode subsystem results in the gradual divergence of individual currents from each other as demonstrated in Figure 3.9, but the total output current remains essentially constant as illustrated in Figures 3.10.

Common-mode poles:

$$\begin{aligned}
 s^3 + K_0 s^2 + K_0 K_1 s + K_0 K_1 K_2 &= 0 \\
 s_1 &= -1.8790 \times 10^4 \\
 s_2 &= -0.1954 \times 10^4 \\
 s_3 &= -0.4256 \times 10^4
 \end{aligned} \tag{3.52}$$

Differential-mode poles:

$$\begin{aligned}
 s^2 + K_0 s + K_0 K_1 (1 + M) &= 0 \\
 s_{4,5} &= 50 \\
 s_{6,7} &= -2.505 \times 10^4
 \end{aligned}$$

Figure 3.8. Output voltage of three paralleled DC-DC converters when $M < -1$.

Figure 3.9. Individual currents of three paralleled DC-DC converters when $M < -1$.

Solid line: Converter #1, Semi-dotted-line: Converter #2, Dotted line: Converter #3.

Figure 3.10. Total current of three paralleled DC-DC converters when $M < -I$.

This simulation results attests the analysis results obtained, where the differential-mode subsystem are dependent on the current-sharing loops and is decoupled from the common-mode subsystem. Likewise, any changed in differential-mode properties does not affect the poles of the common-mode subsystem. Nevertheless, when $M < -I$, the complete paralleled system is unstable due to the divergence of individual currents. The analysis presented here shows that $M = -I$ is the point of stability transition for the differential-mode subsystem. Under normal operation, M is chosen positive and high in magnitude to reduce current errors (2.26) and $M = -I$ is never encountered. It will however be seen in Section 4.4.1 that $M = -I$ will be adopted for fault compensation purpose for a short duration and the marginally stable property shown here confirms that its application for a short duration will not lead to sudden divergence of the error currents.

Another matter of concern is that the analysis here shows that M is not limited in terms of magnitude if it remains positive from the stability perspective. This is true with the present model because the differential-mode subsystem in the present model comprises $N-1$ identical second order systems (3.20). In the event that any additional lag is present in the current sharing loops, the system order will increase and instability will result if an excessively high value for M is employed. This can be demonstrated using the state variable approach presented in this chapter but it will not be dealt with. A transfer function approach to analyse this phenomena is presented in [15,16].

The effect of differential-mode instability will not be realized immediately at the output of the paralleled power modules as the total current and output voltage remains constant. In general, the aftermath of this differential-mode instability can be disastrous if the paralleled system does not include a protection scheme against this phenomenon.

3.3 SMALL SIGNAL STABILITY ANALYSIS FOR DROOP METHOD

The small signal stability of three single-phase inverter connected to a common load is analyzed this section. Figure 3.11 shows the equivalent circuit of a three UPS inverter connected in parallel to a common resistive load, where $\vec{E}_i = E_i \angle \delta_i$ and $\vec{V} = V \angle 0$.

Figure 3.11. Equivalent circuit of three paralleled inverter supplying a common load.

Based on Figure 3.11, the active and reactive powers for each inverters at steady state can be deduced as (3.27) and (3.28), where $X = \omega L$, $\omega = 2\pi f$ and δ is the phase angle between the output voltage of the inverter and the voltage of the common load. E and V are the amplitude of the output voltage of the inverter and the load voltage respectively.

$$P = \frac{EV}{X} \sin \delta \quad (3.53)$$

$$Q = \frac{EV \cos \delta - V^2}{X} \quad (3.54)$$

Both (3.27) and (3.28) demonstrate that the active power P is predominately dependent on the power angle δ , while the reactive power Q mostly depends on the output voltage amplitude. Thus, the conventional droop method used the above relations to introduce the following droop characteristics defined by (3.29) and (3.30).

$$\omega = \omega^* - m P_{avg} \quad (3.55)$$

$$E = E^* - n Q_{avg} \quad (3.56)$$

where m = frequency droop coefficient and n = voltage droop coefficient.

The inverter output frequency ω is controlled by (3.29), whereas inverter output voltage E is controlled by (3.30), as illustrated in Figure 3.3. In order to employ (3.29) and (3.30) as control laws in droop scheme, it is necessary to obtain the average output power of each inverter over one line-cycle. This can be implemented by using a low-pass filter (LPF) with a smaller bandwidth than that of the voltage loop of the inverter. The active and reactive output power obtained using LPF are equated in (3.31) and (3.32), where ω_f is the cutoff frequency of the LPF.

$$P_{avg} = \frac{\omega_f}{s + \omega_f} P_{inst} \quad (3.57)$$

$$Q_{avg} = \frac{\omega_f}{s + \omega_f} Q_{inst} \quad (3.58)$$

Substitute (3.29) - (3.30) into (3.31) - (3.32), the droop characteristic for each inverter can be computed as (3.33) and (3.34).

$$\omega = \omega^* - m \frac{\omega_f}{s + \omega_f} P_{inst} \quad (3.59)$$

$$E = E^* - n \frac{\omega_f}{s + \omega_f} Q_{inst} \quad (3.60)$$

Figure 3.12. Static droop characteristics of (a) frequency and (b) voltage droop.

Furthermore, the individual current of each inverter can be further obtained as (3.35), with the assumption that all three inverters are identical.

$$\begin{bmatrix} \bar{I}_1 \\ \bar{I}_2 \\ \bar{I}_3 \end{bmatrix} = \begin{bmatrix} \frac{2R_{Load} + j\omega_1 L}{-L^2 \omega_1^2 + j3R_{Load} L \omega_1} & \frac{-R_{Load}}{-L^2 \omega_2^2 + j3R_{Load} L \omega_2} & \frac{-R_{Load}}{-L^2 \omega_3^2 + j3R_{Load} L \omega_3} \\ \frac{-R_{Load}}{-L^2 \omega_1^2 + j3R_{Load} L \omega_1} & \frac{2R_{Load} + j\omega_2 L}{-L^2 \omega_2^2 + j3R_{Load} L \omega_2} & \frac{-R_{Load}}{-L^2 \omega_3^2 + j3R_{Load} L \omega_3} \\ \frac{-R_{Load}}{-L^2 \omega_1^2 + j3R_{Load} L \omega_1} & \frac{-R_{Load}}{-L^2 \omega_2^2 + j3R_{Load} L \omega_2} & \frac{2R_{Load} + j\omega_3 L}{-L^2 \omega_3^2 + j3R_{Load} L \omega_3} \end{bmatrix} \begin{bmatrix} \bar{E}_1 \\ \bar{E}_2 \\ \bar{E}_3 \end{bmatrix} \quad (3.61)$$

It is assumed that at steady-state, $\omega_1 = \omega_2 = \omega_3 = \omega$, and hence (3.35) can be simplified to (3.36).

$$\begin{bmatrix} \bar{I}_1 \\ \bar{I}_2 \\ \bar{I}_3 \end{bmatrix} = \begin{bmatrix} G_d + jB_d & G + jB & G + jB \\ G + jB & G_d + jB_d & G + jB \\ G + jB & G + jB & G_d + jB_d \end{bmatrix} \begin{bmatrix} \bar{E}_1 \\ \bar{E}_2 \\ \bar{E}_3 \end{bmatrix} \quad (3.62)$$

where

$$\begin{aligned} G_d &= \frac{R_{Load} L \omega}{L^3 \omega^3 + 9R_{Load}^2 L \omega} \\ B_d &= -\frac{6R_{Load}^2 + L^2 \omega^2}{L^3 \omega^3 + 9R_{Load}^2 L \omega} \\ G &= \frac{R_{Load} L \omega}{L^3 \omega^3 + 9R_{Load}^2 L \omega} \\ B &= \frac{3R_{Load}^2}{L^3 \omega^3 + 9R_{Load}^2 L \omega} \end{aligned}$$

The apparent power contributed by each inverter is (3.37) - (3.39).

$$\begin{aligned} \bar{S}_1 &= \bar{E}_1 \bar{I}_1^* \\ &= (G_d - jB_d) \bar{E}_1 \bar{E}_1^* + (G - jB) \bar{E}_1 \bar{E}_2^* + (G - jB) \bar{E}_1 \bar{E}_3^* \end{aligned} \quad (3.63)$$

$$\begin{aligned}\bar{S}_2 &= \bar{E}_2 \bar{I}_2^* \\ &= (G - jB) \bar{E}_2 \bar{E}_1^* + (G_d - jB_d) \bar{E}_2 \bar{E}_2^* + (G - jB) \bar{E}_2 \bar{E}_3^*\end{aligned}\quad (3.64)$$

$$\begin{aligned}\bar{S}_3 &= \bar{E}_3 \bar{I}_3^* \\ &= (G - jB) \bar{E}_3 \bar{E}_1^* + (G - jB) \bar{E}_3 \bar{E}_2^* + (G_d - jB_d) \bar{E}_3 \bar{E}_3^*\end{aligned}\quad (3.65)$$

The term $\bar{E}_\alpha \bar{E}_\beta^*$ (where $\alpha = 1, 2, 3$ and $\beta = 1, 2, 3$) can be further represented as (3.40), with the assumption that $\Delta\delta$ is small such that $\cos\Delta\delta \approx 1$ and $\sin\Delta\delta \approx \Delta\delta$. The symbol Δ denotes the small deviation of the respective variable from the equilibrium point. The voltage amplitude at steady-state is represented by E .

$$\bar{E}_\alpha \bar{E}_\beta^* = (E + \Delta E_\alpha)(E + \Delta E_\beta)(1 + j\Delta\delta_{\alpha\beta}) \quad (3.66)$$

where $\Delta\delta_{\alpha\beta} = \delta_\alpha - \delta_\beta$; $\alpha = 1, 2, 3$ and $\beta = 1, 2, 3$

Substituting (3.40) into (3.37) - (3.39), the active and reactive power for each inverter are (3.41) - (3.46), with the assumption that the product of $\Delta\delta\Delta E \approx 0$ and $\Delta E_\alpha\Delta E_\beta \approx 0$.

$$P_1 = G_d(E^2 + 2E\Delta E_1) + 2GE^2 + GE(2\Delta E_1 + \Delta E_2 + \Delta E_3) + BE^2(\Delta\delta_{12} + \Delta\delta_{13}) \quad (3.67)$$

$$Q_1 = -B_d(E^2 + 2E\Delta E_1) - 2BE^2 - BE(2\Delta E_1 + \Delta E_2 + \Delta E_3) + GE^2(\Delta\delta_{12} + \Delta\delta_{13}) \quad (3.68)$$

$$P_2 = G_d(E^2 + 2E\Delta E_2) + 2GE^2 + GE(\Delta E_1 + 2\Delta E_2 + \Delta E_3) + BE^2(\Delta\delta_{21} + \Delta\delta_{23}) \quad (3.69)$$

$$Q_2 = -B_d(E^2 + 2E\Delta E_2) - 2BE^2 - BE(\Delta E_1 + 2\Delta E_2 + \Delta E_3) + GE^2(\Delta\delta_{21} + \Delta\delta_{23}) \quad (3.70)$$

$$P_3 = G_d(E^2 + 2E\Delta E_3) + 2GE^2 + GE(\Delta E_1 + \Delta E_2 + 2\Delta E_3) + BE^2(\Delta\delta_{31} + \Delta\delta_{32}) \quad (3.71)$$

$$Q_3 = -B_d \left(E^2 + 2E\Delta E_3 \right) - 2BE^2 - BE \left(\Delta E_1 + \Delta E_2 + 2\Delta E_3 \right) + GE^2 \left(\Delta \delta_{31} + \Delta \delta_{32} \right) \quad (3.72)$$

Based on the droop characteristic of (3.33) - (3.34) and Figure 3.12, all the three inverters will eventually settle down to a new steady-state value of ω and E . Hence, assuming that the new steady-state reference is $\bar{E}_1$, the small deviation of ω_2 and ω_3 from ω_1 can be written as (3.47) and (3.48) respectively, whereas (3.49) and (3.50) represent the small deviation of ΔE_2 and ΔE_3 from ΔE_1 .

$$\Delta \omega_{12} = -m \frac{\omega_f}{s + \omega_f} \Delta P_{12} \quad (3.73)$$

$$\Delta \omega_{13} = -m \frac{\omega_f}{s + \omega_f} \Delta P_{13} \quad (3.74)$$

$$\Delta E_{12} = -n \frac{\omega_f}{s + \omega_f} \Delta Q_{12} \quad (3.75)$$

$$\Delta E_{13} = -n \frac{\omega_f}{s + \omega_f} \Delta Q_{13} \quad (3.76)$$

where

$$\Delta \omega_{\alpha\beta} = \omega_\alpha - \omega_\beta$$

$$\Delta P_{\alpha\beta} = P_\alpha - P_\beta$$

$$\Delta E_{\alpha\beta} = E_\alpha - E_\beta$$

$$\Delta Q_{\alpha\beta} = Q_\alpha - Q_\beta$$

Since $\Delta \omega = s\Delta \delta$, (3.47) and (3.48) can be further written as (3.51) and (3.52), with the substitution of ΔP from (3.41), (3.43) and (3.45).

$$-\left(\frac{s^2 + \omega_f s}{m\omega_f} + 3BE^2\right)\Delta\delta_{12} = (2G_d + G)E\Delta E_{12} \quad (3.77)$$

$$-\left(\frac{s^2 + \omega_f s}{m\omega_f} + 3BE^2\right)\Delta\delta_{13} = (2G_d + G)E\Delta E_{13} \quad (3.78)$$

Using (3.41) - (3.46) and (3.49) - (3.50), the above equations can be further represented as (3.53) and (3.54).

$$(s^3 + as^2 + bs + c)\Delta\delta_{12} = 0 \quad (3.79)$$

$$(s^3 + as^2 + bs + c)\Delta\delta_{13} = 0 \quad (3.80)$$

where

$$\begin{aligned} a &= \omega_f (2 - nE(2B_d + B)) \\ b &= \omega_f (3mE^2B + \omega_f - nE\omega_f(2B_d + B)) \\ c &= 3mE^2\omega_f^2 (B - nEG(2G_d + G) - nEB(2B_d + B)) \end{aligned}$$

Both (3.53) and (3.54) describes the free motion of the system for small disturbances around equilibrium point. Thus, the system response can be analyzed through the characteristic equation of (3.55).

$$\lambda^3 + a\lambda^2 + b\lambda + c = 0 \quad (3.81)$$

3.3.1 SIMULATION RESULTS

Simulation results for three single-phase inverters connected in parallel as shown in Figure 3.11 are presented to validate (3.55). Two examples with different frequency and voltage droop coefficients are presented in this simulation study.

3.3.1.1 CONDITION I: DROOP COEFFICIENT OF 0.0005

The system parameters are shown in Table 3.4. The initial active and reactive output powers are zero and the droop coefficients for both frequency and voltage droop are 0.0005. Since all inverters are identical, only system response of Inverter #2 is shown. The poles of the characteristic equation (3.55) based on given values are shown in (3.56).

Table 3.4. System parameters for single inverter.

Item	Symbol	Value	Unit
Line impedance	L	0.015	H
Filter cut-off frequency	ω_f	$2\pi 5$	rad/s
Frequency droop coefficient	m	0.0005	$(rad/s)/W$
Voltage droop coefficient	n	0.0005	V/Var
Nominal frequency	ω^*	$2\pi 50$	rad/s
Nominal voltage amplitude	E^*	152	V
Nominal apparent power	S	1000	VA
Load	R	12	Ω

$$\begin{aligned}
 \lambda_1 &= -31.92 \\
 \lambda_2 &= -28.79 \\
 \lambda_3 &= -2.63
 \end{aligned}
 \tag{3.82}$$

Based on (3.56), the system has all three negative real poles that denote a stable damped response of the system. The active and reactive powers are shown in Figures 3.13 and 3.14 respectively, where both demonstrate a damped response. The oscillations at 100Hz for both figures are not completely filtered by the LPF of the power measurements.

Figure 3.13. Transient response of active power under condition I.

Figure 3.14. Transient response of reactive power under condition I.

3.3.1.2 CONDITION II: DROOP COEFFICIENTS OF 0.005

The poles shown in (3.57) are obtained by using the same parameters as shown in Table 3.4, but with an increase of droop coefficients by ten times for both voltage and frequency droop.

$$\begin{aligned}\lambda_1 &= -36.5 \\ \lambda_2 &= -15.74 + j22.56 \\ \lambda_3 &= -15.74 - j22.56\end{aligned}\tag{3.83}$$

From (3.57), it indicate that the system also has a stable system but with an underdamped response. Figures 3.15 and 3.16 depict the underdamped response of active and reactive powers under condition II.

Figure 3.15. Transient response of active power under condition II.

Figure 3.16. Transient response of reactive power under condition II.

3.4 CONCLUSION

The stability analysis of commonly employed paralleling methods for power modules are presented in this chapter. Those methods are the democratic and master-slave topologies that are under the category of centralized control scheme and the droop method of decentralized control scheme.

The general framework for N -paralleled power modules under a centralized control scheme with and without a current-sharing controller is presented. The analysis demonstrates that the system stability of paralleled power modules with current-sharing controller can be examined by analyzing two different subsystems, i.e. the common-mode and differential-mode subsystems. The differential-mode subsystem's stability involves the current-sharing loops. Its instability can result in diverging individual currents among the modules while the total output current remains unaffected. On the contrary, the common-mode subsystem is independent of the current-sharing loop gain. The analysis also illustrates that in order to ensure stable operation of paralleled modules for a centralized control scheme, the parameter constraints of $K_0 > K_2$, $K_0 > 0$ and $M > -1$ should be met under all conditions.

The small signal stability analysis for droop method is also presented in the preceding sections. The analysis in (3.53) and (3.54) further illustrates that the transient response of the droop method is dependent upon the droop coefficient (m and n) and filter cut-off frequency (ω). In addition, the transient response of droop method is very slow compare to the centralized control scheme.

In general, it can be concluded that with a centralized control scheme, as long as care is taken on the choice of the current sharing feedback gain to ensure stability, better current sharing performance can be achieved compared to a decentralized control scheme based on the droop method. Better performance is achieved in both areas of current sharing precision (in terms of magnitude) and response.

Present centralized control scheme however suffer from the need of communication cables linked to the individual controllers from the central controller which the droop method based decentralized control scheme does not require. This leads to examine the possibility of having a scheme that retains the control performance of the centralized control scheme while maintaining the simplified physical structure of the decentralized control scheme. In addition, it is also desire to have a decentralized structure which has a means of rapid information exchange between modules without relying on the relatively slow droop mechanism. This matter will be discussed in Chapter 5 where a novel communication strategy between modules is proposed.

In the subsequent chapter, another important stability aspect of paralleled converters will be discussed, which is the performance of the system in the event of module failure.

Chapter 4 TRANSIENT ANALYSIS AND FAULT COMPENSATION DURING MODULE FAILURE IN PARALLELED POWER MODULES

4.1 INTRODUCTION

One of the main design issues over the past decade in the paralleling of power modules is the control of the current sharing among the constituent modules. This has led to the stability analysis of paralleled power modules [15,17,45-48,50] and many controller design techniques [18,19,24-28,51]. Another important area which is the fault transient analysis in the paralleled system has been neglected and is yet being explored.

Paralleling operation is commonly employed in a system because of advantages such as increased power processing capability, improved reliability, enhanced availability with $N + 1$ modules and such, as described in Chapter 1. However, when one of the paralleled modules fails to function, the system performance could be shaped by the behavior of the faulty module before it is being excluded from the system. Thus, the understanding of the system's transient during fault is critical to ensure its reliability and availability being sustained in all conditions. This chapter presents a fault transient analysis using the principle of superposition where a pictorial way of analyzing the fault is adopted.

Furthermore, in the event of a fault, the time interval between the fault detection and the isolation of the faulty module from the system could range from 1 to 100

milliseconds depending on fuse type. Within this interval, the system is vulnerable to internal and external sources of disturbance that could jeopardize its overall performance. Therefore, the system's robustness could be further improved by identifying the disturbance signals and mitigating their effects during this interval. This chapter also presents a compensation methodology to achieve this.

The outline of this chapter is as follows: In Section 4.2, the system modeling and stability analysis of healthy paralleled buck converters with the presence of a faulty module is presented using state variable approach. Section 4.3 is devoted to the identification of sources of disturbance in such a paralleled system and how the disturbance effects can be segregated by superposition. The fault compensation strategies in the paralleled system are discussed in Section 4.4. The overall improvement in the system performance is verified in Section 4.5 via simulation and experimental results. Section 4.6 gives a practical discussion on how the proposed fault compensation works for a Proportional Integrator (PI) compensator. A concluding discussion is given in Section 4.7.

4.2 SEPARATION OF FAULTY MODULE IN SYSTEM MODELING

In this section, a model of paralleled buck configuration with active current sharing is established using state variable representation for the purpose of separating the faulty module from the paralleled system. Section 4.2.1 illustrates the system modeling of paralleled power modules and section 4.2.2 demonstrates the equivalent system representation during fault. Section 4.2.3 analyzes the stability of the system with fault.

4.2.1 SYSTEM MODELING OF PARALLELED POWER MODULES

Figure 4.1 shows a simplified block diagram of N -paralleled converters of buck configuration incorporating current sharing controller, with only the first, j -th and n -th modules shown. The common coupling point for each module is at point P . The resistive parts for both inductor and capacitor are assumed to be very small and they are neglected in this analysis, i.e. $R_{int}=0$. Each module is capable of measuring its own inductor current i_j . These signals are summed to obtain the total current I_{total} , which is then multiplied by $\frac{1}{N}$ to generate a common reference current i_{ref} . This reference i_{ref} can be of any value depending on the type of current sharing scheme, such as democratic scheme [15,19,26] and master-slave current sharing scheme [15,17,19]. In this study, a democratic current sharing scheme is adopted.

The equivalent state variable representation of the paralleled system is reproduced as shown in Figure 4.2, with only the first, j -th and n -th modules shown. $G_{o_j}(s)$ represents the j -th controlled current source as shown in Figure 4.2(b), without showing R_{int} in the diagram ($R_{int}=0$). Each parallel path is fed by three feedback loops, viz. the inner current feedback loop, the voltage feedback loop and the current-sharing loop. The purpose of having multiple feedback loop control strategy [52] is to ensure that the system has good performance for both steady states as well as transient response.

Figure 4.1. Block diagram of N -paralleled buck configuration converters with current sharing controller supplying a common load.

(a)

(b)

Figure 4.2. State variable representation of system (a) with N -paralleled modules and (b) controlled current source $G_{oj}(s)$.

The system gain controllers for current loop, voltage loop and current sharing loop are K_1 , K_2 and M respectively. The design and selection of these controller gains are described in Chapter 2 and 3. The error between i_{ref} and individual module inductor current i_j is fed back to each $G_{oj}(s)$ with gain M , as deduced in (4.1). The current sharing error is reduced for higher values of M allowing near perfect current sharing, as analyzed in Section 2.4.1.2. However, the increase of gain M will magnify any fault current. This will be elaborated in Section 4.4.1.

$$\varepsilon_j = i_{ref} - i_j = \frac{I_{total}}{N} - i_j = \frac{1}{M} i'_j \quad (4.1)$$

4.2.2 EQUIVALENT SYSTEM REPRESENTATION

To facilitate analysis of system dynamics in the faulty period, any state i'_j arising from the current sharing loop in Figure 4.2 is firstly rewritten by segregating a current (4.2) indexed k . This current i_k is later used to represent the uncontrollable current of the faulty module (i.e. $i_k = I_{fault}$).

$$\begin{aligned} i'_j &= M\varepsilon_j = M \left(\frac{\sum_{j=1}^n i_j}{N} - i_j \right) \\ &= M \left(\left(\frac{\sum_{j \neq k}^{n-1} i_j}{N-1} - i_j \right) + \frac{i_k}{N-1} + \left(\frac{1}{N} - \frac{1}{N-1} \right) \sum_{j=1}^n i_j \right) \\ &= M \left(\varepsilon'_j + \frac{I_{fault}}{N-1} + \left(\frac{1}{N} - \frac{1}{N-1} \right) I_{total} \right) \end{aligned} \quad (4.2)$$

Based on (4.2), the system with the faulty module can be reconstructed as shown in Figure 4.3, where $Go_k(s)$ is excluded from the system as it is uncontrollable and can be viewed as an external source of disturbance injected into the system. This representation of Figure 4.3 is equivalent to the original N modules system and presents explicitly an $N-1$ module system embedded in the former. With a faulty k -th module, Figure 4.3 shows that the system behaves as an $N-1$ module system with disturbances. The effects of various disturbances in Figure 4.3 can now be studied by segregating them using the principle of superposition. This will be discussed in Section 4.3. For ease of visualization, the remaining diagrams will combine the current sharing loop and the controlled current source $Go_j(s)$ as $Ho_j(s)$.

Figure 4.3. Equivalent N system representation with $N-I$ healthy modules and a faulty module as external disturbance injection of I_{fault} .

4.2.3 SYSTEM STABILITY ANALYSIS WITH FAULT

Prior to analyzing the stability of the system with fault, it is beneficial to study the dynamics of the system under normal democratic sharing as shown in Figure 4.2a.

Consider first the dashed block system in Figure 4.2a. The state variables of concern are the individual module currents $\{i_1, \dots, i_N\}$. Using (4.1), an equivalent representation with states comprising the $N-1$ current errors and total current $\{\varepsilon_1, \dots, \varepsilon_{N-1}, I_{total}\}$ can be used.

From Figure 4.2a, the democratic current sharing scheme is (4.3).

$$i_j = G_o(s) \cdot [M \cdot \varepsilon_j + \frac{I_{total}^*}{N}] \quad (4.3)$$

The sum of (4.3) for all modules gives (4.4).

$$\begin{aligned} \sum i_j &= G_o(s) \cdot M \cdot \sum \varepsilon_j + G_o(s) \cdot \sum \frac{I_{total}^*}{N} \\ \Rightarrow I_{total} &= G_o(s) \cdot I_{total}^* \end{aligned} \quad (4.4)$$

since $\sum \varepsilon_j = 0$.

Equation (4.4) reveals that the input-output properties of the system in the dashed block of Figure 4.2(a), and in particular the dynamics of the state I_{total} , are neither dependant on the current errors ε_j nor on the feedback gain M . The total current I_{total} is only dependent on the common transfer function $G_o(s)$ and I_{total}^* . This is the common-mode subsystem property discussed in Section 3.2.1.

Having obtained the dynamics of I_{total} , it remains to examine that of ε_j . By introducing the expression of ε_j (4.1) in place of i_j , (4.3) can be written as (4.5).

$$\frac{I_{total}}{N} - \varepsilon_j = G_o(s) \cdot [M \cdot \varepsilon_j + \frac{I_{total}^*}{N}] \quad (4.5)$$

Further reintroducing the numerator and denominator polynomials of

$$G_o(s) = \frac{N_o(s)}{D_o(s)}, (4.5) \text{ is rewritten as (4.6).}$$

$$[D_o(s) + M.N_o(s)]\varepsilon_j = \frac{1}{N} \cdot [D_o(s).I_{total} - N_o(s).I_{total}^*] \quad (4.6)$$

It has been shown from (4.4) that $[D_o(s).I_{total} - N_o(s).I_{total}^*]$ is null. The differential equation that governs the dynamics of ε_j is thus reduced to (4.7).

$$\begin{aligned} [D_o(s) + M.N_o(s)]\varepsilon_j &= 0 \\ [1 + M.G_o(s)]\varepsilon_j &= 0 \end{aligned} \quad (4.7)$$

The poles of (4.7) satisfy the equation $D_o(s) + M.N_o(s) = 0$. The number of poles corresponds to the degree of the polynomial $D_o(s)$. Equivalently, the poles representing the system dynamics of (4.7) are those of the transfer function $\frac{1}{1 + M.G_o(s)}$. Thus, (4.7) reveals that the dynamics of the individual ε_j are all decoupled from each other and also I_{total} . Hence, the stability of the complete system of Figure 4.2(a), as represented through a study of the dynamics of $\{\varepsilon_1, \dots, \varepsilon_{N-1}, I_{total}\}$, is equivalent to the stability of $\frac{1}{1 + M.G_o(s)}$ (for ε_j) and the closed loop stability of $G_o(s)$ under feedback of $\frac{K_2}{C} \cdot \frac{1}{s}$ (for I_{total}).

Based on the above analysis, the system in the dashed block in Figure 4.3 under fault condition is exactly an $N-1$ module system under a democratic current sharing scheme. It is thus not only stable from an input-output perspective with a transfer function

of $G_o(s)$, the new state errors $\mathcal{E}'_j$ will also decay in a manner that is determined by the poles

of $\frac{1}{1+M.G_o(s)}$.

By re-introducing $I_{total} = I_{fault} + \sum_{j \neq fault}^{N-1} i_j$, with I_{fault} as an uncontrolled disturbance,

the stability of the system under fault in Figure 4.3 is identical to that in Figure 4.4 where

the additional feedback loop is due to $\sum_{j \neq fault} i_j$ component of I_{total} (i.e. only $N-1$ currents)

with no inputs to the system.

Figure 4.4. System with identical poles to that of closed loop system under fault.

The term $G_o(s)$ in Figure 4.4 is equivalent to the system in dashed block of Figure 4.3 according to (4.4) and the internal system with unobservable states $\mathcal{E}'_j$ has been proven

stable by (4.7). The feedback system in Figure 4.4 can now be viewed as one having an

open loop gain $G_o(s)$ and a negative feedback gain of $\frac{(N-1)}{N} \cdot \frac{K_2}{C} \cdot \frac{1}{s} + \left(\frac{M}{N}\right)$. The feedback

gain prior to fault occurrence is $\frac{K_2}{C} \cdot \frac{1}{s}$. Therefore, the system at fault is one with a

reduced feedback gain of factor $\frac{(N-1)}{N}$ and an additional proportional feedback gain of

$\frac{M}{N}$. Its stability is generally maintained unless exceptionally high M is used. In

particular, the system parameters in Table 4.1 maintain a stable system under fault. Thus, one can be assured that during fault, the errors introduced are basically due to input ‘disturbances’ and will not be excessively amplified by system instability.

4.3 SEGREGATION OF $N-1$ SYSTEM USING SUPERPOSITION PRINCIPLE

Figure 4.3 can be further divided into three individual subsystems using the principle of superposition, as shown in Figures 4.5 - 4.7. Subsystem I, as illustrated in Figure 4.5, consists of all the external signals injected into a system of zero initial states during the fault period. These signals are the fault current (I_{fault}) with entry points at P and Q , and the total current (I_{total}) with entry point at R .

Figure 4.5. Subsystem I with external signals and zero initial states

Figure 4.6. Subsystem II with internal state signals

Figure 4.7. Subsystem III or system of $N-1$ modules at steady state

Subsystem II is a naturally decaying system that comprises only internal state signals, as shown in Figure 4.6. These states have for initial values the difference in inductor currents and capacitor voltage between a healthy N module system and a healthy $N-1$ module system at the starting instant of a fault.

The final Subsystem III is the new $N-1$ system with input reference as external excitation, as shown in Figure 4.7. This system is one in steady state and the objective of compensation would be to eliminate the effects of the previous two subsystems on the output voltage as well as to make this last steady state system identical to the one prior the fault's occurrence. Adopting this approach would effectively allow smooth ride-through of output voltage throughout the fault.

The sum of the above-mentioned subsystems in Figures 4.5 - 4.7 is an equivalent representation of that in Figure 4.3. To exemplify the ease of using the principle of superposition in fault transient analysis, the system in Figure 4.3 is simulated with three paralleled modules ($N = 3$), where individually shared the load current of 1A equally before fault occurred, with the component parameter listed in Table 4.1.

At $t = 2ms$, a fault of uncontrolled current occurred in one of the modules, where the faulty module is simulated in Figure 4.3, with a unit step change of the faulty current (I_{fault}) that injects into the paralleled system from points P and Q . This caused the output voltage (V_o) to increase by about 20%, as shown in Figure 4.8. This sudden increase of voltage can be computed by superposition principle using the cumulative contribution from the previously mentioned subsystems, where $V_o = V_{o_Sub\ I} + V_{o_Sub\ II} + V_{o_Sub\ III}$. This failure case will be used for all simulations and experiments that follow.

The objective of this analysis and simulation is to identify and then reduce the signals of $V_{o_Sub\ I}$, $V_{o_Sub\ II}$ during fault, which comes from Subsystems I and II respectively, to as near zero as possible, and also to make $V_{o_Sub\ III}$ output identical to that of the healthy system before the fault occurred. The following section described how to reduce those signals with respective proposed compensations for each subsystem.

Figure 4.8. Simulated system output overvoltage (V_o) waveform of Figure 4.3 when fault occurred at $t=2ms$, where I_{fault} is simulated as a unit step input.

4.4 FAULT COMPENSATION IN PARALLELED SYSTEM

Since Subsystem III in Figure 4.7 represents the final steady state, the transients generated during a fault would only be contributed by Subsystems I and II in Figures 4.5 and 4.6 respectively. For purpose of identifying the individual contribution of each subsystem to a fault, the respective output voltages for Subsystems I (solid lines) and II (solid-dotted lines) are shown in Figure 4.9, with their arithmetic sum as well in dotted lines for the fault case mentioned. In this case, Figure 4.9 clearly shows that Subsystem I (the external signals) contributes more to the disturbance as compared with Subsystem II (the decaying of initial states).

Figure 4.9. Output voltages for Subsystem I (Solid line), Subsystem II (Solid-dotted line) and Summation (Dotted line) when fault occurs.

These waveforms in Figure 4.9 are obtained by simulating the fault on those Subsystems I and II as shown in Figures 4.5 and 4.6 respectively. At $t=2ms$, the fault occurred and Subsystem I in Figure 4.5 is simulated with I_{fault} of a unit step input. This fault has caused the output voltage of Subsystem I ($V_{o_Sub\ I}$) changed from 0V to about 1.6V, as shown in Figure 4.9. In addition, the Subsystem II as shown in Figure 4.6, is simulated with initial values of inductor currents and capacitor voltage at the starting instant of a fault. The output voltage of Subsystem II ($V_{o_Sub\ II}$) due to this fault is as shown in Figure 4.9.

After identifying them, the disturbances from each subsystem can be dealt with individually. It is assumed in this analysis that the system is able to detect the fault immediately and inject necessary compensation signals before the fault is cleared. The

fault compensation for each source of disturbance will be discussed in the following subsections.

4.4.1 IMPROVEMENT IN SUBSYSTEM I (EXTERNAL)

As mentioned in Section 4.3, Figure 4.5 consists of external signals injected into the paralleled system, viz. the fault current (I_{fault}) and the total current (I_{total}). I_{fault} has the injection point at P and Q , whereas I_{total} injects its signal at point R . The cancellation of I_{total} in Figure 4.5 can be achieved by feedforward injection of an equivalent signal at point R , as highlighted with dotted lines in Figure 4.10. This requires measurement of I_{total} which is readily available in the original system and does not require information of the faulty current. With this compensation, the remaining signal that demands attention is I_{fault} .

Figure 4.10. Fault compensation in dotted box for Subsystem I.

Although I_{fault} has two entry points into the system, both injected signals at different points are not the same. This is because I_{fault} that enters at point Q into the system is multiplied by the current sharing controller gain M . If gain M is made large for

better current sharing (for example, $M = 10$), the disturbance injected here would be ten times of I_{fault} . Therefore, a tradeoff between current sharing performance and improved fault ride-through is inevitable.

One way to reduce the effects of I_{fault} in the system is by allowing the entry signals at points P and Q cancel each other in terms of their voltage contribution at the output. This can be achieved promptly for the system in Figure 4.5 by utilizing its structure. By inspection from Figure 4.5, the way I_{fault} enters the system at point Q can be seen as a natural feedforward cancellation for its entry at point P when controller gain M is changed to -1 . This change is made momentarily for all gains M in the system and will be restored back to its original value once the fault is cleared (i.e. $I_{fault} = 0$). When M is changed to -1 , the modified disturbance contribution of I_{fault} is reduced to (4.8) at point P where $G_o(s)$ is the gain in $H_o(s)$ for input i_j^* .

$$I_{fault_reduced \text{ (at P)}} = (1 - G_o(s)) I_{fault} \quad (4.8)$$

The output of compensated Subsystem I ($V_{o_Sub \text{ I, Compensated}}$) in Figure 4.11 is obtained by simulating Figure 4.10 with the respective compensations as denoted by dotted lines in Figure 4.10, when the fault occurred at $t=2ms$. These compensations were activated and injected into the system, as shown in Figure 4.10, at that instant when the fault occurred until the fault is cleared. The waveform indicated as $V_{o_Sub \text{ I, Uncompensated}}$ in Figure 4.11 is reproduced from Figure 4.9 of $V_{o_Sub \text{ I}}$, which is obtained by simulating Figure 4.5, for comparison purpose. Therefore, by compensating for I_{total} and I_{fault} in Subsystem I, the improvement can be seen in the reduced capacitor voltage disturbance at the output in Figure 4.11. The next stage will be focused on the improvement in Subsystem II.

Figure 4.11. Reduced output overvoltage contribution by Subsystem I under fault.

Compensated case (Solid line). Uncompensated case (Dotted line).

4.4.2 IMPROVEMENT IN SUBSYSTEM II (INTERNAL)

As mentioned in Section 4.3, Subsystem II comprises of all the internal state signals. The Subsystem II can be further separated into a system comprising the currents states only for one and the voltage state only for another as shown in Figures 4.12 and 4.13 respectively. These are named Subsystems IIA and IIB.

Figure 4.12. Subsystem IIA – Initial states with inductor current differences.

Figure 4.13. Subsystem IIB – Initial states with capacitor voltage difference.

Subsystem IIA consists of non-zero initial values for inductor currents and a zero initial value for the capacitor voltage, and vice versa for Subsystem IIB. The state signal in Subsystem IIA, i.e. the initial values of inductor currents, is obtained by taking the difference between the inductor current at the start of the fault and the corresponding current for the steady state Subsystem III in Figure 4.7 at that instant. Likewise, the initial capacitor voltage in Subsystem IIB can also be obtained by taking the difference between the output voltage at the start of the fault and the corresponding voltage for the steady state Subsystem III at the same instant.

4.4.2.1 IMPROVEMENT IN SUBSYSTEM IIA (INITIAL INDUCTOR CURRENTS)

In order to remove the effects of the decaying internal current states, it would be theoretically necessary to inject at the point marked $\boxed{I}$ in Figure 4.14 a Dirac signal of opposite sign scaled by the inductance and the magnitude of the original state for it to be cancelled at the output of that integrator. However, in practice, a short pulse of unity area could be used in place of a Dirac. This can be practically generated and represented as the output of a low pass filter (LPF) excited by a Dirac as shown near point $\boxed{I}$ in Figure 4.14.

Figure 4.14. Injection point for improvement in Subsystem IIA during fault.

This system, nevertheless, has a preferred common point of injection at point R as shown in Figure 4.14. Hence, the injected signal's input is transferred from point $[I]$ to point $[3]$ as marked in Figure 4.14. While transferring the injected signal to point R , additional compensation would be required to take into account the PWM lag, controller gain K_I as well as gain $\frac{1}{N}$ in the system.

Figure 4.14 was simulated with respective compensations that are activated and injected into the system at that instant when the fault occurred until the fault is cleared. The resultant waveform from these compensations are shown in Figure 4.15 which is marked as $V_{o_SubIIA, Compensated}$ (Solid line). In addition, the output voltage of Subsystem IIA without compensation, as shown in Figure 4.12, was simulated and presented as $V_{o_SubIIA, Uncompensated}$ (Dotted line) in Figure 4.15 for comparison purpose. This simulation result validates the compensation methodology. However, it can be seen that the original contribution of these decaying current states to the output capacitor voltage is negligible compared to that of other sources. It would thus not be required in practice for this case.

Figure 4.15. Output voltage disturbance reduction in Subsystem IIA with compensation.

Uncompensated case (Dotted line) and Compensated case (Solid line).

4.4.2.2 IMPROVEMENT IN SUBSYSTEM IIB (INITIAL CAPACITOR VOLTAGE)

As mentioned in Section 4.4.2, the initial capacitor voltage in Subsystem IIB is obtained by taking the difference between the output voltage (V_o) at the start of the fault and the corresponding voltage for the steady state Subsystem III (V_{steady}) at this instant. At the start of the fault, the capacitor voltage of the faulty N -module system is identical to that of the healthy N -module system (V_o) since it cannot change instantaneously. Thus, one way to mitigate the effect of the disturbance in Subsystem IIB is to make the output capacitor voltage of Subsystem III (an $N-1$ module system) identical to that of the N module system. This is done by modifying controller gain K_2 to a new value of (4.9) to compensate the effect of $\frac{(N-1)}{N}$, as shown in Figure 4.16 with the dotted box.

$$K_{2_{new}} = K_2 \left(\frac{N}{N-1} \right) \quad (4.9)$$

Figure 4.16. Modification in Subsystem IIB to compensate error due to fault.

The overall output voltage improvement in Subsystem IIB is illustrated in Figure 4.17. The dotted line in Figure 4.17 is the uncompensated output voltage contribution and the solid line shows the much reduced output voltage contribution with compensation (4.9) by Subsystem IIB.

Figure 4.17. Output overvoltage contribution by Subsystem IIB. Original uncompensated case with unchanged K_2 gain (Dotted line) and improved compensated case with new K_2 gain (Solid line).

4.5 SIMULATION AND EXPERIMENTAL RESULTS

A paralleled power supply of three DC-DC buck converters is used to verify the fault compensation strategies discussed here. The experiment setup is illustrated in Figure 4.1 where there are only three modules and the power stage comprises the Buck Converter's switches. The control scheme for each module is as shown in Figure 4.2. The buck converter is designed to produce an output of 5Vdc and 1A rated current. The input voltage is 12Vdc. Table 4.1 provides the hardware and controller parameters. Each module is armed with a crowbar protection [43] and a switch is used to emulate the faulty module (shorted MOSFET switch) as shown in Figure 4.18. This setup is for concept testing. In order to have better fault current magnitude control, other circuit configurations

can be used. As an example, a well designed capacitor can be put in series with the crowbar.

Table 4.1. Experiment and simulation Parameters

Parameter	Value	Description
L	1mH	Filter Inductor
C	470 μ F	Filter Capacitor (Aluminium Electrolytic)
K_o	25krads ⁻¹	PWM model gain in Figure 4.2 (Lag)
F	25kHz	PWM Switching frequency
$K_1=K_1'L$	$K_1'/2\pi = 10\text{kHz}$	$K_1' =$ Current loop bandwidth
$K_2=K_2'C$	$K_2'/2\pi = 2.5\text{kHz}$	$K_2' =$ Voltage loop bandwidth
M	5	Current sharing loop gain
$Load$	5 Ω	Output resistive load

Figure 4.18. Circuit for fault simulation (MOSFET short-circuit) with crowbar.

This experiment is conducted by closing the switch in Figure 4.18. The situation is thus identical to a shorted MOSFET. A predetermined error current threshold is used to detect the fault. When this is exceeded, the thyristor crowbar is turned on. This drains the input and output capacitors temporarily till the fuses blow. The main focus of this experimental is to investigate the effectiveness of the compensation methods proposed to allow smooth ride-through in terms of output voltage throughout the fault period.

From previous analysis, the main contribution to output voltage disturbance is from Subsystem I, as shown by the signal magnitude in Figure 4.9. The mitigation of this disturbance should thus be given highest priority. Subsystem IIA contributes least to the disturbance as shown in Figure 4.15. Its compensation method also requires the generation of special Dirac related signal which complicates the compensation circuit in practice. It is thus not implemented here from a practical viewpoint. Thus, only the compensation of Subsystems I and IIB is implemented in this experiment.

The dotted lines of the simulation results in Figures 4.19a and 4.19b are the uncompensated output load voltage and total current respectively, which corresponds to the experimental results in Figure 4.20. The total current (Channel 1) in Figure 4.20 differs from that of simulation in Figure 4.19b at the beginning of the fault. This is due to current sensor signal saturation in the experiment. The solid lines in Figures 4.19a and 4.19b are the compensated output load voltage and total current respectively during fault.

The corresponding experimental results are shown in Figure 4.21 and agree with the simulated results. Figure 4.21 shows that the output load voltage has achieved smooth ride-through during fault and validates the effectiveness of the proposed compensation schemes.

Figure 4.19. Overall improvement in (a) output load voltage and (b) total current with implementation of compensation in Subsystems I and IIB. Uncompensated signal (Dotted line) and Compensated signal (Solid line).

Figure 4.20. Uncompensated system output when MOSFET is shorted. Channel 1: Total current (1A/div) and Channel 2: Output load voltage (2V/div).

Figure 4.21. Compensated system output with compensation in Subsystems I and IIB activated. Channel 1: Total current (1A/div) and Channel 2: Output load voltage (2V/div).

4.6 DISCUSSION ON PROPOSED SCHEME FOR PROPORTIONAL-INTEGRAL CONTROLLER

In order to demonstrate the generality of the proposed technique for feedback controllers apart from a proportional feedback, a discussion is presented here on the application of the proposed scheme for the case where $K_2(s)$ in Figure 4.2 is a Proportional-Integral (PI) controller and individual voltage references are adopted. The PI controller has been chosen due to its wide usage for steady state error compensation under different load conditions; and the case of individual voltage sources is considered since the latter is commonly employed to avoid single point failure. This section will also indicate how integral windup in the PI controller is dealt with by the scheme.

Figure 4.22 illustrates the PI controller with individual references, where $\langle V_{ref} \rangle$ denotes the averaged reference voltage among all modules and $\Delta V_{ref,j}$ represents its deviation in individual modules. With the present of an integrator in $K_2(s)$ in Figure 4.22(a), the DC error $\varepsilon_{v,j}$ has to be null at steady state for a stable system. Since each individual source can be different being $\langle V_{ref} \rangle + \Delta V_{ref,j}$ for the j -th module; while the output signal feedback being V_o is common to all; the individual $\Delta V_{ref,j}$ for each module needs to be compensated for (or cancelled) to ensure $\varepsilon_{v,j}$ be null for all modules at steady state. Thus, a modified entry point for the proportional current sharing scheme M' is necessary in this case, as shown in Figure 4.22(a). This ensures that the error $\varepsilon_{v,j}$ for all modules be zero at steady state under different voltage references as each $\Delta V_{ref,j}$ will be compensated for by $M'\varepsilon_j$. Based on Figure 4.22a, $\varepsilon_{v,j}$ can be computed as (4.10). Hence, the signals at steady state for N healthy identical modules in Figure 4.22(a) can be deduced

as (4.11). Figure 4.22(a) can be furthered view as Figure 4.22(b) with modified current

sharing gain $M = M' . K_2(s) \left(\frac{1}{N} \right)$ for the purpose to analyze the dynamics of $\mathcal{E}_j$.

Figure 4.22. Paralleled converters, showing j -th module, with individual PI controller of $K_2(s)$ and individual V_{ref} . (a) Modified current sharing scheme M' for PI controller; and (b)

Equivalent representation of (a) with $M = M' . K_2(s) \left(\frac{1}{N} \right)$.

$$\mathcal{E}_{V,j} = \langle V_{ref} \rangle + \Delta V_{ref,j} - V_o + M' . \mathcal{E}_j \quad (4.10)$$

$$\begin{aligned} \langle V_{ref} \rangle &= V_o \\ \Delta V_{ref,j} &= -M' . \mathcal{E}_j \end{aligned} \quad (4.11)$$

$$I_{Load} = K_2(s) . \mathcal{E}_{V,j} \quad (\text{at steady state, } G_{Oj}(s) = 1)$$

Upon fault detection, the proposed compensation is shown in Figure 4.23 (dotted lines and blocks), where the current sharing gain is changed to $M = -1$, the feedforward injection of I_{total} with gain $\frac{M}{N-1}$ and the insertion of a gain $\frac{N}{N-1}$ after $K_2(s)$.

Figure 4.23. Proposed compensation scheme (dotted-lines and blocks) upon detection of fault.

Under this scheme, the remaining $N-1$ currents are deduced as (4.12) where i_h represents currents of healthy modules. The total current in Figure 4.23 is computed as (4.13) where the faulty module's current is the uncontrolled fault current.

$$i_j = G_o(s) \cdot [M \cdot \epsilon'_j + M \cdot \frac{I_{fault}}{N-1} + \frac{1}{N-1} \cdot K_2(s) \cdot \epsilon_{V,j}] \quad (4.12)$$

$$\text{where } \epsilon'_j = \left[\frac{1}{N-1} \sum_{h=1}^{N-1} i_h \right] - i_j$$

$$I_{total} = [G_o(s) \cdot M + 1] \cdot I_{fault} + G_o(s) \cdot [K_2(s) \cdot \epsilon_{V,j}] \quad (4.13)$$

Upon fault occurrence, without implementing the recommended compensation, the erroneous signal continues to be transmitted via $M' \cdot \epsilon_j$ to the PI controller in Figure 4.22a giving rise to windup. By early fault detection and immediate implementation of the

compensation scheme, error accumulation in $K_2(s)$ will be checked as the feedback signal $M.\varepsilon_j$ is diverted and bypasses $K_2(s)$ as shown in Figure 4.23. Subsequent error accumulation are only due to reference errors $\Delta V_{ref,j}$ which are small.

With $M = -1$, $[G_o(s).M.\frac{I_{fault}}{N-1}]$ in (4.12) shows that the individual modules are actively controlled to share the fault current disturbance. Similarly, assuming that the PI output $K_2(s).\varepsilon_{v,j}$ has not deviated significantly from the load current as in (4.11), the contribution $G_o(s).\frac{1}{N-1}.K_2(s).\varepsilon_{v,j}$ in (4.12) indicates that load current is equally distributed by the controls to individual modules. This presents the best scheme in terms of current sharing. In practice, one has to ensure that the modules are capable of delivering this load due to I_{fault} and a reduction in functional modules. The additional load in the fault transient can be minimized by limiting the magnitude of I_{fault} with proper choice of filtering inductor and fuses.

Once the fault is cleared, the current sharing scheme reverts to that in Figure 4.24.

The compensations comprising the new gain $\frac{N}{N-1}$ after $K_2(s)$ and feedforward of I_{total} remains. Accumulated errors in each module's $K_2(s)$ will decay according to system dynamics as in Subsystem II in Figure 4.6. Democratic current sharing among modules will also be actively implemented with dynamics (4.14) based on (4.7).

$$[1 + M'.K_2(s).\frac{1}{N-1}.G_o(s)]\varepsilon_j' = 0 \quad (4.14)$$

Figure 4.24. New structure with compensations after fault has cleared.

4.7 CONCLUSION

The fault transient analysis for module failure in an N module converter is presented and compensation methods are recommended in this chapter. The principle of superposition is employed to separate the original system to subsystems, which contribute individually to the total disturbance. This facilitates identification of the major contributors of disturbance and their required compensation methods.

The recommended compensation method involves primarily a modified current sharing feedback gain of $M = -1$ prior to isolation of the faulty module, the addition of a feedforward injection of I_{total} and the insertion of a gain $\frac{N}{N-1}$ after the existing feedback controller $K_2(s)$. No additional current sensing is required for individual modules and in particular, direct measurement of I_{fault} is not required. It can thus be adapted with only compensator modifications on existing paralleled modules under democratic current sharing designs.

The analysis results and compensation methods are verified via simulation and experiments for the case of three paralleled buck converters with a shorted switch and

smooth ride-through of output voltage is achieved. The methodology is applicable for paralleled step-down converters in continuous conduction mode.

The analysis though presented with proportional feedback compensators can be adopted in general for frequency dependant compensators as shown in the discussion for the PI compensator. The analysis also assumes the general case of the presence of an uncontrolled current from one of the modules and adapts well to other fault scenarios (open or short circuit). In conclusion, this chapter has provided an analysis of the paralleled system's behaviour when one of its modules fails. It has shown that in the fault duration, the system remains stable and that by adopting the compensation methods proposed, smooth ride-through can be achieved at the output of the converter.

Chapter 5 A NOVEL COMMUNICATION STRATEGY FOR DECENTRALIZED CONTROL OF PARALLELED MULTI-INVERTER SYSTEMS

5.1 INTRODUCTION

The need for highly reliable power supplies has increased in recent years with the proliferation of critical loads (such as computers, medical equipment, satellite systems, telecommunications and others electronic dependent equipment), which are intensely in demand in the present society. Notwithstanding, the role of uninterruptible power supply (UPS) has also increased tremendously in sustaining high reliable power to those critical loads. One of the ways to achieve higher reliability is by paralleling two or more units of UPS. This is because the paralleled system has wide advantages over single unit UPS, as exclusively exemplified in Chapter 1.

As discussed in Chapter 2, the control of paralleled inverters can be categorized into two main schemes, i.e. centralized and decentralized control. The advantages and disadvantages of both schemes are also clearly outlined in Section 2.3. Based on the arguments presented for both centralized and decentralized control, a decentralized control with high modularity and reliability, fast transient response, good voltage regulation and without the inherent drawbacks of the droop method is deemed most desirable and ideal for paralleling UPS. Therefore, this chapter proposes such a scheme by allowing information sharing between inverters without the need for a centralized controller.

Information such as number of modules paralleled, synchronization signal, detection of healthy or faulty modules and others can be shared among the inverters by this scheme.

The main feature of this proposed strategy is that it utilizes the common-mode current, which is inherent in a PWM rectifier-inverter system [53], as signal carrier to all paralleled multi-inverters and this is detailed in Section 5.2. The common-mode current controller of each inverter, as described in Section 5.2.2, generates this signal carrier. The communication behaviour in the paralleled system is dependent upon the individual common-mode controller parameters, and each inverter can be made to behave as an information source to the other inverters or as a passive-receiving branch.

In order to apprehend this communication strategy, voltage command synchronization of paralleled multi-inverters will be demonstrated using this method. Such synchronization is important and necessary in a paralleled system in order to ensure that all output voltages are synchronized in frequency, phase and amplitude [7,32-34,36-39,41]. This avoids large circulating currents flowing among the inverters that will otherwise decrease system capability by forcing the components to operate beyond their rated current value. The commonly used synchronization method for droop control is through a phase-locked-loop (PLL) circuit [34,39,41], whereas the centralized control utilizes the central reference synchronization block [36]. This chapter will focus on proposing a synchronization strategy with common-mode current limitation for paralleled multi-inverters, which will be described in Section 5.3. The inverters are assumed identical and load sharing, though achievable is not discussed in this chapter and will be discussed in Chapter 6.

5.2 SYSTEM CONFIGURATION OF DECENTRALIZED CONTROL

Figure 5.1 depicts the power supply system with parallel-connected single-phase inverter modules and a load connected on the ac bus. The proposed communication strategy can be implemented in either the common DC source configuration [Figure 5.1(a)] or the individual DC source [Figure 5.1(b)] configuration. In the case of the individual DC source configuration, a connection between the midpoints of the DC-link capacitors, as shown in Figure 5.1(b), is required to allow flow of the carrier signal in the system.

Figure 5.1. Paralleled multi-inverters supplying common load from (a) common DC source and (b) individual DC sources.

Each inverter consists of a common-mode choke (L_{com}) and a filter inductor (L_{diff}), which are used to filter the switching component of both the common-mode current (i_{com}) and the differential-mode current (i_{diff}). A single-phase inverter with mutual inductances is shown in Figure 5.2 for an inverter in the common DC-link configuration. The parameters r_+ and r_- in Figure 5.2 represent the line resistance of the inverter. l_+ and l_- represents the leakage inductances of L_{com} and L_{diff} .

Figure 5.2. Power stage of the k -th single-phase inverter with shared common load.

The induced voltages for both common-mode choke and filter inductor in Figure 5.2 are (5.1) and (5.2) respectively.

$$e_1 = L_{com} \frac{d(i_+ + i_-)}{dt} \quad (5.1)$$

$$e_2 = L_{diff} \frac{d(i_+ - i_-)}{dt} \quad (5.2)$$

The common-mode and differential-mode voltages and currents in Figure 5.2 are defined as (5.3) - (5.6).

$$V_{com} = \frac{V_{a+} + V_{a-}}{2} \quad (5.3)$$

$$V_{diff} = \frac{V_{a+} - V_{a-}}{2} \quad (5.4)$$

$$i_{com} = \frac{i_+ + i_-}{2} \quad (5.5)$$

$$i_{diff} = \frac{i_+ - i_-}{2} \quad (5.6)$$

By analyzing the circuit in Figure 5.2, V_{a+} (5.7) and V_{a-} (5.8) can be deduced.

$$V_{a+} = r_+ i_+ + l_+ \frac{di_+}{dt} + e_1 + e_2 + V_{C+} \quad (5.7)$$

$$V_{a-} = r_- i_- + l_- \frac{di_-}{dt} + e_1 - e_2 + V_{C-} \quad (5.8)$$

Using (5.1) - (5.8), V_{com} and V_{diff} can be further written as (5.9) and (5.10).

$$V_{com} = \left(\frac{r_+ + r_-}{2} \right) i_{com} + \left(\frac{r_+ - r_-}{2} \right) i_{diff} + \left(\frac{l_+ + l_-}{2} + 2L_{com} \right) \frac{di_{com}}{dt} + \left(\frac{l_+ - l_-}{2} \right) \frac{di_{diff}}{dt} + V_{Load,com} \quad (5.9)$$

$$V_{diff} = \left(\frac{r_+ - r_-}{2} \right) i_{com} + \left(\frac{r_+ + r_-}{2} \right) i_{diff} + \left(\frac{l_+ - l_-}{2} \right) \frac{di_{com}}{dt} + \left(\frac{l_+ + l_-}{2} + 2L_{diff} \right) \frac{di_{diff}}{dt} + V_{Load} \quad (5.10)$$

where

$$V_{Load,com} = \frac{V_{C+} + V_{C-}}{2} \quad (5.11)$$

$$V_{Load} = \frac{V_{C+} - V_{C-}}{2} \quad (5.12)$$

Since r_+ and r_- as well as l_+ and l_- are small, they are assumed to be negligible in this analysis. Hence, as a first approximation, (5.9) and (5.10) can be further simplified to (5.13) and (5.14).

$$V_{com} = 2L_{com} \frac{di_{com}}{dt} + V_{Load,com} \quad (5.13)$$

$$V_{diff} = 2L_{diff} \frac{di_{diff}}{dt} + V_{Load} \quad (5.14)$$

From (5.14), one sees that the design of the differential-mode controller is independent of common-mode variables. Based on (5.13), if the variable $V_{Load,com}$ is decoupled from the differential-mode system, then the design of the common-mode controller can be dealt with independently as well. Derivation of $V_{Load,com}$ requires the combination of the common-mode equation (5.13) for all inverters and this decoupling aspect will be demonstrated in Section 5.2.2.

5.2.1 DESIGN OF DIFFERENTIAL-MODE CONTROLLER FOR SINGLE PHASE INVERTER

The linear model of inverter (5.14) with multi-loop feedback control of differential-mode can be represented as shown in Figure 5.3(a), where $L'_{diff} = 2L_{diff}$. K_1 and K_2 are proportional gains of the inductor current feedback loop and voltage feedback loop respectively. The selections and limitations of these proportional gains are detailed in Chapter 2 and 3. This multiple-loop proportional feedback control strategy is sufficient to ensure good performance for both steady states as well as transient responses in the present application. Furthermore, the derivative of the filtered load voltage is used in this system to implement both the load current feedforward loop and inner inductor current feedback loop as deduced in (5.15). This is particularly useful since the capacitor voltage, unlike the total load current, can be locally measured for each decentralized controller of individual inverters in the system. Eventually, each single-phase inverter requires only one load voltage sensor in order to implement both control loops in the system, viz. the inner capacitor current feedback loop and the outer voltage feedback loop, as shown in Figure 5.3(b).

$$i_C = C \frac{dV_{load}}{dt} = i_L - i_{load} \quad (5.15)$$

(a)

(b)

Figure 5.3. (a) Linear model of inverter with multiloop feedback of differential-mode control, and (b) implementation of load current feedforward and inductor current feedback loops with derivative of load voltage.

5.2.2 DESIGN OF COMMON-MODE CONTROLLER

When single phase inverters are paralleled together as shown in Figure 5.1, there is possibility of having i_{com} circulating among the inverters [32,35]. Hence, a common-mode controller is included in each inverter to limit and control i_{com} in the paralleled system.

The common-mode structure based on (5.13) and its proportional controller with gain K_3 are illustrated in Figure 5.4, where $L'_{com} = 2L_{com}$.

Figure 5.4. Common-mode current controller.

Figure 5.4 can be represented by (5.16).

$$V_{Load,com} + L'_{com} \frac{di_{com}}{dt} = K_3 (i^*_{com} - i_{com}) \quad (5.16)$$

To provide a circuit representation, one can define $R_{com} = K_3$ and $V^*_{com} = i^*_{com} \cdot R_{com}$, and (5.16) can be rewritten as (5.17).

$$V^*_{com} = V_{Load,com} + L'_{com} \frac{di_{com}}{dt} + R_{com} i_{com} \quad (5.17)$$

Based on (5.17), the common-mode dynamics can be represented by an equivalent circuit shown in Figure 5.5. The voltage source V^*_{com} in Figure 5.5 generates desired signals into the circuit and it behaves as an information source to the other inverters.

Figure 5.5. Common-mode circuit for single inverter.

In this proposed scheme, the magnitude of i_{com}^* is kept below 5% of i_{diff_rated} (for example, $i_{diff_rated_peak} = 7\text{A}$ corresponds to $i_{com_peak} = 0.35\text{A}$), in order to avoid high circulating currents.

Since $V_{Load,com}$ is common to all paralleled multi-inverters based on Figure 5.2 and (5.11), the combined common-mode circuit comprising N paralleled inverters is shown in Figure 5.6, where Z_{com_k} is R_{com_k} and L'_{com_k} in series for $k=1, 2, \dots, N$.

Figure 5.6. Paralleled common-mode circuit representation.

The sum of common-mode currents in Figure 5.6 is $\sum_{k=1}^N i_{com_k} = i_{Load,com}$, where

$$i_{Load,com} = \frac{i_{Load+} + i_{Load-}}{2} \text{ (refer to Figure 5.2). This is the load common-mode current.}$$

Under normal operation, $i_{Load,com}$ is zero unless a leakage path is present at the load side (as

shown in Figure 5.2) for the common-mode current to flow. Thus, $\sum_{k=1}^N i_{com_k}$ is

effectively zero. In this case, Figure 5.6 will be reduced to Figure 5.7 which illustrates the paralleled common-mode circuit with $i_{Load,com} = 0$. Figure 5.7 reveals that $V_{Load,com}$ is dependent only on common-mode variables $V_{com_k}^*$ and Z_{com_k} . Therefore, the design of common-mode controller can be dealt independently from differential-mode variables.

Figure 5.7. Paralleled inverters' common-mode current controller circuit.

By assigning each individual voltage source $V_{com_k}^*$ in Figure 5.7 with a different k -th frequency carrier, the k -th inverter's common-mode current controller can act as an information source with the k -th carrier frequency as well as a passive receiver for information from another inverter with a different carrier frequency. In a similar manner, multiple frequencies can be generated by each source $V_{com_k}^*$ if more carrier frequencies are required for additional channels per source inverter. This mode of communication will be discussed in Section 5.3.1.

Taking now as example the case where inverter #1 acts as the only information source, the circuit is reduced to that in Figure 5.8. $V_{com_1}^*$ is the only active source and the remaining $N-1$ branches have $V_{com_k}^*=0$; thus behaving as a passive receiving branch.

Figure 5.8. Common-mode circuit with single source and $N-1$ passive receiving branches.

From Figure 5.8, the common-mode currents, (5.18) and (5.19), can be derived with the assumption that $Z_{com_1} = Z_{com_k} = Z_{com}$, where $k=1, 2, \dots, N$.

$$i_{com_1} = \frac{R_{com}}{Z_{com}} \left(1 - \frac{1}{N} \right) i_{com_1}^* \quad (5.18)$$

$$i_{com_k} = -\frac{R_{com}}{Z_{com}} \left(\frac{1}{N} \right) i_{com_1}^*, \text{ where } (k \neq 1) \quad (5.19)$$

Both (5.18) and (5.19) indicate that the amplitude of the individual common-mode currents is dependent on variables R_{com} and Z_{com} . If, for example, information such as number of modules N is obtained based on (5.18) and (5.19), the precise value of R_{com} and Z_{com} is required in order to obtain an accurate N . Therefore, by making $Z_{com} \approx R_{com}$, (5.18) and (5.19) can be further simplified to (5.20) and (5.21), which are independent from the impedances in the common-mode circuit. This can be realized by manipulating both parameters, R_{com} and L'_{com} , such that R_{com} is more dominant than L'_{com} .

$$i_{com_1} = \left(1 - \frac{1}{N} \right) i_{com_1}^* \quad (5.20)$$

$$i_{com_k} = -\frac{1}{N} i_{com_1}^*, \text{ where } (k \neq 1) \quad (5.21)$$

5.3 SYNCHRONIZATION STRATEGY FOR PARALLELED MULTI-INVERTERS

In this section, the proposed synchronization strategy will be illustrated in detail. The mode of communication among the paralleled multi-inverters is discussed in Section 5.3.1. Section 5.3.2 will describe the structure of the proposed synchronization strategy. Factors affecting the performance of this common-mode communication strategy are discussed in Section 5.3.3.

5.3.1 MODE OF COMMUNICATION

One of the modes to send the synchronization signal is through frequency modulation (FM). In FM the amplitude is kept constant and the frequency is modulated by the amplitude of the modulating signal. The FM signal of i_{com}^* can be represented as

$$i_{com}^* = A_c \cos(\omega_c + m)t \quad (5.22)$$

where

A_c = Amplitude of carrier signal

ω_c = Frequency of carrier signal

m = $A_m \cos \omega_m t$ (Modulating signal)

A_m = Maximum frequency deviation of the modulation scheme

ω_m = Frequency of the modulating signal, which is synchronization frequency (60Hz) in this case.

Another mode of communication that is feasible in the application will be amplitude modulation (AM). In AM, the amplitude of carrier signal at frequency ω_c is modulated as shown in (5.23).

$$i_{com}^* = A_c (1 + k \cos \omega_m t) \cos \omega_c t \quad (5.23)$$

where

A_c = Amplitude of carrier signal without modulation signal

ω_c = Frequency of carrier signal

k = Modulation index of A_m/A_c

A_m = Amplitude of modulation signal

ω_m = Frequency of the modulating signal, which is 60Hz in this case.

AM requires accurate signal amplitudes and is highly dependant of the parameters in the common-mode circuit in Figure 5.5. On the other hand, FM only requires that the individual modules signal frequencies to be near identical as the frequency varies. This requires the system to achieve its steady state quickly for each new frequency and is less parameter dependant. For purpose of source synchronization, the information signal to be shared is a sinusoidal signal at line frequency. This is relatively slow changing compared to the time-constants ($\cong L'_{com}/R_{com}$) of the complete common-mode circuit in Figure 5.7. FM is thus the preferred method and will be used here to demonstrate the synchronization strategy among paralleled multi-inverters.

5.3.2 STRUCTURE OF SYNCHRONIZATION STRATEGY

In order to achieve synchronization among parallel multi-inverters, one of the inverters will be sending the synchronized command signal through a frequency modulated i_{com}^* to all inverters and the remaining inverters will set their $i_{com}^*=0$ to act as a

receiving branch as depicted in Figure 5.8. All inverters, inclusive of sender, will retrieve the signal by measuring the individual i_{com} within their own module. Figure 5.9 illustrates the synchronization strategy in each inverter. The synchronous signal receiver's structure is further illustrated in Figure 5.10.

Figure 5.9. Structure of synchronization strategy in each inverter.

Figure 5.10. Synchronous signal receiver structure

The raw signal received i_{com} (5.5) consists of the carrier signal, synchronization signal and noise. The signal is firstly filtered by a band-pass-filter (BPF-1) with the carrier frequency as its center frequency and a bandwidth based on the magnitude of the modulation signal m . This filtered signal is subsequently tracked by a phase-locked loop (PLL), as shown in Figure 5.11, to extract the running frequency ($\omega_c + m$).

The signal obtained from the PLL-1 in Figure 5.10 will be filtered again by another band-pass filter (BPF-2) centered about the line-frequency of 60Hz to extract m . The synchronization signal is thus obtained at the output of PLL-2 and is used as the command voltage V_{ref}^* for respective inverters. The implementation approach will be discussed in the following section.

Figure 5.11. Block diagram of a phase-locked loop (PLL).

5.3.3 FACTORS AFFECTING PERFORMANCE OF COMMON-MODE COMMUNICATION STRATEGY

In this proposed common-mode communication strategy, there are parameter (i.e. software programmable) and hardware factors that determine the quality and speed of the transmitted signals via the common-mode path. The parameter factors are mainly in the choice of the PLLs and BPFs in Figure 5.10. The hardware factors are the PWM switching frequency, sampling and conversion time of analog-to-digital converter (ADC) or digital-to-analog converter (DAC), and the speed of the digital-signal-processor (DSP). The following subsections will elaborate on these factors.

5.3.3.1 PARAMETER FACTORS

In order to retrieve accurate transmitted signals, the choice of the PLL's loop filter in Figure 5.11 is crucial. An excessively high pass filter will not filter off sufficiently the noise primarily due to the PWM's switching and an excessively low pass filter will result in slower PLL tracking capability and correspondingly, a delay in the received modulated signal. In this chapter, the carrier signal is at 500 Hz and the modulated signal for synchronization is at the line frequency of 60 Hz. The major noise contributor is the PWM switching at 20 kHz. The *Loop Filter* gains of the PLLs are given in Section 5.4.3. They are chosen to minimize the lag involved in tracking the carrier and the modulating signal as well as to attenuate sufficiently the PWM's switching noise. PLL structures and gain selections are widely discussed in literature and papers [54,55] are given for reference. Appendix 3 records the structure and gain selection used in this chapter.

Another component that requires attention at the receiving end is the choice of the BPF in Figure 5.10. This is because the common-mode currents before filtering via the BPF carry both transmitted signal and noise. The noise can be filtered with appropriate selection of the BPF's type and bandwidth. The criterion of choice is identical to that of the PLL, i.e. the tradeoff between signal lag and noise transmission. The BPF's type and parameters are given in Section 5.4.3. Details on BPF choice can be found in literature and [56] are given as a reference. Nevertheless, the basic BPF used in this chapter is also recorded in Appendix 4.

5.3.3.2 HARDWARE FACTORS

The other limitations are mainly contributed by hardware factors such as PWM switching frequency, sampling and conversion time of ADC/DAC, as well as the DSP

speed. The PWM switching frequency limits the carrier frequency since the physical carrier signal is the common-mode current and the PWM frequency limits the common-mode current controller's bandwidth. Finally, ADC/DAC characteristics and DSP computation speed affect transmission and reception of the common-mode signals. The relatively low carrier frequency of 500 Hz in this case however does not impose a stringent requirement and most present day DSP hardware can meet the requirement. The DSP sampling frequency is given in Table 5.1.

Table 5.1. Parameter List

Component	Nominal Value	Description
L'_{diff}	6mH	Filter inductor
L'_{com}	1mH	Common-mode choke
C	18 μ F	Filter capacitor
f_{pwm}	20kHz	PWM switching frequency
$K_1=K'_1L'_{diff}$	$2\pi \times 1000 \times 6m$	Differential current loop bandwidth
$K_2=K'_2C$	$2\pi \times 250 \times 18\mu$	Voltage loop bandwidth
$K_3=K'_3L'_{com}$	$2\pi \times 5000 \times 1m$	Common-mode current loop bandwidth
$f_{sampling}$	10kHz	DSP sampling frequency
V_{dclink}	200V	Input DC voltage source

5.4 PROTOTYPE SYSTEM IMPLEMENTATION APPROACH

Three 110V_{rms}/550VA 60Hz single-phase inverters are constructed and connected as illustrated in Figure 5.1a. The hardware and controller parameters for each inverter are listed in Table 5.1. Three main aspects of implementation will be addressed in this section

are the experimental setup (Section 5.4.1), implementation of derivative $C \frac{dV}{dt}$ (Section 5.4.2) and the implementation of synchronization strategy (Section 5.4.3).

5.4.1 EXPERIMENTAL SETUP FOR SYNCHRONIZATION STRATEGY

Figure 5.12 illustrates the experimental setup of the proposed synchronization strategy. This prototype is implemented in the *Matlab-Simulink* and *dSPACE* environment. The differential-mode controller, common-mode controller and synchronous signal receiver structure as shown in Figures 5.9 - 5.11 are configured in the *Matlab-Simulink* environment and downloaded into the *dSPACE* for execution. All the voltage and current sensors are connected to the external interface of *DS1103PCC* controller board. There are two ‘*LTA50-P/SPI*’ current sensors and one ‘*LEM LV25-P*’ voltage sensor for each inverter. In the event that the DC link voltages of individual inverters is not common as in Figure 5.1(a) but only the mid-point of the DC link capacitors are connected as shown in Figure 5.1(b), a current sensor or small resistor can be placed at this mid-point of the DC link of each inverter prior the common mid-point connection for a cost effective solution to the measurement of the common-mode current.

The *DS1103 PCC* controller board is installed inside the computer. This controller board is interfaced with external hardware via connectors of 16-bit ADC and DAC. Each paralleled UPS consists of single PWM unit that will drive two legs of V_{a+} and V_{a-} (as shown in Figure 5.2) through two gate drivers.

Figure 5.12. Experimental setup for synchronization strategy.

5.4.2 IMPLEMENTATION THE FEEDBACK OF $C \frac{dV}{dt}$

As described in Section 5.2.1, the implementation of both the load current feedforward loop and inner inductor current feedback loop can be realized by utilizing the derivative of load voltage. However, direct derivative is not realizable and in actual practical implementation, derivation introduces high-frequency noise. Differentiation of high frequencies can lead to large unwanted signals or saturation of amplifiers and other components. Thus, in order to realize it, a first order low-pass-filter (LPF), which also attenuates high frequency noise, will be included in the derivative term. The resulting derivative term used to compute capacitor current is (5.24).

$$\frac{s}{1 + \tau s} = \frac{1}{\tau} \left(1 - \frac{1}{1 + \tau s} \right) \quad (5.24)$$

Therefore, the feedback of capacitor current is done by employing (5.24) to obtain an approximated derivative of the load voltage. The time constant $\tau = 10^{-4} s$ is applied with the nominal capacitor of $C = 18 \mu F$.

5.4.3 IMPLEMENTATION OF THE SYNCHRONIZATION STRATEGY

To achieve synchronization among paralleled multi-inverters, each inverter will sense its own i_{com} using a hall-effect current sensor and the synchronization signal is obtained as shown in Figure 5.10. The FM based on (5.22) is employed as the mode of communication among the paralleled multi-inverters with its parameters as shown in (5.25).

$$\begin{aligned} i_{com}^* &= 0.2 \cos(2\pi 500 + m)t \\ m &= 2\pi 20 \cos(2\pi 60)t \end{aligned} \quad (5.25)$$

The first inverter of the paralleled three inverters injects the source signal (5.25). All other inverters obtain their respective i_{com} and each inverter's controller will then extract the synchronization signal as illustrated in Figure 5.10.

Both BPF-1 and BPF-2 in Figure 5.10 are second order Butterworth band-pass filters. Based on (5.25), the center frequency of BPF-1 is set to 500Hz and the bandwidth is 40Hz. BPF-2 has its center frequency set to 60Hz and has a narrow bandwidth of 1Hz.

The loop filter of both phase-locked loops PLL-1 and PLL-2 in Figure 5.10 are proportional-integral (PI) filters. The proportional gain (K_{p_PLL}) and integral gain (K_{i_PLL}) of PLL-1 are 500 and 6.4×10^5 respectively. The PLL-2 gains are set at $K_{p_PLL}=10$ and $K_{i_PLL}=250$. ω_{ref} for PLL-1 and PLL-2 are $2\pi 500 \text{ rad/s}$ and $2\pi 60 \text{ rad/s}$ respectively.

5.5 EXPERIMENTAL RESULTS

The experiment results will show the synchronization signals obtained as well as its insensitivity to various load conditions for three paralleled inverters. The different types of load include linear resistive and inductive loads, a nonlinear load comprising a rectifier and the no load condition.

Figure 5.13 depicts the per-unit synchronization signals (V_{syn}) obtained by individual inverters for the resistive load. In Figure 5.14, the command voltage V_{ref}^* for each inverter's differential controller (Figure 5.9) is synchronized with their respective V_{syn} and both command and output voltages are shown. The delay in the output voltage with respect to command voltage in Figure 5.14 is due to the closed-loop bandwidth of the controller and can be resolved by applying a pre-compensator if required.

Figure 5.13. Individual per-unit V_{syn} (Channel #1:1-3: Inverter #1-3) obtained from i_{com} with resistive load. (1 p.u./div). Time: 10ms/div.

Figure 5.14. Individual output load voltages (Channel #1:1-3) and respective V_{syn} (Channel #2:1-3) (100V/div). Time: 10ms/div.

Figure 5.15. Individual filtered i_{com} (Channel #1:1-3: Inverter #1-3) at the output of BPF-1. (0.1A/div). Time: 1ms/div.

Figure 5.15 shows the magnitude of each i_{com} , where the i_{com} magnitude of information source (Inverter #1) is about 0.1333A and receiver branches (Inverters #2 - #3) are about -0.0667A. These i_{com} magnitudes correspond to (5.20) and (5.21). Figure

5.16 shows the output voltage and the load current. Both are not affected by signals sent in the common-mode path.

Figure 5.16. Output load voltage (Channel 1: 100V/div) and load current (Channel 2: 10A/div). Time: 10ms/div.

Figure 5.17 shows the differential-mode current and common-mode current of Inverter #2. The common-mode current in Figure 5.17(b) contains the carrier signal and a 60Hz line frequency component. This is linked to the weak coupling of differential-mode components to the common-mode circuits as indicated in (5.9). With proper decoupling of differential-mode components from the common-mode circuit, the compensated common-mode current containing only the carrier frequency is obtained as shown in Figure 5.18.

(a)

(b)

Figure 5.17. (a) Differential-mode current (2A/div) and (b) common-mode current (0.2A/div) of Inverter #2. Time: 10ms/div.

Figure 5.18. Compensated common-mode current (0.2A/div) of Inverter #2. Time: 10ms/div

Figure 5.19. Respective per-unit V_{syn} for inductive load (Channel #1:1-3 :1 p.u./div) (Time: 10ms/div).

Figure 5.20. Output load voltage (Channel 1: 100V/div) and load current (Channel 2: 2A/div) of an inductive load. Time: 10ms/div.

Figures 5.19 - 5.20 show results for an inductive load. The synchronization signals in respective inverters are shown in Figure 5.19. Figure 5.20 shows that the common-mode signals have no effect on the load voltage and current.

Figures 5.21 - 5.23 exhibit the feasibility of the proposed synchronization strategy when the inverters are supplying power to a nonlinear load. Figure 5.21 shows the individual synchronization signals obtained while supplying the nonlinear load. The load voltage and current in Figure 5.22 are again not affected by the synchronization strategy. Figure 5.23(a) shows the three differential-mode currents with good harmonic current sharing and Figure 5.23(b) shows the common-mode current of Inverter #1 for this case.

Figure 5.21. Per-unit V_{syn} of respective inverters with a nonlinear load (Channel #1:1-3: 1 p.u./div) (Time: 10ms/div).

Figure 5.22. Output load voltage (Channel 1: 100V/div) and load current (Channel 2: 10A/div) of a nonlinear load. Time: 10ms/div.

(a)

(b)

Figure 5.23. (a) Respective differential-mode currents (2A/div) and (b) common-mode current (0.2A/div) of Inverter #1. Time: 10ms/div

Eventually, the proposed synchronization strategy is validated under no load condition, as demonstrated in Figure 5.24.

Figure 5.24. Respective per-unit V_{syn} in no load condition (Channel #1-3: 1p.u./div)
(Time: 10ms/div).

5.6 CONCLUSION

A novel communication strategy that utilizes the common-mode current as signal carrier to achieve decentralized control of paralleled multi-inverters is introduced in this chapter. This is demonstrated for the communication of a synchronization signal that is used to synchronize the voltage command of individual inverters. The proposed strategy eliminates the need for a centralized controller for distribution of information to individual inverters. The method is not affected by load condition or load type.

Apart from voltage command synchronization, the proposed communication strategy can also be used to share other information, such as number of inverters connected and fault information. This information can be transmitted to the neighboring inverters either via FM or AM.

Three single-phase prototypes of $110V_{\text{rms}}/550\text{VA}$ 60Hz inverters are built to verify the proposed strategy. The performances of the prototype system under different load conditions have been measured and they validate the analysis shown previously.

In conclusion, this chapter has presented a novel communication strategy among individual converters without the need of a centralized controller and additional communication cables.

Chapter 6 IMPROVED AND TUNED DECENTRALIZED CONTROLLERS OF PARALLELED MULTI- INVERTERS FOR CURRENT SHARING AND STRATEGY FOR TRANSIENTLESS HOT PLUG-IN

6.1 INTRODUCTION

The most desired control scheme for paralleled multi-inverters is the decentralized control scheme without the inherent drawbacks of the conventional droop method. Some desirable features absent in a droop based decentralized control scheme are fast transient response, good voltage regulation; while its inherent strengths are its flex-modularity structure via ease of hotswapping and high reliability via redundancy. In order to incorporate all desired features into the decentralized control scheme, issues such as voltage command synchronization of individual modules, near-perfect equal load current sharing among the inverters, and stable and smooth transitions of the paralleled system need to be resolved. Unsynchronized voltage command not only causes current sharing problem, but it would also cause large circulating currents flowing among the inverters that will otherwise decrease system capability by forcing the components to operate beyond their rated current value.

This chapter focuses on some controller design improvements to resolve these issues in the proposed decentralized control scheme. These issues are near-perfect equal current sharing as discussed in Section 6.2 and to achieve transientless hotswapping of paralleled multi-inverters in Section 6.3, especially during plug-in process. The plug-out process can be easily achieved by disconnecting the specific module from the paralleled

system using switch without causing any severity phenomena during the transition. Eventually, Section 6.4 concludes by summarizing the results of the improved decentralized control scheme.

6.2 INVESTIGATION OF SOURCES TO UNEQUAL LOAD CURRENT SHARING

In order to investigate the sources to unequal load current sharing, the decentralized controller structure for the paralleled multi-inverters has to be clearly defined, as described in Section 6.2.1. Based on this structure, the investigation to the current sharing problem will be carried out in Section 6.2.2. Mitigation solutions for each source will be given in Section 6.2.3. Section 6.2.4 compiles the experimental results from the mitigation solutions.

6.2.1 STRUCTURE OF DECENTRALIZED CONTROLLER FOR PARALLELED MULTI-INVERTERS

Figure 6.1 depicts the block diagram of a power supply system with parallel-connected single-phase inverter modules sharing a common load. Each inverter has its individual voltage command (V_{ref}^*) and two control loops, viz. the inner current feedback loop and the outer voltage feedback loop. The model of a single inverter with this multi-loop feedback controller is shown in Figure 6.2. The selection of proportional controller gains $K_1=K'_1L$ and $K_2=K'_2C$ are outlined in Chapters 2 and 3. The gain values for K_1 and K_2 are 12π rad/s and $9\pi 10^{-3}$ rad/s respectively whereas the capacitance value is $C=18\mu F$ and the inductance value is $L=6mH$ in this investigation. This multiple-loop proportional feedback control strategy is sufficient to ensure good performance for both steady state as well as transient responses in the present application.

Figure 6.1. Block diagram of parallel multi-inverter system.

Figure 6.2. Linear model of single inverter with multiloop feedback.

In Figure 6.2, the derivative of the load voltage is used to implement the capacitor current feedback loop. Since a direct derivative is not realizable and derivation introduces high-frequency noise, a first order low-pass-filter (6.1) is employed to obtain an

approximated derivative of the load voltage, where $\tau_c=100\mu s$. τ_c is chosen sufficiently small to avoid excessive lag between the available i_c and the true capacitor current.

$$\begin{aligned} i_c &= CsV_c \\ &\cong C \frac{s}{1+\tau_c s} V_c \\ &\cong C \frac{1}{\tau_c} \left(1 - \frac{1}{1+\tau_c s} \right) V_c \end{aligned} \quad (6.1)$$

Eventually, as shown in Figure 6.2, each single phase inverter requires only its local load voltage sensor in order to implement both control loops in the system, viz. the inner capacitor current feedback loop and the outer voltage feedback loop.

The inclusion of a pre-compensator in the system as shown in Figure 6.2 is to compensate the lag of the output load voltage (V_{load}) with respect to V_{ref}^* at the fundamental frequency. Without the pre-compensator in Figure 6.2, the relationship between V_{load} and V_{ref}^* can be deduced as (6.2), for $K'_1=4K'_2$.

$$\frac{V_{Load}}{V_{ref}^*} = \frac{1}{\left(1 + \frac{2s}{K'_1} \right)^2} \quad (6.2)$$

Therefore the pre-compensator block, as derived in (6.3), is implemented in order to achieve $V_{Load} \approx V_{ref}^*$, where $\tau_2=65\mu s$, $\tau_1 = \frac{2}{K'_1}$, $s = j\omega$ and $\omega = 2\pi(60)$.

$$\begin{aligned} \frac{V_{Load}}{V_{ref}^*} &= \frac{1}{\left(1 + \frac{2j\omega}{K'_1} \right)^2} \left(\frac{1+\tau_1 j\omega}{1+\tau_2 j\omega} \right)^2 \\ &\cong 1 \text{ (for the frequency and signal in concerned)} \end{aligned} \quad (6.3)$$

6.2.2 SOURCES OF UNEQUAL LOAD CURRENT SHARING

Based on Figure 6.2, one can investigate the sources of unequal load current sharing by considering the contribution of two different sources; the source of error contributed firstly by the controller blocks and subsequently by the system plant.

In the controller blocks as shown in Figure 6.2, each inverter has its individual voltage command and a single voltage sensor is used to implement two control loops. The possibility of having a slight different in the V_{ref}^* for each inverter is unavoidable in the actual implementation. Notwithstanding, there will also be in practice gain differences in the voltage sensors of different modules. Each of these error contributions can be represented as an external signal injection into the system as shown in Figure 6.3, where ΔV_{ref} and ΔV_{sen} denote the errors contributed by the differences in V_{ref}^* and voltage sensor gain respectively.

Figure 6.3. Sources of error in controller block.

Based on Figure 6.3, the output of control signal (V_{PWM}) will be affected by these two sources of disturbances through four paths, viz. paths $E1$ to $E4$. ΔV_{ref} enters into the

system through path $E4$, whereas ΔV_{sen} enters through paths $E1$ to $E3$. Since the pre-compensator is of unity gain, the contribution of ΔV_{ref} as seen by V_{PWM} is $K_2' C K_1' L \Delta V_{ref} = 1.06 \Delta V_{ref}$ in magnitude. This value is obtained based on the parameter values given in Section 6.2.1. Likewise, the total contribution through the loops $E1$, $E2$, $E3$ of ΔV_{sen} towards V_{PWM} , in this example, is $(1 - K_2' C K_1' L + C) \Delta V_{sen} \approx 18 \mu \Delta V_{sen}$. Therefore, based on these parameters, the analysis shows that the most significant contribution of error towards V_{PWM} is ΔV_{ref} and that from ΔV_{sen} can be neglected here. The effect of this ΔV_{ref} source towards load current sharing error is demonstrated in Section 6.2.4, where a phase different of 1° between two voltage commands of 160V amplitude will result in an error injection of $\Delta V_{ref} \approx 3V$ into the system. This ΔV_{ref} will act as an error in the current reference for the current loop just at the output of the block $K_2' C$ in Figure 6.3. Hence, minimizing of ΔV_{ref} in the system will help to ensure that the load current is shared evenly among the paralleled modules.

The system plant error, on the other hand, arises due to components' parameter deviation from that of the assumed identical module. These components include the inductor, capacitor and internal resistances, as shown in Figure 6.4. The differences in capacitance and inductance value for each inverter will result in gain errors for controller gains K_1 and K_2 . This eventually will cause the inverters to have different controller gains that will affect their transient and steady state response. Therefore, a parameters tuning technique for controllers gain is recommended in order to ensure that all inverters will have identical input-output response.

Likewise, if there is no cancellation of the plant internal resistance (R_L) in the controller blocks, each inductor current (i_L) deviate from that of other inverters due to the

difference in this internal resistive value. Thus, in order to mitigate these problems, an adaptive technique will be proposed to ensure that each controller and inverters' parameters are closely matched.

Figure 6.4. Components in system plant.

6.2.3 MITIGATION OF UNEQUAL CURRENT SHARING

As identified in Section 6.2.2, the sources to unequal load current sharing in the paralleled system are contributed by differences in V_{ref}^* and system plant mismatching. Mitigation techniques to deal with the error from these two sources will be discussed in Section 6.2.3.1 and 6.2.3.2 respectively.

6.2.3.1 IMPROVED OF SYNCHRONIZATION CONTROLLER FOR VOLTAGE COMMAND (V_{ref}^*)

In this paralleled system with decentralized controllers, the synchronization signal V_{ref}^* is obtained for each inverter through the common-mode current of each inverter. This synchronization strategy has been illustrated and practically verified in Chapter 5. Figure 6.5 illustrates the synchronization controller structure that is used in Chapter 5 to obtain V_{ref}^* , where the reference frequency (ω_{ref}) in this analysis is $2\pi 60$ rad/s.

Figure 6.5. Block diagram of synchronization controller.

Though this synchronization strategy has generated individual V_{ref}^* to be practically in phase with each other, there might be tracking error in this controller can still cause a slight phase shift in the V_{ref}^* among the paralleled inverters. Hence, a modified synchronization controller structure is proposed as shown in Figure 6.6. This modified controller structure utilizes the common load voltage V_{Load} to fine tune the synchronization of each V_{ref}^* after the inverters are connected in parallel. This V_{Load} is available and measurable locally from the voltage sensor for each inverter and this technique maintains the decentralized nature for the controller.

This modified controller structure includes the contribution of V_{Load} by obtaining its phase error (θ_{LC}) from the cross product with V_{ref}^* as shown in Figure 6.6. The proportional controller (K_{LC}) is used to amplify θ_{LC} before it is summed with the phase error θ_{SC} of V_{synch} obtained from the common-mode currents. The total error (θ_e) is then fed into the loop filter in order to generate each inverter's source voltage signal V_{ref}^* at the output of the oscillator.

Figure 6.6. Modified synchronization controller.

Based on Figure 6.6, the transient response of this modified controller can be characterized by the characteristic equation under small signal analysis computed as (6.4), where K_P and K_I are proportional and integral gain of the loop filter, $\omega = s\theta$ and $\theta_e = \theta_{LC} + \theta_{SC}$.

$$(s^2 + K_P s + K_I) \theta_e = 0 \quad (6.4)$$

This modified controller is proposed based on the idea that if the reference voltages V_{ref}^* for each controller differs slightly, V_{Load} which is common to all will still be close to the phasor sum of the V_{ref}^* 's. Includes V_{Load} in the tuning process will thus bring each V_{ref}^* closer in phase to V_{Load} and thus to each other. The effectiveness of this proposed controller is presented in Section 6.2.4.1.

6.2.3.2 ADAPTIVE CONTROLLER FOR PLANT UNCERTAINTIES

One of the ways to ensure that the plant internal resistance (R_L), in Figure 6.4, is closely match among the inverters is by introducing a high resistive feedback gain (R_e) into the controller system, as shown in Figure 6.7. The value of this R_e is chosen such that $R_e + R_L \cong R_e$, and eventually all the inverters will have a closely matched internal

resistance of R_e . However, the drawback of this method is that the output voltage will drop due to this high internal resistance.

Figure 6.7. Additional resistive feedback.

Therefore, another way of plant matching technique is by engaging the model reference adaptive control (MRAC) based on Lyapunov redesign approach with Luenberger observer. The purpose of using MRAC is to tune the parameters in the controller blocks such that the subsystem within the current loop in question will be tuned to behave identically to a reference subsystem. This will result in evenly shared load current among the inverters. The proposed structure of the MRAC is as shown in Figure 6.8. The control parameters, $\hat{K}_i$ and $\hat{R}_i$, are tuned in a stable manner to ensure that the output error, ε converges to zero.

Based on Figure 6.8, the plant and reference model are described by (6.5) and (6.6)

respectively, with $G = \frac{\hat{L}}{L}$ and $\hat{L}$ denotes the estimated plant inductance in the adaptive controller.

$$\frac{d}{dt}i_L = \hat{K}_i Gx + \frac{1}{L}(\hat{R}_i - R_L)i_L \quad (6.5)$$

$$\frac{d}{dt}i_{ref} = K_1'x + \varepsilon v \quad (6.6)$$

Figure 6.8. Model reference adaptive controller with Luenberger observer.

Subtracting (6.6) from (6.5), the resultant equation is as shown in (6.7),

with $\varepsilon = i_L - i_{ref}$, $z = \hat{K}_t G - K_1'$ and $w = \frac{1}{L}(\hat{R}_t - R_L)$.

$$\frac{d}{dt}\varepsilon = zx + wi_L - \varepsilon v \quad (6.7)$$

Multiplying (6.7) with the term ε , it can be rewritten as (6.8).

$$\varepsilon \frac{d}{dt}\varepsilon = \varepsilon zx + \varepsilon wi_L - \varepsilon^2 v \quad (6.8)$$

In this case, the updating laws for both variable z and w are chosen as (6.9) and (6.10) respectively.

$$\lambda_z \frac{d}{dt} z = -\varepsilon x \quad (6.9)$$

$$\lambda_w \frac{d}{dt} w = -\varepsilon i_L \quad (6.10)$$

Posing $\frac{1}{\lambda_z} = \frac{1}{\lambda_w} = v$ and substituting (6.9) and (6.10) into (6.8) yields (6.11).

$$\frac{d}{dt} (\varepsilon^2 v + z^2 + w^2) = -2v^2 \varepsilon^2 \leq 0 \quad (6.11)$$

Therefore (6.11) shows that the chosen updated laws (6.9) and (6.10) guarantee that $(\varepsilon^2 v + z^2 + w^2)$ is decreasing along the trajectories of (6.8) - (6.10) and variables ε , z , w are bounded. This ensures stability in the adaptive system. For the convergence of z and w to zero, the input signal needs to excite sufficiently the system. For a system with two parameters to be tuned, a sinusoidal signal is deemed sufficient.

Based on (6.9) and (6.10), the equivalent block diagram for parameter tuning of $\hat{K}_t$ and $\hat{R}_t$ are shown in Figures 6.9(a) and 6.9(b) respectively.

Figure 6.9. Block diagram of parameter tuning controller for (a) $\hat{K}_t$ and (b) $\hat{R}_t$.

Substituting Figure 6.9 into 6.8, and letting $x = x_o \sin \omega t$ and $i_L = i_o \sin\left(\omega t - \frac{\pi}{2}\right)$,

the time response of parameter tuning $\hat{K}_t$ and $\hat{R}_t$ can be deduced as (6.12) and (6.13), where $\Delta R = \hat{R}_t - R_L$, $\Delta K = \hat{K}_t - K_1$ and assuming $G = 1$. Therefore, the time responses for both $\Delta K(t)$ and $\Delta R(t)$ can be computed by solving (6.12) and (6.13) with choices of controller gain Q_K and Q_R .

$$\Delta K(t) = e^{-\alpha Q_K x_o^2 t} \left(-\int \beta Q_K \Delta R(t) e^{\alpha Q_K x_o^2 t} dt + c_K \right) \quad (6.12)$$

$$\Delta R(t) = e^{-\alpha Q_R i_o^2 t} \left(-\int \beta Q_R \Delta K(t) e^{\alpha Q_R i_o^2 t} dt + c_R \right) \quad (6.13)$$

$$\text{where } \alpha = \frac{v}{2(\omega^2 + v^2)}, \beta = \frac{x_o i_o \omega}{2(\omega^2 + v^2)} \text{ and } c_K, c_R \text{ are constants.}$$

If $\Delta R \approx 0$ and $c_K = \Delta K(0)$, then (6.12) can be further simplified as (6.14).

Likewise, (6.13) can also be rewritten as (6.15) if $\Delta K \approx 0$ and $c_R = \Delta R(0)$. Both (6.14) and (6.15) denote that the parameter tuning of $\hat{K}_t$ and $\hat{R}_t$ will converge to zero exponentially with time constant of $t_K = \alpha Q_K x_o^2$ and $t_R = \alpha Q_R i_o^2$ respectively.

$$\Delta K(t) = \Delta K(0) e^{-\alpha Q_K x_o^2 t} \quad (6.14)$$

$$\Delta R(t) = \Delta R(0) e^{-\alpha Q_R i_o^2 t} \quad (6.15)$$

6.2.4 EXPERIMENTAL RESULTS

In order to apprehend the proposed mitigation measures, three 110V_{rms}/550VA 60Hz single-phase inverters are constructed and connected as illustrated in Figure 6.1. The hardware and controller parameters for each inverter are listed in Table 6.1. The

synchronization strategy based on the common-mode current, as discussed in Chapter 5, is employed in this experimental setup to transmit V_{ref}^* to each paralleled inverter.

The experiment results demonstrate that the modified synchronization controller and the MRAC remain effective at various load conditions in improving equal current sharing for three paralleled inverters. The different types of load include linear resistive and inductive loads and a nonlinear load comprising of a rectifier with a paralleled capacitor filter.

Table 6.1. Parameter List

Component	Nominal Value	Description
L	6mH	Filter inductor
L'_{com}	1mH	Common-mode choke
C	18 μ F	Filter capacitor
f_{pwm}	20kHz	PWM switching frequency
$K_1=K'_1L$	$2\pi \times 1000 \times 6m$	Differential current loop bandwidth
$K_2=K'_2C$	$2\pi \times 250 \times 18\mu$	Voltage loop bandwidth
$K_3=K'_3L'_{com}$	$2\pi \times 5000 \times 1m$	Common-mode current loop bandwidth
$f_{sampling}$	10kHz	DSP sampling frequency
V_{dclink}	200V _{dc}	Input DC voltage source
i^*_{com}	$0.2\cos(2\pi 500 + m)t$	Common-mode current transmitting synchronization signal in FM mode
M	$2\pi 20\cos(2\pi 60)t$	Modulating signal

6.2.4.1 EXPERIMENTAL RESULTS WITH IMPROVED SYNCHRONIZATION CONTROLLER FOR V_{ref}^*

Figures 6.10 and 6.11 show the individual current obtained without and with the modified synchronization controller respectively, for a resistive load. Figure 6.11 demonstrates that the modified synchronization controller is effective and able to achieve near-perfect equal current sharing.

Figures 6.12 and 6.13 depict the individual current obtained while supplying an inductive load. The uneven sharing of the load current as shown in Figure 6.12 is obtained from the unmodified synchronization controller. After the modification, the total current is shared almost evenly by each inverter as illustrated in Figure 6.13. This demonstrates the effectiveness of the modified controller.

Figure 6.10. Individual currents supplying resistive load before modification of synchronization controller. (Channel #1:1-3: Inverter #1-3; 2A/div) Time: 10ms/div.

Figure 6.11. Individual currents supplying resistive load with modified synchronization controller. (Channel #1:1-3: Inverter #1-3; 2A/div) Time: 10ms/div.

Figure 6.12. Individual currents supplying inductive load before modification of synchronization controller. (Channel #1:1-3: Inverter #1-3; 2A/div) Time: 10ms/div.

Figure 6.13. Individual currents supplying inductive load with modified synchronization controller. (Channel #1:1-3: Inverter #1-3; 2A/div) Time: 10ms/div.

Figures 6.14 and 6.15 exhibits the feasibility of the modified synchronization controller when the inverters are supplying power to a nonlinear load. Figure 6.14 shows uneven current sharing when individual V_{ref}^* 's are not properly synchronized. An improved version of current sharing as shown in Figure 6.15 is obtained from the modified synchronization controller.

Figure 6.14. Individual currents supplying nonlinear load before modification of synchronization controller. (Channel #1:1-3: Inverter #1-3; 2A/div) Time: 10ms/div.

Figure 6.15. Individual currents supplying nonlinear load with modified synchronization controller. (Channel #1:1-3: Inverter #1-3; 2A/div) Time: 10ms/div.

6.2.4.2 EXPERIMENTAL RESULTS WITH MRAC

In order to demonstrate the effectiveness of the MRAC proposed in Section 6.2.3.2 towards matching the controller parameters with plant parameters, each internal resistance $\hat{R}_i$ for three inverters is artificially deviated from one another. Those values are $\hat{R}_{i1} = 6\Omega$, $\hat{R}_{i2} = 4\Omega$ and $\hat{R}_{i3} = 5\Omega$. Figures 6.16 and 6.17 show the sharing of individual current without and with MRAC incorporated into the system respectively, while supplying to a resistive load.

Figure 6.16. Individual inductor currents supplying resistive load without MRAC. (Channel #1:1-3: Inverter #1-3; 2A/div) Time: 10ms/div.

Figure 6.17. Individual inductor currents supplying resistive load with MRAC. (Channel #1:1-3: Inverter #1-3; 2A/div) Time: 10ms/div.

Figures 6.18 - 6.20 illustrate the time response of each inverter's parameter tuning of $\Delta \hat{R}_i$. The time response for a step change in $\hat{R}_i$, as shown in Figures 6.18 - 6.20, is about 0.9 second, which attest to (6.15) with $Q_R = 400$, $\nu = 50$, $\omega = 2\pi 60$ and $i_o \approx 3.5\text{A}$.

Figure 6.18. A step response of $\Delta \hat{R}_l$ in inverter #1. Figure 6.19. A step response of $\Delta \hat{R}_l$ in inverter #2. Figure 6.20. A step response of $\Delta \hat{R}_l$ in inverter #3.

Furthermore, the MRAC is also tested on an inductive load as well as a nonlinear load, where the internal resistance for each inverter initiated as $\hat{R}_{i1} = 6\Omega$, $\hat{R}_{i2} = 5\Omega$ and $\hat{R}_{i3} = 4\Omega$. Figures 6.21 and 6.22 demonstrate the effectiveness of MRAC in ensuring near-perfect load current sharing while supplying power to an inductive load. Likewise, Figures 6.23 and 6.24 depicts the feasibility of the MRAC in improving load sharing while delivering power to a nonlinear load.

In conclusion, these experimental results have shown that by adopting the improved synchronization controller together with the MRAC proposed within the current loop, the decentralized controllers are able to achieve near equal load current sharing among the paralleled inverters.

Figure 6.21. Individual inductor currents supplying inductive load without MRAC.
(Channel #1:1-3: Inverter #1-3; 2A/div) Time: 10ms/div.

Figure 6.22. Individual inductor currents supplying inductive load with MRAC.
(Channel #1:1-3: Inverter #1-3; 2A/div) Time: 10ms/div.

Figure 6.23. Individual inductor currents supplying nonlinear load without MRAC.
(Channel #1:1-3: Inverter #1-3; 2A/div) Time: 10ms/div.

Figure 6.24. Individual inductor currents supplying nonlinear load with MRAC.
(Channel #1:1-3: Inverter #1-3; 2A/div) Time: 10ms/div.

6.3 TRANSIENTLESS HOTSWAPPING STRATEGY (PLUG-IN)

One of the desired features in a paralleled system is the modular structure of the individual modules. This feature can be further enhanced with the flexibility of plug-in and plug-out of each module without disrupting the normal operation of the paralleled system. The plug-in strategy used in this chapter exploits the common-mode subsystem of the paralleled system as discussed in Chapter 5 to transmit a synchronization signal between the existing system and the module to be plugged in. In order to achieve this feature, further investigation and analysis is performed for plug-in issues. Three scenarios of plug-in are presented in this analysis, viz. the direct plug-in, plug-in with high resistor and the proposed plug-in strategy. These analyses will focus on the performance and effect of each scenario towards the system when they are plugged into the existing paralleled multi-inverters.

6.3.1 DIRECT PLUG-IN

Figure 6.25 illustrates the direct plug-in scenario where a new module (Inverter #4) is connected into an existing three inverter system. V_{cp} and V_{cn} are the potential differences across the capacitor of the paralleled inverters and Inverter #4 respectively. Figure 6.26 illustrates the circuit representation of the common-mode structure of the paralleled inverters, where $Z_{com} = R_{com} + jX_{com}$, $X_{com} = \omega L'_{com}$ and $V_{com}^* = i_{com}^* R_{com}$ as defined in Chapter 5. Since both V_{cp} and V_{cn} are at different potential levels initially, the load common-mode voltage for both paralleled multi-inverters and Inverter #4 is not equal and hence they are written as (6.16) and (6.17) respectively.

$$V_{Load,com_p} = \frac{V_{cp+} + V_{cp-}}{2} \quad (6.16)$$

$$V_{Load,com_n} = \frac{V_{cn+} + V_{cn-}}{2} \quad (6.17)$$

Figure 6.25. Direct plug-in of Inverter #4 into paralleled multi-inverter.

Figure 6.26. Paralleled multi-inverters common-mode circuit.

Initially, the switch S1 will be turned on prior to switching on of S2. This step will cause $V_{cp-} = V_{cn-}$. Hence, using (6.16) and (6.17) the potential difference between both common-mode voltages can be related to the difference in the differential voltages (capacitor voltages) as shown in (6.18). Figure 6.27 illustrates the new common-mode structure when S1 is turned on.

$$\begin{aligned} V_{Load,com_n} - V_{Load,com_p} &= \frac{V_{cn+} - V_{cp+}}{2} \\ &= \Delta V_{diff, np} \end{aligned} \quad (6.18)$$

Figure 6.27. New common-mode circuits with the insertion of Inverter #4 prior to switching switch S2.

Based on Table 6.1, $V^*_{com_1}$ is generating a 500Hz carrier signal with a 60Hz modulation signal for synchronization across the common-mode structure and the

remaining common-mode voltage sources are passive receiving branches, i.e. $V_{com}^* = 0$.

Thus, none of the voltage sources, $V_{com_1}^*$ to $V_{com_4}^*$, is generating a signal at the line frequency of 60Hz. On the other hand, if measures the voltage across Switch S2, (6.18) shows that, in this case, the difference of the differential voltages between the three-inverter system and that of inverter #4 is obtained; (i.e. the difference in their output capacitor voltages). This is depicted in Figure 6.27.

In this analysis, $\Delta V_{diff,np}$ is a signal with 60Hz frequency. At 60Hz, the Z_{com} 's become more resistive because $X_{com} = 2\pi 60.(0.001) = 0.38\Omega$ is relatively small and can be neglected compared to $R_{com} = K_3 = 31.4\Omega$. Thus, when switch S2 is closed, the worst condition arises when both V_{cp} and V_{cn} in Figure 6.25 are in anti-phase with each other which gives $\Delta V_{diff,np} = 220V_{rms}$ (since the inverters are generating an output voltage of $110V_{rms}$). If switch S2 is close at that instant, a high common-mode current (i_{com}) will be generated in the common-mode branch #4 and flows into the common-mode path of existing paralleled inverters, as shown in Figure 6.28, and thus saturates the common-mode chokes (L_{com}). The presence of L_{com} is to limit high common-mode flow in the paralleled system. Hence, in order to avoid this incident, the addition of a high resistance in series with the switch S2 is suggested to limit i_{com} initially. This will be discussed in the following section.

Figure 6.28. High inrush current when switch S2 is turn on at the instant where V_{cp} is anti-phase with V_{cn} .

6.3.2 PLUG-IN SWITCH WITH HIGH RESISTANCE

Figure 6.29 illustrates the plug-in of the additional module into an existing paralleled multi-inverters system using a high resistance R_s in series with the switch S2. The purpose to include R_s into the switch is to avoid saturation of L_{com} by a high inrush i_{com} when the switch S2 is turned on. The equivalent common-mode circuit based on this new feature is shown in Figure 6.30.

Figure 6.29. Plug-in of additional module (Inverter #4) with high resistance R_s in series with switch S2.

Figure 6.30. Common-mode circuit with high resistance R_s in series with switch $S2$.

The following analysis will describe how to select a suitable R_s for this purpose. Firstly, consider the condition when $\Delta V_{diff, np} = 220V_{rms}$ and the desired limit of i_{com} generated from this newly inserted module is $1A_{rms}$. Based on these parameters, the selection of R_s will be 220Ω with the possible maximum power dissipation of 220Watt (based on $i_{com} = 1A_{rms}$). Thus, this choice is not practical because of the high power dissipation requirement for the resistor.

In order to avoid such a situation, a second consideration is to increase the resistance R_s such that the power dissipation requirement is reduced. Nevertheless, high R_s (for example $R_s = 100k\Omega$ with power dissipation will require 0.484Watt) will reduce the i_{com} signal level from other common-mode sources (V_{com}^*) flowing/transmitting into branch #4, as shown in Figure 6.30. This will make extraction of the synchronization signal from the small i_{com} signal in inverter #4 difficult. Hence, in the next section, another strategy to overcome this inevitable trade-off between R_s and i_{com} will be proposed.

6.3.3 PROPOSED PLUG-IN STRATEGY

The structure of this proposed plug-in strategy is based on an improved strategy after including a high resistance R_s , as illustrated in Figure 6.31.

Figure 6.31. Proposed plug-in strategy for adding new modules.

Firstly, switches S1 and S2 are closed while S3 remains open. In this case, the common-mode circuit is that shown in Figure 6.30 with S2 closed. In this situation, (6.18) shows that the voltage drop across R_s is the difference in the capacitor voltages V_{cp} and V_{cn} . With a high R_s in series in the common-mode circuit for Inverter #4, a low power rating resistor can be employed. However, it is difficult to collect the synchronization signal issued by the multi-inverter system at this stage. To alleviate this problem of initial synchronization, V_{ref}^* of Inverter #4 is made to operate independently at a frequency slightly above or below the required line frequency (for example 59Hz or 61Hz). The voltage across R_s is now measured (V_{sense}) as shown in Figure 6.31 by inverter #4 and this gives a beat signal of 0.5 Hz. The moment the low frequency envelope of the beat signal detected by V_{sense} crosses zero, the signals V_{cp} and V_{cn} are in phase and switch S3 is closed. Thus, any inrush current is limited in magnitude at this point and with S3 closed, the flow

of the synchronizing common-mode current into Inverter #4 is no longer inhibited and synchronization can be achieved accordingly at this stage. This recommended method will thus allow a near transientless plug-in of Inverter #4 to the existing paralleled system.

6.4 DISCUSSION AND CONCLUSION

The investigations of unequal load current sharing and ways of mitigation in a decentralized controller based parallel multi-inverters are discussed in this chapter. A transientless hotswapping strategy is also proposed. The investigation identified two sources of uneven load current sharing. They are the error in V_{ref}^* and differences in plant parameters. The first source is dealt with by a modification of the V_{ref}^* synchronization controller to reduce synchronization error and the second source is dealt with by the implementation of an MRAC to achieve modules with identical responses. Three single-phase prototypes of 110V_{rms}/550VA 60Hz inverters are built to verify the proposed methods. Load condition or types did not affect the proposed mitigation solutions and near equal load current sharing is achievable with the respective mitigation methods.

A hot plug-in strategy is also discussed and analyzed in this chapter. The proposed hot plug-in strategy can achieve a transientless plug-in by employing the beat phenomenon at the initial connection and by subsequently applying the proposed common-mode current synchronization method. This avoids in particular saturation of the common-mode chokes in the presence of high in-rush common-mode currents. In recap, two main design issues of the decentralized control scheme are presented in this chapter. They are the near-perfect equal current sharing capability and the transientless hotswapping of paralleled multi-inverters. The proposed strategy and mitigation solutions are analytically discussed and verified experimentally.

Chapter 7 CONCLUSION AND RECOMMENDATIONS

7.1 SUMMARY AND CONCLUSION

This thesis explores and investigates the paralleling of power modules, with the aim to achieve decentralized control scheme that assured reliability, flexibility, reduces power ratings of each module, as well as to overcome the limitation in centralized control scheme as well as conventional droop method. A new communication strategy is developed to eliminate the need of additional interconnections among modules to transmit information across modules, and hence enhanced the system flexibility. Furthermore, the investigation of stability analysis as well as fault compensation technique is also developed to improve the overall performance and enhanced system reliability during module failure in the paralleled power modules. The basic desired features such as near-perfect equal current sharing, fast transient respond and synchronized voltage command, are also ensured in this newly developed decentralized scheme. All these features were experimentally verified to demonstrate the effectiveness and their feasibility in practical implementations.

Overall, there are three main conclusions that can be drawn from this thesis. The decentralized control without conventional limitation or additional cable drawbacks is achievable and can be implemented. The developed communication strategy further enhanced flexibility of paralleled power modules. This is desirable in many applications where information is important and required in the paralleled system.

In addition, smooth-ride through technique proposed for the output voltage when one of the paralleled modules fails is both effective and feasible. This technique is desirable in a system where reliability is uncompromised.

Eventually, all the desired features for decentralized power modules, such as near-perfect equal current sharing, synchronization of voltages, transientless hot-swapping of modules and fast transient respond, are both realizable and feasible. These features further enhance the benefits of paralleling multiple power modules. Additional features in the decentralized architecture are viable and can be attainable through further investigation and proper design. This fact, together with the advantages of paralleled modules, argues compellingly for its continuous development.

7.2 RECOMMENDATIONS FOR FUTURE WORK

There are several directions in which the continuation development of decentralized paralleled power modules should proceed. The fault compensation techniques in this thesis have been tested only in paralleled DC-DC buck converter environments. Validating these techniques in paralleled inverters is a necessary step in the next development. One possibility is to implement these techniques on the prototype developed in Chapters 5 and 6. The development of alternative techniques for fault compensation is also a worthwhile endeavor.

Further investigation and development of the common-mode communication strategy is also worthwhile. The utilization of this strategy for other purposes is greatly commendable, especially when the system requires more advanced features. Other alternatives to the encoding and decoding signals are also desirable.

Further work should also be directed at experimental verification of the hot swapping technique developed in this thesis. While this thesis has focused on mitigating the disadvantages of the existing paralleled power modules, the experimentation of the hot swapping has yet to be undertaken. In addition, the economics of this decentralized paralleled power modules over single module is also left unattended. This study may yield the insights of the full potentials in the design architecture of paralleled power modules.

Finally, the development of decentralized power supply, such as paralleling of UPS for some specific industrial or commercial applications should also be executed in the future. This step would allow direct performance and economical comparison to be made with existing solutions and also provide realistic framework for assessing the design approach.

AUTHOR'S PUBLICATIONS

1. Cheng, Y.J. and Sng, E.K.K., "Transient Analysis And Fault Compensation During Module Failure In Paralleled Power Modules", *Proc. IEEE Applied Power Electronics Conf.*, 2004, pp.1810 – 1816.
2. Cheng, Y.J. and Sng, E.K.K., "A Novel Communication Strategy for Decentralized Control of Paralleled Multi-Inverter Systems", *IEEE Transactions on Power Electronics*, vol. 21, no. 1, pp. 148-156, January 2006.
3. Cheng, Y.J. and Sng, E.K.K., "Transient Analysis And Fault Compensation During Module Failure In Paralleled Power Modules", *IEEE Transactions on Industry Applications*, vol.42, no. 2, pp. 591-601, March/April 2006.

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Appendix 1 CATEGORY AND TYPICAL CHARACTERISTICS OF POWER SYSTEM ELECTROMAGNETIC PHENOMENA [1]

Categories	Typical spectral content	Typical duration	Typical voltage magnitude
1.0 Transients			
1.1 <i>Impulsive</i>			
1.1.1 Nanosecond	5 ns rise	< 50 ns	
1.1.2 Microsecond	1 μ s rise	50 ns-1 ms	
1.1.3 Millisecond	0.1 ms rise	> 1 ms	
1.2 <i>Oscillatory</i>			
1.2.1 Low frequency	< 5 kHz	0.3-50 ms	0-4 pu
1.2.2 Medium frequency	5-500 kHz	20 μ s	0-8 pu
1.2.3 High frequency	0.5-5 MHz	5 μ s	0-4 pu
2.0 Short duration variations			
2.1 <i>Instantaneous</i>			
2.1.1 Sag		0.5-30 cycles	0.1-0.9 pu
2.1.2 Swell		0.5-30 cycles	1.1-1.8 pu
2.2 <i>Momentary</i>			
2.2.1 Interruption		0.5 cycles-3 s	< 0.1 pu
2.2.2 Sag		30 cycles-3 s	0.1-0.9 pu
2.2.3 Swell		30 cycles-3 s	1.1-1.4 pu
2.3 <i>Temporary</i>			
2.3.1 Interruption		3 s-1 min	< 0.1 pu
2.3.2 Sag		3 s-1 min	0.1-0.9 pu
2.3.3 Swell		3 s-1 min	1.1-1.2 pu
3.0 Long duration variations			
3.1 Interruption, sustained		> 1 min	0.0 pu
3.2 Undervoltages		> 1 min	0.8-0.9 pu
3.3 Overvoltages		> 1 min	1.1-1.2 pu
4.0 Voltage imbalance		steady state	0.5-2%

Categories	Typical spectral content	Typical duration	Typical voltage magnitude
5.0 Waveform distortion			
5.1 DC offset		steady state	0-0.1%
5.2 Harmonics	0-100th H	steady state	0-20%
5.3 Interharmonics	0-6 kHz	steady state	0-2%
5.4 Notching		steady state	
5.5 Noise	broad-band	steady state	0-1%
6.0 Voltage fluctuations	< 25 Hz	intermittent	0.1-7%
7.0 Power frequency variations		< 10 s	

Appendix 2 POWER QUALITY STANDARDS AND GUIDELINES FROM INTERNATIONAL ORGANIZATIONS

IEEE Power Quality Standards and Guidelines:

- IEEE SCC-22: Power Quality Standards Coordinating Committee
- IEEE 1159: Monitoring Electric Power Quality
 - IEEE 1159.1: Guide For Recorder and Data Acquisition Requirements
 - IEEE 1159.2: Power Quality Event Characterization
 - IEEE 1159.3: Data File Format for Power Quality Data Interchange
- IEEE P1564: Voltage Sag Indices
- IEEE 1346: Power System Compatibility with Process Equipment
- IEEE P1100: Power and Grounding Electronic Equipment (Emerald Book)
- IEEE 1433: Power Quality Definitions
- IEEE P1453: Voltage flicker
- IEEE 519: Harmonic Control in Electrical Power Systems
 - IEEE P519A: Guide for Applying Harmonic Limits on Power Systems
- IEEE P446: Emergency and standby power
- IEEE P1409: Distribution Custom Power
- IEEE P1547: Distributed Resources and Electric Power Systems Interconnection

IEC Power Quality Standards and Guidelines:

- IEC Power quality standards - numbering system
 - 61000-1-X - Definitions and methodology
 - 61000-2-X - Environment 61000-3-X - Limits
 - 61000-4-X - Tests and measurements 61000-5-X - Installation and mitigation
 - 61000-6-X - Generic immunity & emissions standards
- IEC SC77A: Low frequency EMC Phenomena
 - TC 77/WG 1: Terminology
 - SC 77A/WG 1: Harmonics and other low-frequency disturbances

- SC 77A/WG 6: Low frequency immunity tests
- SC 77A/WG 2: Voltage fluctuations and other low-frequency disturbances
- SC 77A/WG 8: Electromagnetic interference related to the network frequency
- SC 77A/WG 9: Power Quality measurement methods
- SC 77A/PT 61000-3-1: Electromagnetic Compatibility (EMC) - Part 3-1: Limits - Overview of emission standards and guides

SEMI Standards and Guidelines:

- SEMI F47 and F42: The voltage sag standards

Other Organizations Related To Power Quality Standards and Guidelines:

- UIE: International Union for Electricity Applications
- CENELEC: European Committee for Electrotechnical Standardization
- UNIPED: International Union of Producers and Distributors of Electrical Energy
- ANSI: American National Standards Institute
 - ANSI C62: Guides and standards on surge protection
 - ANSI C84.1: Voltage ratings for equipment and power systems
 - ANSI C57.110: Transformer derating for supplying non-linear loads
- CIGRE: International Council on Large Electric Systems
- CIRED: International Conference on Electricity Distribution
- CBEMA / ITIC curve: Industry-standard way of graphing depth vs. duration of voltage sags

Appendix 3 SIMPLE PHASE-LOCK-LOOP STRUCTURE

A simple Phase-Lock-Loop (PLL) structure will be discussed in this section. The advanced/latest PLL structures will not be described and they can be found in literatures and published papers.

Consider a simple PLL structure shown in Figure A3-1.

Figure A3.1. A simple PLL block diagram

The resultant cross product of X_{1ref} , X_{2ref} and X_1 , X_2 is (A3.1).

$$\begin{aligned}\varepsilon_{CP} &= (X_{1ref} \cdot X_2) - (X_{2ref} \cdot X_1) \\ &= \left(\sqrt{X_1^2 + X_2^2} \right) \left(\sqrt{X_{1ref}^2 + X_{2ref}^2} \right) \sin \theta_{CR} \\ &= X \sin \theta_{CR}\end{aligned}\tag{A3.1}$$

where $\theta_{CR} = \theta_{ref} - \theta_o$, $X = \left(\sqrt{X_1^2 + X_2^2} \right) \left(\sqrt{X_{1ref}^2 + X_{2ref}^2} \right)$.

Case 1: Proportional Controller as Loop Filter

If the loop filter is a proportional controller with the gain K_p , the dynamics of θ_{CP} can be determined as (A3.2).

$$\begin{aligned}\frac{d\theta_o}{dt} &= \frac{d\theta_{ref}}{dt} + K_p \sin \theta_{CP} \\ \frac{d\theta_{CP}}{dt} &= -K_p \sin \theta_{CP}\end{aligned}\tag{A3.2}$$

Since θ_{CR} is small, it is assumed that $\sin \theta_{CR} \approx \theta_{CR}$ and (A3.2) can be further simplified as (A3.3).

$$\frac{d\theta_{CP}}{dt} = -K_p \theta_{CP}\tag{A3.3}$$

Taking the Laplace transform of (A3.3), the pole of the system can be determined as $s = -K_p$. Hence, the dynamics of the PLL can be determined by selecting the appropriate controller gain of K_p .

Case 2: PI Controller as Loop Filter

Likewise, by letting PI controller gain $= \left(K_p + \frac{K_I}{s} \right)$, the dynamics of θ_{CR} can also be deduced in (A3.4). Thus, the dynamics of PLL with PI controller can be determined by selecting the desired controller gains K_p, K_I and solving the second order system in (A3.4).

$$(s^2 + sK_p + K_I)\theta_{CP} = 0\tag{A3.4}$$

Appendix 4 SIMPLE BAND-PASS FILTER

A simple band-pass filter (BPF) structure will be discussed in this section. The advanced/latest BPF structures will not be described and they can be found in literatures and published papers. The transfer function of a second-order band-pass filter can be written as (A4.1).

$$G(s) = \frac{G_o \alpha s}{s^2 + \alpha s + \omega_o^2} \quad (A4.5)$$

where

ω_o = center frequency (rad/s)

α = bandwidth

G_o = maximum amplitude of the filter

(A4.1) can be further demonstrated in Figure A4.1, where $f_o = \frac{\omega_o}{2\pi}$ and $A = \frac{\alpha}{2\pi}$.

Figure A4.2. Gain vs. frequency curve of a band-pass filter

The quality factor is defined as $Q = \frac{\omega_o}{\alpha}$. Hence, BPF will have sharper filtering feature by making Q higher.