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Achieving Near Unity Power Factor in Three-Phase Diode Bridge Rectifier-Inverter Structure

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Summary

In most line-interfaced power converter applications, the ac mains voltage is first rectified to a dc voltage/current, which is subsequently converted into voltages and currents of appropriate amplitude, frequency and shape to meet the load requirements. The front side rectifier must satisfy two main requirements: minimum harmonic injection into ac mains and high input power factor to minimize reactive power; high efficiency, high reliability and low cost to ensure competitiveness in the market. The challenge is therefore to provide a conversion scheme, which delivers high quality output waveforms without distorting the ac mains, and without drawing any reactive power.

This research project makes an effort to reduce the input current total harmonic distortion as well as to improve input power factor for three-phase diode bridge rectifiers. This thesis mainly covers the flowing aspects: development of a near unity power factor converter topology; study the feasibility of incorporating a chosen rectifier topology into a rectifier-inverter structure; investigate the effect of voltage unbalance as well as distorted input voltage in the proposed rectifier-inverter system.

A recently developed near unity power factor rectifier topology operating at low frequency was analyzed in detail and modeled with accurate mathematical equations in this thesis. A simple yet intelligent controller is proposed for the intended rectifier-inverter structure capable of operating within a wide load range and large variation of the source voltage. A prototype of the converter with the proposed controller has been built and tested to verify its feasibility. The converter shows characteristics of simplicity, low cost, near unity power factor and high efficiency. With these features, the proposed converter is suitable for mid to high power application.

Detailed analysis was further made for the proposed rectifier topology operating at relatively high frequency. A synchronous reference frame based hysteresis current

controller is proposed as well for the rectifier, to make the proposed rectifier-inverter structure perform optimally well under unbalanced and distorted supply voltage conditions. Such a situation is occasionally encountered in real life applications. Simulation and experimental results show that with the proposed controller, the converter can achieve near unity input power factor even under non-ideal supply voltage conditions. It is suitable for low power applications.

When operating at relatively high frequency, the rectifier may be controlled with either conventional hysteresis current control having random switching frequency or average current control having fixed switching frequency. It shows that the converter with average current control yields a slightly better performance than the hysteresis current control under equal conditions of permissible input current distortion. However, this is achieved at higher switching frequency compared to its counterpart. Finally, a simple and novel variable hysteresis band current control is proposed for the rectifier in this thesis. This technique overcomes the drawbacks of the above two current modulation strategies, and shows the features of constant switching frequency, easy implementation, and immunity to converter source voltages as well as load parameter variations. Laboratory prototypes for all the above mentioned controllers as well as the converters were built that confirmed the analytical and simulation results.

Chapter 1

Introduction

1.1 Motivation

Power electronics is widely applied in industrial, commercial, residential, aerospace, utility and military applications with the emphasis for energy conversion and solving environmental pollution problems [1-3]. It is estimated that roughly 60 percent of generated electrical energy is consumed by electrical motors. This has made motor drive systems a major target for numerous energy saving schemes. It is well established that adjustable speed drives (ASD) can save a considerable amount of energy by adding flexibility to the process. Therefore, more and more industries are using these schemes. This means that more electrical devices are connected to the ac systems. There are also other applications which need interfacing with utility voltage source. These include dc power supplies, uninterruptible power supplies (UPS), battery chargers and HVDC transmission systems. Interfacing with ac system is usually achieved through an ac/dc stage or rectifier [2]. As the number of applications of adjustable speed drives increases and static power converters proliferates, an undesirable impact is caused on the power system. Interactions between the power system and the converter and conversely the effect of power system disturbances on the converter performance have therefore become a major issue in the widespread use of power electronic conversion.

A. Generation of Harmonics

The switching action of converters causes a current to be drawn from the ac system that is far from the ideal sine wave shape. The distorted currents flowing through the supply ac system cause a number of undesirable effects, like distortion of supply voltage, resonance overvoltage, interference with communication circuits, equipment overheating, malfunction, and possible damage. This situation has drawn the attention of regulatory bodies around the world. Governments are tightening regulations, setting new specifications for low harmonic current and restricting the amount of electro-magnetic

waves that can be emitted [4, 5]. Minimum harmonic injection into the power system has been stipulated in standards such as IEEE-519 [5] and IEC 61000-3 [6]. Table 1.1 lists the limits on the harmonic currents that the user of power electronic equipment and other nonlinear loads is allowed to inject to the utility system.

Table 1.1 Harmonic current distortion (I_h/I_1)

I_{sc}/I_1	Odd Harmonic Order h (%)					Total Harmonic Distortion (%)
	h<11	11≤h<17	17≤h<23	23≤h<35	35≤h	
<20	4.0	2.0	1.5	0.6	0.3	5.0
20-50	7.0	3.5	2.5	1.0	0.5	8.0
50-100	10.0	4.5	4.0	1.5	0.7	12.0
100-1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Note: Harmonic current limits for nonlinear load connected to a public utility at the point of common coupling (PCC) with other loads at voltages of 2.4-69 kV. I_{sc} and I_1 are the maximum short circuit current and fundamental frequency load current at PCC respectively. Even harmonics are limited to 25% of the odd harmonic limits above.

The amount of distortion in the current waveform is quantified by means of an index called the current total harmonic distortion (THD). It is defined as [3]:

$$THD = 100 \times \frac{I_{dis}}{I_{s1}} = 100 \times \frac{\sqrt{I_s^2 - I_{s1}^2}}{I_{s1}} = 100 \times \frac{\sqrt{\sum_{h=2}^{\infty} I_{sh}^2}}{I_{s1}} \tag{1-1}$$

where I_s, I_{s1}, I_{sh} and I_{dis} are the net rms current, fundamental rms component, h order rms harmonic component and distortion component respectively.

B. The Input Power Factor

The input power factor (PF) at which an equipment operates is defined by the following equation [3]:

$$PF = \frac{real\ power}{apparent\ power} = \frac{VI_1 \cos\varphi_1}{VI_s} = \frac{I_1}{I_s} \cdot DPF \tag{1-2}$$

"The displacement power factor (DPF) equals to the cosine of the angle φ_1 by which the fundamental frequency component in the current waveform is displaced with respect to

the input line to neutral voltage waveform. The current ratio I_1/I_s is the ratio of the rms value of the fundamental frequency current component to the rms value of the total current. The power factor indicates how effectively the equipment draws power from utility. At a low power factor operation for a given voltage and power level, the current drawn by the equipment will be large, thus requiring increased volt-ampere ratings of the utility equipment such as transformer, transmission line, and generator" [3]. For example, a drop of power factor from 1.0 to 0.7 requires approximately 43% more current to supply the same rated load. This may lead to higher utility bills because of the larger current drawn by the equipment under low power factor operation.

From (1-1) and (1-2), the relationship between input power factor and current THD can be given by,

$$PF = \frac{1}{\sqrt{1+THD^2}} \cdot DPF \tag{1-3}$$

In order to achieve a high power factor, the displacement power factor should be high. Moreover, the current total harmonic distortion should be lower. Electrical utilities charge a penalty for low power factor. The additional undesirable effects caused by current harmonics, such as supply voltage distortion, resonance overvoltage and unwanted heating in the utility line, circuit breaker and transformer, can be considerably reduced when the current THD is lower. These specifications have promoted many power supply manufactures to intensify their efforts toward finding simple and cost-effective solutions for complying with the specifications.

Diode and thyristor rectifiers, the front stage of conventional ac drives, cannot meet such requirements. The typical values of input PF and current total harmonic distortion are 0.72 and 30% respectively. According to IEEE-519, for small to medium size ac drives, UPS and other loads, the required PF after improvement is 0.94. The ratio I_{sc}/I_1 of the utility a rectifier connected to is usually in the range of 50-100. And referred to Table 1.1, the current THD limit is 12%. For a rectifier operation with unity displacement power factor and 12% supply current THD, the input power factor is already 0.993. In order to reduce reactive power and comply with current harmonic limit, it is no harm if the technology permits, to improve the power factor higher than 0.94.

Recently, many innovations have been made to improve the input power factor and reduce the current harmonics [6-14]. However, the cost, volume, weight and additional power losses on magnetic components needed in those topologies withstand as a major limitation for high-power application [15]. In recent years, PWM switching-mode rectifiers have been very popular to regenerate power and to operate at near unity input power factor. However, these features are achieved by means of complicated modern control techniques and render a challenge to the switches. Moreover, the bidirectional power flow may not be necessary in some circumstance.

In practice, voltage unbalance often occurs in supply systems. The main cause is single phase loads that are not evenly distributed across all three phases [16]. The performance of rectifier-inverter structure based system will be influenced. It is necessary to investigate the effect of voltage unbalance on rectifier-inverter structure.

1.2 Objectives

In order to comply with harmonic limits and to minimize the reactive power, the rectifier must draw near sinusoidal current at high power factor. Furthermore, the rectifier must achieve high operating efficiency with low cost and small size, in order to be competitive in the market [2]. The main focus of this research project lies in the improvement of the input power factor (PF) as well as reduction of the input current THD for three-phase rectifiers. The main objectives of the research project are given below.

(1) To conduct a literature survey on existing power factor correction techniques for three-phase rectifier and investigate the limitation and application of these techniques.

(2) To develop appropriate converter topology governed by intelligent controllers.

(3) To develop a filterless (both active and passive) converter topology in order to enhance its weight, cost and efficiency.

(4) To study the feasibility of incorporating a chosen rectifier topology into a rectifier-inverter structure.

(5) To investigate the effect of voltage unbalance and non-ideal supply on the proposed rectifier-inverter system.

(6) To investigate whether the converter meets IEEE Standard 519 for power quality application.

1.3 Major contribution of the Thesis

The following original contributions have been made in the near unity power factor three-phase diode bridge rectifier-inverter structure.

(1) A recently developed near unity power factor rectifier topology [15] operating at low frequency (few times of the line frequency) was analyzed in detail and modeled with accurate mathematical equations. A simple intelligent controller is proposed for the intended rectifier-inverter structure. Due to the controller's intelligence in determining appropriate conduction times for different switches, high performance can be achieved within a wide load range and large variation of the source voltages. A prototype of the converter has been modeled, designed, built and tested. It shows the characteristics of simplicity and high efficiency. With these features, the proposed converter will be an excellent energy saver and a power factor enhancer required in a clean power environment for high power applications.

(2) Detailed further analysis was made for the rectifier topology working at higher frequency. In such operating conditions, synchronous reference frame based hysteresis current control is proposed for the rectifier to make the proposed rectifier-inverter work well under unbalanced and distorted supply voltage conditions, a situation encountered in real life application. The converter draws high quality sinusoidal supply currents and maintains good dc link voltage regulation under wide load variation. The intended converter is expected to be suitable for low to mid power applications.

(3) Variable hysteresis band current control is proposed for the rectifier. This technique overcomes the drawbacks of popular conventional hysteresis current control and average

current control strategies such as the requirement of large input filters. The controller operates by creating a variable hysteresis band envelope, and then compensating for the interaction between phases that occurs when the dc link capacitor middle point is floating. The three-phase rectifier with the proposed controller shows features of consistent near unity power factor, good adaptability to load variation, high reliability and simple control.

1.4 Organization of the Thesis

Organization of the thesis is shown in Fig. 1.1. The thesis consists of six chapters. Chapter 1 gives the brief introduction of the thesis.

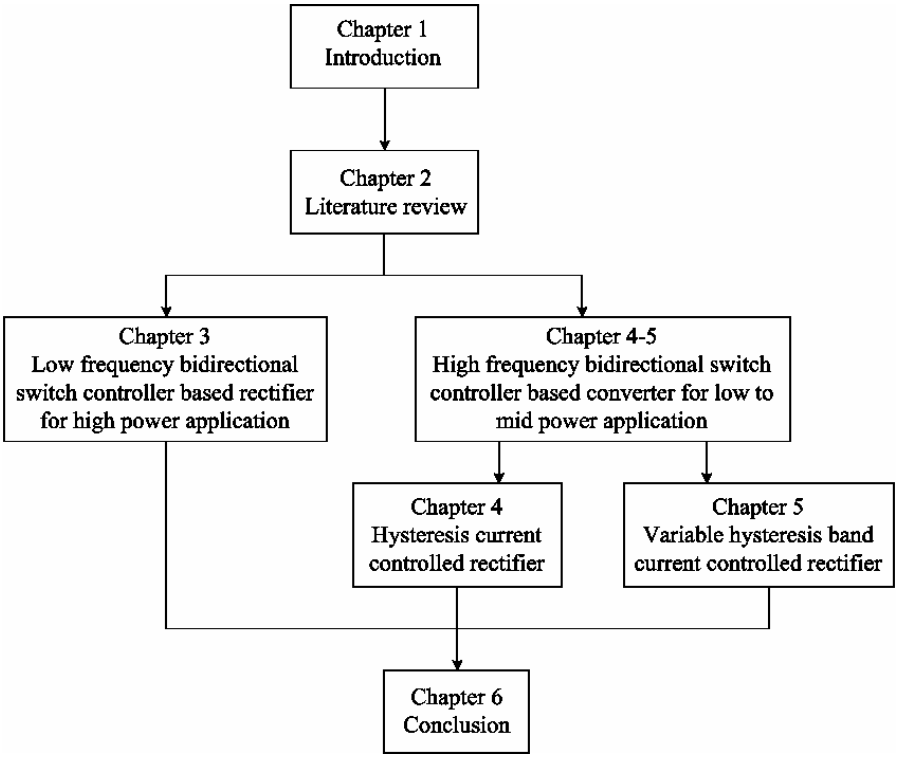


Fig. 1.1 Organization of the thesis

Chapter 2 gives the background on existing rectifier topologies, the classification and literature review of various power factor correction techniques. The advantages and disadvantages of each available technique are discussed.

Chapter 3 presents a low switching frequency near unity power factor rectifier. The rectifier with three bidirectional switches operation is well described with mathematical equations. An intelligent controller that determines the appropriate conduction times of these switches is therefore proposed. This method is found more suitable for high power application.

Chapter 4 presents the detailed mathematical analysis of the rectifier operating with high frequency bidirectional switch controller. A synchronous reference frame based hysteresis current controller is proposed for the rectifier to make the proposed rectifier-inverter function well under unbalanced and distorted supply voltage conditions.

The performance of the conventional hysteresis current control strategy and the average current strategy for the rectifier is compared and evaluated in chapter 5. Variable hysteresis band current control which can overcome the drawbacks of the former two methods is therefore proposed.

Chapter 6 gives the conclusion of this thesis, and recommendations for future work.

Chapter 2

Existing Three-Phase Rectifier Topologies and Power Factor Correction Techniques

2.1 Introduction

In most line-interfaced power conversion, the ac main voltage is first rectified to a dc voltage/current with rectifier. Analyses are given to different kinds of three-phase rectifiers, from conventional diode rectifiers to now popular PWM rectifiers [1-4]. As more stringent restrictions on power quality, such as IEEE-519 and IEC 61000-3, many power factor correction (PFC) techniques have been proposed for the rectifiers, both in terms of topologies and control methods. These methods are classified and reviewed here, advantages and disadvantages of each converter are also analyzed.

2.2 Three-phase rectifier topologies

2.2.1 Diode rectifier

Diode rectifiers are widely used in power electronic circuits for power conversion. A three-phase full bridge diode rectifier for ac/dc conversion is shown in Fig. 2.1. The rectifier input current has the well known characteristic harmonics of 5^{th}, 7^{th}, 11^{th}, 13^{th}, etc [3]. The magnitudes of these harmonic currents are inversely proportional to the harmonic order. Therefore, the diode rectifier injects large current harmonics into the ac mains, while maintaining a high displacement power factor (DPF=1).

The ac source can be converted into an uncontrolled fixed dc source in this simple and reliable way. Therefore, even in present days, diode rectifiers are still the first choice for application just requiring a fixed dc voltage. However as more stringent restrictions on harmonics, some methods have been proposed to eliminate the current harmonics of three-phase diode rectifier, as described later in this chapter.

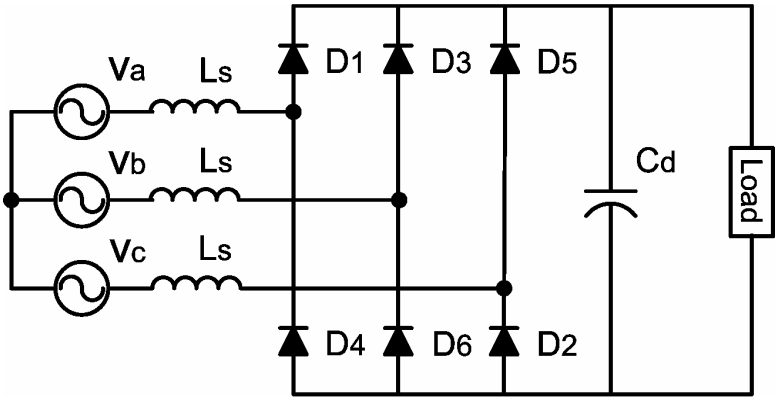


Fig. 2.1 Three-phase diode bridge rectifier

2.2.2 Phase controlled rectifier

The output voltage of the rectifier in Fig. 2.1 cannot be varied. If the diodes are replaced by thyristors, as shown in Fig. 2.2, the output voltage can be controlled by delaying the firing angle. Firing angle also influences the magnitude of the current harmonics. The power factor increases as the firing angle decreases. This topology is attractive due to its inherent ruggedness, high efficiency and simple control circuit. However, it has the well-documented drawbacks of poor input power factor and large low order harmonics in the input line currents.

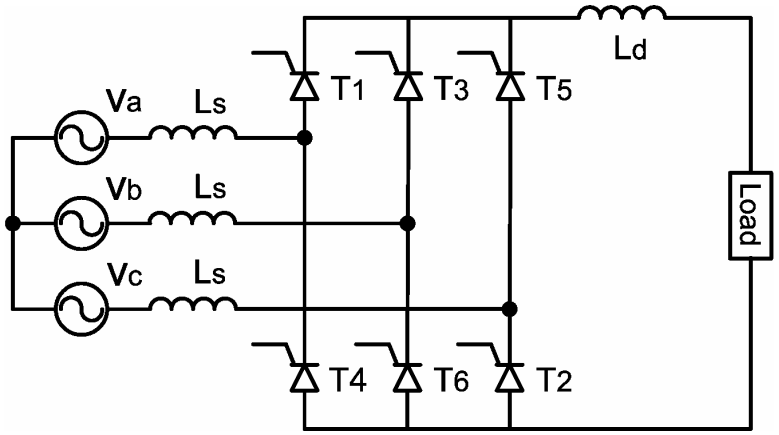


Fig. 2.2 Line-frequency phase controlled rectifier

With the growing use of such kind of rectifiers, utility systems are facing serious power quality problems. As it was mentioned before, recently proposed standards tend to

severely restrict harmonic injection into ac mains. Bulky and expensive filters have been used to suppress the injected harmonics. However, the cost and complexity of such compensating schemes will tend to reduce phase-controlled converters application in the future.

2.2.3 PWM rectifier

Recent advances in power semiconductor technology have produced high voltage/high current fast gate turn-off switching devices such as GTOs and IGBTs. Consequently, the thyristor switches in converter are being replaced by these devices, making it feasible to apply pulse width modulation (PWM) techniques to converters. Operation of the converters with PWM switching patterns offers features such as sinusoidal input current at unity displacement power factor and a high quality dc output voltage. Successful application of PWM techniques to forced commutated converters has prompted recent investigations in finding more suitable topologies for ac to dc conversion. Two significant trends are current source topology and voltage source topology.

Current source topology

The ac and dc sides of current source PWM rectifier [17-19] are interfaced by means of six unidirectional (current)/bidirectional (voltage) switches, as shown in Fig. 2.3.

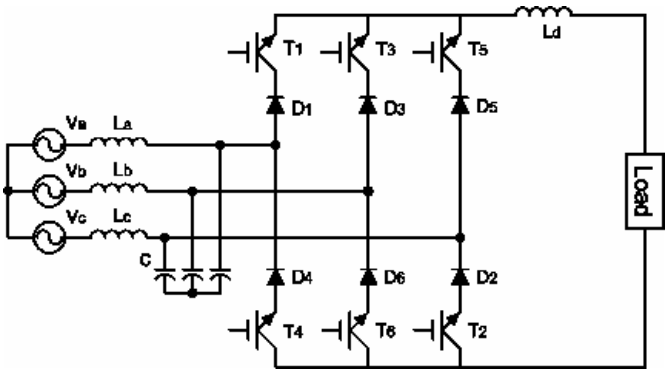


Fig. 2.3 Current source PWM rectifier

These switches must be operated so as to avoid an open circuit on the dc link or a short circuit in the ac side. The input capacitors, used as input filter and voltage spike suppression, make the rectifier prone to resonance problems. A path for the output dc

current must exist at all times which requires short-circuiting pulses when no current is drawn from the utility [2]. This brings the difficulty to generate proper switching gating signals. Moreover, a large inductor is required to smooth the dc current. This causes significant increase of cost, size, weight and losses.

Voltage source topology

Fig. 2.4 shows the topology of a voltage source PWM rectifier. Here, the ac and dc sides are interfaced by six bidirectional (current)/unidirectional (voltage) switches. These switches must avoid short circuit on the dc side or open circuit on the ac side. In the literature, there are many excellent papers about the PWM theory and the associated control methods [20-27]. Voltage source converter can provide a high performance while the high switching power losses limits its application on high power conversion. Moreover, complicated gating circuits also added its higher cost.

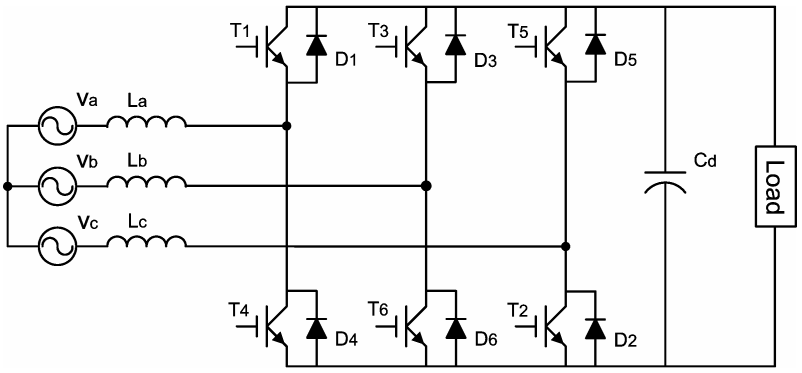


Fig. 2.4 Voltage source PWM rectifier

2.3 Power factor correction techniques

High power factor requires high displacement factor and low current harmonics. Two ways to improve the power factor and minimize the apparent power drawn from the power source are:

- Compensate for the lagging reactive current by supplying leading reactive current to the power system.
- Reduce the lagging reactive current demand and current harmonics from the load side.

"Lagging reactive current represents the inductance of the power system and power system components. Lagging reactive current demand may not be totally eliminated but may be reduced by using power system devices or components designed to operate with low reactive current requirements. Practically no devices in a typical power system require leading reactive current to function; therefore, in order to produce leading currents certain devices must be inserted in a power system" [28]. The simplest way is to install capacitor banks to the power system. By proper selection of capacitor banks, a high power factor can be achieved.

Instead of using capacitors, it is possible to use an unloaded synchronous motor to provide leading power factor. Synchronous motors applied for power factor controls are called synchronous condensers. A synchronous motor normally draws lagging currents, but when its field is overexcited, the motor draws leading reactive currents. By adjusting the field currents, the synchronous motor can be made to operate in the lagging, unity, or leading power factor region to maintain the system power factor at a specified level [28].

The second method of "reducing the lagging reactive current demand and current harmonics from the load side" is the topic of interest in this work. Most electronic equipment uses rectifiers in its power conversion process. However, rectifiers are nonlinear loads and generate a lot of current harmonics. In order to achieve high power factor, the supply current should be nearly sinusoidal and the phase shift between corresponding voltage and current should be nearly zero. In the three phase rectifier system, the displacement factor of diode bridge rectifier is almost 1. The supply current of actively controlled three phase rectifier can be easily synchronized with corresponding voltage with modern control method. Thus the main task of power factor correction techniques in three phase rectifier system is to reduce current harmonics.

The techniques for power factor correction and harmonic reduction in rectifier system can be broadly classified as shown in Fig. 2.5 [6]. Filters when used alone do not provide a regulated dc output voltage while active waveshaping techniques provide a regulated dc output voltage. Considerable portion of this section is dedicated to the modern current waveshaping techniques in three-phase rectifier.

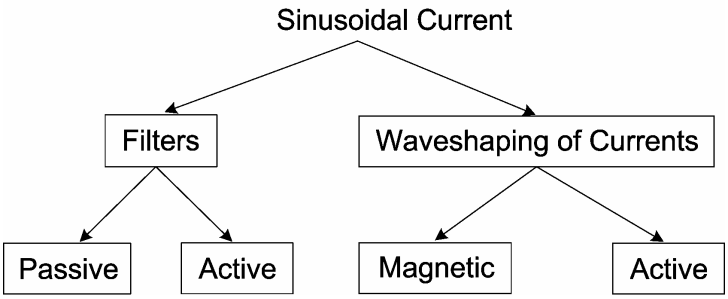


Fig. 2.5 Classification of power factor correction and harmonic reduction techniques

2.3.1 Filters

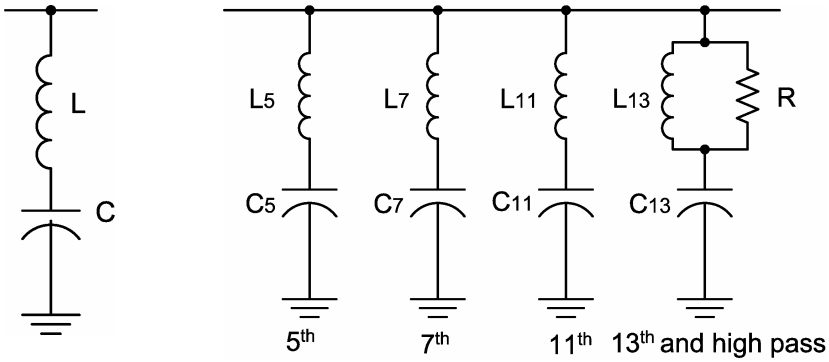
1) Passive filters

Passive filtering, the traditional approach for harmonic reduction, is a straightforward method. Passive harmonic filters are constructed from passive elements, namely resistors, inductors and capacitors and thus the name. Undesirable harmonic currents can be prevented from flowing into utility grid by either a high impedance series blocking element or a low impedance shunt pass element. Series filters are seldom used due to their high cost, inefficiency and size [29].

A shunt filter is required to trap the harmonic currents to correct the power factor of the load and properly filter the harmonics of the load [30, 31]. Fig. 2.6(a) shows a simple single frequency tuned filter with a high admittance at its tuned frequency. Fig. 2.6(b) shows a system of multiple filters tuned to different frequencies.

However one major problem is their tendency to create harmonic resonance. This will cause many dangerous problems such as overheating of capacitors, appearance of excessive harmonic overvoltage, and electromagnetic interference problems as well as other electrical problems. Although this inherent resonance problem can be eliminated, a well designed small-rated series active filter is required to combine with the shunt passive filter [32]. Furthermore the optimal performance of a filter system can be achieved under a unique system state. When the system is not in the optimized state of passive filter, filter performance is degraded. In this situation, harmonics in the power

system may not be substantially reduced under certain load and system impedance conditions. Therefore extra care must be taken when designing passive harmonic filters.



(a) Single filter (b) Multiple filters

Fig. 2.6 Shunt passive filters

2) Active filters

The limitation of the passive filtering method is that optimal performance is expected only under a unique system state. For variable loads, the system characteristics may change significantly. An active filter operates in closed loop feed back configuration and will have an adaptive nature [3]. It compensates for harmonics and corrects the power factor by supplying the harmonic currents drawn by nonlinear loads. Fig. 2.7 shows a one-line diagram of how an active filter functions.

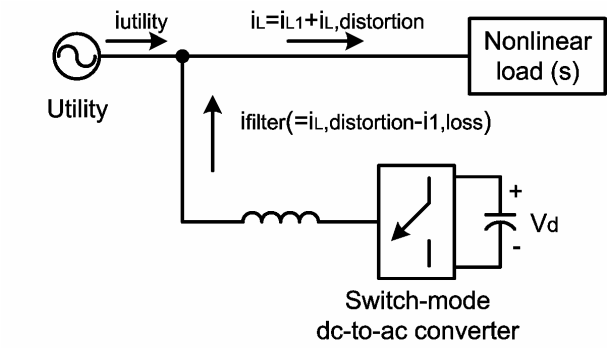


Fig. 2.7 Active filter

The current drawn by the nonlinear load(s) consists of a fundamental-frequency component i_{L1} and a distortion component $i_{L,\,distortion}$. The load current is sensed and filtered to provide a signal proportional to the distortion component $i_{L,\,distortion}$. Under a current-mode control, a switch mode dc-to-ac converter is operated to deliver the current $i_{L,\,distortion}$ to the utility. Therefore, in an ideal case, only a capacitor with minimum energy storage is needed, because the dc voltage across it is maintained by the switch-mode converter that transfers real power from the utility to compensate for its own losses by drawing a small current $i_{1,\,loss}$.

The main disadvantage of active filtering is that the extra converter and its control circuits are needed which will increase the total cost. However this is a good solution for harmonic compensation with variable nonlinear loads. Therefore active filters are mainly installed by high power consumers such as industry plants in the vicinity of harmonic producing loads, or by electric power utilities in substations and/or distribution feeders.

2.3.2 Single-phase passive PFC techniques

Passive PFC methods use additional passive components in conjunction with the diode bridge rectifier. One of the simplest methods is to add an inductor at the ac side of the diode bridge, in series with the line voltage. The maximum power factor that can obtained is PF=0.76, with the theoretical assumption of constant dc output voltage [3]. A good approach is to use a harmonic trap filter. The harmonic trap consists of series resonant network, connected in parallel to the ac source and tuned at a harmonic that must be attenuated [33]. For example, the filter shown in Fig. 2.8 has two harmonic traps, which are tuned at the 3rd and 5th harmonic, respectively. The line current waveform is well improved, at the expense of increased circuit complexity.

Passive power factor correctors have certain advantages, such as simplicity, reliability and ruggedness, insensitivity to noise and surges and no high frequency switching losses. On the hand, they also have several drawbacks. Solutions based on filters are heavy and bulky, because line-frequency reactive components are used. They also have poor

dynamic response, lack voltage regulation and the shape of their input current depends on the load [33].

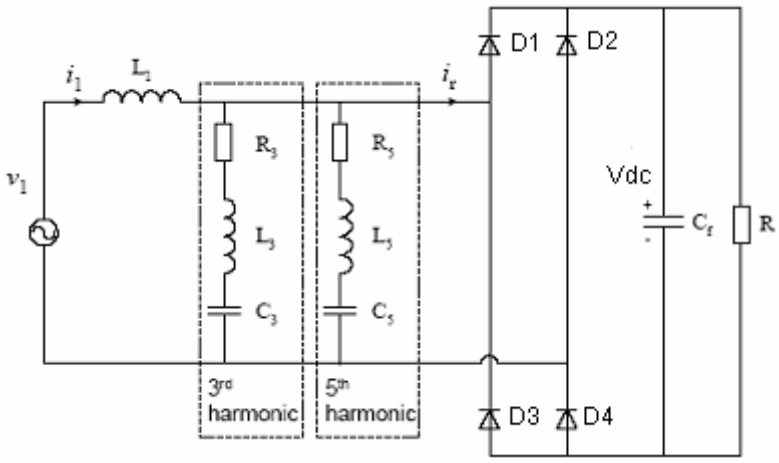


Fig. 2.8 Rectifier with harmonic trap filters

2.3.3 Single-phase active PFC techniques

The single-phase active PFC techniques for diode rectifier can be divided into two categories: the two-stage approach and the single-stage approach.

Two-stage approach

The two-stage method is widely used. In this kind of converters, an active PFC stage is adopted as the front-end to force to the line current to track the line voltage, and therefore achieve high input power factor. The PFC front-end stage converts the ac input voltage into dc voltage on a bulk energy-storage capacitor. Then a conventional DC/DC converter is used as the second output stage to provide isolation and regulated output voltage. Fig. 2.9 shows the general structure of the two-stage PFC converter with two independent power stages [34]. The first PFC stage can be a boost, buck/boost or flyback converter. Generally, the boost converter is the most popular topology for this purpose, since the boost inductor is in series with the input line voltage.

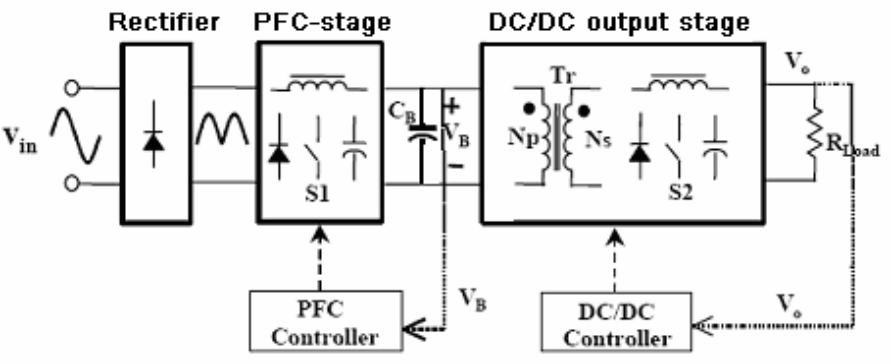


Fig. 2.9 General structure for two-stage PFC approach

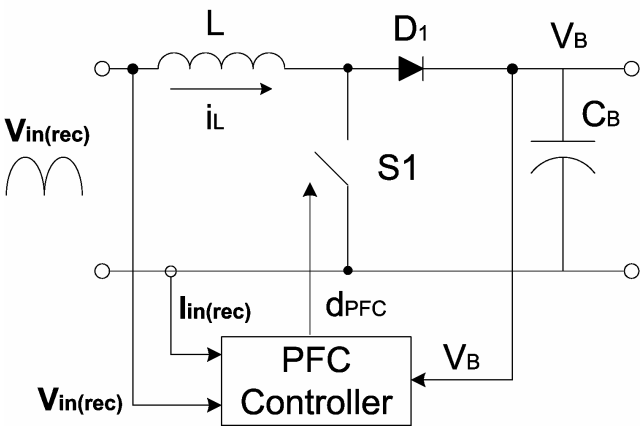


Fig. 2.10 Boost PFC stage

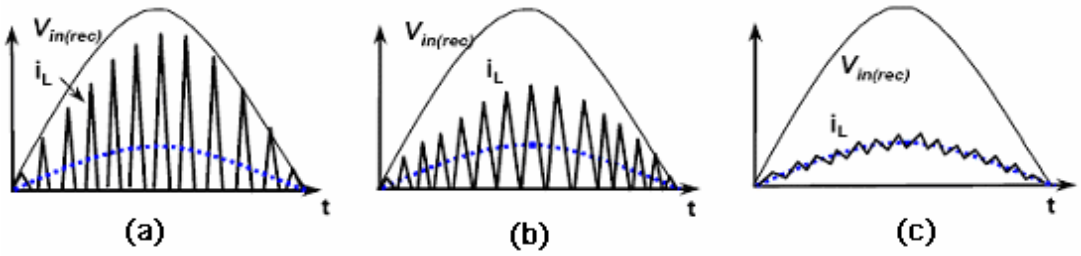


Fig. 2.11 Typical boost PFC stage in different operations: (a) DCM mode; (b) critical (boundary) mode; and (c) CCM mode

"Fig. 2.10 shows a typical boost PFC stage of the two-stage converter. Fig.2.11 show that the boost inductor can be operated in several different conduction modes, such as discontinuous-conduction-mode (DCM), variable-frequency critical (boundary) conduction mode, and continuous-conduction-mode (CCM). In terms of control implementation, the DCM PFC approach requires the simplest control: the PFC switch S1 is operated with a constant duty-cycle and fixed frequency during a half-line cycle,

without sensing the input voltage or current [35]. This provides a low-cost solution for low-power applications. The drawback of the DCM boost rectifier is its high input inductor current ripple, which causes high current stress on the power switch and requires a large electromagnetic-interference (EMI) filter. In the critical mode PFC, the boost switch is operated with a variable switching frequency in a half-line cycle [36], which keeps the inductor operating at the boundary of DCM and CCM. The boost inductor current ripple has a peak value of twice that of the average input current. The variable frequency control also spreads the noise spectrum in the wide frequency range, which can further reduce the EMI filter size [37]. However, the wide switching frequency range causes problems for design optimization and implementation. With CCM PFC approach, the current ripples and EMI filter size are well reduced. However, it requires complicated control implementation [38]. In summary, the active two-stage PFC converter provides good input power factor with good performance" [34].

Single-stage approach

In order to reduce the added component and cost in two-stage approach, single-stage power factor correction techniques have been developed [39-41]. Fig 2.12 shows the general structure of a single-stage PFC converter [34]. The only controller is the dc/dc controller, which focuses on the tight regulation of the output voltage. The input PFC function is automatically achieved based on the principle of circuit operation. Generally, the input power factor of a single-phase PFC converter is not unity, but its input current harmonics are small enough to meet the specifications.

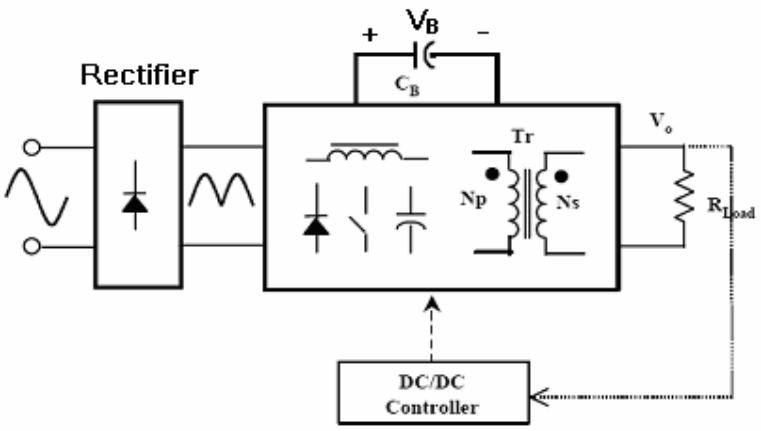


Fig. 2.12 General structure of integrated single-stage PFC converters

Single-phase PWM rectifier

Single-phase PWM rectifier, depicted in Fig. 2.13, is now becoming popular thanks to low distortion input current, near unity power factor and bidirectional power flow ability [42, 43]. It is used as active front end for bidirectional power flow applications such as locomotives, downhill conveyers, cranes etc. However, the PWM action demands high switching frequency resulting in large switching losses.

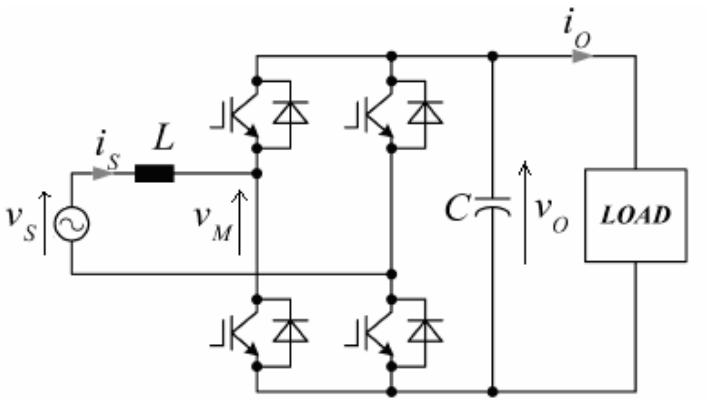


Fig. 2.13 Single-phase PWM rectifier

2.3.4 Magnetic waveshaping of currents in three-phase rectifier

In this approach, the line currents are mainly shaped by magnetic devices to be nearly sinusoidal. Among them, multiple bridge connection and third harmonic injection show much attention.

1) Multiple bridge connection

As the characteristic harmonics generated by a full-wave bridge rectifier is a function of the pulse number of that rectifier [44]. The harmonic currents in the ac side of 12-pulse rectifier only have the order of $12n \pm 1$ where n is an integer, and the main harmonics, 5^{th} and 7^{th} orders, are theoretically nonexistent. However, a 12-pulse rectifier needs two 6-pulse bridges and two sets of 30° phase shifted ac inputs. The phase shift can be achieved by an autotransformer that provides phase shifted outputs. A typical 12-pulse rectifier is shown in Fig. 2.14. With the help of phase shifting transformers, the number of phases can be increased to 18, 24, etc.

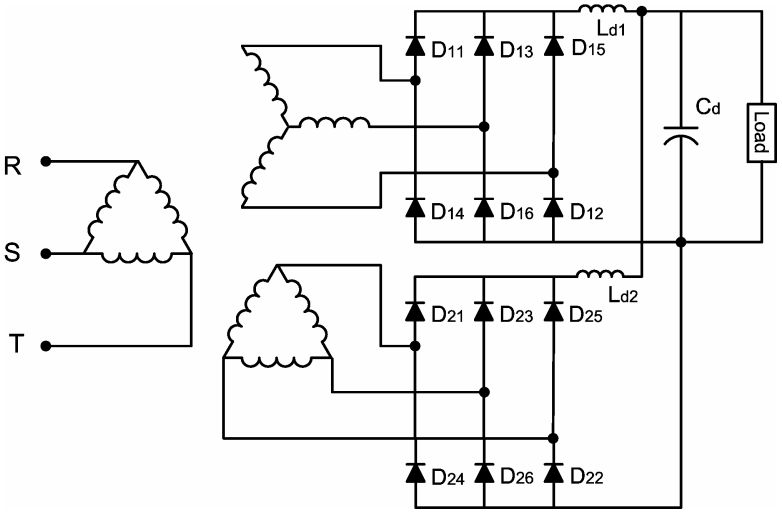


Fig. 2.14 A 12-pulse rectifier employing a three-winding transformer

2) Third harmonic current injection

Third harmonic current injection is an approach to reduce the input current harmonics of three-phase rectifier. This technique applies injection of the third harmonic currents in the rectifier supply lines in order to modify the input current waveform and to reduce its distortion. This method is originated in [45] and generalized in [46]. Lim et al proposed a completely passive approach based on the interconnection of the rectifier ac and dc sides through a star/delta transformer [11], as shown in Fig. 2.15.

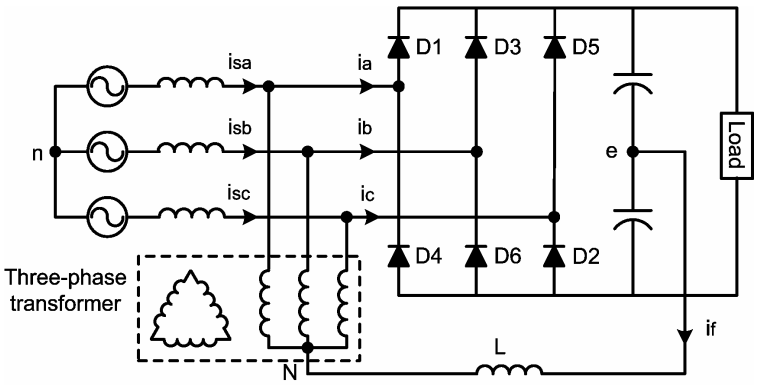


Fig. 2.15 Third harmonic current injection to improve power factor

This approach consists of a novel connection of a star/delta transformer between the ac and dc sides of the diode rectifier. This novel interconnection, in combination with 120° conduction intervals of each diode, is shown to generate a circulating third current i_f between the ac and dc sides of the rectifier topology. This third harmonic current i_f, equally divided in three limbs of the transformer, is shown to drastically improve the input power factor and reduce current harmonics.

The third harmonic current i_f is not tunable and therefore optimum operation cannot be achieved under varying load conditions. This drawbacks was overcome in [12] by employing a zigzag transformer along with a two-switch PWM current controlled converter to circulate a variable amplitude third harmonic current. A new technique based on optimum re-rectification of the third-harmonic ripple power is proposed in [47], where the above mentioned magnetic current injection device can be replaced with multifunctional capacitances. However, large capacitors and inductors are needed in the dc link, resulting in large volume and higher weight. Pejovic made a detailed analysis on the current injection method and its power aspects in [48], and introduced a more advanced current injection scheme through the use of a tuned R-L-C current injection [49]. He also explored the simultaneous current injection in all three of the phases and current injection to only one of the phases [48, 50]. Maswood extended the usage of harmonic injection method to thyristor rectifier [51]. It shows that the proposed R-L-C scheme in [49] with the addition of a compensating current phase shifter and synchronization can significantly reduce the input current harmonics and improve input power factor of thyristor rectifier.

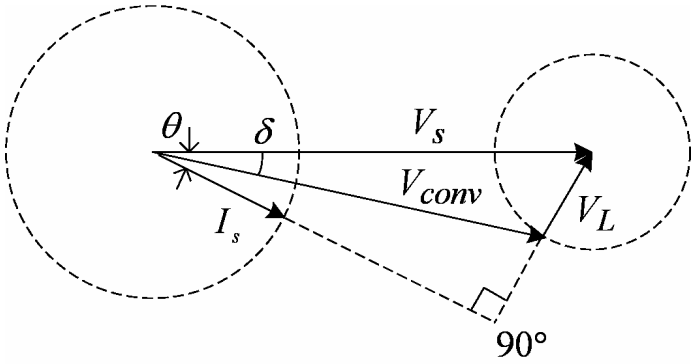
The current injection network is usually complex and extra care should be taken to choose the components. Moreover, a regulated dc output voltage cannot be provided. Thus the application of third current harmonic injection to improve input power factor is limited.

2.3.5 Active waveshaping of currents in three-phase rectifier

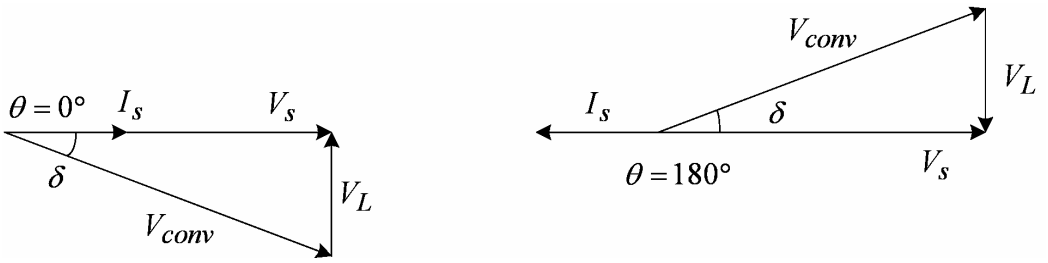
In this approach, the line currents are shaped to be sinusoidal by actively controlling the semiconductor switches at a high switching frequency. And the generation of an output voltage is constant independently of the mains voltage and the load.

1) PWM rectifier

Because of the capability to regenerate power, near sinusoidal input current and controllable dc link voltage the PWM rectifier, as shown in Fig. 2.4, is popular in high-performance ASDs where frequent acceleration and deceleration are needed [52]. The power topology of the PWM rectifier is identical to that of PWM inverter. Thus the control concepts used for inverter operation can also be used for the rectifier circuits. The basic control of the PWM rectifier [3] is explained in Fig. 2.16 (a), while the line current I_s is controlled by the voltage drop across the inductance interconnecting the two voltage supplies (source and converter). The inductance voltage (V_L) equals to the difference between the line voltage (V_s) and the converter voltage (V_{conv}). It can also be seen in Fig. 2.16 (b) and (c) that it is possible to control both the active and reactive power flow.



(a) general vector diagram



(b) unity power factor rectification (c) unity power factor inversion

Fig. 2.16 Vector diagram for PWM rectifier

Control of PWM rectifier can be considered as a dual problem with vector control of an induction motor [53]. The speed control loop of the vector drive corresponds to the dc link voltage control, and the reference angle between the stator current and the rotor flux is replaced by the reference angle of the line voltage. Various control strategies have been proposed in recent works on this type of rectifier. The voltage oriented control (VOC), which guarantees high dynamics and static performance via an internal current control loop, has become very popular and has constantly been developed and improved [54, 55]. Consequently, the final configuration and performance of the VOC system largely depends on the quality of the applied current control strategy [56]. Another strategy called direct power control (DPC) is based on the instantaneous active and reactive power control loops [57, 58]. The key point of the DPC implementation is a correct and fast estimation of the active and reactive line power.

However, the PWM rectifier has the drawbacks of high cost, high switching losses and complicated control algorithm. Moreover, the bidirectional power flow is not necessary in some circumstance. The rectifier can be designed in unidirectional version, if according to the specific application, no energy feedback from the dc side into the mains is required. This is the case, e.g., in drive systems with low dynamics (fan drives, air conditioners, etc.), uninterruptible power supplies (UPS), battery chargers (electric vehicles), electric power supply for process technology (welding units, laser and plasma power supplies) and power supply for higher power switch mode amplifiers (measurement and test equipment). This makes possible a significant reduction of the circuit complexity as compared to bidirectional systems [59]. The following parts will discuss the unidirectional rectifier power factor correction techniques.

2) Unidirectional single-switch boost rectifier

A well known topology [60] for three-phase boost line-current shaping is shown in Fig. 2.17. The active waveshaping of line currents is obtained through the use of boost chopper composed of L_b, Q_b and D_b. Since the switching frequency of Q_b can be in the order of several tens of kHz, the inductor and capacitor of input filter are quite small in size. The overall input power factor after filtering is very close to unity.

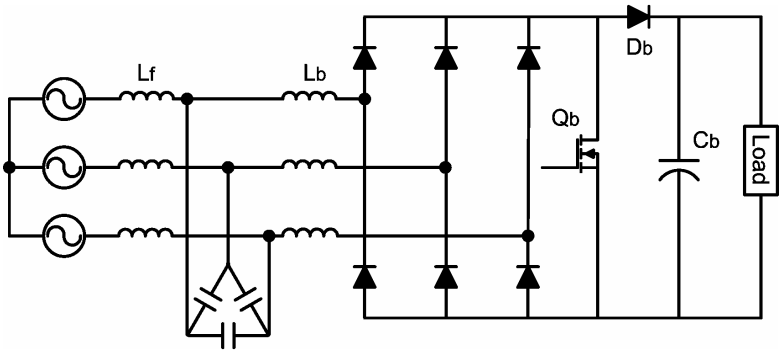


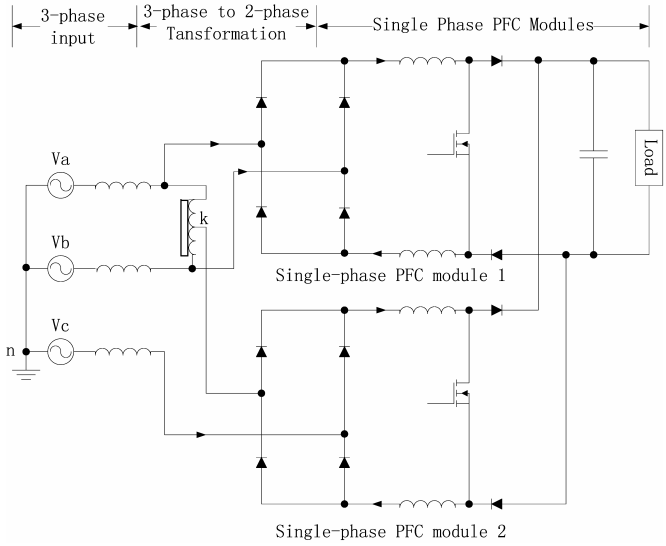
Fig. 2.17 Diode rectifier with boost chopper for active line current waveshaping

However, the discontinuous input current of the circuit shows low frequency spectral components [61] with relative amplitudes being dependent on the value of the voltage transfer ratio (output voltage related to the amplitude of the mains line-to-line voltage). A high mains current quality requires a high voltage transfer ratio, thus a high voltage stress on the switches. Further disadvantages of the circuit are the high peak current stress on the switches and a high filtering effort for guaranteeing electromagnetic compatibility. Despite of these disadvantages this circuit is suitable for different industrial applications due to its low complexity and simple control. This scheme is also an effective retrofit to improve the performance of diode rectifiers.

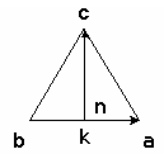
3) Three-phase power factor correction using two single-phase PFC modules

A new three-phase power factor correction scheme was proposed using two single-phase PFC modules in [62]. As shown in Fig. 2.18, three-phase input is transferred to “two” phases by means of an autotransformer. Two standard single-phase PFC modules are

employed, one on each phase to process the power. Split inductors and diodes are used to limit interaction between two PFC stages. The outputs of two PFC modules are connected to the common dc output.



(a)



(b)

Fig. 2.18 Three-phase scheme using two single-phase PFC modules
(a) Topology (b) Vector diagram of two phases

The three-phase input v_a, v_b and v_c (120° phase shift) is first transformed to two phase v_{ab} and v_{ck} (90° phase shift). Although $|V_{ab}| \neq |V_{ck}|$ (Fig. 2.12(b)), the two boost PFC stages are suitably controlled with different gains to supply one-half of the output power and operates in current continuous mode with unity power factor. With staggered PWM, the interaction between PFC modules is virtually eliminated. The resulting input line currents are nearly sinusoidal in shape. Although the PFC modules can be easily got, the additional use of transformer increases the cost. Furthermore, the control circuit of two PFC modules is a little complicated.

4) Three-phase rectifier with high power factor using Zeta converter

An isolated three phase rectifier with high power factor using a Zeta converter operating in continuous conduction mode is proposed in [63]. The topology is shown in Fig. 2.19. A Zeta converter is used to shape the line current waveform. This converter shows features of one power processing stage, lower harmonic distortion of input current and natural isolation. The high performance of this circuit is only achieved through the proper control of the zeta converter operating in continuous conduction mode.

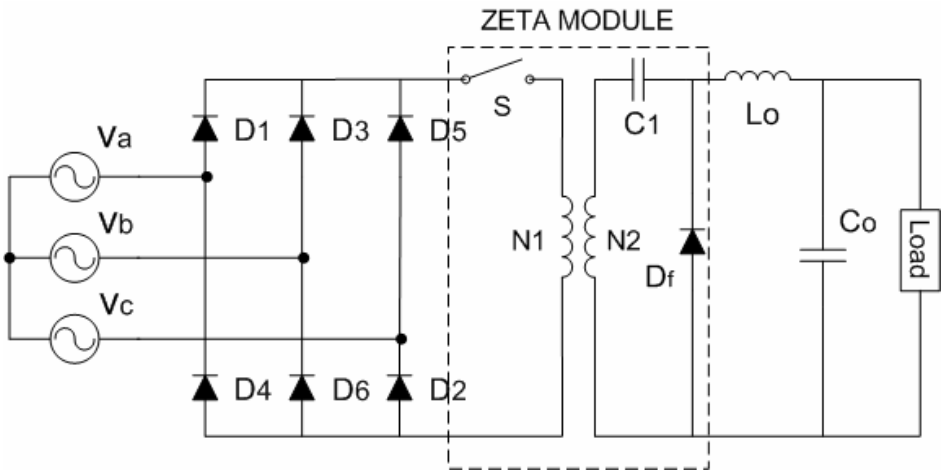


Fig. 2.19 Three-phase rectifier with high power factor using Zeta converter

5) Two diode bridges based active input current shaping

Reference [64] proposed a new three-phase diode rectifier that actively shapes the input current by means of two direct current dc-dc converters operating at continuous conduction mode. Fig. 2.20 shows the basic configuration of the proposed diode rectifier system that employs a three-phase autotransformer and two three phase diode rectifiers, each followed by a dc-to-dc boost converter operating at continuous conduction mode. The two diodes and inductors in the boost converter prevent the interaction between them. Two dc-dc converter outputs are directly connected without using low-frequency interphase transformers. Instead, four small high frequency boost inductors are used. By proper control of the switches S1 and S2, the converter draws sinusoidal input current at unity power factor and has output voltage regulation capability. However, an autotransformer is required and the control method is a little complicated.

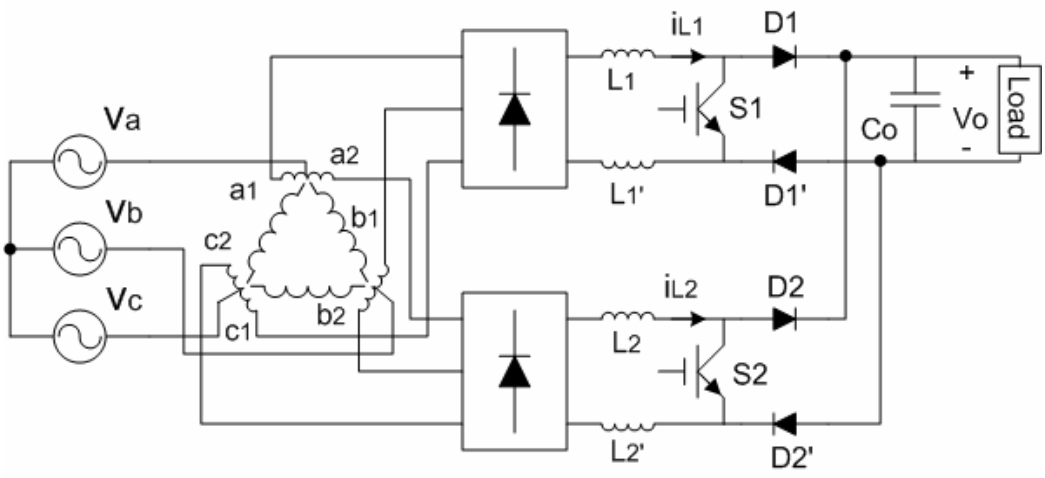


Fig. 2.20 Two diode bridges based active input current shaping

6) Three-phase three-level rectifier

Among the latest developments the three-phase three-level rectifier draws much attention. A circuit (developed at the Technical University Vienna, [65]), which is dedicated to minimizing the stresses on the devices and the level of current harmonics with switching frequency, is shown in Fig. 2.21.

When a transistor is turned on, the corresponding phase is connected to the output voltage central point, causing a rise of the associated phase current. Turning off the transistor leads to conduction of the associated diode in the upper or lower half bridge (depending on the direction of the current flow) and therefore, to a reduction of the phase current. As a result, the possibility of a sinusoidal current control is given.

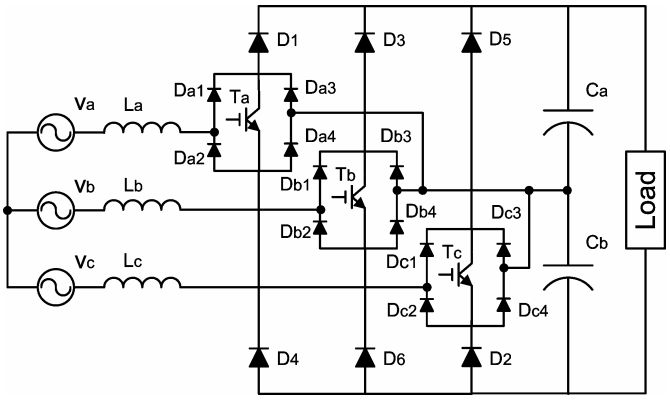


Fig. 2.21 Three-phase three-level VIENNA rectifier

Due to the inclusion of the central point of the output voltage into the system function, the bridge legs of the rectifier circuit show three-level characteristic. As opposed to two-level converter topology, the harmonic level of the mains current is significantly reduced. Furthermore, the switch voltage stress is reduced to half of the output voltage.

A space vector control technique is proposed in [66] for force commutated three-level boost type rectifier. It solved the dc link voltage middle point drifting problem. However this method needs well ascertained space vectors and is a little complicated to implement. A unified constant frequency integration controller based on one-cycle controller is well applied in the three-phase three-switch three-level rectifier with simplicity and reliability [67-69]. Comprehensive investigations of low input current distortion three-phase diode rectifier with boost converter are discussed in [69-71].

A low frequency version of this kind of topology has been proposed in [72, 73]. There, the switches are operated at low frequency. Due to low switching losses and the low transistor conduction times, this circuit achieves an outstanding high efficiency but is characterized by relatively high amplitudes of low frequency mains current harmonics occurring for low-load condition.

2.4 Concluding remarks

This chapter gives a general review of typical three-phase near unity power factor rectifier topologies. Section 2.2 reviews the diode rectifier, phase controlled rectifier and PWM rectifier. Advantages and disadvantages of each rectifier are given. Section 2.3 provides a general review of the power factor correction techniques, especially focusing on the active current waveshaping method. Among these methods, the three-phase three-level rectifier is drawing more attraction due to its near unity power factor operation and low voltage stress on the power devices.

Chapter 3

Low Frequency Controlled Near Unity Power Factor Input Stage

3.1 Introduction

A conventional inverter for three-phase induction motor drives uses a diode bridge rectifier to provide the dc link voltage. However, this kind of topology injects a large number of current harmonics into utility. This chapter presents a new method of improving the input current total harmonic distortion (THD) as well as power factor of a three-phase rectifier-inverter circuit.

This technique involves the use of three bidirectional switches across the front side diode rectifier ac side and dc side, and a microprocessor based control algorithm. Due to the controller's intelligence in determining appropriate conduction times for different bidirectional switches, high performance can be achieved within a wide output power range and even with a certain variation of input inductance. A prototype with rated output power of 1.5 kW was built in the laboratory environment for verification, and it was also tested under unbalanced supply conditions.

3.2 A low frequency controlled near unity power factor rectifier

3.2.1 A recent high power factor rectifier topology and its limitation

PWM rectifier is very popular; however, the bidirectional power flow is not necessary in some circumstance, such as uninterruptible power supplies and battery chargers. Although the circuit in Fig. 2.17 draws a high quality current from the ac source, the boost switch endures a high voltage stress. A high performance of the circuit in Fig. 2.19 is only achieved through the proper control of the zeta converter operating in continuous conduction mode. Other proposals (the circuits in Fig. 2.14, Fig. 2.15, Fig. 2.18 and Fig.

2.20) utilize special magnetic devices and sometimes even with complicated control method to achieve a high-power factor. In such cases, the total cost, volume, weight, and additional power losses on the magnetic components withstand as a major limitation for high-power factor. A recent method to improve the input power factor of three-phase rectifier, proposed by Mehl and Barbi [15], is investigated in this research work. The topology is shown in Fig. 3.1. It operates with low input current harmonic distortion and high input power factor, and does not need any clamping circuit to prevent excessive overvoltage across the active switches during the turn-off commutation. No filters or current inject transformers are needed. The main features are low cost, high efficiency, simplicity and easy to assemble. Thus this kind of topology is chosen here.

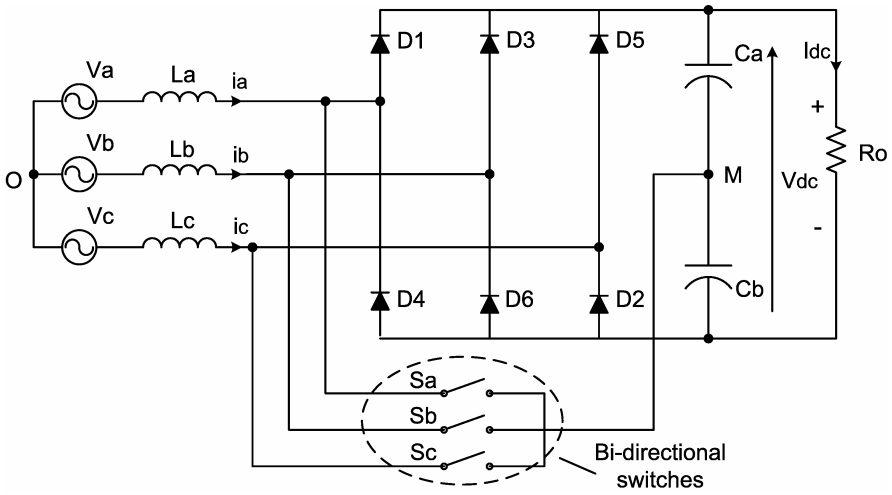


Fig. 3.1 The high power factor rectifier with three bidirectional switches

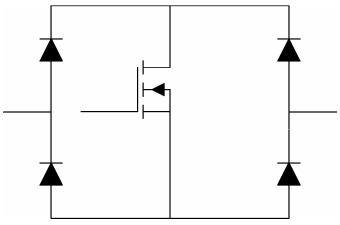


Fig. 3.2 Implementation of bidirectional switch

With reference to Fig. 3.1, V_a, V_b and V_c represent the voltage source of the three-phase ac system. Diodes D1 to D6 are line frequency rectifiers, with load Ro and input inductors L_a, L_b and L_c. Two identical capacitors C_a and C_b help to provide a balanced

central node between the positive and negative output terminals (see Appendix A). The assembly of S_a, S_b and S_c using four diodes and a low power MOSFET (or IGBT) to form a bidirectional switch is illustrated in Fig. 3.2. Although the power circuit is similar to the high-frequency pulse width modulation (PWM) rectifier presented in [50], the bidirectional switches operate at low frequency and the gating circuit is relatively simple.

The gating scheme used for the three bidirectional switches is depicted in Fig. 3.3. The line current shows a delay of approximately 30° relative to the line-to-neutral supply voltage in a conventional three-phase diode rectifier, resulting in periodical intervals where such current is null. The effect is a low input power factor and high harmonic distortion of the input current. Using the gating scheme shown in Fig. 3.3, each of the bidirectional switches S_a, S_b and S_c is turned on during a specific interval, providing an alternative path for the input current. Thus the input current waveform is well shaped to nearly sinusoidal and a gate pulse with a fixed duration of 1/12 of line voltage period (30°) results in a remarkable improvement of the input power factor and input current THD.

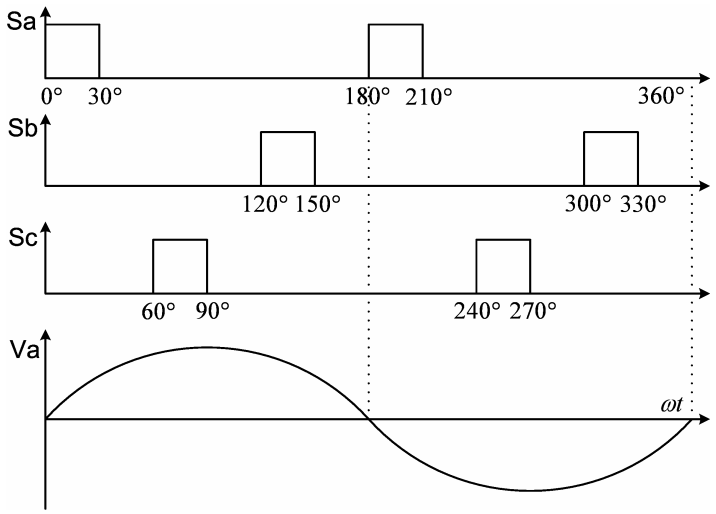
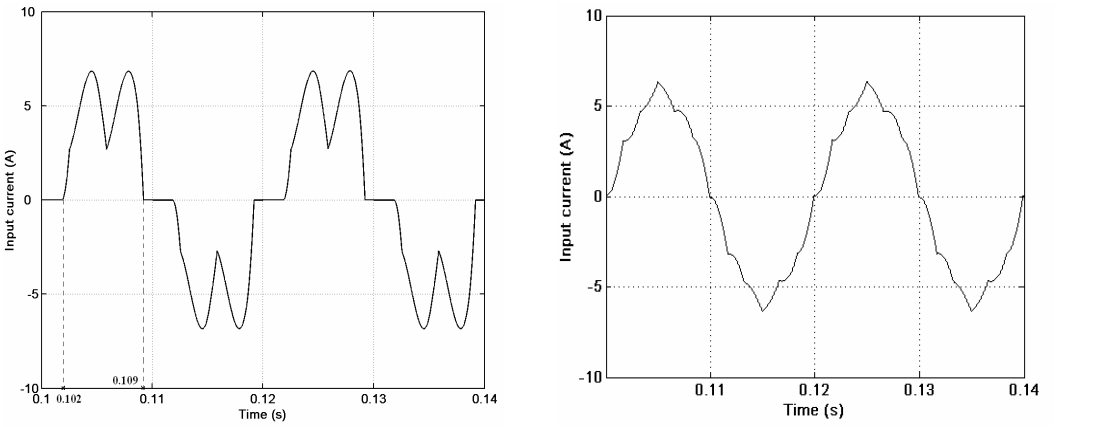


Fig. 3.3 Gating signals for Sa, Sb and Sc

Fig. 3.4 shows the input current waveform of a typical three-phase diode bridge rectifier without power factor improvement and the input current waveform of the diode bridge rectifier with three bidirectional switches.



(a) A typical diode bridge (b) Diode bridge with bidirectional switches

Fig. 3.4 Rectifier supply current waveforms

The input current waveform without bidirectional switches in a half line voltage cycle mainly has two zero-current intervals. The first zero-current interval (as 0.1s-0.102s interval shown in Fig. 3.4 (a)) can be eliminated by connecting the corresponding phase to the capacitor middle point M through turning on the corresponding bidirectional switch. The input current thus can be built. By choosing proper input inductance, the commutation time between two phases will increase and the second zero-current interval (as 0.109s-0.11s interval shown in Fig. 3.4 (b)) can be eliminated. There is a particular value to L inductance of the rectifier input inductors that can be considered as the "critical inductance". With such value of inductance, the phase current reaches zero concomitant with the corresponding phase voltage zero-volt transition as shown in Fig. 3.4 (b). This current waveform is well patched to be nearly sinusoidal and in phase with corresponding phase voltage. Therefore, the rated output voltage of the converter can be calculated by assuming that the phase current is zero when $\omega t = 180°$ [15].

$$V_o = \frac{36\sqrt{2}V_i}{7\pi\sqrt{3}} = 1.3366V_i \tag{3-1}$$

where V_o is the rated output voltage and V_i is the rms value of input line to line voltage.

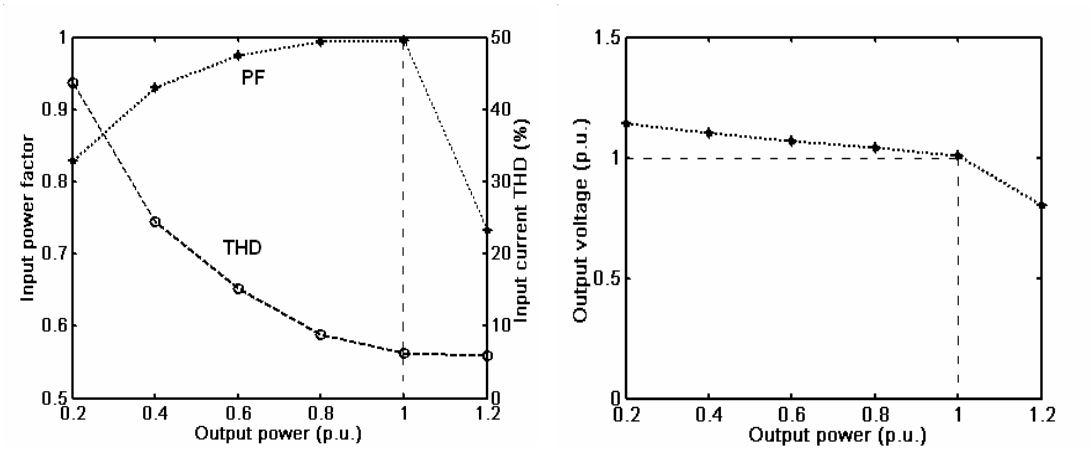
From Mehl and Barbi's work in reference [15], the "critical inductance" is given by (3-2) This equation can be also obtained by assuming that the input current (the current

expression in Table 3.2 with α=30°) supplies the load during the 90° to 120° interval of phase a voltage.

$$L = \frac{36}{7}(2\sqrt{2}-3)\cdot\frac{V_i^{\,2}}{2\pi^3 f P_o} = 3.8489\times10^{-2}\cdot\frac{V_i^{\,2}}{f P_o} \tag{3-2}$$

where f is the ac system frequency and P_o is the rectifier rated output power. The inductance of input inductors La, Lb and Lc should be the sum of line inductance (ac source inductance) and the added inductance. Assuming the ac line-to-line voltage and rated output power as base quantities, the critical input inductance from (3-2) is 0.242 p.u.. The ratio Isc/I_1 of the utility this kind of rectifier connected to is usually in the range of 50-100, and the line inductance per-unit value is less than 0.02. Thus the line inductance is considerably small compared with the required critical inductance. Thus the added inductance is determined by the required critical input inductance L.

With the above method, the input current THD can be as low as 6.6% and input power factor as high as 0.996. However, this simple diode rectifier was proposed to operate with a fixed load and fixed 'optimal' input inductance [74]. Since the bidirectional switches work independently of load on the rectifier bridge, this method cannot provide optimum input power factor as well as input current THD under varying load conditions [73]. For example, the rectifier input power factor (PF) can drop below 0.9 and input current THD increased to 20% due to the input current discontinuity at low power conditions. Fig. 3.5 shows the rectifier performance under various load conditions. When delivering a higher power than rated value, the rectifier operates in a non-efficient mode [75-77]. The phase shift between input current and voltage of the rectifier is found to exceed 30°, resulting in a lower input power factor. At the same time, the voltage drop on the input inductance is large due to the high input current.



(a) Input PF and input current THD (b) Output voltage

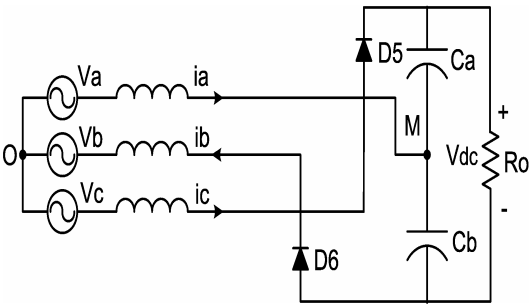
Fig. 3.5 Rectifier performance under various load conditions

3.2.2 Proposed method to improve power factor within a wide output power range

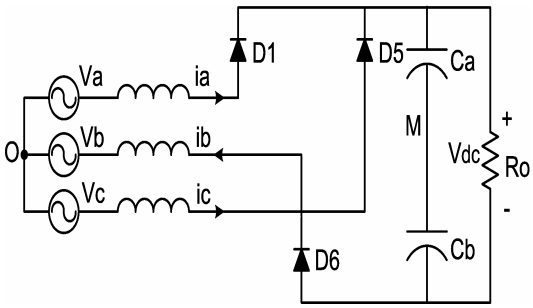
A unity power factor rectifier is proposed here to overcome all the drawbacks mentioned in 3.2.1 under varying load. It is achieved through the intelligent controller that varies the conduction period of bidirectional switches. These switches operate at only two times the line frequency and gating circuit is relatively simple. Due to the low frequency nature of the switching patterns, power losses are reduced and low-cost devices can be used. This results in a significant reduction in cost.

A. Converter operation below its rated power

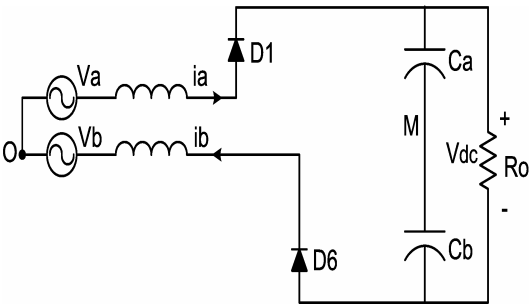
When the output power is lower than the rated output power, bidirectional switch conduction angle α is adjusted to make the output voltage constant and at the rated value. Due to phase current discontinuity, there will be nine conduction stages corresponding to the 0º–180º half period as shown in Fig. 3.6. Parameter β denotes the phase current discontinuity interval in radian per half line voltage cycle.



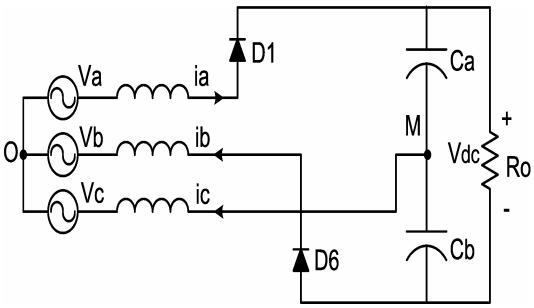
(a) Stage 1: $0-\alpha$ interval



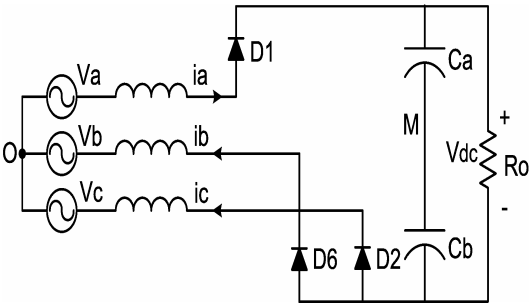
(b) Stage 2: $\alpha-(\pi/3-\beta)$ interval



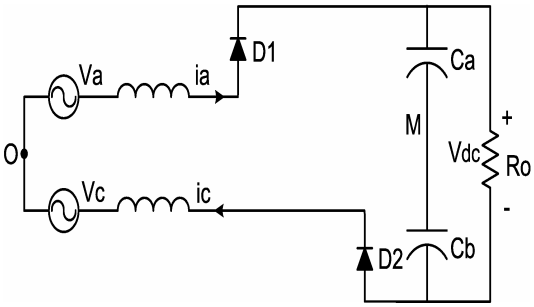
(c) Stage 3: $(\pi/3-\beta)-\pi/3$ interval



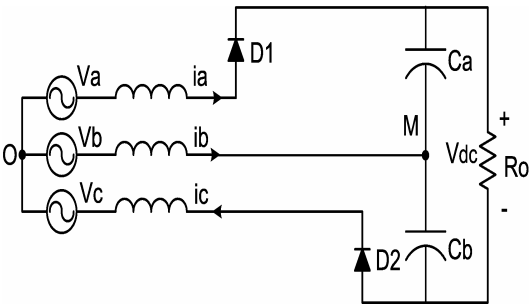
(d) Stage 4: $\pi/3-(\pi/3+\alpha)$ interval



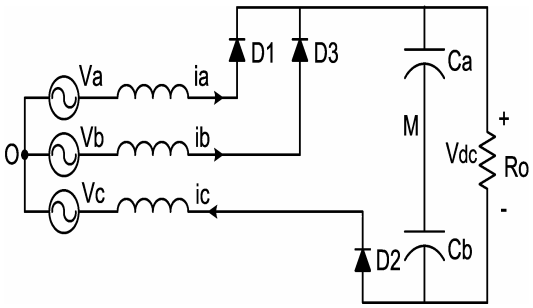
(e) Stage 5: $(\pi/3+\alpha)-(2\pi/3-\beta)$ interval



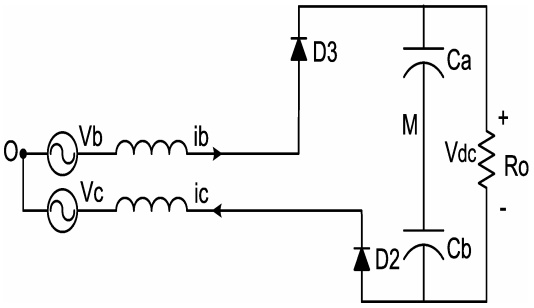
(f) Stage 6: $(2\pi/3-\beta)-2\pi/3$ interval



(g) Stage 7: $2\pi/3-(2\pi/3+\alpha)$ interval



(h) Stage 8: $(2\pi/3+\alpha)-(\pi-\beta)$ interval



(i) Stage 9: $(\pi-\beta)-\pi$ interval

Fig. 3.6 Topological stages for 0 – π interval of the Va input voltage

There are only two conducting diodes in the stages 1, 4 and 7 and three conducting diodes in the stags 2, 5 and 8. In the stages 3, 6 and 9, only two phases are conducting and the third phase current is discontinuous.

For $0-\alpha$ interval, the following equations can be obtained with reference to Fig. 3.5 (a),

$$\begin{cases} v_a = L\dfrac{di_a}{dt} + v_{MO} \\ v_b = -L\dfrac{di_b}{dt} - \dfrac{1}{2}V_{dc} + v_{MO} \\ v_c = L\dfrac{di_c}{dt} + \dfrac{1}{2}V_{dc} + v_{MO} \end{cases} \tag{3-3}$$

where, v_{MO} is the voltage between node M and node O.

For three-phase supply without neutral, the three-phase current in Fig. 3.5 (a) is guaranteed by,

$$i_a - i_b + i_c = 0 \tag{3-4}$$

From (3-3) and (3-4), we can get (3-5) for $0-\alpha$ interval,

$$v_{MO} = 0 \tag{3-5}$$

Thus,

$$v_a = L\frac{di_a}{dt} \tag{3-6}$$

Since the input phase current i_a starts from zero ($i_a(0) = 0$), it can be solved as,

$$i_a(t) = \frac{\sqrt{2}V_i}{\omega L\sqrt{3}}(1-\cos\omega t) \tag{3-7}$$

For $\alpha-(\pi/3-\beta)$ interval, (3-8) can be obtained according to Fig. 3.3 (b),

$$\begin{cases} v_a = L\dfrac{di_a}{dt} + v_{MO} \\ v_b = -L\dfrac{di_b}{dt} - \dfrac{1}{2}V_{dc} + v_{MO} \\ v_c = L\dfrac{di_c}{dt} + \dfrac{1}{2}V_{dc} + v_{MO} \\ i_a - i_b + i_c = 0 \end{cases} \tag{3-8}$$

The voltage v_{MO} and the phase current i_a can be calculated as (3-9) and (3-10) respectively.

$$v_{MO} = -\frac{V_{dc}}{6} \tag{3-9}$$

$$v_a = L\frac{di_a}{dt} + \frac{V_{dc}}{3} \tag{3-10}$$

Employing the value of i_a at $\omega t = \alpha$ as the initial value of interval $\alpha-(\pi/3-\beta)$, (3-10) can be solved as,

$$i_a(t) = \frac{\sqrt{2}V_i}{\omega L\sqrt{3}}(1-\cos\omega t) - \frac{V_{dc}t}{3L} + \frac{V_{dc}\alpha}{3\omega L} \tag{3-11}$$

The phase current of next stages is similarly analyzed and formulated in Table 3.1.

Table 3.1 Input current expressions at individual stage for $P_{out} < P_o$

Stage (ωt)	Equation
1 $0 - \alpha$	$i_a(t) = \frac{\sqrt{2}V_i}{\omega L\sqrt{3}}(1-\cos\omega t)$
2 $\alpha - (\frac{\pi}{3} - \beta)$	$i_a(t) = \frac{\sqrt{2}V_i}{\omega L\sqrt{3}}(1-\cos\omega t) - \frac{V_{dc}t}{3L} + \frac{V_{dc}\alpha}{3\omega L}$
3 $(\frac{\pi}{3} - \beta) - \frac{\pi}{3}$	$i_a(t) = \frac{\sqrt{2}V_i}{2\omega L}[\sin\beta - \cos(\omega t + \frac{\pi}{6})] + \frac{\sqrt{2}V_i}{\omega L\sqrt{3}}[1-\cos(\frac{\pi}{3}-\beta)] - \frac{V_{dc}t}{2L} + \frac{V_{dc}}{6\omega L}(\frac{\pi}{3} - \beta + 2\alpha)$
4 $\frac{\pi}{3} - (\frac{\pi}{3} + \alpha)$	$i_a(t) = \frac{\sqrt{2}V_i}{2\omega L}\sin\beta + \frac{\sqrt{2}V_i}{\omega L\sqrt{3}}[\frac{3}{2} - \cos\omega t - \cos(\frac{\pi}{3}-\beta)] - \frac{V_{dc}t}{2L} + \frac{V_{dc}}{6\omega L}(\frac{\pi}{3} - \beta + 2\alpha)$
5 $(\frac{\pi}{3} + \alpha) - (\frac{2\pi}{3} - \beta)$	$i_a(t) = \frac{\sqrt{2}V_i}{2\omega L}\sin\beta + \frac{\sqrt{2}V_i}{\omega L\sqrt{3}}[\frac{3}{2} - \cos\omega t - \cos(\frac{\pi}{3}-\beta)] - \frac{2V_{dc}t}{3L} + \frac{V_{dc}}{6\omega L}(\frac{2\pi}{3} - \beta + 3\alpha)$
6 $(\frac{2\pi}{3} - \beta) - \frac{2\pi}{3}$	$i_a(t) = \frac{\sqrt{2}V_i}{2\omega L}[2\sin\beta - \cos(\omega t - \frac{\pi}{6})] + \frac{\sqrt{2}V_i}{\omega L\sqrt{3}}(\frac{3}{2} - \sqrt{3}\sin\beta) - \frac{V_{dc}t}{2L} + \frac{V_{dc}\alpha}{2\omega L}$
7 $\frac{2\pi}{3} - (\frac{2\pi}{3} + \alpha)$	$i_a(t) = \frac{\sqrt{2}V_i}{\omega L}\sin\beta + \frac{\sqrt{2}V_i}{\omega L\sqrt{3}}(1 - \cos\omega t - \sqrt{3}\sin\beta) - \frac{V_{dc}t}{2L} + \frac{V_{dc}\alpha}{2\omega L}$
8 $(\frac{2\pi}{3} + \alpha) - (\pi - \beta)$	$i_a(t) = \frac{\sqrt{2}V_i}{\omega L}\sin\beta + \frac{\sqrt{2}V_i}{\omega L\sqrt{3}}(1 - \cos\omega t - \sqrt{3}\sin\beta) - \frac{V_{dc}t}{3L} - \frac{V_{dc}\pi}{9\omega L} + \frac{V_{dc}\alpha}{3\omega L}$
9 $(\pi - \beta) - \pi$	$i_a(t) = 0$

Note: P_{out} and P_o are the rectifier output power and rated output power respectively.

The phase current is discontinuous and deceases to zero at the end of stage 8. In addition, the output voltage is kept constant at the rated output voltage V_o. So one can get $i_a(\pi - \beta) = 0$ for the input current expression of stage 8 in Table 3.1. Thus the relationship between α and β is solved as:

$$\cos\beta = \frac{9}{7} - \frac{12}{7\pi}(\alpha + \beta) \tag{3-12}$$

For a small value of β, one can get the approximate equation as:

$$\beta \approx \frac{\pi}{6} - \alpha \tag{3-13}$$

In order to find the relationship between the conduction angle α and normalized dc link current k, several attempts have been made utilizing Table 3.1. The following relationship was found to best match its behavioral pattern:

$$\alpha = (14.9 + 15.1k) \times \frac{\pi}{180} \tag{3-14}$$

Here, k denotes the normalized dc link current with respect to the rated dc link current.

B. Converter operation above its rated power

When the output power is higher than the rated output power, the conduction angle is adjusted to maintain the output voltage constant around the value V_o. In this case, as expected the conduction angle α will be larger than 30º. The phase current is continuous and β equals to zero. Therefore there are six well-known conduction stages and two-phase conduction stages 3, 6 and 9 of low power operation do not exist here. The phase current in each stage is investigated and expressions are developed and presented in Table 3.2.

Table 3.2 Input current expressions at individual stage for $P_{out} > P_o$

Stage (ωt)	Equation
1 $0 - \alpha$	$i_a(t) = -\frac{\sqrt{2}V_i}{\omega L\sqrt{3}}\cos\omega t + \frac{2\pi V_{dc}}{9\omega L} - \frac{V_{dc}\alpha}{6\omega L}$
2 $\alpha - \frac{\pi}{3}$	$i_a(t) = -\frac{\sqrt{2}V_i}{\omega L\sqrt{3}}\cos\omega t - \frac{V_{dc}t}{3L} + \frac{V_{dc}\alpha}{6\omega L} + \frac{2\pi V_{dc}}{9\omega L}$
3 $\frac{\pi}{3} - (\frac{\pi}{3} + \alpha)$	$i_a(t) = -\frac{\sqrt{2}V_i}{\omega L\sqrt{3}}\cos\omega t - \frac{V_{dc}t}{2L} + \frac{V_{dc}\alpha}{6\omega L} + \frac{5\pi V_{dc}}{18\omega L}$
4 $(\frac{\pi}{3} + \alpha) - \frac{2\pi}{3}$	$i_a(t) = -\frac{\sqrt{2}V_i}{\omega L\sqrt{3}}\cos\omega t - \frac{2V_{dc}t}{3L} + \frac{V_{dc}\alpha}{3\omega L} + \frac{\pi V_{dc}}{3\omega L}$
5 $\frac{2\pi}{3} - (\frac{2\pi}{3} + \alpha)$	$i_a(t) = -\frac{\sqrt{2}V_i}{\omega L\sqrt{3}}\cos\omega t - \frac{V_{dc}t}{2L} + \frac{V_{dc}\alpha}{3\omega L} + \frac{2\pi V_{dc}}{9\omega L}$
6 $(\frac{2\pi}{3} + \alpha) - \pi$	$i_a(t) = -\frac{\sqrt{2}V_i}{\omega L\sqrt{3}}\cos\omega t - \frac{V_{dc}t}{3L} + \frac{V_{dc}\alpha}{6\omega L} + \frac{\pi V_{dc}}{9\omega L}$

Similarly utilizing the equations in Table 3.2, the relationship between α and k can be expressed as follows.

$$\alpha = (30k) \times \frac{\pi}{180} \tag{3-15}$$

C. Converter controller design

Once the input phase voltage crosses zero-volt point, the corresponding switch will be triggered. So each of the bidirectional switches (S_a, S_b and S_c) conducts twice in every line voltage cycle. The drive pulse width for the bidirectional switches is determined by the dc link current being supplied. According to (3-14) and (3-15), one can measure the dc link current I_{dc} to control the conduction angle α (thus pulse width). The proposed control circuit block diagram is shown as Fig. 3.7.

The dc link voltage is also detected and compared with reference voltage to provide the compensation for α. Due to the uncontrolled characteristic of diode rectifier, a tiny compensation can achieve optimum performance. After performing a number of analysis and simulation to find the most suitable value, 0.5 was chosen for K_p to be used in the voltage compensation block.

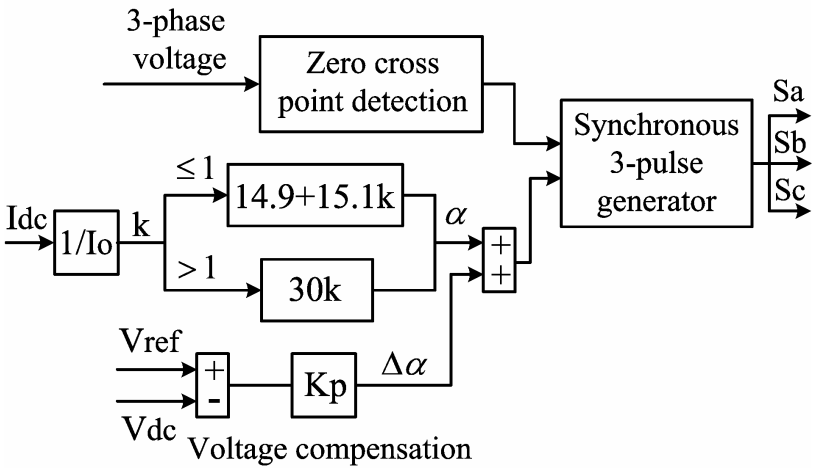


Fig. 3.7 Control block diagram

3.2.3 Evaluation of bidirectional switch ratings

Taking phase 'a' as reference, the peak current through the bidirectional switch can be calculated by substituting the upper limiter of 40° for α into the equation of stage 1 in Table 3.2. This angle is limited to such value to avoid overloading the bidirectional switches. Hence, (3-16) can be used to calculate the bidirectional switch peak current.

$$I_{sw(peak)} = 0.6291 \cdot \frac{P_o}{V_i} \tag{3-16}$$

Since the switch is off during the 40°-180° and 220°-360° intervals. The rms value of the switch's current is given by (3-17) and the average current is calculated with (3-18).

$$I_{sw(rms)} = 0.1225 \cdot \frac{P_o}{V_i} \tag{3-17}$$

$$I_{sw(avg)} = 0.0238 \cdot \frac{P_o}{V_i} \tag{3-18}$$

The bidirectional switches operate at only two times line frequency, with reduced power losses, and use low cost devices. Meanwhile, the voltage across the switch's terminals is lower than half of the dc link voltage when the switch is off, eliminating any undue voltage stress.

3.3 Design example and implementation

A sinusoidal PWM (SPWM) voltage source inverter, a very popular topology in industry for ease of implementation, is connected to the rectifier for the intended rectifier-inverter structure as depicted in Fig. 3.8.

For the purpose of illustrating the design procedure, a converter with the following specifications is chosen:

- AC supply: 220 V (line-to-line), 50Hz;
- Rated output power 1.5 kW.

The critical input inductance of L_a, L_b and L_c at the rectifier input side is calculated using (3-2), giving:

$$L_{critical} = 3.8489\times10^{-2}\cdot\frac{220^2}{50\times1500} = 24.84mH$$

For the rated output power of 1.5 kW, the dc link voltage of the front-end converter is calculated with (3-1) and results:

$$V_o = 1.3366\times220 = 294.05V$$

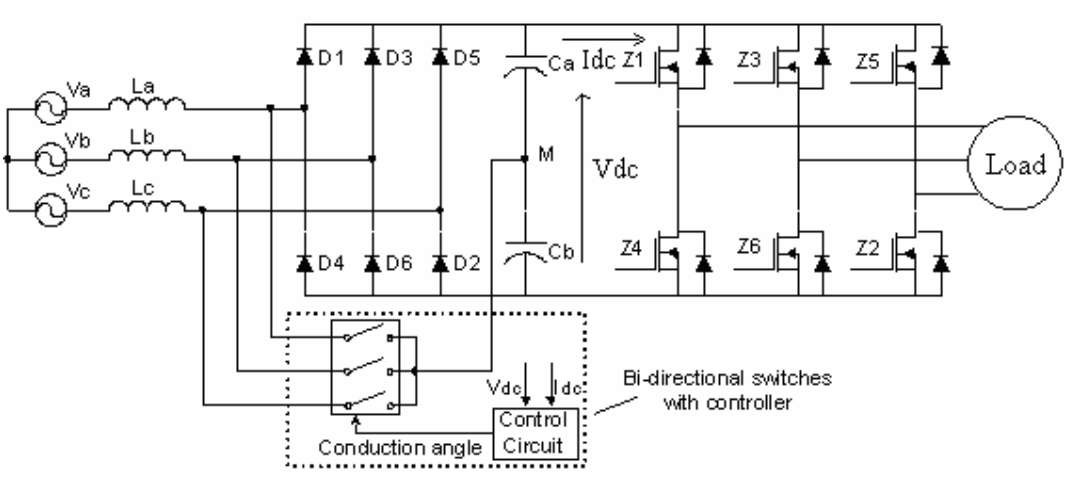


Fig. 3.8 Complete circuit diagram of the proposed unity power factor ac drive

3.3.1 Simulation results

Using the dynamic ac motor drive model, one can get the proposed converter input current waveform at rated load as shown in Fig. 3.9. The same waveform for a conventional converter is shown in Fig. 3.10.

Before improvement, the THD of the rectifier input current was found to be 85.5%, and the input power factor was 0.75. After the improvement, the input current THD is 6.5% and the input power factor is 0.995. With this method, the harmonics are effectively reduced and the highest two harmonics 5^{th} and 11^{th} are only 3.9% and 3.8% of the fundamental component respectively.

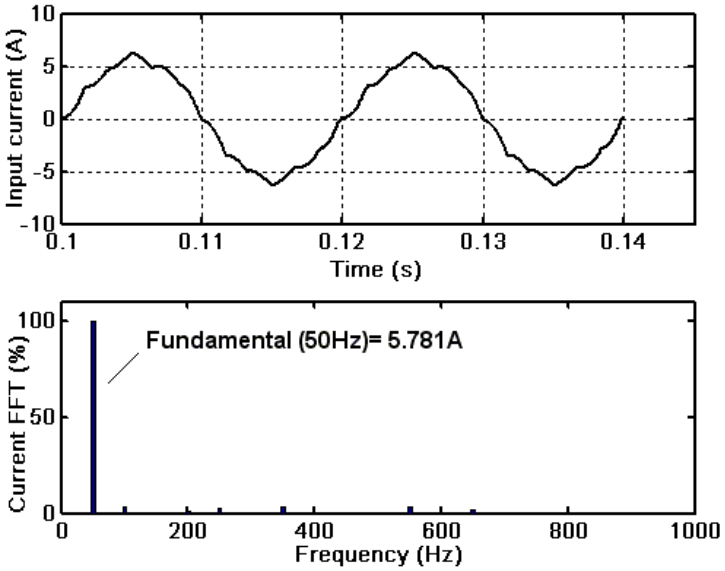


Fig. 3.9 Input current and its spectral composition with the proposed scheme at rated load

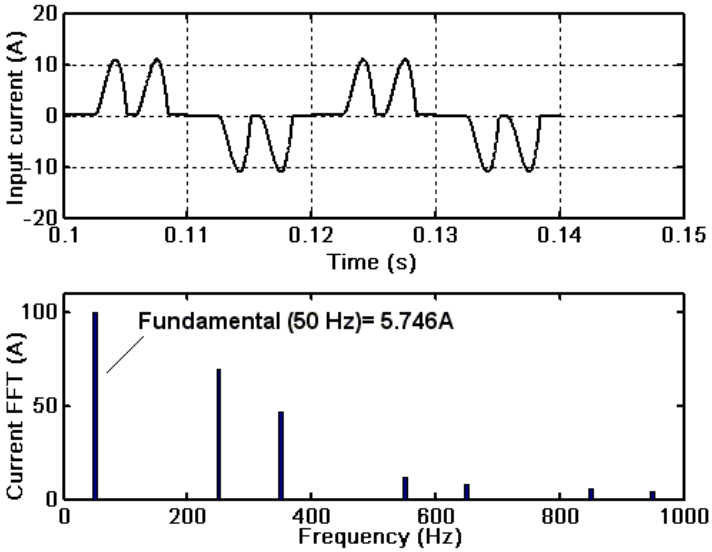


Fig. 3.10 Input current and its spectral composition of a typical 3-phase rectifier without bidirectional switches

The voltage and current through the bidirectional switch at converter rated output power are shown in Fig. 3.11. The rms values of the bidirectional switch voltage and current are 134.8 V and 0.565 A respectively. The bidirectional KVA rating is only 5.1% of the converter at rated load. Since the controlled bidirectional switch conducts for only fraction of the total conduction period and low-cost switching devices can be used.

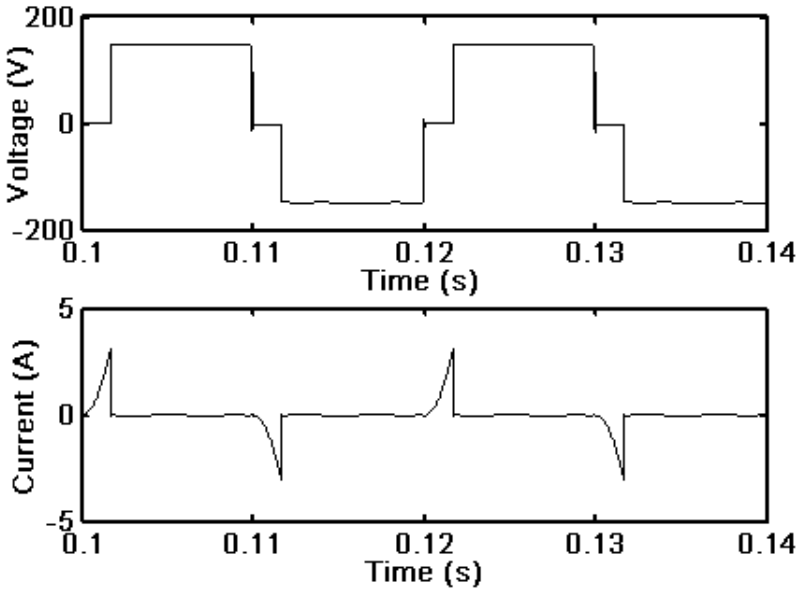
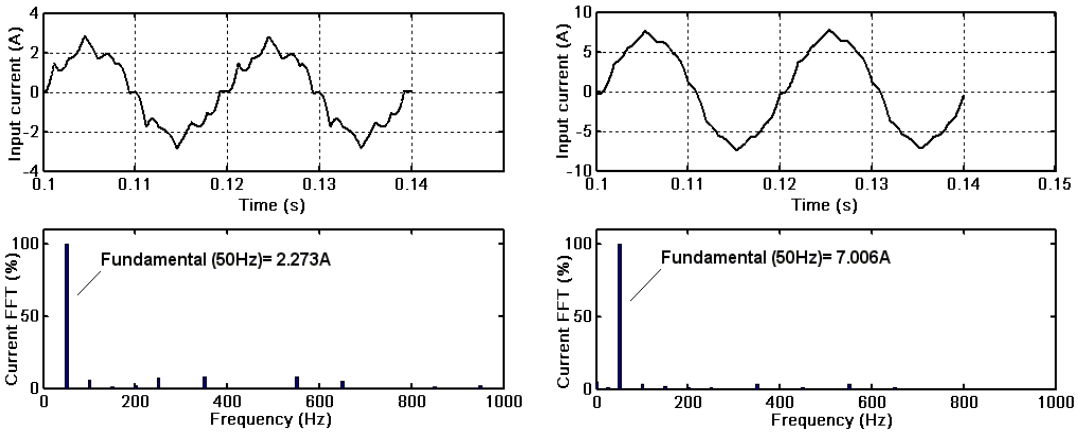


Fig. 3.11 Bidirectional switch voltage (upper trace) and current (lower trace)

The input current and its spectral compositions of the proposed converter, under 40% rated load and 120% rated load are presented in Fig. 3.12. The input power factors at 40% rated load and 120% rated load are 0.987 and 0.976 respectively. Table 3.3 gives the performance parameters at various load conditions.



(a) 40% rated load

(b) 120% rated load

Fig. 3.12 Input phase current and its spectral composition at various load conditions

Table 3.3 Performance parameters at various load conditions

Load (P_o)	φ_1 (°)Δ	THD	PF •	V_{dc} (V) ∗
40%	3.8	14.9%	0.987	295.9
100%	-4.6	6.5%	0.995	294.7
120%	-12.1	6.4%	0.976	293.1

Δ φ_1 denotes the angle between the input line to neutral voltage and fundamental current

• Where power factor is defined as: $PF = \cos\varphi_1 \Big/ \sqrt{1+THD^2}$

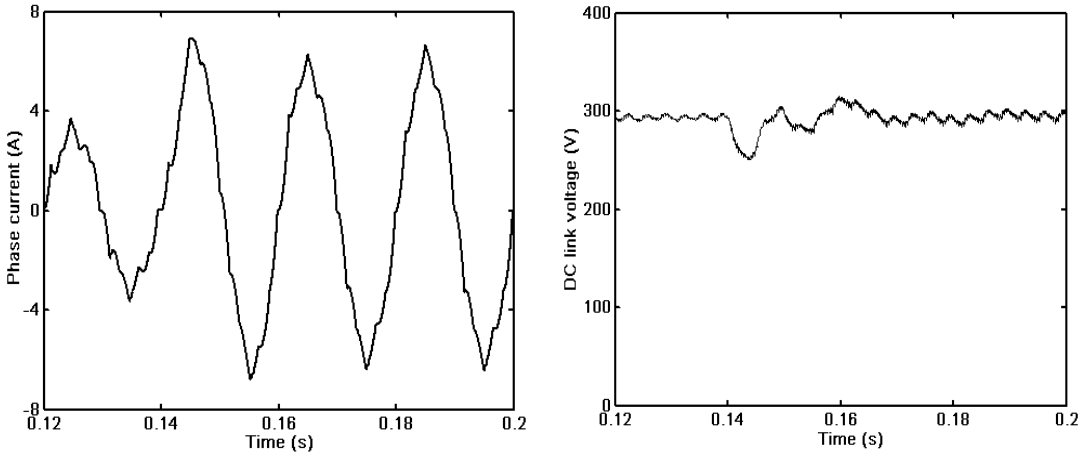
∗ The rated dc link voltage is 294.05 V

From the discussions above, one can see that the input inductance plays a vital role on rectifier optimum performance. In a given ac network, the line inductance may vary due to various reasons. However, the proposed control technique can overcome such difficulties. When the input inductance varies within a certain range, the bidirectional switches conduction angle is calculated with the help of voltage compensation part to achieve optimum performance. Table 3.4 gives the performance parameters for the converter operating at rated output power and under various input inductance conditions. One can see that this topology can achieve a good performance even with the input inductance variation of ±10% range.

Table 3.4 Performance parameters with controller under varying input inductances

Input inductance	α(°)	φ_1(°)	THD	PF	V_{dc} (V)
90%$L_{critical}$	29.7	-3.0	6.9%	0.996	296.4
100%$L_{critical}$	30.4	-4.6	6.5%	0.995	294.7
110%$L_{critical}$	32.2	-8.7	6.0%	0.987	290.0

The response to a load change from 50% to 100% rated converter output power is shown in Fig. 3.13. The change was introduced at 0.14s while the rectifier is in steady state. From these two figures one can see that this proposed control technique has a good adaptability to load variations.



(a) Input phase current (b) Dc link voltage

Fig. 3.13 Converter response due to load change

3.3.2 Experimental results

The controller is implemented using a single-board ds1102 microprocessor and developed under the integrated development environment of MATLAB-SIMULINK RTW provided by the Math Works, inc. A prototype of the rectifier-inverter structure depicted as in Fig. 3.7 is constructed, and its performance is observed. The hardware prototype is shown in Fig. 3.14.

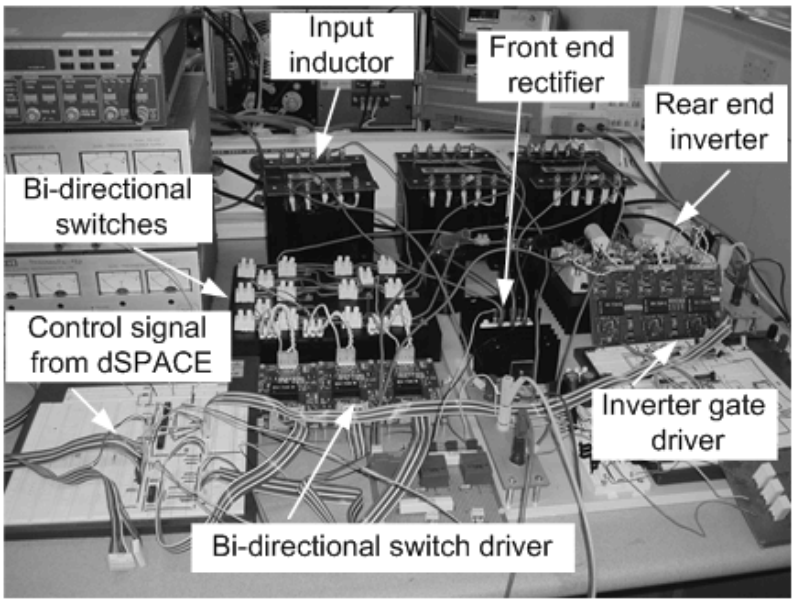
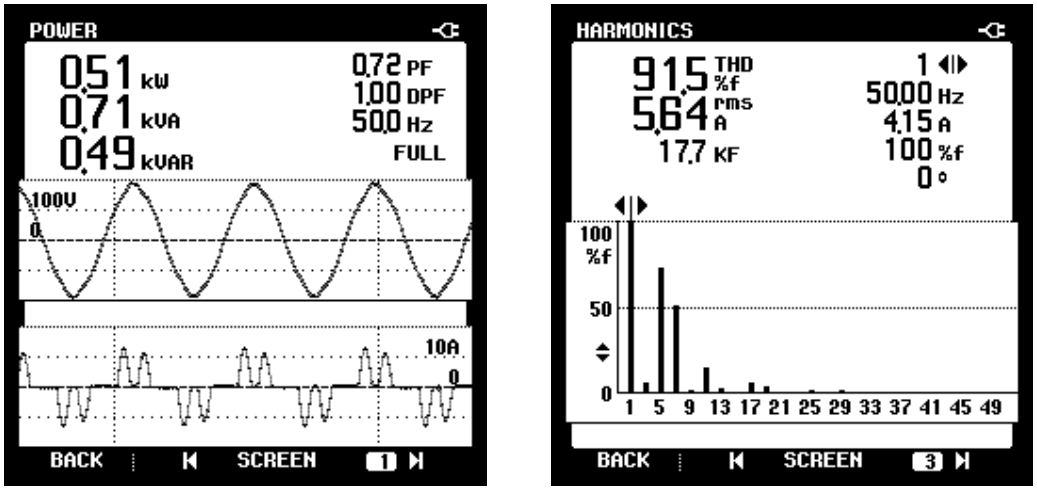


Fig. 3.14 Top view of the hardware prototype without the motor load

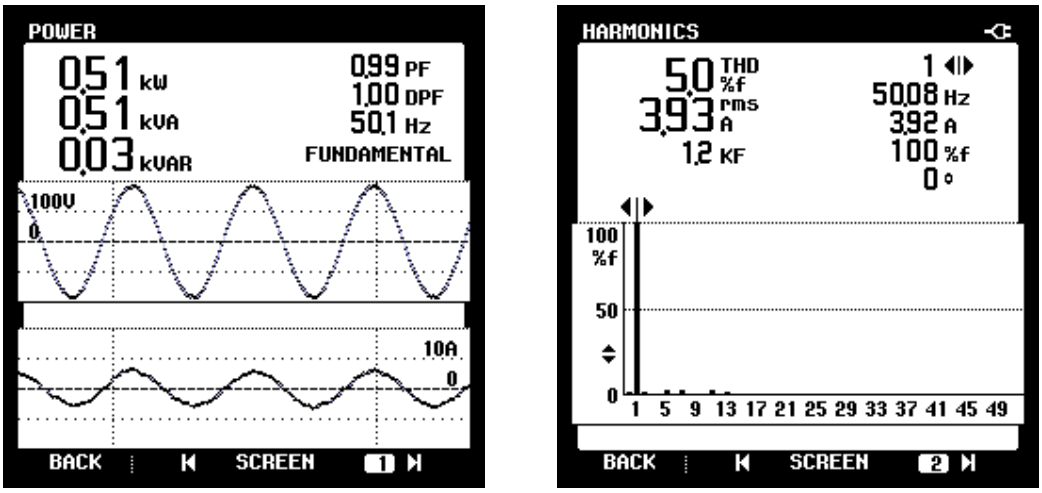
A commercial rectifier-inverter structure (Yaskawa VS-606V7 series, compact general-purpose inverter, without input inductors) was also used to obtain the input power factor and input current THD. This was done to obtain a realistic comparison between the developed prototype, and its commercial counterpart without power factor improvements.

The input power factor, as well as the input current THD of the commercial converter at 1.5 kW output power can be seen in Fig. 3.15, while those of the developed prototype are shown in Fig. 3.16. Fluke-43 power quality analyzer with online numerical value illustration is used to monitor the waveforms. The input PF is shown online at the upper right-hand side of Fig. 3.15 (a) and Fig. 3.16 (a). Prior to improvement, the input current THD and power factor was 91.5% and 0.72 respectively. The proposed scheme is able to improve the input current THD to 5.0% and the input power factor to 0.99. There is a remarkable improvement in power factor and THD. The experimental results agree with the MATLAB predicted ones calculated based on the waveforms in Fig. 3.10 and Fig. 3.11.



(a) Input current and voltage (b) Current FFT

Fig. 3.15 Input current and voltage and current FFT of a typical commercial converter



(a) Input current and voltage (b) Current FFT

Fig. 3.16 Input current and voltage and current FFT of the proposed prototype at rated load

Fig.3.17 shows the voltage across the IGBT of the bidirectional switch and the current through the bidirectional switch. Notice that there are no voltage overshoots during the on-off transition. This allows the IGBT to be used without snubber circuits. Hence, this converter is cheaper, simpler and easier to build. For 1.49 kW rectifier dc link power, the measured ac input power of the proposed scheme was 1.54 kW, resulting an efficiency of 96.8%. The rear-end converter output phase to neutral voltage and phase current are shown in Fig. 3.18.

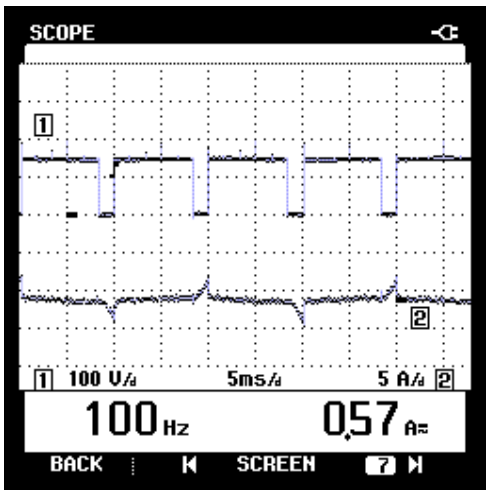


Fig. 3.17 Voltage across IGBT (trace 1) and bidirectional switch current (trace 2)

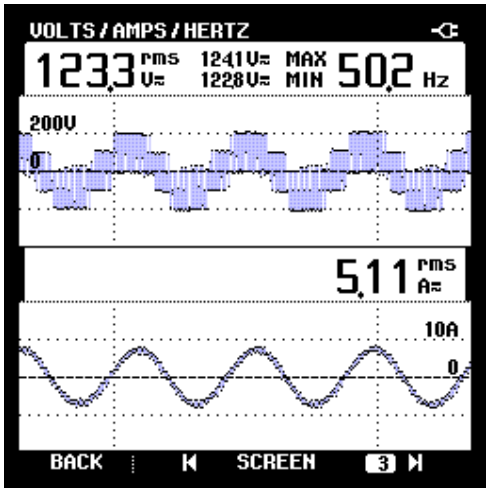
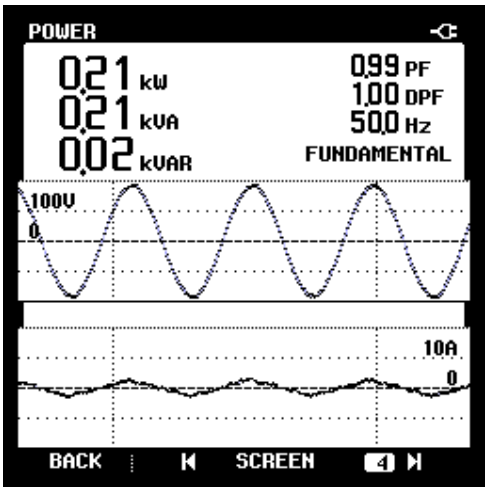
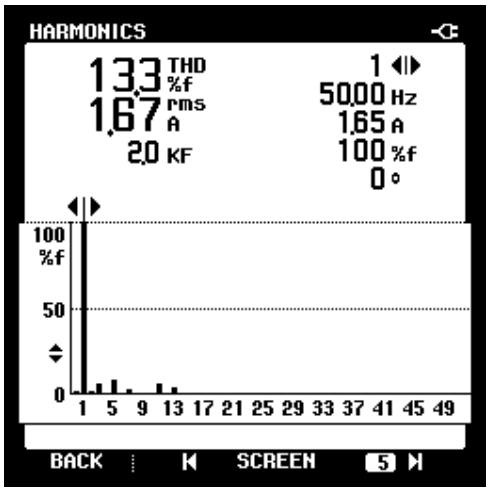


Fig. 3.18 Inverter output phase to neutral voltage and current

At 40% rated load, the proposed converter input current and voltage and current spectrum are shown in the Fig. 3.19. The converter input current THD is 13.3% and input PF is 0.99. At 120% of rated load, the proposed converter input current and voltage and current spectrum are shown in the Fig. 3.20. The converter input current THD and input PF are 5.5% and 0.99 respectively.

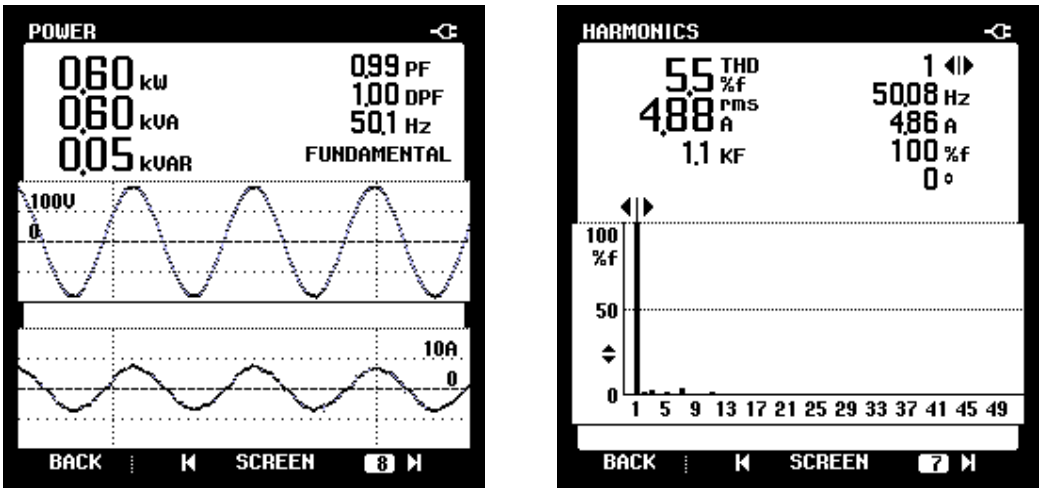


(a) Input current and voltage



(b) Current FFT

Fig. 3.19 Converter input current and voltage and current FFT at 40% rated load



(a) Input current and voltage (b) Current FFT

Fig. 3.20 Converter input current and voltage and current FFT at 120% rated load

The controller maintains the dc link voltage variation within 3% of its rated value throughout its operation. And the conduction angle α at different load conditions is shown in Fig. 3.21.

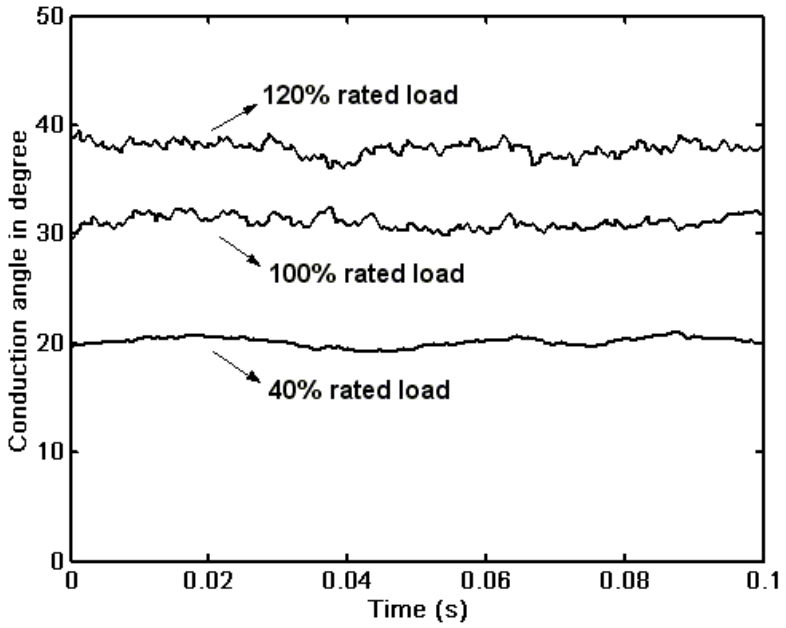


Fig. 3.21 Variations in bidirectional switch conduction angles (α) at different load conditions

3.4 Effects of unbalanced supply on the rectifier-inverter structure

In practice, the three-phase supply voltage can be unbalanced for various reasons. The converter characteristics and the quality of the input current get worse with the increase of unbalance [76]. In recent years, the use of static converters (ac-dc and ac-ac) has been seen a sharp increase in industrial applications. These converters are nonlinear in nature, and as a consequence, harmonic currents are injected into the ac mains. Therefore, the input power factor of these converters is usually poor and changes with load.

Most electrical systems are designed based on the assumption that the three-phase supply is symmetrical and at the fundamental frequency of 50/60 Hz. With proper design, the performance of forced commutated converter under unbalanced supply could be improved [76, 77]. However, three-phase diode rectifiers with capacitive filters are highly sensitive to supply voltage unbalance, drawing significant unbalanced line current even under slightly unbalanced voltage condition [78, 79].

The American National Standards Institute (ANSI) standard C84.1-1995 recommends that electrical supply systems should be designed and operated to limit the maximum voltage unbalance to 3% when measured at the electric-utility revenue meter under no-load conditions. And the International Electrotechnical Commission (IEC) recommends that the maximum voltage unbalance of electrical supply systems be limited to 2% [80]. The developed rectifier-inverter ac drive structure is connected to an unbalanced three-phase supply with 10% unbalance to test its performance.

If the supply phase voltages are assumed as V_{an}, V_{bn} and V_{cn}, their corresponding zero, positive and negative sequence can be expressed as:

$$V_0 = \frac{V_{an} + V_{bn} + V_{cn}}{3} \tag{3-19}$$

$$V_p = \frac{V_{an} + a \cdot V_{bn} + a^2 \cdot V_{cn}}{3} \tag{3-20}$$

$$V_n = \frac{V_{an} + a^2 \cdot V_{bn} + a \cdot V_{cn}}{3} \tag{3-21}$$

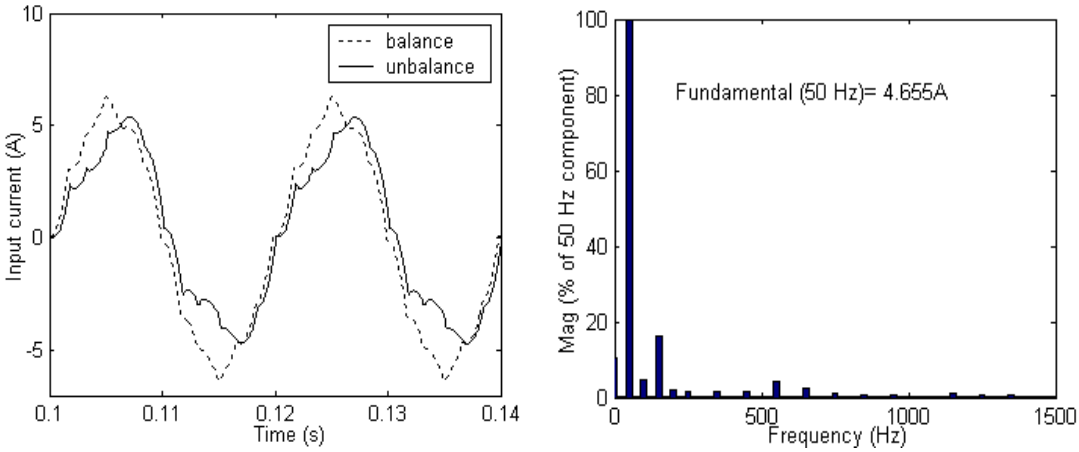
where $a = 1\angle 120°$ and $a^2 = 1\angle 240°$. The unbalance factor u can be defined as [64, 69]:

$$u = \frac{|V_n|}{|V_p|} \tag{3-22}$$

The specification of 10% unbalance supply is chosen as follows: phase 'a' 127 V (1 p.u.), phase 'b' 108 V (0.85 p.u.) and phase 'c' 152 V (1.20 p.u.)

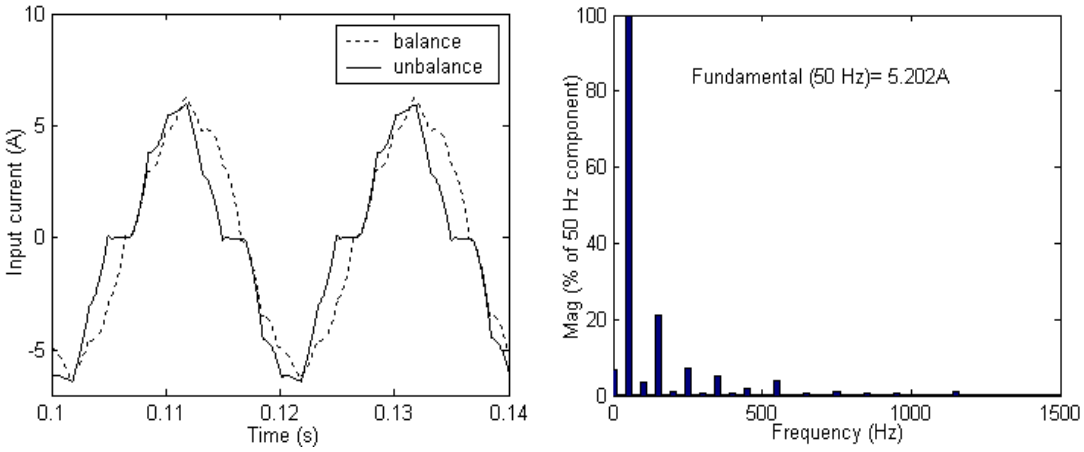
3.4.1 Simulation results

Through MATLAB SIMULINK modeling, the phase 'a' input current waveform (solid line) and its FFT are shown in Fig. 3.22, where the dashed line is the corresponding current waveform under balanced supply conditions. The same waveforms for phase 'b' and 'c' are shown in Fig. 3.23 and Fig. 3.24 respectively.



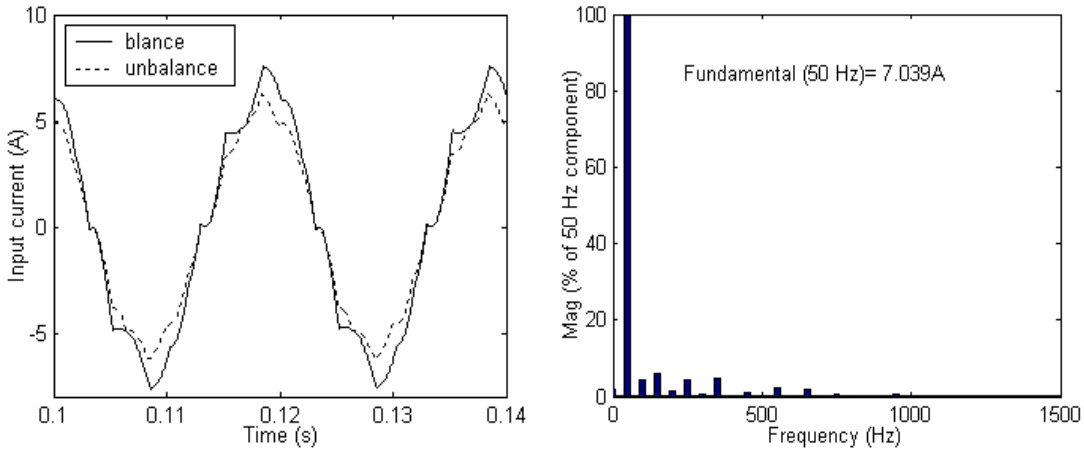
(a) Input current (b) Current FFT

Fig. 3.22 Phase 'a' current waveform and its FFT under 10% unbalanced supply



(a) Input current (b) Current FFT

Fig. 3.23 Phase 'b' current waveform and its FFT under 10% unbalanced supply



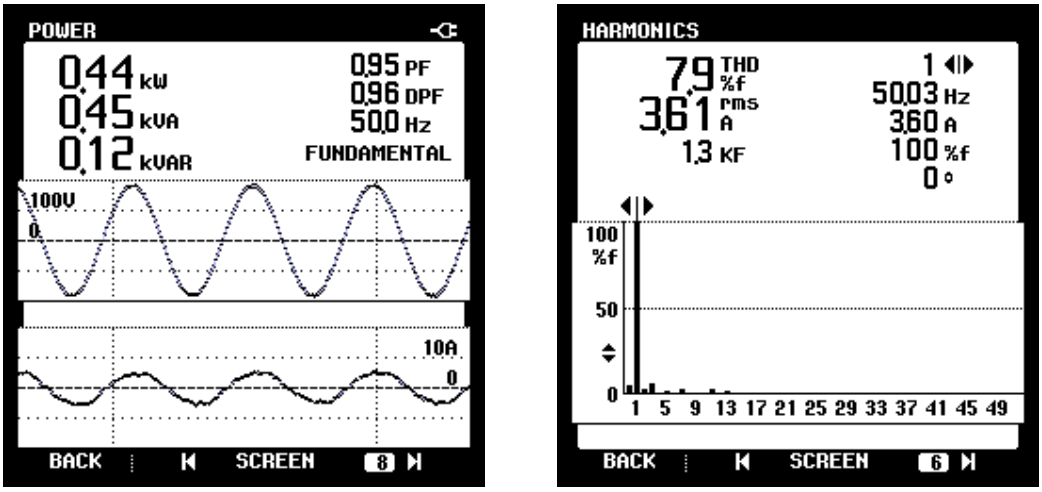
(a) Input current (b) Current FFT

Fig. 3.24 Phase 'c' current waveform and its FFT under 10% unbalanced supply

3.4.2 Experimental results

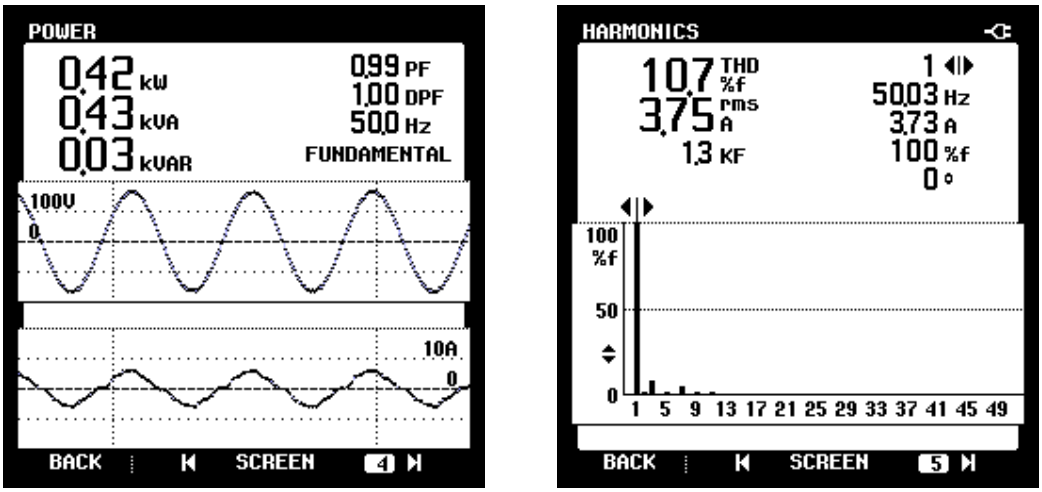
The current waveforms for phase 'a', both in the time and frequency domain are shown in Fig. 3.25, while those of phase 'b' are shown in Fig. 3.26. The corresponding waveforms for phase 'c' are shown in Fig. 3.27.

The supply voltage of course causes deterioration in the input power factor and input current THD of the rectifier-inverter structure. However, this deterioration is not significant, and the proper operation of the converter has not been impaired. The input current THD for all three phases is below 10.7% and the input power factor is above 0.95. It is evident that the converter is still able to perform well even when the supply voltage is slightly unbalanced.



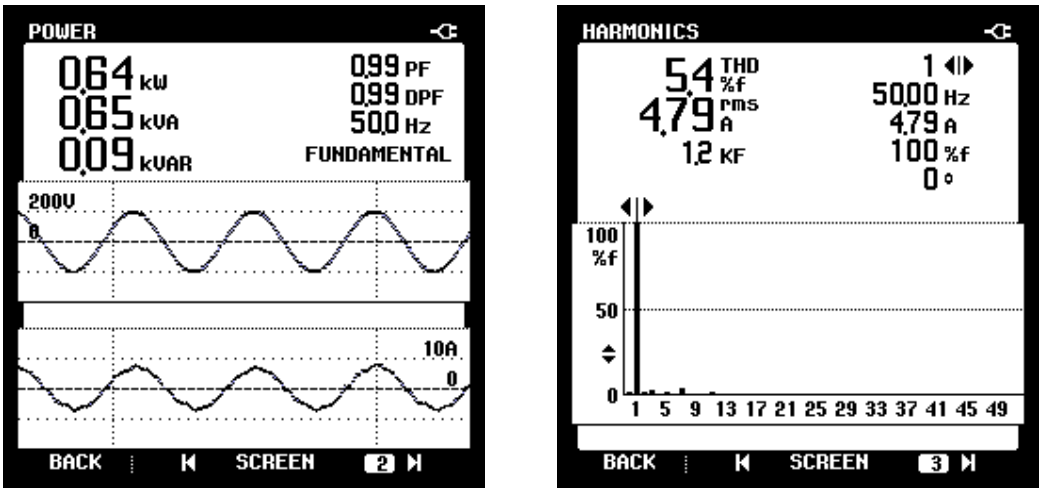
(a) Time domain (b) Frequency domain

Fig. 3.25 Phase 'a' current under 10% unbalanced supply



(a) Time domain (b) Frequency domain

Fig. 3.26 Phase 'b' current under 10% unbalanced supply



(a) Time domain (b) Frequency domain

Fig. 3.27 Phase 'c' current under 10% unbalanced supply

3.5 Concluding remarks

For mid to high power ac motor drives, traditional converter input power factor can be poor especially at low motor speeds. Passive filters or 12-pulse topology for the front-end converter only adds to its heavy weight and complexity.

Based on a recently developed rectifier power factor correction technique, a novel rectifier is proposed and is verified to be efficient and functional over a wide operating range. A prototype of the converter has been designed, built and tested. It shows the characteristics of simplicity and high efficiency. Through the use of this new method, a highly efficient and low cost rectifier-inverter can be easily built to operate within a wide load range i.e., from 40% to 120% rated load with power factor above 0.99. It also exhibits good performances, even with a large variation of the input line inductances and unbalanced supply voltage. The proposed bidirectional switch along with its controller is also a good power factor correction retrofit to the front-end converters of the existing ac drives. With these features, the proposed converter will be an excellent energy saver and a power factor enhancer required in a clean power environment.

Chapter 4

High Frequency Controlled Near Unity Power Factor Input Stage

4.1 Introduction

In their bench mark work, Mehl and Barbi [15] proposed a method to improve the input power factor of a three-phase diode rectifier with three additional bidirectional switches operating at a low switching frequency, as shown in Fig. 3.1. Each bidirectional switch is turned on when corresponding phase voltage crosses zero-volt point and conducts for 1/12 of line voltage cycle. Thus the input current waveform is well shaped and approximately sinusoidal with input current THD as low as 6.6% and power factor as high as 0.99. However, the input inductance required to obtain such result is usually large (determined by the input line voltage V_L, line frequency f and rated output power P_o as dictated by (3-2)). This technique was proposed for the rectifier operating with a fixed load and fixed 'optimal' input inductor [74]. Therefore, the dc link voltage is sensitive to the load variation and good performance is achieved within a very limited output power range.

Based on the same structure, a novel control strategy that takes into account actual load level on the rectifier was proposed in Chapter 3. With this method, high performance can be achieved within a wide output power range. This is possible due to the controller's intelligence in determining appropriate conduction times for different bidirectional switches. However, this method is especially suitable for mid to high power applications due to the requirement of larger input inductance for low power converters. For example, the required optimal input inductance is around 4 mH for a prototype rated 8 kW while 24 mH for a 1.5 kW rated one. This can result in a bulky and impractical structure for low power converter. With more importance on power quality, an efficient unity power factor drive required for low to mid power level ac motors is growing.

The key approach to reduce the converter input inductance requirement is to operate the bidirectional switches at high switching frequency. The topology works as a three-phase three-level VIENNA Rectifier [84]. In this chapter the converter is first described with detailed mathematic model under high switching frequency control. And this three-phase front-end rectifier capable of sustaining sinusoidal input currents in phase with their corresponding input phase voltage, and performing a wide dc link voltage regulation is also analyzed and presented.

However, under real operation conditions not only the unbalance, but also the distortion in supply voltage may be frequent, particularly in a weak ac system. The research of high frequency controlled input stage for unity power factor ac drive is also extended to unbalanced and distorted supply conditions. Thus a unity power factor converter using the synchronous reference frame based hysteresis current control (HCC) is proposed. With the proposed control algorithm, the converter draws high quality sinusoidal supply currents and maintains good dc link voltage regulation under wide load variation, and even under unbalanced and nonsinusoidal supply voltage conditions.

4.2 A near unity power factor rectifier with hysteresis current control

Hysteresis current control technique is adopted for the front-end rectifier bidirectional switches as shown in Fig. 4.1.

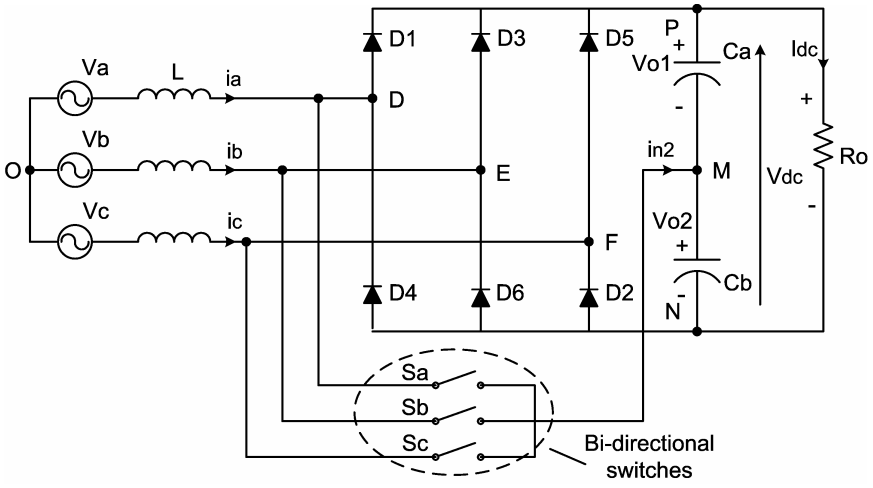


Fig. 4.1 Three-phase diode rectifier with bidirectional switches

It makes use of continuous conduction of the input current and operates with unity input power factor. The idea lies in high switching frequency, resulting in the input inductor size to be effectively reduced. The converter has characteristics of unity input power factor, high output voltage, wide output power capability, simplicity and robustness.

4.2.1 Analysis and model of the rectifier

The power circuit of the rectifier is shown in Fig. 4.1. For phase 'a', the following expression is valid:

$$L\frac{di_a}{dt} = v_a - (v_{DN} + v_{NO}) \tag{4-1}$$

where v_{DN} is the voltage between point D and N, and v_{NO} is the voltage of point N referred to neutral point O. s_a, s_b and s_c denote the switching states for switches Sa, Sb and Sc respectively. $s_a = 1$ signifies for switch-on and $s_a = 0$ for switch-off of Sa. When Sa is off, one can get:

$$v_{DN} = \begin{cases} v_{o1} + v_{o2} & (i_a > 0) \\ 0 & (i_a < 0) \end{cases} \tag{4-2}$$

And when Sa is on,

$$v_{DN} = v_{o2} \tag{4-3}$$

From (4-2) and (4-3), the voltage v_{DN} can be expressed as:

$$v_{DN} = v_{o2}s_a + (1 - s_a)sign(i_a)(v_{o1} + v_{o2}) \tag{4-4}$$

where,

$$sign(i_a) = \begin{cases} 1, & i_a > 0 \\ 0, & i_a < 0 \end{cases} \tag{4-5}$$

Therefore, (4-1) becomes:

$$L\frac{di_a}{dt} = v_a - v_{o2}s_a - (1-s_a)sign(i_a)(v_{o1}+v_{o2}) - v_{NO} \tag{4-6}$$

Similarly, for phase b and c:

$$L\frac{di_b}{dt} = v_b - v_{o2}s_b - (1-s_b)sign(i_b)(v_{o1}+v_{o2}) - v_{NO} \tag{4-7}$$

$$L\frac{di_c}{dt} = v_c - v_{o2}s_c - (1-s_c)sign(i_c)(v_{o1}+v_{o2}) - v_{NO} \tag{4-8}$$

For the balanced three-phase system, v_{NO} can be obtained by adding (4-6) to (4-8) together:

$$\begin{aligned} v_{NO} = &-\frac{v_{o1}}{3}(1-s_a)sign(i_a) - \frac{v_{o2}}{3}[s_a + (1-s_a)sign(i_a)] \\ &-\frac{v_{o1}}{3}(1-s_b)sign(i_b) - \frac{v_{o2}}{3}[s_b + (1-s_b)sign(i_b)] \\ &-\frac{v_{o1}}{3}(1-s_c)sign(i_c) - \frac{v_{o2}}{3}[s_c + (1-s_c)sign(i_c)] \end{aligned} \tag{4-9}$$

Thus, (4-6), (4-7) and (4-8) can be rewritten as:

$$\begin{cases} L\dfrac{di_a}{dt} = v_a + v_{o1}a_1 + v_{o2}a_2 \\ L\dfrac{di_b}{dt} = v_b + v_{o1}b_1 + v_{o2}b_2 \\ L\dfrac{di_c}{dt} = v_c + v_{o1}c_1 + v_{o2}c_2 \end{cases} \tag{4-10}$$

where, x_1 denotes a_1, b_1 and c_1; x_2 denotes a_2, b_2 and c_2.

$$\begin{cases} x_1 = [-(1-s_x)sign(i_x) + \dfrac{1}{3}(1-s_a)sign(i_a) + \dfrac{1}{3}(1-s_b)sign(i_b) + \dfrac{1}{3}(1-s_c)sign(i_c)]v_{o1} \\ x_2 = [-(1-s_x)sign(i_x) + \dfrac{1}{3}(1-s_a)sign(i_a) + \dfrac{1}{3}(1-s_b)sign(i_b) + \dfrac{1}{3}(1-s_c)sign(i_c)]v_{o2} \\ \quad + [-s_x + \dfrac{1}{3}(s_a + s_b + s_c)]v_{o2} \qquad x = a,b,c \end{cases}$$

(4-11)

For the circuit of Fig. 4.1, further two equations can be expressed as:

$$C_a \frac{dv_{o1}}{dt} = i_a d_1 + i_b d_2 - (v_{o1} + v_{o2})/R_o \tag{4-12}$$

$$C_b \frac{dv_{o2}}{dt} = i_a e_1 + i_b e_2 - (v_{o1} + v_{o2})/R_o \tag{4-13}$$

where,

$$\begin{cases} d_1 = (1-s_a)sign(i_a) - (1-s_c)sign(i_c) \\ d_2 = (1-s_b)sign(i_b) - (1-s_c)sign(i_c) \\ e_1 = -(1-s_a)[1-sign(i_a)] + (1-s_c)[1-sign(i_c)] \\ e_2 = -(1-s_b)[1-sign(i_b)] + (1-s_c)[1-sign(i_c)] \end{cases} \tag{4-14}$$

4.2.2 Hysteresis current control principle

The bidirectional switches shown in Fig. 4.1 are controlled with hysteresis current control (HCC) technique. In the balanced three-phase system and unity power factor operation, the three-phase voltage (v_a, v_b, v_c) and reference current ($i_{refa}, i_{refb}, i_{refc}$) are expressed as:

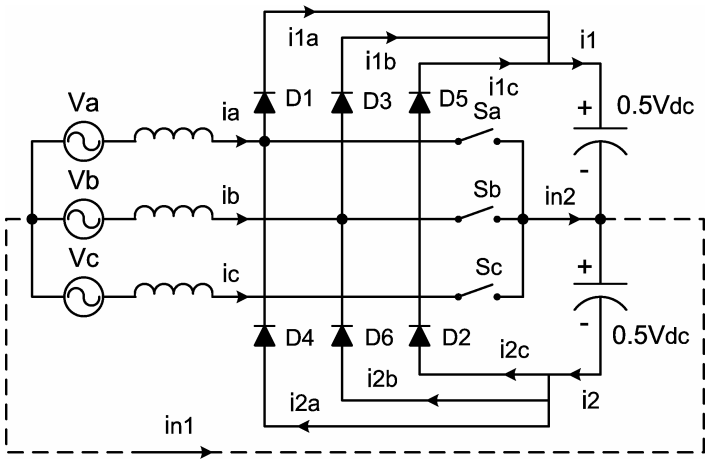
$$\begin{cases} v_a = \sqrt{2}V_p \sin \omega t \\ v_b = \sqrt{2}V_p \sin(\omega t - \frac{2\pi}{3}) \\ v_c = \sqrt{2}V_p \sin(\omega t + \frac{2\pi}{3}) \end{cases} \tag{4-15}$$

$$\begin{cases} i_{refa} = \sqrt{2}I_{ref} \sin \omega t \\ i_{refb} = \sqrt{2}I_{ref} \sin(\omega t - \frac{2\pi}{3}) \\ i_{refc} = \sqrt{2}I_{ref} \sin(\omega t + \frac{2\pi}{3}) \end{cases} \tag{4-16}$$

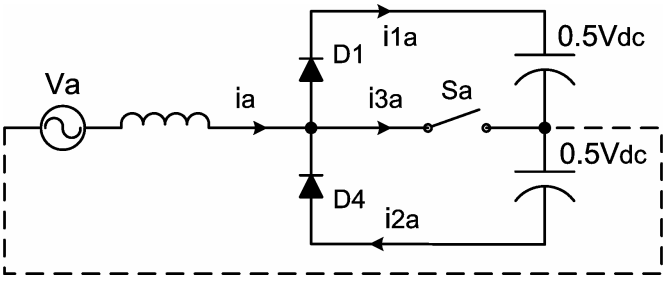
Where V_P and I_{ref} are the rms value of supply phase to neutral voltage and the rms value of the supply current. The diode D1, D3 and D5 conduct when corresponding phase

voltage is in positive half cycle and the bidirectional switch is in switched-off state. Similarly, the diodes D4, D6 and D2 conduct when corresponding phase voltage is in negative half cycle and the bidirectional switch is also in switched-off state.

In order to prove the instantaneous power balance between ac source and dc bus, the local average method is adopted [85-89]. The operation of the three-phase rectifier with bidirectional switches shown in Fig. 4.2 (a) can be described in the form of three single-phase circuits, one of which is shown in Fig. 4.2 (b). The line between three-phase neutral point and capacitor middle point does not really exist. It is used for better description of the rectifier operation principle and depicted with dashed line.



(a) Equivalent circuit of three-phase module



(b) Single phase equivalent circuit

Fig. 4.2 Equivalent circuit of three-phase diode rectifier with bidirectional switches

Using the hysteresis current control technique, the phase 'a' current i_a is controlled to track the reference current within the window width I_w as shown in Fig. 4.3.

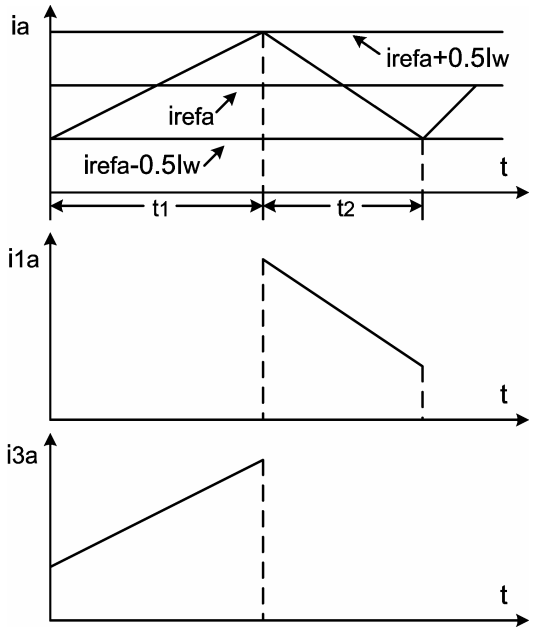


Fig. 4.3 Currents within one switching period: phase 'a' current being switched between upper and lower bounds to track the reference current (upper trace); diode D_1 current (mid trace); bidirectional switch Sa current (lower trace).

A. Operation during the positive interval of i_{refa}

For the period $0 < t < t_1$, the supply current i_a flows through bidirectional switch Sa, rising from $i_{refa} - 0.5I_w$ to $i_{refa} + 0.5I_w$. For the period $t_1 < t < (t_1 + t_2)$, the switch Sa is off and the current in the input inductor is continued through the rectifier diode D1. It is assumed the time period $t_1 + t_2$ is so brief that i_{refa} is substantially constant.

The current i_{1a} of D1 and the current i_{3a} of Sa are shown in Fig. 4.3. The local average current $\hat{i}_{1a}$ and $\hat{i}_{3a}$ are:

$$\hat{i}_{1a} = \frac{\int_{t_1}^{t_1+t_2} i_{refa}\,dt}{t_1 + t_2} \approx \frac{i_{refa} t_2}{t_1 + t_2} \tag{4-17}$$

$$\hat{i}_{3a} = \frac{i_{refa} t_1}{t_1 + t_2} \tag{4-18}$$

When the bidirectional switch Sa is on, the corresponding equation is

$$L\frac{di_a}{dt} = v_a \tag{4-19}$$

The phase 'a' current i_a rises from $i_{refa} - 0.5I_w$ to $i_{refa} + 0.5I_w$ within the transit time t_1 and (4-19) can be represented as

$$L\frac{I_w}{t_1} = v_a \tag{4-20}$$

Then t_1 can be obtained as

$$t_1 = \frac{LI_w}{v_a} \tag{4-21}$$

When bidirectional switch Sa is switched off and diode D1 is on, phase 'a' current i_a falls from $i_{refa} + 0.5I_w$ to $i_{refa} - 0.5I_w$ within the transit time t_2.

$$L\frac{di_a}{dt} = v_a - 0.5V_{dc} \tag{4-22}$$

And based on (4-22)

$$t_2 = \frac{LI_w}{0.5V_{dc} - v_a} \tag{4-23}$$

where $0.5V_{dc} > v_a$. If $0.5V_{dc} < v_a$, the phase a current cannot be well limited in the hysteresis boundary and the rectifier fails to achieve high power factor goal. Substituting (4-21) and (4-23) into (4-17), the local average current $\hat{i}_{1a}$ can be obtained:

$$\hat{i}_{1a} = \frac{2v_a}{V_{dc}} i_{refa} \tag{4-24}$$

During the positive interval of reference current i_{refa}, diode D4 is reverse-biased and the current through it is zero.

B. Operation during the negative interval of i_{refa}

At this condition, the phase 'a' voltage is in negative half cycle. Diode D1 is reverse-biased and the phase 'a' current will flow through diode D4. It is similar to the operation of positive interval of i_{refa}.

The local average current of $\hat{i}_{2a}$ is

$$\hat{i}_{2a} = \frac{2v_a}{V_{dc}} i_{refa} \tag{4-25}$$

Using the similar analysis, the local average currents of phase 'b' and phase 'c' can be obtained as

$$\hat{i}_{1b} = \begin{cases} \dfrac{2v_b}{V_{dc}} i_{refb} & (i_{refb} \geq 0) \\ 0 & (i_{refb} < 0) \end{cases} \tag{4-26}$$

$$\hat{i}_{2b} = \begin{cases} 0 & (i_{refb} \geq 0) \\ \dfrac{2v_b}{V_{dc}} i_{refb} & (i_{refb} < 0) \end{cases} \tag{4-27}$$

$$\hat{i}_{1c} = \begin{cases} \dfrac{2v_c}{V_{dc}} i_{refc} & (i_{refc} \geq 0) \\ 0 & (i_{refc} < 0) \end{cases} \tag{4-28}$$

$$\hat{i}_{2c} = \begin{cases} 0 & (i_{refc} \geq 0) \\ \dfrac{2v_c}{V_{dc}} i_{refc} & (i_{refc} < 0) \end{cases} \tag{4-29}$$

The upper dc link current $\hat{i}_1$, the sum of the upper diodes current $\hat{i}_{1a}$, $\hat{i}_{1b}$ and $\hat{i}_{1c}$, is given as (4-30).

$$\hat{i}_1 = \begin{cases} \frac{2v_a}{V_{dc}} i_{refa} + \frac{2v_c}{V_{dc}} i_{refc} & (0 < \omega t < \pi/3) \\ \frac{2v_a}{V_{dc}} i_{refa} & (\pi/3 < \omega t < 2\pi/3) \\ \frac{2v_a}{V_{dc}} i_{refa} + \frac{2v_b}{V_{dc}} i_{refb} & (2\pi/3 < \omega t < \pi) \\ \frac{2v_b}{V_{dc}} i_{refb} & (\pi < \omega t < 4\pi/3) \\ \frac{2v_b}{V_{dc}} i_{refb} + \frac{2v_c}{V_{dc}} i_{refc} & (4\pi/3 < \omega t < 5\pi/3) \\ \frac{2v_c}{V_{dc}} i_{refc} & (5\pi/3 < \omega t < 2\pi) \end{cases} \tag{4-30}$$

The lower dc link current $\hat{i}_2$, the sum of the lower diodes current $\hat{i}_{2a}$, $\hat{i}_{2b}$ and $\hat{i}_{2c}$, is given as (4-31).

$$\hat{i}_2 = \begin{cases} \frac{2v_b}{V_{dc}} i_{refb} & (0 < \omega t < \pi/3) \\ \frac{2v_b}{V_{dc}} i_{refb} + \frac{2v_c}{V_{dc}} i_{refc} & (\pi/3 < \omega t < 2\pi/3) \\ \frac{2v_c}{V_{dc}} i_{refc} & (2\pi/3 < \omega t < \pi) \\ \frac{2v_a}{V_{dc}} i_{refa} + \frac{2v_c}{V_{dc}} i_{refc} & (\pi < \omega t < 4\pi/3) \\ \frac{2v_a}{V_{dc}} i_{refa} & (4\pi/3 < \omega t < 5\pi/3) \\ \frac{2v_a}{V_{dc}} i_{refa} + \frac{2v_b}{V_{dc}} i_{refb} & (5\pi/3 < \omega t < 2\pi) \end{cases} \tag{4-31}$$

The total instantaneous dc link power p_{dc} is

$$p_{dc} = \hat{i}_1 \frac{V_{dc}}{2} + \hat{i}_2 \frac{V_{dc}}{2} = v_a i_{refa} + v_b i_{refb} + v_c i_{refc} \tag{4-32}$$

In the balanced three-phase system and unity power factor operation without considering the losses, one can get the following relationship from (4-15), (4-16) and (4-32)

$$p_{dc} = 3V_p I_{ref} = p_{ac} \tag{4-33}$$

On the other hand, the ac supply instantaneous power is equal to the dc link power. The reference supply current under unity power factor can be obtained as

$$I_{ref} = \frac{V_{dc} I_{dc}}{3V_p} \tag{4-34}$$

where V_{dc} and I_{dc}, as shown in Fig. 4.1, are the dc link voltage and current respectively. It is evident from the equation above that when there is a variation on the load, the reference current can be adjusted by the output power estimator and dc link voltage regulator.

In the balanced three phase system, the ac side neutral current i_{n1} (ref. to Fig. 4.2 (a) and (4-16)) is given by:

$$i_{n1} = \sqrt{2} I_{ref} [\sin \omega t + \sin(\omega t - \frac{2\pi}{3}) + \sin(\omega t + \frac{2\pi}{3})] = 0 \tag{4-35}$$

As a consequence, the conductor connecting the neutral of the three-phase voltage to the central tap of the dc link in Fig. 4.2 (a) can be removed. Substituting (4-15), (4-16) and (4-34) to (4-30) one can get

$$\hat{i}_1 = I_{dc} \left[1 - \frac{1}{3} \sin(3\omega t) \right] \tag{4-36}$$

Similarly, $\hat{i}_2$ is given as

$$\hat{i}_2 = I_{dc} \left[1 + \frac{1}{3} \sin(3\omega t) \right] \tag{4-37}$$

So the injection current $\hat{i}_{n2}$, which consists of the sum of currents through three bidirectional switches, is given as:

$$\hat{i}_{n2} = \hat{i}_2 - \hat{i}_1 = \frac{2I_{dc}}{3} \sin(3\omega t) \tag{4-38}$$

4.2.3 Evaluation of bidirectional switch ratings

Take phase 'a' as reference, (4-18), (4-21) and (4-23) can be used to calculate the bidirectional switch average current,

$$I_{sw(avg)} = \frac{1}{\pi}\int_0^{\pi} \hat{i}_{3a}\, d\omega t = \frac{2P_{dc}}{3V_p}\left(\frac{2}{\pi} - \frac{V_p}{V_{dc}}\right) \tag{4-39}$$

Similarly, the rms value of the bidirectional switch can be calculated as

$$I_{sw(rms)} = \sqrt{\frac{1}{\pi}\int_0^{\pi} (\hat{i}_{3a})^2\, d\omega t} = \frac{P_{dc}}{3V_p}\sqrt{1 - \frac{32\sqrt{2}}{3\pi}\left(\frac{V_p}{V_{dc}}\right) + 6\left(\frac{V_p}{V_{dc}}\right)^2} \tag{4-40}$$

Meanwhile, the voltage across the bidirectional switches is only half of the dc link voltage. Hence, low cost switching devices can be used.

4.2.3 Converter design and implementation

Fig. 4.4 shows the block diagram of the proposed control scheme. The bidirectional switches are controlled with hysteresis current control (HCC) technique to ensure sinusoidal input current with unity power factor and dc link voltage regulation.

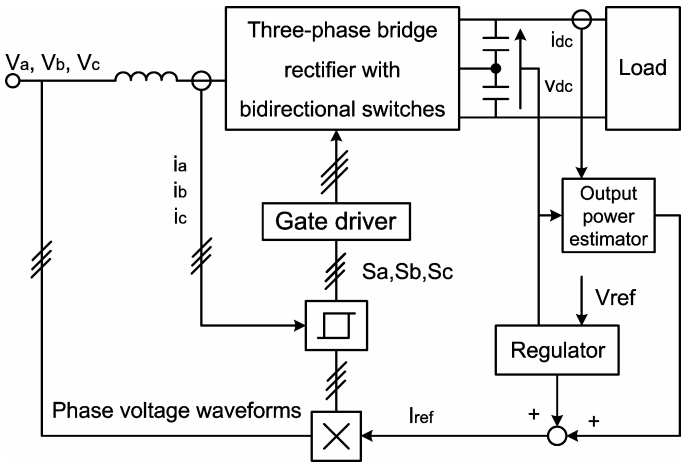


Fig. 4.4 Block diagram of bidirectional switches control scheme

Since the dc link voltage response lags the variation of load power, it becomes difficult to design proper control parameters to let such dc link voltage controller to fit any output operating condition [90]. In this proposed controller, the output power detection feed forward control as the main control loop, and dc link voltage regulator as the minor

control loop are adopted [91, 92]. For balancing the active power flow between the ac source and load, the magnitude of the reference current is generated by the sum of signals from the dc link voltage regulator and the output power estimator which guaranties stable operation in any conditions. This utilizes the three phase voltages to get the synchronized input reference currents. Three input phase currents and corresponding reference currents are sent to the hysteresis current comparator to generate the proper switching signals for three-phase bidirectional switches Sa, Sb and Sc.

The switching signals s_x (x=a, b, c) of the bidirectional switches are given by (4-41).

$$s_x = \begin{cases} 1 & if\ (i_x > 0\ and\ i_x < i_x^* - h)\ or\ (i_x < 0\ and\ i_x > i_x^* + h) \\ 0 & if\ (i_x > 0\ and\ i_x > i_x^* + h)\ or\ (i_x < 0\ and\ i_x < i_x^* - h) \end{cases} \tag{4-41}$$

where h is the hysteresis band. Since the rectifier provides continuous conduction for the input currents, the current stresses on the switching devices are reduced. The switching pattern is illustrated by Fig. 4.5 for phase 'a'.

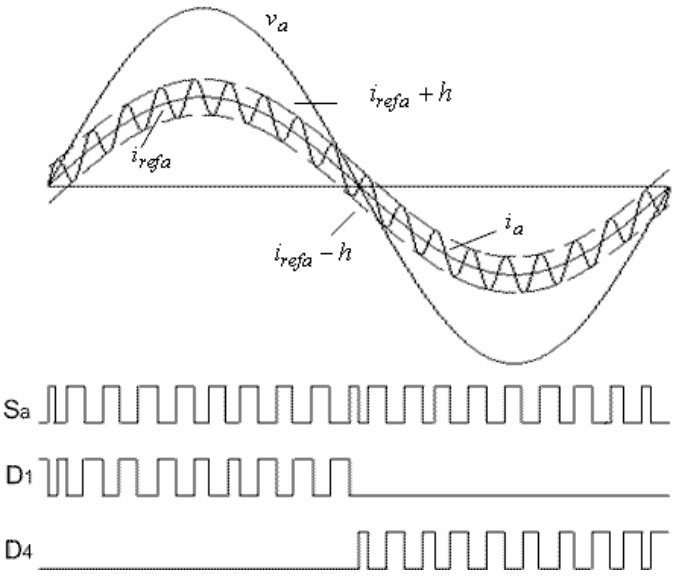


Fig. 4.5 Switching operation pattern of phase 'a': Sa for bidirectional switch, D1 and D4 for upper and lower bridge diodes respectively

When the rectifier is operating at high switching frequency, there's no special requirement for the input inductance L as compared to the critical input inductance in Chapter 3. Lower input inductance calls for higher switching frequency. If the line

inductance is too small, additional small inductance can be added to the input side of the rectifier. If the line inductance is high, no added inductance is required. A sinusoidal PWM (SPWM) voltage source inverter, a very popular topology in industry for ease of implementation and good harmonic profile, is connected to the rectifier for the intended rectifier-inverter structure as depicted in Fig. 4.6.

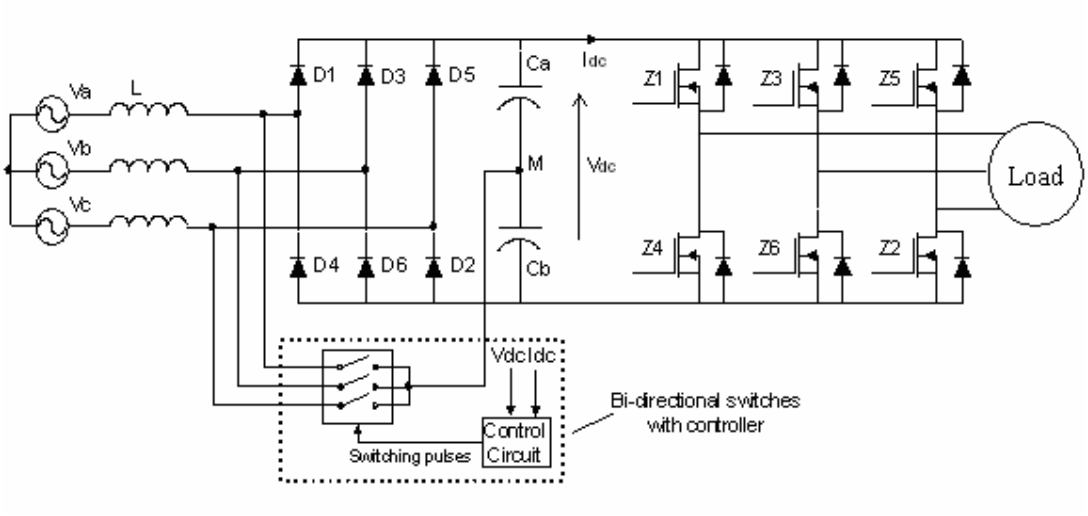


Fig. 4.6 Complete circuit diagram of the proposed near unity power factor converter

To illustrate the design feasibility of the proposed converter, a prototype with the following specification is chosen:

- Input line-to-line voltage 220 V;
- Dc link reference voltage 370 V (1.68 p. u.);
- Input inductance 5 mH (0.033 p. u.);
- Rated output power 1 kW;
- Current window: 10% of rated reference current.

Simulation results

A MATLAB/SIMULINK model for the proposed rectifier-inverter structure (converter) is developed to perform a digital simulation. Fig. 4.7 shows the converter input phase current waveform and its harmonic spectrum at rated output power operation. The converter input power factor is found to be 0.999 and input current THD 4.3%.

The voltage and current through the bidirectional switch at converter rated output power are shown in Fig. 4.8. The rms values of bidirectional switch voltage and current are 154.2 V and 1.01 A respectively. The bidirectional KVA rating is 15.6% of converter rated load, two times higher than that at low frequency operating condition mentioned in Chapter 3. This will inevitably result in a higher switching power loss and a lower efficiency of the converter. However, it may be still acceptable for converter at low to medium power operation.

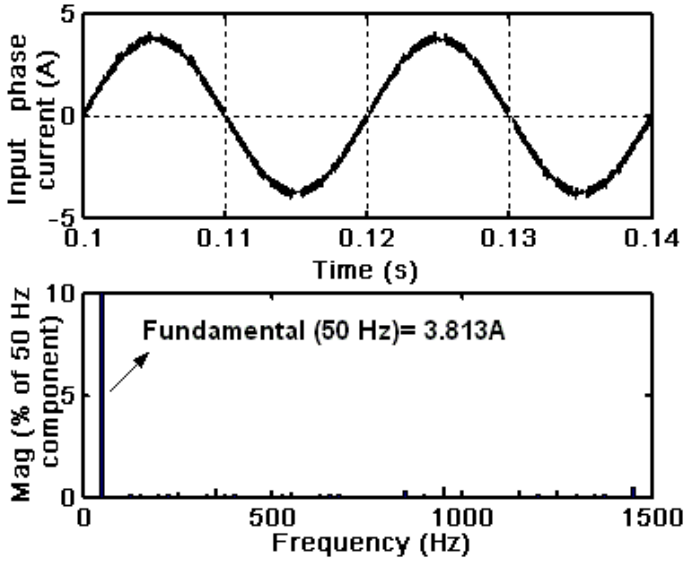


Fig. 4.7 Converter input current with harmonic spectrum at rated output power

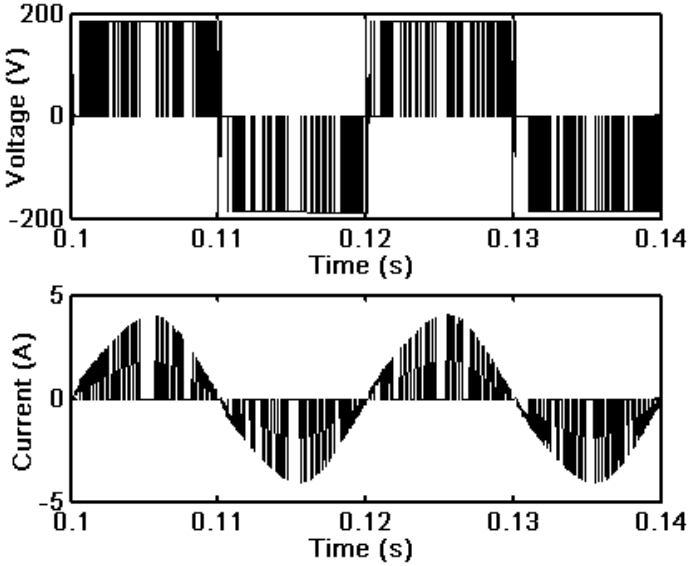


Fig. 4.8 Bidirectional switch voltage (upper trance) and current (lower trace)

In order to show the performance of the converter under varying load conditions, it is operated at below and above its rated value. The converter input phase current waveform and its harmonic spectrum at 50% rated output power are shown in Fig. 4.9. The converter input power factor is found to be 0.996 and input current THD 8.4%. The converter input phase current waveform and its harmonic spectrum at 150% rated output power are shown in Fig. 4.10. The converter input power factor is found to be 0.999 and input current THD 3.0%.

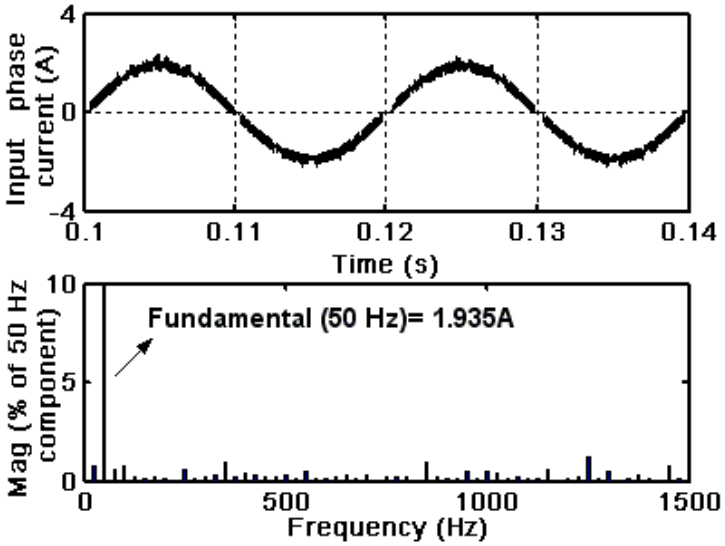


Fig. 4.9 Converter input current with harmonic spectrum at 50% rated output power

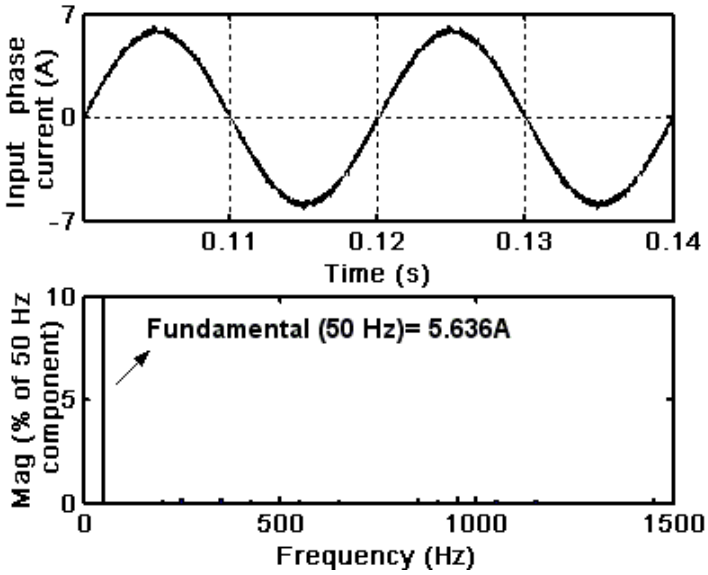


Fig. 4.10 Converter input current with harmonic spectrum at 150% rated output power

The variations of average switching frequency of the bidirectional switches under rated input inductance at various output power conditions are tabulated in Table 4.1. One can notice that the average switching frequency of the bidirectional switches changes little with load variations.

Table 4.1 Average switching frequency at various output power conditions

Load	50%P_o*	100%P_o	150%P_o
Switching frequency (kHz)	6.3	6.6	7.0

* P_o is the converter rated output power

In order to investigate its universality, the converter is also operated under various input inductances, since it was found to substantially change the input current harmonic spectrum in the previously proposed converters of [16, 74].

Table 4.2 gives the performance parameters with proposed method at rated load and under various input inductance conditions. It is found that the variation of input inductance does not change converter operation and the input power factor and input current harmonics are essentially the same. A reduction in input inductance leads to higher switching frequencies and as a result expected to yield higher switching losses. However, the maximum frequency and the consequent switching losses here will be acceptable especially at low power levels.

Table 4.2 Performance parameters under various input inductance conditions (rated load)

Input inductance (mH)	3	4	5	6	7
Input current THD	4.2%	4.2%	4.3%	4.2%	4.3%
Input power factor	0.999	0.999	0.999	0.999	0.999
Average switching frequency (kHz)	12.2	8.5	6.6	5.2	4.7

Fig. 4.11 illustrates the input phase currents and dc link voltage waveform when the converter output power demand changes instantaneously from 50% to 100% and then changes back to 50% of its rated value due to load disturbance. The load change was

initiated at 0.12s where the converter was in steady state and settled back at 0.13s. One can clearly see that the converter exhibits a good response to the sudden load variation. This illustrates the capability of the proposed controller to accommodate a sudden load torque change.

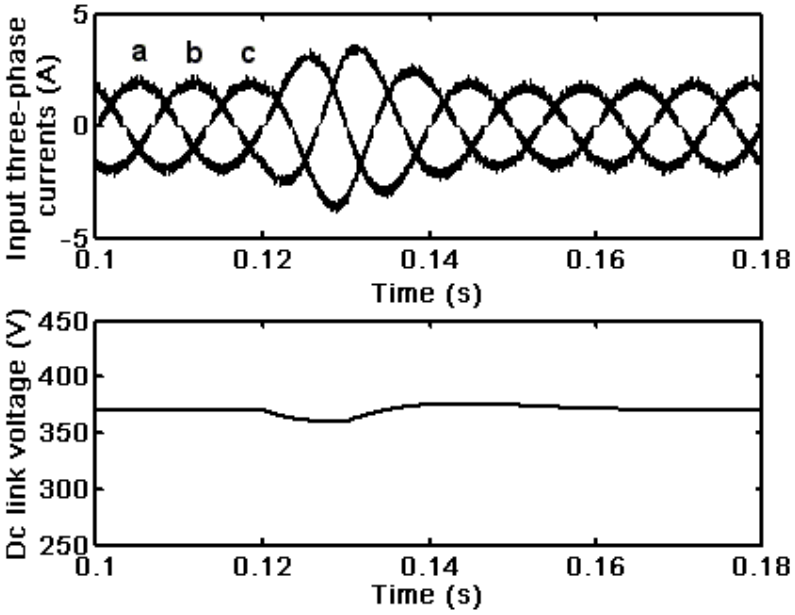


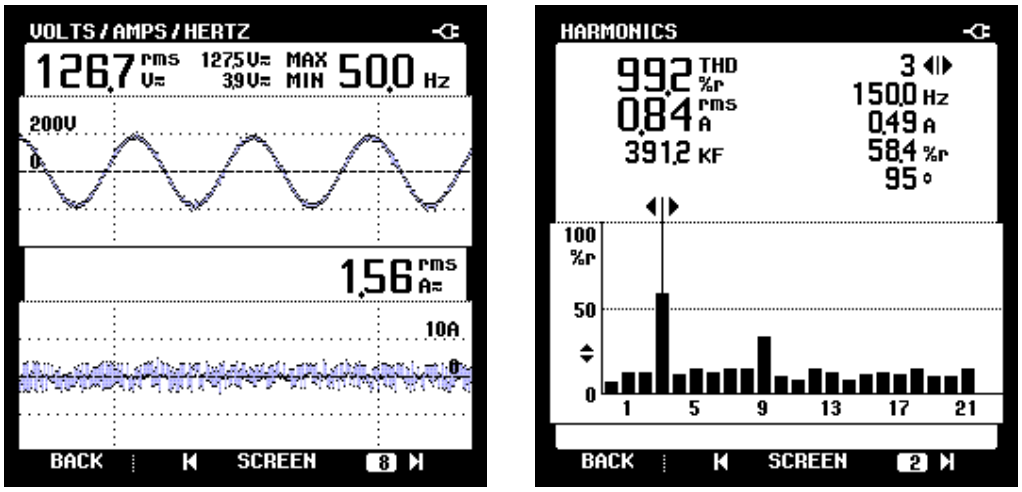
Fig. 4.11 Converter response to a sudden load change

Experiment results

The proposed control system is implemented using a single-board ds1103 microprocessor manufactured by dSPACE GmbH and developed under the integrated development environment of MATLAB-SIMULINK RTW provided by The MathWorks. The single board ds1103 is a real-time interface (RTI) including a PowerPC 604e processor and a TMS320F240 DSP microprocessor. The PowerPC 604e is the arithmetic operation kernel and TMS320F240 responds for special peripherals handling. A 1 kW hardware prototype of the rectifier-inverter structure as depicted in Fig. 4.6 was constructed and its performance is observed.

The injection current i_{n2} (ref. to Fig. 4.2 (a)), which is the sum of three bidirectional switch currents, is shown in the bottom trace of Fig. 4.12 (a). The spectrum of current

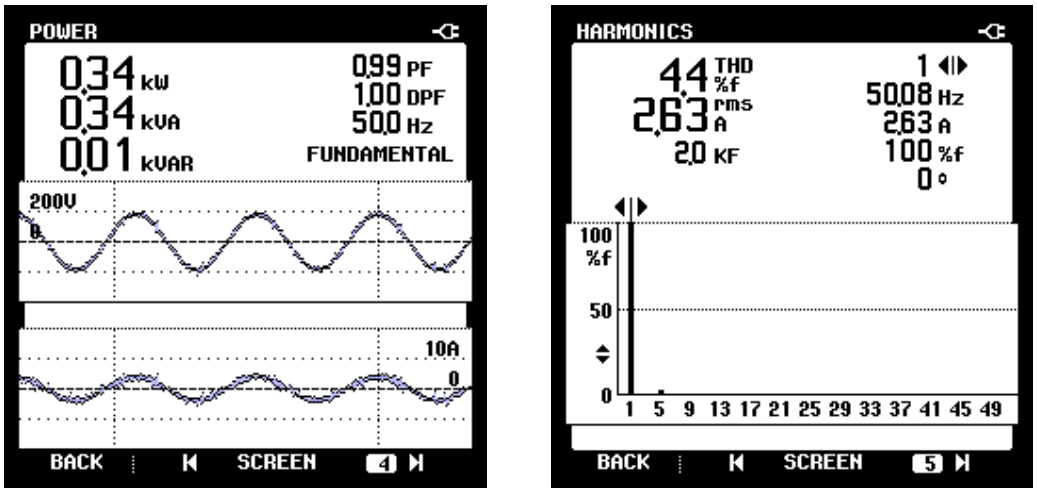
i_{n2} is shown in Fig. 4.12 (b). From its harmonic spectrum, it is evident that the third harmonic is the main component.



(a) Injection current i_{n2} (bottom trace) (b) Injection current i_{n2} FFT

Fig. 4.12 Injection current i_{n2} and its FFT

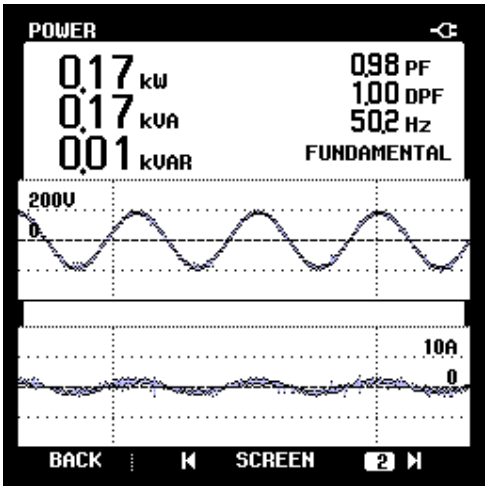
The converter input phase voltage (upper trace) and current waveforms (bottom trace) under its rated output power are shown in Fig. 4.13 (a). The corresponding input current FFT are shown in Fig. 4.13 (b) and it can be seen that its THD is limited to 4.4%.



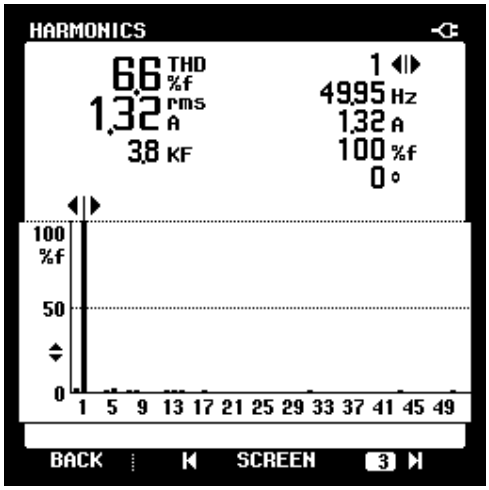
(a) Input phase voltage and current (b) Input current FFT

Fig. 4.13 Converter input phase voltage and current and current FFT at rated output power

At 50% converter rated output power, its input PF is found to be 0.98 while the input current THD has increased to 6.6%, as shown in Fig. 4.14. At 150% rated output power, the converter input PF is found to be 0.99, and the input current THD is reduced to 3.7% as shown in Fig. 4.15. The controller maintains the dc link voltage variation within 3% of its rated value throughout its operation.

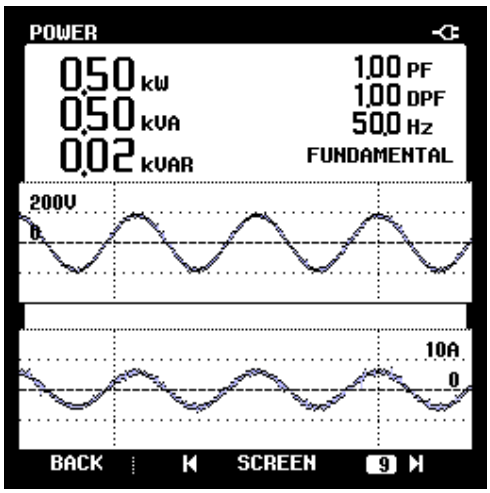


(a) Input phase voltage and current

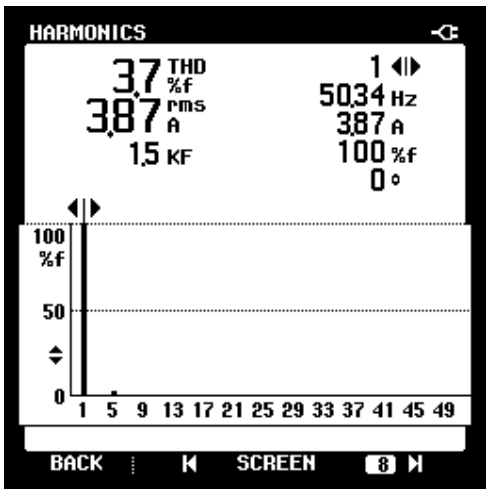


(b) Input current FFT

Fig. 4.14 Converter input phase voltage and current and current FFT at 50% rated output power



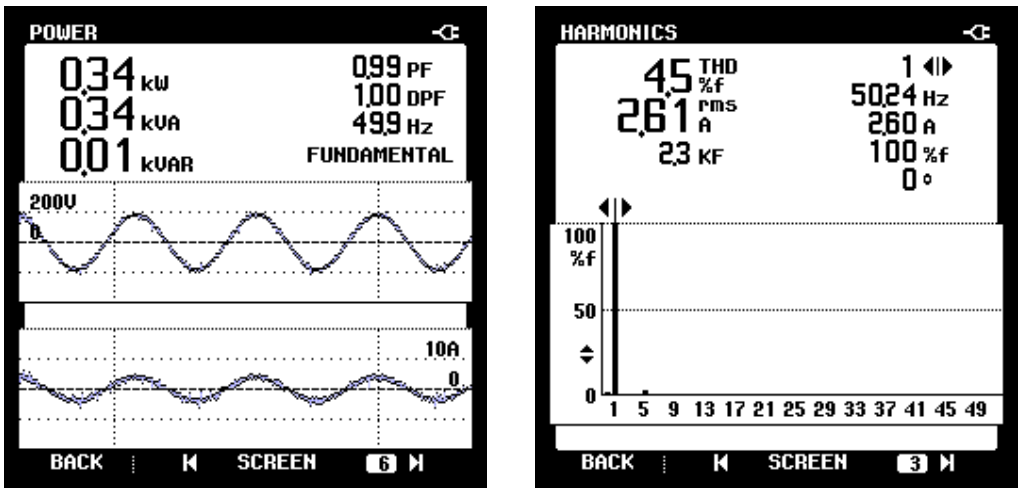
(a) Input phase voltage and current



(b) Input current FFT

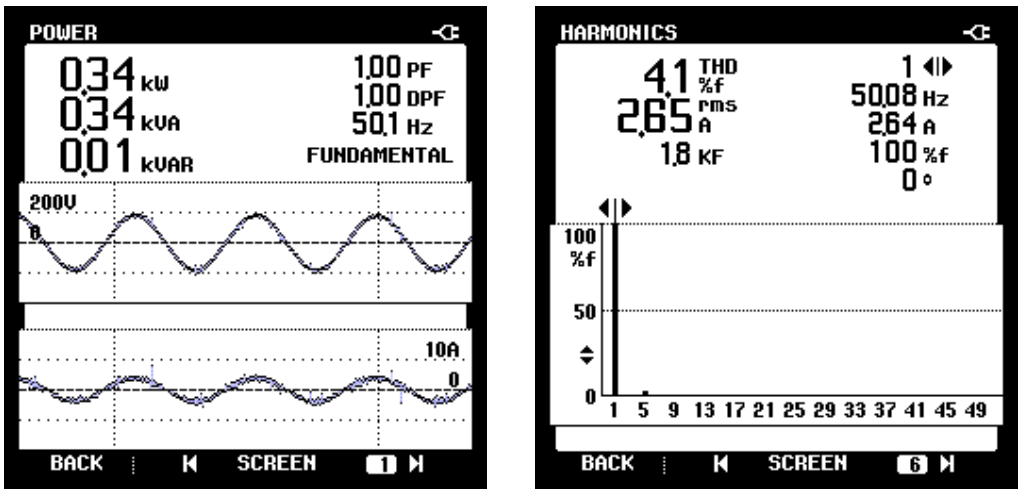
Fig. 4.15 Converter input phase voltage and current and current FFT at 150% rated output power

To investigate the effect of input inductance, its values are varied within a certain range. Under 3mH and 7mH input inductances (ref. to Table 4.2), the converter input voltages and currents and current FFTs are shown in Fig. 4.16 and Fig. 4.17 respectively. These results illustrate that the proposed converter with bidirectional switches coupled with HCC controller overcomes most of the shortcomings of the earlier converters, e.g. change of the input PF due to output power, input inductance and load torque variations.



(a) Input phase voltage and current (b) Input current FFT

Fig. 4.16 Converter input phase voltage and current and current FFT for 3 mH input inductance



(a) Input phase voltage and current (b) Input current FFT

Fig. 4.17 Converter input phase voltage and current and current FFT for 7 mH input inductance

4.3 A near unity power factor converter using the synchronous reference frame based hysteresis current control

Unbalance and distortion in supply voltage may be frequently happening in a weak ac system under practical operating condition. In typical rectifier controller, the reference supply current is derived through the multiplication of a term proportional to the dc link voltage error by a current template. And this current template is generated by supply voltages. This type of control will generate undesirable phenomena on the converter ac and dc sides under unbalanced and nonsinusoidal supply voltage conditions. On the ac side, unbalanced and nonsinusoidal supply current will be obtained, causing an increase in the supply voltage distortion. This can be a problem particularly for generators and high rating power supplies. On the dc side, low frequency power will be produced, resulting in a poor dc link voltage regulation. Hence, higher value of dc capacitors must be used, increasing the total cost [16].

In this chapter, a synchronous frame based hysteresis current control as the inner loop and dc link voltage control as outer loop are adopted for the above discussed rectifier (as shown in Fig. 4.1). This is found to be especially suitable for mid to low power application (i.e., 1-10 kW). The proposed control strategy maintains high quality sinusoidal supply currents and good dc link voltage regulation even under unbalanced and nonsinusoidal supply voltage conditions.

4.3.1 Converter working principle and proposed controller design

The three bidirectional switches, as shown in Fig. 4.1, are controlled to ensure supply current shaping, dc link voltage regulation and the two-capacitor voltage balance. Referring to the topology depicted in Fig. 4.1, the following equation can be formulated:

$$\begin{cases} L\dfrac{di_a}{dt} = v_a - (v_{DM} + v_{MO}) \\ L\dfrac{di_b}{dt} = v_b - (v_{EM} + v_{MO}) \\ L\dfrac{di_c}{dt} = v_c - (v_{FM} + v_{MO}) \end{cases} \tag{4-42}$$

where v_{MO} is the voltage of the node M referring to neutral point O. v_{DM}, v_{EM} and v_{FM} are the voltages at nodes D, E and F referring to the node M. They can be expressed as:

$$\begin{cases} v_{DM} = sign(i_a)(1-s_a)\dfrac{V_{dc}}{2} \\ v_{EM} = sign(i_b)(1-s_b)\dfrac{V_{dc}}{2} \\ v_{FM} = sign(i_c)(1-s_c)\dfrac{V_{dc}}{2} \end{cases} \tag{4-43}$$

where $sign(i_a)$, $sign(i_b)$ and $sign(i_c)$ depend on the polarity of inductor currents. For example,

$$sign(i_a) = \begin{cases} 1 & if\ i_a \geq 0 \\ -1 & if\ i_a < 0 \end{cases} \tag{4-44}$$

For a balanced three-phase system, the voltage v_{MO} can be written as:

$$v_{MO} = -(v_{DM} + v_{EM} + v_{FM})/3 \tag{4-45}$$

The injection current i_{n2}, which is consisted of the sum of the currents through three bidirectional switches, is given as:

$$i_{n2} = i_a s_a + i_b s_b + i_c s_c \tag{4-46}$$

Fig. 4.18 shows the proposed control strategy for the rectifier. The outer dc voltage loop ensures that the dc link voltage is constant, and that it also tracks the reference input. It includes dc link voltage feedback control and dc link current feedforward control. The supply current regulation is accomplished through the use of conventional hysteresis current controller. Park's Transformation is applied to the reference current and the parameter ωt derived from the phase-locked loop (PLL) circuit to obtain the three-phase reference currents. The potential of the dc link middle point M is also controlled to ensure the voltage balance of two capacitors.

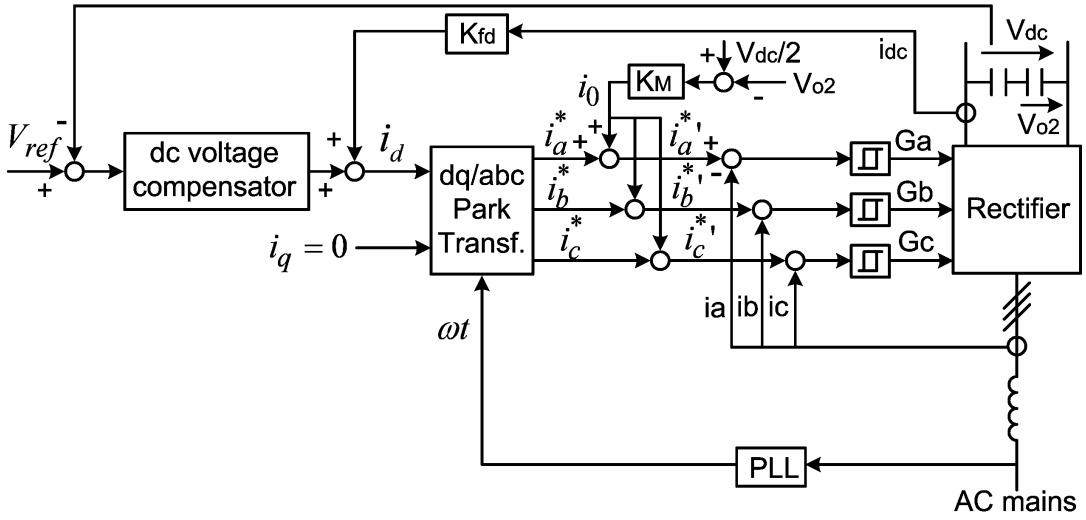


Fig. 4.18 Proposed rectifier control circuit

A. Current controller

The conduction period of the three bidirectional switches is implemented through a simple approach, by the hysteresis control of the supply currents with independent controllers. The switching signals s_x (x=a, b, c) of the bidirectional switches are given by (4-41) and the switching pattern is illustrated with Fig. 4.5.

The voltage v_{MO} is determined by the switching states and current signs of all phases. Due to this interaction, the instantaneous current error can be beyond the hysteresis band 'h' and can reach up to '2h' [93-96]. However, it has been shown that this does not degrade the operation.

B. Voltage controller

The control system is based on the synchronous reference frame method [16, 97, 98]. The angular position (ωt) of the ac supply voltage is determined by a phase-locked loop (PLL) circuit (see Appendix B), as shown in Fig. 4.18. The converter reference currents in three-phase stationary coordinate are obtained by the Park's transformation as (4-47).

$$\begin{bmatrix} i_a^* \\ i_b^* \\ i_c^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \omega t & -\sin \omega t \\ \cos(\omega t - 120°) & -\sin(\omega t - 120°) \\ \cos(\omega t + 120°) & -\sin(\omega t + 120°) \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{4-47}$$

The current i_d and i_q are the active and reactive components of converter Park's currents respectively. Due to the PLL circuit, ωt is a uniformly increasing function of time whose derivative is constant under any ac supply voltage conditions. Thus this transformation angle is insensitive to voltage harmonics and unbalanced voltage [99].

The converter dc voltage must be also controlled at a constant value. This is achieved through the action of Park's active current i_d. The Park's reactive current i_q must be kept in a null value in order to obtain an almost unity power factor. Due to absence of connection between ac supply neutral point and the rectifier, the zero sequence is always zero.

In this model, negligible losses are anticipated in the ac input inductances and in the rectifier. The rectifier input power at any instant is the sum of output power and the rate of change of the energy storage elements. A power balance equation for a synchronous frame based controller of the rectifier is given as:

$$\frac{d}{dt}\left(\frac{1}{2} C_{eq} {v_{dc}}^2\right) + v_{dc} i_{dc} = \sqrt{3} V_p i_d \cos\varphi - \frac{d}{dt}\left(\frac{1}{2} L_s {i_d}^2\right) \tag{4-48}$$

where, $C_{eq} = C/2$ (half of capacitor Ca value), and V_p is the amplitude of supply voltage.

With unity power factor operation ($\cos\varphi = 1$), the above equation can be linearized around the steady-state operating point (I_{dc} and V_{dc}) as,

$$(C_{eq} V_{dc} s + I_{dc}) \tilde{v}_{dc}(s) = (\sqrt{3} V_p - L_s I_d s) \tilde{i}_d(s) - V_{dc} \tilde{i}_{dc}(s) \tag{4-49}$$

The steady state operating current I_{dc} can be obtained by solving (4-50).

$$\sqrt{3} V_p I_d = V_{dc} I_{dc} \tag{4-50}$$

Since the response time of the inner current loop is much faster than the outer voltage loop, the two loops can be delinked. The inner current control block can be ignored by assuming that the output of the current controller is completely followed by its input current command. A simple voltage control scheme is shown in Fig. 4.19. A current feed-forward control loop is also used here to improve the dc link voltage response to load disturbance.

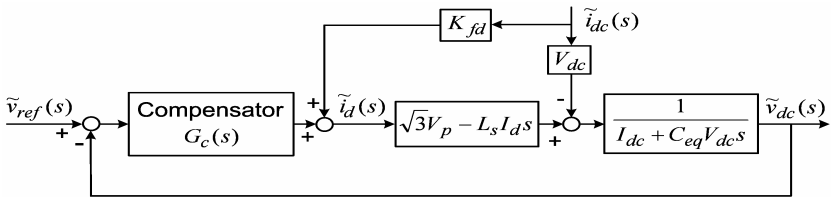


Fig. 4.19 A simple voltage control scheme

From (4-49) one can see that a right half plane (RHP) zero is in the control system. The open loop transfer function of voltage control can be written as (4-51), and the close transfer function is given by (4-52).

$$L(s) = G_c(s) \cdot \frac{L_s I_d}{C_{eq} V_{dc}} \cdot \frac{(\sqrt{3}V_p / L_s I_d) - s}{s + (I_{dc} / C_{eq} V_{dc})} \tag{4-51}$$

$$\frac{\tilde{v}_{dc}(s)}{\tilde{v}_{ref}(s)} = \frac{G_C(s)(\sqrt{3}V_P - L_S I_d s)}{I_{dc} + C_{eq} V_{dc} s + G_C(s)(\sqrt{3}V_P - L_s I_{dc} s)} \tag{4-52}$$

Thus the right half plane zero can be obtained as:

$$z_{zero} = \frac{\sqrt{3}V_p}{L_s I_d} \tag{4-53}$$

A RHP zero imposes fundamental limitations on the control bandwidth, as it forces an upper limit to the achievable gain crossover frequency for stable operation [100]. It is shown in [100] that for systems with one RHP zero at z, the maximum achievable gain crossover frequency ω_{gc}, of the open loop compensated system is limited to:

$$\omega_{gc} \le z \tan\left(\frac{\pi}{2} - \frac{\varphi_m}{2} + n_{gc}\frac{\pi}{4}\right) \tag{4-54}$$

where, φ_m is the phase margin in radian, n_{gc} is slope of the Bode plot of compensated minimum phase part of control to output transfer function at ω_{gc}.

The current feed-forward control parameter K_{fd} hence is determined by:

$$K_{fd} = \frac{V_{dc}}{\sqrt{3}V_p - L_s I_d s}\bigg|_{s=0} = \frac{V_{dc}}{\sqrt{3}V_p} \tag{4-55}$$

C. Balancing the dc link capacitor voltages

In practice, due to the existence of errors in the current hysteresis comparators, the two dc capacitor voltages can become different. This asymmetry will cause an increased voltage stress on the capacitors and hence an increased blocking voltage stress on the converter power semiconductor devices.

The dc capacitors voltages difference v_M is given as:

$$v_M = \frac{1}{2}(v_{o2} - v_{o1}) = \frac{1}{2C}\int_{t1}^{t2} i_{n2}\,dt \tag{4-56}$$

where v_{o1} and v_{o2} are the voltages across capacitor Ca and Cb respectively.

Due to the three independent hysteresis current controllers, from (4-46) and (4-56) one can see that i_{n2} is not always zero. Thus, an asymmetry of the output voltage occurs. However, the voltage balance between the two dc capacitors can be reached by introducing a tiny dc offset as presented below to the reference currents [84]:

$$\begin{cases} i_a^{*}{}' = i_a^{*} + i_0 \\ i_b^{*}{}' = i_b^{*} + i_0 \\ i_c^{*}{}' = i_c^{*} + i_0 \end{cases} \tag{4-57}$$

This zero current component is obtained by expression (4-58). Under steady state, this dc component is zero.

$$i_0 = K_M (v_{o1} - v_{o2}) / 2 \tag{4-58}$$

4.3.2 Converter design and implementation

A sinusoidal PWM voltage source inverter is connected to the rectifier for the intended rectifier-inverter structure as depicted in Fig. 4.6. To illustrate the design feasibility of the proposed converter, a prototype with the same specifications shown in Section 4.2.3 is chosen.

According to (4-50) and (4-51), a simple proportional-integral controller ($0.4+15/s$) is chosen for the dc voltage compensator $G_c(s)$ [100, 101]. A MATLAB/SIMULINK model for the proposed rectifier-inverter structure is developed to perform a digital simulation and verify the predicted results.

A. Simulation results

Under balanced supply and nominal output power condition, the converter supply voltage and current waveforms are shown in Fig. 4.20. The input power factor is found to be 0.999 and supply current THD 3.9%.

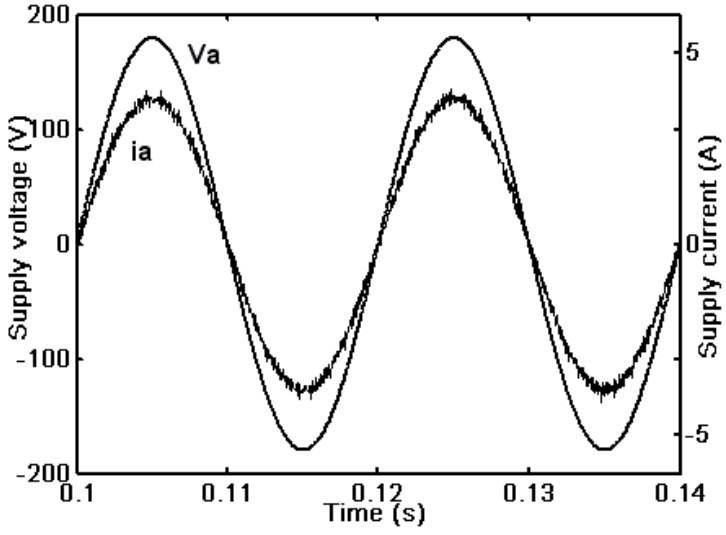


Fig. 4.20 Converter supply voltage and current waveform under balanced supply

Fig. 4.21 shows the 10% unbalanced supply voltage waveforms. Without the proposed synchronous reference frame based controller, the converter supply currents under 10% supply voltage unbalance are shown in Fig. 4.22 and inevitably unbalanced. Fig. 4.23 shows the proposed converter supply current waveforms under 10% supply voltage unbalance. It is quite evident that due to the fast action of the proposed control strategy, unbalanced supply voltage has practically no effect on the supply currents and all three currents are identical and nearly sinusoidal. The input power factor is found to be 0.997 and supply current THD 4.3%.

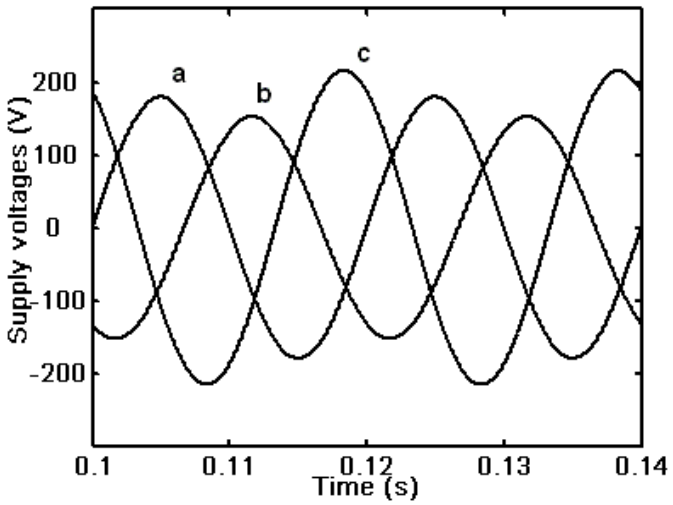


Fig. 4.21 10% unbalanced supply voltage waveforms

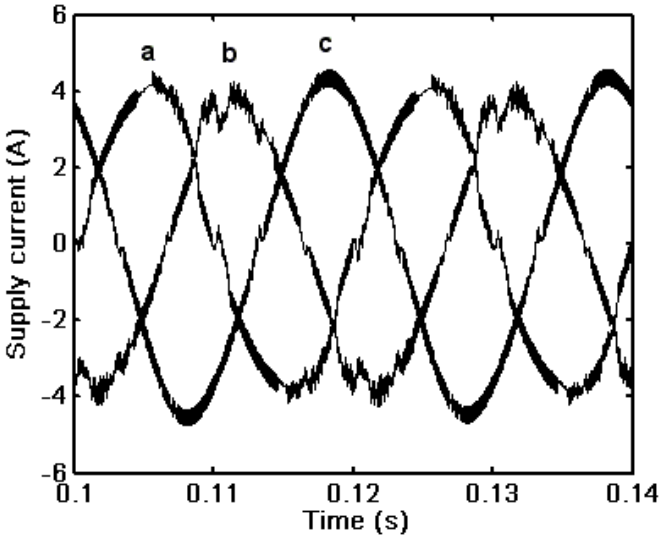


Fig. 4.22 Converter currents under 10% supply voltage unbalance and without the proposed controller

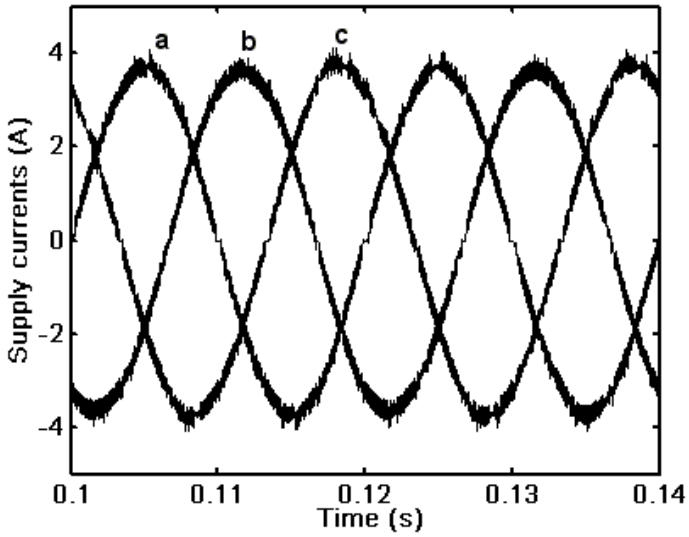


Fig. 4.23 Converter supply currents under 10% supply voltage unbalance and with the proposed controller

The converter supply voltage and current waveform and current spectrum under nonsinusoidal supply voltage are shown in Fig. 4.24 and Fig. 4.25 respectively. The supply voltage has 10% fifth harmonic (introduced). It is evident that the supply current waveform is nearly sinusoidal even when the supply voltage has harmonics. The input power factor is found to be 0.998 and the supply current THD 4.5%. This also proves the proposed synchronous reference frame based hysteresis current controller deals effectively with all kinds of non-ideal conditions that a converter can be subjected to.

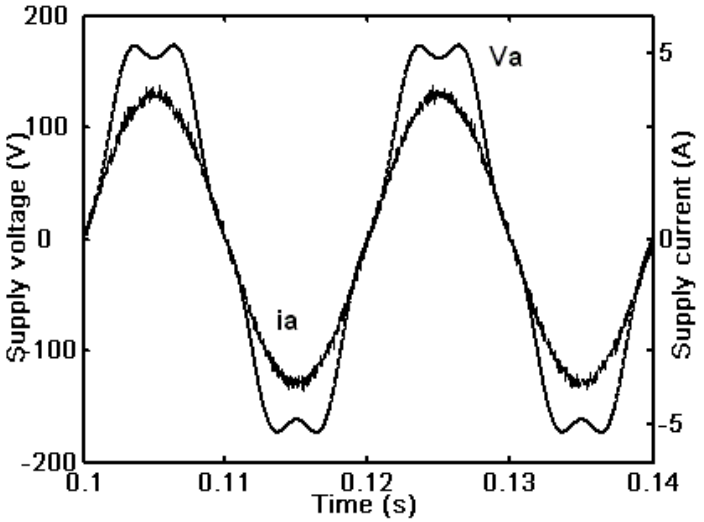


Fig. 4.24 Converter supply voltage and current under nonsinusoidal supply voltage

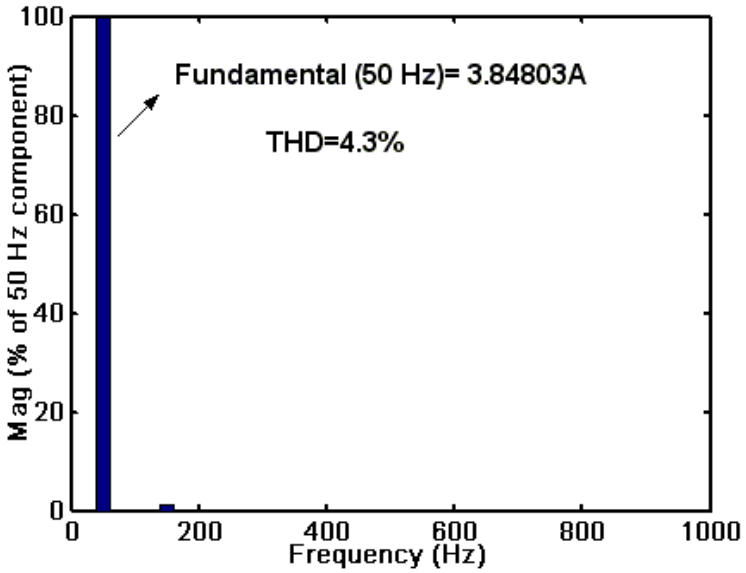
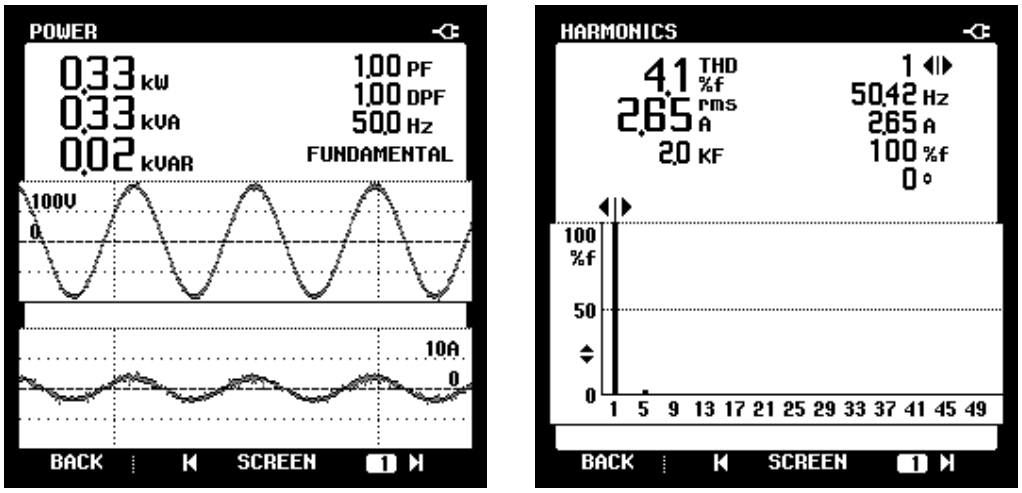


Fig. 4.25 Converter supply current FFT under nonsinusoidal supply voltage

B. Experimental results

The proposed control system is implemented using a single-board ds1103 microprocessor and developed under the integrated development environment of MATLAB-SIMULINK RTW. A 1 kW hardware prototype of the rectifier-inverter structure depicted as in Fig. 4.6 was constructed and its performance is observed.

The converter supply voltage and current waveform and current FFT at balanced supply voltage and rated output power are shown in Fig. 4.26. Fluke-43 spectrum analyzer with online numerical value illustration was used to monitor the waveform. With the proposed synchronous reference frame based hysteresis current control strategy, the supply current total harmonic distortion (THD) is reduced to 4.1% and unity input power factor is achieved.



(a) Supply voltage and current (b) Supply current FFT

Fig. 4.26 Converter supply voltage and current and current FFT at rated output power

The capacitor voltages (captured from ds1103 based controller) are shown in Fig. 4.27. Through the precise action of the ds1103-based controller, both capacitors have equal voltages.

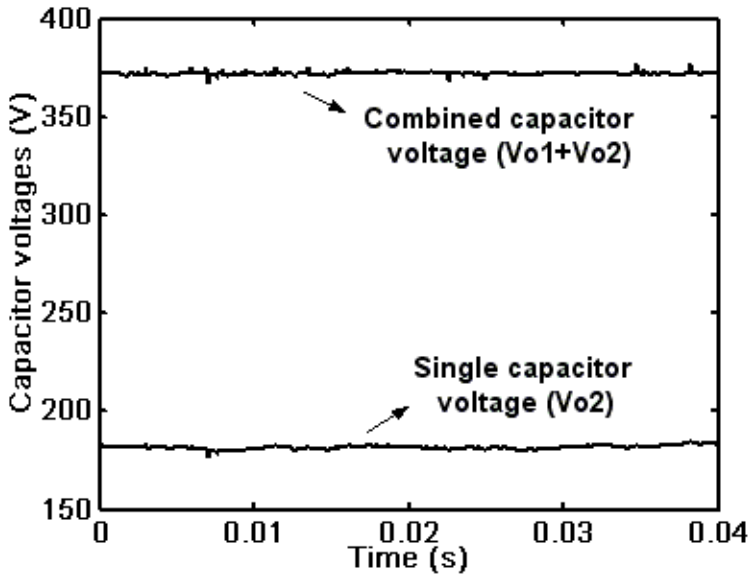


Fig. 4.27 Individual and combined capacitor voltages

The three-phase supply currents with the proposed controller under 10% supply voltage unbalance are shown in Fig. 4.28. The phase ‘a’ supply voltage and current waveform and the current FFT are shown in Fig. 4.29. The corresponding waveforms for phase ‘b’

and phase 'c' are shown in Fig. 4.30 and Fig. 4.31 respectively. All three currents are practically identical and nearly sinusoidal. The input power factor is found to be above 0.99 and supply current THD less than 4.2%.

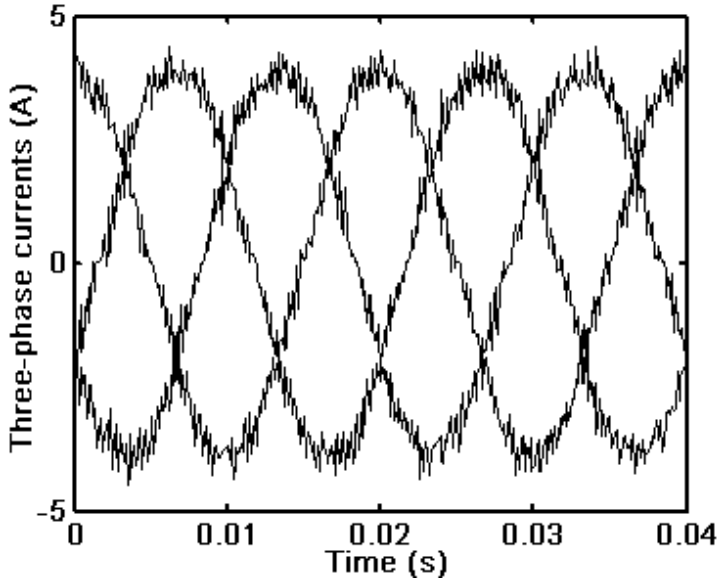
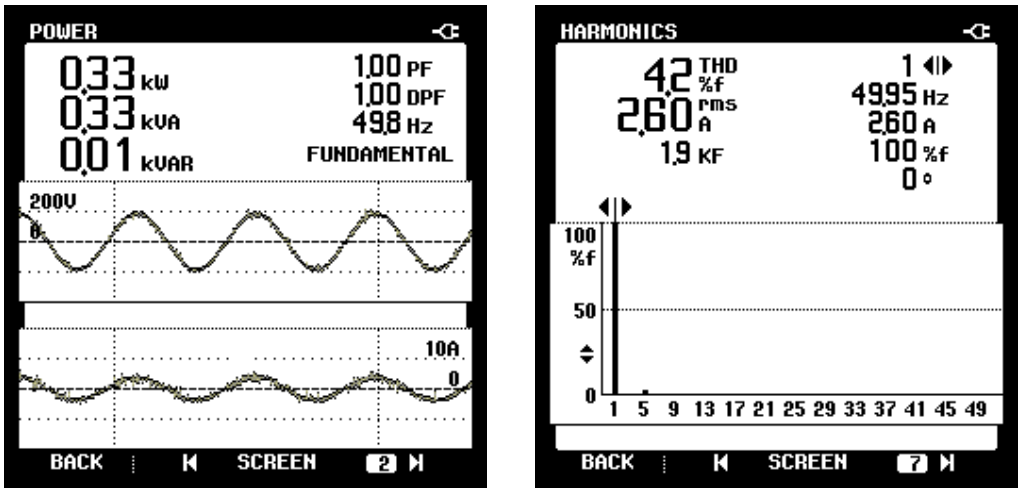
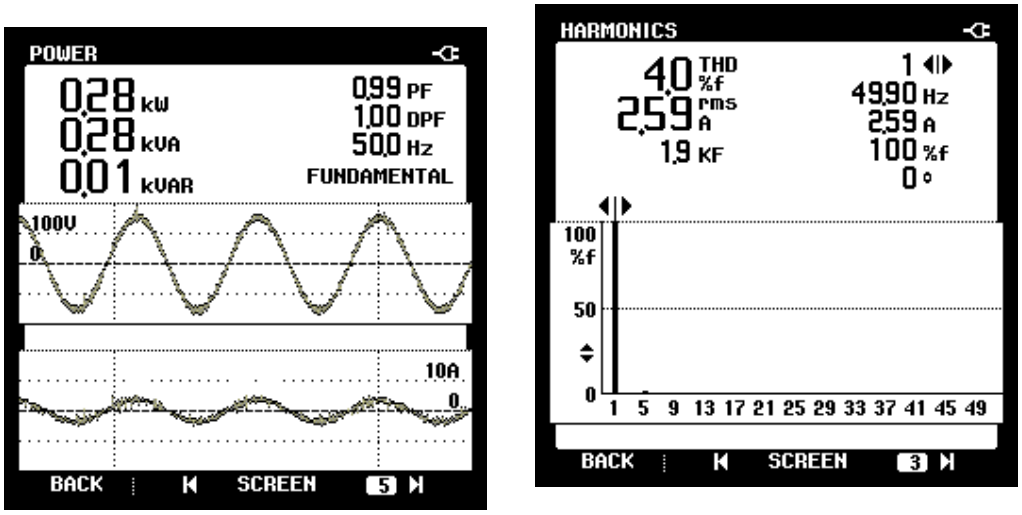


Fig. 4.28 Three-phase supply currents under 10% voltage unbalance



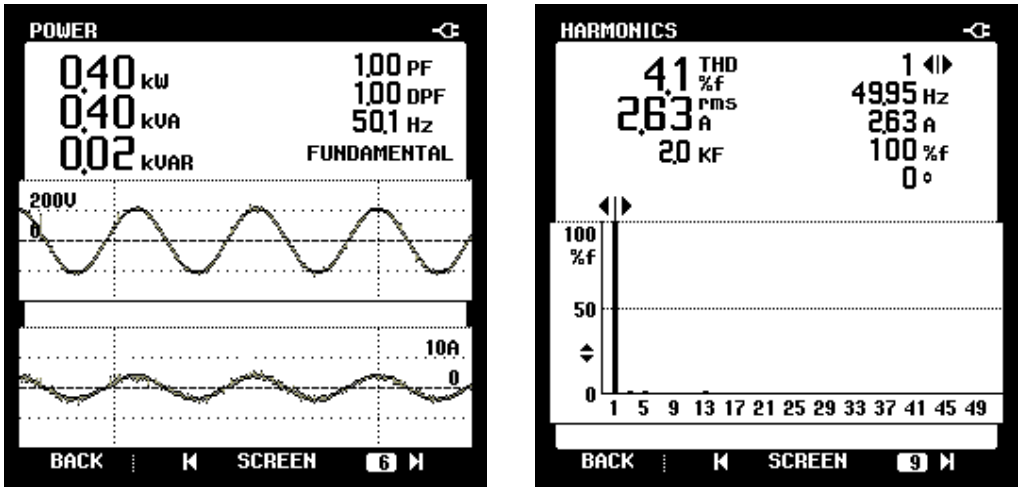
(a) Supply voltage and current (b) Supply current FFT

Fig. 4.29 Phase 'a' waveforms under 10% supply voltage unbalance



(a) Supply voltage and current (b) Supply current FFT

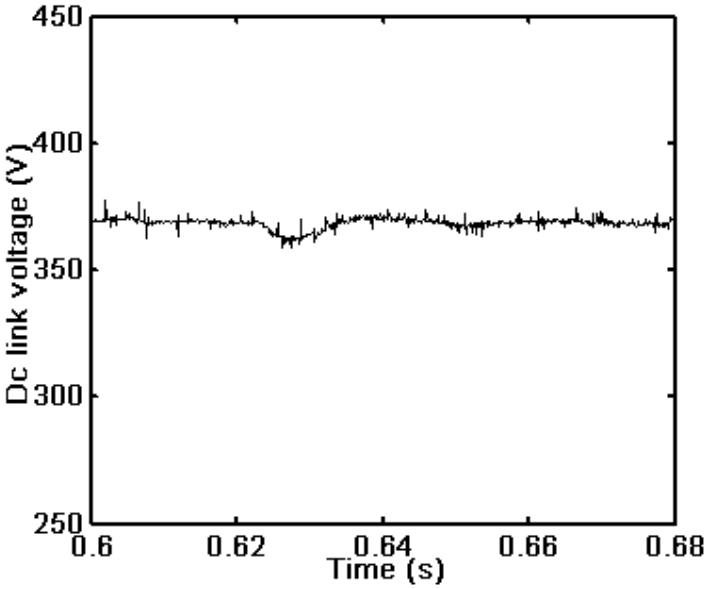
Fig. 4.30 Phase 'b' waveforms under 10% supply voltage unbalance



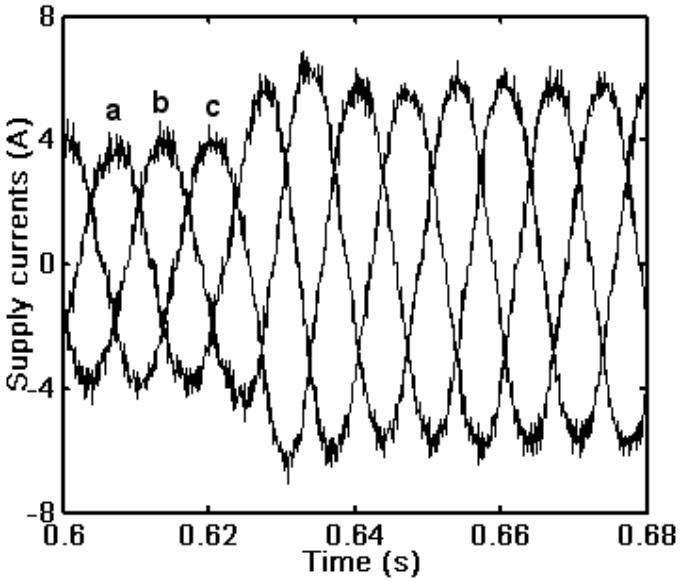
(a) Supply voltage and current (b) Supply current FFT

Fig. 4.31 Phase 'c' waveforms under 10% supply voltage unbalance

Fig. 4.32 shows the dc link voltage and supply current waveforms when the converter output power suddenly changed from 100% to 150% of its rated value responding to a sudden change in load power demand. The dc bus voltage momentarily dropped. However, due to the fast controller action on the bidirectional switches, this voltage recovered quickly. One can clearly see that with the proposed controller the converter exhibits a good response to a sudden load variation.



(a) Response in dc link voltage



(b) Response in supply currents

Fig. 4.32 Converter response to a sudden load change

4.4 Concluding remarks

The proposed low frequency controlled near unity power factor rectifier in Chapter 3 shows a high performance converter and is very suitable for high power application.

However, when used in low power, it will result in a bulky and rather uneconomical structure due to the requirement of larger input inductances.

In this chapter, the bidirectional switches of the rectifier are operated at high frequency to reduce the input inductance to overcome the drawbacks of its application in low power. First, hysteresis current controlled rectifier bidirectional switches are well described with mathematical model. Accordingly, a rectifier-inverter model is analyzed and its performance is evaluated. The scheme shows the characteristics of simplicity and robustness. With such power factor correction technique, the ac drive is capable of functioning throughout a wide load range (i.e., from 50% to 150% rated output power) with power factor above 0.98. It exhibits good performance under input inductance variations, a factor that hindered most previously proposed unity power converters.

Unbalance and distortion in supply voltage may happen frequently in real operation. The research for this low to mid power ac drive is also extended to unbalanced and distorted supply conditions. A synchronous reference frame based hysteresis current control as inner loop and dc link voltage control as outer loop are adopted for the rectifier. With such control strategy, the proposed rectifier-inverter structure draws unity power factor and offers good dc link voltage regulation. It also exhibits good performance to supply voltage distortion and unbalance, and has a good adaptability to address a sudden load change. In addition, the rectifier has a common capacitive point that allows the three-level operation and a low blocking voltage stress on the power switches (half of the dc link voltage). The reduction of blocking voltage allows the use of low cost and low loss power devices, increasing the efficiency and power density with reduced production cost. The proposed bidirectional switch controller with high switching frequency is expected to be a good power factor correction retrofit to the front-end rectifiers of the existing small to medium power ac drives.

Chapter 5

Variable Hysteresis Band Current Controlled Rectifier with Constant Switching Frequency

5.1 Introduction

In the previous chapter, we can see that hysteresis current controlled rectifier shows features of easy implementation, high robustness, and good tracking ability. However, its drawback remains random switching frequency, resulting in unpredictable input current harmonic spectrum. Moreover, the current hysteresis band is fixed, and hence it cannot always provide the optimum current waveform. Especially the instantaneous current error can reach double the value of the hysteresis band due to interference between the three phases.

In this chapter, average current control strategy, a high performance and popular fixed switching frequency controlled current modulation technique, is adopted for three-phase three-level rectifier. The performance of the rectifier under average and hysteresis current control strategies is investigated and compared. It shows that although the converter with average current control yields a better performance than hysteresis current control, this is achieved at higher switching frequency. A simple and novel variable hysteresis band current control technique, which can overcome the drawbacks of the above discussed current modulation strategies, is proposed for this three-phase three-level rectifier. The rectifier has the characteristic of drawing nearly sinusoidal current with unity power factor.

5.2 Comparison of average and hysteresis current controlled three-phase three-level rectifiers

Average current control technique, with its good noise immunity and no slope compensation requirement, exhibits high performance among fixed switching frequency

controlled current modulation methods. It is first adopted for the three-phase three-level rectifier (ref. to Fig. 4.1) and then compared with hysteresis current control technique (random switching frequency).

5.2.1 Implementation of average current controller for three-phase three-level rectifier

A. Current controller

The average current controller is based on the principle of ramp comparison as shown in Fig. 5.1. The instantaneous current error is fed to a proportional-integral (PI) regulator. The resulting output of the PI regulator is compared with a sawtooth carrier. If intersections are obtained, the error is forced to remain within the band defined by the amplitude of the sawtooth waveform. All three phases use a common carrier signals. The integral term improves the tracking by reducing the instantaneous error between the reference and the actual error [90]. The slope of the output of PI regulator should be less than the sawtooth carrier slope to guarantee the intersections. The carrier signal frequency and amplitude and the PI regulator parameters can be chosen according to the standard design presented in [91-93].

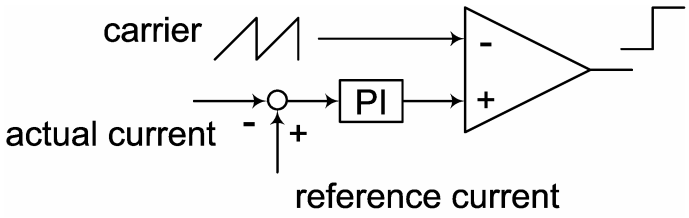


Fig. 5.1 Average current controller

B. Voltage controller

The instantaneous power equation relating input and output quantities of the rectifier (ref. to Fig. 4.1) is obtained by differentiating the energy quantities

$$\frac{d}{dt}\left(\frac{1}{2}C_{eq}v_{dc}^2\right)+\frac{v_{dc}^2}{R}=\frac{3}{2}\left[V_s I_s \cos\varphi-\frac{d}{dt}\left(\frac{1}{2}LI_s^2\right)\right] \tag{5-1}$$

where, $C_{eq} = C/2$ (half of capacitor Ca value). V_s and I_s are the supply voltage and current amplitude respectively; φ is the phase shift between V_s and I_s.

Linearizing the power equation around the operation point (V_{dc0}, I_{dc0}) and considering unity power factor operation ($\varphi = 0$) yields:

$$G_v(s) = \frac{3(V_{s0} - sLI_{s0})}{2sC_{eq}V_{dc0} + 4V_{dc0}/R} \tag{5-2}$$

Since the inner current loop is much faster than the outer voltage loop, the inner current control block can be ignored by assuming the output of the current controller is completely followed by its input current command. A very simple voltage control scheme shown in Fig. 5.2 can serve this purpose.

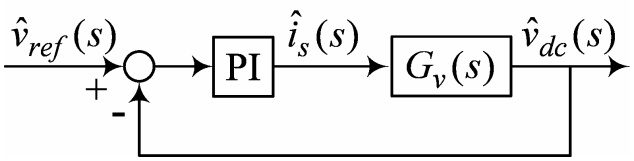


Fig. 5.2 Voltage control scheme

Fig. 5.3 shows the complete control diagram of average current control for three-phase three-level rectifier. The PI_1 in Fig. 5.3 is the average current PI controller as shown in Fig. 5.1. And the PI_2 is the voltage PI controller as shown in Fig. 5.2.

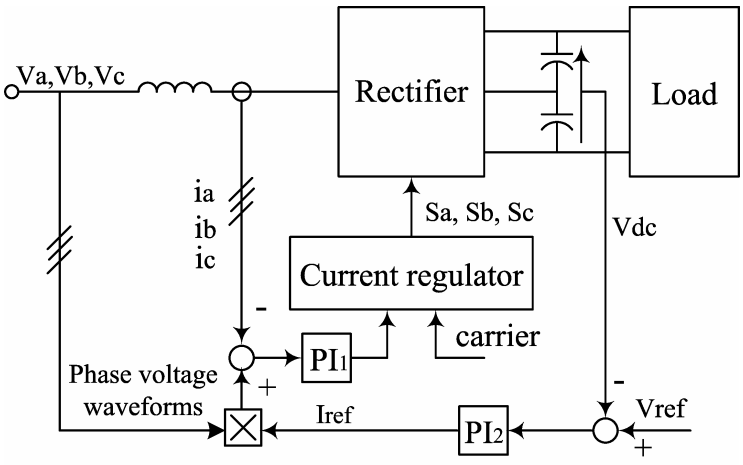


Fig. 5.3 Block diagram of the three-phase three-level rectifier with average current control

5.2.2 Digital simulation and comparative study

To evaluate the relative strengths of both current control strategies, the following parameters are chosen for average and hysteresis current controlled three-phase three-level rectifiers:

- Ac supply: 220 V (line-to-line), 50 Hz;
- Input inductors: 3 x 1 mH (0.033 p. u.);
- Dc capacitors: 2 x 1000μF;
- Dc link reference voltage: 450 V (2.05 p. u.);
- Rated output power: 5 kW.

For average current control, the sawtooth carrier frequency is chosen as 20 kHz. This is to provide equal base for comparison as follows. The converter average input current ripples could be estimated by (5-3)

$$\Delta i = \frac{V_{in}}{L} \alpha T_s \tag{5-3}$$

where V_{in}, α and T_s are the single phase boost rectifier average input voltage, average duty ratio and switching frequency respectively.

According to the standard design [91-93], a PI controller of $0.4 + 4000/s$ is chosen for the average current controller (PI_1 in Fig. 5.3). And $0.12 + 6/s$ is chosen for the dc link voltage controller (PI_2 in Fig. 5.3).

With the above design parameters and (5-3), the rectifier input current ripples can be estimated as 2.81A. To facilitate comparison purposes, the current boundary of hysteresis current controller is also chosen to be the same value ($2h = 2.81A$).

A MATLAB-SIMULINK simulation of the rectifier is conducted based on the above chosen parameters. Fig. 5.4 shows the supply current and current tracking error waveforms of average current controlled rectifier under rated output power. The input power factor is found to be 0.999 and current THD 4.4%. The hysteresis current controlled rectifier supply current and current tracking error waveforms under rated

output power are shown in Fig. 5.5, with input power factor of 0.998 and current THD 6.7%. The average current control technique yields a better rectifier supply current.

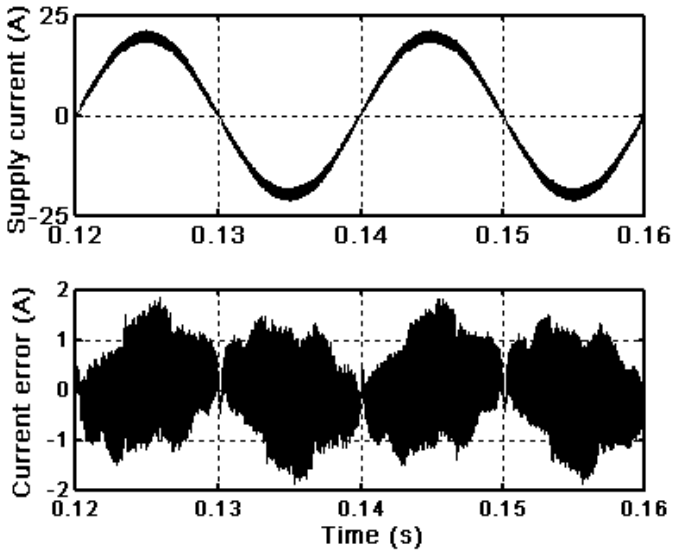


Fig. 5.4 Average current controlled rectifier supply current and current tracking error waveforms at rated output power

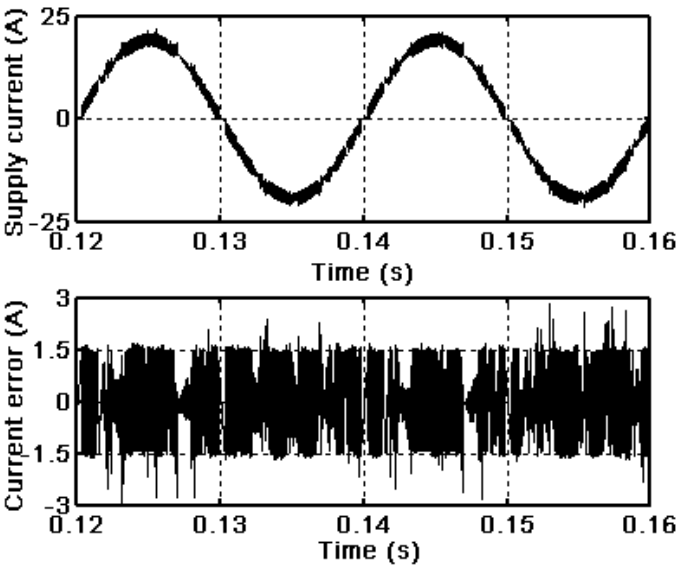


Fig. 5.5 Hysteresis current controlled rectifier supply current and current tracking error waveforms at rated output power

Fig. 5.6 shows the supply current and current tracking error waveforms of average current controlled rectifier under 50% rated output power. The input power factor is found to be 0.997 and current THD 8.1%. The hysteresis current controlled rectifier

supply current and current tracking error waveforms under 50% rated output power are shown in Fig. 5.7, with input power factor of 0.992 and current THD of 12.7%.

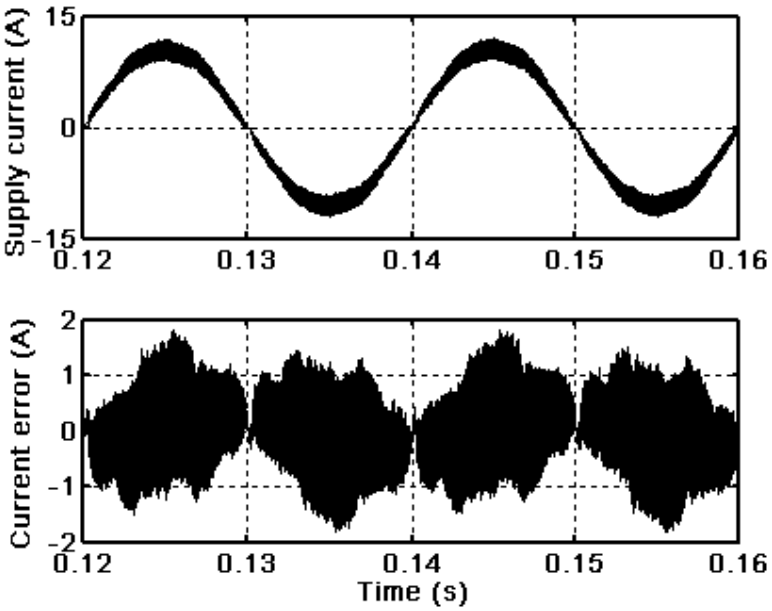


Fig. 5.6 Average current controlled rectifier supply current and current tracking error waveforms at 50% rated output power

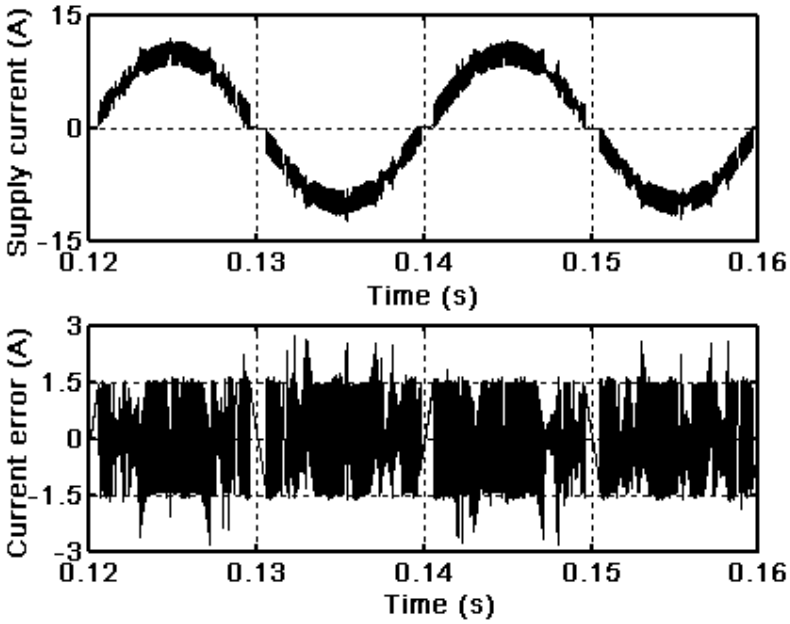


Fig. 5.7 Hysteresis current controlled rectifier supply current and current tracking error waveforms at 50% rated output power

The rectifier performance parameters under various load conditions are summarized in Table 5.1. A general degradation of power factor and THD is obvious under both control schemes when the rectifier does not operate around its rated value. It is clear that hysteresis current control technique offers a significantly lower switching frequency stress due to almost fixed current error as is evident in Fig. 5.5. This is a sharp contrast to the average current control technique (Fig. 5.4). Hysteresis current controller is robust and easy to implement while the PI regulator parameters should be carefully chosen for average current controller. However, the hysteresis current control has a random frequency even though the current band is fixed. The instantaneous error can reach double the value of the hysteresis band due to interference between the three phases [44], as can be seen at the bottom waveforms of Fig. 5.5 and Fig. 5.7 (lower trace).

Table 5.1 Rectifier performance parameters under selected load conditions

Method	Load (Po)	Input power factor	Input current THD
Average current control	50%	0.997	8.1%
	100%	0.999	4.4%
Hysteresis current control	50%	0.992	12.7%
	100%	0.998	6.7%

Fig. 5.8 shows the average switching frequency of the rectifier bidirectional switches under hysteresis current control. From the comparative study, one can conclude that average current control technique yields lower THD and slightly higher power factor compared to its hysteresis counterpart under equal conditions of permissible input current distortion. This is achieved at higher switching frequency of 20 kHz, as opposed to 8 kHz required for hysteresis current control. This phenomenon and its consequent expected high switching losses make the average current control limited to low power converter application. A novel method that overcomes the drawbacks of both these control techniques will be proposed in next section.

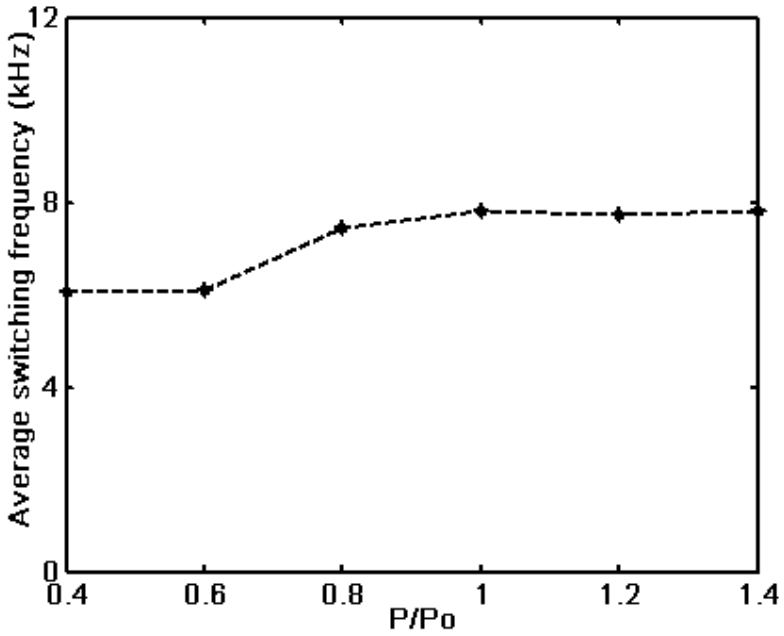


Fig. 5.8 Average switching frequency of bidirectional switches with hysteresis current controller versus normalized converter output power

5.3 Variable hysteresis band current controlled rectifier

The three-phase three-level rectifier was proposed by Kolar in [72], and controlled with the conventional hysteresis current control. This control strategy shows the advantages of easy implementation, good accuracy and high robustness. However, a conventional hysteresis current controller with a fixed hysteresis band has the drawbacks that the modulation frequency varies throughout the fundamental period, and the instantaneous error can reach double the value of the hysteresis band due to interference between the three phases [44]. A space vector control [54] and double ramp comparison control [9] can overcome the above shortcomings and show a high performance. However, these methods either needs well ascertained the space vectors or are complicated to implement.

In this section, a simple and novel variable hysteresis band current control strategy [94-96] for three-phase three-level rectifier is proposed, where the band is controlled as variations of input voltage and output dc link voltage in order to hold the switching frequency constant at any operating conditions. A detailed analysis of the hysteresis band

and elimination of the interference between three phases are provided. The proposed method is verified by simulations and hardware experiments.

5.3.1 Variable hysteresis band current control strategy

The basic structure of a three-phase three-level rectifier is redrawn as in Fig. 5.9. The analysis of variable hysteresis band current control strategy will be considered for the case when the middle point 'M' of dc link capacitors is connected to ground, as well as when that point is floating.

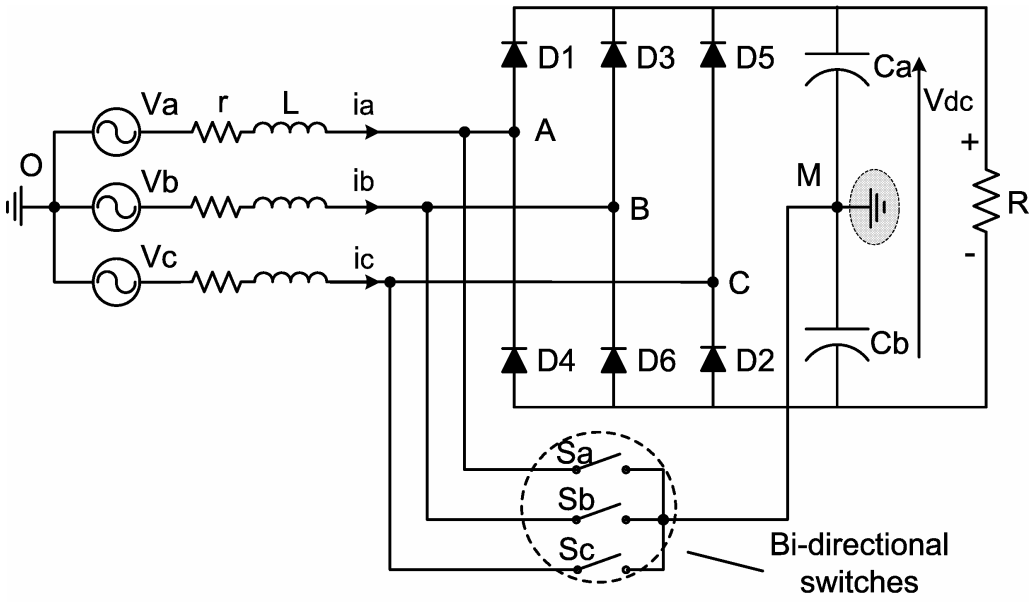


Fig. 5.9 Three-phase three-level rectifier

A. Capacitors middle point connected to ground

When the middle point M of dc capacitors is connected to ground, each phase can be regarded as independent. Referring to the topology, the relationship for phase 'a' voltage and current can be formulated as,

$$v_a = L\frac{di_a}{dt} + ri_a + v_A \tag{5-4}$$

where v_A is the voltage of point A referred to the ground. In practice, it can only take the values of $-V_{dc}/2$, 0, and $V_{dc}/2$, depending on the state of the bidirectional switch and the direction of current i_a. If i_a^* is the reference current for phase 'a', the fictitious reference voltage v_A^* would exist, given by (5-5)

$$v_a = L\frac{di_a^*}{dt} + ri_a^* + v_A^* \tag{5-5}$$

For hysteresis current control, the difference between the actual and the reference current can be defined as:

$$\delta_a = i_a^* - i_a \tag{5-6}$$

Subtracting (5-4) from (5-5) and substituting (5-6), one can write:

$$L\frac{d\delta_a}{dt} + r\delta_a + (v_A^* - v_A) = 0 \tag{5-7}$$

The effect of the input inductor resistance r can be neglected, so that (5-7) becomes:

$$L\frac{d\delta_a}{dt} = -(v_A^* - v_A) \tag{5-8}$$

1) Operation during the positive interval of i_a^*

The operation of the hysteresis current controller over one switching cycle during the positive interval of i_a^* is shown in Fig. 5.10.

From (5-8), this can be expressed mathematically as:

$$-(v_A^* - 0) = L\frac{\Delta\delta_a}{\Delta t} = L\cdot\left\{\frac{\delta_a(t_1) - \delta_a(0)}{t_1 - 0}\right\} = L\cdot\left\{\frac{-h-h}{t_1 - 0}\right\} \tag{5-9}$$

for the period $0 < t < t_1$, and

$$-(v_A^* - \frac{V_{dc}}{2}) = L\frac{\Delta\delta_a}{\Delta t} = L\cdot\left\{\frac{\delta_a(T_s)-\delta_a(t_1)}{T_s - t_1}\right\} = L\cdot\left\{\frac{h+h}{T_s - t_1}\right\} \tag{5-10}$$

for the period $t_1 < t < T_s$. Here T_s is the reciprocal of the switching frequency f_s.

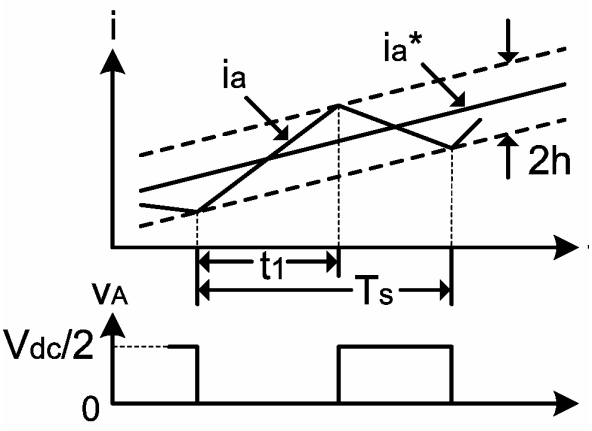


Fig. 5.10 Current and voltage waveforms with hysteresis current control when $i_a^* > 0$

From (5-9) and (5-10) the overall time period for one complete switching transition can be calculated as,

$$T_s = \frac{2hLV_{dc}}{V_{dc}v_A^* - 2(v_A^*)^2} \tag{5-11}$$

Substituting (5-5) into (5-11), the expression for phase 'a' hysteresis current band can be written as:

$$h = \frac{(v_a - L\frac{di_a^*}{dt})V_{dc} - 2(v_a - L\frac{di_a^*}{dt})^2}{2f_sLV_{dc}} \tag{5-12}$$

2) Operation during the negative interval of i_a^*

The operation of the hysteresis current controller over one switching cycle during the negative interval of i_a^* is shown in Fig. 5.11.

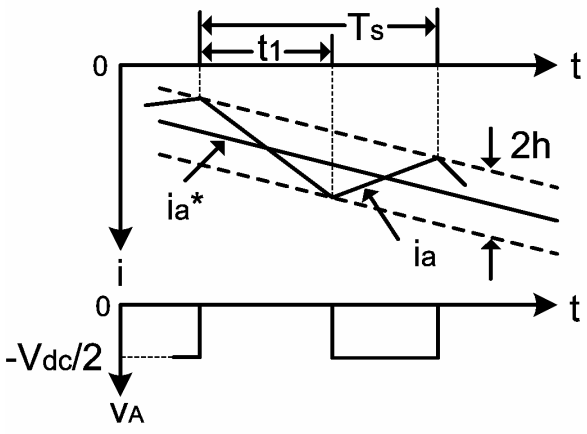


Fig. 5.11 Current and voltage waveforms with hysteresis current control when $i_a^* < 0$

From (5-8), this can be expressed mathematically as:

$$-(v_A^* - 0) = L\frac{\Delta\delta_a}{\Delta t} = L\cdot\left\{\frac{\delta_a(t_1)-\delta_a(0)}{t_1-0}\right\} = L\cdot\left\{\frac{h+h}{t_1-0}\right\} \tag{5-13}$$

for the period $0 < t < t_1$, and:

$$-(v_A^* + \frac{V_{dc}}{2}) = L\frac{\Delta\delta_a}{\Delta t} = L\cdot\left\{\frac{\delta_a(T_s)-\delta_a(t_1)}{T_s-t_1}\right\} = L\cdot\left\{\frac{-h-h}{T_s-t_1}\right\} \tag{5-14}$$

for the period $t_1 < t < T_s$.

Similarly the expression for phase 'a' hysteresis current band can be written as:

$$h = \frac{[(-v_a) - L\frac{d(-i_a^*)}{dt}]V_{dc} - 2(v_a - L\frac{di_a^*}{dt})^2}{2f_sLV_{dc}} \tag{5-15}$$

Since i_a^* is sinusoidal and in phase with v_a, the hysteresis current band for the whole line voltage cycle can be written in a uniform format as:

$$h = \frac{(|v_a| - L\frac{d|i_a^*|}{dt})V_{dc} - 2(|v_a| - L\frac{d|i_a^*|}{dt})^2}{2f_sLV_{dc}} \tag{5-16}$$

The relationship between hysteresis band h and switching frequency f_s is governed by (5-16). When the hysteresis band h is fixed as in conventional hysteresis current control, the switching frequency f_s will be varying. For a detailed switching frequency on the other hand, if the hysteresis band h is calculated using (5-13), the constant switching frequency operation can be ensured. Similar expressions can be derived for phase 'b' and 'c' as well.

B. Capacitors middle point without connection to the ground

In practice the dc link capacitors middle point M is normally floating to avoid the third current harmonic (triplen harmonics in general) in the neutral wire, the previous analysis now will be extended to allow for floating point M.

When point M is floating, the relationship for phase 'a' voltage and current can be reformulated as:

$$v_a = L\frac{di_a}{dt} + ri_a + v_{AM} + v_{MO} \tag{5-17}$$

where v_{AM} is the voltage between point A and M and v_{MO} is the voltage of point M referred to ground. Subtracting (5-5) from (5-17) gives:

$$L\frac{d\delta_a}{dt} + r\delta_a + (v_A^* - v_{AM}) - v_{MO} = 0 \tag{5-18}$$

Compared with (5-7), (5-18) has introduced a new term v_{MO}. From (5-6), the current error $(i_a^* - i_a)$ here can be decoupled into two parts as [95],

$$\delta_a = i_a^* - i_a = \delta_{a1} + \delta_{a2} \tag{5-19}$$

where δ_{a1} is non-interacting error and δ_{a2} is interacting error. Non-interacting error δ_{a1} is the current error without voltage v_{MO} (or v_{MO}=0). Interacting error δ_{a2} is the current error introduced by voltage v_{MO}.

Hence (5-19) can be separated into two sections, as follows:

$$-(v_A^* - v_{AM}) = L\frac{d\delta_{a1}}{dt} + r\delta_{a1} \tag{5-20}$$

$$v_{MO} = L\frac{d\delta_{a2}}{dt} + r\delta_{a2} \tag{5-21}$$

(5-20) shows that δ_{a1} only depends on the corresponding voltage v_{AM}, similar to (5-8). Hence current error δ_{a1} can be treated in the same way as the error δ_a in the case of the capacitive middle point M connected to ground. One can see that the three-phase interacting errors are the same ($\delta_{a2} = \delta_{b2} = \delta_{c2}$).

To determine δ_{a1}, it is necessary to determine δ_{a2}, which depends only on v_{MO}. However, the voltage v_{MO} is determined by the supply phase voltage and bidirectional switching patterns. Table 5.2 illustrates the voltage v_{MO} at various switching positions.

Table 5.2 The voltage v_{MO} at various switching positions

Sa,Sb,Sc / Va, Vb, Vc	000	001	010	011	100	101	110	111
+ - +	$-\frac{V_{dc}}{6}$	0	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{6}$	0	$\frac{V_{dc}}{6}$	$-\frac{V_{dc}}{6}$	0
+ - -	$\frac{V_{dc}}{6}$	0	0	$-\frac{V_{dc}}{6}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{6}$	$\frac{V_{dc}}{6}$	0
+ + -	$-\frac{V_{dc}}{6}$	$-\frac{V_{dc}}{3}$	0	$-\frac{V_{dc}}{6}$	0	$-\frac{V_{dc}}{6}$	$\frac{V_{dc}}{6}$	0
- + -	$\frac{V_{dc}}{6}$	0	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{6}$	0	$-\frac{V_{dc}}{6}$	$\frac{V_{dc}}{6}$	0
- + +	$-\frac{V_{dc}}{6}$	0	0	$\frac{V_{dc}}{6}$	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{6}$	$-\frac{V_{dc}}{6}$	0
- - +	$\frac{V_{dc}}{6}$	$\frac{V_{dc}}{3}$	0	$\frac{V_{dc}}{6}$	0	$\frac{V_{dc}}{6}$	$-\frac{V_{dc}}{6}$	0

5.3.2 Proposed converter implementation

Fig. 5.12 shows the schematic single phase diagram of the variable hysteresis band current controller when the capacitive middle point M is floating. Due to the simplicity, attraction and popularity of this technique, the rest of the work is dedicated to it. The feedback current i_a is initially subtracted from the reference current i_a^* to produce the current error δ_a. This step is identical to a conventional hysteresis current controller. Further the interacting error term δ_{a2} is subtracted from δ_a to produce the non-interacting error δ_{a1}, which is in turn used for the hysteresis controller. The variable hysteresis band h is calculated from (5-15) with the help of v_a, i_a^* and V_{dc}. And the current interacting error δ_{a2} is obtained from v_{MO}, which is generated from Table 5.2 in combination with the three-phase supply voltage and three bidirectional switching patterns.

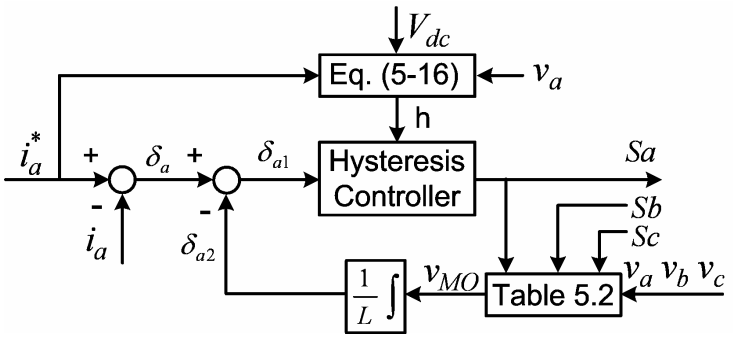


Fig. 5.12 Block diagram for phase 'a' of the variable hysteresis band current controller

The control system is implemented using a single-board ds1103 microprocessor manufactured by dSPACE GmbH and developed under the integrated development of MATLAB-SIMULINK RTW provided by The MathWorks.

To illustrate the design feasibility of the rectifier, the following specification is chosen:

- Ac supply: 220 V (line-to-line), 50 Hz;
- Input inductors: 3 x 5 mH (0.033 p. u.);
- Dc link reference voltage 370 V (1.68 p. u.);
- Dc capacitors: 2 x 1000 μF;
- Rated output power 1 kW.

5.3.3 Simulation and experimental results

To verify the performance of the proposed variable hysteresis band current control compared with conventional hysteresis current control, initially a MATLAB-SIMULINK prototype of the rectifier is developed and its simulation results are illustrated in Fig. 5.13 through Fig. 5.18.

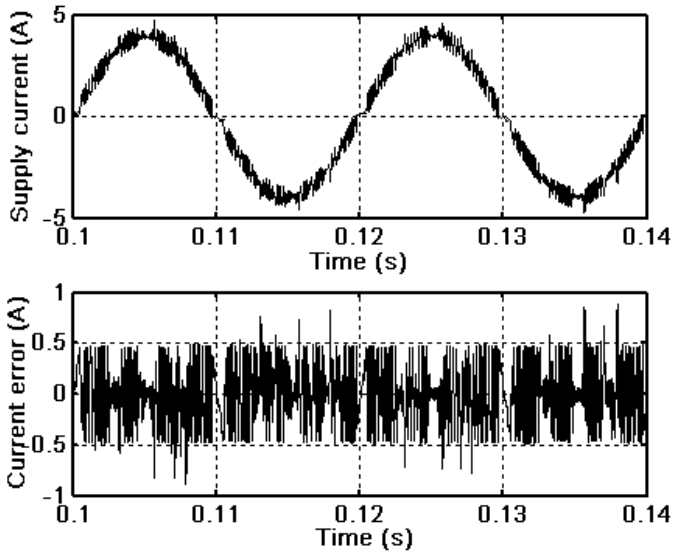


Fig. 5.13 Rectifier supply current (upper trace) and current error (lower trace) for conventional hysteresis current control

Fig. 5.13 shows the rectifier supply current and current error waveforms for conventional hysteresis current control, where the fixed current band 'h' is set to 0.5 A to achieve an optimal switching frequency of 7 kHz. From (5-17) and Table 5.2, one can see that the rectifier supply current in one phase is inevitably influenced by the switching patterns of bidirectional switches in the other two phases. Due to such interaction of three phases, the supply current instantaneous error is not always limited within the hysteresis band 'h' and may reach up to '2h', as evident from some of the random spikes of Fig. 5.13 (lower trace). The rectifier supply current and current error waveforms for the adopted variable hysteresis band current control are shown in Fig. 5.14. Referring to Fig. 5.14 (lower trace), one can notice that the current error can go beyond 'h', but to a much smaller extend, and never to '2h'.

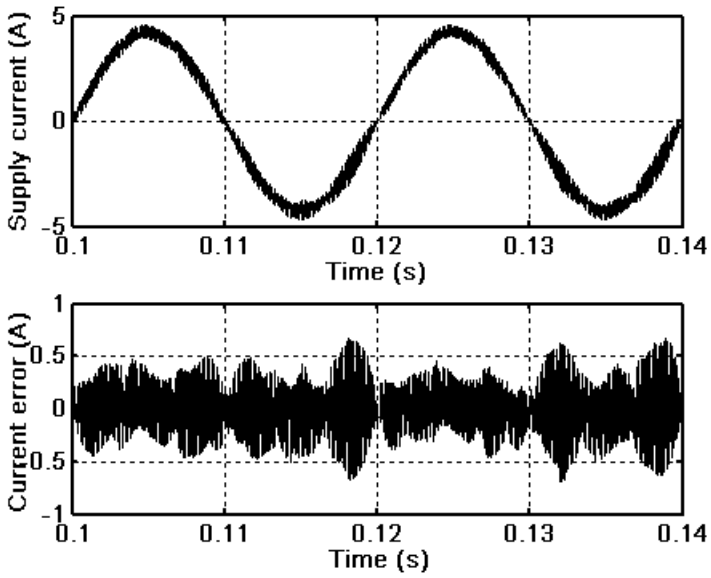


Fig. 5.14 Rectifier supply current (upper trace) and current error (lower trace) for variable hysteresis band current control

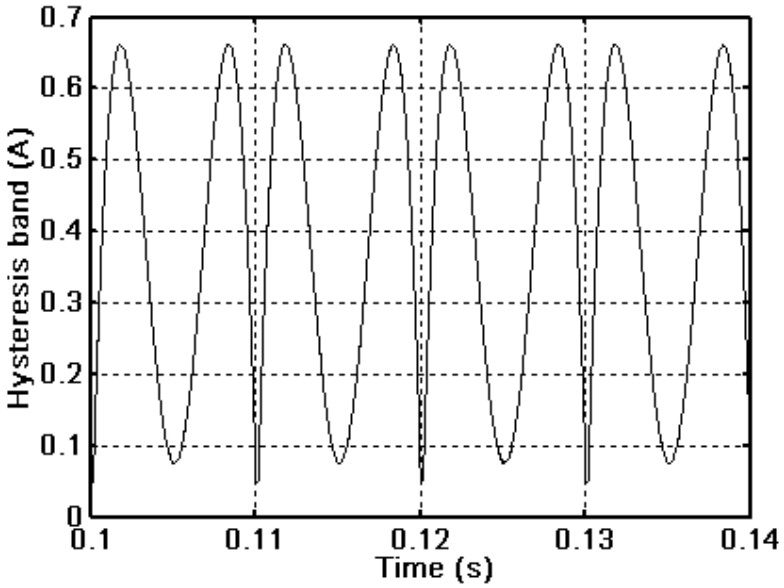


Fig. 5.15 Variable hysteresis band

The variable hysteresis current band and the rectifier supply current interacting error and non-interacting error are shown in Fig. 5.15 and Fig. 5.16 respectively. The hysteresis band in Fig. 5.15 is varying instead of fixed, thus trying to provide required optimal current error boundary. The non-interacting error (lower trace of Fig. 5.16), which is the decoupled part of rectifier supply current error (lower trace of Fig. 5. 14) without the

interacting error (upper trace of Fig. 5.16), can be seen to strictly follow the variable hysteresis band (Fig. 5.15). Thus the influence of three-phase current interaction is eliminated and a constant switching frequency is guaranteed.

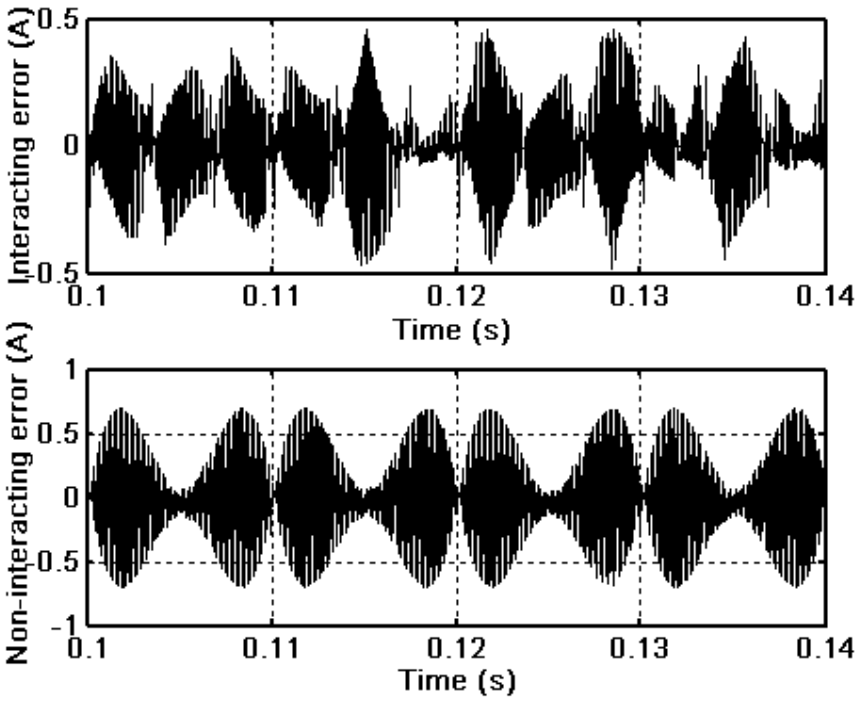


Fig. 5.16 Rectifier supply current interacting error (upper trace) and non-interacting error (lower trace)

The rectifier supply current FFTs obtained from Fig. 5.13 (upper trace) and Fig. 5.14 (upper trace) for conventional hysteresis current control and variable hysteresis band current control are shown in Fig. 5.17 and Fig. 5.18 respectively. In conventional hysteresis current control, the supply current harmonics are distributed within a wide frequency spectrum from hundreds of Hertz to several kilohertz. However, for variable hysteresis band current control, a switching frequency is held at 7 kHz in this case, and thus the supply current harmonics are concentrated around 7 kHz frequency. This is a major advantage in converter design and operation. High frequency harmonics result in smaller L-C components in terms of size and ratings. Moreover, absence of low frequency harmonics avoids possible resonance between tuned ac filters and the ac network, especially hazardous at lower frequency around 50 Hz. Additional advantage

includes the possibility of replacing a tuned filter by a high-pass one with much lower KVA rating, because of the absence of a resonance problem.

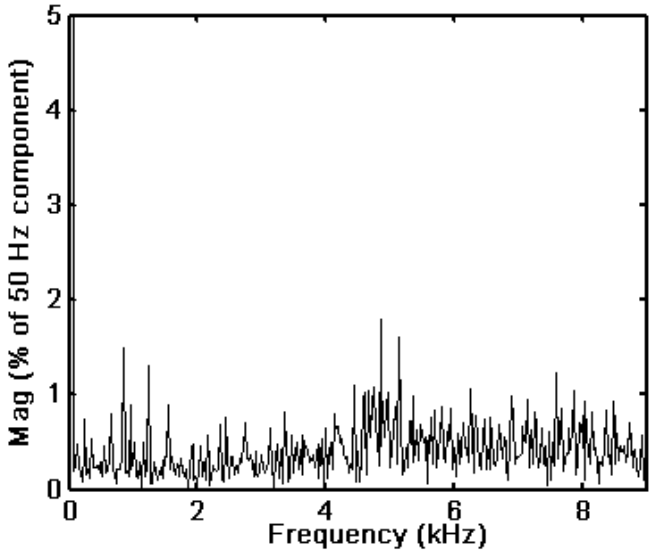


Fig. 5.17 Rectifier supply current FFT for conventional hysteresis current control

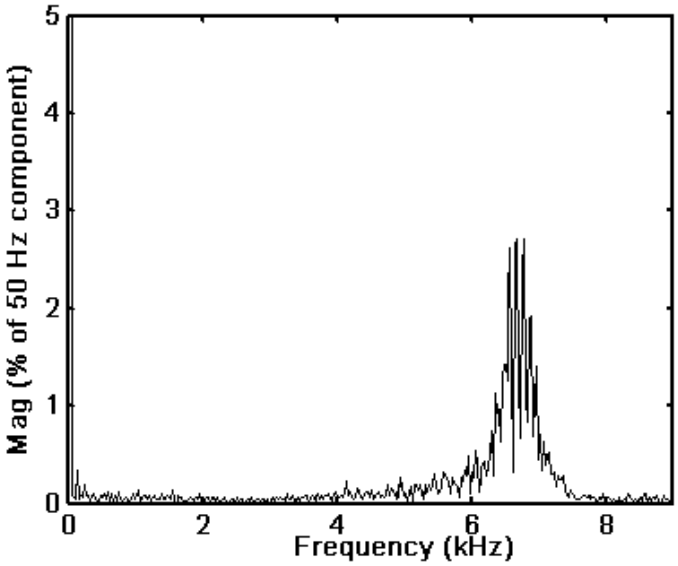
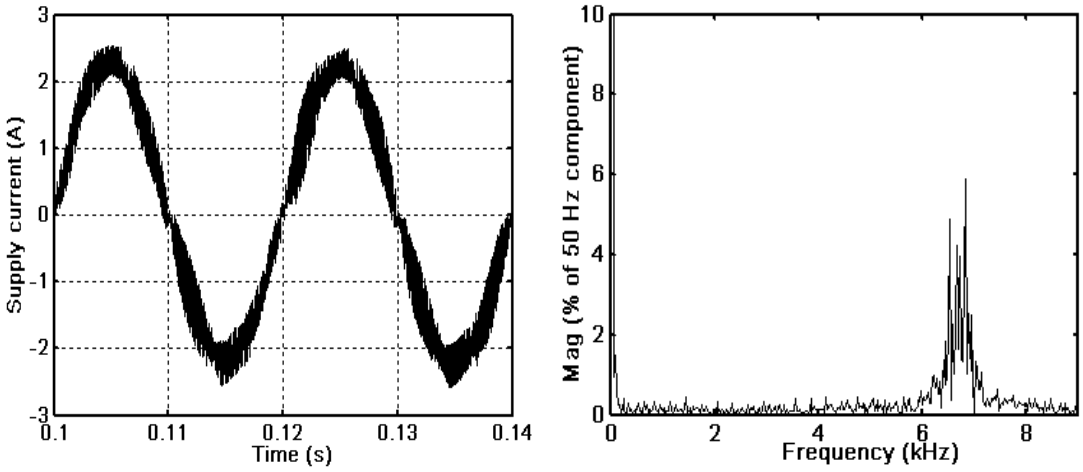


Fig. 5.18 Rectifier supply current FFT for variable hysteresis band current control

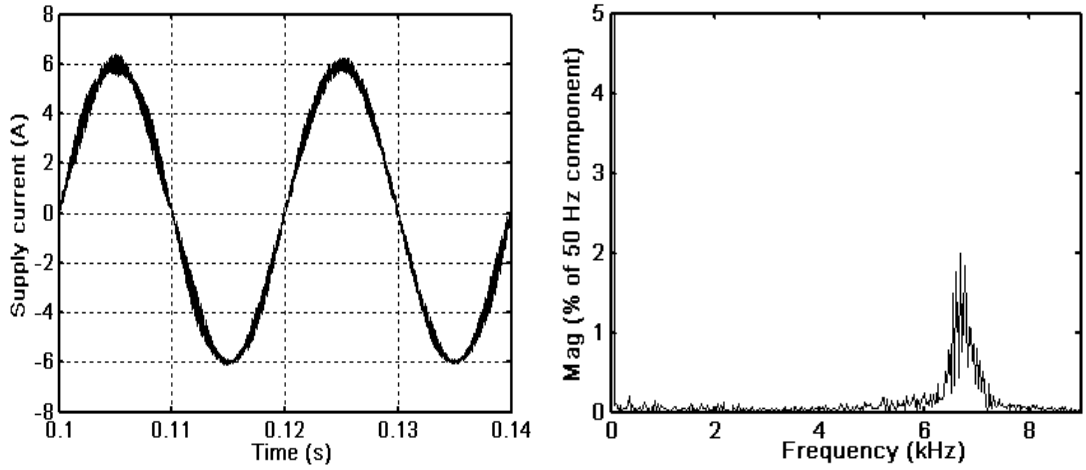
In order to test the feasibility of this kind of current control strategy under various load conditions, the rectifier is also operated at below and above its rated power. The converter supply currents and current FFTs at 50% and 150% rated output power are shown in Fig. 5.19 and Fig. 5.20 respectively. A general degradation of the supply

current THD when the rectifier operate at low power conditions. However, the current THD at 50% rectifier rated output power is less than 8% and still acceptable. We can also see that the current main harmonics at 50% and 150% rated rectifier output power are both concentrated around 7 kHz. It is evident that variable hysteresis band current control has a good adaptability to different load conditions. Since implication of (5-16) is universal, this technique can be also used for rectifiers operating at other switching frequencies and rectifiers operating at various rated power levels.



(a) Current waveform (b) Current FFT

Fig. 5.19 Rectifier supply current under 50% rated output power

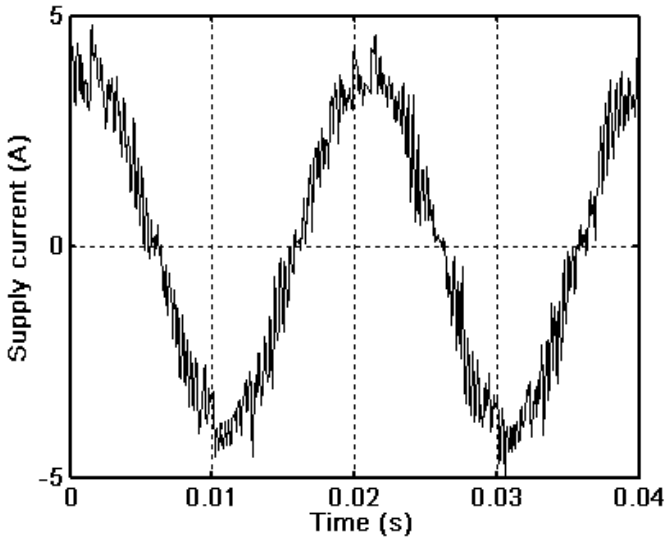


(a) Current waveform (b) Current FFT

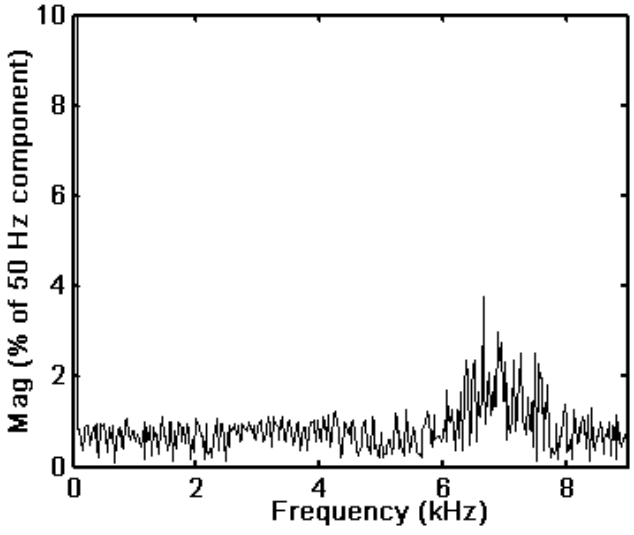
Fig. 5.20 Rectifier supply current under 150% rated output power

The operation of the proposed variable hysteresis band current control has also been verified by experiment. The supply current and its FFT under rectifier rated output power,

obtained from ds1103 based controller, are shown in Fig. 5.21. We can see that the main current harmonics are centralized around 7 kHz. In order to show the relative position of the rectifier supply current with respect to its corresponding voltage, both waveforms are captured online using a Fluke-43 power quality analyzer as shown in Fig. 5.22. The readings show a unity displacement factor with a high input power factor of 0.99 and virtually no reactive power.



(a) Current waveform



(b) Current FFT

Fig. 5.21 Rectifier supply current under rated output power (experimental)

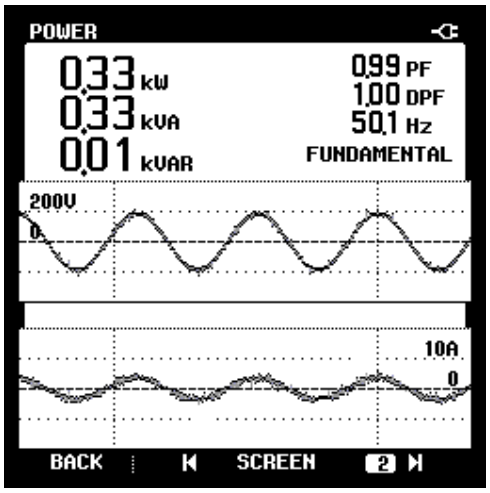
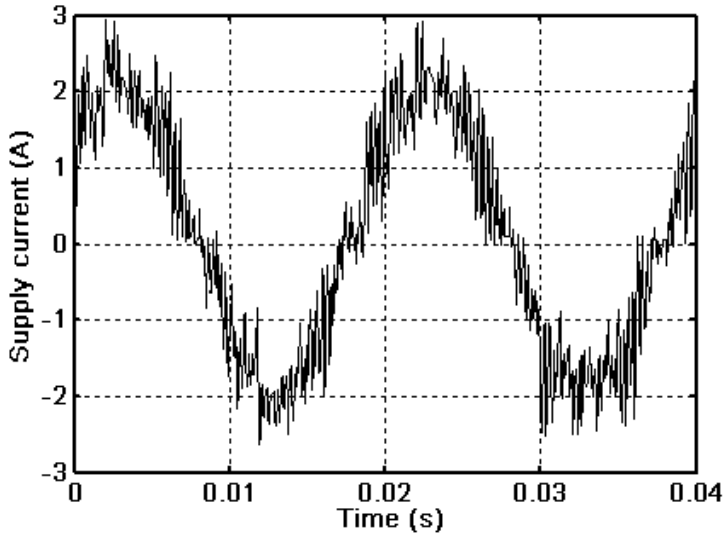
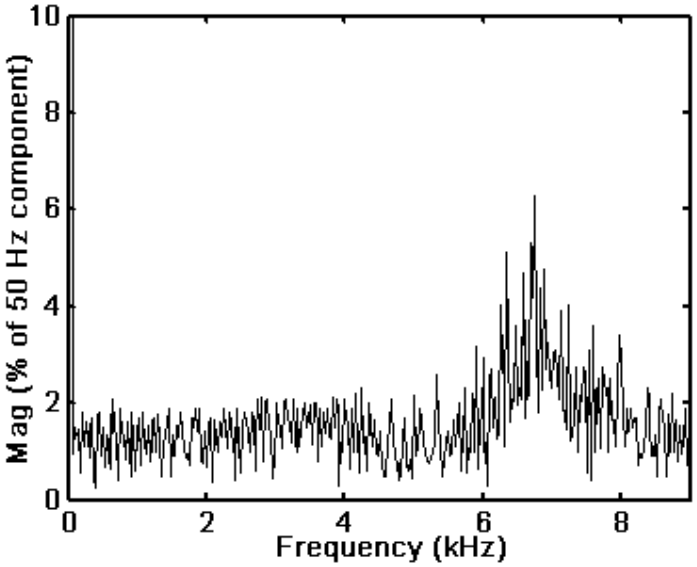


Fig. 5.22 Rectifier supply current and voltage under rated output power

The rectifier supply current waveform and its spectrum under 50% rated output power are shown in Fig. 5.23. Although the rectifier supply current becomes more distorted at low power output, the current spectrum harmonics are still concentrated around 7 kHz. The corresponding rectifier supply voltage and current waveform along with its performance parameters are shown in Fig. 5.24. We can see that the rectifier input power factor is still as high as 0.98. The reduction of PF is mainly due to increase in distortion of the supply current waveform at light load as is evident in Fig. 5.23 (b). The displacement factor is still at 1 and no phase shift between voltage and current occurs.



(a) Current waveform



(b) Current FFT

Fig. 5.23 Rectifier supply current under 50% rated output power (experimental)

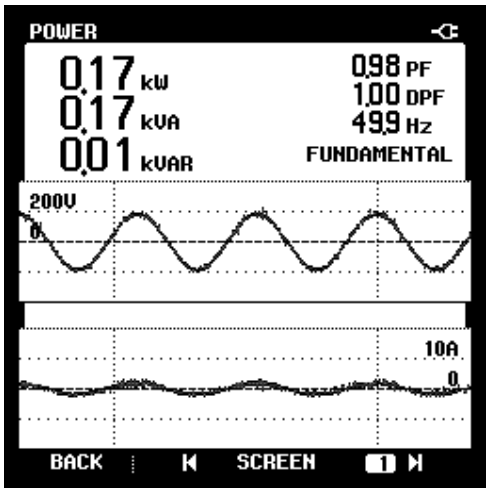
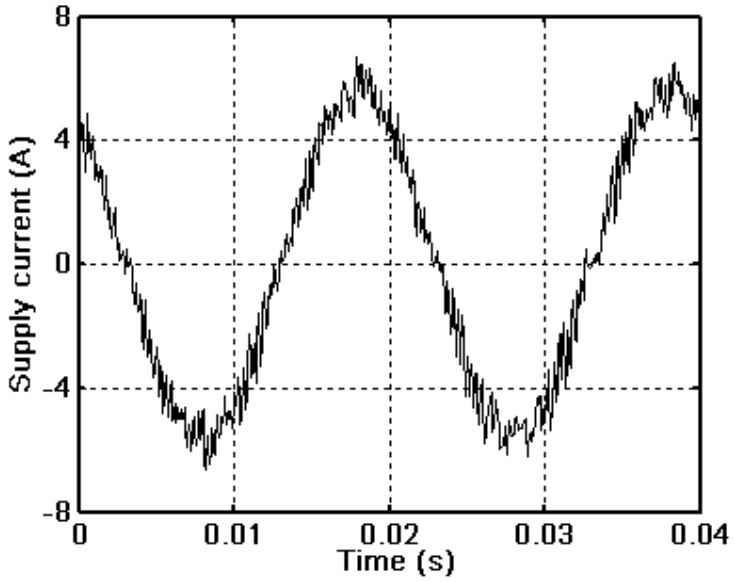
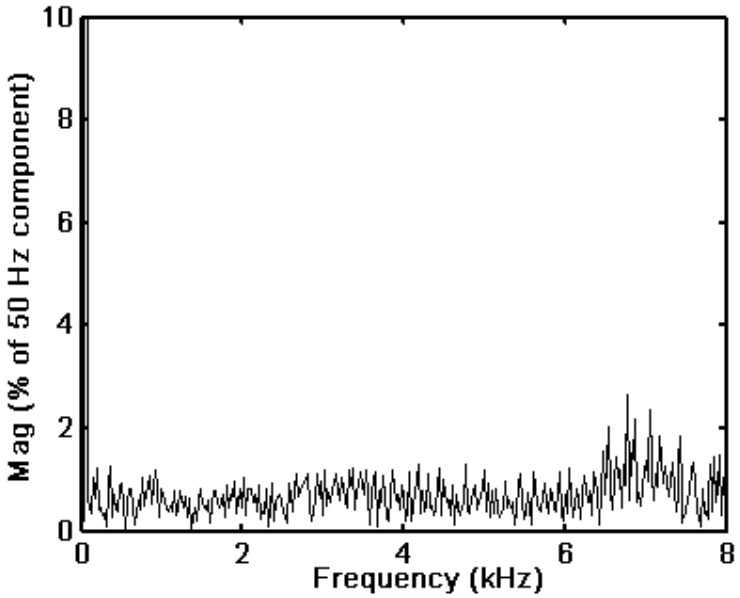


Fig. 5.24 Rectifier supply current and voltage under 50% rated output power

The rectifier supply current waveform and its spectrum under 150% rated output power are shown in Fig.5.25. The current waveform is less distorted and the current harmonic spectrum is also concentrated around 7 kHz. The corresponding rectifier supply voltage and current waveform along with its performance parameters are shown in Fig. 5.26. The converter input power factor is as high as 0.99.



(a) Current waveform



(b) Current FFT

Fig. 5.25 Rectifier supply current under 150% rated output power (experimental)

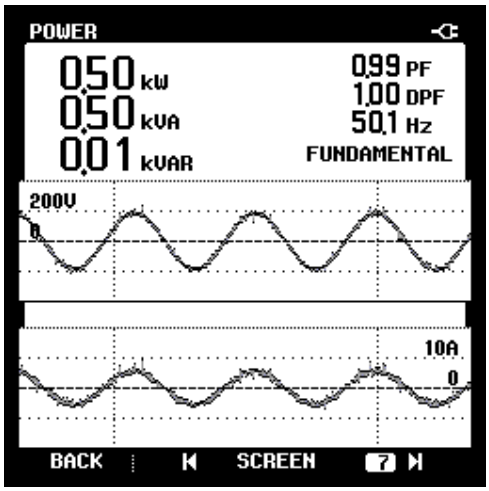


Fig. 5.26 Rectifier supply current and voltage under 150% rated output power

5.4 Concluding remarks

Conventional hysteresis current control strategy shows a high performance for the three-phase three-level rectifier. However, the switching frequency is random, resulting in an unpredictable supply current harmonic spectrum. Average current control, a popular strategy among constant switching frequency current modulation techniques can be applied for same topology with much better results. The performance of the converter under these two kinds of current modulation techniques is compared. Although the average current control technique can overcome the drawbacks of random switching frequency that the hysteresis current control exhibits, it does so at a higher switching frequency. Hence, a novel variable hysteresis band current controller for the three-phase three-level rectifier operating at constant switching frequency is proposed in this chapter. The proposed controller performs by creating a variable hysteresis band envelope, and then compensating for the interaction between phases that occurs when the middle point of dc link capacitors is floating. The proposed controller also exhibits a good adaptability to sudden load variations. The three-phase rectifier with the proposed controller shows features of unity power factor, high reliability and simple control.

Chapter 6

Conclusion and Recommendations

6.1 Conclusion

Modern power electronic load such as electrical motor drives, uninterruptible power supplies (UPS) in emergency and standby systems, etc., employ a three-phase rectifier. However the rectifier interfaced to the electrical utility exhibits nonlinear characteristics with poor input power factor. Moreover, due to the nonlinear nature, the rectifier injects significant harmonic currents into the utility lines resulting in a number of undesirable effects. Therefore, the front-end converter at present day is required to be harmonic-free, preferably at near unity power factor and highly efficient.

The existing principal types of three-phase rectifier topologies are firstly analyzed and their advantages and disadvantages compared. Conventional diode and phase-controlled rectifier operation yields the characteristics of simplicity and easy implementation, while causing large low order harmonics in the input line currents. PWM rectifier is attractive due to the capability of regenerate power, near sinusoidal input current and controllable dc link voltage. However, it has the drawbacks of high cost, high switching losses and complicated control algorithm. Various methods of improving input power factor and reducing current harmonics are also classified and reviewed.

A recently developed near unity power factor rectifier topology operating at low frequency was analyzed in detail and modeled with accurate mathematical equations. Based on this, an intelligent controller is proposed for the intended rectifier-inverter structure to operate within a wide load range and large variation of the input inductance and supply voltages. All former rectifier-inverter structures were restricted because of their requirement of large input inductances to achieve a near unity power factor. A 1.5 kW experimental prototype was built and it successfully verified the initial design. In general it was found that such a converter, operating at a low switching frequency (two

times the line frequency of 50/60 Hz), will be an excellent energy saver and a power factor enhancer for mid to high power applications.

A similar rectifier topology operating at high switching frequency is also investigated and modeled supported by detailed mathematical equations. A synchronous reference frame based hysteresis current controller is proposed for the rectifier bidirectional switches to make the proposed rectifier-inverter structure perform effectively under unbalanced and distorted supply voltage conditions, a possibility prevalent especially in developing countries. A 1 kW laboratory prototype was also built and the experimental results matched the predicted analytical and simulation results very well. Such a current controlled converter is found to be suitable for mostly low power applications.

Table 6.1 Comparison of the rectifier working at low and high frequency

Operation mode	Low frequency (2X line frequency described in Chapter 3)	High frequency (with hysteresis current control described in Chapter 4)
Input inductance (p. u.)	0.242	0.033
Dc link voltage (p. u.)	1.3366 (fixed)	1.68 (variable)
Input current THD (%)	5.0%	4.4%
Input power factor	0.99	0.99
Bidirectional kVA rating (p. u.)	0.051	0.156

The performance of the rectifier working at low and high frequency under rated output power is compared and the performance parameters are listed in Table 6.1. Input line to line voltage and rated output power are the base quantities in p. u. calculation. Although the input current THD and power factor are similar, the input inductance is different. A higher switching frequency will result in a significant reduction of the input inductor size. The bidirectional switch kVA ratings will also increase significantly due to the higher

switching frequency. The rectifier working at low frequency requires an optimal input inductance of 0.242 p.u.. The converter can still achieve a good performance even with the input inductance variation of ±10% range. When the converter operating at high frequency, the converter has no special requirements of input inductance. Although the required input inductance is rather large under low frequency operation, the input inductors can be assembled using ordinary silicon-steel material for the cores. The cost of low frequency core material is also insignificant in contrast to the high-frequency core material used for building high frequency inductors. The bidirectional switching kVA rating even under high frequency operation is 15.6% of rated load power. Low cost switches can be used. Furthermore, the voltage stress across the bidirectional switch is clamped to half of dc output voltage by the dc link capacitors and no clamping circuits are necessary. The dc link voltage under lower switching frequency is fixed. However, the rectifier under high switching frequency provides a higher dc link voltage and this voltage is tunable. The rectifier with low switching frequency operation is suitable for mid to high power application (i.e., from 8 kW-50 kW). However, when it is operated at high switching frequency, it is suitable for low to mid power application (i.e.1 kw-10 kw). Table 6.1 provides a comprehensive reference for the customer to choose the rectifier operation mode.

The rectifier under commonly used hysteresis current control (random switching frequency) and average current control (fixed switching frequency) is tested and compared. The average current control yields slightly higher input line current performance parameters compared to its hysteresis counterpart under equal conditions of permissible input current distortion. However, this is achieved at the cost of higher switching frequency. Finally a variable hysteresis band current control with constant switching frequency is proposed for the rectifier. This technique overcomes all the drawbacks of the popular conventional hysteresis current control and average current control strategies, and smoothly operates at constant switching frequency. Such features are greatly sought after for lack of low frequency resonance possibility, and low filter KVA ratings. This variable hysteresis band current control technique was also implemented for a typical 1 kW rated three-phase three-level rectifier. The experimental results successfully verified the initial design, and it shows that this technique is easy to implement and is quite suitable for practical use.

6.2 Recommendations for further research

The aim of this project was to study and develop a near unity power factor converter for power quality application. In this work, few key areas have been thoroughly investigated. Hence, it is also worthwhile to mention some other related supplementary areas that are worth looking into.

Even though a near unity power factor rectifier-inverter structure prototype has been successfully developed, there are always rooms for improvement. The front-end converter, coupled with different control methods and current modulation techniques, is suitable for both low and high power applications. However, only an open-loop control is currently adopted for the rear-end inverter. A close loop control should be designed for the rear-end inverter to make the proposed rectifier-inverter ac drive suitable for more sophisticated application.

The bidirectional switch current ratings under both low frequency and high frequency operation are mentioned in this work. It's worth further investigating the switching losses of the main circuit including the rear-end PWM inverter. This will help to give some specifications for switching devices selection and improve the converter efficiency. When the rectifier bidirectional switches operate at a high switching frequency, the switch KVA increases significantly compared to it's counterpart at low frequency and switching losses will increase accordingly. High switching frequency also causes electro magnetic interference (EMI) due to large di/dt and dv/dt. And these shortcomings are exacerbated if the switching frequency is increased in order to reduce the converter size and weight. It may be interesting to investigate the effect of zero-voltage/zero-current switching technique in the proposed converter, especially in the rear-end PWM inverter.

The proposed rectifier-inverter structure is capable of functioning well over a wide load range and offers a good dc link voltage regulation. Moreover, it exhibits stable operation under supply voltage distortion, and has a good adaptability to a sudden load change. However, one should further investigate the converter's ride-through capability under voltage dip, or even during a short power outage. Voltage dip, a typical power quality

problem, effects a wide range of ASDs. Thus, it is essential to improve the converter's ride-through capability for industry customer to overcome such detrimental effects.

The power flow of the rectifier in this research work is unidirectional, resulting in a lower cost compared with bidirectional power flow rectifiers. It may also be worthwhile to introduce bidirectional power flow capability in the proposed converter. Another attractive application of this near unity power factor converter would be in the field of uninterruptible power supplies (UPS).

Author's Publications

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2 A. I. Maswood and F. Liu, "A novel unity power factor input stage for ac drive application", *IEEE Transactions on Power Electronics*, vol. 20, no. 4, July 2005, pp. 839-846.

3 A. I. Maswood and F. Liu, "A novel variable hysteresis band current control of three phase three-level rectifier with constant switching frequency", *IEEE Power Engineering Society General Meeting*, San Francisco, USA, June 2005.

4 A. I. Maswood and F. Liu, "A unity power factor converter using the synchronous reference frame based hysteresis current control", *20th Applied Power Electronics Conference and Exposition*, Austin, USA, March 2005, pp. 1667-1673.

5 F. Liu and A. I. Maswood, "A novel near-unity power factor ac drive", *5th International Conference on Power Electronics and Drive Systems*, Singapore, November 2003, pp. 1090-1094.

6 A. I. Maswood and F. Liu, "A unity power factor converter using the synchronous reference frame based hysteresis current control", *IEEE Transactions on Industry Applications* (under review).

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Appendix A

Two DC-Link Capacitors Voltage Balance Verification

The front-end converter with low frequency controlled bidirectional switches is shown in Fig. A1. Since two identical capacitors are selected as Ca and Cb, input voltages are balanced and the bidirectional switches conduction periods are usually balanced, the voltage across Ca and Cb are expected to be equal.

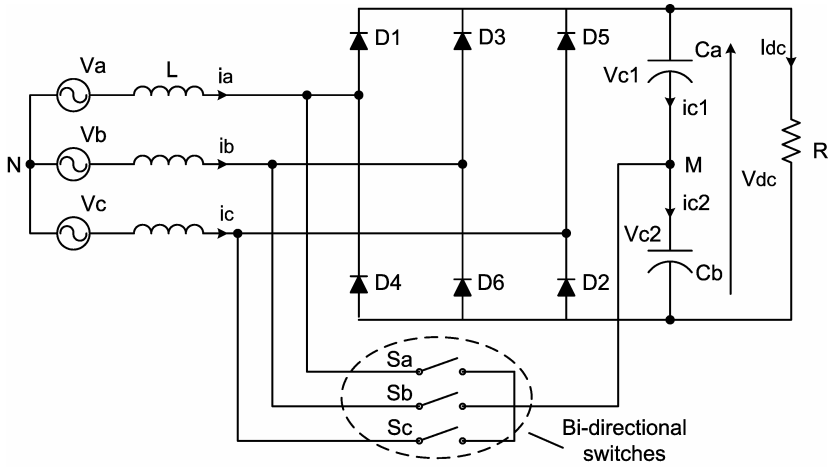

Fig. A1 The front-end converter with three bidirectional switches

Switch Sa conducts at interval $0-\alpha$ and $\pi-(\pi+\alpha)$, where

$$i_{c2} = i_{c1} + i_a \tag{A1}$$

Switch Sb conducts at interval $\frac{2\pi}{3}-(\frac{2\pi}{3}+\alpha)$ and $\frac{5\pi}{3}-(\frac{5\pi}{3}+\alpha)$, where

$$i_{c2} = i_{c1} + i_b \tag{A2}$$

Switch Sc conducts at interval $\frac{\pi}{3}-(\frac{\pi}{3}+\alpha)$ and $\frac{4\pi}{3}-(\frac{4\pi}{3}+\alpha)$, where

$$i_{c2} = i_{c1} + i_c \tag{A3}$$

When three bidirectional switches are all off, the currents of two capacitors are the same. The net change of capacitor a voltage in one line voltage cycle can be expressed as:

$$\Delta v_{c1} = \frac{1}{C}\int_0^{2\pi} i_{c1}(\omega t)d\omega t \tag{A4}$$

The net change of capacitor b voltage in one line voltage cycle can be expressed as:

$$\Delta v_{c2} = \frac{1}{C}\int_0^{2\pi} i_{c2}(\omega t)d\omega t = \frac{1}{C}\int_0^{2\pi} i_{c1}(\omega t)d\omega t + \frac{1}{C}\int_0^{\alpha} i_a(\omega t)d\omega t + \frac{1}{C}\int_{\pi}^{\pi+\alpha} i_a(\omega t)d\omega t + \frac{1}{C}\int_{2\pi/3}^{2\pi/3+\alpha} i_b(\omega t)d\omega t + \frac{1}{C}\int_{5\pi/3}^{5\pi/3+\alpha} i_b(\omega t)d\omega t + \frac{1}{C}\int_{\pi/3}^{\pi/3+\alpha} i_c(\omega t)d\omega t + \frac{1}{C}\int_{4\pi/3}^{4\pi/3+\alpha} i_c(\omega t)d\omega t \tag{A5}$$

For the input current waveforms have half wave symmetry, one can get:

$$i_a(\omega t) = -i_a(\pi + \omega t) \tag{A6}$$

$$i_b(\omega t) = -i_b(\pi + \omega t) \tag{A7}$$

$$i_c(\omega t) = -i_c(\pi + \omega t) \tag{A8}$$

So ΔVc2 can be reformed as:

$$\Delta v_{c2} = \frac{1}{C}\int_0^{2\pi} i_{c1}(\omega t)d\omega t = \Delta v_{c1} \tag{A9}$$

Thus the two capacitor average voltages are equal.

Appendix B

Operation Principle of PLL

The basic configuration of the PLL (phase locked loop) system is shown in Fig. B1. V_a, V_b and V_c are sampled input three-phase voltages. These stationary reference frame voltages are transformed to voltage V_d , V_q (in a rotating frame of reference synchronized to utility frequency) using the 3/2 and s/r transformations. The angle θ^* used in these transformation is obtained by integrating a frequency command ω^*. If the frequency command ω^* is identical to the utility frequency, the voltages V_d and V_q appear as dc values depending on the angle θ^*.

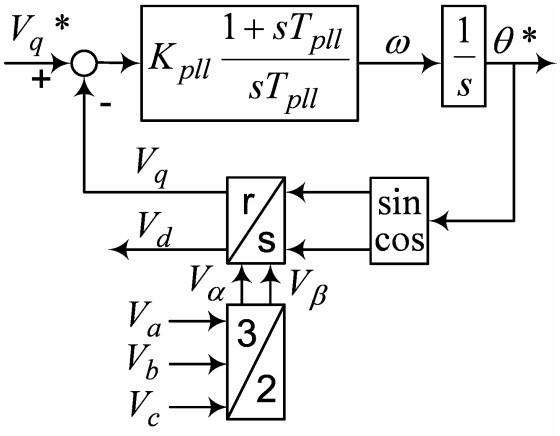

Fig. B1 Control diagram of phase control loop

A PI regulator is used to obtain that value of θ^* (or ω^*) which drives the feedback voltage V_q to a command value V_q^*. The magnitude of the controlled quantity V_q determines the phase difference between the utility voltage and $\sin(\theta^*)$ or $\cos(\theta^*)$. The method results not only in the utility frequency but also allows one to lock at arbitrary phase angle θ^* with respect to the utility angle θ. The angle $\Delta\theta$ $(\theta-\theta*)$ is controlled by the commanded value V_q^*.

The sampled voltage V_a, V_b and V_c when transformed to the synchronous frame of reference result in the quadrature voltages V_d and V_q (as shown in Fig. B1). In the PLL presented here, only a single control loop is closed around V_d. Assuming a balanced three-phase system, a simplified control model of the PLL can be developed using the following transformations [83]:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} V\cos(\theta) \\ V\cos(\theta - 2\pi/3) \\ V\cos(\theta + 2\pi/3) \end{bmatrix} \tag{B1}$$

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} V_a \\ (V_c - V_b)/\sqrt{3} \end{bmatrix} \tag{B2}$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos\theta^* & -\sin\theta^* \\ \sin\theta^* & \cos\theta^* \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{B3}$$

Substituting (B1) and (B2) in (B3), the voltages V_d and V_q are given by (B4):

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = V\begin{bmatrix} \cos(\theta^* - \theta) \\ \sin(\theta^* - \theta) \end{bmatrix} = V\begin{bmatrix} \cos(\Delta\theta) \\ \sin(\Delta\theta) \end{bmatrix} \tag{B4}$$

If the error $\Delta\theta$ between the utility angle θ and the PLL output θ^* is set to zero, $V_d = V$ and $V_q = 0$. This offers immediate possibility to lock onto the utility voltage by regulation of V_q to zero. No information is needed about the magnitude V of the utility voltage.

Properly selecting the PI controller parameters with the method in [83], the three-phase PLL system can operate even under supply voltage distortion and unbalanced conditions.

Appendix C

Hardware Components

The hardware components used in this project are list in Table C1.

Table C1 Hardware Components

Name	Model No.
Diode Rectifier	SKD 33/08
Inverter Bridge	SKM 50GB 123D
IGBT of Bidirectional Switch	IRG4PC40F
Diode of Bidirectional switch	STTA1206D
Bidirectional Driver Board	SKHI10
Inverter Driver Board	SKHI60
DSP Controller	DS 1102/1103 PPC Controller Board

The components datasheet are available on the following websites:

http://ec.irf.com/v6/en/US/adirect/ir?cmd=catNavigateFrame

http://www.semikron.com/internet/index.jsp?sekId=12

http://www.dspace.de/ww/en/pub/products/ace_kits/ace_kit_1103.htm

Appendix D

DS 1103 PPC Controller Board

Key Features

- **Single-board system with comprehensive I/O**
- **CAN interface and serial interfaces**
- **Interfaces for connecting incremental encoders**
- **High I/O speed and accuracy**
- **PWM-synchronous or externally triggered I/O strobe**
- **32 MB application memory**
- **PLL-driven UART for accurate baud rate selection**

Description

Key Benefits

The DS1103 PPC Controller Board is an all-rounder in rapid control prototyping. You can mount the board in a PC or a dSPACE AutoBox to test your control functions in a laboratory or directly in the vehicle. Its processing power and fast I/O are vital for applications that involve numerous actuators and sensors. Used with Real-Time Interface (RTI), the DS1103 is fully programmable from the Simulink block diagram environment. You can configure all I/O graphically by dragging RTI blocks (p. 214). Hence, your control functions can be implemented on the board quickly and easily.

Application Areas

The DS1103 is designed to meet the requirements of modern rapid control prototyping and is highly suitable for applications such as:

- Induction motor control
- Robotics
- Positioning systems and stepper motors
- Active vibration control
- Rapid control prototyping for automotive controllers

Comprehensive and Renewed Interfaces

The unparalleled number of I/O interfaces makes the DS1103 a versatile controller board for numerous applications. It provides a great selection of interfaces, including 50 bit-I/O channels, 36 A/D channels, and 8 D/A channels. For additional I/O tasks, a DSP controller unit built around Texas Instruments' TMS320F240 DSP is used as a subsystem. The control of electrical drives requires accurate recording and output of I/O values. It is possible to synchronize the A/D channels and D/A channels, and the position of the incremental encoder interface, with an internal PWM signal or an external trigger signal. Also, the serial interface (UART) is driven by a phase-locked loop to achieve absolutely accurate baud rate selection.

Technical Details

Parameter		Specification
Processor	PowerPC Type	■ PPC750GX
	CPU clock	■ 933 MHz
	Cache	■ 32 KB level 1 (L1) instruction cache ■ 32 KB level 1 (L1) data cache ■ 1 MB level 2 (L2)
Memory	Local memory	■ 32 MB application SDRAM as program memory, cached
	Global memory	■ 96 MB communication SDRAM for data storage and data exchange with host
Timer	2 general-purpose timers	■ One 32-bit down counter ■ Reload by software ■ 15 ns resolution
		■ One 32-bit up counter with compare register ■ Reload by software ■ 30 ns resolution
	1 sampling rate timer (decrementer)	■ 32-bit down counter ■ Reload by software ■ 30-ns resolution
	1 time base counter	■ 64-bit down counter ■ 30-ns resolution
Interrupt controller		■ 3 timer interrupts ■ 7 incremental encoder index line interrupts ■ 1 UART interrupt ■ 1 CAN interrupt ■ 1 slave DSP interrupt ■ 2 slave DSP PWM interrupts ■ 1 host interrupt ■ 4 external interrupts (user interrupts)
A/D converter	Channels	■ 16 multiplexed channels equipped with 4 sample & hold A/D converters ■ 4 parallel channels each equipped with one sample & hold ADC
	Resolution	■ 16-bit
	Input voltage range	■ ±10 V
	Overvoltage protection	■ ±15 V
	Conversion time	■ Multiplexed channels: 1 µs [1)] ■ Parallel channels: 800 ns [1)]
	Offset error	■ ±5 mV
	Gain error	■ ±0.25%
	Offset drift	■ 40 µV/K
	Gain drift	■ 50 ppm/K
	Signal-to-noise-ratio	■ >83 dB
D/A converter	Channels	■ 8 channels
	Resolution	■ 16-bit
	Output range	■ ±10 V
	Settling time	■ 5 µs (14 bits) [*)]
	Offset error	■ ±1 mV
	Gain error	■ ±0.5%
	Offset drift	■ 30 µV/K
	Gain drift	■ 25 ppm/K
	Signal-to-noise-ratio	■ >83 dB
	Imax	■ ±5 mA
	Cimax	■ 10 nF

Parameter		Specification
Digital I/O	Channels	■ 32-bit parallel I/O ■ Organized in four 8-bit groups ■ Each 8-bit group can be set to input or output (programmable by software)
	Voltage range	■ TTL input/output levels
	Ioutmax	■ ±10 mA
Digital incremental encoder interface	Channels	■ 6 independent channels ■ Single-ended (TTL) or differential (RS422) input (software programmable for each channel)
	Position counters	■ 24-bit resolution ■ Max. 1.65 MHz input frequency, i.e. fourfold pulse counts up to 6.6 MHz ■ Counter reset or reload via software
	Encoder supply voltage	■ 5 V/1.5 A ■ Shared with analog incremental encoder interface
Analog incremental encoder interface	Channels	■ 1 channel ■ Sinusoidal signals: 1 V_{pp} differential or 11 μA_{pp} differential (software programmable)
	Position counters	■ < 5° resolution ■ 32-bit loadable position counter ■ Max. 0.6 MHz input frequency, i.e., fourfold pulse counts up to 2.4 MHz
	A/D converter performance	■ 6-bit resolution ■ 10 MSPS
	Encoder supply voltage	■ 5 V/1.5 A ■ Shared with digital incremental encoder interface
CAN interface	Configuration	■ 1 channel based on SAB 80C164 microcontroller ■ ISO DIN 11898-2 CAN high-speed standard
	Baud rate	■ Max. 1 Mbit/s
Serial interface	Configuration	■ TL6C550C single UART (universal asynchronous receiver and transmitter) with FIFO ■ PLL-driven UART for accurate baud rate selection ■ RS232/RS422 compatibility
	Baud rate	■ Up to 115.2 Kbaud (RS232) ■ Up to 1 Mbaud (RS422)
Slave DSP	Type	■ Texas Instruments TMS320F240 DSP
	Clock rate	■ 20 MHz
	Memory	■ 64Kx16 external code memory ■ 28Kx16 external data memory ■ 4Kx16 dual-port memory for communication ■ 32 KB flash memory
	I/O channels	■ 16 A/D converter inputs ■ 10 PWM outputs ■ 4 capture inputs ■ 2 serial ports
	Input voltage range	■ TTL input/output level ■ A/D converter inputs: 0 … 5 V
	Output current	■ Max. ±13 mA
Host interface		■ Eight 16-bit I/O ports in the 64K host I/O space ■ Processor/host and host/processor interrupts ■ Plug & Play support ■ Requires a full-size 16-bit ISA slot
Physical characteristics	Physical size	■ 340 x 125 x 45 mm (13.4 x 4.9 x 1.77 in)
	Ambient temperature	■ 0 … 50 °C (32 … 122 °F)
	Cooling	■ Passive cooling
	Power supply	■ +5 V ±5%, 4 A ■ +12 V ±5%, 750 mA ■ -12 V ±5%, 250 mA

Appendix E

Variable Hysteresis Band Current Controller Implementation with DS 1103 PPC Controller Board

Variable hysteresis band current controller is first built in Matlab Simulink environment, compiled and downloaded to DS 1103 PPC Controller Board. The following figures and programs show the Simulink model of variable hysteresis band current controller.

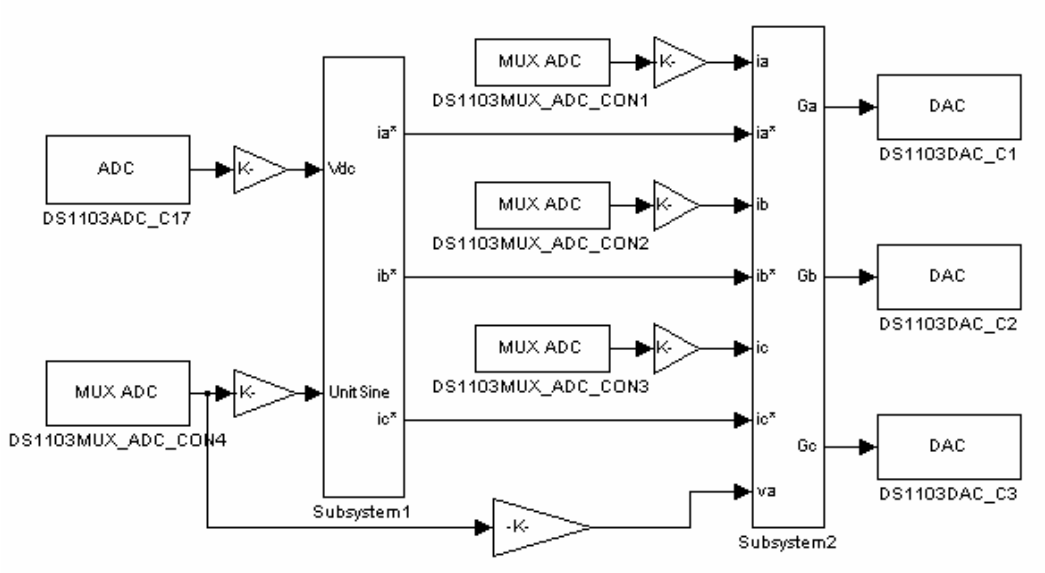

Fig. E1 Variable hysteresis band current controller overview

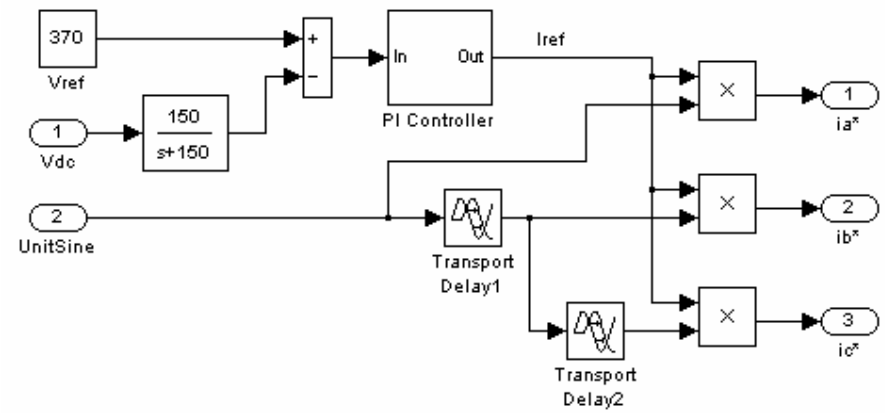

Fig. E2 Subsystem1

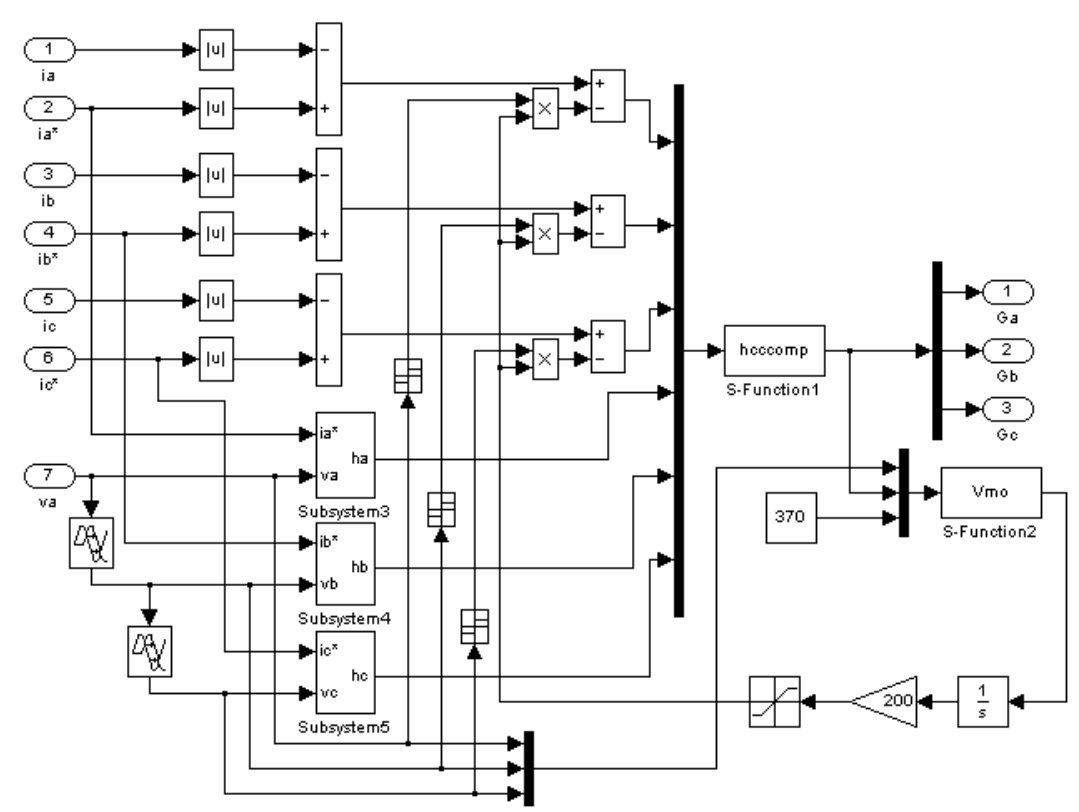

Fig. E3 Subsytem2

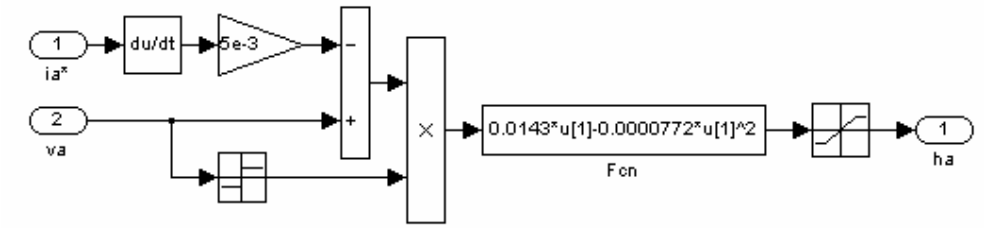

Fig. E4 Subsytem3

S Function of “hcccomp”:

```
/*
   hccomp: variable hysteresis band comparator
   Input 1,2,3: three-phase current errors; input 4,5,6: hysteresis bands (h1,h2,h3);
   Output 1,2,3: gating signals for Sa, Sb, Sc respectively
*/
//
#define S_FUNCTION_LEVEL 2
#define S_FUNCTION_NAME  hcccomp

/*
```

```
 * Need to include simstruc.h for the definition of the SimStruct and
 * its associated macro definitions.
 */
#include "simstruc.h"

/* Function: mdlInitializeSizes ===============================================
 * Abstract:
 *    The sizes information is used by Simulink to determine the S-function
 *    block's characteristics (number of inputs, outputs, states, etc.).
 */
static void mdlInitializeSizes(SimStruct *S)
{
   ssSetNumSFcnParams(S, 0);  /* Number of expected parameters */
   if (ssGetNumSFcnParams(S) != ssGetSFcnParamsCount(S)) {
      /* Return if number of expected != number of actual parameters */
      return;
   }

   ssSetNumContStates(S, 0);
   ssSetNumDiscStates(S, 0);

   if (!ssSetNumInputPorts(S, 1)) return;
   ssSetInputPortWidth(S, 0, 6);
   ssSetInputPortDirectFeedThrough(S, 0, 1);

   if (!ssSetNumOutputPorts(S, 1)) return;
   ssSetOutputPortWidth(S, 0, 3);

   ssSetNumSampleTimes(S, 1);
   ssSetNumRWork(S, 3);
   ssSetNumIWork(S, 0);
   ssSetNumPWork(S, 0);
   ssSetNumModes(S, 0);
   ssSetNumNonsampledZCs(S, 0);

   ssSetOptions(S, 0);
}

/* Function: mdlInitializeSampleTimes =========================================
 */
static void mdlInitializeSampleTimes(SimStruct *S)
{
   ssSetSampleTime(S, 0, INHERITED_SAMPLE_TIME);
   ssSetOffsetTime(S, 0, 0.0);
}

#define MDL_INITIALIZE_CONDITIONS   /* Change to #undef to remove function */
#if defined(MDL_INITIALIZE_CONDITIONS)
 /* Function: mdlInitializeConditions ========================================
  */
 static void mdlInitializeConditions(SimStruct *S)
 {
            real_T             *Rwork = ssGetRWork(S);
                  Rwork[0] = 0;
                  Rwork[1] = 0;
    Rwork[2] = 0;
 }
#endif /* MDL_INITIALIZE_CONDITIONS */

/* Function: mdlOutputs =======================================================
```

```
 */
static void mdlOutputs(SimStruct *S, int_T tid)
{
          InputRealPtrsType          uPtrs = ssGetInputPortRealSignalPtrs(S,0);
          real_T                              *y = ssGetOutputPortRealSignal(S,0);
          real_T                              *Rwork = ssGetRWork(S);
  real_T                              k0,k1,k2;
  real_T          m0,m1,m2;

  k0=Rwork[0];
  k1=Rwork[1];
  k2=Rwork[2];
  m0=*uPtrs[3];
  m1=*uPtrs[4];
  m2=*uPtrs[5];

  if (*uPtrs[0]>=m0)
    {  y[0]=1;      }
  else if (*uPtrs[0]<=-m0)
    {  y[0]=0;      }
  else
    {  y[0]=k0;     }

  if (*uPtrs[1]>=m1)
    {  y[1]=1;      }
  else if (*uPtrs[1]<=-m1)
    {  y[1]=0;      }
  else
    {  y[1]=k1;     }

  if (*uPtrs[2]>=m2)
    {  y[2]=1;      }
  else if (*uPtrs[2]<=-m2)
    {  y[2]=0;      }
  else
    {  y[2]=k2;     }

  Rwork[0]=y[0];
  Rwork[1]=y[1];
  Rwork[2]=y[2];

}

/* Function: mdlTerminate =====================================================
 * Abstract:
 *    In this function, you should perform any actions that are necessary
 *    at the termination of a simulation.  For example, if memory was
 *    allocated in mdlInitializeConditions, this is the place to free it.
 */
static void mdlTerminate(SimStruct *S)
{
}

#ifdef  MATLAB_MEX_FILE    /* Is this file being compiled as a MEX-file? */
#include "simulink.c"      /* MEX-file interface mechanism */
#else
#include "cg_sfun.h"       /* Code generation registration function */
#endif
```

S function of "Vmo"

```
/*
   Input: the three-phase voltages and bi-directional switching patterns.
   Output: the capacitive middle point voltage.
*/
//
#define S_FUNCTION_LEVEL 2
#define S_FUNCTION_NAME  neuvoltage

/*
 * Need to include simstruc.h for the definition of the SimStruct and
 * its associated macro definitions.
 */
#include "simstruc.h"

/* Function: mdlInitializeSizes ========================================================
 * Abstract:
 *    The sizes information is used by Simulink to determine the S-function
 *    block's characteristics (number of inputs, outputs, states, etc.).
 */
static void mdlInitializeSizes(SimStruct *S)
{
   ssSetNumSFcnParams(S, 0);  /* Number of expected parameters */
   if (ssGetNumSFcnParams(S) != ssGetSFcnParamsCount(S)) {
      /* Return if number of expected != number of actual parameters */
      return;
   }

   ssSetNumContStates(S, 0);
   ssSetNumDiscStates(S, 0);

   if (!ssSetNumInputPorts(S, 1)) return;
   ssSetInputPortWidth(S, 0, 7);
   ssSetInputPortDirectFeedThrough(S, 0, 1);

   if (!ssSetNumOutputPorts(S, 1)) return;
   ssSetOutputPortWidth(S, 0, 1);

   ssSetNumSampleTimes(S, 1);
   ssSetNumRWork(S, 0);
   ssSetNumIWork(S, 0);
   ssSetNumPWork(S, 0);
   ssSetNumModes(S, 0);
   ssSetNumNonsampledZCs(S, 0);

   ssSetOptions(S, 0);
}

/* Function: mdlInitializeSampleTimes ==================================================
  */
static void mdlInitializeSampleTimes(SimStruct *S)
{
   ssSetSampleTime(S, 0, INHERITED_SAMPLE_TIME);
   ssSetOffsetTime(S, 0, 0.0);
}

/* Function: mdlOutputs ================================================================
```

```
 */
static void mdlOutputs(SimStruct *S, int_T tid)
{

            InputRealPtrsType            uPtrs = ssGetInputPortRealSignalPtrs(S,0);
            real_T                              *y = ssGetOutputPortRealSignal(S,0);
  real_T            m;

  m=*uPtrs[6];

/*
 * Interval 1: Va>0, Vb<0 and Vc>=0
 */
  if  ((*uPtrs[0]>0)&&(*uPtrs[1]<0)&&(*uPtrs[2]>=0))
   { if ((*uPtrs[3]==0)&&(*uPtrs[4]==0)&&(*uPtrs[5]==0))
      {y[0]=-0.16667*m;}

     if ((*uPtrs[3]==0)&&(*uPtrs[4]==0)&&(*uPtrs[5]==1))
      {y[0]=0;}

     if ((*uPtrs[3]==0)&&(*uPtrs[4]==1)&&(*uPtrs[5]==0))
      {y[0]=-0.33333*m;}

     if ((*uPtrs[3]==0)&&(*uPtrs[4]==1)&&(*uPtrs[5]==1))
      {y[0]=-0.16667*m;}

     if ((*uPtrs[3]==1)&&(*uPtrs[4]==0)&&(*uPtrs[5]==0))
      {y[0]=0;}

     if ((*uPtrs[3]==1)&&(*uPtrs[4]==0)&&(*uPtrs[5]==1))
      {y[0]=0.16667*m;}

     if ((*uPtrs[3]==1)&&(*uPtrs[4]==1)&&(*uPtrs[5]==0))
      {y[0]=-0.16667*m;}

     if ((*uPtrs[3]==1)&&(*uPtrs[4]==1)&&(*uPtrs[5]==1))
      {y[0]=0;}
    }
/*
 * Interval 2: Va>0, Vb<=0 and Vc<0
 */
  else if  ((*uPtrs[0]>0)&&(*uPtrs[1]<=0)&&(*uPtrs[2]<0))
   { if ((*uPtrs[3]==0)&&(*uPtrs[4]==0)&&(*uPtrs[5]==0))
      {y[0]=0.16667*m;}

     if ((*uPtrs[3]==0)&&(*uPtrs[4]==0)&&(*uPtrs[5]==1))
      {y[0]=0;}

     if ((*uPtrs[3]==0)&&(*uPtrs[4]==1)&&(*uPtrs[5]==0))
      {y[0]=0;}

     if ((*uPtrs[3]==0)&&(*uPtrs[4]==1)&&(*uPtrs[5]==1))
      {y[0]=-0.16667*m;}

     if ((*uPtrs[3]==1)&&(*uPtrs[4]==0)&&(*uPtrs[5]==0))
      {y[0]=0.33333*m;}

     if ((*uPtrs[3]==1)&&(*uPtrs[4]==0)&&(*uPtrs[5]==1))
      {y[0]=0.16667*m;}
```

```
    if ((*uPtrs[3]==1)&&(*uPtrs[4]==1)&&(*uPtrs[5]==0))
      {y[0]=0.16667*m;}

    if ((*uPtrs[3]==1)&&(*uPtrs[4]==1)&&(*uPtrs[5]==1))
      {y[0]=0;}
    }
/*
 * Interval 3: Va>=0, Vb>0 and Vc<0
 */
  else if  ((*uPtrs[0]>=0)&&(*uPtrs[1]>0)&&(*uPtrs[2]<0))
    { if ((*uPtrs[3]==0)&&(*uPtrs[4]==0)&&(*uPtrs[5]==0))
      {y[0]=-0.16667*m;}

    if ((*uPtrs[3]==0)&&(*uPtrs[4]==0)&&(*uPtrs[5]==1))
      {y[0]=-0.33333*m;}

    if ((*uPtrs[3]==0)&&(*uPtrs[4]==1)&&(*uPtrs[5]==0))
      {y[0]=0;}

    if ((*uPtrs[3]==0)&&(*uPtrs[4]==1)&&(*uPtrs[5]==1))
      {y[0]=-0.16667*m;}

    if ((*uPtrs[3]==1)&&(*uPtrs[4]==0)&&(*uPtrs[5]==0))
      {y[0]=0;}

    if ((*uPtrs[3]==1)&&(*uPtrs[4]==0)&&(*uPtrs[5]==1))
      {y[0]=-0.16667*m;}

    if ((*uPtrs[3]==1)&&(*uPtrs[4]==1)&&(*uPtrs[5]==0))
      {y[0]=0.16667*m;}

    if ((*uPtrs[3]==1)&&(*uPtrs[4]==1)&&(*uPtrs[5]==1))
      {y[0]=0;}
    }
/*
 * Interval 4: Va<0, Vb>0 and Vc<=0
 */
  else if  ((*uPtrs[0]<0)&&(*uPtrs[1]>0)&&(*uPtrs[2]<=0))
    { if ((*uPtrs[3]==0)&&(*uPtrs[4]==0)&&(*uPtrs[5]==0))
      {y[0]=0.16667*m;}

    if ((*uPtrs[3]==0)&&(*uPtrs[4]==0)&&(*uPtrs[5]==1))
      {y[0]=0;}

    if ((*uPtrs[3]==0)&&(*uPtrs[4]==1)&&(*uPtrs[5]==0))
      {y[0]=0.33333*m;}

    if ((*uPtrs[3]==0)&&(*uPtrs[4]==1)&&(*uPtrs[5]==1))
      {y[0]=0.16667*m;}

    if ((*uPtrs[3]==1)&&(*uPtrs[4]==0)&&(*uPtrs[5]==0))
      {y[0]=0;}

    if ((*uPtrs[3]==1)&&(*uPtrs[4]==0)&&(*uPtrs[5]==1))
      {y[0]=-0.16667*m;}

    if ((*uPtrs[3]==1)&&(*uPtrs[4]==1)&&(*uPtrs[5]==0))
      {y[0]=0.16667*m;}

    if ((*uPtrs[3]==1)&&(*uPtrs[4]==1)&&(*uPtrs[5]==1))
```

```
      {y[0]=0;}
    }
/*
 * Interval 5: Va<0, Vb>=0 and Vc>0
 */
  else if  ((*uPtrs[0]<0)&&(*uPtrs[1]>=0)&&(*uPtrs[2]>0))
    { if ((*uPtrs[3]==0)&&(*uPtrs[4]==0)&&(*uPtrs[5]==0))
      {y[0]=-0.16667*m;}

     if ((*uPtrs[3]==0)&&(*uPtrs[4]==0)&&(*uPtrs[5]==1))
      {y[0]=0;}

     if ((*uPtrs[3]==0)&&(*uPtrs[4]==1)&&(*uPtrs[5]==0))
      {y[0]=0;}

     if ((*uPtrs[3]==0)&&(*uPtrs[4]==1)&&(*uPtrs[5]==1))
      {y[0]=0.16667*m;}

     if ((*uPtrs[3]==1)&&(*uPtrs[4]==0)&&(*uPtrs[5]==0))
      {y[0]=-0.33333*m;}

     if ((*uPtrs[3]==1)&&(*uPtrs[4]==0)&&(*uPtrs[5]==1))
      {y[0]=-0.16667*m;}

     if ((*uPtrs[3]==1)&&(*uPtrs[4]==1)&&(*uPtrs[5]==0))
      {y[0]=-0.16667*m;}

     if ((*uPtrs[3]==1)&&(*uPtrs[4]==1)&&(*uPtrs[5]==1))
      {y[0]=0;}
    }
/*
 * Interval 6: Va<=0, Vb<0 and Vc>0
 */
  else if  ((*uPtrs[0]<=0)&&(*uPtrs[1]<0)&&(*uPtrs[2]>0))
    { if ((*uPtrs[3]==0)&&(*uPtrs[4]==0)&&(*uPtrs[5]==0))
      {y[0]=0.16667*m;}

     if ((*uPtrs[3]==0)&&(*uPtrs[4]==0)&&(*uPtrs[5]==1))
      {y[0]=0.33333*m;}

     if ((*uPtrs[3]==0)&&(*uPtrs[4]==1)&&(*uPtrs[5]==0))
      {y[0]=0;}

     if ((*uPtrs[3]==0)&&(*uPtrs[4]==1)&&(*uPtrs[5]==1))
      {y[0]=0.16667*m;}

     if ((*uPtrs[3]==1)&&(*uPtrs[4]==0)&&(*uPtrs[5]==0))
      {y[0]=0;}

     if ((*uPtrs[3]==1)&&(*uPtrs[4]==0)&&(*uPtrs[5]==1))
      {y[0]=0.16667*m;}

     if ((*uPtrs[3]==1)&&(*uPtrs[4]==1)&&(*uPtrs[5]==0))
      {y[0]=-0.16667*m;}

     if ((*uPtrs[3]==1)&&(*uPtrs[4]==1)&&(*uPtrs[5]==1))
      {y[0]=0;}
    }

   else
```

```
    y[0]=0;

}

/* Function: mdlTerminate =====================================================
 * Abstract:
 *    In this function, you should perform any actions that are necessary
 *    at the termination of a simulation.  For example, if memory was
 *    allocated in mdlInitializeConditions, this is the place to free it.
 */
static void mdlTerminate(SimStruct *S)
{
}

#ifdef  MATLAB_MEX_FILE    /* Is this file being compiled as a MEX-file? */
#include "simulink.c"      /* MEX-file interface mechanism */
#else
#include "cg_sfun.h"       /* Code generation registration function */
#endif
```