Power quality enhancement of isolated power systems through series compensation

Wang, Tongxun

2007

Wang, T. (2007). Power quality enhancement of isolated power systems through series compensation Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/3473>

<https://doi.org/10.32657/10356/3473>

Nanyang Technological University

Downloaded on 26 Apr 2023 17:10:00 SGT

Power Quality Enhancement of Isolated Power Systems through Series Compensation

Tongxun Wang

School of Electrical and Electronics Engineering

A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Doctor of Philosophy

2007

Acknowledgements

I am greatly indebted to my supervisor, Prof. Choi San Shing, for his knowledge, guidance, dedication and exemplary academic standards. He always provides thoughtful guidance which contributes significantly towards the derivation of this thesis. I am deeply impressed by his rigorous attitude to do research, an attitude that will have lasting effect on my future research and work.

I am deeply grateful to Dr. Sng Eng Kian Kenneth for his invaluable suggestions, comments and support in my studies. I am also very grateful to Dr. Don Mahinda Vilathgamuwa for the valuable discussions, suggestions, and support I have received from him throughout my research.

Financial assistant provided by Nanyang Technological University is sincerely appreciated as it supports the completion of my study. In particular, I am deeply thankful to Mr. Foo Mong Keow for the support he has given to me in the course of experiments. I am also thankful to the technicians Ms. Chew Sim Annie, Mr. Yeoh Tiow Koon and Mr. Lee Ting Yeng for their technical support in the use of computers, software, and other equipment.

Special thanks go to my wife, Jiao Rui, for her always being supportive, patient and loving. The constant support from my parents is deeply felt and appreciated.

Summary

Power quality problems have increasingly become a concern over the last decade or so because they impact greatly on the operations of electrical equipment. Often the consequence would be significant economic losses to customers. While enhancing power quality in interconnected systems has attracted much research interest, unfortunately much less attention has been directed toward solving the same problems in isolated power systems. This is despite the fact that one can still encounter situations where loads are supplied by a relatively small capacity power system which is not part of a grid. Examples of such isolated power systems include small networks in oil exploration areas and remote mining districts. The main focus of this project is to examine issues closely related to power quality enhancement in such an isolated power system.

These isolated power systems are typically characterized by generation capacity of up to a few MVA. The electrical source can be in the form of diesel generator-sets and the p.u. equivalent source impedances tend to be high because of the sparsity of the networks. The loads are often relatively large DC or AC motor-drives: the variable-speed drives or machinery would be supplied by the generators via power converters. The loads are non-linear and would involve the commutation process of the converters. The consequence would be distortions in the voltage/current waveforms in the supply systems, the extents of which are likely to fluctuate as the loads change. Hence under such a situation, any attempt to enhance power quality will need to take into consideration the presence of harmonic distortions in the network.

In an attempt to address the growing concern on power quality much research attention have been directed toward the design of so-called Custom Power devices. Among such devices are those which are based on series compensation technique, applied to interconnected or grid systems. A series compensator (SC) is intended for use in a distribution system, with rating of between a few hundred kVA to 2 MVA typically. Central to its design is a voltage-source inverter connected to a DC energy storage system.

The SC is designed to be installed upstream of loads which are to be protected against short-duration voltage disturbances. The basic operating principle of a SC is by injecting a voltage component in series with the load voltage so that the load-side voltage is maintained at its nominal level during a voltage disturbance. Due to its quick response and high reliability, the SC is considered to be an effective device in mitigating the impacts of voltage sags/swells and can provide good power quality for customers.

Currently, most studies on series compensation are focused on applying the technique in mitigating the effects of voltage sags. However harmonic voltages/currents in the network have been ignored. This thesis therefore begins with a detailed analysis concerning the mitigation of the effects of voltage sags under distorted conditions through series compensation. A method to control the injection voltage of the SC that can mitigate the effects of the harmonics on voltage compensation is proposed. The method is based on the control of the SC branch impedance. In the process of harmonic voltage compensation, it is shown that power exchange exists between the SC and the external network. It would then result in a variation in the terminal voltage of the energy storage system (ESS) within the SC. Permitting the phase adjustment of the fundamental frequency component of the reference voltage of the SC, a method to control the voltage of ESS is proposed. Simulation results indicate that using the suggested method, harmonic distortion in an isolated power system can be mitigated.

To further demonstrate the effectiveness of the proposed method, a prototype of series compensator is constructed in the laboratory. The proposed method is applied to the laboratory set-up. Experimental results show the power quality of the system can be improved through series compensation.

In the process of harmonic voltage compensation, it is shown that power exchange exists between the SC and the external network. Based on the analysis of the harmonic real power flow in the power system, it is seen that the SC would import harmonic real power from the external system. A new SC control strategy is then proposed which involves the phase adjustment of the fundamental frequency component of the sensitive load terminal voltage. Through the analysis on the power exchange, it is shown that the load ride-

through capability during voltage sag can be improved with the support of the harmonic real power absorbed by the SC. The capacity of the SC required is modest. Therefore it makes the SC a viable device for such an application. Simulations have confirmed the effectiveness of the proposed method, as it is applied on the SC to achieve improved quality of supply in the power system.

Much of the research attention on SC is to ensure that it can react as quickly and as effectively as possible for an upstream fault. Unfortunately faults do occur on the distribution system downstream of the SC. Should such a fault occur anywhere on the feeder connecting the SC and the protected load, and as the SC is series connected to the faulted feeder, a large current will flow in the VSI. Without proper measure, this could damage the compensator. A series compensator with fault current limiting function is proposed and its principle of operation is elaborated. When a downstream fault occurs, the SC achieves the current limiting function by injecting a voltage component to restore the PCC voltage to its pre-fault phasor value. It is shown that under this condition, the SC absorbs energy from the external system. The consequence is a voltage rise in the energy storage capacitor of the SC. Based on an analysis of the voltage rise effect, a method to determine the rating of the capacitor is proposed. Simulation results show the effectiveness of the proposed series compensator system for fault current limiting.

Table of Contents

Acknowledgements.....	i
Summary	ii
List of Figures	ix
List of Tables	xiii
List of Symbols	xiv
Chapter 1 Introduction.....	1
1.1 Motivation.....	1
1.2 Major Contributions.....	4
1.3 Thesis Organization	6
Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems.....	8
2.1 General Attributes of Isolated Power Systems	8
2.2 Power Quality Issues.....	10
2.2.1 Power Quality Terms and Definitions	11
2.2.2 ITIC Curve	12
2.3 Causes of Voltage Sags/Swells and Harmonics.....	14
2.3.1 Causes of Voltage Sags/Swells.....	14
2.3.2 Causes of Harmonic Distortions	18
2.4 Impacts of Disturbances on Equipment	21
2.4.1 Impacts of Voltage Sags/Swells on Loads.....	21
2.4.2 Impacts of Harmonic Distortions on Loads	26
2.5 Mitigation Methods: a Brief Review	27

2.5.1	Conventional Mitigation Equipment.....	28
2.5.2	Custom Power Devices	31
2.6	Conclusions.....	41
Chapter 3	A Series Compensation Method to Mitigate Harmonics	43
3.1	Introduction.....	43
3.2	System Model	45
3.3	Harmonic Compensation	46
3.3.1	Principle of Harmonic Compensation.....	46
3.3.2	A Possible SC Control Scheme.....	48
3.3.3	Effects of Commutation and Design Constraints.....	51
3.4	Proposed Design	54
3.5	Control of Sensitive Load Terminal Voltage.....	57
3.5.1	Description of the Control Strategy	58
3.5.2	Simplified ESS Control Dynamics	62
3.6	Verification through Simulation	65
3.6.1	Effectiveness of Harmonic Mitigation.....	66
3.6.2	Effectiveness of the Voltage Control of ESS.....	68
3.7	Conclusions.....	69
Chapter 4	Experimental Prototype of a Series Compensator to Mitigate Harmonics	71
4.1	Introduction.....	71
4.2	On Overview of the Completed Prototype System.....	71
4.3	Description of the SC Hardware Prototype	73
4.3.1	Voltage Source Inverter	74
4.3.2	PWM Module and Gate-drive Module	76
4.3.3	Current Transducers.....	77
4.3.4	Voltage Transducers	77
4.3.5	Feedback Control Module.....	77

4.4	Implementation of the Control Scheme	78
4.5	Experimental Results	79
4.5.1	Effectiveness of SC for Harmonic Compensation	79
4.5.2	Effectiveness of Voltage Control of ESS.....	80
4.6	Conclusions.....	83
Chapter 5	An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions	84
5.1	Introduction.....	84
5.2	Harmonic Mitigation and Power Flows.....	85
5.2.1	Control of Harmonic Distortions	86
5.2.2	Power Flow Control through SC.....	88
5.2.3	Harmonic Power Flows.....	91
5.3	Voltage Restoration	95
5.3.1	Voltage Swell.....	97
5.3.2	Voltage Sag.....	100
5.4	Illustrative Examples	104
5.5	Conclusions.....	108
Chapter 6	Control of Series Compensator under Downstream Fault Condition	109
6.1	Introduction.....	109
6.2	Principle of Series Compensation.....	111
6.2.1	Voltage Restoration	111
6.2.2	Fault Current Limiting	113
6.3	Voltage Rise within the Energy Storage Device.....	119
6.4	Control Scheme.....	122
6.5	A Dual Function Series Compensator.....	127
6.6	Illustrative Examples	129

6.7	Conclusions.....	135
Chapter 7	Conclusions and Recommendations	136
7.1	Conclusions.....	136
7.2	Recommendations.....	139
	References.....	141
	Appendices.....	153
	VITA	159

List of Figures

Fig. 2-1 ITIC (CBEMA) curve.	13
Fig. 2-2 System model for the study of a voltage sag/swell.	15
Fig. 2-3 Equivalent circuit for voltage sag due to large load.	17
Fig. 2-4 Six-pulses bridge fed from an infinite bus.	19
Fig. 2-5 Six-pulses bridge fed from a non-infinite bus.	20
Fig. 2-6 A typical computer power supply.	21
Fig. 2-7 Typical AC drive configuration.	23
Fig. 2-8 DC motor drive with separately excited armature and field winding	25
Fig. 2-9 Principle of motor-generator set.	28
Fig. 2-10 (a) Single-tuned shunt filter circuit; (b) single-tuned shunt filter impedance versus frequency.	29
Fig. 2-11 (a) Damped filter circuit; (b) damped filter impedance versus frequency.	30
Fig. 2-12 Configuration of a Static Transfer Switch (STS).	32
Fig. 2-13 Schematic diagram of the prototype Solid State Breaker.	33
Fig. 2-14 Schematic diagram of a solid-state current limiter.	34
Fig. 2-15 Typical configuration of DSTATCOM.	36
Fig. 2-16 Schematic diagram of a typical SC.	37
Fig. 2-17 Transient state during injection.	38
Fig. 2-18 The principle of an active filter.	40
Fig. 3-1. A typical isolated power system installed with a SC.	45
Fig. 3-2 Schematic diagram showing the interconnection of the SC with the sensitive load.	48
Fig. 3-3 A possible closed-loop control scheme for the SC.	49
Fig. 3-4 (a) Waveforms of V^* and V_{out} of SC; (b) Difference between V^* and V_{out}	52
Fig. 3-5 A typical frequency response characteristic (a) the RC load and (b) the combined filter L and RC load.	52
Fig. 3-6 Determine the magnitude of the square wave.	53
Fig. 3-7 Block diagram of the SC-sensitive load with load current feedback.	55

Fig. 3-8 Frequency response characteristic of (a) $R'(s)$ and (b) $R'(s) \cdot G_{cl}(s)$.	56
Fig. 3-9. A typical frequency response characteristics of $Z'(s)$	57
Fig. 3-10 The isolated power system with the SC.	58
Fig. 3-11. Phasor diagram showing voltage injection for a leading power factor load: fundamental frequency component.	61
Fig. 3-12 (a) Dynamic model describing the relationship between $\hat{V}_{DC}$ and $d\alpha/dt$; (b) Block diagram of the proposed closed-loop control scheme.	64
Fig. 3-13 Terminal voltage (V_L) and current (I_L) drawn by the sensitive load: without SC.....	67
Fig. 3-14 Terminal voltage (V_L) and current (I_L) drawn by the sensitive load: with SC.	67
Fig. 3-15 Terminal voltage of ESS without phase shift in the reference voltage.	68
Fig. 3-16 Terminal voltage (V_{DC}) of ESS with phase shift in the fundamental component of the reference voltage: (a) at nominal load level; (b) with a 20% decrease in load level.....	69
Fig. 4-1 Laboratory prototype of the isolated power system showing the main load and components of the series compensator.....	72
Fig. 4-2 Layout of the Series Compensator.	73
Fig. 4-3 Single-phase full bridge inverter.	74
Fig. 4-4 Pulse width modulation.....	75
Fig. 4-5 Block diagram of DS1103 controller board.	78
Fig. 4-6 Terminal voltage and current drawn by the sensitive load: without SC.	79
Fig. 4-7 Terminal voltage and current drawn by the sensitive load: with SC.	80
Fig. 4-8 Terminal voltage of ESS (a) without and (b) with phase shift in the reference voltage.....	81
Fig. 4-9 Converter load change by -20%: (a) Terminal voltage of ESS with phase shift in the reference voltage; (b) Corresponding terminal voltage and current of the sensitive load.....	82
Fig. 4-10 Sensitive load terminal voltage (a) without SC and (b) with SC when the main load changes.....	82
Fig. 5-1 A typical isolated power system installed with a SC.	85

Fig. 5-2 Equivalent circuits of the sensitive load-SC branch for: (a) fundamental component and (b) h^{th} harmonic component.	87
Fig. 5-3 Sensitive load-SC branch: (a) Equivalent circuit describing harmonic compensation in practice; (b) Phasor diagram for h^{th} harmonic order.....	90
Fig. 5-4 Harmonic power flow in the isolated system: h^{th} harmonic component.	91
Fig. 5-5 Phasor diagram showing voltage restoration during (a) a voltage swell and (b) a voltage sag: fundamental frequency component.....	98
Fig. 5-6 Phasor diagram of voltage sag condition when $V_{s1}/V_{L1} = \gamma < \cos \theta$: (a) without harmonic power taken into consideration, (b) with harmonic power taken into consideration.	101
Fig. 5-7 Terminal voltage (V_L) of the sensitive load before and after a +25% main load change - without the SC.	104
Fig. 5-8 Terminal voltage (V_L) of the sensitive load before and after a 25% main load increase: with SC.	105
Fig. 5-9 Harmonic power flows in the isolated power system prior to and after the 25% main load increase.....	105
Fig. 5-10 Terminal voltage of ESS (V_{DC}) following load change: 70% voltage sag.	106
Fig. 5-11 Firing angle of rectifier during main load changes due to the 70% voltage sag.	106
Fig. 5-12 Terminal voltage (V_L) of the sensitive load: with SC for a 40% load increase.	107
Fig. 5-13 Terminal voltage of ESS for the 40% load increase.	107
Fig. 6-1 A typical distribution network incorporating a SC.	109
Fig. 6-2 Network model under an upstream fault condition.	112
Fig. 6-3 Network pre-fault condition and phasor diagram.	113
Fig. 6-4 Network condition under a downstream fault.	115
Fig. 6-5 Downstream fault condition with the FCL in service : $\vec{V}_{pf} = \vec{V}_p$, $\vec{I}_f = \vec{I}_L$ at full restoration.....	116
Fig. 6-6 Dynamic process of voltage injection.	118
Fig. 6-7 χ versus T	121
Fig. 6-8 A typical SC-connected distribution system.	122
Fig. 6-9 Open-loop controller for the FCL.	123

Fig. 6-10 Proposed control system for the FCL.....	126
Fig. 6-11 Structure of a Dual Function SC.	128
Fig. 6-12 PCC voltage and line current under a downstream L-G fault- no FCL.	130
Fig. 6-13 PCC voltage and line current: FCL on open-loop control but without DC voltage compensation.....	130
Fig. 6-14 Voltage across the terminals of the energy storage capacitor.	131
Fig. 6-15 PCC voltage and line current: FCL with open-loop control and DC voltage compensation.	132
Fig. 6-16 PCC voltage and line current: FCL with outer voltage and inner current control.	132
Fig. 6-17 PCC voltage and line current: remote single-phase-ground fault.	133
Fig. 6-18 PCC voltage and line current under a downstream 3-phase fault: FCL in service.	134
Fig. 6-19 PCC voltage and Load-side voltage: SC with closed-loop control.....	134

List of Tables

Table 2-1 Categories and characteristics of short-duration variation and waveform distortion in power systems.....	11
Table 2-2 Voltage distortion limits.....	14
Table 2-3 The Custom Power family.....	31
Table 3-1 Variations of P_1 with α	62
Table 3-2 System parameters for simulation and experiment.	66
Table 6-1 System Parameters.....	129

List of Symbols

ω_o	Fundamental frequency
Z_S	Thevenin equivalent impedance of the system source
Z_L	Equivalent impedance of the sensitive load
$Z_{L,fullload}$	Impedance of the load under the full load condition
$Z_{SC,Inv}$	Equivalent series impedance of the SC
$\vec{E}$	Voltage phasor of upstream source
V_S	Upstream source voltage
V_L	Terminal voltage of the sensitive load
V_{S1}	Fundamental components of the upstream supply voltage
V_{Sh}	Harmonic components of the upstream supply voltage
V^*	Desirable injection voltage of the SC
V_{Sa}, V_{Sb}, V_{Sc}	Phase voltages of upstream supply voltage
$V_{Sa1}, V_{Sb1}, V_{Sc1}$	Fundamental components of the upstream phase voltages
V_{S1}	RMS value of fundamental component of source voltage
V_{L1}	RMS value of fundamental component of sensitive load voltage
V_{DC}	Voltage at the terminal of the energy storage system of the SC
V_{out}	Injected voltage of the SC
V_P	Equivalent fundamental component of V_{out} that meets $V_P I_{L1} = P_{Ch}$
$\vec{V}_P$	Phasor vector of the PCC voltage
$\vec{V}_{SC}$	Injection voltage of the series compensator
$\vec{V}_L$	Phasor vector of the load side voltage
$\hat{V}_{0n}$	Magnitude of the zero phase sequence voltage component
$\hat{V}_{1n}$	Magnitude of the positive phase sequence voltage component

$\hat{V}_{2n}$	Magnitude of the negative phase sequence voltage component
$\vec{V}_{S1}$	Phase vector of fundamental component of source voltage
$\vec{V}_{L1}$	Phase vector of fundamental component of sensitive load voltage
$\vec{V}_1$	Phase vector of fundamental component of the SC injected voltage
$\vec{V}_f$	Pre-fault voltage at f
$\vec{V}_{pf}$	PCC voltage during a downstream fault
I_L	Current flowing through sensitive load
$\vec{I}_{L1}$	Phase vector of fundamental component of sensitive load current
I_{L1}	RMS value of fundamental component of sensitive load current
I_{Lf}	SC output filter inductor current
I_C	SC output filter capacitor current
$\vec{I}_f$	Fault current during fault
ϕ_{1n}	Phase of the positive phase sequence voltage component
ϕ_{2n}	Phase of the negative phase sequence voltage component
C_f	Capacitance of the SC output filter
G_{cl}	Closed loop transfer function of the system
P_1	Fundamental power flow
P_h	Harmonic power flow
$\cos \theta$	Sensitive-load power factor at the fundamental frequency
α	Phase shift angle
E	ESS energy
C	Capacitor of the ESS
P_s	Power flow of source side
P_{S1}	Fundamental power flow of source side
P_{Sh}	Harmonic power flow of source side
P_D	Power flow of main drive loads
P_{D1}	Fundamental power flow of main drive loads

P_{Dh}	Harmonic power flow of main drive loads
P_L	Power flow of sensitive load
P_{L1}	Fundamental power flow of sensitive load
P_{Lh}	Harmonic power flow of sensitive load
P_C	Power flow of the SC
P_{C1}	Fundamental power flow of the SC
P_{Ch}	Harmonic power flow of the SC
δ_1	Delay angle of converter
δ_2	Overlap angle of converter
α_0	Phase angle between $\vec{V}_{S1}$ and $\vec{V}_{L1}$ at the condition $P_C = 0$
γ	Ratio of V_{S1}/V_{L1}
β	Ratio of V_P/V_{L1}
X_S	Reactance of the upstream system
X_L	Effective series reactance between the SC and the sensitive load
X	Effective reactance between the PCC and the location f

Chapter 1 Introduction

1.1 Motivation

Interest into power quality issues has intensified significantly in recent years. This is partly as a result of the wide-spread proliferation of modern electronic equipment in present-day power systems. The equipment can be susceptible to power system disturbances. Such loads include computers, automated machinery and micro-controllers and their peripheral devices. Since poor power quality could cause the shutdown or malfunction of the equipment and lead to economic loss to customers, a secure and reliable power supply is therefore a prerequisite to ensure customers' satisfaction [1-15].

While quality of supply can have a direct financial impact on the customers, electric utility is also concerned about quality issues as well. Meeting customer expectations and maintaining customer confidence are strong motivators. This is more so under the deregulated competitive market environment. The loss of a disgruntled customer to a rival electricity supplier will impact economically on a utility. For these reasons, both customers and electricity utilities become increasingly more acutely aware of the need for quality power supply [1, 3, 6, 9, 12].

A survey of the open literature will clearly show that although enhancing power quality in interconnected systems has attracted much research interest, unfortunately considerably less attention has been directed toward solving the same problem in isolated power systems. This is despite the fact that one can still encounter situations where loads are supplied by relatively small-capacity power systems which are not parts of a large-scale grid network.

Isolated power systems are typically characterized by generation capacity of up to a few MVA. The electrical source can be in the form of diesel generator-sets and source impedances tend to be high because of sparsity of the network. However, often due to the relatively low inertia and short-circuit levels, disturbances such as voltage variations and harmonics in the isolated power systems become challenging issues to be addressed. Furthermore, as more advanced generation and load-controlled techniques are being utilized in the systems, the power quality issues become more complex and require additional considerations.

In this connection, attempts to find ways of mitigating the effects of the power quality problems in distribution networks have captured much research interest. A recent development in this field is the use of Customer Power devices [1]. The approach is based on utilizing advanced power electronics technology to ensure a high quality of supply. Among the many technical solutions for improving supply to sensitive loads, series compensation technique has been shown to be particularly promising and effective [16-34]. As will be shown in the following Chapters, the fundamental principle of a Series Compensator (SC) operation in mitigating the effects of a voltage disturbance which occurs upstream of the system is that the SC will inject a voltage component to restore the load-side voltage to its nominal level. SC is considered to be effective for such disturbance mitigation due to its quick response and high reliability. Indeed, the focus of this thesis is on the power quality enhancement in an isolated power system through the application of the series compensation technique.

A possible alternative to the SC solution would be to use an Un-interruptible Power Supply (UPS) to cater for each of the sensitive loads. In practical application, a cost evaluation can be carried out to see whether a power quality enhancement system based on UPS or SC is more attractive economically. In the likely event that there are several sensitive loads to be protected, there would be a need to install several UPS. A typical UPS includes a rectifier, an inverter and a battery. Such an on-line UPS system is based on the use of power switching devices which are rated to operate to provide power to the protected load for an extended duration without interruption. The UPS battery also adds to the cost of the device and must be replaced periodically. Therefore, the total capital

plus operating cost of such a practice could be high, as compared to that of a SC. In fact, it is precisely because of economic consideration that the VSI-based series compensator was proposed some years ago to replace the practice of using of individual UPS, such device such as the DVR came into existence [33]. A SC is expected to be a lower cost alternative to UPS for applications at distribution substation level, especially if the transformer-less SC is used. Unlike UPS systems, the inverter switching devices used in the SC are not in operation most of the time. Thus for the SC, the switching devices of smaller power rating can thus be selected, since switching devices of a given rating can be operated from a cold state for a longer duration than from a warm state.

Another interesting feature to consider is that loads in the isolated power systems are often relatively large DC or AC variable-speed motor-drives. Due to the commutation process of the converters in the drive systems, the voltage/current waveforms in the supply system would be distorted. The extents of the distortions are likely to fluctuate as the loads change. Hence, under such a condition, any attempt to improve power quality will need to take into consideration the presence of harmonic distortions in the system. Furthermore, often the switching on/off of the large drive loads will cause voltage sags or swells. To protect sensitive loads from the voltage sags/swells, a series compensator can also be used to mitigate the harmful effects of the voltage sags/swell under distorted conditions. Details of such a scheme will be described in Chapter 3. Central to the proposed technique is the control of the SC branch impedance through a combined load-current feedback and inductive filter scheme. In the process of harmonics compensation, it is shown that power exchange exists between the SC and the external network. Through a phase adjustment technique, it is shown that the voltage across the terminals of the energy storage system within the SC can be controlled. At the same time, the method proposed in Chapter 3 is then applied to an experimental prototype to demonstrate its efficacy. Details of the laboratory set-up and experimental results will be given in Chapter 4.

In the isolated power systems, variations in the drive loads would result in momentary voltage excursions appearing in the network. These are often called voltage sags/swells. As a consequence, combined with the presence of the harmonics, the sensitive loads

would encounter not only harmonic distortions but also the voltage sags/swells. Thus a new challenge in power quality enhancement is to regulate the sensitive load terminal voltage and any harmonic distortion is to be controlled to within acceptable level. By extending the method proposed in Chapter 3, a series compensation strategy to mitigate harmonics and voltage sag/swell simultaneously will be described in Chapter 5.

Finally, most of the research attention described in the literature is directed towards controlling the SC to protect the sensitive loads from upstream disturbances. Little attention has been paid to the occurrence of downstream disturbances. Unfortunately, faults do occur downstream of the SC device. Should such a fault occur anywhere on the feeder connecting the device and the protected sensitive load, and as the device is series connected to the faulted feeder, a large current will appear in the SC. Without proper measure, this could damage the SC. In order to overcome this problem, Chapter 6 will propose a new design feature on the SC which will include fault current limiting function.

1.2 Major Contributions

In the course of this research work, original contributions achieved thus far can be summarized as follows:

- i. Series compensation method to mitigate harmonics.* In examining the power quality of an isolated power system, it is seen that if the power system supplies loads which consist of drives or industrial processes, often high levels of harmonic distortions can be observed. Under such a distorted condition, voltage compensation of the SC would cause voltage pulses to appear due to time-lag of the controller. It will result in large harmonic currents in the sensitive loads because the load is capacitive in nature and the load impedance is low at high frequency. A method to control the SC so that it can mitigate the effects of the harmonics is proposed. The method is based on the control of the SC branch effective impedance through the manipulation of SC injection voltage. To alleviate the high frequency voltage components and maintain the fundamental frequency component of the voltage at the sensitive load terminals constant, an

inductive filter and a load-current feedback scheme are incorporated into the network. Simulation results confirm the effectiveness of the proposed method, as it is applied on the SC to achieve improved quality of supply in the power system.

- ii. Construction of an experimental prototype of the SC.* As the key to the effective power quality enhancement is through the control of the SC, a laboratory prototype of the compensator has been constructed and used to demonstrate the efficacy of the proposed method. Details of the system design and experimental results are given.
- iii. A new voltage compensation strategy.* In the process of harmonic voltage compensation, it is shown that power exchange exists between the SC and the external network. Based on the analysis of the harmonic real power flows in the power system, it is seen that the SC would absorb harmonic real power from the external system. A new SC control strategy which involves the phase adjustment of the fundamental frequency component of the load terminal voltage is proposed. This is for the purpose to mitigate the effects of the voltage sag/swell. It is also shown that the absorbed harmonic power can enhance the capability of load ride-through in the power system, as compared to existing techniques.
- iv. Control of series compensator under downstream fault condition.* Most of the studies on SC consider voltage perturbations that originate upstream of the compensator. However, when a fault occurs downstream of the compensator, large short circuit current would flow through the SC. Without proper measures, this could damage the device. A method by which the SC is able to limit the fault current has been proposed. With the incipient of the downstream fault, the SC is controlled to inject a voltage component to restore the voltage at its upstream terminals to its pre-fault phasor value so that the fault current will be limited. Under such a condition, voltage of the energy storage system (ESS) of the SC will increase due to the energy absorbed from the external power system. Based on an analysis of the voltage rise effect, a method to determine the rating of the ESS has

been developed. Simulation results indicate the effectiveness of the proposed SC for fault current limiting as well as for voltage restoration.

1.3 Thesis Organization

The focus of the thesis is on enhancing power quality of isolated power systems. Chapter 1 provides a brief summary of the motivation and lists the major contributions made in this project. Chapter 2 describes electrical attributes pertaining to the isolated power systems, the associated power quality problems and their impacts on typical loads in the systems. A literature review pertaining to the research area of series compensator is also included.

Original contributions of this research are described in details in Chapter 3- Chapter 6. In Chapter 3, a series compensation method to mitigate harmonics is presented. The effect of harmonics compensation on the energy storage system (ESS) is analyzed and a method to control the terminal voltage of ESS is proposed.

To verify the effectiveness of the method proposed in Chapter 3, a laboratory set-up of an isolated power system with a prototype of the SC has been constructed. Details of the prototype are described in Chapter 4. Experimental results are also included.

The isolated power system considered in Chapter 3 is re-examined in Chapter 5. This is with regard to harmonic real power flow and its impacts on load ride-through. Based on the analysis, a new strategy is proposed.

Unlike Chapters 3 and 5 which consider disturbances originated upstream of the SC, the control of SC under downstream fault condition is studied in Chapter 6. A method to limit fault current through the SC is given. The voltage-rise effect in the ESS is analyzed. Based on the analysis, the rating of the ESS capacity can be determined.

Chapter 1 Introduction

Conclusions based on the research and recommendations for future works are given in Chapter 7.

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

As pointed out in Chapter 1, power quality problems in isolated power system have attracted increasing attention in recent years. In this Chapter, a general review of isolated power systems and the related power quality issues will be given. Since voltage sag/swell and harmonic distortion are the most common and/or severe power quality disturbances that can exist on the power systems, a detailed description on the nature of these disturbances and their impacts on different types of loads will be given. Some of the present techniques for power quality enhancement based on Custom Power technology will also be presented. As a method of mitigating the effects of the disturbances, Series Compensation (SC) technique is well-known and is one of the most promising and effective solution. A detailed description concerning the SC is also included.

2.1 General Attributes of Isolated Power Systems

Despite wide coverage of the land area of the earth by electricity networks, not all consumers are served by large interconnected systems. A small power system that is not connected to a much larger grid is often called an isolated power system and such a network can be found in rural and remote areas of the world. The system represents the alternative to grid connection, where interconnection to a large grid is not viable due to high costs and/or geographical obstacles. Examples of isolated power system are those found serving

- Ships
- Offshore platforms
- Oil exploration area

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

- Remote mining districts
- Small islands
- Isolated villages far from a well-developed transmission and distribution grid

Isolated power systems are gaining importance because of the push by governments and utilities on the electrification of rural and remote areas. From a utility perspective, the construction and maintenance of ever increasing interconnected grids can become both economically and environmentally less attractive. Operational and administrative costs associated with providing power to remote locations may not compensate the gains of bulk production. Thus, utilities may not opt for grid expansion and large-scale, centralized generating plants. Instead, it may be more attractive to adopt decentralized small-scale generation policy, with the generation sited near the loads. The opportunity to optimize resources and reduce costs can be significant. The above factors have created a new situation in which large scale centralized systems may become less prevalent, even in some of the most developed countries [35].

Typically, an isolated power system is usually made up of autonomous free-standing generating sets, cable lines, switchboards to which various kinds of loads are served. Such a system is often radial in structure, in which one or more generators are connected to the same busbar. The loads are connected to a switchboard, which is often termed the Point of Common Coupling (PCC) [36].

Furthermore, a present-day generating set in isolated power system is typically a synchronous generator coupled to internal diesel combustion engine. On the other hand, due to concerns with dwindling fuel reserves and the potential negative impact of conventional electricity generating systems on the environment, increasingly attention has been directed in recent years towards the use of renewable energy sources [37]. The capacity of the generators is relatively small, say, of a few MVA. The ratio of the nominal power of singular energy receiver to one generating set can be high. In some cases, the nominal power of single load may even exceed the nominal power of each generator [38]. Thus the characteristic attributes of an isolated power system are that of relatively low

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

inertia, large short circuit impedance and low fault level. Therefore an isolated power system is often regarded as being “electrically weak”.

Another point which has important bearing on network performance is if in an isolated power system, the loads are predominantly rotating machinery or motors. The increasing emphasis on overall system efficiency has resulted in a continued growth in the applications of devices such as high-efficiency, adjustable-speed motor drives and shunt capacitors for power factor correction. The emphasis is to reduce losses. The use of speed-controllers and the potential for resonance can result in higher harmonic levels being observed within the networks. It has lead to concern on the impact of the harmonics on system capacities [39, 40]. In the event when more advanced generation and load-control techniques are implemented in order to increase efficiency and reduce costs [41], it would demand the use of microprocessor-based controls and power electronic devices. These equipment are themselves particularly sensitive to disturbances such as the harmonics.

In general, it can be concluded that isolated power systems, which have relatively low inertia and short-circuit levels, and/or experience relatively large load variations, tend to result in higher levels of power quality degradation. Harmonics, voltage variations, voltage unbalance and frequency variations are some of the most important issues on power quality in such system and could be of much concern.

The above points on power quality due to load changes also apply when the generation is from a renewable source.

2.2 Power Quality Issues

There is much confusion on the meaning of the term ‘power quality’ because different authors use different definitions. A consistent set of definitions is given as follows [11]:

- **Voltage quality** is concerned with deviations of the voltage from the ideal. The ideal voltage is a single-frequency sine wave of constant amplitude and frequency.

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

- **Current quality** is the complementary term to voltage quality: it is concerned with the deviation of the current from the ideal. The ideal current is again a single-frequency sine wave of constant amplitude and frequency, with the additional requirement that the current sine wave is in phase with the voltage sine wave in order to achieve efficient energy usage or reduce losses.
- **Power quality** is the combination of voltage quality and current quality.

2.2.1 Power Quality Terms and Definitions

Table 2-1 Categories and characteristics of short-duration variation and waveform distortion in power systems.

Categories	Typical Spectral content	Typical duration	Typical magnitude
Short duration variation			
1 <i>Instantaneous</i>			
1.1 Sag		0.5 – 30 cycles	0.1 – 0.9 pu
1.2 Swell		0.5 – 30 cycles	1.1 – 1.8 pu
2 <i>Momentary</i>			
2.1 Interruption		0.5 cycle – 3 s	< 0.1 pu
2.2 Sag		30 cycles – 3 s	0.1 – 0.9 pu
2.3 Swell		30 cycles – 3 s	1.1 – 1.4 pu
3 <i>Temporary</i>			
3.1 Interruption		3s – 1 min	< 0.1 pu
3.2 Sag		3s – 1 min	0.1 – 0.9 pu
3.3 Swell		3s – 1 min	1.1 – 1.2 pu
Waveform distortion			
1 DC offset		Steady state	0 – 0.1%
2 Harmonics	0 – 100 th	Steady state	0 – 20%
3 Inter harmonics	0 – 6 kHz	Steady state	0 – 2%
4 Notching		Steady state	
	Broad-band	Steady state	0 – 0.1%
5 Noise			

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

Power quality standards vary between societies and countries. It is therefore important to provide a clear understanding of the terms and definitions that are used in the literature before one can proceed to consider detailed analysis work. A IEEE Working Committee has declared unique definitions for the various power system disturbances in IEEE 1159 [42]. Since voltage sag and harmonic distortion are the most common power quality problems in an isolated power system, Table 2-1 shows only the two categories and characteristics of the electromagnetic phenomena. Each type of variation can be designated as instantaneous, momentary or temporary depending on its duration as defined in the table. For example, it is shown that typical duration of momentary sag is defined to be 30 cycles to 3s. And harmonics are sinusoidal voltages or currents having frequencies that are integer multiples of the power frequency, up to perhaps 100 times of the fundamental.

2.2.2 ITIC Curve

One of the most frequently quoted form of data to describe power quality is the so-called ITIC curve [43] shown in Fig. 2-1. This curve was originally developed by the Information Technology Industry Council (ITIC) as a guideline to help ITIC members in the design of the power supply for their computers and electronic equipment. With many modern equipment, the ITIC curve has become a standard design criterion for them and it is also a common format for reporting power quality variation data. It can be used to evaluate the voltage quality of a power system with respect to voltage interruptions, sags or swells.

The curve relates the magnitude and duration of voltage variations which can be tolerated for such equipment connected to a power system. As will be discussed in Section 2.3, load change in an isolated power system would result in voltage sag/swell. The voltage disturbance will persist until the controllers of generators or other voltage control devices take corrective actions to mitigate the effects. Possible operating range over which such control actions can be effective is shown over the shaded area in Fig. 2-1. In the event when a voltage disturbance has resulted in the voltage magnitude being outside the upper or lower envelop, then the equipment will not be able to function or will be damaged.

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

Fig. 2-1 ITIC (CBEMA) curve [43].

In conjunction with the ITIC curve which has set limits as to the duration and amplitude values of supply voltage, the IEEE has a recommended practice on limiting harmonic distortion. IEEE 519 specifies the limits for the voltage provided by the utility and shows the general level of harmonics in the supply network at the PCC, as a percent of the rated voltage. For the system whose voltage level is 69 kV and below, the individual voltage distortion should be less 3%, while the Total Harmonic Distortion (THD) on the voltage should be less than 5%.

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

Table 2-2 Voltage distortion limits.

Bus voltage	Individual Voltage Distortion (%)	Total Voltage Distortion THD (%)
69 kV and below	3.0	5.0
69.001 kV through 161 kV	1.5	2.5
161.001 kV and above	1.0	1.5

Even though IEEE 519 is proposed for interconnected power system, it can provide a design criterion for harmonics mitigating in an isolated power system. Indeed, the mitigation of harmonics associated with an isolated power system will be investigated in the Chapter 3.

2.3 Causes of Voltage Sags/Swells and Harmonics

Since voltage sags/swells and harmonic distortion are considered the most common power quality occurrences in an isolated power system and could significantly impact the electric utility customers [44], an understanding of the causes will help one to search for effective solutions to these problems. Thus, an explanation of the causes of the disturbances will be given in this section.

2.3.1 Causes of Voltage Sags/Swells

An underlying cause of sags or swells is a sudden change of current flow through source impedance. Application of Ohm's Law and Kirchoff's Equations, as they related to real-life, non-ideal sources, is necessary to understanding the effect of such an event. For this purpose, a simple system model shown in Fig. 2-2 can be used. Consistent with the "List of Symbols" shown in Appendix A, in Fig. 2-2, $\vec{E}$ and $\vec{Z}_s$ represents the source voltage and source impedance respectively, and in which $\vec{I}_s$ represents the current supplying the load through $\vec{Z}_s$. Thus the voltage at the PCC bus can be obtained

$$\vec{V}_p = \vec{E} - \vec{Z}_s \vec{I}_s \quad (2.1)$$

Fig. 2-2 System model for the study of a voltage sag/swell.

A sudden increase in $\vec{I}_s$ will cause a larger voltage to be developed across $\vec{Z}_s$. This will result in a reduction in $|\vec{V}_p|$. Likewise, a sudden reduction in the current flow will cause an increase in $|\vec{V}_p|$.

Voltage sags/swells due to fault

A sudden increase in $|\vec{I}_s|$ can be due to a downstream fault. For instance, one of the important causes of the voltage sag is the occurrence of a fault within an industrial facility or on parallel feeders in the electrical neighborhood. Accordingly, the system model show in Fig. 2-2 could be used to explain the origin of a voltage sag due to a short-circuit fault in an isolated power system. Assume that initially the parallel feeder is on no load. Then prior to the fault, $\vec{I}_s$ supplies the load and it can be expressed by

$$\vec{I}_s = \frac{\vec{E}}{\vec{Z}_s + \vec{Z}_{Load}} \quad (2.2)$$

where $\vec{Z}_{Load}$ is the load impedance.

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

Suppose then a fault occurs on the parallel feeder. Let $\vec{Z}_f$ represents the feeder impedance between the PCC and the fault location. During fault, the standing feeder current could be approximately expressed as (since $|\vec{Z}_{Load}| \gg |\vec{Z}_f|$)

$$\vec{I}_{sf} \approx \frac{\vec{E}}{\vec{Z}_s + \vec{Z}_f} \quad (2.3)$$

From (2.1), the standing voltage at the PCC during fault, also becomes as the sag voltage, can be obtained

$$\vec{V}_{sag} = \frac{Z_f}{Z_s + Z_f} \vec{E} \quad (2.4)$$

One sees that the sag becomes deeper for faults electrically closer to the customer (i.e. when $|\vec{Z}_f|$ becomes smaller), and for systems with a lower fault level (i.e. when $|\vec{Z}_s|$ becomes larger). The duration of the sag is mainly determined by the fault-clearing time associated with the protection system in the network.

A short circuit fault could also lead to voltage swell. A single line-to-ground fault on the system would result in a temporary voltage rise on the unfaulted phases. This is especially so in ungrounded systems often used in low-voltage marine systems, where the sudden change in ground reference results in a voltage rise on the ungrounded phases.

Sags/swells due to fluctuations of large loads

Fluctuations of large loads such as motors in isolated power systems will also result in voltage sags/swells. As individual load capacity can be relatively large in an isolated power system, load changes would result in appreciable current fluctuations in the system. With high source impedance, such current fluctuations will prone to cause voltage sags/swells at the PCC. Consider the system shown in Fig. 2-3. The difference between this figure and Fig. 2-2 is that the fault impedance $\vec{Z}_f$ shown earlier is replaced by the load impedance $\vec{Z}_M$.

Fig. 2-3 Equivalent circuit for voltage sag due to large load.

When large load changes occur, the PCC voltage is given by

$$\vec{V}_P = \frac{\vec{Z}_M}{\vec{Z}_M + \vec{Z}_S} \vec{E} \quad (2.5)$$

An estimate of the PCC voltage during large load changes can be obtained in the following way. When a large load of VA rated at S_M p.u. is fed from a source with short-circuit level S_S p.u., the source impedance can be expressed as:

$$\vec{Z}_S = \frac{|\vec{V}_n|^2}{S_S} \quad (2.6)$$

where $|\vec{V}_n|$ is the rated voltage of the large load. The impedance of the large load is

$$\vec{Z}_M = \frac{\vec{V}_n^2}{\beta S_M} \quad (2.7)$$

β is the ratio between the operating current and the nominal current of the load which is rated at S_M p.u.

From (2.5), the PCC voltage due to the load switch-on can now be written as:

$$|\vec{V}_P| = \frac{S_S}{S_S + \beta S_M} |\vec{E}| \quad (2.8)$$

Depending on the magnitude of β , the severity of the voltage sag/swell can be estimated.

2.3.2 Causes of Harmonic Distortions

Electricity generation is normally produced at constant frequencies of 50 Hz or 60 Hz and the generators' e.m.f. can be considered practically sinusoidal. However, when a source of sinusoidal voltage is applied to a non-linear device or load, the resulting current is not perfectly sinusoidal. In the presence of system impedance, this current causes a non-sinusoidal voltage drop. Therefore, it produces voltage distortion at the load terminals, i.e. the latter contains harmonics. As the system impedance can be of relatively high value in an isolated power system, one can expect harmonic distortions to appear even more prevalently in such a system. Harmonic distortion is common because of the presence of non-linear devices in the systems such as transformer, rotating machine and power electronic device.

Power transformers are sources of harmonics since they use magnetic materials that are operated very close to the non-linear region of the B-H curves for economic reason [45]. The resulting transformer magnetizing current is non-sinusoidal and contains harmonics even if the applied voltage were sinusoidal.

Rotating machines are considered sources of harmonics because the windings are embedded in slots which can never be exactly sinusoidally distributed so that the m.m.f. is distorted [45].

Yet another common source of harmonics is the power electronic devices. In an isolated power system such as offshore platforms and ships, one often encounters the use of three-phase Graetz bridge [46]. An example of such a bridge is shown in Fig. 2-4. It is known as a six-pulse bridge, there being six pulses or ripples on the DC-side voltage per cycle of AC fundamental. If it is assumed that the bridge is fed from a strong AC busbar and the DC-side consists of a large reactor, the AC phase current is then made up of "blocks" of ripple-free currents as shown in Fig. 2-4. Using Fourier analysis, it can be shown that this waveshape could be described by the series [47]:

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

$$i = \frac{2\sqrt{3}}{\pi} I_d \left(\cos(\omega t) - \frac{1}{5} \cos(5\omega t) + \frac{1}{7} \cos(7\omega t) - \frac{1}{11} \cos(11\omega t) \dots \right) \quad (2.9)$$

where I_d is the DC current.

Fig. 2-4 Six-pulses bridge fed from an infinite bus.

The situation changes somewhat in an isolated power system. The bridge will be fed from an AC system which has significant impedance because of a relatively low short-circuit level compared to the load rating. The handover of current from one phase to the next is prolonged by the AC system impedance. This delay period (or overlap) is due to the commutation process. The waveforms will then appear such as that shown in Fig. 2-5. In this case the AC current drawn by the bridge is slightly less rectangular-shaped. If a Fourier analysis is carried out, it can be shown that this affects in particular higher

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

frequencies which can be significantly reduced [48]. And, the overlap has a significant effect on the AC busbar voltage which will exhibit notching as shown in Fig. 2-5.

Fig. 2-5 Six-pulses bridge fed from a non-infinite bus.

2.4 Impacts of Disturbances on Equipment

If an isolated power system supplies industrial or mining activities, it can be envisaged that there will be a large number of AC or DC motor loads. The machineries are usually of the form of adjustable-speed AC or DC drives. One would also find electronic devices such as computers and process control systems within the loads. These loads are often found to be sensitive to the power quality disturbances. In this Section, a brief description on the impact of voltage sags/swells and harmonics on the electrical equipment will be given. For further reading, interested readers may wish to refer to [13, 45, 49-54].

2.4.1 Impacts of Voltage Sags/Swells on Loads

Most common equipment sensitive to voltage sags/swells include power supply for electronic devices, AC or DC adjustable-speed drives.

Power supply for electronic devices:

Fig. 2-6 A typical computer power supply.

Fig. 2-6 depicts a typical configuration of a computer power supply. It consists mainly of a two-arm diode bridge rectifier, a DC capacitor and a DC/DC converter. The AC input power is rectified through the diode bridge and the bridge output DC voltage ripples are smoothed out by the capacitor. The DC/DC converter then regulates the DC voltage of (typically) few hundreds volts into a regulated DC output of the order of 10V.

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

When the AC supply voltage drops due to an upstream fault, the diodes stop conduction. However energy has to be transferred to the computer and this energy is drawn from the stored energy in the DC capacitor. It results in a continuous drop in the now unregulated V_{DC} . The DC/DC converter is able to keep its output voltage at constant level only down to a certain minimum value of V_{DC} . If V_{DC} is too low and outside its control range, the DC/DC converter will output a low voltage. The control system of the computer will detect this undervoltage and will automatically initiate an action to shut down the computer. In this way, the voltage sag has resulted in an interruption to the computer operation. It leads to the undesirable loss of data and interrupts the flow of work. The decay of V_{DC} , under the unregulated DC-link voltage condition, can be estimated using equation (2.10) taken from [3], if one assumes the computer is a constant power load and the converter system is lossless.

$$V_{DC}(t) \approx V_{DC} \left[1 - \frac{Pt}{C_{DC}V_{DC}^2} \right] \quad (2.10)$$

In this equation: $V_{DC}(t)$ — instantaneous DC-link voltage, P — load real power, V_{DC} — initial DC-link voltage before the voltage sag, C_{DC} — DC-link capacitance, t — time from the start of the sag.

The maximum duration of the voltage that the regulated power supply can provide to the load without loosing its controllability can be obtained from (2.11)

$$t_{sag \max} = \left[\frac{1 - V_{DC \min}^2}{4\varepsilon} \right] T \quad (2.11)$$

where $\varepsilon = \frac{PT}{2C_{DC}V_{DC}^2}$ is the unregulated DC-link voltage ripple, T — period of the fundamental frequency of the input AC supply voltage, $V_{DC \min}$ — minimum DC-link voltage under which the DC/DC converter can provide constant output voltage.

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

It is clear from (2.11) that the lower the ripple voltage in the unregulated V_{DC} , the longer the voltage sag duration which the power supply can operate properly without losing its controllability to the voltage sag.

The effect of a swell can often be more destructive than that of a sag. The overvoltage condition may cause breakdown of components on the power supply of the computer, though the effect may be a gradual, accumulative effect [10].

Adjustable-speed AC drives [49-52]:

The configuration of a most typical AC drive in an isolated power system is shown in Fig. 2-7. The three AC voltages are fed to a three-phase diode rectifier. The output voltage of the rectifier is smoothed by means of a capacitor connected to the DC bus. The DC voltage is inverted to an AC voltage of variable frequency and magnitude. This is the so-called voltage-source converter (VSC). The most commonly used method to achieve the conversion is through pulse-width modulation (PWM) technique. The motor speed is controlled through varying the magnitude and frequency of the output voltage of the VSC. For AC motors, the rotational speed is determined mainly by the frequency of the stator voltages. Thus, by changing the frequency, a ready method of speed control is obtained.

Fig. 2-7 Typical AC drive configuration.

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

Adjustable-speed drives are equally sensitive to voltage sags/swells just like the computer power supply discussed in the previous section. Tripping of adjustable-speed drives can occur due to one or more of the following reasons:

- The drive controller or protection will detect the sudden change in operating conditions and trip the drive to prevent damage to the power electronic components.
- The drop in the DC bus voltage that results from a sag will cause the maloperation or tripping of the drive controller or of the PWM inverter. An increase in the DC bus voltage due to a swell could damage the component.
- The increased AC currents during the sag or the post-sag overcurrents charging the DC capacitor will cause an overcurrent trip or blowing of fuses which protect the power electronics components.
- The process driven by the motor will not be able to tolerate the drop in speed or the torque variations due to the sag.

Adjustable-speed dc drives [53]:

DC motors are used extensively in isolated power systems such as on offshore platforms, since they can provide a high starting torque and offer relatively easy speed control over a wide range.

A typical configuration of a DC motor drive is shown in Fig. 2-8. The armature winding, which uses most of the power supplied, is fed via a three-phase controlled rectifier. The armature voltage is controlled through the control of the firing angle of the thyristors. The longer the delay in the firing angle, the lower is the armature voltage. The torque produced by the DC motor is determined by the armature current I_a , which usually shows almost no ripple due to the large inductance of the armature winding. The field winding is normally powered from one of the phase-to-phase voltages of the supply, and it draws only a small amount of power. Thus a single-phase rectifier is sufficient. To limit

the field current, a resistance (R) is placed in series with the field winding. A capacitor (C) is used to limit the voltage (and torque) ripple.

Fig. 2-8 DC motor drive with separately excited armature and field winding

DC motor drives are particularly susceptible to voltage sag since they normally have no extra energy storage medium, other than the motors' own inertia. Whenever a voltage sag occurs, the DC motor will slow down due to undervoltage or unbalance. Furthermore, since the field winding of most DC motor drives is supplied from an uncontrolled diode rectifier bridge, during a voltage sag, the voltage applied to the field winding will also collapse, thus weakening the field. The time constant of the field winding is rather large compared to the sag duration, and when power is restored, the DC motor may experience an overcurrent in the armature circuit. This is accompanied by an overshoot in the motor speed during the motor re-acceleration. Also, the phase-angle jumps following sags/swells could affect the angle at which the thyristors are triggered. This could cause commutation failures in the controlled rectifier. Since the firing angle of thyristors determines the DC output voltage, this could also affect the normal operation of the DC motor drives. For these reasons, it is clear that voltage sags/swells would interrupt the operations of DC drives in many ways.

2.4.2 Impacts of Harmonic Distortions on Loads

In an isolated power system, there are several mechanisms by which harmonic distortion can affect electronic equipment. Multiple voltage zero crossings as a result of harmonic distortions is the first one to come to consider. It is common for electronic circuits to use the voltage zero-crossing of the fundamental frequency for timing purposes. Semiconductors are often switched at zero voltage crossing to reduce electromagnetic interference and inrush current [55]. However, harmonic distortions that result in more frequent zero crossing than the fundamental frequency can disrupt operation of the equipment. Hence, any device that synchronizes to the zero crossing should be considered vulnerable to disruption by the presence of harmonics.

Electronic power supplies, as shown in Fig. 2-6, use the peak voltage of the AC-side voltage waveform to maintain the filter capacitor C_{DC} at full charge [3]. Depending on the harmonic frequency and phase relationship to the fundamental, harmonic voltage distortion can increase or flatten the waveform peak. Consequently, the power supplies will be effectively operating with over or under input voltage even though the rms input voltage can be nominal. With severe distortion, equipment operation may be disrupted. A moderately flattened waveform may reduce effective operating voltage to the point that equipment is vulnerable to minor voltage sags [56].

Voltage notching can also disrupt operation of electronic equipment [57]. Notches are produced by the commutation of power semiconductors in converters and are quantified by the voltage rate of change (dv/dt) and the volt-time product indices. A voltage notch may cross zero and affect zero crossing sensitive equipment as explained above. For high value of dv/dt , the notch is seen as a voltage step change by the power supply network and can cause the power supply to ring at its natural frequency. The notch, amplified by the power supply resonance, can then disrupt equipment. It is also possible that the high rate of change of voltage associated with the notch can couple through the power supply into digital circuitry and cause a state change that disrupts operation. A large dv/dt may also falsely trigger thyristors into conduction in power circuits.

2.5 Mitigation Methods: a Brief Review

In the previous Sections, voltage sags/swells and harmonics in an isolated power system have been discussed in terms of their origin and their effects on equipment. In this Section a brief description of current as well as some advanced methods to mitigate the effects of the disturbance will be given.

As discussed in Section 2.3, short-circuit faults in an isolated power system would result in voltage sag/swell. Thus reducing the number of short-circuit faults could reduce frequency of such disturbances in the system. Some existing practices to achieve this are: replace overhead lines by underground cables, increase the insulation level of the system or increase maintenance and inspection frequencies. However, these measures may be very expensive and the cost has to be weighted against the consequences of the equipment trips.

When a short-circuit fault occurs, faster fault clearing can significantly limit the sag/swell duration. Rapid fault clearance can be achieved by using current limiting fuses or modern static circuit breakers. Presently, the devices are able to clear fault well within half a cycle of the power frequency, thus preventing sag/swell from lasting for too long.

Installation of redundant component is also an alternative mitigation method. For example, a generator installed near sensitive loads will attempt to maintain the voltage during a sag/swell. It may also be prudent to supply the sensitive loads from two or more busbar. Thus a voltage sag/swell on one busbar will be mitigated by the infeed from the other busbars.

Improvement of equipment immunity is probably one of most the effectively solution against equipment trips. Unfortunately, it is hard to achieve because a customer often have no knowledge of the information about the equipment's immunity at the time of installation. Boosting the equipment immunity after that is often expensive and inconvenient.

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

The most commonly applied method of mitigation is the installation of additional equipment at the system-equipment interface. Conventional mitigation equipment for voltage sag/swell and harmonic distortion are motor-generator set [58] and passive filter [45], respectively. Details of the equipment will be discussed later in this Section.

Due to widespread availability of cost effective high power solid state switches such as GTO and IGBT, a class of mitigation equipment based on power electronic has been proposed relatively recently. This class of power-conditioning devices is called Custom Power devices [1-3, 15]. Details of the equipment will also be discussed in latter part of this Section.

2.5.1 Conventional Mitigation Equipment

In conjunction with the mitigation of voltage sag/swell and harmonics, two conventional equipment will be described.

- **Motor-Generator Set with Flywheel**

Fig. 2-9 Principle of motor-generator set.

A motor-generator set coupled to a flywheel is an old solution for mitigating voltage sag/swell. It consists of an induction motor and a synchronous generator, as shown in Fig. 2-9. They are coupled on a common axis to a large flywheel. The flywheel acts as an energy buffer. The motor would convert the incoming electrical energy to mechanical energy, and the mechanical energy would keep the generator to rotate to supply the

sensitive load. When the source supply suffers a sag or interruption, the flywheel could maintain the synchronous generator rotation and thus continues to supply the sensitive load. However, normal operation losses are high which makes this an expensive solution.

- **Passive filter**

A passive filter is a well-known device for mitigating harmonic distortions. The most common type of passive filter is the single-tuned shunt “notch” filter. A typical example of single-tuned shunt filter circuit and its impedance variation with frequency is illustrated in Fig. 2-10. The notch filter is series-tuned to present low impedance to a particular harmonic current, as shown. As it is shunt-connected, harmonic currents are diverted from their normal flow path on the line into the filter. ω_r is the resonant frequency corresponding to the inductive (L) and capacitive (C) reactances of the filter, i.e. $\omega_r = 1/2\pi\sqrt{LC}$. Thus the impedance of the filter at ω_r is the filter resistance (R). The quality of the filter Q is defined as the ratio of the inductive reactance (or the capacitive reactance) to R at ω_r , i.e. $Q = \omega_r L / R$. Q determines the sharpness of the tuning and a typical value is between 30 and 60. PB is the filter pass band which is defined as being bounded by the frequencies at which the filter reactance equals its resistance, i.e. the impedance angle is 45° and the impedance module $|Z| = \sqrt{2}R$.

Fig. 2-10 (a) Single-tuned shunt filter circuit; (b) single-tuned shunt filter impedance versus frequency.

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

While single-tuned shunt filter is sharply tuned to one of the lower harmonic frequencies, damped filter has a low impedance over a wide range of frequency. When used to eliminate the higher-order harmonics (e.g. 17th upwards) it is also referred to as a high-pass filter. A typical example of damped filter circuit and its impedance variation with frequency are illustrated in Fig. 2-11. For this case, $Q = R/\omega_r L$ and has a typical value in the region of 0.1-0.5.

Fig. 2-11 (a) Damped filter circuit; (b) damped filter impedance versus frequency.

In applications in which six-pulse converters are present for example, considerable $6h \pm 1$ ($h=1, 2, 3, \dots$) order harmonics would be produced. These can be filtered out using a hybrid combination of single-tuned branches for the low orders, i.e. 5th, 7th, 11th, and 13th, and high-pass damped filter for the 17th and higher orders.

There is one major disadvantage of passive filters: they are designed to deal with specific harmonic components. They are not adaptable to successfully filter varying harmonics. For instance, a cycloconverter can present particular difficulties since the frequencies of the harmonics produced will vary with operation. Likewise, a system experiencing much supply or load changes can also expect a variation in the harmonics produced. In addition, interaction between the capacitance in the passive filters and system impedance can, in fact, result in a system resonance condition. The resonant point itself will subject to

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

change as the distribution system varies. These are serious drawbacks on the use of the passive filters.

2.5.2 Custom Power Devices

Custom Power, a term first introduced by N. G. Hingorani [1], describes a technology-driven product and service solution which embraces a family of power electronic based devices. The purpose of it is to enhance power quality at distribution level. The rapid response of these devices to disturbances enables them to operate in real-time, providing continuous and dynamic control of the supply including: sub-cycle transfer of critical loads, voltage regulation and elimination of harmonics [14, 59, 60]. Custom Power devices and their functions are listed in Table 2-3. Among the devices, one of the most promising Custom Power devices is the Series Compensator (SC). The SC can be used to realize dynamic voltage control and regulate voltage at the terminals of loads. Details of the SC will be discussed later.

Table 2-3 The Custom Power family

Device	Function
Static Transfer Switch (STS)	<ul style="list-style-type: none"> • Fast bus transfer (sub-cycle)
Solid State Breaker (SSB)	<ul style="list-style-type: none"> • Rapid interruption • Fault current limitation
Solid State Current Limiter (SSCL)	<ul style="list-style-type: none"> • Slows the rate of rise for large fault current • Amplitude damping of minor disturbance
Distribution Static Compensator (DSTATCOM)	<ul style="list-style-type: none"> • Shunt connected • Provide real time Var compensation • Minimize transient and harmonics
Series compensator (SC)	<ul style="list-style-type: none"> • Series connection • Dynamic voltage compensation • Voltage regulation
Active Filter (AF)	<ul style="list-style-type: none"> • Reduction of harmonic and transients

Static Transfer Switch (STS)

Static Transfer Switch (STS) is a solid-state switch based on the Silicon Controlled Rectifier (SCR), as shown in Fig. 2-12 [61]. The strategy of the STS is to supply the sensitive loads from preferred source while having an alternate source available, in the event there is a disturbance on the preferred source. Each source is connected to the load with anti-parallel switches SW1 or SW2. The transfer can be achieved within $\frac{1}{4}$ - $\frac{1}{2}$ cycle of the fundamental frequency [62]. Sensitive loads usually can tolerate a disturbance of such magnitude and duration. The normally closed isolating switches B1 and B2 are required in order to disconnect the STS for maintenance of SCR modules and testing purpose. The STS system must be able to supply loads even if the SCR switches are not in service. Therefore two bypass switches are connected to the preferred and alternate feeder, as shown. One disadvantage of the STS is that the STS cannot mitigate the effects of an upstream common voltage disturbance that affect both feeders.

Fig. 2-12 Configuration of a Static Transfer Switch (STS).

Solid State Breaker (SSB)

Solid State breaker (SSB) is a gate turn-off thyristor (GTO) based device [63]. A typical SSB is shown schematically in Fig. 2-13. The GTO switch is the normal current carrying

element. At the onset of a fault, the GTO switch goes through a number of sub-cycle auto-reclose operations. If the fault does not clear, the GTO switch is turned off and the SCR switch is turned on such that fault current flows through the current limiting reactor. The current is eventually cut off by blocking the SCR. The zinc oxide (ZnO) arrester is used to protect the power electronics from lightning and switching transient. After the SCR switch is blocked, there can be a small amount of feeder current still flowing through the ZnO arrester. Thus a conventional switch installed (CB) in the system can interrupt the current. SSB can disconnect the faulted circuit in less than $\frac{1}{2}$ cycle of the fundamental supply frequency [64]. However, the SSB cannot be used to mitigate voltage disturbances that originate upstream of the device.

Fig. 2-13 Schematic diagram of the prototype Solid State Breaker.

Solid State Current Limiter (SSCL)

Solid State Current Limiter (SSCL) offers a viable solution to the power quality problems caused by high fault current [65]. SSCL can be divided into two types: non-superconducting and superconducting types. Non-superconducting current limiters are based on power electronic devices with conventional series reactors or a combination of capacitors and reactors [66].

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

The schematic diagram of a typical non-superconducting current limiter is shown in Fig. 2-14. It consists of a SCR switch in parallel with the current limiting reactor L_{lim} . Generally, the current limiter is connected in series with a feeder. Under normal operation, the SCR switch is in on-state and carries the line current. When a downstream fault is detected, the switch opens so that the fault current will flow through the current limiting inductor (L_{lim}) and therefore the current would be limited. In addition, a series RC combination ($R_{snubber}$ and $C_{snubber}$) is connected in parallel with the SCR switch. This RC combination can reduce the high transient current caused by SCR switching operation. One disadvantage of the non-superconducting current limiter is the power loss in the power electronics during normal operation.

Fig. 2-14 Schematic diagram of a solid-state current limiter.

On the other hand, due to the low loss in the superconducting current limiter during normal operation, a device based on this limiter can be an attractive solution in controlling fault current levels in the power networks [67]. In the event of a fault, the superconducting current limiter (L_{lim}) will produce an impedances due to their losing its superconductivity. The impedance is inserted into the circuit. Superconducting current limiter currently available include magnetic-shield type [68], saturable magnetic core type [69], and diode bridge type [70]. Advantages of all superconducting devices are their low reactance on the grid during normal operation as well as their quick reaction when desired, even with high rated powers. The disadvantages are that they are still rather expensive, and the presence of extremely high magnetic fields can be a concern.

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

It should be noted the existing fault current limiter could only be used to limit downstream fault current. They can also be used to mitigate the impacts of the voltage sag due to a downstream fault on upstream equipment. For upstream fault condition, however, these devices are not capable of maintaining downstream load voltages. As will be shown in Chapter 6, this shortcoming is not seen in the SC described there as it is a Custom Power device designed to mitigate the effect of voltage sag resulting from upstream fault. Furthermore, by introducing fault current limiting function to it, the SC can reduce voltage sag resulting from downstream fault. This latter function will be discussed in details in Chapter 6.

Distribution Static Compensator (DSTATCOM)

Distribution Static Compensator (DSTATCOM) is normally used for reactive power compensation at a particular bus of a power system. The STATCOM is connected to the bus in the power system via a coupling transformer, as shown in Fig. 2-15, to maintain the bus voltage at a desired level. This is achieved by absorbing or injecting reactive power. The compensator basically consists of a voltage source inverter (VSI), coupling transformer, connection filter and a small DC energy storage device normally in the form of a capacitor. As the capacitor has very small DC energy storage capacity and is merely sufficient to cater for system losses, DSTATCOM only draws or injects reactive power. The operating principle of the DSTATCOM is that the VSI generates a variable voltage with controllable magnitude on the filter-side of the coupling transformer and injects a controllable current which maintains the load voltage at a desired value.

Unfortunately, some voltage disturbances cannot be mitigated without the injection of real power to the load [71]. If the DSTATCOM is to be used to compensate for all type of sags, where both magnitude and phase angle of the injected voltage are required to be controlled, additional energy storage would be needed in the DSTATCOM [29]. Thus the cost of the device will increase.

Fig. 2-15 Typical configuration of DSTATCOM.

Series Compensator (SC)

Among the novel Custom Power devices, the Series Compensator (SC) is the most technically advanced and promising device developed so far for mitigating voltage sag/swell [72-75]. Indeed, the world's first SC was installed by Westinghouse-EPRI in August 1996 on one part of the Duke Power Company (North Carolina) 12.47 kV distribution system to protect an automated yarn manufacturing and weaving factory from disturbances, originating from the utility distribution system. The experience of this installation in terms of SC mounting structure, testing of the SC, protection, etc. is given in [33]. With the increase in interest and the necessity in mitigating voltage sags in power systems, ABB has also introduced a SC composed of newly developed Integrated Gate Commutated Thyristors (IGCT) [76]. The basic design criteria of the ABB SC, IGCT technology and protection measures of the SC have all been well addressed in this work. The operating principle and the topology used are similar to that of the Westinghouse-EPRI SC except for the switching devices used. As the main focus of the thesis is on series compensation, a more detailed description of the technology will now be given.

As a general observation, the SC shares a similar hardware structure to the DSTATCOM. The major difference is that this controller is connected in series with the distribution feeder and the protected sensitive load through an injection transformer. A typical SC schematic is shown in Fig. 2-16. The power system upstream to the SC is represented

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

herewith by a voltage source V_s and a series impedance Z_s , calculated based on the fault level at the point of common coupling (PCC). Both V_s and Z_s can substantially vary during fault condition. When the PCC voltage ($\vec{V}_p$) is under voltage disturbance condition, the role of the SC is to restore the load-side voltage $\vec{V}_L$ to its nominal level through injecting a voltage $\vec{V}_{sc}$ in series with the incoming supply voltage. Thus $\vec{V}_{sc}$ can be expressed as

$$\vec{V}_{sc} = \vec{V}_L - \vec{V}_p \quad (2.12)$$

Fig. 2-16 Schematic diagram of a typical SC.

Fig. 2-17 shows, in time-domain, this injection strategy in restoring the sensitive load voltage. The sag event is initiated at 0.02s. When the sag occurs, the SC will inject voltage as shown. The sensitive load voltage (V_L) is then restored to the pre-sag voltage.

Fig. 2-17 Transient state during injection.

The central part of the SC is a voltage source inverter (VSI) which produces the required voltage $\vec{V}_{sc}$ to be injected in series with the incoming supply voltage. Pulse width modulation (PWM) technique is usually used in the VSI, due to the flexibility of controlling the ratio between the fundamental frequency component of output voltage and the DC-link voltage, its fast response to load and source changes, elimination of low order harmonic which results in reduction of output filter rating and the simplicity of implementation. The series injection transformer is used to boost and couple the injection voltage generated by VSI into the feeder circuit.

The output of the PWM-controlled VSI will include a large amount of high-order harmonics due to the high switching frequency of the VSI. Therefore, a harmonic-filtering system is necessary to offer a clean injected voltage on the primary-side of the injection transformer. Generally, the filter system will consist of a L-C section. The values of the filter components will depend on the switching frequency of VSI. The filtering system can be placed either on the primary side (line-side filter system) or on the secondary side (inverter-side filtering system) [28, 77]. In this thesis and where relevant, inverter-side filter is adopted in the design of the SC.

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

The controller is also needed to provide the necessary signal in order to generate the PWM gating pulse for the SC inverter. The scheme can be in the form of open loop control [25] or closed-loop control [78]. In the open loop control, the control signal is derived by comparing the load voltage (V_L) against a desired reference (V_{ref}), as shown. The output voltage is sensed and fed back to be compared with a desired reference in the closed-loop control technique. The details will be included in subsequent chapters.

During voltage compensation, the SC would supply (or absorb) real and reactive power to (from) the system. Thus energy storage system is required to provide the needed real power buffer. Large capacitors are used as the storage medium in most of the commercially available SC. Other possible energy storage devices are battery bank, supercapacitor, superconducting magnetic energy storage (SMES) and flywheel.

One distinct feature of the SC is that it can provide voltage support for individual load. This is not possible with DSTATCOM unless the load is fed by a dedicated feeder. In the event if the SC is without energy storage, it is still capable of providing series compensation by injecting a continuously variable, leading or lagging voltage vector in quadrature with the line current and hence providing a complementary set of function to the DSTATCOM. When sufficient energy storage facility is added, the SC can mitigate almost all types of the voltage sags, a feature which will be illustrated in Chapter 5. In this way, the SC is capable of providing a far more economical solution to DSTATCOM for situations where sags are the major concern. Mitigating voltage sags originated in the distribution feeders are impractical with DSTATCOM while the SC can mitigate them readily.

In conclusion, the SC is preferred over the DSTATCOM in mitigating the effects of voltage sags/swells in an isolated power system. It will be shown in the subsequent chapters that the function of the SC can be extended to mitigate harmonics and to limit fault current.

Active Filter (AF)

Active filter (AF) is a Custom Power device intended essentially for eliminating harmonics [79]. They have the distinct advantage that they do not resonate with the system. They can also address more than one harmonic at a time and mitigate other power quality problems such as flicker. They are particularly useful for situations involving the supply to large, distorting loads fed from relatively weak points in a power system.

Fig. 2-18 The principle of an active filter.

Active filter is simple in concept in that if one were to add two currents, identical in magnitude and frequency but opposite in phase, then the net result will be zero. Advances in digital signal processing (DSP) and power electronic switches mean that this simple concept can now be applied to the cancellation of unwanted harmonics in electricity supply system. As shown in Fig. 2-18, the filter is connected in parallel with the nonlinear load. For each phase, the distorted load current I_L and the filter current I_C are sampled at

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

high frequency, providing an error signal for the feedback control loop. The signals from the current transformers are digitized, and advanced DSP techniques are then used to implement filtering to the specified level for the individual harmonics at the required speed [80]. The end result would be a source current I_s which is essentially sinusoidal.

The inverter used in the active filter is basically a three-phase IGBT bridge with the DC bus being sustained by a DC capacitor [81]. The inverter charges the capacitor while it is generating the compensation current and thus a separate power supply is not required. Depending on what filtering is desired, the inverter generates a PWM output voltage, which is converted into the required current by a PWM reactor and an output filter.

The active filter can also produce reactive power. It can be set to produce a fixed amount of reactive power, or to achieve a user-specified power factor. However, as power factor correction is not the main task of the filter, and it is often recommended that a detuned capacitor bank is used to provide power factor correction and some harmonic cancellation. This will allow the use of a smaller active filter, resulting in lower overall cost [82].

2.6 Conclusions

A description of some common features of an isolated power system and the associated power quality problems are given in this chapter. Since voltage sag and harmonic distortion are the two most common power quality disturbances in such a power system, simple analysis of the disturbances illustrating the origin and their impacts on loads are also presented. The mitigation methods for these disturbances are also described. Among the mitigation methods described, the use of a series compensator (SC) is explained. In dealing with voltage sags/swells, the application of a SC is viable because it is of much smaller capacity compared to a shunt compensator such as a DSTATCOM. Details of SC structure and functions are also included in this chapter.

As will be shown in the next chapters, the SC is a promising Custom Power device to mitigate voltage sag/swell. Furthermore, the function of the SC can be extended through relatively inexpensive modification of its control scheme. The present work will attempt

Chapter 2 Supply Quality Issues Pertaining to Isolated Power Systems

to explore these techniques by which the compensator role can be extended to include that of the mitigation of harmonics and that of the fault current limiting in an isolated power system.

Chapter 3 A Series Compensation Method to Mitigate Harmonics

3.1 Introduction

As discussed in Chapter 2, the growing concern on power quality has resulted in much research attention being directed toward the design of Custom Power devices [1]. Among such devices are those which are based on series compensation technique applied to interconnected or grid systems [83-85]. The compensator is designed to mitigate voltage perturbations, in the form of voltage-sag or voltage-swell. The series compensator (SC) achieves the mitigation function through a scheme of injecting a voltage $\vec{V}_{sc}$, generated from a voltage-source inverter (VSI) system as described in Section 2.5.2.

While enhancing power quality in interconnected systems has attracted much research interest, unfortunately much less attention has been directed toward solving the same problem in isolated power systems. This is despite the fact that one can still encounter situations where loads are supplied by relatively small-capacity power networks which are not parts of a grid. Examples of such isolated power systems include small networks in oil exploration areas and remote mining districts. These isolated power systems are typically characterized by generation capacity of up to a few MVA. The electrical sources can be in the form of diesel generator-sets and the p.u. equivalent source impedances tend to be high because of the sparsity of the networks. The loads are often relatively large DC or AC motor-drives: the variable-speed drives or machinery would be supplied by the generators via power converters. The loads are non-linear and would involve the commutation process of the converters. The consequence would be distortions in the voltage/current waveforms in the supply system, the extents of which are likely to

Chapter 3 A Series Compensation Method to Mitigate Harmonics

fluctuate as the loads change [40]. At the same time, the variations in the drive load would result in voltage sags/swells appearing in the upstream voltage.

In addition to the industrial-drive loads, one can also expect the presence of low-power sensitive loads such as electronic power supplies or electronic controllers in the power systems. These devices are necessary to ensure the proper functioning of the exploration/mining activities. Even though the total capacity of the sensitive loads can be much smaller than that of the drives or machinery, short-duration disturbances in the form of the voltage sags or swells can affect the operations of the sensitive loads and thus the whole power system. Hence industry standards, such as that prescribed under the ITI curve [43], have been developed to quantify what would be considered acceptable power quality for these sensitive loads. With regard to mitigation methods, the authors of [86, 87] propose methods to improve power quality of isolated power systems through the use of flywheel energy storage system or active power filter respectively, such as those described in Section 2.5.1. These are promising technologies and no doubt, will find ready applications if they can be made cost-effective.

A possible alternative method to improving the power quality of an isolated system is through the use of a series compensator (SC). The application of a SC is viable because it is of smaller capacity compared to a shunt compensator, and through which one can still expect to achieve similar level of voltage quality control. Unlike previous works [18, 33, 76] on SC in which harmonic voltages/currents in the networks have been ignored, this chapter will explore the technique by which the compensator role can be extended to include that of the mitigation of harmonics in an isolated power system. Generally speaking of course, the harmonic problem should be solved at source, e.g. at the terminals of the main drive loads. However, the proposed technique is shown to require only relatively modest modification of the SC control scheme and the addition of a small inductive filter. Therefore, the proposed scheme could be an attractive alternative to that described in [86, 87]. Furthermore, besides the control of the SC to achieve harmonics mitigation, the control of the voltage in the energy storage system in the SC will also be described. The proposed scheme is then validated through simulation. Simulation results

Chapter 3 A Series Compensation Method to Mitigate Harmonics

are included to show the effectiveness of the technique on harmonics mitigation and on network voltage control.

Laboratory measurements on an experimental prototype of the proposed system will be described in Chapter 4, for the purpose of verifying the theoretical results.

The contents of part of this Chapter also appear in [88].

3.2 System Model

Fig. 3-1. A typical isolated power system installed with a SC.

The simple power system model shown in Fig. 3-1 is used to explain the principle of the proposed compensation method. The upstream generators are represented as an ideal voltage source and Z_S represents the equivalent source impedance. The main drives or machinery loads are modeled as a lumped resistance-inductance load connected to the source through a power converter, which is assumed to be an uncontrolled six-pulse rectifier in this study. The much smaller-capacity sensitive loads are assumed supplied through a separate feeder. Often, such critical or sensitive loads such as PC and control devices contain input rectifiers that are capacitive in nature. Although these loads could also be non-linear, however, their combined capacity is small compared to the main

Chapter 3 A Series Compensation Method to Mitigate Harmonics

rectifier loads. Hence, the sensitive loads are assumed to be linear as their contributions towards the distortions in V_s is negligible. In the investigation, the combined sensitive load is modeled by the resistance R in parallel with the capacitor C shown in Fig. 3-1. The value of R will be obtained based on the real power drawn by the sensitive load at the voltage V_L . C can be obtained from the data supplied by the rectifier manufacturer.

The SC is connected upstream of the sensitive load through an injection transformer. It is series-connected with the sensitive load and its function is to ensure that the voltage across the sensitive load terminals (V_L) is of high quality. The function of the SC to mitigate voltage disturbances has been briefly described in Section 2.5.1, details can be found in [16]. It is suffice to state herewith that the VSI synthesizes the required voltage quantity (V_{out}) which would be injected in series with V_L . The ESS would act as a buffer and provides the energy needed for load ride-through during a voltage-sag. Conversely, during a voltage-swell, excess energy from the network would be stored in the SC. In this way, the terminal voltage V_L of the protected sensitive load can be regulated to maintain at a constant level [16, 32].

During the operations of the main non-linear converter-drive loads, harmonic currents generated by the loads will cause a voltage drop across Z_s . Thus it results in distortions in V_s : V_s consists of the fundamental and harmonic voltage components.

While the above assumes the harmonic source is of the non-linear loads, the case of a harmonic generating renewable source upstream can also be dealt with using the technique shown below.

3.3 Harmonic Compensation

3.3.1 Principle of Harmonic Compensation

The underlying principle when the SC is used to compensate for upstream voltage sag/swell has been briefly explained in Chapter 2. In Fig. 3-1, distorted voltage V_s will

Chapter 3 A Series Compensation Method to Mitigate Harmonics

appear on the upstream source-side of the sensitive load and the phase voltages can be expressed as

$$\mathbf{V}_S = \begin{bmatrix} V_{Sa} \\ V_{Sb} \\ V_{Sc} \end{bmatrix} = \begin{bmatrix} \sum_{n=1}^{\infty} [V_{0n} + \hat{V}_{1n} \sin(n\omega_o t + \varphi_{1n}) + \hat{V}_{2n} \sin(n\omega_o t + \varphi_{2n})] \\ \sum_{n=1}^{\infty} [V_{0n} + \hat{V}_{1n} \sin(n\omega_o t + \varphi_{1n} - 2n\pi/3) + \hat{V}_{2n} \sin(n\omega_o t + \varphi_{2n} + 2n\pi/3)] \\ \sum_{n=1}^{\infty} [V_{0n} + \hat{V}_{1n} \sin(n\omega_o t + \varphi_{1n} + 2n\pi/3) + \hat{V}_{2n} \sin(n\omega_o t + \varphi_{2n} - 2n\pi/3)] \end{bmatrix} \quad (3.1)$$

for phases a, b and c, where ω_o is the fundamental frequency, n is the harmonic order; V_{0n} is the zero phase sequence voltage component; $\hat{V}_{1n}$ and φ_{1n} are the magnitude and phase of the positive phase sequence voltage component; $\hat{V}_{2n}$ and φ_{2n} are the magnitude and phase of the negative phase sequence voltage component. Clearly, distorted voltage is undesirable at the sensitive load terminals. The desirable terminal voltage is the fundamental components of the voltages contained in equation (3.1), i.e.

$$\mathbf{V}_{S1} = \begin{bmatrix} V_{Sa1} \\ V_{Sb1} \\ V_{Sc1} \end{bmatrix} = \begin{bmatrix} \hat{V}_{11} \sin(\omega_o t + \varphi_{11}) \\ \hat{V}_{11} \sin(\omega_o t + \varphi_{11} - 2\pi/3) \\ \hat{V}_{11} \sin(\omega_o t + \varphi_{11} + 2\pi/3) \end{bmatrix} \quad (3.2)$$

The proposed voltage injection method is to compensate for the difference between V_S and the desired voltages described by equation (3.2). This can be achieved by injecting an ac voltage component in series with V_S and the desirable injected voltages would have to contain all the harmonic components in equation (3.1). Let $\mathbf{V}_{Sh}$ be the vector containing all the harmonic components in equation (3.1). Hence, from equations (3.1)-(3.2), the injection voltage from the SC would have to be

$$\mathbf{V}^* = -\mathbf{V}_{Sh} = \mathbf{V}_{S1} - \mathbf{V}_S \quad (3.3)$$

$\mathbf{V}_S$ can be measured online and its fundamental voltage component $\mathbf{V}_{S1}$ can be extracted using, for example, a Phase Locked Loop (PLL) scheme. Hence using equation (3.3), the

desirable injection voltage V^* can be generated online and used to mitigate the harmonic distortions in the manner described below.

3.3.2 A Possible SC Control Scheme

Fig. 3-2 shows the sensitive load-SC branch whereby the SC, through the injection of the voltage V_{out} , compensates for the harmonic voltage. In this study, the resistance and leakage inductance of the injection transformer are assumed negligible. The distorted source-side voltage V_S is represented as a harmonic voltage source. Z_L denotes the parallel RC load shown in Fig. 3-1 and its terminal voltage is V_L . The corresponding line current is I_L .

Fig. 3-2 Schematic diagram showing the interconnection of the SC with the sensitive load.

From Fig. 3-2, the following differential equations can also be obtained:

$$\left. \begin{aligned} V_{inv} &= V_{out} + L_f \frac{dI_{Lf}}{dt} \\ I_{Lf} &= I_c + I_L \\ I_c &= C_f \frac{dV_{out}}{dt} \end{aligned} \right\} \quad (3.4)$$

The block diagram of the control scheme for a conventional SC designed for load ride-through enhancement function during a voltage-sag is given in Fig. 3-3 [17]. The reason for adopting this scheme is that previous works which use this technique of current-voltage feedback scheme appear to produce promising results. Hence as an initial attempt,

Chapter 3 A Series Compensation Method to Mitigate Harmonics

the same scheme could be adopted here for the purpose of mitigating harmonic distortions as well. As shown, the control scheme consists of an outer voltage feedback loop as well as an inner current feedback loop, with gain settings (K_1, K_2) as shown. In this scheme, the injection voltage V_{out} is regulated to follow the reference voltage V^* which is generated through equation (3.3). Thus it requires V_{out} to be compared with V^* . The error is multiplied by the voltage error feedback gain $K_2 C_f$ and fed to the second stage as the reference for the inductor current. This virtual inductor current reference I_{Lf}^* is compared with the actual inductor current I_{Lf} and the error is multiplied with the current error gain $K_1 L_f$ to form the inner feedback loop. The resulting quantity of this loop is subsequently fed to the PWM generator of the inverter.

Fig. 3-3 A possible closed-loop control scheme for the SC.

During voltage compensation, V_{DC} will change due to the interchanges in energy flow. To compensate for the changes in V_{DC} , the duty cycle command to the VSI will be multiplied by a factor V_{ref}/V_{DC} . In this case, V_{ref} corresponds to the full-scale command voltage of the inverter. As the switching frequency of the inverter is usually several orders of magnitude above the fundamental, the dynamics of the inverter are ignored. The inverter is thus assumed as a simple unity gain in the subsequent analysis. In this way, it simplifies the analysis.

The load current I_L is considered as a disturbance caused by sensitive load changes. The effect of I_L on the harmonic distortions is not the main concern in the design of this controller. Instead, the present focus is on the control of V_{out} to track V^* , i.e. the SC is

Chapter 3 A Series Compensation Method to Mitigate Harmonics

only used to mitigate the effect of the distortions in V_L caused by the upstream main rectifier loads. For this purpose, the closed-loop transfer function between V_{out} and V^* of Fig. 3-3 can be shown to be:

$$G_{cl}(s) = \left. \frac{V_{out}(s)}{V^*(s)} \right|_{I_L=0} = \frac{K_1 K_2}{s^2 + K_1 s + K_1 K_2} \quad (3.5)$$

However, Fig. 3-3 shows that the load current (I_L) also affects V_{out} and the complete expression of V_{out} can be expressed as

$$V_{out}(s) = G_{cl}(s)V^*(s) + Z_{SC,Inv}(s)I_L(s) \quad (3.6)$$

where $Z_{SC,Inv}(s) = -\frac{s}{s^2 + K_1 s + K_1 K_2} \cdot \frac{1}{C_f}$. Expressed in this way, $Z_{SC,Inv}(s)$ is the equivalent series impedance of the SC, which will be designed to have a very low value at ω_o . $G_{cl}(s)$ is a second-order system; therefore, the damping ratio and the un-damped natural frequency of the SC control system are given as

$$\xi = 0.5\sqrt{K_1/K_2} \quad (3.7)$$

$$\omega_n = \sqrt{K_1 K_2} \quad (3.8)$$

In order to obtain a critically damped response, $\xi = 1$ and this can be achieved when

$$K_2 = K_1/4 \quad (3.9)$$

Substituting (3.9) into (3.5), $G_{cl}(s)$ can be rewritten as

$$G_{cl}(s) = \frac{1}{\left(1 + \frac{s}{K_1/2}\right)^2} \quad (3.10)$$

With regard to the selection of K_1 , increasing K_1 will improve any disturbance rejection property of the closed-loop system. However, in practice, K_1 cannot be increased without

limit due to the presence of delay in the VSI. This delay has not been considered in the above analysis. This can be incorporated because over low-frequency range, the inverter could be approximated as a zero-order hold of duration T equals to the duration of the PWM's period. The inverter can therefore be represented by a first order lag block, of time constant T . The bandwidth of such a first order lag is $1/T$ rad/s. Even though this is an approximation, it does provide one an idea on the limit of K_1 . A typical setting range for K_1 is less than $2/T$.

3.3.3 Effects of Commutation and Design Constraints

As stated, the reference voltage (V^*) of the control system can be obtained according to equation (3.3). Due to the effect of commutation, V^* consists of six distinct segments per cycle. By adopting the control scheme shown in Fig. 3-3, typical waveforms of V^* and V_{out} of the SC are shown in Fig. 3-4 (a). As the SC has a finite bandwidth, a phase lag would be introduced into the control system. Hence it explains the observation that V_{out} lags V^* . As a consequence, large voltage pulses appear in the difference between the two voltages at the beginning of each segment. The difference is shown in Fig. 3-4 (b). Obviously a more detailed analysis of the controller scheme is called for because the large voltage errors are detrimental to the satisfactory performance of the power system.

(a)

(b)

Fig. 3-4 (a) Waveforms of V^* and V_{out} of SC; (b) Difference between V^* and V_{out} .

The difference in the voltages can be ‘modeled’ approximately as a train of square waves, with six pulses appearing per cycle. Notice that the RC sensitive load impedance decreases rapidly at high frequency, in a manner shown as curve (a) in Fig. 3-5. As a result, the voltage pulses will cause large harmonic current distortions to appear in I_L . The distortions have to be mitigated to protect the sensitive load.

Fig. 3-5 A typical frequency response characteristic (a) the RC load and (b) the combined filter L and RC load.

Limited by the finite bandwidth of the SC, the high-frequency components of I_L cannot be effectively eliminated solely by controlling the SC itself through the controller shown

Chapter 3 A Series Compensation Method to Mitigate Harmonics

in Fig. 3-3. It is proposed that an inductive filter L be installed between the SC and the sensitive load, as shown in Fig. 3-2. L can act as a low-pass filter to eliminate the high-frequency components of I_L . However the presence of L could cause fundamental frequency voltage regulation problem. Additional consideration has to be taken and this will be dealt with in Section 3.4.

With L in place, only the square wave voltage components shown in Fig. 3-4(b) will appear across the sensitive load terminals, as the high-frequency components would have been filtered off. During the commutation process, the reference voltage is a sine function [47], the slope of which could be obtained. As each diode conducts for 120° for an uncontrolled six-pulse rectifier, thus results in the waveform of V^* shown in Fig. 3-4 (a). Hence, the duty cycle of the square wave is $2/3$. Furthermore, from the series compensator transfer function shown in equation (3.10), the time lag in the SC system can be determined. The magnitude of the square wave can therefore be estimated using the slope and the time lag, in the manner as shown in Fig. 3-6. The voltage harmonic components of the square wave can be obtained through Fourier analysis. This will provide the necessary information to generate the additional voltage harmonic injection voltage through the SC into the circuit. The injection will therefore comprise of the harmonics of the pulse waveform.

Fig. 3-6 Determine the magnitude of the square wave.

Chapter 3 A Series Compensation Method to Mitigate Harmonics

The RMS value of the final harmonic current can then be determined (or at least approximated), using the voltage harmonics determined and applied across the impedance of the circuit external to the SC.

The aim would then be to design the impedance for the external circuit to meet a certain criterion: i.e. to limit the total harmonic distortion (THD) in $\mathbf{I}_L$.

3.4 Proposed Design

With the filter L included, the impedance of the combined RC load and L will increase at high frequencies. Unfortunately, a resonance will occur due to the combination of L and C in the circuit, shown by curve (b) in Fig. 3-5. This is a concern because any harmonic voltage which has a frequency close to the resonant frequency will result in large resonant current. To overcome this problem, one possibility is to introduce a damping resistor into the circuit but the increase in line loss does not make it an attractive proposition. Instead, a method to control the equivalent impedance ($Z_{SC,inv}$) shown in equation (3.6) is proposed herewith. The technique would produce the same effect as that of the damping resistor but without causing increased line losses. Suppose $Z_{SC,inv}(s)$ is adjusted by an amount $\Delta Z(s)$. Then from equation (3.6) the resulting output voltage of the SC is

$$\mathbf{V}_{out}(s) = G_{cl}(s)[\mathbf{V}^*(s) + R'(s)\mathbf{I}_L(s)] + Z_{SC,inv}(s)\mathbf{I}_L(s) \quad (3.11)$$

where the function $R'(s) = \Delta Z(s)/G_{cl}(s)$.

From Fig. 3-2, the following differential equations can also be obtained:

$$\left. \begin{aligned} (\mathbf{V}_{S1} + \mathbf{V}_{Sh} - \mathbf{V}_{out} - \mathbf{V}_L) \cdot \frac{1}{Ls} &= \mathbf{I}_L \\ (\mathbf{I}_L - \frac{\mathbf{V}_L}{R}) \cdot \frac{1}{Cs} &= \mathbf{V}_L \end{aligned} \right\} \quad (3.12)$$

Fig. 3-7 Block diagram of the SC-sensitive load with load current feedback.

The block diagram of the L - RC branch with the SC is thus re-drawn as shown in Fig. 3-7, but with the load current feedback through $R'(s)$. Source-side voltage (V_s) consists of the fundamental frequency voltage V_{s1} and the harmonic voltage V_{sh} . From previous section, equation (3.3) shows that V_{sh} is the reference voltage V^* to be injected into the system. $G_{cl}(s)$ is the transfer function defined by equation (3.10). From equation (3.11), it can be seen that V^* will now become $V^* + R'(s)I_L(s)$. $R'(s)I_L(s)$ can be readily implemented since I_L is measurable and can be used in the feedback control scheme.

In the proposed method, $R'(s)$ is designed as a lead-lag filter of the form $(s + \omega_1)/(s + \omega_2)$ and has the typical frequency response characteristic shown as curve (a) in Fig. 3-8. Thus $R'(s)$ appears as high impedance for high frequency current components while the fundamental frequency component in I_L will not be affected.

With $R'(s)$ in place, the total impedance of the sensitive load branch is now modified to become

$$Z'(s) = L(s) + R'(s)G_{cl}(s) + Z_L(s) \quad (3.13)$$

where $L(s)$ is the impedance of the inductive filter.

Chapter 3 A Series Compensation Method to Mitigate Harmonics

Fig. 3-8 Frequency response characteristic of (a) $R'(s)$ and (b) $R'(s) \cdot G_{cl}(s)$.

The voltage drop term $[L(s) + R'(s)G_{cl}(s)]I_L$ at the fundamental frequency ω_o will have to be controlled to satisfy prescribed voltage regulation requirement. Suppose the sensitive load terminal voltage is to be at least $V_{\min}$ p.u. Then the voltage drop is to be at most $(1 - V_{\min})$ p.u., assuming the nominal load voltage is 1 p.u. Thus the following voltage regulation constraint has to be met:

$$|L(j\omega) + R'(j\omega) \cdot G_{cl}(j\omega)| \cdot |I_L| < (1 - V_{\min}) |Z_{L,fullload}(j\omega)| \cdot |I_L| \quad (3.14)$$

has to be satisfied. $Z_{L,fullload}(j\omega)$ is the impedance of the sensitive load under the full load condition.

From equation (3.10), it can be seen that $G_{cl}(j\omega)$ is close to unity at ω_o as V_{out} has to track V^* . Then equation (3.14) reduces to

$$|L(j\omega) + R'(j\omega)| < (1 - V_{\min}) |Z_{L,fullload}(j\omega)| \quad (3.15)$$

This places a constraint on the choice of L and $R'(s)$.

To limit the high-frequency harmonics, one also has to maximize the total branch impedance Z' described by equation (3.13) at high frequency. The variables in this design are $L(j\omega)$ and $R'(s)G_{cl}(s)$. Note that for $R'(s)$ to assume the form of a lead-lag

Chapter 3 A Series Compensation Method to Mitigate Harmonics

filter with two cutoff frequencies ω_1, ω_2 , the difference in the magnitude of $R'(s)$ at low frequency and that at high frequency is governed by the ratio ω_1/ω_2 , as shown in Fig. 3-8 (a). It is desirable for $R'(s)$ to be small at low frequencies such that it does not cause excessive voltage drop across the SC terminals for $\omega = \omega_o$. So if ω_2 can be pushed higher, the low frequency impedance due to $R'(s)$ can then be reduced. Limited by the bandwidth of $G_{cl}(s)$, $R'(s)G_{cl}(s)$ assumes high impedance value over a range of frequencies, in the manner shown as curve (b) in Fig. 3-8. If the series resonant frequency happens to fall within this frequency range, the possibility of having large current at the resonant frequency is removed. Beyond this frequency band, the contribution of L in providing the high frequency impedance into the branch comes into effect. The frequency response characteristics of the branch impedance will then assume the form shown in Fig. 3-9.

Fig. 3-9. A typical frequency response characteristics of $Z'(s)$.

The above analysis is based on the condition that the SC contains no injection transformer. With an injection transformer included, the plant model needs to include the transformer turns-ratio, and its impedance. However the approach to the design will be similar.

3.5 Control of Sensitive Load Terminal Voltage

Previous section describes the consideration on the conceptual design of the SC. However, there is one important aspect of the design which has not been considered in detail. This is pertaining to the control of voltage at the terminals of the sensitive load. Thus the purpose

of this section is to describe a control scheme so that the SC will then be able to achieve the dual function of compensating momentary voltage sags/swells in the power system, in addition to mitigating harmonic distortions as considered earlier.

3.5.1 Description of the Control Strategy

Fig. 3-10 The isolated power system with the SC.

For the convenience of analysis, a single-phase equivalent system (phase “a”) is used to describe the three-phase system shown in Fig. 3-10. As the harmonic distortions have been dealt with in Section 3.3, only the fundamental frequency component of the voltages and currents will be considered in this section. Let $\vec{V}_{S1}$ denotes the fundamental frequency component of the source-side voltage and that of the load-side voltage is $\vec{V}_{L1}$. $\vec{V}^*$ is the fundamental component of the injection voltage (also the reference voltage) and $\vec{I}_{L1}$ is the fundamental component of the sensitive load current. $\vec{I}_{L1}$ is taken as the reference phasor.

In (3.3), one has only considered the condition that V_s contains harmonic distortions. However, a voltage sag/swell may appear in V_s and hence, V_{S1} could differ from specified desirable value. Assume the desirable load side fundamental voltage component is

Chapter 3 A Series Compensation Method to Mitigate Harmonics

$$V_{L1}(t) = \hat{V}_{L1} \sin(\omega_o t + \varphi_{11}) \quad (3.16)$$

From (3.3), let $V_{out}(t)$ be the injected voltage across the primary winding of the SC injection transformer. Therefore,

$$V_{out}(t) = V_{L1}(t) - V_{S1}(t) - V_{Sh}(t) \quad (3.17)$$

The instantaneous power at the SC output is

$$p(t) = V_{out}(t)I_L(t) = \sum_{k=1}^{\infty} \hat{V}_{Sk} \sin(k\omega_o t + \varphi_k) \sum_{k=1}^{\infty} \hat{I}_{Lk} \sin(k\omega_o t + \varphi_k) \quad (3.18)$$

As the only significant source of energy storage in the SC is the ESS, $p(t) > 0$ will result in the export of energy from the SC to the external system and a decrease in the voltage V_{DC} . Conversely V_{DC} will rise if $p(t)$ is continuously negative. Variation of V_{DC} will affect the compensation capability of the SC and excessive voltage rise will damage the ESS. Hence V_{DC} has to be controlled to within certain acceptable range, i.e. $p(t)$ has to be regulated. One way to achieve this is by adjusting the phase angle of the fundamental component of the load voltage $\vec{V}_L$. If a phase-shift α is introduced into $\vec{V}_{L1}$, from (3.17) one obtains a new injection voltage:

$$V_{out}(t) = \hat{V}_{L1} \sin(\omega_o t + \varphi_{11} + \alpha) - [V_{S1}(t) + V_{Sh}(t)] \quad (3.19)$$

where

$$V_{S1}(t) = \hat{V}_{S1} \sin(\omega_o t + \varphi_{11}) \quad (3.20)$$

In the present problem formulation, it is assumed that the process of the upstream load change brings about momentary sags and swells in $\vec{V}_{L1}$. The basic requirement of the compensation is that the magnitude of the load voltage $\vec{V}_{L1}$ be maintained constant. Assuming constant impedance for the sensitive load, it follows from equations (3.18) and (3.19) that the instantaneous power flow at the SC output is:

Chapter 3 A Series Compensation Method to Mitigate Harmonics

$$\begin{aligned}
 p(t) &= V_{out}(t)I_{Load}(t) = \\
 &[\hat{V}_{L1} \sin(\omega_o t + \varphi_{11} + \alpha) - \hat{V}_{S1} \sin(\omega_o t + \varphi_{11}) - \sum_{k=2}^{\infty} \hat{V}_{Sk} \sin(k\omega_o t + \varphi_k)] \\
 &\cdot [\hat{I}_{L1} \sin(\omega_o t) + \sum_{k=2}^{\infty} \hat{I}_{Lk} \sin(k\omega_o t + \varphi_k)]
 \end{aligned} \tag{3.21}$$

The cycle-average value of $p(t)$ is

$$\left. \begin{aligned}
 P &= P_1 + P_h \\
 P_1 &= -\frac{1}{2} \hat{V}_{S1} \hat{I}_{L1} \cos(\varphi_{11} + \alpha) + \frac{1}{2} \hat{V}_{L1} \hat{I}_{L1} \cos(\varphi_{11}) \\
 P_h &= -\frac{1}{2} \sum_{k=2}^{\infty} \hat{V}_{Sk} \hat{I}_{Lk} \cos(\phi_k) \quad \text{where } \phi_k = \varphi_k - \theta_k
 \end{aligned} \right\} \tag{3.22}$$

P contains two terms: a contribution each from the fundamental frequency component and the harmonics. P_1 corresponds to the power flow of the fundamental component. From equation (3.22), it is readily seen that it is controllable through the introduced phase shift α . The harmonic power flow term, P_h , is assumed to be constant under the steady-state considered. Thus P can be controlled through P_1 via the adjustment in α . P_h will not be included in the subsequent analysis shown in this chapter. It would be re-introduced in Chapter 5 where an alternate SC scheme is proposed.

Based on the above principle, the control strategy of α for varying load conditions can be obtained. Let the sensitive-load power factor at the fundamental frequency be $\cos \theta$. This implies that in equation (3.19), $\theta = \varphi_{11} + \alpha$ since $\vec{I}_{L1}$ is considered as the reference phasor. P_1 can be rewritten as:

$$P_1 = \frac{1}{2} [-\hat{V}_{S1} \cos \theta + \hat{V}_{L1} \cos(\theta - \alpha)] \cdot \hat{I}_{L1} \tag{3.23}$$

It would be reasonable to assume that the speed by which the sensitive load could vary is slow compared to that of adjusting α . Hence one may assume the load power factor and hence θ is constant over the interval when α changes. By differentiating equation (3.23), the rate of change of P_1 , as α varies, is therefore

$$\frac{dP_1}{dt} = \frac{dP_1}{d\alpha} \frac{d\alpha}{dt} = -\frac{1}{2} \hat{V}_{L1} \hat{I}_{L1} \sin(\theta - \alpha) \cdot \frac{d\alpha}{dt} \quad (3.24)$$

The last expression shows that the direction of change of P_1 due to a change in α will depend on the sign of $\sin(\theta - \alpha)$. This can be illustrated by the phasor diagram of Fig. 3-11. As the intention of the voltage injection is to ensure that the fundamental component of the load voltage $\vec{V}_{L1}$ is to be maintained constant, the loci of $\vec{V}_{L1}$ will be a circle with the radius equal to the nominal value of the load terminal voltage V_{L1} , as defined in equation (3.16).

Fig. 3-11. Phasor diagram showing voltage injection for a leading power factor load: fundamental frequency component.

Fig. 3-11 shows the condition of a voltage swell as the load-side voltage is higher than its nominal value, i.e. $V_{S1} > V_{L1}$. The phasor triangle consisting of $\vec{V}_{S1}$, $\vec{V}^*$ and $\vec{V}_{L1}$ (in solid lines) depicts the final result after the voltage injection has been carried out. From equation (3.23) and also can be seen from Fig. 3-11, P_1 is proportional to the difference in the magnitudes of the components of $\vec{V}_{S1}$ and $\vec{V}_{L1}$ projected onto $\vec{I}_{L1}$. As shown, it shows the case of $P_1 > 0$. If the intention is to reduce P_1 , a continued reduction of α (i.e. forcing α to move in the clockwise direction) from this point onward will achieve this

Chapter 3 A Series Compensation Method to Mitigate Harmonics

objective. Indeed, one can continue to adjust α until $\vec{V}^*$ is perpendicular to $\vec{I}_{L1}$ and $P_1 = 0$. This is the condition shown by the dotted lines in the figure. Also from equation (3.24), one observes that an increase in α will result in an increase in P_1 for $\theta < \alpha < 180^\circ + \theta$, i.e. $\sin(\theta - \alpha) < 0$. The relationship between α and P_1 for other range of α can be similarly obtained under the leading power factor condition, i.e. $-90^\circ < \theta < 0$. The results of the above analysis are summarized in Table 3-1. From the results shown in the table, it is clear that a simple strategy to effect changes in P_1 can be readily realized through the adjustment in α . Although the case of lagging power factor load can be similarly analyzed, in the present investigation, only the case of leading power factor load has been studied because the sensitive load is assumed to be capacitive in nature.

Table 3-1: Variations of P_1 with α .

	$\theta < \alpha < 180^\circ + \theta$	$\theta - 180^\circ < \alpha < \theta$
α decreases	P_1 decreases	P_1 increases
α increases	P_1 increases	P_1 decreases

3.5.2 Simplified ESS Control Dynamics

Having obtained the relationship between P_1 and α , the dynamics of the ESS voltage during the phase adjustment stage will now be examined. The instantaneous rate of change of the ESS energy (E) is given by

$$\frac{dE}{dt} = CV_{DC} \frac{dV_{DC}}{dt} \quad (3.25)$$

where C and V_{DC} are the capacitance and the terminal voltage across the ESS. In general, V_{DC} comprises of a slow-varying average value and a pulsating voltage ripple. To study the dynamic behavior of $\hat{V}_{DC}$, one will need to consider the relatively slow-varying average E, denoted as $\hat{E}$. The averaging could be carried out (say) over 10 cycles of the fundamental frequency. In this way, one can express the instantaneous ESS energy and capacitor voltage as

Chapter 3 A Series Compensation Method to Mitigate Harmonics

$$\left. \begin{aligned} E &= \hat{E} + \delta E \\ V_{DC} &= \hat{V}_{DC} + \delta V_{DC} \end{aligned} \right\} \quad (3.26)$$

δE and δV_{DC} in (3.26) represent the difference between the respective instantaneous values and their averages. δV_{DC} would contain frequency components higher than the fundamental. Substituting (3.26) into (3.25) yields:

$$\left. \begin{aligned} \frac{d\hat{E}}{dt} + \frac{d(\delta E)}{dt} &= C\hat{V}_{DC} \frac{d\hat{V}_{DC}}{dt} + \\ C[\delta V_{DC} \frac{d\hat{V}_{DC}}{dt} + \hat{V}_{DC} \frac{d(\delta V_{DC})}{dt} + (\delta V_{DC} \frac{d(\delta V_{DC})}{dt})] & \end{aligned} \right\} \quad (3.27)$$

Extracting from (3.27) the low frequency term which has frequency lower than the fundamental yields

$$\frac{d\hat{E}}{dt} \approx C\hat{V}_{DC} \frac{d\hat{V}_{DC}}{dt} \quad (3.28)$$

Neglecting inverter losses and the negligible change in the stored energy in the filter elements, re-arrange terms in (3.28), one concludes that the rate of change of V_{DC} is proportional to the power exchange between the SC and the external power system, thus

$$\frac{d\hat{V}_{DC}}{dt} \approx \frac{1}{C\hat{V}_{DC}} \frac{d\hat{E}}{dt} \approx \frac{P}{C\hat{V}_{DC}} \quad (3.29)$$

By consolidating (3.22), (3.24) and (3.29), the simplified dynamic model relating the rate of change of α and $\hat{V}_{DC}$ is obtained as shown in Fig. 3-12 (a). Using the model, one can readily obtain the proposed control scheme shown in Fig. 3-12 (b) in which $\hat{V}_{DC}$ is regulated to its nominal value $\hat{V}_{DC}^*$ through the use of the feedback variables P_1 and $\hat{V}_{DC}$. The voltage loop has been included as it is desirable to exercise some control on $\hat{V}_{DC}$ and regulate it with respect to the reference $\hat{V}_{DC}^*$. The voltage error is multiplied by the voltage error feedback gain K_v/G_2 and fed to a second stage as the reference for P_1 . This virtual power reference is compared with the actual P_1 . The error is multiplied with the power

Chapter 3 A Series Compensation Method to Mitigate Harmonics

error gain K_p/G_1 to form an inner feedback loop. The resulting quantity of this loop is $d\alpha/dt$.

(a)

(b)

Fig. 3-12 (a) Dynamic model describing the relationship between $\hat{V}_{DC}$ and $d\alpha/dt$; (b)

Block diagram of the proposed closed-loop control scheme.

From Fig. 3-12(b), it can be shown that the closed-loop transfer function between $\hat{V}_{DC}^*$ and $\hat{V}_{DC}$ is

$$G_{DC}(s) = \frac{\hat{V}_{DC}}{\hat{V}_{DC}^*} = \frac{K_V K_P}{s^2 + K_P s + K_V K_P} \quad (3.30)$$

$G_{DC}(s)$ is a second-order system; therefore, the damping ratio and the un-damped natural frequency of the SC control system are

$$\xi = 0.5\sqrt{K_P/K_V} \quad (3.31)$$

$$\omega_n = \sqrt{K_P K_V} \quad (3.32)$$

Chapter 3 A Series Compensation Method to Mitigate Harmonics

For a critically damped response system, $\xi = 1$ and this is achieved when

$$K_V = K_P / 4 \quad (3.33)$$

Substituting (3.33) into (3.30), $G_{DC}(s)$ can be rewritten as

$$G_{DC}(s) = \frac{1}{\left(1 + \frac{s}{K_P / 2}\right)^2} \quad (3.34)$$

Note that the inner loop of the controller in Fig 3-12 is to control the average fundamental power and the calculation of the average power. This requires at least one power-frequency cycle. The control action of the outer loop should be on a longer time-scale, otherwise the system will be unstable. So ω_n should be selected to be less than the bandwidth of the inner loop.

3.6 Verification through Simulation

A series of simulation studies have been carried out using MATLAB/SIMULINK software to verify the efficacy of the SC and its control strategy. The example used in the simulation is similar to that shown in Fig. 3-1. The corresponding parametric values used are given in Table 3-2. It is observed that the VA capacity of the study system is much smaller compared to a typical isolated system. The reason is because the parameters were chosen so that an identical system can be implemented in a laboratory prototype, to be described in the next Chapter. The design of the filter for the SC is based on the technique described in [24]. The energy storage capacitor and inductive filter is chosen to be 6000 μ F and 20 mH respectively. The selection is again based on the availability of the components in the laboratory. The controller design is based on the method described earlier. As the switching frequency of the VSI was chosen to be 20 kHz the controller shown in Fig. 3-3 was used for harmonic compensation and based on the setting of damping ratio of 1 and the un-damped natural frequency of $2\pi \cdot 500$ rad/sec. Notice that this choice of the undamped natural frequency is for the purpose of harmonic level control. It corresponds to 10th harmonic order.

Chapter 3 A Series Compensation Method to Mitigate Harmonics

Using the method described in Section 3.3, thus $K_1 = 2\pi \cdot 1000$ and $K_2 = 2\pi \cdot 250$. The controller shown in Fig. 3-12 was used for ESS voltage control. Thus the controller was determined based on the setting of $\xi = 1$ and $\omega_n = 7.5$ rad/sec. Thus from (3.31) and (3.32), $K_p = 15$ and $K_v = 3.75$. Notice that this lower ω_n has been selected because this is for the purpose of controlling the ESS voltage due to the power exchange between the SC and the external system. Hence, a much lower ω_n has been selected.

Table 3-2 System parameters for simulation and experiment.

Parameters	Value
Main rectifier load capacity	900VA (p.f. 0.98)
Sensitive load capacity	100VA
Filter inductor for SC (L_f)	4 mH
Filter capacitor for SC (C_f)	18 μ F
Energy storage capacitor (C)	6000 μ F
Inductive filter (L)	20mH

3.6.1 Effectiveness of Harmonic Mitigation

Fig. 3-13 shows the waveforms of terminal voltage and current drawn by the sensitive load without the SC. It can be readily shown that the voltage has a THD level of 23%. The current has a large harmonic content: its THD is 110%.

Fig. 3-14 shows the corresponding waveforms when the SC is switched into service at $t=0.05$ s. The initial transient lasts for almost 0.1s. With harmonics compensation by the SC, the sensitive load is protected against the distortion introduced by the main drive load and the THD of I_L has been significantly reduced to about 4%. And the fundamental rms value of the sensitive load is 35V and the voltage THD is close to 1%.

Chapter 3 A Series Compensation Method to Mitigate Harmonics

Fig. 3-13 Terminal voltage (V_L) and current (I_L) drawn by the sensitive load: without SC.

Fig. 3-14 Terminal voltage (V_L) and current (I_L) drawn by the sensitive load: with SC.

3.6.2 Effectiveness of the Voltage Control of ESS

Fig. 3-15 shows the voltage V_{DC} across the ESS but without the phase shifting of the fundamental frequency component (V_{L1}) of the reference voltage. The main rectifier load is at 900 VA. As soon as the SC starts to mitigate the harmonic distortions and momentary sag, it is seen that V_{DC} decreases. It shows that the SC is injecting power to the external system. This is obviously un-sustainable for the continuous operations of the SC.

Fig. 3-15 Terminal voltage of ESS without phase shift in the reference voltage.

Fig. 3-16 (a) shows V_{DC} when the main load is at 900 VA but with the proposed phase shifting of the fundamental frequency component of the SC reference voltage (V^*). As before, once the SC starts to mitigate the harmonics, V_{DC} decreases as the SC injects power to the external power system. When V_{DC} reaches the minimum threshold value of 50V set in the study, the controller begins to introduce the phase shift. Indeed, Fig. 3-16(a) shows that the voltage can be restored to its nominal level.

It is also interesting to illustrate how the SC would response to changes in the main drive load. Fig. 3-16 (b) shows V_{DC} when a decrease of 20% in the main drive-load from its rated level has been introduced at the instance indicated. The reduction in the main load has resulted in a decrease of the harmonic currents and voltages. Thus the harmonic power ($\hat{P}_h$) that the SC needs to compensate also decreases and V_{DC} increases. Upon reaching the maximum threshold value set at 80V, phase adjustment is initiated. Fig. 3-16 (b) shows that the technique is again effective in maintaining the ESS voltage.

Fig. 3-16 Terminal voltage (V_{DC}) of ESS with phase shift in the fundamental component of the reference voltage: (a) at nominal load level; (b) with a 20% decrease in load level.

3.7 Conclusions

In this chapter, power quality improvement in an isolated power system through series compensation has been investigated. The power system is assumed to contain a significant proportion of non-linear loads and a high level of harmonic distortions is observed. A method to control the injection voltage of the SC so that it can mitigate the effects of the harmonics has been proposed. The method is based on the control of the SC branch impedance. A load-current feedback scheme is incorporated in the control system of the SC, in conjunction with an inductive filter intended for mitigating the high-order harmonic currents. The design of the filter and feedback scheme has been described. In the process of harmonic voltage compensation, it is shown that power exchange exists between the SC and the external network. The function of the SC is then extended to control the terminal voltage of the protected sensitive load. The technique used is through

Chapter 3 A Series Compensation Method to Mitigate Harmonics

the phase adjustment of the fundamental frequency component of the reference voltage of the SC. Through the analysis of the energy exchange, a strategy on the phase adjustment has been obtained. Simulations results have confirmed the effectiveness of the proposed method, as it is applied on the SC to achieve improved quality of supply in the power system.

Chapter 4 Experimental Prototype of a Series Compensator to Mitigate Harmonics

4.1 Introduction

In Chapter 3, power quality enhancement in an isolated power system through series compensation has been studied. A method to control the SC so that it can mitigate the effects of the harmonics has been described. The simulation results given in Chapter 3 show the effectiveness of the proposed method. To verify the efficacy of the proposed strategy in a practical environment, a hardware prototype of the isolated power system and a series compensator has been constructed as part of the present investigation. In this Chapter, the design of the prototype will be described. Experimental results showing the performance of the system are also included.

4.2 On Overview of the Completed Prototype System

This Chapter deals with the real-time digital control of a Series Compensator. The technique is based on cost effective digital signal processor (DSP) hardware system which has become popular in the field of digital control. The DSP hardware architecture enables most of its instruction to be executed in a single instruction cycle and complex control algorithm can be implemented in a much faster rate compared to the single-chip microprocessors. Thus, with this development in the digital control, the performance of the proposed control method of SC can be easily implemented by setting up a prototype of an isolated power system with the proposed SC in a DSP hardware architecture environment.

Chapter4 Experimental Prototype of a Series Compensator to Mitigate Harmonics

A photograph of the completed system is shown in Fig. 4-1. The parametric values of the prototype correspond to those given in Table 3-2. The isolated power system is a four-wire three-phase system and is supplied by an independent source. The main load is a lumped resistance-inductance load supplied by an uncontrolled six-pulse rectifier. The capacity of the non-linear load is 900VA, as was in the simulation described in Chapter 3. In order to reduce the complexity of the laboratory setup, the sensitive load used is a single-phase resistive-capacitive load of 100VA. Hence the SC was constructed using an IGBT, 2-legs single-phase full bridge. The proposed controller was implemented using a DS1103 controller card, with its output signals driving the hardware IGBT inverter.

Fig. 4-1 Laboratory prototype of the isolated power system showing the main load and components of the series compensator.

4.3 Description of the SC Hardware Prototype

As the SC is the key part in the test power system, in this Section, the design of the SC is described. The specifications of the SC are:

- Inverter type: Single-phase Full Bridge “H” PWM Inverter
- Inverter output: 0.55 kVA, 110Vrms, 50Hz
- Input DC link voltage: 300V DC
- IGBT modules: SKM 50 GAL 123D
- Gate drive: HCPL-3120
- Applied gate drive voltage: 0-15V (floating supply)
- Switching frequency: 20 kHz
- Individual Voltage Distortion: 3% (Based on IEEE standards)

The layout of the SC in the single-phase configuration is shown in Fig. 4-2. The SC is made up of the full bridge inverter, PWM module, IGBT gate drive module, output LC filter and feedback control module. It also includes energy storage capacitor, DC power supply connected to the DC-link, current transducers, voltage transducers, interface circuit, and 15V DC power supply.

Fig. 4-2 Layout of the Series Compensator.

4.3.1 Voltage Source Inverter

The single-phase full bridge voltage source inverter consists of two legs of IGBTs as shown in Fig. 4-3. The inverter is rated 0.55 kVA which is much larger than that of the sensitive load. The reason is that the inverter is intended to be built and then used in another project investigation in the laboratory. This is in order to save cost. Nevertheless, the results obtained in this prototype will still be very useful to validate the theoretical work of Chapter 3. Two IGBT modules (SKM50) each consists of two switches have been used for the inverter, denoted by IGBT A, IGBT A', IGBT B and IGBT B'. These switches can operate up to the switching frequency of 20 kHz. Voltage and current rating of IGBTs in the modules is 1200V and 50A respectively.

Fig. 4-3 Single-phase full bridge inverter.

The Pulse-Width Modulation switching pattern is used to control the output voltage of VSI in this project. In the converter circuits, in order to produce a sinusoidal output voltage waveform at a desired frequency, a sinusoidal control signal at the desired frequency is compared with a triangular waveform, in the manner as shown in Fig. 4-4 (a). The triangular waveform V_{tri} , which is also called the carrier wave, is at a switching frequency of, in this case, 20 kHz. It establishes the frequency with which the converter switches are turned on/off. $V_{control}$ has a frequency of 50 Hz in this set-up. When $V_{control}$ is greater than V_{tri} , IGBT A and B will turn on and when the opposite condition occurs,

Chapter 4 Experimental Prototype of a Series Compensator to Mitigate Harmonics

IGBT A' and B' will turn on. Due to the switching pattern of the IGBTs, a pulse waveform shown in Fig. 4-4 (b) is obtained.

Fig. 4-4 Pulse width modulation.

An output LC filter is connected to the output of the inverter to filter off any high frequency components in the pulses generated by the switches. The LC filter also smoothes the pulses fed into it to generate an almost ripple free output signal. An inductor of 4mH and a capacitor of 18 μ F have been used as filter inductance and filter capacitor. Details of the design will be given in the next section. A DC capacitor of 6000 μ F is used as the energy storage capacitor. A resistor of 20 $k\Omega$ connected to the capacitor provides a path for the capacitor to discharge when the system is off.

As the DC link voltage source is normally fed from the system, hence the loop inductance and resistance seen by the IGBTs will be very larger. In order to reduce the loop inductance and resistance seen by the IGBTs, a capacitor of 0.1 μ F and a resistor of 1.2M Ω is connected in parallel with the IGBT. By so doing, the IGBTs will see the

Chapter4 Experimental Prototype of a Series Compensator to Mitigate Harmonics

capacitor as the DC link voltage source and hence reduce the loop inductance and resistance.

As heat is dissipated during the switching of the IGBTs, to prevent overheating of the IGBTs, the IGBT modules were mounted on a heatsink.

4.3.2 PWM Module and Gate-drive Module

The IGBTs are turned on by applying a positive gate-emitter voltage of 15V and turn off by connecting the gate to emitter. The PWM circuit generates the logic control signals used to control the turning on and off of the power switches. Its input is the scaled voltage signal that represents the desired voltage. The output signal of the PWM Generator is sent to a Dead Time Circuit. To avoid turning on the upper and lower IGBTs in the same leg simultaneously, the Dead Time Circuits are introduced. The Gate Drive Circuit is the interface between the control circuit and the IGBTs. It provides electrical isolation and scales the control signals to the required level to drive the IGBTs. For each leg of the IGBTs, one module of Gate Driver module is required. Thus, for one single-phase inverter system, two Gate Driver modules are needed to drive the two legs of the IGBTs.

The signal from the PWM module to the Gate Driver module is of different grounding potential; hence a ground loop is created. When the loop is created, a small current flows in the interconnection of two grounds and a voltage is induced. The induced voltage is able to pick up noise and this can introduce unwanted signal into the switching signals and hence cause false triggering of the IGBTs. Also with such a path to provide current flow, should there be faults occurring on either side of the system, the fault current may also flow from the affected part to the unaffected part of the system. This high fault current can damage the electronic circuits in the system. Therefore, it is best to avoid creating ground loop in the system, or the number of ground loops in the system shall be kept to the minimum.

Besides taking note of the ground loop issue, false triggering of the IGBTs can also be due to the presence of leakage inductance. Therefore, it is a general good practice to keep

Chapter4 Experimental Prototype of a Series Compensator to Mitigate Harmonics

the length of cables connecting the Gate Driver module and the two legs of IGBTs as short as possible. The cables are twisted together to reduce interference. In this way, leakage inductance produced by the twisted cable is minimized.

4.3.3 Current Transducers

LEM current transducers which use Hall effect principle to measure instantaneous value of complex waveform are used as CTs, as analog input of the DS1103 controller board accepts only voltage signals. The output of the LEM current transducers can vary from -10 V to 10 V .

4.3.4 Voltage Transducers

PCB mounting voltage transducers (LEM LV25-P) are used for measuring the source voltage and the output voltage of VSI. The voltage measurements of these transducers are also based on the Hall effect principle. An external resistor is connected in series with the primary circuit of the unit in order to obtain the voltage measurements: the transducer provides a current in the secondary side which is directly related to the primary-side current. The secondary current is then converted to a voltage using a known resistor connected on the secondary side of the unit.

4.3.5 Feedback Control Module

Control algorithms are implemented using a DSP 1103 PPC controller board shown in Fig. 4-5. The DSP 1103 PPC controller board consists of a Motorola Power PC 6043/333MHz main processor and Texas instruments TMS320F240/40MHz slave subsystem with powerful features. It has 16 channels of 16-bit ADC, 4 channels of 12-bit ADC, 8 channels of 14-bit DAC, 6 channels of digital input incremental encoder subsystem and 4 channels of 8-bit digital I/O ports. The slave DSP is an independent subsystem that supports symmetric and asymmetric PWM generation. It also consists of capture inputs, 16 channels of 10-bit ADC and digital I/O system. All off-chip memory and I/O can be

Chapter 4 Experimental Prototype of a Series Compensator to Mitigate Harmonics

accessed by the host even while the DSP is running, thus allowing easy setting up and monitoring.

Fig. 4-5 Block diagram of DS1103 controller board.

4.4 Implementation of the Control Scheme

The supply voltage, sensitive load current, output voltage of the SC, filter inductor current and DC-link capacitor voltage are measured using the voltage and current transducers and fed to the A/D converters of the DSP controller board. A/D outputs are then multiplied by appropriate scale factors, determined by a preliminary test in order to obtain the actual values of the measured quantities. The implementation of the control algorithm is accomplished by the dSPACE DS1103 PPC/333MHz controller board connected to a Pentium II host computer. The real-time interface (RTI) adds a hardware specific block library to the MATLAB/SIMULINK software environment which allows SIMULINK to be linked with the real-time hardware of the DSP. Once the controller is built in the

Chapter4 Experimental Prototype of a Series Compensator to Mitigate Harmonics

SIMULINK environment, it is then downloaded to the dSPACE Control Desk Software in order to implement the controller in real-time. The sampling frequency of controller is set to 10 kHz. The supply voltage, sensitive load current, output voltage of the SC, filter inductor current and DC-link capacitor voltage are measured in every sampling interrupt and the reference signal is generated. The generated reference signal is fed to the gate drive board through the D/A converter of the DSP controller board. The output signal of the gate drive board is used to drive the IGBT inverter.

4.5 Experimental Results

4.5.1 Effectiveness of SC for Harmonic Compensation

Fig. 4-6 shows the waveforms of the terminal voltage and current drawn by the sensitive load without the SC in service. The loads are at rated values. It is seen that voltage distortion at the load terminal is much higher than normally considered acceptable: indeed it can be shown that the terminal voltage THD is 41%. The sensitive load current is also high in harmonics, with its THD at 143%. The test condition is worse than that of simulation because the independent source used in the laboratory is far from ideal: its generated voltage contains harmonic components even before the loads were connected.

Fig. 4-6 Terminal voltage and current drawn by the sensitive load: without SC.

Chapter4 Experimental Prototype of a Series Compensator to Mitigate Harmonics

Fig. 4-7 shows the corresponding waveforms when the SC is in service. With harmonics compensation provided by the SC, the sensitive load is protected against the distortion introduced by the main drive load and the THD of the sensitive load current has been significantly reduced to 10% and that of its terminal voltage is only 3%. In this part of the experiment, the ESS capacitor was actually connected in parallel with an additional DC source. The reason for this is because during compensation the SC was supplying power to the external system. Without the DC source, this operation is not sustainable because V_{DC} will reduce very quickly before any meaningful measurements could be obtained.

Fig. 4-7 Terminal voltage and current drawn by the sensitive load: with SC.

4.5.2 Effectiveness of Voltage Control of ESS

Fig. 4-8(a) shows the voltage across the ESS without the phase adjustment of the fundamental frequency component of the reference voltage. As was pointed out in Section 3.5 and illustrated by the simulation result, the voltage decreases as the SC injects power into the external system. Clearly this is not a sustainable operation.

Chapter 4 Experimental Prototype of a Series Compensator to Mitigate Harmonics

Fig. 4-8 Terminal voltage of ESS (a) without and (b) with phase shift in the reference voltage.

Fig. 4-8 (b) shows the voltage of the ESS but with the proposed phase shifting of the fundamental frequency component of the reference voltage. Very much similar to the simulation result, it shows that indeed the ESS voltage can be regulated by the proposed phase adjustment of V^* .

The performance of the power system under the condition of main load change of -20% is shown in Fig. 4-9(a). It shows conclusively that following the decrease in the load level, the proposed strategy for the SC is effective in maintaining V_{DC} . Fig. 4-9 (b) shows the corresponding sensitive load terminal voltage and current drawn by the sensitive load. The THD of the terminal voltage is again at an acceptable level of 3% and that of the current is only 9%. Fig. 4-10 (a) and (b) shows the respective RMS value of the sensitive load terminal voltage without/with the SC, measured during the load change test. It can be seen that the voltage has been kept constant by the SC.

Chapter4 Experimental Prototype of a Series Compensator to Mitigate Harmonics

(a)

(b)

Fig. 4-9 Converter load change by -20%: (a) ESS voltage with phase shift in the reference voltage; (b) Corresponding terminal voltage and current of the sensitive load.

(a)

(b)

Fig. 4-10 Sensitive load terminal voltage (a) without SC and (b) with SC when the main load changes.

4.6 Conclusions

In the Chapter, the hardware prototype of an isolated power system is described. To verify the efficacy of control scheme described in Chapter 3, a prototype of the SC has been constructed in laboratory. The control method proposed in Chapter 3 has been implemented in the experimental setup. Experimental results demonstrate that the proposed scheme is effective to improve the power quality of the isolated power system, not only in terms of reducing harmonic distortion but also mitigating voltage sags/swells that can occur due to load changes. At the same time, the voltage of the ESS can also be maintained during the operation. The experimental results are essentially in line with the simulation results, thus giving increased confidence in the approach used in the analysis described earlier.

Chapter 5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

5.1 Introduction

As discussed in Chapter 3, isolated power systems such as those on-board of ships, in oil exploration areas and remote mining districts are characterized by limited generating capacity, supplying loads which can consist of significant amount of motor-drives and power converters. The power systems are often considered weak in that they possess relatively low short-circuit ratio, in comparison to a grid. Network voltage control becomes a challenging task as a result. The power quality problem is compounded as the drive-converter loads are likely to fluctuate in conjunction with the mining or exploration activities. The motor-converter load is non-linear and would involve the commutation process of the converter. The consequence would be distortions in the voltage/current waveforms in the supply system, the extents of which are likely to fluctuate as the load changes [38, 39]. At the same time, the variations in the drive load would result in voltage sags/swells appearing in the upstream voltage. As a consequence, the sensitive load in parallel with the main load would face not only harmonic distortion but also voltage sag/swell. Thus the challenge is to regulate the sensitive load terminal voltage so that its magnitude remains constant and any harmonic distortion is within an acceptable level. In Chapter 3, a series compensation method is proposed to mitigate the harmonics problem encountered by the protected sensitive load. However the compensation for voltage sags/swells has been considered in which the harmonic power has been ignored. Indeed, this is the same shortcoming as can be seen in [32, 33]. The investigation described in this chapter is intended to fill this gap. Essentially, the intention is to develop a method to control the fundamental component of the sensitive load terminal voltage. The control is

Chapter 5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

achieved by regulating power flow via phase angle adjustment. Unlike the previous methods described in [32, 33], one important finding is that the investigation also shows that the voltage-sag ride-through capability of the sensitive load can be improved through importing harmonic power from the external system into the SC.

The technique to be considered is also applicable if the upstream source is of a renewable generator.

5.2 Harmonic Mitigation and Power Flows

In this chapter, similar system model as that used in Chapter 3 would be considered. The system is redrawn here as shown in Fig. 5-1. With regard to the problem in hand, it is assumed that the non-linear converter and the sensitive loads are balanced. In what follows, symbols with the subscript “ S ” denote those quantities which are associated with the upstream source, “ L ” for those associated with the sensitive load, “ D ” with the downstream main converter drive and “ C ” with the series compensator. Subscript “ h ” denotes the h^{th} harmonic component and “ I ” that of the fundamental. Voltage and current phasors are denoted with a symbol “ $\rightarrow$ ” on the top of the respective quantities. Their magnitudes (rms) are shown as capital letters while their peak values are denoted with “ $\wedge$ ” on top. Vectors are denoted by bold letters.

Fig. 5-1 A typical isolated power system installed with a SC.

5.2.1 Control of Harmonic Distortions

As defined in Chapter 3, distorted phase voltage $\mathbf{V}_s$ on the upstream source-side of the sensitive load can be expressed as in equation (4.1) for phases a, b and c. Clearly, distorted voltage is undesirable at the sensitive load terminals. The fundamental components of the voltages contained in equation (4.1) are shown in equation (4.2).

$$\mathbf{V}_s = \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \begin{bmatrix} \sum_{n=1}^{\infty} [V_{0n} + \hat{V}_{1n} \sin(n\omega_o t + \varphi_{1n}) + \hat{V}_{2n} \sin(n\omega_o t + \varphi_{2n})] \\ \sum_{n=1}^{\infty} [V_{0n} + \hat{V}_{1n} \sin(n\omega_o t + \varphi_{1n} - 2n\pi/3) + \hat{V}_{2n} \sin(n\omega_o t + \varphi_{2n} + 2n\pi/3)] \\ \sum_{n=1}^{\infty} [V_{0n} + \hat{V}_{1n} \sin(n\omega_o t + \varphi_{1n} + 2n\pi/3) + \hat{V}_{2n} \sin(n\omega_o t + \varphi_{2n} - 2n\pi/3)] \end{bmatrix} \quad (4.1)$$

$$\mathbf{V}_{s1} = \begin{bmatrix} V_{sa1} \\ V_{sb1} \\ V_{sc1} \end{bmatrix} = \begin{bmatrix} \hat{V}_{11} \sin(\omega_o t + \varphi_{11}) \\ \hat{V}_{11} \sin(\omega_o t + \varphi_{11} - 2\pi/3) \\ \hat{V}_{11} \sin(\omega_o t + \varphi_{11} + 2\pi/3) \end{bmatrix} \quad (4.2)$$

The proposed voltage injection method shown in Chapter 3 is to compensate for the difference between $\mathbf{V}_s$ and $\mathbf{V}_{s1}$ described by equations (4.1) and (4.2), respectively. This can be achieved by injecting an ac voltage component in series with $\mathbf{V}_s$ and the desirable injected voltages would have to contain all the harmonic components in equation (4.1). From equations (4.1) and (4.2), therefore

$$\mathbf{V}_s = \mathbf{V}_{s1} + \mathbf{V}_{sh} \quad (4.3)$$

where $\mathbf{V}_{sh}$ contains all the harmonic components in equation (5.1). Hence, from equations (4.1) and (4.2), the injection voltage from the SC would have to be

$$\mathbf{V}_{out} = -\mathbf{V}_{sh} = \mathbf{V}_{s1} - \mathbf{V}_s \quad (4.4)$$

Chapter5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

Thus far, one has only considered the condition that V_S contains harmonic distortions. A voltage sag/swell may appear in V_S and V_{S1} would be less or larger than specified desirable value. Assume the desirable load side fundamental voltage components are

$$\mathbf{V}_{L1} = \begin{bmatrix} V_{La1} \\ V_{Lb1} \\ V_{Lc1} \end{bmatrix} = \begin{bmatrix} \hat{V}_{L1} \sin(\omega_o t + \varphi_{11}) \\ \hat{V}_{L1} \sin(\omega_o t + \varphi_{11} - 2\pi/3) \\ \hat{V}_{L1} \sin(\omega_o t + \varphi_{11} + 2\pi/3) \end{bmatrix} \quad (4.5)$$

Ideally, the injected voltage from the SC would then have to be

$$\mathbf{V}_{out} = \mathbf{V}_{L1} - \mathbf{V}_S = \mathbf{V}_{L1} - \mathbf{V}_{S1} - \mathbf{V}_{Sh} \quad (4.6)$$

Extract the fundamental component of $\mathbf{V}_{out}$ and denote it by the phasor $\vec{V}_1$, one obtains

$$\vec{V}_1 = \vec{V}_{L1} - \vec{V}_{S1} \quad (4.7)$$

In this way, the equivalent circuit describing the sensitive load branch can then be decomposed into the fundamental frequency component and harmonic component circuits, as shown in Fig. 5-2 (a) and (b) respectively.

Fig. 5-2 Equivalent circuits of the sensitive load-SC branch for: (a) fundamental component and (b) h^{th} harmonic component.

Under such an ideal compensation situation, there is no harmonic component in the sensitive load current I_L and thus, no harmonic energy exchange between the SC and the external system. Energy exchange is only due to the fundamental frequency components

Chapter 5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

of V_{out} and I_L .

In practice and as described in Chapter 3, however, the SC has a finite bandwidth. A phase lag would exist between V_{sh} and the actual injected voltage (V'_{sh}) from the SC. The lag results in voltage pulses appearing at the terminals of the sensitive load. As the RC sensitive load impedance decreases with frequency, the voltage pulses will cause large harmonic current distortions to appear in I_L . A practical method to limit the THD in I_L to a pre-specified level has been proposed in Chapter 3. It involves a new strategy to control V_{out} and the use of a series filter. Hence in practice, there will be harmonic components in I_L as shown in Fig. 3-14. As V'_{sh} contains harmonic components, harmonic power flow can exist between the SC and the external system.

5.2.2 Power Flow Control through SC

Having presented the harmonic compensation method, power flow control through the SC will be investigated next. For the convenience of analysis, a single-phase equivalent system (phase “a”) is used to describe the three-phase system shown in Fig. 5-1. Let $\vec{I}_{L1}$, the fundamental frequency component of the sensitive load current, be taken as the reference phasor.

In general, the instantaneous SC output power is given by

$$p_C(t) = V_{out}(t)I_L(t) \quad (4.8)$$

Suppose the upstream load change has resulted in momentary sags/swells in $\vec{V}_{s1}$. The aim of the compensation is to ensure the magnitude of $\vec{V}_{L1}$ is maintained constant. If one were to introduce a phase-shift α into $\vec{V}_{L1}$, one would obtain a new injection voltage from that described by equation (4.6), i.e.

$$V_{out}(t) = \hat{V}_{L1} \sin(\omega_o t + \varphi_{11} + \alpha) - [V_{s1}(t) + V'_{sh}(t)] \quad (4.9)$$

Chapter5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

In this way,

$$p_C(t) = V_{out}(t)I_L(t) = [\hat{V}_{L1} \sin(\omega_o t + \varphi_{11} + \alpha) - \hat{V}_{S1} \sin(\omega_o t + \varphi_{11}) - \sum_{h=2}^{\infty} \hat{V}'_{Sh} \sin(h\omega_o t + \varphi'_h)] [\hat{I}_{L1} \sin(\omega_o t) + \sum_{h=2}^{\infty} \hat{I}_{Lh} \sin(h\omega_o t + \sigma_h)] \quad (4.10)$$

where h is the harmonic order, $\hat{V}'_{Sh}$ and φ'_h are the peak value and phase of the harmonic component of the actual injection voltage; $\hat{I}_{Lh}$ and σ_h are the peak value and phase of the h^{th} harmonic component in I_L .

The cycle-average value of $p_C(t)$ is seen to contain two terms: a contribution each from the fundamental frequency component and the harmonics:

$$\left. \begin{aligned} P_C &= P_{C1} + P_{Ch} \\ P_{C1} &= \frac{1}{2} \hat{V}_{L1} \hat{I}_{L1} \cos(\varphi_{11} + \alpha) - \frac{1}{2} \hat{V}_{S1} \hat{I}_{L1} \cos(\varphi_{11}) \\ P_{Ch} &= -\frac{1}{2} \sum_{h=2}^{\infty} \hat{V}'_{Sh} \hat{I}_{Lh} \cos(\theta_h) \quad \text{where } \theta_h = \varphi'_h - \sigma_h \end{aligned} \right\} \quad (4.11)$$

P_{C1} corresponds to the power flow of the fundamental frequency component. It is controllable through the introduced phase shift α in $\vec{V}_{L1}$. Thus P_C can be regulated through P_{C1} via the adjustment in α . P_{Ch} corresponds to the power flow of the harmonic components. In regulating the power flow, P_{Ch} is assumed constant over the time interval when α is being adjusted. This is a reasonable assumption because the adjustment in α can be accomplished in a much shorter time, as the rate by which the electro-mechanical drive-load and therefore the harmonic level can vary is slow in comparison.

Also, as the only significant source of energy storage in the SC is the ESS, $P_C > 0$ would indicate an export of power from the SC to the external system. It will cause a decrease in the voltage V_{DC} across the ESS. Conversely V_{DC} will begin to rise if the SC starts to import P_C from the external system. Variation of V_{DC} will affect the compensation

Chapter 5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

capability of the SC and excessive voltage rise will damage the ESS. Hence V_{DC} has to be controlled within acceptable range, i.e. P_c has to be regulated.

Fig. 5-3 Sensitive load-SC branch: (a) Equivalent circuit describing harmonic compensation in practice; (b) Phasor diagram for h^{th} harmonic order.

Fig. 5-3(b) shows the phasor diagram of h^{th} harmonic order compensation by the SC. For perfect harmonic voltage cancellation, the ideal voltage injected by the SC is $-\vec{V}_{Sh}$ but due to SC bandwidth limitation described earlier, the actual voltage injection is $-\vec{V}'_{Sh}$. Although the phase difference between $-\vec{V}_{Sh}$ and $-\vec{V}'_{Sh}$ would depend on the SC controller design, this phase difference is expected to be small in practice in order for the cancellation to be reasonably effective. Since the sensitive load is assumed to be resistive-capacitive, the h^{th} harmonic voltage component across the load ($\vec{V}_{Lh}$) lags the harmonic current $\vec{I}_{Lh}$. The direction of power flow could be determined by observing the polarity of the voltage and the reference direction of the current. With reference to Fig 5.3, one can compute the harmonic power using the equation $P_{Ch} = \sum_{h=2}^{\infty} \text{Re}\{-\vec{V}'_{Sh} \vec{I}_{Lh}^*\}$. From Fig. 5.3 (a) and by examining the phasor diagram Fig 5.3(b), it can be readily established that if the phase angle between $-\vec{V}'_{Sh}$ and $\vec{I}_{Lh}$ is larger than 90 degrees, then $P_{Ch} < 0$. This means the SC will absorb power from the external system, based on the voltage polarity and current direction shown. The extent of the power import will depend on the injection voltage, which in terms depends on the main drive load operating conditions. P_{Ch} will be examined in greater details next.

5.2.3 Harmonic Power Flows

In Fig. 5-4, the main load is shown as a DC drive system. The DC motor, represented by the equivalent RL circuit, is assumed to be fed by a six-pulse controlled converter. The firing angle δ_1 of the converter determines the average value (V_d) of the output voltage. The converter output current can be controlled via a PI regulator which changes the firing angle δ_1 [48]. In this way, the effect of a load change can be readily simulated by altering the reference current I_{ref} .

The main converter load is the dominant harmonic source in the power system due to its much larger capacity compared to the SC and sensitive load. The SC is assumed to be “ideal” in that whatever harmonics generated by the VSI are effectively dealt with by its LC filter. The SC is a harmonic “sink”. In this way, the harmonic power P_{Dh} produced by the nonlinear main drive load is dissipated in the upstream source impedance and absorbed by the sensitive load. The harmonic power flows to the upstream source (P_{Sh}) and into the sensitive load (P_{Lh}) are as shown in Fig. 5-4.

Fig. 5-4 Harmonic power flow in the isolated system: h^{th} harmonic component.

Chapter5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

To assess the value of P_{Dh} , the harmonic contents of $v_s(t)$ and $i_D(t)$ have to be known. In order to do so, the following assumptions are made: upstream source consists of balanced sinusoidal EMFs of constant voltage with equal inductances and its phase “a” terminal voltage is of the form $v_{s1}(t) = \hat{V}_m \sin \omega_o t$; the DC load current I_d is assumed to be constant and ripple-free.

The firing angle δ_1 changes as load condition varies and in general, δ_1 and the overlap angle of the converter determine the exact waveform of $v_s(t)$ [90]. Harmonic components of $v_s(t)$ and $i_D(t)$ could be obtained through Fourier analysis and P_{Dh} can be evaluated. Furthermore, once $v_s(t)$ has been determined, P_{Sh} can also be determined as the source impedance Z_S is assumed known. The balance of the harmonic power is diverted to the SC branch. Part of this harmonic power (P_{Lh}) will be absorbed by the sensitive load. Once P_{Dh} , P_{Sh} and P_{Lh} are obtained, the harmonic power imported by the SC, P_{Ch} could be obtained. Numerical examples will now be used to illustrate how the harmonic power flows in the network can be assessed.

Example 1:

Suppose the ratio between the VA capacity of the main drive load and that of the sensitive load is k . The upstream source fault level is “ m ” times that of the main drive load capacity. The X/R ratio of Z_S at the fundamental frequency is q , i.e. $X_{s1}/R_s = q$.

Assume the drive-load converter operates at a delay angle $\delta_1 = 10^\circ$ and an overlap angle $\delta_2 = 20^\circ$. The resulting waveforms of $v_s(t)$ and $i_D(t)$ can be derived using the expressions given in [89]. As shown in Appendix A, Fourier analysis of $v_s(t)$ and $i_D(t)$ yields the following characteristics harmonic components

$$v_{sh}(t) = \hat{V}_m [0.28 \sin(5\omega_o t + 70^\circ) + 0.16 \sin(7\omega_o t + 75^\circ) + 0.1 \sin(11\omega_o t + 56^\circ) + \dots] \quad (4.12)$$

$$i_{Dh}(t) = 3.46 \times \frac{I_d}{\pi} \left[\frac{1}{5} \sin(5\omega_o t - 50^\circ) + \frac{1}{7} \sin(7\omega_o t + 110^\circ) + \frac{1}{11} \sin(11\omega_o t - 110^\circ) + \dots \right] \quad (4.13)$$

Chapter5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

From (4.12) and (4.13), the harmonic power P_{Dh} (up to the 11th harmonic) generated by the main drive load can be obtained

$$P_{Dh} = \frac{3}{2} \sum_{h=5}^{11} \hat{V}_{hm} \hat{I}_{hm} \cos(\varphi_k - \sigma_k) = -0.032 \hat{V}_m I_d$$

The average DC voltage can be calculated using the results of [89]:

$$V_d = 1.65 \hat{V}_m (\cos \delta_1 + \cos(\delta_1 + \delta_2)) / 2 = 1.53 \hat{V}_m$$

and the power of the fundamental frequency component of the main drive load is

$$P_{D1} = V_d I_d = 1.53 \hat{V}_m I_d$$

The converter is assumed lossless. Using P_{D1} and $\hat{V}_m$ as base values, the harmonic power exported by the main load is

$$P_{Dh} = -0.02 \text{ p.u.}$$

As the system short-circuit ratio is m and $X_{S1}/R = q$, $\vec{I}_{Sh}$ can be calculated. Apply

$$P_{Sh} = \sum_{h=5}^{11} \text{Re}\{\vec{V}_{SL} \vec{I}_{Sh}^*\} \text{ and from [90], it can be readily shown that}$$

$$P_{Sh} = -\frac{0.0014m}{q^2} \text{ p.u.}$$

Suppose the THD of the voltage at the terminal of the sensitive load is to be limited to (say) 3%. As

$$THD_V = \frac{1}{V_1} \sqrt{\sum_{h=2}^{\infty} V_h^2}$$

Then the power in pu can be expressed in

Chapter5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

$$P = \frac{\frac{1}{2R} \sum_{h=2} V_h^2}{\frac{1}{2R} V_1^2} = THD_V^2$$

Thus, P_{Lh} can be obtained using the result [91]

$$P_{Lh} = \frac{(THD_V)^2}{k} \approx \frac{0.001}{k} p.u.$$

Whence the harmonic power imported by the SC is estimated to be

$$P_{Ch} = P_{Sh} - P_{Dh} - P_{Lh} = (0.02 - \frac{0.0014m}{q^2} - \frac{0.001}{k}) p.u.$$

As an illustration, for typical values of $m=10$, $q=5$, and $k=10$, the last expression shows that $P_{Ch} \approx 0.019$ p.u. Since it is assumed that the sensitive load capacity is 1/10 that of the main drive-load, therefore P_{Ch} corresponds to some 19% of the sensitive load capacity.

Example 2:

If the converter operates at a delay angle of 30° and an overlap angle 25° instead, Fourier analysis of $v_s(t)$ and $i_D(t)$ yields

$$v_{Sh}(t) = \hat{V}_m [0.18 \sin(5\omega_o t - 140^\circ) + 0.24 \sin(7\omega_o t - 129^\circ) + 0.08 \sin(11\omega_o t - 148^\circ) + \dots] \quad (4.14)$$

$$i_{Dh}(t) = 3.46 \times \frac{I_d}{\pi} \left[\frac{1}{5} \sin(5\omega_o t + 30^\circ) + \frac{1}{7} \sin(7\omega_o t - 30^\circ) + \frac{1}{11} \sin(11\omega_o t + 30^\circ) + \dots \right] \quad (4.15)$$

Then following the same procedure as shown earlier, one can show that:

$$P_{Dh} = -0.08 \hat{V}_m I_d,$$

$$V_d = 1.19 \hat{V}_m,$$

$$P_{D1} = V_d I_d = 1.19 \hat{V}_m I_d,$$

Chapter5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

$$P_{Dh} = -0.067 \text{ p.u.},$$

$$P_{Sh} = -\frac{0.0006m}{q^2} \text{ p.u.},$$

$$P_{Lh} \approx \frac{0.001}{k} \text{ p.u.}.$$

The harmonic power imported by the SC is

$$P_{Ch} = P_{Sh} - P_{Dh} - P_{Lh} = (0.067 - \frac{0.0006m}{q^2} - \frac{0.001}{k}) \text{ p.u.}$$

In this case, P_{Ch} is seen to be equivalent to some 67% of the sensitive load capacity, if the same numerical values of m , q and k used earlier were again assumed. This is a substantial amount of absorbed power, in so far as the sensitive load is concerned.

The above examples show that the operating states of the converter will affect the harmonic power exported by the main load which, in terms, determines the amount of the harmonic power absorbed by the SC. The dominant factor governing P_{Ch} appears to be P_{Dh} , i.e., a significant part of P_{Dh} will be absorbed by the SC. For a range of the converter operating conditions, it is possible to obtain expressions for P_{Ch} , such as illustrated earlier.

5.3 Voltage Restoration

Having considered harmonic power flows in the isolated power system, voltage restoration will be examined next. As stated earlier, voltage control of the ESS is necessary to ensure the proper operation of the SC and to protect the device. Thus it is desirable to regulate the power transfer between the SC and the external system so that V_{DC} across the ESS of the SC can be maintained. Once this is achieved, the SC will be able to exercise network voltage control, in a manner described in [32, 33]. The SC will assume this role of voltage control until such time when the excitation system of the

Chapter5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

upstream generator becomes effective in forcing the generator to share the voltage regulation duty. However, if the excitation system is a slow-acting electromechanical type, the sensitive load would have to rely very much on the SC to achieve a constant V_L . It is therefore necessary to examine the extent by which the SC can achieve such control. Furthermore, in terms of voltage quality, it is the fundamental component of V_L which is of the greatest importance. Hence in what follows, the focus is on maintaining this voltage component, denoted as $\vec{V}_{L1}$ in Fig. 5-5.

The condition of zero power transfer between the SC and the external system is examined first. From equation (4.11), this means that $P_C = P_{C1} + P_{Ch} = 0$, i.e. when

$$P_{C1} = -P_{Ch} \quad (4.16)$$

As shown in Section 5.2, it is concluded that the SC absorbs harmonic power from the external system, i.e. $P_{Ch} < 0$. Thus from (4.16), at zero power transfer, the SC should export power of the fundamental frequency component equal to an amount P_{Ch} in order to balance the imported harmonic power.

Next, define an equivalent fundamental frequency component voltage V_P of the SC injected voltage V_{out} such that

$$V_P I_{L1} = P_{Ch} \quad (4.17)$$

The last expression means that when the projection of the fundamental frequency component of V_{out} onto $\vec{I}_{L1}$ (shown as $\vec{V}_1$ in Fig. 5-5) is V_P , the condition for zero power transfer is reached. As shown in previous section, for given power system operating conditions, $\vec{I}_{L1}$ and P_{Ch} are known quantities. Hence from equation (4.17), one would be able to obtain V_P readily.

5.3.1 Voltage Swell

When the drive load varies and causes a voltage swell, V_{s1} is higher than its nominal value, as shown in Fig. 5-5 (a), where $\vec{I}_{L1}$ is shown as the reference phasor. Since V_{L1} denotes the desired voltage magnitude at the sensitive load terminals, the aim is to maintain it constant through the action of the SC. Assume the sensitive load is of constant power factor ($\cos \theta$) at the fundamental frequency. Therefore from equation (4.11), $\theta = \phi_{11} + \alpha$ i.e. the phase angle between $\vec{I}_{L1}$ and $\vec{V}_{L1}$ is constant at θ . α is the phase shift described in Section 5.2. From equation (4.7), the SC injected voltage is $\vec{V}_1 = \vec{V}_{L1} - \vec{V}_{s1}$ and since $P_{C1} = \text{Re}\{\vec{V}_1 \vec{I}_{L1}^*\}$, P_{C1} can be rewritten as:

$$P_{C1} = \frac{1}{2} [\hat{V}_{L1} \cos \theta - \hat{V}_{s1} \cos(\theta - \alpha)] \cdot \hat{I}_{L1} \quad (4.18)$$

(b)

Fig. 5-5 Phasor diagram showing voltage restoration during (a) a voltage swell and (b) a voltage sag: fundamental frequency component.

The situation depicting $\vec{V}_{L1}$ and $\vec{V}_{S1}$ by the solid lines in Fig. 5-5 (a) shows that P_{C1} is negative. This corresponds to the situation when the SC imports P_{C1} from the external system. By continuously adjusting α and shifting $\vec{V}_{S1}$ in the clockwise direction, P_{C1} will become less and less negative and it eventually will become positive, i.e. the SC will then export P_{C1} to the external system. The condition shown by the dotted lines in Fig. 5-5 (a) is when the projection of $\vec{V}_1$ onto $\vec{I}_{L1}$ is equal to the value of V_P given by equation (4.17) precisely. Hence, at this point, the SC output power contributed by the fundamental frequency component voltage and current is $V_P I_{L1} = P_{C1} > 0$. From equation (4.17), $P_{C1} + P_{Ch} = 0$. It then arrives at the zero power transfer condition between the SC and the external system. Mathematically, this can be expressed by the condition when

$$V_{L1} \cos \theta - V_{S1} \cos(\theta - \alpha) = V_P \quad (4.19)$$

Whence at this zero power transfer condition, the phase angle between $\vec{V}_{S1}$ and $\vec{V}_{L1}$ is α_0 where

Chapter 5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

$$\alpha_0 = \theta - \arccos\left(\frac{\cos\theta - \beta}{\gamma}\right) \quad (4.20)$$

with

$$\gamma \triangleq \frac{V_{S1}}{V_{L1}}, \quad \beta \triangleq \frac{V_P}{V_{L1}} \quad (4.21)$$

For a voltage swell, α_0 is negative, i.e. $\vec{V}_{S1}$ lags $\vec{V}_{L1}$ at zero power transfer. At this instance, the phase angle of $\vec{V}_{S1}$ is $\arccos[(\cos\theta - \beta)/\gamma]$.

Furthermore, one concludes that the SC will import power ($P_C = P_{C1} + P_{Ch} < 0$) when $\alpha < \alpha_0$, i.e. $\vec{V}_{S1}$ is shifted in the counter-clockwise direction from the condition $\alpha = \alpha_0$. Conversely, if α were adjusted in the clockwise direction, and as the projected component of $\vec{V}_1$ onto $\vec{I}_{L1}$ is larger than V_P , then $P_C = P_{C1} + P_{Ch} > 0$. The SC would then export power to the external system

The above analysis suggests a means to regulate the ESS voltage V_{DC} . If V_{DC} decreases below a set value, it means that the SC is exporting total power P_C to the external system. One can then reverse the fall in V_{DC} by adjusting the VSI firing angle to effect a counter-clockwise phase shift in $\vec{V}_{S1}$ such that $\alpha < \alpha_0$, in order to force a net import of P_C and vice-verse. In this way, V_{DC} can be regulated through the control of α . Since the power factor angle θ , β and γ (as defined by (4.21)) can be readily determined on-line, the calculation for α_0 can be accomplished as part of the SC real-time control system. The phase-shift control strategy to regulate P_C can be realized.

It is interesting to note that if P_{Ch} increases due to drive-load changes, V_P and α_0 will also increase. This means that $|\vec{V}_1|$ also increases. Hence, the SC voltage rating has to be adequate in order to cater for this injection method.

Chapter 5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

5.3.2 Voltage Sag

The above analysis can be extended to deal with the event of voltage sag, i.e. $V_{S1} < V_{L1}$. Fig. 5-5(b) shows a general phasor diagram during voltage sag. By similar reasoning as shown for voltage swell, $P_C < 0$ when

$$\alpha > \alpha_0 = \theta - \arccos\left(\frac{\cos \theta - \beta}{\gamma}\right) \quad (4.22)$$

α_0 is positive. Phase shifting of $\vec{V}_{S1}$ can lead to zero power transfer when $\alpha = \alpha_0$. This is shown by $\vec{V}_{S1}$ and $\vec{V}_1$ in dotted lines in the figure. From this condition of zero power transfer, if one were to adjust $\vec{V}_{S1}$ to shift it in the counter-clockwise direction, $P_C < 0$ when $\vec{V}_{S1}$ leads $\vec{V}_{L1}$ by an angle α where $\alpha > \alpha_0$. The SC then imports power from the external system. Conversely, adjusting $\vec{V}_{S1}$ in the clockwise direction can lead to $\alpha < \alpha_0$. Whence $P_C > 0$, the SC will export real power to the external system. An example of such a condition is shown by $\vec{V}_{S1}$ and $\vec{V}_1$ by the solid lines shown in Fig. 5-5 (b). Hence if it is noted that V_{DC} is above a set value, it will then be necessary to introduce a phase shift α in $\vec{V}_{S1}$ such that $\alpha < \alpha_0$. The SC then exports real power to the external system. The ESS voltage should decrease. Conversely, if V_{DC} is below the set value, $\vec{V}_{S1}$ phase should be adjusted to meet the condition $\alpha > \alpha_0$.

If one were to exclude harmonic power from the above analysis, such as in [17, 32, 33], Fig 5-6(a) shows the condition in which the severity of the sag is such that $V_{S1}/V_{L1} = \gamma < \cos \theta$. It can be seen that by shifting $\vec{V}_{S1}$ until it aligns with $\vec{I}_{L1}$, P_{C1} is exported from the ESS to the external system at the minimum value. This is the condition indicated by $\vec{V}_1$ assuming the position of the dotted line in the figure. The minimum exported power is

$$P_{C1\min} = V_{L1} \cdot I_{L1} (\cos \theta - \gamma) \quad (4.23)$$

Chapter5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

(a)

(b)

Fig. 5-6 Phasor diagram of voltage sag condition when $V_{s1}/V_{L1} = \gamma < \cos \theta$: (a) without harmonic power taken into consideration, (b) with harmonic power taken into consideration.

In the event if V_{DC} is already lower than its desirable set value, one would need to adjust α in such a way that P_{C1} can be absorbed from the external system. From the phasor diagram, however, it shows that it is impossible to effect such a condition for power

Chapter 5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

absorption. At best, with $\vec{V}_{S1}$ adjusted to be in-phase with $\vec{I}_{L1}$, the SC exports P_{C1} at the minimum value given by (4.23). It can only minimize the rate of the decrease of V_{DC} .

With the harmonic power flow included in the compensation process, the situation is improved somewhat. Fig 5-6(b) shows the most severe sag that can be compensated for: when $\vec{V}_{S1}$ is shifted to be in-phase with $\vec{I}_{L1}$, and the harmonic power P_{Ch} absorbed by the SC is given by (4.17), i.e. $P_{Ch} = -V_P I_{L1}$, with V_P equal to that shown in the figure. In this way, zero power exchange between the SC and the external system has been achieved. From Fig 5.6(b), it is seen that

$$V_{S1} + V_P = V_{L1} \cos \theta \quad (4.24)$$

Hence the most severe voltage sag that the SC can compensate while maintaining zero power transfer is

$$\gamma_{\min} = \cos \theta - \beta \quad (4.25)$$

where as defined by (4.21), $\gamma = V_{S1}/V_{L1}$, $\beta = V_P/V_{L1}$. Hence by adjusting α and taking advantage of the presence of the harmonic power P_{Ch} , the proposed compensation strategy compares favorably with that shown in Fig. 5-6(a) where the most severe sag that can be compensated for is $\cos \theta$, if V_{DC} is to be maintained constant. The proposed method improves the ride-through capability of the sensitive load by a margin β , through the SC absorbing the harmonic power generated by the main load and converting it into real power for supporting the sensitive load voltage. From (4.25), clearly the most onerous ride through condition is when the sensitive load power factor is unity. Also, the following observation can also be arrived at:

(a) Since $\beta = V_P/V_{L1}$, β decreases with V_P . However, from equation (4.17), it is seen that V_P decreases with an increase in I_{L1} for a given P_{Ch} . Hence the margin β would be at the minimum when I_{L1} is at its maximum value, i.e. when the sensitive load is at full load;

Chapter5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

(b) P_{Ch} depends most significantly on P_{Dh} which in terms bears a complex relationship to the operating state of the motor-drive. While it is difficult to generalize this relationship, it is clear that when the motor-load is at full load, full-conduction in the rectifier occurs and harmonic distortions are expected to be at the minimum. Hence P_{Dh} , and correspondingly P_{Ch} , will be at the minimum. Again from equation (4.17), V_p and therefore β will be at the minimum.

Based on the above observation, it can therefore be concluded that the most onerous sensitive-load ride through condition would be when the load is at full load, unity power factor, while P_{Dh} is at the minimum or when the motor-load is operating at rated power.

Also from equation (4.25), one notices that the most severe voltage-sag that the SC can provide load ride-through is when $\gamma = \gamma_{\min}$. For small β , $\gamma_{\min}$ is close to the load power factor. From Fig. 5-6(b), the maximum injection voltage is approximately equal to $V_{Li} \sin \theta$. Hence, the SC must be rated to be at least $\sin \theta$ times of that of the sensitive load.

Although not shown in the above analysis, similar conclusions can also be reached if the power factor of the sensitive load is lagging.

Under the condition when a sag/swell occurs but without any harmonic contents, the imported harmonic power of the SC will be zero. The same phase-shift compensation strategy can still be used to achieve zero power transfer. However, as $P_{Ch}=0$ and thus $\beta=0$, the phase shift angle at the zero power transfer condition will be changed accordingly. The method described in for example [89] can be used instead. Also, from (5.25), it can be seen that $\gamma_{\min}$ will be the load power factor. It shows that the ability of the SC to mitigate sag reduces.

When an isolated power system is supplied by a generation vary in nature, e.g. a wind farm, fluctuating generation would also cause voltage changes. The proposed technique for SC control can still be used.

5.4 Illustrative Examples

The example shown on Fig. 5-4 may now be used to verify the effectiveness of the SC in enhancing the voltage quality of the power system. The upstream generator is represented as a 220-V voltage source, with its AVR action ignored. The source is assumed to have a reactance value $X_{s1} = 0.05$ p.u. on the generator base, and $q = 20$. The main load converter is assumed to be a six-pulse controlled rectifier. The DC motor, as shown in Fig. 5-4, has $R_a = 2 \Omega$ and $L_a = 25$ mH. The rating of the DC load is 2 kW and 2 kVA is chosen as the base value for the system. The current of the motor is controlled and the load change is simulated by changing I_{ref} of the motor. The capacity of the sensitive load is assumed to be 0.2 kVA and its power factor at the fundamental frequency is 0.75 leading. The sensitive load level is assumed to be at full load in these examples. The SC was modeled as a PWM inverter and its detail model is given in Chapter 3. A capacitor is used as the ESS. The simulations were accomplished using MATLAB.

The voltage at the sensitive load terminals is shown in Fig. 5-7 when a load change occurs but without the SC in service. Before the load change, the motor-drive is at 0.5p.u. loading and it can be shown that V_L has a THD level of 30%.

Fig. 5-7 Terminal voltage (V_L) of the sensitive load before and after a +25% main load change - without the SC.

Chapter 5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

Fig. 5-8 shows the corresponding waveforms when the SC is in service. With harmonics compensation by the SC, the sensitive load is protected against the harmonic distortion and the THD of the voltage has been significantly reduced to 3%.

Fig. 5-8 Terminal voltage (V_L) of the sensitive load before and after a 25% main load increase: with SC.

Fig. 5-9 Harmonic power flows in the isolated power system prior to and after the 25% main load increase.

The harmonic power flows (expressed on the base of the sensitive load capacity of 0.2 kVA) in the isolated power system are shown in Fig. 5-9. Prior to a +25% load change, P_{Ch} imported by the SC during compensation is about 0.13 p.u. On 0.2 kVA base, $I_{L1} = 1$ p.u. and from (4.17), $V_p = 0.13$ p.u. Thus $\beta = 0.13$ p.u. According to (4.25), the sag ride-through limit $\gamma_{\min}$ is about 0.62 p.u. The 25% load change has resulted in a 70% voltage

Chapter 5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

sag, as shown in Fig. 5-7, when the SC is not in service. The load change has caused P_{Ch} to decrease to about 0.1 p.u., which means that β also decreases correspondingly. $\gamma_{\min}$ is now about 0.65 p.u. but it is still less than the load power factor. Hence the SC can still assist the load in riding through the sag as shown in Fig. 5-8. Fig. 5-10 shows the ESS voltage during the voltage restoration. V_{DC} decreases marginally and is restored in some 10 cycles or so in the face of the voltage sag. Fig. 5-9 shows that as the load changes, P_{Dh} also varies because the firing angle is adjusted. This can be seen in Fig. 5-11.

Fig. 5-10 Terminal voltage of ESS (V_{DC}) following load change: 70% voltage sag.

Fig. 5-11 Firing angle of rectifier during main load changes due to the 70% voltage sag.

From the above results, the VA capacity of the SC has been evaluated using Fig. 5-5(b) and is estimated to be some 36% of the sensitive load rated capacity. The corresponding $\alpha_0 = 13.7^\circ$.

Chapter 5 An Improved Compensation Strategy to Mitigate Sags/Swells under Distorted Voltage Conditions

Fig. 5-12 shows the waveform of V_L during a 50% voltage sag when the DC motor-load is increased by 40%. The sensitive load is seen restored through the voltage sag. However, the load increase is so large that it has resulted in V_{L1} to be below the limit predicted by (4.25). V_L is sustained only through the continuous export of P_C from the ESS. Hence, the voltage of the ESS cannot be maintained as is shown in Fig. 5-13. Clearly this is not a sustainable operation as the ESS energy will eventually be depleted and the SC will no longer be effective.

Fig. 5-12 Terminal voltage (V_L) of the sensitive load: with SC for a 40% load increase.

Fig. 5-13 Terminal voltage of ESS for the 40% load increase.

Similar studies have also been carried out under voltage swell conditions to confirm that the SC can indeed provide satisfactory ride-through performance for the power system.

5.5 Conclusions

In Chapter 3, a method to control the injection voltage of the SC so that it can mitigate the effects of the harmonics has been proposed. In this Chapter, the SC is designed to maintain the fundamental frequency component of the terminal voltage of protected sensitive load. In the process of harmonic voltage compensation, it is shown that power exchange exists between the SC and the external network. Based on the analysis of the harmonic real power flows in the power system, it is seen that the SC would import harmonic real power from the external system. The new SC control strategy is then proposed which involves the phase adjustment of the fundamental frequency component of the load terminal voltage. Through the analysis on the energy exchange, it is shown that the load ride through capability during voltage sag can be improved with the support of the harmonic real power absorbed by the SC. The capacity of the SC required is modest and is approximately equal to $\sin\theta$ times of the protected load capacity. Therefore makes it a viable device for such an application. Simulations have confirmed the effectiveness of the proposed method, as it is applied on the SC to achieve improved quality of supply in the power system.

Chapter 6 Control of Series Compensator under Downstream Fault Condition

6.1 Introduction

In the previous Chapters, power quality enhancement in an isolated power system through series compensator has been investigated. The compensator is designed to mitigate voltage perturbations which originate from the upstream network. Since in most cases the isolated power system is radial in structure, the SC is incorporated to protect sensitive load in a manner as shown in Fig. 6-1. In the figure, $\vec{V}_s$ and X_s denote the Thevenin equivalent source voltage phasor and the Thevenin equivalent reactance of the upstream system. X_L is the effective distribution system series reactance between the SC and the downstream protected load. The voltage phasor on the load-side of SC is denoted as $\vec{V}_L$. Also shown are a number of parallel feeders connected to the Point of Common Coupling (PCC) bus at which the voltage is denoted as $\vec{V}_P$.

Fig. 6-1 A typical distribution network incorporating a SC.

Chapter 6 Control of Series Compensator under Downstream Fault Condition

As discussed earlier, the primary function of the SC is to mitigate against voltage sags/swells or distortions due to operation of nonlinear loads connected to the parallel feeders. It achieves this by injecting a voltage $\vec{V}_{sc}$ in series with $\vec{V}_L$. The SC is online at all time so that there is minimal delay in providing the voltage support as and when it is needed. One common feature of the previous chapters is that the focus is on upstream disturbances or faults. Unfortunately faults do occur on the distribution system downstream of the SC. Should such a fault occur any where on the feeder connecting the SC and the protected load, and as the SC is series connected to the faulted feeder, a large current will be induced through the injection transformer and into the VSI. Without proper measure, this could damage the compensator.

To isolate the downstream fault, one can of course rely on the circuit breakers (shown as CB in Fig. 6-1) installed upstream of the SC. Depending on the design of the protection system and the exact location/nature of the fault, the fault clearing action may typically take ten or more cycles. However, fault of such duration is considered damaging to the power switching devices within the VSI. Furthermore, for the other loads also connected to the PCC, the voltage sag event can be harmful as it can cause equipment on these parallel feeders to fail, mal-operate or shut down.

To protect against the large induced currents from exceeding the converter rating, a SC may make use of a bypass scheme to protect the power electronics switching devices. Protection can be provided by a solid-state SCR thyristor shorting switch that closes across the secondary terminals of the injection transformer when a downstream fault occurs [33]. While the bypass switch is effective in protecting the SC, it cannot mitigate the impact of the fault on the parallel loads. Hence, the scheme does not completely solve the problem.

Having considered the above, it is clear that an alternative method to limit the fault current is most desirable. This chapter examines such a method to achieve the fault current limiting function through the control of the injection voltage, $\vec{V}_{sc}$. As reported in the literature, existing fault current limiter (FCL) can be broadly categorized into two types: non-superconducting [92-94] and superconducting types [95, 96]. The underlying

Chapter 6 Control of Series Compensator under Downstream Fault Condition

operating principle of these limiters is to effectively insert a series reactance between source and fault location during fault. These FCL could only be used to limit fault current and to mitigate the impacts of the voltage sag due to a downstream fault on upstream equipment. Unlike the SC device considered in this chapter, however, these FCL are not capable of maintaining downstream load voltages in the event of an upstream fault.

It must be emphasized that the role of the SC under such a downstream fault condition is to limit the fault current until such time when the protection system upstream of the SC operates. The SC is not intended to replace the protection system in that the compensator only provides a short-term measure to limit the fault current. To this extent, the principle of operation of such a FCL, its control method and a dual-function SC will be described. The effectiveness of the proposed scheme is illustrated through simulation examples.

Unlike Chapters 3 and 5, harmonics are not considered because it is more important and urgent to control current than to keep THD within limit. The contents of part of this chapter also appear in [97].

6.2 Principle of Series Compensation

6.2.1 Voltage Restoration

As the proposed SC control scheme also involves voltage restoration, a review of the principle when the SC is used to compensate for upstream voltage sag will be given first. To facilitate discussion and with reference to Fig. 6-1, it is assumed that the series reactance of the injection transformer is negligible and the protected load is of constant power factor. Furthermore, non-linearities existing in the VSI have been ignored and the transmission-distribution network has been assumed lossless. The last assumption is reasonable for most of overhead transmission networks are predominantly reactive. On the other hand, overhead distribution line series impedances may have appreciable resistive parts. In which case, the analysis to follow can be readily modified without any loss of generality.

Chapter 6 Control of Series Compensator under Downstream Fault Condition

Prior to the on-set of any fault disturbance, the SC is inactive. Under this condition, the load-side voltage phasor $\vec{V}_L$ is given by

$$\vec{V}_L = \vec{V}_S - jX_S \vec{I}_L \quad (5.1)$$

where $\vec{I}_L$ is the line current under normal condition.

If an upstream fault occurs, the voltage sag event could be modeled as a change in the source voltage to $\vec{V}_{sag}$, as shown in Fig. 6-2. Without series voltage compensation, the circuit equation becomes

$$\vec{V}_{Pf} = \vec{V}_L' = \vec{V}_{sag} - jX_S \vec{I}_L' \quad (5.2)$$

where $\vec{I}_L'$, $\vec{V}_{Pf}$ and $\vec{V}_L'$ are the standing line current, PCC and load-side voltages respectively during sag.

Fig. 6-2 Network model under an upstream fault condition.

To protect the load against this voltage sag, the SC will inject a voltage $\vec{V}_{SC}$ to restore the load-side voltage to its pre-fault level $|\vec{V}_L|$. In Fig. 6-2, the SC is represented by a voltage source. Under this condition, once the load-side voltage has been completely restored, one can obtain

$$\vec{V}_L = \vec{V}_{sag} - jX_S \vec{I}_L + \vec{V}_{SC} \quad (5.3)$$

The techniques described in [32, 33] allow the determination of $\vec{V}_{SC}$ so that dynamic restoration of $\vec{V}_L$ can be realized. For example, the method in [33] uses the pre-fault PCC voltage, $\vec{V}_p$ as reference. $\vec{V}_p$ is readily measurable, its magnitude and phase can be logged

Chapter 6 Control of Series Compensator under Downstream Fault Condition

using the phase lock loop technique. $\vec{V}_L$ is set equal to $\vec{V}_P$ in equation (5.3). $\vec{V}_{sag} - jX_S\vec{I}_L$ is the voltage on the source-side of the SC. It can be measured directly on the network. Therefore the injection voltage $\vec{V}_{SC}$ is

$$\vec{V}_{SC} = \vec{V}_P - \vec{V}'_{pf} \quad (5.4)$$

where $\vec{V}'_{pf}$ denotes the measured source-side voltage of the SC.

6.2.2 Fault Current Limiting

The simple power system model shown in Fig. 6-3 (a) is used to explain the principle of the proposed fault current limiting method of the SC. In this model, X is the effective reactance between the PCC and the location, node f , where a solid three-phase fault occurs. The pre-fault voltage at f is $\vec{V}_f$.

Fig. 6-3 Network pre-fault condition and phasor diagram.

Chapter 6 Control of Series Compensator under Downstream Fault Condition

The relationship between the line current and the voltages under the pre-fault condition can be expressed as

$$\vec{V}_S - \vec{V}_P - jX_S \vec{I}_L = 0 \quad (5.5)$$

$$\vec{V}_P - \vec{V}_f - jX_L \vec{I}_L = 0 \quad (5.6)$$

where $\vec{V}_P$ is the pre-fault voltages at the PCC. Phasor diagram of the current and voltages is shown in Fig. 6-3. Normally, the line impedance is much smaller than the impedance of the load, so the voltage drop across the line is small when compared to the load voltage. Thus, $\vec{V}_P$ and $\vec{V}_f$ have almost the same magnitude.

When the downstream fault occurs at f, thus $\vec{V}_f = 0$. As the focus now is on downstream fault condition, one may assume that the equivalent source voltage $\vec{V}_S$ and reactance X_S remain unchanged. From Fig. 6-4 (a), the following circuit equations can be established

$$\vec{V}_S - \vec{V}_{Pf} - jX_S \vec{I}_f = 0 \quad (5.7)$$

$$\vec{V}_{Pf} - jX \vec{I}_f = 0 \quad (5.8)$$

where $\vec{V}_{Pf}$ and $\vec{I}_f$ are the respective PCC voltage and fault current during fault, without the SC in the network. The phasor diagram of the voltages and current is shown in Fig. 6-4 (b). As line losses have been neglected, therefore, the voltage phasors are perpendicular to the fault current $\vec{I}_f$.

(a)

Fig. 6-4 Network condition under a downstream fault.

From equation (5.5), one notes that the pre-fault current is

$$\vec{I}_L = \frac{\vec{V}_S - \vec{V}_P}{jX_S} \quad (5.9)$$

whereas from equation (5.7), the fault current will be

$$\vec{I}_f = \frac{\vec{V}_S - \vec{V}_{Pf}}{jX_S} \quad (5.10)$$

From equationa (5.9) and (5.10), one can readily show that if $|\vec{V}_P| \cos \theta > |\vec{V}_{Pf}|$ where θ is the phase angle between $\vec{V}_P$ and $\vec{V}_S$, the fault current $|\vec{I}_f|$ will be larger than the pre-fault line current $|\vec{I}_L|$. This is a condition most likely to occur in practice when the downstream fault occurs.

The proposed scheme to limit the fault current can be described in the following way. It is proposed that as soon as the fault is detected, the SC will inject a series voltage $\vec{V}_{SC}$ through the injection transformer, as shown in Fig. 6-5 (a). Furthermore, $\vec{V}_{SC}$ will attain such a value that the PCC voltage will be restored back to its phasor value identical to that prior to the fault. This restoration is to be carried out through a continuous adjustment in $\vec{V}_{SC}$. Thus, when full restoration has been achieved, $\vec{V}_{Pf} = \vec{V}_P$. Once that happens, from equationa (5.9) and (5.10), it can be seen that the fault current will be limited to its pre-

Chapter 6 Control of Series Compensator under Downstream Fault Condition

fault level, i.e. $\vec{I}_f = \vec{I}_L$. At this stage, the relationship between the line current and the voltages can be expressed as

$$\vec{V}_S - \vec{V}_P - jX_S \vec{I}_L = 0 \quad (5.11)$$

$$\vec{V}_P - \vec{V}_{SC} - jX \vec{I}_L = 0 \quad (5.12)$$

The corresponding phasor diagram is shown in Fig. 6-5 (b).

(a)

(b)

Fig. 6-5 Downstream fault condition with the FCL in service : $\vec{V}_{pf} = \vec{V}_P$, $\vec{I}_f = \vec{I}_L$ at full restoration.

By comparing the phasor diagrams of Fig. 6-3(b) and Fig. 6-5 (b), one notes that when

$$\vec{V}_{SC} = \vec{V}_f \quad (5.13)$$

Chapter 6 Control of Series Compensator under Downstream Fault Condition

i.e. at the precise condition when the injection voltage phasor is identical to the pre-fault voltage phasor at f where the fault occurs, the fault current $\vec{I}_f$ would have been limited to the pre-fault load current $\vec{I}_L$. Unfortunately, as the fault location is random and unknown, $\vec{V}_f$ will not be known a priori. One way to overcome this problem is now described.

Rewrite equation (5.12), the injection voltage can be expressed as

$$\vec{V}_{SC} = \vec{V}_P - jX\vec{I}_L \quad (5.14)$$

Thus one notes that the injection voltage can be synthesized if the pre-fault PCC voltage ($\vec{V}_P$) and the voltage component $jX\vec{I}_L$ are known. As is in the case of voltage restoration during an upstream fault, $\vec{V}_P$ is readily measurable and can be logged using the phase lock loop technique. Hence $\vec{V}_P$ can be tracked from the pre-fault condition right through the fault incident. The voltage $jX\vec{I}_L$ is the voltage $\vec{V}_L$ on the load side of the SC. It can also be measured on-line and used in equation (5.14) to determine $\vec{V}_{SC}$. Thus $\vec{V}_{SC}$ can be generated and updated in a continuous manner.

The phasor diagram shown in Fig. 6-6 is used to illustrate the injection process. Before injection, $\vec{V}_{SC} = 0$ and the fault current is $\vec{I}_f$. The PCC voltage is $\vec{V}_{Pf}$, as in Fig. 6-4 (b). The voltage $\vec{V}_L = j\vec{I}_f X$ is measured on the load-side of the SC. As the pre-fault PCC voltage $\vec{V}_P$ is tracked continuously, the injection voltage $\vec{V}_{SC}$ is generated using $\vec{V}_{SC} = \vec{V}_P - \vec{V}_L$. With the injection, the PCC voltage will move progressively toward $\vec{V}_P$. In Fig. 6-6 for example, an intermediate step could be when the PCC voltage reaches $\vec{V}_{Pf1}$ and the line current phasor moves to $\vec{I}_{f1}$. The process will continue until finally the PCC voltage is restored to $\vec{V}_P$ and the line current reaches the pre-fault level $\vec{I}_L$. The adjustment of $\vec{V}_{SC}$ will then end. The process enters into a steady state.

Fig. 6-6 Dynamic process of voltage injection.

Thus for a line equipped with the SC, the fault current will be limited to the pre-fault level should a downstream fault occur. Under such a situation and in order to guarantee that the upstream CB will still operate quickly to clear the fault, the line protection system must be integrated with an additional device capable of detecting the FCL action and alerting this to the CB relay. A technical solution could be to install a communication channel which could be used to send a signal to the CB relay indicating that the SC is operating as a FCL. The CB would be tripped based on its relay inverse definite minimum-time setting. This will ensure the shortest fault clearing time possible to clear the fault.

From the above analysis, it can be seen that the steady-state line current during the fault-current limiting stage is the pre-fault load current $|\vec{I}_L|$. The maximum injected voltage occurs when $X = 0$, i.e. the 3-phase fault is just next to the load-side of the SC. Hence, the voltage rating of the primary winding of the injection transformer of the SC is $|\vec{V}_p|$. Furthermore, the steady-state VA rating of the SC is equaled to $|\vec{V}_f \vec{I}_L|$ or approximately that of the downstream load capacity.

6.3 Voltage Rise within the Energy Storage Device

During the fault-current limiting stage, it can be seen from Fig. 6-5(b) that the SC acts as a load absorbing power from the upstream source. With the PCC voltage restored to $\vec{V}_p$ and the line current to $\vec{I}_L$, the absorbed power equals to the power delivered to the protected load before the fault event, as line losses have been ignored. Suppose the duration of the current limiting action is T . The energy absorbed by the SC is approximately given by

$$E = P_L T \quad (5.15)$$

where P_L is the pre-fault load power. Note that T corresponds to the operating time of the upstream CB considered earlier. The absorbed energy is stored in the energy storage device of the SC. The storage medium is often in the form of capacitor banks, as shown in Fig. 6-1. The absorbed energy will cause a steady-state voltage rise, ΔV , across the capacitor. If losses in the SC are ignored, then E is also given by

$$E = \frac{1}{2} C (\Delta V)^2 + CV \cdot \Delta V \quad (5.16)$$

where V is the voltage rating and C is the capacitance of the energy storage capacitor. From equations (5.15) and (5.16) and ignoring second order effects,

$$\Delta V \approx \frac{P_L T}{CV} \quad (5.17)$$

When the SC is used to limit the fault current, the voltage rating of the injection transformer needs not be increased. This is because voltage restoration following an upstream fault also requires the SC injection voltage to be as high as V_p , in case the fault is next to the PCC. On the other hand, the current rating of the SC has to increase due to the current surge at the beginning of the downstream fault and before the FCL action can be effected completely. Also, the energy storage device is expected to experience a voltage rise given by equation (5.17).

Chapter 6 Control of Series Compensator under Downstream Fault Condition

For a given distribution system, the duration of the injection T is known, as it is equal to the operating time of the line circuit breaker CB. One can define a factor χ as the ratio of rated energy storage capacity of the capacitor to the energy (E) absorbed by the downstream load over the interval T . Energy storage capacity is given by

$$E_c = \frac{1}{2} CV^2 \quad (5.18)$$

From equation (5.15), thus, χ can be expressed as

$$\chi = \frac{E_c}{E} = \frac{CV^2}{2P_L T} \quad (5.19)$$

From equations (5.17) and (5.19), one can obtain an important relationship between the steady-state voltage rise in the SC energy storage capacitor and χ ,

$$\frac{\Delta V}{V} = \frac{1}{2\chi} \quad (5.20)$$

The results of the above analysis can be used to advantage in the design of the FCL. This pertains to the sizing of the energy storage capacitor. Usually one technical requirement on the capacitor is its voltage withstand capability. This means that $\Delta V/V$ must be less than a certain value, typically 0.1-0.2, or the capacitor will be damaged. Given the maximum $\Delta V/V$ allowable and the capacity of the load, one can determine the required capacitance and rated voltage for the energy storage device because :

1. there exists a minimum threshold value for χ , below which the capacitor voltage will exceed the maximum $\Delta V/V$ allowable. This follows from equation (5.20);
2. it then follows from equation (5.19) that if χ has to exceed this threshold value, the most onerous load condition must be when P_L is at the maximum, for this is when χ is at the minimum;

Chapter 6 Control of Series Compensator under Downstream Fault Condition

3. equation (5.19) also indicates that in conjunction with the maximum load condition, χ would also be smallest when the upstream CB operating time T is at the maximum. This means that the worst case fault incident has to be when it occurs right at the end of the reach of the line protection system when T is of the highest value, if one assumes a typical inverse-time over-current protection scheme often used on distribution lines.

Thus one can conclude that with the combination of the load and fault conditions described under scenarios 2 and 3 above, it must result in the highest capacitor energy storage capacity (E_C) requirement.

This last point is perhaps best illustrated using a numerical example. Suppose a 20-kV distribution system has a SC supporting a maximum load of 5 MVA, lowest lagging pf of 0.8. In view of the results from Section 6.2, the SC injection transformer primary voltage rating shall be equal to the nominal voltage at the PCC i.e. 20 kV. If the injection transformer turns-ratio is 1:1, it also means that the equivalent AC voltage rating of the capacitor is $V = 20/\sqrt{3}$ kV/ph. Using these data, then the curves showing χ as a function of T are shown in Fig. 6-7 for the various values of C .

Fig. 6-7 χ versus T .

Suppose the maximum allowable $\Delta V/V$ is 0.1. From equation (5.20) the minimum threshold value of k will be 5. In Fig. 6-7, point A is the intersection of the line $\chi = 5$ and the curve described by (5.19) when $C = 0.06 F$ for a range of values of T . Point A corresponding to $T = 0.16 s$, and this is therefore the maximum upstream CB operating

time during which the SC can maintain V_p , and the capacitor voltage rise will be at 10% above rating. It can be seen in Fig. 6-7 that when increasing the capacitance for energy storage, the intersection point will increase, which means that the maximum allowable fault clearing time T can be higher before the 10% voltage rise constraint is violated. Consequently if the maximum T and P_L are given, the minimum size of the capacitor can be determined.

6.4 Control Scheme

Having established the injection strategy for the FCL function, it still remains to incorporate this function into a control scheme of a SC. The schematic diagram in Fig. 8 shows a typical scheme whereby the PCC voltage is restored by the SC through the injection of the voltage $\vec{V}_{SC}$. A second-order LC filter is used to block all but the desired output voltage fundamental frequency component. Interested readers may wish to refer to the systematic filter design method described in [24]. Assume that the SC harmonic filter has an inductance of L_f with an internal resistance of r_f and a capacitance of C_f . These are included in the circuit. Even though the load is shown in Fig. 6-8 as the impedance Z_L , it must be emphasized that in the following analysis, the precise nature of the load needs not be known, except that it is of constant power factor. The resistance and leakage inductance of injection transformer is assumed negligible and its turns-ratio is 1:n.

Fig. 6-8 A typical SC-connected distribution system.

The following state equations can be obtained:

Chapter 6 Control of Series Compensator under Downstream Fault Condition

$$V_i = V_c + I_f r_f + L_f \frac{dI_f}{dt} \quad (5.21)$$

$$I_f = I_c + nI_L \quad (5.22)$$

$$I_c = C_f \frac{dV_c}{dt} \quad (5.23)$$

$$V_{SC} = nV_c \quad (5.24)$$

Based on equations (5.21)-(5.24), the transfer function block-diagram of the power system under open-loop control can be obtained readily. This is shown in Fig. 6-9. $V_{SC}^*(s)$ is the reference injection voltage, which is generated through the application of equation (5.13). $V_{SC}(s)$ is the actual SC output voltage. $V_{SC}(s)$ for this control configuration can be written as

$$V_{SC}(s) = G_1 V_{SC}^*(s) + G_2 I_L(s) \quad (5.25)$$

$$G_1(s) = \frac{nk_i}{L_f C_f s^2 + r_f C_f s + 1} \quad (5.26)$$

$$G_2(s) = \frac{-n^2(L_f s + r_f)}{L_f C_f s^2 + r_f C_f s + 1} \quad (5.27)$$

where $G_1(s)$ is the transfer function from the reference signal $V_{SC}^*(s)$ to $V_{SC}(s)$ while $G_2(s)$ is the transfer function from $I_L(s)$ to $V_{SC}(s)$.

Fig. 6-9 Open-loop controller for the FCL.

Chapter 6 Control of Series Compensator under Downstream Fault Condition

For the second-order power system, the natural damping frequency ω_{n0} and damping constant ξ_{n0} are given by

$$\omega_{n0} = \sqrt{\frac{1}{L_f C_f}} \quad (5.28)$$

$$\xi_{n0} = \frac{r_f}{2L_f \omega_{n0}} \quad (5.29)$$

ω_{n0} equals to the filter resonance frequency and ξ_{n0} is very much dependent of the filter inductor resistance. Let ω_{n0} be K_f times of system base frequency. As the filter is designed to alleviate the harmonics produced by the inverter, $K_f \gg 1$. The damping constant is then given by

$$\xi_{n0} = \frac{r_f}{2X_{L_f} K_f} \quad (5.30)$$

where X_{L_f} is the reactance value of L_f at the base frequency. For practical filter design, the Q factor of the filter inductor is usually greater than 10 so as to keep the losses in the filter to an acceptable value. This means that r_f/X_{L_f} is likely to be less than 0.1. Hence $\xi_{n0} \ll 1$ since $K_f \gg 1$. This analysis reveals that when the SC is operating under this open-loop control mode, an inherently low damping level can be expected in the power system. Similar conclusion has also been reached in [20].

As discussed in Section 6.3, the capacitor voltage (V_{DC}) will increase when energy is absorbed from the source. V_{DC} directly affects the gain k_i of the VSI and causes k_i to increase. Consequently, the PCC voltage will have a tendency to increase under fault-current limiting condition. To compensate for these changes in V_{DC} , it is proposed that V_{DC} be monitored and its value is used to scale the duty cycle command to the VSI. In this way, the original error reference voltage will be multiplied by a factor V_{ref}/V_{DC} , and the resulting value is fed to the PWM pulse generator. V_{ref} in this case corresponds to the

Chapter 6 Control of Series Compensator under Downstream Fault Condition

full-scale command voltage of the inverter. Thus the inverter can be assumed to be of unity gain in the controller design.

To improve the damping of the system, the control system shown in Fig. 6-10 is considered. The details within the SC block are identical to that shown in Fig. 6-9. In addition, however, as $V_{sc}(s)$ has to track $V_{sc}^*(s)$, so an outer voltage loop has been included. Notice that the rate of change of $V_{sc}(s)$ is proportional to the capacitor current $I_c(s)$ in the filter. If this current can be regulated appropriately, $V_{sc}(s)$ can also be controlled in the event of load current changes. Therefore, the effect of this current disturbance can be effectively alleviated. The proposed inner current loop and the outer voltage feedback loop controllers are the two proportional regulators k_c and k_v . This is because since the output voltage is sinusoidally varying, a PI regulator will introduce additional phase shift. Hence, integral control action is not considered.

From Fig. 6-10, it can be shown that the closed-loop transfer function between $V_{sc}^*(s)$ and $V_{sc}(s)$ can be obtained

$$V_{sc}(s) = G_{1c}(s)V_{sc}^*(s) + G_{2c}(s)I_L(s) \quad (5.31)$$

$$G_{1c}(s) = \frac{nk_vk_ck_i}{L_fC_fs^2 + (r_fC_f + k_ck_iC_f)s + nk_vk_ck_c + n} \quad (5.32)$$

$$G_{2c}(s) = \frac{-n^2(L_fs + r_f)}{L_fC_fs^2 + (r_fC_f + k_ck_iC_f)s + nk_vk_ck_c + n} \quad (5.33)$$

where $G_{1c}(s)$ is the closed-loop transfer function from the reference signal $V_{sc}^*(s)$ to $V_{sc}(s)$ while $G_{2c}(s)$ is that between $I_L(s)$ and $V_{sc}(s)$.

Fig. 6-10 Proposed control system for the FCL.

The resulting system will have the un-damped natural frequency (ω_{nc}) and damping constant (ξ_{nc}) given by

$$\omega_{nc} = \sqrt{nk_vk_ck_i + n} \cdot \sqrt{\frac{1}{L_f C_f}} \quad (5.34)$$

$$\xi_{nc} = \frac{r_f + k_i k_c}{2L_f \omega_{nc}} \quad (5.35)$$

The un-damped natural frequency of the resulting system is therefore $\sqrt{n + nk_vk_ck_i}$ times filter resonance frequency. If the filter resonance frequency is K_f times system frequency, then

$$\xi_{nc} = \frac{r_f + k_i k_c}{2X_{Lf} K_f \sqrt{n + nk_vk_ck_i}} \quad (5.36)$$

where X_{Lf} is the reactance of the harmonic filter inductance at system frequency. The degree of damping can be increased considerably, as compared to the open-loop control scheme, by the judicious choice of k_v and k_c . Indeed, the above results provide sufficient information for the control system to be designed in the following way. The value of ω_{nc} is determined from the requirement of the closed-system response settling time. Given ω_{nc} , the product k_vk_c can be determined, as the other parameters on the right hand side of equation (5.33) have been assumed known. Next, the value of ξ_{nc} is determined from the

Chapter 6 Control of Series Compensator under Downstream Fault Condition

requirement of permissible maximum overshoot. Given ξ_{nc} , k_c can be chosen to achieve the desired damping constant for the other parameters on the right hand side of (5.34) are known. In this way, the gains k_v and k_c are determined.

With the increase of k_c , a system with improved stability will be obtained. The selection of k_c is limited by the desired value of the damping level ζ and practical consideration such as capacitor current noise amplification and immunity to switching noise. An increase of k_v tends to reduce steady-state error. However it will also reduce the damping level, as can be seen from (6-36). Thus the value of k_v is chosen such that the steady-state error is within an acceptable value, e.g. 2%.

From previous sections, the largest fault current would be obtained when the downstream fault occurs next to the SC. For the selected ω_{nc} and ξ_{nc} , therefore k_v and k_c should be determined under such a fault condition and that the fault current is to be limited close to its pre-fault level. This is because the fault current due to a downstream fault which is further from the SC will be limited to an even lower level. The transient fault current will be properly damped so as not to damage the VSI.

In the event of an upstream fault, the control system shown in Fig. 6-10 is also applicable except that $V_{sc}^*(s)$ is generated through the application of (5.4). In this case, replace $V_L(s)$ by the variable $V_{pf}'(s)$.

6.5 A Dual Function Series Compensator

Having described the FCL function of the SC and the control method by which such capability can be achieved, it is now possible to amalgamate this function with the voltage restoration role of the device to form a new design.

A schematic diagram of the structure of SC with the dual function is shown in Fig. 6-11. The SC can be divided into two distinct parts: power circuit and control circuit.

Chapter 6 Control of Series Compensator under Downstream Fault Condition

The power circuit is identical to that used for normal voltage restoration when an upstream disturbance occurs. For the control system, the measuring system must operate independently on each phase. The output of the controller in Fig. 6-11 is the duty ratio (m_a) for the VSI. There is also the need to generate the reference signal which is the pre-fault PCC voltage V_p used in (5.13). V_p estimation is achieved through the phase locked loop (PLL) scheme. This function is to be realized in the Function Generator shown in Fig. 6-11.

Fig. 6-11 Structure of a Dual Function SC.

In view of the dual functions, there are three modes of operation: dynamic voltage restoration, fault current limiting and stand-by modes. The operation mode selector activates either one of these modes. The strategy for identifying the appropriate operation mode could be based on the signals obtained from I_L and the PCC voltage.

Suppose the power system is in a normal healthy state initially. When either an upstream or a downstream fault occurs, the PCC voltage would decrease. With the occurrence of such a voltage sag event, the SC will depart from its stand-by mode, and enters into one of the two remaining operating modes. The mode by which it should enter would depend on the line current. If the line current increases, it shows that it is a downstream fault event, the device should enter the FCL mode. Otherwise, the device should enter into its

Chapter 6 Control of Series Compensator under Downstream Fault Condition

normal voltage restoration mode as the disturbance is identified as an upstream fault event. Once the operating mode has been decided, the corresponding reference voltage would be generated and inputted to the controller, as described in Section 6.4.

6.6 Illustrative Examples

The example of Fig. 6-8 is used to verify the effectiveness of the SC and its control strategy. The corresponding parametric values used are given in Table 6-1 and simulations are accomplished using MATLAB. The distribution system voltage is assumed to be 11 kV as this is a typical level used in practice. The source is assumed to have a reactance value of $30\ \Omega$. This corresponds to a fault level of 4 MVA at the PCC. The load is nominally 0.4 MVA. Hence the short-circuit ratio of the supply system is 10, a representative value for typical distribution systems. The injection transformer is assumed to have a turns-ratio of 1:1. This is a reasonable assumption as the focus of the study is to demonstrate the principle of operation of the SC and not on the detailed design of the compensator. With this turns-ratio and in order to be able to achieve the maximum injected voltage equal to the PCC rated voltage, the DC link voltage is chosen to be $\sqrt{2} * 11\text{ kV} \approx 15.5\text{ kV}$. The design of the filter is based on the technique described in [24]. The design criterion is that the voltage THD on the load side of the SC is to be less than 5%.

Table 6-1 System Parameters

Parameters	Values used in the simulation model
Distribution supply voltage	11 kV
Equivalent source reactance	$60\ \Omega$
Injection transformer turns ratio	1:1
DC link voltage	15.5 kV
Filter capacitor	48 μF
Filter inductance	0.2 mH

Fig. 6-12 shows the waveforms of PCC voltage and line current under a downstream single-phase fault condition. The fault occurs at the end of reach of the line protection system. Fig. 6-13 shows the corresponding PCC voltage and line current with open-loop controlled FCL under the same fault condition.

Chapter 6 Control of Series Compensator under Downstream Fault Condition

Fig. 6-12 PCC voltage and line current under a downstream L-G fault- no FCL.

Fig. 6-13 PCC voltage and line current: FCL on open-loop control but without DC voltage compensation.

Chapter 6 Control of Series Compensator under Downstream Fault Condition

With the FCL, the fault current is restrained and the steady-state line current is kept close to the pre-fault level. The PCC voltage has also been restored. However with the open-loop controller but without the DC voltage compensation, it is seen that the PCC voltage has a tendency to increase slightly. This was explained in Section 6.4 in term of the SC absorbing energy and thus gives rise to a voltage swell across the energy storage capacitor, as shown in Fig. 6-14.

Fig. 6-14 Voltage across the terminals of the energy storage capacitor.

With the DC voltage compensation, the PCC voltage is kept constant, as shown in Fig. 6-15. V_{DC} will continue to rise but the corresponding decrease in the PWM gain has been compensated adequately for the voltage rise, in order to keep V_p constant. However, there is large transient voltage and current at the beginning of the voltage injection, and the PCC voltage requires close to 1 cycle to settle.

Suppose it is desirable to obtain a proper natural damping frequency (ω_{nc}) of 3 kHz and damping constant (ξ_{nc}) of 0.75 for the power system, the parameters of the proposed controller are chosen according to equations (6.34) and (6.35). This yields $k_v = 0.7$ and $k_c = 71$. With the proposed closed-loop controller, the steady-state current and PCC voltage are kept close to the pre-fault level, as shown in Fig. 6-16. It can be seen that the proposed controller results in a much shorter settling time, i.e. the degree of damping has been increased.

Chapter 6 Control of Series Compensator under Downstream Fault Condition

Fig. 6-15 PCC voltage and line current: FCL with open-loop control and DC voltage compensation.

Fig. 6-16 PCC voltage and line current: FCL with outer voltage and inner current control.

Chapter 6 Control of Series Compensator under Downstream Fault Condition

The case of a remote downstream single-phase-ground fault some 10 km from the SC has also been examined. The 11-kV distribution line reactance is assumed to be $0.3 \Omega/\text{km}$. The restored PCC voltage and line current with the FCL in service are as shown in Fig. 6-17. Again it can be seen that the fault current has been limited successfully.

Fig. 6-17 PCC voltage and line current: remote single-phase-ground fault.

The case of a downstream three-phase-ground fault has also been studied. Fig. 6-18 shows that the FCL is again effective under such a severe fault condition.

Finally, Fig. 6-19 shows the consequence of an upstream 3-phase fault when the PCC voltage is depressed. Nevertheless, the SC is successful in restoring the load voltage so that minimal disturbance is experienced at the load. The SC is operating as a voltage restorer, as intended.

Chapter 6 Control of Series Compensator under Downstream Fault Condition

Fig. 6-18 PCC voltage and line current under a downstream 3-phase fault: FCL in service.

Fig. 6-19 PCC voltage and Load-side voltage: SC with closed-loop control.

6.7 Conclusions

In previous Chapters, the mitigation of the impacts of upstream disturbances through SC has been discussed. In this Chapter, the control of the SC under downstream fault condition is investigated. The purpose is to design the compensator with fault current limiting function. The principle of operation of the compensator is elaborated. When a downstream fault occurs, the SC achieves the current limiting function by injecting a voltage component to restore the PCC voltage to its pre-fault phasor value. It is shown that under this condition, the SC absorbs energy from the external system. The consequence is a voltage rise in the energy storage capacitor of the SC. Based on an analysis of the voltage rise effect, a method to determine the rating of the capacitor has been proposed. The outer voltage and inner current feedback control scheme shown in this Chapter allows the SC to achieve load-side voltage restoration function for upstream fault and current limiting for downstream fault. The effectiveness of the proposed series compensator system for FCL as well as for voltage restoration functions has been verified through simulations.

Chapter 7 Conclusions and Recommendations

7.1 Conclusions

The thesis is concerned with power quality enhancement in an isolated power system. The series compensation technique is applied for the purpose of providing customers with an acceptable level of electrical supply quality. Likely causes of poor power quality considered are harmonics generated by non-linear loads, voltage sags/swells due to faults or load fluctuations. Mitigation of the disturbances is achieved by injecting/absorbing energy from the external power system through the adjustment of a voltage component in series with the load terminal voltage. The series compensator considered in this thesis is a VSI- based Custom Power equipment.

Currently most of research works on power quality are focused on interconnected power systems. However with the push for the de-regulation of the power utility industry, one can envisage the growth of small isolated power systems in locations where it becomes un-economical to have grid connections. Of the power quality issues in such a small electrical system, harmonic distortion is one of the most commonly encountered phenomena. Thus, a series compensation method has been proposed in Chapter 3 to mitigate the impact of the harmonics. The proposed technique is based on the control of the SC branch impedance. A load-current feedback scheme is incorporated into the control system of the SC. The feedback current will pass through a lead-lag filter $R'(s)$ which appears as high impedance for high frequency current component while the fundamental component will not be affected. Limited by the bandwidth of the controller, the load-current feedback current scheme can have effect only on those current components lower than bandwidth frequency. Thus the scheme is to operate in conjunction with an inductive filter which is intended for mitigating high-order harmonic currents. The design of the filter and feedback scheme has been described. In the process

Chapter 7 Conclusions and Recommendations

of harmonic voltage compensation, it is shown that power exchange exists between the SC and the external network. It would result in the variation of the terminal voltage of the energy storage system (ESS) of the SC. It is shown that the injected real fundamental power of SC can be controlled by shifting the fundamental frequency component of the SC control system reference voltage. Thus a method to maintain the voltage of the ESS through the phase shifting of the fundamental frequency component of the SC control system reference voltage has been described. From the analysis of the process of the energy exchange, a strategy on the phase adjustment has been obtained. Simulation results have confirmed the effectiveness of the proposed method, as it is applied on the SC to achieve improved quality of supply in the power system.

To verify the efficacy of the control scheme described in Chapter 3, a prototype of the SC has been constructed in the laboratory. The proposed technique in the chapter has been implemented in an experimental prototype. Results obtained demonstrate that the proposed scheme is effective to improve the power quality of the isolated power system, not only in terms of reducing harmonic distortions but also in mitigating voltage sags/swells that can occur due to load changes. At the same time, the voltage of the ESS can also be maintained during the operation.

By the nature of isolated power system, sensitive loads would face harmonics and load-change induced voltage sags/swells simultaneously. Chapter 5 considers the design of a voltage compensation strategy under such a scenario. The SC is designed to maintain the fundamental frequency component of the terminal voltage of the protected sensitive load. In the process of harmonic voltage compensation, it is shown that power exchange exists between the SC and the external network. Based on the analysis of the harmonic real power flows in the power system, it is seen that the SC would import harmonic real power from the external system. Considering the presence of harmonic power absorption and the fact that the SC requires extra energy to ride through severe voltage sags, a series compensation strategy has been proposed to take advantage of the harmonic power. The proposed method improves the ride-through capability of the sensitive load by a margin, through the SC absorbing the harmonic power generated by the main load and converting it into real power for supporting the sensitive load voltage. It is shown that the most

onerous sensitive-load ride through condition is that when the load is at full load, unity power factor, while harmonic power flow of the main non-linear load is at the minimum. It is also shown that the maximum injection voltage is approximately equal to $V_{L1} \sin \theta$. So the capacity of the SC required to realize the load ride-through is modest and is approximately equal to $\sin \theta$ times of the protected load capacity. Therefore it makes the SC a viable device for such an application.

In Chapters 3 and 5, the SC is controlled to mitigate the impacts of disturbances originated upstream of the protected sensitive load. While the downstream system is far less extensive than the upstream power system, however, there is no guarantee that downstream fault would not occur. Under a downstream fault condition, the large fault current could damage the SC. To prevent excessive fault current from flowing through the SC, a method to control the SC with a fault current limiting function is investigated in Chapter 6. The principle of operation of the compensator is elaborated there. It is proposed that as soon as a downstream fault is detected, the SC will inject a series voltage $\vec{V}_{SC}$ to the system such that the PCC voltage will be restored back to its phasor value identical to that prior to the fault. This restoration is to be carried out through a continuous adjustment in $\vec{V}_{SC}$. When the PCC voltage is restored to its pre-fault phasor value, it is shown that the fault current will be limited to its pre-fault level. It is also shown that under this condition, the SC absorbs energy from the external system. This will result in a voltage rise in the energy storage capacitor of the SC. It is shown that the most onerous load condition must be when the power supplied by the upstream feeder is at the maximum. And the worst case fault incident is when it occurs right at the end of the reach of the line protection system. With the combination of the load and the fault conditions, it will result in the highest amount of power the capacitor would absorb. Based on an analysis of the voltage rise effect, a method to determine the rating of the capacitor has been proposed. By combining with the results of Chapters 3 and 5, an outer voltage and inner current feedback control scheme shown in the chapter allows the SC to achieve load-side voltage restoration function for an upstream fault as well as for current limiting during a downstream fault. The effectiveness of the proposed series compensator system has been verified through simulations.

7.2 Recommendations

In view of the progress described in the previous chapters, the following directions are suggested as possible areas for further investigation.

In Chapters 3 and 5, the schemes for the mitigation of disturbances in an isolated power system have been derived based on the assumption that the system voltage/current is balanced during disturbance as well as during the restoration process. In many cases, this assumption may not be valid. For example, if the system experiences a phase-to-ground fault, an unbalanced voltage sag/swell will be seen by the sensitive load. The faulted phase voltage would be depressed whereas the unfaulted phase voltages could rise. Therefore, further study should be carried out on how to realize the proposed method under such case. It may require the SC to operate as three independent single-phase units.

Chapter 5 describes a new voltage sag/swell compensation strategy, including the presence of harmonics. In the real harmonic power analysis given in Section 5.2.3, only limited number of operating conditions have been studied to show the effect of load changes on the harmonic power (P_{Ch}). If one can obtain a more general analytical relationship between the harmonic power and the load changes, in terms of firing angle and overlap angle, and develop a method to determine P_{Ch} , this will be much more useful for the SC design. In addition, if a sag is too severe and even the harmonic power absorbed is insufficient for ride-through, the ESS has to inject energy to the external system to maintain the sensitive load voltage. It would result in the excessive decrease of the ESS voltage. A possible method to alleviate this problem is to connect the DC link with an active source. Furthermore, the proposed compensation strategy has only been verified through simulations. It will be interesting to demonstrate its effectiveness experimentally, by extending the prototype described in Chapter 4.

Chapter 6 suggests a method to control the SC to limit fault current under a downstream fault condition. It is important to note that an accurate and rapid method will be required to detect such a fault occurrence. The fault current has to be controlled as quickly as possible to avoid damage to the SC. A fast fault detection method based on the measured

Chapter 7 Conclusions and Recommendations

instantaneous value of the voltage/current waveforms may be needed. The so-called traveling wave method used in transmission network protection system design could be one possible approach.

In the studies, the injection transformer of the SC is assumed to be linear. However the transformer could saturate when it experiences high level flux-linkage. Thus it is necessary to look into the possibility of the injection transformer saturation affecting the injection capability. One design which has been considered is to omit the series transformer from the design. It will, however, require a re-design of the VSI and ESS. This could be a very fruitful area for future work.

References

- [1] N. Hingorani, "Introducing Custom Power," *IEEE Spectrum*, vol. 32, pp. 41-48, 1995.
- [2] B. M. Hughes, J. S. Chan, and D. O. Koval, "Distribution customer power quality experience," *IEEE Transactions on Industry Applications*, vol. 29, pp. 1204-1211, 1993.
- [3] M. H. J. Bollen, *Understanding power quality problems: voltage sag and interruptions*. New York: IEEE Press, 2000.
- [4] J. Arrillaga, M. H. J. Bollen, N. R. Watson, "Power Quality Following Deregulation", *Proceedings of the IEEE*, Vol. 88, pp.246-261,2000.
- [5] J. Stones and A. Collinson, "Power quality," *Power Engineering Journal*, vol. 15, pp. 58-64, 2001.
- [6] A. Collinson, "Power quality, the volts and amps of electricity supply," *IEE Review*, vol. 45, pp. 122, 124, 1999.
- [7] K. Price, "Practices for solving end-user power quality problems," *IEEE Transactions on Industry Applications*, vol. 29, pp. 1164-1169, 1993.
- [8] D. O. Koval, J. C. Chang, and J. Leonard, "Rural power quality," *IEEE Transactions on Industry Application*, vol. 28, pp. 761-766, 1992.
- [9] J. Douglas, "Power quality solutions," *IEEE Power Engineering Review*, vol. 14, pp. 3-7, 1994.

References

- [10] M. E. Baran, J. Maclaga, A. W. Kelley, and K. Craven, "Effects of power disturbances on computer systems," *IEEE Transactions on Power Delivery*, vol. 13, pp. 1309-1315, 1998.
 - [11] M. H. J. Bollen, "What is power quality ?," *Electric Power System Research*, vol. 66, pp. 5-14, 2003.
 - [12] B. H. Chowdhury, "Power quality," *IEEE Potentials*, vol. 20, pp. 5-11, 2001.
 - [13] O. C. N. Souto, J. C. De Oliveira, L. M. Neto, and P. F. Ribeiro, "Power quality impact on performance and associated costs of three-phase induction motors," *8th International Conference on Harmonics and Quality of Power*, vol. 2, pp. 791-797, 1998.
 - [14] A. Ghosh and G. Ledwich, *Power Quality Enhancement using Custom Power Devices*. Boston: Kluwer Academic Publishers, 2002.
 - [15] R. C. Dugan, M. F. McGranaghan, and H. W. Beaty, *Electric power systems quality*. New York: McGraw-Hill, 1996.
 - [16] S. S. Choi, J. D. Li, and D. M. Vilathgamuwa, "A generalized voltage compensation strategy for mitigating the impacts of voltage sags/swells," *IEEE Transactions on Power Delivery*, vol. 20, pp. 2289-2297, 2005.
 - [17] E. K. K. Sng, S. S. Choi, and D. M. Vilathgamuwa, "Analysis of series compensation and DC-link voltage controls of a transformerless self-charging dynamic voltage restorer," *IEEE Transactions on Power Delivery*, vol. 19, pp. 1511-1518, 2004.
 - [18] J. G. Nielsen, M. Newman, H. Nielsen, and F. Blaabjerg, "Control and testing of a dynamic voltage restorer (DVR) at medium voltage level," *IEEE Transactions on Power Electronics*, vol. 19, pp. 806-813, 2004.
-

References

-
- [19] S. Samineni, B. K. Johnson, H. L. Hess, and J. D. Law, "Modeling and analysis of a flywheel energy storage system for voltage sag correction," *IEEE International Electric Machines and Drives Conference, IEMDC'03*, vol. 3, pp. 1813-1818, 2003.
 - [20] M. Vilathgamuwa, A. A. D. Ranjith Perera, and S. S. Choi, "Performance improvement of the dynamic voltage restorer with closed-loop load voltage and current-mode control," *IEEE Transactions on Power Electronics*, vol. 17, pp. 824-834, 2002.
 - [21] B. H. Li, S. S. Choi, and D. M. Vilathgamuwa, "Transformerless dynamic voltage restorer," *IEE Proceedings of Generation, Transmission and Distribution*, vol. 149, pp. 263-273, 2002.
 - [22] A. Ghosh and G. Ledwich, "Compensation of distribution system voltage using DVR," *IEEE Transactions on Power Delivery*, vol. 17, pp. 1030-1036, 2002.
 - [23] C. Fitzer, A. Arulampalam, M. Barnes, and R. Zurowski, "Mitigation of saturation in dynamic voltage restorer connection transformers," *IEEE Transactions on Power Electronics*, vol. 17, pp. 1058-1066, 2002.
 - [24] S. S. Choi, B. H. Li, and D. M. Vilathgamuwa, "Design and analysis of the inverter-side filter used in the dynamic voltage restorer," *IEEE Transactions on Power Delivery*, vol. 17, pp. 857-864, 2002.
 - [25] H. Awad and J. Svensson, "Charging techniques for energy-storage capacitors of static series compensator," *Proceeding of IEEE International Symposium on Industrial Electronics*, vol. 3, pp. 930-935, vol. 3, 2002.
 - [26] C. Zhan, V. K. Ramachandaramurthy, A. Arulampalam, C. Fitzer, S. Kromlidis, M. Barnes, and N. Jenkins, "Dynamic voltage restorer based on voltage-space-vector PWM control," *IEEE Transactions on Industry Applications*, vol. 37, pp. 1855-1863, 2001.
-

References

- [27] J. G. Nielsen, and F. Blaabjerg, "A detailed comparison of system topologies for dynamic voltage restorer," *IEEE Transactions on Industry Applications*, vol. 41, pp. 1271-1280, 2005.
 - [28] A. Ghosh and G. Ledwich, "Structures and control of a dynamic voltage regulator (DVR)," *Proceedings of IEEE Power Engineering Society Winter Meeting*, vol. 3, pp. 1027-1032, 2001.
 - [29] I. Papic, "Power quality improvement using distribution static compensator with energy storage system," *Ninth International Conference on Harmonics and Quality of Power*, vol. 3, pp. 916-920, 2000.
 - [30] B. H. Li, S. S. Choi, and D. M. Vilathgamuwa, "On the injection transformer used in the dynamic voltage restorer," *Proceeding of International Conference on Power System Technology*, 2000.
 - [31] A. Ghosh and A. Joshi, "A new algorithm for the generation of reference voltage of a DVR using the method of instantaneous symmetrical components," *IEEE Power Engineering Review*, pp. 63-65, 2002.
 - [32] S. S. Choi, B. H. Li, and D. M. Vilathgamuwa, "Dynamic voltage restoration with minimum energy injection," *IEEE Transactions on Power Systems*, vol. 15, pp. 51-57, 2000.
 - [33] N. H. Woodley, L. Morgan, and A. Sundaram, "Experience with an inverter-based dynamic voltage restorer," *IEEE Transactions on Power Delivery*, vol. 14, pp. 1181-1186, 1999.
 - [34] M. Vilathgamuwa, A. A. D. Ranjith Perera and S. S. Choi, "Voltage sag compensation with energy optimized dynamic voltage restorer," *IEEE Transaction on Power Delivery*, vol. 18, 1999.
-

References

- [35] P. F. Ribeiro, "An overview of power quality problems in transportation and isolated power systems," *Proceeding of IEEE Power Engineering Society Summer Meeting*, vol. 1, pp. 196-197, 2001.
 - [36] J. Mindykowski, M. Szweda, and T. Tarasiuk, "Measurement equipment for ships' electrical power systems," *Proceeding of the 21st IEEE Instrumentation and Measurement Technology Conference*, vol. 2, pp. 1367-1372, 2004.
 - [37] R. Billinton and R. Karki, "Maintaining supply reliability of small isolated power systems using renewable energy," *IEE Proceedings of Generation, Transmission and Distribution*, vol. 148, pp. 530-534, 2001.
 - [38] I. Jonasson and L. Soder, "Power quality on ships-a questionnaire evaluation concerning island power system," *Proceeding of IEEE Power Engineering Society Summer Meeting*, vol. 1, pp. 216-221, 2001.
 - [39] J. J. Graham, C. L. Halsall, and I. S. McKay, "Isolated power systems. Problems of waveform distortion due to thyristor converter loading," *Fourth International Conf. on Power Electronics and Variable-Speed Drives*, pp. 327-330, 1990.
 - [40] K. S. Smith and L. Ran, "Voltage stability assessment of isolated power systems with power electronic converters," *IEE Proceedings of Generation, Transmission and Distribution*, vol. 141, pp. 310-314, 1994.
 - [41] G. V. Hicks, B. Jeyasurya, and W. F. Snow, "An investigation of automatic generation control for an isolated power system," *IEEE Conference on Electrical and Computer Engineering*, vol. 1, pp. 31-34, 1997.
 - [42] "IEEE recommended practice for monitoring electric power quality," in *IEEE Std 1159-1995*, 1995.
 - [43] I. T. I. C. I. ITI (CBEMA) Curve Application Note, available at <http://www.itic.org>.
-

References

- [44] R. Lamedica, G. Esposito, E. Tironi, D. Zaninelli, and A. Prudenzi, "A survey on power quality cost in industrial customers," *Proceeding of IEEE Power Engineering Society Winter Meeting*, vol. 2, pp. 938-943, 2001.
- [45] J. Arrillaga and N. R. Watson, *Power Systems Harmonics*. Chichester: John Wiley & Sons, 2003.
- [46] R. Yacamini, "Power system harmonics. Part 1. Harmonic sources," *Power Engineering Journal*, vol. 8, pp. 193-198, 1994.
- [47] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power electronics-converters, applications and design (2nd Edition)*. New York: John Willy & Sons Inc., 1995.
- [48] P. C. Sen, *Principles of Electric Machines and Power Electronics*, 2nd Edition. New York: John Wiley & Sons, 1997.
- [49] E. R. Collins, Jr. and A. Mansoor, "Effects of voltage sags on AC motor drives," *IEEE Annual Textile, Fiber, and Film Industry Technical Conf.*, pp. 97, 1997.
- [50] F. Jurado, N. Acero, A. Lopez, and J. I. Rojas, "Adjustable speed drives and voltage stability," *IEEE International Electric Machines and Drives Conf.*, pp. 522-527, 2001.
- [51] R. Langley, A. Mansoor, E. R. Collins, Jr., and R. L. Morgan, "Voltage sag ride-through testing of adjustable speed drives using a controllable dynamic dynamometer," *Proceeding of 8th International Conference on Harmonics and Quality of Power*, vol. 1, pp. 566-571, 1998.
- [52] M. B. R. Correa, C. B. Jacobina, A. M. N. Lima, and E. R. C. da Silva, "Adjustable-speed single-phase induction motor drive," *Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition*, vol. 2, pp. 770-776, 2002.

References

- [53] N. S. Tunaboylu, E. R. Collins, Jr., S. W. Middlekauff, and R. L. Morgan, "Ride-through issues for DC motor drives during voltage sags," *Proceeding of IEEE Southeastcon*, pp. 52-58, 1995.
- [54] J. C. Gomez, M. M. Morcos, C. A. Reineri, and G. N. Campetelli, "Behavior of induction motor due to voltage sags and short interruptions," *IEEE Transactions on Power Delivery*, vol. 17, pp. 434-440, 2002.
- [55] A. A. Girgis, J. W. Nims, J. Jacamino, J. G. Dalton, and A. Bishop, "Effect of voltage harmonics on the operation of solid state relays in industrial applications," *Proceeding of IEEE Industry Applications Society Annual Meeting*, pp. 1821-1828, 1990.
- [56] V. E. Wagner, "The effects of harmonic on equipment," *IEEE Transactions on Power Delivery*, vol. 8, pp. 672-680, 1993.
- [57] A. Ludbrook, "Harmonic filters for notch reduction," *IEEE Transactions on Industry Applications*, vol. 24, pp. 947-954, 1988.
- [58] J. F. J. Roesel, "Improved power quality with 'Written-Pole' motor-generators and 'Written-Pole' motors," *Proceeding of the 1996 IEEE SOUTHEASTCON Conference*, pp. 565-570, 1996.
- [59] G. A. Taylor, "Power quality hardware solutions for distribution systems: Custom Power," *IEE North Eastern Centre Power Section Symposium on the Reliability, Security and Power Quality of Distribution Systems*, pp. 111-119, 1995.
- [60] S. W. Middlekauff and E. R. Collins, Jr., "System and customer impact: considerations for series custom power devices," *IEEE Transactions on Power Delivery*, vol. 13, pp. 278-282, 1998.

References

- [61] H. Mokhtari, S. B. Dewan, and M. R. Iravani, "Performance evaluation of thyristor based static transfer switch," *Proceeding of IEEE Power Engineering Society Summer Meeting*, vol. 2, pp. 961, 2001.
- [62] J. E. Jipping and W. E. Carter, "Application and experience with a 15 kV static transfer switch," *IEEE Transactions on Power Delivery*, vol. 14, pp. 1477-1481, 1999.
- [63] C. W. Brice, R. A. Dougal, and J. L. Hudgins, "Review of technologies for current-limiting low-voltage circuit breakers," *IEEE Transactions on Industry Applications*, vol. 32, pp. 1005-1010, 1996.
- [64] L. Palav and A. M. Gole, "On using the solid state breaker in distribution systems," *IEEE Canadian Conference on Electrical and Computer Engineering*, vol. 2, pp. 693-696, 1998.
- [65] T. Ueda, M. Morita, H. Arita, Y. Kida, Y. Kurosawa, and T. Yamagiwa, "Solid-state current limiter for power distribution system," *IEEE Transactions on Power Delivery*, vol. 8, pp. 1796-1801, 1993.
- [66] B. Korobeynikov, D. Ishchenko, and A. Ishchenko, "Solid-state fault current limiter for medium voltage distribution systems," *Proceeding of IEEE Bologna Power Tech Conference*, vol. 2, pp. 6, 2003.
- [67] D. Ito, K. Tsurunaga, E. S. Yoneda, Y. Sugiyama, T. Hara, K. Okaniwa, H. Hoshino, and T. Yamamoto, "Superconducting fault current limiter development," *IEEE Transactions on Magnetics*, vol. 27, pp. 2345-2348, 1991.
- [68] M. Ichikawa and M. Okazaki, "A magnetic shielding type superconducting fault current limiter using a Bi2212 thick film cylinder," *IEEE Transactions on Applied Superconductivity*, vol. 5, pp. 1067-1070, 1995.

References

- [69] J. X. Jin, S. X. Dou, H. K. Liu, C. Grantham, Z. J. Zeng, Z. Y. Liu, T. R. Blackburn, X. Y. Li, H. L. Liu, and J. Y. Liu, "Electrical application of high T_c superconducting saturable magnetic core fault current limiter," *IEEE Transactions on Applied Superconductivity*, vol. 7, pp. 1009-1012, 1997.
 - [70] S. Lee, C. Lee, M. C. Ahn, H. Kang, D. K. Bae, and T. K. Ko, "Design and test of modified bridge type superconducting fault current limiter with reverse magnetized core," *IEEE Transactions on Applied Superconductivity*, vol. 13, pp. 2016-2019, 2003.
 - [71] M. H. Haque, "Compensation of distribution system voltage sag by DVR and D-STATCOM," *Proceeding of IEEE Porto Power Tech*, vol. 1, pp. 5, 2001.
 - [72] G. T. Heydt, W. Tan, T. LaRose, and M. Negley, "Simulation and analysis of series voltage boost technology for power quality enhancement," *IEEE Transactions on Power Delivery*, vol. 13, pp. 1335-1341, 1998.
 - [73] K. Haddad and G. Joos, "Distribution system voltage regulation under fault conditions using static series regulators," *IEEE Industry Applications Conference*, 1997.
 - [74] M. Fang, A. I. Gardiner, A. MacDougall, and G. A. Mathieson, "A novel series dynamic voltage restorer for distribution systems," *Proceeding of International Conference on Power System Technology*, vol. 1, pp. 38-42, 1998.
 - [75] M. H. J. Bollen, "Voltage, power and current ratings of series voltage controllers," *Proceeding of IEEE Power Engineering Society Winter Meeting*, vol. 4, pp. 2910-2915, 2000.
 - [76] T. Wunderlin, O. Amhof, P. Dahler, and H. Guning, "Power supply quality improvement with a dynamic voltage restorer (DVR)," *Proceeding of International Conference on Energy Management and Power Delivery*, vol. 2, pp. 518-525, 1998.
-

References

- [77] B. H. Li, S. S. Choi, and D. W. Vilathgamuwa, "Design considerations on the line-side filter used in the dynamic voltage restorer," *IEE Proceeding of Generation, Transmission and Distribution*, vol. 148, pp. 1-7, 2001.
 - [78] Hyosung Kim and Seung-Ki Sul, "Compensation voltage control in dynamic voltage restorers by use of feed forward and state feedback scheme," *IEEE Transactions on Power Electronics*, vol. 20, pp. 1169-1177, 2005.
 - [79] H. Akagi, "New trends in active filters for power conditioning," *IEEE Transactions on Industry Applications*, vol. 32, pp. 1312-1322, 1996.
 - [80] S. Bhattacharya, T. M. Frank, D. M. Divan, and B. Banerjee, "Active filter system implementation," *IEEE Industry Applications Magazine*, vol. 4, pp. 47-63, 1998.
 - [81] H. Akagi, Y. Tsukamoto, and A. Nabae, "Analysis and design of an active power filter using quad-series voltage source PWM converters," *IEEE Transactions on Industry Applications*, vol. 26, pp. 93-98, 1990.
 - [82] J.-H. Sung, S. Park, and K. Nam, "New hybrid parallel active filter configuration minimising active filter size," *IEEE Proceeding of Electric Power Applications*, vol. 147, pp. 93-98, 2000.
 - [83] J. G. Nielsen, M. Newman, H. Nielsen, and F. Blaabjerg, "Control and testing of a dynamic voltage restorer (DVR) at medium voltage level," *IEEE Transactions on Power Electronics*, vol. 19, pp. 806-813, 2004.
 - [84] I. Papic, "Power quality improvement using distribution static compensator with energy storage system," *Proceedings of Ninth International Conference on Harmonics and Quality of Power*, 2000.
 - [85] N. Abi-Samra, D. Carnovale, A. Sundaram, and W. Malcolm, "The role of the distribution system dynamic voltage restorer in enhancing the power at sensitive facilities," *WESCON/96*, 1996.
-

References

- [86] S. Samineni, B. K. Johnson, H. L. Hess, and J. D. Law, "Modeling and analysis of a flywheel energy storage system for voltage sag correction," *IEEE International Electric Machines and Drives Conference*, 2003.
 - [87] D. H. Pontoriero and P. E. Mercado, "Network compensation with active power filters integrated to PV generation," *Proceeding of IEEE Porto Power Tech*, vol. 2, pp. 6, 2001.
 - [88] S. S. Choi, T. X. Wang, and E. K. Sng, "Power quality enhancement in an isolated power system through series compensator," *Proceeding of 15th Power System Computation Conference, PSCC'05*, 2005.
 - [89] E. W. Kimbark, *Direct Current Transmission*, vol. 1. New York: Wiley-Interscience, 1971.
 - [90] J. P. Tamby and V. I. John, "Q'HARM-a harmonic power-flow program for small power systems," *IEEE Transactions on Power Systems*, vol. 3, pp. 949-955, 1988.
 - [91] G. J. Wakileh, *Power System Harmonics: Fundamental, Analysis and Filter Design*. New York: Springer, 2001.
 - [92] F. Tosato and S. Quaia, "Reducing voltage sags through fault current limitation," *IEEE Transactions on Power Delivery*, vol. 16, pp. 12-17, 2001.
 - [93] S. Sugimoto, J. Kida, H. Arita, C. Fukui, and T. Yamagiwa, "Principle and characteristics of a fault current limiter with series compensation," *IEEE Transactions on Power Delivery*, vol. 11, pp. 842-847, 1996.
 - [94] M. Steurer, K. Frohlich, W. Halaus, and K. Kaltenegger, "A novel hybrid current-limiting circuit breaker for medium voltage: principle and test results," *IEEE Transactions on Power Delivery*, vol. 18, pp. 460-467, 2003.
-

References

- [95] B. Gromoll, G. Ries, W. Schmidt, H.-P. Kramer, P. Kummeth, H.-W. Neumuller, and S. Fischer, "Resistive current limiters with YBCO films," *IEEE Transactions on Applied Superconductivity*, vol. 7, pp. 828-831, 1997.
- [96] L. Ye, L. Lin, and K. P. Juengst, "Application studies of superconducting fault current limiters in electric power systems," *IEEE Transactions on Applied Superconductivity*, vol. 12, pp. 900-903, 2002.
- [97] S. S. Choi, T. X. Wang, and D. M. Vilathgamuwa, "A series compensator ewith fault current limiting function," *IEEE Transactions on Power Delivery*, vol. 20, pp. 2248-2256, 2005.

Appendices

Appendix A

Fourier analysis of $v_s(t)$ and $i_D(t)$

When the drive-load converter operates at a delay angle δ_1 and an overlap angle δ_2 , the resulting waveforms of $v_s(t)$ and $i_D(t)$ take the form shown in the following Figure.

- For $\delta_1 = 10^\circ$ and $\delta_2 = 20^\circ$, phase “a” waveform of $v_{Sa}(t)$ and $i_{Da}(t)$ can be expressed:

ωt	$v_{Sa}(t)$
$0 \sim 40^\circ$	$\hat{V}_m \sin \omega_o t$
$40^\circ \sim 60^\circ$	$\frac{\hat{V}_m}{2} (\sin \omega_o t + \sin(\omega_o t + 120^\circ)) = \frac{\hat{V}_m}{2} \sin(\omega_o t + 60^\circ)$
$60^\circ \sim 160^\circ$	$\hat{V}_m \sin \omega_o t$
$160^\circ \sim 180^\circ$	$\frac{\hat{V}_m}{2} (\sin \omega_o t + \sin(\omega_o t - 120^\circ)) = \frac{\hat{V}_m}{2} \sin(\omega_o t - 60^\circ)$
$180^\circ \sim 220^\circ$	$\hat{V}_m \sin \omega_o t$
$220^\circ \sim 240^\circ$	$\frac{\hat{V}_m}{2} (\sin \omega_o t + \sin(\omega_o t + 120^\circ)) = \frac{\hat{V}_m}{2} \sin(\omega_o t + 60^\circ)$
$240^\circ \sim 340^\circ$	$\hat{V}_m \sin \omega_o t$
$340^\circ \sim 360^\circ$	$\frac{\hat{V}_m}{2} (\sin \omega_o t + \sin(\omega_o t - 120^\circ)) = \frac{\hat{V}_m}{2} \sin(\omega_o t - 60^\circ)$

ωt	$i_{Da}(t)$
$0 \sim 40^\circ$	0
$40^\circ \sim 160^\circ$	I_d
$160^\circ \sim 220^\circ$	0
$220^\circ \sim 340^\circ$	I_d
$340^\circ \sim 360^\circ$	0

Assume

$$v_{Sa}(t) = \sum_{n=1}^{\infty} (a_n \cos n\omega_o t + b_n \sin n\omega_o t)$$

$$i_{Da}(t) = \sum_{n=1}^{\infty} (c_n \cos n\omega_o t + d_n \sin n\omega_o t) \quad (n=1, 2, 3 \dots)$$

So

$$a_n = \frac{1}{\pi} \int_0^{2\pi} v_{Sa}(t) \cos(n\omega_o t) d(\omega_o t)$$

$$b_n = \frac{1}{\pi} \int_0^{2\pi} v_{Sa}(t) \sin(n\omega_o t) d(\omega_o t)$$

$$c_n = \frac{1}{\pi} \int_0^{2\pi} i_{Da}(t) \cos(n\omega_o t) d(\omega_o t)$$

$$d_n = \frac{1}{\pi} \int_0^{2\pi} i_{Da}(t) \sin(n\omega_o t) d(\omega_o t)$$

Let $x = \omega_o t$, then

$$\begin{aligned} a_n &= \frac{1}{\pi} \left\{ \int_0^{40^\circ} \hat{V}_m \sin x \cos nxdx + \int_{40^\circ}^{60^\circ} \hat{V}_m \sin(x+60^\circ) \cos nxdx + \int_{60^\circ}^{160^\circ} \hat{V}_m \sin x \cos nxdx \right. \\ &\quad + \int_{160^\circ}^{180^\circ} \hat{V}_m \sin(x-60^\circ) \cos nxdx + \int_{180^\circ}^{220^\circ} \hat{V}_m \sin x \cos nxdx + \int_{220^\circ}^{240^\circ} \hat{V}_m \sin(x+60^\circ) \cos nxdx \\ &\quad \left. + \int_{240^\circ}^{340^\circ} \hat{V}_m \sin x \cos nxdx + \int_{340^\circ}^{360^\circ} \hat{V}_m \sin(x-60^\circ) \cos nxdx \right\} \\ &= \frac{\hat{V}_m}{2\pi} \left\{ \left(-\frac{\cos(n-1)x}{n-1} - \frac{\cos(n+1)x}{n+1} \right) \Big|_{0^\circ}^{40^\circ} + \frac{1}{2} \left(-\frac{\cos[(n-1)x-60^\circ]}{n-1} - \frac{\cos[(n+1)x+60^\circ]}{n+1} \right) \Big|_{40^\circ}^{60^\circ} \right. \\ &\quad + \left(-\frac{\cos(n-1)x}{n-1} - \frac{\cos(n+1)x}{n+1} \right) \Big|_{60^\circ}^{160^\circ} + \frac{1}{2} \left(-\frac{\cos[(n-1)x+60^\circ]}{n-1} - \frac{\cos[(n+1)x-60^\circ]}{n+1} \right) \Big|_{160^\circ}^{180^\circ} \\ &\quad + \left(-\frac{\cos(n-1)x}{n-1} - \frac{\cos(n+1)x}{n+1} \right) \Big|_{180^\circ}^{220^\circ} + \frac{1}{2} \left(-\frac{\cos[(n-1)x-60^\circ]}{n-1} - \frac{\cos[(n+1)x+60^\circ]}{n+1} \right) \Big|_{220^\circ}^{240^\circ} \\ &\quad \left. + \left(-\frac{\cos(n-1)x}{n-1} - \frac{\cos(n+1)x}{n+1} \right) \Big|_{240^\circ}^{340^\circ} + \frac{1}{2} \left(-\frac{\cos[(n-1)x+60^\circ]}{n-1} - \frac{\cos[(n+1)x-60^\circ]}{n+1} \right) \Big|_{340^\circ}^{360^\circ} \right\} \end{aligned}$$

$$\begin{aligned} b_n &= \frac{1}{\pi} \left\{ \int_0^{40^\circ} \hat{V}_m \sin x \sin nxdx + \int_{40^\circ}^{60^\circ} \hat{V}_m \sin(x+60^\circ) \sin nxdx + \int_{60^\circ}^{160^\circ} \hat{V}_m \sin x \sin nxdx \right. \\ &\quad + \int_{160^\circ}^{180^\circ} \hat{V}_m \sin(x-60^\circ) \sin nxdx + \int_{180^\circ}^{220^\circ} \hat{V}_m \sin x \sin nxdx + \int_{220^\circ}^{240^\circ} \hat{V}_m \sin(x+60^\circ) \sin nxdx \\ &\quad \left. + \int_{240^\circ}^{340^\circ} \hat{V}_m \sin x \sin nxdx + \int_{340^\circ}^{360^\circ} \hat{V}_m \sin(x-60^\circ) \sin nxdx \right\} \end{aligned}$$

$$\begin{aligned}
&= \frac{\hat{V}_m}{2\pi} \left\{ \left(\frac{\sin(n-1)x}{n-1} - \frac{\sin(n+1)x}{n+1} \right) \right|_{0^\circ}^{40^\circ} + \frac{1}{2} \left(\frac{\sin[(n-1)x - 60^\circ]}{n-1} - \frac{\sin[(n+1)x + 60^\circ]}{n+1} \right) \right|_{40^\circ}^{60^\circ} \\
&\quad + \left(\frac{\sin(n-1)x}{n-1} - \frac{\sin(n+1)x}{n+1} \right) \right|_{60^\circ}^{160^\circ} + \frac{1}{2} \left(\frac{\sin[(n-1)x + 60^\circ]}{n-1} - \frac{\sin[(n+1)x - 60^\circ]}{n+1} \right) \right|_{160^\circ}^{180^\circ} \\
&\quad + \left(\frac{\sin(n-1)x}{n-1} - \frac{\sin(n+1)x}{n+1} \right) \right|_{180^\circ}^{220^\circ} + \frac{1}{2} \left(\frac{\sin[(n-1)x - 60^\circ]}{n-1} - \frac{\sin[(n+1)x + 60^\circ]}{n+1} \right) \right|_{220^\circ}^{240^\circ} \\
&\quad + \left(\frac{\sin(n-1)x}{n-1} - \frac{\sin(n+1)x}{n+1} \right) \right|_{240^\circ}^{340^\circ} + \frac{1}{2} \left(\frac{\sin[(n-1)x + 60^\circ]}{n-1} - \frac{\sin[(n+1)x - 60^\circ]}{n+1} \right) \right|_{340^\circ}^{360^\circ} \}
\end{aligned}$$

$$\begin{aligned}
c_n &= \frac{1}{\pi} \left\{ \int_{40^\circ}^{160^\circ} I_d \cos nx dx - \int_{220^\circ}^{340^\circ} I_d \cos nx dx \right\} \\
&= \frac{I_d}{\pi} \left\{ \sin nx \Big|_{40^\circ}^{160^\circ} - \sin nx \Big|_{220^\circ}^{340^\circ} \right\}
\end{aligned}$$

$$\begin{aligned}
d_n &= \frac{1}{\pi} \left\{ \int_{40^\circ}^{160^\circ} I_d \sin nx dx - \int_{220^\circ}^{340^\circ} I_d \sin nx dx \right\} \\
&= \frac{I_d}{\pi} \left\{ -\cos nx \Big|_{40^\circ}^{160^\circ} + \cos nx \Big|_{220^\circ}^{340^\circ} \right\}
\end{aligned}$$

Thus, it can be obtained

$a_1 = \frac{-0.66\hat{V}_m}{2\pi}$	$a_5 = \frac{1.6995\hat{V}_m}{2\pi}$	$a_7 = \frac{\hat{V}_m}{2\pi}$	$a_{11} = \frac{0.51\hat{V}_m}{2\pi}$
$b_1 = \frac{5.673\hat{V}_m}{2\pi}$	$b_5 = \frac{0.6\hat{V}_m}{2\pi}$	$b_7 = \frac{0.26\hat{V}_m}{2\pi}$	$b_{11} = \frac{0.34\hat{V}_m}{2\pi}$
$c_1 = \frac{-0.6I_d}{\pi}$	$c_5 = \frac{-2.23I_d}{5\pi}$	$c_7 = \frac{3.255I_d}{7\pi}$	$c_{11} = \frac{-3.255I_d}{11\pi}$
$d_1 = \frac{3.4I_d}{\pi}$	$d_5 = \frac{2.65I_d}{5\pi}$	$d_7 = \frac{-1.18I_d}{7\pi}$	$d_{11} = \frac{-1.18I_d}{11\pi}$

Then

$$\begin{aligned}
v_{Sa}(t) &= \frac{\hat{V}_m}{2\pi} \{ -0.66 \cos \omega_o t + 5.673 \sin \omega_o t + 1.6995 \cos 5\omega_o t + 0.6 \sin 5\omega_o t + \\
&\quad \cos 7\omega_o t + 0.26 \sin 7\omega_o t + 0.51 \cos 11\omega_o t + 0.34 \sin 11\omega_o t \} \\
&= \hat{V}_m \{ 0.91 \sin(\omega_o t - 6.6^\circ) + 0.28 \sin(5\omega_o t + 70^\circ) + 0.16 \sin(7\omega_o t + 75^\circ) \\
&\quad + 0.1 \sin(11\omega_o t + 56^\circ) \}
\end{aligned}$$

$$\begin{aligned}
i_{Da}(t) &= \frac{I_d}{\pi} \{ -0.6 \cos \omega_o t + 3.4 \sin \omega_o t - 2.23 \cos 5\omega_o t + 2.65 \sin 5\omega_o t + \\
&\quad 3.255 \cos 7\omega_o t - 1.18 \sin 7\omega_o t - 3.255 \cos 11\omega_o t - 1.18 \sin 11\omega_o t \} \\
&= 3.46 \times \frac{I_d}{\pi} \{ \sin(\omega_o t - 10^\circ) + \frac{1}{5} \sin(5\omega_o t - 50^\circ) + \frac{1}{7} \sin(7\omega_o t + 110^\circ) \\
&\quad + \frac{1}{11} \sin(11\omega_o t - 110^\circ) \}
\end{aligned}$$

Hence, equations (5.12) and (5.13) are obtained.

- For $\delta_1 = 30^\circ$ and $\delta_2 = 25^\circ$

$a_1 = \frac{1.263\hat{V}_m}{2\pi}$	$a_5 = \frac{-0.734\hat{V}_m}{2\pi}$	$a_7 = \frac{-1.186\hat{V}_m}{2\pi}$	$a_{11} = \frac{-0.271\hat{V}_m}{2\pi}$
$b_1 = \frac{4.648\hat{V}_m}{2\pi}$	$b_5 = \frac{-0.882\hat{V}_m}{2\pi}$	$b_7 = \frac{-0.944\hat{V}_m}{2\pi}$	$b_{11} = \frac{-0.4242\hat{V}_m}{2\pi}$
$c_1 = \frac{-1.732I_d}{\pi}$	$c_5 = \frac{1.732I_d}{5\pi}$	$c_7 = \frac{-1.732I_d}{7\pi}$	$c_{11} = \frac{1.732I_d}{11\pi}$
$d_1 = \frac{3I_d}{\pi}$	$d_5 = \frac{3I_d}{5\pi}$	$d_7 = \frac{3I_d}{7\pi}$	$d_{11} = \frac{3I_d}{11\pi}$

Then

$$\begin{aligned}
v_{Sa}(t) &= \frac{\hat{V}_m}{2\pi} \{ 1.263 \cos \omega_o t + 4.684 \sin \omega_o t - 0.734 \cos 5\omega_o t - 0.882 \sin 5\omega_o t \\
&\quad - 1.186 \cos 7\omega_o t - 0.944 \sin 7\omega_o t - 0.27 \cos 11\omega_o t - 0.4242 \sin 11\omega_o t \} \\
&= \hat{V}_m \{ 0.77 \sin(\omega_o t + 15.2^\circ) + 0.18 \sin(5\omega_o t - 140^\circ) + 0.24 \sin(7\omega_o t - 129^\circ) \\
&\quad + 0.08 \sin(11\omega_o t - 148^\circ) \}
\end{aligned}$$

$$\begin{aligned}
i_{Da}(t) &= \frac{I_d}{\pi} \{ -1.732 \cos \omega_o t + 3 \sin \omega_o t + 1.732 \cos 5\omega_o t + 3 \sin 5\omega_o t - \\
&\quad 1.732 \cos 7\omega_o t + 3 \sin 7\omega_o t + 1.732 \cos 11\omega_o t + 3 \sin 11\omega_o t \} \\
&= 3.46 \times \frac{I_d}{\pi} \{ \sin(\omega_o t - 30^\circ) + \frac{1}{5} \sin(5\omega_o t + 30^\circ) + \frac{1}{7} \sin(7\omega_o t - 30^\circ) \\
&\quad + \frac{1}{11} \sin(11\omega_o t + 30^\circ) \}
\end{aligned}$$

Hence, equations (5.14) and (5.15) are obtained.

VITA

Wang Tongxun was born in 1977 in P. R. China. He received B. Eng. Degree from Xi'an Jiao Tong University, Xi'an, P. R. China in 1998 and M. Eng. Degree from Tsinghua University, Beijing, P. R. China in 2002 respectively, both in Electrical Engineering.

Since August 2002, he is pursuing for his Ph.D Degree in Power Engineering in Nanyang Technological University. His research interests are in Power System Analysis, Power Quality and Control.

Research related to this dissertation has resulted in the following publications:

- [1] S. S. Choi, T. X. Wang, and D. M. Vilathgamuwa, "A Series Compensator With Fault Current Limiting Function," *IEEE Transactions on Power Delivery*, vol. 20, pp. 2248-2256, 2005.
- [2] S. S. Choi, T. X. Wang and E. K. Sng, "Power Quality Enhancement in an Isolated Power System through Series Compensator," Proc. of 15th Power System Computation Conference, PSCC'05, Liege, Belgium, August, 2005.
- [3] T. X. Wang, S. S. Choi, and E. K. Sng, "A Series Compensation Method to Mitigate Harmonics and Voltage Sags/Swells in an Isolated Power System", in print, *IEE Proceedings of Generation, Transmission and Distribution*.
- [4] T. X. Wang and S. S. Choi, "Enhancement of Voltage Quality of an Isolated Power System", accepted, *IEEE Transactions on. Power Delivery*.