High-k hafnium oxide based thin films using laser molecular beam epitaxy for gate dielectrics

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**HIGH-K HAFNIUM OXIDE BASED THIN FILMS
USING LASER MOLECULAR BEAM EPITAXY FOR
GATE DIELECTRICS**

LU YUEKANG

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

2006

High-K Hafnium Oxide Based Thin Films Using Laser Molecular Beam Epitaxy for Gate Dielectrics

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A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Doctor of Philosophy

2006

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

Date

Lu Yuekang

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SUMMARY

The constant increase in integrated circuit densities predicted by Moore's law requires the continuous reduction of the CMOS device dimensions such as the gate length, gate oxide thickness, etc. Silicon dioxide (SiO_2) has been used as the gate oxide and been aggressively scaled for more than 30 years. Nowadays in the state-of-the-art MOSFET, the gate oxide thickness is reduced to 1.2 nm. However, with the use of such thin SiO_2 , direct tunneling dominates the dielectric conduction which results in high leakage current and unacceptable power dissipations. In order to maintain the performance improvement trends, there are growing interests in the replacement of SiO_2 with a high- k dielectric material. According to the recent researches, hafnium oxide based materials, such as hafnium oxide (HfO_2), hafnium silicate (HfSiO) and hafnium silicon oxynitride (HfSiON), are considered promising materials as the future gate dielectric. Therefore in this thesis, these materials have been systematically investigated for potential gate dielectric application.

For high- k gate dielectrics deposition, it is essential to control the thickness and roughness of the films down to an atomic scale, thus provides the MOS device with low defect densities and good reliability property. For this reason, Laser-MBE, which has the merits of both pulsed laser deposition (PLD) and conventional MBE, is

Summary

installed and employed to deposit the high- k materials in this research work.

The formation of a low- k interface layer, which seriously deteriorates the gate performance, is usually observed for most high- k gate dielectrics. HfO_2 is of no exception. By optimizing the deposition parameters, the interfacial reaction in Laser-MBE derived HfO_2 has been greatly suppressed. It has been found that by optimizing the oxygen partial pressure as well as adopting a two-step deposition scheme, high quality ultrathin HfO_2 films have been achieved. It is clearly shown that with the same equivalent oxide thickness (EOT) of 1.3 nm, the leakage current density in HfO_2 is about 4 orders of magnitude lower compared to the conventional SiO_2 . And the investigation of the conduction mechanisms in the HfO_2 demonstrates that the Schottky model, Poole-Frenkel (PF) model and Fowler-Nordheim (FN) tunneling dominate the conduction mechanisms in different electric field regions.

Furthermore, RuO_2 has been investigated as an alternative gate electrode for pMOS devices. It is shown that RuO_2 has acceptable resistivity ($400 \mu\Omega \cdot \text{cm}$) and work function (5.0 eV), as well as good thermal stability up to 800 °C. The $\text{RuO}_2/\text{HfO}_2/\text{n-Si}$ MOS capacitors show good dielectric and electrical properties, such as negligible flat band shift and hysteresis ($< 10 \text{ mV}$), very strong breakdown strength ($> 10 \text{ MVcm}^{-1}$).

Summary

For the purpose of increasing the crystalline temperature of the hafnium oxide based gate dielectrics, optimized concentration of silicon is incorporated into hafnium oxide. It is found that even after rapid thermal annealing (RTA) at 950 °C in N₂ for 30 seconds, hafnium silicate (Hf_{0.23}Si_{0.12}O_{0.65}) is still in amorphous state and no obvious interface exists. Compared to hafnium oxide with the same thickness, Hf_{0.23}Si_{0.12}O_{0.65} (EOT~ 1.2 nm) shows improved electrical and dielectric properties.

Moreover, by incorporating nitrogen into Hf_{0.23}Si_{0.12}O_{0.65}, it is demonstrated that the EOT has been further reduced to 0.95 nm which is contributed to the further suppression of the interface growth. In addition, the leakage current of HfSiON is about 3 to 4 orders of magnitude lower than that of SiO₂ with the same thickness. The excellent electrical and dielectric properties suggest that HfSiON dielectric is a quite suitable candidate for gate dielectric application.

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LIST OF ABBREVIATIONS

AES	Auger Electron Spectroscopy
ALD	Atomic Layer Deposition
CCS	Constant-Current Stress
CMOS	Complementary Metal-Oxide-Semiconductor
CV	Capacitance-Voltage
CVD	Chemical Vapor Deposition
CVS	Constant-Voltage Stress
EOT	Equivalent Oxide Thickness
FN	Fowler-Nordheim
ITRS	International Technology Roadmap for Semiconductors
IV	Current-Voltage
MBE	Molecular Beam Epitaxy
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
PDA	Post Deposition Anneal
PF	Poole-Frenkel
PLD	Pulsed Laser Deposition
PMA	Post Metallization Anneal
RHEED	Reflection High Energy Electron Diffraction
RTA	Rapid Thermal Anneal
RTP	Rapid Thermal Processing
SIA	Semiconductor Industries Association

List of Abbreviations

SILC	Stress-Induced Leakage Current
SOI	Silicon-on-Insulator
TDDDB	Time-Dependent Dielectric Breakdown
TEM	Transmission Electron Microscopy
VLSI	Very-Large-Scale-Integration
UHV	Ultra-High Vacuum
ULSI	Ultra-Large-Scale-Integration
XPS	X-Ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction

CHAPTER ONE

INTRODUCTION

1.1 Motivation

In the past three decades, the semiconductor industry has grown continuously by offering higher speed and function of the circuitry. This success is mainly achieved by reducing the dimension of the key component of the integrated circuit (IC): silicon-based metal-oxide-semiconductor field-effect transistor (MOSFET) [1-9]. The scaling of MOSFET is generally governed by the Moore's law, which predicts that the number of components per IC doubles every 18 months [10-12].

Throughout the history of the semiconductor industry, many critical challenges have to be overcome in order to shrink the sizes of the transistors has required. With the development of new lithography tools, masks and photoresist materials, the MOSFET has been scaled continuously for more than three decades. Several forms of scaling such as constant field and constant voltage scaling can be found [13]. However

recently, the requirements outlined by the International Technology Roadmap for Semiconductors (ITRS) indicate that there are no existing solutions for several critical technologies [12]. In particular, the traditional transistor and capacitor formation materials, silicon, silicon dioxide, and polysilicon have been pushed to the fundamental physical limits [14-19, 36-51]. Therefore, new materials and technologies are required to be introduced in the near future to maintain the Moore's law [20-31].

1.1.1 High- k gate dielectrics

One of the critical issues for MOSFET scaling is silicon dioxide. Because of its desirable amorphous structure, large bandgap, compatibility with silicon, low interface state densities and excellent reliability properties, silicon dioxide has been used as the gate dielectric for more than 30 years [32-37, 52-88]. The rapid scaling trend of CMOS technology has resulted in the reduction of gate dielectric thickness to 1.2 nm for currently-used high performance logic devices [24]. However, the use of ultrathin silicon dioxide gives rise to a number of problems. For example, the direct tunneling is dominant in the gate conduction at such dimensions and the leakage current shows an exponential increase as the thickness is reduced. At a gate bias of 1V, the leakage current changes from 1×10^{-12} A/cm² at 3.5 nm to 10 A/cm² at 1.5 nm and above 100 A/cm² at 1.2 nm, levels unsuitable for IC applications [19, 23].

Considering the intrinsic limitations of ultrathin silicon dioxide, the search for an alternative high- k gate dielectric has begun recently. The increase of k value allows a thicker dielectric to be implemented to maintain the performance of silicon dioxide as well as alleviate its critical problems such as large direct tunneling currents [23]. In the current 90 nm technology, silicon oxynitride ($k = 5\sim 7$) is being used as the gate dielectric [24]. However, it only has a k value slightly larger than silicon dioxide ($k = 3.9$) and thus cannot be continuously scaled as suggested by the ITRS roadmap [12, 24]. Therefore, many potential candidates with higher- k value for gate dielectric application have been extensively studied, such as Ta_2O_5 [89-103], TiO_2 [104-110], Y_2O_3 [111-117], CeO_2 [118-121], Al_2O_3 [122-132], ZrO_2 [133-146], HfO_2 [147-168], HfAlO_3 [169-172] and Hf, Zr silicates [173-180].

Among all the high- k materials listed above, HfO_2 -based gate dielectrics such as hafnium oxide, hafnium silicate and hafnium silicon oxynitride are the most promising candidates which generally have large k value and bandgap, good thermal stability and interfacial properties with Si, and long lifetime. Laser-MBE is an emerging thin film deposition tool which benefits from the intrinsic advantages of pulsed laser deposition (PLD) such as producing a variety of high melting-point materials and multi-component films under quite simple process. Besides, Laser-MBE also inherits the merits of conventional MBE such as ease to deposit films with smooth surfaces and interfaces. To our knowledge, there are few reports on Laser-MBE fabricated

HfO₂-based gate dielectrics. Therefore, it is very worthwhile to explore the microstructural, elemental, dielectric and electrical properties of Laser-MBE fabricated HfO₂-based gate dielectrics. It will have great significance for both scientific understanding and technological application.

1.1.2 Metal gate

For gate electrode materials, polysilicon is known to be compatible with high temperature processing and interfaces very well with thermal SiO₂. As a gate electrode, it has also been proven to be more reliable than Al. However, as the gate oxide is scaled to the ultrathin region (< 2 nm), the penetration of boron dopant into and through the gate oxide of pMOS devices has become a serious problem which will deteriorate the device performance [44-46]. Besides the boron penetration, polysilicon depletion also occurs as the device scaling which will cause the reduction of the gate capacitance in inversion. In addition, for the introduction of high-*k* dielectrics into future CMOS platforms, the compatibility of dielectric layer with polysilicon gate electrodes is very important. However, poor leakage behavior, yield reduction, and threshold voltage instability for high-*k*/polysilicon devices have been reported [23]. Therefore, the latest 2005 ITRS roadmap suggests using metal gate electrode to replace the polysilicon gate at 65 nm node and beyond [12, 24].

Many electrode materials with high work function (~ 5 eV) such as Pt, Ru, Ni and RuO_2 are promising candidates for pMOS transistors [24]. RuO_2 , especially, has many additional desirable properties such as good integration with ZrO_2 , Y_2O_3 , and Al_2O_3 high- k dielectrics, good etching property, excellent thermal stability, and inhibition to the oxygen diffusion [267-271]. But so far, to the best of our knowledge, little research work has been done on the electrical properties evaluation of the $\text{RuO}_2/\text{HfO}_2$ gate stack in the literature. Therefore, it is necessary to study RuO_2 for its possible application to replace the polysilicon as metal gate.

1.2 Objectives

In this thesis, the goal is to investigate the HfO_2 -based dielectric thin films for potential gate dielectric applications. These HfO_2 -based dielectric thin films are deposited using the Laser-MBE technique. Then systematic characterizations of physical, chemical, electrical and dielectric properties are investigated, followed by the mechanism studies for deep fundamental understandings.

Firstly, the Laser-MBE system is successfully installed and employed to deposit the hafnium oxide gate dielectric. The influence of the deposition process is systematically studied in order to fabricate the state-of-the-art dielectric thin films. A two-step deposition scheme is adopted as well to further improve the qualities of the resulting films. And the conduction mechanisms of HfO_2 are also discussed. Based on

these studies, the process-dependence of the dielectric thin films performance are expected to extend the understanding of the Laser-MBE-deposited hafnium oxide ultrathin films for the potential high- k microelectronic device applications.

Secondly, the effect of RuO₂ as an alternative top electrode on pMOS RuO₂/HfO₂ devices has been investigated. The prescribed research works include the microstructure, thermal stability, dielectric and electrical studies. It is anticipated that these research works would extend our knowledge on the properties of RuO₂, and in turn afford useful understanding for the applications of RuO₂ as metal gate.

Finally, for the purpose of keeping the gate dielectrics amorphous after high temperature annealing ($> 900\text{ }^{\circ}\text{C}$) and suppressing the interface growth more effectively, silicon and nitrogen are incorporated into the hafnium oxide. High resolution transmission electron microscopy (HRTEM) is intensively employed to investigate directly the interface growth. The electrical and dielectric measurements are used to illustrate the effectiveness of the incorporations. Based on these investigations, the thermal stability and scaling limit of these gate dielectrics can be well determined and discussed.

1.3 Major contributions of the thesis

The major contributions achieved in this thesis are summarized as follows:

1. The Laser-MBE system has been successfully set up and calibrated. More than 100 layers of SrTiO_3 have been epitaxially deposited on the SrTiO_3 substrate suggesting that Laser-MBE is capable of precisely controlling the growth of oxide thin films in a layer-by-layer mode.
2. RHEED has been used as a surface characterization tool for silicon surface prior to the gate oxide deposition. The silicon surface condition, such as the surface roughness and the existence of native oxide, can be well determined from the RHEED diffraction pattern.
3. It has been found that for the HfO_2 deposition, by lowering the oxygen partial pressure to an optimized level, the growth of the low- k interfacial layer can be effectively suppressed. A two-step deposition method has been adopted to further reduce the thickness of this interface layer. The interfacial reaction is better controlled by using this two-step deposition method, resulting in high quality ultrathin HfO_2 films on Si with desired and improved dielectric properties.
4. The conduction mechanisms in the HfO_2 gate dielectric have been systematically investigated, and it is found that the Schottky model is the main conduction mechanism at low electric field of $E < 1 \text{ MV/cm}$; the PF conduction mechanism is dominant in the medium field range of $1 \text{ MV/cm} < E < 4 \text{ MV/cm}$; with further increasing electrical field into the high region of $4 \text{ MV/cm} < E < 6 \text{ MV/cm}$, the current behavior turns to the FN tunneling conduction.

5. RuO₂ has been deposited by RF sputtering and investigated as an alternative gate electrode for pMOS devices. The RuO₂/HfO₂/n-Si capacitors show negligible flat band voltage shift (<10 mV), very strong breakdown strength (>10 MVcm⁻¹). Compared to the SiO₂ dielectric with the same EOT value, RuO₂/HfO₂/n-Si capacitors exhibit at least 4 orders of leakage current density reduction. The work function value of the RuO₂ top electrode is calculated to be about 5.0 eV by two methods, and the effective fixed oxide charge density is determined to be 3.3×10^{12} cm⁻². All the results above indicate that RuO₂ is a promising alternative gate electrode for Laser-MBE grown HfO₂ gate dielectrics.
6. By incorporation of an optimized concentration of Si into HfO₂, the hafnium silicate shows improved electrical and dielectric properties compared with hafnium oxide of the same thickness. HRTEM results show that even after RTA at 950 °C in N₂ for 30 seconds, the 3-nm thick Hf_{0.23}Si_{0.12}O_{0.65} film is still in amorphous state and no obvious interface exists in between Hf_{0.23}Si_{0.12}O_{0.65}/Si.
7. By incorporating nitrogen into the hafnium silicate film, it has been found that the resulting HfSiON is still in amorphous state after RTA at 950 °C in N₂ for 30 seconds and the electrical and dielectric properties of this HfSiON gate stack are further improved. High quality HfSiON film has been obtained with an equivalent oxide thickness (EOT) value of about 0.95 nm as well as low leakage current density. Therefore, HfSiON is a promising candidate for gate dielectric application.

8. Both the HRTEM results and CV measurement indicate that further scaling the HfSiON thickness below 1.5 nm does not contribute to the reduction of EOT, suggesting that under the current deposition scheme, 0.95 nm (EOT) is the scaling limit for Laser-MBE-deposited HfSiON gate dielectrics.

1.4 Organization of the thesis

This thesis has studied HfO₂-based high- k dielectric thin films for potential microelectronic device applications, and is organized into seven chapters.

Chapter 1 provides a general introduction to the state-of-the-art on the high- k materials and electronic devices. The motivations for developing HfO₂-based high- k dielectric thin films and RuO₂ gate electrode are explained. Then, the objectives, major contributions, and organization of the thesis are presented.

Chapter 2 devotes to the fundamental background and related literature review with respect to the applications of high- k dielectric materials. First, the brief history of MOSFET is reviewed. Next, the traditional scaling methodologies, the need for the equivalent scaling solution and potential new transistor design are introduced. Then, the fundamental physical limits for ultrathin SiO₂ are discussed. After that, the present status of the high- k dielectric thin film development is summarized, followed by the

introduction of our considerations of these dielectrics. Finally, the conduction mechanisms in gate dielectrics are discussed.

Chapter 3 describes the installation of Laser-MBE system. First, the basic working principles of PLD are introduced. Next, the theories behind the RHEED diffraction pattern and oscillation are explained. In the third part, the history and fundamentals of Laser-MBE are briefly described. And the detailed description of our Laser-MBE system is given in the fourth part. Finally, some experimental results are discussed such as the observation of epitaxial growth and investigation of the silicon surface condition

Chapter 4 gives the detailed experimental procedures used in this research project, including the fabrication and characterization of the MOS capacitors. The first part describes the silicon substrate preparation process. Next, the experimental parameters for the gate oxide deposition are given, followed by the fabrication of the gate electrode for electrical and dielectric measurements. Finally, the instruments for characterizing properties of HfO₂-based thin films are presented.

Chapter 5 presents the details of the microstructural, chemical and physical properties of the obtained hafnium oxide thin films. The influence of the oxygen partial pressure and the two-step deposition scheme on the HfO₂ film properties is firstly discussed.

Then, the current conduction mechanisms in HfO_2 are systematically studied, followed by the investigation of the breakdown and reliability issues of HfO_2 gate dielectric. Finally, RuO_2 is deposited on HfO_2 and intensively studied as a possible candidate for metal gate application.

In Chapter 6, HfSiO and HfSiON are deposited by adding silicon and nitrogen into the HfO_2 dielectrics. In the first part, the fabrication details of hafnium silicate are given. The concentration ratio of Si in hafnium silicate is properly adjusted in order to achieve the desirable properties. Next, the thermal stability, electrical and dielectric properties of hafnium silicate are presented. Finally, based on the hafnium silicate, nitrogen is further incorporated and the resulting HfSiON has been characterized and compared with HfSiO .

Finally, the conclusion from this work and recommendations for future work are given in Chapter 7.

CHAPTER TWO

LITERATURE REVIEW

In this chapter, the fundamental knowledge and related literature review with respect to high- k gate dielectric materials and conduction phenomena are presented. This chapter serves to provide the related background of the research work on the high- k dielectric materials for semiconductor device applications and consists of five sections. The first section gives the brief history of the MOSFET. Then the traditional scaling methodologies for CMOS devices are introduced in the second section. In the third part, issues related to the ultrathin SiO₂ gate dielectrics are discussed. After that, the considerations on high- k materials properties for gate dielectric applications are presented and the materials studied in this research work are introduced. Finally, the basic principles of the conduction phenomena in the gate dielectric materials are discussed.

2.1 Brief history of MOSFET

The integration of semiconductor devices has gone through small-scale integration (SSI), medium-scale integration (MSI), large-scale integration (LSI) and very-large-scale integration (VLSI). Since beginning in 1990, the semiconductor industry has entered the ultra-large-scale integration (ULSI) era with 10 million or more devices per chip. And it is expected that this trend towards higher integration levels will continue at least to year 2020. By then, the most advanced chip will contain more than 1 trillion (10^{12}) devices.

At each stage of evolution, limits were reached and then surpassed subsequently. But now it seems to be in serious danger. Fundamental physical limits are being reached in many critical areas. And unless new, innovative solutions are found, the current rate of improvement cannot be maintained.

Compared to all the other semiconductor electronic devices, silicon-based MOSFET is of dominant importance because of its low power dissipation, high yield and many significant advantages in device miniaturization. MOSFET serves as a basic component for many key devices such as the complementary metal oxide semiconductor (CMOS), the static random access memory (SRAM), and the dynamic random access memory (DRAM).

Figure 2-1 shows the cross section of a typical MOSFET which mainly consists of a source, drain, channel, and gate region. The transistor acts as a digital switch that is turned on or off by applying a voltage to the gate.

Figure 2-1 Cross section of a typical MOS transistor. [14]

The concept of MOSFET structure was proposed and patented independently by Lilienfeld [2] and by Heil [3] in 1930s. However, there was little understanding of the physical phenomena involved, and practical means were not available for implementing these concepts at that time. In 1948, an unequivocal demonstration of the field effect was made in the classic paper “Modulation of conductance of thin films of semi-conductors by surface charges” by Shockley and Pearson [4]. In 1960, Atalla proposed that thermally grown SiO_2 on silicon single crystal surfaces should be used as the gate insulator [5]. And since then, SiO_2 has been used as the primary gate

dielectric material in field-effect devices. In the same year, Kahng and Atalla at Bell Labs fabricated the first enhancement-mode MOSFET which has a channel length of $25\ \mu\text{m}$ and a thermally-grown SiO_2 with the thickness of about $100\ \text{nm}$ [6].

In 1963, Grove, Deal and Snow developed the first commercially usable process for the construction of MOSFETs with stable characteristics [7]. In their developed process, sodium levels were minimized by scrupulous care and cleanliness in every critical process step [7]. The next key step to commercialization was the development of CMOS devices which was proposed by Wanlass and Sah in 1963 [8]. The circuitry based on CMOS structure shrank the stand-by power consumption significantly, reduced the device overlap capacitance and improved frequency performance dramatically. By 1968, both CMOS structure and polysilicon gate technology had been successfully developed [9]. From then on, CMOS has dominated in semiconductor devices.

Since the beginning of the microelectronics era, the minimum feature length of an integrated circuit has been continuously reduced. At the birth of MOSFET, channel length, a critical feature of MOSFET, was on the scale of $100\ \mu\text{m}$. However, in 2006, the channel length is about $90\ \text{nm}$ which is scaled over 1000 times. By reducing the size of the device, the switching speed of the MOS transistor has been increased continuously for more than 30 years [1]. There are no better words to describe this

phenomenon than the famous Moore's law. In 1965, Moore observed that the complexity for minimum component had increased at a rate of roughly a factor of two per year in his famous paper entitled "Cramming more components onto integrated circuits" [10]. This observation became known as Moore's Law which was later amended to that the number of components per IC doubles every 18 months. Besides the growth of the density of the circuitry, the speed and function of circuitry have also grown at roughly the same rate. Moore's Law also means decreasing cost. As silicon-based components and platform ingredients gain in performance, they become exponentially cheaper to produce, and therefore more plentiful, more powerful, and more seamlessly integrated into our daily lives.

Figure 2-2 shows the exponential increase of the Intel microprocessor computational power [11]. The computational power increases by a factor of 2 every 18 months.

Figure 2-2 Exponential increase of microprocessor computational power versus year. [11]

2.2 CMOS device scaling

As discussed in the Moore's Law, scaling of semiconductor devices leads to ever smaller dimensions, resulting directly in a constant increase in the number of components per chip. This section will briefly introduce the traditional scaling methodologies, the need for the equivalent scaling solution, and the potential new transistor design.

2.2.1 Traditional scaling

The reduction of the dimensions of a MOSFET has been dramatic during the last three decades. Starting at a minimum feature length of 10 μm in 1970 the gate length was gradually reduced to 32 nm minimum feature size in 2005, resulting in a 13% reduction per year [12]. Proper scaling of MOSFET however requires not only a size reduction of the gate length and width, it also requires a reduction of all other dimensions including the gate/source and gate/drain alignment, the oxide thickness and the depletion layer widths [1]. Scaling of the depletion layer widths also implies scaling of the substrate doping density.

Two types of scaling are common: constant field scaling and constant voltage scaling. Constant field scaling requires all vertical and lateral dimensions to be scaled simultaneously [1]. So both the length of the channel and the thickness of the gate oxide should be scaled. And also as supply voltages are scaled with each generation,

the oxide thickness must be scaled to maintain the same maximum electric field as applied on the original device. The circuit speed increases from several sources: the reduction in the voltage swing, the reduction in the capacitance that must be driven due to the smaller device sizes, and the reduced wire capacitance due to the decreased distance between devices. Constant field scaling yields the largest reduction in the power-delay product of a single transistor. And it is an elegant approach to reduce the short-channel effects by maintaining the internal electric field as same as that of a long-channel MOSFET [36]. However, it requires a reduction in the power supply voltage during the scaling which is not practical when the circuit is interfaced with other devices.

Constant voltage scaling does not have this voltage reduction problem since it provides voltage compatibility with other circuit technologies. As the supply voltage is not scaled down, it produces more speed improvement than the constant field method. The disadvantage of constant voltage scaling is that the electric field increases as the minimum feature length is reduced. This leads to velocity saturation, mobility degradation, increased leakage current and lower breakdown voltage.

The scaling of MOSFET device parameters is illustrated by Table 2-1 where constant field, constant voltage and constant voltage scaling in the presence of velocity saturation are compared [13].

Table 2-1 Comparison of the effect of scaling on MOSFET device parameters ($\kappa > 1$).

Parameter	Symbol	Constant Field Scaling	Constant Voltage Scaling
Gate length	L	$1/\kappa$	$1/\kappa$
Gate width	W	$1/\kappa$	$1/\kappa$
Field	ε	1	κ
Oxide thickness	t_{ox}	$1/\kappa$	$1/\kappa$
Substrate doping	N_a	κ^2	κ^2
Gate capacitance	C_G	$1/\kappa$	$1/\kappa$
Oxide capacitance	C_{ox}	κ	κ
Transit time	t_T	$1/\kappa^2$	$1/\kappa^2$
Transit frequency	f_T	κ	κ^2
Voltage	V	$1/\kappa$	1
Current	I	$1/\kappa$	κ
Power	P	$1/\kappa^2$	κ
Power delay	$P\Delta T$	$1/\kappa^3$	$1/\kappa$

2.2.2 Fundamental limits of traditional scaling

It should be noted that it is the rapid development of new lithography tools, masks, and photoresist materials that has propelled the unprecedented gains in productivity and performance in the traditional scaling methodologies. However, in recent years, people have begun to realize that this scaling trend is facing some fundamental limitations [14].

2.2.2.1 Solid solubility

One of the limitations is the solid solubility of different doping atoms. The dopant concentrations in MOS transistors have increased more than 100-fold over the past 20 years and are on the order of 1% of the silicon lattice density for current device technologies. The maximum thermodynamically stable concentration of atoms in silicon, or solid solubility, varies for different doping atoms. It is a fundamental thermodynamic property and is not dependent on the method of incorporation of the dopants. Above the solid solubility limit, the doping atoms begin to interact with each other as a result of electrochemical interactions and the strain fields caused by the atomic size mismatch of the doping atoms and the silicon lattice. This leads to the formation of clusters of dopants, which are not located on silicon lattice sites and do not increase the mobile charge density [15].

Unfortunately, the charge concentrations needed for current process technologies are at the solid solubility limit for the doping atoms currently in use. New dopants have been evaluated, but none has yet been found to create higher concentrations of mobile charge. Thus, unless new methods are developed, future scaling of the transistor will result in a loss of total charge, an increase in resistance, and a potential decrease in performance.

2.2.2.2 Statistical fluctuation

Besides the solubility issue, statistical fluctuation is also a potentially fundamental limit for continued transistor scaling [16]. The transistor dimensions have become so small that the number of doping atoms that control the electrical characteristics is on the order of a hundred. Unless ways for reducing statistical variation are found, it may not be possible to scale dimensions to the point where tens of atoms determine the device characteristics.

2.2.2.3 Gate oxide scaling

Gate oxide scaling is facing an equally critical fundamental limit. Within the last few technology generations, the silicon dioxide layer has become so thin that quantum mechanical tunneling of electrons from the silicon substrate to the gate electrode is now possible [17, 38]. The probability of an electron tunneling through a potential barrier depends exponentially on the thickness and potential energy of the barrier which ultimately cannot be mitigated by improvement in the quality of a given dielectric material [18]. This results in a real limit to the minimum useful dielectric thickness for SiO₂, as indicated in Figure 2-3 [19].

From the above discussion, it is clearly noted that the materials constituting the building block of traditional CMOS transistors such as silicon, silicon dioxide, polysilicon, have been pushed to the fundamental physical limits. These fundamental

issues have not previously limited the scaling of transistors and represent a considerable challenge for the semiconductor industry. In order to continue the performance trends of the past 20 years and maintain the Moore's law of improvement, new materials and technologies should be introduced. This trend is called equivalent scaling.

Figure 2-3 Gate leakage density versus gate voltage for various oxide thicknesses. [19]

2.2.3 Equivalent scaling

2.2.3.1 Shallow junction

Reducing the source and drain junction depth is an effective way to suppress short channel effects since it leads to a longer effective channel length for a given gate length [20]. Traditional scaling technology is ultrashallow junction scaling which will

drive implantation energies to ultra-low energies of 200-500 eV. Such a change requires fundamental redesign of existing high-current beam line implanters to reduce energy contamination and improve productivity. However, by using equivalent scaling, this redesign problem can be avoided [21,22]. For instant, in p-type doping, a change to a higher-mass dopant species from boron to $B_{10}H_{14}$ or $B_{18}H_{22}$ increases the effective energy and beam current by a factor of 10 to 20.

2.2.3.2 Channel engineering

The scaling theory requires not only scaling of the supply voltage but also increasing the channel impurity concentration. This theory leads to an unscaled threshold voltage, which results in a reduced drain current. In order to avoid the trade-off between immunity of short-channel effects and low threshold voltage, we must optimize the channel impurity profile two-dimensionally. The lateral profile with a high peak concentration is implemented by angled ion implantation after patterning the gate [21]. This design extends CMOS scaling to the low threshold voltage and strong immunity to short-channel effects.

2.2.3.3 Strained silicon

Strained Si technology enables channel mobility improvements via replacement of the bulk, cubic-crystal Si substrate with a Si substrate that contains a tetragonally-distorted, biaxial strained Si thin film at the surface. Due to changes in its crystalline

structure (i.e. its symmetry is different due to its strain state), the strained Si film has electronic properties that are superior to those of bulk Si. Specifically, the strained Si film has greater electron and hole mobility, which translate into greater drive current capabilities for NMOS and PMOS transistors, respectively. This increased transistor drive current can be traded off for a reduction of dynamic power consumption.

2.2.3.4 Gate stack engineering

Scaling of the gate oxide thickness has already approached a limit because of the increase of direct tunneling current through the thin SiO₂ gate insulator [23]. From the 2005 ITRS, the targeted EOT and gate leakages (I_g) for high performance (HP), low operating power (LOP), and low standby power (LSTP) logic devices are listed in Table 2-2 for the technology nodes from 90 to 22 nm [24].

Table 2-2 Gate leakage roadmap. [24]

Technology node (nm)	LOP		LSTP		HP	
	EOT (nm)	I_g (A/cm ²)	EOT (nm)	I_g (A/cm ²)	EOT (nm)	I_g (A/cm ²)
90	1.5	1.89	2.1	5.1×10^{-3}	1.2	4.5×10^2
65	1.2	5.21	1.6	2.3×10^{-3}	0.9	9.3×10^2
45	0.9	11	1.3	0.08	0.7	1.9×10^3
32	0.8	21	1.1	0.15	0.6	7.7×10^3
22	0.7	91	1	0.26	0.5	1.9×10^4

The semiconductor industry has already switched from pure SiO₂ gate dielectric to lightly nitrated oxides for logic devices as the gate thickness scaled below 2.2 nm at the 180 nm node. Heavily nitrogen-doped silicon dioxide increases the k value from SiO₂ ($k=3.9$) toward Si₃N₄ ($k=7.8$) and reduces gate leakage [25]. Precise interfacial layer control and film compositional control are needed to extend SiON layers with high nitrogen content to 90 nm node HP logic devices. However, Bohr of Intel has reported recently that from 90 nm to 65 nm node, Intel will not scale its SiON gate below an EOT of 1.2 nm due to the large gate leakage current density of about 100 A/cm² [26]. And high- k gate dielectrics are needed to be introduced at the 65 nm node to overcome the physical limits of SiO₂.

2.2.4 Emerging device structure

The scaling of CMOS is rapidly approaching fundamental limits imposed by discrete atomic dimensions of critical materials and the quantum effects in conventional MOSFET structures. A broad array of new materials integrated into both conventional and new MOSFET device structures is being explored and developed to extend CMOS technology to its ultimate limit over the next 10-15 years.

Following the recent introduction of strained silicon into the channel of the MOSFET, new materials in R&D are focused on completely replacing conventional SiO₂/Poly-Si gate stacks in CMOS transistors with new high- k gate dielectrics and metal

gate electrodes. In addition to these materials, many new device structures have been developed. IBM is using Silicon-on-Insulator (SOI) technology to enhance CMOS performance [27]. SOI differs from typical CMOS in that its silicon junction is above an electrical insulator. The advantage is that this insulator reduces the capacitance. It means that the transistor has less to charge-up before completing a switch, which results in a reduced switching time. SOI devices are usually inherently latchup resistant. Also, there is a reduction in transistor leakage current thereby making this fabrication technology an attractive choice for low power circuit design. Many other structures such as double-gate transistor [28], tri-gate transistor [29], Fin-FET [30], are still under development to achieve the best performance. The newly completed 2005 ITRS roadmap concludes that highly innovative changes will be needed to extend more-or-less conventional CMOS technology down to the 22 nm technology node [24, 31].

2.3 Ultrathin SiO₂ gate dielectric issues

Silicon dioxide has been used as the primary gate dielectric material in field-effect devices since 1957, when the usefulness of the Si/SiO₂ material system was first demonstrated [32-35]. The reason for the nearly exclusive use of SiO₂ in this application is that SiO₂ uniquely possesses the required combination of several properties: good mobility of both holes and electrons flowing in silicon at the SiO₂ interface, ability to keep low interface electronic states, relatively low trapping rates of

holes and electrons, and excellent compatibility with CMOS processing [36, 37]. And now, with the trend of scaling, the SiO₂ thickness is less than 1.2 nm for HP logic devices [24]. The recent roadmap of ITRS (Table 2-2) clearly indicates that the thickness still needs be reduced. However within the last few technology generations, the fundamental physical limits to the scaling of the SiO₂ has emerged which are discussed as follows:

2.3.1 Short-channel effects

Scaling down of the channel length (L) improves the driving current ($I_D \sim 1/L$) and, thus the operation performance. However, with a shortened channel length, the gate faces a much stronger influence from the source, drain and isolation edge than that in the device with a longer channel. The device characteristics, therefore, deviate from those derived from the long-channel approximation [36].

When the channel side effect becomes non-negligible, the threshold voltage decreases as the channel length reduces. When the distance between the source and drain is comparable to the depletion width of the source or drain, the space-charge region will take a significant part of the channel region. In this case, the MOSFET needs fewer carriers to invert the channel, which results in a lower threshold voltage. In the extreme case, as the increase of drain voltage, the depletion region of the drain junction merges with that of the source junction. As a result, the carriers can move

freely between source and drain without an inverted channel. A large leakage current may flow from the drain to the source through the bulk. This is called bulk punch-through. Consequently, the gate can no longer turn the device completely off and loses control of the drain current.

2.3.2 Direct tunneling leakage current

For a large number of dielectrics, the tunneling current is exponentially dependent upon the dielectric thickness [36, 38] as shown in following equation (2-1):

$$J = \frac{A}{d^2} \exp\left(-2d\sqrt{\frac{2m^*q}{\hbar^2}\left\{\Phi_B - \frac{V}{2}\right\}}\right) \quad (2-1)$$

here A is a constant, d is the physical thickness of the dielectric, m^* is the electron effective mass in the dielectric, Φ_B is the potential barrier between the metal and dielectric, and V is the voltage drop across the dielectric.

It is clearly seen that the tunneling leakage current increases exponentially with the decrease of the SiO₂ thickness. For extremely thin oxides ($d < 1.5$ nm), direct tunneling occurs between gate metal and interface trap levels when the Fermi level in the gate is opposite to the silicon bandgap. The resulting large tunnel current strongly couples interface trap levels to the Fermi level in the gate. Every 0.5 nm reduction of the SiO₂ thickness can result in about two orders of magnitude increase of the tunneling leakage current. However, at slightly thicker oxide thickness (~ 3 nm), direct tunneling is greatly reduced [38].

Such high tunneling current causes several serious consequences. First, it creates intolerably high power consumption for both low-power and high-power logic applications. Second, SiO_2 is no longer acting as an effective insulator with such a small thickness. It can no longer hold the channel carriers and thus a big portion of the channel carriers transports through SiO_2 to the gate of MOSFET instead of conducting between the source and drain. Third, it has been shown that due to the voltage drop in the gate electrode, the statistical distribution of direct tunneling leakage current causes significant fluctuations in threshold voltage when the gate oxide tunneling resistance becomes comparable to gate electrode resistance [39, 40]. When the threshold voltage fluctuations are large enough, it will cause failure of the device.

The transistors with SiO_2 gate oxides as thin as 1.3-1.5 nm continue to operate satisfactorily [41, 42], although high leakage current densities of 1-10 A/cm^2 are measured for such devices [43]. However, Timp et al. reported that scaling of CMOS structures with SiO_2 gate oxides thinner than about 1.2 nm results in no further gains in transistor drive current [42]. And SiON seems to be only a short-term replacement for SiO_2 and will reach its physical limit by the end of 2006 [26]. Alternative high- k gate dielectrics must be used in the near future [12, 24].

2.3.3 Boron penetration

In addition to the gate oxide, the polysilicon gate electrode is also a critical part of the gate stack. Currently, heavily doped polysilicon is used as the electrode for ease of fabricating source and drain regions self-aligned to the etched gate. As the gate oxide is scaled to the ultrathin region, the penetration of boron dopant into and through the gate oxide of pMOS devices has become a serious problem [44-46].

The dopant for p-polysilicon gate, boron or boron difluoride (BF_2), can diffuse rapidly into the silicon channel region upon thermal annealing, which results in a large positive shift in threshold voltage, increased PMOS subthreshold slope and electron trapping rate, and decreased low-field mobility and interface trap density [44]. Therefore, it will alter the intended device properties in an unacceptable way [44, 47].

In order to solve this diffusion problem, researchers have found that the addition of nitrogen to SiO_2 significantly reduces boron diffusion through the dielectric and improves device performance [48, 49]. However, large amounts of nitrogen doped into the SiO_2 resulted in poor pMOS performance with significant degradation of channel mobility and drive current [50]. Therefore, as the boron penetration mainly worsens to the thinner gate oxide, a thicker gate oxide with higher k value should be employed to overcome this fundamental limitation [23].

2.3.4 Polysilicon depletion

The doped polysilicon gates offer the desired workfunction for scaled threshold voltage [51]. However, it is well known that with the gate dielectric scaling and the reduction of the effective polysilicon doping concentration, the gate capacitance in inversion will be reduced. This degradation is attributed to the formation of a depletion layer near the polysilicon/SiO₂ interface and is often referred to as polysilicon depletion. If the polysilicon doping density could be increased without limit, the depletion effect could be minimized. However, in practice, polysilicon can only be doped to 10^{19} - 10^{20} cm⁻³ which results in a significant degradation in current drive capability and unacceptable transconductance of the transistors.

The current technology trend to solve this critical problem is to use metal gate electrodes to replace the traditional polysilicon gate at 65 nm node and beyond [12, 24].

2.3.5 SiO₂ reliability

Gate oxide reliability has been an extremely important concern in the semiconductor industry [52-89]. Traditionally, there are two distinct types of breakdown: defect-related and intrinsic breakdown. Defect-related breakdown has been well studied. The breakdown is dominated by the defects in the underlying substrate [66-70], by additional impurities in the oxide [71-81], by the surface roughness

[82-88], etc. The requirements for the continuous scaling of the gate oxide have pushed the industry to concentrate on the defect-related breakdown. We are now capable of fabricating devices with fewer defects and higher reliability. Therefore, the intrinsic breakdown mechanism generally dominates the thick SiO₂ reliability.

However, with respect to the films thinner than 5 nm, the breakdown mechanism is fundamentally different because several defect generation processes are triggered as the high current flows across the dielectrics. As the leakage current density increases dramatically with the scaling of gate oxide thickness, the ultrathin SiO₂ no longer works as a good insulator. Therefore, the SiO₂ reliability limit has been drastically reduced.

2.4 Alternative high-*k* gate dielectrics

For a given technology, CMOS devices are designed with a specific gate capacitance, which is proportional to the dielectric constant and inversely proportional to the thickness of the gate material as shown in equation (2-2). The gate leakage current, at least for direct quantum mechanical tunneling, is exponentially dependent upon the dielectric thickness. Therefore, for the purpose of maintaining the same gate capacitance as well as reducing the leakage, a thicker film with a higher dielectric constant is required to replace the SiO₂.

$$C_{gate} = \frac{3.9 \cdot S}{t_{SiO_2}} = \frac{\epsilon_{high-k} \cdot S}{t_{high-k}} \quad (2-2)$$

Here C_{gate} is the gate capacitance, S is the area of the gate capacitor and t_{SiO_2} , t_{high-k} represents the thickness of SiO_2 and high- k material respectively.

According to the latest ITRS roadmap, high- k gate dielectric will be needed by 2008 to meet the scaling goals and at the same time to keep the gate leakage within tolerable limits. A potential roadmap for the alternative gate dielectric films is given in Figure 2-4 [24].

Figure 2-4 DRAM potential solutions. [24]

Many materials have been suggested that could replace silicon dioxide or silicon oxynitride as a possible gate dielectric. The most common of these are the simple metal oxides such as Ta_2O_5 [89-103], TiO_2 [104-110], Y_2O_3 [111-117], CeO_2 [118-121], Al_2O_3 [122-132], ZrO_2 [133-146], HfO_2 [147-168], $HfAlO_3$ [169-172] and the metal silicates, such as the Hf, Zr silicates [173-180]. Following are the primary

considerations of the appropriate materials properties on the selection of materials for the gate dielectric application.

2.4.1 Barrier height

The gate leakage current is exponentially dependent upon the dielectric thickness as well as the barrier height between the cathode and the conduction band of the gate oxide. Generally, the tunneling current through the gate oxide can be divided into two regions. In the low electric field region, where the oxide voltage is smaller than the barrier height, direct tunneling occurs and electrons can directly tunnel into the electrode [36]. In the high electric field region, where the oxide voltage is higher than the barrier height, electrons tunnel into the oxide conduction band first, then travel towards the electrode. This process is called Fowler-Nordheim (FN) tunneling [36]. The current transport for direct tunneling and FN tunneling are described by equations (2-3) and (2-4), respectively;

$$J_{DT} = \frac{q^2}{2\pi\hbar t_{ox}^2} \left[\left(\phi_B - \frac{V}{2} \right) \cdot \exp \left(-\frac{4\pi\epsilon_{ox}\sqrt{2m^*}q}{h} \sqrt{\phi_B - \frac{V}{2}} \right) - \left(\phi_B + \frac{V}{2} \right) \cdot \exp \left(-\frac{4\pi\epsilon_{ox}\sqrt{2m^*}q}{h} \sqrt{\phi_B + \frac{V}{2}} \right) \right] \quad (2-3)$$

$$J_{FN} = \frac{q^2}{8\phi_B\pi\hbar} E^2 \cdot \exp \left(-\frac{8\pi\sqrt{2m^*}q\phi_B^{3/2}}{3\hbar E} \right) \quad (2-4)$$

Here, ϕ_B is the barrier height, V is the voltage drop across the dielectric, E is the electric field in the insulator, m^* is the effective mass of an electron and t_{ox} is the thickness of the dielectric.

Moreover, for highly defective films which have electron trap energy levels in the insulator band gap, a trap-assisted mechanism such as the Poole-Frenkel emission or hopping conduction will govern the electron transport [181], as described by equations (2-5) and (2-6), respectively;

$$J_{PF} = E \exp \left(-\frac{q}{kT} \left\{ \Phi_B - \sqrt{\frac{qE}{\pi\epsilon_i}} \right\} \right), \quad (2-5)$$

$$J_{hop} = \frac{q^2 l^2 n^* \Gamma E}{kT}, \quad (2-6)$$

here, l is the interval of separation between adjacent hopping sites, n^* is the density of free electrons in the dielectric, and Γ is the mean hopping frequency.

Therefore, it is clearly noted that besides the increase of dielectric thickness, the dielectric barrier height should be sufficiently large so that the tunneling current can be reduced. In addition, in order to ensure the large barriers for both electrons and holes, the gate oxide bandgap needs to lineup closely with Si midgap. In a general case, one design rule for transistors is that the barriers for both holes and electrons should be larger than 1 eV. Figure 2-5 shows the barrier height of various oxides [182].

It is seen that most high- k materials have lower barrier heights than the barrier height of SiO₂ and the band offsets for most transition metal oxides are quite asymmetric, with barriers for electrons much less than half the oxide band gap. For example, the

Figure 2-5 Calculated conduction band and valence band offsets of various oxides on Si. [182]

Figure 2-6 Relationship between bandgap and permittivity for several commonly studied gate dielectric materials. [183, 184]

electron barriers for Ta₂O₅ and BaTiO₃ are very small which make them unlikely the choices for alternative gate oxide.

For most of the high- k materials, the bandgap is inversely proportional to the dielectric constant, following empirically a $E_g \approx 1/k^2$ law as shown in Figure 2-6 [183, 184]. Due to this relationship, the dielectrics which have very large k values such as SrTiO₃ and (Ba, Sr)TiO₃ are generally not considered as the possible candidates for the gate dielectric application.

Among all the candidates, alumina (Al₂O₃) has the largest bandgap with many favorable properties for the gate application, such as a thermodynamic stability on Si up to high temperatures, and is amorphous under the conditions of interest [122-132]. The biggest drawback is that pure Al₂O₃ has a low k of $\sim 8 - 10$; therefore makes it a relatively short-term solution for industry needs (1 - 2 generations). Considering this trade-off between the band gap and dielectric constant, HfO₂, which has a large dielectric constant around 20 and reasonably high barrier height for both electrons and holes (>1 eV), appears to be the most promising candidate for gate dielectric applications.

2.4.2 Thermodynamic stability on Si

In typical semiconductor device fabrication process, gate stacks are exposed to high temperature (around 1000 °C) RTA. Therefore, an important factor for selection of the

alternative gate dielectrics is its thermal stability in contact with Si and the gate electrode, respectively. This problem was first considered by Hubbard and Schlom who evaluated the thermodynamic stability of a large set of binary oxides (MO_x) in contact with Si [184, 185]. Many intensively researched high- k candidates show good thermal stability in contact with Si such as Al_2O_3 , Y_2O_3 , La_2O_3 , HfO_2 , ZrO_2 , etc. However, most of the high- k metal oxide systems investigated so far form interfaces with Si. These interfacial phases, such as SiO_2 , silicate or silicide, are often observed in high- k gate stacks after the high temperature treatments, as systematically shown in Figure 2-7 [186].

Figure 2-7 Interface phases in high- k gate stacks: (a) SiO_2 layer, (b) silicate layer, (c) silicide layer at the interface with Si substrate, (d) silicide layer at the interface with the poly-Si gate electrode. [186]

The interfacial layer may reduce the interface trap density and the leakage current. And for the purpose of improving device mobility, the growth of a high quality low- k interfacial layer is considered desirable between the Si and the high- k dielectric. However, this underlying layer also severely compromises the capacitance gain from any high- k layers. And the EOT of the gate stack is expressed in equation (2-7).

$$EOT_{total} = \frac{3.9}{\epsilon_{high-k}} t_{high-k} + t_{interface} \quad (2-7)$$

2.4.3 Interface quality

Interface problem is the most critical problem for high- k gate dielectrics nowadays. For all thin gate dielectrics, the interface with Si plays a key role, and in most cases it is the dominant factor in determining the overall electrical properties. One major reason for the industry to delay the high- k gate at 45 nm node is that high- k gate dielectric still cannot create a better interface to Si than that of SiO₂ or SiON. Therefore recently, nearly all the efforts have been dedicated to optimizing the interface for better gate properties.

Many gate oxides such as ZrO₂ and HfO₂ are well known to exhibit high oxygen diffusivities and oxygen can easily penetrate through the dielectric layer to reach the Si surface. As discussed in the previous section, this O₂ diffusion results in the formation of SiO₂-containing interfacial layer which compromises the capacitance gain from the high- k layer. Besides limiting EOT scaling, the interfacial oxide layer also affects channel mobility: reducing the interfacial oxide from 1.2 nm to 0.8 nm thereby reduces mobility by a factor of two from 150 cm²/Vs to 75 cm²/Vs [187]. Therefore, it is a dilemma to choose between a better interface and a smaller EOT.

Several methods have been used to block the oxygen diffusion. Among them, one promising solution is to incorporate an oxygen diffusion barrier to protect the Si surface from oxidation. Kang et al. found that by the incorporation of nitrogen into HfO_2 , the oxygen diffusion has been substantially inhibited [188]. In addition, since Al_2O_3 is a well-known good oxygen diffusion barrier, many researchers have tried to make multicomponent MAl_xO_y ($\text{M}=\text{Hf}, \text{Zr}$) films to take advantages of the Al_2O_3 [124, 171, 189-191]. Recent results indicate that such material system controls the interfacial growth effectively and exhibits encouraging gate properties [171, 190, 191]. Besides the oxygen barrier, hydrogen annealing has also been proven to be an effective method to inhibit the oxygen diffusion. Fakhruddin et al. found that by using in situ hydrogen baking prior to the high- k deposition, the interfacial layer can be totally eliminated [192].

Many high- k gate dielectrics also exhibit a tendency to trap electrons. Most of the charge is being trapped in the interface layers. With charge trapping, the voltage applied at the gate is instead absorbed in the “traps” that mine the channel. It degrades transistor performance by slowing mobility and causing threshold voltage instability. A team from University of Texas at Austin leaded by Lee tackled the problem by incorporating nitrogen in the HfO_2 gate dielectric and by high-temperature forming gas anneal, which increased electron mobility while reducing the boron penetration of the gate oxide [193]. That has allowed them to achieve an ultrathin equivalent oxide

thickness of 0.7 nm. Even with a 0.7-nm-thin gate oxide, mobility is still too low compared with silicon dioxide. To boost capacitance, this team has tried a hydrogen-based forming gas anneal at temperatures ranging from 500°C to 600°C, rather than the standard 400°C. With the use of hydrogen, the charge traps are reduced because the hydrogen ions fill dangling bonds at the interfacial layer and in the dielectric. That yields substantial improvements in rooting out traps in the dielectrics and therefore the increase of the mobility.

In Nov. 2005, Hsing-Huang Tseng and his team from Freescale Semiconductor Inc. announced that the defects in the hafnium oxide layer could be passivated by implanting fluorine into the gate stack [194, 195]. Tseng said his team created NMOS transistors with a thin layer of amorphous silicon on top of a tantalum carbide metal gate electrode. The electrode was above a hafnium dioxide layer. After the source and drain were annealed, fluorine was diffused into the gate stack using implant techniques. Since fluorine has a strong propensity to bond with silicon, it will reduce silicon's ability to attract oxygen in the bulk oxide layer, or in the interface layer. T.P. Ma at Yale University suggested that fluorine is the best means of creating "high- k interfaces that are as good as what we have with SiO_2 " [195].

Besides the MO_x/Si interface, the poly-Si/ MO_x interface is of the same importance and should also be considered. Capping layers have been proven to have a significant

effect on scaling by suppressing reactions between the gate dielectric and the gate electrode. Depositing CVD silicon gates directly onto Al_2O_3 capped HfO_2 showed greater than a 10^4 times reduction in gate leakage compared to the poly-Si/ HfO_2 with control of similar electrical thickness [196]. The addition of an HfSi_xO_y capping layer to HfO_2 films has resulted in an EOT reduction by as much as 0.4 nm. This improvement is most likely due to a reduction in interfacial reactions between the polysilicon electrode and the high- k material [197].

One of the most dramatic effects on scaling comes from the use of metal gate electrodes. In the case of the following evaluation taken by Murto et al., a 10 nm CVD TiN layer was deposited prior to the polysilicon gate electrode. This resulted not only in a significant reduction in the capacitance equivalent thickness due to elimination of gate depletion, but also in a significant reduction of 0.5 nm in the EOT, due to the elimination of the upper interfacial layer [197].

2.4.4 Film morphology

Given the concerns regarding to polycrystalline and single crystal films, it appears that an amorphous film structure is the ideal one for the gate dielectric.

One of the main problems is that common high- k dielectrics will crystallize at a fairly low temperature (much less than 900°C). Nearly all metal oxides of interest, with the

exception of Al_2O_3 , will form a polycrystalline film either during deposition or upon modest thermal treatments, and HfO_2 and ZrO_2 are not exception. Crystal grain boundaries then can act as high dopant diffusivity paths and may also be the cause of device failure and high leakage. For example, Toshiba announced that crystallized HfO_2 portions strongly degraded the electron mobility in hafnium silicate MOSFETs. And it should be noted that single crystal oxides grown by MBE methods can in principle avoid grain boundaries while providing a good interface, but these materials require submonolayer deposition control, which is not compatible with the current CMOS processing [113, 198].

The good news is that adding nitrogen to the film helps keep the film amorphous at temperatures of up to 700-800°C and also helps increase the dielectric constant, Samsung, for example, found that incorporating nitrogen in hafnium silicate definitely enhanced its dielectric constant. HfSiON was amorphous up to 1100°C and showed a reduction in leakage current by more than three orders of magnitude compared with that of SiO_2 obtained with a nitrogen concentration of 30 % [199]. Researchers said that excellent properties of HfSiON were due to the suppression of crystallization, phase separation and microscopic inhomogeneity of the film, which can be achieved with nitrogen over 20 %. In addition, by controlling the ratio between Si and Hf in hafnium silicate [173] and the ratio between Al and Hf in hafnium aluminate [200], one can increase their crystallization temperature to 900-1000°C.

2.4.5 Gate electrode

Besides finding other suitable high- k gate dielectrics to replace silicon dioxide to meet the challenge in gate scaling, another solution is to switch from a polysilicon gate to a metal gate electrode, which has virtually no depletion, better threshold voltage control and increased mobility.

A significant issue for integrating any advanced gate dielectric into standard CMOS is that the dielectric should be compatible with Si-based gates, rather than require a metal gate. Si-based gates are desirable because dopant implant conditions can be tuned to create the desired threshold voltage for both nMOS and pMOS, and the process integration schemes are well established in industry. However, nearly the entire potential advanced gate dielectrics investigated to this point requires metal gates.

A well-known problem with polysilicon gates is that a depletion region (Figure 2-8) forms not only under the gate, where it's needed, but also on top of the gate which is undesirable. The origin of this gate depletion is the lower concentration of dopant carriers near the gate electrode/dielectric interface (less than 10^{21} carriers per cm^3), which results in a depletion layer under gate inversion conditions. This depleted layer introduces an additional capacitance (0.3-0.4 nm in thickness) which is in series with the gate dielectric. Thus, it has the effect of increasing the gate dielectric thickness.

Furthermore, since the impact of this depleted region increases as the gate oxide capacitance increases, it becomes compulsory to consider metal gates as the gate scaling.

Figure 2-8 (a) The energy band diagram of an nMOS device (b) The poly-Si gate depletion effect. [201]

Besides the problem of polysilicon depletion, reactions between the polysilicon gate and high- k gate dielectrics can produce silicide, which deteriorates the work function and dielectric integrity of the gate stack. With a metal gate, this depletion region in the gate electrode is avoided. Recently, Hobbs et al. have also reported that a polysilicon gate suffers from Fermi level pinning on HfO_2 based dielectrics which limit their usefulness on high- k gate stacks [202]. Therefore, Toshiba announced that metal gates should be integrated with the high- k dielectrics. And according to the ITRS roadmap, the metal gates are still under development and will be ready for production in the near future [24].

Another advantage of the metal gate is that it can improve the mobility of electrons and holes in the channel. For example, for a given EOT, electrons in the TiN gate have a higher mobility than in the polysilicon gate. This is attributed to a decrease in the upper SiO₂-like interface layer, which may have an effect on channel mobility due to remoteness from the channel/dielectric interface [197].

Traditionally, technologists prefer to limit risks by making one material change at a time, moving to copper interconnects at one node, for example, and to low- k dielectrics at the next. For that reason, many companies plan to switch from silicon oxynitride to a high- k gate insulator during the 45 nm node, as early as 2007 [24]. Their next step would be the move to metal gates, replacing the n⁺ and p⁺ doped polysilicon gate electrodes with metallic alloys to eliminate polysilicon depletion at the gate [24]. Specially, metal gates such as TiN and Pt have been used with most of the high- k gate dielectrics. AMD, as announced, will use nickel silicide (NiSi) to replace polysilicon. As an alternative to elemental metals, conducting metal oxides such as IrO₂ and RuO₂, which have been studied for years in DRAM applications, can provide high ϕ_M values in addition to affording the use of standard etching and processing techniques [37].

2.4.6 Process compatibility

A crucial factor in determining the final film quality and properties is the method by which the dielectrics are deposited in a fabrication process. The deposition process for

the dielectric must be compatible with current or future CMOS processing, cost, and throughput. Some methods used are physical vapor deposition (PVD) (e.g. sputtering, pulsed laser deposition, evaporation and MBE) and chemical vapor deposition (CVD) (e.g. metal-organic CVD, atomic-layer CVD).

PVD methods have provided a convenient means to evaluate materials systems for alternate dielectric applications. The damage inherent in a sputter PVD process, however, results in surface damage and thereby creates unwanted interfacial states. Additionally, device morphology inherent to the scaling process generally rules out such line-of-sight PVD deposition approaches. For this reason, CVD methods have proven to be quite successful in providing uniform coverage over complicated device topologies. The recent application of ALCVD methods for depositing Al_2O_3 [189], ZrO_2 [203], and HfO_2 [107] appears to provide much promise, where self-limiting chemistries are employed to control film formation in a layer-by-layer fashion.

In addition, very high- k dielectrics, such as SrTiO_3 have been deposited directly on Si using MBE methods. An EOT of less than 1 nm was reported with dramatic improvements in transistor performance [204]. And crystalline ZrO_2 has also been examined by MBE methods [137]. However, a manufacturable scaled CMOS process incorporating MBE methods, with the inherent poor throughput relative to present Si-based fabrication operations, remains as a challenge.

2.4.7 Reliability

It is of no doubt that the electrical reliability of a new gate dielectric must also be considered critical for application in CMOS technology. The determination of whether or not a high- k dielectric satisfies the strict reliability criteria requires a well-characterized materials system. The nuances are listed below: (1) the dependence of voltage acceleration extrapolation on dielectric thickness and (2) the improvement of reliability projection arising from improved oxide thickness uniformity.

Much of the understandings for ultrathin oxides have come about only in the past seven years, despite decades of research on SiO₂. This suggests that understanding the reliability and failure mechanisms in high- k materials will require significant effort, especially if any material is to replace SiO₂ within two years, as suggested by most roadmaps [12, 24].

2.4.8 Our consideration of high- k dielectric materials

According to the discussions above, we now give a comparison of properties of most commonly investigated alternative dielectrics, which is shown in Table 2-3.

Table 2-3 Comparison of relevant properties for high- k candidates.

Material	Dielectric constant	Bandgap (eV)	Crystal structure(900°C)	Drawbacks for application
SiO ₂	3.9	8.9	Amorphous	
Al ₂ O ₃	9	8.7	Amorphous	low dielectric constant
Y ₂ O ₃	15	5.6	Cubic	relatively low dielectric constant thermodynamic instability
Ta ₂ O ₅	26	4.5	Orthorhombic	low bandgap thermodynamic instability
TiO ₂	80	3.5	Tetrag (rutile,anatase)	very low bandgap thermodynamic instability
ZrO ₂	25	7.8	Mono,tetrag,cubic	high oxygen diffusivity
HfSiO	11	5.3	Amorphous	relatively low dielectric constant
HfON	18	--	Amorphous	relatively low dielectric constant
HfSiON	14	--	Amorphous	relatively low dielectric constant
HfO ₂	25	5.7	Mono,tetrag,cubic	high oxygen diffusivity
HfAlO	16	--	Amorphous	relatively low dielectric constant

The major drawbacks associated with the metal oxides are: (1) thermal instability on silicon, namely for Ta₂O₅ and TiO₂, resulting in a low- k interface layer, (2) the tendency of pure metal oxides to crystallize at relatively low temperatures. Although the silicate films may alleviate some of these problems by combining the high- k advantages of the pure metal oxide with the electrical advantages of SiO₂. But, it has been previously seen that the k value of the films is decreased. As of today, no one material has been identified that meets all the requirements of an alternative high- k gate dielectric. Although many kinds of high- k materials have been studied, the final focus has been placed onto the hafnium oxide based materials [147-168].

Among all these candidates, HfO₂ seems to be the most promising gate dielectric candidate for several reasons such that it has a high dielectric constant (20 - 30), large energy band gap (~ 5.68 eV), good interface properties ($D_{it} \sim 10^{11} \text{eV}^{-1} \text{cm}^{-2}$), low leakage current density, good reliability with long lifetime (> 10 years), lattice parameter similar to that of Si with a small lattice mismatch ($< 5\%$), thermodynamically stable with the silicon substrate and suitable tunneling barrier height for both electrons and holes (> 1 eV) [23]. Therefore, in our work, HfO₂ based materials have been systematically investigated as the alternative gate dielectrics.

However, relatively low crystallization temperature (< 600 °C) is the major drawback of HfO₂. In addition, high oxygen diffusivity, significant charge trapping at the bulk, uncontrolled oxide formation at the interface, large hysteresis, fixed oxide charge, and low channel mobility are also the serious concerns as regard to the HfO₂ for the gate dielectrics application [148, 205, 206]. In order to further improve the gate dielectric properties, we try to incorporate silicon and nitrogen into the HfO₂ dielectrics.

2.5 Conduction mechanisms in gate dielectrics

For a thermal grown SiO₂ film, it could be considered basically as an ideal insulator under moderate bias conditions. When the electrical field is sufficiently high or when a dielectric other than SiO₂ such as HfO₂ is used, however, the conductance is generally much higher. Table 2-4 summarizes the typical conduction processes in thin

Table 2-4 Typical conduction mechanisms in MOS capacitors along with their expressions and illustrations. [37]

Fowler-Nordheim Tunneling	$J = \frac{A}{4\phi_B} E_i^2 \cdot \exp\left(-\frac{2B\phi_B^{3/2}}{3E_i}\right)$	
Direct Tunneling	$J = \frac{A}{d^2} \left\{ \left(\phi_B - \frac{V}{2} \right) \cdot \exp\left(-Bd\sqrt{\phi_B - \frac{V}{2}}\right) - \left(\phi_B + \frac{V}{2} \right) \cdot \exp\left(-Bd\sqrt{\phi_B + \frac{V}{2}}\right) \right\}$	
Schottky Emission	$J \propto T^2 \cdot \exp\left(-\frac{\phi_B - \sqrt{E_i/C}}{kT}\right)$	
Poole-Frenkel Emission	$J \propto E_i \cdot \exp\left(-\frac{\phi_t - 2\sqrt{E_i/C}}{kT}\right)$	
Hopping Conduction	$J \propto E_i \cdot \exp\left(-\frac{\Delta E_{ah}}{kT}\right)$	

$$A = \frac{q^2}{2\pi h}, B = \frac{4\pi\sqrt{2m^*}q}{h}, C = \frac{4\pi\epsilon_i}{q^3}$$

dielectric films [37]. For an ideal insulator at low temperature, tunneling should be the dominant conduction mechanism. However, at elevated temperatures, due to the limited size of barriers and various defects in oxides which can be thermally excited,

Schottky emission or Poole-Frenkel emission may emerge as the dominant conduction mechanisms. Moreover, high- k materials usually have a smaller barrier and a larger trap density than SiO_2 . Therefore, it is very important to study the thermally excited conduction mechanisms in high- k gate dielectrics. In addition, as suggested by the expressions of the different mechanisms listed in table 2-4, the barrier height of the dielectric can also be determined.

2.5.1 The tunneling phenomenon

Tunneling emission is caused by field ionization of trapped electrons into the conduction band or by electrons tunneling from the metal Fermi energy into the insulator conductor band. Mainly, there are two types of tunneling occurring in the dielectrics: direct tunneling and FN tunneling. Direct tunneling, which is defined in equation (2-3), usually occurs in ultrathin dielectrics (< 3 nm) [207]. For a relatively thick SiO_2 film, no detectable current flows until the FN tunneling occurs at a large electric field. In 1969, Lenzlinger and Snow investigated the electrical conduction in SiO_2 with thickness ranging from 64 to 500 nm [208]. The conduction is more dependent on the electrode than any other issues because SiO_2 has an extremely wide bandgap, low trap density in the forbidden band, high electron mobility in the conduction band and a high energy barrier at its contact with an electrode. Lenzlinger and Snow pointed out that the density of conduction current in conventional SiO_2 films can be excellently described by the classical FN formula as described in

equation (2-4) [208]. In the electrode-limited conduction cases, different metals would have different barrier heights for the FN injection and the slopes in FN plots are governed by the effective electron or hole mass which is also dependent on the electrode materials.

2.5.2 Schottky barrier emission conduction

An electron to escape into vacuum has to overcome the work function, if no electric field is applied. This can be realized by thermal activation. When an electric field is applied, it can enhance the electron emission by lowering the potential barrier for thermionic emission. The carrier injection from a metal electrode into the bulk dielectric is governed by the Schottky theory [181]:

$$J = AT^2 \exp\left[-\frac{e\phi - \beta E^{1/2}}{kT}\right] \quad (2-8)$$

where A is given by $4\pi emk^2/h^3$, a constant independent of E and β is given by

$$\beta = \left[\frac{e^3}{4\pi\epsilon_0\epsilon_\infty} \right]^{1/2} \quad (2-9)$$

ϵ_0 and ϵ_∞ are the permittivity of free space and relative permittivity at high frequencies. According to equation (2-8) a plot of $\ln(J/T^2)$ versus $E^{1/2}$ yields a straight line. The intercept is the pre-exponential and the slope is the term in brackets. And the barrier height and the relative permittivity can be obtained by the intercept and slope respectively.

2.5.3 Poole-Frenkel conduction

An electron transferring from a trap to another localized state under the influence of an electric field is known as the Poole-Frenkel effect. The Poole-Frenkel mechanism occurs within the bulk of the dielectric where the barrier between localized states can be lowered due to the influence of the high electric field. For the mechanism to occur the material must have a wide bandgap and must have donors or acceptors. Because the localized states of the valence band do not overlap those in the conduction band, the donors or acceptors do not gain enough energy to move into the conduction band or valence band, unlike in normal semiconductors.

Below is the Poole-Frenkel expression from which the current may be calculated for a given electric field. A plot of $\log (J/E)$ versus $E^{1/2}$ yields a straight line with slope M_{pf} :

$$J = eN_C \mu E \exp \left[\frac{-q \left(\phi_t - \sqrt{eE / \pi \epsilon_r \epsilon_0} \right)}{kT} \right] \quad (2-10)$$

$$M_{pf} = \frac{e^{3/2}}{(\pi \epsilon_0 \epsilon_r)^{1/2} kT}, \quad (2-11)$$

where N_C is the effective density of states in the conduction band,, Φ_t is the trap depth, ϵ_r is the relative dielectric constant.

And as previously discussed, the same plot of $\log J$ versus $E^{1/2}$ is also used for determining whether the Schottky emission occurs. And in order to resolve between these two mechanisms, additional tests have been applied. The conduction mechanism generally does not remain the same as the temperature is raised and it is not unusual to find two mechanisms operating simultaneously, though one may predominate over the other depending on the experimental conditions.

2.5.4 Hopping mechanism

Hopping can occur from one trapping site to the other; the mechanism is visualized: the electron acquires some energy, but not sufficient, to move over a barrier to the next energy state. Tunneling then takes place, and from the probability of tunneling and thermal excitation the conductivity is obtained as:

$$\sigma = A \exp \left[-\frac{B}{T^n} \right] \quad (2-12)$$

where A, B are constants and $0.25 < n < 0.5$.

CHAPTER THREE

Laser Molecular Beam Epitaxy System Installation

Laser-MBE has become an important technique for fabricating novel materials, which has benefited from the intrinsic advantages of PLD such as producing a variety of high melting-point materials and multi-component films under quite simple process, reproducing the target composition with relative ease under the appropriate conditions. Besides, with the employment of reflection high energy electron diffraction (RHEED), Laser-MBE also inherits the merits of conventional MBE for film deposition, especially for the growth of multi-layer films in atomic scale control [209-212].

In the research work for my Ph. D study, a Laser-MBE system has successfully been setup and used to fabricate various kinds of thin films ranging from metals, semiconductors to insulators. In this chapter, the installation of the Laser-MBE system is described in detail and some basic working principles of PLD and RHEED are described as well.

3.1 Pulsed laser deposition

In condensed matter science, lasers play an important role either as a passive component for process monitoring or as an active tool by coupling its radiation energy into the material being processed which leads to various applications such as localized melting during optical fiber pulling, laser annealing of semiconductors, surface cleaning by desorption and ablation, laser-induced rapid quench to improve surface hardening and most recently, pulsed laser deposition for deposition of thin films. Conceptually and experimentally, PLD is simple. The basic concept of PLD is shown in Figure 3-1. The system consists of a target holder and a heatable substrate holder housed in a vacuum chamber. A high-power laser is used as an external energy source. A set of optical components, which is not shown in this figure, is used to focus and raster the laser beam over the target surface. After transmitting through the optical components, the laser beam is focused and impinges on the target surface. The evaporated species from the target are contained in a forward ejected flame, called “plume” as shown in Figure 3-1. These species expand into the surrounding ambient, reach the substrate with high kinetic energy (typical in the order of 10 eV) and finally, are deposited on the substrate. From the above, four aspects can be distinguished at the film fabrication with PLD:

- (1) interaction between the laser beam and the target;
- (2) interaction of evaporated materials with the laser beam;
- (3) expansion of the plume;
- (4) growth of the film.

Film growth can be carried out in a reactive environment containing any kind of gases with or without plasma excitation. It can also be operated in conjunction with other types of evaporation sources such as the effusive cell of MBE in a hybrid approach [209].

Figure 3-1 Schemaic diagram of a pulsed laser deposition apparatus.

The first application of laser ablation to vaporize materials and to deposit thin films in a vacuum chamber was reported by Smith and Turner in 1965 [213]. Systematic investigations were performed in the late 1970s followed in the late 1980s by the fabrication of highly crystalline dielectric thin films, semiconductor epitaxial films for

bandgap engineering and the high T_c superconductors [214-216]. And the successful growth of high T_c superconducting films in 1987 triggered the major breakthrough of PLD, which literally lifted PLD off the ground [214]. In 1993, Cheung pointed out that the total number of publications in PLD since 1987 was more than 10 times the combined publications in the previous 25 years [217]. The simplicity and versatility of the experimental setup makes it an affordable technique to explore new frontiers in condensed matter science. In addition, PLD has been developed into several novel branches, such as dual-beam laser ablation, ion-beam-assisted deposition and most recently, the Laser molecular beam epitaxy which consists of the typical PLD technique as well as the RHEED technique. And similar to typical MBE, the Laser-MBE technique also provides the layer-by-layer growth of thin films with smooth surfaces and interfaces.

3.1.1 Lasers

In general, the useful range of laser wavelengths for PLD lies between 193 nm and 400 nm because most materials used for deposition work exhibit strong absorption in this spectral region [217].

Nd^{3+} : YAG (yttrium aluminum garnet) or excimer lasers are normally used as the laser source in PLD. Nd^{3+} : YAG lasers are solid-state systems. The neodymium ions serve as the active medium and are present as impurities in the YAG host. The laser

emission of Nd^{3+} : YAG occurs at 1064 nm, quite outside the desired range indicated earlier. By using a nonlinear crystal, the output frequency can be converted to 355 nm or 266 nm.

Unlike Nd^{3+} : YAG, excimer is a gas laser system and can emit the radiation directly in the UV region. High outputs delivering in excess of 1J/pulse are commercially available. These systems can also achieve pulse repetition rates up to several hundred hertz with energies near 500 mJ/pulse. Consequently, the excimer is generally the choice for PLD work. Table 3-1 gives a list of excimer wavelengths. The corresponding active excimer molecule is indicated as well. Among the listed excimers, KrF and XeCl have been extensively used for PLD. KrF is the highest gain system for electrically-discharged pumped excimer lasers and is the popular choice among the PLD community. Although KrCl operates at a shorter wavelength than KrF, it is a low-gain system and does not output the pulse energies required for PLD work. Therefore, Lambda COMpex 205 KrF laser is chosen as the laser source in our system.

Table 3-1 The operating wavelengths of excimer laser.

Excimer	Wavelength (nm)
F_2	157
ArF	193
KrCl	222
KrF	248
XeCl	308
XeF	351

3.1.2 Optics

Between the output port of the laser and the laser input port of the deposition chamber, optical elements are placed in order to steer and focus the beam. These optical elements include lenses, apertures, mirrors, beam splitters and laser windows. One of the most important deposition parameters in PLD that controls the film stoichiometry and crystallographic quality is the laser energy density incident on the target. Thus, lenses are the most important among the optical elements. And the aperture is used to minimize the lens aberrations.

In comparison to most simple deposition systems, such as the parallel magnetron or cylindrical magnetron sputtering systems, the laser deposition system will be more expensive for a single deposition system owing to the cost of a laser. However, by using standard mirrors and beam delivery tubes which reflect the primary beam into different chambers, one can easily share the laser in between many deposition chambers. In addition, by precisely controlling the rotation of the mirrors, the reflected laser beam can be confined in a specific region which makes multi-component deposition very convenient.

Beam splitters split the laser beam into two or more separate beams. Both equal and unequal beam splitting, in terms of energy throughput, are possible depending on the type of beam splitters used. For the dual-beam PLD, the primary beam is split into two

equal-intensity beams, directed into the deposition chamber and impinging on two targets. Each target is offset an equal distance from the substrate center. If two identical targets are used, the dual-beam deposition is a method to improve the characteristics of target erosion and the homogeneity of thin films. In addition, two different targets can be used as well to co-deposit novel films with desired compositions.

The laser windows through which the laser enters the deposition chamber should be made out of laser-quality optical material and polished to a very high degree of flatness. The wavelength of the laser should be in the transmittance range of the window material. Therefore, UV-graded fused silica is chosen as the window material because the fused silica has a suitable transmittance range of 190 - 2500 nm for our 248 nm KrF laser. In addition, these windows must be free of defects such as bubbles and inclusions which can deteriorate the beam quality seriously.

3.1.3 Deposition system

The deposition chamber is one of the most crucial components in a PLD system. In addition to the standard ports required on all vacuum chambers (e. g., pumping port, gas inlet, pressure gauging and viewports), the PLD chamber must have ports for the laser beam. The beam path must be completely unobstructed. Various targets can be used in PLD, such as pressed powders, sintered pellets, cast material, single crystal,

and metal foils. The main difference between these different target morphologies is in the nature of the target erosion, and the generation of particulates. A good rule of thumb is that high-density and highly homogeneous targets yield the best films. In terms of uniform target erosion and consumption, the most common practice is to rotate the target during deposition. In this fashion, an annular region of a disk-shaped target will be ablated. One of the great advantages of PLD over other thin film deposition techniques is the ease with which in situ multilayer structures can be formed. And the targets are much easier to be replaced compared to MBE or sputtering.

3.1.4 Mechanisms of laser ablation

In contrast to the simplicity of the hardware, the laser-solid interaction is a very complicated physical phenomenon. The mechanism that leads to material ablation from the target depends on laser characteristics, as well as the optical, topological, and thermodynamic properties of the target [216, 217]. Kelly et al. pointed out that thermal, electronic, exfoliation, cluster formed by condensation, together with hydrodynamic sputtering are all possible primary mechanisms for laser ablation [218]. In addition, it is found that the background gas pressure and the laser energy density are well decoupled, which gives the process a significant degree of freedom. As a result, the dynamic range of deposition pressure is the largest compared to any other deposition technique.

3.2 Reflection high energy electron diffraction (RHEED)

The success of MBE is largely attributed to its compatibility with in-situ surface characterization. Most other thin film growth environments require ambient pressures or fields too hostile to apply the developed electron probes to study the surfaces. The vacuum requirements and geometry of MBE, however, conveniently permit the use of RHEED. RHEED is not a complicated apparatus. Only an electron gun and a phosphor-covered viewport are needed for these measurements. The diffraction pattern on a fluorescent phosphor screen can be recorded by a computer controlled CCD camera. A frame grabber and software collect the images. For observing RHEED oscillations, a high speed camera must be used. With this simple apparatus, it is easy to obtain important information about the character of the surface and the nature of the growth mode.

3.2.1 Diffraction theory

A crystalline surface is assumed to have a two-dimensional array of reciprocal lattice rods satisfying simultaneously the conditions of constructive interference and elastic scattering. These conditions are used to predict the location of intensity maxima in the diffraction pattern. The geometry of a RHEED pattern may be determined with kinematical theory. With a well-ordered sample surface, the reflected electrons form a diffraction pattern consisting of bright spots and/or streaks observable on the fluorescent screen. In the RHEED system, electrons having energy of typical 10–50

keV are incident on the sample surface at a variable glancing angle α ($0^\circ \leq \alpha \leq 5^\circ$) and are reflected onto a fluorescent screen as shown in Figure 3-2. And due to the grazing angle of incidence, the electrons only interact with the top layer of atoms (1-2 nm) on the surface.

Figure 3-2 Typical setup for RHEED experiment.

The diffraction of the incoming primary beam leads to the appearance of a characteristic RHEED pattern with intensity-modulated streaks normal to the shadow edge. Figure 3-3 shows the diffraction pattern of the SrTiO_3 (100) surface. From the symmetry and separations of the diffracted beams, one can determine the surface reconstruction and the lattice constant. From the disappearance of the reconstruction, one can determine the flux ratios. From phase transitions, one can calibrate temperature. From the qualitative appearance of the pattern, cluster growth or layer growth can be distinguished [219, 220].

Figure 3-3 Diffraction Pattern from the SrTiO_3 (100) surface.

3.2.2 RHEED oscillation

Compared to other diffraction methods, the glancing incidence angle geometry of RHEED makes it ideal for combining with MBE to monitor the growth of epitaxial layers by the intensity oscillations of RHEED pattern [221]. When the growth is initiated on a smooth surface, the intensity of the RHEED pattern starts to oscillate. Arthur explained this oscillation using a layer-by-layer growth model as illustrated in Figure 3-4 [222].

The arriving atoms first nucleate in 2-D islands if steps are not present on the smooth surface. Subsequently, arriving atoms can migrate to the existing step edges to complete the monolayer and return the surface to a smooth condition. Thus the surface cycles between smooth and atomically rough, with a period corresponding to the time to complete a monolayer of growth. The rougher surface causes more diffuse

scattering of the RHEED beam, leading to a lower intensity of the diffracted beams. As illustrated in Figure 3-4, the RHEED oscillation period corresponds exactly to the monolayer growth rate. Therefore, the RHEED oscillations provide a precise method of monitoring the epitaxial growth of thin films as well as measuring growth rates in real time.

Figure 3-4 Schematic diagram of the correlation of surface coverage of 2-D clusters with idealized RHEED oscillations. [222]

3.3 History and fundamentals of Laser-MBE

Based on a typical MBE system, Cheung used an Nd: YAG laser as the evaporation source combined with the Knudsen effusive cells in 1986 [209, 223]. The schematic drawing of the apparatus is shown in Figure 3-5. In this particular case, $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$

was epitaxially grown. The Hg and tellurium beams were effused from Knudsen cells.

CdTe beam was produced by evaporating a CdTe target with a pulsed laser beam.

Figure 3-5 Schematic drawing of the apparatus for HgCdTe deposition. [209, 223]

Compared with the traditional Knudsen source oven, the laser source has the merit of evaporating ultrahigh melting-point material ($> 1500\text{ }^{\circ}\text{C}$). And the beam flux intensity can be much more easily modulated by laser than the Knudsen source. In thermal evaporation, the beam flux intensity is controlled by changing the temperature of the effusive cell. It is a very slow process, depending on the thermal mass and the temperature of the cell. Furthermore, since the flux intensity varies exponentially with temperature, very precise temperature regulation is required for accurate flux intensity control. However, by changing the power density and the repetition rate of the laser beam, the beam flux intensity can be modulated more easily and precisely.

In 1991, for the first time, by modifying a conventional PLD system shown in Figure 3-6, Kanai demonstrated the layer-by-layer deposition of high T_c (Ca,Sr)CuO₂ superconductor with the observation of well-formed RHEED oscillations [210]. The application of the oscillation of RHEED intensity permits in-situ growth control of one atomic layer and makes it possible to control the composition of the films strictly.

Figure 3-6 Computer-controlled Laser-MBE apparatus used for the successive deposition of (Ca,Sr)CuO₂ films. [210]

As a matter of fact, Laser-MBE is the only technique known today that can produce a fraction of monolayer of materials on a surface in a short time scale of about a microsecond for high-melting solid state materials. In this sense, for study of the dynamics of atoms on surfaces, Laser-MBE is an excellent apparatus in combination with a fast surface analysis tool. The quality of the surface coverage of films deposited by Laser-MBE at rates of 0.1-1.0 Å/sec is excellent as a result of which fine

superlattices have been prepared by a number of groups in the early 1990s [224-227]. Many kinds of dielectric thin films and their heterostructures have been fabricated by Laser-MBE. Table 3-2 lists some materials which have been epitaxially grown by Laser-MBE. Most of the materials fabricated have perfect lattice structures with atomic scale smooth surfaces and interfaces, which can be used for constructing artificially designed oxides with new layered lattices [212, 228]. The atomic-scale controlled epitaxial growth of oxide thin films opens a door for investigating the mechanism and application of multi-functional oxide superlattices [212].

Table 3-2 Some materials fabricated by Laser-MBE. [227-238]

Dielectrics	SrTiO ₃ LaAlO ₃ LaTiO ₃ ZrO ₂
Ferroelectrics and optics	BaTiO ₃ (Nb, Ba)TiO ₃
Magnetoresistance	(La, Sr)MnO ₃ (La, Te)MnO ₃
Conductor	SrVO ₃ SrMoO ₃
Semiconductor	(Nb, Sr)TiO ₃ (In, Sr)TiO ₃
Superconductor	YBCO (YBa ₂ Cu ₃ O ₇)

3.4 Description of Laser-MBE System

The Laser-MBE system which has been set up in our laboratory is schematically illustrated in Figure 3-7 and Figure 3-8. This system is composed of five main parts:

- (1) An ultrahigh vacuum (UHV) epitaxial chamber with a background pressure of 2×10^{-8} Pa containing a four-target holder and a substrate holder. In order to achieve such a UHV environment, ion pump and sublimation pump have been employed in the

system in addition to the machine pump and turbo molecular pump. The platinum filament, which is resistant to oxidation, is used to heat up the substrate to a maximum temperature of 850 °C. And the substrate temperature is measured and calibrated by a thermocouple and an infrared thermometer.

Figure 3-7 The schematic diagram of the Laser-MBE apparatus.

(2) A KrF excimer laser with a wavelength of 248 nm (Lambda COMpex 205). The COMpex 205 laser is a highly effective tool, featuring a compact design and easy installation and operation. Due to its ultrahigh pulse energy of 700 mJ and average power of 30 W, it is especially designed for demanding high-pulse energy applications. The maximum repetition rate is 50 Hz which enables the fast deposition of films. And

Figure 3-8 the Laser-MBE system.

the pulse duration is about 25 ns. COMpex 205 also delivers the beam stability and energy stability performance (1 sigma: 1%) which are essential factors to achieve stable and superior results in sophisticated research applications.

(3) A motion controller system combined with a linear stage for the scanning of laser beam; In order to further improve the uniformity and homogeneity of the deposited films, the laser beam is made to scan over a large area of the target instead of impinging only at a point or a circle. The specific methodology is described as follows: The mirror, which is used to reflect the focused laser beam on the target, is mounted on a linear stage, and the linear stage is controlled by a motion controller which can

drive and control the two-dimensional motion of the linear stage precisely and periodically. Thus this combined system can make the focused laser beam scan over the target surface. In practice, combining the target rotation with this two-dimensional scan, the effective laser scan area can be as large as the size of the target. Furthermore, since the controller system can precisely confine the laser ablation in a specific region, multi-component thin films can be easily fabricated. For example, in our work, hafnium silicate (HfSiO_4) was deposited by the ablation of a “Hf/Si” target. This multi-component target was prepared as follows: the two targets were first cut into halves, then a half of the Hf and a half of the Si target were mounted into one target holder as shown in Figure 3-9. After that, by using the motion controller, the laser can impinge two-dimensionally on either Hf or Si part in a precisely confined area as shown in the shadow region of Figure 3-9. Consequently, the hafnium silicate can be easily fabricated by the ablation of these two regions alternatively. In addition, by varying the amount of the laser pulses impinging on the various materials, the Hf/Si ratio can be tuned and hafnium silicate with different Hf/Si ratio can thus be fabricated with ease.

Figure 3-9 Multi-component Hf/Si target used in Laser-MBE system.

(4) A RHEED system and charge coupled device (CCD) camera. As discussed in the previous section, the RHEED system acts as the “eye” of Laser-MBE and is of great importance.

(5) A DC ion source. The DC filament-driven ion source is highly suitable for applications such as ion-beam assisted deposition, etching, sputtering and substrate cleaning. In our Laser-MBE system, a DC ion source is built in the system. Various gases such as O_2 and N_2 can be used. The use of atomic oxygen enables the fabrication of high quality oxide thin films under an oxygen pressure as low as 1×10^{-2} Pa. And by the activation of the ion source, atomic nitrogen can be doped into many dielectrics such as $SrTiO_3$, HfO_2 and $HfSiO$.

3.5 Results and Discussion

3.5.1 Epitaxial growth of SrTiO₃ thin films

The epitaxial growth of thin films with fine lattice structure and surface morphology is essential to fabricate SIS (semiconductor-insulator-semiconductor) tunnel junctions and other kinds of artificial superlattices.

In our work, SrTiO₃ thin films were deposited epitaxially on SrTiO₃ (100) single crystal substrates. The in-situ RHEED provides useful information of the surface structure, morphology and growth modes. The RHEED intensity oscillation enables us to control the exact number of deposited molecular layers. For the growth of SrTiO₃ thin film, a focused pulsed laser beam impinged onto a single-crystal SrTiO₃ target. The repetition rate was set at 4 Hz and the energy density was about 0.8 J/cm². The target was held on a rotating disk controlled by a pulsed motor which makes the laser beam always hit a fresh surface on the target. The SrTiO₃ substrate temperature was held at 550°C; and the O₂ partial pressure was kept at 9×10^{-5} Pa during deposition.

The pre-treatment of SrTiO₃ substrate is very important for the growth of high-quality epitaxial films in the layer-by-layer mode. In our experiment, the substrate was first annealed at 650°C for 20~30 min under 2×10^{-4} Pa O₂ to clean up the surface followed by the homoepitaxial growth of SrTiO₃ films. Figure 3-10 shows the RHEED diffraction pattern before and after the annealing. Obviously, as indicated by

the sharpness of the diffraction pattern, the surface smoothness was improved after the thermal annealing in oxygen.

Figure 3-10 RHEED diffraction pattern of the SrTiO_3 (100) surface (a) as-received; (b) after the thermal annealing in oxygen.

Then on a smooth substrate surface, the epitaxial growth of SrTiO_3 was carried out. Figure 3-11 shows the RHEED oscillation of the specular spot during the epitaxial growth of the 20-layer SrTiO_3 . The continuous and well-behaved RHEED oscillations identify the fine two-dimensional layer-by-layer growth of SrTiO_3 . The abrupt change of the oscillation intensity at the on and off state of the laser indicates the sudden change of the surface roughness which well corresponds to Arthur's 2-D island growth mechanism [222].

Figure 3-11 RHEED oscillation of the specular spot during the epitaxial growth of the 20-layer SrTiO_3 .

By controlling the deposition parameters precisely, more than 100-layer of SrTiO_3 have been continuously deposited epitaxially which is shown in Figure 3-12. Besides SrTiO_3 , LaAlO_3 and MgO have also been epitaxially grown on SrTiO_3 (100) substrate in our work. Compared to a typical MBE, the intrinsic advantage of Laser-MBE is the flexibility in fabricating single crystal oxides and their superlattices. Therefore, Laser-MBE is proven to be a natural choice for oxide epitaxy.

Figure 3-12 RHEED oscillation of the specular spot during the epitaxial growth of the 100-layer SrTiO_3 .

3.5.2 RHEED characterization of Si surface roughness

In MOS technology, native oxide, metal contaminations and particles have commonly been suggested as one of the main origins of defect-related breakdown of gate oxides. It is well known that these factors inflict harmful effects, deform physical structure, generate additional electrical states and induce secondary defects. Compared to the thermal SiO_2 , the native SiO_2 contains more pinholes and defects, and thus degrades the quality of the final SiO_2 . As the thickness of SiO_2 decreases and the design rule shrinks, the quality of this surface layer is an important yield and reliability concern in advanced ULSI technologies. Therefore, the cleaning step is especially critical prior to high-temperature treatments.

The cleaning process which is most often applied before gate oxidation is the RCA cleaning and HF-last process [239]. This cleaning consists of two steps: SC1 and SC2. The SC1 step is a 10 minute cleaning in a $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ (1/1/5) mixture at a temperature between 75 and 90 °C immediately followed by a DI-water rinse. This step is used to remove the organic impurities of the Si surface. In between the two steps of the RCA cleaning, the Si wafer undergoes a $\text{HF}/\text{H}_2\text{O}$ (1/50) cleaning to remove the native oxide followed by a DI-water rinse. The SC2 step consists of a 10 minute cleaning in $\text{HCl}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ (1/1/5) mixture at temperature between 75 and 90 °C, again followed by a DI-water rinse. This step is used to remove the metallic impurities of the Si surface.

In order to illustrate the effectiveness of the cleaning process, many material characterization techniques including AFM, XPS, EELS, and FTIR have been utilized. RHEED is a powerful tool for surface characterization. However, it has seldom been used for the investigation of the Si surface in the literature. Therefore, in our work, RHEED is applied to identify the effectiveness of the cleaning process and modify the process parameters according to the Si diffraction patterns to get a smooth surface free of impurities.

Meuris et al. have pointed out that the ratio between NH_4OH and H_2O_2 (1/1) in SC1 is an important parameter in the RCA cleaning which affects the roughness of the silicon

surface [240]. By using AFM, Meuris found out that a lower NH_4OH concentration results in a less severe silicon surface roughening. However, it was also found that reduction of the NH_4OH concentration below (0.25/1) not only has a negligible effect on the silicon surface topography but also deteriorates the effectiveness of the particle-removal. Therefore, Meuris suggested that a modified SC1 with a $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ ratio of 0.25/1/5 could be the best compromise in the experimental condition.

In our experiment, three NH_4OH concentrations: 0.15, 0.25 and 1 were tried in the SC1 process. After the RCA cleaning, the silicon wafers were immediately loaded into the deposition chamber with a background pressure of about 1×10^{-5} Pa, followed by the RHEED observations.

Figure 3-13 shows the RHEED diffraction patterns. It is clearly noted that there is no obvious diffraction streaks in Figure 3-13 (a) indicating that the particles on Si have not been fully removed under such a low NH_4OH concentration. On the contrary, very clear Si (100) diffraction peaks have been recorded in Figure 3-13 (b), showing that the Si surface is very smooth and free of contaminations. Meanwhile, compared with the peaks in Figure 3-13 (b), the diffraction peaks in Figure 3-13 (c) are much vaguer. These results are consistent with Meuris's AFM data. From the diffraction pattern, the quality of the Si surface can be estimated prior to the thin film deposition. Therefore, RHEED is an effective tool for Si surface characterization.

Figure 3-13 Silicon surface diffraction pattern after RCA cleaning with different modified SC1 process: (a) $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2$ (0.15/1); (b) $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2$ (0.25/1); (c) $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2$ (1/1).

3.6 Conclusion

The Laser-MBE system has been successfully set up and calibrated in our research work. Many kinds of oxides, such as SrTiO_3 , LaAlO_3 and MgO , have been successfully grown on SrTiO_3 (100) substrate in the layer-by-layer mode. For example, more than 100 layers of SrTiO_3 have been epitaxially deposited on the SrTiO_3 substrate; and well-formed RHEED oscillation has been recorded, which illustrates the capability of Laser-MBE in controlling the epitaxial growth of oxide thin films.

RHEED is a powerful surface characterization tool. In addition to the in-situ monitoring of the epitaxial growth, RHEED has also been used to investigate the Si surface roughness. From the diffraction pattern of Si, the surface condition after cleaning can be well identified.

CHAPTER FOUR

EXPERIMENTAL PROCEDURES

The dielectric hafnium oxide (HfO_2), hafnium silicate (HfSiO) and hafnium silicon oxynitride (HfSiON) thin films prepared by the Laser-MBE process have been systematically investigated in this study for the high- k microelectronic device applications. The Laser-MBE derived thin films have been characterized using various measurement methods. In this chapter, the description is given for the detailed experimental procedures: (1) preparation of the HfO_2 -based dielectric thin films; and (2) characterizations of these HfO_2 -based thin films including microstructure, compositional analysis, dielectric and electrical properties.

4.1 Substrate preparation

As mentioned in the previous chapter, in order to achieve a high quality interface between the high- k gate oxide and Si substrate, the substrate preparation is an important step. A thoroughly-cleaned substrate should be smooth and free of

impurities such as organics, native oxide, heavy metals or mobile ions. Both n and p type (100) oriented silicon wafers, with 1-10 $\Omega \cdot \text{cm}$ resistivity, are used as the substrate for the deposition experiments. Before deposition, the substrates were cleaned by a modified RCA procedure, the industry standard method for removing contaminants from wafers [239, 240]. The RCA procedure is described in details as follows:

- I. **Modified SC1 (organic clean):** Removal of insoluble organic contaminants with a $\text{H}_2\text{O} : \text{H}_2\text{O}_2 : \text{NH}_4\text{OH}$ (5:1:0.25) solution at 70-80 °C for 10 minutes;
- II. **Oxide Strip:** Removal of the native silicon dioxide layer where metallic contaminants (such as Fe) may have accumulated as a result of (I), using a diluted $\text{H}_2\text{O} : \text{HF}$ (50:1) solution for 15 seconds;
- III. **SC2:** Removal of ionic and heavy metal atomic contaminants using a solution of $\text{H}_2\text{O} : \text{H}_2\text{O}_2 : \text{HCl}$ (6:1:1) at 70-80 °C for 10 minutes.

After the RCA cleaning, the wafers were loaded immediately into the deposition chamber followed by the RHEED observation of Si surface at a background pressure of 1×10^{-5} Pa. As discussed in the previous chapter, the Si surface condition such as the existence of the native oxide and the roughness of the surface can be judged from the RHEED diffraction pattern. Once a high-quality silicon substrate is prepared, the gate oxide is ready for deposition.

4.2 Gate oxide deposition

All the gate oxides have been deposited by Laser-MBE technique. For the HfO_2 , pure hafnium metal has been used as the target and it is oxidized into HfO_2 in the oxygen atmosphere. As illustrated in Figure 3-8, by co-sputtering Hf and Si targets in oxygen, hafnium silicate is thus obtained. Table 4-1 listed the detailed targets and deposition parameters used in the thin film deposition.

Table 4-1 Gate dielectrics deposition parameters.

Gate dielectrics	Targets (Purity)	Deposition Temperature	Ambient Pressure (Pa)
HfO_2	Hf (99.9 %)	200-500 °C	$3 \times 10^{-2} \sim 3$ (Ar/ O_2)
HfSiO	Hf, Si (99.999%)	300 °C	0.3 (O_2)
HfSiON	Hf, Si (99.999%)	300 °C	0.3 (N_2/O_2)

The power density of the laser beam was fixed at 1.8 J/cm^2 and the laser pulse repetition rate was 2 Hz. For HfO_2 deposition, the background pressure (Ar/ O_2) was fixed at 3 Pa, but the oxygen partial pressure ranged from 3×10^{-2} Pa to 3 Pa. And for the hafnium silicate deposition, the oxygen pressure was kept at 0.3 Pa. By changing the total pulses of laser ablation, a set of dielectric thin films with different thickness was fabricated. And by changing the pulse ratio between Hf and Si, hafnium silicate films with different stoichiometries were fabricated. In addition, by incorporating nitrogen into the hafnium silicate, HfSiON films were thus deposited.

After the deposition, post deposition annealing (PDA) was performed ex situ in a RTA furnace (MODEL: Jipelec, JETFirst) at 500-950 °C for 20-30 seconds in a N₂ ambient.

4.3 Fabrication of the MOS capacitors

For the purpose of performing dielectric and electrical measurements, MOS-structured capacitor devices were fabricated, and the detailed experimental procedure is described as follows.

In the first step, the top electrode contact windows were defined using the lift-off technique. The windows for the top electrode were defined on patterned photoresist by the image reversal process as illustrated in Figure 4-1. The photoresist AZ5214 was spin-coated onto the thin film with a spin rate of 3000 rpm for 30 seconds. Then the photoresist was soft-baked at 105 °C for 90 seconds. The shadow mask pattern was in a square matrix pattern with the cell dimension of $1 \times 10^{-4} \text{ cm}^2$. After aligning the plastic mask and the sample, the top photoresist layer was exposed at the conditions of UV source density 14 mW/cm^2 and exposure time of 4 seconds.

After that, the image reversal process was carried out by annealing at 110 °C for 8 minutes, and the flood exposure was followed for 25 seconds. Finally the top electrode opening was defined by developing in the 1:2 diluted AZ developer 712712-5 solution.

Figure 4-1 The flow chart of the image reversal process for the top electrode window opening.

Two kinds of conducting materials, platinum (Pt) and ruthenium oxide (RuO_2), are chosen as the gate electrode. For the Pt metallization, 2 nm of titanium (Ti) and 200 nm of Pt were deposited onto the dielectric thin films using the RF magnetron sputtering (Model:Univex 450B Leybold). For the RuO_2 deposition, Ru metal was used as the target and RuO_2 was deposited in O_2/Ar ambient at room temperature using the same RF magnetron sputtering system. The top electrode pattern was shown by bathing in acetone to remove the photoresist layer. After the top electrode

metallization, in order to make an ohmic contact backside, the backside of the wafer was first etched by a mixture solution of $\text{NH}_4\text{OH}/\text{HF}$ (10/1) for 10 seconds to remove the native oxide. Then, 300 nm Al was sputtered in direct contact with the Si. After that, the device was annealed by a tube furnace in the forming gas (95% N_2 , 5% H_2) at 420 °C for 30 minutes to further reduce the contact resistance. The detailed sputtering process parameters for all the electrodes used are summarized in Table 4-2.

Table 4-2 The sputtering parameters of the metal contact.

Electrode	Pt	RuO_2	Al
Target	3" Pt (purity>99.99%)	3" Ru (purity>99.99%)	3" Al (purity>99.99%)
Sputtering pressure	4×10^{-1} Pa (Ar 24 sccm)	5.4×10^{-1} Pa (Ar 18 sccm, O_2 2 sccm)	3.6×10^{-1} Pa (Ar 20 sccm)
Sputtering power	200 W	300 W	450 W
Growth temperature	Room Temperature	Room Temperature	Room Temperature
Thickness	200 nm	200 nm	300 nm

As a summary, the complete device fabrication procedure is summarized in Figure 4-2.

Figure 4-2 The flow chart of the fabrication procedure of the MOS capacitors.

4.4 Characterizations of the high- k gate oxide

4.4.1 Surface and stoichiometry characterization

4.4.1.1 Auger electron spectroscopy (AES)

AES is a widely used surface-analytical technique. The surface to be analyzed is irradiated with a beam of electrons of sufficient energy, typically in the range of 2-10 keV, to ionize one or more core levels in surface atoms. After ionization, the atom, left in an excited state, de-excites through the emission of x-rays or Auger electrons which are characteristic of the energy levels involved. Figure 4-3 shows an energy

level diagram which depicts the Auger electron process and the kinetic energy of the Auger electron illustrated is typically described as

$$E_{KL_1L_{2,3}} = E_K - E_{L_1} - E_{L_{2,3}} - \phi \quad (4-1)$$

Where E_K is the energy of the ionized core level, E_{L_1} is the energy of the level from which the electron originates to fill the initial core hole, $E_{L_{2,3}}$ is the energy level from which the Auger electron originates and ϕ is the work function. The kinetic energy of the Auger electron is characteristic of the element on the solid surface and independent of the excitation source. And the normal range of the kinetic energies recorded in an AES spectrum would be typically from 20 to 1000 eV, corresponding to inelastic mean free path values of 2 to 6 monolayers. Therefore, it only provides the surface information of the solid.

Figure 4-3 Energy level diagram describing the process for the emission of Auger electrons.

Figure 4-4 shows a schematic diagram of an Auger spectrometer [241]. The optics for the primary beam are coincident with the cylindrical mirror analyzer. In most modern spectrometers a LaB₆ filament is used to provide high brightness. Spatial resolution of 25-50 nm may be achieved by sacrificing beam current and sensitivity. A secondary electron detector is incorporated to facilitate locating the electron beam on the sample area of interest. The focal point of the electron optics and the electron spectrometer are designed to be identical. When a sample is positioned at the focal point, the electron beam irradiates the surface, giving rise to the Auger electrons which pass through the acceptance slits into the spectrometer. A negative potential applied to the outer cylinder of the spectrometer deflects the electrons through the exit slit onto the electron multiplier. By sweeping the voltage on the outer cylinder, the electron energy spectrum may be scanned.

Figure 4-4 Schematic diagram of a cylindrical mirror analyzer Auger spectrometer. [241]

Our AES characterization was carried out using JEOL JAMP-7800F scanning Auger microscope. A Schottky field emitter is used as the electron source for generating the microprobe, and the electron beam can be made extremely fine, thus enabling high spatial resolution analysis to be carried out easily. In addition, improved energy resolution, provided by this analyzer, enables the JAMP-7800F to measure the specimen's chemical shift with Auger analysis.

4.1.1.2 X-ray photoelectron spectroscopy (XPS)

Photoelectron spectroscopy is a technique which has many similarities to AES. The same energy level diagram used to describe the Auger process may be used to describe the photoelectron process. For XPS, the use of a monochromatic excitation source is essential, since the photoelectron's kinetic energy is directly dependent on the energy of the excitation source. By knowing the energy of the x-ray with a high degree of accuracy and measuring the kinetic energy of the emitted photoelectron from the relationship:

$$BE = h\nu - KE + \phi \quad (4-2)$$

one can determine the binding energy (BE) of any electron energy level less than the photo energy. The binding energy is influenced by its chemical surroundings making BE suitable for determining chemical states. This leads to a major strength of XPS; it allows chemical identification. In addition, x-ray tends to be less destructive, making the method more suitable for organics as compared to AES.

Figure 4-5 shows a schematic diagram of a common XPS spectrometer [241]. Similar to that used for AES, it is the cylindrical mirror analyzer. A two-stage, two cylindrical mirror analyzers in tandem device is employed to enhance the energy resolution. An x-ray source, either an Al or Mg anode, mounted in proximity to the sample is used for excitation. The x-ray floods a broad area of the sample since it cannot be easily focused, unlike the electron source in AES. In our experiment, XPS investigation was performed using a VG ESCALAB 220I-XL system and Al $K\alpha$ was used as the x-ray source. The VG ESCALAB 220I-XL system is an extremely versatile XPS system. It is equipped with two types of x-ray sources (Mg $K\alpha$ and Al $K\alpha$), the twin-anode and the twin crystal monochromated source, producing spectra from areas ranging from 8 mm down to $20\ \mu\text{m}$ in diameter. The use of x-ray monochromator, the spot size of which can be selected to suit the analysis, ensures that only the area of interest is exposed to x-ray. In this case, lens and analyzer combination can be operated at maximum sensitivity.

Figure 4-5 Schematic diagram of a two-stage cylindrical mirror analyzer and x-ray source used for XPS. [241]

4.4.2 Microstructure investigation

The microstructure of the films was investigated by HRTEM. TEM was originally used for highly magnified sample images. In principle, TEM is similar to optical microscopy; both contain a series of lenses to magnify the sample. The main strength of TEM lies in its high resolution, approaching 0.15 nm when working at 400 kV.

A schematic of the TEM is shown in Figure 4-6. Electrons from an electron gun are accelerated to high voltage typically from 100 to 400 kV and focus on the sample by the condenser lenses. The sample is placed on a small copper grid a few millimeters in diameter. The static beam has a diameter of a few microns. The sample must be sufficiently thin to be transparent to electrons. The transmitted and forward scattered electrons form a diffraction pattern in the back focal plane and a magnified image in the image plane. As shown in Figure 4-6, with additional lenses, either the image or the diffraction pattern is projected onto a fluorescent screen for viewing of electrical or photographic recording. The ability to form a diffraction pattern allows structural information to be obtained.

In our experiment, the structural information was investigated by using FEI Tecnai F20 HRTEM equipped with energy dispersive x-ray spectrometer (EDX). This system has an accelerating voltage of 200 kV and a point-to-point spatial resolution of 0.24 nm.

Figure 4-6 Schematic diagram of a transmission electron microscope.

4.4.3 Thickness measurement

In our work, the thickness of the gate oxide was measured by two kinds of technique: depth profiling using AES and cross-section view using HRTEM.

4.4.3.1 High resolution transmission electron microscopy (HRTEM)

The cross-section view of the HRTEM is the only method which directly measures the interface and ultrathin film thickness. Therefore, it is the most important characterization method for ultrathin high- k gate dielectrics. In this work, the cross-section view of the thin films was examined using FEI Tecnai F20 HRTEM which is described in details previously.

Unlike AES or XPS which does not need sophisticated sample preparation process, the success of TEM observation is extremely dependent on its sample preparation. Typically, samples as thin as tens of nanometers are needed. The typical procedure for the preparation includes cutting, bonding, grinding, dimpling, polishing, and ion milling.

4.4.3.2 AES depth profiling

In the AES depth profiling, accurate in-depth element distribution is obtainable with the combination of an ion-etching technique, due to its high surface sensitivity. To obtain information about the variation of composition with depth of a sample, it is necessary to gradually remove materials from the surface region, whilst continuing to monitor and record the Auger spectra. This controlled surface etching of the analyzed region can be accomplished by simultaneously exposing the surface to an ion flux which leads to sputtering of the surface atoms. As the ion beam etches away material from the surface, the Auger signals corresponding to the elements present in this layer will rise and then decrease again. Therefore, by collecting Auger spectra as the sample is simultaneously subjected to etching by ion bombardment, it is possible to obtain information on the variation of composition with depth below the surface.

Besides AES, another depth profiling method is dynamic secondary ion mass spectrometry (SIMS). The unique advantage of SIMS is that it has unsurpassed

sensitivity and good spatial resolution which make it the main instrument for dopant profiling of semiconductor devices. The main disadvantage of SIMS is its high matrix effect, which makes quantification of the major constituents of a sample more difficult. However, this is the domain of AES that may be looked upon as the most versatile technique. Allowing surface and interface studies with optimum spatial resolution (~ 10 nm), excellent surface sensitivity ($< \sim 2$ nm depth), it has relatively small matrix effects (< 2) and the depth profiling in very thin layers up to 5 nm can be performed by AES. Therefore, sputter depth profiling using AES has become the most frequently used method for thin-film chemical analysis in materials science [242].

In our JEOL JAMP-7800F AES system, the ion etching rate is calibrated by JEOL every month using a thermally-grown 100 nm SiO_2 as the specimen. After etching for a certain period, the remnant thickness of SiO_2 is measured directly by HRTEM. The accurate etching velocity is thus obtained. Besides the calibration done on SiO_2 gate dielectrics, in our experiment, the cross-section HRTEM results of HfO_2 have also been used as the calibration tool for AES depth profiling. All these advantages make the JAMP-7800F a highly reliable, high performance Auger microprobe.

4.4.4 Electrical and dielectric characterization

The measurements of dielectric and electrical properties of high- k gate dielectrics were carried out on a Mitutoyo vibration-proof microprobing station, equipped with a

thermal chuck (Temptronic, Ramp range: 25-300 °C). The capacitance-voltage (C-V) measurements were recorded by a HP 4284A LCR meter while the current-voltage (I-V) measurements were measured by a HP 4155B semiconductor parameter analyzer.

From the I-V measurement, the leakage current density as a function of applied voltage and temperature can be extracted. As discussed in Chapter 2, the conduction mechanisms can be determined from this measurement. And the reliability properties of the gate dielectrics have also been studied by the I-V measurement.

C-V measurement was used to extract a variety of dielectric properties of bulk films and of the interface. The EOT values of the high- k gate capacitors have been derived directly from the C-V measurement. Hysteresis measurement was performed to evaluate the interface properties. Multi-frequency measurement (10k-1M Hz) was used to estimate the contact resistance.

4.5 Conclusion

The thin film deposition procedures of the HfO₂, HfSiO₄, and HfSiON are described in details in this chapter. And multiple characterization tools have been utilized to investigate the gate dielectrics properties. The chemical information has been analyzed by AES and XPS, whereas the interface structure has been examined by AES

and HRTEM, and the electrical and dielectric measurements have been carried out by HP 4155B and HP 4284A analyzer accordingly.

CHAPTER FIVE

LASER-MBE DEPOSITION OF HAFNIUM OXIDE

As discussed in Chapter 2, the conventional gate dielectric needs to be aggressively scaled down below 1.2 nm for 90 nm node CMOS technology. For the purpose of maintaining a given storage capacitance, keeping device drive current at an acceptable level as well as reducing the short-channel effects, alternative high- k gate dielectrics are being pursued as possible replacement for SiO₂. However, employing high- k gate dielectrics presents tremendous challenges. A suitable replacement gate dielectric with a high permittivity must exhibit low leakage current, compatibility with CMOS process flow, and exhibit at least the same equivalent capacitance, performance and reliability of SiO₂. Among various candidates, HfO₂ seems most promising for several reasons as discussed in Chapter 2, such that it has a high dielectric constant (20-30), large energy band gap (~ 5.68 eV), good interface properties ($D_{it} \sim 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$), low leakage current density, good reliability with long lifetime (> 10 years), lattice

parameter similar to that of Si with a small lattice mismatch ($< 5\%$), thermodynamically stable with the silicon substrate and suitable tunneling barrier height for both electrons and holes (> 1 eV) [23].

In addition to the scaling limits due to the gate oxide, as the gate length is scaled down below 50 nm, the poly-Si gate depletion problem becomes very serious [201]. There is therefore immense interest in replacing conventional poly-Si gates with metal gates. A metal gate material not only eliminates the gate depletion and boron penetration problems but also reduces the gate sheet resistance. According to the ITRS roadmap, RuO_2 , with high work function (~ 5 eV) and many additional desirable properties, is a promising candidate for pMOS transistors [24].

In this chapter, we systematically investigate the fabrication of high-quality HfO_2 thin films by using the Laser-MBE technique. The influence of the oxygen partial pressure and the effectiveness of a two-step deposition scheme on the physical and electrical properties of the HfO_2 thin films were studied by using AES, HRTEM, XPS, electrical and dielectric property measurements.

This chapter is divided into four sections. The first section discusses the optimization of deposition parameters of HfO_2 and the influence of deposition parameters on the properties of HfO_2 thin films. Next, the studies on the conduction mechanisms of

HfO₂ dielectrics are presented. In the third part, the breakdown and reliability characteristics of HfO₂ are investigated. Lastly, conductive RuO₂ has been deposited and investigated as a potential metal gate for HfO₂-based pMOS devices.

5.1 Optimization of the deposition parameters

Since neither Hf nor HfO₂ can effectively block oxygen diffusion, oxygen ions in the processing environment or in the hafnium oxide thin film can easily reach the Si surface, interact with it, and form an undesirable low- k layer at the interface between the substrate and the high- k HfO₂ dielectric film. Therefore in most cases, a considerably thick low- k layer usually exists at the HfO₂/Si interface, which will largely increase the EOT and degrade the significance of scaling down for CMOS transistors [154, 243, 244]. In recent research development, a number of methods or techniques have been employed by many researchers to suppress the formation of this low- k interfacial layer. Low temperature deposition is one of the methods attempted [153, 154], however, it generally also results in a relatively low dielectric constant and poor leakage current property. Thus, how to effectively suppress the formation of this low- k layer in the deposition process is a challenging issue in alternative high- k dielectric materials for Si CMOS and for nanoelectronics applications.

In our work, the effect of oxygen partial pressure on the HfO₂ film properties is studied. In addition, a two-step deposition scheme on HfO₂ film growth and properties

are also presented and discussed. By a delicate control of the oxygen partial pressure as well as the introduction of the two-step deposition scheme, high quality HfO_2 thin films have been deposited and characterized.

5.1.1 Effect of O_2 partial pressure

The effect of oxygen partial pressure during the deposition process in the Laser-MBE chamber on the formation and growth of the interfacial low- k layer was studied by fabricating a set of 15-nm-thick HfO_2 films at 500 °C under different oxygen partial pressure as listed in Table 5-1.

Table 5-1 Fabrication of HfO_2 films in different oxygen partial pressure ambient.

Sample	Oxygen partial pressure (sccm/ Pa)	Argon gas flow (sccm)	Deposition pressure (Pa)
A1	30/3	0	3
A2	$3/3 \times 10^{-1}$	20	3
A3	$0.3/3 \times 10^{-2}$	22	3
A4	$0.1/1 \times 10^{-2}$	22.2	3

As expected for growth of any oxide thin films, oxygen partial pressure plays a very important and critical role in depositing this high- k hafnium oxide film. Figure 5-1 depicts the AES depth profiles of the four samples listed above. It is seen from Figure 5-1 that with the decrease of oxygen partial pressure from 3 to 3×10^{-2} Pa, the thickness of the interfacial silicate layer between the silicon substrate and HfO_2 is effectively reduced from 6.0 to 3.2 nm [245]. Although the Auger electron profiles do

not give a directly visual picture like the lattice image by TEM, the above AES data, however, clearly demonstrate the trend of thickness reduction for the interfacial low- k layer with lowering the oxygen partial pressure in the Laser-MBE deposition chamber. But with further decreasing the oxygen pressure to 1×10^{-2} Pa, the thickness of the interfacial layer remains almost the same as that of the sample deposited at 3×10^{-2} Pa oxygen partial pressure, indicating that there might be some limiting factors for completely suppressing the formation of this low- k interfacial layer. Post deposition annealing could be one of the main factors attributing to it.

Figure 5-1 AES depth profiles of the $\text{HfO}_2/\text{p-Si}$ films deposited at different oxygen partial pressure.

It is clearly noted that with the reduction of the oxygen partial pressure, the interface growth has been effectively suppressed. However, it could also result in another serious problem: oxygen deficiency which deteriorates the electrical and dielectric properties of oxide thin films. In our work, AES was employed again to determine the stoichiometry of the HfO_2 deposited under different oxygen partial pressure. Figure 5-2 shows the Auger differential spectra of sample A1 after 6 seconds ion etch. And the concentration ratio between hafnium and oxygen can be calculated by the spectra together with the relative sensitivity factors (RSF).

Figure 5-2 Auger differential spectra of sample A1.

By conducting the Auger analysis on all the four samples, the relative concentrations of the elements have been calculated and listed in Table 5-2. As indicated in Table 5-2, the ratio between Hf and O increases with the reduction of oxygen. Sample A1 and A2 show a little bit oxygen-rich. Sample A3 is slightly oxygen-deficient with a Hf/O ratio of 1:1.8. However, the oxygen-deficiency problem in sample A4 (with a Hf/O ratio of

1:1.4) is considerably serious suggesting that such low oxygen partial pressure is not favorable for HfO_2 deposition.

Table 5-2 Relative Concentration of the Elements (at.%).

Element Sample	Hf/O ratio	C	Si	Na	P	K
A1	28:62 (1 : 2.2)	3	5	-	-	2
A2	30:64 (1 : 2.1)	2	3	-	1	-
A3	33:61 (1 : 1.8)	2	4	-	-	-
A4	40:56 (1 : 1.4)	1	3	-	-	-

Furthermore, another important issue should also be considered. Although low oxygen pressure deposition can yield a higher k value, the leakage current density will increase due to the increase of the content of oxygen vacancies, which act as electron donors to the samples. However, from the I-V measurement of this series of samples as shown in Figure 5-3, except sample A4, there is only slight increase about the leakage current density as the oxygen pressure decreases. Compared to sample A1, sample A3 shows only about one order in the increase of leakage current density. In addition, compared to the SiO_2 with the same EOT value of 5 nm, Sample A3 exhibits at least three orders of reduction in leakage current density. Meanwhile, it is also noted in Figure 5-3 that the leakage current density of sample A4 is much larger than those of other three samples, which could be attributed to the over-lowered oxygen partial pressure, and therefore the large content of oxygen vacancies in Sample A4. This observation is consistent with our previous Auger study listed in Table 5-2.

Figure 5-3 Current-voltage measurement of Pt/HfO₂/Si capacitors deposited at different oxygen partial pressures.

The suppression to the growth of this interfacial low- k layer has direct impact on the improvements of the dielectric properties of our Laser-MBE prepared high- k HfO₂ capacitors. Figure 5-4 shows the high frequency (1M Hz) C-V measurement for samples A1 – A4 listed in Table 5-1. It is clearly seen that the capacitance increases with the decrease of the oxygen partial pressure, and sample A3 and A4 with lowest interfacial layer thickness exhibit the largest capacitance value of about 70 pF. Another issue should be pointed out is that with the decrease of oxygen partial pressure, the flat band voltage has a leftward shift on the CV curve. This can be attributed to the increase of fixed oxide charge as the oxygen partial pressure decreases.

Figure 5-4 High frequency CV measurement of Pt/HfO₂/p-Si capacitors deposited at different oxygen partial pressures.

The reduction of the oxygen partial pressure during the deposition process has yielded much better capacitance and EOT values. The above C-V and I-V experimental results show that further decrease of oxygen partial pressure to an overly low level such as 1×10^{-2} Pa does not provide an overall beneficial improvements to the high- k HfO₂ gate dielectric properties; and therefore, the oxygen partial pressure was fixed at 3×10^{-2} Pa in our subsequent Laser-MBE deposition process.

Figure 5-5 summarizes the relationship between EOT and physical thickness for HfO₂ deposited at 3×10^{-2} Pa oxygen partial pressure. For an ideal capacitor, with the scaling of the gate dielectrics, the EOT should also decrease. It is consistent with our results that at first with the thickness reduced from 20 to 7 nm, the EOT value was linearly

scaled. However, further thickness reduction to 4 nm and 2.5 nm didn't have any positive impact on the scaling of EOT value. This could be attributed to the diffusion of oxygen into the interface of HfO_2/Si . Oxygen can easily penetrate such a thin HfO_2 layer and react with Si substrate to form SiO_2 . Therefore, thicker interface is supposed to form as the scaling of HfO_2 layer.

Figure 5-5 The relationship between EOT and physical thickness for HfO_2 deposited at 3×10^{-2} Pa oxygen partial pressure.

Figure 5-6 shows the cross-section image of the 2.5-nm-thick HfO_2 film. And it is clearly observed that a 2.5-nm-thick interfacial layer exists in between the HfO_2 and the Si. Therefore, the process parameter should be further optimized in order to keep the scaling of EOT.

Figure 5-6 Cross section of a 2.5-nm-thick HfO_2 deposited at 3×10^{-2} Pa oxygen partial pressure.

5.1.2 Two-step deposition scheme

In this two-step deposition scheme, a hafnium metal layer was first deposited onto the Si substrate in an ultrahigh vacuum of 1×10^{-6} Pa at 200 °C, then the substrate temperature was raised up to 500 °C, and HfO_2 film was subsequently deposited onto the Hf layer in Ar/ O_2 ambient while keeping the optimized oxygen partial pressure at 3×10^{-2} Pa. Two batches of HfO_2/Hf stacked samples were prepared to investigate the effect of this two-step deposition scheme, as listed in Table 5-3.

Table 5-3 Structure of the HfO_2/Hf stacks.

Sample No.	B1	B2	B3	B4	B5	B6	B7	B8
Hf (nm)	0	1	2	3	4	3	3	3
HfO_2 (nm)	4	4	4	4	4	6	13	18

In the first batch of samples, the thickness of the HfO_2 was fixed at 4 nm while varying the thickness of the buried Hf layer from 0 to 4 nm (Samples: B1- B5); for samples in the second batch, thickness of the buried Hf layer was fixed at 3 nm while the HfO_2 thickness was varied from 6 to 18 nm (Samples: B6 – B8). PDA was performed ex-situ in a RTA chamber at 500 °C for 30 seconds in N_2 ambient with residual O_2 . Since oxygen ions can penetrate through both Hf and HfO_2 , Hf layer was oxidized into HfO_2 during the annealing [154].

Figure 5-7 shows the high frequency (1M Hz) C-V measurement of samples with different thicknesses of Hf buried layers. Sample B1 and B2 give almost the same capacitance value, and their effective dielectric constant is calculated to be about 8. The capacitance value of Sample B3 is slightly larger than B1 and B2, and its effective dielectric constant is estimated to be about 10.

Figure 5-7 High frequency C-V measurement on Pt/HfO₂/Si capacitors with different Hf buried layers.

The low dielectric constant values of these samples, less than reported value of about 20-30 for HfO₂ are believed to be mainly due to the formation of the thick low- k interfacial layer at the HfO₂/Si interface. Sample B4 shows the largest capacitance value, its effective dielectric constant is calculated to be 19.5, and thus the EOT value for sample B4 is determined to be 1.4 nm. The C-V curve for sample B5, which is not shown in Figure 5-7, is not an ideal curve for MOS capacitor, suggesting that under the currently used PDA treatment scheme the 4-nm-thick Hf metal layer cannot be fully oxidized into HfO₂ and the residual Hf metal layer at the interface is believed to be the primary reason for the poor dielectric property for sample B5.

Figure 5-8 (a) shows the cross-section HRTEM image of the as-deposited sample B4 [246]. The as-deposited sample is very smooth and it shows a sharp interface almost without interface reaction between HfO_2 and the Si substrate. This may be attributed to the relatively thick Hf metal layer and low oxygen partial pressure ambient. After RTA of the sample in N_2 for 30 seconds, an interfacial layer, brighter in contrast and less than 0.4 nm thick, can be observed in Figure 5-8 (b). And the interfacial layer remains in amorphous state and still very smooth at the interface. This result suggests that this two-step deposition scheme effectively inhibits the growth of interface layer and enhance the thermal stability of the film. In addition, there is a bright line just below the oxide layer, which is attributed to the artifacts of the TEM during the process of image capturing.

The cross-section images of sample B6 which also contains a 3-nm-thick buried Hf layer are illustrated in Figure 5-9. Again, the interface shows almost unchanged after the thermal annealing indicating the effectiveness of this two-step deposition scheme.

(a)

(b)

Figure 5-8 Cross-section TEM images of sample B4. (a) As-grown film; (b) annealed in N_2 at 500 °C for 30 s.

(a)

(b)

Figure 5-9 Cross-section TEM images of sample B6. (a) As-grown film; (b) annealed in N₂ at 500 °C for 30 seconds.

Chemical compositions of sample B4 were characterized by XPS. Figure 5-10 shows the Hf 4f features for the as-received film and samples annealed at 500 °C and 950 °C. A feature peak is found in the range of 16-19 eV, indicating the forming of Hf-O bonding [173]. For samples treated by RTA in nitrogen, the feature peak shifts gradually to the deeper binding energy. This observation indicates the decrease of Hf-O bonds after N₂ annealing.

Figure 5-10 Hf 4f XPS data from HfO₂ films annealed at different temperatures.

The Si 2p features for the same annealing sequence are shown in Figure 5-11. The peak at 99.4 eV is attributed to pure Si of the substrate. Another peak at higher binding energy originates from the interfacial Si⁴⁺ oxide. Upon RTA annealing, the oxide feature shifts continuously to the shallower binding energy. Since Hf is more electropositive than Si, insertion of Hf ion to form an Hf-O-Si complex would reduce the ionicity in the Si-O bond [247-249]. Thus it could reduce the Si 2p binding energy.

As a result, this energy shift indicates that hafnium silicate is probably formed at the interface during the RTA annealing which is consistent with the AES depth profiling results shown in Figure 5-1.

Figure 5-11 Si 2p XPS data from HfO₂ films annealed at different temperatures.

Figure 5-12 shows the O 1s features for these samples. For all the samples, the O 1s peak is located around 532 eV indicating the oxygen is in the form of Hf-O bonding. In addition, the feature peak does not shift as the annealing temperature increases which suggests that the total number of the Hf-O bonds after the RTA is almost unchanged and the films are stoichiometric and thermodynamically stable on Si.

In order to further investigate the thermal stability of sample B4, the films have been annealed under different temperatures from 500-950 °C for 30 seconds, and the EOT and J values have been measured accordingly. As indicated in Figure 5-13, even after

annealing at 950 °C for 30 seconds, the EOT increase of the gate capacitor is less than 0.4 nm. And the leakage current is about one order lower than the sample annealed at 500 °C. These results indicate that after the optimization, the HfO₂ films show immunity to high temperature thermal budget.

Figure 5-12 O 1s XPS data from HfO₂ films annealed at different temperatures.

Figure 5-13 I_g and EOT change after different thermal treatments.

Figure 5-14 shows the EOT values for the second batch samples calculated from their measured C-V curves. The value of effective dielectric constant is calculated to be around 20 in all these samples. The good linear fitting plot for EOT versus the thickness of HfO_2 thin films indicates that the interfacial layer is independent of the HfO_2 thickness and this interfacial layer is formed at the onset of the film deposition [153, 154]. The value of the linear curve intercept at the y-axis is determined to be 0.88 nm, which is associated with the thickness of the interfacial layer. This thin interfacial layer is attributed to the employment of the two-step deposition method.

Figure 5-14 EOT as a function of HfO_2 thickness.

In summary, the experimental results show that the thickness of the interfacial layer depends strongly on the oxygen partial pressure in the Laser-MBE chamber during the deposition process. With the reduction of the oxygen partial pressure to an optimized level, the growth of the low- k interfacial layer has been substantially controlled. A

two-step deposition method has been adopted to further reduce the thickness of the interfacial layer. It is found that a 3-nm-thick Hf buried metal layer can effectively block the oxygen diffusion into the Si substrate, and thus largely suppress the growth of the interfacial layer. In addition, it is also found that the interfacial layer is formed at the early stage of the HfO_2 deposition and its growth is independent of the thickness of high- k HfO_2 gate dielectric films.

5.2 Current conduction mechanisms in HfO_2

In order to replace the SiO_2 with high- k gate dielectrics, many challenging issues should be considered and investigated. The current transport is one of the most critical issues in gate dielectrics since the major concern to use high- k materials is to suppress the leakage current [23], and therefore, understanding of the conduction mechanism in the HfO_2 gate dielectrics is essential and very critical.

In our work, we investigated the electrical properties of Pt/ HfO_2 /p-Si gate stacks with EOT values ranging from 1.4 to 4.1 nm. The conduction mechanisms in these HfO_2 gate dielectrics as a function of temperature and electric field were discussed.

The temperature and electric field dependence of I-V for the HfO_2 /Si capacitors were systematically studied to elucidate the electrical conduction mechanisms. It is found from I-V measurements on all the samples with different thickness that the conduction

mechanism shows almost on dependence on the oxide thickness. Therefore, the HfO_2 film with an EOT value of 1.4 nm has been investigated here for the conduction mechanisms in such Laser-MBE prepared gate dielectrics.

Figure 5-15 shows the I-V characteristics of a Pt/7 nm HfO_2 (EOT = 1.4 nm)/p-Si capacitor from 25 °C to 275 °C. The capacitor was driven in accumulation condition and J was measured under gate injection. It is clearly seen that at the electric field $E < 4.0$ MV/cm, the leakage current depends on the temperature, suggesting that either the Schottky emission or PF mechanism dominates the conduction in this region. Meanwhile, in the high electric field range of $4.0 \text{ MV/cm} < E < 6.0 \text{ MV/cm}$, all I-V curves are nearly temperature independent, indicating that either direct or FN tunneling is the main conduction mechanism.

Figure 5-15 I-V characteristics of Pt/ HfO_2 / p-Si capacitor at different temperatures.

The PF plot of the leakage current behaviors is depicted in Figure 5-16. It is noted that in the electric fields $E < 1.0$ MV/cm and 4.0 MV/cm $< E < 6.0$ MV/cm, the curves do not show any linear relationship, suggesting that the PF conduction mechanism is ruled out in these regions.

Figure 5-16 PF plot of the leakage current characteristics at different temperature.

However, in the electric field 1.0 MV/cm $< E < 4.0$ MV/cm, a linear fit is observed, which indicates that PF maybe the possible conduction mechanism. To further confirm the validity of the PF conduction mechanism, the dynamic dielectric constant ϵ_r is derived from the slope of this region. In ideal case, if PF is the dominant conduction mechanism, the extracted ϵ_r should correspond to n^2 where n is the refractive index of the dielectric material [181]. The calculated ϵ_r is 3.9. It is close to n^2 of the HfO_2 films ($n = 2.0$ - 2.2) in optical frequency range [250-252]. Based on

the above evidence, the PF conduction model is confirmed as the dominant mechanism in this electric field region.

Figure 5-17 shows the curve of $\ln(J/E)$ vs. $1/T$. The well-behaved linear fit confirms our results again that PF dominates this region, and the value of trap depth ϕ_t in HfO_2 thin film is obtained to be 0.75 eV from the slope.

Figure 5-17 Poole-Frenkel emission plot of $\ln(J/E)$ vs. $1/T$.

In the electrical field $E < 1.0$ MV/cm, the current is temperature dependence but the PF is not the dominant conduction mechanism. According to the Schottky emission model, the I-V behavior in this field range is perfectly fitted with the linear relationship of $\ln(J/T^2)$ versus $E^{1/2}$ as required, shown in Figure 5-18. However, O'Dwyer [253] pointed out that owing to the space-charge effect, a good linear

Schottky plot does not essentially imply a Schottky emission. Only if the derived dynamic dielectric constant is consistent with n^2 , it can then ensure the Schottky emission conduction mechanism. From the slope of Figure 5-18, ϵ_r is determined to be 5.1, which is close to n^2 of the HfO_2 films ($n=2.0$ - 2.2) [250-252]. Hence, in the low field $E < 1.0$ MV/cm, the Schottky emission model is confirmed to be the conduction mechanism.

Figure 5-18 Schottky emission plot of $\ln(J/T^2)$ vs. $E^{1/2}$.

Figure 5-19 depicts the characteristics of the FN plot of the leakage current behavior in the high electric field range of $4.0 \text{ MV/cm} < E < 6.0 \text{ MV/cm}$. The data are fitted very well in straight lines, indicating that FN tunneling is the main conduction mechanism in this electric field region.

Figure 5-19 FN tunneling plot of $\ln(J/E^2)$ vs. E^{-1} .

In conclusion, the conduction mechanisms in the HfO_2 gate dielectric have been systematically investigated, and it is found that the Schottky model is the main conduction mechanism at low electric field of $E < 1$ MV/cm; the PF conduction mechanism is dominant in the medium field range of $1 \text{ MV/cm} < E < 4 \text{ MV/cm}$; with further increasing electrical field into the high region of $4 \text{ MV/cm} < E < 6 \text{ MV/cm}$, the current behavior turns to the FN tunneling conduction.

5.3 Breakdown and reliability of HfO_2 gate dielectrics

For the SiO_2 gate dielectrics, the breakdown mechanisms generally follow a two-stage model, degradation of the SiO_2 film succeeded by the oxide breakdown [254, 255]. In the first stage, the injection of the hot electrons and the migration of hydrogen degrade the Si/ SiO_2 interface by the creation of fast interface states and charged slow traps

[256-258]. While in the second step, both soft breakdown (SBD) and hard breakdown (HBD) have been identified in the SiO_2 gate dielectrics [59]. The SBD and HBD are believed to have the same physical origin which results from a weak localized path between the gate electrode and the substrate, caused by the degradation of the oxide in the first step. The transformation from SBD to HBD is determined by the location of oxide breakdown spots, thermal energy for device discharge, and resistance of the percolation path [259].

As in SiO_2 , high- k gate dielectrics also exhibit both SBD and HBD characteristics [260]. However since high- k gate stack is basically a multi-layer structure (containing the bulk oxide and the interface layers), the origin of the SBD in high- k gate dielectrics could be quite different from SiO_2 . In addition, in SiO_2 dielectrics, either SBD or HBD could be the first breakdown. But in the high- k case, SBD has predominantly observed as the first breakdown.

In our experiment, the MOS capacitor was stressed at a constant voltage (CVS) mode in accumulation condition (gate injection) and the stress voltage was set from -4.5 to -5.5 V. In this stress area, SBD has been predominantly observed as the first breakdown. And the time between SBD and HBD significantly decreases as the stress voltage increases. Figure 5-20 depicts the SBD and HBD events in HfO_2 ($\text{EOT} = 1.4$

nm) with the CVS of -4.5 V. It is observed that several SBD occurred before the final HBD of the device.

Figure 5-20 Leakage current density vs. constant voltage stress time.

The breakdown statistics provides important information about the dielectric strength of a film, such as its intrinsic bonding strength, defect density, surface roughness, oxide impurities, material quality, and process uniformity. And this statistics distribution is usually described by the Weibull distribution using the following equation:

$$F(x) = 1 - \exp\left[-(x/\alpha)^\beta\right] \quad (5-1)$$

Where F is the cumulative failure probability, x is the time, α is the characteristic lifetime where 63.2% of the samples fail, and β is called the slope parameter which is an important parameter when evaluating the gate-oxide reliability [64]. In the case of SiO_2 , β becomes smaller as the gate oxide scaling and approaches 1 as the thickness

is smaller than 3 nm [64]. Therefore, a larger β is usually desirable for the reliability consideration. Figure 5-21 shows the HBD Weibull distribution of the HfO_2 (EOT = 1.4 nm) under different CVS from -4.5 to -5.5 V.

Figure 5-21 Weibull distribution of 1.4-nm HfO_2 dielectrics for various stress voltages.

The Weibull distribution results show that β increases with the reduction of the stress voltage but there is no significant difference in the Weibull slope as the stress voltage changes, implying the same effective defect radius and physical breakdown mechanisms. And the relatively large β around 2.0 also indicates that the HfO_2 gate dielectrics shows good reliability properties.

A forward and back sweep of C-V measurement known as a hysteresis measurement can be used to monitor trapped charges by obtaining the difference in the flat band

voltage. The temperature dependence of the hysteresis is a good indicator of dielectric properties. Figure 5-22 shows the C-V measurements of a 2.2-nm thick (EOT) HfO_2 films which were performed at elevated temperature. At room temperature, the film showed negligible hysteresis which indicates excellent interface and bulk property. However, as the temperature increased to 150 °C, the films exhibited large clockwise hysteresis of > 100 mV at flat band.

The hysteresis can be attributed to the slow states buried at shallow depths in the conduction band [261]. These states could not be filled or emptied on changing dc bias and do not contribute to capacitance at room temperature under high-frequency measurement. However at elevated temperature, because the emission time of these states was reduced to a moderate value, these states contributed to form a nonequilibrium capacitance. Still, the emission time was not low enough to reach the equilibrium capacitance value. Thus, hysteresis occurred during the forward and backward bias sweep. Furthermore, the flat band voltage shows a positive shift as the temperature increases indicating that negative charges are activated at high temperature.

Figure 5-22 C-V hysteresis measurement performed at different temperatures.

Figure 5-23 shows the SILC (stress induced leakage current) characteristics of the HfO₂ gate dielectrics under CVS mode after 500-2000 seconds. SILC is defined as the

difference in leakage current after stress. The physics behind it is still not fully understood but general consensus exists about the fact that it is due to trap-assisted conduction. A model which is based on trap-assisted tunneling suggests that stress induced leakage is attributed to the tunneling of electrons from the valence band assisted by the stress-induced traps [262]. In Figure 5-23, the leakage current density shows only a slight increase after 2000 seconds stress indicating that few traps had been generated by the stress.

Figure 5-23 SILC characteristics of HfO₂ under constant voltage stress.

5.4 Effect of RuO₂ electrode on HfO₂ gate dielectrics

When the transistor gate length is scaled down below 50 nm, the depletion of poly-Si will become a very serious problem due to the active dopant density saturation [24,

263]. Hence, alternative gate electrodes should be employed to replace the poly-Si gate in future MOSFET device with dimension of 50 nm or below [264-266].

According to the ITRS roadmap, electrode materials with high work function (~ 5 eV) such as Pt, Ru, Ni and RuO_2 are promising candidates for pMOS transistors [24]. RuO_2 , especially, has many additional desirable properties such as good integration with high- k dielectrics, good etching properties, excellent thermal stability, and inhibition to the oxygen diffusion [267-271]. Therefore, in this work, RuO_2 has been deposited as the gate electrode which is described in detail in Chapter 3, and the effect of RuO_2 electrode on HfO_2 has been systematically studied.

5.4.1 Structure properties

The XRD pattern of the sputtered RuO_2 film is shown in Figure 5-24. It is clearly seen from this figure that even though the film was deposited at room temperature, the RuO_2 is in the polycrystalline phase and the diffraction peaks match the stoichiometric RuO_2 crystal phase [267].

5.4.2 Resistivity

The resistivity change of RuO_2 films as a function of RF power of the sputtering is shown in Figure 5-25. It is observed that with the increase of RF power, the resistivity has been reduced continuously. At an RF power of 100 W, the resistivity of RuO_2 is

about $2000 \mu\Omega \cdot \text{cm}$. However when the RF power increasing to 300 W, the resistivity of RuO_2 is reduced to $400 \mu\Omega \cdot \text{cm}$, suggesting that high RF power deposition is desirable for the RuO_2 fabrication.

Figure 5-24 X-ray diffraction of the sputtered RuO_2 film.

Figure 5-25 The resistivity of RuO_2 as a function of RF power.

Figure 5-26 shows the variation of resistivity and thermal stability of RuO₂ gate electrode. The resistivity of the RuO₂ keeps a constant value of 400 $\mu\Omega \cdot \text{cm}$ up to RTP annealing at 500 °C in N₂ for 30 seconds and abruptly reduced to 250 $\mu\Omega \cdot \text{cm}$ as the annealing temperature increased to 600 °C. The minimum resistivity value of 100 $\mu\Omega \cdot \text{cm}$ is obtained after annealed at 800 °C in N₂ for 30 seconds. The decrease of resistivity is thought to be caused by the improvement of the crystallinity of RuO₂ films. Thus the RuO₂ shows very promising thermal stability and resistivity properties as the candidate of an alternative gate electrode.

Figure 5-26 The resistivity of RuO₂ as a function of annealing temperature.

5.4.3 Capacitance-voltage characteristics

The C-V measurement of RuO₂/HfO₂/Si gate stack at various frequencies is depicted in Figure 5-27. As seen from the figure, when $V_g < -0.75$ V, the MOS capacitor in depletion shows almost no dependence on the frequency. However, when the V_g is

further increased from -0.75 to 0.3 V, the capacitor, changed from inversion to accumulation, exhibits some capacitance dispersion which may be caused by the presence of the leakage current and the excessive series resistance as discussed by Norton [272]. In such a case, the low frequency data is not quite reliable, and therefore the capacitance measured at 1 MHz is used to calculate the more accurate EOT. The accumulation capacitance measured at 1 MHz is 260 pF and the corresponding EOT value of 1.3 nm is thus obtained.

Figure 5-27 C-V measurement of RuO₂/HfO₂/Si gate stack at different frequencies.

A hysteresis measurement was performed to monitor the trap charges from the difference in the flat band voltage. As shown in Figure 5-28, the well-behaved C-V curve exhibits negligible flat band shift and hysteresis (< 10 mV), indicating that there is minimal charge trapping in the capacitor [38].

Figure 5-28 Hysteresis measurement of RuO₂/HfO₂/n-Si capacitor.

5.4.4 Work function extraction

5.4.4.1 Work function extraction methodology

Two methods are described here in order to calculate the work function of the RuO₂ gate electrode.

In the first method, under the assumption that the fixed oxide charge in the dielectric qN_{eff} is mainly located at the HfO₂-Si interface, which means that the effective charge density N_{eff} is independent of the dielectric thickness, the work function ϕ_m can be described as below [38]:

$$\phi_m = \phi_{Si} + V_{FB} + \frac{qN_{eff}}{\epsilon_{ox}} t_{ox} \quad (5-2)$$

where ϕ_{Si} is the work function of the Si substrate, t_{ox} is the oxide thickness and q is the electric charge. Under the above assumption, V_{FB} is measured as a function of t_{ox} . A straight line plot of V_{FB} versus t_{ox} yields a slope equal to qN_{eff}/ϵ_{ox} , and then N_{eff} can be derived. Meanwhile, since ϕ_{Si} is known, the value of ϕ_m can also be obtained at the interception for $t = 0$. This method is generally used in the extraction of the work function [38, 267, 268].

In addition, the work function value of ϕ_m can also be obtained by comparing the flat band voltage shifts of MOS capacitors made using different gate electrodes [38]. To obtain the ϕ_{RuO_2} , the value of ϕ_m for another metal electrode should be known independently from a photoemission measurement for reference and comparison purposes. From the high frequency C-V curves taken using the reference and RuO₂ gate metals, the difference in flatband voltage can be directly determined. In addition, the terms in equation (5-2) due to qN_{eff} can be cancelled out because qN_{eff} is the same for the two capacitors, then equation (5-2) can be rewritten as:

$$(V_{FB})_{reference} - (V_{FB})_{RuO_2} = \phi_{reference} - \phi_{RuO_2} \quad (5-3)$$

If $\phi_{reference}$ is known, ϕ_{RuO_2} can then be calculated. Unlike the first method, this method is seldom used in the extraction of metal work function. In our work, we also employ this method to verify the validity of the work function result extracted from the first method.

5.4.4.2 Work function extraction

In order to determine the work function of the RuO_2 gate, we fabricated the $\text{RuO}_2/\text{HfO}_2/\text{n-Si}$ capacitors with different HfO_2 thickness as listed in Table 5-4.

The C-V curves were measured on all the capacitors and the values of V_{FB} were recorded. As previously discussed, a straight line plot of V_{FB} versus t_{ox} , as shown in Figure 5-29, yields a slope equal to qN_{eff}/ϵ_{ox} ; and at the interception for $t = 0$, the value of ϕ_{ms} can also be obtained. Since ϕ_{Si} is known, the work function value of RuO_2 extracted from the linear least-square fit is derived as about 4.98 eV.

Table 5-4 Nominal and measured HfO_2 thickness.

Nominal HfO_2 thickness (nm)	Measured EOT (nm)
6.0	1.3
8.0	1.6
10.0	2.2
15.0	2.7
20.0	4.4

Table 5-5 Summary of the research on RuO_2 as the gate electrode. [267, 268, 273]

Gate stack	EOT Thickness (nm)	Fabrication method	ϕ_m (eV)	N_{eff} (cm^{-2})
$\text{RuO}_2/\text{SiO}_2$ [268]	6.5-25	Evaporation/ Thermal	5.06	2.5×10^{12}
$\text{RuO}_2/\text{Al}_2\text{O}_3$ [268]	5-15	Evaporation/ ALCVD	5.17	2.3×10^{12}
$\text{RuO}_2/\text{Y}_2\text{O}_3$ [268]	3-9	Evaporation/ E-Beam	5.0	-8.2×10^{12}
$\text{RuO}_2/\text{ZrSiO}$ [267]	2.7	Sputtering/ MOCVD	5.1	—
$\text{RuO}_2/\text{ZrO}_2$ [267]	2.9	Sputtering/ MOCVD	—	—
$\text{RuO}_2/\text{HfO}_2$ [273]	1.3-4.4	Sputtering/ LMBE	4.98	3.3×10^{12}

Figure 5-29 Flatband voltage (V_{FB}) shift as a function of oxide thickness.

As listed in Table 5-5, this is almost the same as the results reported by other research groups. In addition, the calculated effective fixed oxide charge is positive with a density of $3.3 \times 10^{12} \text{ cm}^{-2}$. However, Tapajna reported that the fixed oxide charge is negative with a density of $-3.3 \times 10^{12} \text{ cm}^{-2}$ [271]. Since N_{eff} is sensitive to the processing used to fabricate the dielectrics, different fabrication method of the HfO_2 could contribute to it.

In the second method, in order to obtain ϕ_{RuO_2} , the value of ϕ_m for another metal electrode should be known independently. Since Pt is a well known noble metal electrode and its work function has been widely investigated in many cases [244-247], therefore, it was chosen as the other electrode in this study. The Pt top electrode with (111) orientation was deposited using the same RF sputtering system. The reported

work function value of 6.08 ± 0.15 eV for Pt (111) has been well determined by the photoemission measurement [244-246]. From the high frequency C-V curves shown in Figure 5-30, the V_{FB} difference is estimated to be about 1.2 eV. Hence, derived from equation (5-3), the work function of RuO_2 is calculated to be 4.88 ± 0.15 eV which is in good agreement with the value obtained from the first method. The above results indicate that this method is also valid to determine the work function of metal gates.

Figure 5-30 High frequency C-V measurement with two different metals used as the gate electrode.

5.4.5 Current-voltage characteristics

The leakage current density versus gate voltage of $\text{RuO}_2/\text{HfO}_2/\text{n-Si}$ is shown in Figure 5-31. It is seen in this figure that the very low leakage current density of this MOS of $1.5 \times 10^{-2} \text{ A cm}^{-2}$ at 1V is observed, which is at least 4 orders of magnitude lower

than that of SiO₂ with the same thickness of 1.3 nm. In addition, this MOS capacitor shows a very high breakdown strength of > 10 MV/cm.

Figure 5-31 I-V measurement for the RuO₂/HfO₂/n-Si capacitor.

In summary, the RuO₂/HfO₂/n-Si MOS capacitors show good dielectric and electrical properties: (1) the negligible flat band voltage shift from the hysteresis measurement, indicates that the trap charge density is very low; (2) the work function value of 4.98 eV for the RuO₂ top electrode obtained from the high-frequency C-V measurement, is suitable and high enough for the pMOS gate application; and (3) the effective fixed oxide charge density is $3.3 \times 10^{12} \text{ cm}^{-2}$. The MOS capacitors also show a very strong breakdown strength (> 10 MVcm⁻¹), at least 4 orders in magnitude for the leakage current density reduction compared to that of the SiO₂ with the same equivalent oxide

thickness. These results reveal that RuO_2 is a promising candidate for pMOS technology.

5.5 Conclusion

In summary, our results have demonstrated that HfO_2 gate dielectrics can be deposited on Si substrates without the formation of low- k interfacial layer. And these films also exhibit acceptable leakage current densities, good dielectric properties, excellent breakdown strength and high reliability. Figure 5-32 shows the leakage current densities of the HfO_2 with an EOT thickness of 1.3 nm, and it is clearly seen that compared to the conventional SiO_2 with the same EOT, the leakage current density in HfO_2 is about 4 orders of magnitude lower.

Figure 5-32 The Leakage current density comparison between HfO_2 and SiO_2 with the same EOT of 1.3 nm.

The investigation of the conduction mechanisms in the HfO_2 gate dielectric demonstrates that the Schottky model, PF model and FN tunneling dominate the conduction mechanisms in different electric field regions as shown in Figure 5-33.

Figure 5-33 Conduction mechanisms of HfO_2 gate dielectrics in different electric field region.

In addition to Pt electrode, RuO_2 has been investigated as a novel gate material for pMOS technology. RuO_2 has good thermal stability and acceptable resistivity. And the $\text{RuO}_2/\text{HfO}_2/\text{n-Si}$ MOS capacitors show good dielectric and electrical properties.

CHAPTER SIX

LASER-MBE DEPOSITION OF HAFNIUM SILICATE

Although HfO_2 has many excellent characteristics for gate dielectric applications as studied in the previous chapter, it also has several drawbacks that limit its potential as a gate oxide. Some of the limiting factors include relatively low crystallization temperature ($< 600\text{ }^\circ\text{C}$) and boron penetration in pMOSFET [23]. The crystallized gate dielectrics suffer from large leakage through the grain boundaries.

To reduce electrical leakage and dopant diffusion along the grain boundaries, it is desirable to choose a dielectric that can stay in the amorphous phase after high temperature annealing ($> 900\text{ }^\circ\text{C}$). In addition, to prevent the advantages gained from employing a high- k dielectric to be negated, the material must not be prone to reactions with the Si substrate which results in an interfacial SiO_2 layer formation.

In order to not only take the advantages of HfO_2 but also overcome its limitations, we have studied hafnium silicate films by doping Si into HfO_2 . Based on the desirable properties for a gate dielectric material mentioned above, hafnium silicate is a promising candidate which has many favorable properties listed as below [173]:

- (1) Hafnium silicate is thermally stable in direct contact with Si ($> 1050^\circ\text{C}$);
- (2) By incorporating a suitable level of Si into HfO_2 , hafnium silicate can yield lower leakage current than HfO_2 with the same EOT due to its larger band gap and heavier effective mass for electron tunneling;
- (3) The use of hafnium silicate allows the control of the Si interface which removes the key obstacle that limited other gate dielectric scaling. Therefore, although the dielectric constant of hafnium silicate is substantially lower than that of HfO_2 , this tradeoff for interface control will still be acceptable as long as the resulting hafnium silicate is beneficial to provide a smooth interface with Si and reduce the interfacial charge densities and leakage current.

The role of nitrogen in gate oxides has been extensively studied in recent years [278-284]. The nitrogen incorporation in the gate dielectrics provides an increase of the dielectric constant. For instance, the currently-used gate oxide in the 90 nm technology is SiON which has a dielectric constant slightly larger than that of pure SiO_2 . In addition, nitrogen can inhibit the boron penetration as well as the oxygen

diffusion through the gate oxide. Thus it can help improve the interface quality which finally results in a decrease of EOT value and gate leakage.

In this work, hafnium silicate has been fabricated by Laser-MBE. And the concentration ratio of Hf in hafnium silicate has been properly adjusted in order to achieve the desirable electrical and dielectric properties. HRTEM and AES have been used to investigate the interface growth and to illustrate the scaling limit of this gate oxide. Furthermore, based on the hafnium silicate, nitrogen is doped in order to further enhance the gate property. By comparing HfSiON with HfSiO, it is found that HfSiON shows even better properties after 950 °C annealing such as lower EOT value (0.95 nm), desirable amorphous phase and lower leakage current.

6.1 Fabrication of the hafnium silicate dielectrics

The hafnium silicate films were deposited by co-depositing of the Hf and Si targets in oxygen ambient. As described in Chapter 3, the relative concentrations of Hf and Si were tuned by varying the number of the laser pulses impinging on the certain target material. P-type silicon (100) wafers with resistivity of 1-10 $\Omega\cdot\text{cm}$ were used as the substrate. The substrate temperature was held at 300 °C during deposition while the oxygen pressure was kept at 0.3 Pa. The post deposition annealing was performed at 950 °C in N₂ for 30 seconds. A series of hafnium silicate samples with different Hf/Si

ratios have been fabricated. Table 6-1 lists the compositions of these hafnium silicates in atomic percentage derived from the AES analysis.

Table 6-1 Deposition conditions and the compositions of the hafnium silicate.

Sample	Pulse ratio (Hf: Si)	Thickness (nm)	Atomic Percentage (at. %)		
			Hf	Si	O
C1	0.3:1	12.5	6	27	67
C2	0.6:1	12.0	14	23	63
C3	0.8:1	12.8	17	15	68
C4	1.3:1	12.5	23	12	65
C5	1.5:1	13.0	28	3	69

It is found in Table 6-1 that with the increase of the pulse ratio between Hf and Si, the atomic percentage of Hf in the hafnium silicate film increases accordingly. And the oxygen percentage, which is almost unchanged in all these films, is close to the ideal stoichiometric oxygen percentage in HfSiO_4 films (66.7%). This suggests that oxygen is sufficient in all these samples. The thickness of these films has been measured from the depth profiling of AES. Figure 6-1 shows the AES depth profiling of sample C4 and the thickness of hafnium silicate is determined to be about 12.5 nm.

Figure 6-2 shows the C-V measurement of these hafnium silicates. It is found that the dielectric constant strongly depends on the hafnium concentration and film composition. It is clearly seen that with the increase of Hf composition from 6 at. % to 23 at. %, the capacitance in accumulation increases accordingly corresponding to the

increase of the effective dielectric constant. Sample C4 has the largest capacitance of about 92 pF and the derived effective dielectric constant is about 13. In contrast, the

Figure 6-1 AES Depth profiling of sample C4.

Figure 6-2 The gate capacitance as a function of Hf concentration in hafnium silicates.

further increase of the Hf content to 28% in sample C5 results in a reduction of the gate capacitance. This may be caused by the uncontrolled interface growth. At such a high level of Hf concentration, the hafnium silicate exhibits properties very similar to that of the pure hafnium oxide. Therefore, as previously discussed in Chapter 5, the oxygen diffusion problem in HfO_2 may also play an important role in the interface growth between this hafnium silicate and Si substrate. Oxygen can directly diffuse through this hafnium silicate layer and interact with Si to form a SiO_2 -like interface which finally results in a decrease of the total gate capacitance [154].

In this case, for the purpose of achieving the largest effective dielectric constant, a series of hafnium silicates with the same composition as in sample C4 ($\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$) has been fabricated and investigated in our following experiment.

Figure 6-3 shows the EOT value as a function of the physical thickness of $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$ films. As the hafnium silicate is scaled from 12.5 nm to 3 nm, the EOT is also scaled from 3.8 nm to 1.2 nm. The well-behaved linearity in EOT versus the physical thickness indicates that the effective dielectric constant of the gate stack is independent of the film thickness. However, as the film physical thickness is further reduced to 1.5 nm, the EOT doesn't decrease accordingly but increases to 1.6 nm, which is almost the same as the EOT of a 5-nm hafnium silicate. In order to investigate the mechanism of this abnormal phenomenon, cross section HRTEM

investigation has been performed on the 3-nm thick $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$ and 1.5-nm thick $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$ films respectively.

Figure 6-3 The EOT value of $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$ gate stack as a function of physical thickness.

Figure 6-4 (a) and 6-4 (b) illustrate the cross section TEM micrographs of the 3-nm thick $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$ before and after the RTA at 950 °C for 30 seconds. It can be seen that the silicate remains entirely unchanged after the thermal treatment. The film is still completely amorphous which shows no evidence of phase separation, and no obvious interface layer exists in both of the samples, demonstrating the stability of the hafnium silicate films in direct contact with Si. And under the current process conditions, the interface growth can be well controlled up to 950 °C thermal annealing while the film is still at the favorable amorphous state.

(a)

(b)

Figure 6-4 Cross section image of 3-nm thick $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$ film (a) before (b) after RTA at 950 °C in N_2 for 30 seconds.

(a)

(b)

Figure 6-5 Cross section image of 1.5-nm thick $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$ film (a) before (b) after RTA at 950 °C in N_2 for 30 seconds.

Figure 6-5 (a) shows the cross section of the as-received 1.5-nm thick hafnium silicate. Again, the $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$ -Si interface is seen to be atomically sharp. In contrast, as seen in Figure 6-5 (b), although hafnium silicate is still amorphous, the thickness of the interfacial oxide below the hafnium silicate film increases to 1.4 nm, indicating that oxygen can easily penetrate through this ultrathin silicate layer and react with Si. Therefore, the abnormal increase of the EOT value for 1.5-nm thick hafnium silicate in Figure 6-3 is mainly attributed to the growth of this interface layer. In this case, further reducing the hafnium silicate thickness to 1.5 nm provides no positive effect on the gate oxide scaling.

6.2 Characterizations of the hafnium silicate films

In this section, the 3-nm thick hafnium silicate film has been investigated. Figure 6-6 illustrates the EOT and leakage current characteristics of $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$ after annealing at different temperatures. It is observed that the EOT remains almost stable up to 950 °C thermal treatment. Compared to the sample annealed at 500 °C, the sample annealed at 950 °C shows only a 0.21-nm increase of EOT. And the leakage current density decreases slightly as the annealing temperature increases.

Figure 6-6 Effect of RTA temperature on EOT and leakage current density for the 3-nm thick $Hf_{0.23}Si_{0.12}O_{0.65}$.

Figure 6-7 Typical C-V and hysteresis curves of $Hf_{0.23}Si_{0.12}O_{0.65}$ measured at 25 °C and 275 °C.

Figure 6-7 shows the C-V and hysteresis measurement of $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$ at 1 MHz. Well-behaved C-V profile indicates the good electrical stability of Pt/Hf-silicate structures up to 950 °C. Compared to the large hysteresis in HfO_2 ($> 100 \text{ mV}@150 \text{ }^\circ\text{C}$) as shown in Figure 5-22, the hysteresis in the hafnium silicate is negligible ($< 50 \text{ mV}@275 \text{ }^\circ\text{C}$). Therefore, it suggests that there is minimal charge trapping inside the hafnium silicate and better interface quality can be achieved by using hafnium silicate.

6.3 Incorporation of nitrogen into hafnium silicate

6.3.1 Effect of nitrogen in gate dielectrics

Currently there is an intensive trend to incorporate nitrogen into high- k films such as HfO_2 , HfAlO and HfSiO [278-280]. The addition of nitrogen has led to significant improvements concerning crystallization, dopant diffusion and electrical performance [278-284].

Several mechanisms of nitrogen incorporation have been proposed: nitridation at the interface between high- k film and the Si substrate [282], at the gate electrode/high- k interface [283] and throughout the whole high- k films [284]. The main purpose of the nitridation of the silicon surface is to block the oxygen diffusion and thus reduce the interface reaction and consequently the EOT. Besides, better thermal stability and reliability have been achieved as well [282]. The nitrogen incorporation at the upper

interface can block the boron diffusion and thus improve the electrical properties and thermal stability of the high- k films [283].

Compared with the two nitridation mechanisms discussed above, the incorporation of nitrogen throughout the gate oxide seems to be one of the most efficient and favorable ways to improve the properties of gate dielectrics. Since the nitrogen is distributed throughout the whole film, both of the interfaces are nitrified as well, which will improve the electrical properties and thermal stability of gate dielectrics. In addition, the nitrified gate oxide shows an increase of the dielectric constant which directly contributes to the decrease of the EOT. Therefore, in order to improve the gate property more effectively, the nitrogen incorporation throughout the whole hafnium silicate films have been performed in our work and the fabricated HfSiON films have been systematically studied and characterized.

6.3.2 Fabrication procedures

The nitrified gate oxide has usually been prepared using furnace nitridation (using NO or N₂O gases) or postnitridation (in NH₃ ambient). These approaches not only require high processing temperatures (> 800 °C), but also provide very limited control over the nitrogen distribution and result in a nitrogen content peak at the channel-dielectric interface [285]. Therefore, in order to incorporate nitrogen at low temperature, plasma enhanced CVD, low temperature CVD have successfully been used [286, 287].

However, for the fabrication of HfSiON, if NH_3 and SiH_4 are used as the ambient gas, inherent incorporation of hydrogen into the films would enhance the boron diffusion and thus deteriorate the device performance [288]. In this case, we have fabricated the HfSiON films under atomic nitrogen/oxygen ambient. The atomic nitrogen/oxygen is generated by a DC ion source as described in Chapter 3. The substrate temperature was held at 300 °C. For the purpose of fabricating the HfSiON with a similar Hf concentration to that of sample C4 ($\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$), the pulse ratio between Hf and Si was also kept at 1.3:1. And the deposition pressure was 0.3 Pa with a N_2/O_2 ratio of 1:1. Before characterization, the films have been annealed at 950 °C in N_2 for 30 seconds and patterned with Pt top electrode and Al back contact.

Figure 6-8 shows the AES depth profiling of a 7-nm thick HfSiON. It is evident that nitrogen distributes throughout the whole hafnium silicate. And the carbon concentration is negligible. The film composition is determined to be $\text{Hf}_{0.21}\text{Si}_{0.12}\text{O}_{0.56}\text{N}_{0.11}$.

Figure 6-8 AES depth profiling of the 7-nm thick HfSiON.

Figure 6-9 C-V curves of 3-nm thick HfSiO and HfSiON.

6.3.3 Characterization of HfSiON gate dielectrics

In order to illustrate the effectiveness of the nitridation, a set of HfSiON samples with the same thickness of hafnium silicates listed in Figure 6-3 has been fabricated. Figure 6-9 depicts the C-V curve of a 3-nm HfSiON measured at 1 M Hz. As observed in the C-V curve, the HfSiON exhibits improved dielectric properties. Compared to the 3-nm thick $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$, the EOT value of HfSiON is further reduced from 1.2 nm to 0.95 nm. And the effective dielectric constant is calculated to be about 12.

Figure 6-10 shows the leakage current density curves of HfSiON and $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$ in terms of leakage current. Compared to $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$, HfSiON dielectric exhibits 1 - 2 orders of magnitude lower leakage current density, and after annealed at 950 °C, an EOT value of 0.95 nm with a leakage current density of $3.8 \times 10^{-3} \text{ A/cm}^2$ is obtained. The excellent electrical and dielectric properties after annealing suggest that HfSiON dielectric is a quite suitable candidate for gate dielectric application.

Figure 6-11 depicts the EOT values as a function of the thickness of HfSiON. It is noted that compared to $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$ with the same thickness, HfSiON shows a smaller EOT value with a larger dielectric constant. As the oxide thickness being further scaled to 1.5 nm, in contrast to the abnormal increase of EOT value to 1.6 nm observed in hafnium silicate, the EOT of HfSiON film is 0.95 nm, almost the same as that of 3-nm thick HfSiON.

Figure 6-10 Leakage current density comparison between the 3-nm thick HfSiO and HfSiON.

Figure 6-11 The EOT values of HfSiON gate stack as a function of the physical thickness.

In order to illustrate the origin of this phenomenon, cross section TEM study is further carried out. Figure 6-12 shows the cross section images of the 1.5-nm thick HfSiON

before and after 950 °C annealing. It is clearly observed in Figure 6-12 (a) that there is a 0.2-nm thickness interface exists between HfSiON/Si. And this interface layer is increased to about 0.8 nm after the annealing as shown in Figure 6-12 (b). This suggests that 1.5-nm thick HfSiON is not thick enough to block the oxygen diffusion to form a low- k interface. Furthermore, from the TEM image of the as-received 1-nm thick HfSiON shown in Figure 6-13, it is clearly found that even without any thermal treatment, a 2-nm thick interface has already been grown during the gate oxide deposition. Therefore, under the current process conditions, an EOT value of 0.95 nm is probably the scale limit for HfSiON gate stack.

(a)

(b)

Figure 6-12 Cross section images of 1.5-nm thick HfSiON film (a) before (b) after RTA at 950 °C in N₂ for 30 seconds.

Figure 6-13 Cross section image of the as-received 1-nm thick HfSiON film.

6.4 Conclusion

In summary, $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$ shows very good electrical and dielectric properties. After RTA at 950 °C in N_2 for 30 seconds, the 3-nm thick $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}$ film is still in amorphous state and no obvious interface exists in between $\text{Hf}_{0.23}\text{Si}_{0.12}\text{O}_{0.65}/\text{Si}$. The lowest EOT value obtained is about 1.2 nm with low leakage current density. Both the C-V and HRTEM results indicate that further reducing the hafnium silicate thickness does not provide any positive improvement on the scaling of EOT values, and a relatively thick interface has been observed for the 1.5-nm thick hafnium silicate after RTA. By incorporating nitrogen into the hafnium silicate film, it is found that the interface reaction can be better controlled as compared to hafnium silicate. High quality HfSiON film has thus been obtained with an EOT value of about 0.95 nm as well as low leakage current density, 3 to 4 orders of magnitude lower than that of SiO_2 with the same thickness. Therefore, HfSiON is a promising candidate for gate dielectric application.

CHAPTER SEVEN

CONCLUSION AND RECOMMENDATIONS

7.1 Conclusion

This thesis has aimed at the fabrication and characterization of HfO_2 -based high- k gate dielectrics for CMOS gate and nanoelectronics applications. HfO_2 , HfSiO and HfSiON have been systematically studied. And encouraging results have been obtained. Major accomplishments of the thesis are listed below:

The Laser-MBE system has been successfully installed. And for calibration purpose, more than 100 layers of SrTiO_3 have been successfully deposited on the SrTiO_3 substrate in a layer-by-layer mode, suggesting that Laser-MBE is capable of precisely controlling the epitaxial growth of oxide thin films.

RHEED system has been employed to investigate the silicon surface prior to the gate oxide deposition. The silicon surface condition, such as the roughness and the

existence of native oxide, has been well determined from the RHEED diffraction pattern. A smooth silicon surface which is free of native oxide can thus be prepared and ready for gate oxide deposition.

It has been found that oxygen partial pressure plays an important role in gate oxide deposition. For the hafnium oxide deposition, by lowering the oxygen partial pressure to an optimized level, the growth of the low- k interfacial layer can be effectively suppressed. A two-step deposition method has been adopted to further inhibit the growth of interfacial layer. By using this two-step deposition method, high quality ultrathin HfO_2 films have been deposited on Si with desired and improved dielectric properties.

The current conduction in the HfO_2 gate dielectric has been systematically investigated, and it is found that at low electric field of $E < 1 \text{ MV/cm}$, the Schottky model is the main conduction mechanism; in the medium field range of $1 \text{ MV/cm} < E < 4 \text{ MV/cm}$, the PF conduction mechanism is dominant; with further increasing electrical field into the high field region of $4 \text{ MV/cm} < E < 6 \text{ MV/cm}$, the current behavior turns to the FN tunneling.

RuO_2 has been deposited by RF Sputtering and investigated as an alternative gate electrode for pMOS devices. The $\text{RuO}_2/\text{HfO}_2/\text{n-Si}$ capacitors show excellent gate

properties such as negligible flat band voltage shift (< 10 mV), very strong breakdown strength (> 10 MVcm⁻¹). Compared to the SiO₂ dielectric with the same EOT value, RuO₂/HfO₂/n-Si capacitors exhibit at least 4 orders of leakage current density reduction. The work function value of the RuO₂ top electrode is calculated to be about 5.0 eV by two methods, and the effective fixed oxide charge density is determined to be 3.3×10^{12} cm⁻². All the results above indicate that RuO₂ is a promising alternative gate electrode for Laser-MBE grown HfO₂ gate dielectrics.

In order to further inhibit the growth of the low- k interface layer and increase the crystalline temperature of the HfO₂-based dielectrics, silicon has been incorporated into hafnium oxide. By incorporation of an optimized concentration of Si into HfO₂, the hafnium silicate shows improved electrical and dielectric properties compared with hafnium oxide of the same thickness. HRTEM results show that even after RTA at 950 °C in N₂ for 30 seconds, the 3-nm thick Hf_{0.23}Si_{0.12}O_{0.65} film is still in amorphous state and no obvious interface exist in between Hf_{0.23}Si_{0.12}O_{0.65}/Si.

It has been found that by incorporating nitrogen into the hafnium silicate film, the electrical and dielectric properties of this HfSiON gate stack are further improved. And the resulting film is still in the favorable amorphous state after RTA at 950 °C in N₂ for 30 seconds. State-of-the-art HfSiON film has been obtained with an EOT value

of about 0.95 nm as well as low leakage current density. Therefore, HfSiON is a promising candidate for gate dielectric application.

Both the HRTEM results and C-V measurement indicate that further scaling the HfSiON thickness below 1.5 nm does not contribute to the reduction of EOT. A relatively thick interface exists between the gate oxide and substrate. Therefore, under the current deposition scheme, 0.95 nm (EOT) is the scaling limit for Laser-MBE-deposited HfSiON gate dielectrics.

7.2 Recommendations for future work

It is evident in this thesis that the studies on Laser-MBE deposited HfO₂-based thin films exhibit a good prospect for potential high-*k* microelectronic device applications. However, for the implementation of HfO₂-based gate dielectrics in the semiconductor industry in 65 nm technology, there is still much work to be done which is listed as follows:

7.2.1 Charge trapping in HfO₂-based thin films

Unlike SiO₂, HfO₂-based gate oxides, such as HfO₂, exhibit significant charge trapping which cause the threshold voltage instability, frequency dependent mobility values, C-V hysteresis, etc. Therefore, how to reduce the charge trapping density in HfO₂-based gate dielectrics is a challenging issue and need to be considered.

7.2.2 MOSFET characterization with HfO₂-based gate dielectrics

Although our studies on HfO₂-based gate dielectrics show that these materials can be promising candidates for gate oxide, there is still a long way to the application of HfO₂-based gate dielectrics in the area of silicon-based devices. The most direct method to further narrow this gap is to study the work performance of MOSFET fabricated with HfO₂-based gate oxide.

AUTHOR'S PUBLICATIONS

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