Characterization and modeling of on-wafer interconnects for RFICs

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Characterization and Modeling of On-Wafer Interconnects for RFICs

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University

in fulfillment of the requirement for the degree of

Doctor of Philosophy

2007

Statement of Originality

I hereby certify that the work presented in this thesis is the result of original research and has not been submitted for a degree to any other university or institution.

Shi Xiaomeng

Date

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Summary

Driven by the recent explosive growth in the wireless telecommunication, the field of radio frequency integrated circuits (RFICs) design is gaining more and more attention. Because of its mature technology, low fabrication cost as well as high packing density, complementary metal oxide silicon (CMOS) has been recognized as the most suitable process to meet the demands from this rapidly growing wireless communication market.

As the operating frequency reaches RF spectrum, the interconnect has become one of the most crucial factors affecting the performance of RFICs. Thereafter, incorporating the interconnect effects into the RFIC design flow becomes increasingly essential.

This thesis addresses the characterization and modeling of on-wafer interconnects for CMOS RFICs. A scalable equivalent circuit model for complex-shaped interconnects is proposed. In this proposed structure, frequency-variant characteristics are modeled by frequency independent components. Therefore, the proposed model is compatible with commercial electronic design automation (EDA) tools. The accuracy of the model is verified with on-wafer measurements. Moreover, the proposed model is employed in the post-layout simulation of a real circuit. The simulated and measured figures of merit (FoM) of the circuit are compared and analyzed. The proposed model demonstrates higher accuracy than the foundry provided model. Also addressed in this thesis is the sensitivities of interconnects to CMOS process

parameters.

Chapter 1

Introduction

In recent years, wireless devices, such as pagers, cellular and cordless phones, global positioning system (GPS) devices and personal communication system (PCS) devices, have penetrated into all aspects of our daily lives. Several mobile/wireless communication standards have been widely used, covering the frequency range from 0.9 GHz to 5.9 GHz. To list a few, they include the global system for mobile communications (GSM), code division multiple access (CDMA), Bluetooth, IEEE802.11 [1, 2]. As seen from the market point of view, the cost and ease of system implementation must take priority [3, 4]. Thereby, there is an increased interest in the development of radio-frequency system-on-chips (RF-SoC) that integrate RF, analog and digital circuits [3, 5]. Besides circuit design, the choice of the implementation technology is also very important and complicated. Compared to other available technologies, such as bipolar complementary metal oxide semiconductor (BiCMOS), GaAs metal semiconductor field effect transistor (MESFET),

heterojunction bipolar transistor (HBT), CMOS technology is deemed as the most attractive and promising one in the long run [3, 5–8].

Due to the increased circuit complexity and higher operating frequencies of the CMOS RF-SoC, the circuit performance becomes more and more subjected to interconnect behaviors [9–17]. Inappropriate decision of interconnects in the design stage may lead to either over-design or excessive design iterations after tapeout. Therefore, there is an increasing need of adequate electronic design automation (EDA) tools for interconnect modeling from the industry [5, 14, 16, 17].

On-chip interconnects can be categorized into two groups: local interconnects and global interconnects [18, 19]. Local interconnects are connections between circuit elements, namely, transistors, inductors, capacitors, etc. These local wires tend to be less than 1000 μm in scale in the current technologies ($\sim 0.18\mu\text{m}$). Global interconnects serve to connect separate functional units and the length are much longer [19, 20]. In this work, we focus on the modeling and characterization of local interconnects.

1.1 Model Development

1.1.1 Simulators and Models

Due to increased circuit complexity and higher operating frequencies, simulation has become indispensable in the design of ICs. SPICE (simulation program with

integrated circuit emphasis), developed by the University of California, Berkeley has become the industry standard simulation tool. With accurate device models and precise model parameters, useful simulation results can be achieved to aid the IC design and significantly shorten the product-to-market time [21].

Besides SPICE-like circuit simulators, there are also electromagnetic (EM) simulators based on numerical solutions of Maxwell's equations that describe the EM behaviors of physical structures. EM simulators are able to precisely analyze the high frequency effects of the devices. However, they take up extremely high computing power and are time consuming. Moreover, in-depth EM knowledge is required for using those EM simulators [22]. Therefore, circuit models represented in capacitance, resistance and inductance, for instance, which are much easier to handle, are preferred by circuit designers [21, 23]. Thus, in this work we focus on characterizing interconnects with an equivalent circuit model. This is compatible with SPICE-like circuit simulators.

1.1.2 Stages of Model Development

In order to develop a desired equivalent circuit model for on-wafer interconnects, there are mainly four stages to follow, namely: test structure measurement, model construction, parameter extraction and model verification.

In the first stage, a library of typical interconnect structures are established. The characteristic parameters of the interconnect structures are used as a database for

the model parameter extraction as well as the model verification.

In the second stage, the model structure is established. The constructed interconnect model should be capable of characterizing the high frequency effects as well as incorporable with conventional EDA tools. The main challenge in this stage is that the interconnect behavior becomes frequency-variant at high frequencies [24–27]. Although behavioral models, which can characterize the frequency-dependent characteristics, can be used in SPICE-like simulators, it is much slower than those only involve frequency-independent components. Therefore, characterizing the frequency dependent characteristics with frequency independent components would be more desirable.

Parameter extraction comes after model construction. Essentially, the problem in parameter extraction is multi-parameter and multi-target optimization. The performance of the extracted data, their accuracy, convergency and efficiency, strongly depends on the chosen algorithm. Therefore, the algorithm should be selected, developed and applied appropriately.

Finally, the proposed model is verified with on-wafer measurements to ensure accuracy.

1.2 On-wafer RF CMOS Interconnect Analysis

In recent CMOS technology, designs can exploit up to six metal layers [17, 28]. Fig. 1.1 illustrates a six-layer interconnect stack. Hence, the on-wafer interconnection of

Figure 1.1: Approximation of six metal layers interconnect stack

the whole chip could be very complicated. Additionally, the low-resistivity nature of the substrate used in the conventional CMOS technology causes significant high frequency substrate losses. More specifically, the conducting nature of the Si substrate leads to various forms of losses, namely conversion of electromagnetic energy into heat in the volume of the substrate. Causes of the losses can be described in two separate loss mechanisms, i. e., losses induced by eddy current and displacement current. At high frequencies, the substrate losses will always exist. Same as other devices, interconnects also suffer from the substrate losses [5,12,13,26]. Moreover, as the operating frequency of RFICs reaches multi-Gigahertz, the inductive effect [27,29,30], skin effect [31–33] and distributed effect [34–36] become significant [37,38]. All these effects are dependent on the frequency. Consequently, the characteristics of RF interconnects are frequency-variant as well. All these issues

bring great challenges to the modeling and characterization of RF CMOS interconnects.

1.3 Motivations

Precise RF device models are prerequisites for reliable circuit design. For years, device studies for RFICs have been mainly focused on active devices such as MOSFETs and passive devices such as capacitors and inductors. Interconnect design has always been neglected or overlooked [39]. However, unlike in the low frequency ranges, as the operating frequency reaches RF spectrum, many high frequency effects of the interconnects, such as the skin effect, inductive effect, distributed effect, substrate effect, are no longer negligible [40]. Hence, the interconnect has become one of the most crucial factors affecting the performance of the RFICs [12, 13, 41]. Thereafter, incorporating the interconnect into the RFIC design flow becomes increasingly essential.

Since nowadays EDA tools such as SPICE and Spectre have become indispensable in the IC design process, accurate and efficient interconnect models that could be readily implemented into the commercial simulation environment are desirable [42]. Thus, the purpose of this thesis is to investigate the characteristics of on-wafer interconnects in RF ranges and to propose interconnect models that are compatible with EDA tools to aid RFIC design.

1.4 Objectives

As mentioned above, at radio frequencies, the frequency-dependent nature of the interconnects must be considered. Ideally, the frequency-dependent components should be used in the models. However, behavioral models which can characterize the frequency-dependent elements are much slower than models only involve frequency-independent components. The main objective of this project is to propose frequency-independent equivalent circuit models to characterize these frequency-variant effects.

Most of the models reported in [15, 24, 25, 43, 44] are for straight-line interconnects. However, the shapes of interconnects on a real chip are much more complicated. Interconnect models, which handle straight lines only, are far from sufficient. In this work, interconnects with various lengths, widths and shapes will be considered. Scalable interconnect models will be proposed.

Additionally, aiming to develop silicon-verified interconnect models, the values of the model components are obtained from on-wafer measurements. In order to extract the component values accurately and efficiently, optimization algorithms will be studied and applied.

Furthermore, the evolving pace of the CMOS technology is very fast. Hence, the variations of process parameters on interconnect behaviors have rarely been reported in the literature. The investigation of the sensitivities of interconnects to process parameters will also be addressed.

1.5 Organization of the Thesis

This chapter has given an overview of the project by presenting the essential background of interconnect modeling. Motivations and objectives of this project are also described. The remainder of this thesis is organized as follows.

In Chapter 2, the physical background of on-wafer interconnects is presented. An overview of existing interconnect models as well as the optimization algorithms for model parameter extraction are also introduced. After that, the design and measurement of interconnect test structures are discussed in Chapter 3. Chapter 4 gives details of the proposed scalable interconnect model. Chapter 5 describes the application of two different optimization algorithms for the model parameter extraction. In Chapter 6, extracted parameters are presented as functions of design parameters, i.e., the length and width of the interconnect. The validity of the proposed model is demonstrated by comparison with on-wafer measurements. Chapter 7 shows the implementation of the proposed interconnect model in a practical RF circuit. A transimpedance amplifier is designed to help access the importance of interconnect effects and the accuracy of the proposed model. Chapter 8 focuses on the sensitivity investigation of on-wafer interconnects to CMOS process parameters. Finally, Chapter 9 concludes the thesis and outlines some aspects of future work.

Chapter 2

Background and Previous Work

2.1 Physical Background

In current CMOS processes, on-chip interconnects are generally made of metallic conductors, although doped semiconductors can be employed as well. The focus of the author's work is on the metallic interconnect.

When an electric field, E , is applied, free electrons of the conductor begin to accelerate in the opposite direction to the applied E . Thus the average electron movement is in one direction. The movement of the charges and the established electric and the magnetic fields are the basis for information transfer in interconnects.

In order to propose accurate interconnect models which are accurate in the RF ranges, several physical phenomena must be taken into consideration.

2.1.1 Inductive Effect

The movement of the charges results in a magnetic field and hence the storage of the magnetic energy. The ability of a conductor to store the magnetic energy is described by its inductance.

At low frequencies, the impact of the magnetic field is often neglected, and the interconnects are usually characterized by the conventional RC models [24,45]. However, when the frequency increases beyond multi-Gigahertz, the inductive reactance of the interconnect becomes comparable to or dominant over the resistance. Therefore, the inductance and magnetic field must be considered [38] in the Gigahertz frequency range. Hence, it becomes a major concern of current interconnect modeling [39].

2.1.2 Skin Effect

At low frequencies, current flow is uniformly distributed over its cross section. The resistance of an interconnect with length l (m), width W (m) and thickness t (m) is given by [46]:

$$R = \rho \frac{l}{tW} = R_s \frac{l}{W} \quad (\Omega) \quad (2.1.1)$$

where ρ ($\Omega \cdot m$) is the resistivity of the interconnect material and R_s (Ω) is the sheet resistance based on DC measurements.

However, at high frequencies, say above 5 GHz, the EM fields attenuate substantially

when they pass through the conductor. The current crowds to the surface of the conductor, as shown in Fig. 2.1. This is known as skin effect [47].

Figure 2.1: Illustration of skin effect [18]

The mechanism of skin effect [18,46] can be explained either from an electrical circuit or an electromagnetic perspective. From the circuit perspective, in the conductor, the currents always flow in a way, which has the least impedance, i.e., $R + j\omega L$. For direct current, the imaginary part of the impedance is zero; the currents are distributed uniformly. This way of distribution has the least resistance or impedance. As the frequency increases, the imaginary part becomes more and more significant. While the current crowds to the surface of the conductor, the average distance between the currents is more than that of the currents which are distributed uniformly. Consequently, the magnetic coupling and the inductance are minimal, so is the impedance.

From electromagnetic perspective, the electromagnetic waves are attenuated when they pass through the conductor. At a sufficient depth, all electric and magnetic

fields are negligible and there is no current flow. The high-frequency voltage between the two terminals of the conductor creates a high-frequency electric field and a high-frequency current in the conductor leading a magnetic field to be created. This is equivalent to the situation where electromagnetic waves penetrate the conductor. Those fields are attenuated as they passing into the conductor. The currents inside the conductor weaken as well with the attenuation of the electric field.

At a sufficient depth, all the fields are negligible and there is no current. Hence, the effective cross section of the conductor shrinks with the increase of the frequency. Skin depth δ is defined in Eq. (2.1.2) in [46]. It refers to the depth from the surface of a conductor, where the currents are confined to flow.

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} = \frac{1}{\sqrt{f\pi\mu\sigma}} \quad (m) \quad (2.1.2)$$

where μ (H/m) and σ (S/m) stand for the permeability and the conductivity of the conductor respectively. ω (rad/s) represents the angular frequency, which is the product of 2π and the operating frequency f (Hz).

We now need to modify the conventional calculation of the resistance shown in Eq. (2.1.1) by replacing the geometrical cross-sectional area with the effective one. When $\delta \ll W, t$, the resistance formula could be approximated as Eq. (2.1.3) [46].

$$R = \frac{\rho l}{Wt - (W - 2\delta)(t - 2\delta)} \quad (\Omega) \quad (2.1.3)$$

As the skin depth decreases with the increasing frequency, the resistance of the conductor becomes frequency-variant as well. It increases along with the frequency. On the contrary, the inductance reduces. The reason is that at low frequencies, the magnetic energy is stored inside as well as outside the conductors. However, as frequency increases, the current flow is mostly concentrated near the surface of the conductor. Hence, the magnetic field becomes confined to the region outside the conductor.

2.1.3 Substrate Effect

In current CMOS technologies, low-resistivity substrate is used to improve yields and suppress the latchup [48]. However, in RF ranges, the low-resistivity substrate causes significant high frequency losses. The silicon substrate therefore appears to be a major concern of the use of CMOS in multi-Gigahertz applications. Therein, its mechanism must be studied thoroughly and its effect must be considered in the process of interconnect modeling.

The substrate affects interconnects in two ways: eddy current losses and substrate losses that are induced by the displacement currents injecting into the substrate [49]. Fig. 2.2 illustrates the eddy currents in the substrate which are induced by the current flowing through the conductor. The eddy-current [5,50], in turn, will change the magnetic field and the inductance of the conductor. Particularly, if a high conductivity substrate is used at high frequencies, the eddy currents are strong and crowded near the surface of the substrate [23]. The inductance is reduced and there

Figure 2.2: Eddy currents in the substrate [23]

are significant eddy current losses.

The impact of the eddy current is frequency dependent. For direct current, no eddy current is induced. The inductance is equivalent to that in the free space. As the frequency increases, the eddy current becomes stronger and more crowded to the surface.

The substrate losses are derived from the substrate injection of the displacement currents. Fig. 2.3 illustrates the procedure. The displacement currents flowing through the capacitance terminating on the substrate result in additional resistive losses. The capacitance to the substrate is also frequency-dependent. It is larger at higher frequencies because of skin effect of both the conductor and the substrate, as well as the frequency dependence of the effective permittivity [18].

Figure 2.3: Displacement current injected into the substrate [23]

2.1.4 Corner Effect

In most cases, straight-line interconnects are not adequate for on-wafer interconnections. Interconnects with bends are required. These bends usually pass through angles of 90° or 45° . As mentioned in Section 2.1.2, the currents tend to flow in a path with the least impedance. Hence, in consequence of the appearance of the bends, the current distribution is different from that in straight-line interconnects. Fig. 2.4 illustrates the current distribution at the area in the corner. This difference is known as the corner effect [18].

2.1.5 Distributed Effect

When the length of the interconnect is less than $\frac{1}{20}$ of the wavelength λ , the signal can be deemed as reasonably constant along the entire length. Hence it can be

Figure 2.4: Magnitude of the current densities at 10 GHz
(a) right-angled bend; (b) 45° bend [18]

characterized with lumped components. However, when the length of the conductor is longer than $\frac{1}{10}$ of λ , the capacitance and inductance are distributed throughout the interconnect. They cannot be confined to a lumped element. This effect is called distributed effects [18].

2.2 Introduction to S-parameters

The first step of model development is the acquisition of a characteristic parameter database of various interconnect structures.

At very high frequencies, measuring the voltages and currents is difficult in practice, since direct measurements usually involve the magnitude and phase of wave traveling in a given direction, or of a standing wave. Thus equivalent voltages, currents, related impedance and admittance matrices become somewhat of an abstraction.

Figure 2.5: Definition of S-parameters of a two-port network [51]

While the impedance (or admittance) matrices relate to the total voltages and currents at the ports of the system, the scattering parameters (S-parameters) [51] relate to the voltage waves incident on the port to those reflected from the ports. It is known that only S-parameters are measurable in the RF range [39, 51]. The definition of S-parameters of a two-port network is illustrated in Fig. 2.5. a_1 and a_2 represent the amplitudes of the incident waves, while b_1 and b_2 represent the amplitudes of the reflected waves.

The S-parameters [51] are defined as follows:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = [S] \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (2.2.4)$$

where a_1 , a_2 , b_1 and b_2 carry the same meaning as defined in the previous paragraph, while

$$[S] = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \quad (2.2.5)$$

2.3 Existing Interconnect Models

In most available EDA tools, the interconnects are insufficiently modeled as resistance and capacitance (RC) components [52, 53]. As stated in Section 2.1.1, at high frequencies, the inductive effect of the interconnect must be taken into consideration. Hence, resistance, inductance, and capacitance (RLC) models have been exploited. Unfortunately, drawbacks still exist in those RLC models. The frequency-variant characteristics, which cannot be neglected at high frequencies, are not included in these RLC models [39]. As an improvement, some models employ frequency-variant components to characterize the frequency-variant behaviors [24, 54, 55]. However, although behavioral models, which can characterize the frequency-dependent characteristics, can be used in SPICE-like simulators, it is much slower than those only involve frequency-independent components. Therefore, there is an urgent demand of precise, simple and scalable interconnect models that can be implemented by conventional EDA tools, so that the circuit design and analysis can be much more accurate and easier.

Many interconnect modeling methods have been introduced in literature. These approaches are mainly classified into two categories: One is the transmission line

model, another is the lumped equivalent circuit model.

2.3.1 Transmission Line Model

As the operating frequency reaches multi-Gigahertz, the distributed effect must be considered. Therefore, transmission line models are mostly studied and employed in [55, 56]. The transmission line characteristics of an interconnect line can be mathematically formulated with the Telegrapher's equations [51] as listed below,

$$\begin{aligned}\frac{dV(x,t)}{dx} &= -(R + j\omega L)I(x,t) \\ \frac{dI(x,t)}{dx} &= -(G + j\omega C)V(x,t)\end{aligned}\tag{2.3.6}$$

where the voltage V and the current I along the line both are functions of position x and time t . R is per-unit-length (PUL) resistance, L is PUL inductance, G is PUL conductance and C is PUL capacitance. The RLGC model of the classical transmission line is shown in Fig. 2.6.

The standard solution to the Telegrapher's equations is

$$\begin{cases} V = V^+e^{-\gamma x} + V^-e^{+\gamma x} \\ I = \frac{1}{Z}(V^+e^{-\gamma x} + V^-e^{+\gamma x}) \end{cases}\tag{2.3.7}$$

where

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}\tag{2.3.8}$$

Figure 2.6: Classical transmission line RLGC model [51]

In order to solve the above equations, the propagation constant γ and characteristic impedance Z of the interconnect must be known. The line parameters (γ , Z , R , L , G and C) can be extracted from S-parameter measurements.

$$e^{-\gamma x} = \left\{ \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right\}^{-1} \quad (2.3.9)$$

where

$$K = \left\{ \frac{(1 + S_{11}^2 - S_{21}^2)^2 - (2S_{11})^2}{(2S_{21})^2} \right\}^{1/2} \quad (2.3.10)$$

$$Z^2 = Z_0^2 \frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2} = \frac{(R + j\omega L)}{(G + j\omega C)} \quad (2.3.11)$$

where Z_0 denotes the reference impedance of the S-parameter measurement system.

50 Ω is usually used for convenience and standardization for on-wafer interconnect

modeling [45]. Detailed derivations of Eq. (2.3.9) to Eq. (2.3.11) are given in [57]. During the extraction of γ and Z from $e^{-\gamma x}$ and Z^2 , extracted parameters with values that are not physically real, such as negative attenuation constants are ignored [57]. The line parameters R , L , G and C are extracted from S-parameter measurements as follows:

$$R = \operatorname{Re}\{\gamma Z\} \quad (2.3.12)$$

$$L = \frac{\operatorname{Im}\{\gamma Z\}}{\omega} \quad (2.3.13)$$

$$G = \operatorname{Re}\left\{\frac{\gamma}{Z}\right\} \quad (2.3.14)$$

$$C = \frac{\operatorname{Im}\left\{\frac{\gamma}{Z}\right\}}{\omega} \quad (2.3.15)$$

Since the characteristics of the interconnects are frequency-variant, the extracted parameters are also frequency-dependent [58, 59], although their simulations are not supported by commercial circuit simulators. To fully describe the behavior of high frequency interconnects with frequency independent components, the classical transmission line model is optimized. As shown in Fig. 2.7 to Fig. 2.10, several improved interconnect models can be found in [24, 45, 60, 61].

The RLGC parameters of the transmission line model characterize the per-unit-length property. Therefore, simulation complexity is proportional to the physical dimension of the interconnects. In addition, this method should also be utilized with simplified neighborhood assumptions, such as uniformity [62].

Figure 2.7: Improved transmission line model 1 [60]

Figure 2.8: Improved transmission line model 2 [24]

Figure 2.9: Improved transmission line model 3 [45]

Figure 2.10: Improved transmission line model 4 [61]

Figure 2.11: Lumped equivalent circuit model proposed by You and Kuester. (The number of the parallel R-L sections corresponds to the number of stable poles.) [63, 64]

Figure 2.12: One- Π lumped equivalent circuit model for inductors [66–69]

2.3.2 Lumped Element Model

In [63,64], You and Kuester presented a SPICE-compatible lumped element model for interconnects (Fig. 2.11). The model is extracted from the solutions of the finite-element method (FEM) [65] matrix equations. The FEM is a method that divides complex or irregularly shaped structures into a large number of discrete elements, which is easy to analyze.

As shown in Fig. 2.12, this one- Π model is conventionally used for on-wafer inductors [66–69], which are inherently spiral interconnects. The distributed effect cannot be applied in the one- Π model, since it will become insufficient when the interconnect is long.

2.4 Methodologies of Parameter Extraction

Essentially, the problem of the parameter extraction is a multi-parameter and multi-target optimization. The performance of the extraction, i.e., the accuracy, convergence and efficiency, strongly depends on the chosen algorithm.

2.4.1 Literature Review

Several parameter extraction methods have been reported. There are systematic method, which can be applied for general structures [70, 71], and optimization method, which fits the parameter values of predefined networks [70].

In this project, the model topology is determined before the parameter extraction. Therefore, optimization method is employed. Many optimization algorithms [72] such as genetic algorithms (GA) [73], genetic programming (GP) [74], evolutionary strategies (ES) [75], particle swarm optimization (PSO) [76] have been reported in literature. In the following subsections, two algorithms applied in this project are introduced.

2.4.2 Genetic Algorithm

Genetic algorithm (GA) [73, 77] was invented by John Holland and his colleagues in 1975. It is designed to simulate the genetic recombination and mutation to promote the evolution of a population to best satisfy a predefined goal. A candidate

solution to a specific problem is represented as an individual or a chromosome. Each chromosome consists of a set of genes and obtains its fitness value after being evaluated according to the objective function. The chromosome with the smallest or largest fitness value is called the fittest chromosome. Based on the fitness value and a series of GA operators, a new generation is generated. There are three basic operators in GA, namely reproduction, crossover and mutation. Reproduction is a process whereby the fittest chromosomes in the parent generation have the highest chance to reproduce offsprings in the new generation. Crossover is a genetic operator used to vary the programming of a chromosome or chromosomes from one generation to the next. Mutation is a random alteration of some gene values in a chromosome.

2.4.3 Particle Swarm Optimization

PSO is a high performance optimizer developed by Kennedy and Eberhart [78] in 1995. It is one of the evolutionary computation (EC) techniques. PSO originates from the behaviors of animal groups such as a flock of birds or a school of fishes. It simulates the simplified movement of a society composed by individuals to solve optimization problems. In PSO, each solution is represented as a particle in the search space. Initially, the population of particles is randomly generated. All particles have fitness values derived from an objective function. They move through the problem space and adjust their search directions according to various velocities. Fig. 2.13 shows the concept of searching point modification [79]. Each particle keeps track of the best solution obtained by itself (*pbest*) as well as the best record

Figure 2.13: Modification of searching point [78]

among all the particles ($gbest$). The consciousness of the whole particle society is the most distinguished point of PSO. The manipulation of the particles is based on Eq. (2.4.16) and Eq. (2.4.17):

$$S_{i,t+1} = S_{i,t} + V_{i,t+1} \quad (2.4.16)$$

$$\begin{aligned}
 V_{i,t+1} = & w_i V_{i,t} + c_1 rand \times (pbest_i - S(i, t)) \\
 & + c_2 rand \times (gbest_i - S(i, t))
 \end{aligned} \quad (2.4.17)$$

where $S_{i,t}$ and $V_{i,t}$ are the current position and velocity vector of particle i at generation t . $pbest_i$ is the position vector of the best experienced particle i , while $gbest_i$ is the best particle in the swarm. w_i is the weight function for the velocity of particle i . c_i is the weight coefficient for each term. $rand$ is a random number between 0

and 1.

Unlike GA, in which the individuals are not conscious of others, the most distinguished point of PSO is that the members of the group share information among themselves. Therefore, the efficiency is increased. It is computationally inexpensive in terms of memory and time. Moreover, PSO requires only very primitive mathematical operations. It can be implemented within a few lines of computer codes [76].

Chapter 3

On-wafer Measurements of Test Structures

In RFICs, the routing density is not as high as in digital circuits. Therefore, not all the metal layers are needed for routing [80]. Since the top metal layer has lower sheet resistance and suffers less from the substrate losses, it is commonly allocated for routing critical high frequency paths. Therefore, in this project the test structures are designed and fabricated on the top metal layer employing a Chartered Semiconductor Manufacture Ltd. (CHRT)'s 0.18 μm RF CMOS technology. The IC technology cross-sectional view of the test structure is shown in Fig. 3.1.

Figure 3.1: A cross-sectional view of on-wafer interconnect using CMOS technology [81]

3.1 Test Structures for Straight-line Interconnects

The physical dimensions of the test structures are carefully selected. The lengths of the test structures vary from $100\ \mu\text{m}$ to $800\ \mu\text{m}$, while the widths are in the range between $1.5\ \mu\text{m}$ and $20\ \mu\text{m}$. The criteria for selecting the minimum width are derived from foundry design rules, which state that the minimum top-metal width is $1.5\ \mu\text{m}$. The reason for selecting $20\ \mu\text{m}$ as the maximum width is that the inductor, which is the largest passive device in a circuit, usually has a width of less than $20\ \mu\text{m}$.

Figure 3.2: Top view of a fabricated interconnect test structure

μm in a typical RF circuit design. The selection of the minimum length for the test structure is based on the concern of the minimum distance that the probes can be placed together. Therefore, the measurement precision is ensured. For typical RF circuit sub-blocks, such as the low noise amplifier (LNA), voltage controlled oscillators (VCO) and mixer, the total die size is around $800\ \mu\text{m}$ by $800\ \mu\text{m}$. That is the reason why $800\ \mu\text{m}$ is selected as the maximum length in our test structures.

Due to the space limitation of the figure, only six sets of the fabricated test structures are shown in Fig. 3.2. The lengths of the shown sets are all $400\ \mu\text{m}$, while the widths are $1.5\ \mu\text{m}$, $3\ \mu\text{m}$, $5\ \mu\text{m}$, $10\ \mu\text{m}$ and $20\ \mu\text{m}$ respectively from the bottom of the figure. As it is known, three pairs of pads, i.e., ground-signal-ground (GSG) are required for the measurement of each interconnect. From Fig. 3.2 it is also observed that the ground pads are shared between two adjacent test sets. This so-called pad

sharing technique [41] is employed here in order to reduce the total size of the die.

3.2 Test Structures for Interconnects with Bends

The straight-line interconnect itself does not satisfy the operational efficiency. In most cases, interconnects with bends are also required. According to design rules, 90° and 45° bends are most commonly used.

In order to characterize the bending interconnects, corresponding test structures are designed. The top views of two fabricated test structures are shown in Fig. 3.3. The total length of each test structure is fixed at $300\ \mu\text{m}$; the widths vary from $3\ \mu\text{m}$, $5\ \mu\text{m}$, $10\ \mu\text{m}$ and $20\ \mu\text{m}$, while the angles of the bends are 45° and 90° respectively.

3.3 De-embedding, Calibration and Measurement

It can be observed that in both Fig. 3.2 and Fig. 3.3, there are open structures designed for de-embedding [39, 57]. The open structures are basically the same layout as the interconnect test structures, except without the center conductors.

The test structure can be viewed as a combination of both the open structure and the interconnect (Fig. 3.4), in which Y_{p1} , Y_{p2} and Y_{p3} represent the influence of the parallel parasitic contributed by the open structure, the unwanted contributions of the pads can be removed using the Y-parameter-based technique described in Eq. (3.3.1) [82].

Figure 3.3: Fabricated interconnect test structures: interconnects with bends
 (a) interconnects with 45° bends; (b) interconnects with 90° bends.

$$Y_{interconnect} = Y_{test-structure} - Y_{open} \quad (3.3.1)$$

After fabrication, a Cascade Microtech Probe Station and a HP 8510C Vector Network Analyzer are employed for on-wafer measurement. The connection of the measurement equipment is illustrated in Fig. 3.5.

In order to null the parasitics of the test setup, calibrations are performed before test structure measurement. As illustrated in Fig. 3.6, a short-open-load-through (SOLT) calibration technique [83] is used. S-parameter measurements are performed on the test structures from 50 MHz to 25 GHz. After that, de-embedding is carried

Figure 3.4: Equivalent network block of interconnect test structure
 (a) entire test structure; (b) open structure. [82]

out. The probing pads and other parasitic contributions are removed.

Figure 3.5: Illustration of the connection of the measurement equipment

Figure 3.6: The SOLT calibration technique [83]

Chapter 4

Model Construction

4.1 Straight-line Interconnects

The function of interconnects is to connect different devices or blocks together. In the low frequency ranges, interconnects can be characterized by frequency-independent resistors (R) and capacitors (C). However, this RC model is not applicable at high frequencies. The reason is that as the frequency increases, the inductive effect, skin effect, substrate effect and distributed effect of the interconnects begin to have significant influences on its function [37, 38]. All these effects are dependent on the frequency, which shows that the characteristics of RF interconnects are frequency-variant.

Ideally, frequency-variant models should be used in the simulation. However, behavioral models which can characterize the frequency-dependent elements are much

slower than models only involve frequency-independent components. Thus, an equivalent circuit model characterizing these frequency-variant effects with frequency-independent components is proposed in this project.

4.1.1 Schematic Model Diagram

According to the notion described by Edwards and Steer in [18], when the length of the interconnect is less than $\frac{1}{20}$ of the wavelength λ , the signal can be deemed to be reasonably constant along the entire length. Hence a lumped one- Π model (Fig. 4.1) is adequate. This one- Π model topology is widely used in the modeling of on-chip inductors [68, 84, 85].

Figure 4.1: Schematic diagram of one- Π model [51]

With the increase in the length of the interconnect, the distributed effect begins to show its impact. When the length is longer than $\frac{1}{10}$ of λ , the transmission line model should be used [18]. λ is calculated using Eq. 4.1.1.

Table 4.1: Critical Length of various frequency

Frequency (GHz)	0.5	5	15	25
lumped element model (μm)	8695.6	869.6	289.9	173.9
transmission line model (μm)	17391.2	1739.1	579.8	347.8

$$\lambda = \frac{c}{\sqrt{\mu_r \varepsilon_r} f} \quad (m) \quad (4.1.1)$$

where c is the speed of light in free space ($3 \times 10^8 \text{m/s}$), f is the frequency under consideration, μ_r and ε_r are the relative permeability and permittivity of the material in which the signal propagates in. $\mu_r = 1$ and $\varepsilon_r = 11.9$ are used here to represent the silicon based process.

The criteria for choosing the model topology at various operating frequencies are summarized in Table 4.1.

In Table 4.1, it reveals that for the intended frequency range, i.e., from 500 MHz to 25 GHz, the one- Π model is suitable only when the lengths are less than 174 μm , otherwise the validity of the model cannot be guaranteed. The transmission line model is appropriate only when the lengths are longer than 17391 μm ; otherwise, it is not necessary to employ this topology. As stated in Chapter 3, the lengths of our test structures vary from 100 μm to 800 μm . Both the lumped one- Π model and the transmission line model are therefore not ideal. The proposed model should be capable of characterizing high frequency behaviors of the interconnects while keeping the model simple.

Figure 4.2: Schematic block diagram of two- Π model

In order to maintain the simplicity, the proposed model is developed based on the one- Π model. The problem of the one- Π model is that it cannot characterize the distributed effect which is significant at high frequencies. In our work, by strategically cascading two- Π lumped blocks together, as illustrated in Fig. 4.2, the distributed effects can be represented. The validity of the model will be demonstrated in Chapter 6. In order to simplify the model construction and parameter extraction, series blocks and shunt blocks of each Π are made to be identical. This optimization is physically acceptable due to the symmetrical structure of the interconnect.

As shown in Fig. 4.3, based on the schematic block model, a two- Π equivalent circuit model is proposed from a physical point of view.

Traditionally, on-chip interconnects were modeled as coupled RC networks [52]. The impact of the magnetic field was generally neglected. However, with the significant increase in operating frequency, the impact of magnetic field and magnetic coupling becomes one of the most emergent concerns of RFIC design [22, 45]. In the proposed model, the inductance is introduced by L_s , which represents the ideal series

Figure 4.3: Equivalent circuit model for straight-line interconnects

inductance.

In RFICs, as the operating frequency approaches multi-Gigahertz, the skin effect becomes very significant. Although it must be included in the simulation, frequency-variant components are not supported by conventional circuit simulators. Hence, mimicking the frequency-variant skin effect with frequency-independent components becomes the straightforward solution.

In Fig. 4.3, the series components R_{sk} and L_{sk} connected in parallel in our proposed model are introduced to characterize the skin effect. As stated above, due to the skin effect, the behavior of the interconnect becomes more resistive rather than inductive at high frequencies. In this parallel branch at low frequencies, most of the currents pass through L_{sk} . When the operating frequency rises, more currents shift to the path of R_{sk} . With these two frequency-independent components, the frequency-variant skin effect characteristics are thus well captured.

Besides the skin effect, at gigaHertz frequencies the substrate losses are also substantial. In current CMOS RF technologies, high frequency losses are caused by the low-resistivity substrate [5, 49, 50]. The substrate affects interconnects in two ways: eddy current losses and displacement current losses. The eddy currents in the substrate are induced by the current flowing through the conductor. The eddy currents, in turn, change the magnetic field and the inductance of the conductor. Particularly, if a high conductivity substrate is used at high frequencies, strong eddy currents will crowd near the surface of the substrate. As a result, inductance is reduced and significant eddy current losses occur. In a direct current (DC), no eddy currents are induced. The inductance is as the same as that in free space. As frequency increases, eddy currents become stronger and are more crowded at the surface. Changes to the inductance and eddy current losses become more noticeable. This effect is characterized by L_{sk} and R_{sk} as well. As the frequency increases, the flow of the current shifts from L_{sk} to R_{sk} . Hence, the equivalent inductance reduces and the loss increases.

Another part of the substrate losses is derived from the substrate injection of the displacement currents. The displacement currents flow through the capacitance which terminates on the substrate. This results in additional resistive losses. The capacitance in the substrate is frequency-variant as well. It is larger at higher frequencies because of skin effect of both the conductor and the substrate, as well as the frequency dependence of the effective permittivity [18]. This effect is modeled by the resistor and capacitors in the shunt block. The shunt block is proposed in Fig.

4.3, where C_{ox} represents the oxide layer capacitance; R_{sub} represents the substrate resistance; C_{sub} represents the capacitance of the substrate.

4.2 Interconnects with Bends

According to the physical configuration of the test structures (Fig. 3.3), the entire tracing of the interconnects with bends can be divided into different sub-segments, i.e., straight-line segments and corner segments. The structural analysis and nomenclatures are illustrated in Fig. 4.4.

Figure 4.4: Structural analysis of interconnect with bends

Henceforth, the model development methodology can be proposed. Firstly, a complex-shaped interconnect is decomposed into subsegments (Fig. 4.5). Secondly, equivalent circuit models are developed for these subsegments. Lastly, the subsegments are cascaded to form the model of the entire interconnect.

Figure 4.5: Schematic block model of interconnect with bends

4.2.1 Corner Segment

The lumped equivalent circuit model for microstrip bends [18] is introduced in Fig. 4.6. However, this model is unable to sufficiently characterize the lossy substrate in the CMOS process, which is commonly used for RFIC designs.

Figure 4.6: Original equivalent circuit model of the corner segment [18]

A T-network (Fig. 4.7) is thus proposed for the interconnect bends of the CMOS process.

Figure 4.7: Modified equivalent circuit model of the corner segment

Currents that flow round the corners distribute unevenly, such that most of the flows crowd around the inner edge [18]. Given in [86], the sheet resistance of straight lines is R_{square} , and the sheet resistance of corners is approximately $0.6 \times R_{square}$. Additionally, considering the relatively smaller physical size of the corner compared to the straight line, R_b can be removed from the series branch. Moreover, a further simplification of the shunt block does not reduce the precision of the model significantly. Thus, the model can be further simplified as shown in Fig. 4.8.

Figure 4.8: Simplified equivalent circuit model of the corner segment

Figure 4.9: Illustration of the application of factor α

4.2.2 Cascading of Subsegments

The construction for the complex-shaped interconnect model seems quit straightforward. However, simply connecting the subsegments together will not lead to a precise model. The reason is that the inductance of a curved interconnect does not equal to the sum of the inductances of the straight-line subsegments. Due to the mutual inductance cancelation of different subsegments, the general trend is that the larger curvature an interconnect has the smaller is the inductance [87]. In order to characterize this effect, the series inductance in the Π -network of the straight-line segments which is connected to the corner segment should be modified. An additional parameter α ($0 < \alpha < 1$), i.e., the multiplication factor, is introduced to represent this variation of the inductance. As illustrated in Fig. 4.9, inductance L_s in the second Π -network of *Straight-line Segment 1*, L_s in both of the two Π -networks of *Straight-line Segment 2*, and L_s in the first Π -network of *Straight-line Segment 3* are multiplied with the multiplication factor α . The influences of the corner can be omitted in the shunt blocks of the straight-line segments, so that the

parameters are kept unchanged.

4.3 Summary

In this chapter, the methodology of model development for complex shaped RF on-wafer interconnects is presented.

A two- Π lumped equivalent circuit model is proposed for the straight-line segment. The inductive property, as well as the skin effect and the substrate losses at high frequencies, are considered. The distributed effect is also included. A simplified T-lumped equivalent circuit model is proposed for the corner segment. The equivalent circuit of the entire interconnect is obtained by cascading basic subsegment models - the straight-line segment and corner segment - according to its physical structure.

It is highlighted that the proposed model is capable of characterizing the frequency-variant features of RF interconnects with frequency-independent components. It can be easily implemented in standard simulation environments, such as SPICE. Moreover, given the compact nature of the model, sophisticated EM background is not required by circuit simulations. These advantages make it convenient for IC designers to use.

Chapter 5

Model Parameter Extraction

5.1 Straight-Line Interconnects

5.1.1 Objective Function

In the parameter extraction stage, an objective function is formulated to which an optimization algorithm is applied. All optimizations were made based on on-wafer measurements of the test structures.

The function formulation is summarized as follows. Firstly, the admittance of each sub-block (as shown in Fig. 4.2) is derived as a function of the circuit components.

$$Y_1 = \frac{1}{j\omega L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}}} \quad (5.1.1)$$

$$Y_2 = \frac{1}{\frac{1}{j\omega C_{ox}} + \frac{R_{sub}}{j\omega C_{sub}R_{sub}+1}} \quad (5.1.2)$$

The Y-parameters are presented as functions of the admittance of each sub-block Y_1 and Y_2 , as illustrated in Eq. (5.1.3) to Eq. (5.1.6) [51]:

$$Y_{11} = Y_2 + \frac{Y_1(Y_1 + 2Y_2)}{2(Y_1Y_2)} \quad (5.1.3)$$

$$Y_{12} = -\frac{1}{\frac{Y_1+2Y_2}{Y_1^2} + \frac{1}{Y_1}} \quad (5.1.4)$$

$$Y_{21} = -\frac{1}{\frac{Y_1+2Y_2}{Y_1^2} + \frac{1}{Y_1}} \quad (5.1.5)$$

$$Y_{22} = Y_2 + \frac{Y_1(Y_1 + 2Y_2)}{2(Y_1Y_2)} \quad (5.1.6)$$

On the other hand, the measured S-parameters are converted into Y-parameters, based on the equations from Eq. (5.1.7) to Eq. (5.1.10) [51] as follows:

$$Y_{11} = \frac{1}{Z_0} \times \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \quad (5.1.7)$$

$$Y_{12} = \frac{1}{Z_0} \times \frac{-S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \quad (5.1.8)$$

$$Y_{21} = \frac{1}{Z_0} \times \frac{-S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \quad (5.1.9)$$

$$Y_{22} = \frac{1}{Z_0} \times \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} \quad (5.1.10)$$

where Z_0 is the characteristic impedance of the interconnects under test, which is

50 Ω in this work.

By combining Eq. (5.1.3) - Eq. (5.1.6) with Eq. (5.1.7) - Eq. (5.1.10), Eq. (5.1.11) - Eq. (5.1.14) are obtained. Solving the substitution gives the values of Y_1 and Y_2 .

$$\frac{1}{Z_0} \times \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} = Y_2 + \frac{Y_1(Y_1 + 2Y_2)}{2(Y_1Y_2)} \quad (5.1.11)$$

$$\frac{1}{Z_0} \times \frac{-S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} = -\frac{1}{\frac{Y_1 + 2Y_2}{Y_1^2} + \frac{1}{Y_1}} \quad (5.1.12)$$

$$\frac{1}{Z_0} \times \frac{-S_{12}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} = -\frac{1}{\frac{Y_1 + 2Y_2}{Y_1^2} + \frac{1}{Y_1}} \quad (5.1.13)$$

$$\frac{1}{Z_0} \times \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}} = Y_2 + \frac{Y_1(Y_1 + 2Y_2)}{2(Y_1Y_2)} \quad (5.1.14)$$

Therefore, the model parameter extraction becomes an optimization. The objective function $F_0(X)$ of the optimization in Eq. (5.1.15) can be divided into two parts using the plus sign. The first part is the average error between the derived admittances and those obtained from measurements. The second part is the variance of the error. The proposed $F_0(X)$ is:

$$F_0(X)|_{X=(X_1, X_2, \dots, X_n)} = \sum_{i=1}^m (f_i(X)^2 + [f_i(X) - F_{mean}]^2) \quad (5.1.15)$$

In Eq. (5.1.15), the vector $X = (X_1, X_2, \dots, X_n)$ represents the component values to be extracted (L_s, R_s, L_{sk} and R_{sk} of block Y_1 and C_{ox}, C_{sub} and R_{sub} of block Y_2). n is the total number of parameters in each block. m is the total number of frequency

points under consideration. $f_i(x)$ is the error between the simulated admittance and the ones obtained from measurement results at each frequency point. The definition of $f_i(x)$ is given in Eq. (5.1.16). F_{mean} in Eq. (5.1.17) is the mean error of the whole concerned frequency range.

$$f_i(X) = \left| \frac{Y_{simulated(i)} - Y_{measured(i)}}{Y_{measured(i)}} \right| \quad (5.1.16)$$

$$F_{mean} = \frac{\sum_{i=1}^m f_i(X)}{m} \quad (5.1.17)$$

5.1.2 Application of Optimization Algorithms

Application of HGA

A Hybrid Genetic Algorithm (HGA) is employed to search for optimal model parameters. The algorithm is named as a hybrid GA because in the evaluation stage, the *fminsearch* function provided by Matlab is employed. The flowchart of the proposed HGA is illustrated in Fig. 5.1. There are 20 chromosomes in the population pool. Each chromosome is a vector consisting of values of L_s , R_s , L_{sk} and R_{sk} of block Y_1 and C_{ox} , C_{sub} and R_{sub} of block Y_2 . The fitness value of each chromosome is evaluated according to the objective junction $F_0(X)$ presented in Eq. (5.1.15). Chromosomes with smaller fitness values have more chance to be selected to reproduce. The generated offsprings are then evaluated and selected, and crossover

is performed. The cycle is repeated. When the change in the fitness value of the fittest chromosome is less than 0.05 for 20 iterations, the optimization process is terminated. The computed results will be the optimized component values which are able to fit the simulated data with the measured data.

Figure 5.1: Flowchart of the proposed HGA

Application of PSO

PSO is also used for the parameter extraction. The procedure is summarized as follows:

- (1) Initialize a population pool of particles with random positions and velocities in the problem space. The population size is set at 20 in this work.
- (2) Evaluate the fitness values according to Eq. (5.1.15).
- (3) Compare each particle's fitness value against the record of $pbest$. If the current value is smaller than the value of $pbest$, $pbest$ is changed to the current value and its location is replaced with the current location vector.
- (4) Compare $pbest$ of each particle with $gbest$. If the current value is smaller than $gbest$, change $gbest$ into the current value and keep track of the location.
- (5) Change the velocity and position of the particle according to Eq. (2.4.16) and Eq. (2.4.17). In this work, $w=[0.4, 0.9]$, $c_1=1$, $c_2=3$.
- (6) Repeat step (2) until the terminating condition is satisfied, i.e., the change of the fitness value is less than 0.05 for 20 iterations of the objective function.

Performance Analysis

The optimization performances of HGA and PSO are compared. In order to make the comparison, the population size, terminating condition and fitness function are set the same. The comparison results are given in Table 5.1.

It can be seen that PSO reaches the optima significantly faster than HGA. The computation time is saved as much as 18.3%. However, the accuracy is slightly compromised.

Table 5.1: Comparison of performance between PSO and HGA for straight-line interconnects

Method		Error (%)	Time (s)
HGA	F_{10}	0.476	2.514
	F_{20}	1.243	2.855
PSO	F_{10}	0.483	1.920
	F_{20}	1.260	1.447

5.2 Interconnects with Bends

5.2.1 Objective Function

The parameter extraction of the interconnect with bends can also be formulated as an objective function.

As shown in Fig. 4.4, three straight-line segments and two corner segments are cascaded in a sequence. Therefore, in order to get the ABCD matrix of the whole trace, five corresponding ABCD matrixes of each segment are multiplied (Eq. (5.2.18)).

$$T_{wire} = T_{\Pi} \cdot T_{\Pi corner} \cdot T_{corner} \cdot T_{\Pi corner} \cdot T_{\Pi corner} \cdot T_{corner} \cdot T_{\Pi corner} \cdot T_{\Pi} \quad (5.2.18)$$

where T_{Π} denotes the ABCD matrix of each Π -network of the equivalent circuit model in Fig. 4.3; $T_{\Pi corner}$ denotes the ABCD matrix of the Π -network, which is influenced by the corner; and T_{corner} denotes the ABCD matrix of the corner segment.

T_{corner} (Eq. (5.2.19)) can be derived as a function matrix of the circuit components

L_b , R_b and C_b , based on the proposed model shown in Fig. 4.8. The elements of T_{corner} are presented in Eq. (5.2.20) - Eq. (5.2.23).

$$T_{corner} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \quad (5.2.19)$$

where

$$A = 1 + \frac{j\omega L_b}{\frac{1}{j\omega C_b} + R_b} \quad (5.2.20)$$

$$B = 2j\omega L_b - \frac{\omega^2 L_b^2}{\frac{1}{j\omega C_b} + R_b} \quad (5.2.21)$$

$$C = \frac{1}{\frac{1}{j\omega C_b} + R_b} \quad (5.2.22)$$

$$D = 1 + \frac{j\omega L_b}{\frac{1}{j\omega C_b} + R_b} \quad (5.2.23)$$

T_{Π} is defined based on Eq. (5.2.24) - Eq. (5.2.28). The derived ABCD matrix elements are functions of the equivalent circuit components L_s , R_s , L_{sk} , R_{sk} , C_{ox} , C_{sub} and R_{sub} .

$$T_{\Pi} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \quad (5.2.24)$$

where

$$A = 1 + \frac{j\omega C_{ox}(j\omega C_{sub} + \frac{1}{R_{sub}})(j\omega L_s + R_s + \frac{j\omega L_{sk}R_{sk}}{j\omega L_{sk} + R_{sk}})}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}} \quad (5.2.25)$$

$$B = j\omega L_s + R_s + \frac{j\omega L_{sk}R_{sk}}{j\omega L_{sk} + R_{sk}} \quad (5.2.26)$$

$$C = \frac{2j\omega C_{ox}(j\omega C_{sub} + \frac{1}{R_{sub}})}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}} + (j\omega L_s + R_s + \frac{j\omega L_{sk}R_{sk}}{j\omega L_{sk} + R_{sk}}) \left[\frac{j\omega C_{ox}(j\omega C_{sub} + \frac{1}{R_{sub}})}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}} \right]^2 \quad (5.2.27)$$

$$D = 1 + \frac{j\omega C_{ox}(j\omega C_{sub} + \frac{1}{R_{sub}})(j\omega L_s + R_s + \frac{j\omega L_{sk}R_{sk}}{j\omega L_{sk} + R_{sk}})}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}} \quad (5.2.28)$$

The matrix elements presented in Eq. (5.2.25) to Eq. (5.2.28) are for the Π -network without corner influence. For the corner-influenced Π -network, $T_{\Pi corner}$ is similar to T_{Π} . We just have to replace the item L_s with $\alpha \cdot L_s$ to account for the corner effect as illustrated in Eq. (5.2.29) - Eq. (5.2.33).

$$T_{\Pi corner} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \quad (5.2.29)$$

where

$$A = 1 + \frac{j\omega C_{ox}(j\omega C_{sub} + \frac{1}{R_{sub}})(j\omega \alpha L_s + R_s + \frac{j\omega L_{sk}R_{sk}}{j\omega L_{sk} + R_{sk}})}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}} \quad (5.2.30)$$

$$B = j\omega\alpha L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}} \quad (5.2.31)$$

$$C = \frac{2j\omega C_{ox}(j\omega C_{sub} + \frac{1}{R_{sub}})}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}} + (j\omega\alpha L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}}) \left[\frac{j\omega C_{ox}(j\omega C_{sub} + \frac{1}{R_{sub}})}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}} \right]^2 \quad (5.2.32)$$

$$D = 1 + \frac{j\omega C_{ox}(j\omega C_{sub} + \frac{1}{R_{sub}})(j\omega\alpha L_s + R_s + \frac{j\omega L_{sk} R_{sk}}{j\omega L_{sk} + R_{sk}})}{j\omega C_{ox} + j\omega C_{sub} + \frac{1}{R_{sub}}} \quad (5.2.33)$$

The values of all the components in the straight-line segment, namely L_s , R_s , L_{sk} , R_{sk} , C_{ox} , C_{sub} and R_{sub} are obtained from the previous section. Thereafter, the ABCD matrix of the entire wire are interpreted as functions of L_b , C_b , R_b and α . Corresponding S-parameters are expressed as functions of these variables under the following transformation formulas from Eq. (5.2.34) to Eq. (5.2.37).

$$S_{11} = \frac{A + \frac{B}{Z_0} - CZ_0 - D}{A + \frac{B}{Z_0} + CZ_0 + D} \quad (5.2.34)$$

$$S_{12} = \frac{2(A + \frac{B}{Z_0} - CZ_0 - D)}{A + \frac{B}{Z_0} + CZ_0 + D} \quad (5.2.35)$$

$$S_{21} = \frac{2}{A + \frac{B}{Z_0} + CZ_0 + D} \quad (5.2.36)$$

$$S_{22} = \frac{-A + \frac{B}{Z_0} - CZ_0 + D}{A + \frac{B}{Z_0} + CZ_0 + D} \quad (5.2.37)$$

The proposed objective function $F_0(X)$ can then be obtained as Eq. (5.2.38).

$$\begin{aligned} F_0(X)|_{X=(\alpha, L_b, C_b, R_b)} &= \sum_{i=1}^m (f_{1i}^2(X) + [f_{1i}(X) - F_{1mean}]^2 \\ &\quad + f_{2i}^2(X) + [f_{2i}(X) - F_{2mean}]^2) \end{aligned} \quad (5.2.38)$$

where m is the total number of the frequency points under consideration. f_{1i} is the error between the simulated S_{11} and those acquired from the measured results at each frequency point i . It is stated in Eq. (5.2.39). f_{2i} is the error between the simulated S_{21} and the measured results at each frequency point i , which is stated in Eq. (5.2.40). F_{1mean} and F_{2mean} (Eq. (5.2.41) and Eq. (5.2.42)) are the mean errors of S_{11} and S_{21} at each frequency point i . Given the symmetry of the interconnect test structure, it is known that $S_{ij}=S_{ji}$ and $S_{ii}=S_{jj}$ [57]. We apply the average value of the measured S_{11} and S_{22} , S_{12} and S_{21} as follows. They are denoted by S'_{11} and S'_{21} , respectively.

$$f_{1i}(X) = \left| \frac{S_{11-i_simulated} - S'_{11-i_measured}}{S'_{11-i_measured}} \right| \quad (5.2.39)$$

$$f_{2i}(X) = \left| \frac{S_{21-i_simulated} - S'_{21-i_measured}}{S'_{21-i_measured}} \right| \quad (5.2.40)$$

$$F_{1mean} = \frac{\sum_{i=1}^m f_{1i}(X)}{m} \quad (5.2.41)$$

$$F_{2mean} = \frac{\sum_{i=1}^m f_{2i}(X)}{m} \quad (5.2.42)$$

5.2.2 Performance Analysis of Applied Optimization Algorithms

Both HGA and PSO are employed for the model parameter extraction. In order to make comparisons, all the simulation settings, including the objective function, the population size and the terminating condition, are ensured to be similar. The comparison results are given in Table 5.2.2.

Table 5.2: Comparison of performance between PSO and HGA for interconnects with bends

Applied Methodology	Error (%)	Time (s)
HGA	2.067	244.84
PSO	2.922	209.15

From Table 5.2.2, it is clear that PSO edges towards the optima significantly faster than HGA, however the accuracy is compromised.

5.3 Summary

Problems of model parameter extraction are formulated into objective functions.

Two different optimization algorithms, namely, HGA and PSO are applied. It can

been observed from both Table 5.1 and Table 5.2.2 that HGA yields less error, but takes a longer time to optimize. PSO offers shorter searching time, but its accuracy is slightly less than that of HGA. In the solution of the two problems specified in this thesis, the accuracy and the searching time of both HGA and PSO are acceptable. It implies that either of the two can be selected as the optimization algorithm for similar cases depending on the researcher's preference.

Chapter 6

Results and Verification

6.1 Straight-Line Interconnects

With the extracted component values of various interconnect dimensions, empirical formulas of the circuit components are summarized as functions of design parameters. Therefore, with every set of the length (l) in the unit of μm and width (W) in the unit of μm , the model components can be calculated.

The summarized formulas are presented below. A Software named DataFit by Oakdale Engineering was used for the empirical formula formulation and the coefficient extraction. By importing the component values and the corresponding geometrical information, the software returns a report, including the possible expressions of the component as a function of the geometrical parameters, standard errors, confidence intervals and residual probabilities, etc.

The formulated expressions for L_s and L_{sk} are defined in Eq. (6.1.1) and Eq. (6.1.2).

The corresponding coefficients for each expression are shown in Table 6.1 and 6.2.

$$L_s = a + bl + c\ln W + d(\ln W)^2 + e\ln W \quad (H) \quad (6.1.1)$$

$$(1.5\mu m \leq W \leq 20\mu m)$$

Table 6.1: Coefficients of L_s

Coefficient	Value
a	-7.31643E-12
b	5.51876E-13
c	1.37238E-11
d	-4.13401E-12
e	-7.0167E-14

$$L_{sk} = a + bl + \frac{c}{W} + \frac{d}{W^2} \quad (H) \quad (6.1.2)$$

$$(1.5\mu m \leq W \leq 20\mu m)$$

Table 6.2: Coefficients of L_{sk}

Coefficient	Value
a	-9.64956E-13
b	1.9307E-14
c	1.655E-11
d	1.99008E-11

From Eq. (6.1.1) and Eq. (6.1.2), it is observed that both the L_s and L_{sk} are proportional to the length and inversely proportional to the width of the interconnects. This can be explained with using EM concepts. When the length of the interconnect increases, the magnetic flux linkage also increases. As the inductors represent the magnetic energy storage capacity, the value of the inductance increases. When

the interconnect has a narrower width, the cross section is also smaller. Hence it generates more magnetic flux external to the wire and the inductance increases [67].

The formulas for R_s and R_{sk} are presented in Eq. (6.1.3) and Eq. (6.1.4) respectively.

The related coefficients are listed in Table 6.3 and Table 6.4.

$$R_s = a + bl + \frac{c}{W} + \frac{d}{W^2} \quad (\Omega) \quad (6.1.3)$$

$$(1.5\mu m \leq W \leq 20\mu m)$$

Table 6.3: Coefficients of R_s

Coefficient	Value
a	0.03644663
b	5.76521E-4
c	0.04092424
d	-0.246694897

$$R_{sk} = a + bl + \frac{c}{W} + \frac{d}{W^2} + \frac{el}{W} \quad (\Omega) \quad (6.1.4)$$

$$(1.5\mu m \leq W \leq 20\mu m)$$

Table 6.4: Coefficients of R_{sk}

Coefficient	Value
a	-0.124733535
b	1.670241E-3
c	2.018170489
d	-2.332177206
e	6.04339E-4

Observing Eq. (6.1.3) and Eq. (6.1.4), we can find that the two resistance are proportional to the length and inversely proportional to the width. It is congruent with the definition of the resistors.

Eq. (6.1.5) and Eq. (6.1.6) are expressions for C_{ox} and C_{sub} . The coefficients are presented in Table 6.5 and Table 6.6.

$$C_{ox} = a + bl + cW + dW^2 + eW^3 \quad (F) \quad (6.1.5)$$

$$(1.5\mu m \leq W \leq 20\mu m)$$

Table 6.5: Coefficients of C_{ox}

Coefficient	Value
a	4.58957E-17
b	1.16724E-17
c	2.69628E-18
d	-7.56085E-19
e	1.20727E-18

$$C_{sub} = al^bW^c \quad (F) \quad (6.1.6)$$

$$(1.5\mu m \leq W \leq 20\mu m)$$

Table 6.6: Coefficients of C_{sub}

Coefficient	Value
a	5.10835E-18
b	1.2102712
c	0.082382533

$$R_{sub} = al^bW^c \quad (\Omega) \quad (6.1.7)$$

$$(1.5\mu m \leq W \leq 20\mu m)$$

In Eq. (6.1.5) and Eq. (6.1.6), both of these capacitances are proportional to the length and the width, which agrees with our understanding of the definition of capacitors.

Table 6.7: Coefficients of R_{sub}

Coefficient	Value
a	1.233421E6
b	-1.146377345
c	-0.25549637

Eq. (6.1.7) and Table 6.7 are defined for R_{sub} .

From Eq. (6.1.7), R_{sub} is inversely proportional to both the length and the width. The reason is that the interconnect with a larger physical dimension has larger substrate losses. As a result, its equivalent substrate resistance is smaller.

With the aid of Matlab, simulations of the proposed two- Π lumped equivalent circuit model are performed based on the parameter values derived from the empirical formulas. The simulated S-parameters are compared with the corresponding measured ones. The plots are presented in Fig. 6.1 to Fig. 6.2. Based on the symmetry of the interconnect test structure, $S_{ij}=S_{ji}$ and $S_{ii}=S_{jj}$ [57]. Therefore, only S_{11} and S_{21} are compared here. The magnitudes and phases are plotted separately. An EM simulator IE3D from Zeland Software Inc. was employed for additional validation.

From these four figures, satisfactory agreements between the simulated S-parameters and the measurement results over a whole frequency range are achieved within a tolerance of 2%. It demonstrates that the proposed two- Π equivalent circuit model and the formulated empirical parameter expressions are capable of accurately characterizing the behaviors of the on-wafer straight-line interconnects over a large range of frequencies up to 20 GHz, which is adequate for RF applications.

6.1 Straight-Line Interconnects

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6.1.1: Comparison among modeled, IE3D simulated and measured magnitude of S_{11} 6.1.2: Comparison among modeled, IE3D simulated and measured phase of S_{11} Figure 6.1: Comparison among modeled, IE3D simulated and measured S_{11}

6.1 Straight-Line Interconnects

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6.2.1: Comparison among modeled, IE3D simulated and measured magnitude of S_{21} 6.2.2: Comparison among modeled, IE3D simulated and measured phase of S_{21} Figure 6.2: Comparison among modeled, IE3D simulated and measured S_{21}

6.3.1: Comparison between cascaded and measured magnitude of S_{11} 6.3.2: Comparison between simulated and measured phase of S_{11} Figure 6.3: Comparison between simulated and measured S_{11}

6.4.1: Comparison between cascaded and measured magnitude of S_{21} 6.4.2: Comparison between simulated and measured phase of S_{21} Figure 6.4: Comparison between simulated and measured S_{21}

6.5.1: Comparison of magnitude of S_{11} : measured and cascaded with two and four sections

6.5.2: Comparison of phase of S_{11} : measured and cascaded with two and four sections

Figure 6.5: Comparison of S_{11} : measured and cascaded with two and more sections

6.1 Straight-Line Interconnects

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6.6.1: Comparison of S_{21} : measured and cascaded with two and four sections 6.6.2: Comparison between simulated and measured phase of S_{21} Figure 6.6: Comparison of S_{21} : measured and cascaded with two and more sections

It is important to note that the given formulas of the model parameters are fit to our specific test chip and process. Moreover, these formulas are only valid within a geometrical range, which is within the coverage of our test structures. For the length, the valid range is from $100\text{ }\mu\text{m}$ to $800\mu\text{m}$; while for the width, they are only applicable between $1.5\text{ }\mu\text{m}$ and $20\mu\text{m}$. However, as stated in Chapter 3.1, most of the on-chip interconnects used in RFICs are within this range. The provided geometrical extent are sufficient in most cases. In rare cases, in which the lengths of the interconnects are beyond $800\text{ }\mu\text{m}$, a cascading methodology can be applied. Firstly, the long wire is split into smaller sections with lengths less than $800\text{ }\mu\text{m}$. Next, two- Π models are developed for each subsection. After that, the two- Π blocks are cascaded together to form the complete model for the entire wire. We have employed this method to form an $800\text{ }\mu\text{m}$ interconnect with two $400\text{ }\mu\text{m}$ subsections, and a $400\text{ }\mu\text{m}$ wire with two $200\text{ }\mu\text{m}$ subsections. Referring to Fig. 6.3 to Fig. 6.4, the simulated results agree well with the measurement data. These experiments also prove the scalability of our proposed model. In Fig. 6.5 and Fig. 6.5, two $800\text{ }\mu\text{m}$ interconnects, with the width of $1.5\text{ }\mu\text{m}$ and $20\text{ }\mu\text{m}$ were formed by cascading two $400\text{ }\mu\text{m}$ sections and four $200\text{ }\mu\text{m}$ sections respectively. It could be observed that, the accuracy for larger number of cascaded subsections is lower, however it is still acceptable.

6.2 Interconnects with Bends

The extracted model parameters of the corner segment by using DataFit are summarized in Table 6.8, Table 6.9 and Table 6.10.

Table 6.8: Extracted Multiplication Parameter α

Angle ($^{\circ}$)	45	90
α	0.90	0.82

Table 6.9: Extracted Parameters of the 45° Angled Corner Segment

Parameter	W=3 (μm)	W=5 (μm)	W=10 (μm)	W=20 (μm)
L_b (pH)	1.339	2.718	5.910	9.535
C_b (fF)	1.023	2.677	4.016	7.356
R_b (k Ω)	20.041	18.712	16.122	15.433

Table 6.10: Extracted Parameters of 90° Angled Corner Segment

Parameter	W=3 (μm)	W=5 (μm)	W=10 (μm)	W=20 (μm)
L_b (pH)	1.452	3.089	6.563	9.706
C_b (fF)	1.521	3.122	4.725	7.118
R_b (k Ω)	19.430	16.025	14.069	12.040

Table 6.8 shows the multiplication factor α . Table 6.9 and Table 6.10 illustrate the component values of the 45° and 90° corner segment respectively. From Table 6.8, it is observed that α is smaller than 1 in both of the two cases. The value of α of the 90° corner segment is smaller than that of the 45° corner segment. This is explained in Chapter 4.2.2. The multiplication parameter applied to L_s is introduced to characterize the inductance reduction which is the result of mutual inductance cancelation of different subsegments. The general trend is that the larger

curvature an interconnect has, the smaller the inductance is. Hence, α should always be smaller than 1 and inversely proportional to the curvature of the interconnect.

The component values of the corner segment model are summarized as functions of the width of the interconnect (W) (μm) with the aid of the software DataFit by Oakdale Engineering. The summarized formulas (Eq. (6.2.8) - Eq. (6.2.13)) are presented one by one as listed below. The coefficients of each formula are listed in separate tables (Table 6.11 - Table 6.16).

45° bends:

$$L_b = a + b \ln W + \frac{c}{W^2} \quad (pH) \quad (6.2.8)$$

$$(3\mu\text{m} \leq W \leq 20\mu\text{m})$$

Table 6.11: 45° bends: Coefficients of L_b

Coefficient	Value
a	-6.839120451
b	5.449835441
c	19.71196245

$$C_b = a + bW^3 + \frac{c}{W^{1.5}} \quad (fF) \quad (6.2.9)$$

$$(3\mu\text{m} \leq W \leq 20\mu\text{m})$$

Table 6.12: 45° bends: Coefficients of C_b

Coefficient	Value
a	4.070618918
b	4.331584189E-4
c	-15.93719268

$$R_b = a + bx + c \frac{\ln W}{W} \quad (K\Omega) \quad (6.2.10)$$

$$(3\mu m \leq W \leq 20\mu m)$$

Table 6.13: 45° bends: Coefficients of R_b

Coefficient	Value
a	3.417349987
b	0.2775711464
c	43.15074288

90° bends:

$$L_b = a + bW + cW^{2.5} \quad (pH) \quad (6.2.11)$$

$$(3\mu m \leq W \leq 20\mu m)$$

Table 6.14: 90° bends: Coefficients of L_b

Coefficient	Value
a	-1.192315505
b	0.901463848
c	-3.986251312E-3

$$C_b = a + bW^2 + \frac{c}{W} \quad (fF) \quad (6.2.12)$$

$$(3\mu m \leq W \leq 20\mu m)$$

Table 6.15: 90° bends: Coefficients of C_b

Coefficient	Value
a	5.244102649
b	6.104506355E-3
c	-11.34178096

$$R_b = a + bW^{1.5} + \frac{c}{W^2} \quad (K\Omega) \quad (6.2.13)$$

$$(3\mu m \leq W \leq 20\mu m)$$

Table 6.16: 90° bends: Coefficients of R_b

Coefficient	Value
a	14.5363397
b	-0.02917570996
c	45.4040604

With the aid of Matlab, simulations of the proposed model are performed based on the methodology described in the previous sections. Since $S_{ij}=S_{ji}$ and $S_{ii}=S_{jj}$ [57], only S_{11} and S_{21} are compared here. The simulated S-parameters are compared with the corresponding measured ones. The plots are presented in Fig. 6.7 to Fig. 6.10. The magnitudes and phases are plotted separately. In each of the eight figures, there are four different dimensions of the test structures. These are described in Section III Part A. The lengths are fixed at 300 μm . The widths range from 20 μm , 10 μm , 5 μm and 3 μm .

Fig. 6.7 illustrates the comparative results of interconnects with 45° bends. Fig. 6.7.1 and Fig. 6.7.2 compare the simulated and measured magnitude and phase of S_{11} respectively. Fig. 6.8.1 and Fig. 6.8.2 show the comparisons of the magnitude and phase of S_{21} respectively. Fig. 6.9 shows the comparative results of interconnects with 90° bends. Fig. 6.9.1 and Fig. 6.9.2 compare the simulated and measured magnitude and phase of S_{11} respectively. Fig. 6.10.1 and Fig. 6.10.2 illustrate the comparisons of magnitude and phase of S_{21} respectively.

From Fig. 6.7 to Fig. 6.10, satisfactory agreement is achieved between the simulated S-parameters and the measured results over the whole frequency range. The error is less than 7%. It demonstrates that the proposed model and the extracted parameters

6.7.1: Comparison between simulated and measured magnitude of S_{11} with 45° bends

6.7.2: Comparisons between simulated and measured phase of S_{11} with 45° bends

Figure 6.7: Comparisons between simulated and measured of S_{11} with 45° bends

6.8.1: Comparison between simulated and measured magnitude of S_{21} with 45° bends

6.8.2: Comparison between simulated and measured phase of S_{21} with 45° bends

Figure 6.8: Comparison between simulated and measured of S_{21} with 45° bends

6.9.1: Comparison between simulated and measured magnitude of S_{11} with 90° bends

6.9.2: Comparison between simulated and measured phase of S_{11} with 90° bends

Figure 6.9: Comparisons of simulated and measured of S_{11} with 90° bends

6.10.1: Comparison between simulated and measured magnitude of S_{21} with 90° bends

6.10.2: Comparison between simulated and measured phase of S_{21} with 90° bends

Figure 6.10: Comparisons of simulated and measured of S_{21} with 90° bends

are capable of accurately characterizing the behaviors of the on-wafer interconnect with bends over a large range of frequencies of up to 20 GHz.

6.3 Summary

The extracted model components are formulated into empirical expressions. Thus, once the physical dimension of the interconnect is given, the component values of the equivalent circuit model is obtainable.

The accuracy of the models are verified with on-wafer measurements. The error of the straight-line interconnects is less than 2 %, while the error of the interconnects with bends is within the tolerance of 7 %. Additionally, the scalability of the proposed model has also been demonstrated.

Chapter 7

Implementation

The ultimate targets for the proposed interconnect model are to provide IC designers with efficient interconnects at the design stage and also to ensure easy implementation in commercial EDA tools. Therefore, design iterations after tapeout or too much over-design can be prevented. In this chapter, the proposed interconnect model is used in the post-layout simulation of a transimpedance amplifier (TIA). Simulation results using the proposed model and the foundry-provided model are compared with on-wafer measurements. The feasibility of using the proposed model is demonstrated.

7.1 Transimpedance Amplifier

The dramatic growth of data transportation volume and speed over the Internet in recent years entails the development of low-cost, integrated optical communi-

cation systems with the ever-increasing transmission bandwidth [88]. Currently, the most successful high-speed digital communication is SONET OC-192. The 10 Gb/s Ethernet (IEEE 802.3ae) is also emerging as an alternative for point-to-point applications. Therefore, optical communication systems operating at 10 Gb/s is attractive [89, 90]. TIAs, which convert the current signals from photo-detectors to voltage signals, are essential building blocks of modern optical communication systems. The basic characteristic of a receiver front-end is determined by the performance of the TIA in terms of bandwidth and input referred noise. In high speed CMOS design, such performances are extremely susceptible to parasitic and interconnect effects and therefore need to be handled with great care. However, up to date, the relevant research is very rare.

The schematic of a TIA is shown in Fig. 7.1. The corresponding layout is illustrated in Fig. 7.3. The circuit is composed of four parts: the input matching network, the regulated cascode (RGC) input stage, the common source voltage gain stage, and the source-follower output stage. The parasitic capacitance of the photo-detector C_{pd} , the large gate capacitance of M_2 , and L_1 and L_2 , comprise the input matching network which is used to boost the bandwidth and optimize the noise performance. The RGC input stage, which consists of M_1 , M_2 , R_1 , R_2 and R_s is used to present very low input impedance. The common drain voltage gain stage is composed of M_4 , R_4 . R_c/C_c is designed to suppress intolerable gain overshoot as well as phase deviation at high frequencies which may lead to instability. R_F is the feedback resistor to relieve the stringent noise-bandwidth tradeoff. M_5 and R_5 together form

the source follower as the output buffer.

The TIA is designed and fabricated using CHRT's $0.18\ \mu\text{m}$ RF CMOS technology. It takes an area of $656\ \mu\text{m} \times 653\ \mu\text{m}$. The die photograph of the fabricated TIA is shown in Fig. 7.2. As stated in our previous work [91], the proposed model is only eligible for interconnects longer than $50\ \mu\text{m}$. In this work, the interconnects which are longer than $50\ \mu\text{m}$ in the layout, are referred to as critical interconnects. In Fig. 7.1, they are highlighted as shaded boxes; and in Fig. 7.3, the corresponding critical interconnects are also labeled.

Figure 7.1: Schematic diagram of the TIA with illustration of critical interconnects

Figure 7.2: Die photograph of the fabricated TIA

7.2 Comparisons and Analyses

7.2.1 Comparison of the Transimpedance

Post-layout simulations are performed for the layout of the TIA as shown in Fig. 7.3. The critical interconnects are characterized with CHRT's traditional RC model and our proposed model respectively. The comparison of their transimpedances (Z_{21}) are illustrated in Fig. 7.4.

Line A represents the measurement results. Line B characterizes simulation results

Figure 7.3: Layout of the TIA

using foundry-provided interconnect model, while Line C represents simulation results using the proposed interconnect model only. It is observed that the proposed model predicts the appearance and the value of the peak quite accurately, while the foundry-provided model fails to do so. However, the predicted bandwidth is 2 GHz wider compared to the measurements. The decrease of the bandwidth may be caused by the pad parasitics. Line D represents the simulation results after the addition of pad parasitics [92]. It is seen that the fitting is better. Nevertheless, the Q factor of the inductors decrease dramatically in the high frequency range. Hence, another reason for the decrease in bandwidth is due to the degradation of the employed inductors at high frequencies and the inadequate inductor model. Detailed

Figure 7.4: Comparison of transimpedance

analyses explaining the causes of the peaking of the transimpedance are given in the following paragraphs.

The first part of the proposed TIA circuit is the input matching network, which includes C_{pd} , C_{gs2} (the gate capacitance of M_2), L_1 and L_2 . The interconnection line between L_1 and L_2 (*Inter1*) will not introduce considerable impact due to its relatively shorter length and the fact that it is small as compared to L_1 and L_2 . However, the interconnection line between L_1 and the gate of M_2 (*Inter3*), as well as the line between the source of M_2 and ground (*Inter2*), cannot be neglected. The schematic diagram in Fig. 7.5 shows part of the input matching network and

Figure 7.5: Illustration of input matching network with interconnects

the corresponding interconnects. Without considering these interconnect effects, the gain of the circuit tends to drop as frequency increases due to the C_{gs2} capacitance connected directly to ground. However, in reality, the inductive effects of the two interconnect lines become significant at high frequencies. It counteracts the gain-roll-off effect and therefore helps to boost the bandwidth.

In the second part of the TIA, the interconnection line between L_2 and the source of M_1 (*Inter5*), as well as that between the gate of M_1 and the drain of M_2 (*Inter4*), need to be considered. The effects of these two interconnects on the bandwidth are insignificant. However, it is known that the first stage of the amplifier is the major noise contributor and inductive elements can reduce the noise. M_1 and M_2 are the first stage of the TIA and because of the inductive behavior of the interconnect at high frequencies, *Inter4* and *Inter5* may have a tuning effect on the noise performance.

As for the interconnection line to the supply voltage and ground (*Inter6* and *Inter7*), the interconnect effect is weak. At the output stage, the interconnect line between the output and M_5 (*Inter8*) also tends to boost the bandwidth due to its inductive effect.

7.2.2 Figure of Merit (FoM)

The equivalent input noise current, which is also called input referred noise current [93], is one of the TIA design's figures of merit (FoM). It directly affects the optical link budget [94]. Therefore, the noise performance of TIA is modeled in terms of the equivalent input noise current. This noise current, together with a noiseless TIA, reproduces the same output noise as the actual noisy TIA. Fig. 7.6 shows the comparison between the measured and simulated input referred noise current spectral density and the proposed interconnection model with the foundry-provided RC model.

Theoretically, the series inductors between the photodiode and the core TIA can help to reduce the input referred noise current [95]. Hence, simulation with series inductance of the interconnect should have better noise performance. In Fig. 7.6, the simulated noise with the proposed interconnection model is lower than that generated by the foundry-provided model. However, in reality, the noise performance is affected by many factors besides interconnects. From Fig. 7.6 it can be seen that the measured noise is much larger than the noises in all the simulations. Possible reasons for the large discrepancies may be: 1) Our measurement setup does not have

Figure 7.6: Comparison of input referred noise current

a shield chamber for the noise measurement; 2) The lack of accurate noise models from the foundry.

Phase linearity is another FoM of the TIA design to limit the generation of data-dependant jitter. Fig. 7.7 shows the comparisons of the simulated group delay employing the proposed interconnection model and the foundry provided RC model with on-wafer measurements. In Fig. 7.7, the simulated group delay from the proposed interconnection model has a significant peak. It is due to the peaking effect of the parasitic inductive element of the interconnection. However, the peak of the measurements is much smaller and appears at a much lower frequency. After considering the pad effect, the peak moves towards the lower frequency and the peak

value decreases. It fits the measured data better. Possible reason for the differences between the measured and simulation results may be the lack of accurate inductor models provided by the foundry.

Figure 7.7: Comparison of group delay

7.3 Summary

The proposed EDA tool-compatible interconnect models are used in the post-layout simulation of the TIA. Simulation results are verified with on-wafer measurements. The simulation with the proposed interconnect model successfully predicted the characteristics of the transimpedance, while the foundry-provided model fails to do so. Two other FoM of the TIA design, namely, the input noise current and phase

linearity, are also discussed. The importance of interconnect effects is demonstrated.

Chapter 8

Sensitivities of On-wafer

Interconnects to CMOS Process

Parameters at Radio Frequency

Due to the combination of the shrinking device size and the higher operating frequencies of CMOS ICs, circuit performance becomes more and more subjected to interconnect behaviors [96]. Process parameters are optimized to improve circuit performance. However, the influences of process parameter variations on interconnect behaviors have rarely been reported. In this Chapter, the sensitivities of both single-lined and coupled on-wafer interconnects are investigated. The influences of process parameters on interconnects at radio frequency are discussed. In this work we dedicate our study to the interconnect on the top metal layer, since it is most commonly allocated for routing critical high frequency paths.

8.1 Test Structure

In order to analyze the sensitivities of the on-wafer interconnects, a large number of interconnect samples with various process parameters are needed. There are two ways to obtain the required samples. The most straightforward way is to design and fabricate all the possible test structures with different process parameters. However, it is extremely costly, time consuming and impractical. An alternative way is to design and fabricate several typical test structures and conduct tests using an electromagnetic (EM) simulator. Using the fabricated samples to calibrate the EM simulator, other possible interconnect structures can be investigated using the calibrated simulator.

Figure 8.1: Cross view of test structure

In this work, IE3D from Zeland Software Inc. is employed to do the EM simulations. The cross views of the test structures are shown in Fig. 8.1. Fig. 8.1.(a) and Fig. 8.1.(b) are dedicated to investigate the single-line interconnect and coupled interconnects respectively.

Three sets of test structures using a $0.18\ \mu\text{m}$ RF CMOS process by CHRT are designed and fabricated. In order to verify the settings of the EM simulator, on-wafer measurements of the three sets of fabricated test structures are performed.

As an illustration, a single-line interconnect structure with a length of $400\ \mu\text{m}$ and width of $10\ \mu\text{m}$ is examined. S-parameters, i.e., S_{11} and S_{21} are investigated.

Figure 8.2: Top view of test structure

As for coupled interconnects, the top view and the assignment of the ports are shown in Fig. 8.2. The length (L) of both interconnects is $400\ \mu\text{m}$; the width (W) is $10\ \mu\text{m}$; and the line spacing (S) of the two interconnects is $10\ \mu\text{m}$. *Interconnect1* is assumed to be the active line and *Interconnect2* is assumed to be the victim line. An input signal is applied to *port1*. S-parameters, i.e., S_{11} , S_{21} , S_{31} and S_{41} are examined.

8.2 Influences of Process Parameters

Four major process parameters are considered, namely, the conductivity of the substrate, the permittivity of the dielectric, the thickness of the dielectric and the conductivity of the metallic conductor. During simulation, these four parameters are changed respectively. Only one parameter is changed each time while the rest are kept unchanged. The variation range of the parameters are chosen to emulate the state-of-the-art and future Si CMOS technologies.

8.2.1 Conductivity of the Substrate

In CMOS technology, low-resistivity substrate is used to improve the yields and suppress the latchup. The performance of on-wafer interconnects is significantly affected by the lossy nature of the silicon substrate [48]. In the current technology, the substrate conductivity (σ) is usually around 6 S/m to 50 S/m (2 Ω -cm to 18 Ω -cm) [45]. In some processes, the conductivity of the substrate may reach as high as 5×10^3 S/m to 1×10^4 S/m (10 $m\Omega$ -cm to 20 $m\Omega$ -cm) [97].

In order to study the influence of the substrate conductivity, typical values of 6 S/m, 50 S/m, 5×10^3 S/m, 1×10^4 S/m, and 19 S/m are used for the simulation. For single-lined interconnects, comparison between S_{11} and S_{21} are shown in Fig. 8.3 and Fig. 8.4. For coupled lines, comparison between S_{11} , S_{21} , S_{31} and S_{41} are shown in Fig. 8.6 to Fig. 8.9 respectively.

Unlike microstrip lines, S_{21} of interconnects using CMOS process does not increase

Figure 8.3: Single line: Comparison of S_{11} with respect to various substrate conductivities

with the decrease of the substrate conductivity. It can be explained with the help of the commonly-used shunt branch equivalent circuit model for CMOS inductors (Fig. 8.5) [69, 85]. The admittance of the shunt branch, including the dielectric layer and substrate layer, is described in Eq. (8.2.1).

$$Y = \frac{C_{ox}^2 G_{sub}}{(\frac{G_{sub}}{\omega})^2 + (C_{ox} + C_{sub})^2} + \frac{\omega C_{ox} G_{sub}^2 + \omega^3 (C_{ox} + C_{sub}) C_{ox} C_{sub}}{(G_{sub})^2 + \omega^2 (C_{ox} + C_{sub})^2} j \quad (8.2.1)$$

where C_{ox} is the capacitance of the dielectric layer; C_{sub} and G_{sub} are the capacitance

Figure 8.4: Single line: Comparison of S_{21} with respect to various substrate conductivities

and conductance of the substrate, respectively.

The equivalent admittance of the shunt branch is thus not a monotonic function of the substrate conductivity, although as a rule, the bigger the shunt conductivity, the more severe the loss and the smaller the S_{21} is.

For the coupled lines S_{11} , as shown in Fig. 8.6, its dependence on the substrate conductivity and its corresponding values are the same as that of the single-line interconnect (Fig. 8.3). It indicates that the reflection of the active line is not influenced much by the victim line. For S_{21} in Fig. 8.7, it follows the same trend as the single-line interconnect. However, for interconnects with low substrate conductivities, the corresponding values of S_{21} are lower than those of the single interconnect

Figure 8.5: Equivalent circuit model of the shunt branch

(Fig 8.4), while for interconnects with very high substrate conductivities, i.e., 5000 S/m and 10000 S/m, the values of S_{21} do not change much as compared to those of the single interconnect. The reason is that the energy loss caused by the coupling can be neglected compared to the substrate losses. Fig. 8.8 and Fig. 8.9 illustrate the coupling at the far-end and the near-end of the victim interconnect. It can be seen that the interconnect with a bigger S_{11} has a larger near-end coupling while the interconnect with a larger S_{21} experiences a larger far-end coupling. This is because the energy in the victim line originates from the energy in the active line. Given the same dielectric permittivity and interconnect physical dimension, the coupling capacitance [98] of the two interconnects is identical. The more energy at the active line, the more coupled energy at the corresponding victim line.

Figure 8.6: Coupled lines: Comparison of S_{11} with respect to various substrate conductivities

Figure 8.7: Coupled lines: Comparison of S_{21} with respect to various substrate conductivities

Figure 8.8: Coupled lines: Comparison of S_{31} with respect to various substrate conductivities

Figure 8.9: Coupled lines: Comparison of S_{41} with respect to various substrate conductivities

8.2.2 Distance from the Substrate

The current trend of metal technology scaling is shown in Fig. 8.10. Due to the increase of metal layers, the vertical dimensions do not scale down with the horizontal dimensions. Until 2007, there will be as many as 10 metal layers, and the distance of the top metal layer from the Si substrate will be as far as $16\ \mu\text{m}$ [99].

Fig. 8.2.2 and Fig. 8.2.2 compare the S_{11} and S_{21} of single-line interconnects with different distances from the top metal layer to the substrate. The three chosen distances are: $5.5\ \mu\text{m}$ (provided by CHRT), $16\ \mu\text{m}$ (predicted value for year 2007), and $10\ \mu\text{m}$ (a value in between).

Figure 8.10: Trend of the interconnect stack

Figure 8.11: Single line: Comparison of S_{11} with respect to various distances from the substrate

Figure 8.12: Single line: Comparison of S_{21} with respect to various distances from the substrate

In Fig. 8.2.2 and Fig. 8.2.2, it is shown that structures with larger distances from the substrate have larger S_{11} and S_{21} . The increase of S_{11} results from the mismatch against the 50Ω test system. As for S_{21} , it is affected by both of the reflection of the ports and the substrate losses. When the interconnect is further away from the substrate, it suffers less from substrate losses. Hence, although the mismatch reflection increases, the transmission of the interconnect is improved.

Figure 8.13: Coupled lines: Comparison of S_{11} with respect to various distances from the substrate

Figure 8.14: Coupled lines: Comparison of S_{21} with respect to various distances from the substrate

Figure 8.15: Coupled lines: Comparison of S_{31} with respect to various distances from the substrate

For the coupled lines, comparison of S_{11} to S_{41} with different top metal distances (T) from the substrate is illustrated in Fig. 8.2.2 to Fig. 8.2.2. The chosen distances are also $5.5 \mu\text{m}$, $10 \mu\text{m}$ and $16 \mu\text{m}$.

For S_{11} , as shown in Fig. 8.2.2, both its dependence on the substrate conductivity and the corresponding values are the same as those of single-line interconnects depicted in Fig. 8.2.2. It indicates that the reflection of the active line is not influenced much by the appearance of the victim line. For S_{21} , the same trend is observed. However, the corresponding values are smaller than those of the single-line interconnect in Fig. 8.2.2. The reason is that a portion of the input energy has been

Figure 8.16: Coupled lines: Comparison of S_{41} with respect to various distances from the substrate

coupled to the victim line.

Fig. 8.2.2 and Fig. 8.2.2 show that the coupling is more significant for interconnects that are located further from the substrate. Generally, metal layers further away from the substrate are recommended for critical interconnects to reduce the substrate losses. However, thicker dielectric also causes more coupling at the same time. This reduces the circuit performance.

8.2.3 Permittivity of the Dielectric

Recently, numerous low- k materials spanning a wide range of dielectric constants, from air ($k = 1$) to fluorinated oxides ($k = 3.6$) have been explored for interconnect systems [15].

The values of 4.0, 3.6 and 1 are used as the relative permittivity (k) of the dielectric for simulation. They are values of traditionally used silicon dioxide and novel low- k materials.

Corresponding comparisons of S_{11} and S_{21} of the single-line interconnect are given in Fig. 8.17 and Fig. 8.18. S_{11} is inversely proportional to the relative permittivity of the dielectric. It is due to the mismatch against the 50 Ω test system. From Fig. 8.18, it is observed that S_{21} is also inversely proportional to k , and is influenced by both the reflection and the loss. From Eq. (8.2.2), it is clear that the loss of the interconnect is proportional to the permittivity.

$$C = \varepsilon_0 \frac{kS}{d} \quad (8.2.2)$$

The increase of the permittivity leads to the increase of the parasitic capacitance. As a result, the loss increases. Since the loss dominates during the determination of S_{21} compared to the reflection, the behavior of S_{21} against the permittivity of the dielectric can be explained.

Figure 8.17: Single line: Comparison of S_{11} with respect to various dielectric permittivities

Figure 8.18: Single line: Comparison of S_{21} with respect to various dielectric permittivities

Comparisons of S_{11} to S_{41} of the coupled lines are given in Fig. 8.19 to Fig. 8.22, respectively. As shown in Fig. 8.19 and Fig. 8.20, both S_{11} and S_{21} are inversely proportional to the relative permittivity of the dielectric. It follows the same characteristics as the single-line interconnects in Fig. 8.17 and Fig. 8.18. From Fig. 8.22, it is observed that the interconnect structure with higher dielectric permittivity suffers more near-end coupling. As presented in Eq. (8.2.2), given the same physical dimension, the structure with larger dielectric permittivity has a larger coupling capacitance. With the same energy in the active line, the larger the coupling capacitance, the greater the coupling capacity is. Therefore, the near-end coupling is proportional to k .

The far-end coupling is affected by both of the coupling capacitance and the energy in the active line. Interconnects with larger dielectric permittivity have larger coupling capacitances, however, they have smaller transmitted energy at the far-end port (S_{21}). Affected by both of the factors, the far-end coupling, as shown in Fig. 8.21, is inversely proportional to the dielectric permittivity.

Figure 8.19: Coupled lines: Comparison of S_{11} with respect to various dielectric permittivities

Figure 8.20: Coupled lines: Comparison of S_{21} with respect to various dielectric permittivities

Figure 8.21: Coupled lines: Comparison of S_{31} with respect to various dielectric permittivities

Figure 8.22: Coupled lines: Comparison of S_{41} with respect to various dielectric permittivities

8.2.4 Conductivity of the Metallic Conductor

Due to its higher conductivity ($\sim 5.8 \times 10^7 S/m$), copper metallization has been introduced for aggressive interconnects instead of traditional Al ($\sim 2.7 \times 10^7 S/m$) or AlCu ($\sim 3.3 \times 10^7 S/m$) metallization [15].

S_{11} and S_{21} of the single-line interconnects are shown in Fig. 8.2.4 and Fig. 8.2.4. As predicted, the interconnect with higher conductivity has less loss and improved transmission capability.

Figure 8.23: Single line: Comparison of S_{11} with respect to various metallic conductor conductivities

Figure 8.24: Single line: Comparison of S_{21} with respect to various metallic conductor conductivities

The coupled lines S_{11} and S_{21} , as shown in Fig. 8.2.4 and Fig. 8.2.4, follow the same trend as the single-line interconnects. However, the transmission capacity (S_{21}) is slightly lesser compared to the single interconnects because of the energy coupling. Fig. 8.2.4 and Fig. 8.2.4 show that the interconnects with larger conductivity experience slightly more coupling than those with lower conductivities. A conductor with higher conductivity has larger currents and hence generates a larger induced magnetic field and more coupling. However, at high frequencies, the resistance is not dominant compared with the inductance. As shown in Fig. 8.2.4 and Fig. 8.2.4, the couplings are not strongly affected by the variation of the conductor's conductivities.

Figure 8.25: Coupled lines: Comparison of S_{11} with respect to various metallic conductor conductivities

Figure 8.26: Coupled lines: Comparison of S_{21} with respect to various metallic conductor conductivities

Figure 8.27: Coupled lines: Comparison of S_{31} with respect to various metallic conductor conductivities

Figure 8.28: Coupled lines: Comparison of S_{41} with respect to various metallic conductor conductivities

8.3 Summary

The sensitivities of on-wafer single-line interconnects and coupled interconnects of current and future Si CMOS technologies have been investigated based on a calibrated deck of a 0.18 μm RF CMOS process.

It is observed that both the reflection (S_{11}) and transmission (S_{21}) of the interconnect are influenced by the process parameters. S_{11} is proportional to the thickness of the dielectric while inversely proportional to the permittivity of the dielectric and the conductivity of the metallic conductor. As for S_{21} , it is proportional to the thickness of the dielectric and the conductivity of the metallic conductor while inversely proportional to the permittivity of the dielectric. The impact of the substrate conductivity on both S_{11} and S_{21} is more complicated. No monotonic relationship is observed.

By comparing the sensitivities of single-line interconnects, it is observed that S_{11} and S_{21} of the coupled interconnects follow similar characteristics when the process parameters (conductivity of the substrate, the permittivity of the dielectric, the thickness of the dielectric and the conductivity of the metallic conductor) vary. Both the far-end coupling (S_{31}) and the near-end coupling (S_{41}) are proportional to the conductivity of the conductors and the distance between the conductors and the substrate. It is highlighted that although further distance between the interconnects and the substrate can reduce substrate losses, more significant coupling occurs. This degrades the circuit performance. Hence, a trade-off must be decided. We also

discovered that S_{31} is inversely proportional to dielectric permittivity, whereas S_{41} is proportional to it. The impact of the substrate conductivity is more complicated. No monotonic relationship between S-parameters and the substrate conductivity is observed.

Chapter 9

Conclusions and Future Directions

9.1 Conclusions

Recent decades have been a prominent period in the development of microelectronics. Boosted by great demand from the wireless telecommunication market, RFICs are gaining more and more attention. Currently, due to its mature technology, low fabrication cost, high packing density and low power consumption, CMOS technology is acquiring growing popularity in RFIC design. At the same time, RFIC design faces a new challenge: The inductive effect, skin effect, distributed effect, substrate losses of on-wafer interconnects have been brought to our concerns. Circuit performance is getting increasingly dependent on interconnects. One of the limiting factors in the development of RFIC today is the absence of adequate interconnect models.

The focus of this thesis is on the characterization and modeling of on-wafer interconnects for CMOS RFICs.

The major contributions of the thesis are summarized as follows:

- Scalable equivalent circuit models have been proposed for complex-shaped interconnects. Frequency-variant high frequency effects are characterized with frequency independent components. Hence, the models are incorporated into conventional EDA tools. Model components are formulated into empirical expressions based on the length and width of the target interconnect. The proposed models are verified with on-wafer measurements. The accuracy is validated within a tolerance of 7% up to 20 GHz.
- Two optimization algorithms, namely HGA and PSO, have been studied and applied for the model parameter extraction. Performance comparisons suggest that the accuracy and the optimization speed of both algorithms are acceptable. Researchers can make their selection based on their own preferences.
- The proposed interconnect model has been employed in the design of a broadband 10 Gb/s transimpedance amplifier. Post-layout simulation using the proposed interconnect model and the foundry-provided model are compared with on-wafer measurements. The feasibility of using accurate interconnect model is demonstrated and the impacts of interconnect effects on the circuit performance are analyzed.
- The sensitivities of interconnects to CMOS process parameters have been in-

vestigated. It is also observed that the behaviors of both single-line interconnect and coupled interconnect are affected by the variation of process parameters, e.g., substrate conductivity, thickness of the dielectric, permittivity of the dielectric and conductivity of the metallic conductor.

9.2 Future Directions

Practical structures of on-wafer interconnects are too complicated to be discussed in this thesis. This dissertation only covers the single-lined interconnect. As the importance of interconnects continues to escalate, further studies on different interconnect configurations will be helpful. Here are some suggestions for future researches:

- Interconnect modeling using behavioral models
- Comparisons between equivalent circuit modeling and behavior modeling
- Characterization and modeling of vias
- Characterization and modeling of coupled interconnects
- Development of accurate layout parameter extraction tools

Author's Publications

Journals

1. X. Shi, K. S. Yeo, J.-G. Ma and M. A. Do, "Distortion of pulsed signals in carbon nanotube interconnects," *Microelectron. J.*, accepted in 2007.
2. X. Shi, K. S. Yeo, J.-G. Ma, M. A. Do and E. Li, "Sensitivity analysis of coupled interconnects for RFIC applications," *IEEE Trans. Electromagn. Compat.*, vol. 48, no. 4, pp. 607-613, Nov., 2006.
3. X. Shi, K. S. Yeo, J.-G. Ma, M. A. Do and E. Li, "Scalable model of on-wafer interconnects for high-speed CMOS ICs," *IEEE Trans. Adv. Packag.*, vol. 29, no. 4, pp. 770-776, Nov., 2006.
4. X. Shi, J.-G. Ma, K. S. Yeo, M. A. Do and E. Li, "Equivalent circuit model of on-wafer CMOS interconnects for RFICs," *IEEE Trans. VLSI Syst.*, vol. 13, no. 9, pp. 1060-1071, Sept., 2005.
5. X. Shi, J.-G. Ma, B. H. Ong, K. S. Yeo, M. A. Do and E. Li, "Equivalent circuit model of interconnect bends based on S-parameter measurements," *Microwave Opt. Technol. Lett.*, vol. 45, no. 2, pp. 170-173, Apr., 2005.

Conferences

1. X. Shi, J.-G. Ma, B. H. Ong, K. S. Yeo, M. A. Do and E. Li, "Equivalent circuit model of on-wafer interconnects for CMOS RFICs", *Proc. of IEEE*

- RAWCON*, pp. 95-98, Atlanta, GA, U.S.A., Sept., 2004.
2. X. Shi, Z. Lu, J.-G. Ma, E. Li, K. S. Yeo and M. A. Do, "Investigation of Interconnect Effects in A Transimpedance Amplifier", *Proc. of EMC-Zurich*, pp. 586-589, Singapore, Mar., 2006.
3. X. Shi, J.-G. Ma, E. Li, K. S. Yeo and M. A. Do, "Sensitivity of On-Wafer Interconnects to CMOS Process Parameters at Radio Frequency", *Proc. of EMC-Zurich*, pp. 590-594, Mar., Singapore, 2006.

Bibliography

- [1] J. D. Vriendt, P. Laine, C. Lerouge, and X. Xu, “Mobile network evolution: a revolution on the move,” *IEEE Commun. Mag.*, vol. 40, pp. 104–111, Aug. 2002.
- [2] J. uddenfeldt, “Digital cellular - its roots and its future,” *Proc. IEEE*, vol. 86, pp. 1319–1324, July 1998.
- [3] A. Matsuzawa, “RF-SoC-expectations and required conditions,” *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 245–253, Jan. 2002.
- [4] L. E. Larson, “Silicon technology tradeoffs for radio-frequency/mixed signal system-on-chip,” *IEEE Trans. Electron Devices*, vol. 50, pp. 683–699, Mar. 2003.
- [5] J. Zheng, V. K. Tripathi, and A. Weisshaar, “Characterization and modeling of multiple coupled on-chip interconnects on silicon substrate,” *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 1733–1739, Oct. 2001.

-
- [6] L. E. Larson, "Integrated circuit technology options for RFIC's - present status and future directions," *IEEE J. Solid-State Circuits*, vol. 33, pp. 387–399, Mar. 1998.
- [7] B. Razavi, "RF CMOS transceivers for cellular telephony," *IEEE Commun. Mag.*, vol. 41, pp. 124–128, Aug. 2003.
- [8] T. H. Lee and S. S. Wong, "CMOS RF integrated circuits at 5 GHz and beyond," *Proc. IEEE*, vol. 88, pp. 1560–1571, Oct. 2000.
- [9] R. Hossain, F. Viglione, and M. Cavalli, "Designing fast on-chip interconnects for deep submicrometer technologies," *IEEE Trans. VLSI Syst.*, vol. 11, pp. 276–280, Apr. 2003.
- [10] Q. Xu and P. Mazumder, "The fifth-order differential quadrature methods," *IEEE Trans. VLSI Syst.*, vol. 11, pp. 1068–1079, Dec. 2003.
- [11] J. a. Davis, R. Venkatesan, A. Kaloyeros, M. Beylansky, S. J. Souri, K. Banerjee, K. C. Saraswat, A. Rahman, R. Reif, and J. D. Meindl, "Interconnect limits on gigascale integration (GSI) in the 21st century," *Proc. IEEE*, vol. 89, pp. 305–324, Mar. 2001.
- [12] A. Weisshaar and A. Luoh, "Closed-form expressions for the series impedance parameters of on-chip interconnects on multilayer silicon substrates," *IEEE Trans. Adv. Packag.*, vol. 27, pp. 126–134, Feb. 2004.
- [13] D. D. Roest, H. Ymeri, S. vandenbergh, M. Stucchi, D. Schreurs, K. Maex, and B. Nauwelaers, "Some measurement results for frequency-dependent inductance

- of ic interconnects on a lossy silicon substrate,” *IEEE Trans. Adv. Packag.*, vol. 23, pp. 103–104, Feb. 2002.
- [14] A. E. Ruehli and A. C. Cangellaris, “Progress in the methodologies for the electrical modeling of interconnects and electronic packages,” *Proc. IEEE*, vol. 89, pp. 740–771, May 2001.
- [15] R. H. Havemann and J. A. Hutchby, “High-performance interconnects: an integration overview,” *Proc. IEEE*, vol. 89, pp. 586–601, May 2001.
- [16] R. Achar and N. M. S, “Simulation of high-speed interconnects,” *Proc. IEEE*, vol. 89, pp. 693–728, May 2001.
- [17] F. Caignet, S. Delmas-Bendhia, and E. Sicard, “The thallenge of signal integrity in deep-submicrometer CMOS technology,” *Proc. IEEE*, vol. 89, pp. 556–573, Apr. 2001.
- [18] T. C. Edwards and M. B. Steer, *Foundations of Interconnect and Microstrip Design*. Chicester. New York. Brisbane. Toronto. Singapore: John Wiley & Sons Inc., 3rd ed., 2000.
- [19] D. Sylvester and C. Hu, “Analytical modeling and characterization of deep-submicrometer interconnect,” *Proc. IEEE*, vol. 89, pp. 634 – 664, May 2001.
- [20] W. Sun, W.-M. Dai, and W. Hong, “Fast parameter extraction of general interconnects using geometry independent measured equation of invariance,” *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 827–836, May 1997.

- [21] F. Sischka, *IC-CAP characterization and modeling handbook*. PhD thesis, Agilent Technologies, 2000.
- [22] M. A. Azadpour and T. S. Kalkur, “Interconnect model at multi-ghz frequencies incorporating inductance effect,” in *Proc. of ICSE*, pp. 82–86, 2002.
- [23] Y. Zheng, *High-frequency on-chip interconnect characterization and measurement*. PhD thesis, Columbia University, 2003.
- [24] B. Kleveland, X. Qi, L. Madden, T. Furusawa, R. W. Dutton, M. A. Horowitz, and S. S. Wong, “High-frequency characterization of on-chip digital interconnects,” *IEEE J. Solid-State Circuits*, vol. 37, pp. 716–725, June 2002.
- [25] N. D. Arora, “Modeling and characterization of copper interconnects for soc design,” in *Proc. of IEEE SISPAD 2003*, pp. 1–6, Sept. 2003.
- [26] R. Achar and N. M. S, “EPEEC: comprehensive SPICE-compatible reluctance extraction for high-speed interconnects above lossy multilayer substrates,” *IEEE Trans. Computer-Aided Design*, vol. 24, pp. 693–728, Oct. 2005.
- [27] I. M. Elfadel, A. Deutsch, G. V. Kopcsay, J. B. Rubin, and H. H. Smith, “A CAD methodology and tool for the characterization of wide on-chip buses,” vol. 28, pp. 63–70, July 2005.
- [28] A. Deutsch, H. H. Smith, C. W. Surovic, G. V. Kopcsay, D. A. Webber, P. W. Coteus, G. A. Katopis, W. D. Becker, A. H. Dansky, G. A. Sai-Halasz, and P. J. Restle, “Frequency-dependent crosstalk simulation for on-chip interconnections,” *IEEE Trans. Adv. Packag.*, vol. 22, pp. 292 – 308, Aug. 1999.

- [29] P. J. Restle, A. E. Riehli, S. G. Walker, and G. Papadopoulos, "Full-wave PEEC time-domain method for the modeling of on-chip interconnects," *IEEE Trans. Computer-Aided Design*, vol. 20, pp. 877–886, July 2001.
- [30] A. Naeemi, J. A. Davis, and J. D. Meindl, "Analysis and optimization of coplanar RLC lines for GSI global interconnection," *IEEE Trans. Electron Devices*, vol. 51, pp. 985–994, June 2004.
- [31] K. M. Coperich, A. E. Ruehli, and A. Cangellaris, "Enhanced skin effect for partial-element equivalent-circuit (PEEC) models," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 1435–1442, Sept. 2000.
- [32] A. Orlandi and C. R. Paul, "An efficient characterization of interconnected multiconductor-transmission-line networks," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 466–470, Mar. 2000.
- [33] J. D. Morsey, V. I. Okhmatovski, and A. C. Cangellaris, "Finite-thickness conductor models for full-wave analysis of interconnects with a fast integral equation method," vol. 27, pp. 24–33, Feb. 2004.
- [34] Q. Xu and P. Mazumder, "Equivalent-circuit interconnect modeling based on the fifth-order differential quadrature methods," *IEEE Trans. VLSI Syst.*, vol. 11, pp. 1068–1079, Dec. 2003.
- [35] Q. Xu and P. Mazumder, "Accurate analysis of interconnect trees with distributed RLC model and moment matching," *IEEE Trans. Microwave Theory Tech.*, vol. 52, pp. 2199–2206, Sept. 2004.

- [36] K. Banerjee and A. Mehrotra, "Analysis of on-chip inductance effects for distributed RLC interconnects," *IEEE Trans. Computer-Aided Design*, vol. 21, pp. 904–915, Aug. 2002.
- [37] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Figures of merit to characterize the importance of on-chip inductance," *IEEE Trans. VLSI Syst.*, vol. 7, pp. 442–449, Dec. 1999.
- [38] K. Gala, D. Blaauw, V. Z. adn P. M. Vaidya, and A. Joshi, "Inductance model and analysis methodology for high-speed on-chip interconnect," *IEEE Trans. VLSI Syst.*, vol. 10, pp. 730–745, Dec. 2002.
- [39] Y. Eo, W. R. Eisenstadt, and J. Shim, "S-parameter-measurement-based high-speed signal transient characterization of VLSI interconnects on $\text{SiO}_2\text{-Si}$ substrate," *IEEE Trans. Adv. Packag.*, vol. 23, pp. 470–479, Aug. 2000.
- [40] D. A. White and M. Stowell, "Full-wave simulation of electromagnetic coupling effects in RF and mixed-signal ics using a time-domain finite-element method," *IEEE Trans. Microwave Theory Tech.*, vol. 52, pp. 1404 – 1413, May 2004.
- [41] X. Shi, J. Ma, B. H. Ong, K. S. Yeo, M. A. Do, and E. Li, "Equivalent circuit model of on-wafer interconnects for CMOS RFICs," in *Proc. of IEEE RAWCON*, (Atlanta,GA), pp. 95–98, Sept. 2004.
- [42] S. Lee, J. Choi, G. S. May, and I. Yun, "Modeling and analysis of 3-D solenoid embedded inductors," *IEEE Trans. Electron. Packag. Manufact.*, vol. 25, pp. 34–41, Jan. 2002.

-
- [43] E.-P. Li, E.-X. Liu, L.-W. Li, and M.-S. Leong, "A coupled efficient and systematic full-wave time-domain macromodeling and circuit simulation method for signal integrity analysis of high-speed interconnects," *IEEE Trans. Adv. Packag.*, vol. 27, pp. 213 – 223, Feb. 2004.
 - [44] L. M. Elfadel, A. deutsch, H. H. S. adn B. J. Rubin, and G. V. Kopcsay, "A multiconductor transmission line methodology for global on-chip interconnect modeling and analysis," *IEEE Trans. Adv. Packag.*, vol. 27, pp. 71–78, Feb. 2004.
 - [45] A. Deutsch, P. W. Coteus, G. V. Kopcsay, H. H. Smith, C. W. Surovic, B. L. Krauter, D. C. Edelstein, and P. L. Restle, "On-chip wiring design challenges for gigahertz operation," *Proc. IEEE*, vol. 89, no. 4, pp. 529–555, Apr. 2001.
 - [46] C. Plett and J. Rogers, *Radio frequency integrated circuit design*. Artech House, 2003.
 - [47] D. K. Cheng, *Fundamentals of Engineering Electromagnetics*. Addison-Wesley Publishing Company, Inc., 1993.
 - [48] J. Zheng, Y. Hahm, V. K. Tripathi, and A. Weisshaar, "CAD-oriented equivalent circuit modeling of on-chip interconnects on lossy silicon substrate," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 1443–1451, Sept. 2000.
 - [49] E. Chiprout, "Interconnect and substrate modeling and analysis: an overview," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1445 – 1452, Sept. 1998.

- [50] H. Braunisch and H. Grabinski, "Time-domain simulation of large lossy interconnect systems on conducting substrates," *IEEE Trans. Circuits Syst.*, vol. 45, pp. 909–918, Sept. 1998.
- [51] D. M. Pozar, *Microwave Engineering*, p. 221. Chicester . New York . Brisbane . Toronto . Singapore: John Wiley & Sons Inc., 1998.
- [52] M. A. Azadpour and T. S. Kalkur, "A clock interconnect extractor for multigigahertz frequencies incorporating inductance effect," *IEEE Trans. VLSI Syst.*, vol. 11, pp. 1143–1146, Dec. 2003.
- [53] S. Shin, Y. Eo, W. R. Eisenstadt, and J. Shim, "Analytical models and algorithms for the efficient signal integrity verification of inductance-effect-prominent multicoupled," *IEEE Trans. VLSI Syst.*, vol. 12, pp. 395–407, Apr. 2004.
- [54] A. Deutsch, P. W. Coteus, G. V. Kopcsay, H. H. Smith, C. W. Surovic, B. L. Krauter, D. C. Edelstein, and P. J. Restle, "On-chip wiring design challenges for gigahertz operation," *Proc. IEEE*, vol. 89, pp. 529–555, Apr. 2001.
- [55] K. M. C. Branch, J. Morsey, A. C. Cangellaris, and A. E. Ruehli, "Physically consistent transmission line models for high-speed interconnects in lossy dielectrics," vol. 25, pp. 129–235, May 2002.
- [56] X. Huang, P. Restle, t. Bucelot, Y. Cao, T.-J. King, and C. Hu, "Loop-based interconnect modeling and optimization approach for multigigahertz clock net-

- work design,” *IEEE Trans. Syst. Sci. Cybernetics*, vol. 38, pp. 457–464, Mar. 2003.
- [57] W. R. Eisenstadt and Y. Eo, “S-parameter-based IC interconnect transmission line characterization,” *IEEE Trans. Comp., Hybrids, Manufact. Technol.*, vol. 15, pp. 483 – 490, Aug. 1992.
- [58] P. Wang and E. C.-C. Kan, “High-speed interconnects with underlayer orthogonal metal grids,” vol. 27, pp. 497–507, Aug. 2004.
- [59] G. Wang, X. Qi, and Z. Yu, “Device level modeling of metal-insulator-semiconductor interconnects,” *IEEE Trans. Electron Devices*, vol. 48, pp. 1672–1682, Aug. 2001.
- [60] Y. Eo and W. R. Eisenstadt, “High-speed VLSI interconnect modeling based on S-parameter measurements,” *IEEE Trans. Comp., Hybrids, Manufact. Technol.*, vol. 16, pp. 555–562, Aug. 1993.
- [61] G. Wang, X. Qi, and Z. Yu, “Device level modeling of metal-insulator-semiconductor interconnects,” *IEEE Trans. Electron Devices*, vol. 48, pp. 1672–1682, Aug. 2001.
- [62] E. Chiprout, “Hierarchical interconnect modeling,” in *1997 IEEE IEDM*, pp. 125–128, Dec. 1997.
- [63] S. You and E. F. Kuester, “Fast and efficient interconnect modelling using finite element method and model order reduction,” in *2004 IEEE MTT-S International*, vol. 3, pp. 1377–1380, June 2004.

- [64] S. You and E. F. Kuester, "Guaranteed passive direct lumped-element modeling of transmission lines," *IEEE Trans. Microwave Theory Tech.*, vol. 53, pp. 2826–2834, Sept. 2005.
- [65] J. N. Reddy, *Introduction to the Finite Element Method*. McGraw-Hill Science/Engineering/Math, 1993.
- [66] A. Scuderi, T. Biondi, E. Ragonese, and G. Palmisano, "A lumped scalable model for silicon integrated spiral inductors," *IEEE Trans. Circuits Syst. I*, vol. 52, pp. 318–323, Feb. 2005.
- [67] C. P. Yue and S. S. Wong, "Physical modeling of spiral inductors on silicon," *IEEE Trans. Electron Devices*, vol. 47, pp. 560–568, Mar. 2000.
- [68] J. Sieiro, J. M. Lopez-Villeas, J. Cabanillas, J. A. Osorio, and J. Samitier, "A physical frequency-dependent compact model for RF integrated inductors," *IEEE Trans. Microwave Theory Tech.*, vol. 50, pp. 384–392, Jan. 2002.
- [69] J. R. Long and M. A. Copeland, "The modeling, characterization, and design of monolithic inductors for silicon RF IC's," *IEEE Trans. Syst. Sci. Cybernetics*, vol. 32, pp. 357–369, Mar. 1997.
- [70] I. Timmins and K.-L. Wu, "Full-wave modeling and automatic equivalent-circuit generation of millimeter-wave planar and multilayer structures," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 1565–1573, Sept. 2000.

-
- [71] T. Mangold and P. Russer, "An efficient systematic approach to model extraction for passive microwave circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 851–858, June 1999.
- [72] W. M. Spears, K. A. D. Jong, T. Back, D. B. Fogel, and H. Garis, "An overview of evolutionary computation," in *Proc. of European Conf. Machine Learning (ECML-93)*, vol. 667, pp. 442–459, 1993.
- [73] D. E. Goldberg, *Genetic Algorithms In Search Optimization And Machine Learning*. Adison-Wesley, 1989.
- [74] J. K. Koza, *Genetic Programming: On the Programming of Computers by Means of Natural Selection*. MIT press, 1992.
- [75] H.-G. Beyer, *Theory of Evolution Strategies*. Springer, 2001.
- [76] R. Eberhart and Y. Shi, "Tracking and optiimizing dynamic systems with particle swarms," in *Proc. IEEE Int. Conf. on Evolutionary Computation*, pp. 94–100, 2000.
- [77] R. L. Haupt and S. E. Haupt, *Practical Genetic Algorithms*. John Wiley & Sons Inc., 1998.
- [78] J. Kennedy and R. Eberhart, "Particle swarm optimization," in *Proc. of IEEE Inter. Conf. on Neural Networks*, vol. IV, (Perth, Australia), pp. 1942–1948, 1995.

-
- [79] D. W. Boeringer and D. H. Werner, "Particle swarm optimization versus genetic algorithms for phased array synthesis," *IEEE Trans. Antennas Propagat.*, vol. 52, pp. 771–779, Mar. 2004.
 - [80] B. Kleveland, *CMOS interconnects beyond 10 GHz*. PhD thesis, Stanford University, Aug. 2000.
 - [81] C. S. M. LTD, *0.18 μm CMOS digital/analog/RF technology topological and reliability design rules*. 2001.
 - [82] P. J. V. Winjnen, H. R. Claessen, and E. A. Wolsheimer, "A New straightforward calibration and correction procedure for on-wafer high frequency S-parameter measurements (45 MHz - 18 GHz)," in *Proc. of IEEE BCTM, 1987, Bipolar Circuits and Technology Meeting*, pp. 70–73, 1987.
 - [83] M. J. Deen and T. A. Fjeldly, *CMOS RF modeling, characterization and applications*. New Jersey: World Scientific, 2002.
 - [84] T. Kurbara, M. Yamaguchi, and K.-I. Arai, "Equivalent circuit analysis of an RF integrated ferromagnetic inductor," *IEEE Trans. Magn.*, vol. 38, pp. 3159–3161, Sept. 2002.
 - [85] C.-J. Chao, S.-C. Wong, C.-H. Kao, M.-J. Chen, and L.-Y. Leu, "Characterization and modeling of on-chip spiral inductors for Si RFICs," *IEEE Trans. Semiconduct. Manufact.*, vol. 15, pp. 19–29, Feb. 2002.
 - [86] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS: Circuit Design, Layout and Simulation*. The Institute of Electrical and Electronics Engineers, Inc., 1997.

-
- [87] X. Qi, *High frequency characterization and modeling of on-chip interconnects and RFIC wire bonds*. PhD thesis, Stanford University, June 2001.
- [88] A. Tzanakaki, I. Zacharopoulos, and I. Tomkos, "Broadband building blocks," *IEEE Circuits Devices Mag.*, vol. 20, pp. 32–37, Mar. 2004.
- [89] A. Tzanakaki, I. Zacharopoulos, and I. Tomkos, "Broadband building blocks," *IEEE Circuits Devices Mag.*, vol. 20, no. 2, pp. 32–37, 2004.
- [90] D. Cavendish, "Evolution of optical transport technologies: from SONET/SDH to WDM," *IEEE Commun. Mag.*, vol. 38, pp. 164–172, June 2000.
- [91] X. Shi, J.-G. Ma, K. S. Yeo, M. A. Do, and E. Li, "Equivalent circuit model of on-wafer CMOS interconnects for RFICs," *IEEE Trans. VLSI Syst.*, vol. 13, pp. 1060–1071, Sept. 2005.
- [92] M. J. Deen and C.-H. Chen, "The impact of noise parameter de-embedding on the high-frequency noise modeling of MOSFETs," in *Proc. IEEE 1999 Int. Conf. Microelectronic Test Structures*, vol. 12, pp. 34–39, Mar. 1999.
- [93] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. John Wiley & Sons Inc., 1997.
- [94] B. Razavi, *Design of Integrated Circuits for Optical Communications*. McGraw-Hill, 2002.

- [95] M. S. Park and R. A. Minasian, "Ultra-low noise and wideband-tuned optical receiver synthesis and design," *J. Lightwave Technol.*, vol. 12, pp. 254–259, Feb. 1994.
- [96] X. Shi, J. Ma, B. H. Ong, K. S. Yeo, M. A. Do, and E. Li, "Equivalent circuit model of interconnect bends based on S-parameter measurements," in *Microwave Opt. Technol. Lett.*, vol. 45, pp. 170–173, Apr. 2005.
- [97] B. Kleveland, C. H. Diaz, L. Madden, T. H. Lee, and S. S. Wong, "Exploiting CMOS reverse interconnect scaling in multigigahertz amplifier and oscillator design," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1480–1489, Oct. 2001.
- [98] Y. Eo, W. R. Eisenstadt, J. Y. Jeong, and O.-K. Kwon, "A new on-chip interconnect crosstalk model and experimental verification for CMOS VLSI circuit design," *IEEE Trans. Electron Devices*, vol. 47, pp. 129–142, Jan. 2000.
- [99] B. Kleveland, T. H. Lee, and S. S. Wong, "50-GHz interconnect design in standard silicon technology," in *1998 IEEE MTT-S International, Microwave Symposium Digest*, vol. 3, pp. 1913–1916, 1998.