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SPACE VECTOR BASED HYSTERESIS CURRENT CONTROL (HCC) STRATEGIES FOR MATRIX CONVERTER

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2006

**Space Vector Based Hysteresis Current Control (HCC)
Strategies for Matrix Converter**

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Master of Engineering

2006

Statement of originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for higher degree to any other university or institution.

Date

Wang Xiao

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Summary

In many ac drive applications, it is desirable to use a compact voltage source converter to provide sinusoidal output voltage and current with varying amplitude and frequency, while drawing sinusoidal input current from the ac source, and having high regulation bandwidth, and efficiency. The matrix converter is a self-commutated direct converter and enables the conversion of a constant three-phase system into a three-phase system with variable voltage and frequency. Through the arrangement of the bidirectional power switches in a three-times-three switch matrix, each of the three output phases of the matrix converter can be electrically connected to any one input phase. The matrix converter does not require an intermediate circuit in contrast to traditional AC-DC-AC converter with bulk DC-link capacitor to store energy. Due to its topology, the matrix converter has energy recovery capability and achieves sinusoidal input currents through a suitably designed controller. The matrix converter thus offers an all-silicon solution which has the merit of compact design in contrast to traditional converter.

The most general modulation method for matrix converter, is the indirect modulation, which decouples the control of the input current and the output voltage and regards the matrix converter as a back-to-back PWM converter without DC-link energy storage. This means that the well-known Space Vector Modulation (SVM) can be applied to the rectifying stage and inverting stage, independently. The SVM method can help to reduce the duty cycle calculation complexity of the matrix converter. With the concept of space vector modulation, the matrix converter received considerable attention in these recent years.

Compared with Space Vector Modulation methods for power converter, the hysteresis

current control (HCC) offers the advantages of very simple structure, quick response, maximum current limit and insensitivity to load parameter variations. So the hysteresis current control (HCC) has been frequently used in traditional voltage source inverter (VSI) because it is simple to implement and provides a good current amplitude control. In this thesis, two kinds of novel but simple space vector based hysteresis current control strategies for matrix converter are proposed. One is based on three-level hysteresis comparator and the other is based on four-level hysteresis comparator. Both comparators select appropriate space vector combinations via switching table including zero vector combination to reduce the switching frequency in matrix converter, and they do not require complex calculations. Both regulators work with current components represented in $\alpha - \beta$ stationary coordinate system, and need only two multi-level comparators to achieve space vector selection. So these kinds of controllers can help to further simplify the complexity of the overall control circuit.

The implementation and verification of both the SVM control system and the proposed HCC control systems for matrix converter are done in Matlab/Simulink simulation environment. Both of the proposed HCC control systems are simulated with the same input and output parameters as the SVM system, in order to make comparison with the SVM system. Simulation results show that HCC system can generate the desired sinusoidal output current and obtain sinusoidal input current at the input side like the SVM system. The four-level HCC system can accurately determine the voltage vector, and the switching frequency is reduced compared to that of the three-level system. Results also demonstrate that HCC systems offer faster dynamic behavior than SVM system.

The performance of space vector modulation (SVM) technique and hysteresis current control (HCC) technique for matrix converter under abnormal input voltage conditions were investigated and compared. The SVM and HCC techniques are based on different modulation principle, and the HCC technique do not need to calculate duty cycle for the fictitious inverting part. So under abnormal input voltage conditions, the HCC technique has the inherent ability of preventing the disturbance at the grid side from propagating to the output side, and thereby obtaining better output characteristics than SVM technique. Simulation results have shown that the hysteresis current control strategy

has produced improved output characteristics under abnormal input voltage conditions. For SVM system, when abnormal input voltages occurred at the input side, the output characteristics are affected. Under unbalanced input voltage condition, the output currents of SVM system contain harmonic components at frequency of $(2f_i \pm f_o)$. Under non-sinusoidal input voltage condition, the output currents of SVM system contain harmonic components at frequency of $(k - 1)\omega_i \pm \omega_o$ and $(k + 1)\omega_i \pm \omega_o$ (note: f_i is the input frequency, f_o is the output frequency, ω_i is the input angular frequency, ω_o is the output angular frequency and k is the harmonic order). Under input voltage sag, the output current of SVM system shows a significant drop in magnitude. But for HCC system, although the magnitude of generated inverting switching vectors is varying under abnormal input voltage conditions, yet if the smallest output voltage vectors V'_n is still large enough to make the output current tracks its reference, the output current waveform will not be influenced by abnormal input voltages. Simulation results proved that under all these three kinds of abnormal input voltage conditions, the HCC system can still produce very sinusoidal output currents without significant harmonic components at frequencies of $(2f_i \pm f_o)$, $(k - 1)\omega_i \pm \omega_o$ and $(k + 1)\omega_i \pm \omega_o$.

KEY WORDS: Matrix Converter, AC/AC Converter, Space Vector Modulation (SVM), Hysteresis Current Control (HCC), Induction Motor Drive.

Table of Contents

Acknowledgements	i
Summary	ii
List of Figures	ix
List of Tables	xiv
1 Introduction	1
1.1 Background and Motivation	1
1.2 Objectives	2
1.3 Contributions	4
1.4 Thesis Outline	4
2 Matrix Converter Topology	6
2.1 Introduction	6
2.2 Matrix Converter Circuit	7
2.3 Analysis of Bidirectional Switch Topologies	9
2.4 Bidirectional Switch Commutation Techniques	11

2.4.1	Current Direction Four-step Commutation Strategy	14
2.4.2	Two-Step Commutation Strategy	17
2.4.3	Current Direction Detection Methods	18
2.5	Peripheral Circuit for Matrix Converter	19
2.5.1	The input filter	19
2.5.2	The clamp circuit	20
2.5.3	The Power-Up Circuit	24
2.6	Concluding Remarks	26
3	Modulation Techniques for Matrix Converter	28
3.1	Introduction	28
3.2	Matrix Converter Control Principles	29
3.3	Venturini Modulation (Scalar Modulation) Method	35
3.4	Space Vector Modulation Method	36
3.4.1	VSI Output Voltage SVM	38
3.4.2	VSR Input Current SVM	41
3.4.3	Entire Matrix Converter Modulation	42
3.5	Optimized Space Vector Modulation	46
3.6	Concluding Remarks	48
4	Hysteresis Current Control Strategies for Matrix Converter	50
4.1	Introduction	50
4.2	The Basic Hysteresis Current Controller	51

4.3	Mathematical Model for Current Controllers in The Complex Plane . . .	53
4.4	Hysteresis Current Controller Working in $\alpha - \beta$ Stationary Coordinate .	56
4.5	Improved HCC Controller Working in $\alpha - \beta$ Stationary Coordinate . . .	61
4.6	Concluding Remarks	64
5	Modeling of SVM and HCC Control Systems for Matrix Converter	66
5.1	Introduction	66
5.2	Simulation Model of SVM System	67
5.2.1	Results Obtained	69
5.3	Simulation Model of HCC systems	74
5.3.1	Results Obtained From Three-Level HCC System	74
5.3.2	Results Obtained From Four-Level HCC System	78
5.4	Results of Dynamic Behavior of SVM System and HCC System	84
5.5	Concluding Remarks	86
6	Comparison of SVM and HCC Control Strategies for Matrix Converter under Abnormal Input Voltage Conditions	88
6.1	Introduction	88
6.2	Analysis of Matrix Converter under Abnormal Input Voltage Conditions	89
6.2.1	Unbalanced Input Voltages	91
6.2.2	Non-Sinusoidal Input Voltages	94
6.2.3	Input Voltage Sag	95
6.3	Analysis of SVM and HCC Systems under Abnormal Input Voltage Con- ditions	97

6.3.1	Output Characteristics of SVM System under Abnormal Input Conditions	97
6.3.2	Output Characteristics of HCC System under Abnormal Input Conditions	98
6.4	Simulation Results	101
6.4.1	Simulation under Unbalanced Input Voltages	101
6.4.2	Simulation under Non-Sinusoidal Input Voltages	103
6.4.3	Simulation under Input Voltage Sag	104
6.5	Concluding Remarks	105
7	Conclusions and Recommendations	107
7.1	Conclusions	107
7.2	Recommendations	110
	Author's Publications	112
	Bibliography	113
	Appendix	119
A	C Program for Matrix Converter Matlab Model	120

List of Figures

2.1	Circuit of traditional AC-DC-AC converter	7
2.2	Basic topology of matrix converter	8
2.3	Symbolic representation of matrix converter	9
2.4	Bidirectional switch topologies using unidirectional switches: (a) diode-embedded switch; (b) RB-IGBT switch; (c) common-emitter switch (CE); (b) common-collector switch (CC)	11
2.5	Commutation of the output phase <i>out</i> from input phase <i>x</i> to input phase <i>y</i> : (a) principle diagram; (b) ideal commutation; (c) dead-time commutation; (d) overlap commutation	12
2.6	Four-step commutation scheme depending on the current direction	15
2.7	Illustration of current path allowed during the four-step commutation . .	16
2.8	Two-step current commutation timing diagram	17
2.9	Two-step current commutation state changing diagram	17
2.10	The current direction detection method based on the voltage drop [1] . .	18
2.11	The clamp circuit	21
2.12	Discharging of the induction machine inductances to the clamp capacitor during a fault situation. (a) Equivalent model of converter and induction motor. (b) Currents in induction motor	22

2.13	Power-up circuit for matrix converter using series damping resistors . . .	25
2.14	Power-up circuit for matrix converter using parallel damping resistors . .	26
3.1	Simplified matrix converter circuit	30
3.2	Equivalent VSR-VSI circuit of matrix converter	37
3.3	Output voltage vectors in SVM hexagon	39
3.4	Output line voltage 60° segments	40
3.5	Input current vectors in SVM hexagon	41
3.6	5-step switching time diagram	46
3.7	9-step switching time diagram	46
4.1	The basic hysteresis current controller diagram	52
4.2	Waveforms associated to the basic hysteresis current controller diagram .	52
4.3	Voltage vector selection	55
4.4	The SVM based matrix converter hysteresis current control system . . .	57
4.5	Three level hysteresis comparator	58
4.6	VSI output voltage vector position and current error band	59
4.7	Improved VSI voltage vector position and current error band	62
4.8	Four-level hysteresis comparator	63
5.1	Matrix converter SVM control diagram	68
5.2	Three phase balanced input voltage	68
5.3	Three phase output current of SVM system under 25Hz output condition	70
5.4	FFT of output current of SVM system under 25Hz output condition . . .	70

5.5	Output line voltage of SVM system under 25Hz output condition	70
5.6	FFT of output line voltage of SVM system under 25Hz output condition	71
5.7	Three phase input current of SVM system under 25Hz output condition .	71
5.8	FFT of input current of SVM system under 25Hz output condition . . .	71
5.9	Three phase output current of SVM system under 80Hz output condition	72
5.10	FFT of output current of SVM system under 80Hz output condition . . .	72
5.11	Output line voltage of SVM system under 80Hz output condition	72
5.12	FFT of output line voltage of SVM system under 80Hz output condition	73
5.13	Three phase input current of SVM system under 80Hz output condition .	73
5.14	FFT of input current of SVM system under 80Hz output condition . . .	73
5.15	Three phase output current of three-level HCC system	75
5.16	FFT of output current of three-level HCC system	75
5.17	Output line voltage of three-level HCC system	75
5.18	FFT of output line voltage of three-level HCC system	76
5.19	Current waveform of i_α and i_α reference of three-level HCC system . . .	76
5.20	Current waveform of i_β and i_β reference of three-level HCC system . . .	76
5.21	Error area of three-level HCC system in stationary coordinates	77
5.22	Obtained inverting stage voltage vector of three-level HCC system	77
5.23	Three phase input current of three-level HCC system	77
5.24	FFT of input current of three-level HCC system	78
5.25	Three phase output current of four-level HCC system	79
5.26	FFT of output current of four-level HCC system	80

5.27	Output line voltage of four-level HCC system	80
5.28	FFT of output line voltage of four-level HCC system	80
5.29	Current waveform of i_α and i_α reference of four-level HCC system	81
5.30	Current waveform of i_β and i_β reference of four-level HCC system	81
5.31	Error area of four-level HCC system in stationary coordinates	81
5.32	Obtained inverting stage voltage vector of four-level HCC system	82
5.33	Three phase input current of four-level HCC system	82
5.34	FFT of input current of four-level HCC system	82
5.35	Number of switchings in period of 0.16s for three-level HCC system . . .	83
5.36	Number of switchings in period of 0.16s for four-level HCC system	83
5.37	Output current dynamic behavior of SVM system	85
5.38	Output current dynamic behavior of three-level HCC system	85
5.39	Output current dynamic behavior of four-level HCC system	85
6.1	Three phase unbalanced input voltages	92
6.2	The fictitious DC-link voltage under unbalanced input condition	92
6.3	Three phase non-sinusoidal input voltages	95
6.4	The fictitious DC-link voltage under non-sinusoidal input condition . . .	95
6.5	Three phase input voltage under voltage sag condition	96
6.6	The fictitious DC-link voltage under voltage sag input condition	96
6.7	Output voltage hexagon	99
6.8	Output voltage hexagonal diagram under abnormal input voltage condition	100
6.9	Output current of SVM system under balanced input voltage condition .	102

6.10 FFT of output current of SVM system under balanced input voltage condition	102
6.11 Output current of HCC system under balanced input voltage condition .	102
6.12 FFT of output current of HCC system under balanced input voltage condition	102
6.13 Output current of SVM system under unbalanced input voltage condition	103
6.14 FFT of output current of SVM system under unbalanced input voltage condition	103
6.15 Output current of HCC system under unbalanced input voltage condition	103
6.16 FFT of output current of HCC system under unbalanced input voltage condition	103
6.17 Output current of SVM system under non-sinusoidal input voltage condition	104
6.18 FFT of output current of SVM system under non-sinusoidal input voltage condition	104
6.19 Output current of HCC system under non-sinusoidal input voltage condition	104
6.20 FFT of output current of HCC system under non-sinusoidal input voltage condition	104
6.21 Output current of SVM system under input voltage sag condition	105
6.22 Output current of HCC system under input voltage sag condition	105

List of Tables

3.1	Matrix converter switching combinations ($K=2/\sqrt{3}$)	31
3.2	Switching sequence example	45
3.3	Standard double-sided vector sequence	47
3.4	Non-optimized standard double-sided vector sequence	47
3.5	Optimized double-sided vector sequence	47
4.1	Switching logic for three-level hysteresis controller	59
4.2	Matrix converter switching sequence example in the case of $v_{pn} = v_{ab}$. .	61
4.3	Switching logic for four-level hysteresis controller	63
5.1	Simulation results of matrix converter SVM system under different output conditions	69
5.2	Comparison of three kinds of controller at 50Hz input and 25Hz output .	79
5.3	Summary of distinctions between Three-level HCC and Four-level HCC .	87
6.1	Switch states and generated vectors for inverting stage	100

Chapter 1

Introduction

1.1 Background and Motivation

During the last 20 years, the matrix converter has been investigated as an alternative AC/AC converter topology. The matrix converter consists of a matrix of bidirectional switches linking two independent poly-phase systems. Each output line is linked to an input line via a bi-directional switch. The matrix converter, which is a direct AC/AC converter, features some advantages over the commonly used AC-DC-AC converters. The most important advantages are the lack of DC-link capacitor, the ability of four-quadrant operation and high power factor input current. The main disadvantages are the inherent restriction of the voltage transfer ratio to less than 0.866, and the high number of semiconductor devices needed to realize the matrix converter, as bidirectional power switches are not yet available.

Due to the high number of semiconductors, the control of the matrix converter becomes quite complicated. The first generation control method for matrix converter was first reported by Venturini [2] in terms of direct modulation using a complicated scalar model. Subsequently the indirect modulation concept for matrix converter based on space vector modulation was fully reported by Huber [3]. With the concept of indirect modulation, the matrix converter received considerable attention in these recent years. Compared

with direct modulation method, the indirect modulation method simplified the modulating model by making it possible to implement classical PWM modulation strategies in matrix converters.

Use of space vector modulation (SVM) simplified the modulator model, making it easier to control the converter or to implement high-performance control of the induction motors. The SVM method uses a combination of two adjacent vectors and a zero vector to produce the reference vector. The proportion between the two adjacent vectors gives the direction and the zero vector duty cycle determines the magnitude of the reference vector. The input current vector corresponding to the rectification stage and the output voltage vector corresponding to the inversion stage are the reference vectors.

The current control technique is another kind of control method for power converter. Comparing with other control methods, the hysteresis current controller offers very simple structure, quick response, maximum current limit and insensitivity to load parameter variations. A space vector modulation based hysteresis current controller (SVM-HCC) for matrix converter was proposed by Youm and Kwon [4]. This kind of controller was based on six two-level current hysteresis comparators which control three output legs independently and can suppress the high harmonic current components in steady state. It gives quick current response in transient state, and also utilizes zero switching combination to reduce the switching frequency. However, this method is still fairly complex. It utilizes six current hysteresis comparators to detect the current error of the position of the output space vector. It is proposed in this thesis that this scheme can be further simplified by just using two multi-level hysteresis comparators.

1.2 Objectives

The objectives of this research project are:

- Study of the matrix converter topology and the indirect modulation structure based on space vector modulation. This includes studies of matrix converter bidi-

rectional switch configuration, bidirectional switch commutation techniques, analysis of matrix converter input-output transfer function, derivation of equations for input-output duty cycle calculation, and combining the calculated duty cycle to generate the desired switching sequence for entire matrix converter.

- Study of hysteresis current control technology, and its application to modulate the matrix converter. Proposal of two novel but simple space vector based hysteresis current control strategies for matrix converter. One is based on three-level hysteresis comparator and the other is based on four-level hysteresis comparator. Both comparators select appropriate space vector combinations via switching table including zero vector combination to reduce the switching frequency and do not require complex calculations. Also, because both regulators work with the current components represented in stationary coordinate system, only two multi-level comparators will be needed to achieve space vector selection.
- Implementation of models of the indirect modulation structure based space vector modulation, and of the space vector based hysteresis current modulation using a commercially available simulation software such as Matlab/Simulink. Their different input-output characteristics and dynamic behavior are to be compared.
- Since the matrix converter is a direct frequency conversion device without DC-link components, the disturbances at the ac utility grid side are immediately reflected to the output side. So several performance and reliability issues of the matrix converter still need to be addressed, particularly, the influences of input line voltage disturbances on the output behavior of matrix converter. The performance of space vector modulation (SVM) technique and hysteresis current control (HCC) technique for matrix converter under abnormal input voltage conditions are to be investigated and critically compared. The SVM and HCC techniques are based on different modulation principles, and the HCC technique does not need to calculate the duty cycle for the fictitious inverting part. So under abnormal input voltage conditions, the HCC technique will have the inherent ability of preventing the disturbance at the grid side from propagating to the output side, and thereby

obtaining better output characteristics than SVM techniques.

1.3 Contributions

The main contributions of this study can be summarized as the following:

- Two kinds of novel SVM based HCC controllers for matrix converter have been proposed. Both controllers select appropriate space vector combinations via switching table including zero vector combination to reduce the switching frequency in matrix converter and do not require complex calculations.
- Simulation has been performed to verify that both of the proposed controllers can produce good sinusoidal output current and line voltage, and sinusoidal input current similar to those obtained by conventional SVM control technique of matrix converter. Because the four-level HCC system can more accurately determine the voltage vector, the switching frequency was reduced compared to that of the three-level system. Results also demonstrated that HCC systems offer faster dynamic behavior than SVM system.
- Abnormal supply voltage such as unbalanced voltage, non-sinusoidal voltage and voltage sag was introduced into the Matlab models of matrix converter SVM control system and HCC control system to investigate their different output behaviors. Simulation results show that under abnormal voltage supply condition, HCC modulation method can get much better output characteristics than SVM modulation method.

1.4 Thesis Outline

The rest of this thesis is organized as follows:

Chapter 2 gives the literature review of state-of-the-art matrix converter topologies, bidirectional switch configurations, commutation techniques for bidirectional switch, and

peripheral circuits for matrix converter. The advantages and disadvantages of each available technique are discussed.

Chapter 3 provides a detailed explanation on the working principle of matrix converter. This include the matrix converter control principle, Venturini modulation method, conventional indirect space vector modulation method, and optimized space vector modulation method. The detailed matrix converter input and output system analysis, derivation of matrix converter transfer function, and analysis of indirect SVM control method are given in this chapter.

Chapter 4 presents the hysteresis current control strategies for matrix converter. Hysteresis current control is one of the simplest techniques which can be used to control the phase currents in high speed drive systems, primarily because of its ease of implementation, fast current response, and inherent peak current limiting capability. This chapter describes how to apply hysteresis current control strategies to the matrix converter. The structure, switching table and working principle of both the three-level hysteresis current controller and the four-level hysteresis current controller are presented.

Chapter 5 gives the implementation and verification of both the SVM control system and the proposed multi-level HCC control systems for matrix converter in Matlab/Simulink simulation environment. Simulation results are provided in order to analyse the performances of the proposed HCC systems and to compare with that of the SVM system in terms of output line voltage, output and input currents, and their dynamic responses.

Chapter 6 presents the investigation of the performances of space vector modulation (SVM) technique and hysteresis current control (HCC) technique for matrix converter under abnormal input voltage conditions and to make critical comparison. The SVM and HCC techniques are based on different modulation principles, and the HCC technique does not need to calculate the duty cycle for the fictitious inverting part. So under abnormal input voltage conditions, the HCC technique has the inherent ability of preventing any disturbances at the grid side from propagating to the output side, and thereby obtaining better output characteristics than those of SVM technique.

Chapter 7 gives the conclusions of this thesis, and recommendations for future research.

Chapter 2

Matrix Converter Topology

2.1 Introduction

The most desirable features in power frequency converter can be summarized as follow:

1. simple and compact power circuit;
2. generation of load voltage with variable amplitude and frequency;
3. sinusoidal input and output current;
4. operation with unity power factor;
5. regeneration ability;

These ideal characteristics can be fulfilled by matrix converters, and this is the reason for the tremendous interest in the topology. The matrix converter is a forced commutated converter which uses an array of controlled bidirectional switches as the main power elements to create a variable output voltage system with unrestricted frequency. It does not have any DC-link circuit and does not need any large energy storage elements.

This chapter presents the literature review of those most fundamental and important theories applied in matrix converter topology: its bidirectional switch configuration,

commutation method for matrix converter, current direction detection methods, input filter, clamp circuit, and power-up circuit for matrix converter . In the process of review, the methodologies and techniques are described and their advantages and disadvantages are analyzed.

2.2 Matrix Converter Circuit

The circuit of traditional AC-DC-AC converter is shown in figure 2.1. The traditional AC-DC-AC converter topology includes the front rectifier, DC-link with bulk capacitor, and the inverter part. The front rectifier can be a diode rectifier as shown in this figure, or a controllable rectifier, which is implemented by replacing the diodes with controllable semiconductor switches such as MOSFET or IGBT.

Figure 2.1: Circuit of traditional AC-DC-AC converter

The key elements in a matrix converter are the fully controlled four-quadrant bidirectional switches, which allow high-frequency operation. The early work dedicated to unrestricted frequency changers used thyristors with external forced commutation cir-

cuits to implement the bidirectional controlled switches [5,6]. With this solution, the power circuit was bulky and the performance was poor. The modern commonly accepted basic matrix converter configuration with high-frequency (HF) control was subsequently introduced in 1980 [2]. This converter circuit is shown in figure 2.2.

Figure 2.2: Basic topology of matrix converter

Compared with the circuit of traditional AC-DC-AC converter in figure 2.1, this arrangement of bidirectional switches connects directly any of the input lines (a, b, or c) to any of the output lines (A, B, or C). The bidirectional switch is able to control the current and to block the voltage in both directions. The matrix converter does not require an intermediate circuit in contrast to traditional AC-DC-AC converter with bulky DC-link capacitor for storing energy. Due to its topology, the matrix converter has energy recovery capability and achieves sinusoidal input currents through a suitably designed controller. Also, the matrix converter offers an all-silicon solution which has the merit of compact design in contrast to traditional converter. The matrix converter

has the potential to meet desired qualities in power frequency converter mentioned in the beginning of section 2.1. Because of this, matrix converter has been the subject of intensive research in recent years.

If the input and the output of three-phase systems are orthogonally disposed, the converter diagram becomes similar to a matrix, with the rows consisting of the three input lines (a, b, c), the columns consisting of the three output lines (A, B, C), and bidirectional switches connecting each row to each column, which in figure 2.3 are symbolized with circles.

Figure 2.3: Symbolic representation of matrix converter

2.3 Analysis of Bidirectional Switch Topologies

In a paper written in 1988 [7], one of the first presenting the expectations for future development in ac drives, the matrix converter was credited with great potential. This was before important advances in this technology were achieved, such as reaching the highest limit of the voltage transfer ratio (0.866), proposal of space vector modulation for matrix converter, and proposal of a semisoft commutation strategy for bidirectional switches. At that time, it was considered that the MOS controlled thyristor (MCT)

will evolve toward having reverse blocking capability and will provide the “ideal” switch for matrix converter. Later, because of the soft commutation advantage, it has been shown that higher efficiency compared to that of a standard voltage source inverter (VSI) may be reached at higher switching frequencies, of more than 10kHz. As the MCT is a relatively slow device, the solution to implement a bidirectional switch is best based on the IGBT device. Other papers published later [8–11] give similar credit to the matrix converter technology, with the trend towards improving the interaction with the power grid, providing bidirectional power flow, increasing the efficiency of the drive while operating at higher switching frequency, decreasing the physical drive size, and integrating more complex silicon structures into the power modules.

Attempts were reported in the literature [12] and a patent was issued [13], for a new power device for matrix converter applications: the reverse blocking IGBT (RB-IGBT), which decreases to one the number of semiconductor devices per load phase path. The RB-IGBT is a new class of devices, with an inherent capability to block voltage in both the forward direction and the reverse direction. Standard IGBT and power MOSFET in the market today do not have a reverse blocking capability. In year 2003 [14], the first commercial RB-IGBT device was reported to be available on the market.

The industrial development of the matrix converter has been obstructed by the lack of a true force-commutated bidirectional switch. Using unidirectional devices available on the market, there are four ways to obtain a bidirectional switch: the diode embedded unidirectional switch (figure 2.4a), the two common-emitter (CE) unidirectional switches (figure 2.4c), the two common-collector (CC) unidirectional switches (figure 2.4d), or the two reverse blocking IGBT switches (figure 2.4b). The diode embedded switch requires only one gate driver and one active switch, which is more convenient for implementation than the other two configurations. A comprehensive analysis [12, 15, 16] shows that the embedded switch topology causes higher conduction losses because the current path consists of two fast recovery diodes (FRDs) and one IGBT and higher switching losses because all commutations are hard switched. The two topologies based on antiparallel connection of two unidirectional switches (CE and CC) allow for lower conduction loss because the current path consists of only one FRD and one IGBT, and for semisoft

Figure 2.4: Bidirectional switch topologies using unidirectional switches: (a) diode-embedded switch; (b) RB-IGBT switch; (c) common-emitter switch (CE); (d) common-collector switch (CC)

switching (half soft switching and half hard switching), as will be presented in the following section.

It is expected that when the RB-IGBT technology is mature and this kind of device becomes available for mass production, it will minimize the device count and the conduction losses in a matrix converter, while the control circuit will need little modification.

2.4 Bidirectional Switch Commutation Techniques

Similar to voltage source inverter (VSI), where dead-time commutation is necessary to eliminate the risk of shoot-through (short-circuit of the DC-link capacitors through an inverter leg) caused by non-ideal commutation characteristics, specific commutation techniques must be implemented when bidirectional switches are operated. Figure 2.5a

Figure 2.5: Commutation of the output phase *out* from input phase *x* to input phase *y*: (a) principle diagram; (b) ideal commutation; (c) dead-time commutation; (d) overlap commutation

shows the basic circuit and figure 2.5b shows the ideal command signals when the output line *out* is switched from one input line *x* to the other input line *y*, by operating two bidirectional switches S_x and S_y . The commutation technique depends on the type of bidirectional switches employed in the matrix converter hardware.

In the case of ideal four-quadrant switches, there are two possibilities for performing the commutation:

- The dead-time current commutation, referred to as “break before make,” is shown in figure 2.5c. This method consists of turning off the off-going switch while the on-coming switch is still disconnected, to avoid short-circuit of the inputs and thereby eliminate the over-current risk. This will cause over-voltage on the output side; therefore a clamp circuit connected to the output to provide a continuity of the load current is necessary, but it will cause high switching losses. The use of a regenerative clamp circuit has been reported in [17];
- The overlap current commutation, referred to as “make before break,” is shown in figure 2.5d. This method consists of turning on the in-coming switch while the off-going switch is still conducting, to provide continuity for the output line circuit in order to eliminate the risk of over-voltage. This will cause high circulating current between the input phases, which have to be limited during the commutation, by adding extra chokes in the input to decrease di/dt ;

Both methods require extra reactive elements and produce high losses. Because of practical implementation reasons, a bidirectional switch uses antiparalleled unidirectional switches, which provide independent control for each direction of the current. Therefore, other commutation strategies have been proposed [1, 4, 18–23] to provide safe commutation. Basically, the operation principle of such a method consists of two or four-step commutation technique, which avoids the disadvantage of the methods discussed before because it does not interrupt the load circuit or short-circuit the power grid lines, and therefore it does not require any additional reactive elements to provide safe commutation.

There are two ways to perform the so-called safe commutation: one is based on the direction of the output current [1, 4, 18–21, 23] and the other one is based on the polarity of the line-to-line voltage between the switches involved in the commutation process [22]. In the case of an output current direction detection based control, the first action is to disable the current path for circulating currents and then to apply overlapping commutation for the on-coming switch with the off-going switch. Therefore, the risk of short circuit on the input side is eliminated, and semisoft commutation, which means that half of the switch commutations are performed naturally, is achieved. In the case of a line-to-line voltage sign detection based control, the first action is to close a unidirectional path in the on-coming switch, which will not cause circulating currents, to ensure that there is a path for the load current before opening a unidirectional path in the off-going switch; this is identical for the other direction of current. The difference between the two methods is that for the output current direction control, a maximum of two unidirectional switches will be closed at any instant, whereas for the line-to-line voltage sign control, three unidirectional switches are closed at some instants. Because the load is usually inductive, while on the input side an LC circuit is usually used, it is considered that current sign detection offers safer and more stable operation even though it requires current transducers on the output side. For the other method, voltage transducers are necessary anyway for the control, but this signal may be noisy and more difficult to implement in hardware setup. Here, only the current direction controlled commutation will be presented.

2.4.1 Current Direction Four-step Commutation Strategy

This strategy [4, 18–20] operates the switches in such a way that after the commutation is completed, the switch acts as a four-quadrant bidirectional switch, so that the load current can freely reverse direction. The commutation takes place in four steps:

1. Turn off the off-going non-conducting switch. This way, current direction is not able to change;
2. Turn on the on-coming conducting switch. Now, there is a unidirectional connection between the input lines, but no circulating current may occur. In cases where there is a condition for natural commutation between the off-going switch and on-coming switch, it starts at this moment;
3. Turn off the off-going conducting switch. At this time, in the case of hard commutation, the current is forced to switch from the off-going switch to the on-coming switch;
4. Turn on the on-coming non-conducting switch. This is a passive step, with the purpose of reestablishing the four-quadrant characteristic of ac switch, so that the currents can change direction naturally;

This is shown in figure 2.6 where the commutation scheme takes into account the current sign and also the possibility to switch from one steady switching state to the other steady switching state.

In figure 2.7 the possible path for the output current allowed by the four-step commutation strategy is illustrated for both current directions. The duration of the “passive” commutation is step 1 and 4, because it is supposed that the device that is switched will or will not conduct; therefore it may change state faster. The duration of the “active” commutation is step 2 and 3, and the commutation is critical and should be chosen in agreement with the switching characteristics of devices employed in the antiparallel topology.

Figure 2.6: Four-step commutation scheme depending on the current direction

A complicated solution to adapt the duration of this “active” commutation has been proposed in [19], which modifies the period of the commutation clock with respect to the output current magnitude, but implies more complicated hardware. However, by adjusting the commutation clock period according to the maximum current magnitude, a safe and low-loss commutation is achieved, and for smaller output current the commutation will take place faster than the clock period, which does not cause any problem. The variation of the duty-cycle duration caused by the load current, according to the actual commutation situation, maybe satisfactorily compensated in the processor control program as with the dead-time in a voltage source inverter (VSI). This will be dependent on load current, which is measured, and the device parameters, which are known in advance.

Another problem is the commutation at nearly zero output current, where errors in the current sign may cause dead-time commutation. However, the energy in the inductance of the load, at the very low current levels that are susceptible to being affected by offset, does not cause dangerous over-voltage. This may be handled by the clamp circuit, without causing an additional increase in the commutation losses.

Figure 2.7: Illustration of current path allowed during the four-step commutation

2.4.2 Two-Step Commutation Strategy

Figure 2.8: Two-step current commutation timing diagram

Figure 2.9: Two-step current commutation state changing diagram

This strategy [1,21,23] has been developed in order to reduce the number of steps and the complexity of the commutation control unit. To perform the commutation in only two

steps, the bidirectional current path of the switch in the turn-on steady state is normally disabled, but the strategy is performed similarly to the four-step commutation, while the steady states of the bidirectional switches correspond to step 1, and step 3, presented in figure 2.7. At low current level where the current transducer may be affected by offset, it has been proposed to enable bidirectional current path of the on-state switch. In order to avoid the risk of a short circuit of the input lines during the commutation, a true dead-time current commutation has to be used. The timing diagram and state changing diagram of two-step commutation are shown in figure 2.8 and figure 2.9 respectively.

2.4.3 Current Direction Detection Methods

In order to control the bidirectional switch commutation properly, current transducers such as Hall transducers have been used. Also, a few other methods, which claimed not to be susceptible to offset error and exploiting the characteristics of the bidirectional switch topology, have been reported in the literature:

Figure 2.10: The current direction detection method based on the voltage drop [1]

- Comparing the magnitude of the voltage across the unidirectional switches in a CE bidirectional topology [1], as shown in figure 2.10. This method has the advantage that it does not require any transducer and provide good precision, but it requires components to handle the peak line-to-line voltage which appears across nonconducting unidirectional switches (IGBT+FRD);
- Measuring the voltage drop across two antiparallel diodes connected on the output line [21]. This method is very simple, but causes voltage drop on the output side, in an application where the voltage transfer ratio is a sensitive issue. However,

for a normal (slow) diode, which causes a 0.7V-1V voltage drop, the decrease of voltage transfer ratio is only 0.2%-0.3%;

2.5 Peripheral Circuit for Matrix Converter

We can see from figure 2.2 that the silicon structure of the nine bidirectional switches needs a few reactive elements in order to work properly, and these are found in the input filter and the clamp circuit (see figure 2.11). Below, a few aspects regarding the hardware implementation, such as auxiliary circuits needed for safe matrix converter operation and design criteria for these circuits, will be presented.

2.5.1 The input filter

This has to reduce the input current ripple with minimum installed energy on the reactive elements. The most used topology is LC series circuit. The use of more complex topologies has been recommended in the literature in order to achieve higher attenuation at the switching frequency, but they are not practical. The design of the input filter has to accomplish the following:

- Produce an input filter with a cutoff frequency lower than the switching frequency:

$$L_{\text{in}} \cdot C_{\text{in}} = \frac{1}{\omega_0^2} \quad (2.1)$$

where L_{in} , C_{in} are the respective values of the inductance and the capacitor of the input filter and $\omega_0 = 2\pi \cdot f_0$ is the resonance pulsation of the input filter.

- Maximize the displacement angle $\varphi_{\text{min-in}}$ for a given minimum output power:

$$\frac{C_{\text{in}}}{P_{\text{n}}} = k_{\text{min}} \cdot \tan \varphi_{\text{min-in}} \frac{1}{3 \cdot \omega_{\text{n}} \cdot V_{\text{n}}^2} \quad (2.2)$$

where $P_{\text{n}} \cong 3 \cdot V_{\text{n}} \cdot I_{\text{n}}$ is the input active power (considering a close to unity power factor at full load); V_{n} , I_{n} are the respective rated input phase voltage and

current of the converter, $P_{\min} = k_{\min} \cdot P_n$ is the minimum power level where the displacement angle $\varphi_{\min-\text{in}}$ reaches its limit and $\omega_n = 2\pi \cdot f_n$ is the pulsation of the power grid.

- Minimize the input filter volume or weight for a given reactive power, by taking into account the energy densities which are different for film capacitors from iron chokes:

$$\frac{S_L}{S_C} = \frac{1}{(3 \cdot \omega_0 \cdot V_n^2)^2} \cdot \left(\frac{P_n}{C_{\text{in}}} \right)^2 \quad (2.3)$$

where $S_L = \omega_n \cdot L_{\text{in}} \cdot I_n^2$ (choke), $S_C = \omega_n \cdot C_{\text{in}} \cdot V_n^2$ (capacitor) are the installed VA in reactive components and $\omega_0 = 2 \cdot \pi \cdot f_0 = (L_{\text{in}} \cdot C_{\text{in}})^{-1/2}$.

- Minimize the voltage drop on the filter inductance at the rated current in order to provide the highest voltage transfer ratio:

$$\frac{\Delta V}{V_n} = 1 - \sqrt{1 - (\omega_n \cdot L_{\text{in}})^2 \cdot \left(\frac{I_n}{V_n} \right)^2} = 1 - \sqrt{1 - l_{\text{in}}^2} \quad (2.4)$$

where ΔV is the drop in voltage magnitude due to the influence of the input filter and l_{in} is the filter inductance in p.u.

Usually, the cutoff frequency of the LC input filter ω_0 is chosen to provide a given attenuation at the switching frequency. In addition, the value of the capacitor or the inductance is chosen based on one of the previous criteria.

2.5.2 The clamp circuit

Similar to standard diode bridge VSI, the matrix converter topology needs to be protected from over-voltage and over-current. Furthermore, the topology of matrix converter is more sensitive to disturbances and therefore more susceptible to failures due to the lack of an energy storage element in the DC-link. Disturbances, which may cause hardware failures, are:

- Faulty inter switch commutations, such as internal short circuit of the mains or

disconnecting the circuit of the motor currents;

- Shutdown of the matrix converter during an over-current situation on the motor side;
- Possible over-voltage on the input side caused by the converter power-up or by voltage sags;

The protection issues for matrix converter have received increased attention, in order to build a reliable prototype. A solution to solve some of the problems is based on connecting a clamp circuit on the output side [24]. One patent issued for the clamping of the output lines [25] is shown in figure 2.11. The clamp consists of two diode rectifier

Figure 2.11: The clamp circuit

bridges using fast-recovery diodes at the input and output. A capacitor C_C stores the commutation energy. A resistor may be used to discharge the capacitor. Under normal conditions, the clamp only has to cope with the energy stored in the leakage inductances. The critical situation for the design of C_C concerns the faults. The design of the clamp is carried out under the assumption that a fault has generated an error signal to the power converter. All switches in the converter are turned off immediately. The task of the clamp is now to de-energize the load without damaging the power switches. The total energy stored in a three-phase inductance carrying sinusoidal balanced currents is calculated as

$$Q_L = \frac{1}{2}L(i_a^2 + i_b^2 + i_c^2) = \frac{3}{4}L\hat{I}^2 \quad (2.5)$$

Figure 2.12: Discharging of the induction machine inductances to the clamp capacitor during a fault situation. (a) Equivalent model of converter and induction motor. (b) Currents in induction motor

where Q_L is the total energy stored in the three load inductances, i_a , i_b , and i_c are the three phase currents, and $\hat{I}$ is the rms value of the line currents. Q_L is the energy to transfer to the clamp in the case that the matrix converter feeds a passive load. In the case of an induction motor load, the situation is more complicated. Figure 2.12 shows a simplified equivalent circuit of the induction motor when the clamp capacitor

is charged through the clamp diodes. All switches in the converter are turned off. In figure 2.12, i_s is the stator current, i_r the rotor current, and i_m the magnetizing current. $L_{\delta s}$ is the stator leakage inductance and $L_{\delta r}$ the rotor leakage inductance. L_m is the magnetizing inductance of the motor, and C_c is the clamp capacitor. During the fault when the clamp diodes are in conduction, the clamp capacitor will be connected across the input terminals of the motor with such a voltage polarity that the motor will be de-energized. The initial clamp voltage v_{c0} equals the peak line input voltage, which for a 400V network corresponds to 565V. The magnetizing current is assumed constant during the discharge. The rotor current will change from the initial current i_r to the level of the magnetizing current i_m . The clamp diodes will conduct until the stator current reaches zero. This is shown in figure 2.12(b). The total amount of energy transferred to the clamp is, therefore, calculated as

$$\Delta Q_{motor} = \frac{3}{4}(L_{\delta s}\hat{i}_s^2 + L_{\delta r}\hat{i}_r^2 + L_m\hat{i}_m^2) \quad (2.6)$$

which, for the worst case condition where i_m equals zero, corresponds to

$$\Delta Q_{motor,max} = \frac{3}{4}\hat{i}_s^2(L_{\delta s} + L_{\delta r}), \quad \text{for } i_m=0 \quad \wedge \quad i_r = i_s \quad (2.7)$$

The energy $\Delta Q_{motor,max}$ is used as a design parameter for the clamp capacitor. The voltage rise of the clamp capacitor is calculated as

$$v_{c1} = \sqrt{\frac{(\frac{1}{2}v_{c0}^2 C_c) + \Delta Q_{motor,max}}{\frac{1}{2}C_c}} \quad (2.8)$$

where v_{c1} is the voltage across the clamp capacitor after the motor has been de-energized. Only the magnetic energy is transferred to the clamp capacitor. Due to the large mechanical time constants, the speed of the motor is unaffected during the clamp operation. When the motor is de-energized, the inertia of the motor and load will determine the time to standstill. To calculate the capacitance needed in the clamp, (2.7) is inserted

into (2.8).

$$C_c = \frac{2\Delta Q_{motor,max}}{v_{max}^2 - v_{c0}^2} = \frac{\frac{3}{2}I_{lim}^2(L_{\delta s} + L_{\delta r})}{v_{max}^2 - 565^2} \quad (2.9)$$

where v_{c1} is substituted by v_{max} which is the maximum acceptable clamp voltage. The term $\hat{i}_s^2$ in (2.7) has been substituted with the hardware current limit of the converter I_{lim} . This shows that there are three design parameters for the clamp capacitor: the voltage rating of the semiconductors, the leakage inductances of the attached motor, and the hardware current limit of the converter. Also, the same but more generalized equation to calculate the clamp capacitor is formulated in [26].

$$\frac{3}{4} \cdot i_{max}^2 \cdot (L_{\delta S} + L_{\delta R}) = \frac{1}{2} \cdot C_C \cdot \left[V_{max}^2 - (\sqrt{2} \cdot V_{line})^2 \right] \quad (2.10)$$

where i_{max}^2 is the over-current protection level, $L_{\delta S} + L_{\delta R}$ is the total motor leakage inductance, V_{max} is the maximum admissible over-voltage, and V_{line} is the rms line-to-line input voltage.

2.5.3 The Power-Up Circuit

The purpose of this circuit is to provide a fast and safe power-up of the matrix converter, by eliminating the transients with higher over-voltage levels, which are characteristics of the LC-series circuit. Damping of the inductance is most convenient for implementation. Series damping eliminates the transients, but after the power-up, the damping resistors should be bypassed in order to avoid higher power loss and therefore, the bypass relay should be able to handle the nominal current of the converter continuously. The principle diagram is presented in figure 2.13.

The voltage across the clamp capacitor controls the bypass relay, which has normal open (NO) armatures: if the voltage is low, the relay is de-energized, and therefore the damping resistors are introduced in the main circuit, in series with the filter inductance. The value of the series damping resistors R_s should satisfy (2.11), in order to eliminate

the transients:

$$R_s \geq 2\sqrt{\frac{L_{in}}{C_{in}}} \quad (2.11)$$

In order to reduce the level of oscillating energy that accumulates in the filter inductance during the transients, by-passing the inductors with parallel damping resistors is another solution. The principle diagram is presented in figure 2.14. The value of the parallel damping resistor R_p should be smaller than the reactance of the choke, calculated at the cut-off frequency ω_0 of the input filter.

$$R_p \leq \omega_0 \cdot L_{in} \quad (2.12)$$

Figure 2.13: Power-up circuit for matrix converter using series damping resistors

The voltage across the clamp capacitor controls the relay. If the voltage is low, the relay is de-energized and the normally closed (NC) armatures introduce the damping resistors in the circuit, by-passing the input filter inductance. If the voltage increases above a certain level, the relay is energized and damping resistors are disconnected. The relay contacts are used only during the power-up. The in-rush current into the clamp circuit is higher, but it is similar to the situation when no over-voltage reduction scheme is used. In this case, the disadvantage is that the diodes from the clamp circuit should be

Figure 2.14: Power-up circuit for matrix converter using parallel damping resistors

able to handle large currents during power-up. If no neutral current flows in the input filter circuit, it is possible to simplify these schemes, by damping the input filter only in two phases, which will require less components.

2.6 Concluding Remarks

In this chapter, a general description of the matrix converter topology is given. In section 2.2, the matrix converter circuit is compared with the circuit of traditional AC-DC-AC converter. With the arrangement of the bidirectional power switches in a three-times-three switch matrix, the matrix converter offers the advantage of bidirectional power flow, four quadrant operation, and the merits of compact design because it does not need the bulk DC-link capacitor in contrast to traditional AC-DC-AC converter.

Section 2.3 and section 2.4 provide a general review of bidirectional switches topology and its commutation techniques. There are four ways to construct the bidirectional switch required for matrix converter, each way has its own characteristics in terms of how many semiconductor components are required and how much loss will be caused. The commutation techniques for matrix converter bidirectional switches are totally dif-

ferent from traditional voltage source inverter. The specific aspects for commutation of bidirectional switch is described, include four-step commutation, two-step commutation, and current sign detection method.

Section 2.5 gives the review of peripheral circuit for matrix converter, and focuses on three specific topics: the input filter, the clamp circuit, and the power-up circuit. For each kind of peripheral circuit, the detail descriptions for why the system need such circuits, how to calculate the components rating, and how to construct such circuits are given.

Chapter 3

Modulation Techniques for Matrix Converter

3.1 Introduction

This chapter provides a detailed explanation on the well established working principle of matrix converter. The first modulation method proposed for matrix converter, known as Venturini modulation, used a complicated scalar model that gave a maximum voltage transfer ratio of 0.5 [2, 27]. An injection of a third harmonic of the input and output voltage (3.1) was proposed in order to fit the reference output voltage in the input voltage system envelope, and the voltage transfer ratio was able to reach the maximum value of 0.866 [28–32].

$$\begin{aligned} \begin{bmatrix} V_A(t) \\ V_B(t) \\ V_C(t) \end{bmatrix} &= \sqrt{2} \cdot V_o \cdot \begin{bmatrix} \cos(\omega_o \cdot t) \\ \cos(\omega_o \cdot t - 2\pi/3) \\ \cos(\omega_o \cdot t - 4\pi/3) \end{bmatrix} - \sqrt{2} \cdot \frac{V_o}{6} \cdot \begin{bmatrix} \cos(3\omega_o \cdot t) \\ \cos(3\omega_o \cdot t) \\ \cos(3\omega_o \cdot t) \end{bmatrix} \\ &\quad + \sqrt{2} \cdot \frac{V_i}{4} \cdot \begin{bmatrix} \cos(3\omega_i \cdot t) \\ \cos(3\omega_i \cdot t) \\ \cos(3\omega_i \cdot t) \end{bmatrix} \end{aligned} \quad (3.1)$$

where V_o and V_i are the respective RMS values of the output and input voltage systems, and ω_o and ω_i are the respective angular frequencies of the output and input voltage systems.

Next, indirect modulation was proposed [17, 25, 33]. This approach simplified the modulator model by making it possible to implement classical PWM modulation strategies in matrix converter [17]. Modulation models using space vectors (SVM) [3, 34–37] or the direct torque control (DTC) [38] simplified the modulator model, making it easier to control the converter under unbalanced and distorted power supply condition or to implement high-performance control of the induction motors.

3.2 Matrix Converter Control Principles

In order to provide safe operation of the matrix converter, two basic rules have to be followed:

- Do not connect two different input lines to the same output line since this will result in an input line to line short circuit leading to switch over currents;
- Do not disconnect the output line circuits since there would be then no path for the inductive load current and large over voltage would destroy the switches;

The simplified matrix converter circuit is shown in figure 3.1. If the switching function of a switch, S_{jk} in figure 3.1, is defined as

$$S_{jk}(t) = \begin{cases} 1, & S_{jk} \text{ closed} \\ 0, & S_{jk} \text{ open} \end{cases} \quad j \in \{A, B, C\}, \quad k \in \{a, b, c\} \quad (3.2)$$

the constraints can be expressed as

$$S_{ja} + S_{jb} + S_{jc} = 1, \quad j \in \{A, B, C\} \quad (3.3)$$

With these constraints, the $3\phi - 3\phi$ matrix converter from figure 3.1 can assume only

Figure 3.1: Simplified matrix converter circuit

27 allowed combinations (see Table 3.1). The table also shows which input and output phases are mutually connected for each allowed switching combination, as well as the resulting output line voltages and input phase currents. The switching combinations can be classified into three groups. The first group includes six combinations where each output phase is connected to a different input phase. In the second group, there are 18 combinations with two output phases shorted. The third group includes three combinations with all three output phases shorted. From Table 3.1 and figure 3.1, the following expressions for the output line voltages and input phase currents are directly obtained:

$$\begin{aligned}
 \mathbf{V}_{oL} &= \begin{bmatrix} v_{AB} \\ v_{BC} \\ v_{CA} \end{bmatrix} \\
 &= \begin{bmatrix} s_{Aa} - s_{Ba} & s_{Ab} - s_{Bb} & s_{Ac} - s_{Bc} \\ s_{Ba} - s_{Ca} & s_{Bb} - s_{Cb} & s_{Bc} - s_{Cc} \\ s_{Ca} - s_{Aa} & s_{Cb} - s_{Ab} & s_{Cc} - s_{Ac} \end{bmatrix} \cdot \begin{bmatrix} v_{a0} \\ v_{b0} \\ v_{c0} \end{bmatrix} \\
 &= \mathbf{T}_{PhL} \cdot \mathbf{v}_{iPh}
 \end{aligned} \tag{3.4}$$

Table 3.1: Matrix converter switching combinations ($K = 2/\sqrt{3}$)

Group	A B C	V_{AB} V_{BC} V_{CA}	i_a i_b i_c	V_o α	i_i β
I	a b c	V_{ab} V_{bc} V_{ca}	i_A i_B i_C	V_i $\omega_i t$	I_o $\omega_o t$
	a c b	$-V_{ca}$ $-V_{bc}$ $-V_{ab}$	i_A i_C i_B	$-V_i - \omega_i t + 4\pi/3$	$-I_o - \omega_o t$
	b a c	$-V_{ab}$ $-V_{ca}$ $-V_{bc}$	i_B i_A i_C	$-V_i - \omega_i t$	$-I_o - \omega_o t + 2\pi/3$
	b c a	V_{bc} V_{ca} V_{ab}	i_C i_A i_B	$V_i \omega_i t + 4\pi/3$	$I_o \omega_o t + 2\pi/3$
	c a b	V_{ca} V_{ab} V_{bc}	i_B i_C i_A	$V_i \omega_i t + 2\pi/3$	$I_o \omega_o t + 2\pi/3$
	c b a	$-V_{bc}$ $-V_{ab}$ $-V_{ca}$	i_C i_B i_A	$-V_i - \omega_i t + 2\pi/3$	$-I_o - \omega_o t + 2\pi/3$
II-A	a c c	$-V_{ca}$ 0 V_{ca}	i_A 0 $-i_A$	KV_{ca} $7\pi/6$	Ki_A $\pi/6$
	b c c	V_{bc} 0 $-V_{ca}$	0 i_A $-i_A$	KV_{bc} $\pi/6$	Ki_A $\pi/2$
	b a a	$-V_{ab}$ 0 V_{ab}	$-i_A$ i_A 0	KV_{ab} $7\pi/6$	Ki_A $5\pi/6$
	c a a	V_{ca} 0 $-V_{ca}$	$-i_A$ 0 i_A	KV_{ca} $\pi/6$	Ki_A $7\pi/6$
	c b b	$-V_{bc}$ 0 V_{bc}	0 $-i_A$ i_A	KV_{bc} $7\pi/6$	Ki_A $3\pi/2$
	a b b	V_{ab} 0 $-V_{ab}$	i_A $-i_A$ 0	KV_{ab} $\pi/6$	Ki_A $-\pi/6$
II-B	c a c	V_{ca} $-V_{ca}$ 0	i_B 0 $-i_B$	KV_{ca} $-\pi/6$	Ki_B $\pi/6$
	c b c	$-V_{bc}$ V_{bc} 0	0 i_B $-i_B$	KV_{bc} $5\pi/6$	Ki_B $\pi/2$
	a b a	V_{ab} $-V_{ab}$ 0	$-i_B$ i_B 0	KV_{ab} $-\pi/6$	Ki_B $5\pi/6$
	a c a	$-V_{ca}$ V_{ca} 0	$-i_B$ 0 i_B	KV_{ca} $5\pi/6$	Ki_B $7\pi/6$
	b c b	V_{bc} $-V_{bc}$ 0	0 $-i_B$ i_B	KV_{bc} $-\pi/6$	Ki_B $3\pi/2$
	b a b	$-V_{ab}$ V_{ab} 0	i_B $-i_B$ 0	KV_{ab} $5\pi/6$	Ki_B $-\pi/6$
II-C	c c a	0 V_{ca} $-V_{ca}$	i_C 0 $-i_C$	KV_{ca} $\pi/2$	Ki_C $\pi/6$
	c c b	0 $-V_{bc}$ V_{bc}	0 i_C $-i_C$	KV_{bc} $3\pi/2$	Ki_C $\pi/2$
	a a b	0 V_{ab} $-V_{ab}$	$-i_C$ i_C 0	KV_{ab} $\pi/2$	Ki_C $5\pi/6$
	a a c	0 $-V_{ca}$ V_{ca}	$-i_C$ 0 i_C	KV_{ca} $3\pi/2$	Ki_C $7\pi/6$
	b b c	0 V_{bc} $-V_{bc}$	0 $-i_C$ i_C	KV_{bc} $\pi/2$	Ki_C $3\pi/2$
	b b a	0 $-V_{ab}$ V_{ab}	i_C $-i_C$ 0	KV_{ab} $3\pi/2$	Ki_C $-\pi/6$
III	a a a	0 0 0	0 0 0	0 —	0 —
	b b b	0 0 0	0 0 0	0 —	0 —
	c c c	0 0 0	0 0 0	0 —	0 —

and

$$\mathbf{i}_{\text{Ph}} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \mathbf{T}_{\text{PhL}}^T \cdot \begin{bmatrix} i_{AB} \\ i_{BC} \\ i_{CA} \end{bmatrix} = \mathbf{T}_{\text{PhL}}^T \cdot \mathbf{i}_{oL} \quad (3.5)$$

where the superscript T denotes a transpose and the matrix $\mathbf{T}_{\text{PhL}}$ is the instantaneous input-phase to output-line transfer function matrix of the $3\phi - 3\phi$ matrix converter. Alternatively, the output phase voltages referenced to the input neutral and the input

phase currents can be expressed as

$$\begin{aligned} \mathbf{v}_{oPh} &= \begin{bmatrix} v_{A0} \\ v_{B0} \\ v_{C0} \end{bmatrix} = \begin{bmatrix} s_{Aa} & s_{Ab} & s_{Ac} \\ s_{Ba} & s_{Bb} & s_{Bc} \\ s_{Ca} & s_{Cb} & s_{Cc} \end{bmatrix} \cdot \begin{bmatrix} v_{a0} \\ v_{b0} \\ v_{c0} \end{bmatrix} \\ &= \mathbf{T}_{PhPh} \cdot \mathbf{v}_{iPh} \end{aligned} \quad (3.6)$$

and

$$\mathbf{i}_{iPh} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \mathbf{T}_{PhPh}^T \cdot \begin{bmatrix} i_{AB} \\ i_{BC} \\ i_{CA} \end{bmatrix} = \mathbf{T}_{PhPh}^T \cdot \mathbf{i}_{oPh} \quad (3.7)$$

where the matrix $\mathbf{T}_{PhPh}$ is the instantaneous input-phase to output-phase matrix. In order to use the HF(high frequency) synthesis methodology, the switching frequency must be much higher than the frequencies of the input voltages and output currents, which are assumed to be continuous LF(low frequency) functions. Then, the HF components of the variables in (3.4)-(3.7) can be neglected. The low-frequency or local-averaged value of a switching function s_{jk} is the duty cycle of the switch S_{jk} , and it is denoted as d_{jk} . The LF equivalents of (3.2)-(3.7) are

$$0 \leq d_{jk} \leq 1, \quad j \in \{A, B, C\}, \quad k \in \{a, b, c\}, \quad (3.8)$$

$$d_{ja} + d_{jb} + d_{jc} = 1, \quad j \in \{A, B, C\}, \quad (3.9)$$

$$\bar{\mathbf{v}}_{oL} = \bar{\mathbf{T}}_{PhL} \cdot \mathbf{v}_{iPh}, \quad (3.10)$$

$$\bar{\mathbf{i}}_{iPh} = \bar{\mathbf{T}}_{PhL}^T \cdot \mathbf{i}_{oL}, \quad (3.11)$$

$$\bar{\mathbf{v}}_{oPh} = \bar{\mathbf{T}}_{PhPh} \cdot \mathbf{v}_{iPh}, \quad (3.12)$$

$$\bar{\mathbf{i}}_{iPh} = \bar{\mathbf{T}}_{PhPh}^T \cdot \mathbf{i}_{oPh} \quad (3.13)$$

respectively, where

$$\bar{\mathbf{T}}_{PhL} = \begin{bmatrix} d_{Aa} - d_{Ba} & d_{Ab} - d_{Bb} & d_{Ac} - d_{Bc} \\ d_{Ba} - d_{Ca} & d_{Bb} - d_{Cb} & d_{Bc} - d_{Cc} \\ d_{Ca} - d_{Aa} & d_{Cb} - d_{Ab} & d_{Cc} - d_{Ac} \end{bmatrix} \quad (3.14)$$

and

$$\bar{\mathbf{T}}_{\text{PhPh}} = \begin{bmatrix} d_{Aa} & d_{Ab} & d_{Ac} \\ d_{Ba} & d_{Bb} & d_{Bc} \\ d_{Ca} & d_{Cb} & d_{Cc} \end{bmatrix} \quad (3.15)$$

are the LF input-phase to output-line and input-phase to output-phase transfer matrices.

Let the input phase voltage be given by

$$\mathbf{v}_{i\text{Ph}} = V_{im} \cdot \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t - 120^\circ) \\ \cos(\omega_i t + 120^\circ) \end{bmatrix} \quad (3.16)$$

If it is desired that the local-averaged output line voltages be sinusoidal, i.e.

$$\begin{aligned} \bar{\mathbf{v}}_{oL} &= \begin{bmatrix} \bar{v}_{AB} \\ \bar{v}_{BC} \\ \bar{v}_{CA} \end{bmatrix} \\ &= \sqrt{3} \cdot V_{om} \cdot \begin{bmatrix} \cos(\omega_o t - \varphi_o + 30^\circ) \\ \cos(\omega_o t - \varphi_o + 30^\circ - 120^\circ) \\ \cos(\omega_o t - \varphi_o + 30^\circ + 120^\circ) \end{bmatrix} \end{aligned} \quad (3.17)$$

then with the LF input-phase to output-line transfer matrix chosen as

$$\bar{\mathbf{T}}_{\text{PhL}} = m \cdot \begin{bmatrix} \cos(\omega_o t - \varphi_o + 30^\circ) \\ \cos(\omega_o t - \varphi_o + 30^\circ - 120^\circ) \\ \cos(\omega_o t - \varphi_o + 30^\circ + 120^\circ) \end{bmatrix} \cdot \begin{bmatrix} \cos(\omega_i t - \varphi_i) \\ \cos(\omega_i t - \varphi_i - 120^\circ) \\ \cos(\omega_i t - \varphi_i + 120^\circ) \end{bmatrix}^T \quad (3.18)$$

where $0 \leq m \leq 1$ is the modulation index and φ_i is an arbitrary angle, (3.16)-(3.18) satisfy (3.10) with

$$V_{om} = \frac{\sqrt{3}}{2} \cdot V_{im} \cdot m \cdot \cos(\varphi_i) \quad (3.19)$$

In this case, due to the inductive nature of the load, the output line currents can be assumed sinusoidal, and hence given by

$$\mathbf{i}_{oL} = \sqrt{3} \cdot I_{om} \cdot \begin{bmatrix} \cos(\omega_o t - \varphi_o - \varphi_L + 30^\circ) \\ \cos(\omega_o t - \varphi_o - \varphi_L + 30^\circ - 120^\circ) \\ \cos(\omega_o t - \varphi_o - \varphi_L + 30^\circ + 120^\circ) \end{bmatrix} \quad (3.20)$$

where φ_L is the load displacement angle at the output frequency f_o . If (3.18) and (3.20) are substituted into (3.11), the local-averaged input phase currents are obtained as

$$\bar{\mathbf{i}}_{iPh} = \begin{bmatrix} \bar{i}_a \\ \bar{i}_b \\ \bar{i}_c \end{bmatrix} = I_{im} \cdot \begin{bmatrix} \cos(\omega_i t - \varphi_i) \\ \cos(\omega_i t - \varphi_i - 120^\circ) \\ \cos(\omega_i t - \varphi_i + 120^\circ) \end{bmatrix} \quad (3.21)$$

where

$$I_{im} = \frac{\sqrt{3}}{2} \cdot I_{om} \cdot m \cdot \cos(\varphi_L) \quad (3.22)$$

It follows from (3.19) that one can make a trade-off between the modulation index, m , the voltage gain, V_{om}/V_{im} , and the input displacement angle, φ_i , independently of the load displacement angle. Unity input displacement factor is obtained for $\varphi_i = 0$, which from (3.19), with $m = 1$, also results in the maximum voltage gain of $\sqrt{3}/2$. Physically, the only restriction is the equality of the input and output active powers, because from (3.19) and (3.22) it follows that:

$$\begin{aligned} P_i &\equiv \frac{3}{2} \cdot V_{im} \cdot I_{im} \cdot \cos(\varphi_i) \\ &= \frac{3}{2} \cdot V_{om} \cdot I_{om} \cdot \cos(\varphi_L) \equiv P_o \end{aligned} \quad (3.23)$$

By rewriting (3.17), (3.18), and (3.20) without $\sqrt{3}$ and 30° and writing $m/2$ instead of m in (3.18), equations for synthesis of output phase voltages can be obtained. In this case, the maximal voltage gain is $3/4$. Obviously, the whole procedure from this section can be repeated starting from the input line voltages.

To make a final $3\phi - 3\phi$ matrix converter control algorithm using the HF-synthesis methodology, two additional steps are needed. First, the switch duty cycles, d_{jk} , which implement a desired LF transfer matrix (e.g., (3.18)) and satisfy (3.8) and (3.9), have to be determined. Second, the position of the switching pulses within the switching cycle has to be defined.

3.3 Venturini Modulation (Scalar Modulation) Method

In order to provide balance for the output voltages and also for the input current, it is necessary that the modulation strategy uses the input voltages equally when producing the output voltages. Scalar modulation, also referred to as Venturini modulation, establishes independent relations for each output, by sampling and distributing slices of input voltage in such a way that the average result follows the reference output phase voltage and the average input currents are sinusoidal. The relation between the input and output voltage and that of the input and output current can be written as (3.24) and (3.25) [2], in order to provide balance during the switching period:

$$\begin{bmatrix} V_A(t) \\ V_B(t) \\ V_C(t) \end{bmatrix} = \begin{bmatrix} m_{11}(k) & m_{12}(k) & m_{13}(k) \\ m_{21}(k) & m_{22}(k) & m_{23}(k) \\ m_{31}(k) & m_{32}(k) & m_{33}(k) \end{bmatrix} \cdot \begin{bmatrix} V_a(t) \\ V_b(t) \\ V_c(t) \end{bmatrix} \quad (3.24)$$

$$\begin{bmatrix} I_a(t) \\ I_b(t) \\ I_c(t) \end{bmatrix} = \begin{bmatrix} m_{11}(k) & m_{21}(k) & m_{31}(k) \\ m_{12}(k) & m_{22}(k) & m_{32}(k) \\ m_{13}(k) & m_{23}(k) & m_{33}(k) \end{bmatrix} \cdot \begin{bmatrix} I_A(t) \\ I_B(t) \\ I_C(t) \end{bmatrix} \quad (3.25)$$

where $m_{ij}(k)$ represents the duty cycles of a switch connection output line i to input line j in the k switching period.

The input phase voltage and the output currents are considered constant during the switching period. At any time, $0 \leq m_{ij}(k) \leq 1$, and also, because the output phase

circuit should not remain disconnected from an input phase:

$$\sum_{j=1}^3 m_{ij}(k) = 1 \quad (3.26)$$

If the reference voltage vector, given in (3.1), is replaced in the transfer function of the output voltages depending on the duty cycles and input voltages (3.24), a complicated duty cycle equation appears:

$$\begin{aligned} m_{ij} = & \frac{1}{3} \cdot \{1 + (1 - \tan \varphi_i / \tan \varphi_o) \cdot \frac{V_o}{V_i} \cdot \cos((\omega_o + \omega_i) \cdot t - 2 \cdot ((i + j) - 4) \cdot \pi/3) \\ & + (1 - \tan \varphi_i / \tan \varphi_o) \cdot \frac{V_o}{V_i} \cdot \cos((\omega_o - \omega_i) \cdot t - 2 \cdot (i - j) \cdot \pi/3) \\ & - \frac{1}{6} \cdot \frac{V_o}{V_i} \cdot [\cos((3\omega_o + \omega_i) \cdot t - 2 \cdot (j - 1) \cdot \pi/3) + \cos((3\omega_o - \omega_i) \cdot t - 2 \cdot (1 - j) \cdot \pi/3)] \\ & + \frac{V_o}{V_i} \cdot [-\frac{1}{6\sqrt{3}} \cos(4\omega_i \cdot t - 2 \cdot (j - 1) \cdot \pi/3) + \frac{7}{6\sqrt{3}} \cos(2\omega_i \cdot t - 2 \cdot (1 - j) \cdot \pi/3)]\} \end{aligned} \quad (3.27)$$

where φ_i and φ_o are the input and output displacement angles respectively.

Because of the complexity of the duty cycle computation, this algorithm is time consuming. Other modulation methods have been derived by employing space vector representation of three phase output voltage, called space vector modulation. The space vector modulation method can help to simplify the duty cycle calculation for each switch so that it can be efficiently implemented with modern high speed digital signal processor.

3.4 Space Vector Modulation Method

Equation (3.18) presents an indirect transfer function (ITF) approach. The transfer matrix is equal to the product of two matrices

$$\bar{\mathbf{T}}_{\text{PhL}} = \bar{\mathbf{T}}_{\text{VSI}}(\omega_o) \cdot \bar{\mathbf{T}}_{\text{VSR}}^T(\omega_i) \quad (3.28)$$

By multiplication of matrix $\bar{\mathbf{T}}_{\text{VSR}}^T(\omega_i)$ with the input voltage vector (3.16), a constant voltage is obtained

$$\bar{\mathbf{T}}_{\text{VSR}}^T(\omega_i) \cdot \mathbf{v}_{i\text{Ph}} = \frac{3}{2} \cdot V_{im} \cdot \cos(\varphi_i) = \text{const.} \quad (3.29)$$

This is equivalent to the operation of a voltage source rectifier (VSR). By multiplying the voltage (3.29) with the matrix $\bar{\mathbf{T}}_{\text{VSI}}(\omega_o)$, the operation of a voltage source inverter (VSI) is performed. Therefore, the ITF approach emulates a VSR-VSI conversion, as shown in figure 3.2. It follows from figure 3.2 that at any instance the $3\phi - 3\phi$ matrix converter

Figure 3.2: Equivalent VSR-VSI circuit of matrix converter

reduces to one of the six possible VSI subtopologies with $v_{pn} \in \{v_{ab}, v_{bc}, v_{ca}, v_{ba}, v_{cb}, v_{ac}\}$. It can be easily verified that for each allowed switching combination in figure 3.2, there is only one switching combination in Table 3.1 that results in the same output voltages and input currents. This correspondence includes all combinations from the second and third groups in Table 3.1, and none from the first group. The ITF approach enables application of well-known standard VSI and VSR PWM techniques for matrix converter control. In the case of output line-voltage synthesis, the maximal VSI voltage gain is

equal to unity, and hence from (3.29) the maximal matrix converter gain is $\sqrt{3}/2$. When sinusoidal output phase voltages are synthesized, the maximal phase voltage amplitude is one half of the DC-link voltage, and from (3.29) the maximal matrix converter gain is $3/4$. In this case, the output neutral point voltage is equal to the DC-link midpoint voltage which varies as $(V_{im}/4) \cdot \cos(3\omega_i t)$ with respect to the input neutral.

In the following section, based on the ITF approach, the space vector modulation is simultaneously employed in both VSR and VSI parts of the matrix converter. First, the VSI-SVM and VSR-SVM procedures are reviewed, and the respective LF transfer functions are derived. Then, the three steps of the HF-synthesis of the simultaneous output-voltage and input-current SVM for control of the $3\phi - 3\phi$ matrix converter are performed. Finally, a simple geometric representation in the complex plane of the modulation process is given.

3.4.1 VSI Output Voltage SVM

Consider the VSI part of the circuit in figure 3.2 as a stand-alone VSI supplied by dc voltage source, $v_{pn} = V_{dc}$. The VSI switches can assume only six allowed combinations which yield nonzero output voltages, and two combinations with zero output voltage. Hence, the resulting output line-voltage space vector defined by

$$\mathbf{v}_{oL} = \frac{2}{3} \cdot (v_{AB} + v_{BC} \cdot e^{+j120^\circ} + v_{CA} \cdot e^{-j120^\circ}) \quad (3.30)$$

can assume only seven discrete values, $\mathbf{V}_0 - \mathbf{V}_6$ in figure 3.3, called output voltage switching state vectors (SSV's). The space vector of the desired output line voltages

$$\bar{\mathbf{v}}_{oL} = \sqrt{3} \cdot V_{om} \cdot e^{j(\omega_o t - \varphi_o + 30^\circ)} \quad (3.31)$$

can be approximated by two adjacent SSV's, $\mathbf{V}_\alpha$ and $\mathbf{V}_\beta$, and the zero voltage vector, $\mathbf{V}_0$, using PWM as shown in figure 3.3, where $\bar{\mathbf{V}}_{oL}$ is the sampled value of $\bar{\mathbf{v}}_{oL}$ at an instant

Figure 3.3: Output voltage vectors in SVM hexagon

within the switching cycle T_s . Using the law of sines, the duty cycles of the SSV's are

$$\begin{aligned}
 d_\alpha &= T_\alpha / T_s = m_v \cdot \sin(60^\circ - \theta_O) \\
 d_\beta &= T_\beta / T_s = m_v \cdot \sin(\theta_O) \\
 d_{0v} &= T_{0v} / T_s = 1 - d_\alpha - d_\beta
 \end{aligned} \tag{3.32}$$

where m_v is the VSI modulation index

$$0 \leq m_v = \left(\sqrt{3} \cdot V_{om} \right) / V_{dc} \leq 1 \tag{3.33}$$

The sectors of the VSI hexagon in figure 3.3 correspond directly to the six 60° segments within a period of the desired 3ϕ output line voltages shown in figure 3.4. The local

Figure 3.4: Output line voltage 60° segments

averaged output line voltages are

$$\begin{bmatrix} \bar{v}_{AB} \\ \bar{v}_{BC} \\ \bar{v}_{CA} \end{bmatrix} = \begin{bmatrix} d_\alpha + d_\beta \\ -d_\alpha \\ -d_\beta \end{bmatrix} \cdot V_{dc} = m_v \cdot \begin{bmatrix} \cos(\theta_O - 30^\circ) \\ -\sin(60^\circ - \theta_O) \\ -\sin(\theta_O) \end{bmatrix} \cdot V_{dc} \quad (3.34)$$

For the first 60° segment

$$\begin{aligned} -30^\circ \leq \omega_o t - \varphi_o + 30^\circ \leq 30^\circ \quad \text{and} \\ \theta_O = (\omega_o t - \varphi_o + 30^\circ) + 30^\circ \end{aligned} \quad (3.35)$$

By substitution of (3.35) into (3.34)

$$\begin{bmatrix} \bar{v}_{AB} \\ \bar{v}_{BC} \\ \bar{v}_{CA} \end{bmatrix} = m_v \cdot \begin{bmatrix} \cos(\omega_o t - \varphi_O + 30^\circ) \\ \cos(\omega_o t - \varphi_O + 30^\circ - 120^\circ) \\ \cos(\omega_o t - \varphi_O + 30^\circ + 120^\circ) \end{bmatrix} \cdot V_{dc} = \bar{\mathbf{T}}_{VSI} \cdot V_{dc} \quad (3.36)$$

The matrix $\bar{\mathbf{T}}_{VSI}$, defined in (3.36), is the LF transfer matrix of the VSI. Substituting the modulation index from (3.33) in (3.36), the desired output line voltage (3.17) are

obtained. The VSI local-averaged input current is determined as

$$\bar{i}_p = \bar{\mathbf{T}}_{\text{VSI}}^T \cdot \mathbf{i}_{oL} = \frac{\sqrt{3}}{2} \cdot I_{om} \cdot m_v \cdot \cos(\varphi_L) = \text{const.} \quad (3.37)$$

3.4.2 VSR Input Current SVM

Figure 3.5: Input current vectors in SVM hexagon

Consider the VSR part of the circuit in figure 3.2 as a stand-alone VSR loaded by a dc current generator, $i_p = I_{dc}$. The VSR input-current SVM is completely analogous to the VSI output-voltage SVM. The VSI subscripts α and β are replaced with the VSR subscripts γ and δ respectively. The VSR hexagon is shown in figure 3.5. The VSR duty cycles are

$$\begin{aligned} d_\gamma &= T_\gamma / T_s = m_c \cdot \sin(60^\circ - \theta_I) \\ d_\delta &= T_\delta / T_s = m_c \cdot \sin(\theta_I) \\ d_{0c} &= T_{0c} / T_s = 1 - d_\gamma - d_\delta \end{aligned} \quad (3.38)$$

where m_c is the VSR modulation index

$$0 \leq m_c = I_{im}/I_{dc} \leq 1 \quad (3.39)$$

Examples of the local-averaged input phase current, for a switching cycle within the first sector of the VSR hexagon, are

$$\begin{bmatrix} \bar{i}_a \\ \bar{i}_b \\ \bar{i}_c \end{bmatrix} = \begin{bmatrix} d_\gamma + d_\delta \\ -d_\gamma \\ -d_\delta \end{bmatrix} \cdot I_{dc} = m_c \cdot \begin{bmatrix} \cos(\theta_I - 30^\circ) \\ -\sin(60^\circ - \theta_I) \\ -\sin(\theta_I) \end{bmatrix} \cdot I_{dc} \quad (3.40)$$

By substitution of

$$\theta_I = (\omega_i t - \varphi_i) + 30^\circ, \quad -30^\circ \leq \omega_i t - \varphi_i \leq +30^\circ \quad (3.41)$$

for the first sector in (3.40), the LF transfer matrix of the VSR, $\bar{\mathbf{T}}_{\text{VSR}}$, is defined as

$$\begin{bmatrix} \bar{i}_a \\ \bar{i}_b \\ \bar{i}_c \end{bmatrix} = m_c \cdot \begin{bmatrix} \cos(\omega_i t - \varphi_i) \\ \cos(\omega_i t - \varphi_i - 120^\circ) \\ \cos(\omega_i t - \varphi_i + 120^\circ) \end{bmatrix} \cdot I_{dc} = \bar{\mathbf{T}}_{\text{VSR}} \cdot I_{dc} \quad (3.42)$$

Replacing the modulation index from (3.39) in (3.42), the desired input phase current (3.21) are obtained. The VSR local-averaged output voltage is determined as

$$\bar{v}_{pn} = \bar{\mathbf{T}}_{\text{VSR}}^T \cdot \mathbf{v}_{iPh} = \frac{3}{2} \cdot m_c \cdot V_{im} \cdot \cos(\varphi_i) = \text{const.} \quad (3.43)$$

3.4.3 Entire Matrix Converter Modulation

As the local-averaged output voltage of the SVM VSR, (3.43), and the local-averaged input current of the SVM VSI, (3.37), are constant, from the local-averaged point of view the SVM VSR and the SVM VSI can be directly connected. Substituting $\bar{v}_{pn}$ from (3.43) for V_{dc} in (3.36) and using $\bar{\mathbf{T}}_{\text{VSR}}$ from (3.42), the same expression for the LF transfer matrix of the $3\phi - 3\phi$ matrix converter is obtained as (3.18) with $m = m_v \cdot m_c$.

For simplicity, it is convenient to choose $m_c = 1$ and $m = m_v$. This completes the first step of the HF-synthesis procedure.

In the second step of the HF-synthesis procedure, the modulation algorithm is derived from the LF transfer matrix (3.18) in the same way as for the SVM VSI, (3.34)-(3.36), and SVM VSR, (3.40)-(3.42), only in the opposite direction. Since both the VSI and the VSR hexagons contain six sectors, there are $6 \times 6 = 36$ combinations or operation modes. If at a particular instant, the first output-voltage 60° segment and the first input-current 60° segment are active, then by using (3.35) and (3.41), the LF transfer matrix (3.18) becomes

$$\bar{\mathbf{T}}_{\text{PhL}} = m \cdot \begin{bmatrix} \cos(\theta_O - 30^\circ) \\ -\sin(60^\circ - \theta_O) \\ -\sin(\theta_O) \end{bmatrix} \cdot \begin{bmatrix} \cos(\theta_I - 30^\circ) \\ -\sin(60^\circ - \theta_I) \\ -\sin(\theta_I) \end{bmatrix}^T \quad (3.44)$$

Substituting (3.32) and (3.38) in (3.44), with $m = m_v \cdot m_c$, the local-averaged output line-voltages from (3.10) are

$$\begin{bmatrix} \bar{v}_{AB} \\ \bar{v}_{BC} \\ \bar{v}_{CA} \end{bmatrix} = \begin{bmatrix} d_\alpha + d_\beta \\ -d_\alpha \\ -d_\beta \end{bmatrix} \cdot \begin{bmatrix} d_\gamma + d_\delta \\ -d_\gamma \\ -d_\delta \end{bmatrix}^T \cdot \begin{bmatrix} v_{a0} \\ v_{b0} \\ v_{c0} \end{bmatrix} \quad (3.45)$$

Using

$$v_{ab} = v_{a0} - v_{b0} \quad \text{and} \quad v_{ac} = v_{a0} - v_{c0} \quad (3.46)$$

it is finally obtained

$$\begin{bmatrix} \bar{v}_{AB} \\ \bar{v}_{BC} \\ \bar{v}_{CA} \end{bmatrix} = \begin{bmatrix} d_{\alpha\gamma} + d_{\beta\gamma} \\ -d_{\alpha\gamma} \\ -d_{\beta\gamma} \end{bmatrix} \cdot v_{ab} + \begin{bmatrix} d_{\alpha\delta} + d_{\beta\delta} \\ -d_{\alpha\delta} \\ -d_{\beta\delta} \end{bmatrix} \cdot v_{ac} \quad (3.47)$$

where

$$d_{\alpha\gamma} = d_\alpha \cdot d_\gamma = m \cdot \sin(60^\circ - \theta_O) \cdot \sin(60^\circ - \theta_I) = T_{\alpha\gamma}/T_s,$$

$$\begin{aligned}
d_{\beta\gamma} &= d_{\beta} \cdot d_{\gamma} = m \cdot \sin(\theta_O) \cdot \sin(60^\circ - \theta_I) = T_{\beta\gamma}/T_s, \\
d_{\alpha\delta} &= d_{\alpha} \cdot d_{\delta} = m \cdot \sin(60^\circ - \theta_O) \cdot \sin(\theta_I) = T_{\alpha\delta}/T_s, \\
d_{\beta\delta} &= d_{\beta} \cdot d_{\delta} = m \cdot \sin(\theta_O) \cdot \sin(60^\circ - \theta_I) = T_{\beta\delta}/T_s
\end{aligned} \tag{3.48}$$

As can be seen, the output line voltages are synthesized inside each switching cycle from samples of two input line voltages, v_{ab} and v_{ac} for the above example. By comparison of (3.47) and (3.34), it can be concluded that simultaneous output-voltage and input-current SVM can be obtained by employing the standard VSI SVM sequentially in two VSI-subtopologies of the $3\phi - 3\phi$ matrix converter. When the standard VSI SVM is applied in the first VSI-subtopology, where $v_{pn} = v_{ab}$, the duty cycles of the two adjacent voltages SSV's are $d_{\alpha\gamma}$ and $d_{\beta\gamma}$, as defined in (3.48). The standard VSI SVM in the second VSI-subtopology, with $v_{pn} = v_{ac}$, results in the SSV duty cycles $d_{\alpha\delta}$ and $d_{\beta\delta}$, also defined in (3.48). During the remaining part of the switching cycle

$$d_0 = 1 - d_{\alpha\gamma} - d_{\beta\gamma} - d_{\alpha\delta} - d_{\beta\delta} = T_0/T_s \tag{3.49}$$

the output line voltages are equal to zero, by employing a zero SSV. It is easily verified that with (3.43), the conditions (3.8) and (3.9) are also satisfied. The duty cycle expressions (3.48) remain the same for all operating modes. This completes the second step of the HF-synthesis procedure.

In the third step, a switching sequence within one switching cycle is defined. This requires decisions on which of the three switching combinations from Group III in Table (3.1) is used for the zero SSV, and on how the five switching combinations are ordered within the switching cycle. Among the possible combinations, those which require switches to change state only once during a switching cycle should be used. For example, the switching sequence $d_{\alpha\gamma} \rightarrow d_{\beta\gamma} \rightarrow d_{\beta\delta} \rightarrow d_{\alpha\delta} \rightarrow d_0$ is used, and the optimum zero SSV is chosen for each of the 36 operation modes. The input phase currents, for the

above example, are synthesized according to the following:

$$\begin{bmatrix} \bar{i}_a \\ \bar{i}_b \\ \bar{i}_c \end{bmatrix} = \begin{bmatrix} d_{\alpha\gamma} \\ -d_{\alpha\gamma} \\ 0 \end{bmatrix} \cdot (-i_B) + \begin{bmatrix} d_{\beta\gamma} \\ -d_{\beta\gamma} \\ 0 \end{bmatrix} \cdot i_A + \begin{bmatrix} d_{\beta\delta} \\ 0 \\ -d_{\beta\delta} \end{bmatrix} \cdot i_A + \begin{bmatrix} d_{\alpha\delta} \\ 0 \\ -d_{\alpha\delta} \end{bmatrix} \cdot (-i_B) \quad (3.50)$$

A particular set of five switching combinations is selected, depending on the actual operating mode. By simultaneous observation of the desired LF voltage vector in the matrix converter inverter hexagon, and desired LF current vector in the matrix converter rectifier hexagon (see figure 3.3 and figure 3.5), the matrix converter SVM procedure can be easily followed. Note that the desired LF current vector magnitude (3.22) is equal to the local-averaged input current of the fictitious VSI, (3.37), because $m = m_v$.

Table 3.2: Switching sequence example

SSV Pair	Switching Combination p n A B C	ON Time	Output Line Voltage			Input Phase Current		
			V_{AB}	V_{BC}	V_{CA}	i_a	i_b	i_c
$\mathbf{I}_6 - \mathbf{V}_6$	a b a b a	$d_{\alpha\gamma} \cdot T_s$	V_{ab}	$-V_{ab}$	0	$-i_B$	i_B	0
$\mathbf{I}_6 - \mathbf{V}_1$	a b a b b	$d_{\beta\gamma} \cdot T_s$	V_{ab}	0	$-V_{ab}$	i_A	$-i_A$	0
$\mathbf{I}_1 - \mathbf{V}_1$	a c a c c	$d_{\beta\delta} \cdot T_s$	V_{ac}	0	$-V_{ac}$	i_A	0	$-i_A$
$\mathbf{I}_1 - \mathbf{V}_6$	a c a c a	$d_{\alpha\delta} \cdot T_s$	V_{ac}	$-V_{ac}$	0	$-i_B$	0	i_B
$\mathbf{I}_0 - \mathbf{V}_0$	a a a a a	$d_0 \cdot T_s$	0	0	0	0	0	0

For example, if at an instant $\bar{\mathbf{v}}_{oL}$ is in the first sector of the matrix converter inverter hexagon, the actual voltage SSV's are $\mathbf{V}_\alpha = \mathbf{V}_6$ and $\mathbf{V}_\beta = \mathbf{V}_1$; and if $\bar{\mathbf{i}}_{iPh}$ is in the first sector of the matrix converter rectifier hexagon, the actual current SSV's are $\mathbf{V}_\gamma = \mathbf{V}_6$ and $\mathbf{V}_\delta = \mathbf{V}_1$. Voltage-current SSV pair are applied in the following sequence: $\mathbf{I}_6 - \mathbf{V}_6$, $\mathbf{I}_6 - \mathbf{V}_1$, $\mathbf{I}_1 - \mathbf{V}_1$, $\mathbf{I}_1 - \mathbf{V}_6$, and $\mathbf{I}_0 - \mathbf{V}_0$. To each voltage-current SSV pair, there corresponds a switching combination with the on-time determined by (3.48), as shown in Table 3.2. For example, while applying $\mathbf{I}_6$, it follows from figure 3.5 that $p = a$ and $n = b$. With simultaneous application of $\mathbf{V}_6$, from figure 3.3, $A = p$, $B = n$, $C = p$. Therefore, the voltage-current SSV pair $\mathbf{I}_6 - \mathbf{V}_6$ is realized with the switching combination $A = a$, $B = b$, and $C = a$, which is kept ON for the time interval $d_{\alpha\gamma} \cdot T_s$. On-times of the individual matrix converter switches can be determined from table 3.2. The table also shows the resulting output line-voltages and input phase-currents. Figure 3.6 shows

the switching time distribution within one switching cycle based on the computation results of (3.48) and (3.49). In order to achieve lower input-output ripple performance, the four switching time segments are halved into eight time segments and distributed symmetrically around zero vector time to form double-sided vector sequence of nine-step switching modulation as shown in figure 3.7.

Figure 3.6: 5-step switching time diagram

Figure 3.7: 9-step switching time diagram

3.5 Optimized Space Vector Modulation

The standard nine-step modulation mentioned in the above section can also be illustrated in Table 3.3 where $\bar{\mathbf{v}}_{oL}$ is in the first sector of the matrix converter inverter hexagon while

$\bar{\mathbf{i}}_{iPh}$ is in the second sector of the matrix converter rectifier hexagon. We can see that there are only one switch status change during each step and a total of eight switchings during a whole vector sequence.

Table 3.3: Standard double-sided vector sequence

$\gamma\alpha$	$\gamma\beta$	$\delta\beta$	$\delta\alpha$	0	$\delta\alpha$	$\delta\beta$	$\gamma\beta$	$\gamma\alpha$
<i>aca</i>	<i>acc</i>	<i>bcc</i>	<i>bcb</i>	<i>bbb</i>	<i>bcb</i>	<i>bcc</i>	<i>acc</i>	<i>aca</i>

Unfortunately, some exceptions will occur to the nine-step switching modulation mentioned in the above paragraph, when $\bar{\mathbf{v}}_{oL}$ is in the first sector of the matrix converter inverter hexagon while $\bar{\mathbf{i}}_{iPh}$ is in the second sector of the matrix converter rectifier hexagon. It is seen from Table 3.4 that the vector sequence is now realized by ten switchings, which

Table 3.4: Non-optimized standard double-sided vector sequence

$\gamma\alpha$	$\gamma\beta$	$\delta\beta$	$\delta\alpha$	0	$\delta\alpha$	$\delta\beta$	$\gamma\beta$	$\gamma\alpha$
<i>aba</i>	<i>abb</i>	<i>acc</i>	<i>aca</i>	<i>aaa</i>	<i>aca</i>	<i>acc</i>	<i>abb</i>	<i>aba</i>

is two more than the previous minimum one. The increased number of switchings are caused by the shift between the second $\gamma\beta$ and the third $\delta\beta$ vector of the sequence. Two switchings are needed for this operation instead of one. As the sequence is repeated in the opposite direction, the double-switching occurs twice in the sequence.

Table 3.5: Optimized double-sided vector sequence

$\gamma\beta$	$\gamma\alpha$	$\delta\alpha$	$\delta\beta$	0	$\delta\beta$	$\delta\alpha$	$\gamma\alpha$	$\gamma\beta$
<i>abb</i>	<i>aba</i>	<i>aca</i>	<i>acc</i>	<i>ccc</i>	<i>acc</i>	<i>aca</i>	<i>aba</i>	<i>abb</i>

In order to obtain a desired output, and simultaneously minimizing the switching numbers in a sampling period, the optimized ISV-PWM (indirect space vector modulation) method was proposed [36]. It changes the output voltage vector sequence according to whether the sum of the input and output switching hexagon sector is even or odd. By changing the output vector sequence from $\alpha\beta\beta\alpha 0$ to $\beta\alpha\alpha\beta 0$, and at the same time choose the zero vector *ccc* instead of *aaa*, the sequence can be realized by eight switchings, which is the minimum. This is shown in Table 3.5 as the optimized vector sequence.

Analyzing all 36 combinations of input and output hexagon sectors, leads to the following

strategy for composing the vector sequence to obtain the minimum number of switchings in all cases:

- The input current modulation vector sequence is always $\gamma\delta 0$;
- When the sum of the input and output hexagon sectors is even, the output vector sequence must be $\alpha\beta\beta\alpha 0$;
- When the sum of the input and output hexagon sectors is odd, the output vector sequence must be $\beta\alpha\alpha\beta 0$;
- The zero vector should be chosen according to having only one switching change from the previous vector;

This method will slightly increase in complexity of the modulation, but the average number of switchings per cycle will always be eight, while the total switching number will be reduced in comparison to conventional vector sequence.

3.6 Concluding Remarks

In this chapter, traditional control and design methods of the $3\phi-3\phi$ matrix converter are described. The $3\phi-3\phi$ matrix converter output-voltage and input-current space vector modulation algorithms are systematically reviewed. A simple geometric representation in complex plane of the $3\phi-3\phi$ matrix converter space vector modulation procedure is given. This systematic approach enables a clear comprehension of the modulation algorithm.

After analysis of the matrix converter input and output transfer functions, the indirect transfer function approach for matrix converter modulation is derived. The indirect transfer function approach emulates a VSR-VSI conversion, and enables application of the well-known standard VSR and VSI PWM techniques for matrix converter control.

An optimized space vector switching sequence combination can help to reduce the total switching number to a minimum, by mean of revising the switching sequence according

to certain input and output sector combination. After having adopted this method, the average number of switchings per cycle will always be eight, with only a slight increase in complexity of the modulation process.

Chapter 4

Hysteresis Current Control Strategies for Matrix Converter

4.1 Introduction

From the description in the previous chapter, we notice that the SVM-based matrix converter modulation needs to pre-calculate the duty cycle for each switching sequence, and apply these switching sequences to generate the desired output line voltage. And for AC machine drive application, the pulse-width-modulated (PWM) voltage control is usually associated with the stator current control because the current is directly related to the developed torque of a machine. A PWM voltage controlled converter may have either a scalar or a vector current control in its outer loop. A scalar current control may be adequate for a simple low-performance drive system. In the high-performance vector or field-oriented current control systems, the torque and flux components are decoupled so that independent torque and flux control are possible as in DC machines. Therefore, the current controller has direct influence on the drive performance and its design requires particular considerations. The basic requirements for the current controller are fast dynamic response during transient state, optimal switching pattern and low current ripple in the steady state, maximum current limit, and stable performance under variations of load parameters such as $R - L$ impedances and operating conditions. The

current control for traditional voltage source inverter (VSI) can be achieved by means of three major techniques: predictive and deadbeat current control method [39–42], ramp comparison technique [43], and hysteresis current control method [44–61].

Predictive control involves the selection of the optimum space vector voltage to be applied to the motor at any instant, to force the motor currents to follow an optimum trajectory. This gives excellent current control when the load torque profile is known before-hand, since the stator current trajectory can then be pre-determined. But it is complex to implement, requires good knowledge of the motor parameters, has relatively poor transient performance, and does not provide implicit current limiting.

Ramp-comparison techniques are based on an asynchronous PWM technique with the error between the reference and the measured current acting as the modulating function. They offer the particular advantage of a constant inverter switching frequency, but the system response can be affected by the stability requirements of the current feed-back loop which in turn depend on motor parameters. Also there can be a time delay between reference current changes and the implementation of corrective switching action by the current controller, which limits its transient performance.

Hysteresis current control is probably one of the simplest technique used to control the phase currents for high speed drive systems, primarily because of its ease of implementation, fast current control response, and inherent peak current limiting capability. The basic concept is to switch each phase leg to the opposite voltage polarity whenever the measured current goes above or below a given boundary.

4.2 The Basic Hysteresis Current Controller

A block diagram of the basic hysteresis current controller is shown in figure 4.1. A hysteresis comparator is used to compare the reference signal with the feedback of the output signal to generate the output pulses (please refer to figure 4.2). The feedback current I is compared with the reference current I_{ref} to derive the current error ΔI and feed the current error to the hysteresis comparator. Based on the digital output

Figure 4.1: The basic hysteresis current controller diagram

Figure 4.2: Waveforms associated to the basic hysteresis current controller diagram

of the hysteresis comparator, the appropriate switches are gated in order to make the output current traces its reference current within the hysteresis band. For example, when the feedback current signal increases until it reaches beyond the upper boundary $I_{ref} + H$, the digital output of the hysteresis comparator will change to E , which makes the output current decreases towards the lower boundary $I_{ref} - H$. When the feedback current signal reaches the lower boundary $I_{ref} - H$, the digital output of the hysteresis comparator will change to $-E$, and this will cause the output current to revert back towards the upper boundary $I_{ref} + H$. This cycle will be repeated at a certain frequency.

It can be concluded that the hysteresis current controller is actually a forced oscillator that produces limit cycles in the absence of an input reference signal. The typical waveforms that are associated with the basic hysteresis current controller when driven by a sinusoidal reference signal are shown in figure 4.2. Notice that the feedback signal is actually tracking the sinusoidal reference signal within a certain margin of error, which is termed as the hysteresis band. The boundaries of the hysteresis band are marked by $\pm H$.

4.3 Mathematical Model for Current Controllers in The Complex Plane

From figure 3.2 we can assume that the basic circuit of a matrix converter is feeding a Y -connected, three phase load, where the load is modelled by phase resistances, inductances and induced voltages. The equation of the Y -connected, three phase load is expressed as follow

$$\mathbf{V}_o = \mathbf{R} \cdot \mathbf{i} + \mathbf{L} \cdot \frac{d\mathbf{i}}{dt} + \mathbf{E} \quad (4.1)$$

where

$$\mathbf{V} = \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix}; \mathbf{i} = \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix}; \mathbf{E} = \begin{bmatrix} E_A \\ E_B \\ E_C \end{bmatrix}; \mathbf{L} = \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & L \end{bmatrix}; \mathbf{R} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix};$$

and the three phase balanced output currents satisfy the linear constraint

$$i_A + i_B + i_C = 0 \quad (4.2)$$

The current control problem is the tracking of the three phase current reference signal. For hysteresis current control, the difference between the reference and the actual current can be defined as

$$\mathbf{i}_e = \mathbf{i}_{ref} - \mathbf{i} \quad (4.3)$$

Substitute (4.3) into (4.1) gives

$$\mathbf{L} \cdot \frac{d\mathbf{i}_e}{dt} = \mathbf{L} \cdot \frac{d\mathbf{i}_{ref}}{dt} + \mathbf{R} \cdot \mathbf{i} + \mathbf{E} - \mathbf{V}_o \quad (4.4)$$

If the ideal reference current $\mathbf{i}_{ref}$ is assumed to flow through the three phase load, then the fictitious desired phase voltage $\mathbf{V}_{ref}$ is given by

$$\mathbf{V}_{ref} = \mathbf{L} \cdot \frac{d\mathbf{i}_{ref}}{dt} + \mathbf{R} \cdot \mathbf{i}_{ref} + \mathbf{E} \quad (4.5)$$

So equation (4.4) will become

$$\mathbf{L} \cdot \frac{d\mathbf{i}_e}{dt} = \mathbf{R} \cdot \mathbf{i}_e + \mathbf{V}_{ref} - \mathbf{V}_o \quad (4.6)$$

Equation (4.6) can be simplified by neglecting $\mathbf{R} \cdot \mathbf{i}_e$

$$\mathbf{L} \cdot \frac{d\mathbf{i}_e}{dt} = \mathbf{V}_{ref} - \mathbf{V}_o \quad (4.7)$$

In order to represent the three phase voltage and current components in the $\alpha - \beta$ stationary coordinate system, the standard transformation to the two phase equivalent system is determined by the matrix

$$\mathbf{C} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \quad (4.8)$$

By defining $\mathbf{i}_{e\alpha\beta} = \mathbf{C} \cdot \mathbf{i}_e$, $\mathbf{V}_{ref\alpha\beta} = \mathbf{C} \cdot \mathbf{V}_{ref}$, $\mathbf{V}_{o\alpha\beta} = \mathbf{C} \cdot \mathbf{V}_o$, (4.7) becomes

$$\mathbf{L} \frac{d\mathbf{i}_{e\alpha\beta}}{dt} = \mathbf{V}_{ref\alpha\beta} - \mathbf{V}_{o\alpha\beta} \quad (4.9)$$

Figure 4.3: Voltage vector selection

From figure 4.3 we can see that, the matrix converter VSI output voltage vector hexagon has eight space vectors. Two vectors $V_0 = (p, p, p) \text{ or } (n, n, n)$ correspond to zero amplitude voltage vectors, while the other six vectors have constant amplitude but different space orientations. So the equivalent space vector representation can be expressed as

$$\mathbf{L} \frac{d\vec{\mathbf{i}}_e}{dt} = \vec{\mathbf{V}}_{ref} - \vec{\mathbf{V}}_k \quad (4.10)$$

Equation (4.10) shows that the current error evolves in the same direction of $(\vec{\mathbf{V}}_{ref} - \vec{\mathbf{V}}_k)$. In order to achieve low harmonic currents in the steady state, we should only apply those

output space vectors $\vec{V}_k$ adjacent to $\vec{V}_{ref}$, as shown in figure 4.3.

According to equation (4.10) and figure 4.3, when voltage reference is located in section II of the voltage vector hexagon, in order to achieve low harmonic currents in the steady state, one should only apply the three voltage vectors of V_1 , V_2 , and V_0 to produce low differences in $\vec{V}_{ref} - \vec{V}_k$ (dashed lines in figure 4.3) and thus low harmonics. These vectors are called optimum voltage vectors. This is similar to the SVM matrix technique, which utilizes three space vectors V_α , V_β , and V_0 to generate the output voltage vector $\mathbf{V}_o^*$ (as shown in figure 3.3). If quick current response is required in the transient mode such voltage vectors should be applied which produce large differences in $\vec{V}_{ref} - \vec{V}_k$. This will force the current to track as fast as possible to its new reference value, as shown in figure 4.3 as the dotted lines (the non adjacent voltage vectors V_3 , V_4 , V_5 , and V_6 as shown in figure 4.3).

4.4 Hysteresis Current Controller Working in $\alpha - \beta$ Stationary Coordinate

A simple but good current control scheme in the $\alpha - \beta$ stationary coordinate system for traditional voltage source inverter was first presented in [51]. This control scheme uses two three-level comparators together with a switching table to make the output current track the current reference within the hysteresis band. Every change of a comparator output makes the corresponding component of the output voltage step change in the desired direction. The detailed description for applying this strategy to modulate the output current of the matrix converter will be shown in the following paragraphs.

The proposed matrix converter current control diagram is shown in figure 4.4. For full control of the matrix converter system using hysteresis current controller, we also need to divide the matrix converter system into VSR-VSI equivalent systems as shown in figure 3.2. For the VSR part of the matrix converter, the SVM PWM rectifier modulation is performed with the modulation index m_c set to unity, in order to provide the VSI part with the maximum fictitious DC-link voltage. There exist only six non-zero space

vectors and three zero space vectors at the DC output of the matrix converter VSR component $v_{pn} = (v_{ab}, v_{bc}, v_{ca}, v_{ba}, v_{ca}, v_{ac}, v_{aa}, v_{bb}, v_{cc})$ shown in figure 3.5, generated from PWM rectifier, and then apply appropriate v_{pn} to the VSI component of the matrix converter.

Figure 4.4: The SVM based matrix converter hysteresis current control system

For the VSI component of the matrix converter, the system samples three phase currents from the output side, and converts the three phase quantities into $\alpha - \beta$ stationary coordinate quantities based on equation (4.11).

$$\vec{X} = X_\alpha + jX_\beta = 2/3 \cdot (x_A + x_B \cdot e^{+j120^\circ} + x_C \cdot e^{-j120^\circ}) \quad (4.11)$$

The derived output currents i_α and i_β are then feedback to the system and compared with the reference current signals $i_{\alpha ref}$ and $i_{\beta ref}$ to get the current error signals. Two three-level hysteresis comparators for the α and β components of the current signals are implemented. Accuracy of the current formations is determined by the width of hysteresis zone of the three-level comparators. The practical implementation of the three-level hysteresis comparator is shown in figure 4.5. According to the digital outputs of the comparators, the appropriate VSI switches are selected from the VSI switching table in order to keep the current error inside the hysteresis band.

Figure 4.5: Three level hysteresis comparator

To understand the working principle of the hysteresis current controller, it is necessary to compare the mutual positions of the voltage vectors and the limits of the current error area (figure 4.6). This comparison points out: if the outputs of both comparators are in

Figure 4.6: VSI output voltage vector position and current error band

Table 4.1: Switching logic for three-level hysteresis controller

$d_\beta \backslash d_\alpha$	1	0	-1
1	V_1	V_2	V_3
0	V_1 or V_6	V_0	V_3 or V_4
-1	V_6	V_5	V_4

the active state (1 or -1) then the output voltage vector is exactly defined; if one of the comparator outputs takes non-active state (zero level) the second one makes a choice of the output voltage vector; if both comparators have the zero state then the zero vector is applied to the load. The switching table is defined in Table 4.1.

A detailed analysis of the above scheme shows the following properties:

- The zero states V_0 and V_7 are applied systematically, which helps to reduce the switching frequency. The state V_0 is chosen when coming from V_1 , V_3 , V_5 , and the state V_7 is chosen when coming from V_2 , V_4 , V_6 because in these cases only one

inverter leg has to be switched at any instant. In this way, the switching frequency is further reduced.

- The control of the β -component is independent from the α -component. If $d_\alpha = 1$ and $d_\beta = 1$, then state V_1 is applied. If $d_\alpha = -1$ and $d_\beta = -1$, then state V_4 is applied. If $d_\alpha = 1$ and $d_\beta = -1$, then state V_6 is applied. If $d_\alpha = -1$ and $d_\beta = 1$, then state V_3 is applied.
- For $d_\alpha = 1$ and $d_\beta = 0$, two states are equivalent (V_1 and V_6). And for $d_\alpha = -1$ and $d_\beta = 0$, there are also two equivalent states (V_3 and V_4).

A particular set of switching combination is selected at each moment, depending on the actual operational mode. By simultaneously combining VSR and VSI switching sequences, the total desired switching combination for the matrix converter is obtained, as shown in Table 4.2 in the case of VSR output ($p = a$) and ($n = b$). For example if ($p = a$) and ($n = b$) and VSI output is $V_3 = (A = n, B = p, \text{ and } C = n)$, then the actual matrix converter switching combination is realized as $A = b, B = a, \text{ and } C = b$. Because this kind of VSR and VSI sub-topology has already been well defined in [3], so this kind of switching combination for the whole matrix converter will not break the basic rules for the proper operation of the matrix converter, that is to avoid short circuit at the input side and to avoid open circuit at the output side.

Table 4.2: Matrix converter switching sequence example in the case of $v_{pn} = v_{ab}$

d_β d_α	VSI Output Vector	Switching combination p n A B C	Switching State $S_{Aa}S_{Ab}S_{Ac}$ $S_{Ba}S_{Bb}S_{Bc}$ $S_{Ca}S_{Cb}S_{Cc}$
-1 1	V_3	a b b a b	0 1 0 1 0 0 0 1 0
-1 0	V_3 or V_4	a b b a b or a b b a a	0 1 0 1 0 0 0 1 0 or 0 1 0 1 0 0 1 0 0
-1 -1	V_4	a b b a a	0 1 0 1 0 0 1 0 0
0 1	V_2	a b a a b	1 0 0 1 0 0 1 0 0
0 0	V_0	a b a a a or a b b b b	1 0 0 1 0 0 1 0 0 or 0 1 0 0 1 0 0 1 0
0 -1	V_5	a b b b a	0 1 0 0 1 0 1 0 0
1 1	V_1	a b a b b	1 0 0 0 1 0 0 1 0
1 0	V_1 or V_6	a b a b b or a b a b a	1 0 0 0 1 0 0 1 0 or 1 0 0 0 1 0 1 0 0
1 -1	V_6	a b a b a	1 0 0 0 1 0 1 0 0

4.5 Improved HCC Controller Working in $\alpha - \beta$ Stationary Coordinate

As discussed, in the three-level hysteresis comparator scheme, the inappropriate voltage vector may occur when d_β outputs zero state while d_α outputs nonzero state as shown in the second row of Table 4.1. For example, when the output voltage vector V_o is located in the sector II, and β current component exceeds the upper hysteresis band, the system needs to take the action that will draw β current back towards zero. So based on the

three-level hysteresis comparator output and switching table in Table 4.1, both V_1 and V_6 meet the requirement. However, according to figure 4.3 and equation (4.10), in this situation, only V_1 is the optimum switching vector that should be chosen in order to get a lower current ripple.

An optimized current controller can be used in order to more accurately determine which one is the optimum switching vector to be chosen, and does not need any other additional information. This kind of current controller can be constructed from one four-level hysteresis comparator and one three-level hysteresis comparator which were firstly utilized in traditional inverter [62]. The analysis of the optimized current control method is shown in figure 4.7.

Figure 4.7: Improved VSI voltage vector position and current error band

It has already been proven in [3] that, the fictitious DC link voltage v_{pn} is constant ($v_{pn} = 3/2 \cdot V_{im}$) during the VSR modulation of matrix converter, so the magnitudes of each of the six non-zero vectors in VSI sub-topology hexagon are also constant. The

Table 4.3: Switching logic for four-level hysteresis controller

$d_\beta \backslash d_\alpha$	$\frac{1}{\sqrt{3}}v_{pn}$	0	$-\frac{1}{\sqrt{3}}v_{pn}$
$\frac{2}{3}v_{pn}$	V_1	V_2	V_3
$\frac{1}{3}v_{pn}$	V_1	V_0	V_3
$-\frac{1}{3}v_{pn}$	V_6	V_0	V_4
$-\frac{2}{3}v_{pn}$	V_6	V_5	V_4

Figure 4.8: Four-level hysteresis comparator

complex plane of VSI voltage vector can be divided into different sectors as defined by the dashed lines in figure 4.7. In the α -axis it is possible to apply three different voltage levels $V_{d\alpha} = (-1/\sqrt{3} \cdot v_{pn}, 0, \text{ and } 1/\sqrt{3} \cdot v_{pn})$. In the β -axis it is possible to apply four different voltage levels $V_{d\beta} = (-2/3 \cdot v_{pn}, -1/3 \cdot v_{pn}, 1/3 \cdot v_{pn}, 2/3 \cdot v_{pn})$. The switching logic for four-level comparator is shown in Table 4.3. From figure 4.7 and Table 4.3, the switching sequence of the four-level hysteresis current controller and selection of the appropriate voltage vector is achieved according to different output combination of d_α

and d_β . When V_o is located in sector II, then only V_1 , V_2 , and V_0 are selected to regulate the current so that it does not exceed the inner hysteresis band. If V_o changes into sector III, the current will exceed the inner hysteresis band because at this moment the controller still applies those voltage vectors that belong to sector II. According to the structure of the hysteresis comparators, the action of leaving the inner band will cause a change of the comparator output and thus change to a new group of voltage vectors (such as V_2 , V_3 , and V_0) for the current controller and bring the current back into the current band. The practical implementation of the four-level hysteresis comparator is shown in figure 4.8.

Similar to the three-level HCC controller, the full control of the whole matrix converter system is achieved by combining the VSR output vectors and VSI output vectors together to generate the appropriate switching sequence for the matrix converter. And the theory of combination is the same as the three-level HCC controller.

4.6 Concluding Remarks

This chapter presents two novel space vector based hysteresis current control strategies for matrix converter. In order to apply hysteresis current control strategy to the modulation of the matrix converter, the indirect modulation method was adopted. The SVM PWM modulation was applied to the rectifying stage with modulation index equal to unity in order to provide the inverting stage with maximum fictitious DC-link voltage. And the HCC control technique was applied to the inverting stage. One of these two HCC controllers is based on three-level hysteresis comparator and the other is based on four-level hysteresis comparator. Both comparators select the appropriate space vector combinations via switching table including zero vector combination to reduce the switching frequency of the matrix converter and do not require complex calculations. Also, both regulators work with the current components represented in the $\alpha - \beta$ stationary coordinate system, and need only two multi-level comparators to achieve space vector selection. So these proposed controllers can help to further simplify the complexity of

the overall control circuit.

Chapter 5

Modeling of SVM and HCC Control Systems for Matrix Converter

5.1 Introduction

This chapter presents the implementation and verification of both the SVM control system and the proposed HCC control strategies for matrix converter in Matlab/Simulink simulation environment. The comparison of both systems is presented to illustrate their different performances in terms of output voltage, output and input currents and dynamic response.

With the evolution of powerful computers which are capable of executing hundreds of millions of calculations in a fraction of second, mathematical problems which were once very tedious to solve can now be tackled with great ease. These computers can now be used to solve complex mathematical problems, which arise from determining the operational condition of electronic circuits during simulation.

Simulation software is now a powerful tool when it comes to rapid prototyping; this is because a great deal of knowledge can be acquired before actually implementing the final prototype. Optimization of a given circuit performance can be carried out during the simulation stage. The time required to investigate circuit performance for different

component values is significantly reduced as compared to that of an actual circuit implementation. Testing of high voltage circuits can be hazardous to engineers, especially when the selection of an incorrect component may result in fatal results. With the availability of simulation software, such circuit can now be simulated to ensure proper and safe performance before actual implementation. In this situation, the ability to simulate the circuit can help to ensure safety during testing.

Matlab is built upon a foundation of sophisticated matrix software for analyzing complicated systems. The Simulink tools available in the simulation environment is an extension of Matlab. In addition, there are many control toolboxes available in Matlab/Simulink environment. In this research work, Matlab version 6.5.1 was utilized to investigate the performance of SVM and HCC control systems for matrix converter.

5.2 Simulation Model of SVM System

The matrix converter SVM control system diagram is shown in figure 5.1, and the system was simulated under open loop control. The reference output voltage was directly set and the modulation index was set to 0.5. The system samples three phase input voltages from the input side and converts the three phase quantities into single space vector representation. C language is used to program the kernel duty cycle calculation algorithm. Based on the location of the input current space vector and output reference voltage space vector in their hexagons, the system selects the appropriate switching sequences according to the specified switching tables and applies the calculated duty cycles to these switching sequences respectively before feeding them to the pulse width generator. The outputs of the pulse width generator represent gate signals for the bidirectional switches of the matrix converter. Also, the three phase output currents are detected from the output side, for the purpose of calculating output current direction and applying four-step commutation strategy for the bidirectional switches. This system was simulated with three phase balanced R - L load (11Ω , 27mH) and three phase balanced 380-V peak value, 50-Hz input utility. The three phase balanced input voltages are

shown in figure 5.2. At the input side, the parameters with 10Ω , 2mH , and $15\mu\text{F}$ R - L - C series input filter was chosen. The system switching frequency was set to 3000Hz .

Figure 5.1: Matrix converter SVM control diagram

Figure 5.2: Three phase balanced input voltage

5.2.1 Results Obtained

From the simulated steady-state waveforms shown in figure 5.3 to figure 5.14, we can see that the sinusoidal output currents with variable frequency are obtained at the output side, and sinusoidal input currents are obtained at the input side. Figure 5.3 to figure 5.8 are input and output waveforms obtained under 25Hz output condition. Figure 5.3 and figure 5.4 are the three phase output currents and FFT(Fast Fourier Transformation) waveforms respectively. The output current is fairly sinusoidal and the THD(total harmonic distortion) of the output current is 5.14%. The output line voltage and FFT waveforms are shown in figure 5.5 and figure 5.6 respectively. The three phase input currents and FFT waveforms are shown in figure 5.7 and figure 5.8 respectively with the input current being quite sinusoidal with $\text{THD} = 8.34\%$.

Figure 5.9 to figure 5.14 are input and output waveforms obtained under 80Hz output condition. Figure 5.9 and figure 5.10 are the three phase output currents and FFT waveforms respectively, the output current is quite sinusoidal and the total harmonic distortion of the output current is 3.16%. The output line voltage and FFT waveforms are shown in figure 5.11 and figure 5.12 respectively. The three phase input currents and FFT waveforms are shown in figure 5.13 and figure 5.14 respectively. The input current is quite sinusoidal with $\text{THD} = 8.63\%$. The reason for the magnitude of the output current and input current under 80Hz output condition being lower than those for 25Hz output condition is that under 80Hz output condition, the impedances of the input and output inductors are higher than that of 25Hz output condition based on the equation $Z_L = \omega \cdot L$. The results can also be summarized in Table 5.1.

Table 5.1: Simulation results of matrix converter SVM system under different output conditions

		25Hz	80Hz
Input current	Amplitude of fundamental (A)	11.88	5.87
	THD	8.34%	8.63%
Output current	Amplitude of fundamental (A)	15.36	8.03
	THD	5.14%	3.16%

Figure 5.3: Three phase output current of SVM system under 25Hz output condition

Figure 5.4: FFT of output current of SVM system under 25Hz output condition

Figure 5.5: Output line voltage of SVM system under 25Hz output condition

Figure 5.6: FFT of output line voltage of SVM system under 25Hz output condition

Figure 5.7: Three phase input current of SVM system under 25Hz output condition

Figure 5.8: FFT of input current of SVM system under 25Hz output condition

Figure 5.9: Three phase output current of SVM system under 80Hz output condition

Figure 5.10: FFT of output current of SVM system under 80Hz output condition

Figure 5.11: Output line voltage of SVM system under 80Hz output condition

Figure 5.12: FFT of output line voltage of SVM system under 80Hz output condition

Figure 5.13: Three phase input current of SVM system under 80Hz output condition

Figure 5.14: FFT of input current of SVM system under 80Hz output condition

5.3 Simulation Model of HCC systems

The proposed simulation diagram of matrix converter HCC controller in Matlab has already been shown in figure 4.4. The system sampled three phase input voltages to perform front-end SVM PWM rectifying stage calculation. Three phase output currents are sampled and converted into the $\alpha - \beta$ stationary coordinate representation and fed-back to the system. The feedback current signals are compared with their reference signals to generate current error signals that are fed to the multi-level comparators. Based on the digital outputs of the hysteresis comparators, the system selects the appropriate inverting voltage space vectors based on the switching table. Finally, the generated inverting voltage space vectors are combined with the rectifying space vectors to get the appropriate overall switching combinations that are applied to the matrix converter switches. In order to verify the feasibility of the proposed current controllers, and to make comparison with the SVM control system, the simulations were done with the same three phase balanced $R-L$ load (11Ω , 27mH) and three phase balanced 380-V peak value, 50-Hz utility.

5.3.1 Results Obtained From Three-Level HCC System

The simulated steady-state waveforms of three-level HCC system are shown in figure 5.15 to figure 5.24. Figure 5.15 and figure 5.16 are the three phase output currents and FFT waveforms respectively with the output current being quite sinusoidal with $\text{THD} = 1.54\%$. The output line voltage and FFT waveforms are shown in figure 5.17 and figure 5.18 respectively. Figure 5.19 and figure 5.20 are α current and β current with their references respectively. From these two figures we can see that the three-level HCC system can generate the desired α current and β current and can follow their reference values pretty well. Figure 5.21 shows the error area in stationary coordinates. The obtained inverting stage voltage vector is shown in figure 5.22. The three phase input currents and FFT waveforms are shown in figure 5.23 and figure 5.24 respectively. The input current is quite sinusoidal with $\text{THD} = 6.36\%$.

Figure 5.15: Three phase output current of three-level HCC system

Figure 5.16: FFT of output current of three-level HCC system

Figure 5.17: Output line voltage of three-level HCC system

Figure 5.18: FFT of output line voltage of three-level HCC system

Figure 5.19: Current waveform of i_α and i_α reference of three-level HCC system Figure 5.20: Current waveform of i_β and i_β reference of three-level HCC system

Figure 5.21: Error area of three-level HCC system in stationary coordinates

Figure 5.22: Obtained inverting stage voltage vector of three-level HCC system

Figure 5.23: Three phase input current of three-level HCC system

Figure 5.24: FFT of input current of three-level HCC system

5.3.2 Results Obtained From Four-Level HCC System

The simulated steady-state waveforms of four-level HCC system are shown in figure 5.25 to figure 5.34. Figure 5.25 and figure 5.26 are the three phase output currents and FFT waveforms respectively with the output current being quite sinusoidal and the total harmonic distortion of the output current being 1.08%. The output line voltage and FFT waveforms are shown in figure 5.27 and figure 5.28 respectively. Figure 5.29 and figure 5.30 are α current and β current with their references respectively. From these two figures we can see that four-level HCC system can generate the desired α current and β current that follow their reference values pretty well. Figure 5.31 shows the error area in stationary coordinates. The obtained inverting stage voltage vector is shown in figure 5.32. The three phase input currents and FFT waveforms are shown in figure 5.33 and figure 5.34 respectively, with the input current being sinusoidal and $\text{THD} = 6.33\%$. From figure 5.21 and figure 5.31 we can see that both kinds of comparators can force the current error trajectories within the specified band. And from figure 5.22 and figure 5.32 we can see that the four-level hysteresis comparator can obtain more optimum vectors than the three-level hysteresis comparator.

From figure 5.15 to figure 5.34, we can notice that, both of the proposed controllers can produce the desired output line voltage and good sinusoidal input and output currents

similar to SVM control techniques. The output line voltage spectrum generated is different from the spectrum of SVM system as shown in figure 5.6, figure 5.18, and figure 5.28. For the SVM system, because the switching frequency is defined as 3000 Hz, so from the spectrum of the SVM controller we can notice that the spectrum has harmonics concentration at 3000Hz, 6000Hz and 9000Hz. For the HCC systems, because the switching frequency is not fixed at a certain value, these spectral lines are spreaded over a relatively wide frequency range. The differences in these three controllers are summarized in Table 5.2 for 50Hz input and 25Hz output.

Table 5.2: Comparison of three kinds of controller at 50Hz input and 25Hz output

		SVM	Three-level HCC	Four-level HCC
Input current	Amplitude of fundamental (A)	11.88	12.74	12.65
	THD	8.34%	6.36%	6.33%
Output current	Amplitude of fundamental (A)	15.36	9.983	9.981
	THD	5.14%	1.54%	1.08%

Figure 5.25: Three phase output current of four-level HCC system

Figure 5.26: FFT of output current of four-level HCC system

Figure 5.27: Output line voltage of four-level HCC system

Figure 5.28: FFT of output line voltage of four-level HCC system

Figure 5.29: Current waveform of i_α and i_α reference of four-level HCC system Figure 5.30: Current waveform of i_β and i_β reference of four-level HCC system

Figure 5.31: Error area of four-level HCC system in stationary coordinates

Figure 5.32: Obtained inverting stage voltage vector of four-level HCC system

Figure 5.33: Three phase input current of four-level HCC system

Figure 5.34: FFT of input current of four-level HCC system

Because the four-level hysteresis comparator can more accurately determine the voltage vector as shown in Table 4.1 and Table 4.3, the switching frequency was reduced compared to that of the three-level hysteresis comparator. This result is clearly shown in figure 5.35 and figure 5.36: for the same time period of 0.16s, the three-level hysteresis comparator has a total number of 2710 switchings and the four-level hysteresis comparator has a total switching number of 2500 switchings, which means that the total number of switching of the four-level hysteresis controller in the period of 0.16s is 7.7% lower than that of the three-level hysteresis controller.

Figure 5.35: Number of switchings in period of 0.16s for three-level HCC system

Figure 5.36: Number of switchings in period of 0.16s for four-level HCC system

5.4 Results of Dynamic Behavior of SVM System and HCC System

As indicated before, in comparison to SVM control method, the HCC control method has the following advantages such as control of instantaneous current waveform with high accuracy, peak current protection, reduced computational overheads of the controller, and good dynamic behavior. The first three advantages have been shown in previous chapters and figures, and the advantage of good dynamic behavior will be shown in this section.

For the purpose of comparing the dynamic performance of both kinds of controllers, the amplitude of the output current is increased from 5A to 10A at the instant $t = 0.085$ s. For the SVM system, the change of output current amplitude is achieved by change of reference output voltage. While for the HCC system, the change of output current amplitude is achieved by changing the $\alpha - \beta$ reference current. The simulation results are shown in figure 5.37 to figure 5.39.

From figure 5.37 to figure 5.39 we can see that at the time of 0.085s the output current peak values changed from 5A to 10A. Figure 5.37, figure 5.38 and figure 5.39 depict the SVM system, the three-level HCC system, and the four-level HCC system dynamic behavior respectively. These figures verify that the HCC systems using the three-level or four-level comparators both have very fast dynamic response. The output currents of both HCC systems have changed from 5A to 10A in several milliseconds. But for the SVM system, the output current cannot change suddenly, it needs much longer transient to change the output current from 5A to 10A. These results prove that HCC system has faster dynamic behavior than SVM system.

Figure 5.37: Output current dynamic behavior of SVM system

Figure 5.38: Output current dynamic behavior of three-level HCC system

Figure 5.39: Output current dynamic behavior of four-level HCC system

5.5 Concluding Remarks

This chapter includes the simulation studies of indirect space vector modulation (SVM) system, three-level hysteresis current control (HCC) system, and four-level hysteresis current control system under Matlab/Simulink simulation environment.

The SVM system involves sampling three phase input voltages from the input side and converting them into single space vector representation. Duty cycles are calculated based on the sampled input space vector and reference output space vector. Based on the position of input and output space vectors in their respective hexagons, the system distributes the calculated duty cycles to form appropriate switching sequence based on the switching table and feeds into a pulse width generator. The outputs of the pulse width generator are gate signals for each IGBT, and are fed to the matrix converter plant. Simulation results of SVM system show that, output currents with variable frequency are obtained at the output side and sinusoidal input currents are derived at the input side.

The multi-level HCC systems are simulated with the same input and output parameters as the SVM system, in order to make comparison with the SVM system. HCC system samples three phase input voltages at the input side to perform front-end rectifier calculation. Three phase output currents are sampled at the output side and converted into $\alpha - \beta$ stationary coordinate representation and are feedback to the system. The feedback current signals are compared with their reference signals to generate current error signals which are fed to the multi-level comparators. Based on the digital output of the multi-level comparator, the system selects the appropriate voltage vectors that are combined with the rectifying output to generate the overall switching sequences for the matrix converter.

Simulation results show that the HCC system can generate the desired sinusoidal output current and obtain sinusoidal input current at the input side like the SVM system. The four-level HCC system can accurately determine the voltage vector, and the switching frequency is reduced compared to that of the three-level system. Results also demon-

strate that HCC systems offer faster dynamic response than SVM system. Table 5.3 summarizes the distinction between three-level HCC and four-level HCC.

Table 5.3: Summary of distinctions between Three-level HCC and Four-level HCC

		Three-level HCC	Four-level HCC
Input current	Amplitude of fundamental (A)	12.74	12.65
	THD	6.36%	6.33%
Output current	Amplitude of fundamental (A)	9.983	9.981
	THD	1.54%	1.08%
Hysteresis comparators		2 three-level comparators	1 three-level and 1 four-level comparator
Voltage vector selection		not optimized	optimized
Switching frequency		high	low
Switching loss		high	low

Chapter 6

Comparison of SVM and HCC Control Strategies for Matrix Converter under Abnormal Input Voltage Conditions

6.1 Introduction

Adjustable speed drives using AC induction motors have been widely used in industrial applications. These drives are usually based on indirect power conversion scheme using PWM AC-DC-AC converters. As it is known, the indirect power converters require a bulky capacitor or inductor in the DC-link for energy storage. The matrix converter performs the power conversion directly from AC to AC without any intermediate DC-link. The lack of reactive components in the DC-link is one of the salient advantages of matrix converter which allows a compact design. Furthermore, the matrix converter provides four-quadrant operation, sinusoidal input/output current, and adjustable input power factor. As a consequence, this topology has received considerable attention because it provides an attractive alternative to intermediary-stage topologies.

Since the matrix converter is a direct frequency conversion device without DC-link components, the disturbances at the ac utility grid side are immediately reflected to the output side. So several performance and reliability issues of the matrix converter still need to be addressed. In particular, the influences of input line voltage disturbances on the output behavior of matrix converter and the drive performance of motor load are significant and undesirable. The unbalanced and non-sinusoidal input voltages can result in unwanted output harmonic currents. The short duration input voltage sag could bring the voltage sag effects to the load side instantly. These abnormal input voltage behaviors degrade the output characteristics of the matrix converter and deteriorate the drive performance of induction motor.

The aim of this chapter is to investigate the performance of space vector modulation (SVM) technique and hysteresis current control (HCC) technique for matrix converter under abnormal input voltage conditions and to make critical comparison. The SVM and HCC techniques are based on different modulation principle, and the HCC technique does not need to calculate the duty cycle for the fictitious inverting part. So under abnormal input voltage conditions, the HCC technique has the inherent ability of preventing the disturbance at the grid side from propagating to the output side, and thereby obtaining better output characteristics than SVM techniques. Simulation results are given to demonstrate these advantages of HCC technique.

6.2 Analysis of Matrix Converter under Abnormal Input Voltage Conditions

The abnormal input voltage conditions usually include: unbalanced input voltages, non-sinusoidal input voltages and short duration input voltage sag. The output characteristics of the matrix converter under these three conditions are discussed here. In order to clearly analyse the matrix converter transfer function under abnormal input voltage condition, some of the equations that have already been introduced in Chapter 3 will be listed here for convenience.

Under normal input conditions, the input three phase voltages can be expressed as

$$\mathbf{V}_{iPh} = V_{im} \cdot \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t - 120^\circ) \\ \cos(\omega_i t + 120^\circ) \end{bmatrix} \quad (6.1)$$

And the desired local-averaged output line voltages can be expressed as

$$\begin{aligned} \bar{\mathbf{V}}_{oL} &= \begin{bmatrix} \bar{v}_{AB} \\ \bar{v}_{BC} \\ \bar{v}_{CA} \end{bmatrix} \\ &= \sqrt{3} \cdot V_{om} \cdot \begin{bmatrix} \cos(\omega_o t - \varphi_o + 30^\circ) \\ \cos(\omega_o t - \varphi_o + 30^\circ - 120^\circ) \\ \cos(\omega_o t - \varphi_o + 30^\circ + 120^\circ) \end{bmatrix} \end{aligned} \quad (6.2)$$

The input-phase to output-line transfer function matrix in low frequency $\bar{\mathbf{T}}_{PhL}$ should be chosen as

$$\bar{\mathbf{T}}_{PhL} = m \cdot \begin{bmatrix} \cos(\omega_o t - \varphi_o + 30^\circ) \\ \cos(\omega_o t - \varphi_o + 30^\circ - 120^\circ) \\ \cos(\omega_o t - \varphi_o + 30^\circ + 120^\circ) \end{bmatrix} \cdot \begin{bmatrix} \cos(\omega_i t - \varphi_i) \\ \cos(\omega_i t - \varphi_i - 120^\circ) \\ \cos(\omega_i t - \varphi_i + 120^\circ) \end{bmatrix}^T \quad (6.3)$$

where $0 \leq m \leq 1$ is the modulation index.

Equation (6.3) presents the indirect modulation strategy. The transfer function matrix is equal to the product of two matrices

$$\bar{\mathbf{T}}_{PhL} = \bar{\mathbf{T}}_{VSI}(\omega_o) \cdot \bar{\mathbf{T}}_{VSR}^T(\omega_i) \quad (6.4)$$

where $\bar{\mathbf{T}}_{VSR}$ is the transfer function of rectifying stage, and $\bar{\mathbf{T}}_{VSI}$ is the transfer function of inverting stage.

By multiplication of matrix $\bar{\mathbf{T}}_{VSR}^T(\omega_i)$ with the input voltage vector (6.1), a constant

voltage is obtained

$$V_{pn} = \bar{\mathbf{T}}_{\text{VSR}}^T(\omega_i) \cdot \mathbf{V}_{i\text{Ph}} = \frac{3}{2} \cdot V_{im} \cdot \cos(\varphi_i) = \text{const.} \quad (6.5)$$

6.2.1 Unbalanced Input Voltages

In three phase power systems the generated voltages should be sinusoidal and equal in magnitude, with the adjacent phases 120° apart. However, the resulting power system voltages at the distribution end and at the point of utilization can be unbalanced for several reasons. When under balanced input voltages condition, the magnitude of the input phase voltage vector remains constant and rotates at a constant angular velocity. In the case of sinusoidal and unbalanced supply voltages, the input voltages can be decomposed into a positive sequence component V_P and a negative sequence component V_N [63–65].

$$V_P = \frac{V_a + a \cdot V_b + a^2 \cdot V_c}{3} \quad (6.6)$$

$$V_N = \frac{V_a + a^2 \cdot V_b + a \cdot V_c}{3} \quad (6.7)$$

where $a = 1\angle 120^\circ$, $a^2 = 1\angle 240^\circ$ and the three phase unbalanced input voltages can be represented as a sum of the positive and negative sequence components [66]:

$$\mathbf{V}_{i\text{Ph}} = \mathbf{V}_P + \mathbf{V}_N \quad (6.8)$$

where

$$\mathbf{V}_P = V_P \cdot \begin{bmatrix} \cos(\omega_i t + \varphi_\alpha) \\ \cos(\omega_i t - 120^\circ + \varphi_\alpha) \\ \cos(\omega_i t + 120^\circ + \varphi_\alpha) \end{bmatrix} \quad (6.9)$$

and

$$\mathbf{V}_N = V_N \cdot \begin{bmatrix} \cos(\omega_i t + \varphi_\beta) \\ \cos(\omega_i t + 120^\circ + \varphi_\beta) \\ \cos(\omega_i t - 120^\circ + \varphi_\beta) \end{bmatrix} \quad (6.10)$$

The fundamental negative sequence component which appears causes variations in both magnitude and angular velocity of the input voltage vector: the input voltage vector trajectory changes from circular to elliptical. Due to the counter-rotating voltage systems (positive and negative sequence), the variations occur at twice the input grid frequency. As a result, the virtual DC-link voltage will be pulsating at twice the input grid frequency during the unbalance as shown in figure 6.2. The three phase unbalanced input voltages used in system simulation are V_a (50Hz 160V peak value), V_b (50Hz 200V peak value), and V_c (50Hz 240V peak value) and are shown in figure 6.1.

Figure 6.1: Three phase unbalanced input voltages

Figure 6.2: The fictitious DC-link voltage under unbalanced input condition

The output line voltage of matrix converter can then be expressed as

$$\begin{aligned}\mathbf{V}_{oL} &= \bar{\mathbf{T}}_{\text{Ph}L} \cdot \mathbf{V}_{i\text{Ph}} \\ &= \bar{\mathbf{T}}_{\text{VSI}}(\omega_o) \cdot \bar{\mathbf{T}}_{\text{VSR}}^T(\omega_i) \cdot \mathbf{V}_{i\text{Ph}}\end{aligned}\quad (6.11)$$

For simplification purpose, the analysis of the output performance of $3\phi - 3\phi$ matrix converter can take a $3\phi - 1\phi$ matrix converter as an example. Then the output voltage of $3\phi - 1\phi$ matrix converter can be expressed as

$$\mathbf{V}_o = \mathbf{V}_{i\text{Ph}}^T \cdot \bar{\mathbf{T}}_{\text{VSR}}(\omega_i) \cdot \bar{\mathbf{T}}_{\text{VSI}}^{(1)}(\omega_o) \quad (6.12)$$

Transfer function $\bar{\mathbf{T}}_{\text{VSR}}(\omega_i)$ and $\bar{\mathbf{T}}_{\text{VSI}}^{(1)}(\omega_o)$ can be expressed in Fourier series as

$$\bar{\mathbf{T}}_{\text{VSR}}(\omega_i) = \begin{bmatrix} A_1 \sin(\omega_i t) + \sum_{n=n_1, n_2 \dots}^{\infty} A_n \sin n(\omega_i t) \\ A_1 \sin(\omega_i t - 120^\circ) + \sum_{n=n_1, n_2 \dots}^{\infty} A_n \sin n(\omega_i t - 120^\circ) \\ A_1 \sin(\omega_i t + 120^\circ) + \sum_{n=n_1, n_2 \dots}^{\infty} A_n \sin n(\omega_i t + 120^\circ) \end{bmatrix} \quad (6.13)$$

$$\bar{\mathbf{T}}_{\text{VSI}}^{(1)}(\omega_o) = \begin{bmatrix} B_1 \sin(\omega_o t) + \sum_{n=n_1, n_2 \dots}^{\infty} B_n \sin n(\omega_o t) \end{bmatrix} \quad (6.14)$$

where $\sum_{n=n_1, n_2 \dots}^{\infty} A_n \sin n(\omega_i t)$ and $\sum_{n=n_1, n_2 \dots}^{\infty} B_n \sin n(\omega_o t)$ are high order harmonics. Substituting (6.8), (6.9), (6.10), (6.13), and (6.14) into (6.12) the following equation is derived.

$$\begin{aligned}\mathbf{V}_o &= (\mathbf{V}_P^T + \mathbf{V}_N^T) \cdot \bar{\mathbf{T}}_{\text{VSR}}(\omega_i) \cdot \bar{\mathbf{T}}_{\text{VSI}}^{(1)}(\omega_o) \\ &= \mathbf{V}_P^T \cdot \bar{\mathbf{T}}_{\text{VSR}}(\omega_i) \cdot \bar{\mathbf{T}}_{\text{VSI}}^{(1)}(\omega_o) + \mathbf{V}_N^T \cdot \bar{\mathbf{T}}_{\text{VSR}}(\omega_i) \cdot \bar{\mathbf{T}}_{\text{VSI}}^{(1)}(\omega_o)\end{aligned}\quad (6.15)$$

The same as the balanced input voltage condition, the positive sequence component will not generate harmonics in the system. The output voltage generated by negative sequence can be expressed as

$$\begin{aligned}\mathbf{V}_N^T \cdot \bar{\mathbf{T}}_{\text{VSR}}(\omega_i) \cdot \bar{\mathbf{T}}_{\text{VSI}}^{(1)}(\omega_o) &= \\ \frac{3A_1 B_1 V_N}{4} \cdot \{ \sin[(2\omega_i + \omega_o)t + \varphi_\beta] - \sin[(2\omega_i - \omega_o)t + \varphi_\beta] \} + O(V^n)\end{aligned}\quad (6.16)$$

where $O(V^n)$ is the high order harmonics generated by the negative sequence.

Equation (6.16) shows that the presence of the negative sequence components will introduce harmonics with the frequency of $(2\omega_i + \omega_o)$ and $(2\omega_i - \omega_o)$ to the output side.

6.2.2 Non-Sinusoidal Input Voltages

The non-sinusoidal input voltages mean that at the input side, the voltages contain both fundamental component and low order harmonic components. When non-sinusoidal input voltages occur, the fictitious DC-link voltage will not remain at a constant value. If k^{th} order harmonics are injected into the input voltages, the fictitious DC-link will pulsate at $(k + 1)$ times the grid frequency. Figure 6.3 and figure 6.4 show 30% 5^{th} harmonic was injected into the input voltages and the resulting fictitious DC-link voltage respectively.

Under non-sinusoidal input voltages condition, the non-sinusoidal input voltages can be expressed by

$$\mathbf{V}_{iPh} = \mathbf{V}_1 + \mathbf{V}_k \quad (6.17)$$

where $\mathbf{V}_k$ is the k^{th} order harmonics

$$\mathbf{V}_k = V_k \cdot \begin{bmatrix} \cos k(\omega_i t) \\ \cos k(\omega_i t - 120^\circ) \\ \cos k(\omega_i t + 120^\circ) \end{bmatrix} \quad (6.18)$$

Substituting (6.17) and (6.18) into (6.12), the output voltage generated by k^{th} order harmonics is derived as:

$$\begin{aligned} \mathbf{V}_k^T \cdot \bar{\mathbf{T}}_{VSR}(\omega_i) \cdot \bar{\mathbf{T}}_{VSI}^{(1)}(\omega_o) = \\ \begin{cases} \frac{3A_1 B_1 V_k}{4} \cdot \{\sin[(k-1)\omega_i + \omega_o]t - \sin[(k-1)\omega_i - \omega_o]t\} & k = 7, 13, 19... \\ -\frac{3A_1 B_1 V_k}{4} \cdot \{\sin[(k+1)\omega_i + \omega_o]t - \sin[(k+1)\omega_i - \omega_o]t\} & k = 5, 11, 17... \end{cases} \end{aligned} \quad (6.19)$$

From equation (6.19), we can notice that if the input voltages contain k^{th} order har-

monics, the low order harmonic components with frequency of $(k - 1)\omega_i \pm \omega_o$ and $(k + 1)\omega_i \pm \omega_o$ will be introduced into the output side.

Figure 6.3: Three phase non-sinusoidal input voltages

Figure 6.4: The fictitious DC-link voltage under non-sinusoidal input condition

6.2.3 Input Voltage Sag

Voltage sags are currently a matter of great interest because they can pose a number of problems in certain equipment depending on their particular sensitivity [67]. In here, we only consider the symmetrical sag, the type of sag with three-phase equal reduction in voltage magnitude of duration between one cycle and a few seconds. It is caused by fault conditions either within the plant or at the customer bus.

Because the matrix converter does not have DC-link capacitor, this means that when input voltage sag occurs, the magnitude of fictitious DC-link voltage will decrease accordingly. Figure 6.5 shows the three phase input voltages under voltage sag condition, and figure 6.6 shows the fictitious DC-link voltage under the voltage sag input condition.

Figure 6.5: Three phase input voltage under voltage sag condition

Figure 6.6: The fictitious DC-link voltage under voltage sag input condition

The consequences of a voltage sag on matrix converter fed induction motor drive can cause the following effects:

- Due to the sudden decrease of the fictitious DC-link voltage and the lack of energy storage component in the matrix converter, the converter will not be able to deliver the required constant output voltage level, which will cause over-current in the induction motor;

6.3. Analysis of SVM and HCC Systems under Abnormal Input Voltage Conditions 97

- The induction motor protection systems may be triggered during voltage sag, for example, inrush protection circuit should be turned off immediately if the input voltage sag is below certain level. Otherwise, when the input voltage is reestablished, over current will be caused at the induction motor input side and will cause serious damage to the induction motor system;

6.3 Analysis of SVM and HCC Systems under Abnormal Input Voltage Conditions

From the above analysis, during the abnormal input voltage conditions, the fictitious DC-link voltage of matrix converter will no longer be kept constant and will further influence the output voltage characteristics, which will cause distorted output currents. However, because SVM and HCC modulation methods are based on different operational principles, the outputs of SVM and HCC systems of matrix converter will show different characteristics.

6.3.1 Output Characteristics of SVM System under Abnormal Input Conditions

It has already been pointed out in Chapter 3 that the indirect SVM modulation for matrix converter is based on the modulation of input current space vector and the modulation of output voltage space vector separately, and the combination of these two modulations together to generate the total duty cycles and switching sequence for the entire matrix converter modulation. For the inverting stage, the duty cycle calculation equations are

$$\begin{aligned} d_\alpha &= T_\alpha/T_s = m_v \cdot \sin(60^\circ - \theta_O) \\ d_\beta &= T_\beta/T_s = m_v \cdot \sin(\theta_O) \\ d_{0v} &= T_{0v}/T_s = 1 - d_\alpha - d_\beta \end{aligned} \tag{6.20}$$

6.3. Analysis of SVM and HCC Systems under Abnormal Input Voltage Conditions 98

where m_v is the VSI modulation index

$$0 \leq m_v = \left(\sqrt{3} \cdot V_{om} \right) / V_{dc} \leq 1 \quad (6.21)$$

And for the rectifying stage the duty cycle calculation equations are

$$\begin{aligned} d_\gamma &= T_\gamma / T_s = m_c \cdot \sin(60^\circ - \theta_I) \\ d_\delta &= T_\delta / T_s = m_c \cdot \sin(\theta_I) \\ d_{0c} &= T_{0c} / T_s = 1 - d_\gamma - d_\delta \end{aligned} \quad (6.22)$$

where m_c is the VSR modulation index

$$0 \leq m_c = I_{im} / I_{dc} \leq 1 \quad (6.23)$$

The output voltage and the input voltage relationship can be expressed as

$$V_{om} = \frac{\sqrt{3}}{2} \cdot V_{im} \cdot m \cdot \cos(\varphi_i) \quad (6.24)$$

Thus, the SVM technique utilizes input and output switching space vectors to generate the output voltage vector in the specified region. When abnormal voltage conditions occurred at the input side, the magnitude and angular speed of the input voltage space vector will not remain constant, and distortion will be transmitted to the output side.

6.3.2 Output Characteristics of HCC System under Abnormal Input Conditions

The proposed matrix converter current control diagram is shown in figure 4.4. As discussed in Chapter 4, for full control of the matrix converter system using hysteresis current controller, we also need to divide the matrix converter system into VSR-VSI equivalent systems as shown in figure 3.2. For the VSR part of the matrix converter, the SVM PWM rectifier modulation is performed with the modulation index m_c set to unity

6.3. Analysis of SVM and HCC Systems under Abnormal Input Voltage Conditions 99

in order to provide the VSI part with the maximum fictitious DC-link voltage. There exist only six non-zero space vectors and three zero space vectors at the DC output of the matrix converter VSR component $v_{pn} = (v_{ab}, v_{bc}, v_{ca}, v_{ba}, v_{ca}, v_{ac}, v_{aa}, v_{bb}, v_{cc})$ as shown in figure 3.5, generated from PWM rectifier. The appropriate v_{pn} are then applied to the VSI component of matrix converter.

For the VSI component of the matrix converter, the system samples the three phase currents from the output side, and converts the three phase quantities into the $\alpha - \beta$ stationary coordinate quantities. The derived output currents i_α and i_β are then feedback to the system and compared with the reference current signals $i_{\alpha ref}$ and $i_{\beta ref}$ to get the current error signals. Two multi-level hysteresis comparators for the α and β components of the current signals are implemented. Accuracy of the current formations is determined by the width of the hysteresis zone of the multi-level comparators. According to the digital outputs of the comparators, the appropriate VSI switches are selected from the VSI switching table in order to keep the current error inside the hysteresis band.

Figure 6.7: Output voltage hexagon

6.3. Analysis of SVM and HCC Systems under Abnormal Input Voltage Condition 100

Table 6.1: Switch states and generated vectors for inverting stage

Type	$V_n(x,x,x)$	V_A	V_B	V_C	$ \vec{V}_o $	$\angle \vec{V}_o$
		V_{AB}	V_{BC}	V_{CA}		
Active	$V_1(p,n,n)$	$2/3V_{pn}$	$-1/3V_{pn}$	$-1/3V_{pn}$	$\frac{2}{\sqrt{3}}V_{pn}$	$\frac{\pi}{6}$
		V_{pn}	0	$-V_{pn}$	$\frac{2}{\sqrt{3}}V_{pn}$	$\frac{\pi}{6}$
	$V_2(p,p,n)$	$1/3V_{pn}$	$1/3V_{pn}$	$-2/3V_{pn}$	$\frac{2}{\sqrt{3}}V_{pn}$	$\frac{\pi}{2}$
		0	V_{pn}	$-V_{pn}$	$\frac{2}{\sqrt{3}}V_{pn}$	$\frac{\pi}{2}$
	$V_3(n,p,n)$	$-1/3V_{pn}$	$2/3V_{pn}$	$-1/3V_{pn}$	$\frac{2}{\sqrt{3}}V_{pn}$	$\frac{5\pi}{6}$
		$-V_{pn}$	V_{pn}	0	$\frac{2}{\sqrt{3}}V_{pn}$	$\frac{5\pi}{6}$
	$V_4(n,p,p)$	$-2/3V_{pn}$	$1/3V_{pn}$	$1/3V_{pn}$	$\frac{2}{\sqrt{3}}V_{pn}$	$-\frac{5\pi}{6}$
		$-V_{pn}$	0	V_{pn}	$\frac{2}{\sqrt{3}}V_{pn}$	$-\frac{5\pi}{6}$
	$V_5(n,n,p)$	$-1/3V_{pn}$	$-1/3V_{pn}$	$2/3V_{pn}$	$\frac{2}{\sqrt{3}}V_{pn}$	$-\frac{\pi}{2}$
		0	$-V_{pn}$	V_{pn}	$\frac{2}{\sqrt{3}}V_{pn}$	$-\frac{\pi}{2}$
	$V_6(p,n,p)$	$1/3V_{pn}$	$-2/3V_{pn}$	$1/3V_{pn}$	$\frac{2}{\sqrt{3}}V_{pn}$	$-\frac{\pi}{6}$
		V_{pn}	$-V_{pn}$	0	$\frac{2}{\sqrt{3}}V_{pn}$	$-\frac{\pi}{6}$
Zero	$V_0(p,p,p)$ or $V_0(n,n,n)$				0

Figure 6.8: Output voltage hexagonal diagram under abnormal input voltage condition

Figure 6.7 shows the vectors that the output inverter can form by applying the fictitious DC-link voltage to the output terminals. Table 6.1 shows the possible switch states and the resulting length and direction of the output voltage vectors. When abnormal input voltages occur at the main side, the magnitude and phase angle of input voltage vector will vary and cause pulsations at the fictitious DC-link voltage. So according to Table 6.1, the length of output voltage switching vectors will vary because of the pulsations at the fictitious DC-link voltage as shown by the shaded area in figure 6.8. In figure 6.8, the six switching vectors V'_n of the inner hexagon represent the generated vectors when fictitious DC-link is at the lowest voltage level. According to equations (4.1) to (4.10), the HCC controller is aimed at selecting appropriate inverting switching vectors to make the output current track its reference. Although the length of the generated inverting switching vectors is varying under abnormal input voltage conditions, yet if the smallest output voltage vector V'_n is still large enough to make the output current track its reference, the output current waveform will not be influenced by abnormal input voltages.

6.4 Simulation Results

In order to illustrate and compare the output characteristics of both SVM and HCC systems under abnormal input voltage conditions, both systems has been simulated with three-phase balanced R - L load (11Ω , 10mH) by using Matlab. For SVM system, the output frequency is 25Hz , the modulation index is 0.5 and the switching frequency is defined as 3000Hz . For HCC system, the current reference is defined as 25Hz , 9A peak value and the hysteresis comparator band is 10% of reference value.

6.4.1 Simulation under Unbalanced Input Voltages

The unbalanced input voltages used for the simulation test are $V_a = 160\text{V}$, $V_b = 200\text{V}$ and $V_c = 240\text{V}$ respectively. Figure 6.9 and figure 6.12 show output current waveforms of SVM system and HCC system under balanced input voltages respectively and their

FFT figures. Figure 6.13 to figure 6.16 show output current waveforms of SVM system and HCC system under unbalanced input voltages respectively and their FFT figures. We can notice that the output current of SVM system has current waveform distortion under unbalanced input condition. According to equation (6.16), the main low order harmonics in output current resulting from unbalanced input voltages in SVM system are the harmonic components at frequencies of $(2f_i \pm f_o)$. And it can be clearly seen from FFT figure of output current in figure 6.14, there exist significant harmonic components at frequencies of 75Hz and 125Hz. While for HCC system under unbalanced input condition, the output current distortion and harmonic components at frequency of $(2f_i \pm f_o)$ are insignificant as shown in figure 6.15 and figure 6.16.

Figure 6.9: Output current of SVM system under balanced input voltage condition Figure 6.10: FFT of output current of SVM system under balanced input voltage condition

Figure 6.11: Output current of HCC system under balanced input voltage condition Figure 6.12: FFT of output current of HCC system under balanced input voltage condition

Figure 6.13: Output current of SVM system under unbalanced input voltage condition

Figure 6.14: FFT of output current of SVM system under unbalanced input voltage condition

Figure 6.15: Output current of HCC system under unbalanced input voltage condition

Figure 6.16: FFT of output current of HCC system under unbalanced input voltage condition

6.4.2 Simulation under Non-Sinusoidal Input Voltages

Each of the three phase input voltages containing 30% 5th-order harmonic were used for simulation testing under non-sinusoidal conditions. Figure 6.17 and figure 6.19 show output current waveforms of SVM system and HCC system under non-sinusoidal input voltages respectively. From figure 6.17, we can notice that, the output current of SVM system has significant current waveform distortion under non-sinusoidal input condition. According to equation (6.19), the main low order harmonics in output current that result from 5th order harmonic input voltages in SVM system are the harmonic components

at frequencies of $(6f_i \pm f_o)$. And it can be clearly seen from the FFT figure of output current in figure 6.18 that there exist significant harmonic components at frequencies of 275Hz and 325Hz. While for HCC system under 5th order harmonic input condition, the output current distortion and harmonic components at frequencies of $(6f_i \pm f_o)$ are insignificant as shown in figure 6.19 and figure 6.20.

Figure 6.17: Output current of SVM system under non-sinusoidal input voltage condition

Figure 6.18: FFT of output current of SVM system under non-sinusoidal input voltage condition

Figure 6.19: Output current of HCC system under non-sinusoidal input voltage condition

Figure 6.20: FFT of output current of HCC system under non-sinusoidal input voltage condition

6.4.3 Simulation under Input Voltage Sag

The voltage sag with the magnitude of the input voltage decreases to 80% of the rated value from 0.06s to 0.14s is simulated. The simulation results show that when the voltage

sag occurs at the input side, the SVM system output current magnitude will decrease accordingly as shown in figure 6.21, but the HCC system output current will not be influenced (as shown in figure 6.22) because the generated inverting output voltage switching vectors still can make the output current track its reference very well.

Figure 6.21: Output current of SVM system under input voltage sag condition

Figure 6.22: Output current of HCC system under input voltage sag condition

6.5 Concluding Remarks

In this Chapter, both of the matrix converter SVM system and HCC system under abnormal input voltage conditions were investigated. The output characteristics of SVM and HCC systems under unbalanced, non-sinusoidal input voltages, and short duration input voltage sag conditions have been extensively analyzed.

The matrix converter transfer function of indirect modulation was analyzed under abnormal input voltage conditions. The analytical results show the following characteristics: (i) Under unbalanced input voltage condition, the fundamental negative sequence component will cause variations in both magnitude and angular velocity of the input voltage vector; the input voltage vector trajectory thus changes from circular to elliptical. Due to the counter-rotating voltage systems (positive and negative sequences), the variations occur at twice the input grid frequency. As a result, the virtual DC-link voltage will pulsate at twice the input grid frequency during the input unbalance. (ii) Under non-sinusoidal input voltage condition, the input voltage contains both the fundamental

component and low order harmonic components which can cause the fictitious DC-link voltage to deviate from a constant value. If k^{th} order harmonics are injected into the input voltages, the fictitious DC-link will pulsate at $(k+1)$ times the grid frequency. (iii) Under input voltage sag condition, because the matrix converter does not have a DC-link capacitor, the magnitude of the fictitious DC-link voltage will decrease accordingly and further influence the magnitude of the output voltage and current.

The matrix converter indirect space vector modulation is based on the modulation of input current and output voltage according to their respective transfer functions. When abnormal input voltages occurred at the input side, the output characteristics will be influenced. As shown from the simulation results, under unbalanced input voltage condition, the output current of SVM system will contain harmonic components at frequencies of $(2f_i \pm f_o)$. Under non-sinusoidal input voltage condition, the output current of SVM system will contain harmonic components at frequencies of $(k-1)\omega_i \pm \omega_o$ and $(k+1)\omega_i \pm \omega_o$. Under input voltage sag, the output current of SVM system shows a significant drop in magnitude.

The matrix converter hysteresis current control strategy shows improved output characteristics under abnormal input voltage conditions. In HCC system, the SVM PWM is adopted at the rectifying stage. When abnormal input voltages occurred, the fictitious DC-link voltage will also be influenced and is pulsating at a certain level which further influences the length of output voltage switching vectors at the inverting part. However, for the inverting stage, the aim of HCC controller is to select the appropriate inverting switching vectors to make the output current track its reference well. Although the magnitude of the generated inverting switching vectors is varying under abnormal input voltage conditions, yet if the smallest output voltage vector V'_n is still large enough to make the output current track its reference, the output current waveform will not be influenced by abnormal input voltages. Simulation results proved that under all these three kinds of abnormal input voltage conditions, the HCC system can still produce very sinusoidal output currents without significant harmonic components at frequencies of $(2f_i \pm f_o)$, $(k-1)\omega_i \pm \omega_o$ and $(k+1)\omega_i \pm \omega_o$.

Chapter 7

Conclusions and Recommendations

7.1 Conclusions

The project described in this thesis was carried out in the following stages: (i) Study on matrix converter topology and its well established indirect space vector modulation (SVM) method; (ii) Proposal of two kinds of novel space vector based hysteresis current control (HCC) strategies for matrix converter; (iii) Comparison of different output characteristics of SVM and HCC control strategies for matrix converter under abnormal input voltage conditions.

In the first stage, the matrix converter topology was compared with traditional AC-DC-AC converter topology. The major advantage of matrix converter in comparison with traditional AC-DC-AC converter is the absence of bulk DC-link capacitor, and furthermore this offers matrix converter the advantage of all silicon solution in terms of compact design. The matrix converter switches are bidirectional switch cells, which are usually constructed by anti-parallel connection of two unidirectional switches together because currently in the market, there are no practical single-device bidirectional switch. The switch configuration offers the matrix converter the advantages of bidirectional power flow and also four-quadrant operation ability. The commutation methods for the bidirectional switches of matrix converter are the four-step commutation and the two-

step commutation methods. In addition to these basic characteristics, the whole circuit for matrix converter also includes: input filter, clamp circuit, and power-up circuit. The most well established modulation method for matrix converter is the indirect space vector modulation method, which decouples the modulation of input current and output voltage, and regards the matrix converter as a back to back PWM converter. The indirect SVM method simplifies the analysis and duty cycle calculation procedure, and can be realized by using modern DSP.

In the the second stage, two novel space vector based hysteresis current control strategies for matrix converter have been proposed. Because hysteresis current control is the simplest technique used to control the phase currents for high speed drive systems, primarily because of its ease of implementation, fast current control response, and inherent peak current limiting capability. So the aim here is to further simplify the matrix converter control system complexity and reduce the controller computational burden. In order to apply hysteresis current control strategy to the modulation of the matrix converter, the indirect modulation method was adopted. The SVM PWM modulation was applied to the rectifying stage with the modulation index set to unity, in order to provide the inverting stage with the maximum fictitious DC-link voltage. The HCC control technique was applied to the inverting stage. One of these two HCC controllers is based on three-level hysteresis comparator and the other is based on four-level hysteresis comparator. Both comparators select the appropriate space vector combinations via switching table including zero vector combination to reduce the switching frequency of the matrix converter and they do not require complex calculations. Also, both regulators work with the current components represented in the $\alpha - \beta$ stationary coordinate system, and need only two multi-level comparators to achieve space vector selection.

In the third stage, both the SVM system and HCC system under abnormal input voltage conditions were investigated. The output characteristics of SVM and HCC systems under unbalanced, non-sinusoidal input voltages, and short duration input voltage sag conditions have been thoroughly analyzed.

The analysis results show the following characteristics: (i) Under unbalanced input

voltage condition, the fundamental negative sequence component causes variations in both magnitude and angular velocity of the input voltage vector which means that the input voltage vector trajectory changes from circular to elliptical. Due to the counter-rotating voltage systems (positive and negative sequence), the variations occur at twice the input grid frequency. As a result, the virtual DC-link voltage will be pulsating at twice the input grid frequency during the input unbalance. (ii) Under non-sinusoidal input voltage condition, the input voltage contains both fundamental component and low order harmonic components which cause the fictitious DC-link voltage to deviate from a constant value. If k^{th} order harmonics are injected into the input voltages, the fictitious DC-link will pulsate at $(k + 1)$ times the grid frequency. (iii) Under input voltage sag condition, because the matrix converter does not have a DC-link capacitor, the magnitude of the fictitious DC-link voltage will decrease accordingly and further influence the magnitude of the output voltage and current.

The matrix converter indirect space vector modulation is based on the modulation of input current and output voltage according to their transfer functions. When abnormal input voltages occur at the input side, the output characteristics will be influenced. As shown from the simulation results, under unbalanced input voltage condition, the output current of SVM system will contain harmonic components at frequencies of $(2f_i \pm f_o)$. Under non-sinusoidal input voltage condition, the output current of SVM system will contain harmonic components at frequencies of $(k - 1)\omega_i \pm \omega_o$ and $(k + 1)\omega_i \pm \omega_o$. Under input voltage sag, the output current of SVM system shows a clear drop in magnitude.

The matrix converter hysteresis current control strategy shows improved output characteristics under abnormal input voltage conditions. In HCC system, the SVM PWM is adopted at the rectifying stage. When abnormal input voltages occur, the fictitious DC-link voltage will also be influenced and is pulsating at a certain level and further influence length of output voltage switching vectors at the inverting part. However, for the inverting stage, the aim of HCC controller is to select appropriate inverting switching vectors to make the output current track its reference. Although the magnitude of generated inverting switching vectors is varying under abnormal input voltage conditions, yet if the smallest output voltage vector V'_n is still large enough to make the output

current track its reference, the output current waveform will not be influenced by abnormal input voltages. Simulation results proved that under all three kinds of abnormal input voltage conditions, the HCC system can still make output current very sinusoidal and does not introduce significant harmonic components at frequencies of $(2f_i \pm f_o)$, $(k-1)\omega_i \pm \omega_o$ and $(k+1)\omega_i \pm \omega_o$ to the output current.

7.2 Recommendations

The main aim of this research project is to study and develop suitable control system for matrix converter. The matrix converter hysteresis current control method has been investigated and compared with the well established indirect space vector modulation method. Therefore I would like to highlight the areas which need further analysis and research on the control of matrix converter.

In Chapter 4, two kinds of novel space vector based multi-level hysteresis current control strategies for matrix converter have been proposed. One is based on three-level hysteresis comparator and the other is based on four-level hysteresis comparator. Because the four-level hysteresis comparator can determine switching vectors more accurately than the three-level hysteresis comparator, the four-level structure can help to reduce the transistors' switching frequency compared to that of the three-level one. But for hysteresis current control structure, a kind of sequential design (such as Moore State Machine) of the controller can achieve further reduction of the transistors' switching frequency. The sequential design keeps track of past error location and control vector to determine which should be the next optimum switching vector. This kind of switching vector selection principle permits one to solve many kinds of redundancies in the selection of control command, and leads to a significant reduction of transistors' switching frequency.

The conventional hysteresis current controller with a fixed hysteresis-band has the disadvantage that the modulation frequency is not fixed. If the hysteresis-band is set too small, very high switching frequency will occur which affects the losses and efficiency of

the drive system. For addressing this problem, the fixed frequency phase current PWM control is preferred. This can be realized using many methods: predictive current control, dead-beat control, and neural and fuzzy logic control [68–75]. However, the fuzzy logic controllers are not suitable because of their complexity and computational time. For the predictive current control and dead-beat control, these techniques predict the current error on the basis of the actual error and of the ac-side load parameters R , L and E . The voltage vector to be generated by PWM during the next modulation period is thus determined, so as to minimize the forecast error [40–42]. An interesting dead-beat predictive current controller can be adopted [76–78]. It involves the selection of the optimum space vector voltage to be applied to the converter at any instant to force the output current to follow its reference, and it operates with a fixed switching period to give a better quality current control both at steady state and transient conditions.

Author's Publications

1. S.Y. Jia, K.J. Tseng, X. Wang "Study on Reverse Recovery Characteristics of Reverse-Blocking IGBT Applied in Matrix Converter", In *Proceedings of Applied Power Electronics Conference APEC'05*, Volume 3, pages:1917 - 1921 Mar. 2005.
2. X. Wang, K.J. Tseng "Novel Space Vector Based Hysteresis Current Control Strategies (HCC)for Matrix Converter", In *Proceedings of European Conference on Power Electronics and Application EPE'05*, Sept. 2005.
3. X. Wang, K.J. Tseng "Comparison of SVM and HCC Control Strategies for Matrix Converter under Abnormal Input Voltage Conditions", Submitted to *IEEE Transactions on Industry Electronics*, 2005.

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Appendix A

C Program for Matrix Converter Matlab Model

Duty Cycle Calculation

```

/*
    Matrix Converter Space Vector Modulation Look Up Table And Switch Duty
    Cycle Calculation And Optimized Switching Sequence To Reduce Switching.
*/

//
#define S_FUNCTION_LEVEL 2 #define S_FUNCTION_NAME Dc_0

#define u(index) (*uPtrs[index]) /* for convenient to access
input port 0) Ts, V_om, V_thita, V_im, cos(alfa), I_thita */
#define PI (3.141593)

/*
 * Need to include simstruc.h for the definition of the SimStruct and
 * its associated macro definitions.
 */
#include "simstruc.h" #include "math.h"

    real_T V_thita, I_thita;
    int_T S_i, S_o;
    int_T flag;
    real_T d_tao, d_gama, d_beta, d_alfa, d_0;
    real_T d_gama_beta, d_gama_alfa, d_tao_alfa, d_tao_beta;
    real_T d_gama_alfa, d_gama_beta, d_tao_beta, d_tao_alfa;
    real_T m_c=1., m_v, v_pn;
    real_T t1, t2, t3, t4, t0;

```

```

/* Function: mdlInitializeSizes
=====
* Abstract:
*   The sizes information is used by Simulink to determine the S-function
*   block's characteristics (number of inputs, outputs, states, etc.).
*/
static void mdlInitializeSizes(SimStruct *S) {

    ssSetNumSFcnParams(S, 0); /* Number of expected parameters is 0*/
    if (ssGetNumSFcnParams(S) != ssGetSFcnParamsCount(S)) {
        /* Return if number of expected != number of actual parameters */
        ssSetErrorStatus(S,"mismatch parameters number");
        return;
    }

    ssSetNumContStates(S, 0); /* number of continous states is 0 */

    ssSetNumDiscStates(S, 0); /* nubmer of discrete states is 0 */

    if (!ssSetNumInputPorts(S, 1)) return; /* set inputPort number to 1 */
    ssSetInputPortWidth(S, 0, 6); /* 0 is the inputPort index, 6 is the width */
    /* A port has direct feedthrough if the input is used in either
    * the mdlOutputs or mdlGetTimeOfNextVarHit functions */
    ssSetInputPortDirectFeedThrough(S, 0, 1); /* 0 is the inputport index
        /* and the second 0 means no feed through */

    if (!ssSetNumOutputPorts(S, 1)) return;
    ssSetOutputPortWidth(S, 0, 7); /* number is 7 */

    ssSetNumSampleTimes(S, 1); /* number of sample times is 1 */

    ssSetNumRWork(S, 0); /* number of real work vector elements */
    ssSetNumIWork(S, 0); /* number of integer work vector elements*/
    ssSetNumPWork(S, 0); /* number of pointer work vector elements*/
    ssSetNumModes(S, 0); /* number of mode work vector elements */
    ssSetNumNonsampledZCs(S, 0); /* number of nonsampled zero crossings */

    ssSetOptions(S, 0); /* no options */
}

/* Function: mdlInitializeSampleTimes
=====
* Abstract:
*   This function is used to specify the sample time(s) for your

```

```

*   S-function. You must register the same number of sample times as
*   specified in ssSetNumSampleTimes.
*/
static void mdlInitializeSampleTimes(SimStruct *S) { /* A
continuous function that changes during minor integration steps */
ssSetSampleTime(S, 0, INHERITED_SAMPLE_TIME); /* 0 is the index of
sample time number as defined in above, I defined 1 */
ssSetOffsetTime(S, 0, 0.0); /* 0 is the index */

}

#define MDL_INITIALIZE_CONDITIONS /* Change to #undef to remove
function */ #if defined(MDL_INITIALIZE_CONDITIONS)
/* Function: mdlInitializeConditions =====
* Abstract:
*   In this function, you should initialize the continuous and discrete
*   states for your S-function block. The initial states are placed
*   in the state vector, ssGetContStates(S) or ssGetRealDiscStates(S).
*   You can also perform any other initialization activities that your
*   S-function may require. Note, this routine will be called at the
*   start of simulation and if it is present in an enabled subsystem
*   configured to reset states, it will be call when the enabled subsystem
*   restarts execution to reset the states.
*/
static void mdlInitializeConditions(SimStruct *S)
{
}
#endif /* MDL_INITIALIZE_CONDITIONS */

#define MDL_START /* Change to #undef to remove function */ #if
defined(MDL_START)
/* Function: mdlStart =====
* Abstract:
*   This function is called once at start of model execution. If you
*   have states that should be initialized once, this is the place
*   to do it.
*/
static void mdlStart(SimStruct *S)
{
}
#endif /* MDL_START */

/* Function: mdlOutputs
=====
*/

```

```

static void mdlOutputs(SimStruct *S, int_T tid) {

    real_T *y = ssGetOutputPortRealSignal(S,0); /* output */
    InputRealPtrsType uPtrs=ssGetInputPortRealSignalPtrs(S, 0);/*input port0*/

/*
 * Judge output voltage sector
 */
    if((u(2)>0.)&&(u(2)<PI/6.))
        {S_o=0;
         V_thita=u(2)+PI/6.;
        }
    if ((u(2)>PI/6.)&&(u(2)<PI/2.))
        {S_o=1;
         V_thita=u(2)-PI/6.;
        }
    if ((u(2)>PI/2.)&&(u(2)<5.*PI/6.))
        {S_o=2;
         V_thita=u(2)-PI/2.;
        }
    if ((u(2)>5.*PI/6.)&&(u(2)<7.*PI/6.))
        {S_o=3;
         V_thita=u(2)-5.*PI/6.;
        }
    if ((u(2)>7.*PI/6.)&&(u(2)<3.*PI/2.))
        {S_o=4;
         V_thita=u(2)-7.*PI/6.;
        }
    if ((u(2)>3.*PI/2.)&&(u(2)<11.*PI/6.))
        {S_o=5;
         V_thita=u(2)-3.*PI/2.;
        }
    if ((u(2)>11.*PI/6.))
        {S_o=0;
         V_thita=u(2)-11.*PI/6.;
        }

/*
 *Judge input current sector
 */
    if((u(5)>0.)&&(u(5)<PI/6.))
        {S_i=0;
         I_thita=u(5)+PI/6.;
        }

```

```

    if ((u(5)>PI/6.)&&(u(5)<PI/2.))
        {S_i=1;
         I_thita=u(5)-PI/6.;
        }
    if ((u(5)>PI/2.)&&(u(5)<5.*PI/6.))
        {S_i=2;
         I_thita=u(5)-PI/2.;
        }
    if ((u(5)>5.*PI/6.)&&(u(5)<7.*PI/6.))
        {S_i=3;
         I_thita=u(5)-5.*PI/6.;
        }
    if ((u(5)>7.*PI/6.)&&(u(5)<3.*PI/2.))
        {S_i=4;
         I_thita=u(5)-7.*PI/6.;
        }
    if ((u(5)>3.*PI/2.)&&(u(5)<11.*PI/6.))
        {S_i=5;
         I_thita=u(5)-3.*PI/2.;
        }
    if ((u(5)>11.*PI/6.))
        {S_i=0;
         I_thita=u(5)-11.*PI/6.;
        }

/* When the number of S_o+S_i is even, the sequence should be
beta, alfa, alfa, beta */

    if ((S_i+S_o)%2==0)
    { flag=0;
    }

/* When the number of S_o+S_i is odd, the sequence should be alfa,
beta, beta, alfa */

    if ((S_i+S_o)%2!=0)
    { flag=1;
    }

/* Compute each duty cycle and assign each duty cycle to each
switch */

/* Compute duty cycle for output voltage hexagon */

v_pn=(3./2.)*m_c*u(3)*u(4);

```

```

m_v=(sqrt(3)*u(1))/v_pn;
d_alfa=m_v*sin(PI/3.-V_thita);
d_beta=m_v*sin(V_thita);

/* Compute duty cycle for input current hexagon */

d_gama=m_c*sin(PI/3.-I_thita);
d_tao=m_c*sin(I_thita);

/* Assign different duty cycle according to different sector combination */

if (flag==1)
{ d_gama_alfa=d_gama*d_alfa;
  d_gama_beta=d_gama*d_beta;
  d_tao_beta=d_tao*d_beta;
  d_tao_alfa=d_tao*d_alfa;
  d_0=1.-(d_gama_alfa+d_gama_beta+d_tao_beta+d_tao_alfa);
  t1=d_gama_alfa*u(0);
  t2=d_gama_beta*u(0);
  t3=d_tao_beta*u(0);
  t4=d_tao_alfa*u(0);
  t0=d_0*2.*u(0);
}

if (flag==0)
{ d_gama_beta=d_gama*d_beta;
  d_gama_alfa=d_gama*d_alfa;
  d_tao_alfa=d_tao*d_alfa;
  d_tao_beta=d_tao*d_beta;
  d_0=1.-(d_gama_beta+d_gama_alfa+d_tao_alfa+d_tao_beta);
  t1=d_gama_beta*u(0);
  t2=d_gama_alfa*u(0);
  t3=d_tao_alfa*u(0);
  t4=d_tao_beta*u(0);
  t0=d_0*2.*u(0);
}

y[0]=t0;
y[1]=t1;
y[2]=t2;
y[3]=t3;
y[4]=t4;
y[5]=S_o;
y[6]=S_i;

```

```

}

/* Function: mdlTerminate
=====
* Abstract:
*   In this function, you should perform any actions that are necessary
*   at the termination of a simulation. For example, if memory was
*   allocated in mdlInitializeConditions, this is the place to free it.
*/
static void mdlTerminate(SimStruct *S) { }

/*=====
* See sfuntmpl.doc for the optional S-function methods *
*=====*/

/*=====
* Required S-function trailer *
*=====*/

#ifdef MATLAB_MEX_FILE /* Is this file being compiled as a
MEX-file? */ #include "simulink.c" /* MEX-file interface
mechanism */ #else #include "cg_sfun.h" /* Code generation
registration function */ #endif

```

Pulse Width Generator

```

#define S_FUNCTION_LEVEL 2 #define S_FUNCTION_NAME Po_0

#define u(index) (*uPtrs[index])
#define PI (3.141593)

/*
* Need to include simstruc.h for the definition of the SimStruct and
* its associated macro definitions.
*/
#include "simstruc.h" #include "math.h"

int_T S_i, S_o, Output;
int_T V[6][30]={6,9,10,1,21,6,15,16,1,21,12,15,16,7,
21,12,3,4,7,21,18,3,4,13,21,18,9,10,13,21},
          {10,1,2,11,20,16,1,2,17,20,16,7,8,17,
20,4,7,8,5,20,4,13,14,5,20,10,13,14,11,20},
          {2,11,12,3,19,2,17,18,3,19,8,17,18,9,
19,8,5,6,9,19,14,5,6,15,19,14,11,12,15,19},

```

```

        {12,3,4,7,21,18,3,4,13,21,18,9,10,13,
        21,6,9,10,1,21,6,15,16,1,21,12,15,16,7,21},
        {4,7,8,5,20,4,13,14,5,20,10,13,14,11,
        20,10,1,2,11,20,16,1,2,17,20,16,7,8,17,20},
        {8,5,6,9,19,14,5,6,15,19,14,11,12,15,
        19,2,11,12,3,19,2,17,18,3,19,8,17,18,9,19}};
int_T D[18][21]={1,0,0,0,0,1,0,0,1,1,0,0,0,0,1,1,0,0,1,0,0},
        {1,0,0,0,0,1,0,0,1,1,0,0,0,0,1,1,0,0,1,0,0},
        {0,1,1,0,0,0,0,0,0,0,1,1,0,0,0,0,1,1,0,1,0},
        {0,1,1,0,0,0,0,0,0,0,1,1,0,0,0,0,1,1,0,1,0},
        {0,0,0,1,1,0,1,1,0,0,0,0,1,1,0,0,0,0,0,0,1},
        {0,0,0,1,1,0,1,1,0,0,0,0,1,1,0,0,0,0,0,0,1},
        {0,0,1,1,0,0,1,0,0,0,0,1,0,0,1,1,0,0,1,0,0},
        {0,0,1,1,0,0,1,0,0,0,0,1,0,0,1,1,0,0,1,0,0},
        {0,0,0,0,1,1,0,1,1,0,0,0,0,0,0,0,1,1,0,1,0},
        {0,0,0,0,1,1,0,1,1,0,0,0,0,0,0,0,1,1,0,1,0},
        {1,1,0,0,0,0,0,0,0,1,1,0,1,1,0,0,0,0,0,0,1},
        {1,1,0,0,0,0,0,0,0,1,1,0,1,1,0,0,0,0,0,0,1},
        {0,0,1,1,0,0,0,0,1,1,0,0,1,0,0,0,0,1,1,0,0},
        {0,0,1,1,0,0,0,0,1,1,0,0,1,0,0,0,0,1,1,0,0},
        {0,0,0,0,1,1,0,0,0,0,1,1,0,1,1,0,0,0,0,1,0},
        {0,0,0,0,1,1,0,0,0,0,1,1,0,1,1,0,0,0,0,1,0},
        {1,1,0,0,0,0,1,1,0,0,0,0,0,0,0,0,1,1,0,0,0,1},
        {1,1,0,0,0,0,1,1,0,0,0,0,0,0,0,0,1,1,0,0,0,1}};

```

```
/* Function: mdlInitializeSizes
```

```
=====
```

```
* Abstract:
```

```
* The sizes information is used by Simulink to determine the S-function
* block's characteristics (number of inputs, outputs, states, etc.).
```

```
*/
```

```
static void mdlInitializeSizes(SimStruct *S) {
```

```

    ssSetNumSFcnParams(S, 0); /* Number of expected parameters is 0*/
    if (ssGetNumSFcnParams(S) != ssGetSFcnParamsCount(S)) {
        /* Return if number of expected != number of actual parameters */
        ssSetErrorStatus(S,"mismatch parameters number");
        return;
    }

```

```
    ssSetNumContStates(S, 0); /* number of continous states is 0 */
```

```
    ssSetNumDiscStates(S, 0); /* nubmer of discrete states is 0 */
```

```
    if (!ssSetNumInputPorts(S, 1)) return; /* set inputPort number to 1 */
```

```

    ssSetInputPortWidth(S, 0, 2); /* 0 is the inputPort index, 3 is the width */
    /* A port has direct feedthrough if the input is used in either
     * the mdlOutputs or mdlGetTimeOfNextVarHit functions */
    ssSetInputPortDirectFeedThrough(S, 0, 1); /* 0 is the inputport index
                                                /* and the second 0 means no feed through */

    if (!ssSetNumOutputPorts(S, 1)) return;
    ssSetOutputPortWidth(S, 0, 18); /* number is 18 */

    ssSetNumSampleTimes(S, 1); /* number of sample times is 1 */

    ssSetNumRWork(S, 0); /* number of real work vector elements */
    ssSetNumIWork(S, 0); /* number of integer work vector elements*/
    ssSetNumPWork(S, 0); /* number of pointer work vector elements*/
    ssSetNumModes(S, 0); /* number of mode work vector elements */
    ssSetNumNonsampledZCs(S, 0); /* number of nonsampled zero crossings */

    ssSetOptions(S, 0); /* no options */
}

/* Function: mdlInitializeSampleTimes
=====
* Abstract:
* This function is used to specify the sample time(s) for your
* S-function. You must register the same number of sample times as
* specified in ssSetNumSampleTimes.
*/
static void mdlInitializeSampleTimes(SimStruct *S) {
    /* A continuous function that changes during minor integration steps */
    ssSetSampleTime(S, 0, INHERITED_SAMPLE_TIME); /* 0 is the index of sample
time number as defined in above, I defined 1 */ ssSetOffsetTime(S,
0, 0.0); /* 0 is the index */
}

#define MDL_INITIALIZE_CONDITIONS /* Change to #undef to remove
function */ #if defined(MDL_INITIALIZE_CONDITIONS)
/* Function: mdlInitializeConditions =====
* Abstract:
* In this function, you should initialize the continuous and discrete
* states for your S-function block. The initial states are placed
* in the state vector, ssGetContStates(S) or ssGetRealDiscStates(S).
* You can also perform any other initialization activities that your
* S-function may require. Note, this routine will be called at the
* start of simulation and if it is present in an enabled subsystem
* configured to reset states, it will be call when the enabled subsystem

```

```

    *   restarts execution to reset the states.
    */
static void mdlInitializeConditions(SimStruct *S)
{
}
#endif /* MDL_INITIALIZE_CONDITIONS */

#define MDL_START /* Change to #undef to remove function */ #if
defined(MDL_START)
/* Function: mdlStart =====
    * Abstract:
    *   This function is called once at start of model execution. If you
    *   have states that should be initialized once, this is the place
    *   to do it.
    */
static void mdlStart(SimStruct *S)
{
}
#endif /* MDL_START */

/* Function: mdlOutputs
=====
    */
static void mdlOutputs(SimStruct *S, int_T tid) {

    real_T *y = ssGetOutputPortRealSignal(S, 0); /* output */
    InputRealPtrsType uPtrs=ssGetInputPortRealSignalPtrs(S, 0);/*input port0*/

    S_o=u(0);
    S_i=u(1);

/*
    * According to sector number to select the switching combination and
    Assign each conducting time to each switch selected */

    Output=V[S_i][S_o]-1;
    y[0] = D[0][Output];
    y[1] = D[1][Output];
    y[2] = D[2][Output];
    y[3] = D[3][Output];
    y[3] = D[3][Output];
    y[4] = D[4][Output];
    y[5] = D[5][Output];
    y[6] = D[6][Output];
    y[7] = D[7][Output];

```

```

    y[8] = D[8][Output];
    y[9] = D[9][Output];
    y[10]=D[10][Output];
    y[11]=D[11][Output];
    y[12]=D[12][Output];
    y[13]=D[13][Output];
    y[14]=D[14][Output];
    y[15]=D[15][Output];
    y[16]=D[16][Output];
    y[17]=D[17][Output];

}

/* Function: mdlTerminate
=====
* Abstract:
*   In this function, you should perform any actions that are necessary
*   at the termination of a simulation. For example, if memory was
*   allocated in mdlInitializeConditions, this is the place to free it.
*/
static void mdlTerminate(SimStruct *S)
{ }

/*=====
* See sfuntmpl.doc for the optional S-function methods *
*=====*/

/*=====
* Required S-function trailer *
*=====*/

#ifdef MATLAB_MEX_FILE /* Is this file being compiled as a
MEX-file? */ #include "simulink.c" /* MEX-file interface
mechanism */ #else #include "cg_sfund.h" /* Code generation
registration function */ #endif

```