A 2.45GHz CMOS PA+T/R switch for wireless communication

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2006

Hu, C. (2006). A 2.45GHz CMOS PA+T/R switch for wireless communication. Master's thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/3514>

<https://doi.org/10.32657/10356/3514>

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A 2.45GHz CMOS PA+T/R Switch for Wireless Communication

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University

in fulfillment of the requirement for the degree of

Master of Engineering

2006

STATEMENT OF ORIGINALITY

I hereby certify the content of this thesis is the result of work done by me and has not been submitted for higher degree to any other University or Institution.

Date

Hu Changhui

Abstract

The rapid growth of wireless communication requires low-cost, low-power and high-integration RF front ends. The CMOS process is more cost-efficient than other processes such as SiGe, GaAs; but due to its poorer performance characteristic at high frequency, it is very challenging to implement the complete RF front end in CMOS. The high integration of RF front ends to reduce the on board components is, however, the key factor to reduce the production cost. Although the Power Amplifier (PA) and transmit/receive (T/R) switch have been implemented in CMOS, the implementation of a CMOS PA combined with a T/R switch has not been reported. Most reported single-chip transceivers actually exclude the Power Amplifier (PA), T/R switch and band selection filter, and these three components are often implemented separately. An integration of PA, T/R switch and band-selection filter will significantly reduce the overall cost of the transceiver, and provide a low cost single-chip solution to wireless communications.

Recent efforts in the design of integrated RF transmitters have been focused on the Power Amplifier. In general, it is difficult to integrate the PA in CMOS because of technology limitations that severely limit the efficiency of the PA.

This thesis describes the design of an RF CMOS Power Amplifier (PA) combined with a T/R switch in a conventional CMOS process. The Power Amplifier is designed for all applications in the ISM (Industry Science and Medical) band, which has a transmit frequency of 2.4~2.4835 GHz and requires a peak output power of 100mW (EIRP). A Class A CMOS PA with T/R switch in a 0.18 μ m thick gate standard CMOS

process which can generate 100mW of output power into a 50ohms load is presented in this report. Packaging, PCB and testing issues are also described in this report. The PA and T/R switch is also designed and taped out in the SiGe BiCMOS process to compare with the PA and T/R switch in the CMOS process.

Acknowledgement

There are many people whom I would like to thank for their assistance, advice and support in completing this work.

First and foremost, I would like to thank my supervisor, Professor Do Manh Anh, for his support over the whole research process. His advices on technical matters are invaluable, and his guidance is very critical for the successful of my research. Professor Do's patience in answering questions and instruction of writing papers are greatly appreciated.

I'd like to thank Professor Ma Jian-Guo for his help on my paper and questions that I have had along the way. Professor Yeo Kiat Seng's help during my research is also appreciated.

Next I would thank my colleagues in ARFIC who have helped me. Thanks to Mr. Sia Choon Beng for his assistance with the measurements. From discussions with Mr. Ong Chongyong, Mr. Sia Choon Beng and Mr. Tong Afat, I learn greatly in TL CPW design, RF system design and deep understanding of IC design from the device modeling aspect.

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1 Introduction

1.1 Motivation

The rapid growth of wireless systems requires low-cost, low-power and high-integration RF front ends. The high integration of RF front ends to reduce the on board components is a key to reduce the cost and size. Currently, the whole transceiver excluding the PA, T/R switch and the band selection filter can be integrated into a single chip. The integration of the T/R switch and band-selection filter will further reduce the overall cost of the transceiver. As shown in Figure 1.1, this project will include BPF (Band Pass Filter), T/R switch and Power Amplifier(PA), but the BPF is inherited in the matching networks, which will further improve the circuit performance.

Figure 1.1 Diagram of BPF, T/R Switch and PA

For high integration, CMOS process is a very good choice for two reasons. Firstly, CMOS is inexpensive compared with other processes such as SiGe, InP, and GaAs. Secondly, most base band circuits and part of the RF front end (such as LNA, Mixer and filter) are already implemented in CMOS process.

For the past decade, applications in the 2.4GHz Industrial, Scientific, and Medical

(ISM) frequency band have gained popularity through various standards such as Bluetooth and IEEE802.11b/g. Wi-Fi is another name for 802.11. Currently, most popular mobile phones are integrated with a Bluetooth earphone, and most mobile laptops are integrated with both Bluetooth and WLAN 11b/g. However, low cost RF front ends for Bluetooth and WLAN 802.11b/g are highly sought after to further lower the cost of these products.

The PA and T/R switch designed in this project will be targeted to these standards.

1.2 Objective

The objective of this project is to design a PA and T/R switch for the Bluetooth and IEEE 802.11b/g WLAN standards in standard CMOS. The Power Amplifier will operate in the frequency band of 2.4~2.4835 GHz and produce a maximum output power of 100mW (EIRP) i.e. 20dBm for a 50 Ω system. The T/R switch will have to meet the specifications of commercial products.

In order to accomplish this, there must be an understanding of what functions are implemented in the high-frequency analog portion of the RF transceiver.

A brief introduction of RF transceiver architectures and the Bluetooth and 802.11b/g standards will be covered here.

Figure 1.2 shows the basic architecture of a radio transceiver, which contains two main blocks: the receiver and the transmitter.

Figure 1.2 Radio transceiver architectures[8]

The function of the analog portion of the receive chain is to take a radio-frequency (RF) analog signal and convert that into the digital bit stream which it represents. The basic blocks in the receive path are a low-noise amplifier (so called because it is critical to amplify the incoming signal without contributing any significant noise), a frequency translation block (generally also known as a mixer), and a block which demodulates the signal and outputs the desired digital bits. A block that is required but which is not directly in the signal path is the local oscillator (LO), which is used by the mixer to convert the signal to low-frequency.

On the transmit side, essentially the reverse path is followed. First, the digital bit stream is modulated and converted to an analog signal. The resulting analog signal is then frequency translated by an up-conversion mixer, and the final signal is amplified to the power level that the antenna needs to radiate, as required by the standard. This final block is generally known as a Power Amplifier (PA) [8].

1.3 Standards of Bluetooth and WLAN 802.11b/g

Since this project is targeted for Bluetooth and WLAN 802.11b/g applications, a introduction about the standards is necessary.

1.3.1 Bluetooth

Bluetooth wireless technology is the prevalent WPAN (Wireless Personal Area Network) technology today. It operates in the 2.4-GHz unlicensed frequency band. Bluetooth evolves from version 1.1 at a data rate of 1 Mbps to version 1.2, which improves the signaling and frequency band coexistence mechanisms. The 3-Mbps Bluetooth 2.0+ Enhanced Data Rate (EDR) was ratified in November 2004 and products are beginning to appear on the market.

Bluetooth V1.1 and V1.2 use GFSK modulation, the linearity requirement is relatively low. However, Bluetooth V2.0+EDR use $\pi/4$ DQPSK and 8DPSK modulation schemes, which require a high linearity output power.

Frequency Band and Channel Arrangement

The Bluetooth system operates in the 2.4 GHz ISM band, i.e. 2400 - 2483.5 MHz. RF channels are spaced 1 MHz and are ordered in channel number k as shown in Table 1-1.

Regulatory Range	RF Channels
2.400-2.4835 GHz	$f=2402+k$ MHz, $k=0,\dots,78$

Table 1-1 Bluetooth operating frequency bands

In order to comply with out-of-band regulations in each country, a guard band as

shown in Table 1-2 is used at the lower and upper band edge [41].

Lower Guard Band	Upper Guard Band
2 MHz	3.5 MHz

Table 1-2 Guard Bands

Transmission Power Characteristic

The requirements stated in this section are given as power levels at the antenna connector of the Bluetooth device. If the device does not have a connector, a reference antenna with 0 dBi gain is assumed. The transmit power classes of Bluetooth are shown in Table 1-3.

Power Class	Maximum Output Power (P _{max})	Nominal Output Power	Minimum Output Power	Power Control
1	100 mW (20 dBm)	N/A	1 mW (0 dBm)	P _{min} <+4dBm to P _{max} Optional: P _{min} ² to P _{max}
2	2.5 mW (4 dBm)	1 mW (0 dBm)	0.25 mW(-6 dBm)	Optional: P _{min} ²) to P _{max}
3	1 mW (0 dBm)	N/A	N/A	Optional: P _{min} ²) to P _{max}

Table 1-3 Transmit Power Classes of Bluetooth

1. Minimum output power at maximum power setting.
2. The lower power limit P_{min}<-30dBm is suggested but is not mandatory, and may be chosen according to application needs.

This project will target for 100mW i.e. 20dBm maximum output power.

Spurious Emission

Within the ISM band the transmitter shall pass a spectrum mask, given in Table

- 1-4. An adjacent channel power on adjacent channels with a difference in RF channel

number of two or greater is defined. This adjacent channel power is defined as the sum of the measured power in a 1 MHz RF channel. The transmitted power shall be measured in a 100 kHz bandwidth using maximum hold. The device shall transmit on RF channel M and the adjacent channel power shall be measured on RF channel number N .

Frequency offset	Transmit Power
± 500 KHz	-20 dBc
2MHz ($ M-N =2$)	-20 dBm
3MHz or greater ($ M-N \geq 3$)	-40 dBm

Table 1-4 Bluetooth transmit spectrum mask

Exceptions are allowed in up to three bands of 1 MHz width centered on a frequency which is an integer multiple of 1 MHz. They shall comply with an absolute value of -20 dBm [41].

1.3.2 WLAN IEEE 802.11b/g

In contrast to WPANs, WLANs provide robust wireless network connectivity over a local area of approximately 100 meters between the access point and associated clients. Today's WLANs are based on the IEEE 802.11 standard and are referred to as Wi-Fi networks. 802.11b was the first commercially successful WLAN technology. It operates in the 2.4-GHz frequency band at 11 Mbps. By implementing a different data transmission method, data rates were increased to 54 Mbps in 2003 with 802.11g in the 2.4-GHz band.

Frequency Band and Channel Arrangement

The channel center frequencies and CHNL_ID numbers are listed in Table 1-5. The FCC (US), IC (Canada), and ETSI (Europe) specify operation from 2.4–2.4835 GHz. For Japan, operation is specified as 2.471–2.497 GHz. France allows operation from 2.4465–2.4835 GHz, and Spain allows operation from 2.445–2.475 GHz. For each supported regulatory domain, all channels in Table 1-5 marked with an “X” shall be supported.

CHNL_ID	Frequency (MHz)	Regulatory domains					
		X' 10' FCC	X' 20' IC	X' 30' ETSI	X' 31' Spain	X' 32' France	X' 40' MKK
1	2412	X	X	X	—	—	—
2	2417	X	X	X	—	—	—
3	2422	X	X	X	—	—	—
4	2427	X	X	X	—	—	—
5	2432	X	X	X	—	—	—
6	2437	X	X	X	—	—	—
7	2442	X	X	X	—	—	—
8	2447	X	X	X	—	—	—
9	2452	X	X	X	—	—	—
10	2457	X	X	X	X	X	—
11	2462	X	X	X	X	X	—
12	2467	—	—	X	—	X	—
13	2472	—	—	X	—	X	—
14	2484	—	—	—	—	—	X

Table 1-5 Frequency Channel Plan for 802.11b/g

In a multiple cell network topology, overlapping and/or adjacent cells using different channels can operate simultaneously without interference if the distance between the center frequencies is at least 25 MHz(the occupied bandwidth of the main lobe of the signal is 22MHz) [42].

Figure 1.3 shows the channel frequency arrangement of FCC (US). There are 11 channels with a center frequency spacing of 5MHz. Figure 1.4 shows the non-overlapping channels in FCC, and they are channel 1, 6 and 11.

Figure 1.3 Channel frequency plan of FCC [42]

Figure 1.4 Non-overlapping channel and channel spectrum mask [42]

Transmission Power Characteristic

The maximum output power of 802.11b/g is shown in Table 1-6. The target output power of this project will be 100mW, i.e. 20dBm, which is same as the Class 1 output power requirement of Bluetooth.

Maximum output power	Geographic location	Compliance document
1000 mW	USA	FCC 15.247
100 mW (EIRP)	Europe	ETS 300-328
10 mW	Japan	MPT ordinance for Regulating Radio Equipment, Article 49-20

Table 1-6 Transmit power levels of 802.11b/g

Transmit Power Spectrum Mask

The transmitted spectral products shall be less than -30 dBr (dB relative to the SINx/x peak) for

$$fc - 22 \text{ MHz} < f < fc - 11 \text{ MHz}; \text{ and}$$

$$fc + 11 \text{ MHz} < f < fc + 22 \text{ MHz};$$

and shall be less than -50 dBr for

$$f < fc - 22 \text{ MHz}; \text{ and}$$

$$f > fc + 22 \text{ MHz}.$$

where

fc is the channel center frequency.

The transmit spectral mask is shown in Figure 1.5. The measurements shall be made using a 100 kHz resolution bandwidth and a 100 kHz video bandwidth.

Figure 1.5 Transmit spectrum mask of IEEE 802.11b/g [42]

An introduction of Bluetooth and 802.11b/g is shown above. Both are operating in the ISM band, 2.4 to 2.4835GHz. Bluetooth V1.1, V1.2 and V2.0 use GFSK modulation scheme, require relatively lower linearity; while Bluetooth V2.0+EDR use $\pi/4$ DQPSK and 8DPSK, 802.11b/g use CCK (11Mbps) and OFDM (54Mbps), which require higher linearity. In this project, output referred 1dB compression point of 20dBm is desired.

1.4 Significance of the problem

The standard lossy substrate of CMOS technology can significantly degrade the RF front-end performance. Such substrate loss results in high insertion loss in the T/R switch and low gain in the PA. However, the implementation of the PA and T/R switch in a standard CMOS process offers two very attractive challenges. Firstly, once the PA and T/R switch are designed in a CMOS process, the whole transceiver can be integrated into a single chip. Secondly, this will reduce the cost of the RF transceiver in two ways: (i) The reduction of the component count, and (ii) The implementation of these components on a low cost process.

Thus, we can see that this project has a good commercial value. However, due to the low resistive substrate, high knee voltage, low breakdown voltage, and low Q on chip inductor in the CMOS process, the design will be challenging.

1.5 Organization of the thesis

This thesis is organized into nine chapters. Chapters 2 and 3 provide a literature survey and a background of the Power Amplifier (PA) and T/R switch. Chapter 4 introduces the limitations of CMOS technology. Chapter 5 describes the design of the T/R switch. Chapters 6, 7 and 8 describe the details of the PA and T/R switch design, including the schematic, simulation, package, PCB design and testing. Chapter 9 gives the conclusion and recommendations.

2 Fundamentals of Power Amplifier

Generally, the requirements of Power Amplifier are high output power, high linearity, high power gain and high PAE (Power Added Efficiency).

2.1 Power Amplifier Terminologies

Some terminologies related to RF Power Amplifiers are introduced in this part, including non-linearity, harmonic distortion, P1dB (1dB compression point), IP3 (3rd order intercept point), ACPR (Adjacent Channel Power Ratio), EVM (Error Vector Magnitude), efficiency, Load-pull, matching and so on.

Non-linearity

All real-life systems exhibit some degree of nonlinearity. Hence the output response of a system can be described by equation (2.1). The coefficients a_n are assumed to be frequency independent. For analytical simplicity, terms higher than the third power are often neglected in normal calculations.

$$v_o = a_0 + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \dots \quad (2.1)$$

Many linearity related problems can be analyzed by substituting

$$v_i = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t \quad (2.2)$$

into equation (2.1)

After the expansion and arrangement of the frequency components at the fundamental frequencies, we have:

$$\text{At } \omega_1: \left(a_1 + \frac{3}{2} a_3 A_2^2 + \frac{3}{4} a_3 A_1^2 \right) A_1 \cos \omega_1 t \quad (2.3)$$

$$\text{At } \omega_2: \left(a_1 + \frac{3}{2} a_3 A_1^2 + \frac{3}{4} a_3 A_2^2 \right) A_2 \cos \omega_2 t \quad (2.4)$$

Second-order terms:

$$\text{At } 2\omega_1: \left(\frac{1}{2} a_2 A_1^2 \right) \cos 2\omega_1 t \quad (2.5)$$

$$\text{At } 2\omega_2: \left(\frac{1}{2} a_2 A_2^2 \right) \cos 2\omega_2 t \quad (2.6)$$

$$\text{At } \omega_1 \pm \omega_2: (a_2 A_1 A_2) [\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t] \quad (2.7)$$

Third-order terms:

$$\text{At } 3\omega_1: \left(\frac{1}{4} a_3 A_1^3 \right) \cos 3\omega_1 t \quad (2.8)$$

$$\text{At } 3\omega_2: \left(\frac{1}{4} a_3 A_2^3 \right) \cos 3\omega_2 t \quad (2.9)$$

$$\text{At } 2\omega_1 \pm \omega_2: \left(\frac{3}{4} a_3 A_1^2 A_2 \right) [\cos(2\omega_1 + \omega_2)t + \cos(2\omega_1 - \omega_2)t] \quad (2.10)$$

$$\text{At } \omega_1 \pm 2\omega_2: \left(\frac{3}{4} a_3 A_1 A_2^2 \right) [\cos(\omega_1 + 2\omega_2)t + \cos(\omega_1 - 2\omega_2)t] \quad (2.11)$$

Harmonic distortion

If a sinusoid is applied to a nonlinear system, the output generally exhibits frequency components that are integer multiples of the input frequency. The output component whose frequency is equal to the input frequency is called the “fundamental”, and the other components are called “harmonics”. The higher power of the harmonics the nonlinear the system is. Usually the ratios of the 2nd and 3rd harmonics to the fundamental are also important specifications related to linearity.

1dB Compression Point

The input level at which the small-signal gain is reduced by 1dB is called 1dB compression point. For a single frequency input signal, $A_2 = 0$ in equation (2.3), by equating the coefficient of equation (2.3) to 1dB less than the small-signal gain, a_1 , we have:

$$20 \log a_1 - 1dB = 20 \log \left(a_1 + \frac{3}{4} a_3 A_{-1dB}^2 \right) \quad (2.12)$$

After solving the above equation, we have

$$A_{-1dB} = \sqrt{0.145 \frac{|a_1|}{|a_3|}} \quad (2.13)$$

The 1dB compression is typically measured in dBm.

The most common used unit for power is dBm, which is defined as:

$$P_{dBm} = 10 \log \frac{P}{1mW} \quad (2.14)$$

where P is in mW.

IP3

The third-order intercept point (IP3) is found by a two-tone test. As the amplitudes of the two equal sinusoidal test tones at ω_1 and ω_2 in equation (2.2) are increased, the third-order intermodulation distortion (IMD) products will be increased at a rate of A^3 as shown in equation (2.10) and (2.11). IP3 is the point at which the amplitude of the third-order IMD equals that of the fundamental. The input level at which this occurs is called the input referred third-order intercept point, IIP3. The fundamental amplitude is a linear extrapolation of the small signal fundamental curve without the effect of

gain compression. By setting the amplitude of the 3rd order output component or the coefficient of equation (2.10) equal to the output small signal amplitude $a_1 A$, we have

$$a_1 A_{IP3} = \frac{3}{4} a_3 A^3_{IP3} \quad (2.15)$$

$$A_{IP3} = \sqrt{\frac{4}{3} \frac{|a_1|}{|a_3|}} \quad (2.16)$$

By comparing equations (2.13) and (2.16), we obtain

$$\frac{A_{IP3}}{A_{-1dB}} = \frac{\sqrt{4/3}}{\sqrt{0.145}} \approx 9.6dB \quad (2.17)$$

ACPR (Adjacent Channel Power Ratio)

The Adjacent Channel Power Ratio (ACPR) is an increasingly critical measurement, particularly for the Power Amplifier. It is an important specification for the linearity of a Power Amplifier.

A popular measurement of ACPR is to find the ratio of the output power of desired channel in a small bandwidth centered around the carrier to the power in the adjacent channel. The small bandwidth is equal to the bandwidth of the adjacent channel signal.

EVM (Error Vector Magnitude)

Figure 2.1 shows the diagram of EVM, which illustrate the definition of EVM.

Figure 2.1 Diagram for EVM

EVM is another specification related to linearity. When input signals become strong, the system's nonlinearity will cause the signal to deviate from the ideal point in the constellation. EVM is a measure of the amplitude and phase difference between the (ideal) waveform and the measured waveform. The difference is called the error vector, usually referred to with regard to M-ary I/Q modulation schemes like QPSK, and shown on an I/Q "constellation" plot of the demodulated symbols.

Efficiency

PAE (Power Added Efficiency) and Power efficiency are popularly used for Power Amplifiers, and show how efficiently DC power is converted to RF signal power.

$$\text{Power Added Efficiency: } PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} \quad (2.18)$$

$$\text{PA's Efficiency: } \eta = \text{efficiency} = \frac{P_{OUT}}{P_{DC}} \quad (2.19)$$

Power Gain and Voltage Gain

Power Gain shows how many times the RF input signal power is amplified, and is usually specified in dB.

$$G_P = 10 \log\left(\frac{P_{out}}{P_{in}}\right) = 10 \log\left(\frac{V_{out}^2 / 2R_{out}}{V_{in}^2 / 2R_{in}}\right) \quad (2.20)$$

Voltage Gain shows how many times the RF input signal voltage is amplified.

$$G_V = 20 \log\left(\frac{V_{out}}{V_{in}}\right) \quad (2.21)$$

It can be seen from the above that, only when $R_{in}=R_{out}$, $G_P=G_V$.

Gain match, Power match and Load-Pull

In a typical situation, the conjugate match yields a 1dB compression power of about 2dB lower than that which can be obtained by the correct power tuning [53]. In order to get the maximum linear output power, we need to do a power match for the output of the Power Amplifier.

Load-pull measurement is a very popular method to find the optimum load impedance of the PA for the maximum linear output power. Usually Power Amplifier is not directly terminated with 50Ω since this would not result in the optimum linearity. Because the power amplifier must be interfaced with a 50Ω load, an impedance transmission network is needed.

Back-off and PAR (Peak to Average Ratios)

Figure 2.2 illustrates power amplifier output back-off. The back-off is the voltage difference between the operation point and the saturation point.

Figure 2.2 Simplified input-output amplitude characteristics for a power amplifier

The peak to average ratio (PAR) of the transmitted waveform determines the bias point and efficiency of the transmitter PA and the resulting amplifier efficiency. For a given required power output, the greater the peak to average ratio, the greater the PA back-off.

In modern communication systems, multi-carrier signals, and even single-carrier signals such as those employing WCDMA (Wide-band Code-Division Multiple Access) can have a peak-to-average ratio of 10dB or above.

Load Mismatch

Load Mismatch determines the Maximum VSWR the PA can support before damaging the PA. Usually it is considered with ACPR, ie. the impact of load-mismatch on ACPR.

2.2 High Power Added Efficiency (PAE) methods

There are three ways to improve the power efficiency:

A Adjusting the bias conditions in the output stage of the power amplifier

As the transmitted power in a wireless system is below the maximum for most of the transmission period, adjusting the output power by adjusting the biasing condition in the Power amplifier can improve the efficiency of the power amplifier. In Figure 2.3, the circuit has the power detector to adjust the biasing condition based on the input power [11]. This architecture is widely used in commercial power amplifiers for its easy realization.

Figure 2.3 Architecture of bias control high efficiency [11]

B Vary the supply voltage (by DC-DC Power Converter)

In Figure 2.4, the circuit varies the supply voltage to improve the efficiency of the power amplifier. A synchronous buck DC-DC converter is integrated to provide the supply voltage, while tracking the envelope of the RF input signal [27]. The advantage is its performance is close to peak-power efficiency. The disadvantage is that the large converter BW (Band-width) and higher switching frequency result in degraded light-load efficiency [12].

Figure 2.4 Envelope following system simplified block [27]

C Parallel Amplification for Efficient Power Control

Usually a fixed matching network is used at the output of the power amplifier. The power amplifier can only be optimized for a specific operating condition in terms of the biasing conditions and supply voltage. Any deviation from this condition results in a degraded power efficiency. A typical amplifier only achieves its peak efficiency at a specific output power level, usually the maximum. Statistically, the transmitted power in a wireless system is below its maximum.

In Figure 2.5, the architecture employs three amplifiers, the outputs of which are binary weighted and combined in a power-combining network implemented using quarter-wave length transmission lines. The capability to turn off each individual amplifier, with no penalty on power dissipation, essentially provides high efficiency over a broad range of output power [10].

Figure 2.5 Parallel-amplifier architecture [10]

This architecture, however, occupies a large die area, and the $\lambda/4$ transmission line is too long to be implemented on chip at 2.45GHz, so it has to be implemented off-chip on PCB.

2.3 High linearity methods

A Cartesian Feedback

Figure 2.6 shows the architecture of Cartesian feedback. Cartesian feedback amplifiers have been seen to provide as much as 50 dB of linearization; i.e the magnitude of undesired spectral components adjacent to the desired signal, due to inter-modulation, spectral regrowth, or other phenomena, can be reduced by 50 dB or more through this technique [16].

Figure 2.6 Cartesian Feedback Architecture [16]

Several papers have also reported linearizing bandwidths on the order of several hundred kHz inside operating bandwidths of tens of MHz. However, the linearization is only as good as the matching of both gain and phase between the up-converting modulator in the forward path and the down-converting modulator in the feedback

path. The stability of the loop must be guaranteed, which sets tight requirements on the loop gain and loop bandwidth. Both of these requirements affect the amount of linearization provided as well as the available linearizing bandwidth. Thus a very tight control must be exerted over the components in the loop as well as the overall performance of the loop.

B Predistortion and Adaptive Predistortion

In Figure 2.7, the Predistortion method of linearization is similar to the Cartesian feedback method, in that it looks to modify the signal at the input of the PA, but moves the linearization one step back in the transmitter chain [17].

Figure 2.7 Digital Predistortion Architecture [17]

The Predistortion method makes use of a DSP and stores known predistortion coefficients in a lookup table (LUT), which can be used to predistort the input digital bitstream to create a signal that will generate a linear representation of the desired input. In general, this method is difficult to implement [18].

This method can be useful when the system already incorporates a DSP, which may remain unused or partially unused in this transmit time. So the disadvantage is

that it includes DSP increasing the complexity and cost of the system.

C Feed Forward

This method does not use feedback, as the name implies, it uses a feed-forward technique in order to linearize the PA output [17]. As shown in Figure 2.8, the RF input is split into two paths.

Figure 2.8 Feed Forward Architecture [17]

The first path contains the nonlinear power amplifier which is to be linearized. The nonlinear signal is then sensed at the output of the PA and subtracted from a delayed version of the original RF input. The nonlinearity of the PA output is finally removed by subtracting the output of the error amplifier from a delayed version of the PA output.

D Diode linearizer

Figure 2.9 shows the schematic of the diode linearizer in a PA.

Figure 2.9 Schematic of the diode linearizer in PA [9]

The integrated diode linearizer in HBT PA can effectively improve the gain compression and phase distortion performances by compensating the effects suffered from the gate dc bias level V_{gs} which decreases as the input power increases [9]. The method is easy to implement, but the linearity improvement is limited.

2.4 Classification of Power Amplifier

A Linear Power Amplifiers

Class A

Figure 2.10 shows the operation of a class A PA. In Class A operation, the transistor is in its active region for the entire input cycle, and thus is always conducting current. As such, the device maintains approximately the same gain throughout the entire active region, and in the case of a MOS device, is linear in that region. As most popular wireless systems require high linearity power amplifiers, Class A PA is generally used.

Figure 2.10 Class A PA Operation [6]

In theory, the maximum theory efficiency is 50%, but the efficiency of a practical PA can reach no more than 40%. However, in the case of an FET, it is not possible to have an output swing of VDD and still keep the device in saturation. As a result, the peak efficiency of an FET Class A PA is significantly lower. Reported PA's of this nature have an efficiency which is limited to around of 30% [19].

Class B

Figure 2.11 shows the implementation of class B Power Amplifier. In a class B structure, there are two devices, one which supplies current to the load (pushes current into the load), and one which "removes" current from the load (pulls current from the load). The ideal maximum efficiency of class B PA is 78.5% [6]. This structure is usually called a "push-pull" structure. During the positive half of the signal swing, one device will pull current from the load, and during the negative half of the signal swing the other device will push current into the load. Class B PA is only a concept, the practical implementation is Class AB PA.

Figure 2.11 Class B PA Implementation [6]

Class AB

However, in situations where the linearity is still an important requirement, it is desirable to utilize the push-pull concept and yet at the same time to minimize the cross-over distortion inherent in a class B structure. This idea is implemented in the Class AB structures, which, as its name implies, is a cross between Class A and Class

B structure. The idea here is to use a push-pull structure, where each device is biased slightly above the threshold. Circuit implementations of a Class AB PA are similar to those of the Class B architecture; what differs is the biasing and output waveforms. The waveforms of a class AB PA are shown in Figure 2.12.

Figure 2.12 Class AB PA waveforms

Table 2-1 shows the performances that CMOS PA attained in the previous research.

It can be seen that Class AB are very popular in CMOS PA design and usually get a PAE no more than 55%.

Author	Class	Application	Output Power	PAE	Process (μm)	Year
Cheng-Chi Yen[9]	AB	2.45GHz	20dBm P1dB	28%	0.25	2004
I.Aoki [13]	B	1.9GHz	2.8W	50%	0.18	2003
Tangtat Hung [54]	E	2.65GHz	25dBm	62%	0.25	2003
Carsten Fallesen [55]	AB	GSM1800	30.4dBm	55%	0.35	2001
Chengzhou Wang [56]	AB	1.9GHz	100mW	40%	0.6	2001
D. Heo [24]	AB	1.9GHz	26dBm	48%	0.8	2001
A. Giry [57]	AB	1.9GHz	23.5dBm	35%	0.35	2000

Table 2-1 Literature Research of CMOS PA

B Non-linear Power Amplifiers

The previous three classes are examples of linear structures, where the output amplitude and phase are (nominally) linearly related to the input amplitude and phase.

However, in applications where the linearity is not critical, while the efficiency is more important, e.g. the information to be transmitted is not contained in the amplitude of the output, a non-linear power amplifier in which the efficiency is optimized should be used. This leads us to the other classes of power amplifiers.

Class C

A Class C Power Amplifier is the most basic topology of the non-linear Power Amplifiers used at RF frequencies. This architecture takes the idea of a Class B PA, where the device is biased at the edge of conduction. In this case, it prescribes that the PA be biased below threshold [6][8] as shown in Figure 2.13.

Figure 2.13 Class C PA Implementation [6]

Class D

If the transistors act like perfect switches, then the theoretical efficiency of the Class D amplifier is 100%. However, at RF frequency, the MOS transistors do not behave as switches. The nonzero saturation voltage guarantees a static dissipation in the switches. Hence, switch-mode PAs function well only at frequencies substantially below f_T . Furthermore, the transformer action attempts to apply the full supply voltage across the device that is not really off, so the V-I product can be quite large.

A major drawback of the transformer-coupled PA as shown in Figure 2.14 is its linearity requirements for the output balun transformer which make it unsuitable for high-frequency applications.

Figure 2.14 Class D PA Implementation [58]

The output balun transformer in the transformer-coupled CMCD (Current Mode Class D) PA [58] is required to be linear at least from DC to three times the fundamental frequency if I_{tot} (total current at output) should look like a square wave. Realizing balun transformers for high-frequency applications satisfying this requirement is next to impossible. Therefore, the output balun transformer is moved to

the right of the parallel RLC tank which confines the linearity requirement to a narrow band at the fundamental frequency.

Class E

Figure 2.15 shows the implementation of a class E Power Amplifier.

Figure 2.15 Class E PA Implementation [7]

Class E PA was originally designed for use with PA's devices with non-negligible turn-on and turn-off times, where the overlap between the output current and voltage waveforms was significant for the frequency of operation, enough to cause unnecessary power to be consumed within the device.

Because of the poor power capability and the reduced efficiency due to switch turn-off losses, practical implementations of the Class E amplifier do not exhibit any significant improvement over well-executed designs of other types (e.g., Class F PA) [7].

Class F

Figure 2.16 shows the implementation of a class E Power Amplifier.

Figure 2.16 Class F PA Implementation [7]

The idea is that the device will see a non-zero load impedance for odd harmonics and a zero impedance for even harmonics, thus the waveform at the output of the device will be the sum of the first and third harmonics of the fundamental frequency, which make up the first two terms in the series expansion of a square wave. In this way, the output voltage waveform is near to zero at the time when the current is flowing, decreasing the power lost through the device. The waveform at the output is still limited to the fundamental frequency, since the impedance at the actual output is tuned to the fundamental.

The theoretical efficiency of this PA is also 100%. In practice, an efficiency superior to that of Class E PA can be achieved. Additionally, Class F PA has a substantially better normalized power-handling capability [7].

C Analysis of Class A, B, and C Power Amplifiers

Shown in the Figure 2.17 is a basic two-stage linear RF PA which may be biased for operation as Class A, or B, or C.

Figure 2.17 Conventional 2-stage PA

For classes A, B, and C, the transistor is operated as a transconductor rather than as a switch. Its drain current, $i(\theta)$, is modeled as the net positive portion of a cosine wave of peak amplitude i_m superimposed upon a dc bias current I_{dq} that is negative and less than i_m for Class C, zero for Class B, and positive and greater than i_m for Class A.

$$\begin{aligned} i(\theta) &= i_m \cos \theta + I_{dq} \dots \dots \dots -\frac{y}{2} \leq \theta \leq \frac{y}{2} \\ i(\theta) &= 0 \dots \dots \dots \text{otherwise} \end{aligned} \quad (2.22)$$

where y is the conduction angle.

A Fourier series representation of the drain current is:

$$i(\theta) = i_{dc} + \sum_{n \geq 1} i_n \cos n\theta \quad (2.23)$$

$$\text{where } i_{dc} = \left(\frac{I_m}{\pi}\right) \left(\sin \frac{y}{2} + \frac{y}{2} \bullet \frac{I_{dq}}{I_m}\right) = \left(\frac{I_m}{\pi}\right) \left(\sin \frac{y}{2} - \frac{y}{2} \cos \frac{y}{2}\right) \quad (2.24)$$

and

$$i_n(y) = \frac{I_m}{2\pi} \left(\frac{2}{n+1} \sin(n+1) \frac{y}{2} + \frac{2}{n-1} \sin(n-1) \frac{y}{2} \right) + \frac{2I_{dq}}{n\pi} \sin n \frac{y}{2} \quad (2.25)$$

In order to obtain the maximum voltage swing at the drain, a specific load resistance must be presented to the active device. For a given conduction angle y , the product of this load resistance R_{opt} and the peak instantaneous value of the fundamental component of the drain current, should equal the desired maximum voltage swing. Hence, we have:

$$V_{dd} - V_{dsat} = i_1(y) \times R_{opt} \quad (2.26)$$

Where $i_1(y)$ is the amplitude of the fundamental current for conduction angle y .

With the optimum load impedance presented to the PA output, the maximum RF voltage swing $V_{dd} - V_{dsat}$ is obtained at the drain. Hence, the drain efficiency which is the ratio of the RF power to the DC power is easily derived as:

$$\eta_D = \frac{V_{dd} - V_{dsat}}{V_{dd}} \bullet \frac{y - \sin y}{4 \left(\sin \frac{y}{2} - \frac{y}{2} \cos \frac{y}{2} \right)} \quad (2.27)$$

RF power is one-half of the products of the peak RF voltage swing and the peak RF current given by (2.25) for $n=1$. DC power is the product of the supply voltage and average current given by (2.24).

Figure 2.18 shows the drain efficiency vs. the conduction angle, where R_{opt} varied for maximum output voltage swing (V_{dd}) at each point.

Figure 2.18 Drain Efficiency vs. conduction angle [4]

Figure 2.19 shows the drain efficiency vs. conduction angle, where the R_{opt} is fixed.

Figure 2.19 Drain Efficiency vs. conduction angle (R_{opt} fixed) [4]

The output power is expressed as:

$$P_o = \frac{1}{2} v_o i_1 = \frac{1}{2} (V_{dd} - V_{dsat}) \frac{I_m}{2\pi} (y - \sin y) \quad (2.28)$$

Figure 2.20 shows the PA output power (normalized to Class A) versus conduction angle.

Figure 2.20 PA output power (normalized to Class A) versus conduction angle [4]

Figure 2.21 shows the PA normalized fundamental to the third harmonic component ratio versus conduction angle.

Figure 2.21 PA normalized fundamental to third harmonic component ratio versus conduction angle [4]

For Bluetooth and IEEE802.11b/g standards, modern modulation scheme requires a very high linearity of the Power Amplifier, and so the linear PA architecture should be used.

3 T/R switch background

Only recently, the research on the CMOS T/R switch has gained attention. Current results show that the insertion loss, power handle capability and isolation of the CMOS T/R switch are comparable with that of GaAs T/R switch and Pin diode switch [5]. Two types of CMOS T/R switches have shown good performances.

3.1 SPDT T/R Switch in CMOS Process

Two typical circuit configurations for Si-CMOS SW, the series- and shunt/series-type SWs, are shown in Figure 3.1(a) and (b).

Figure 3.1 Circuit configurations for T/R-switches [2]:
(a) Series type and (b) shunt/series type.

The shunt/series-type SW is also known as SPDT (Single Pole Double Throw) switch. In this figure, the FETs, M1 and M2, form the series arms and M5 and M6 form the shunt arms. The FETs, M3 and M4 comprising the control circuit, work in a

complementary fashion, consuming no drain current.

In the case of CMOS switches fabricated on a low-resistivity substrate, enlarging the gate width of M1 and M2 reduces the on-state resistance, thus improving the insertion loss. On the other hand, large transistors will have larger substrate parasitics which cause a degradation of the insertion loss as well as the isolation. This property implies that a proper gate width can provide the minimum insertion loss for the CMOS switches on the low-resistivity substrate. In the CMOS-switch design, it is, therefore, essential to determine the optimum gate width which provides the minimum insertion loss and sufficient isolation level. This subsection first describes the small-signal equivalent analysis of the switch and the analytical expression to calculate the optimum gate width based on the analysis.

The circuit schematics and their on- and off-state equivalent circuits for series and shunt arms used for the switch are illustrated in Figure 3.2. In this figure, the resistances R_s and R_{s2} and capacitances C_s and C_{s2} represent parasitic resistances and capacitances due to the low-resistivity substrate. The resistances R_a and R_{a2} and inductances L_a and L_{a2} are the on-state resistances and parasitic inductances. The resistances R_b and R_{b2} and capacitances C_b , C_{b0} , C_{b1} , and C_{b2} denote the off-state resistances and capacitances [2].

Figure 3.2 Circuit schematics and their on- and off-state equivalent circuits for series and shunt arms [2]:

- (a) Series arm circuit schematic, (b) series arm on-state circuit, (c) series arm off-state circuit, and (d) shunt arm circuit schematic, (e) shunt arm on-state circuit, and (f) shunt arm off-state circuit.

Figure 3.3(a) and (b) show the small-signal equivalent circuits for the series- and the shunt/series-type switches comprising the circuit schematics of Figure 3.2. Both figures represent the equivalent circuits in transmit mode. As shown in Table 3-1, a low-resistivity substrate produces an R_s of 165Ω and a $1/\omega C_s$ of about 390Ω for the $200\text{-}\mu\text{m}$ gate width series arm at 2.4 GHz . These parasitics cannot be neglected for the usual $50\text{-}\Omega$ system because they cause a relatively high loss. Therefore, it is easily predicted that the shunt/series-type SW basically has a larger insertion loss than the series-type one, as will be described later.

Series arm				Shunt arm			
ON		OFF		ON		OFF	
R_a [Ω]	6.5	R_b [Ω]	10^5	R_{a2} [Ω]	4.5	R_{a3} [Ω]	165
L_a [nH]	0.07	C_b [pF]	0.1	L_{a2} [nH]	0.08	C_{s2} [pF]	0.20
R_s [Ω]	165	C_{b0} [pF]	2.0	R_{s2} [Ω]	7.0	C_b [pF]	6.5
C_s [pF]	0.17	R_s [Ω]	165	C_{s2} [pF]	0.80		
		C_s [pF]	0.17				

Table 3-1 Example of the equivalent circuit parameters derived from the measured S-parameters for the 200- μm gate width series and shunt arms [2]

Figure 3.3 Equivalent circuits for T/R-switch in transmit mode [2]:

- (a) series-type and (b) shunt/series-one, and simplified equivalent circuits for the series-type switch to calculate transfer characteristics in transmit mode: (c) insertion loss between TX and ANT ports and (d) isolation between TX and RX ports[2].

To calculate the transfer characteristics for the series-type switch and determine the optimum gate width, we can simplify the circuit schematics shown in Figure 3.3(a) under the conditions that $1/\omega C_b$, $1/\omega C_{b0} \gg Z_0$ ($=50\Omega$), and $\omega L_a \ll Z_0$. The resultant schematics are shown in Figure 3.3(c) and (d). Based on the simplified schematics, we can calculate both the insertion loss between the TX and ANT ports and the isolation

level between the TX and RX ports. From Figure 3.3(c), the insertion loss, I_L , for the series-type SW is expressed by Equation (3.1), where $Q_s = 1/\omega C_s R_s$ and $Z_0 = 50\Omega$.

$$I_L = \left| \frac{2Z_o R_s^2 \{ (1 - Q_s^2) - j2Q_s \}}{2Z_o^2 R_a + 3Z_o (R_a + Z_o) R_s + (R_a + 2Z_o) R_s^2 (1 - Q_s^2) - jR_s Q_s \{ 3Z_o (R_a + Z_o) + 2(R_a + 2Z_o) R_s \}} \right| \quad (3.1)$$

We should note that approximations such as $\omega C_s R_s \ll 1$ or $\omega C_s R_s \gg 1$ [43] are not appropriate for the derivation of this equation. The reason is that the parasitics R_s , and $1/\omega C_s$, on the low-resistivity substrate are comparable with Z_0 , and the proper balance between these parasitics and on-state resistance yields the minimum insertion loss. Assuming that R_s and R_a are inversely proportional to the gate width W for M1 and M2, and C_s is proportional to W , is rewritten as follows [2]:

$$I_L = \frac{2Z_o (1 + Q_s^2)}{\sqrt{AW^2 + \frac{B}{W^2} + CW + \frac{D}{W} + E}} \quad (3.2)$$

$$\begin{aligned} A &= \left(\frac{Z_o^2}{K_2} \right)^2 \{ (2K + 3)^2 + 9Q_s^2 \} \\ B &= K_1^2 (1 + Q_s^2)^2 \\ C &= 2 \left(\frac{Z_o^2}{K_2} \right) Z_o \{ (2K + 3) [2(1 - Q_s^2) + 3K] + 3Q_s (3K + 4) \} \\ D &= 2Z_o K_1 \{ (1 - Q_s^2) [2(1 - Q_s^2) + 3K] + 2Q_s^2 (3K + 4) \} \\ E &= Z_o^2 \{ [2(1 - Q_s^2) + 3K]^2 + 2K(2K + 3)(1 - Q_s^2) + Q_s^2 (3K + 4) + 12Q_s^2 K \} \end{aligned}$$

where K_1 and K_2 are constants, $R_a = K_1/W$, $R_s = K_2/W$, and $K = K_1/K_2$. In the denominator of equation (3.2), the following relationship is satisfied over a practical parameter range such as listed in Table 3-1.

$$A \cdot W^2 + \frac{B}{W^2} \ll C \cdot W + \frac{D}{W} \quad (3.3)$$

The optimum gate width W_m is approximately derived from the right term of Equation (3.3) using the relationship between the arithmetic and geometric means

$$W_m = \sqrt[4]{\frac{D}{C}} \quad (3.4)$$

Thus, Equation (3.4) reveals that there is a proper gate width W_m , which provides the minimum insertion loss for the Si-switch on the low-resistivity substrate.

Based on Figure 3.3(d), the isolation level for the series-type SW is also expressed by the following equations:

$$Iso = \left| \frac{-4Z_o \omega C_b R_s^2 Q_s - j2Z_o R_s^2 \omega C_b (1 - Q_s^2)}{F} \right| \quad (3.5)$$

$$F = 2R_s^2 (1 - Q_s^2) + 5Z_o R_s + 3Z_o^2 + 2\omega C_b Z_o R_s Q_s (R_s + 2Z_o) - jR_s Q_s (4R_s + 5Z_o) + j\omega C_b Z_o R_s \times \{R_s (1 - Q_s^2) + Z_o\}$$

3.2 CMOS T/R Switch with LC-tuned Substrate Bias

Figure 3.5 shows CMOS T/R switch with LC-tuned substrate bias. This CMOS T/R switch is designed in a $0.18\mu\text{m}$ digital CMOS process with 1.8V supply and six metal layers.

Figure 3.5 CMOS T/R switch with LC-tuned Substrate bias [5]

In the TX mode, V_{ctrl} is set to V_{dd} turning on M1 and M2. With the drain of M2 pulled to Gnd, L_2 and C_{2a} form a parallel tank that resonates at 5.2GHz. Thus, the receive path to presents a high impedance of several hundred ohms, assuring that the TX signal leakage to the receive path is small. Similarly, the L_1 - C_1 pair, designed to resonate at 5.2GHz, makes the substrate node of M1 high-impedance ($\sim 2\text{k}\Omega$) thus minimizing substrate loss. This resonance combined with the large gate bias resistor (Rb_1) causes M1 to behave like a “floating” pass-gate. This allows a large ac voltage to be applied at the TX port without causing any two terminals of M1 to develop a voltage difference larger than V_{dd} . At low frequencies less than several hundred

megahertz, L_I shorts the substrate of M1 to ground and thus eliminates any latch-up issue. In the RX mode, V_{ctrl} is set to Gnd turning off M1, which minimizes signal leakage to the TX path. The π -network of $C2_a$ - L_2 - $C2_b$ matches the antenna to the LNA input. While the prototype is designed to operate in a 50Ω environment, the π -network components can be adjusted to match different impedances at the RX (LNA) port. The bias resistors, Rb_3 and Rb_4 , and the inverter are required only for testing purposes and can be eliminated when the switch is integrated with the LNA and PA [5].

In the transmit mode, the switch achieves a 1.5dB IL (Insertion Loss), 30dB isolation, and a 28dBm 1dB compression point. In the receive mode, the above performance is 1.4dB, 15dB, and 12dBm, respectively. The switch uses an LC-tuned substrate biasing technique [5] to dramatically improve the large-signal handling capability.

The P-1dB compression point of 28dBm with a control Voltage 1.8V is very high and even better than that obtained by GaAs and Pin diode T/R switches. The novel technology used here is the LC tuned substrate biasing. In the transmit mode, a good isolation of 30dB isolation is obtained, but any variation of the value of capacitors and inductors can increase the insertion loss. In receive mode, the isolation is only 15dB, as there's no discharge path for power amplifier.

TX and RX ports. Consequently a tradeoff exists between reduction of insertion loss on one hand and degradation of the isolation on the other.

One of the disadvantages of using GaAs FET is their relatively low power handling capability (compared to PIN diodes)[46]. In order to see this, refer back to the simple switch described in Figure 3.6. During TX mode, the gate voltage of FET1 and 3 is left at 0V while a negative gate voltage is applied to FET2 and 4 to turn them off. However, if a large negative voltage signal is present at the TX input, then the gate-to-drain voltage of FET4 may become smaller than its pinch-off voltage (V_p), thereby causing the transistor to conduct and clipping the input. This condition is also true for FET2 where a large RF signal may be present on the antenna. In [47], the maximum transmit power $P_{\max}$ that can be delivered to the switch was found to be

$$P_{\max} = 2(V_c - V_p)^2 / Z_0 \quad (3.6)$$

where V_p is the pinch-off voltage of the switch FET, V_c is a control voltage for off-state FET's and Z_0 is the characteristic impedance of the system.

In order to get around this limitation, T/R switches using stacked gates, LC resonators, feed-forward capacitors or a combination of them have been proposed [46], [47].

3.4 Pin-diode T/R switch

Figure 3.7 shows a basic architecture for a transmit/receive (T/R) switch [44]. DC blocking capacitors are placed at each of the TX, RX and antenna nodes (since the LNA and PA connected to these nodes will, in general, require their own specific DC bias).

Figure 3.7 Pin-diode T/R Switch [44]

The operation of the switch is as follows:

TX Mode: V_{con} is at a positive voltage; both diodes are forward biased and are at low impedance. There is a low impedance path between the TX and antenna ports but a high impedance looking from the TX to the RX port (due to $\lambda/4$ impedance transformation).

RX Mode: V_{con} is at 0V or a negative voltage; both diodes are reverse biased and are at high impedance. As a result, the TX and antenna ports are isolated and a low impedance path exists between the antenna and RX.

One thing to recognize about T/R switches utilizing PIN diodes is that they consume DC power during the transmit operation. Because of this and other factors

(slower switching speed, more complicated bias networks), they have largely been replaced by GaAs FETs in applications where low power consumption is critical (as in battery-powered mobile communication devices).

3.5 Conclusion of T/R switch

Table 3-2 shows the comparison of some T/R switches in the literature.

Specification	PIN Diode TX & RX [61]	MESFET TX & RX [62]	CMOS SPDT TX & RX [1]	CMOS LC_tuned substrate [5]	
				TX	RX
Insertion Loss(dB)	1.0	1.2	1.0	1.5	1.4
Isolation(dB)	15	26	40	30	15
PI dB(dBm)	30.0	31.0	12.0	29.0	11.5
Return Loss(dB)	14	15	N/A	30	11
Control Voltage(V)	+/-8.0	0-3.0	0-3.3	0-1.8	0-1.8
DC Power(W)	~15m	<1m	<1m	<1m	0
Frequency(Hz)	5.6G	5.2G	0.9G	5.2G	

Table 3-2 Comparison of T/R switch

As described above, each type of switch has its advantage and disadvantage respectively. For the CMOS process, the SPDT T/R switch has a small insertion loss, but low power handling capability, smaller than 12dBm for 3.3V control voltage. The LC-tuned substrate biasing CMOS T/R switch can attain a very good power handling capability, but in receiver mode, the isolation is not good. What's more, it requires a triple-well process for LC-tuned substrate biasing.

4 Limitation of the CMOS Technology

4.1 Introduction

Although the CMOS process is cost-efficient and has been used for the base band and analog circuit successfully, it still poses a challenge for RF circuit design, especially for the Power Amplifier and T/R switch. Currently, most commercial products are still using a standalone Power Amplifier and T/R switch fabricated in the GaAs, GaP or SiGe Process.

In order to implement a Power Amplifier and T/R switch in CMOS process, one must understand the CMOS process limitation which is related to the requirements of the Power Amplifier and T/R switch.

Modern wireless communication systems use more complex modulation schemes, which require high linearity Power Amplifiers. For the wireless communication, all mobile systems have to rely on the battery. The Power Amplifier is the most power consuming device, so a high PAE (Power Added Efficiency) is required. A higher PAE, which means higher output power for smaller input power, can also be interpreted as a high gain. The T/R switch is an important circuit after the PA. A low insertion loss of the T/R switch is very critical to improve the efficiency of the whole transmitter and consequently extend the battery life. In order to reduce the interference from Transmitter to Receiver, good isolation is needed for T/R switch.

It can be summarized from above that high linearity, high PAE (Power Added Efficiency) and high power gain are preferred for a Power Amplifier; while for a T/R switch, low insertion loss and high isolation are required. Based on the requirements

of the Power Amplifier and T/R switch, the limitation of the CMOS technology, such as low f_T , high knee voltage, low substrate resistance, low breakdown voltage, low early voltage and low Q of on-chip inductor will be described into details.

A comparison of CMOS/Bipolar/BiCMOS(Si)/SOI/GaAs/SiGe BiCMOS is tabled as below.

Technology	Key Performance Attribute				
	Cost	Power	Integration	Design Margin for RF	Security of Supply
CMOS	Low	Moderate	High	Poor	High
Bipolar	Moderate	High	Low	Good	Moderate
BiCMOS(Si)	Moderate	Moderate	High	Good	Moderate
SOI	High	Moderate	High	Good	Poor
GaAs/Other	High	High	Low	Excellent	Low
SiGe BiCMOS	Moderate	Low	High	Excellent	High

Table 4-1 Comparison of varies process

4.2 f_T and low breakdown voltage

The f_T of a MOS device, which is the maximum frequency at which an equivalent current gain is possible [59], is given by

$$f_T = \frac{g_m}{C_{GS}} = \frac{\mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH})}{W L C_{OX}} \propto \frac{1}{L^2} \quad (4.1)$$

$$\text{where } I_D = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH})^2 (1 + \lambda_{DS}) \quad (4.2)$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{TH}) \quad (4.3)$$

The CMOS device has a very low f_T compared with that of the Si Bipolar, SiGe HBT BiCMOS, GaAs/InGaP HBT and InP HBT in a similar feature-size device, but in the modern CMOS process, the channel length scales down dramatically, and f_T has increased significantly making the CMOS process attractive to RF application at up to 10GHz.

However, the scaling down of the channel length of the CMOS device and the thickness of the gate oxide also decreases the breakdown voltage. As Power Amplifiers are designed to deliver power, a high voltage swing or high current swing or both are preferred. Thus, the low breakdown voltage V_{ds} is an important issue in Power Amplifier design. For a single-ended PA output stage, a basic calculation is derived from Figure 4.1 as follows:

Figure 4.1 Standard Class A PA implementation and waveform [6]

L_1 and C_1 will resonate at the operating frequency, which will present a very large impedance to the drain of the transistor. R_{OPT} is the optimum load impedance of the

Power Amplifier.

$$P_{OUT} = \frac{V_{peak}^2}{2R_{OPT}} \quad (4.4)$$

$$\text{or } P_{OUT} = \frac{I_{peak}^2 R_{OPT}}{2} \quad (4.5)$$

$$R_{OPT} = \frac{V_{peak}}{I_{peak}} \quad (4.6)$$

V_{peak} can't be higher than the supply voltage. In this project, the common 3V power supply is used. From equation (4.4), if the load impedance is 50Ω , the maximum output power is:

$$P = 10 \log\left(\frac{V_{peak}^2}{2R \times 0.001}\right) = 10 \log\left(\frac{3^2}{2 \times 50 \times 0.001}\right) = 19.54dBm \quad (4.7)$$

19.54dBm is close to the Bluetooth requirement of 20dBm for class 1 applications. But in this case, we haven't counted in the effect of knee voltage and some other effects, which will degrade the maximum output power greatly. Furthermore, in this scenario, we assume that the output swing is 3V, hence the maximum voltage at the drain of output transistor is about 6V, which enters the breakdown region of a CMOS transistor. The linearity and reliability of the operation of the Power Amplifier will be an issue when working near or in breakdown region.

The issue will be solved and described into details in Chapter 6.

4.3 High Knee voltage

The knee voltage (pinch-off voltage) divides the saturation and the linear region of a transistor and can be defined as, for example, at the 95% of point[53]. In some case, it is also mentioned as V_{dsat}

$$V_{knee} = V_{dsat} = \sqrt{\frac{2I_D}{\mu_n C_{ox} (1 + \lambda V_{DS}) (W/L)}} \quad (4.8)$$

When we consider about the Knee voltage, equation (4.4) will be changed to[53]

$$P_{OUT} = \frac{(V_{dd} - V_{Knee})^2}{2R_{OPT}} \quad (4.9)$$

Equation (4.9) shows that the output power can be reduced significantly.

For a power transistor(usually in GaAs or InP process)the Knee voltage is usually very low, about 10% to 15% of power supply [53]; while it can be as high as 50% of the supply for deep sub-micron technologies as shown in Figure 4.2[53].

Figure 4.2 Knee voltage of Power transistor and CMOS transistor [53]

If a 3V power supply is used, assume that V_{knee} is 0.2V for a power transistor and 0.8V for a CMOS transistor, then the output power are 18.9dBm and 16.85dBm respectively. It shows that a high Knee voltage of a CMOS transistor will degrade the

output power of a Power Amplifier greatly.

In order to reduce the knee voltage, from Equation (4.8), we can see that if increase the aspect ratio of W/L , then the knee voltage will be reduced. But for CMOS transistor,

$$V_{knee} = V_{dsat} = V_{GS} - V_{TH} \quad (4.10)$$

Hence, in order to reduce V_{knee} , we can reduce the gate biasing voltage V_{GS} . This will however reduce the maximum input signal of the PA for the Class A operation. It is different for SiGe HBT power transistor. Solutions about overcome high knee voltage will be described in the following chapter.

In T/R switch, the transistor will operate in triode region, the performance of T/R switch won't be affected by the high knee voltage.

4.4 Low substrate resistance

4.4.1 Low substrate resistance effect to PA

Due to the low substrate resistance of CMOS process, usually 1-20 ohm-cm, the substrate will easily conduct signals across great chip distances, potentially corrupting other blocks on the chip. Especially in the case of PAs which generate large amounts of output power and large signals into the substrate. In an integrated transceiver, there are several analog and digital circuits of the frequency synthesizer which are extremely sensitive to the PA. The PA signals can corrupt the frequency synthesizer, through a phenomenon known as LO pulling, in which the frequency synthesizer

reacts to signals injected at slightly different frequencies or with slightly different phases and locks to those injected signals rather than the crystal frequency. This distortion can severely impair the operation of the overall transmitter. In addition, if the PA is to be used in a full-duplex transceiver (i.e. where the transmitter and receiver can operate at the same time), extreme care must be taken such that the PA signals do not degrade the receiver sensitivity. Precautions must be taken so that the large substrate currents and voltages that the PA generates do not corrupt other portions of the circuit [8].

4.4.2 Effects of Low substrate resistance on the T/R switch

For the T/R switch, if the signal from Power Amplifier leaks to Receiver through substrate, it will degrade the isolation from the transmitter to the receiver. Currently, most commercial T/R switches are designed with the SOI CMOS process or high substrate impedance process in order to improve the T/R isolation performance.

4.4.3 Low substrate resistance effect to inductor

The substrate layer has a detrimental effect on spiral inductors built above it. Because the substrate has a low resistivity, it creates eddy currents on the substrate due to the magnetic field generated by the planar inductor structure. These eddy currents reduce the effective magnetic field, which in turn dramatically reduce the quality factor (Q) of the spiral inductors [40].

$$Q = \frac{\omega L}{R} = \frac{2\pi f L}{R} \quad (4.11)$$

In a CMOS process, at the frequency of 2.45GHz, if the Q of a 4nH inductor (2um metal thickness) is 6, we can calculate from equation (4.11) that $R=10.26\Omega$. This is a serious issue, especially for PA design. If a PA has an output power of 20dBm, and the efficiency is 30%, then the current will be about 111mA for a 3V power supply. If this large current goes through this inductor, the power wasted on the inductor will be about 60mW.

From the above, reasonable design should avoid any on-chip inductors in the final stage of the PA. Compared with low Q on-chip inductors, MIM (Metal-Insulator-Metal) capacitors have a Q value more than 20, which is more acceptable.

4.4.4 Improving substrate isolation by process technologies

There are some technology options for improving substrate isolation, such as shallow trench, deep trench, moat and P+ guard rings. Figure 4.3 illustrates these technology options.

Technology Options for Substrate Isolation

- Conventional "free" technology Options

- Shallow Trench
- Deep Trench (single and in mazes)
- MOAT - typically a high resistance area separating circuit blocks
- P+ Guard rings

- Technology Choices

- High resistivity substrates
- SOI (DC great isolation, AC poor)

Figure 4.3 Technology Options for Substrate Isolation [63]

5 Design of T/R switch

5.1 Introduction

The designs of a conventional CMOS T/R switch and a CMOS T/R switch with LC-tuned substrate bias are presented in this chapter. The T/R switch is an important front-end block in the RF transceiver characterized by the requirements of high power handling capability (i.e. high linearity), low insertion loss and high isolation.

Because of the low breakdown voltage and low substrate resistance of the CMOS process, it's difficult to achieve the above mentioned requirements. In this report, two CMOS T/R switches have been designed to cater for the requirement of 20dBm power handling capability, 30dB isolation from transmitter to receiver, and about 1.5dB insertion loss, which are compatible or better than specifications of many commercial products.

5.2 Conventional CMOS T/R switch — Design 1

In the modern CMOS process, as the channel length becomes shorter, the thickness of gate oxide becomes thinner, which causes the low breakdown voltage. For example, the variation of the channel versus the gate-source breakdown voltage is as follows: 2.4V for 0.13um CMOS process, 3V for 0.18um CMOS process, and 6V for 0.35um CMOS process. Thus, it is difficult to obtain a power handling capability higher than 20dBm with the modern deep submicron CMOS process [49].

Figure 5.1 shows the typical configuration of a CMOS T/R switch [1]. Transistors M1 and M2 perform the main switching function, while the shunt transistors M3 and

M4 are used to improve the isolation of the switch by grounding RF signals.

Figure 5.1 Typical CMOS T/R switch [1]

When V_{CTRL} is high, the T/R switch works in the transmit mode, transistor M_1 and M_4 will be on, and transistor M_2 and M_3 will be off, so the RF signal will go through M_1 from TX to ATN, where RX will be shorted to ground through M_4 to improve the isolation from TX to RX. When V_{CTRL} is low, the T/R switch works in receive mode, transistor M_2 and M_3 will be on, and transistor M_1 and M_4 will be off, so the RF signal will go through M_2 from ATN to RX, and TX will be shorted to ground through M_4 to improve the isolation from TX to RX.

If a 0.35um CMOS process is used, the common operating voltage is 3V. If $V_{CTRL}=3V$, the maximum voltage can pass the transistor is 3V, the drain and source of the transistor is biased at 1.5V, then $V_{peak}=1.5V$, for a 50Ω, the maximum power that can pass the switch is:

$$P = \frac{V_{peak}^2}{2R} = \frac{1.5^2}{100} = 22.5mW = 13.5dBm \quad (5.1)$$

It is far from our target 20dBm. As V_{peak} is limited by the supply voltage and the CMOS breakdown voltage, the only thing that can be changed here is R . If R is reduced to 12.5Ω , then the output power will be 19.5dBm, almost reach the design target. The solution can be described in Figure 5.2 and Figure 5.3.

Figure 5.2 Block diagram of impedance transformation in T/R switch

Figure 5.3 Schematic of the T/R switch with impedance transformation

Figure 5.2 shows the block diagram of the impedance transformation for the T/R switch and Figure 5.3 shows the schematic of the T/R switch with impedance

transformation.

As discussed in 3.1, when the transistor widths of M1 and M2 are increased, the channel resistance will decrease but the parasitic capacitance, which causes the RF signal leakage, will increase. There's an optimum point, where the sum insertion loss caused by resistance loss and capacitive coupling are minimum. From the simulation, the insertion loss becomes constant around this optimum point. Increasing the size of M3 and M4 can improve the isolation, but at the same time, it will also increase the insertion loss due to the increase of parasitic capacitance. Thus there is a trade off between the isolation and the insertion loss. From the simulation, the proper size of M3 and M4 can be found. This method is verified on silicon by the author in "Power Amplifier combined with T/R Switch".

Figure 5.4 shows the die photo of the T/R switch using only CMOS transistors of the IBM SiGe BiCMOS 5AM process, with a supply voltage of 3V. It implements the idea of using the impedance transformation in Figure 5.2.

Figure 5.4 Die photo of the T/R switch designed by author

5.3 CMOS T/R switch with LC-tuned substrate bias — Design 2

Figure 5.5 shows the simplified schematic of a T/R switch with LC-tuned substrate bias [5]. The detailed schematic was shown in Appendix. This architecture can improve the power handle capability significantly, but it requires a triple-well CMOS transistor process. To improve the large signal handling capability of the CMOS transistor process, a T/R switch with LC-tuned substrate bias is also designed. The triple-well CMOS transistor of the IBM SiGe BiCMOS 5HPE process (bipolar transistor not used) was used for this design due to its availability at the time this project was carried out.

Figure 5.5 CMOS T/R switch with LC-tuned substrate bias [5]

In the TX mode, V_{ctrl} is set to V_{dd} turning on M_1 and M_2 . With the drain of M_2 pulled to Gnd, L_2 and C_{2a} form a parallel tank that resonates at 2.5GHz. Thus, the receive path to presents a high impedance of several hundred ohms, assuring that the

TX signal leakage to the receive path is small. The L_I - C_I pair is designed to resonate at 2.5GHz, to give the substrate node of M1 a high-impedance, thus minimizing the substrate loss. The resonance combined with the large gate bias resistor (Rb_I) causes M1 to behave like a “floating” pass-gate. This allows a large RF signal to be applied at the TX port without causing a voltage difference larger than V_{dd} at any two terminals of M1. At low frequencies less than several hundred megahertz, L_I shorts the substrate of M1 to ground and thus eliminates any latch-up issue. In the RX mode, V_{ctrl} is set to Gnd turning off M1, which minimizes signal leakage to the TX path. The π -network of $C2_a$ - L_2 - $C2_b$ matches the antenna to the LNA input. While the prototype is designed to operate in a 50Ω environment, the π -network components can be adjusted to match different impedances at the RX (LNA) port. The bias resistors, Rb_3 and Rb_4 , and the inverter are required only for testing purposes and can be eliminated when the switch is integrated with the LNA and PA [5].

Figure 5.6 shows the layout diagram of Design 2 in Cadence Virtuoso. The RF input and output are connected to GSG (Ground Signal Ground) Pads. Atn, TX, RX and Vctrl are antenna, transmitter, receiver input and T/R switch control signal respectively.

Figure 5.6 Layout of the T/R switch with LC-tuned substrate bias

Figure 5.7 shows the post-layout simulation results for transmitting and receiving modes. Figure 5.7(a) shows simulation results of harmonics, the output referred 1dB compression point is about 19.1dBm, 2nd and 3rd harmonics are 28.4dB and 34dB lower than the fundamental signal. Figure 5.7(b) shows the S-parameter simulation results in the transmitting mode. Figure 5.7(c) shows the S-parameter simulation results in the receiving mode.

(a) TX Mode harmonics simulation

(b) TX Mode S-parameter simulation

Figure 5.8 shows the die photo of the T/R switch. There are 3 GSG pads in this design, the left one is antenna input, the upper one is receiver output, and the right one is transmitter input. There are also 2 DC pads on the lower side, the left one is V_{dd} and the right one is T/R switch control signal.

Figure 5.8 Die photo of the T/R switch with LC-tuned substrate bias

5.4 On Wafer Measurement

5.4.1 Test equipments

The following equipments are used for on-wafer measurements:

Agilent: Network Analyzer 8510C
 Precision DC source E3631A
 Signal Generator 4438C
 Spectrum Analyzer E4440A

Cascade: Probing Station S300

Probe GSG-100

Figure 5.9 shows the test setup.

Figure 5.9 Probe station test setup

Figure 5.10 shows the photo of probe station setup. On wafer testing is done on this machine with RF GSG probe and DC probe.

Figure 5.10 Photo of probe station setup

5.4.2 S-parameter measurements

Figure 5.15 shows the Measurement Setup and Table 5-1 shows the test conditions.

Figure 5.11 S-Parameter Measurement Setup

Description	Test Conditions
S-Parameter	<ol style="list-style-type: none"> 1. Vdd = 2.7 – 3.3 V, step-size = 0.3V 2. Frequency Sweep = 1 – 8.6 GHz 3. Input Power Level = -35 dBm 4. Single Ended (50Ω) each port. Terminate the unused ports with 50 ohm.

Table 5-1 S-parameter measurement test conditions

Before any measurement is done, a calibration is required. The setting for the calibration is as follows,

- 1) Calibration Method uses Standard Calibration (SOLT)
- 2) Transmission Line Type is selected as Coaxial

- 3) Connector Type is selected as User Defined

For frequency lower than 8.6 GHz, Coaxial Transmission Line Type accuracy is acceptable. The Connector Type should be defined according to the connectors that were used.

5.4.3 P1dB Compression Point Measurement

Figure 5.12 shows the measurement setup for P1dB Compression Point Measurement.

Figure 5.12 P1dB Compression Point Setup

Table 5-2 describes the test conditions for P1dB measurement.

Description	Test Conditions
Input P1 dB	1. Vdd = 2.25 – 2.75 V, step-size = 0.25V 2. SG Frequency = 2.4, 2.45, 2.5 GHz 3. Input Power = -20 to -23 dBm 4. Single Ended (50 Ω)

Table 5-2 P1dB measurement test conditions

Gain compression occurs when a network cannot increase its output amplitude in linear proportion to an increase at its input. The point at which a network's power gain is dropped by 1 dB from the ideal response for a single signal is a figure of merit known as the 1 dB compression point. In the measurement, the input power is increased from a very small level in steps of 1 dB, until the DUT is brought into the strongly nonlinear region.

5.5 T/R Switch Measurement Results

5.5.1 Conventional CMOS T/R switch — Design 1

Figure 5.13 shows the S-parameter measurement results of the T/R switch.

Figure 5.13 Measurement result of T/R switch

Table 5-3 shows the schematic simulation result, the post-layout simulation result as well as the measurement results for the design of Figure 5.3.

Parameter	Symbol	Schematic simulation	Post-layout simulation	Measurement results
OP-1dB (TX Mode)	P1dB	17.4dBm	15.8dBm	15.3dBm
Center Frequency(GHz)	CF	2.45	2.45	2.45
I/O S parameter(TX)(dB)	S11/S22	-19.6/-15.8	-23.2/-18.2	-18.5/-15.3
Insertion Loss(TX Mode)(dB)	IL	2.2	3.3	4.36
Isolation(TX to Rx)(dB)	Isolation	50.4	37	33.5
Insertion Loss(Rx Mode)(dB)	IL	2.2	3.3	4.36

Table 5-3 Comparison of simulation & measurement results for the T/R switch

The differences are caused by the parasitic capacitance, resistance, inductance as well as inaccurate RF transistor model. The results show a good isolation, a high power handling capability, which is higher than calculated value of 13.5dBm according to Equation (5.1) with the 50 Ω load. The insertion loss is higher than expected due to the low Q (lossy substrate) of on-chip inductors in the matching network and R_{ON} of the transistor. However, when the Power Amplifier is combined with the T/R switch, the matching network1 can be removed, because output impedance of PA is not necessary 50 Ω , and is usually smaller than 50 Ω due to high output power requirement, so actual insertion loss of T/R switch is about 2dB and maybe even smaller. Also from this tape-out, it is obvious that for Power Amplifier output, on-chip inductors should be avoided in the signal path. For a high level integration, the on-chip inductor is a choice, but for a high performance and low insertion loss, on board matching networks with high Q components are preferred.

5.5.2 CMOS T/R with LC-tuned substrate bias — Design 2

Table 5-4 summarizes the simulation and measurement results. Post-layout simulation results are obtained from simulation with parasitic resistance and capacitance. High frequency circuit is more sensitive to parasitic capacitance, so post-layout simulation is very important for RF high frequency circuit design.

Parameter	Symbol	Schematic simulation	Post-layout simulation	Measurement results
OP-1dB(TX Mode)	P1dB	27.1dBm	19.2dBm	20.3dBm
Centre Frequency	CF	2.5GHz	2.5GHz	2.5GHz
I/O S parameter(TX)	S11/S22	-17.6dB/-35.7dB	-9.72dB/-11.56dB	<-10dB
Insertion Loss(TX Mode)	IL	1.26dB	0.98dB	3.6dB
Isolation(TX to RX)	Isolation	-31.3dB	-31.5dB	-27.7dB
Insertion Loss(RX Mode)	IL	1.0dB	0.72dB	2.35dB
I/O S parameter(RX)	S22/S33	-18.7dB/-26.5dB	-16.9dB/-26.7dB	<-10dB

Table 5-4 Summary of simulation and Measurement results

Figure 5.14, 5.15 and 5.16 show the measurement results of the S-parameter of the T/R switch in TX and RX modes. They agree with the simulation results well. The frequency responses all peak at 2.5GHz. Input and output return losses are smaller than -10dB. The isolation from TX to RX is 27.65dB. The result shows that the insertion loss is about 3.6dB in the transmission mode, 2.3dB higher than the simulation result. The measured insertion loss in the receive mode is 2.35dB, about 1.3dB higher than the simulation result.

Figure 5.14 S-parameter measurement result in TX mode

Figure 5.15 Measurement result of isolation from TX to RX

Figure 5.16 Measurement result of insertion loss in RX mode

In general, the differences between the measurement results and simulation results are due to the limitation of RF components model and the incomplete compensation for the parasitic of the layout. The T/R switch is very sensitive to the silicon substrate. At high frequencies, the RF signal leakage to substrate will happen through the parasitic capacitance of the inverse biased diode between the transistor inversion channel and the substrate. As discussed in Chapter4, the silicon substrate is low resistive, which will be able to conduct the signal if no proper substrate contacts are available; and even substrate contacts are available, the deep substrate is still conductive. These effects are not included in current RF components' models.

During the post-layout simulation, the RC extraction is used, but the substrate effect is included in the simulation by the design tools. Considering the limitation of the RF components' model, the measured results agree with the simulation.

6 Design Implementation of PA and T/R switch

6.1 Introduction

A linear Power Amplifier and a T/R switch for Bluetooth and WLAN 802.11b/g will be designed in a CMOS process. The targeted output power at the T/R switch is about 20dBm. The TR switch will be designed with 1dB insertion loss; 30dB isolation and 20dBm power handle capability.

For the required performance of the TR switch, especially the power handle capability and isolation, the triple-well transistor will be the ideal choice [4].

For a high power amplifier, an external RF choke is needed. The fabricated die will be packaged and a PCB design is needed for testing. For the non-constant envelope RF signal, high linearity is required. The PAR (Peak to Average Ratio) is up to 10dB in the modern modulation scheme. So a bias control is required to reduce DC power consumption when operating in different power levels. The Power detector will convert the output power level to a voltage, which can be used to control the biasing circuit.

This project uses thick gate transistors of the CSM 0.18 μ m CMOS process, which operates with the 3V power supply. However, this CMOS process doesn't provide triple-well transistors. The impedance transform mentioned in chapter 4 will be used in the design.

6.2 Circuit design

Figure 6.1 shows the block diagram of the whole PA+T/R system, which also provide power detector and biasing control to improve the power efficiency. TX represents transmitter side, and RX represents receiver side. V_{det} will connect to base-band for biasing control or connect to V_b to control the PA biasing condition. V_{ctrl} is the control voltage of the T/R switch.

Figure 6.1 Block diagram of PA and T/R switch

6.2.1 Design of Power Amplifier

Figure 6.2 shows the simplified PA schematic. The first step of the design is to choose the size of the transistor and the proper biasing point of output stage based on the output power requirements (Parametric DC analysis will be used to sweep V_{ds} and V_{gs}).

Figure 6.2 Simplified PA

In this design, we are targeting for the 20dBm output power (100mW), and usually a practical class A Power Amplifier has an efficiency η around 30%. Then for a 3V power supply, the current consumption is:

$$I_{DC} = \frac{P_{out}}{\eta \cdot V_{dd}} = \frac{100mW}{30\% \times 3V} = 111mA \quad (6.1)$$

Figure 6.3 shows the DC parametric simulation for PA output stage transistor. In the DC parametric simulation, both drain voltage V_d and gate voltage V_g are swept. The x-axis is drain voltage V_d , y-axis is current consumption I_d , and each curve represents different gate voltage. Find the Q point at around $V_{dd}=3V$, $I_d=111mA$.

For MOS transistor, the low Knee voltage ($V_{dsat}=V_{GS}-V_{th}$) is preferred for higher power efficiency and higher output power as mentioned in Chapter 4. However, if V_{GS} is too low, a large input signal will force the PA to operate as a class AB amplifier, which results in a degradation of the linearity. So there's a trade-off between power efficiency and linearity, which will be determined by the gate biasing voltage V_{GS} . In this CMOS process, $V_{th}=0.4V$, assume that the amplitude of input signal is $V_{in}=0.5V$,

then $V_{dsat} = V_{in} = 0.5V$ and $V_{GS} = 0.9V$.

Figure 6.3 DC parametric simulation of output transistor

From the above analysis, the biasing point of the transistor is obtained as ($V_d = 3V$, $V_{GS} = 0.9V$, $I_d = 111mA$). The size of the transistor is decided by the selection of this operating condition. Figure 6.3 shows the final DC simulation result. There are 3 points A ($V_{GS} = 1.4V$, $V_{DS} = 0.5V$, $I_D = 277mA$), B ($V_{GS} = 0.9V$, $V_{DS} = 3V$, $I_D = 123mA$) and C ($V_{GS} = 0.4V$, $V_{DS} = 5.5V$, $I_D = 0.35\mu A$) in the figure, which are starting point, Q point and end point of the load line.

The next step is to find the optimum output impedance. For 3V supply, the knee voltage is $V_{knee} = 1V$ when $V_{gs} = 1.4V$, the amplitude of the voltage swing at the drain of the output transistor is $V_p = 3 - 1 = 2V$, then the optimum output impedance shall

$$be R_{out} = \frac{V_p^2}{2P} = \frac{2^2}{2 \times 0.1} = 20\Omega.$$

Because the antenna presents 50Ω impedance, an impedance transfer network is

needed to transform 20Ω to 50Ω .

The output impedance of the output stage is related to the transistor size, the matching network before the transistor and the choke of the output stage. In Appendix A, a small signal equivalent circuit for common source amplifier is shown. By replacing R_L with the impedance of the choke inductor, and R_{in} with Z_{in} , then the output impedance can be found through the equivalent small signal circuit.

The above calculation is only a basic guide line for the optimum load of PA. A more practical approach is to use Load-pull method to sweep the load impedance of the output stage to find the optimum impedance which will produce the maximum output power. EDA tools such as Cadence Spectre RF and ADS are used to implement the design of the project. After simulation, the actual optimum load impedance is about 8Ω .

The driver stage of the PA should provide a linear signal with sufficient power to drive the output stage. For example, the OP1dB of the PA is 20dBm, and the output stage have a gain of 8dB, then the PA driver should have an OP1dB more than 13dBm. Inter-stage matching network will then be designed to match the input impedance of output stage and the output impedance of driver.

6.2.2 Design of T/R switch

As mentioned above that the PA need a load of about 8Ω , we can see that with a control voltage of $V_{dd}=3V$ and $V_{th}=0.4V$, the maximum power handle capability of the

T/R switch is $P = \frac{((3-0.4)/2)^2}{2 \times 8} \approx 106mW$. So the T/R switch should provide a load impedance of 8Ω to the PA.

Figure 6.4 shows the conventional T/R switch. The transistor of T/R switch will work in the triode region when the transistor is on. The main insertion loss is caused by the on resistance and parasitic capacitance to the ground. In order to reduce the insertion loss, the shunt arm in the TX side will be removed. The on resistance of the T/R switch can be found in the followed equation:

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \quad (6.2)$$

Figure 6.4 Conventional T/R Switch [1]

From equation (6.2), it can be seen that the on resistance can be reduced by increasing either W or V_{GS} . The design consideration is already detailed in Chapter 3.

An optimization is done in the simulation. When W is swept from $10\mu\text{m}$ to $600\mu\text{m}$, the insertion loss will decrease first, because R_{ON} decreases with the increase of W . However when reaches a certain value, the insertion begins to increase due to the increasing parasitic capacitance. Thus, there's an optimum point, where the sum of loss caused by R_{ON} and parasitic capacitance is minimum. Through this optimization, the final width of the series transistor in TX is about $300\mu\text{m}$.

Finally the output matching network will transform the 8Ω impedance to 50Ω . When designing the matching network, usually shunt inductor is used to reduce the effect of bond-wire inductance, where the shunt inductance is usually much larger than the parasitic inductance of the bond-wire.

An L matching network is used frequently in RF IC design, due to its simplicity and lower loss. But on chip inductor in series should be avoided in the RF signal path, because it will cause a high loss especially for Power Amplifier output stage.

After the modification from conventional SPDT, the final schematic of the T/R switch of this work is presented in Figure 6.5. The input impedance of TX port is matched to the output impedance of PA, about 8Ω . The output impedance of ATN and the RX port are matched to 50Ω .

Figure 6.5 Modified T/R switch of this work

6.3 Package and Schematic

The simulation of the PA+T/R switch system will include also the effects of packaging. The package model used in the design is based on the simulation result provided by the Package house Advanced Semiconductor Engineering (ASE). In RF design, the effect of bond wire is significant and can't be ignored. For an accurate design, the PCB effect should also be considered.

Figure 6.6 Cross-section of IC package

In Figure 6.7, the bond wire model is described, the mutual inductance is also critical for RF path, since the mutual inductance won't be reduced significantly when the space between two bond-wires increase. The inductance of bond-wire has a more significant effect than that of the parasitic capacitance of bond-wire and lead.

Figure 6.7 Equivalent circuit for a Package in a system

In Figure 6.8, the 3D diagram for the bond-wire and lead are presented. However, only the bond-wire and lead of the important input and output RF signal path are modeled. In RFIC design, the inductance of bond-wire connected to ground must be minimized. More bond-wires or down-bonds can be used to reduce the parasitic inductance. The Double-bond is a very common used method to reduce bond-wire effect.

Figure 6.8 3D diagram for bond wire and lead

Figure 6.9 shows the core circuit of the PA and T/R switch. A power detector will be used to detect the power at the antenna to control the biasing condition of the PA. In the receive mode, the biasing control will shut down the PA and significantly improve the isolation. The transmit path is as simple as possible to reduce the insertion loss.

Figure 6.10 shows the simulation setup of PA and T/R switch, including package and bond-pad model. Grounds are intentionally separated to avoid any feed back loop from grounds which can cause stability issue. For each ground, multiple bond-wires are used to reduce the parasitic inductance at ground, because the parasitic inductance at ground can be seen as a source degenerative inductor, it will reduce the gain of the Power Amplifier.

Figure 6.10 Top schematic simulation

6.4 Simulation Results

Figure 6.11 shows the simulation results of PA and T/R switch in transmission mode. Figure 6.11 A shows that the OP-1dB is more than 19dBm at the antenna, and the saturation power is more than 20dBm, which satisfies the design target. Figure 6.11 B shows that the 2nd and 3rd harmonics are more than 26dB lower than fundamental when the output power is about 20dBm. Figure 6.11 C shows that the gain is about 20dB at 2.45GHz, S11 and S22 are smaller than -20dB and the isolation smaller than -39dB from antenna to TX. Figure 6.11 D shows the input impedance of TX and output impedance of antenna in Smith chart.

A. Output 1dB compression point

B. Output fundamental power and 2nd, 3rd harmonics

C. S-parameter simulation results

D. S-parameter simulation results on Smith Chart

Figure 6.11 Simulation Results of output power and S-parameter in TX Mode

Figure 6.12 shows that the efficiency of Power Amplifier and T/R switch is about 16% when the output power is 19dBm.

Figure 6.12 Simulations results of output power and efficiency in TX mode

Figure 6.13 shows the simulation results of PA and T/R switch in receive mode.

Figure 6.13 A show that the insertion loss is about 2.5dB, isolation more than 50dB, input and output return loss are smaller than -10dB. Figure 6.13 B shows the input impedance at antenna and output impedance at the RX.

A. S-parameter simulation result in magnitude

B. S-parameter simulation result on Smith Chart
Figure 6.13 Simulation Result of RX Mode

Figure 6.14 shows the schematic and the simulation result of a power detector of the Power Amplifier. The capacitor divider will sample the output power, which will be converted to a voltage by a diode and RC network. The output voltage of the power detector indicates the output power strength of the Power Amplifier and can be used to control the biasing condition of Power Amplifier. As mentioned earlier, in modern communication systems, usually the PAR (Power Average Ratio) is quite high, thus, in most of the time the Power Amplifier will work below its peak output power at a low efficiency. So it will be necessary to lower the DC biasing point when operates at lower power to improve the power efficiency. The gain of the Power Amplifier can also be controlled through the biasing control circuit.

7 Layout Consideration

A layout is basically a drawing of the mask from which the integrated circuit will be fabricated. The performance of a high frequency RF IC, especially for GHz applications, is heavily influenced by its layout. Creating the layout is always as critical as specifying the parameters of the devices. It will determine the behavior of the realized design.

In this chapter, the layout design of the PA circuits and the proposed non-sequential linear PD will be described. Some consideration on the layout, including the matching resistors and matching transistors, will be discussed. The information is based on Chartered Semiconductor Manufacturing Ltd (CSM) CMOS 6-Metal, 1-Poly, 0.18 μm process.

7.1 Introduction to Chartered Process Design Kit

The Chartered Process Design Kit (PDK) is a complete set of technology files for the Cadence environment that enables the CSM customers to create a custom IC design. It supports current versions of Cadence Analog Design Environment, Schematic Composer, Spectre circuit simulator, Virtuoso Custom Design, Diva physical verification and Assura physical verification. It is provided for Chartered's 0.35 μm , 0.25 μm , 0.18 μm and 0.13 μm Process Technologies [47].

The PDK for 0.18 μm CMOS Analog/RF technology is employed in the design. It supports the implementation of active devices such as Native and Low Vt transistors, MOS, and BJT; and passive devices such as PN varactors, inductors, insulated

metal-to-metal and insulated poly-to-substrate capacitors, resistors and diodes [49].

There are six layers of metal and one layer of poly available for interconnection. The optional features are Salicide block mask to provide non-salicided diffused and poly regions, thicker top metal, and Polyimide layer passivation.

7.2 Layout of Transistors

In a layout, a transistor with a large W/L aspect ratio is drawn either as multiple transistors or as a multifinger transistor. Multiple transistors are identical devices wired in parallel while a multifinger transistor is a single transistor which is spilt into a number of parallel equal parts arranged in a stack of polysilicon gates within the same active region. The rule of thumb is to choose the width of each finger such that the resistance of the finger is less than the inverse transconductance associated with the finger, i.e., $R_{gi} < 1/g_{mi}$ [50]. Figure 7.1 shows the layout of a multifinger transistor which is employed in this design since most of the transistors are of a large aspect ratio.

Figure 7.1: Layout of a transistor with N fingers

For transistor with a large aspect ratio, the layout should be drawn in matching structures to minimize random mismatches stemming from microscopic fluctuations in dimensions, dopings, oxide thickness, and other parameters that influence component values [51]. Traditionally, there are five types of matching structures commonly used in the layout design: Strip, Common Centroid, ABBA-1, ABBA-2 and ABBA-2 gate separated. The illustration of the configurations of these matching structures is shown in Figure 7.2.

(iv) ABBA-2

(v) ABBA-2 Gate-separated

Figure 7.2 Transistor matching structures

Several guidelines should be considered for achieving a good layout for transistors matching. Firstly, we should keep the transistors to be matched close to each other. Secondly, we should place groups of devices around a common geometric center. Thirdly, we should employ identical devices layouts and place them in identical surroundings. Finally, we should orient devices in the same direction.

7.3 Layout of Resistors

For the CSM 0.18 μ m CMOS process, N-well, N+, P+, and poly are available

layers for implementing resistors. N+ and P+ resistors have a low sheet resistance (79 Ω /square for N+ and 118 Ω /square for P+) and low accuracy (10% and 25% tolerance for N+ and P+ respectively). N-well layer has a high sheet resistance (780 Ω /square), with a tolerance of about 19%. N-Poly resistor (85 Ω /square) and P-Poly resistor (330 Ω /square) have the highest accuracy.

The considerations for matching resistors are similar to those of matching transistors. It is recommended that the matched resistors are constructed from single material and should be of the same width. Identical geometries should be used for all the resistors in one circuit whenever possible [52]. Matched resistors should be placed in close proximity and dummies should be included in either end of resistor arrays [51]. Figure 7.3 depicts the layout drawing of matched array resistors A and B. They are cross-connected to achieve matching structure. It is shown that there are four dummy segments placed on the two ends of the resistor array.

Figure 7.3 Resistor layout

Figure 7.4 shows the final layout of the PA and T/R switch in Cadence Virtuoso. It includes 5 inductors and occupied a die area of $1430\mu\text{m} \times 910\mu\text{m}$. The die size is just able to be fit in a $3 \times 3\text{mm}^2$ QFN package and down-bond can be used in the grounds side to reduce the parasitic inductance to the grounds. Decoupling capacitors between V_{dd} and ground are used as many as possible to reduce the noise between power supply and grounds. Finally metal dummy is fit into the layout to meet the metal density requirements, poly and diffusion are also required to meet the density requirement.

Figure 7.4 Final Layout of PA and T/R Switch

Figure 7.5 shows the bonding diagram of the chip. The paddle size of the 3×3mm QFN package is 2.1×2.1mm, so the maximum die size can be 2.1×2.1mm. But the actual die size is a little bigger than the die size in the layout, considering about the dicing channel width (about 200μm/dicing channel, may vary with different foundry). The down-bond and double-bond are used to reduce parasitic inductance and also the maximum current capability.

Figure 7.5 Bonding diagram of PA and T/R Switch

Figure 7.6 shows the X-ray photo of the chip with the package. 9 vias on the PCB connect the paddle of the package with the ground of the PCB.

Figure 7.6 X-ray photo of the PA and T/R Switch with Package

8 PCB design and Testing

8.1 PCB design

The input and output RF paths are very critical for high frequency PCB design. At $f=2.45\text{GHz}$, the wave length on the PCB board is:

$$\lambda = \frac{C}{f \cdot \sqrt{\epsilon_r}} = \frac{3 \times 10^8 \text{ m/s}}{2.45 \times 10^9 \text{ Hz} \times \sqrt{4.6}} = 57.09 \text{ mm} \quad (8.1)$$

Where ϵ_r is the dielectric constant of FR4 PCB and $C=3 \times 10^8 \text{ m/s}$

As λ is comparable to the PCB dimension, the input and output RF paths should be carefully designed based on the distribute parameters.

In this PCB design, grounded coplanar waveguide (GCPW) is chosen. Based on the parameters of the PCB, the dimensions of a 50Ω GCPW can be calculated with Agilent software APCAD.

Figure 8.1 shows the cross-section of the GCPW. H , ϵ_r and thickness of the metal are fixed for a designated PCB material. The W and S can be found through the simulation of the software APCAD.

Figure 8.1 Cross-section of Grounded Coplanar Waveguide

Figure 8.2 shows the test circuit of PA+T/R switch and Figure 8.3 shows the PCB layout of the PA+T/R switch test circuit. The bold lines in Figure 8.2 are critical RF signal paths. GCPW (grounded coplanar waveguide) are designed at $50\ \Omega$ for TX, RX and Antenna RF signal path. Vctrl will control the operation of the T/R switch. A lot of ground vias are used for better ground connection.

Figure 8.2 Schematic of the PA+T/R switch test circuit

Figure 8.3 PCB layout of PA+T/R Switch test circuit

8.2 Testing

This section discusses the Measurement Setup for measuring the S-parameters and 1dB compression point of the evaluation board.

8.2.1 S-parameter measurement

Figure 8.4 shows the Measurement Setup and Table 8-1 shows the test conditions.

Figure 8.4 S-Parameter Measurement Setup

Description	Test Conditions
S-Parameter	<ol style="list-style-type: none"> 1. Vdd = 2.7 – 3.3 V, step-size = 0.3V 2. Frequency Sweep = 1 – 8.6 GHz 3. Input Power Level = -35 dBm 4. Single Ended (50Ω) each port. Terminate the unused ports with 50 ohm.

Table 8-1 S-parameter measurement test conditions

Before any measurement is done, a calibration is required. The setting for the

calibration is as follows,

- 1) Calibration Method uses Standard Calibration (SOLT).
- 2) Transmission Line Type is selected as Coaxial
- 3) Connector Type is selected as User Defined

For frequency lower than 8.6 GHz, Coaxial Transmission Line Type accuracy is acceptable. The Connector Type should be defined according to the connectors used.

8.2.2 P1dB Compression Point Measurement

Figure 8.5 shows the measurement setup for P1dB Compression Point Measurement.

Figure 8.5 P1dB Compression Point Setup

Table 8-2 shows the test conditions.

Description	Test Conditions
Input P1 dB	1. Vdd = 2.25 – 2.75 V, step-size = 0.25V 2. SG Frequency = 2.4, 2.45, 2.5 GHz 3. Input Power = -20 to 6 dBm 4. Single Ended (50 Ω)

Table 8-2 P1dB measurement test conditions

8.3 Measurement Results

In this project, the Power Amplifier and the PA+T/R Switch have been fabricated.

The power amplifier shows a reasonably good performance, but the PA+T/R Switch have a very poor performance. Table 8-3 shows the measurement results of the Power Amplifier, including output power, gain and efficiency.

Pin(dBm)	ReadOut(dBm)	Pout(dBm)	Gain(dB)	P1dB_reference(dBm)	Idd(mA)	Eff(%)
-20	-1.67	0.00	20.00	-1.00	130.20	0.23
-19	-0.50	1.17	20.17	0.00	130.30	0.30
-18	0.33	2.00	20.00	1.00	130.20	0.37
-17	1.33	3.00	20.00	2.00	130.30	0.46
-16	2.50	4.17	20.17	3.00	130.60	0.61
-15	3.33	5.00	20.00	4.00	130.70	0.73
-14	4.33	6.00	20.00	5.00	130.60	0.92
-13	5.17	6.84	19.84	6.00	130.90	1.12
-12	6.17	7.84	19.84	7.00	131.20	1.40
-11	7.17	8.84	19.84	8.00	131.40	1.77
-10	8.17	9.84	19.84	9.00	131.70	2.22
-9	9.17	10.84	19.84	10.00	132.20	2.78
-8	10.17	11.84	19.84	11.00	132.60	3.49
-7	11.17	12.84	19.84	12.00	133.40	4.37
-6	12.17	13.84	19.84	13.00	134.10	5.47
-5	13.00	14.67	19.67	14.00	135.90	6.54
-4	14.17	15.84	19.84	15.00	136.40	8.52
-3	15.17	16.84	19.84	16.00	138.10	10.60
-2	16.17	17.84	19.84	17.00	139.50	13.21
-1	17.00	18.67	19.67	18.00	141.70	15.74
0	17.83	19.50	19.50	19.00	144.10	18.74
1	18.50	20.17	19.17	20.00	146.80	21.47
2	19.17	20.84	18.84	21.00	150.60	24.42
3	19.67	21.34	18.34	22.00	155.40	26.55
4	20.00	21.67	17.67	23.00	159.90	27.84
5	20.33	22.00	17.00	24.00	164.10	29.27
6	20.50	22.17	16.17	25.00	167.70	29.78

Table 8-3 Measurement Results of Power Amplifier

Figure 8.6 shows the Measurement results of Power Amplifier, which is plotted from the data in Table 8-3. From Figure 8.6, we can see that the output referred 1dB compression point is about 20.5dBm, efficiency at P-1dB is about 25%, and the gain is about 20dB at small input signal.

Figure 8.6 Measurement Results of Power Amplifier

Figure 8.7 shows the measurement results of the PA+T/R switch. The Gain is supposed to be about 19dB, but the measurement result is only about -3dB. It is probably caused by the mismatch between PA and T/R switch. Because the output impedance of PA is very small, it's very sensitive to the process variation and parasitics. The lossy silicon substrate also account for the very poor performance.

2.4GHz PA+T/R Switch Measurement Result(Vdd=3V)
Transmission Mode(Port1: Tx in, Port2: Antenna)

Figure 8.7 S-parameter measurement results of the PA+T/R switch

9 Conclusions and Recommendations

In this project, a SPDT T/R switch and a T/R switch with LC-tuned substrate bias in CMOS process are presented with a reasonably good performance. The theory and design of the T/R switch are described into details.

The design and implementation of Power Amplifier and T/R switch in CMOS process are also described in details, including the chip design and the evaluation board design. Although the measurement result is not good, the concept of the design is according to the idea of commercial product. The failure is due to the poor substrate isolation of CMOS process and the accuracy of device model in high frequency. The performance of PA is also very sensitive to the load impedance, and usually it's tunable with on board components. While in this project, the load of PA is the on-chip T/R switch. The accuracy of the device model and simulator are limited. Beside that, the tolerance of package model can achieve more than 100%, which is another issue limited the performance of RF IC design.

More accurate model of on-chip components and also package model are highly required. Alternatively, flip-chip or COB (Chip on board) of low parasitic are preferred.

More research needs to be done on the substrate effect which causes the degradation of the performance of the circuits. Because for conventional CMOS substrate, the isolation is poor, the substrate connection needs to be designed(p-n-p triple well guard-ring are preferred for better isolation) as mentioned in Chapter 4. Since most foundry design kits ignore substrate effects, the simulation results may not

be accurate. As suggested by IBM, for critical RF circuit design, NS (N-sub collector) back plate is used for bond pads, capacitor, resistor etc., more study should be done on the substrate effect with RFIC design.

Studies are also required to further improve the maximum output power, power efficiency, increase the isolation of T/R switch, and reduce the insertion loss.

Author's Publications

Ch.Hu, M. A. Do, J. G. Ma, and K. S. Yeo, "Power Amplifier combined with T/R switch", *IFIP International Conference on VLSI (Very Large Scale Integration System)*, Perth, western Australia 2005.

Ch.Hu, M. A. Do, J. G. Ma, and K. S. Yeo, "2.45GHz Power Amplifier With T/R Switch", *Asia Pacific Microwave Conference*, China 2005.

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Appendices

APPENDIX A

Figure A.1 Small signal equivalent circuit of common source amplifier

Sum up the currents at gate, drain, and source; we have the following three equations:

$$\frac{V_X + V_S - V_{in}}{R_{in}} + V_X C_{GS} s + (V_X + V_S - V_{out}) C_{GD} s = 0 \quad (A1)$$

$$(V_{out} - V_X + V_S) C_{GD} s + V_{out} \left(\frac{1}{R_L} + C_{DB} s \right) + g_m V_X = 0 \quad (A2)$$

$$V_X C_{GS} s + g_m V_X - \frac{V_S}{R_S} = 0 \quad (A3)$$

From (A3), we have

$$V_S = V_X (C_{GS} s + g_m) R_S \quad (A4)$$

which, upon substitution in (A2), yields

$$[V_{out} - V_X + V_X(C_{GS}s + g_m)R_S]C_{GD}s + V_{out}(\frac{1}{R_L} + C_{DB}s) + g_m V_X = 0 \quad (A5)$$

That is,

$$V_X = \frac{C_{GD}s + C_{DB}s + \frac{1}{R_L}}{C_{GD}s[1 + R_S(g_m + C_{GS}s)] - g_m} V_{out} \quad (A6)$$

Substitute (A4) into (A1), and rearrange it, we have

$$V_X \{C_{GS}C_{GD}s^2 + [1 + R_S(g_m + C_{GS}s)](\frac{1}{R_{in}} + C_{GD}s)\} = \frac{V_{in}}{R_{in}} + V_{out}C_{GD}s \quad (A7)$$

So, by substitution (A6) into (A7), we have

$$\frac{C_{GD}s + C_{DB}s + \frac{1}{R_L}}{C_{GD}s[1 + R_S(g_m + C_{GS}s)] - g_m} V_{out} \{C_{GS}C_{GD}s^2 + [1 + R_S(g_m + C_{GS}s)](\frac{1}{R_{in}} + C_{GD}s)\} = \frac{V_{in}}{R_{in}} + V_{out}C_{GD}s \quad (A8)$$

Rearrange (A8), we have

$$\frac{V_{out}}{V_{in}} = \frac{\{C_{GD}s[1 + R_S(C_{GS}s + g_m)] - g_m\}R_L}{As^3 + Bs^2 + Cs + D} \quad (A9)$$

Where

$$A = R_S C_{GS} C_{GD} C_{DB}$$

$$B = R_{in} R_L R_S [g_m (C_{GD}^2 + C_{GD} C_{DB} - C_{GS} C_{GD}) + \frac{C_{GS} C_{GD}}{R_L} + \frac{C_{GS} (C_{GD} + C_{DB})}{R_{in}}] + R_{in} R_L (C_{GS} C_{DB} + C_{GD} C_{DB} + C_{GS} C_{GD})$$

$$C = R_S [C_{GS} + g_m R_{in} C_{GD} + g_m R_L (C_{GD} + C_{DB})] + R_L (C_{GD} + C_{DB}) + R_{in} [C_{GS} + C_{GD} (1 + g_m R_L)]$$

$$D = 1 + g_m R_S$$

APPENDIX D

A voltage-controlled biasing circuit