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SINGLE-ENDED BROADBAND SILICON
CARBIDE MESFET POWER AMPLIFIER

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Single-Ended Broadband Silicon Carbide MESFET Power Amplifier

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A thesis submitted to the Nanyang Technological University
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ABSTRACT

For decades, the realization of single stage broadband power amplifier has posed a significant challenge to microwave design and system engineers due to the electrical and thermal limitations of matured transistor technology, such as Gallium Arsenide (GaAs). Although broadband power amplifiers are not yet a reality in today's infrastructure, engineers and researchers have focused in the past years for its realization. Research shows that wide bandgap semiconductor Silicon Carbide (SiC) offers an impressive microwave power and frequency capabilities. Its high breakdown voltage results in low operating current and high internal impedance. Therefore, SiC MESFETs have a tremendous prospective for realizing broadband, high-power amplifier at microwave frequencies due to their wide band-gap features of high breakdown field, high electron saturation velocity and high operating temperature.

In this thesis, an accurate small signal model SiC MESFET is developed. The package SiC MESFET device (CRF24010) is used in model derivation and development. Cold bias condition measurement is performed to derive device equations and parameters. Parasitic extrinsic elements are extracted using cold FET technique. Nonlinear equations for drain current and drain voltage relationships are derived as well.

Single-stage hybrid SiC power amplifier has been designed and fabricated for operating frequencies from 650MHz to 1800MHz centered at 1225MHz. The frequency range above is equivalent to more than 90% bandwidth, compared to only 3~4% bandwidth achievable using GaAs technology. Schematic design and simulation are performed.

Detailed design concepts and analyses, which include stabilization, input and output matching networks, and DC bias are presented. Input and output matching networks have been designed using microstrip technique to increase the bandwidth, gain and improve stability. The derived small-signal model is used in this power amplifier design. A good agreement is observed between the simulation result of this design and the one that using “block” S-parameters provided by Cree. The derived nonlinear I-V models are used to design DC bias. The good prediction of device bias nonlinearity is observed from these large-signal DC models.

Simulation results indicate that the power amplifier is unconditionally stable from 500MHz to 4000MHz. The typical gain at 1225 MHz is greater than 9dB. Experimental results show that the gain is more than 8 dB from 850MHz to 1850MHz. Hence both simulation and measured results are in good agreement over the 850MHz-1850MHz frequency range. Large-signal measurement shows that power gain of 8dB and 35dBm minimum output power have been achieved at 1225MHz.

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Chapter 1 Introduction

Designing amplifiers to cover more than one band will reduce both capital equipment and operating cost for the infrastructure market. Currently, RF power amplifiers cover only one band. Carriers, service providers, and equipment manufacturers would greatly prefer to supply and deploy one RF power amplifier that can cover across many bands. This would reduce rack usage in the equipment cabinet, power consumption, and overall equipment cost. When combined with multiband antennas, even the overall footprint of the base station can be reduced. One major trend is the continuous challenge for more power over a very wide bandwidth. Unfortunately, the existing technologies have faced many challenges to satisfy the higher demand. For decades, the realization of single stage broad-band power amplifier has posed a significant challenge to microwave design and system engineers due to the electrical and thermal limitations of GaAs transistor technology.

Under such circumstance, wide band-gap semiconductors are promising to tackle the challenge. Its breakdown voltage that is an order of magnitude higher along with excellent thermal properties, which overcomes the current difficulties. High breakdown voltage results in low operating current and high internal impedance. High internal impedance overcomes the Bode-Fano limitation, as it simplifies the impedance matching networks. This results in efficient power coupling and wide bandwidth. Moreover, due to its excellent thermal properties, the performance of these transistors does not degrade significantly under elevated temperatures. Therefore, temperature dependency of RF power amplifiers performance made of these transistors is expected to be much lower, compared to conventional devices. In other words, these wide-bandgap transistors are

expected to have consistent performance characteristics over both a wide bandwidth and wide temperature range. These amplifiers are very desirable for applications in infrastructure market, aerospace, avionics and military systems. In recent years, Silicon Carbide (SiC) MESFET technology has established itself as a strong contender for such applications because of its large bandgap energy, thermal conductivity, and breakdown electric field.

Recently, the power amplifier design using SiC MESFET has been drawing large attention. An accurate small-signal model is required to observe the internal properties of this device. Nonlinear I-V characterization is important to predict the nonlinearity and bias dependency of the device. Most nonlinear simulators often used empirical table-based models due to better flexibility and high computation efficiency. A lot of empirical models suitable for the simulation of MESFET behavior have been developed. In this work, the tabulated data that represent the extracted nonlinear elements of the small-signal model are mathematically transformed into spline functions.

A detailed approach of small-signal model derivation is presented along with the nonlinear I-V characterization. Single-ended power amplifier design using Cree CRF24010 silicon carbide MESFET is elaborated. Detailed analysis of input and output matching networks are required to achieve the desired bandwidth. This sample amplifier demonstrates the potential that wide band-gap semiconductors hold for this market. Broadband RF power amplifiers are not yet a reality in today's infrastructure, but intensive research and development efforts combined with a strong service provider pull can only hasten the appearance of practical equipment. In this chapter general background of broadband power amplifier design is presented.

1.1 Bandwidth Definitions

Bandwidth is a measure of how wide spectrum a microwave system can respond to. Bandwidth is often given in MHz or GHz, calculated from a lower frequency F_L to an upper frequency F_H , $(F_H - F_L)$. Bandwidth is expressed in a number of ways, which is defined as following.

- 3-dB bandwidth: for a network that has a non-ideal frequency response, the 3-dB bandwidth is where the transmission coefficient S_{21} falls off from its highest peak by three dB. Similarly, expressing a network by its two-dB or one-dB bandwidths is also possible.
- Percentage bandwidth: for a system that works from a lower frequency F_L to an upper frequency F_H , the percentage bandwidth is $100\% \times (F_H - F_L) / F_C$. F_C is the center frequency, equal to $[(F_L + F_H) / 2]$.
- Instantaneous bandwidth: this is a measure of how wide a spectrum system can respond to, without any types of tuning.

There is no official definition of bandwidth that is classified as “broadband”. However, if a circuit of device nominally has a bandwidth of 2 to 3 percent, then 10% would be classified as broadband.

1.2 Broadband Amplifier Design

The design of broadband amplifiers introduces new difficulties, which require careful considerations. The design of constant-gain amplifier over a broad frequency range is a matter of proper matching networks and feedback networks, to compensate $|S_{21}|$ variations with frequency.

Major difficulties encountered in the design of a broadband amplifier are:

1. $|S_{21}|$ and $|S_{12}|$ variations with frequency. Typically, $|S_{21}|$ decreases with frequency at the rate of 6dB/octave and $|S_{12}|$ increases with frequency at the same rate. Typical variations of $|S_{21}|$, $|S_{12}|$, and $|S_{12}S_{21}|$ with frequency are illustrated in Figure 1.1. The variation of $|S_{12}S_{21}|$ affects the circuit stability. The flat region is the critical region of amplifier stability.
2. Scattering parameters S_{11} and S_{22} are also frequency dependant and their variations are significant over a broad range of frequencies.
3. There is a degradation of the noise figure and VSWR in some frequency range of broadband amplifier.

Figure 1.1 Frequency response of $|S_{21}|$, $|S_{12}|$, and $|S_{12}S_{21}|$

Two techniques are commonly applied for designing broadband amplifiers. They are compensated matching networks and negative feedback. The technique of compensated

matching networks involves mismatching the input and output matching networks to compensate for the changes of $|S_{21}|$ with frequency.

1.3 RF Silicon Carbide (SiC) MESFET

RF SiC MESFET is new transistor technology that appeared to be a substantial lead in RF power generation. Silicon carbide (SiC) has received increased attention during the last decade as a promising device material for high temperature, high frequency, and high power device applications due to its high thermal conductivity and high critical field for breakdown. The wide bandgap energy and low intrinsic carrier concentration of SiC allow it to operate at much higher temperatures than silicon and GaAs technologies. As temperature increases, intrinsic carriers increase exponentially so that thermal-runaway phenomenon exists that causes the undesired leakage current increases unacceptably large. Depending on specific device design, the intrinsic carrier concentration of silicon generally confines silicon device operation to junction temperatures less than 300⁰C. In the other hand, SiC's much smaller intrinsic carrier concentration theoretically allows device operation at junction temperatures exceeding 800⁰C [1-2].

The high breakdown field and high thermal conductivity of SiC coupled with high operational junction temperatures theoretically allow high power densities and efficiencies to be realized in SiC devices. As power is a product of voltage and current, it concludes that high operating voltage can result in low current and high characteristic impedance. High characteristic impedance is the important property in designing broadband power amplifier as it simplifies impedance matching which results in efficient power coupling and broad bandwidth. The material superiorities of wide bandgap

materials (SiC, GaN and Diamond) over silicon and GaAs are compared at Table 1. It indicates major advantages such as high breakdown electric field, wide bandgap energy, high thermal conductivity, and high carrier saturation velocity.

Table 1 Material properties of conventional and wide bandgap semiconductors.

Material	E _g (eV)	ε _r	Θ (W/ ⁰ K-cm)	E _c (V/cm)
Si	1.12	11.9	1.5	3x10 ⁵
GaAs	1.43	13.1	0.46	4x10 ⁵
InP	1.34	12.4	0.67	4.5x10 ⁵
3C-SiC	2.3	9.7	4.9	1.8x10 ⁶
4H-SiC	3.2	10.0	4.9	3.5x10 ⁶
6H-SiC	2.86	10.0	4.9	3.8x10 ⁶
GaN	3.45	9	1.3	2x10 ⁶
Diamond	5.45	5.5	20-30	10x10 ⁶

SiC MESFET electrical properties are advantageous compared to silicon. It possesses:

- larger energy bandap, enabling lower leakage current from temperature-induced intrinsic conduction;
- higher thermal conductivity, which can sustain higher power densities by four times compared to GaAs or Si;
- faster saturated electron drift velocity that two times faster than silicon's.
- stronger bonding energy (between Si and C), resulting higher mechanical strength, chemical inertness, and radiation resistance.

Both SiC MESFET and GaN HEMT devices have shown very high power densities. Both of these active devices benefit from the high breakdown voltages afforded by their wide-bandgap semiconductor properties. This high power density, supported with good efficiency and linearity, provide an excellent base for future military and commercial power amplifier applications. However, the gain-bandwidth limitation is worsened due to

the high-impedance load, high power design is possible even over multi-octave bandwidth that makes broadband power amplifier design possible.

1.4 Objective

The main goal of this project is to develop the realization of SiC MESFET broadband power amplifier. A new small-signal empirical model of SiC MESFET is proposed, and single-ended power amplifier is designed and developed.

The objective of this thesis is to propose a new empirical SiC MESFET small-signal model. The design, simulation, fabrication and measurement of the broadband SiC MESFET power amplifier are also highlighted. The module demonstrates good gain-bandwidth performance, with acceptable return loss performance.

1.5 Thesis Organization

This thesis consists of seven chapters. Chapter 1 introduces the current trends of broadband RF power amplifiers and RF Silicon Carbide (SiC) power MESFET as substantial leading wide bandgap semiconductors, which are presented along with the objective of this thesis.

Chapter 2 gives an illustration of the existing problem and reviews on Bode-Fano theorem limitations. The overview of current power amplifier development is introduced. It reveals that broadband and high power amplifiers are increasing in-demand due to increased requirements in communication systems. The major limiting factor in power amplifier design is the availability of transistor device technology. Therefore, these emerging new wide bandgap device technologies have the potential to revolutionize the way we design power amplifier is designed to meet these increased system requirements.

In this chapter, the detailed analysis of single-ended broadband power amplifier using SiC MESFET is discussed. Design considerations and constraints, such as stability and power gain are elaborated in this chapter.

Chapter 3 introduces an accurate small-signal parameter extraction procedure. Extrinsic parameters in both pinch-off and forward bias modes are extracted by cold FET technique whereas the intrinsic parameters are being derived and optimized through simulation.

Chapter 4 presents the model incorporating empirical expressions for DC modeling, by using the available nonlinear models in the Microwave Office simulator. The model accuracy is verified by comparing simulated and measured results.

Chapter 5 presents schematic design, simulation, PCB fabrication and measurement of single-ended SiC MESFET broadband power amplifier. S-parameters of the derived small-signal model is analyzed. Detailed design steps are demonstrated. Simulation results are also presented to validate the design configuration. Single tone power measurement is performed to observe the module linearity under large-signal conditions.

Chapter 6 concludes the work in the thesis with the achievements summarized and the future work suggested.

Chapter 2 Literature Review and Single-Ended Broadband Power Amplifier Architecture

2.1 Overview of Current Power Amplifier Technologies

A power amplifier (PA) is a circuit that converts dc-input power into a significant amount of RF/microwave output power. There are great varieties of available PAs. Most employ design techniques beyond simple linear amplification. The classic architecture continuously adopts larger PAs to boost a low-level signal to desired output power. In early days of wireless communication (1895-mid 1920s), RF power was generated by spark, arc, and alternator techniques. With the invention of the DeForest audion in 1907, the thermoionic vacuum tube offered a means of generating and controlling RF signals, and vacuum-tube PAs were dominant from the late 1920s through the 1970s. Discrete solid-state RF power devices began to appear at the end of the 1960s with the introduction of silicon bipolar transistors such as the 2N6093 [75-W HF single sideband (SSB)] by RCA [2]. Their dominance in the 1980s brought about the use of lower voltages, higher currents, and relatively low load resistances. The 1990s saw a proliferation of a variety of new solid-state devices including high electron mobility transistor (HEMT), pseudomorphic high-electron-mobility transistor (pHEMT), heterostructure FET (HFET), and heterojunction bipolar transistor (HBT), using a variety of new materials such as Indium Phosphide (InP), SiC, and Gallium Nitride (GaN). The combination of digital signal processing (DSP) and microprocessor control allows widespread use of complicated feedback and predistortion techniques to improve efficiency and linearity [3].

High power amplifiers are used in communication, navigation and in Avionics systems. It requires operating frequency from VHF through X-band frequency ranges, with output powers from hundreds of watts to several kilowatts. Linear continuous wave (CW) microwave transmitters at the 100 watts level output are used for very high frequency (VHF) communication, F22 systems, and at L-band for SATCOM systems. Pulsed power microwave transmitters, operating in Class C have been designed with either high or low duty factors and with power outputs of several kilowatts. X-band frequency microwave transmitters with over 160 watts output have been achieved for weather radar applications. Increased operational requirements for communication systems have continuously forced devices to achieve better power control, higher efficiency, higher output power, wider frequency bandwidth, lower temperature and smaller size.

Broadband RF power amplifiers that operate at very wide bandwidth, that is exceeding several bandwidth octaves, are in high demand. The development of most micro/millimeter-wave systems has, for long, been closely related to the progress in semiconductors. The performance development is primarily dependent on the advancement in material technology as well as innovations in the operating principles of the devices. The availability of transistor device technology is one of the major limiting factors in power amplifier designs. Several of these emerging new wide bandgap device technologies have the potential to revolutionize the way power amplifier is designed to meet these increased system requirements. Section 2.2 elaborates wide bandgap semiconductors for power amplifiers application. In this section, the development status and application of advanced semiconductor technologies are described.

2.2 Wide Bandgap Semiconductors for Power Amplifiers Application

In late 1990s, wide bandgap semiconductors with their superior properties, such as high breakdown voltage and good thermal properties make tremendous breakthrough in power amplifier design. In 1999, DenBaars reported the status and application of advanced semiconductor technologies [4]. The selection of high-performance compound semiconductor technology is getting stringent. Wide bandgap semiconductor technologies began to emerge as potential challengers. Such technologies include SiC FETs and GaN HEMTs fit application in broadband and high power application using large supply voltages. InP HBT technology is beginning to be applied for very high-frequency applications. Silicon Germanium (SiGe) technology makes inroads, particularly with the improved understanding of silicon passives and isolation techniques at microwave frequencies. SiGe BiCMOS provides an innovation for highly integrated system-on-a-chip, for frequencies up to 10GHz.

Meanwhile, the availability of high-performance semiconductor technology has improved considerably in recent years as the need for commercial bandwidth increases. Once the exclusive domain of the military, new commercial data centric applications in both wireless and fiber-based product require the high levels of performance offered by these technologies. These conditions have made the task of choosing the most appropriate technology for product applications more challenging.

Semiconductor devices are usually classified into two major categories, i.e. power and speed. One way to classify those devices into their respective categories is by observing its peak cutoff frequency (F_t) and breakdown voltage, as shown in Figure 2.1. It is observed that SiC MESFET possesses largest breakdown voltage yet the lowest peak

cutoff frequency compared to other device technologies, such as GaAs HBT, GaN HEMT, InP HBT and SiGe HBT. Wide bandgap technologies GaN HEMT and InP HBT exhibit a very good potential for very broadband applications, up to few hundreds GHz.

Figure 2.1 Comparison of breakdown voltage versus peak cutoff frequency for current technology trends.

The 0.8 μ m SiC MESFET demonstrates the largest breakdown voltage at 105V. This device yielded output 2.8W/mm at class A using a supply voltage of 40 volts. The 0.3 μ m GaN HEMT demonstrated a breakdown voltage of 35 volts. 4.2W/mm output was achieved using a supply voltage of 10V at a channel temperature approaching 125⁰C [5].

In 2003, Deborgies [6] reported GaN technology development for microwave solid-state power amplifiers (SSPA). Since GaN is a wide bandgap material, this device will have inherent high breakdown voltage capability. Therefore, very high RF power levels (100W at C-band, 40 to 50W at Ku-band and 20 to 30W at Ka-band) on a single chip should be possible. Also, due to the relatively high voltage-current ratio of the transistor channel, the devices have higher output impedance, with significant reduction of output matching loss and thus better efficiency. Another advantage of GaN is related to the

better thermal resistance compared to GaAs. Finally, GaN is able to withstand much higher junction temperatures compared to GaAs, which infer good reliability and high power capability, especially when grown on SiC substrate.

It is predicted that GaN innovates a breakthrough on active transmit antennas for next generation of telecommunication satellite payloads carrying out a very high number of beams. Power amplifiers under these active transmit antennas will work under multi-carrier conditions, with the associated low efficiency and high heat dissipation. GaN, with its excellent power and thermal capabilities will allow very compact and low mass RF front ends from mobile applications (L/S-bands) up to broadband multimedia (Ku/Ka-bands). GaN technology will also play tremendous role in SSPAs for future Ka-Band user terminals. Furthermore, GaN devices have shown very good low RF noise property, comparable to GaAs devices. This feature, along with the very high breakdown voltage and high RF overdrive capabilities can allow the suppression of limiters in front of the LNA in T/R modules, with the associated reduction in complexity, cost and noise figure.

On the other hand, silicon carbide (SiC) has even better RF power and thermal properties than GaN up to C-band due to its very high breakdown electric field, high saturated electron velocity and high thermal conductivity. The high thermal conductivity and high junction temperature of SiC enable higher power levels than any other semiconductor technologies. Compared to a GaAs MESFET, a 30-fold power density improvement is foreseen. Similar to GaN technology, SiC has good perspective in RF performance; compactness and cost for active transmit antennas in mobile service applications at L and S-band. It can amplify very high RF power level in the order of 100W.

Over the last few years the design and processing of silicon carbide MESFETs has matured to the point where Cree has begun the development of a family of commercial RF power products that emphasize of the high voltage and high power capabilities of this technology. Cree's first product is a packaged 10W MESFET (CRF-20010), designed to operate at a drain voltage of 48 V.

SiC MESFETs, based on a similar unit cell as the 10W transistor and scaled up to larger periphery, with 48 mm single-die devices, have the maximum power output of 120W. Due to the thermal limitations of the package, the power output of this device during operation was reduced to 80W. Cree's continuing research and development efforts of SiC MESFETs have been resulted in two new devices exhibit a maximum RF power density of 5.6W/mm at 3.5 GHz and 4.5W/mm at 10GHz.

SiC MESFET has emerged as a new technology with high output power that challenges a variety of very broadband communication applications. The wide bandwidth capability is due to the much higher output impedance for a given power level of SiC as compared to silicon or gallium arsenide RF devices.

2.3 The Bode-Fano Criterion and Analysis

2.3.1 The Bode-Fano Criterion

The Bode-Fano theorem is the theoretical limits that constraint the performance of an impedance matching network. It is concerned with the following issues that might be raised at the stage of designing broadband amplifiers:

- A perfect match (zero reflection) over a specified bandwidth.
- Trade-off between Γ_m , maximum reflection in the operation bandwidth.

- The complexity of matching networks required for a given specification.
- Trade-off between gain and bandwidth.

The Bode-Fano criterion represents the optimum result that can be ideally achieved.

Figure 2.2 shows the Bode-Fano limits for RC and RL loads terminations.

Figure 2.2 The Bode-Fano limits for RC and RL loads matched with passive and lossless networks (ω_0 is the center frequency of the matching bandwidth). (a) Parallel RC. (b) Series RC. (c) Parallel RL. (d) Series RL.

2.3.2 The Bode-Fano Analysis

Some analyses are made on this criterion, with respect to shunt R and shunt C in configuration (a), which is similar to the SiC MESFET capacitive loading property. At this parallel RC load impedance, the Bode-Fano criterion stated that

$$\int_0^{\infty} \ln \frac{1}{|\Gamma(\omega)|} d\omega < \frac{\pi}{RC} \quad (2.1)$$

where $\Gamma(\omega)$ is the reflection coefficient seen looking into the arbitrary lossless matching network.

$$\int_0^{\infty} \ln \frac{1}{|\Gamma|} d\omega = \int_{\Delta\omega} \ln \frac{1}{\Gamma_m} d\omega = \Delta\omega \ln \frac{1}{\Gamma_m} \leq \frac{\pi}{RC} \quad (2.2)$$

Equation (2.2) reveals that :

- For a given load (fixed RC product), a wider bandwidth ($\Delta\omega$) can only be achieved only with a higher reflection coefficient in the passband (Γ_m).
- The passband reflection coefficient, Γ_m , is not possible to be zero unless $\Delta\omega=0$. Thus a perfect match can be only achieved at a finite number of frequencies.
- As R or both C increase(s), the quality of the match ($\Delta\omega$ or both $1/\Gamma_m$) must decrease. Thus, the matching networks requirement is very difficult to achieve as it requires high Q circuits.

The above statements imply the limitations of broadband amplifier design. However, the limitations can be resolved using high impedance characteristic active devices, such as SiC MESFET. The next section shows how the limitations can be solved.

2.4 SiC MESFET Impedance Matrix

SiC MESFET, as the leading wide bandgap semiconductor, demonstrates a higher intrinsic impedance (source and load impedances), compared to other devices with similar power handling capability. Referring to the Bode-Fano's theorem, the match-able bandwidth for the given load depends on the function of quality factor, Q . Here, if the source and load impedances are higher, nearer to 50Ω , broadband matching networks will be simpler. Based on this constraint, SiC MESFET's higher intrinsic impedances makes broadband single-ended SiC MESFET amplifier possible with improvements in circuit topology, matching network design, bias network design, and power combining architectures.

The SiC MESFET possesses high output impedance properties, as shown in Figure 2.3, $Z_{11} = 0.8294\angle -142.3^\circ$ and $Z_{22} = 0.4703\angle -142.7^\circ$. This phenomenon makes single-stage broadband RF power amplifier design feasible as it reduces mismatch over a wide-range of frequencies due to S-parameters variations.

Figure 2.3 Input and output impedance of SiC MESFET.

The mutual impedance Z_{21} and Z_{12} are displayed in Figure 2.4. At the center frequency, $Z_{21} = 42.97\text{ dB} \angle 61.45^\circ$ and $Z_{12} = 11.9\text{ dB} \angle -23.36^\circ$.

(a)

(b)

Figure 2.4 Mutual impedance Z_{21} and Z_{12} of SiC MESFET

To investigate this property further, the SiC MESFET is terminated with input and output port losses from 0.1dB to 0.8dB, as shown in Figure 2.5.

Figure 2.5 Configuration of SiC MESFET terminated with input and output losses.

This configuration is simulated to investigate the impact on GMax decrement, which is shown in Figure 2.6.

Figure 2.6 Overall GMax performance of SiC MESFET terminated with input and output losses from 0.1dB to 0.8dB.

Figure 2.6 shows that the loss does not affect overall GMax decrement significantly. It demonstrates the device capability for single-stage RF broadband power amplifier design, with simple matching networks, despite matching networks losses over wide frequencies.

2.5 Basic Architecture of Single-Ended Power Amplifier

Engineers in RF and wireless industry are constantly seeking to design power amplifiers with broader bandwidth using new technologies. Previously, low frequency method of obtaining broader bandwidth includes feedback and distributed techniques. However, feedback is generally applied only far below a device's maximum usable frequency since there is a gain-bandwidth tradeoff. Distributed amplifiers show very attractive gain-bandwidth and gain flatness. However, it needs large transmission line structure and device periphery. Therefore, single-ended broadband power amplifier has been very attractive recently. For single-ended amplifier design using minimum amount of gate periphery and seeking to optimize gain efficiency and output power for a given bandwidth, simple reactive impedance matching is usually adopted. The generic circuit schematic is shown at Figure 2.7.

Negative feedback technique is preferred in broadband power amplifier design. Negative feedback circuit allows a flat gain response and reduces the input and output return losses over a wide frequency range. This configuration is less sensitive to transistor-to-transistor parameter variations. On the other hand, it tends to limit the maximum power gain of the transistor and increases its noise figures. Therefore, in LNA design, frequency compensated matching networks are preferable. Frequency matching

networks introduce the mismatch on either the input or output port of the device to compensate frequency that is introduced by S-parameters. However, this technique will trade off gain linearity and return losses. Gain linearity tends to improve at the expense of VSWR.

Negative feedback stabilizes the whole network. It allows the signal from the output of the transistor to be coupled back to the input with an opposite phase, thereby neutralizing S_{12} by making $S_{12}=0$. However, this technique might result in lower gain and higher input VSWR.

Figure 2.7 Configuration of single device, single-ended amplifier stage with simple reactive impedance matching

2.6 Design Considerations

Some considerations and basic principles need to be observed in the analysis and design of microwave transistor amplifiers. Based on the S parameters of the transistor provided and performance specification requirements, a systematic procedure is developed for the design of a microwave transistor amplifier.

The most important design considerations in microwave transistor amplifiers are stability, power gain, bandwidth, noise and dc requirements. A proper choice of microwave transistor is necessary, then a systematic mathematical solution should be developed to determine the transistor loading, which includes source and load reflection coefficients for a particular stability and gain criteria. An unconditionally stable transistor will not oscillate with any passive termination, while a potentially unstable transistor requires the proper passive terminations to produce a stable amplifier.

Besides the mentioned considerations, both passive and active DC bias networks for selected transistor should be carefully designed. It is necessary to select the correct dc operating point and the proper dc network topology to obtain the desired ac performance.

The single-ended microwave amplifier topology is shown in Figure 2.8.

Figure 2.8 Topology of a single-ended microwave amplifier

2.6.1 Stability Consideration

The stability of an amplifier is an important priority in designing power amplifier. It can be determined from S-parameters, matching networks and terminations. Generally, in

two-port network, oscillations may occur when either the input or output port presents a negative resistance. This occurs when $|\Gamma_{IN}| > 1$ or $|\Gamma_{OUT}| > 1$, which for an unilateral device [$S_{12}=0$] occurs when $|S_{11}| > 1$ or $|S_{22}| > 1$.

Unconditional stability defined when stability factor, $K > 1$; $|S_{11}S_{22} - S_{12}S_{21}| < 1$; auxiliary stability factor, $B_1 > 0$, $|S_{11}| < 1$ and $|S_{22}| < 1$. (Refer to Appendix 1 for detailed derivation).

From the theoretical point of view, a two-port network can have any value of K and $|\Delta|$. However, in reality, most available microwave transistors are either unconditionally stable or potentially unstable with $K < 1$ and $|\Delta| < 1$. In fact, in potentially unstable active devices most practical values of K are $0 < K < 1$. These potentially unstable transistors have the source and load stability circles that intersect with Smith chart.

2.6.2 Power Gain

In design of amplifiers for maximum gain, the purpose is to transform the input and output loads Γ_S and Γ_L to the matched counterparts of the device: Γ_{SM} and Γ_{LM} . This optimal source and load impedance will allow the maximum power transfer and gain through the two port networks (amplifier). Under this condition, the device is simultaneously conjugate matched.

Figure 2.9 Configuration of conjugate matching circuit.

A two-port network is considered stable at a given frequency when the real parts of input and output impedance are greater than zero for all passive load and source impedances.

Several power gain equations appear in the literature and are used in the design of microwave amplifiers. The transducer power gain G_T , the power gain G_P , and the available power gain G_A are defined as:

- G_T (transducer power gain) defines the ratio of power delivered to the load (P_L) to power available from the source (P_{AVS}).
- G_P (power gain) defines the ratio of power delivered to the load (P_L) to power input to the network (P_{IN}).
- G_A (available power gain) defines the ratio of power available from the network (P_{AVN}) to the power available from the source (P_{AVS}).

Refer to Appendix 2 for the definition of the general microwave two-port network theory.

Chapter 3 Small- Signal Modeling and Parameter Extraction

In power amplifier design, the intrinsic properties and behavior of active devices determine the major performance of the overall amplifier module. In this project, SiC MESFET is chosen as the prospective active device of broadband power amplifier design. Therefore, an accurate small-signal model development of SiC MESFET is required. The SiC MESFET packaged device from Cree (CRF24010) is used in the model derivation and development, which are elaborated in the following sections. The packaged device S-parameters are listed in Appendix 4.

3.1 MESFET Operation

A MESFET device has three terminals like any other FET transistors [9], [10]. The terminals are drain, source, and gate electrodes as shown in Figure 3.1.

Figure 3.1 SiC MESFET structure.

A MESFET device is biased by applying a voltage, V_{GS} between gate and source terminals and another voltage, V_{DS} between drain and source terminals [11]. These voltages vary the height of the gate-depletion region and control the channel current between drain and source. If V_{GS} is larger than the pinch-off voltage, V_p , three conditions can be observed in the I_{DS} - V_{DS} characteristic curve of the MESFET.

1. At low V_{DS} voltage, I_{DS} is linear to V_{DS} .
2. At moderate V_{DS} voltage, I_{DS} shows nonlinear relationship with V_{DS} .
3. At high V_{DS} voltage, current is almost constant or saturated.

Figure 3.2 shows SiC MESFET operating conditions at $V_p < V_{GS} < 0$ and varying V_{DS} values. Figure 3.2(a) shows the SiC MESFET configuration under low V_{DS} biasing. At this region, which is known as the linear region, I_{DS} versus V_{DS} shows linear relationship. Figure 3.2(b) shows the SiC MESFET configuration under moderate V_{DS} biasing. At this condition, I_{DS} starts showing nonlinear relationship with V_{DS} , indicated by a knee voltage phenomenon. Figure 3.2(c) exhibits the operation under large V_{DS} . This region is known as saturation region, where I_{DS} tends to be constant despite the changes of V_{DS} . The detail of each operation is elaborated in the following sections.

When $V_{GS}=0V$, the depletion region under Schottky-barrier gate is relatively narrow. As V_{DS} is increased from 0V to positive values, longitudinal electric field and current are developed in the channel. The voltage across the depletion region at the drain end is greater than at the source end, due to the applied V_{DS} . Therefore, the depletion region becomes wider at the drain end. The increased V_{DS} and the narrowing channel fasten the electrons movement between the drain and source terminals. At low V_{DS} , the current is linearly proportional to V_{DS} . However, as the reversed at the gate is increased, while

keeping the drain bias constant, the depletion region widens and the conductive channel becomes narrower, suppressing the current flow. Once V_{GS} approaches V_p , the drain current is zero as the channel becomes fully depleted, regardless of the V_{DS} values.

Under bias voltages which both V_{GS} and V_{DS} have strong effects on the drain current, it is said to be in its linear or voltage controlled resistive region. If V_{DS} is increased further as shown in Figure 3.2 (b), while $V_{GS} > V_p$, the channel current increases, depletion region becomes deeper at the drain end, and the conductive channel becomes narrower. As a result, while the conductive channel becomes narrower, the electrons move faster. However, the electrons velocity cannot exceed the saturated drift velocity. If V_{DS} is increased beyond the values that cause velocity saturation, the electron concentration must be increased to maintain constant current continuity. Eventually, a region of electron accumulates near the end of the gate. Conversely, after the electrons transit the channel and move at saturated velocity into the wide area between the gate and drain, an electron depletion region is formed.

As V_{DS} is increased further, as shown in Figure 3.2(c), progressively more of the voltage increase is dropped across this region to enforce the electrons to cross it and less is dropped across the unsaturated part of the channel. Eventually, a point is reached where further increase in V_{DS} is dropped entirely across the charge domain and does not substantially increase the drain current. At this point, the electrons move at saturated drift velocity over a large part of the channel length. When the MESFET is operated in this manner, it is said to be in saturation region. Figure 3.2 (a), (b), and (c) show the graphical illustration of the SiC MESFET operation on low V_{DS} , moderate V_{DS} and high V_{DS} , respectively when $V_{GS} < 0$.

Figure 3.2 SiC MESFET operation under different V_{DS} biasing with $V_{GS} < 0$: (a) Linear region (low V_{DS}); (b) moderate V_{DS} ; (c) high V_{DS} .

The small-signal model is derived according to the physical parameters origin of the MESFET device. Most of the available models are based on the model shown in Figure 3.3. This model is based on lumped-element model, which is applicable over a frequency range of several GHz.

Figure 3.3 Small-signal equivalent circuit of a MESFET and the physical origin of the circuit elements related to small-signal model.

The physical meaning of each element is interpreted as follow. L_S , L_D and L_G are the source, drain and gate inductances, respectively. R_S is the source, R_D is drain resistance, and R_G is the gate ohmic resistance, respectively. R_{GS} is the resistance of the region under the gate, between the source and the channel. C_{DS} is the drain-source capacitance that is dominated by geometric capacitance and is usually treated as a constant. C_{GS} and C_{GD} are the channel capacitances, which are nonlinear. I_{DS} is controlled by transconductance g_m , and transit time delay τ , and output resistance R_{DS} . C_{PG} , C_{PD} and C_{PGD} are the pad capacitances of gate, drain and gate-drain respectively.

Under large voltages, the forward bias or reverse avalanche breakdown gate junction can be included as diodes parallel with C_{GS} and C_{GD} . C_{GS} , C_{GD} and I_{DS} are usually nonlinear elements with their strong dependence on V_{GS} and V_{DS} . The circuit model can be divided into two parts, i.e. extrinsic parameters and intrinsic parameters. The intrinsic parameters illustrate the active region under the gate, which are functions of biasing conditions. The intrinsic parameters consist of R_{DS} , C_{DS} , C_{GS} , R_{GS} , g_m , and τ . The extrinsic parameters consist of other elements in the model, which are R_G , R_D , R_S , L_G , L_D , L_S , C_{PG} , C_{PD} , and C_{PGD} . The intrinsic elements C_{DS} , R_{GS} , and τ , are usually presumed as linear due to their negligible dependence on the internal voltages. However, some of intrinsic parameters may be nonlinear if their dependence on the internal voltages is significant.

3.1.1 Parasitic Inductances

The inductances of extrinsic part of the circuit model are represented by parasitic inductances which consist of L_G , L_D , and L_S . Metal contact pads deposited on the device surface result in those inductances. The gate inductance is usually the largest of the three, while the source inductance is comparably small at short gate length devices. These inductances are particularly applicable for bare die devices, hence, for packaged device, any other inductances such as parasitic wire bond inductances or parasitic package inductances must be taken into account for complete circuit model.

3.1.2 Parasitic Resistances

The parasitic resistances R_G , R_D , and R_S are classified as extrinsic parameters. The resistance of the ohmic contacts between the metal electrodes and the N+SiC as well as any bulk resistance leading up to the active channel is characterized as R_S and R_D . The

metallization resistance of the gate of Schottky contact is represented by R_G , the gate resistance. Generally, all three resistances values are considerably small. R_S and R_D are presumed to be constant by most of commercial simulators, although they show a slight bias dependence. However, for significant bias voltages dependence, the nonlinearity must be taken into consideration to result in a more accurate model. Usually, all parasitic resistance values are estimated either from forward DC conduction measurements or directly from cold technique S-parameters measurements. The cold FET technique is preferable as it calculates from high frequency data at the respective bias point.

3.1.3 Pad Capacitances

Pad capacitances are part of extrinsic parameters of the small-signal model. They represent the stray capacitance between the metal pads. The pad capacitances consist of crossover capacitance of the metal lines and the capacitance between the pad and the back face of the semi-insulating substrate that is connected to the source terminal. Generally, the crossover capacitance is much smaller than the substrate capacitance [12]. These pad capacitances consist of the drain pad capacitance C_{PD} , the gate pad capacitance C_{PG} , and the capacitance between the gate pad and drain pad C_{PGD} . C_{PGD} is treated as feedback capacitance between the gate and drain pads. Generally, C_{PGD} is very small, hence it is negligible. The pad capacitances can be placed in two different locations in the small-signal model, either on the most outer terminals of the models or between the corresponding parasitic inductances and resistances as shown in Figure 3.5.

3.1.4 Intrinsic Capacitances

Intrinsic capacitances include C_{GS} , C_{GD} , and C_{DS} . The changes in the depletion region charge with respect to the gate-source and gate-drain voltages are illustrated by C_{GS} and

C_{GD} , respectively. Figure 3.4 shows the depletion region beneath the gate for a symmetric structure where the gate is located midway between the source terminal and drain terminal.

Figure 3.4 Depletion region shapes for different applied bias voltages: (a) Gate-source voltage is equal to gate-drain voltage ($V_{DS} = 0$); (b) Gate-drain reverse bias is larger than gate-source reverse bias.

Figure 3.4(a) illustrates a symmetric bias case when $V_{DS} = 0$ ($V_{GS} = V_{GD}$). Figure 3.4 (b) shows the case when the gate-drain reverse bias is greater than the gate-source reverse bias, which represents the normal MESFET bias conditions in most applications. Figure 3.4 is used to derive the physics of both C_{GS} and C_{GD} . The distribution of the depletion charge is symmetric with respect to the drain and source in Figure 3.4(a). On the other hand, the depletion charge extends deeper at the drain end of the gate than at the source end of the gate and it extends closer to the drain than to the source. This charge distribution in the depletion region with the bias voltage variation identifies the two

depletion region C_{GS} and C_{GD} . The charge of the depletion region is shared between C_{GS} and C_{GD} which is defined in equations (3.1) and (3.2) respectively.

$$C_{GS} = \left. \frac{\partial Q_G}{\partial V_{GS}} \right|_{V_{GD} = \text{const}} \quad (3.1)$$

$$C_{GD} = \left. \frac{\partial Q_G}{\partial V_{GD}} \right|_{V_{GS} = \text{const}} \quad (3.2)$$

Under normal operating conditions, V_{GS} and V_{DS} are the DC controlling bias voltages. Therefore, the gate to source capacitance is often defined as:

$$C_{GS} = \left. \frac{\partial Q_G}{\partial V_{GS}} \right|_{V_{DS} = \text{const}} \quad (3.3)$$

Equations (3.1) and (3.2) are similar, although their values are slightly different. The difference is considerably small, but can be significant if calculations are based on physical model. In the physical model the depletion charge is defined by mathematical expression. In this thesis, capacitances are calculated from S-parameters measurements. The voltages showed in the capacitance definitions are the internal voltages, not the terminal voltages.

It is well known from depletion capacitance analysis that the depletion capacitance decreases as the reverse junction voltage increases. Therefore, under normal bias conditions, the gate-drain capacitance C_{GD} is generally smaller in magnitude compared to C_{GS} ; nevertheless, C_{GD} is critical for obtaining accurate S-parameters predictions. The drain-source capacitance C_{DS} is included in the equivalent circuit as geometric capacitance affects derivation between the source and drain electrodes. Generally, it is considered as bias independent for device modeling purposes.

3.1.5 Charging Resistance R_{GS}

R_{GS} is generally included to improve S_{11} match although it represents the intrinsic resistance under the gate between the source and the channel. For many devices, the extrinsic pad resistance R_G is adequate to match the real part of S_{11} . For power devices, R_{GS} is difficult to extract, hence it is difficult to differ between R_G and R_{GS} . This extraction process will be discussed in section 3.3.

3.1.6 Output Resistance R_{DS}

The output resistance R_{DS} is generally represented by its reciprocal, the output conductance g_{DS} . R_{DS} is the incremental resistance between drain and source. In other words, the output conductance defines the incremental change in output current I_{DS} with output voltage V_{DS} . Hence, it can be defined as the slope of $I_{DS} - V_{DS}$ characteristics at constant gate-source voltage. The output conductance and resistance can be derived as:

$$g_{DS} = \frac{1}{R_{DS}} = \left. \frac{\partial I_{DS}}{\partial V_{DS}} \right|_{V_{GS} = \text{constant}} \quad (3.4)$$

The output conductance of the device is an important characteristic in analog applications. It plays a significant role in determining the maximum voltage gain attainable from a device and is extremely important for determining optimum output matching properties. Generally, it is preferable to have a device with extremely high output resistance, or equivalently, low output conductance, as it will simplify the matching networks required. The low frequency dispersion is more significant in output conductance than in the transconductance. The RF values of transconductance and output conductance are important elements in small-signal modeling process, while both RF and DC values are important for accurate large-signal modeling.

3.1.7 Transconductance, g_m

The small-signal gain is derived from transconductance. The transconductance g_m , is a measure of the incremental change in the output current I_{DS} by varying the internal gate-source input voltage V_{GS} across gate-source junction. In other words, the device transconductance is the slope of the $I_{DS} - V_{GS}$ characteristics with constant drain-source voltage. It can be derived as :

$$g_m = \left. \frac{\partial I_{DS}}{\partial V_{GS}} \right|_{V_{DS} = \text{constant}} \quad (3.5)$$

The device transconductance shows device quality for microwave and millimeter wave applications. With all other equal characteristics, a device with high transconductance will give greater gain and better high frequency performance. Unfortunately, low dispersion frequency commonly affects transconductance. The low frequency dispersion is caused by a parameter variation at low frequencies due to the deep levels in the device structure. In other words, it strongly depends on the semiconductor material quality and fabrication processes. Therefore, the transconductance varies with frequency below 1MHz. RF values of transconductance are typically 5 to 25% lower than DC values for SiC MESFET. Transconductance value varies proportionally to gate width and inversely wide gate length.

3.1.8 Transit Time, τ

The transconductance need time to respond changes in gate-source voltage. The delay is illustrated as transit time (transconductance delay) τ . In physical content, the transconductance delay represents the time that takes for the charge to redistribute itself

after a fluctuation of the gate voltage. Typical values of τ are on the order of 1 psec. From physical considerations, transit time is expected to increase with increasing gate length.

3.2 Small-Signal Modeling and Parameter Derivation

Figure 3.5 shows the most commonly adopted MESFET model at normal bias operating conditions in the saturation region.

Figure 3.5 Small-signal equivalent circuit of SiC MESFET.

As mentioned earlier, MESFET model is classified into two group parameters, i.e. extrinsic and intrinsic parameters. The extrinsic parameters include C_{PG} , C_{PD} , C_{PGD} , R_G , R_D , R_S , L_G , L_D and L_S . The intrinsic parameters consist of C_{gs} , R_{gs} , R_{gd} , g_m , τ , R_{ds} , and C_{ds} . To have the smooth transition from the symmetric cold model ($V_{ds}=0$) to operating points in saturation region, R_{gd} has been added [12]. The main purpose of an extraction process is to remove the extrinsic element parameters from the measurements. Since the

intrinsic section exhibits PI topology, the Y parameters are the most preferable parameters.

3.2.1 Intrinsic Y-Parameters Derivation

Figures 3.6 to 3.9 present the process of Y-parameters determinations. The initial values of some intrinsic elements (R_{ds} , g_m , and τ) were evaluated according to the procedure given in [13]. The measured S-parameters of the device are stored in S-matrix.

Figure 3.6 De-embedding (subtracting) of inductances L_G and L_D .

Figure 3.6 shows the de-embedding configuration of extrinsic gate and drain inductances, L_G and L_D , respectively. The S-matrix S_{measured} in Figure 3.6 is converted into Z-parameters (T-configuration) matrix Z_{int3} $[S_{\text{measured}} \rightarrow Z_{\text{int3}}]$. The parasitic inductances L_G and L_D are subtracted from Z_{int3} .

$$Z_{\text{int2}} = Z_{\text{int3}} - j\omega \begin{bmatrix} L_G & 0 \\ 0 & L_D \end{bmatrix} \quad (3.6)$$

Figure 3.7 De-embedding of the parasitic capacitances C_{PG} , C_{PD} , and C_{PGD} .

The Z-parameters Z_{int2} in Figure 3.7 are converted into Y-parameters Y_{int2} (π -configuration). Pad capacitances C_{PG} , C_{PD} , and C_{PGD} are subtracted from Y_{int2} . The result is Y_{int1} .

$$Y_{int1} = Y_{int2} - j\omega \begin{bmatrix} C_{PG} + C_{PGD} & -C_{PGD} \\ -C_{PGD} & C_{PD} + C_{PGD} \end{bmatrix} \quad (3.7)$$

Y_{int1} is converted into Z_{int1} by a matrix inversion: $[Z_{int1} = Y_{int1}^{-1}]$. This matrix conversion purpose is to subtract the series extrinsic resistances (T-configuration). Figure 3.8 shows the de-embedding configuration of extrinsic gate resistance R_G , drain resistance R_D and source resistance and inductance, R_S and L_S respectively. Equation (3.8) shows the de-embedding configuration in matrix form.

Figure 3.8 De-embedding of the resistances R_G , R_D and R_S .

$$Z_{\text{int}} = Z_{\text{int}1} - \begin{bmatrix} R_G + R_S - j\omega L_S & R_S - j\omega L_S \\ R_S - j\omega L_S & R_D + R_S - j\omega L_S \end{bmatrix} \quad (3.8)$$

Then, the intrinsic MESFET Z-parameters are converted into Y-parameters as shown in Figure 3.9.

$$Y_{\text{int}} = Z_{\text{int}}^{-1} \quad (3.9)$$

Figure 3.9 Intrinsic Z-parameters are converted into Y-parameters.

From equation (3.9), the de-embedded intrinsic Y-parameters, Y_{int} , can be expressed in a matrix form:

$$Y_{\text{int}} = \begin{bmatrix} Y_{11\text{int}} & Y_{12\text{int}} \\ Y_{21\text{int}} & Y_{22\text{int}} \end{bmatrix} = \begin{bmatrix} \text{Re}(Y_{11\text{int}}) + j \text{Im}(Y_{11\text{int}}) & \text{Re}(Y_{12\text{int}}) + j \text{Im}(Y_{12\text{int}}) \\ \text{Re}(Y_{21\text{int}}) + j \text{Im}(Y_{21\text{int}}) & \text{Re}(Y_{22\text{int}}) + j \text{Im}(Y_{22\text{int}}) \end{bmatrix} \quad (3.10)$$

Equation (3.10) shows the Y_{int} elements are classified into real and imaginary parts. Real parts are denoted by “Re” while imaginary parts are denoted by “Im”. From derivations and analytical model shown in Figure 3.1, Y_{int} parameters are defined as follow:

$$Y_{11\text{int}} = \frac{1}{R_{gs} + \frac{1}{j\omega C_{gs}}} + \frac{1}{R_{gd} + \frac{1}{j\omega C_{gd}}} \quad (3.11)$$

$$Y_{12\text{int}} = -\frac{1}{R_{gd} + \frac{1}{j\omega C_{gd}}} \quad (3.12)$$

$$Y_{21\text{int}} = \frac{g_m e^{-j\omega\tau}}{1 + j\omega C_{gs} R_{gs}} - \frac{1}{R_{gd} + \frac{1}{j\omega C_{gd}}} \quad (3.13)$$

$$Y_{22\text{int}} = \frac{1}{R_{ds}} + j\omega C_{ds} + \frac{1}{R_{gd} + \frac{1}{j\omega C_{gd}}} \quad (3.14)$$

Equations (3.11) to (3.14) can be summarized in equation (3.15):

$$Y_{\text{int}} = \begin{bmatrix} \frac{\omega^2 R_i C_{gs}^2}{|D_1|^2} + \frac{\omega^2 R_{gd} C_{gd}^2}{|D_2|^2} + j\omega \left(\frac{C_{gs}}{|D_1|^2} + \frac{C_{gd}}{|D_2|^2} \right) & -\frac{\omega^2 R_{gd} C_{gd}^2}{|D_2|^2} - j\omega \frac{C_{gd}}{|D_2|^2} \\ \frac{g_m e^{-j\omega\tau}}{D_1} - j\frac{\omega C_{gd}}{D_2} & g_{ds} + \frac{\omega^2 R_{ds} C_{gd}^2}{|D_2|^2} + j\omega \left(C_{ds} + \frac{C_{gd}}{|D_2|^2} \right) \end{bmatrix}$$

where D_1 and D_2 are defined in equation (3.15) :

$$D_1 = 1 + j\omega R_{gs} C_{gs} \text{ and } D_2 = 1 + j\omega R_{gd} C_{gd} \quad (3.15)$$

3.2.2 Intrinsic Parameter Determination

From equation (3.15), all the intrinsic parameters are extracted in terms of intrinsic Y-parameters. More detailed derivations of Y-parameters, Y_{int} are discussed in Appendix 3.

The intrinsic parameters can be stated as:

$$C_{gs} = \frac{(1 + d_1^2)}{\omega} (\text{Im}(Y_{11\text{int}}) + \text{Im}(Y_{12\text{int}})) \quad (3.16)$$

$$R_{gs} = \frac{d_1}{(1 + d_1^2) (\text{Im}(Y_{11\text{int}}) + \text{Im}(Y_{12\text{int}}))} \quad (3.17)$$

$$C_{gd} = -\frac{\text{Im}(Y_{12\text{int}})}{\omega} (1 + d_2^2) \quad (3.18)$$

$$R_{gd} = -\frac{d_2}{(1 + d_2^2) \text{Im}(Y_{12\text{int}})} \quad (3.19)$$

$$g_m = |G| \quad (3.20)$$

$$\tau = -\frac{1}{\omega} \angle(G) \quad (3.21)$$

$$R_{ds} = \frac{1}{\text{Re}(Y_{22\text{int}}) + \text{Re}(Y_{12\text{int}})} \quad (3.22)$$

$$C_{ds} = \frac{\text{Im}(Y_{22\text{int}}) + \text{Im}(Y_{12\text{int}})}{\omega} \quad (3.23)$$

Defined :

$$d_1 = \frac{\text{Re}(Y_{11\text{int}}) + \text{Re}(Y_{12\text{int}})}{\text{Im}(Y_{11\text{int}}) + \text{Im}(Y_{12\text{int}})} \quad (3.24)$$

$$d_2 = \frac{\text{Re}(Y_{12\text{int}})}{\text{Im}(Y_{12\text{int}})} \quad (3.25)$$

$$G = g_m e^{-j\omega\tau} = (Y_{\text{int } 21} - Y_{\text{int } 12})(1 + jd_1) \quad (3.26)$$

$$= \sqrt{((\text{Re}(Y_{21\text{int}}) - \text{Re}(Y_{12\text{int}}))^2 + (\text{Im}(Y_{21\text{int}}) - \text{Im}(Y_{12\text{int}})))^2 (1 + jd_1)}$$

$$\angle \tan^{-1} \left(\frac{d_1 (\text{Re}(Y_{21\text{int}}) - \text{Re}(Y_{12\text{int}})) + (\text{Im}(Y_{21\text{int}}) - \text{Im}(Y_{12\text{int}}))}{(\text{Re}(Y_{21\text{int}}) - \text{Re}(Y_{12\text{int}})) - d_1 (\text{Im}(Y_{21\text{int}}) - \text{Im}(Y_{12\text{int}}))} \right)$$

3.3 Derivations of Extracted Parasitic Capacitance

Parasitic capacitances are commonly derived or extracted under pinch-off mode. Simplified model of SiC MESFET can be derived at pinch-off mode operating point, when gate-source bias voltage less than or equal to the pinch-off voltage of the device, V_p , with zero drain-source bias voltage. This simplified model is highly symmetric, that required much simpler analysis. At pinch-off voltages, the channel is closed and therefore it results high resistance (R_{ds}) between the drain and the source. Hence, C_{ds} is the more dominant component between the drain and the source.

At pinch-off voltage, no current is flowing from drain to source, therefore $g_m = 0$. Since both gate-drain and gate-source junctions are reverse biased, C_{gs} and C_{gd} are too small and therefore, R_{gs} and R_{gd} are negligible. Figure 3.10 shows the simplified equivalent circuit at $V_{gs} < V_p$.

Figure 3.10 Simplified equivalent MESFET circuit at pinch-off mode ($V_{gs} < V_p$).

At $V_{ds} = 0$, the device structure is symmetric, therefore it is presumed that $C_{gs} = C_{gd} = C_F$ (C_F is the fringing capacitance). This simplified model is useful to calculate the pad capacitances C_{PG} , C_{PD} , and C_{PGD} .

3.3.1 Extraction of Pad Capacitances

At zero drain-source bias, and gate source voltage lower than pinch-off voltage, the intrinsic capacitance under the gate (C_{gs} and C_{gd}) cancels out. Therefore, the fringing capacitances C_F dominate gate-source and gate-drain capacitances at the extension of the depleted layer at each side of the gate [14].

All parasitic inductances and resistances have no significant influence on the imaginary part of Y-parameters at low frequencies up to few gigahertz. Therefore, the parasitic resistances and inductances can be neglected, results in simpler equivalent circuit configuration as shown in Figure 3.11.

Figure 3.11 Equivalent circuit in the pinch-off mode at low frequencies.

The analytical equations (3.27) to (3.29) of the Y-parameters are determined from Figure 3.11

$$\text{Im}(Y_{11}) = \omega(C_{PG} + 2C_F / 3 + C_{PGD}) \quad (3.27)$$

$$\text{Im}(Y_{12}) = \omega(-C_F / 3 - C_{PGD}) \quad (3.28)$$

$$\text{Im}(Y_{22}) = \omega(C_{PD} + 2C_F / 3 + C_{PGD}) \quad (3.29)$$

It is observed that all imaginary parts of Y-parameters are linearly proportional to the frequency. However, there are only three independent equations with four unknowns: C_{PG} , C_{PGD} , C_{PD} , C_F . Therefore, direct parasitic capacitances extraction from the measured Y-parameters are not possible. Other approaches are required to determine the parasitic capacitances. The methods are:

1. Neglect the effect of parasitic capacitance C_{PGD} at the initial analysis and iteration, thus, the other parasitic capacitances, C_{PG} , C_{PD} , and fringing capacitances C_F can be derived as follow:

$$C_F = -3 \text{Im}(Y_{12}) / \omega \quad (3.30)$$

$$C_{PG} = \text{Im}(Y_{11}) / \omega - 2 \text{Im}(Y_{12}) / \omega \quad (3.31)$$

$$C_{PD} = \text{Im}(Y_{22}) / \omega - 2 \text{Im}(Y_{12}) / \omega \quad (3.32)$$

2. Optimize the extracted parasitic capacitance values. The start value of C_{PGD} is selected to keep the discrepancies between the measured and simulated imaginary Y-parameters at minimum. The error function is represented in equation (3.33).

$$\varepsilon = \sum_{ij=1}^2 \left(\frac{|\text{Im}(Y_{measij}) - \text{Im}(Y_{simij})|^2}{|\text{Im}(Y_{measij})|^2} \right) \quad (3.33)$$

where $\text{Im}(Y_{measij})$ is the imaginary part of measured Y-parameters, while $\text{Im}(Y_{simij})$ is imaginary part of simulated Y-parameters.

3.3.2 Optimization of Extracted Parasitic Capacitances

Firstly, the Y-parameters are extracted from the device. The extraction steps are provided as follows.

1. Calibrate the two-port vector network analyzer with coaxial standards (short, open and load) from 0.1GHz to 4 GHz.
2. Measure S-parameters of the SiC MESFET at pinch-off mode operating point, when gate-source bias voltage is less than or equal to the pinch-off voltage of the device, V_p , with zero drain-source bias voltage.
3. Convert S-parameters into Y parameters according to the equations (3.34) to (3.37)

Figure 3.12 Configuration of [S] to [Y] parameters conversion

$$Y_{11} = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{Z_0 \psi} \quad (3.34)$$

$$Y_{22} = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{Z_0 \psi} \quad (3.35)$$

$$Y_{12} = \frac{-2S_{12}}{Z_0 \psi} \quad (3.36)$$

$$Y_{21} = \frac{-2S_{21}}{Z_0 \psi} \quad (3.37)$$

The result is shown in Figure 3.13.

Figure 3.13 Measured imaginary Y-parameters of SiC MESFET.

At first iteration, C_{PGD} is presumed to be zero. Both simulated and measured Y-parameters are compared as shown in Figure 3.14. Figure 3.15 shows the extracted parasitic capacitances over frequencies.

Figure 3.14 Simulated and measured S-parameters after optimization.

Figure 3.15 Optimized parasitic capacitances vs. frequency.

The optimized parasitic capacitance values are used in the schematic. The Y-parameters are generated and shown in Figure 3.16.

Figure 3.16 ANSOFT simulation result of optimized parasitic capacitances values.

3.4 Derivations of Parasitic Resistances and Inductances

Parasitic resistances and inductances are determined under forward bias condition at cold FET measurements. This condition is defined when $V_{DS} = 0$ and the gate current

$I_g > 0$. Under forward bias condition, the transistor shows nonlinear performance. Therefore, diode model is used to replace intrinsic FET model that depends on external gate voltage. The simplified equivalent circuit is shown in Figure 3.17.

Figure 3.17 Simplified equivalent circuit at forward bias.

The parasitic inductances L_G , L_D , and L_S , and parasitic resistances R_G , R_S , and R_D in Figure 3.17 are derived from Z-parameters of the equivalent circuit. The following equations are applied [15].

$$Z_{11} = R_G + R_S + \frac{R_C}{3} + \frac{r_d}{1 + (\omega r_d c_j)^2} + j\omega \left(L_G + L_S - \frac{c_j r_d^2}{1 + (\omega r_d c_j)^2} \right) \quad (3.38)$$

$$Z_{12} = Z_{21} = R_S + \frac{R_C}{2} + j\omega L_S \quad (3.39)$$

$$Z_{22} = R_D + R_C + R_S + j\omega(L_S + L_D) \quad (3.40)$$

When the gate current I_g increases, r_d decreases and c_j increases, r_d responses exponentially to V_{gs} . Hence, r_d is the dominant factor which can be written in equation (3.41).

$$r_d = \frac{nkT}{q} \frac{1}{I_g} \quad (3.41)$$

By substituting equation (3.41) to equation (3.38), the latter can be written as the function of I_g , as shown in (3.42) and (3.43).

$$\text{Re}(Z_{11}) = f\left(\frac{1}{I_g}\right) = R_G + R_S + \frac{R_C}{3} + r_d = R_G + R_S + \frac{R_C}{3} + \frac{nkT}{q} \frac{1}{I_g} \quad (3.42)$$

$$\text{Im}(Z_{11}) = f\left(\frac{1}{I_g^2}\right) = \omega(L_G + L_S + c_j r_d^2) = \omega\left(L_G + L_S - c_j^2 \left(\frac{nkT}{q}\right)^2 \frac{1}{I_g^2}\right) \quad (3.43)$$

3.4.1 Derivation of Parasitic Inductances

The parasitic inductances L_D and L_S are derived from equations (3.39) and (3.40). The source inductance L_S is derived from imaginary part of Z_{12} or Z_{21} . Drain inductances L_D is derived as:

$$L_D = \frac{1}{\omega} \text{Im}(Z_{22} - Z_{12}) \quad (3.44)$$

Next, gate inductance, L_G can be extracted from equation (3.38) by manipulating line equation as $Y = mX + C$; where

$$C = L_G + L_S \text{ and } m = -c_j \left(\frac{nkT}{q}\right)^2 \quad (3.45)$$

Figure 3.18 represents equation (3.45). The linear relation of $\text{Im}(Z_{11})$ and I_g gives the sum of L_S and L_G .

Figure 3.18 Relations of Im (Z_{11}) and I_g .

By using extrapolation, when I_g^2 tends to infinity, $\left(\frac{1}{I_g^2}\right) \approx 0$ and $\text{Im}(Z_{11})/\omega \approx L_G + L_S$.

3.4.2 Derivation of Parasitic Resistances

Parasitic resistances can be derived from equations (3.38) to (3.40). However there are only three independent equations with four unknowns R_G , R_S , R_D , and R_C . Therefore, it is difficult to extract those parameters directly. There is also dependency of channel resistance R_C on gate-source external voltage (V_{GS}) that can be expressed in equation (3.46) [16].

$$R_C = \frac{R_{C0}}{1 - \sqrt{\frac{V_{GS} - V_{bi}}{V_p}}} \quad (3.46)$$

By substituting equation (3.46) to equation (3.40), the real part of Z_{22} can be expressed as shown in equation (3.47).

$$\text{Re}(Z_{22}) = R_s + R_D + \frac{R_{C0}}{1 - \sqrt{\frac{V_{GS} - V_{bi}}{V_p}}} \quad (3.47)$$

R_{C0} is defined as an independent voltage channel resistance, whereas V_{bi} is the built-in voltage of Schottky diode at forward bias condition when $V_{DS} = 0$. The built-in voltage V_{bi} , is estimated from I_g relation with V_{GS} . The intercept point of the slope to the X-axis is referred to V_{bi} . Figure 3.19 shows the derivation of diode built-in voltage from forward-bias diode characteristics at $V_{DS} = 0$, with V_{GS} values from 0.8V to 1.05V. From the graphical estimation, the built-in voltage, V_{bi} , is estimated at 0.9V.

Figure 3.19 Derivation of diode built-in voltage from forward-bias diode characteristics at $V_{DS}=0$

The sum of $R_D + R_S$ was estimated [15], with the following procedures:

1. Convert measured S-parameters to Z-parameters, due to the T-configuration.

The S-parameters are measured at different V_{GS} values between V_p and V_{bi} .

2. Plot the real part of Z_{22} versus frequency. Average values of different V_{GS} is extracted, and plotted. Refer to Figure 3.20. The curve nonlinearity can be

expressed in equation (3.48), which will be fitted to the measured Z-parameters (Z_{22}) versus V_{GS} .

$$f(V_{GS}) = A + \frac{B}{1 - \sqrt{\frac{V_{GS} - V_{bi}}{C}}} \quad (3.48)$$

The constants A, B and C refer to $R_S + R_D$, R_{C0} and V_p respectively. To simplify the derivations, equation (3.48) is approximated to be linear, which can be written as in equation (3.49).

$$f(V_{GS}) = A + Bx \quad (3.49)$$

where

$$x = \frac{1}{1 - \sqrt{\alpha}} \text{ and } \alpha = \frac{V_{GS} - V_{bi}}{V_p}$$

Figure 3.20 Relation between extracted Re (Z_{22}) and $V_p < V_{GS} < V_{bi}$.

By plotting equation (3.49), constants A and B can be extracted based on the linear regression technique (LRT) as the intercept of the Y-axis and the gradient of the curve, which is presented in Figure 3.21.

Figure 3.21 Estimation of coefficient A from equation (4.40).

The extrinsic parameters values are summarized in Table 2.

Table 2 SiC MESFET extrinsic parameters values.

Extrinsic Parameter	Value	Unit
C_{PG}	0.77	pF
C_{PD}	1.25	pF
C_{PGD}	0	pF
L_G	0.40	nH
L_S	0.25	nH
L_D	0.17	nH
R_G	0.63	Ω
R_S	0.68	Ω
R_D	0.16	Ω

3.5 Extraction of SiC MESFET Intrinsic Parameters

The extraction of intrinsic small-signal parameters follows Dambrine procedure [17].

The intrinsic elements consist of C_{gs} , R_{gs} , R_{gd} , g_m , τ , and R_{ds} , which can be determined by equations (3.16) to (3.23). The Y-parameters are measured and averaged at given V_{GS} and V_{DS} .

To have accurate and reasonable values, the derived values are considered as starting values of optimization in Microwave Office (MWO). Figures 3.22 to 3.24 are the simulated and measured S-parameters after optimization from 100MHz to 4GHz. Figures 3.22 and 3.23 plot S_{11} and S_{22} parameters of SiC MESFET at biasing conditions $V_{DS}=48V$ and $I_{DS}=500mA$, respectively. Figure 3.24 shows the S_{21} and S_{12} parameters respectively.

It is observed that the simulated S-parameters are in good agreement with the measured S-parameters. However, the reverse transmission coefficient parameter S_{12} , has large discrepancy compared to other parameters. However, it might be considered acceptable, since the value of S_{12} is much smaller compared to S_{21} . While all other measured and modeled S-parameters are very close, the extraction procedure is considered fairly accurate.

Figure 3.22 Measured and simulated S_{11} of SiC MESFET for frequency range 100MHz to 4GHz at $V_{DS} = 48V$ and $I_{DS} = 500mA$.

Figure 3.23 Measured and simulated S_{22} of SiC MESFET for frequency range 100MHz to 4GHz at $V_{DS} = 48V$ and $I_{DS} = 500mA$.

Figure 3.24 Measured and simulated S_{21} and S_{12} of SiC MESFET for frequency range 100MHz to 4GHz at $V_{DS} = 48V$ and $I_{DS} = 500mA$.

Chapter 4 DC Nonlinear Characterization

4.1 Modeling in General

By definition, a transistor model is a simplified of the physical entry, constructed to enable analysis to be made in a relatively simple manner. It means that models, although useful, may not be applicable for some application. Designers must learn the useful range of application for each model since all active devices are nonlinear. That can be observed by measuring harmonic output power or intermodulation products at any input RF power level, under any bias conditions. Therefore, the nonlinear model is more presentable than the linear model.

Generally, there are two types of large-signal transistor models. They are the physical or “physics-based” device models and the measurement-based models. Measurement-based models are further classified into analytical model, such as SPICE models and black box models.

Large signal modeling is generally best-suited by measurement-based models. These are empirical models either constructed using analytical equations and called “analytical models” or based on a lookup table developed from the measured data. The latter are known as “table-based” models. For analytical models, the coefficients of the equations serve as a fitting parameter to allow the equations to approximate the measured data. Functions are usually chosen with functional behavior similar to measured data so that the number of fitting parameters is reduced.

The advantages of analytical or empirical models are computational efficiency, automatic data smoothing, and accommodation of device statistics, physical insight, and the ability to be modified in a systematic manner. Disadvantages include restriction of

applicable situation due to over-simplified expressions, and difficulty in parameter extraction in some operating condition. The restricted applicable situation due to the nonphysical behavior, such as polynomial function, only designed to fit data over a specific range of voltages. Therefore, the function may not fit well outside the fitting range. However, the major advantage of analytical model is that most of commercial microwave nonlinear simulators provide some sort of user-defined model interface for analytical model insertion.

The large signal equivalent circuits are usually based on device properties, voltage-current and voltage-charge relations. For most available models, the drain-current expression is not based on the physics of device. The derived equations just resemble tanh curves to approximate the measured or experimental data. The model can be fitted to various devices based on measurements.

The well-known large signal FET model was developed by Curtice in 1980, who famously known, introduced a “quadratic model,” or polynomial law dependency in the “ohmic” region and model saturation in the drain-source current [18]. This model has been continuously improved by many researchers. For example, Tajima models in 1981 and 1984 showed a better fit to dc characteristics and were used in large-signal analysis [19]. In 1983 and 1985, Materka-Kacprzak came with their better-suited model, with fewer parameters, that provided good fits to measured dc data [20]. Statz introduced the Raytheon (Statz) model in 1987, that demonstrated good accuracy by overcame Curtice model limitations, although pinch off voltage dependency on V_{DS} was still neglected [21]. In the later years, Triquint developed the modification of Statz model that is well-known as the Triquint’s Own Model (TOM), which improved the accuracy. Most of these

models are empirical in nature, requiring extensive dc and RF data to obtain good fits to measured results. Many commercial simulators have updated these models inside their nonlinear libraries. Notable examples are the Curtice [18], Materka-Kacprzac [20], and Angelov [22-23] models.

4.2 Equivalent Circuit

The large signal model is approximated on a multiple bias small-signal model. Figure 4.1 shows the equivalent large-signal circuit, which shows the nonlinear parameters of the device under large-signal condition. This circuit features nonlinear elements, such as the gate-source diode d_{GS} , gate-drain diode d_{GD} , the gate-source capacitance C_{GS} , the gate-drain capacitance C_{GD} , the drain-source capacitance C_{DS} , the static drain source I_{dsDC} , as well as the dispersion current source I_{dsRF} .

Figure 4.1 SiC MESFET large signal equivalent circuit.

4.3 Nonlinearity DC I-V Derivation

The dependency of drain-source current (I_{ds}) on gate-source is commonly presented in the algebraic expressions that are used in the commercial simulators. Each model exhibits different approach compared to others. In this section, the simulated I-V results from the model are fit into the measured I-V of SiC MESFET. The DC model parameters are optimized and adjusted using MWO. In this process, the average absolute difference between simulated and measured drain current can be minimized. The objective function ε is defined to compare the discrepancies between the simulation using MWO and the measurements.

$$\varepsilon = \frac{1}{N} \left\{ \frac{|I_{ds,m} - I_{ds,s}|^2}{I_{ds,m}^2} \right\} \quad (4.1)$$

where N is the number of bias points, $I_{ds,m}$ is the measured drain current and $I_{ds,s}$ is the simulated drain current.

4.3.1 TriQuint's Own Model

TOM stands for TriQuint's Own Model. TOM3 is the implementation of a model developed by TriQuint Inc., that can predict the negative output conductance in the high dissipated power region, which occurs due to self-heating. Nowadays, their models have become popular outside the TriQuint foundry as well. The equivalent circuit of this model is shown in Figure 4.2. This model includes extrinsic parameters, such as extrinsic gate resistance R_G , inductance L_G , drain resistance R_D , inductance L_D , source resistance R_S and inductance L_S . Intrinsic parameters, such as gate to drain capacitance C_{GD} , gate to source capacitance C_{GS} , and drain to source capacitance C_{DS} , are also

included. Gate-to- channel diodes and leakage diodes are added in this model to represent the nonlinearity of gate-to-channel junction and leakage from drain-to- channel, respectively.

Figure 4.2 TOM3 equivalent circuit model.

The TriQuint Own Model DC drain-source current is derived using the following equations [24].

$$I_{ds} = \beta(V_G)^Q (1 + \lambda V_{ds}) \frac{\alpha V_{ds}}{(1 + (\alpha V_{ds})^k)^{\frac{1}{k}}} \quad (4.2)$$

$$V_G = QV_{st} \ln(1 + e^u) \quad (4.3)$$

$$u = \frac{V_{gs} - V_{th} + \mathcal{W}_{ds}}{QV_{st}} \quad (4.4)$$

The measured and derived DC characteristics of the CRF24010 based on TOM3 model is shown in Figure 4.3.

The extracted DC parameters of TOM3 model is listed in Table 3.

Table 3 Extracted DC parameters of TOM3 model.

Model Parameter	α (1/V)	β (A/V ²)	γ	λ (1/V)	Q	V _{st} (V)	M _{st} (1/V)	V _{th} (V)	k
Value	0.112	0.089	0.0352	0	1.19	1.86	0	-11.02	1.19

Figure 4.3 Measured and derived (optimized) I-V characteristics of CRF 24010 based on TOM3 model from $V_{gs} = -11$ V to -5 V, step 1 V; V_{ds} from 0 V to 60 V.

4.3.2 Curtice Nonlinear FET Model

Curtice nonlinear FET model is well-known of its cubic polynomial properties to derive the saturation current as a function of both V_{GS} and V_{DS} . Figure 4.4 shows the simplified equivalent circuit of this model. In this simplified model, intrinsic parameters such as gate to source capacitance C_{GS} , gate to drain capacitance C_{GD} , and gate-to source resistance R_{GS} are included. Gate-to-source diode I_{GS} and gate-to-drain diode I_{GD} are included to visualize the nonlinearity of gate-to-source junction and gate-to drain junction respectively.

This model includes additional gate-source R_{gs} , additional diode between drain and additional diode between drain and gate. The nonlinear polynomial equation to model the saturation current is derived in (4.5) and (4.6).

Figure 4.4 Curtice cubic equivalent model.

$$I_{ds} = (A_0 + A_1 V_1 + A_2 V_1^2 + A_3 V_1^3) \tanh(\gamma V_{ds}) \quad (4.5)$$

where
$$V_1 = V_f (1 + \beta (V_{ds0} - V_{ds})) \quad (4.6)$$

The tanh function is applied to smoothen linear and saturation region, γ is the saturation parameter. β relates the pinch-off voltage dependence on the drain-source voltage. Coefficients A_0 , A_1 , and A_3 are polynomial curve coefficients. Figure 4.5 shows the comparison of simulated (by Microwave Office) and measured drain currents. It is observed that there is good agreement between simulated and measured drain currents. The extracted model parameters are shown in Table 4.

Table 4 Extracted DC parameters of Curtice Cubic model

Model Parameter	A_0 (A)	A_1 (A/V)	A_2 (A/V ²)	A_3 (A/V ³)	V _{do} (V)	γ (1/V)	β (1/V)	V _t (V)
Value	2.024	0.161	-0.00905	-0.00072	15.27	0.093	0.001355	-12

Figure 4.5 Measured and derived (optimized) I-V characteristics of CRF 24010 based on Curtice Cubic model from $V_{gs} = -11V$ to $-5V$, step $1V$; V_{ds} from $0V$ to $60V$.

4.3.3 Modified Materka FET Model

The modified materka FET (Rizzoli) model derives the drain-current relationship as shown.

$$I_{ds} = (I_{dss} + S_s V_{ds}) \left(1 - \frac{V_{gs}}{V_{th} + \gamma V_{ds}} \right)^{E + K_E V_{gs}} \tanh \left(\frac{S_L V_{ds}}{I_{dss} (1 - K_G V_{gs})} \right) \quad (4.7)$$

where V_{th} is the threshold voltage, I_{dss} is drain saturation current at zero V_{gs} , γ the drain voltage dependence of the threshold voltage, K_G is the drain V_{gs} dependence in linear region, and S_L the slope of drain I/V in linear region. Parameters E and K_E determine the quadratic behavior. E is the constant part of gate I/V exponent, and K_E is the dependence of power law on V_{gs} . S_s is the slope of drain I/V in saturation.

Figure 4.6 Modified Materka FET model equivalent circuit.

The equivalent circuit of this model is illustrated in Figure 4.6. This model includes intrinsic parameters, such as gate-to-drain capacitance C_{GD} , gate-to-source capacitance C_{GS} , and intrinsic input resistance R_i . Gate-to drain diode I_{GD} and gate-to-source diode I_{GS} are also included to model the nonlinearity of gate-drain junction and gate-source junction respectively. R_G , R_D and R_S are added as gate, drain and source extrinsic resistance respectively.

Figure 4.7 illustrates the comparison of model simulation and measurement drain-current. The DC extracted parameters of this model is listed in Table 5.

Table 5 Extracted DC parameters of modified Materka model

Model Parameter	I_{dss} (A)	V_{th} (V)	γ (1/V)	E (1/V)	K_E (1/V)	S_L	S_S	K_G (1/V)
Value	0.976	-13	0	0.26	-0.1353	0.5598	0.0078	0.602

Figure 4.7 Measured and derived (optimized) I-V characteristics of CRF 24010 based on Modified Materka model from $V_{gs} = -11\text{V}$ to -5V , step 1V ; V_{ds} from 0V to 60V .

4.4 Cripps Method

DC nonlinear characterization model is very useful for high power and high gain amplifier design. It plays an important role for achieving optimum gain and optimizing power matching. Power matching is an important issue in the power amplifier design. Cripps method (optimum load-line method) is a straightforward but effective approach to achieving maximum output power and reasonable gain [25]. It is very effective for the MESFET power amplifier design. This simple yet effective optimum load line is useful to achieve maximum output power. The illustration of the Cripps method is shown in Figure 4.8. In this figure, maximum output power R_{opt} , and power delivered to the load P_{opt} are derived from DC I-V characteristics. These derivations are listed in equations (4.10) to (4.13).

Figure 4.8 Cripps load-line method

Assuming the DC-IV curve of a device is bounded by its maximum drain current $I_{\max}$, knee voltage V_{knee} and drain breakdown voltage V_{br} , and the device is biased in class A conditions that are mentioned in equations (4.8) and (4.9)

$$V_D = \frac{V_{\text{br}} - V_{\text{knee}}}{I_{\max} / 2} \quad (4.8)$$

$$I_D = \frac{I_{\max}}{2} \quad (4.9)$$

From equations (4.8) and (4.9) the optimum load for maximum output power would be

$$R_{\text{opt}} = \frac{V_D - V_{\text{knee}}}{I_{\max} / 2} \quad (4.10)$$

Under this condition, the device could achieve the maximum current and voltage swing at the same time, and the power delivered to the load would be

$$P_{\text{opt}} = \frac{1}{8} (V_{\text{br}} - V_{\text{knee}}) I_{\max} = \frac{1}{8} \frac{(V_{\text{br}} - V_{\text{knee}})^2}{R_{\text{opt}}} = \frac{1}{8} I_{\max}^2 R_{\text{opt}} \quad (4.11)$$

If $R_L > R_{opt}$, then the voltage boundary would be the limiting factor and the power delivered to the load is derived as

$$P_{RF} = \frac{1}{2} \frac{(V_{br} - V_{knee})^2}{R_L} = P_{opt} \frac{R_{opt}}{R_L} < P_{opt} \quad (4.12)$$

Similarly, for $R_L > R_{opt}$, with which the device is limited by the current boundary, the power delivered to the load given by

$$P_{RF} = \frac{1}{8} I_{max}^2 R_L = P_{opt} \frac{R_{opt}}{R_L} < P_{opt} \quad (4.13)$$

When the load is no longer pure resistance, the load line is no longer straight, instead, it becomes ellipse. The major axis of the ellipse lies along the load line for maximum RF output power and the ellipse is bounded by $0 < I_D < I_{max}$ and $V_{knee} < V_D < V_{br}$.

Chapter 5 Schematic Design, Simulation and Measurement

Designing a broadband power amplifier, with nearly constant gain over a defined frequency range is a matter of compensating the variation of forward gain $|S_{21}|$ with frequency. This can be accomplished either by negative feedback or selective mismatch of the input and output circuitry. The latter is chosen in this work. Schematic design, simulation and module measurement are elaborated in this chapter. This single-stage broadband power amplifier using the Cree SiC MESFET CRF24010 is designed based on the derived small-signal model and DC nonlinear characterization.

5.1 S Parameters Analysis

In this schematic design, the derived small-signal model is simulated from 100MHz to 4000MHz as shown.

Figure 5.1 (a) S_{21} and S_{12} SiC MESFET simulation performance. (b) S_{11} and S_{22} SiC MESFET simulation performance.

Figure 5.2 shows the S_{21} gain consideration of this device. The S-parameters of targeted frequencies, 600MHz, 1200MHz and 1800MHz, is observed and tabulated in Table 6.

Figure 5.2 S_{21} SiC MESFET Simulation Performance

Table 6 SiC MESFET Crf 24010 S-parameters at 600MHz, 1200 MHz, and 1800MHz.

Frequency (MHz)	S_{11} (Mag/Angle)	S_{21} (Mag/Angle)	S_{22} (Mag/Angle)
600	$0.859 \angle -106.375^0$	$5.654 \angle 113.216^0$	$0.411 \angle -118.050^0$
1200	$0.830 \angle -141.491^0$	$3.266 \angle 85.096^0$	$0.469 \angle -142.221^0$
1800	$0.830 \angle -157.231^0$	$2.246 \angle 66.896^0$	$0.507 \angle -151.224^0$

The targeted power gain is 10 dB from 600 MHz to 1800 MHz. From the provided S-parameters, $|S_{21}|^2$ is calculated as:

- $|S_{21}|^2 = 15.05$ dB at 600 MHz
- $|S_{21}|^2 = 10.28$ dB at 1200 MHz
- $|S_{21}|^2 = 7.03$ dB at 1800 MHz

In order to compensate the $|S_{21}|$ variations, the matching network must decrease the gain by 5 dB at 600MHz and increase the gain by 3dB at 1800MHz. For this SiC

MESFET, $G_{s,\max}$ and $G_{L,\max}$ are calculated to investigate the possibilities of design realization. G_s and G_L formulae are presented below.

$$G_s = \frac{1}{|1 - S_{11}\Gamma_s|^2} \quad (5.1)$$

$$G_L = \frac{1 - |\Gamma_L|^2}{|1 - S_{22}\Gamma_L|^2} \quad (5.2)$$

Assume $\Gamma_s = S_{11}$ in (5.1) and $\Gamma_L = S_{22}$ in (5.2) gives

$$G_{s,\max} = \frac{1}{1 - |S_{11}|^2} \quad (5.3)$$

$$G_{L,\max} = \frac{1}{1 - |S_{22}|^2} \quad (5.4)$$

The $G_{s,\max}$ and $G_{L,\max}$ of SiC MESFET transistor are tabulated in Table 7.

Table 7 $G_{s,\max}$ and $G_{L,\max}$ calculation.

Frequency (MHz)	$G_{s,\max}$ (dB)	$G_{L,\max}$ (dB)
600	5.73	0.8036
1200	5.07	1.0788
1800	5.07	1.29

Based on the calculations above, it is observed that increasing gain of 3dB at 1800MHz is possible. Since $G_{s,\max}$ is more than 5dB, input matching has more significant role in increasing gain. However, since input matching causes stability and gain trade-off, therefore output matching networks also play significant role in increasing gain at 1800MHz.

5.2 Stability Consideration

Stability is a crucial issue when designing PAs because of the presence of a combination of capacitive shunt and series feedback, which will include both a resistive and an inductive part that can lead to instability. The power amplifier must be stable under all operating frequencies and possible terminations. From the simulated S parameters, the stability performance is shown.

Figure 5.3 Stability of SiC MESFET crf24010.

It is observed that the SiC MESFET does not fulfill the necessary and sufficient conditions for unconditionally stability. It is potentially unstable as $K < 1$, $MU_1 < 1$, $MU_2 < 1$. Therefore, stabilization circuit is required. In this project, resistive loading transistor

is chosen. However, tuning and optimization matching networks are necessary, due to its gain and bandwidth trade-off. Figure 5.4 shows four types of resistive loading to improve stability.

Usually, stabilizing one port of a transistor results in an unconditionally stable device. All four choices of resistive loading affect the gain of the amplifier. It is possible to cause deterioration in the noise performance of the amplifier as well. However, in some potentially unstable design of broadband amplifiers, it might produce a trade-off between gain and stability that is quite acceptable, resulting in a stable two-port with reasonable gain over a wide bandwidth. In a broadband amplifier design using a potentially unstable transistor, a common procedure is to use resistive loading to stabilize the transistor and negative feedback to provide the proper AC performance, by providing constant gain and low input and output VSWR.

Figure 5.4 Four types of resistive loading to improve stability.

In this design, configuration (a) is chosen. The gate resistance is placed as close as possible to the device gate for better protection against ESDs and oscillations. The impedance of this circuit in parallel to the input matching circuit is infinite at the fundamental frequency (assuming the circuit losses are low). The value of R_g is determined between minimum and maximum value conditions that are

▪ R_g Minimum Value Conditions

1. For low frequency stability the gate resistor should be connected as close as possible to the gate. For these frequencies, the DC blocking capacitor is an open circuit, the decoupling capacitors are short circuits and the quarter-wavelength line is a very short electrical length. If negative resistance ($R < 0$) appears in the gate and the sum of the resistances is positive ($R + R_g > 0$), the device will be stable. It requires R_g to have sufficient value and the connection to the ground to be short for low frequencies. Connecting R_g close to the gate reduces the connection length to the ground.
2. The gate current limitation under breakdown, positive voltage, large drive and ESDs requires a sufficient R_g values but the value has to be limited under maximum value conditions.

▪ R_g Maximum Value Conditions

1. The gate voltage V_{gs} should be maintained constant versus the drive level.

The maximum of R_g has to be limited to

$$R_{gMax} = -\Delta V_{gs} / \Delta I_{gs} Max, \Delta V_{gs} < 0 \quad (5.5)$$

Figure 5.5 shows the stabilization circuit with gate resistance. The simulation result of this schematic is shown in Figure 5.6.

Figure 5.5 Stabilization circuit with gate resistance.

Figure 5.6 Stabilization circuit simulation.

It is observed that the stability has improved, as $K > 1$ and $B_1 > 0$. Hence, with the stabilization circuit, the potentially unstable transistor is optimized to be unconditionally stable.

5.3 Design of Matching Networks

The objective of the impedance matching circuitry is to transform the source and load impedances as close to the system characteristic impedance of 50Ω as possible. Unfortunately, only approximation can be done at best, due to dispersive source and load

impedances at wide bandwidth. The matching networks consist of series microstrip transmission lines and ceramic multi-layer capacitors. Proper matching networks are required in order to have the required gain and bandwidth. In addition, broadband amplifier design requires bandwidth extension methods. Selective mismatch configuration of input and output circuitry is probably required. Generally, broadband design involves canceling the poles nearest to the $j\omega$ axis, and changing the positions of the remaining poles to realize the desired transfer characteristic (filter characteristics such as Butterworth or Chebyshev). Matching networks can be either lossless (consist only of L and C elements) or lossy (include R elements with the L and C elements) [27].

5.3.1 Input Matching Networks

The proper impedance for input matching network is determined for the high gain and broad frequency with respectable gain flatness. The best impedance is determined through microwave office optimization. Figure 5.7 shows the circuit configuration for this simulation.

Figure 5.7 Schematic of input matching impedance network.

Port 1 impedance is tuned and optimized to obtain the best gain and gain flatness performance. Figure 5.8 shows the S_{21} simulation performance with the input termination

$0.1947\angle -115.3^\circ$ from 100 MHz to 4000 MHz. The input matching network is designed to have S_{22} impedance as nearest to $0.1947\angle -115.3^\circ$

Figure 5.8 Small-signal gain performance of input port impedance $G_M=0.1947$; $G_A=-115.3^\circ$ at 1225MHz.

From Figure 5.9 S_{22} of the designed input matching network at 1.225 GHz is $0.1709\angle -112^\circ$, which is near to $0.1947\angle -115.3^\circ$. Final tuning and optimization are necessary.

Figure 5.9 S_{22} performance of input matching network.

5.3.2 Output Matching Network

By applying the same method as input matching network, proper output matching networks are determined in the same manner.

Figure 5.10 Schematic of output matching impedance.

Port 2 impedance is tuned to get the best gain and gain flatness performance. The small-signal gain S_{21} of the output matching network when port 2 is terminated with $0.3764\angle 156.5^\circ$ at 1225 MHz is shown in Figure 5.11.

Figure 5.11 Small-signal gain performance of output matching impedance $0.3764\angle 156.5^\circ$ at 1.225GHz.

Figure 5.12 S_{22} performance of output matching network.

The output matching network is designed to get S_{22} impedance as nearest to $0.3764\angle 156.5^\circ$ as shown in Figure 5.12.

5.4 Design of DC Bias Network

The objective of the bias network is to deliver DC power to the device at desirable biasing conditions. However, in general DC biasing networks are designed in such a way that their interaction over the frequency band of interest is as minimum as possible. The DC nonlinear characteristic of the device is an important factor that influences the design of DC bias network. It is imperative to ensure the DC stability performance on power amplifier operation. Excessive current driven and thermal runaway must be avoided during operations, as it may cause devices to burnt the modules. At largely thermal dependency, thermal resistors (thermistors) are needed to stabilize the device performance over wide temperature range.

DC bias networks consist of gate biasing circuit and drain biasing circuit. The gate biasing circuit has several functions :

- To maintain a constant gate-to-source voltage V_{gs} .
- To supply a negative and positive gate current I_{gs} .
- To protect the gate by limiting I_{gs} when the device goes into breakdown (drain-to-gate or gate-to-source) or when the gate-to-source junction is biased with a positive voltage. An operator error, an overdrive, or ESDs can cause these abnormal operating conditions for the devices.
- To stabilize the device in case a negative resistance appears in the gate at any frequency where the device has a positive gain.
- To filter the out of band signal, the intermodulation products and harmonics generated by the device without affecting the device input matching circuit.
- To isolate the gate from any signal coming from the drain through the bias circuits.

Drain bias circuit plays significant role in power amplifier design. It determines the internal performance and behavior of active devices that contribute to the major specifications, such as power capability, nonlinearity and noise performance. Generally, drain bias circuit has several functions :

- To maintain a constant drain-to-source voltage V_{DS} .
- To supply a drain current at least up to I_{ds} maximum under operation.
- To stabilize the device at frequencies outside its operating range.
- To filter out of band signal, the intermodulation products and harmonics generated by the device.

It should be noted that as for the input biasing circuit, the output biasing circuit also could be used as matching element.

It has been said that the least considered factor in microwave transistor amplifier design is the bias network. Although most considerable efforts are spent in designing for a desirable gain and bandwidth, some efforts are still needed in designing the DC bias network. The purpose of a good DC bias design is to select the proper quiescent point and hold the quiescent point constant over variations in transistor parameters and temperature. A resistor bias network can be used with good results over moderate temperature changes. To accommodate transistor characteristics changes due to temperature variations, thermal resistors (thermistors) are usually used.

In this design, the power amplifier is determined to be Class A. From the DC nonlinear characterization model, the maximum output power is determined from the I-V load line. The DC bias networks are designed to select the quiescent point at $V_{DS} = 48V$; $I_{DQ} = 500mA$. The expected output power is 35dBm – 40dBm, with PAE < 50%.

5.5 Schematic Design of Single-stage Power Amplifier

The design of single-ended power amplifier is done by combining input matching, output matching, DC bias network and device schematic that is shown in Figure 5.13.

Figure 5.13 Schematic of single-ended power amplifier in subcircuit level.

The detailed schematic is given in Appendix 5. Figures 5.14 to 5.17 show the simulation results of this schematic design. Figure 5.14 shows the stability performance of the module. The gain performance of this schematic design is shown in Figure 5.15. Where, Figure 5.16 and Figure 5.17 shows input and output return losses in log and smith chart forms, respectively.

Figure 5.14 Stability factor.

Figure 5.15 Simulated S_{21} performance of single-ended SiC power amplifier.

Figure 5.16 Simulated input and output return loss.

Figure 5.17 S_{11} and S_{22} performances.

Based on the above simulation results, the following characteristics are observed:

1. This amplifier is unconditionally stable from 500MHz to 4 GHz as $K > 1$ over the frequency band.

2. The small-signal gain is more than 9dB at center frequency 1225MHz for operating frequency from 650MHz to 1800MHz.
3. Output return loss at center frequency is typically -12 dB which is in acceptable range.
4. Input return loss is typically -4dB. This mismatch at the input matching networks is required at this broadband amplifier design, in order to compensate the changes of $|S_{21}|$ with frequency.

5.6 PCB Fabrication

To enable PCB fabrication, layout design in GerberX format is necessary. Exporting schematic layout to GerberX format is done by ADS 2003. The layout is shown as follows:

Figure 5.18 Fabricated PCB layout.

This conversion was done by exporting the layout to RS-274X format by ADS 2003. This GerberX file is exported through Circuit CAM and Board Master.

5.7 Experimental Results

Experimental test is conducted to check the biasing and small-signal performances using Vector Network Analyze Agilent HP 8719D. Operating point is selected at $V_{GS} = -7V$, $V_{ds} = 48V$, and $I_{ds} = 0.5A$. The test setup is shown in Figure 5.19.

Figure 5.19 Measuring setup for small-signal test.

The device under test (power amplifier) with soldered SiC MESFET and connectors are shown in Figure 5.20.

Figure 5.20 SiC MESFET power amplifier (DUT) with soldered connectors.

Figure 5.21 and Figure 5.22 present the small-signal S-parameters measurement versus simulation results of the DUT.

Figure 5.21 Experimental and simulation gain S_{21} .

Figure 5.22 S_{11} and S_{22} measurement and experimental result

5.8 Single Tone Measurement

Single tone measurement is performed to showcase the nonlinearity performance caused by large-signal condition. Power measurement setup is illustrated in Figure 5.23. Attenuator is used at the output of the device under test (DUT) since the output power

exceeds power sensor handling capability. Calibration process is done before power measurement. This process will offset cable and power sensor losses and attenuator values.

Figure 5.23 Power measurement setup

Figure 5.24 shows power performance results at $f=1.225\text{GHz}$, $V_{DS}=48\text{V}$ and $I_D=500\text{mA}$.

Figure 5.24 Single-tone power performance

5.9 Observations and Discussions

Based on experimental results, the following observations are seen.

1. The gain is more than 8 dB from 850MHz to 1850MHz. However, the gain tends to get lower at 600-700MHz.
2. The input return loss is rather high. This high return loss due to input matching network mismatch. This compensated matching network is required to compensate the $|S_{21}|$ variation with frequency.
3. The single tone power measurement shows good linearity at $f=1.225\text{GHz}$, $V_{DS}=48\text{V}$, $I_D=500\text{mA}$. It is observed that minimum output power of 35dBm and minimum linear gain of 8dB have been obtained.

Compared to simulation results, the following issues are observed:

1. The small-signal gain of the experiment result from 850 MHz to 1850 MHz is close to the simulation result.
2. The experimental result output return loss (S22) shows similar performance and directions compared to simulation result.
3. The experimental result of input return loss (S11) shows difference performance compared to simulation result, due to final module tuning as the input compensated matching network required to widen the covered bandwidth.
4. Experimental result of small-signal gain shows discrepancy at 600-700MHz compared to simulation result.

The difference performance between simulation results and experimental results are caused by the following issues:

1. The small-signal parameters that are provided by the manufacturer considered to be linear, therefore non-linear parameters that affect the performance are not included in simulation.
2. The grounding of fabricated PCB needs to be improved.
3. The heat-dissipation design of heat sink needs to be careful considered under high-voltage performance, since temperature of device rises very fast. This causes performance deterioration.

Chapter 6 Conclusions and Future Work

6.1 Conclusions

A single-ended broadband power amplifier has been developed using SiC MESFET device. The operation frequency is 650MHz-1800MHz, with a center frequency of 1225 MHz, covering bandwidth of more than 90%. The gain is more than 9dB at 1225MHz.

In this thesis, a detailed analysis of the SiC MESFET broadband single-ended power amplifier design architecture has been presented. SiC MESFET is well known for its low dielectric constant resulting in lower capacitive loading and higher impedance compared to conventional semiconductors. This enables broadband single-ended power amplifier. Due to the wide bandgap property of the device, it can be biased under high voltage condition and low current conditions.

An accurate small-signal model development of SiC MESFET has been accomplished. Pinch-off mode simplified model has been applied for parasitic or extrinsic pad capacitances derivations. Parasitic resistances and inductances have been derived through cold FET measurements under forward bias conditions. The intrinsic parameters have been optimized by using Microwave Office. This small-signal model has been verified in power amplifier design, by replacing the provided block S-parameters in the same schematic. It is shown to be in a good agreement with the one provided block by Cree.

SiC MESFET large signal table-based models have been developed by using available models in Microwave Office simulators. TOM3, Curtice Cubic, and Modified Materka (Rizzoli) models have been optimized to fit I-V curve nonlinearity of SiC MESFET. The models have been verified by comparing measured I-V curve with models

based simulated results of V_{GS} from -11V to -5V, and V_{DS} from 0V to 60V. It is observed that the simulated results of three models show good agreements with measured I-V performance.

The design considerations cover stability, gain and bandwidth issues. Stability has been elaborated since SiC MESFET is potentially unstable. Stabilization circuit has been designed to ensure the unconditionally stability conditions. The proper impedance for input matching network and output matching network has been designed for the high gain and broad frequency with respectable gain flatness. The best impedance has been determined through MWO2002 optimization. By simulation, the best gain and bandwidth have been obtained with $\Gamma_{IN} = 0.1947 \angle -115.3^\circ$ and $\Gamma_{OUT} = 0.3764 \angle 156.5^\circ$ at 1225 MHz. Input and output matching networks have been designed to be near to the best port impedances.

Although considerable effort has been spent in designing for a desirable gain and bandwidth, some effort has also been focused in designing the DC bias network. The purpose of a good dc bias design is to select the proper quiescent point and hold the quiescent point constant over variations in transistor parameters and temperature. In this power amplifier design, the simple dc bias network is preferred. The DC bias networks have been designed to select the quiescent point at $V_{DS} = 48V$ and $I_{DQ} = 500mA$.

Experimental result has shown that the gain is more than 8 dB from 850MHz to 1850MHz. Observation has shown that there is similarity gain performance between simulation and experimental results for the frequency range from 850MHz to 1850MHz. Large signal measurement shows that power gain of 8dB and output power of minimum 35 dBm are achieved at 1225 MHz.

From the presented work, it concludes that SiC MESFET technology is very promising for broadband power amplifier application.

6.2 Future Work

The single-ended broadband power amplifier using SiC MESFET has been designed, simulated and fabricated. Small-signal performance measurement has been carried out. The future work should be conducted on designing other configurations, such as multi-stages amplifier, balanced amplifier or Doherty amplifier, in order to improve the linearity and power handling capability. Multi-stages amplifier will give more opportunities for obtaining higher gain as well as wider bandwidth, and also will give some room for power matching in handling high output power.

Balanced amplifier configuration will have the following advantages:

1. Low input and output VSWR since balanced amplifier input and output VSWR is dependent on the coupler. Therefore, the individual amplifiers can be designed for flat gain, and low noise figure (even if the VSWR of individual amplifier is high).
2. There is a high degree of stability.
3. The output power is twice that obtained from the single amplifier.
4. If one of the amplifiers fails, the balanced amplifier unit will still operate with reduced gain.
5. Balanced amplifiers are easy to cascade with other units, since each unit is isolated by the coupler.

However the unit uses two amplifiers that consume more dc power, and is larger in size. Also, in practice there is a finite insertion loss associated with the amplifiers. Doherty

amplifier will improve the amplifier linearity performance, by combining two power amplifiers of equal capacity through lines of a quarter wavelength lines of networks.

Further work on large-signal SiC MESFET modeling to derive and predict nonlinear performance is possible to be carried out in the future. This model will give much closer results between simulation and experimental results, hence will save time and cost in tuning and optimizing of power amplifier design in the future. The model will represent nonlinear performance of different biasing, load-pull measurement under different power levels, especially under large signal condition. By obtaining the nonlinear model of SiC MESFET, power amplifier design for different frequency bands is possible to be done efficiently and accurately.

The load-pull method is important to improve power matching. This load-pull design method is similar to a small-signal amplifier. However, the load-pull method is carried out under the large-signal condition. There is an important issue to be considered that the small-signal extrinsic and intrinsic model parameters are only valid under small-signal conditions. In reality, the measured results will be significantly different from the actual characteristics. This phenomenon is caused due to the high mismatch of power transistors (without any matching networks) under large-signal conditions. Under large signal conditions, the output impedance tends to get lower and it causes output mismatch for maximum output power. Therefore, it is an important point to develop large-signal model to have better design accuracy.

Nonlinearity power performances are also to be carried out in the future. These measurements will determine the output power linearity, such as 1-dB compression point, single-tone harmonics, and dual-tone intermodulation performance, such as IP3.

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Appendix 1 Stability Conditions

Stability conditions are derived from reflection coefficient equations, which are defined in the following equations.

$$\Gamma_{IN} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (\text{A1.1})$$

$$\Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \quad (\text{A1.2})$$

The conditions for a two-port network to be unconditionally stable are given as

$$|\Gamma_S| < 1 \quad (\text{A1.3})$$

$$|\Gamma_L| < 1 \quad (\text{A1.4})$$

$$|\Gamma_{IN}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \quad (\text{A1.5})$$

$$|\Gamma_{OUT}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \quad (\text{A1.6})$$

Equations (A1.4) and (A1.5) define that for all passive load impedances, the real part of the input impedance must be positive while (A1.3) and (A1.6) define that for all passive source impedances, the real part of the output impedance must be positive.

The necessary and sufficient conditions for a two-port network to be unconditionally stable are derived through lengthy manipulations of (A1.3), (A1.4), (A1.5) and (A1.6).

The final results are

$$K > 1 \quad (\text{A1.7})$$

$$|\Delta| < 1 \quad (\text{A1.8})$$

$$1 - |S_{11}|^2 > |S_{12}S_{21}| \quad (\text{A1.9})$$

$$1 - |S_{22}|^2 > |S_{12}S_{21}| \quad (\text{A1.10})$$

where

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (\text{A1.11})$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \quad (\text{A1.12})$$

Another familiar way that defined the necessary and sufficient conditions for unconditionally stability is

$$K > 1$$

and

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0 \quad (\text{A1.13})$$

Most commercial simulators also include other stability conditions :

$$MU_1 = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \Delta| + |S_{12}S_{21}|} > 1 \quad (\text{A1.14})$$

and

$$MU_2 = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^* \Delta| + |S_{12}S_{21}|} > 1 \quad (\text{A1.15})$$

Appendix 2 Power Gain Equations

Several power gain equations appear in the literature and are used in the design of microwave amplifiers. The commonly used power gain equations are transducer power gain G_T , the power gain G_P (also known as the operating power gain), and the available power gain G_A . G_T is defined as the ratio of power delivered to the load (P_L) to power available from the source (P_{AVS}). G_P is defined as the ratio of power delivered to the load (P_L) to the power input to the network (P_{IN}), and G_A is defined as the ratio of power available from the network (P_{AVN}) to the power available from the source (P_{AVS}).

The expressions for G_T , G_P and G_A are simplified as follow:

$$G_T = \frac{1 - |\Gamma_S|^2}{|1 - \Gamma_{IN} \Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22} \Gamma_L|^2} \quad (\text{A2. 1})$$

$$G_T = \frac{1 - |\Gamma_S|^2}{|1 - S_{11} \Gamma_S|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_{OUT} \Gamma_L|^2} \quad (\text{A2. 2})$$

$$G_P = \frac{1}{|1 - \Gamma_{IN}|^2} |S_{21}|^2 \frac{1 - |\Gamma_L|^2}{|1 - S_{22} \Gamma_L|^2} \quad (\text{A2. 3})$$

$$G_A = \frac{1 - |\Gamma_S|^2}{|1 - S_{11} \Gamma_S|^2} |S_{21}|^2 \frac{1}{|1 - \Gamma_{OUT}|^2} \quad (\text{A2. 4})$$

where Γ_{IN} and Γ_{OUT} are defined in (A1.1) and (A1.2), respectively.

For two-port network, the maximum gain is defined as

$$G = |S_{21}|^2 \frac{(1 - |\Gamma_{SM}|^2)(1 - |\Gamma_{LM}|^2)}{|(1 - \Gamma_{SM} S_{11})(1 - \Gamma_{LM} S_{22}) - \Gamma_{SM} \Gamma_{LM} S_{21} S_{12}|^2} \quad (\text{A2. 5})$$

where Γ_{SM} and Γ_{LM} are source and load conjugate matching respectively.

At this point, an important assumption can be made to simplify the calculations. The network is assumed to be unilateral ($S_{12}=0$). The value of this assumption can be assessed by unilateral figure of merit.

$$U = \frac{|S_{11}| |S_{22}| |S_{21}| |S_{12}|}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)} \quad (\text{A2. 6})$$

The following formula defines the boundaries of the error introduced by the simplified calculation between the transducer power gain G and the unilateral transducer power gain G_u .

$$\frac{1}{(1+U)^2} < \frac{G}{G_u} < \frac{1}{(1-U)^2} \quad (\text{A2. 7})$$

If the error is considered small enough to justify the unilateral assumption, then the unilateral transducer power gain is defined as.

$$G_u = |S_{21}|^2 \frac{(1 - |\Gamma_{SM}|^2)(1 - |\Gamma_{LM}|^2)}{|1 - \Gamma_{SM} S_{11}|^2 |1 - \Gamma_{LM} S_{22}|^2} \quad (\text{A2. 8})$$

In this case, the gain only depends on the S parameters of the device and the matching to input and output. G_u will be maximized if $\Gamma_S = S_{11}^*$ and $\Gamma_L = S_{22}^*$, so that maximum gain from device is

$$G_{u,MAX} = |S_{21}|^2 \frac{1}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)} \quad (\text{A2. 9})$$

This formula shows that the maximum unilateral gain of an amplifier is determined solely by the S-parameters of the device chosen, regardless of the source and load impedance. However, in reality S_{12} is not perfectly zero, so that the input match depends

on the load impedance and vice versa. When the device is simultaneously conjugately matched, the maximum transducer (available) gain is defined as

$$G_{MAX} = \left| \frac{S_{21}}{S_{12}} \right| \left(K \pm \sqrt{K^2 - 1} \right) \quad (\text{A2. 10})$$

Appendix 3 Typical Packaged S-Parameters of Cree crf 24010 (Small

Signal, VDS = 48V, IDQ = 500mA, angle in degree)

Freq	S(1,1)	S(2,1)	S(1,2)	S(2,2)
100.0MHz	0.933 / -24.697	9.470 / 164.826	0.022 / 72.184	0.281 / -34.171
200.0MHz	0.917 / -47.336	8.814 / 150.896	0.041 / 60.244	0.311 / -62.220
300.0MHz	0.898 / -66.755	7.970 / 138.866	0.055 / 49.176	0.344 / -83.098
400.0MHz	0.881 / -82.780	7.113 / 128.773	0.066 / 39.787	0.372 / -98.337
500.0MHz	0.867 / -95.802	6.332 / 120.339	0.073 / 31.953	0.394 / -109.583
600.0MHz	0.856 / -106.375	5.654 / 113.216	0.078 / 25.378	0.411 / -118.050
700.0MHz	0.847 / -115.027	5.079 / 107.100	0.082 / 19.781	0.425 / -124.563
800.0MHz	0.841 / -122.187	4.592 / 101.752	0.084 / 14.932	0.436 / -129.678
900.0MHz	0.837 / -128.190	4.179 / 96.993	0.086 / 10.659	0.445 / -133.774
1.000GHz	0.834 / -133.288	3.828 / 92.691	0.088 / 6.834	0.454 / -137.115
1.100GHz	0.831 / -137.674	3.526 / 88.750	0.089 / 3.362	0.462 / -139.886
1.200GHz	0.830 / -141.491	3.266 / 85.096	0.090 / 0.172	0.469 / -142.221
1.300GHz	0.829 / -144.852	3.039 / 81.675	0.090 / -2.790	0.475 / -144.221
1.400GHz	0.829 / -147.841	2.840 / 78.445	0.091 / -5.564	0.482 / -145.960
1.500GHz	0.828 / -150.526	2.665 / 75.375	0.091 / -8.183	0.488 / -147.492
1.600GHz	0.829 / -152.959	2.509 / 72.440	0.091 / -10.671	0.495 / -148.863
1.700GHz	0.829 / -155.183	2.370 / 69.618	0.091 / -13.047	0.501 / -150.104
1.800GHz	0.830 / -157.231	2.246 / 66.896	0.091 / -15.328	0.507 / -151.244
1.900GHz	0.830 / -159.132	2.133 / 64.258	0.091 / -17.526	0.513 / -152.301
2.000GHz	0.831 / -160.907	2.032 / 61.696	0.091 / -19.652	0.519 / -153.294
2.100GHz	0.832 / -162.576	1.940 / 59.200	0.091 / -21.714	0.525 / -154.235
2.200GHz	0.833 / -164.155	1.855 / 56.763	0.091 / -23.720	0.530 / -155.136
2.300GHz	0.834 / -165.657	1.778 / 54.379	0.091 / -25.676	0.536 / -156.004
2.400GHz	0.836 / -167.092	1.708 / 52.042	0.091 / -27.587	0.542 / -156.847
2.500GHz	0.837 / -168.471	1.643 / 49.748	0.091 / -29.458	0.547 / -157.670
2.600GHz	0.838 / -169.802	1.583 / 47.492	0.091 / -31.294	0.552 / -158.479
2.700GHz	0.839 / -171.093	1.528 / 45.273	0.091 / -33.096	0.558 / -159.277
2.800GHz	0.840 / -172.348	1.477 / 43.085	0.091 / -34.870	0.563 / -160.067
2.900GHz	0.842 / -173.575	1.430 / 40.926	0.091 / -36.616	0.568 / -160.852
3.000GHz	0.843 / -174.777	1.386 / 38.795	0.091 / -38.340	0.572 / -161.634
3.100GHz	0.844 / -175.960	1.346 / 36.687	0.091 / -40.041	0.577 / -162.415
3.200GHz	0.845 / -177.126	1.308 / 34.602	0.091 / -41.724	0.581 / -163.197
3.300GHz	0.846 / -178.281	1.273 / 32.537	0.091 / -43.390	0.586 / -163.981
3.400GHz	0.848 / -179.426	1.240 / 30.490	0.091 / -45.041	0.590 / -164.768
3.500GHz	0.849 / 179.435	1.210 / 28.459	0.091 / -46.679	0.594 / -165.559
3.600GHz	0.850 / 178.299	1.181 / 26.443	0.091 / -48.306	0.597 / -166.355
3.700GHz	0.851 / 177.164	1.155 / 24.440	0.091 / -49.924	0.601 / -167.157
3.800GHz	0.852 / 176.027	1.130 / 22.447	0.091 / -51.534	0.604 / -167.966
3.900GHz	0.853 / 174.886	1.107 / 20.464	0.091 / -53.138	0.607 / -168.783
4.000GHz	0.853 / 173.738	1.086 / 18.489	0.091 / -54.738	0.610 / -169.607

Appendix 4 Derivation of Intrinsic Small-Signal Model

The intrinsic small-signal model of MESFET devices is shown in Figure 5.3, which consists of elements C_{GS} , R_{GS} , C_{GD} , R_{GD} , g_m , τ , R_{DS} and C_{DS} . This appendix shows the derivation of the Y-parameters of this model described by (4.11) to (4.14). It also explains how the intrinsic parameters can be derived in the equations (4.16) to (4.23).

A4.1 Derivation of Intrinsic Y-Parameters:

Figure A4.1 shows the intrinsic model simplified from Figure 5.3. The figure illustrates the intrinsic circuit as 2-port network.

Figure A4. 1 Intrinsic Model of MESFET Devices

The terminal voltage relations of this 2-port network can be expressed in terms of the Y-parameters.

$$I_1 = y_{11}V_1 + y_{12}V_2 \quad (\text{A4. 1})$$

$$I_2 = y_{21}V_1 + y_{22}V_2 \quad (\text{A4. 2})$$

The Y-parameters of (A4.1) and (A4.2) can be derived for the circuit in Figure A4.1 as:

$$y_{11} = \left. \frac{I_1}{V_1} \right|_{V_2=0} = \frac{1}{R_{GS} + \frac{1}{j\omega C_{GS}}} + \frac{1}{R_{GD} + \frac{1}{j\omega C_{GD}}} = \frac{j\omega C_{GS}}{1 + j\omega R_{GS} C_{GS}} + \frac{j\omega C_{GD}}{1 + j\omega R_{GD} C_{GD}} \quad (\text{A4. 3})$$

$$y_{21} = \left. \frac{I_2}{V_1} \right|_{V_2=0} = \frac{I_m - \frac{j\omega C_{GD}}{1 + j\omega R_{GD} C_{GD}} V_1}{V_1} = \frac{g_m e^{-j\omega\tau}}{1 + j\omega R_{GS} C_{GS}} - \frac{j\omega C_{GD}}{1 + j\omega R_{GD} C_{GD}} \quad (\text{A4. 4})$$

$$y_{12} = \left. \frac{I_1}{V_2} \right|_{V_1=0} = - \left(\frac{-I_1}{V_2} \right) = - \frac{j\omega C_{GD}}{1 + j\omega R_{GD} C_{GD}} \quad (\text{A4. 5})$$

$$y_{22} = \left. \frac{I_2}{V_2} \right|_{V_1=0} = g_{ds} + j\omega C_{DS} + \frac{j\omega C_{GD}}{1 + j\omega R_{GD} C_{GD}} \quad (\text{A4. 6})$$

By applying simple mathematical manipulations, all Y-parameters can be rewritten in the form of (4.16) to (4.23). For simplicity, the subscript 'int' is omitted.

A4.2 Intrinsic Parameters Derivations

(A4.3), (A4.4), (A4.5) and (A4.6) have eight equations into eight unknowns, which each equation broken into real and imaginary equations. Hence, the intrinsic parameters can be determined from those equations. The real and imaginary parts of all Y-parameters are determined after de-embedding them from the measured S-parameters. Since the real and imaginary parts of y_{11} , y_{12} , and y_{22} are needed in the following derivation, we can write them separately as

$$\text{Re}(y_{11}) = \frac{\omega^2 R_{GS} C_{GS}^2}{|D_1|^2} + \frac{\omega^2 R_{GD} C_{GD}^2}{|D_2|^2} \quad (\text{A4. 7})$$

$$\text{Im}(y_{11}) = \omega \left(\frac{C_{GS}}{|D_1|^2} + \frac{C_{GD}}{|D_2|^2} \right) \quad (\text{A4. 8})$$

$$\text{Re}(y_{12}) = -\frac{\omega^2 R_{GD} C_{GD}^2}{|D_2|^2} \quad (\text{A4. 9})$$

$$\text{Im}(y_{12}) = -\omega \frac{C_{GD}}{|D_2|^2} \quad (\text{A4. 10})$$

$$\text{Re}(y_{22}) = g_{DS} + \frac{\omega^2 R_{GD} C_{GD}^2}{|D_2|^2} \quad (\text{A4. 11})$$

$$\text{Im}(y_{22}) = \omega \left(C_{DS} + \frac{C_{GD}}{|D_2|^2} \right) \quad (\text{A4. 12})$$

where

$$D_1 = 1 + j\omega R_{GS} C_{GS} \quad (\text{A4. 13})$$

$$D_2 = 1 + j\omega R_{GD} C_{GD} \quad (\text{A4. 14})$$

Adding (A4.8) to (A4.10) leads to:

$$\text{Im}(y_{11}) + \text{Im}(y_{12}) = \frac{\omega C_{GS}}{|D_1|^2} \quad (\text{A4. 15})$$

Meanwhile, adding (A4.7) and (A4.9) summarizes to the following:

$$\text{Re}(y_{11}) + \text{Re}(y_{12}) = \frac{\omega^2 R_{GS} C_{GS}^2}{|D_1|^2} \quad (\text{A4. 16})$$

The term D_1 can be eliminated by dividing (A4.16) by (A4.15),

$$\frac{\text{Re}(y_{11}) + \text{Re}(y_{12})}{\text{Im}(y_{11}) + \text{Im}(y_{12})} = \omega R_{GS} C_{GS} \quad (\text{A4. 17})$$

For further simplicity, let us assumed the left hand side of equation (A4.17) is equal to a variable d_1 . Hence, (A4.17) can be rewritten as

$$\omega R_{GS} C_{GS} = d_1 \quad (\text{A4. 18})$$

where

$$d_1 = \frac{\text{Re}(y_{11}) + \text{Re}(y_{12})}{\text{Im}(y_{11}) + \text{Im}(y_{12})} \quad (\text{A4. 19})$$

Hence, term D_1 can be rewritten in terms of d_1 as

$$D_1 = 1 + jd_1 \quad (\text{A4. 20})$$

C_{GS} can be evaluated by substituting (A4.20) into (A4.15),

$$C_{GS} = \frac{(1 + d_1^2)}{\omega} (\text{Im}(y_{11}) + \text{Im}(y_{12})) \quad (\text{A4. 21})$$

Meanwhile, R_{GS} can be determined by substituting C_{GS} into (A4. 18):

$$R_{GS} = \frac{d_1}{(1 + d_1^2)(\text{Im}(y_{11}) + \text{Im}(y_{12}))} \quad (\text{A4. 22})$$

C_{GD} and R_{GD} can be calculated in the similar manner. The term D_2 can be eliminated by dividing (A4.9) by (A4.10).

$$\frac{\text{Re}(y_{12})}{\text{Im}(y_{12})} = \omega R_{GD} C_{GD} \quad (\text{A4. 23})$$

For further simplicity, let us assumed the left hand side of equation (A4.23) is equal to a variable d_2 . Hence, (A4.23) can be rewritten as

$$d_2 = \omega R_{GD} C_{GD} \quad (\text{A4. 24})$$

where

$$d_2 = \frac{\text{Re}(y_{12})}{\text{Im}(y_{12})} \quad (\text{A4. 25})$$

Therefore, term D_2 can be expressed in terms of d_2 as

$$D_2 = 1 + jd_2 \quad (\text{A4. 26})$$

C_{GD} can be estimated by substituting D_2 into (A4.10)

$$C_{GD} = -\frac{\text{Im}(y_{12})}{\omega} (1 + d_2^2) \quad (\text{A4. 27})$$

Meanwhile, R_{GS} can be determined by substituting C_{GD} into (A4. 24)

$$R_{GD} = -\frac{d_2}{(1 + d_2^2)\text{Im}(y_{12})} \quad (\text{A4. 28})$$

The complex transconductance is defined as $G = g_m e^{-j\omega\tau}$, which can be evaluated from the complex parameters y_{12} and y_{21} . The second term of y_{21} in (A4.4) can be eliminated by subtracting (A4.5) from (A4.4).

$$y_{21} - y_{12} = \frac{G}{1 + jd_1} \quad (\text{A4. 29})$$

(A4.29) can be re-arranged to extract G , as follow:

$$G = (y_{21} - y_{12})(1 + jd_1) \quad (\text{A4. 30})$$

The magnitude and phase of G represents g_m and $(-\omega\tau)$, respectively:

$$g_m = |G| = |(y_{21} - y_{12})(1 + d_1^2)| \quad (\text{A4. 31})$$

$$\tau = -\frac{1}{\omega} \angle(G) \quad (\text{A4. 32})$$

The last two parameters g_{DS} and C_{DS} can be estimated using (A4.9) through (A4.12). g_{DS} can be estimated by adding (A4.9) to (A4.11), while C_{DS} can be calculated by adding (A4.10) to (A4.12).

$$g_{DS} = \text{Re}(y_{22}) + \text{Re}(y_{12}) \quad (\text{A4. 33})$$

$$C_{DS} = \frac{\text{Im}(y_{22}) + \text{Im}(y_{12})}{\omega} \quad (\text{A4. 34})$$

In summary, (A4.21), (A4.22), (A4.27), (A4.28), (A4.31), (A4.32), (A4.33), and (A4.34) provide the solution set of the intrinsic parameters at single-frequency measurements.