Fabrication and characterization of AlGaAs/GaAs pseudomorphic high electron mobility transistors for power applications

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Fabrication and Characterization of AlGaAs/GaAs Pseudomorphic High Electron Mobility Transistors for Power Applications

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
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Summary

A robust process technology has been developed for AlGaAs/GaAs pseudomorphic high electron mobility transistors (PHEMTs) suitable for power applications at microwave frequencies. At the same time, in-depth studies have also been conducted to investigate issues affecting the device power performance and hot carrier reliability when operating at a high drain bias.

In recent years, benzocyclobutene (BCB) is increasingly being used as a surface passivation material for III-V PHEMTs. A main advantage of BCB is that it has a lower dielectric constant when compared to that of silicon nitride (SiN). A lower dielectric constant reduces parasitics at high frequencies leading to better performance. In this study, we have also evaluated BCB as an alternative passivation material in addition to the more conventional SiN. This research also aims to advance the understanding in the areas of surface trapping and hot carrier induced degradation in BCB-passivated devices which is currently lacking. These issues are known to affect the device output power and reliability. The findings are compared with the SiN-passivated PHEMTs.

The important contributions from this work are summarized as follows:

- (1) A GaAs-based PHEMT fabrication technology for power applications has been developed. It makes use of a combination of optical and electron beam lithography to develop double-recessed PHEMTs with a gate length of about 0.25 μm . The PHEMT epitaxial structure consists of a double-heterojunction with a δ -doping layer both above and below the channel to increase the channel charge density and

improve the quantum well carrier confinement at the same time. PHEMTs with a high gate-drain breakdown voltage and a high drain current have been demonstrated and characterized at dc and microwave frequency.

(2) PHEMTs are devices whose surface passivation plays an important role in their electrical properties. Other than providing protection from harsh environmental conditions, the passivation film also reduces the adverse effect of surface states which has a direct influence on the device output power. In this work, an experimental investigation into the drain current transient in PHEMTs passivated by low- k BCB has been conducted. It was found that BCB reduces the density of surface states after passivation. When compared to the SiN-passivated PHEMT, the BCB-passivated device demonstrated a larger magnitude of gate lag. This finding has provided us with important information as to the suitability of each kind of passivation film for specific application.

(3) Power PHEMTs are often biased at a high drain bias and as such, there is a large electric field in the device channel. A major reliability concern is device degradation due to the generation of hot electrons under impact ionization conditions. Hot carrier stress has been performed on BCB- and SiN-passivated devices at room temperature to investigate the device dc degradation under a high gate-drain electric field. It was found that the dominant degradation mechanism is different for the two technologies. In the case of the BCB-passivated device, the proposed dominant mechanism is the trapping of hot electrons in states within the BCB film and/or at the interface between the semiconductor and BCB at the gate-drain access region. For the SiN-passivated device, the dominant mechanism seemed to be due to the trapping of

holes in the AlGaAs layer underneath the gate and in the very thin oxide interface layer between the gate metal and AlGaAs semiconductor surface.

(4) The PHEMT device technology that was developed has also been extended to the fabrication of GaAs-based monolithic microwave integrated circuits (MMICs). In this work, a C-X-Ku broadband and Ku-band power amplifier MMIC has been designed, fabricated and measured. The circuit fabrication involves the integration of spiral inductors, metal-insulator-metal capacitors, and tantalum nitride thin film resistors into the device process technology. The circuits were CPW-based as it eliminates the need for via holes and substrate thinning. The design for both circuits was based on the small-signal equivalent circuit model and on-wafer load-pull measurement results of a 10x100 μm double-recessed PHEMT.

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Chapter 1

Introduction

1.1 Motivations

High electron mobility transistors (HEMTs) are the most important class of analog electronic devices for use today in the frequency range 10-100 GHz. This is due to their outstanding performance in both low-noise and power applications. As low-noise devices, HEMTs have no competitors with performance close to theirs. As power devices, the GaAs MESFETs and heterojunction bipolar transistors (HBTs) are potential rivals only in the lower portion of the frequency range. The well-established MESFETs can be used up to about 30 GHz but with a lower power gain. HBT technology is maturing fast and has the potential to be used in the 50 GHz range [1]. For example, HBTs based on the indium phosphide (InP) material system have demonstrated capable high speed performance beyond 50 GHz. However, they suffer from the disadvantages of a lower breakdown voltage and a relatively immature device and circuit processing technology when compared with their GaAs-based counterparts. The former limits its applications to low-power circuit designs while the latter requires a careful validation between the device speed performance benefit and its circuit processing reproducibility [2], [3]. Therefore, in the near future, HEMTs may still remain as the only viable solid-state power device in the high frequency regime.

A major driver for the development of a mature and manufacturable HEMT technology has been the need for ultimate performance in defense and military systems. In the 1970s and 1980s, military applications dominated microwave electronics where performance was (and still is) important. Improved performance figures such as a higher output power and efficiency from HEMTs translate directly into better and more powerful military equipments with increased range, sensitivity and accuracy for RADARs, communications and electronic warfare systems. The situation changed somewhat in the 1990s with considerable budget cuts in defense spending with changing global political arena. At the same time, a shift to applications in civil communications took place where the operating frequencies in this area range from a few hundreds of MHz to 100 GHz. The widespread use of mobile phones created the first real mass demand for microwave transistors including HEMTs. The other commercial applications in the higher frequency range include direct-to-satellite communication (20 GHz downlink, 30 GHz uplink) [4], LDMS (local multipoint communication services, 27.5 GHz – 29.5 GHz) [5], and millimeter-wave digital radio systems [6]. In addition, a number of automotive radar systems are being developed for use in GPS vehicle position location (1.8 GHz), collision avoidance (77 GHz), blind spot detection and traffic management [7]. The GPS system and collision avoidance systems are expected to generate a huge demand for microwave transistors. In general, demand for microwave transistors for use in civil applications is expected to grow quickly in the near future. Several market segments have not saturated yet, and it is certain that new applications will create even larger consumer markets. However, there is no guarantee that new and useful microwave products will find ready commercial acceptance. The WLAN (wireless local area network) operating at 2.4 GHz is one example. The reluctance of consumers to shift

from traditional inexpensive coaxial-based systems has prevented the anticipated large volume production of WLAN in the 1990s.

Of the different classes and material systems of microwave transistors, the GaAs-based pseudomorphic HEMTs (PHEMTs) are probably the most important by virtue of their versatility in both low-noise and power applications. The most significant contribution of PHEMTs is in microwave and millimetre-wave power applications. PHEMTs have demonstrated state-of-the-art millimetre-wave power performance, primarily as a result of their high transconductance, low gate leakage current, high breakdown voltage, excellent pinch-off characteristics, and low output conductance [8].

In recent years, HEMTs based on the wide bandgap semiconductors (WBS) such as silicon carbide (SiC) and III-nitrides (AlN, GaN, and AlGaIn) have matured rapidly and gained increasing importance as their power performance at higher frequencies continued to improve [9]. WBS FETs are particularly suited for high power microwave applications due to their high breakdown field, high electron peak and saturation velocities, and superior thermal conductivity of the SiC substrate when compared with GaAs [10]. GaN HEMTs have been shown to deliver power densities greater than 10 W/mm and this is at least ten times achievable in GaAs-based devices [11], [12]. Cree has reported a power density of 32 W/mm for a GaN HEMT on SiC operating at 4 GHz [13]. Figure 1.1 shows a comparison of the power densities between AlGaIn/GaN HEMTs grown on SiC and GaAs-based PHEMTs [14]. The high breakdown field and high current densities have enabled the power densities of GaN devices to be an order of magnitude larger than GaAs-based ones.

Fig. 1.1. Comparison of power densities of GaN HEMTs grown on SiC and GaAs-based PHEMTs.

With the tremendous progress made in the epitaxial material quality and device fabrication techniques, GaN-based HEMTs with very high speed performance have also been achieved. For example, Kumar and co-workers demonstrated the fabrication of AlGaIn/GaN HEMTs with a gate length of 0.12 μm that has a unity current gain cutoff frequency (f_T) and maximum frequency of oscillation (f_{max}) of 121 GHz and 162 GHz, respectively [15]. Other than their high power capability, device engineers are also becoming increasingly interested in the low-noise performance of GaN HEMTs. For example, GaN HEMTs are ideal candidates that offer better linearity and higher breakdown voltages in applications such as receiver low-noise amplifiers in defense and aerospace systems. This is due to their ability to handle

high-power rf signals in harsh environments. Figure 1.2 shows a comparison of the minimum noise figures of HEMTs based on the different material systems, including GaN HEMTs [14]. It could be seen that at low frequencies, the GaN HEMT noise figures are only slightly higher than that of GaAs and InP HEMTs.

Fig. 1.2. Comparison of minimum noise figures of HEMTs based on different material systems. The noise figures of GaN HEMTs are only slightly higher than that of GaAs and InP HEMTs at low frequencies.

A plot of the output power density for III-V and wide bandgap FETs is shown in Fig. 1.3 [10]. In general, it can be seen that III-V devices demonstrated a much lower power density when compared with WBS FETs. However, the former can operate at higher frequencies but this gap is slowly narrowing as GaN technology matures.

Fig. 1.3. Comparison of output power density of III-V and wide bandgap FETs.

Despite the potential of WBS FETs as excellent candidates for high power and high frequency applications, there still remain issues that need to be evaluated carefully before their use becomes widespread. Its relatively immature technology compared to GaAs might suggest that long term material, device and circuit reliability data could be lacking. Also, most of the state-of-the-art performance figures have been reported for GaN HEMTs grown on SiC substrates which are very costly and are also limited in size [9]. Although the growth of GaN on silicon has been demonstrated, this technology is only available from three companies at the present time, namely Nitronex of the US, Picogiga of France, and Oki Electric of Japan [14]. To complicate matters, the sale of these substrates is subject to strict export control by their governments currently.

1.2 Objectives

There are two main objectives in this work. The first objective is to develop a robust GaAs-based PHEMT fabrication technology for power applications. For this reason, the PHEMT epitaxial layer structure and fabrication process have been optimized to produce a high breakdown voltage and a high maximum drain current at high frequencies. The second objective is to investigate issues such as trapping effects and hot carrier induced degradation affecting power PHEMTs in relation to using low- k benzocyclobutene (BCB) as a passivation material. PHEMTs are devices whose surface passivation plays an important role in their electrical performance. Issues such as output power degradation due to surface traps could be affected by the surface passivation material used. BCB is increasingly being used as a passivation material for III-V PHEMTs and has several advantages such as a lower dielectric constant (2.65) and easier processing requirement when compared to silicon nitride. However, its effect on the device surface states and hot carrier induced degradation has not been investigated so far. In this work, we have carried out systematic investigations to address these two primary objectives.

1.3 Major Contributions of the Thesis

A GaAs-based power PHEMT fabrication process based on both optical and electron beam lithography has been developed in this work. PHEMTs with a high gate-drain breakdown voltage and a high maximum drain current have been demonstrated. The effect of surface trapping and hot electron induced degradation of BCB-passivated PHEMTs have also been investigated and compared with the more

commonly used SiN-passivated devices. The most important contributions of this thesis are summarized as follows:

- (1) GaAs-based PHEMTs with a gate-drain breakdown voltage of 18 V and a maximum drain current of 470 mA/mm have been demonstrated using complete in-house fabrication tools and processes. The PHEMT structure makes use of a double-heterojunction for increased carrier density suitable for use in power applications.
- (2) The power performance and scalability of PHEMTs at 10 GHz on unthinned GaAs substrate has been characterized for use in coplanar waveguide (CPW) circuit applications. CPW circuits have the benefits of less stringent process requirements due to the absence of substrate thinning and via-hole etching which could cause substantial yield loss during processing. This study is useful as the derived relationship enables CPW circuit designers to have a more accurate knowledge of the device performance at different gate width resulting also in a faster design turn-around time.
- (3) The transient drain current of PHEMTs passivated by low- k BCB has been investigated and compared with the commonly used SiN. The surface trap model has been used to quantitatively describe the experimental data. This study

provides a better understanding of the device transient behaviour passivated by BCB and SiN and is useful in deciding on a suitable type of passivation material for the different applications.

- (4) The hot carrier induced degradation of PHEMTs passivated by BCB and SiN has been studied and compared. The experimental findings revealed the different dominant degradation mechanisms in the two technologies when the devices were subjected to hot carrier stress under a high electric field in the channel.

- (5) A C-X-Ku broadband and Ku-band power amplifier MMIC has been designed, fabricated and measured. The process for the circuit fabrication involves the integration of spiral inductors, metal-insulator-metal capacitors, and tantalum nitride thin film resistors into the technology that was developed for the PHEMTs. The circuits were CPW-based and the fabrication process eliminates the need for via holes etching and substrate thinning.

1.4 Organization of the Thesis

This thesis is divided into eight chapters. In Chapter 2, the working principles and the key techniques for the optimization of PHEMTs for power applications are presented. The issues of trapping effects and hot carrier induced degradation are known to be related to power PHEMTs and are also briefly introduced here. Chapter 3 provides a detailed description of the individual process steps that have been developed for the fabrication of GaAs-based power PHEMTs. The technology used for the MIM capacitors and thin film resistors is also documented. The dc and microwave performance of the fabricated PHEMTs are presented in Chapter 4. Following this, Chapter 5 investigates the effect of surface trapping on the transient drain current response of BCB-passivated PHEMTs. The results are compared with the SiN-passivated devices. Next, Chapter 6 studies the hot carrier induced degradation in BCB- and SiN-passivated devices. Chapter 7 presents the design, fabrication and measurement results of a broadband and Ku-band power amplifier MMIC. The results and fabrication challenges faced in the fabrication are discussed. Finally, Chapter 8 presents the conclusions of the work and also recommends future research work that could be carried out.

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Chapter 2

Device Physics, Process Optimization and Issues Related to Power PHEMTs

2.1 Introduction

The development of HEMTs began in 1978 after the demonstration of the formation of a two-dimensional electron gas (2DEG) with improved electron mobility in modulation-doped AlGaAs/GaAs heterostructures [1]. A heterostructure is a structure that consists of a combination of at least two layers of different semiconducting materials with different bandgaps. The widespread use of heterostructures in high-speed transistor devices has been made possible by advances made in the molecular beam epitaxy (MBE) technology. MBE allows the growth of material layers with a thickness of just a few nanometers and with sharp interfaces between them. However, a disadvantage of MBE is its small wafer throughput. Another growth technique that is used to grow heterostructures is the metal-organic chemical vapor deposition (MOCVD). MOCVD offers the benefit of a high production capacity but suffers from the severe drawbacks of the use of extremely toxic gases such as arsine and phosphine and the difficulty of controlling background impurities. Most of the HEMT wafers are grown by MBE today [2], [3], [4].

The first papers on lattice-matched AlGaAs/GaAs HEMT were published in 1980 [5], [6]. The AlGaAs/GaAs HEMT makes use of a 2DEG of extremely high carrier mobility that forms at the heterointerface between AlGaAs and GaAs. The

AlGaAs layer is a higher bandgap material compared to GaAs and is n-doped. As a result, electrons are transferred from the AlGaAs layer into the GaAs quantum well channel as it is energetically more stable for them. The n-doped AlGaAs layer is called the supply layer because electrons available in this layer due to doping are supplied to the channel layer [1], [3]. It is also commonly known as the barrier layer due to its higher bandgap energy compared to the channel material.

However, it was soon recognized that due to the small discontinuity of the conduction band energy at the AlGaAs/GaAs heterointerface, the immobile donor charge in the AlGaAs supply layer is also modulated by the applied gate potential. This results in a premature saturation of the channel sheet charge density leading to degraded modulation efficiency and speed of the AlGaAs/GaAs HEMT device. By replacing the GaAs channel using an InGaAs thin film inserted between the GaAs buffer and the AlGaAs supply layer, the resulting AlGaAs/InGaAs heterostructure has a larger conduction band discontinuity leading to better confinement of the electrons within the InGaAs quantum well. In addition, the electron mobility of the InGaAs material is higher compared to GaAs. As a result, there was a significant improvement in the modulation efficiency and performance of the HEMT device [7], [8]. Although InGaAs has a lattice constant mismatch between AlGaAs and GaAs, it can be grown dislocation-free as long as its thickness is less than a certain critical thickness. Below this critical thickness value, the InGaAs layer can be compressed and distorted from its normal cubic crystalline structure to match the lattice constant of the AlGaAs and GaAs materials. The strain that results from this lattice mismatch is contained entirely within the InGaAs layer. As the InGaAs layer has been unnaturally compressed to match the lattice constant and structure of GaAs, it is thus called a “pseudomorphic”

layer [9]. Therefore, by using an InGaAs layer in place of the GaAs channel, the HEMT has been transformed into a pseudomorphic HEMT (PHEMT) with improved performance. A comparison of the energy band diagrams of a GaAs-based conventional HEMT and PHEMT is shown in Figs. 2.1 (a) and (b), respectively.

(a)

(b)

Fig. 2.1. The energy band diagram of a GaAs-based conventional (a) HEMT and (b) PHEMT showing the Fermi level (E_f) and conduction band (E_c).

The first PHEMT results were published in 1985 where an InGaAs channel and a GaAs supply layer was used [10]. It was Ketterson and co-workers who introduced the standard PHEMT epitaxial layer structure that is commonly used today consisting of a GaAs buffer layer, an InGaAs channel layer, and an AlGaAs supply layer [11]. PHEMTs with this new structure were soon characterized in depth and its potential for microwave and millimeter wave applications was demonstrated [12]. However, the potential of PHEMTs as a power transistor was only exploited only after the so-called double-heterojunction (DH) layer sequence was introduced where there is an n-AlGaAs supply layer not only on top but also below the channel. The present day common power PHEMT structure was created by inserting an InGaAs channel between the two n-AlGaAs supply layers [13], [14].

2.2 PHEMT Layer Structure Design

The basic layer structure and energy band diagram of a GaAs-based PHEMT for power applications are shown in Figs. 2.2(a) and (b), respectively. The layer sequence consists of, from top to bottom, a GaAs cap layer, a barrier layer, an AlGaAs spacer, an InGaAs channel layer, a second spacer and the barrier layer below the channel, a superlattice buffer, a smoothing buffer layer and a GaAs substrate.

(a)

(b)

Fig. 2.2. A GaAs-based PHEMT for power applications showing its (a) typical layer structure (not to scale) and (b) energy band diagram.

The GaAs cap layer is typically 25-50 nm thick and is doped with Si at $10^{18} - 10^{19} \text{ cm}^{-3}$ for good source and drain ohmic contacts to the barrier and channel layers.

The cap layer reduces the device source resistance and also protects the Al-containing

barrier layer from surface oxidation, which is crucial in maintaining the long-term reliability of the device. The barrier layer can be uniformly doped or δ -doped (also called planar-doped or pulse-doped). The structure shown in Fig. 2.2 has two δ -doped electron supply layers, one below and the other on top of the channel layer, to increase the channel sheet carrier density. The δ -doping layer is formed by a few monolayers of Si with a doping concentration of about $5 \times 10^{12} \text{ cm}^{-2}$. Its use allows a lower doping concentration in the AlGaAs layer for the gate barrier. This increases the device breakdown voltage while maintaining a high 2DEG channel sheet charge density [15] and is thus frequently used in power PHEMTs. At the same time, DX-center related problems are reduced due to the spatial separation of the Si donor and $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer.

The spacer is undoped and is of the same material as the barrier layer. It is grown to reduce the Coulomb scattering between the ionized dopant atoms and the negatively charged 2DEG. The channel is a pseudomorphically grown $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($0.15 < x < 0.25$) layer with a thickness between 10-15 nm, well below the critical thickness limit to avoid dislocation formation. For power applications, a second pair of a spacer and a barrier layer is usually grown below the channel. This structure is then known as the DH PHEMT and will be discussed in detail in section 2.4.2. The use of a DH increases the channel charge density and improves the carrier confinement to the quantum well at the same time. In addition, a doped channel is also commonly used to further increase the channel carrier density although the electron mobility is reduced as a result. The requirement of a high carrier density is, however, more important than the device channel electron mobility. Therefore, the use of a doped channel is an epitaxial structure of choice for power PHEMTs [9]. The

buffer layer creates an energy barrier and reduces the electron injection from the channel into the substrate. The material can be undoped GaAs of up to 1 μm thick. The superlattice buffer structure of alternating layers of AlGaAs/GaAs is commonly used these days due to its larger effective band gap compared to the GaAs buffer. This further suppresses the injection of channel electrons into the buffer [16].

2.3 Device Physics

2.3.1 Charge Control Model

The first analytical model for charge transfer across the AlGaAs/GaAs modulation-doped heterojunction was reported by Delagebeaudeuf and Linh in 1982 [17] and was later extended by Lee and co-workers [18]. With the presence of a Schottky gate placed upon the AlGaAs layer, the 2DEG electron concentration n_s can be shown to be approximated by [19]

$$n_s = \frac{\epsilon_s}{q} \left[\frac{V_g - V_{th}}{d + \Delta d} \right] \quad (2.1)$$

where n_s is the 2DEG electron concentration, ϵ_s is the dielectric permittivity of AlGaAs, q is the electronic charge, $d = d_i + d_d$, d_d is the thickness of the doped AlGaAs layer beneath the gate and d_i is the undoped AlGaAs spacer thickness, V_g is the applied gate voltage, $V_{th} \approx \left(\frac{\phi_b}{q} - \frac{qN_d d_d^2}{2\epsilon_s} - \frac{\Delta E_c}{q} \right)$ is the threshold voltage and is the gate bias at which the channel between the drain and source just starts to form, ϕ_b is the Schottky barrier height associated with the metal-AlGaAs junction, $\Delta d = (\epsilon_s a)/q \sim 80 \text{ \AA}$ ($a \sim 0.125 \times 10^{-16} \text{ V}\cdot\text{m}^{-2}$), N_d is the doping concentration in the AlGaAs layer,

and ΔE_c is the discontinuity in the conduction band between the AlGaAs/GaAs interface.

For a delta-doped structure, the threshold voltage is given by

$$V_{th} \approx \left(\frac{\phi_b}{q} - \frac{qn_\delta d_\delta}{2\epsilon_s} - \frac{\Delta E_c}{q} \right) \quad (2.2)$$

where d_δ is the distance between the metal gate and the doped plane and n_δ is the sheet concentration of donors in the doped plane.

2.3.2 Current-Voltage Characteristics

Using the gradual channel approximation [20], the current-voltage (I-V) characteristics of the modulation doped FET can be worked out using the charge control model described by (2.1). The surface carrier concentration in the channel is given by

$$n_s(x) \approx \frac{\epsilon_s}{q(d + \Delta d)} (V_g - V_{th} - V(x)) \quad (2.3)$$

where x is the space coordinate along the channel and $V(x)$ is the channel potential.

The drain-to-source current I_{DS} is related to the electron velocity in the channel by

$$I_{DS} = qn_s v(F)W \quad (2.4)$$

where $v(F)$ is the electron velocity in the channel that is assumed to be a function of the electric field F in the channel, W is the gate width, q is the electronic charge, and n_s is the sheet carrier density in the 2DEG.

Using the gradual channel approximation, it is assumed that the channel electric field is along the direction of the drain to the source and the diffusion current is negligible. Considering the simpler two-piece linear approximation, when V_{DS} is small (i.e. $V_{DS}/L < F_s$), the electron velocity is proportional to the electric field F and is related by [20]:

$$v = \mu F \quad (2.5)$$

where μ is the effective low field mobility. By substituting (2.5) into (2.4) and integrating with respect to x from 0 to L , where L is the gate length, the conventional Shockley model equation describing the I-V characteristics of the transistor at low drain bias can be derived as:

$$I_{DS} = \beta \left[(V_g - V_{th}) V_{DS} - V_{DS}^2 / 2 \right] \quad (2.6)$$

where

$$\beta = \frac{\varepsilon_s \mu W}{(d + \Delta d) L} \quad (2.7)$$

Assuming that current saturation occurs when the electric field at the drain side of the gate exceeds the velocity saturation field $F_s = v_s/\mu$ and using the Schockley model in order to describe the longitudinal field distribution in the channel below the saturation voltage leads to the following relationships [19]-[21]:

$$I_{DS(sat)} = \beta V_0^2 \frac{(1 + 2\beta R_s V_g' + V_g'^2 / V_0^2)^{1/2} - 1 - \beta R_s V_g'}{1 - \beta^2 R_s^2 V_0^2}, \text{ and} \quad (2.8)$$

$$V_{DS(sat)} = V_g' + V_0 - (V_g'^2 + V_0^2)^{1/2} + I_{DS(sat)} (R_s + R_d) \quad (2.9)$$

where $V_g' = V_g - V_{th}$, $V_0 = F_s L$, F_s is the critical electric field for velocity saturation, R_s is the source resistance, and R_d is the drain resistance. The expression derived for $I_{DS(sat)}$ above is quite good for $V_g > V_{th}$ but there is considerable subthreshold current not predicted by the charge control model. For $V_g > V_{th}$ and d of about 300 Å, the charge control model appears adequate enough though.

2.3.3 Small-Signal Device Capacitances

Using the two-piece model for $V_{DS} < V_{DS(sat)}$, the total charge Q_T stored in the 2DEG is given by [22]:

$$Q_T = \left[\frac{2\epsilon_s WL}{3(d + \Delta d)} \right] \left[\frac{V_{gs}^3 - V_{gd}^3}{V_{gs}^2 - V_{gd}^2} \right] \quad (2.10)$$

where V_{gs} is the gate-to-source voltage and V_{gd} is the gate-to-drain voltage.

Then, the gate-source and the gate-drain capacitances, C_{gs} and C_{gd} respectively, can be expressed as:

$$C_{gs} = \frac{\partial Q_T}{\partial V_{gs}} = \frac{2\epsilon_s WL V_{gs} (V_{gs} + 2V_{gd})}{3(d + \Delta d)(V_{gs} + V_{gd})^2}, \text{ and} \quad (2.11)$$

$$C_{gd} = \frac{\partial Q_T}{\partial V_{gd}} = \frac{2\epsilon_s WL V_{gd} (V_{gd} + 2V_{gs})}{3(d + \Delta d)(V_{gs} + V_{gd})^2}. \quad (2.12)$$

Beyond the saturation regime, C_{gs} is approximated by:

$$C_{gs} = \frac{\epsilon_s WL}{d + \Delta d}, \text{ and} \quad (2.13)$$

$$C_{gs} \gg C_{gd}. \quad (2.14)$$

2.3.4 Maximum Transconductance Characteristics

The maximum intrinsic transconductance $g_{m,max}$ of the modulation doped transistor can be derived using the charge control model that is based on the simplified two-piece linear approximation and is shown as

$$g_{m,max} = \frac{q\mu(V_g - V_{th})}{\left[L(d + \Delta d) \left\{ 1 + \frac{\mu(V_g - V_{th})}{v_s L} \right\}^2 \right]^{0.5}} \quad (2.15)$$

2.3.5 RF Figures of Merit

The two most important figures of merit in describing the frequency characteristics of PHEMTs are the cutoff frequency f_T and the maximum frequency of oscillation f_{max} . f_T is defined as the frequency at which the short circuit current gain h_{21} becomes unity (or 0 dB). h_{21} is frequency dependent and its magnitude decreases at higher frequencies at a rate of -6 dB/octave or - 20 dB/decade. The octave and decade is a change of factor of 2 and 10 in frequency, respectively [2]. f_{max} is defined to be the frequency at which the unilateral power gain (U) becomes unity (or 0 dB) and is therefore the maximum frequency at which the device still gives a power gain. Likewise, the magnitude of U decreases at higher frequencies at a rate of -6 dB/octave. Sometimes, f_{max} is referred to be the frequency at which the maximum available gain (MAG) rather than U becomes unity. This is not completely correct. The values of f_{max} extrapolated from U and MAG can be different from each other although they are not significantly different in most cases.

The current gain cut-off frequency f_T is determined by the transit time of carriers under the gate and is given by:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \approx \frac{v_s}{2\pi L} \quad (2.16)$$

and the maximum frequency of oscillation f_{max} [23] is:

$$f_{max} = \frac{f_T}{\sqrt{\frac{4g_0}{g_m} \left(g_m R_i + \frac{R_s + R_g}{\frac{1}{g_m} + R_s} \right) + \frac{4C_{gd}}{5C_{gs}} \left(1 + \frac{5C_{gd}}{2C_{gs}} \right) (1 + g_m R_s)^2}}. \quad (2.17)$$

f_T is more important than f_{max} in terms of digital performance whereas f_{max} is preferred when it comes to characterizing high-frequency devices as it takes into account losses associated with the gate and source resistance and output conductance. As we can see from (2.11)-(2.13) and (2.15)-(2.17), the reduction of gate length leads to the reduction of C_{gs} and C_{gd} improving the transconductance, cut-off frequency and maximum frequency of oscillation.

2.4 Optimization of Power PHEMTs

PHEMTs have demonstrated state-of-the-art millimeter-wave power performance primarily due to their high transconductance, low gate leakage current, high breakdown voltage, excellent pinch-off characteristics and low output conductance [9]. Electrical requirements for power devices include a high full-channel current (I_{max}) and a high gate-drain breakdown voltage (BV_{GD}).

2.4.1 Use of Double Recess for Gate

A high breakdown voltage is needed for power devices for two reasons. First, a higher breakdown voltage has been attributed to longer lifetimes. Second, a higher breakdown voltage allows a higher operating drain voltage resulting in a higher output power density as long as power gain is sustained. Typically, the breakdown voltage of a transistor should be at least twice that of the operating drain bias [24]. The use of a double recess process is a common technique to improve the BV_{GD} of PHEMTs. Double-recessed PHEMTs (DR-PHEMTs) have emerged as excellent transistors for microwave power applications. Since the first double-recessed PHEMT was reported in 1991 [25], its potential for use in high output power and high efficiency systems was soon demonstrated and confirmed [26], [27]-[31]. Fig. 2.3 shows a typical cross section of a double-recessed PHEMT.

Fig. 2.3. A typical cross section view of a double-recessed PHEMT.

During the double recess process, the first wider recess stops at the n-doped GaAs cap layer, leaving a thin layer of about 50 Å of that material underneath the surface. The second narrower recess is then etched into the barrier layer to obtain the desired channel drain current [32]. The gate length is defined by the second recess etch. The double recess technique lowers the peak electric field in the region between the gate and the drain contact thus leading to an improvement in the breakdown voltage [33]. A long first recess (L_{FR}) improves the gate-drain breakdown voltage but degrades f_T at a given drain bias due to the lengthening of the drain depletion zone increasing the drain delay. Similarly, a shorter L_{FR} decreases BV_{GD} but improves f_T as the drain delay becomes shorter [24]. Therefore, a tradeoff is to be made between a reasonable device breakdown voltage and its intended frequency of operation.

2.4.2 Double-Heterojunction Layer Structure

To increase the maximum full channel current (I_{max}), it is necessary to increase the number of charge carriers in the channel. To achieve this, the epitaxial layer structure could be reengineered. As PHEMTs rely on the concept of carrier transfer from a material of a larger bandgap to one of a smaller bandgap, two approaches have been developed to increase the channel carrier sheet density. The first involves the use of two doped layers on both sides of the channel rather than just one in the upper AlGaAs layer above the channel. This method results in the so-called DH structure. Its development meant a breakthrough for PHEMTs which thereby became a universal microwave technology that is applicable for both receivers (low-noise application) and transmitters (power application) [3]. The second technique involves the growth of δ -doped layers with very narrow and concentrated doping pulses instead

of a uniform doping in the AlGaAs supply layers. These δ -doped layers are typically located about 30 Å – 100 Å from the channel. By doing so, the charge transfer efficiency is improved due to the very high doping density of the δ -doped PHEMT device. This could be $3.2 \times 10^{12} \text{ cm}^{-2}$ compared to $1.5 \times 10^{12} \text{ cm}^{-2}$ in a single δ -doped structure, giving a factor of two in improvement. In addition to the increase in the channel charge density through the use of δ -doping, there is also an enhanced energy barrier at the heterointerface below the channel. This significantly improves the confinement of the charge carriers to the quantum well at high drain bias. Therefore, the DH-PHEMT not only provides the amount of current needed for power at high frequencies but also offers the best transport properties at high bias. In summary, the use of a δ -doped DH in the device epitaxial layer structure and the double gate recess process are enabling techniques to maximize the power capability of the PHEMT device. These methods are adopted in this work in the development of a power PHEMT process.

2.4.3 Output Power and Power Added Efficiency

In power PHEMTs, the output power P_{out} and power added efficiency PAE are two figures of merit relating to its power handling capability and power conversion efficiency. In power transistors, the amount of microwave power that is delivered to the load is important. P_{out} is dependent on the frequency and the class of amplifier circuit that the device operates in. The output power is frequently expressed in terms of power density and a commonly used figure of merit for PHEMTs is the output power per millimeter of the device gate width. These parameters give circuit designers an idea of the power handling capability of the transistors and allow them to

choose the appropriate devices in their design. In power amplifiers, where the dissipation of heat or battery power is a concern, the power-added efficiency is an important figure of merit and is defined as the ratio of the difference of the transistor's output and input power to the dc power supplied to it to operate the device. The power-added efficiency PAE is expressed as:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \quad (2.18)$$

where P_{out} and P_{in} represent the microwave output and input power, respectively, and P_{dc} is the dc power delivered by the power supply to the transistor device. A high PAE means that the power losses are small and a longer battery operation can be sustained [3]. For microwave power transistors, a high output power density and PAE are desirable.

2.5 Trapping Effects

It is commonly believed that deep levels in both the substrate and the buffer layers and surface states are responsible for the harmful trapping effects in GaAs MESFETs [34]-[38]. GaAs PHEMTs exhibit similar surface trapping effects as their MESFET counterparts but are possibly worsened due to the smaller separation between the surface and the channel layer [39]. Trapping effects may deteriorate the output power of PHEMTs.

A variety of techniques have been used to characterize trapping effects. Frequency dependence study of the transconductance and conductance are two such techniques. Transconductance dispersion is attributed to trapping at or near the surface while that of conductance dispersion is attributed to the material underlying the active channel [39]. Among the more frequently used ones include the

measurement of the transient drain current as it is sensitive to the entire channel between the source and drain. This is different from the capacitance methods that mainly probe the region under the gate [40]. There are two main transient drain current measurements that are carried out, namely drain lag and gate lag. Gate lag is a phenomenon where the drain current comes on only partially and then slowly increases toward the steady state value when the transistor is turned on by the sudden application of a gate pulse. In drain lag, the presence of slow transients in the drain current is observed when the drain voltage is changed abruptly. It is generally believed that gate lag has its origin in surface states while drain lag is associated with traps in the buffer layer and the substrate [36], [37], [41]-[44].

Gate lag can pose serious problems for digital and analog circuits. In digital circuits, gate lag can result in pulse narrowing and the eventual loss of transmitted pulses leading to functional errors. In analog circuits, gate lag could result in the degradation of output power and distortion characteristics [37], [39], [43], [45], [46].

It is believed that surface states between the gate and source/drain contacts behave as “virtual gates” modulating the depletion region underneath through changes in the density of negatively charged traps. When the gate bias voltage is changed suddenly, these “virtual gates” respond in a manner that is characterized by the carrier capture and emission rate. This leads to a delayed response in the complete turning on of the drain current leading to degraded power performance [45]. The effect of surface trapping has been shown to be effectively suppressed by minimizing the extension of the ungated region of the recess geometry and choosing a suitable passivation film

with optimized deposition conditions [37], [41]. In this work, the surface trapping effect of PHEMTs passivated by SiN and BCB was studied and compared.

2.6 Hot Carrier Induced Degradation

A reliability concern in power PHEMTs is device performance degradation under hot carrier and impact ionization conditions. The high drain bias that the devices are usually subjected to in order to maximize output power creates a high gate-drain electric field that leads to the generation of electron-hole pairs as a result of impact ionization. It is known that the device surface conditions, including the type of surface passivation film, can have a significant effect on the type and extent of degradation after hot carrier stress. Reported degradation in the PHEMT characteristics after hot carrier stress include threshold voltage shift, drain current compression, power slump and breakdown walkout [47]-[50]. Power slump is a phenomenon where the device output power exhibits a gradual but steady decrease over time when it is rf over-driven. It is attributed to changes in the device dc parameters such as the drain current and breakdown voltage. The degradation rate slows with increasing stress time but it does not reach saturation [51]. In breakdown walkout, the device breakdown voltage increased permanently after it is biased at a high electric field under hot carrier conditions. Although this results in the device becoming more resistant to breaking down during subsequent high voltage operations, it is often accompanied by other undesirable effects. These include degradation in the device drain current, transconductance, and rf gain [50], [52]-[56]. In this work, the degradation induced by hot carriers has been investigated in BCB- and SiN-passivated devices. The mechanisms responsible for the different degradation modes have also been proposed.

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Chapter 3

Power PHEMT Process Development

3.1 Introduction

Developing a robust GaAs-based PHEMT fabrication technology for power applications is an important objective of this work. Using a complete line of in-house process steps and characterization equipments, a repeatable fabrication process based on a combination of optical and electron beam lithography (EBL) has been developed for double-recessed PHEMTs with a gate length of about 0.25 μm . The epitaxially grown GaAs substrates were bought from a commercial MBE growth company. The major steps involved in the fabrication of the transistors are (1) mesa isolation, (2) ohmic source and drain contact formation, (3) first metal deposition, (4) T-gate fabrication using the double-recess (DR) technique, (5) surface passivation and finally (6) formation of airbridges to interconnect all the source pads. In this chapter, the key features of each processing step will be described in detail.

3.2 Double-Heterojunction Layer Structure Design

The epitaxial layer structure of the GaAs-based PHEMT designed for power applications is shown in Fig. 3.1. The function of each layer has been described earlier in Chapter 2. The structure makes use of a DH with an upper (δ -doping 1) and a lower (δ -doping 2) silicon δ -doped layer of concentration $4 \times 10^{12} \text{ cm}^{-2}$ and $1 \times 10^{12} \text{ cm}^{-2}$, respectively.

n-GaAs Cap Layer (400 Å), doping = $6 \times 10^{18} \text{ cm}^{-3}$
n-AlGaAs barrier (240 Å), doping = $3 \times 10^{17} \text{ cm}^{-3}$
i-AlGaAs spacer (30 Å) δ doping 1
InGaAs Channel Layer (140 Å)
i-AlGaAs spacer (30 Å)
i-AlGaAs barrier (250 Å) δ doping 2
i-AlGaAs/GaAs (200 Å/15 Å) superlattice buffer (10 periods)
i-GaAs (2500 Å)
S.I. GaAs (100) substrate

Fig. 3.1. PHEMT epitaxial layer structure designed for power applications (dimensions not to scale). It makes use of a DH and two δ -doped layers for improved charge confinement within the quantum well and increased channel sheet charge density.

3.3 Device Fabrication

The fabrication of the submicron DR-PHEMTs involves six primary steps namely,

1. Mesa isolation using a wet etchant,
2. Source and drain ohmic metallization formation using the lift-off technique,
3. First level metallization,
4. EBL consisting of:
 - 4.1 First recess box patterning,
 - 4.2 Submicron T-gate patterning and gate recess,
5. Passivation, and
6. Interconnection of source pads using airbridges.

A mix-and-match technique has been employed whereby all the steps, except step 4, utilized conventional optical contact lithography.

The PHEMT fabrication process began with the lateral isolation of the active areas of the individual devices. After the wafer was cleaned, the positive resist AZ1518 was coated on it and spun at 4000 rpm for 30 s. It was then soft baked at 105°C for 90 s using a hotplate. The mesa patterns were defined using contact lithography and after development, the wafer was baked in a 110°C oven to harden the resist against etching [1]. Except for the active regions, the rest of the wafer was etched using a sulfuric acid: hydrogen peroxide: deionized water mixture in a volume ratio of 4:1:35. The etch rate was about 35 Å/s at 22°C. The isolation process confined the current flow to within the isolated islands on which the PHEMTs were to be fabricated. Typically, the etching was stopped at the buffer layer with an etch depth of about 1250 Å. The end-point was monitored using both a Dektak³ST surface profiler and an HP 4156 semiconductor parameter analyzer (SPA) to measure the isolation current between devices. A leakage current value of about 30 nA was considered acceptable. After etching, the resist was stripped using warm acetone.

Next, the source and the drain ohmic contacts were fabricated using a five-layer metal system of Ni/Ge/Au/Ni/Au (5nm/25nm/100nm/20nm/200nm). The image reversal resist AZ5214 was used for all the lift-off processes in this work. The use of such a resist allowed for the formation of an automatic undercut profile without having the need to use other more difficult techniques such as the chlorobenzene process. Further, the process is usually well-controlled, highly reproducible and offers good resolution [2]. AZ5124 was first coated and then soft baked at 105°C for 90 s

using a hotplate. After alignment and UV exposure, the whole wafer was post-exposure baked in an 110°C oven for about 8 minutes. Finally, the wafer was blanket UV-exposed for 20 s before being developed. It was then loaded into the evaporation chamber and the ohmic metal scheme deposited layer by layer. After the lift-off, the alloy was rapid thermal annealed at about 410°C for 10 s to achieve a typical contact resistance not exceeding 0.3 Ω mm. A similar lift-off process was used for the Ti/Au (0.05 μ m / 0.35 μ m) metal to connect the source, drain, gate, and probe pads together.

3.4 Electron Beam Lithography and Gate Recess

The formation of the 0.25 μ m T-gate involves the use of the double recess technique to improve the breakdown voltage of the transistor. During the double recess, the first wider recess was stopped within the n-doped GaAs cap layer, leaving a thin layer of about 50 Å of that material underneath the surface. The second narrower recess was then etched into the barrier layer to obtain the desired channel drain current [3]. The double recess technique lowers the peak electric field in the region between the gate and the drain leading to an improvement in the breakdown voltage. The schematic of a double-recessed PHEMT is shown in Fig. 3.2.

Fig. 3.2. Schematic cross section view of a double-recessed PHEMT.

The pattern for the first wider recess is a rectangular box that was positioned centrally between the source and drain contact of 3 μm separation. Its length, defined in the same direction as the gate length, was about 0.7 μm . We called this pattern the wide recess box (WRB) in this work and its layout is shown schematically in Fig. 3.3. The WRB was written by first spinning methacrylic acid copolymer (MMA (8.5) MAA, dissolved in 11 % ethyl lactate) at 4000 rpm for 60 s. The thickness obtained was about 470 nm. The box pattern was then defined using an EBL system based on a JEOL JSM 6600 scanning electron microscope (SEM) with a RAITH laser interferometer stage and ELPHY 1.0 lithography software. After exposure, the sample was developed using a methyl isobutyl ketone (MIBK): isopropanol (IPA) = 1:3 mixture at 23°C for one minute. An additional one-minute rinse in IPA acted as a developer stopper. The first wide recess was then carried out where the uppermost cap layer was etched to just tens of angstrom above the barrier layer using a citric acid-

hydrogen peroxide solution at 10°C. The low temperature process enabled the etching rate to be better controlled at about 8 Å/s.

Fig. 3.3. Layout of wide recess box used in the fabrication of a double-recessed PHEMT in this work.

After the first recess process, a two-layer e-beam resist scheme was used to fabricate the submicron T-gate [4]. The first layer involved the spinning of polymethylmethacrylate (950 PMMA C2) at 700 rpm for 1 minute giving a film thickness of about 230 nm. The wafer was then baked dry in a 160°C oven for 1 hour. It is important to note that the thickness uniformity of this resist layer is particularly important as it determines the actual footprint of the gate and can also affect the yield of the subsequent gate recess step. The thickness uniformity can be affected by the temperature and humidity of the surrounding area where the resist was coated. A 10% thickness variation usually translated into very poor device yield as thicker resist portions along the direction of the gate width could not be developed completely. The cap layer underneath it would not be etched away during gate recess. This will create a parallel conduction path between the source and the drain contact and the transistor

will not pinch off. After the PMMA has been baked, a second layer of MMA-MAA was spun at 4000 rpm for 60 s and is baked at the same condition as the PMMA. This layer is 470 nm thick and is used for creating the top part of the T-gate to reduce the gate resistance.

After the T-gate exposure using the EBL system, the gate pattern was developed and then inspected using a SEM under low voltage. Then, the wafer was processed in an oxygen descum machine to remove traces of the residual e-beam resist that might have remained after development. This is a crucial step as the insufficient or absence of resist ashing would result in poor recess uniformity or no gate recess at all.

The next step involved the gate recess and is probably the most critical step in the fabrication of a PHEMT device. The gate recess etchant was the same solution used earlier. Gate recess is performed to adjust the threshold voltage and the saturation drain current of the device. As the epitaxial layer structure has no etch stop layers, constant monitoring of the drain current was required using an HP 4156 SPA with dc tungsten probes as the etching approached the AlGaAs barrier layer. However, too many etch-and-check steps could result in a rough surface. Usually, the desired drain current was achieved in two or at most three steps. After the gate recess process, the wafer was dipped in diluted hydrochloric acid to remove surface oxide and then immediately loaded into the evaporation chamber for gate metal Ti/Au (0.05 μm /0.35 μm) deposition. A schematic flow of the fabrication of a T-gate using the double-recess technique is shown in Fig. 3.4. Figs. 3.5 and 3.6 show the SEM photographs of a 2-finger PHEMT without airbridge and a T-gate with a gate length

of about 0.25 μm , respectively. The width of the T-gate head is about 0.7 μm as indicated in Fig. 3.7.

(a) After EBL of wide recess box using MMA-MAA.

(b) The first recess etch using a citric acid – hydrogen peroxide solution at 10°C was stopped slightly above the cap layer.

(c) The T-gate was patterned using the bilayer e-beam resist system of PMMA and MMA-MAA. The sensitivity of MMA-MAA is higher than that of PMMA.

(d) The resist profile of the T-gate after EBL

(e) The second recess determines the threshold voltage of the PHEMT and is the most critical step in the fabrication process.

(f) The profile of the T-gate after metal lift-off.

Fig. 3.4. Schematic of the fabrication process flow for a double-recessed T-gate.

Fig. 3.5. SEM picture showing the plan view of a 2-finger PHEMT device (without airbridge).

Fig. 3.6. SEM picture showing the cross-section of a T-gate with a gate length of about 0.25 μm.

Fig. 3.7. SEM picture showing the plan view of the top of the T-gate. Head width is about 700 nm.

3.5 Surface Passivation

The surface passivation material used in the baseline process is silicon nitride (SiN) deposited using plasma enhanced chemical vapor deposition (PECVD). SiN is probably the material that is most popularly used as both passivation film and capacitor dielectric in GaAs processing. SiN is a better diffusion barrier layer than silicon dioxide (SiO₂) and therefore is better for encapsulation [5]. It is an almost impermeable diffusion barrier to moisture and mobile ions like sodium [6]. Its higher dielectric constant compared to SiO₂ also makes it the preferred choice as capacitor dielectric.

Other than protecting the wafer from environmental contamination and mechanical damage, the passivation layer also serves to suppress the harmful effects of surface states present at the device ungated active region between the source/drain

and the gate. As discussed earlier in section 2.5, the surface states, or surface traps as they are also commonly known, can result in the eventual loss of transmitted pulses in digital circuits while leading to output power degradation in analog applications. During the passivation of the PHEMT devices, SiN was first grown on the entire wafer at 300°C using silane and ammonia. Then, AZ5214 photoresist was coated on the wafer and patterned. Except for the SiN at the active region between the source and the drain contact (where the gate was located), the rest of it was removed using reactive ion etching. In the fabrication of MMICs, this layer also serves as the capacitor dielectric and is deposited at the same time as the passivation of the active devices.

Recently, the use of BCB as an alternative passivation material has become popular due to its lower dielectric constant compared to SiN [7]-[10]. A lower dielectric constant results in lower parasitics during high frequency operation. However, as a diffusion barrier layer, BCB is inferior to SiN and SiO₂. For example, BCB has a higher water permeability compared to SiO₂ [11]. Moisture penetration through the passivation film under high humidity test conditions has been known to cause degradation of the device drain current and a shift in its threshold voltage [12]. The drain current reduction was attributed to surface damage at the AlGaAs recess region caused by a reaction between the surface and moisture. The shift in threshold voltage was linked to a change in the stress under the gate created possibly as a result of the peeling of the passivation film. Currently, reliability data on BCB-passivated PHEMTs is lacking and more work is needed to provide a clearer picture.

In the selection of a low-k passivation material, many issues need to be taken into consideration. These include the material process integration compatibility and its electrical, thermal, and mechanical properties to meet circuit design requirements. All these need to be evaluated carefully and trade-offs are often made between performance requirements, material properties and process compatibility [13], [14].

In Chapter 5, the effectiveness of BCB as a passivation material in suppressing the device surface states is investigated and compared with the more commonly used SiN. A study of the transient drain current characteristics in both BCB- and SiN-passivated PHEMTs is presented.

3.6 Airbridge Interconnection

The last step in the fabrication flow involved the interconnection of all source pads using airbridges. Fig. 3.8 shows the process sequence for the fabrication of gold plated airbridges. This layer of metal is also commonly referred to as level 2 metal (M2) in commercial foundries. The plating process flow is described here. First, resist AZ5214 was coated on the entire wafer and pillar openings were patterned at the source pads where airbridges would connect them. The resist was then reflowed in a 130°C oven for 20 minutes. After this, Ti/Au (50 nm/100 nm) was blanket evaporated over the entire surface. This layer served as the seedling for gold plating later.

(a) The source pads were to be connected using an airbridge.

(b) Patterning of pillar openings and coating of seedling layer.

(c) Patterning of the upper level AZ5214 was then followed by the plating of gold on areas with exposed seedling metal.

(d) Cross section view of the plated airbridge after the removal of the resists and seedling layer.

Fig. 3.8. Schematic process flow of a plated airbridge.

The upper interconnect metal mask was then patterned using AZ5214 with a bright field mask. It is important that there should be no rework of this step as the removal of this layer of resist would most probably cause the resist underneath the seedling layer to be dissolved as well. This will cause the seedling metal to ‘collapse’ and attach itself onto the whole wafer and destroying it in the process. The total thickness of the two layers of AZ5214 resist was about 4 μm measured using the Dektak³ST surface profiler. Non-cyanide based electroplating was carried out using a beaker bath at 55°C. The thickness of the plated gold was measured by monitoring the height between the top of the resist and the plated metal pad. The difference between the total resist thickness (4 μm) and the height gives the amount of gold that has been plated. A typical gold thickness of about 3 μm was used.

After plating, the uppermost resist layer was removed followed by the etching of the Ti/Au seedling layer using a gold etchant solution ($\text{KI} : \text{I}_2 : \text{deionized H}_2\text{O}$) and diluted hydrofluoric acid (HF), respectively. Extra care needs to be exercised here as HF is an extremely hazardous acid. The etching of Ti could be observed with the production of bubbles, and a 3 s over-etch ensured the complete removal of the material. Finally, the lower layer of resist AZ5214 was rinsed off using warm acetone. The fabrication of airbridges is now complete. The schematic plating process flow and a SEM photograph of a fabricated airbridge are shown in Figs. 3.8 and 3.9, respectively.

Alternatively, the interconnect airbridge could also be deposited using the metal evaporation and lift-off technique. In this case, after the upper interconnect mask was patterned, the seedling layer was etched away and some lateral undercut

was purposely created by a slight over-etch to facilitate metal lift-off later. Then, Ti/Au (0.05 μm /1.2 μm) was evaporated and the whole wafer soaked in acetone for lift-off. Fig. 3.10 shows a SEM photograph of a lift-off airbridge. After the airbridge interconnection was completed, the devices are ready for characterization. Chapter 4 discusses the performance of the PHEMTs in detail.

Fig. 3.9. Microscope photograph of a 6-finger PHEMT device with a plated airbridge.

Fig. 3.10. SEM photograph showing a lift-off airbridge with a gate underneath it.

3.7 MMIC Fabrication

The PHEMT device process technology was extended to the fabrication of GaAs-based MMICs. The circuit process involves the integration of passive elements such as the spiral inductors, metal-insulator-metal (MIM) capacitors and thin film tantalum nitride (TaN) resistors into the device fabrication flow. The insulator used in MIM capacitors is PECVD SiN of thickness of about 1200 Å. It is deposited at the same time during the surface passivation of the gate. The schematic process flow of a PHEMT MMIC based on the coplanar waveguide (CPW) configuration is shown in Fig. 3.11. A more detailed MMIC fabrication showing process conditions is included in Appendix A.

Fig. 3.11. Schematic of fabrication flow of a CPW PHEMT MMIC.

3.7.1 Tantalum Nitride Thin Film Resistors

Resistors are widely used in MMICs for matching and biasing purposes. It can be made using a doped semiconductor film or a metal film such as nickel-chromium (NiCr) or tantalum nitride (TaN). In this work, dc magnetron sputtered TaN film was used as thin film resistors with a sheet resistance of $50 \Omega/\square$. The process variation is within 10% [15]. TaN resistors are commonly used by commercial foundries in MMICs [16], [17].

The realization of the TaN resistors makes use of the lift-off technique. Resistor patterns were first defined using AZ5214. It is important to ensure in this step that the undercut of the resistor pattern is sufficient as the sputtering technique gives a good conformal coverage over the whole wafer. Otherwise, the film will not lift-off easily later. After visual pattern inspection using a microscope, the film was deposited by dc sputtering of the tantalum target using a mixture of argon and nitrogen gas. The thickness of the film was about 450 Å. Finally, the wafer was soaked in acetone to lift-off the unwanted regions. Fig. 3.12 shows a photograph of a patterned TaN thin film resistor.

Fig. 3.12. Microscope photograph of a thin film TaN resistor.

3.7.2 MIM Capacitors

MIM capacitors are commonly used in MMICs with SiN being a popular dielectric [16]-[20]. Fig. 3.13 shows the schematic process flow for an overlay capacitor. Ti/Au (50 nm/350 nm) was used for the bottom plate of the capacitor. This was followed by the deposition of 1200 Å of PECVD SiN using a Plasma Therm 790 machine at 300°C using a mixture of silane and ammonia. Next, AZ1518 was used to define the dielectric window for the capacitors and the PHEMT gate active region for the purpose of passivation. Then, Ti/Au (50 nm/ 100 nm) was evaporated as a seedling layer for plating. Finally, the top plate was connected to the transmission line using gold plated airbridges. The value of the capacitance is about 450 pF/mm² using 1200 Å SiN. Figs. 3.14 and 3.15 show the SEM photographs of a fabricated MIM overlay capacitor.

Fig. 3.13. Schematic process flow of an MIM capacitor

Fig. 3.14. SEM photograph of an MIM overlay capacitor showing the upper capacitor plate.

Fig. 3.15. Close up view showing the airbridge of the capacitor.

3.8 Summary

In this chapter, a GaAs-based PHEMT fabrication technology for power applications has been presented. It makes use of a combination of optical and electron beam lithography to develop DR-PHEMTs with a gate length of about 0.25 μm . The PHEMT epitaxial structure consists of a double-heterojunction with a δ -doping layer both above and below the channel to increase the channel charge density and improve the quantum well carrier confinement at the same time. The major steps involved in the fabrication of the transistors are, in this order, mesa isolation, ohmic source and drain contact formation, first metal deposition, double-recessed T-gate fabrication, surface passivation and finally the formation of airbridges to interconnect all the source pads. The most critical part of the process is probably the fabrication of the T-gate. The e-beam resist thickness has to be properly controlled so that the entire width of the gate could be developed completely after e-beam writing. Otherwise, the uppermost cap layer could not be etched away and the transistor will not pinch off. During gate recess, the timing and drain current need to be monitored closely so that the desired threshold voltage and saturation drain current can be achieved. The technology that was developed for PHEMTs has also been extended to the fabrication of GaAs-based MMICs. The process for the circuit fabrication involves the integration of spiral inductors, MIM capacitors, and TaN thin film resistors into the fabrication flow for PHEMTs.

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Chapter 4

Characterization of Double-Recessed PHEMTs

4.1 Introduction

The performance characteristics of DR-PHEMTs fabricated in this study are presented. DC and rf measurements were carried out on devices with gate width ranging from 40 μm to 1000 μm . The microwave load-pull performance of two devices with a gate width of 200 μm and 1000 μm was characterized at 10 GHz at different bias conditions. To benchmark the performance of the transistors fabricated in this work, a comparison was also made with the technology offered by two commercial foundries, TriQuint Semiconductor of the USA [1] and United Monolithic Semiconductors (UMS) of France [2]. Finally, the effect of device scaling on output power, gain and *PAE* was investigated for PHEMTs with the gate periphery ranging from 200 μm to 1000 μm at 10 GHz. An understanding of the scaling relationship is useful to circuit designers when using devices of different gate width.

4.2 Device Performance

Fig. 4.1 shows a microscope photograph of a 2x100 μm DR-PHEMT with 2 gate fingers of width 100 μm each. Its drain current versus drain voltage (I_{DS} - V_{DS}) performance is shown in Fig. 4.2(a). I_{DS} is about 410 mA/mm at a gate voltage (V_G) of 0.6 V. The maximum transconductance and the gate-drain breakdown voltage (BV_{GD}) are about 350 mS/mm and -21.5 V, respectively as shown in Figs. 4.2(b) and 4.2(c).

Fig. 4.1. Microscope photograph of a $2 \times 100 \mu\text{m}$ device with a total gate width of $200 \mu\text{m}$.

It can be seen from the device I_{DS} - V_{DS} characteristics in Fig. 4.2(a) that there is a kink at about $V_{DS} = 3.5 \text{ V}$. The kink is a phenomenon where there is an abnormal increase in the device drain current observed at relatively low drain-source voltages. It is an undesirable characteristic whose effect includes an increase in the device output conductance and compression of the transistor transconductance. It is a common problem that is present in GaAs- (AlGaAs/GaAs, AlGaAs/InGaAs) and InP-based (InAlAs/InGaAs) HEMTs. It is generally believed that the kink is due to the interaction between the holes generated as a result of impact ionization and the surface deep acceptor traps at the ungated region of the barrier layer semiconductor surface [3], [4], [5]. At a drain-source voltage where the impact ionization in the channel becomes significant, electron-hole pairs are produced. The generated holes can then discharge the negatively charged surface traps and in the process, the depletion region underneath the gate is reduced due to a change in the electric potential. This can then lead to a kink, or an increase in the device drain current. It has

been reported that a proper device surface passivation process can help to suppress the kink effect through reduction of the density of surface traps [4], [6].

(a)

(b)

(c)

Fig. 4.2. DC performance of a 2x100 μm gate width PHEMT device. (a) I_{DS} - V_{DS} characteristics, (b) Transfer characteristics, and (c) Gate-drain breakdown voltage.

Biasing the device at $V_G = -0.5$ V and $V_{DS} = 6$ V with $I_{DS} = 36$ mA, the load-pull results (tuned for maximum power and efficiency) at 10 GHz are shown in Fig. 4.3. The saturated output power (P_{sat}) and PAE was 18 dBm and 40%, respectively, at a corresponding gain of 8 dB. At these bias conditions, the f_T and f_{max} was about 40 GHz and 100 GHz, respectively, as shown in Fig. 4.4. When the drain voltage was increased to 8 V, P_{sat} and gain improved to 20 dBm and 10 dB, respectively, as shown in Fig. 4.5. Fig. 4.6 shows that the corresponding f_T and f_{max} value did not degrade when $V_{DS} = 8$ V.

Fig. 4.3. Load-pull results of a 2x100 μ m device at 10 GHz with the device biased at $V_G = -0.5$ V, $V_{DS} = 6$ V, and $I_{DS} = 36$ mA.

Fig. 4.4. Current gain ($|H_{21}|^2$), maximum available power gain/maximum stable gain (MAG/MSG) and unilateral power gain (U) curves of a 2x100 μm device biased at $V_G = -0.5$ V, $V_{DS} = 6$ V and $I_{DS} = 36$ mA.

Fig. 4.5. Load-pull results of a 2x100 μm device at 10 GHz with the device biased at $V_G = -0.5$ V, $V_{DS} = 8$ V, and $I_{DS} = 41$ mA.

Fig. 4.6. Current gain ($|H_{21}|^2$), maximum available power gain/maximum stable gain (MAG/MSG) and unilateral power gain (U) curves of a $2 \times 100 \mu\text{m}$ device biased at $V_G = -0.5 \text{ V}$ and $V_{DS} = 8 \text{ V}$.

Devices of other gate widths were also measured to demonstrate the relatively good uniformity of the process technology. For example, the device results for a $60 \mu\text{m}$ and a $40 \mu\text{m}$ gate width device are shown in Figs. 4.7 and 4.8, respectively. It can be observed that the measured drain current at $V_G = 0.6 \text{ V}$, the maximum transconductance and the gate-drain breakdown voltage are about 435 mA/mm , 400 mS/mm and -18 V , respectively and are close to each other. These values are also comparable to the performance of the $2 \times 100 \mu\text{m}$ device shown in Fig. 4.2. It can also be seen from Fig. 4.8(a) that the $40 \mu\text{m}$ gate width device has been biased up to $V_{DS} = 10 \text{ V}$ demonstrating that the device is suitable for high drain bias applications.

Therefore, the device results have shown that the process technology that has been developed for the fabrication of PHEMTs using a double-heterojunction epitaxial layer structure together with the double-recess technique is relatively robust, yields good uniformity, and is suitable for use in power applications.

(a)

(b)

(c)

Fig. 4.7. DC performance of a 60 μm gate width device. (a) I_{DS} - V_{DS} characteristics, (b) Transfer characteristics, and (c) Gate-drain breakdown voltage.

(a)

(b)

(c)

Fig. 4.8. DC performance of a 40 μm gate width device. (a) I_{DS} - V_{DS} characteristics, (b) Transfer characteristics, and (c) Gate-drain breakdown voltage.

The performance of the DR-PHEMTs fabricated in this work was also compared with the technology (for the same gate length) offered by two commercial foundries, namely TriQuint Semiconductors of the USA [1] and United Monolithic Semiconductors (UMS) of France [2]. As seen from Table 4.1, the performance of the device fabricated in this work is generally comparable to those that are being offered commercially. For example, the I_{dss} of the NTU device falls between that of the TriQuint Semiconductor and UMS PHEMT while its BV_{DG} is nearer to that of the TriQuint Semiconductor device. However, it was also observed that the f_T of the NTU PHEMT is the lowest among the three technologies. This could be attributed to a higher device C_{gs} and C_{gd} due to the epitaxial layer structure design, as can be seen from (2.16). A lower C_{gs} and C_{gd} can be obtained by increasing the thickness d of the doped barrier AlGaAs layer, as shown in (2.11) and (2.12) respectively. This can

result in a higher device f_T . However, by doing so, the device gain is degraded at the same time, as seen from (2.15). In the design of the epitaxial layer structure, trade-offs are usually made between conflicting device performance requirements. Therefore, the selection of an appropriate device technology for specific circuit applications is a consideration that requires careful and extensive evaluation. This comparison of the NTU device technology with the ones offered by commercial foundries has nevertheless provided for a good initial performance benchmarking exercise. The availability of the device reliability data and qualification test results will further make it more complete, meaningful and fair.

Table 4.1. Comparison of device performance fabricated in this work with the technology offered by two commercial foundries.

	TriQuint Semiconductor (USA)	United Monolithic Semiconductors (France)	This Work (NTU)
Process name	0.25- μ m Ku pHEMT 2MI	PPH25	-
Gate length (μ m)	0.25	0.25	0.25
I_{dss} (mA/mm)	300	200	250
I_{max} (mA/mm)	470	450	430
$g_{m,peak}$ (mS/mm)	400	450	400
BV_{DG} (V)	18	>12	18
f_T (GHz)	65	50	40
Online source	http://www.triquint.com	http://ums.openkast.com/ums/home/home_page.php	-

The photograph of a 10x100 μm device is shown in Fig. 4.9. The I_{DS} - V_{DS} characteristics shown in Fig. 4.10 indicate that the device exhibited an I_{DS} of 450 mA at $V_G = 0.6$ V. The current was observed to drop at higher gate voltages due to self-heating effect and the poor thermal conductivity of the GaAs substrate. It was observed that due to the much larger size of the device in Fig. 4.10 (gate width = 1000 μm), its self-heating effect is more severe compared to the one shown in Fig. 4.8 whose gate width is only 40 μm . The significant self-heating effect in the larger device can be attributed to a higher drain current. For example, at a bias of $V_{DS} = 5$ V and $V_G = 0.6$ V, the absolute drain current flowing through the channel is about 10.4 mA and 300 mA for the devices shown in Figs. 4.8 and 4.10, respectively. The difference is about 29 times.

The microwave output power of the 10x100 μm device shown in Fig. 4.9 was measured on-wafer using an ATN automatic load-pull system at 10 GHz. Biasing the device at $V_G = -0.5$ V and $V_{DS} = 8$ V with $I_{DS} = 176$ mA, the values of the saturated output power, gain, and PAE were about 27 dBm (0.55 W), 8 dB and 48%, respectively as shown in Fig. 4.11. Since the device has a gate width of 1 mm, a P_{sat} of 0.55 W/mm was determined. The device was biased at a maximum drain voltage of 8 V as this value was about half that of BV_{GD} . Table 4.2 summarizes the device performance at both the 1 dB and 3 dB compression points. From Fig. 4.12, the f_T and f_{max} value at this bias condition was approximately 35 GHz and 80 GHz, respectively. For power transistors, f_T and f_{max} should be at least 1-1.5 and 2-3 times respectively that of the maximum operating frequency [7]-[9]. Using this as a guide, the device is therefore capable of being used up to about 25 GHz.

To understand the dependence of the device output power on the drain bias, load-pull measurements were also made at $V_{DS} = 6$ V and 7 V while maintaining V_G at -0.5 V. The results are shown in Fig. 4.13. A summary of comparison of the device load-pull performance at $V_{DS} = 6$ V, 7 V, and 8 V is tabulated in Table 4.3. It could be observed that as the drain voltage was increased from 6 V to 8 V, the output power and PAE at 1 dB compression point improved by about 2.2 dB and 8%, respectively. PAE has become better as the rate of increment in the device output power was higher than the dc power consumption. There was a slight drop in the gain probably due to the increased heat dissipation in the transistor when the dc drain bias was raised.

Fig. 4.9. Microscope photograph of a 10x100 μm device with a total gate width of 1 mm.

Fig. 4.10. I_{DS} - V_{DS} characteristics of a 10x100 μm device biased at $-1.8 \text{ V} < V_G < 0.6 \text{ V}$ and $0 \text{ V} < V_{DS} < 6 \text{ V}$.

Fig. 4.11. Load-pull results of a 10x100 μm device at 10 GHz.

Table 4.2. Summary of load-pull results of the 10x100 μm device at 10 GHz. The bias conditions were: $V_G = -0.5 \text{ V}$, $V_{DS} = 8 \text{ V}$, and $I_{DS} = 176 \text{ mA}$.

	@ 1 dB compression	@ 3 dB compression
P_{out} (dBm)	25.733	27.365
$Gain$(dBm)	10.212	8.178
PAE (%)	28.074	48.99

Fig. 4.12. f_T and f_{max} curves for 10x100 μm device biased at $V_G = -0.5$ V and $V_{DS} = 8$ V.

SG:SEL:NS:1;R:1;IC:500HM;IDOT:PIN;ISTB:A;
 LG:SEL:NS:1;R:1;OC:S#:622;ODOT:POUT;OSTB:A;
 Power Out vs Power In

Frequency (f0): 10 GHz
 Source State: 1 #436
 Source Gamma: .02 178.2
 Bias# 1
 Bias Values Read:
 Vg:-.500 V, Ig:-.007 mA
 Vd:6.000 V, Id:179.020 mA

Load State: 1 # 622
 Load Gamma: .34 77.5
 Pout @ 1 dB: 23.504
 Gain @ 1 dB: 10.972
 Eff @ 1 dB: 20.07
 Pout @ 3 dB: 25.459
 Gain @ 3 dB: 8.951
 Eff @ 3 dB: 35.754
 □ P(Out) (dBm)
 × Efficiency Pwr Added (%)
 + Gain (dB)

(a)

SG:SEL:NS:1;R:1;IC:500HM;IDOT:PIN;ISTB:A;
 LG:SEL:NS:1;R:1;OC:S#:546;ODOT:POUT;OSTB:A;
 Power Out vs Power In

Frequency (f0): 10 GHz
 Source State: 1 #436
 Source Gamma: .02 178.2
 Bias# 1
 Bias Values Read:
 Vg:-.500 V, Ig:-.009 mA
 Vd:7.000 V, Id:178.100 mA

Load State: 1 # 546
 Load Gamma: .42 79.5
 Pout @ 1 dB: 24.22
 Gain @ 1 dB: 10.717
 Eff @ 1 dB: 21.056
 Pout @ 3 dB: 26.255
 Gain @ 3 dB: 8.698
 Eff @ 3 dB: 39.379
 □ P(Out) (dBm)
 × Efficiency Pwr Added (%)
 + Gain (dB)

(b)

Fig. 4.13. Load-pull results at 10 GHz of the 10x100 μm device biased at $V_G = -0.5$ V, $I_{DS} \sim 179$ mA, and (a) $V_{DS} = 6$ V, (b) $V_{DS} = 7$ V.

Table 4.3. Comparison of the device load-pull performance (@ 1 dB compression point) at 10 GHz for $V_{DS} = 6$ V, 7 V and 8 V. The other bias conditions are $V_G = -0.5$ V and $I_{DS} \sim 178$ mA.

	V_{DS} (V)		
	6	7	8
P_{out} (dBm)	23.504	24.22	25.733
$Gain$ (dBm)	10.972	10.717	10.212
PAE (%)	20.07	21.056	28.074

4.3 Scaling Effect Studies

In this section, the effect of device scaling on the output power, gain and PAE of unthinned DR-PHEMTs was studied for its use in coplanar waveguide (CPW) MMIC design. The use of the CPW configuration in power MMIC design is not as popular as the microstrip version due to its poorer heat dissipation capability. The absence of via holes and substrate thinning in CPW circuits has resulted in ineffective heat removal, especially on low thermal conductivity GaAs substrate [10]. However, the CPW technology offers other advantages and can be a cost effective solution for the fabrication of MMICs. Compared to microstrip technology, CPW designs exhibit a lower dispersion characteristic, relatively small discontinuity parasitics, and reduced coupling effects between transmission lines due to better confinement of the electric and magnetic field. In addition, with the availability of modern packaging technologies like flip-chip and thermal bumps, heat removal from the active elements on CPW circuits can be improved significantly while enjoying the yield and cost benefits of doing away with the backend process steps of substrate thinning and via-hole fabrication [10]-[13]. These two process steps could result in relatively substantial yield loss in microstrip circuits.

The performance of a 10x100 μm device has been described in section 4.2. Devices with other gate widths were also characterized at 10 GHz and the results for the output power (P_{1dB}), gain (G_{1dB}) and PAE (PAE_{1dB}) at the 1 dB compression point are shown in Figs. 4.14, 4.15, and 4.16, respectively. It can be seen from Fig. 4.14 that the device output power increased linearly with the device gate width (W_g) from 200 μm to 1000 μm with at least two distinct slopes for each fixed drain voltage. For W_g between 200 μm and 320 μm , the rate of output power increase is about the same for both $V_{DS} = 6\text{ V}$ and $V_{DS} = 8\text{ V}$. For $W_g > 320\text{ }\mu\text{m}$, the slope becomes less steep indicating that the rate of power increase slows down for bigger devices. This could be due to the increased heat that is dissipated within per unit area of the device active region as the gate width is increased. For $W_g > 320\text{ }\mu\text{m}$, the device output power doubles (increase of 3 dB) for every additional 270 μm and 370 μm of gate periphery at 8 V and 6 V of drain bias, respectively. A similar trend was observed in Fig. 4.15 although in this case, the device gain degrades at an approximate rate of 0.002-0.004 dB per μm increase in gate width. It is usual that the device gain degrades as its gate width is increased. This is due to an increase in the gate resistance and the mismatch that results from the phase difference caused by the distributed line effect of the drain and gate interconnects during microwave frequency measurement [14]. From Fig. 4.16, it was observed that for devices with a gate width approximately smaller than 550 μm , the device PAE was better when it is biased at a lower drain voltage of 6 V. This can be explained as follows. As shown in Fig. 4.14, for devices with $W_g < 550\text{ }\mu\text{m}$, the device output power (P_{1dB}) at $V_{DS} = 8\text{ V}$ is not significantly higher than the one at $V_{DS} = 6\text{ V}$. From the corresponding PAE curve in Fig. 4.16, it can be explained that the lower PAE measured for the device biased at $V_{DS} = 8\text{ V}$ is due to the higher device dc power (approximately given by $V_{DS} \times I_{DS}$) compared to the increased output

power when the gate width is increased. This can be seen from the definition for PAE in (2.18). Beyond $W_g = 550 \mu\text{m}$, the device output power increased at a faster rate at $V_{DS} = 8 \text{ V}$ than at $V_{DS} = 6 \text{ V}$ when the gate width is increased. This could be seen from the increasing difference in the device output power between $V_{DS} = 6 \text{ V}$ and $V_{DS} = 8 \text{ V}$ and the steeper slope of the P_{1dB} curve at $V_{DS} = 8 \text{ V}$ in Fig. 4.14. At the same time, as the device gets larger, the thermal self-heating effect becomes more pronounced. This means that the device drain current could be smaller at $V_{DS} = 8 \text{ V}$ than at $V_{DS} = 6 \text{ V}$ resulting in a smaller device dc power at $V_{DS} = 8 \text{ V}$. These two effects of an increasing device output power and decreasing dc power reinforced each other leading to a higher PAE at $V_{DS} = 8 \text{ V}$ for $W_g > 550 \mu\text{m}$.

Fig. 4.14. Device output power scaling at 10 GHz.

Fig. 4.15. Device gain scaling at 10 GHz.

Fig. 4.16. Device PAE scaling at 10 GHz.

4.4 Summary

In this chapter, the performance characteristics of DR-PHEMTs fabricated in this study have been presented. DC and rf measurements were carried out on devices with gate width ranging from 40 μm to 1000 μm . The microwave load-pull performance of two devices with a gate width of 200 μm and 1000 μm was characterized at 10 GHz at different bias conditions. The typical measured DR-PHEMT drain current at $V_G = 0.6$ V, the maximum transconductance and the gate-drain breakdown voltage are about 435 mA/mm, 400 mS/mm and -18 V, respectively. For a 10x100 μm device, it exhibited an I_{DS} of 450 mA at $V_G = 0.6$ V. When this device was biased at $V_G = -0.5$ V and $V_{DS} = 8$ V with $I_{DS} = 176$ mA, the saturated output power, gain, and PAE was about 27 dBm (0.55 W), 8 dB and 48%, respectively at 10 GHz. Since the device has a gate width of 1 mm, a P_{sat} of 0.55 W/mm was determined. Correspondingly, the f_T and f_{max} value at this bias condition was approximately 35 GHz and 80 GHz, respectively. This demonstrates that the technology that has been developed for the fabrication of PHEMTs using a double-heterojunction epitaxial layer structure together with the double-recess technique is suitable for use in power applications up to about 25 GHz.

Devices with different gate widths were also characterized at 10 GHz and the output power, gain and PAE at the 1 dB compression points were measured. It was observed that the relationship between the device output power, gain and PAE is linear. This information is useful to CPW circuit designers as a linear relationship enables a more direct extrapolation of device performance at different gate width.

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Chapter 5

Investigation of Drain Current Transient in BCB- and SiN-Passivated PHEMTs

5.1 Introduction

PHEMTs are devices whose surface passivation plays an important role in their electrical properties. Other than providing protection from harsh environmental conditions, the passivation film also reduces the adverse effect of surface states or surface traps as they are also commonly known. However, the exact mechanism by which passivation achieved that is generally not well understood [1]. BCB is increasingly being used as a passivation material for III-V PHEMTs. Compared to the more commonly used silicon nitride (SiN) deposited by plasma enhanced chemical vapor deposition (PECVD), BCB has several advantages. These include a lower dielectric constant (2.65), lower dissipation factor (0.0008) and easier processing requirement. A comparison of the physical properties of BCB and PECVD SiN is shown in Table 5.1. These attractive material properties of BCB have been shown to improve device and circuit performance when compared to using PECVD SiN as passivation material [2]-[4]. However, it is not clear if this improvement is attributed to a reduction in the density of surface states after BCB passivation or reduced parasitics due to its lower k . Considering that the k value of BCB is almost half that of

SiN, the relative magnitude of improvement in the microwave performance of reported works [2], [3], [5] could have been compromised by the effect of surface states. Surface states are commonly identified using gate lag measurements [6]-[10]. Gate lag is a well-known phenomenon where the drain current comes on only partially and then slowly increases toward the steady state value when the transistor is turned on by the sudden application of a gate pulse. Gate lag can result in pulse narrowing and the eventual loss of transmitted pulses in digital circuits while degrading rf output power in analog circuits [9]-[11]. In this work, the drain current transient resulting from gate lag in BCB-passivated PHEMTs has been investigated. For reference purpose, the data for SiN-passivated devices was also included.

5.2 BCB Passivation of AlGaAs/InGaAs PHEMTs

The fabrication of the BCB-passivated devices was the same as that for the SiN-passivated PHEMTs up to the surface passivation process step. In summary, it began with mesa isolation using a sulfuric acid-based etchant followed by the formation of source-drain ohmic contacts using Ni/Ge/Au annealed at 410°C. The 0.25 μm T-gate was then fabricated using a bilayer P(MMA-MAA) electron beam resist scheme and the gate metal was deposited using evaporated Ti/Au (50 nm/350 nm). For BCB-passivation, the devices were spin coated with the polymer and then cured using a hotplate purged with a constant nitrogen flow. The thickness of the BCB passivation film was about 2.6 μm . Probe pad openings were etched using reactive ion etching. It could be seen from here that the BCB deposition procedure was much simpler. The epitaxial layer structure and cross section view of the BCB-

passivated PHEMT is shown in Fig. 5.1. For the PECVD SiN-passivated PHEMT, the film was 120 nm thick.

Table 5.1. Summary of material properties of BCB and PECVD SiN.

Material	BCB	SiN
Dielectric constant	2.65	6-9
Deposition technique	Spinning	PECVD
Curing or deposition temperature	< 300°C	250°C - 350°C

Fig. 5.1. Cross section view of a BCB-passivated PHEMT. The epitaxial layer structure is the same as that of the SiN-passivated device (dimension not to scale).

5.3 Experiments and Discussion

5.3.1 DC Measurement of BCB-Passivated PHEMTs

To evaluate the effect of BCB passivation on device characteristics, dc measurements were made on unpassivated and BCB-passivated devices. Compared to the unpassivated device, the peak transconductance ($g_{m(peak)}$) of the BCB-passivated transistor is slightly higher (about 5%), as shown in Fig. 5.2. We also observed a slight improvement in the maximum drain current (I_{max}) and two-terminal gate-drain breakdown voltage of the BCB-passivated device as shown in Figs. 5.3 and 5.4 respectively. A summary of comparison of the dc performance of an unpassivated and BCB-passivated device is shown in Table 5.2. These measured parameters demonstrate that there have been no significant differences in the device dc performance after BCB passivation.

Fig. 5.2. Transfer characteristics for an unpassivated and BCB-passivated device at $V_{DS} = 1$ V.

Fig. 5.3. Drain current characteristics for an unpassivated and BCB-passivated for $1\text{ V} < V_{DS} < 5\text{ V}$ and $-1.2\text{ V} < V_{GS} < 0.8\text{ V}$.

Fig. 5.4. Gate-drain breakdown voltage comparison for an unpassivated and BCB-passivated device.

Table 5.2. Summary of dc performance of unpassivated and BCB-passivated device.

Parameter	Unpassivated	BCB-passivated
I_{max} (mA/mm)	448	478
BV_{GD} (V)	-18.3	-19.8
$g_{m(peak)}$ (mS/mm)	387	405
V_{th} (V)	-0.63	-0.64

5.3.2 Gate Lag Transient Investigation of BCB- and SiN-Passivated PHEMTs

It is generally believed that drain transient is caused by surface states at the ungated region between the gate and source/drain contacts. These states can behave as “virtual gates” and modulate the width of the depletion region underneath through changes in the surface density of the negatively charged traps. When the gate bias is changed abruptly, the virtual gates respond according to the characteristic carrier capture and emission times leading to a delay in the switching of the drain current [11].

A common and effective tool used in the characterization of surface traps, also known as deep levels, is the deep level transient spectroscopy (DLTS). It is a technique that gives information about the activation energy, capture cross section and density of traps in semiconductors [12]. In the characterization of n-channel FETs using DLTS, it is common to detect signals that correspond to the emission of holes although the major source of channel carriers is electrons. These signals are also popularly known as “hole-like” peaks, whose physical origin is still debatable since its first observation about 20 years ago [12]-[14]. There are generally two proposed mechanisms on the source of the DLTS hole-like peaks and how the surface traps are responsible for the observed drain transient phenomenon [11], [14]. The first explanation suggests the tunneling and leaking of electrons from the gate edges to the surface states located between the gate and source/drain contacts. The electrons that were laterally injected from the gate drift toward the ohmic source and drain terminals through the repetitive trapping and detrapping of electrons. In this scenario, the DLTS hole-like peaks can be attributed to an increase in the surface density of the trapped

electrons (equivalent to an emission of holes from the traps) resulting from an increase in the reverse bias of the gate-source Schottky contact [12]-[15]. The second explanation results from the numerical calculation of gate lag effects in GaAs MESFETs [8], [16] and the experimental characterizations and numerical simulations of gate lag effects in AlGaAs/GaAs heterostructure FETs [11]. These works described the surface states behaving as hole traps and interact with the holes that were attracted at the ungated surface due to the negatively trapped charge [8]-[11]. The delayed turning-on of the device drain current following the sudden application of a gate bias is then attributed to hole capture by the surface states. Detailed investigations based on experimental and numerical simulation studies have confirmed the acceptor-like nature of the surface traps and the results are in agreement with previous works [8], [11], [12], [15], [16]. With this explanation, the hole-like DLTS peaks are interpreted as actual hole signals [14].

In this work, the drain current transient of SiN- and BCB-passivated PHEMTs has been investigated by means of gate lag characterizations. During measurement, the gate was stepped from -1.8 V (off-state) to 0 V at each fixed drain bias from 1 V to 4 V in a 1 V step. The measured drain current was normalized with respect to the saturated drain current value at steady state ($I_{D(on)}$) and the results are shown in Fig 5.5. The schematic of the measurement setup is shown in Fig. 5.6. The equipments used were HP 85124A K49 pulse generators and HP11612B K61/K62 bias T networks controlled by HP ICCAP. From Fig. 5.5, it was seen that gate lag diminished as the drain voltage was increased. This is due to the generation of holes at higher drain voltages which are then captured by the surface states leading to a thinner

surface depletion region during off-state [11], [17]. It was observed that the normalized drain current of the BCB-passivated device was higher than the unpassivated device at the same drain bias. This demonstrated that BCB has been effective as a passivation material. The SiN-passivated device has the highest normalized drain current value indicating that BCB could be less effective when compared to SiN as seen from its transient drain response. Thus, the potential merit of a lower k in translating into a higher microwave output power for a BCB-passivated device could be compromised by its gate lag performance.

The choice of an appropriate passivation material is also important in applications such as switching where the device could be turned on and off repeatedly with a short duty cycle. A larger magnitude of gate lag could lead to functional errors [9], [17].

Fig. 5.5. Drain current transient for an unpassivated, SiN- and BCB-passivated device at different drain voltages.

Fig. 5.6. Schematic setup used in the gate lag measurement.

5.3.3 Model for Surface Density of States

Extracting the normalized drain current curves for $V_{DS} = 1\text{ V}$ in Fig. 5.5 and re-plotting them in Figs. 5.7(a) and (b) for the unpassivated and BCB-passivated device respectively, it is apparent there were at least three distinct linear slopes (slope 1, slope 2 and slope 3) indicating the existence of three traps with different time constants [18]. For the SiN-passivated device, however, there were only at least 2 linear distinct slopes as shown in Fig. 5.7(c). To further compare the effect of SiN- and BCB-passivation on the density of surface states of the devices, we adopt the surface trap model to investigate this phenomenon. Assuming the presence of i kinds of traps (three for the unpassivated and BCB-passivated device and two for the SiN-

passivated device), the surface potential of the AlGaAs semiconductor surface has been shown by Kohno and co-workers [10] as

$$V_s(t) = V_{bi} - \left[\frac{\Delta Q_{ss1}(t) + \Delta Q_{ss2}(t) + \dots + \Delta Q_{ssi}(t)}{\sqrt{2 \cdot \epsilon_s \cdot \frac{N_D}{q}}} + \sqrt{V_{bi}} \right]^2 \quad (5.1)$$

$$\text{with } \Delta Q_{ssi}(t) = Q_{ssi_0} \cdot \exp\left[-\frac{t}{\tau_i}\right] \quad (5.2)$$

where

$V_s(t)$	surface potential of the ungated AlGaAs surface;
V_{bi}	built-in voltage of the Schottky contact;
$\Delta Q_{ssi}(t)$	charges captured by i th trap at time t ;
ϵ_s	permittivity of AlGaAs;
N_D	effective electron density;
q	electronic charge;
Q_{ssi_0}	charges captured by the i th trap at time 0; and
τ_i	time constant for trap i .

As for the instantaneous drain current, it is related to the surface potential by

$$I_D(t) = g_m \cdot V_s(t) + I_{DSS}. \quad (5.3)$$

The values of the electronic charge q and the dielectric constant of AlGaAs are 1.6×10^{-19} C and 12.4, respectively [19], [20]. The effective electron density N_D of

$8 \times 10^{17} \text{ cm}^{-3}$ has been obtained using the effective sheet carrier density in the quality test report provided by the epiwafer vendor. The value of the built-in voltage of the gate-semiconductor Schottky contact used is 0.7 V [21]. Using (5.1), (5.2), and (5.3), the time dependence of the normalized transient drain current for $V_{DS} = 1 \text{ V}$ was calculated and shown along with the corresponding measured data in Fig. 5.8. The values of Q_{ssi_0} and τ_i for the i th trap were obtained by fitting the calculations to the measured data curves and are shown in Table 5.3. It can be seen from Fig. 5.8 that the calculated values matched the measured experimental data reasonably well.

(a)

(b)

(c)

Fig. 5.7. Demonstration of existence of at least three different time constants for (a) Unpassivated device, (b) BCB-passivated device, and (c) SiN-passivated device.

Fig. 5.8. Comparison of measured data with model for unpassivated, SiN- and BCB-passivated device.

Table 5.3. Parameters used in the theoretical calculations of the normalized transient drain current shown in Fig. 5.8.

Device	τ_1 (ms)	$Q_{ss1,0}$ (10^{11} cm^{-2})	τ_2 (ms)	$Q_{ss2,0}$ (10^{11} cm^{-2})	τ_3 (ms)	$Q_{ss3,0}$ (10^{11} cm^{-2})
Unpassivated	0.0037	2.7	0.3	3.0	6.5	2.1
BCB-passivated	0.0053	3.3	0.1	0.7	7.0	1.1
SiN-passivated	0.003	2.38	0.1– 0.3	~0	170	1.75

From Table 5.3, the data shows that with reference to an unpassivated surface, BCB has effectively reduced the density of surface states with time constant τ_2 (0.1–0.3 ms) and τ_3 (6.5–7.0 ms) by about 75% and 50% respectively. For traps with a shorter time constant of τ_1 (0.0037–0.0053 ms), the number of charges has remained almost unchanged. Comparing the effect of BCB with SiN, it was seen that SiN has almost completely reduced surface states with time constant in the τ_2 range (0.1–0.3 ms) to zero. This accounts for the two distinct time constants for SiN. The SiN-passivated surface has a shorter τ_1 but much longer τ_3 when compared to the BCB-passivated device. The longer τ_3 can be seen from the relatively flatter slope (slope 3) of the SiN device. A flatter slope 3 means that the SiN-passivated drain transient current becomes steady more quickly after the gate pulse is turned on.

5.4 Summary

An experimental investigation into the drain current transient in $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ PHEMTs passivated by low- k BCB has been presented. It was found that BCB reduces the density of surface states after passivation. When compared to the SiN-passivated PHEMT, the BCB-passivated device however demonstrated a larger magnitude of gate lag with its transient drain current rising to a lower value in the same time period after the gate voltage is turned on. Therefore, although BCB has a dielectric constant that is almost half that of SiN, its slower gate lag response could limit its potential for passivation use in III-V PHEMTs. It is also suggested that in the selection of a passivation material for a specific circuit application, it could be useful to take into consideration its gate lag performance as well.

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Chapter 6

Investigation of Hot Carrier Induced Degradation in BCB- and SiN-Passivated Power PHEMTs

6.1 Introduction

One of the most important considerations when using DR-PHEMTs in power applications is their reliability when operated under a high drain bias. Due to the large electric field present in the device channel, a major concern is the generation of hot electrons (HEs) and impact ionization (II) conditions. The use of a low bandgap InGaAs channel in AlGaAs/GaAs PHEMTs further makes the occurrence of II even more favorable. As the gate length shrinks further for the device to operate at even higher frequencies, HEs and II have become crucial issues that device and circuit designers must take into account to ensure proper and long life operation of the circuits in which the devices are used.

For many years, reliability workers have focused their effort on high-temperature storage or temperature-accelerated stress tests. These mainly investigate failure mechanisms that are thermally activated, such as the ohmic and Schottky contact degradation induced by interdiffusion processes and carrier deconfinement caused by dopant migration at elevated temperatures. It was only recently that

attention was shifted toward experiments conducted at room temperature and at a high drain voltage to study hot-carrier induced degradation in these devices [1], [2].

So far, the reported degradation in the PHEMT dc characteristics after hot electron stress (HES) includes threshold voltage shift, transconductance reduction, maximum drain current compression, and breakdown walkout [3]-[8]. These effects were generally linked to the creation of trap and/or accumulation of charge under the gate or at the semiconductor-passivation interface in the gate-drain region by energetic carriers. As a result, electrons are then trapped by these interface states and into the passivation film leading to drain resistance increase, drain current reduction and breakdown walkout [1], [9]-[18].

In this work, we have conducted HES tests to investigate the hot electron reliability of BCB- and SiN-passivated PHEMTs. Degradation of the device dc characteristics has been compared before and after the stress. The degradation mechanisms involved in the two technologies have also been proposed to explain the experimental data.

6.2 Significance of Off-state and On-state Breakdown

DR-PHEMTs are extensively used in power amplifiers within the transceiver (T/R) modules to deliver a high output power at microwave frequencies. Usually, these devices are biased at a high drain bias (7 V – 10 V). At such biasing conditions, the devices are subjected to a severe hot carrier stress owing to high impact ionization

effects caused by hot electrons [19], [20]. This biasing requirement to produce a high output power demands that PHEMTs have high off-state and on-state breakdown voltages. The consideration of whether the off-state or on-state breakdown voltage is more important depends on the type of circuits and the way the PHEMTs are operated at microwave frequencies. For example, when in operation, the devices might operate in the 3-terminal drain-source breakdown regime during the RF swings. As such, the off-state 3-terminal drain-source breakdown voltage would naturally become an important criterion in the selection of a suitable device [20]. In class AB power amplifier design, devices are biased at a high drain voltage for maximum output power. As such, the device on-state breakdown voltage needs to be high so that it will not be destroyed during the high drain bias operation.

The off-state breakdown voltage is commonly referred to as the maximum drain-source or gate-drain voltage that can be applied to a device when it is biased at or below threshold. In this state, the device is in the off condition and a gate current of 1 mA/mm is frequently used as the criterion for the definition of the breakdown voltage. The dominant physical mechanism that governs the device off-state breakdown is commonly attributed to mechanisms such as surface leakage current, tunneling and thermionic-field emission (TFE) or combinations thereof [2], [21]-[25]. Trew and Mishra proposed that at a large drain bias but a low gate voltage, the device surface electric field can become large enough that electrons tunnel from the gate metal onto the gate-drain region where the electric field is the highest. This form of surface leakage current is strongly dependent on the device surface and is thus sensitive to the fabrication technology [26]. The model further predicts that as the gate

is biased toward pinch-off (off-state), its drain-source breakdown voltage increases in agreement with experimental observation. This is due to a lower junction temperature at pinch-off leading to a smaller TFE-induced surface leakage current which then requires a larger drain-source voltage to sustain a fixed gate current. In their explanation of the off-state breakdown mechanism, Takamiya and co-workers suggested a combination of TFE and tunneling for the reverse gate current and its strong dependence on the Schottky gate barrier height and electric field strength [25]. A recent simulation study by Li and co-workers coupled both TFE and II mechanisms into the generation of the reverse gate current in the explanation of the breakdown phenomenon. It was found that the breakdown voltage is lower when both TFE and II effects were simultaneously included in the analysis due to the presence of a higher reverse gate current compared to accounting for them separately [27]. The surface passivation process, including the type of passivation film used and its deposition conditions, plays an important role in determining the device breakdown voltage as it has been shown to influence the surface potential significantly [28].

The dominant mechanism responsible for the on-state breakdown is believed to occur due to II of the channel hot electrons when the device is turned on and the drain current is flowing [2], [24], [29], [30]. The on-state breakdown voltage is usually defined as a locus in the I_D - V_{DS} characteristics that meets a pre-defined breakdown criterion when the device is biased at a gate voltage above the threshold value [24]. However, the challenge in measuring the on-state breakdown voltage lies in the ambiguity of the definition of the criterion and its measurement technique [30]. Somerville and co-workers proposed a simple and reproducible method called the

gate current extraction technique in 1998 where the breakdown condition can be clearly identified as a locus of a pre-defined constant gate current, for example at 1 mA/mm [24], [31]. The details of this characterization technique are explained further in section 6.2.1.

Impact ionization is inversely proportional to the material bandgap energy and in a PHEMT device, the channel has a lower energy compared to the Schottky layer in order to have good carrier confinement in the potential well. As a result, II occurs most readily in the channel at the drain edge of the gate where the electric field is the highest. The magnitude and distribution of the channel electric field can be varied by changing the lateral and vertical geometry of the PHEMT [32]. In a double-recessed PHEMT, the gate-drain peak electric field is lowered due to an extension of the depletion region between the gate and drain region. This results in a stronger immunity to II and the device breakdown performance improves [33], [34]. The II mechanism can be described as follows. When biased at a sufficiently high drain bias, a channel electron in the conduction band gains enough energy to ‘lift’ an electron from the valence band into the conduction band. In the process, an electron-hole (e-h) pair is created and II is said to have occurred. The holes generated by II are collected at the gate terminal and this excess gate current can impose a limit on the maximum drain bias that can be applied to the device [35]. If the field is high enough, these e-h pairs can trigger further II events leading to a carrier multiplication process. The device finally breaks down when the multiplication process runs away and becomes an avalanche [36].

6.2.1 Breakdown Voltage Characterization Techniques

To investigate the breakdown phenomenon, it is necessary to be able to measure the breakdown voltages accurately. Conventionally, the simplest and the most popular method of defining the off-state gate-drain voltage is by measurement of the 2-terminal gate-drain reverse characteristics while leaving the source terminal floating. The gate-drain breakdown voltage (BV_{GD}) is then defined as the gate-drain voltage yielding a pre-defined value of the reverse gate current. This value is typically 1 mA/mm but it does not necessarily have to be so. However, PHEMTs are 3-terminal devices and in actual operation, all 3 terminals are biased with the source usually grounded. Therefore, a 3-terminal measurement method would probably be more suitable to measure BV_{GD} with the source grounded to simulate the actual operation of the device.

Bahl and co-workers proposed a useful method with their so-called drain-current injection technique (DCIT) [37]. In this method, the device is biased with the source grounded and a fixed predefined current is injected into the drain while the gate source bias is ramped down from zero or forward bias to below threshold. The curves of I_G , V_{DS} , and V_{DG} are then traced as a function of V_G . Fig. 6.1 shows the schematic setup of the measurement of the off-state breakdown voltage using the DCIT. When V_{GS} is high and the device is in the on-state, the drain bias that is required to get the small predefined drain current (usually not exceeding 1 mA/mm) is close to zero. As V_{GS} is decreased toward pinch-off, a larger and larger V_{DS} is now required to drive and maintain the fixed drain current flowing. Correspondingly, V_{DG}

state breakdown voltage (BV_{on}) although it is an important figure of merit for power devices [30]. This has been due mainly to challenges faced in measuring BV_{on} in a reproducible and non-destructive manner. Approaches that have been suggested include considering BV_{on} as a significant upturn in the drain current [38] and using a burnout criterion that involves increasing the drain voltage at a given gate bias until the device is destroyed [39]. However, these methods are destructive and whose definitions can be ambiguous sometimes. A simple and reproducible definition and technique to measure BV_{on} was proposed by Somerville and co-workers using the gate current extraction technique (GCET) [31]. Fig. 6.2 shows the schematic setup of the measurement of the on-state breakdown voltage using the GCET.

Fig. 6.2. Schematic diagram of the GCET for measurement of on-state breakdown voltage.

During the extraction of BV_{on} , I_G is held constant at a pre-defined value such as -1 mA/mm and then I_D is ramped from $|I_G|$ to a fixed on-state drain current value. In doing this, a locus of V_{DS} versus I_D is traced at a constant I_G . This locus is defined

as BV_{on} . This definition is also meaningful and consistent in that BV_{on} converges toward BV_{off} as the device is turned off, i.e. $I_D = 0$.

In this work, we have adopted the DCIT and GCET to measure BV_{off} and BV_{on} , respectively.

6.2.2 Breakdown Walkout

A common observation after biasing the FET under a high electric field and hot carrier conditions is that the device exhibits a permanent increase in the breakdown voltage. This phenomenon is popularly known as breakdown walkout [6], [7], [8], [40], [41]. By itself, breakdown walkout is a beneficial by-product as it means that the device has become more resistant to breaking down when operating under a high voltage bias. However, degradation in the drain current, transconductance and rf gain are other undesirable effects that often accompany breakdown walkout after hot electron stress [28].

It is generally believed that the main degradation mechanism induced by high field bias conditions in FETs is the creation of traps by energetic carriers at the semiconductor-passivation interface at the gate-drain access region. Electrons can then be captured by these interface traps and into the passivation leading to a widening of the depletion region and a reduction of the peak electric field. This leads to drain resistance increase, drain current and gain reduction, as well as breakdown walkout [1], [3], [7], [9], [10]. Chou and Li investigated off-state breakdown walkout

on wafers with different surface preparation conditions and on epitaxial wafers from different vendors [20]. They found that the breakdown walkout has a strong dependence on the wafer surface process conditions and depends to a lesser degree on the starting wafers. The surface passivation process, including the type of passivation material and its deposition conditions, can thus be expected to play a significant role in affecting the breakdown characteristics through its influence on the device surface state density and surface potential [28].

6.3 Device Fabrication and Experimental Setup

The fabrication of the BCB- and SiN-passivated PHEMTs has been described earlier in section 5.2. The SiN film was deposited using PECVD with ammonia and silane gas at 300°C while the BCB film was spin coated and then cured using a hot plate purged with nitrogen gas. The devices were hot electron stressed using an HP4155A semiconductor parameter analyzer together with a CASCADE dc probe station as shown in Fig. 6.3

Fig. 6.3. Hot carrier stress experimental setup using an HP 4155A semiconductor parameter analyzer and CASCADE probe station.

6.4 Hot Electron Stress (HES) Procedure

In order to investigate hot electron (HE)-induced degradation, on-state stress was performed at room temperature at a high dc drain bias. Stressing the device at room temperature presents a more stringent reliability condition compared to stress procedures conducted at higher temperatures. This is because electrons are inhibited from gaining maximum kinetic energy due to enhanced phonon scattering at high temperatures [1]. To compare the effect of hot carrier induced degradation in BCB- and SiN-passivated devices, static IV , g_m , gate leakage current, BV_{off} and BV_{on} were measured before and after HES. In this work, BV_{off} and BV_{on} measurements were defined at a current density of 0.01 mA/mm. This low current value was used to avoid the destructive breakdown of the devices [42].

The HES involves stressing the device close to the peak of the typical bell curve which is at about $V_G = 0$ V. We have chosen a value of 7 V for the drain bias where it was observed that the gate current due to II was sufficient to degrade the device gradually and not catastrophically during the stress duration of 20 continuous hours.

6.5 Effects of HES on dc characteristics of BCB-passivated Device

In this section, the dc performance of the BCB-passivated device before and after HES is presented.

6.5.1 Drain Current

The static I_{DS} - V_{DS} characteristics of the BCB-passivated device before and after HES are shown in Fig. 6.4. No evidence of severe current collapse was seen. It was observed that the knee voltage increased after the stress indicating an increase in the channel resistance. Furthermore, after HES, the drain voltage where the kink occurred before the stress shifted toward higher values and the kink amplitude also decreased due to breakdown walkout.

Fig. 6.4. I_{DS} - V_{DS} comparison of BCB-passivated device before (solid lines) and after (dotted lines) HES.

6.5.2 Transconductance and Subthreshold Characteristics

Fig. 6.5 shows the device transfer characteristics at $V_{DS} = 3$ V before and after HES. The peak transconductance has decreased only slightly from 361.8 mS/mm to 351.3 mS/mm (-2.9%). The gate voltage at the maximum transconductance has remained unchanged at $V_G = -0.24$ V while the threshold voltage has shifted slightly from -0.632 V to -0.641 V (-1.4%). From the subthreshold characteristics shown in Fig. 6.6, it was observed that the subthreshold current has remained almost unchanged after the stress. This indicates that the gate quality has not degraded.

Fig. 6.5. Transfer characteristics comparison of BCB-passivated device before (solid lines) and after (dotted lines) HES.

Fig. 6.6. Subthreshold characteristics of BCB-passivated device before (solid line) and after (dotted line) HES.

6.5.3 Gate Leakage Current

The presence of hot electrons and II at drain voltages exceeding 6 V is evident from the I_G - V_G curve shown in Fig. 6.7. The bell shape behavior of the gate current I_G is due to two dominant competing effects at different ranges of gate bias. When the device is biased at gate voltages close to pinch-off, the number of electrons in the channel is low. Therefore, although the electric field between the gate and drain is high, the relatively few electrons available for II result in a low I_G . As the channel opens wider with the application of a more positive V_G , the drain current and the number of electrons available for II also increases with the latter leading to a higher absolute value of I_G . However, the magnitude of the maximum electric field between the gate and drain (which is proportional to the difference between the gate and drain voltage) starts to decrease after a certain gate voltage value. Correspondingly, $|I_G|$ reaches a maximum value and then starts to decrease. This behavior gives rise to the typical bell shape I_G - V_G curve.

It was observed that the gate current decreased significantly after HES indicating that II or the generation of holes by hot electrons has been reduced due to a decrease in the maximum electric field.

Fig. 6.7. Leakage current comparison of BCB-passivated device before (solid lines) and after (dotted lines) HES.

6.5.4 Off-state and On-state Breakdown Voltage

The HES has resulted in an increase in the off-state and on-state breakdown voltages as shown in Figs. 6.8 and 6.9, respectively. The drain-source off-state breakdown voltage before ($BV_{DS'(off)}$) and after ($BV_{DS''(off)}$) HES is 8.6 V and 9.52 V, respectively. The drain-gate off-state breakdown voltage before ($BV_{DG'(off)}$) and after ($BV_{DG''(off)}$) HES is 9.83 V and 10.76 V, respectively. This is the commonly observed breakdown walkout phenomenon after the devices have been subjected to hot carrier

stress as mentioned in section 6.2.2.

Fig. 6.8. Off-state breakdown voltages of BCB-passivated device before (solid lines) and after (dotted lines) HES.

Fig. 6.9. On-state breakdown voltage of BCB-passivated device before (solid line) and after (dotted line) HES.

The increase in the off-state gate-drain breakdown voltage ($BV_{DG(off)}$) and off-state drain-source breakdown voltage ($BV_{DS(off)}$) was about 10%. For the on-state drain-source breakdown voltage ($BV_{DS(on)}$), it increased from 8.66 V to 9.44 V or 9% after the stress.

6.6 Effects of HES on dc Characteristics of SiN-passivated Device

In this section, the dc performance of the SiN-passivated device before and after HES is presented.

6.6.1 Drain Current

The static I_{DS} - V_{DS} characteristics of the SiN-passivated device before and after HES are shown in Fig. 6.10. Similar to the BCB-passivated device, no evidence of severe current collapse was seen. There has been a slight decrease in the drain current at higher V_G values. Unlike the BCB-passivated device, there was no noticeable change in the knee voltage. The drain voltage where the kink occurs before the stress has also remained about the same after HES. This is consistent with the measurement of a much smaller breakdown walkout as will be shown later.

Fig. 6.10. I_{DS} - V_{DS} comparison of SiN-passivated device before (solid lines) and after (dotted lines) HES.

6.6.2 Transconductance and Subthreshold Characteristics

Fig. 6.11 shows the device transfer characteristics at $V_{DS} = 3$ V before and after HES. The maximum transconductance has decreased only slightly from 332 mS/mm to 326.6 mS/mm working out to a relative reduction of -1.6%. However, the gate voltage where the peak transconductance occurs shifted from -0.15 V to -0.18 V (-20%). The threshold voltage has shifted from -0.737 V to -0.761 V (-3.3%) and the relative change is more than twice that in the BCB-passivated device. It was also observed from Fig. 6.12 that the subthreshold current has increased after the stress

indicating that the Schottky gate contact could have degraded.

Fig. 6.11. Transfer characteristics comparison of SiN-passivated device before (solid lines) and after (dotted lines) HES.

Fig. 6.12. Subthreshold characteristics of SiN-passivated device before (solid lines) and after (dotted lines) HES.

6.6.3 Gate Leakage Current

As shown in Fig. 6.13, the peak gate current has reduced after HES. This is due to a decrease in the maximum electric field in the AlGaAs Schottky layer which could be caused by traps generated in this layer by hot electrons [6].

Fig. 6.13. Leakage current comparison of SiN-passivated device before (solid lines) and after (dotted line) HES.

6.6.4 Off-state and On-state Breakdown Voltages

The walkout in the off-state breakdown voltage was much smaller when compared to the BCB-passivated device after HES. As shown in Fig. 6.14, $BV_{DS'(off)}$ and $BV_{DS''(off)}$ is 8.075 V and 8.1 V, respectively. The change is negligibly small at 0.3%. As for the drain-gate breakdown voltage, $BV_{DG'(off)}$ and $BV_{DG''(off)}$ is 10 V and 10.4 V, respectively. Again, there is almost no change. On the other hand, $BV_{DS(on)}$ increased by 11.3% after the stress as shown in Fig. 6.15. The on-state breakdown is

limited by II in the channel and it has increased due to a smaller magnitude of gate current generated by II after HES in Fig. 6.13. A more detailed discussion on the different magnitude of breakdown voltage walkout in BCB- and SiN-passivated device follows in section 6.7.

Fig. 6.14. Off-state breakdown voltages of SiN-passivated device before (solid lines) and after (dotted lines) HES.

Fig. 6.15. On-state breakdown voltage of SiN-passivated device before (solid line) and after (dotted line) HES.

6.7 Discussion

In this section, we discuss the observed changes in the dc performance characteristics of the BCB- and SiN-passivated devices before and after HES. A summary of the device performance comparison is shown in Table 6.1.

Table 6.1. Summary of comparison of changes in dc performance characteristics of BCB- and SiN-passivated devices before and after HES.

Parameter	BCB-passivated Device			SiN-passivated Device		
	Pre Stress	Post Stress	% change	Pre Stress	Post Stress	% change
$BV_{DS(off)}$ (V)	8.6	9.52	+10.7	8.075	8.1	+0.3
$BV_{DG(off)}$ (V)	9.83	10.76	+9.5	10	10.4	+0.4
$BV_{DS(on)}$ (V)	8.66	9.44	+9	7.72	8.59	+11.3
$g_{m(peak)}$ (mS/mm)	361.8	351.3	-2.9	332	326.6	-1.6
$V_G @ g_{m(peak)}$ (V)	-0.24	-0.24	0	-0.15	-0.18	-20%
V_{th} (V)	-0.632	-0.641	-1.4	-0.737	-0.761	-3.3

It was observed that the BCB-passivated PHEMT demonstrated a much larger breakdown walkout when compared to the SiN-passivated device. The increase in the breakdown voltages (breakdown walkout) is a beneficial effect that manifested after HES. This was believed to be due to the creation of interface states by II leading to a local enhancement of the depletion region and a lower surface potential. A lower surface potential spreads out the longitudinal electric field distribution and reduces the peak electric field between the gate and the drain resulting in a larger breakdown voltage [2], [12]. Our experimental findings here are consistent with those found in [10].

The widening of the depletion width in the BCB-passivated device could be seen from the increase of the knee voltage of the I_{DS} - V_{DS} curve shown in Fig. 6.16(a) for $0 \text{ V} < V_{DS} < 1.6 \text{ V}$. The higher knee voltages measured after HES indicate an increased series channel resistance that is most probably caused by an increased surface state density in the gate-drain access region. The degradation is more noticeable at higher gate bias as the current flows closer to the surface and is thus more sensitive to changes in the surface condition [2]. In the case of the SiN-passivated device shown in Fig. 6.16(b), the knee voltages are almost unchanged after HES indicating that the depletion region has not changed much during the 20-hour stress duration. A longer stress period could be needed to observe a significant breakdown walkout. Therefore, the much larger breakdown walkout measured for BCB-passivated devices is consistent with the observation of a more resistive I_{DS} - V_{DS} linear region after the stress. The mechanism of interface states generation seems to be more dominant in the BCB-passivated device.

(a)

(b)

Fig. 6.16. Comparison of slope in the linear region of the I_{DS} - V_{DS} curve of (a) BCB-passivated and (b) SiN-passivated device before (solid lines) and after (dotted lines) HES.

The threshold voltage (V_{th}) shift of the SiN-passivated device (-3.3%) is more than twice that of the device passivated by BCB (-1.4%). In addition, the magnitude of the gate voltage at which the maximum transconductance occurs ($V_G @ g_{m(peak)}$) has increased significantly by 20%. The entire g_m curve has shifted in the negative direction for the SiN-passivated device while there was no noticeable change for the device passivated with BCB. $V_G @ g_{m(peak)}$ did not change for the BCB-passivated device. The negative V_{th} shift has been reported by different groups after hot electron stressing. It could be due to carrier trapping and/or detrapping. For example, some electrons could be present within the DX centers in the AlGaAs Schottky layer above the InGaAs channel. During HES and II conditions, these electrons within the deep levels could be reduced by some of the generated holes due to II and bound for the gate or by field-enhanced electron detrapping. This reduction of the electron population under the gate causes the threshold voltage to become more negative as a more positive charge under the gate enhances channel electron accumulation [2], [4], [5], [16], [43], [44]. Alternatively, a negative shift in V_{th} could also be caused by the trapping of holes at the interface between the gate and the AlGaAs Schottky layer or in the very thin oxide interface layer which is always present in Schottky contacts [45]. The neutralization of negative charges under the gate leading to a reduction of V_{th} will cause an increase in the drain current. However, we have observed a slight reduction in I_{DS} at higher values of V_G in the SiN-passivated device. This could be due to the saturation of the shift of the g_m curve sometime during the 20-hour stress period, and beyond that, the process of interface state generation in the gate-drain access region takes over and becomes the more dominant mechanism. The latter will result in the reduction of the drain current and breakdown walkout. The breakdown

walkout was much smaller for the SiN-passivated device probably because the interface states were generated much later in the stress duration. The consequence of the negative V_{th} shift of the SiN-passivated device is noticeable from its subthreshold characteristics shown in Fig. 6.12 where the drain current increased after the stress. No noticeable change was observed in the BCB-passivated device where the mechanism of the interface state generation in the gate-drain region probably set in much earlier resulting in a much larger walkout.

The larger V_{th} shift in the SiN-passivated device could be due to the presence of hydrogen during the plasma deposition of the dielectric film [6], [46]. Hydrogen is notoriously known to be a serious reliability concern for compound semiconductor FETs and MMICs. Sources of hydrogen include outgassing by most package materials, plasma etching and PECVD deposition which the SiN growth process makes use of. The deposition of the BCB dielectric film was made by spin coating and then cured using a nitrogen purged hotplate. Therefore, in comparison, the amount of hydrogen that the BCB-passivated device was exposed to is minimal. Although many papers have been written on the effect of hydrogen contamination on GaAs MESFETs, GaAs PHEMTs, and InP HEMTs, results were often mixed and a conclusive interpretation has yet to be reached [47]. For example, I_D and V_{th} have been reported to either decrease or increase depending on test conditions and sample characteristics [48], [49]. Proposed explanations involve the role of atomic H in donor neutralization or surface state passivation that leads eventually to a Schottky barrier shift [48]-[50]. A study by Gaddi and co-workers on AlGaAs/GaAs FETs with Ti-Al gates (i.e. Pt free) attributed the negative shift in V_T by hydrogen to two mechanisms,

namely positive piezoelectric charge accumulation underneath the gate due to the formation of titanium hydride (Ti-H_x) and the neutralization of the negatively charged DX centers in the AlGaAs barrier layer by the atomic H [51]. The exposure of the device to hydrogen, such as during the PECVD growth of SiN, can lead to a reaction between the gas and the Ti metal in the gate forming Ti-H_x which then induces a stress in the gate. This in turn leads to a distribution of the polarization volume charge in the semiconductor underneath through the piezoelectric effect causing a shift in the device threshold voltage [51]-[56]. This degradation mechanism is observed not only in GaAs Ti/Pt/Au-gated PHEMTs but also in devices using Ti-only and Ti-Al gates [51], [54]-[56].

Devices with V_{th} shift could pose particular problems in circuits. For example, an amplifier that was designed with transistors biased to work at a constant gate voltage could show a drastic reduction in gain depending on the magnitude of the shift. Biasing the transistors to operate in a constant current mode might be a solution as long as the V_G shift is predictable and is taken into consideration during the design phase. However, such an approach often results in increased hardware requirement and complexity, cost and reduced system reliability [57]. From the technology point of view, it is therefore important to minimize the V_{th} shift through proper device design and process optimizations.

In order to get a more accurate picture of how the two degradation mechanisms interact with each other during the period of the HES, it is necessary to do more work to identify the origin and location of the traps and the mechanisms that

are responsible for their generation. In addition, it would be useful to sample the dc characteristics on a smaller time interval like 1 hour and at the same time extending the stress duration to satisfy a pre-defined failure criterion. A 20% reduction in I_{DSS} is a commonly used performance parameter failure criterion. In this way, the dominant mechanism at work during a specific time frame could be more closely monitored and understood. Our findings and recommendations are similar to those in [58] where Cova and co-workers proposed that hot carrier stress experiments be performed with special consideration of the stress bias and time duration. This is because different conditions could yield different device characteristics after the stress. In this work, we believe that the duration of 20 hours is sufficient to help us determine initially the main mechanism at work on a macroscopic level. Having understood this, the stress time could then be extended and device characteristics data sampled on a smaller time interval like that just suggested.

Lastly, it is important to note that device degradation and degradation mechanisms are strongly dependent on the technology and process conditions as has been demonstrated by Canali, Meneghesso, and co-workers in their assessment of the degradation and mechanisms involved in the hot carrier stressing of PHEMTs from different suppliers [4], [44]. As such, a crucial and important area that could be optimized to improve the hot electron robustness of devices is in the process technology. This includes critical steps such as the ohmic and Schottky contact deposition, gate recess and surface passivation.

6.8 Summary

Hot carrier stress has been performed on BCB- and SiN-passivated devices at room temperature to investigate the device dc degradation. It has been found that the dominant degradation mechanism is different for the two technologies. In the case of the BCB-passivated device, the dominant mechanism appears to be due to the trapping of hot electrons in states within the BCB film and/or at the interface between the semiconductor and BCB at the gate-drain access region. The accumulation of the negative charge between the gate and drain widens the surface depletion and results in a significant increase of the breakdown voltages. During the 20-hour stress duration, the drain current has only changed slightly and the g_m curve has not shifted noticeably. Although a larger breakdown voltage can be considered beneficial by itself, it is important to note that electron trapping in the gate-drain region could result in a worse gate lag behavior as mentioned in chapter 5 resulting in a reduced microwave output power.

For the SiN-passivated device, the dominant mechanism could be due to trapping of holes in the AlGaAs layer underneath the gate and in the very thin oxide interface layer between the gate metal and AlGaAs semiconductor surface. This results in a negative shift of V_{th} that is almost twice that of the BCB-passivated device. The shift in V_{th} could result in improvement or degradation in the circuit performance. Either way, it is not desirable. The breakdown walkout is insignificant compared to the BCB-passivated device leading to the proposition that electron trapping in the semiconductor-SiN interface or in the gate-drain access region could be trivial during the 20-hour stress period.

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Chapter 7

Applications of DR-PHEMTs in Power MMICs

7.1 Introduction

DR-PHEMTs are frequently used in the design of power amplifier MMICs [1]-[8]. In this work, a 6-18 GHz broadband and Ku-band power amplifier MMIC has been designed and fabricated. The MMIC technology utilizes the baseline device process where SiN was used as the capacitor dielectric and surface passivation material. The circuit measurement results and challenges faced in the fabrication work are discussed.

7.2 Small-Signal Modeling

The first step in the design was to extract the small-signal equivalent circuit model for a unit cell. The on-wafer load-pull measurements for a 10x100 μm device were reported earlier in section 4.2. In the design of the MMICs, two kinds of unit cell were used. They consist of a 10- and 20- finger device of unit gate width 100 μm giving a total gate periphery of 1 mm and 2 mm, respectively. As the current device mask layout only has the 10x100 μm device, the extracted model for this configuration was scaled for the 20x100 μm device. Fig. 7.1 illustrates the extracted device model for the 10x100 μm device while Fig. 7.2 shows the comparison of its modeled and measured results up to 40 GHz. It could be seen that the results are close to each other.

Fig. 7.1. Small-signal equivalent circuit model for the 10x100 μm device. The biasing conditions were $V_G = -0.5$ V, $V_{DS} = 8$ V, and $I_{DS} = 177$ mA.

The small signal equivalent circuit model for the 20x100 μm unit cell device is the same as the one shown in Fig. 7.1 but with different element values. A summary of comparison of the element values for the 10x100 μm and 20x100 μm device model is shown in Table 7.1.

Fig. 7.2. Comparison of the modeled (blue) and measured (red) results of the 10x100 μm device. The biasing conditions were $V_G = -0.5$ V, $V_{DS} = 8$ V, and $I_{DS} = 177$ mA.

Table 7.1. Summary of element values of small signal equivalent circuit for the 10x100 μm and 20x100 μm device.

Element Value	10x100 μm Device	20x100 μm Device
L_s (pH)	0.6	0.6
L_d (pH)	12	6
L_g (pH)	7.1	3.6
R_s (Ω)	0.6	0.6
R_d (Ω)	3.6	1.8
R_g (Ω)	0.6	0.3
R_{ds} (Ω)	115	57
R_{in} (Ω)	1.8	0.9
C_{gd} (fF)	27	54
C_{gs} (pF)	1.255	2.51
C_{ds} (fF)	205.5	411

7.3 Broadband Power Amplifier MMIC

In this section, we study the design, simulation and measurement results of the broadband PHEMT power amplifier MMIC. The target was to design a broadband power amplifier operating over 6-18 GHz with an output power of about 1.5 W at 1 dB compression point.

7.3.1 Design and Simulated Results

The layout of the C-X-Ku band power amplifier shown in Fig. 7.3 has a two-channel design with integrated Lange couplers to operate in a balanced configuration. The output stage was broadband-matched to the optimum load point across the C-X-Ku band while the inter-stage and input-stage were designed to level the small-signal gain. Return losses for each channel were not optimized as they were to operate in a balanced configuration. CPW configuration was used to implement the transmission line structures as it eliminates the need for via-hole etching and substrate thinning.

The design of the power amplifier first made use of the wafer load-pull results measured on an actual device and the subsequent extraction of the small-signal model. Based on the performance of the $10 \times 100 \mu\text{m}$ device, it was estimated that each channel of the power amplifier will require 4 mm of output periphery and two channels would have a total of 8 mm of output gate periphery. From Table 4.2, the measured power density of the $10 \times 100 \mu\text{m}$ devices at 1 dB gain compression point was 25.733 dBm/mm or 0.37 W/mm. 8 mm of total gate width will theoretically give 2.97 W. However, the actual output power will be less than this as it did not account for the (a) losses due to mismatch from the optimum load point across frequencies, (b) losses due to phase/amplitude variation and ohmic losses within a bigger unit cell, and (c) losses in the combined structure of the unit cells. After accounting for all these losses, the estimated output power would be between 1.5-2W.

Fig. 7.3. Layout of the C-X-Ku band power amplifier.

Each channel of the power amplifier used two 20x100 μm unit cells to achieve the 4 mm gate periphery. A 2:1 device driving ratio was selected for the three stages. The final device line-up for each channel of the power amplifier used a 10x100 μm device and three 20x100 μm devices. Since the unit cell measured in Fig. 4.11 was a 10x100 μm device, the optimum load point was used to scale for the 20x100 μm device. The biasing conditions were $V_G = -0.5$ V, $V_{DS} = 8$ V and $I_{DS} = 176$ mA.

Fig. 7.4 shows the simulated results for the single-channel of the designed broadband power amplifier. The simulated gain was better than 15 dB and the output power was expected to be between 1.5–2 W across the 6-18 GHz frequency range. The designed biasing conditions were $V_G = -0.5$ V, $V_{DS} = 8$ V and $I_{DS} = 1.24$ A.

Fig. 7.4. Simulated S-parameter performance of the single-channel C-X-Ku band power amplifier.

7.3.2 Measurement Results

The process control monitor (PCM) transistor on the wafer was first characterized to ensure that the process was within control. The I_{DS} - V_{DS} characteristics, transconductance and breakdown voltage of a $2 \times 20 \mu\text{m}$ PHEMT device are shown in Fig. 7.5. The PCM device performance was compared and observed to be close to the ones described in chapter 4. This demonstrated that the fabrication process was within control and repeatable. Table 7.2 summarizes the performance characteristics of the $40 \mu\text{m}$, $60 \mu\text{m}$, $2 \times 100 \mu\text{m}$, and the $2 \times 20 \mu\text{m}$ PCM transistors on the amplifier MMIC chip.

(a)

(b)

(c)

Fig. 7.5. (a) I_{DS} - V_{DS} characteristics, (b) Transfer characteristics, and (c) Gate-drain breakdown voltage of a $2 \times 20 \text{ } \mu\text{m}$ PCM device.

Table 7.2. Summary of dc characteristics of 40 μm , 60 μm , 2x100 μm , and the 2x20 μm PCM transistor on the amplifier MMIC chip.

Device	I_{DS} at $V_G = 0.6$ V (mA/mm)	Maximum Transconductance (mS/mm)	BV_{GD} at $I_G = -1$ mA/mm (V)
40 μm , 60 μm	435	400	-18
2x100 μm	410	350	-21.5
2x20 μm (PCM transistor on amplifier MMIC wafer)	450	380	-16

The measured results of the broadband power amplifier MMIC are shown in Fig. 7.6 together with the simulated response. It was observed that the measured peak gain was about 2 dB at 17 GHz. This was much lower than the simulated value of about 17.5 dB. However, the measured S_{21} clearly depicted a broadband response from 6 – 18 GHz. A more detailed explanation for the discrepancy between the simulated and measured results follows in section 7.5.

Fig. 7.6. (a) Simulation and (b) Measured results of the broadband power amplifier MMIC.

7.4 Ku-band Power Amplifier MMIC

A Ku-band power amplifier MMIC with a desired output power of about 2 W at 1 dB compression point was also designed and fabricated. An application of Ku-band power amplifiers is in direct broadcast satellites (DBS).

7.4.1 Design and Simulated Results

The Ku-band power amplifier was essentially a modified design of the 6-18 GHz power amplifier mentioned in section 7.3.1. It basically consisted of the last stage of the 2-channel amplifier and was specifically tuned to center at 15 GHz. The Lange coupler was replaced with an in-phase combiner. Biasing was applied through the wafer probe thus eliminating the need for dc pads. This circuit has an additional function other than being a Ku-band power amplifier. It could also be used as a useful

debugging circuit for the C-X-Ku band power amplifier. As the biasing was done through the probe, the entire circuit could be characterized as a big transistor for both S-parameter measurements and on-wafer load-pull characterizations. In this way, the accuracy of the matching structure in transforming the $50\ \Omega$ termination to the optimum load impedance could be verified. The layout of the Ku-band amplifier is shown in Fig. 7.7.

Fig. 7.7. Layout of the Ku-band (14-16 GHz) power amplifier MMIC.

As the devices used were identical to those used in the C-X-Ku band power amplifier design, the device models would not be repeated here. Fig. 7.8 shows the simulated response of the Ku-band amplifier. As there was only one stage of amplification, the gain of the amplifier was lower at about 6 dB at 15 GHz. The return loss for the input was tuned to center at 15 GHz while the output return loss

was associated with the optimum load matching condition. As explained earlier, the 1-stage design was to facilitate the debugging of the process and circuit. At the same time, it was capable of demonstrating the power capability of the device at 15 GHz.

7.4.2 Measurement Results

The measured results of the Ku-band amplifier are shown in Fig. 7.9. It was observed that the measured S_{21} gain was barely 0 dB in the 14-16 GHz range. This was much lower than the simulated value of 6 dB. However, the measured S_{21} response from 14-16 GHz was the highest compared to the rest of the frequencies. This demonstrated that the intended operating frequency range of the fabricated MMIC was very close to that of the design. A more detailed explanation for the discrepancy between the simulated and measured results follows in section 7.5. Fig. 7.10 shows a photograph of the wafer where the broadband and Ku-band amplifier MMICs were fabricated. The mask layout of the chip is shown in Fig. 7.11.

Fig. 7.8. Simulated S-parameters of the Ku-band amplifier. The designed biasing conditions were $V_G = -0.5$ V, $V_{DS} = 8$ V, and $I_{DS} = 1.24$ A.

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Fig. 7.9. Measured results of the Ku-band amplifier MMIC.

Fig. 7.10. Photograph of power amplifier MMIC wafer during on-wafer measurement.

Fig. 7.11. Mask layout of power amplifier MMIC chip.

7.5 Discussion of Results and Challenges Faced in the Fabrication Work

In the broadband and Ku-band amplifiers, the measured gain was much less than the simulated value. For the broadband PHEMT amplifier circuit across 6-18 GHz, the simulated small signal gain (S_{21}) was about 17.5 dB whereas the maximum measured value was only 2 dB. As for the Ku-band amplifier centered at 15 GHz, the simulated and measured gain was 6 dB and 0 dB, respectively. The low gain was due to the reason that not all the transistors within the unit cells were working and thus the measured drain current was much lower. The non-uniformity of the ebeam resist thickness, gate writing and recess process has contributed to the non-functionality of some transistors. This conclusion was arrived at after testing the unit cells individually and verifying that the drain current has been much smaller than it would

have been if all the transistors were working. In the fabrication of a PHEMT device, the most important step is in the electron beam patterning of the T-gate and the subsequent recess etch step. In fact, a major challenge faced in the fabrication of the power amplifier MMICs was the process yield of the 0.25 μm T-gate electron beam writing. For the circuits to produce the designed output power, it was required that all 140 gates in the broadband MMIC and 80 gates in the Ku-band MMIC worked. The layout and distribution of the gates for the broadband and Ku-band MMIC is shown in Figs. 7.12 and 7.13, respectively. To accomplish this, the e-beam resist thickness variation, the e-beam writing current stability, gate recess and other factors like temperature and humidity need to be very well-controlled. This has proven to be difficult to achieve in a non-production environment.

Although the measured gain was lower than the simulated value, it was observed that the shape of the measured S_{21} response of both MMICs was close to the design indicating that the modeling and the design methodology used was accurate. If the gate yield could be improved to the extent that all transistors worked in the MMICs, the measured results should be close to the simulated response.

Fig. 7.12. Layout and distribution of the transistors in each unit cell of the broadband amplifier MMIC.

Fig. 7.13. Layout and distribution of the transistors in each unit cell of the Ku-band amplifier MMIC.

7.6 Summary

In this work, we have designed and fabricated a 6-18 GHz broadband and Ku-band power amplifier MMIC. The process for the circuit fabrication involves the integration of spiral inductors, MIM capacitors, and TaN thin film resistors into the baseline technology that was developed for the DR-PHEMTs. The circuits were CPW-based as it eliminates the need for the etching of via holes and substrate thinning. The design for both circuits was based on the small-signal equivalent circuit model and the on-wafer load-pull measurement results at 10 GHz of a 10x100 μm device.

The broadband MMIC consists of a two-channel design with integrated Lange couplers to operate in a balanced configuration. The output stage was broadband-matched to the optimum load point across the C-X-Ku band while the inter-stage and input-stage were designed to level the small-signal gain. Return losses for each channel were not optimized as they were to operate in a balanced configuration.

The Ku-band power amplifier was a modified design of the broadband MMIC. It consisted of the last stage of the 2-channel amplifier specifically tuned to center at 15 GHz. The Lange coupler was replaced with an in-phase combiner. Biasing was applied through the wafer probe thus eliminating the need for dc pads.

The measured gain for both MMICs was much less than the simulated value. The simulated and measured gain of the broadband MMIC was 17.5 dB and 2 dB, respectively. For the Ku-band amplifier centered at 15 GHz, the simulated and

measured gain was 6 dB and 0 dB, respectively. The low gain was attributed to the reason that not all the transistors within the circuit worked. This was due to the non-uniformity of the ebeam resist thickness, gate writing and recess process. Uniformity and yield have proved to be a challenging task to achieve in a non-production environment. However, it was observed that the shape of the measured small signal gain response of both MMICs was close to that of the design indicating that the modeling and the design methodology used has been accurate.

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Chapter 8

Conclusions and Recommendations for Future Work

8.1 Conclusions

In this work, a GaAs-based PHEMT process technology that is suitable for power applications at microwave frequencies has been developed. In-depth studies have also been conducted to investigate the drain current transient and hot carrier reliability in BCB- and SiN-passivated devices. Important contributions drawn from this work are summarized below.

The developed device process technology makes use of a combination of optical and electron beam lithography to develop double-recessed PHEMTs with a gate length of about 0.25 μm . The PHEMT epitaxial structure consists of a double-heterojunction with a δ -doping layer both above and below the channel to increase the channel charge density and improve the quantum well carrier confinement at the same time. PHEMTs with a high gate-drain breakdown voltage and a high drain current that are suitable for use up to about 20 GHz have been demonstrated.

An investigation into the drain current transient in $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ PHEMTs passivated by low- k BCB has been conducted. It was found that BCB reduces the density of surface states after passivation. Surface states are known to have a direct influence on the device microwave output power and it is therefore an important passivation consideration. When compared to the SiN-passivated PHEMT,

the BCB-passivated device demonstrated a larger magnitude of gate lag with its transient drain current rising to a lower value in the same time period after the gate voltage is turned on. Therefore, although BCB has a dielectric constant that is almost half that of SiN, its slower gate lag response could limit its potential for passivation use in III-V PHEMTs. It is also suggested that in the selection of a passivation material for a specific circuit application, it could be useful to take into consideration its gate lag performance as well.

The degradation characteristics due to hot carrier stress in BCB- and SiN-passivated PHEMTs have been studied. Power PHEMTs are often biased at a high drain bias and as such are subject to the generation of hot electrons under impact ionization conditions. Hot carrier stress has been performed on BCB- and SiN-passivated devices at room temperature to investigate the device dc degradation under a high gate-drain electric field. It was found that the dominant degradation mechanism is different for the two technologies. In the case of the BCB-passivated device, the proposed dominant mechanism is the trapping of hot electrons in energy states within the BCB film and/or at the interface between the semiconductor and BCB at the gate-drain access region. For the SiN-passivated device, the dominant mechanism seemed to be due to the trapping of holes in the AlGaAs layer underneath the gate and in the very thin oxide interface layer between the gate metal and AlGaAs semiconductor surface.

A 6-18 GHz broadband and Ku-band power amplifier MMIC has been designed, fabricated and measured. The MMIC process involves the integration of spiral inductors, metal-insulator-metal capacitors, and tantalum nitride thin film

resistors into the device process technology. The circuits were CPW-based as it eliminates the need for via holes etching and substrate thinning. The design for both circuits was based on the small-signal equivalent circuit model and the on-wafer load-pull measurement results at 10 GHz of a 10x100 μm double-recessed PHEMT. In both circuits, the measured gain in both the MMICs was much less than the simulated value. This was due to the reason that not all the transistors within the circuit worked due to non-uniformity of the ebeam resist thickness, gate writing and recess process. Uniformity and yield have proven to be challenging tasks to achieve in a non-production environment. However, it was observed that the response of the measured small signal gain response of both MMICs was close to that of the design indicating that the modeling and the design methodology used has been accurate.

8.2 Recommendations for Future Work

Looking ahead, much work could be carried out to deepen the current level of understanding of the DR-PHEMTs. Thermal modelling is one area that plays an important role in contributing to an accurate circuit design especially in power amplifiers. It gives circuit designers a better understanding of the thermal behaviour of the devices when operating at different bias conditions or output power levels. Thermal modelling includes measurement of the device thermal resistance at various power levels and ambient temperatures. A lower device thermal resistance also contributes to a more reliable circuit. Some of the methods used to reduce thermal resistance include substrate thinning, fabrication of heat sinks and adopting the flip-chip bonding technique.

Next, to further improve the device yield and uniformity of the fabrication process, etch-stop layers could be inserted into the current PHEMT layer structure to facilitate recessing of the gate. A commonly used etch stop material is indium gallium phosphide (InGaP). By far, gate recessing has been the most difficult step of PHEMT fabrication in terms of control. The use of a double etch-stop structure with the double gate recess technique provides a high breakdown voltage that is critical to achieving high power with excellent efficiency. At the same time, the self-limiting nature of the etch-stop layers results in a good uniformity and typically improves device and circuit yield from 20% to 60% [1]. This is key to a high-yield low-cost process. A proposed structure with two InGaP etch-stop layers that is based on our baseline structure is shown in Fig. 8.1. The first etch stop layer was added between the GaAs cap layer and the Si-doped GaAs recess layer to facilitate the recess control of the wide recess box. The second InGaP layer between the Si-doped GaAs recess layer and the AlGaAs Schottky layer is for recess monitoring of the T-gate. However, with the insertion of the etch stop layers, the device current now cannot be tuned by controlling the etch time. Therefore, the PHEMT material structure needs to be properly designed to obtain the desired channel current after recess.

n-GaAs (400 Å), doping = $6 \times 10^{18} \text{ cm}^{-3}$
InGaP Etch Stop Layer 1 (35 Å)
n-GaAs (200 Å), doping = $3 \times 10^{17} \text{ cm}^{-3}$
InGaP Etch Stop Layer 2 (35 Å)
n-AlGaAs barrier (240 Å), doping = $3 \times 10^{17} \text{ cm}^{-3}$
----- $\frac{\delta \text{doping 1}}{(n = 4 \times 10^{12} \text{ cm}^{-2})}$ -----
i-AlGaAs spacer (30 Å)
InGaAs Channel Layer (140 Å)
i-AlGaAs spacer (30 Å)
----- $\frac{\delta \text{doping 2}}{(n = 1 \times 10^{12} \text{ cm}^{-2})}$ -----
i-AlGaAs barrier (250 Å)
i-AlGaAs/GaAs (200 Å/15 Å) superlattice buffer (10 periods)
i-GaAs (2500 Å)
S.I. GaAs (100) substrate

Fig. 8.1. A proposed PHEMT epitaxial structure with InGaP etch stop layers for better double recess control.

The transient drain current investigation in BCB- and SiN-passivated has demonstrated different kinds of surface traps with different time constants in the two technologies. To obtain more information to identify the traps, the temperature dependence of the turn-on time constant of the drain current following the triggering of the gate pulse could first be derived. Then by plotting the time constant against the inverse of temperature in an Arrhenius plot, the activation energy of the traps could be obtained [2], [3]. Alternatively, the activation energy could also be obtained from the temperature dependent low-frequency transconductance dispersion. The two techniques have been proven to give close results [2].

Preliminary investigations have identified two different degradation mechanisms in BCB- and SiN-passivated PHEMTs after hot carrier stress. In order to

get a more accurate picture of how the two degradation mechanisms interact with each other, it is necessary to carry out further works to identify the origin and location of the traps and the mechanisms that are responsible for their generation. In addition, it would be useful to sample the dc characteristics on a smaller time interval like one hour and at the same time extending the stress duration to satisfy a pre-defined performance parameter failure criterion. A 20% reduction in I_{DSS} is a commonly used failure criterion. In this way, the dominant mechanism at work during a specific time frame could be more closely monitored and understood. In this work, we believe that the duration of 20 hours is sufficient to determine initially the main mechanism at work on a macroscopic level. Having understood this, the stress time could then be extended and device characteristics data sampled on a smaller time interval as suggested above.

It has been found that during hot carrier device stressing, different bias conditions and stress duration could yield different device characteristics [4]. In this aspect, off-state stress could be conducted on the device where it has shown that it leads to a remarkably larger degradation compared to the on-state hot carrier stress [5]. This is due to more pronounced electron heating at any fixed value of gate reverse current. The off-state stress could be carried out with the source floating and the gate-drain Schottky contact injected with a reverse gate current equal in magnitude to that obtained during the on-state hot electron stress.

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List of Publications

1. **C. Tan**, K. Radhakrishnan, and H. Wang, "Power performance and scalability study of AlGaAs/GaAs double-recessed pseudomorphic high electron mobility transistors on unthinned substrate for coplanar waveguide circuit applications," *Microelectron. Eng.*, vol. 81, no. 1, pp. 22-28, Jul. 2005.
2. **C. L. Tan**, P. Hui, B. Yan, H. Wang, H. Zheng, H. Yang, and K. Radhakrishnan, "Quick derivation of high-power thermal resistance values of HBT's using an existing measurement technique and a theoretical formula," *Microwave and Optical Technology Letters*, vol. 30, no. 4, pp. 287-289, Aug. 2001.
3. **C. L. Tan**, H. Wang, and K. Radhakrishnan, "Investigation of drain current transient in BCB- and SiN-passivated $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}/\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ pseudomorphic high electron mobility transistors," *Appl. Phys. Lett.*, vol. 90, no. 3, pp. 033 501-033 503, Jan. 2007.
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6. **C. L. Tan**, K. Radhakrishnan, and H. Wang, "Power scalability study of AlGaAs/GaAs double-recessed pseudomorphic high electron mobility transistors on unthinned substrate for coplanar waveguide circuit application," *Int. Conf. on Materials for Advanced Technologies*, 2003.
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9. H. Yang, H. Wang, K. Radhakrishnan, and **C. L. Tan**, "Thermal resistance of metamorphic InP-based HBTs on GaAs substrates using a linearly graded $\text{In}_x\text{Ga}_{1-x}\text{P}$ metamorphic buffer," *IEEE Trans. Electron Devices*, vol. 51, no. 8, pp. 1221-1227, Aug. 2004.

Appendix A: A Generic AlGaAs/GaAs PHEMT MMIC Process Flow

This appendix shows a generic fabrication flow for an AlGaAs/GaAs PHEMT MMIC. The process sequence is shown in Table A.1. To facilitate understanding of the technology, the details for the individual process steps and recipes are shown separately in sections A.2 and A.3 respectively.

A-1 Process Sequence for an AlGaAs/GaAs PHEMT MMIC

Table A.1. Fabrication sequence for an AlGaAs/GaAs PHEMT MMIC.

Step	Module Used	Module Description
1.	1	MESA ISOLATION
2	2	OHMIC METAL DEPOSITION
3	3	TANTALUM NITRIDE THIN FILM RESISTOR DEPOSITION
4	4	FIRST METAL DEPOSITION
5	5	SILICON NITRIDE DEPOSITION, PATTERNING OF DIELECTRIC WINDOW, AND GATE PASSIVATION
6	6	FIRST RECESS BOX LITHOGRAPHY AND RECESSING
7	7	0.25 μm T-GATE LITHOGRAPHY AND RECESSING
8	8	0.25 μm T-GATE METAL DEPOSITION
9	9	AIRBRIDGE PILLAR FORMATION
10	10	SECOND LEVEL METAL PLATING

MODULE 1: MESA ISOLATION			
Step	Process steps or recipes		Completed?
1.	CLEAN STEP		
2.	AZ1518 RECIPE 1		
3.	Hard bake @ 110°C for 30 mins.	Start Time = Stop Time =	
4.	Mesa etch using H ₂ SO ₄ :H ₂ O:H ₂ O ₂	Etched depth = 1500 Å	
5.	Strip resist.		
Remarks: Maximum leakage current should not exceed 50nA at 10 V.			

MODULE 2: OHMIC METAL DEPOSITION			
Step	Process steps or recipes		Completed?
1.	CLEAN STEP		
2.	AZ5214 RECIPE 1		
3.	Inspect source-drain separation of type-B transistors (L_{SD})	$L_{SD} = 3 \mu\text{m}$	
4.	OXIDE REMOVAL STEP		
5.	Metallization of source-drain ohmic alloy.	Ni/Ge/Au/Ni/Au = 5 nm/25 nm/100 nm/20 nm/200 nm	
6.	LIFT-OFF STEP		
7.	Rapid thermal annealing at 400°C for 10 s		
8.	Measure ohmic contact resistance.	$R_c =$ $R_{sh} = dR/dl \times W =$ Specific Contact Resistance, $r_c =$ $\gamma_c = R_c \times W =$	
Remarks:			

MODULE 3: TANTALUM NITRIDE THIN FILM RESISTOR DEPOSITION			
Step	Process steps or recipes		Completed?
1.	CLEAN STEP		
2.	AZ5214 RECIPE 1		
3.	OXIDE REMOVAL STEP		
4.	TaN sputtering using Ta target and nitrogen gas		
5.	LIFT-OFF STEP	Film thickness = 450 nm	
Remarks: Undercut must be sufficient to ensure a smooth lift-off.			

MODULE 4: FIRST METAL DEPOSITION			
Step	Process steps or recipes		Completed?
1.	CLEAN STEP		
2.	AZ5214 RECIPE 1		
3.	OXIDE REMOVAL STEP		
4.	First level metal metallization	Ti/Au = 500 nm/350 nm	
5.	LIFT-OFF STEP		
Remarks:			

MODULE 5: SILICON NITRIDE DEPOSITION, PATTERNING OF DIELECTRIC WINDOW, AND GATE PASSIVATION			
Step	Process steps or recipes		Completed?
1.	CLEAN STEP		
2.	SiN film growth using PECVD with ammonia and silane gas at 300°C.		
3.	AZ1518 RECIPE 1		
4.	Hard bake resist at 110°C for 20 mins.		
5.	SiN etching using RIE with O ₂ and CF ₄ gases.		
6.	Strip off resist		
Remarks:			

MODULE 6: FIRST RECESS BOX LITHOGRAPHY AND RECESSING			
Step	Process steps or recipes		Completed?
1.	CLEAN STEP		
2.	Spin MAA @ 4000 rpm for 60 s	Thickness = 470 nm	
3.	Oven bake @ 160°C for 1 hour		
4.	Pattern first recess box using electron beam writing		
5.	Develop pattern using MIBK:IPA (1:3) mixture @ 23°C	Developing time = 1 min.	
6.	Rinse in IPA for 1 min.		
7.	O ₂ descum for 2 mins. using RIE		
8.	OXIDE REMOVAL STEP		
9.	Recess first recess box recess using citric acid solution: H ₂ O ₂ : H ₂ O @ 10 °C	Gate Recess Time =	
10.	Measure ungated drain current using HP4156	Current =	
11.	Strip off MMA		
Remarks:			

MODULE 7: 0.25 μm T-GATE LITHOGRAPHY AND RECESSING			
Step	Process steps or recipes		Completed?
1.	CLEAN STEP		
2.	Spin PMMA @ 700 rpm for 60 s	Thickness = 230 nm	
3.	Oven bake @ 160°C for 1 hour		
4.	Spin MMA @ 4000 rpm for 60 s	Thickness = 470 nm	
5.	Oven bake @ 160°C for 1 hour		
6.	Patterning of T-gate using electron beam lithography		
7.	Develop pattern using MIBK:IPA (1:3) mixture @ 23°C	Developing time = 60 s.	
8.	Rinse in IPA for 60 s.		
9.	O ₂ descum for 2 mins. using RIE		
10.	OXIDE REMOVAL STEP		
11.	T-gate recess using citric acid solution: H ₂ O ₂ : H ₂ O @ 10 °C	Gate Recess Time =	
12.	Measure ungated drain current using HP4156.	Current =	
13.	Strip off e-beam resists.		
Remarks:			

MODULE 8: 0.25 μm T-GATE METAL DEPOSITION			
Step	Process steps or recipes		Completed?
1.	OXIDE REMOVAL STEP		
2.	Gate metal metallization	Ti/Au = 500 nm/350 nm	
3.	LIFT-OFF STEP		
4.	DC Testing using HP4156: $I_{dmax} =$ $I_{dss} =$ $g_{m(peak)} =$ $V_{th} =$		
Remarks:			

MODULE 9: AIRBRIDGE PILLAR FORMATION			
Step	Process steps or recipes		Completed?
1.	CLEAN STEP		
2.	AZ1518 RECIPE 2	For dark field mask	
3.	Sputter gold seedling layer.	Au = 400 Å	
Remarks:			

MODULE 10: SECOND LEVEL METAL PLATING			
Step	Process steps or recipes		Completed?
1.	CLEAN STEP		
2.	AZ1518 RECIPE 2		
3.	Non-cyanide gold plating	Gold thickness ~ 2.7 μm	
4.	Removal of upper layer resist using developer		
5.	Seedling layer gold etch back		
6.	Removal of bottom layer resist using acetone		
7.	Measure plated gold thickness.		
Remarks:			

A.2 Generic Conditions for Individual Process Steps

CLEAN STEP		
Step 1: Clean beaker, tools, mask and sample) in acetone/IPA		
Step 2: Mask dehydration for 15mins @ 110°C	Start Time =	Stop Time =
Step 3: Sample dehydration for 15 mins @ 110°C	Start Time =	Stop Time =
Remarks:		

OXIDE REMOVAL STEP		
Step 1: Dip in HCl:H ₂ O (1:10) for 30 s		
Step 2: Rinse in DI water and then blow dry using a nitrogen gun. .		
Remarks:		

METAL LIFT-OFF STEP		
Step 1: Soak in acetone for 20 mins.	Removal Time =	
Step 2: Dip in IPA and then blow dry using a nitrogen gun. .		
Step 3: Inspect pattern under a microscope.		
Remarks:		

A.3 Generic Conditions for Individual Process Recipes

AZ1518 RECIPE 1		
Step 1: Coat Photoresist AZ 1518	Spin Speed = 4000rpm Spin Time = 30 s	
Step 2: Soft bake @ 105°C for 90s		
Step 3: Align and expose pattern @ 14 mW/cm ²		
Step 4: Develop pattern using AZ developer: H ₂ O (1:2) for about 90 s.	Under-developed / Over-developed / OK?	
Step 5: O ₂ descum using RIE for 2 mins.		
Step 6: Measure resist thickness (~1.76-1.78 μm)	Thickness =	

AZ1518 RECIPE 2		
Step 1: Coat Photoresist AZ 1518	Spin Speed = 2000rpm Spin Time = 30 s	
Step 2: Soft bake @ 105°C for 120 s		
Step 3: Align and expose pattern @ 14 mW/cm ²		
Step 4: Develop pattern using AZ developer: H ₂ O (1:2) for about 90 s.	Under-developed / Over-developed / OK?	
Step 5: O ₂ descum using RIE for 2 mins.		
Step 6: Measure resist thickness (~2 μm)	Thickness =	

AZ5214 RECIPE 1		
Step 1: Coat Photoresist AZ 5214	Spin Speed = 4000rpm Spin Time = 30 s	
Step 2: Soft bake @ 105°C for 90s		
Step 3: Align and expose pattern @ 14 mW/cm ²		
Step 4: Post exposure bake @ 110°C for 8 mins.	Start Time =	Stop Time =
Step 5: Flood exposure bake @ 14 mW/cm ² for 20 s		
Step 6: Develop pattern using AZ developer: H ₂ O (1:2) for about 90 s.	Under-developed / Over-developed / OK?	
Step 7: O ₂ descum using RIE for 2 mins.		
Step 8: Measure resist thickness (~1.4 μm)	Thickness =	