Failure mechanisms in HfO₂ high-k gate stack MOSFETs

Ranjan Rakesh

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**FAILURE MECHANISMS IN HfO_2 HIGH- κ GATE
STACK MOSFETs**

**RANJAN RAKESH
SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING
2007**

Failure Mechanisms in HfO₂ High-κ Gate Stack MOSFETs

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School of Electrical & Electronic Engineering

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SUMMARY

The failure mechanisms in HfO₂ high- κ /polycrystalline-silicon (poly-Si) and HfO₂ high- κ /TaN/TiN gate stack n/p-metal-oxide-semiconductor field effect transistors (MOSFETs) under inversion and accumulation mode constant voltage stress have been studied both electrically and physically with the aid of high resolution transmission electron microscopy (HRTEM), energy dispersive spectrometry (EDS) and electron energy loss spectrometry (EELS) and EELS elemental dot mapping. Silicon oxynitride (SiO_xN_y)/poly-Si, silicon nitride (Si₃N₄) semi-high- κ /poly-Si gate stack MOSFETs have also been studied for comparison. The associated dielectric degradation has been correlated with the microstructural changes during breakdown event to understand the actual failure mechanisms. It is found that the breakdown phenomenon and the fundamental failure mechanisms responsible for breakdown in HfO₂ high- κ gate stacks are significantly different from that of SiO_xN_y and Si₃N₄ gate stack MOSFETs. Several new failure mechanisms/defects have been observed in HfO₂ high- κ /poly-Si and HfO₂ high- κ /TaN/TiN gate stack n/pMOSFETs.

The results show that the formation of a percolation path is assisted by the existence of grain boundaries in polycrystalline HfO₂ and/or enhanced electric field strength near the poly-Si edge in the HfO₂ high- κ /poly-Si gate stack MOSFETs. The

field assisted corner breakdowns and the grain boundary assisted breakdowns are the dominant failure mechanisms in HfO_2 high- κ /poly-Si gate stacks, and resulted in multiple breakdowns of the nanoscale HfO_2 high- κ gate stack MOSFETs. Besides *polarity-dependent* dielectric-breakdown-induced epitaxy (DBIE), due to the *BD induced thermo-chemical reactions* among HfO_2 , SiO_x (i.e., interfacial layer oxide), Hf-compounds and Si, formation of a “*ball-shaped*” capping layer which is HfSi_xO_y -rich, termed as dielectric-BD-induced *self-healing insulating cap* (SHIC), is proposed and verified. It is established that the microstructures of DBIE and SHIC are responsible for the leakage current evolution during a BD event in HfO_2 high- κ /poly-Si gate stacks.

In addition, a new failure mechanism along the interface of HfO_2 /spacer has been observed in the HfO_2 high- κ /poly-Si gate stack. This breakdown observed in the HfO_2 high- κ /poly-Si gate stack nMOSFET during accumulation mode stress (i.e., gate injection) has not been observed in the oxynitride gate stack. This interfacial breakdown could be dependent on an enhanced electric field strength at the source/drain extension regions and on the corner geometry of the high- κ /poly-Si gate stacks.

On the other hand, ultrafast progressive breakdown (PBD) has been observed in the $\text{HfO}_2/\text{TaN}/\text{TiN}$ gate stack MOSFET compared to the *poly-Si* gate MOSFET. The results show that the ultrafast PBD is attributed to a *metal-like* filament formation of the breakdown path. Ultrafast PBD which leads the device to catastrophic failure is polarity dependent and is found only in the case of substrate injection in the TaN/TiN metal gate n/pMOSFETs. Our results show that the PBD transient of the metal gate pMOSFET is much slower than that of nMOSFET in inversion mode stress. A model

describing the ultrafast PBD associated with the metal-like filamentation of breakdown path during substrate injection is proposed and verified.

In addition, the sequence of the breakdown induced microstructural defects in the HfO_2 high- κ /TaN/TiN gate stacks with various degree of the gate leakage compliance current limit has been defined. The post-breakdown microstructural defects in the HfO_2 high- κ /TaN/TiN gate stacks are also compared with the breakdown associated defects in the HfO_2 /poly-Si gate stack MOSFETs. Besides some common failure defects such as DBIE and silicide migration (i.e., dielectric-breakdown-induced migration), several new post-breakdown microstructural defects such Ta-based intermix at silicon substrate, anode amorphization, metal/high- κ delamination are observed in the metal gate stacks compared to that of the poly-Si gate stacks.

In summary, the study focuses on the correlation of the dielectric degradation with the breakdown induced microstructural damages, which provide a better understanding of the breakdown mechanism in the HfO_2 high- κ /poly-Si and metal gate stack MOSFETs.

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LIST OF ABBREVIATIONS

BD	Breakdown
Co	Cobalt
CVS	Constant voltage stress
CMOS	Complimentary metal-oxide-semiconductor
C	capacitance
C-AFM	Conductive atomic force microscopy
DBIE	Dielectric-breakdown-induced epitaxy
DBIM	Dielectric-breakdown-induced migration
D	Drain
EELS	Electron energy loss spectrometry
EDS	Electron dispersive spectrometry
EOT	Equivalent oxide thickness
E	Electric field
FIB	Focussed ion beam
GB	Grain boundary
g_m	Transconductance
HBD	Hard breakdown
HRTEM	High resolution transmission electron microscopy
H	Hydrogen
HfO ₂	Hafnium oxide
Hf	Hafnium
I	Current
I _g	Gate leakage current

I_s	Source leakage current
I_d	Drain leakage current
I_{sub}	Substrate leakage current
I_{ds}	Source to drain current
I_{sd}	Drain to source current
I_{gl}	Gate leakage compliance current limit
I_{dsat}	Drain saturation current
IL	Interfacial layer
IC	Integrated circuit
L	Gate length
LDD	Lightly doped drain
MOSFET	Metal-oxide-semiconductor field effect transistor
M	Metal
mA	Milli ampere
μA	Micro ampere
μm	Micro meter
n	Ideality factor
nm	Nano meter
N	Nitrogen
Ni	Nickel
NBTI	Negative bias temperature instability
O	Oxygen
PBTI	Positive bias temperature instability
Poly-Si	Polycrystalline silicon
PBD	Progressive breakdown
R_{geff}	effective gate resistance
SCVS	Successive constant constant voltage stress
S	Source
SRAM	Static random access memory
Si	Silicon
SiO_2	Silicon di-oxide
SHIC	Self healing insulating cap
SBD	Soft breakdown
SiO_xN_y	Silicon oxynitride

Si_3N_4	Silicon nitride
SILC	Stress induced leakage current
Ta	Tantalum
TaN	Tantalum nitide
TEM	Transmission electron microscopy
Ti	Titanium
TiN	Titanium nitride
TDDDB	Time dependent dielectric breakdown
T	Temperature
T_B	Barrier thickness of constriction
V	Voltage
V_s	Source voltage
V_g	Gate voltage
V_d	Drain voltage
V_{sub}	Substrate voltage
V_{ds}	Source to drain voltage
V_{sd}	Drain to source voltage
V_{gstress}	Applied gate stress voltage
V_T	Threshold voltage
W	Gate width

LIST OF SYMBOLS

A	ampere
A^{**}	Richrdson's constant
F	farad
μ	micro
k	Boltzmann's constant
κ	Dielectric constant
K	Kelvin
eV	Electron-volt
Ω	Ohm
ϕ	Shottky barrier height
φ	QPC barrier height
q	Electronic charge
ρ	Resistivity

Chapter 1 INTRODUCTION

1.1 Background

The metal-oxide-semiconductor field effect transistor (MOSFET) is currently the device of choice for integrated circuits (ICs). A thermally grown oxide of silicon, forming the insulating layer between the control “gate” and the conducting “channel”, is considered as the heart of a MOSFET. The outstanding properties of silicon dioxide (SiO_2), which include high resistivity ($\sim 10^{15} \Omega \text{ cm}$), excellent dielectric strength ($\sim 1 \times 10^7 \text{ V/cm}$), a large band gap (9 eV), high melting point (1986 K) and a native, low defect density interface with Si ($\sim 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$), are in large part responsible for enabling the microelectronics revolution. The Si/SiO₂ interface is arguably the world’s most economically and technologically important materials interface. In spite of its many attributes, however, SiO₂ suffers from a relatively low dielectric constant ($\kappa = 3.9$). To achieve high drive current for nanoscale devices, the SiO₂ layers have of necessity been scaled down to ever-thinner dimensions. This aggressive scaling of the thickness of the gate insulator in microelectronics to achieve higher performance and circuit density causes a number of problems, including impurity penetration through the SiO₂, enhanced scattering of carriers in the channel, high gate leakage current due to direct tunneling of carriers for thickness less than 5.0 nm and possible reliability degradation. The possible gate leakage at 1.0 V has been suggested to be

between 1 A/cm^2 to 10 A/cm^2 [1-2]. This corresponds to an oxide thickness between $\sim 1.2 \text{ nm}$ to $\sim 1.5 \text{ nm}$ [2]. However, another concern is that the intrinsic reliability may limit the further scaling of the oxide thickness. Lo *et al.* [3] predicted that oxides thinner than 1.2 nm may not have the required post-breakdown reliability margin as a critical voltage of breakdown for thinner oxide ($< 1.2 \text{ nm}$) is in the range of the corresponding nominal operating voltage. It has been also predicted that for 1.6 nm gate oxide thickness the nominal operating voltage should be 1.38 V at a temperature of 298 K [4]. Therefore, for the technology generations that require $< 1.0 \text{ nm}$ equivalent SiO_2 thickness with low gate leakage current and good reliability will have to rely on alternate high- κ dielectrics which provide greater physical thickness while maintaining the same gate capacitance.

Many high- κ materials such as La_2O_3 , ZrO_2 , Ta_2O_5 , HfO_2 and etc. have been explored as the alternative gate dielectrics to overcome the leakage current problem. Among the high- κ alternatives, HfO_2 is a very promising candidate because it has good material properties and has been demonstrated better device characteristics, and is compatible with the polycrystalline silicon (poly-Si) gate process [5-7]. An improvement in the MOSFET performance can be gained by replacing the poly-Si with a metal, eliminating the gate depletion effect. Metal gates are commonly used in conjunction with metal oxide gate dielectrics, such as HfO_2 and $\text{Hf}_{1-x}\text{Si}_x\text{O}_2$. This has the added advantage of avoiding unwanted poly-Si/ HfO_2 interactions [8].

On the other hand, due to the reliability degradation in ultrathin gate dielectric, analysis of the breakdown (BD) phenomenon in gate dielectric has been a potential field of research for decades. Different groups of researchers have analyzed the breakdown phenomenon with different views and with different proposed physical models. First an empirical model for breakdown was developed by observing the

electric field dependence of time-dependent dielectric breakdown (TDDB) data and established that $t_{BD} \sim \exp(-\gamma E)$ [9,10], where γ is the electric field acceleration factor. Later, a physical model was hypothesized based on an electric field driven defect generation known as Thermochemical model or E -model [11, 12]. A second mechanism based on anode hole injection known as I/E -model was also proposed by other groups [13,15], which contradicts the E -model. The validity of the electric field driven model becomes questionable after the observation of degradation in oxide lifetime by substrate hot electron injection experiments [16]. The validity of electric field driven model is also questionable due to polarity and thickness dependence of ultrathin gate oxide breakdown [17, 18].

A third model has been suggested which claims that the critical density of electron traps generated during the stress is required to trigger the oxide breakdown [19, 20]. Another statistical process of breakdown was proposed considering the percolation theory, which links the existing anode hole injection model and electron trap generation model [21, 22]. In this theory the parameters used to fit the experimental data is the trap radius and fraction of defects effective in initiating breakdown. Currently, the percolation model is the most widely accepted model for ultrathin oxide breakdown.

Most of the breakdown phenomena are studied from the electrical point of view. Very few reports on the physical analysis of the breakdown phenomenon can be found in the literature. Recently, Radhakrishnan *et al.* [23] and Pey *et al.* [24] reported that a dielectric-breakdown-induced epitaxy (DBIE) in the vicinity of gate area is associated with ultrathin gate oxide breakdown. The physical analysis results show that DBIE is highly localized, and its location is dependent on the stressing voltage polarity regardless of the compliance current and hardness of the breakdown. The

suggested driving force behind the DBIE formation is a thermal electromigration effect [25]. It is also reported that DBIE formation is one of the major concerns for the reliability of ultrathin gate oxide [26].

1.2 Motivation

Differentiation of the various breakdown hardnesses in ultrathin gate-dielectric breakdown has become extremely challenging because only minute effects can be observed in transistor parameters such as threshold voltage (V_T) and transconductance (g_m) following soft breakdown (SBD) [27]. Similar findings were reported if the breakdown spot is not located in the device source or drain region [28, 29]. It was also reported that a ring oscillator circuit continued to function even after several transistors in the circuit experienced breakdown [30]. Some researchers related SBD and hard breakdown (HBD) to the effective gate resistance (R_{geff}) measured after breakdown, and reported that for the HBD case, R_{geff} ranges from ~ 1 to ~ 30 k Ω whereas for the SBD case, R_{geff} value is greater than 30 k Ω [31,32]. Pey *et al.* [26] further attempted to differentiate the hardness of breakdown by the growth of dielectric-breakdown-induced epitaxy. So far, all the efforts are not fully sufficient for distinguishing the SBD and HBD unambiguously. Furthermore, successive breakdown study by relaxing the gate leakage compliance current limit in the constant voltage stress can give better understanding of the post-breakdown transistor performance.

On the other hand, the reliability study of HfO₂ gate dielectric, which is considered as a potential candidate for the future gate insulator, is getting more attention by the researchers. It has been reported that the Weibull slopes (β) of the breakdown distribution of the soft and hard breakdown in HfO₂/poly-Si gate stacks

have different values, and the β value of HBD is greater than that of the SBD case [33]. It has also been reported that β of thick HfO_2 is smaller than that of SiO_2 with a similar physical thickness. Whereas, β of thinner HfO_2 is similar to that of SiO_2 . Furthermore, the breakdown is intrinsic and can be explained by the percolation model [34]. On the other hand, it has been reported that high degradation rate in the gate leakage current is very common in the breakdown of HfO_2 high- κ /metal gate stack MOSFETs [35]. But the actual failure mechanisms in the HfO_2 high- κ gate stacks are still not well understood. So far, the study of the HfO_2 high- κ gate stacks breakdown is based on pure electrical analysis. No report in the literature has described the physical analysis of the breakdown phenomenon in the HfO_2 high- κ gate stacks. Hence it is of great interest to study the microstructural defects associated with various degrees and hardness of breakdown for better understanding of the failure mechanisms in the HfO_2 high- κ gate stack MOSFETs. This can be achieved with transmission electron microscopy (TEM), high resolution TEM (HRTEM), electron energy loss spectrometry (EELS), and electron dispersive spectrometry (EDS).

1.3 Objectives

The objectives of the research work are the following: (1) To understand the failure mechanisms in HfO_2 high- κ /poly-Si and HfO_2 high- κ /TaN/TiN gate stack MOSFETs by both electrical analysis and physical analysis (TEM/EDS/EELS/EELS elemental dot mapping); (2) To correlate the physical analysis results with the electrical results; (3) To propose models of breakdown describing the failure mechanisms in the HfO_2 high- κ gate stack MOSFETs; and (4) To compare the failure

mechanisms in the HfO_2 high- κ /poly-Si gate stack with the HfO_2 high- κ /metal gate stack MOSFETs.

1.4 Major contribution of the Thesis

The major contributions of this research work are:

- 1) Breakdown failure mechanisms in HfO_2 high- κ /poly-Si gate stack nMOSFETs under inversion and accumulation mode constant voltage stress have been both electrically and physically studied with the aid of HRTEM/EDS/EELS/EELS elemental mapping. It has been observed that the fundamental mechanisms responsible for breakdown in the HfO_2 /poly-Si gate stacks are significantly different from that of SiO_xN_y /poly-Si and Si_3N_4 /poly-Si gate stack MOSFETs.
- 2) New failure mechanisms such as field assisted corner breakdowns and grain boundary assisted breakdowns are the dominant failure mechanisms in the HfO_2 high- κ /poly-Si gate stacks, resulting in multiple breakdowns of the nanoscale HfO_2 high- κ gate stack MOSFETs.
- 3) Breakdown induced thermochemical reactions leading to formation of HfSi_xO_y -rich “ball-shaped” capping layer during breakdown event in the HfO_2 high- κ /poly-Si gate stacks have been observed.
- 4) Dielectric-breakdown-induced self-healing insulating cap (SHIC) model is proposed and verified. On the basis of the SHIC model, the post-breakdown gate leakage current evolution is described.
- 5) HfO_2 high- κ /spacer-interface breakdown has been observed in the HfO_2 high- κ /poly-Si gate stacks. It is found that this breakdown which is more common in accumulation mode stressing conditions in the HfO_2 high- κ /poly-Si gate stacks

has not been observed in oxynitride gate dielectrics. A possible breakdown model describing the high- κ /spacer-interface breakdown has been proposed.

- 6) The failure mechanisms/defects associated with breakdown of HfO₂ high- κ /TaN/TiN gate stack n/pMOSFETs are studied. Polarity dependent ultrafast progressive breakdown (PBD) during substrate injection is found. It is established that the ultrafast PBD, which leads to ultrafast degradation in the device performance is due to metal filament formation of the breakdown path during the breakdown event.
- 7) A metal filamentation model describing failure mechanism in the HfO₂ high- κ /TaN/TiN gate stack n/pMOSFETs has been proposed and further verified by the associated electrical results and indirect physical analysis results.
- 8) The sequence of the breakdown induced microstructural defects in the HfO₂ high- κ /TaN/TiN gate stacks with a gate leakage compliance current limit has been defined.
- 9) The failure mechanisms/defects in the HfO₂ high- κ /TaN/TiN gate stacks are compared to the HfO₂ high- κ /poly-Si gate stack MOSFETs.

1.5 Organization of the Thesis

The thesis consists of seven chapters. Chapter 1 introduces the motivation and the objective of this work, as well as the main contributions of the research and the organization of the thesis.

Chapter 2 provides a literature survey on the study of SiO₂ gate dielectric and HfO₂ high- κ gate stacks reliability.

Chapter 3 focuses on the experimental details. The chapter first explains the details of devices used and then describes different stressing conditions and characterization techniques.

Chapter 4 presents the failure mechanisms/defects in the HfO_2 high- κ /poly-Si gate stack MOSFETs. The chapter describes the common and new failure mechanisms/defects in the HfO_2 high- κ /poly-Si gate stacks as compared to the SiO_xN_y /poly-Si and Si_3N_4 /poly-Si gate stack MOSFETs. The chapter also proposes a model describing the breakdown mechanisms in the HfO_2 high- κ /poly-Si gate stack MOSFETs.

The failure mechanisms and breakdown-induced microstructural defects in the HfO_2 high- κ /TaN/TiN gate stacks are presented in Chapter 5. On the basis of electrical and physical analysis results, ultrafast progressive breakdown associated with metal filamentation of the breakdown path in the metal gate MOSFETs during substrate injection is established. A filamentation model of the breakdown describing the different stages of the breakdown in metal gate stack MOSFETs is also described in Chapter 5.

Chapter 6 discusses the new and common failure mechanisms/defects in the HfO_2 high- κ /TaN/TiN gate stack as compared to the HfO_2 high- κ /poly-Si gate stack MOSFETs.

Summary and conclusions of the failure mechanisms/defects in the HfO_2 high- κ gate stacks as well as suggestions and recommendations for future study for better understanding of the failure mechanisms are presented in Chapter 7.

Chapter 2 LITERATURE REVIEW

2.1 Introduction

This chapter provides an overall view of the breakdown mechanisms in $\text{SiO}_2/\text{poly-Si}$, high- $\kappa/\text{poly-Si}$ and high- $\kappa/\text{metal gate stacks}$, which had been reported in the literature. A few dominant dielectric breakdown models, various modes of breakdowns associated with gate dielectric breakdowns, and different analysis methods are discussed in here. Advantages and concerns of the HfO_2 high- κ gate dielectric compared to that of $\text{SiO}_2/\text{SiO}_x\text{N}_y$ gate dielectric as well as merits of the metal gate electrode over the polycrystalline gate electrode in high- κ gate stacks have also been discussed in this chapter.

2.2 Silicon dioxide gate insulator

The microelectronics industry owes its considerable success largely to the existence of the thermal oxide of silicon i.e., SiO_2 . A thin layer of SiO_2 forms the insulating layer between the control “gate” and the conducting “channel” of the metal-oxide-semiconductor field effect transistor used in the modern integrated circuits. As circuits are made denser, all the dimensions of MOSFET are scaled correspondingly.

Nowadays the SiO_2 layer thickness is 1.4 nm or less in nanoscale Si devices, and the reliability of such ultra-thin oxide layers has become a major concern for continued scaling.

2.2.1 Physical and statistical models for gate oxide breakdown

Figure 2.1. (a) Two-dimensional representation of the tetrahedral bonding of the silicon to itself (in substrate and poly) and to oxygen in the SiO_2 dielectric. Also illustrated is the induced polarization which occurs due to lattice distortion. The permanent dipoles parallel to the electric field grow (by bond distortion) at the expense of those oriented anti-parallel to the electric field. (b) Oxygen vacancy and the Si-Si bond which forms when the bridging oxygen atom is missing due to Si-O bond distortion by local high electric field. Later, the hole trap or electron trap created due breakage of strained Si-Si bond [12].

The breakdown phenomenon in silicon dioxide has always been a potential field of research and a subject of numerous publications over the last three decades. Although the exact physical mechanism responsible for TDDB and eventual breakdown is still an open question, the BD phenomenon in thin SiO_2 has been analyzed with several most probable physical mechanisms. First, an empirical model was suggested on the basis of experimental data showing electric field dependence of TDDB [9]. The time-to-failure is expressed as [9]:

$$t_{BD} \approx C \exp(-\gamma E) \quad (2.1)$$

where C is a constant independent of the electric field E and γ is the electric field acceleration factor. By using this empirical model, Berman *et al.* [10] demonstrated that a ramped voltage breakdown histogram of a sample population could be used to accurately forecast the rate of the BD failures of ICs in the field. The time-to-failure at a given applied field can be predicted as [10]:

$$\ln t_{BD}(F) = \ln t_0 + \gamma[E_B(F) - E_A] \quad (2.2)$$

where $t_{BD}(F)$ is the time to failure at the applied field, $E_B(F)$ is the measured BD field distribution, t_0 is the effective time to BD at field E_B , and E_A is the applied electric field.

Later, a physical model was hypothesized based on the electric field driven defect generation process which supported the same observed dependence of the oxide lifetime on electric field known as thermochemical model [11]. This model is named as the E -model and described that when an electric field E_{ox} is applied, a distortion in the lattice and a shift in the electron cloud about each oxygen nucleus occur [12]. This distortion resulting in a polarization P :

$$P = \chi \epsilon_0 E_{ox} \quad (2.3)$$

where χ is the electric susceptibility and ϵ_0 is the permittivity of the free space. Due to this polarization each SiO_2 molecule will experience the applied electric field

plus the field due to polarization P (see Fig. 2.1(a)). Hence, the molecules experience a local electric field E_{loc} :

$$E_{loc} = (1 + L\chi)E_{ox} \quad (2.4)$$

where L is the Lorentz factor. The local electric field is greater than the applied electric field. This high local electric field distorts the Si-O bonds, resulting in strained Si-Si bonds. Later, the local electric field interacts with the weak strained Si-Si bonds associated with the oxygen vacancies in the amorphous silicon dioxide film and eventually, breaks the weak bond and creates a permanent hole trap or electron trap (see Fig. 2.1(b)) [12].

A second physical model was proposed on the basis of anode hole injection mechanism also known as I/E – model [13-15]. In this model, it was described that tunneling electrons (due to Fowler - Nordheim (FN) tunneling) transferred energy to the holes at the anode side, where they are injected into the oxide film. The injected holes can be trapped and modify the oxide potential barrier to enhance the additional electron injection and eventually, the positive feedback process caused a current runaway leading to thermal catastrophic breakdown of the oxide. In this case the time to BD is proportional to the inverse of the electric field and expressed as:

$$t_{BD} \approx C^* \exp\left(\frac{\beta}{E}\right) \quad (2.5)$$

where C^* is a constant independent of the electric field E , and β is the electric field acceleration factor. It was also reported that holes could be generated in the oxide by impact ionization process at higher applied voltages (~ 9 V) [36]. At energies below ~ 9 V the anode hole injection was believed to take place via surface plasmon process [37-38].

Another breakdown model known as anode hydrogen release (AHR) model based on the release of the atomic hydrogen from the anode by energetic tunneling electrons, which causes defects in the oxide film [39]. This model postulated that electrons with sufficient energy could tunnel through the gate oxide potential and reach the anode. These energetic electrons release hydrogen (H) from the anode/gate oxide interface. The threshold voltage for this process to take place is approximately 5 V [39]. The process has been shown to continue at voltages as low as 1.2 V [40, 41]. The released hydrogen diffuses through the gate oxide and generates electron traps in the gate oxide as shown in Fig. 2.2.

Figure 2.2. Illustration showing the hydrogen release mechanism [39].

On the other hand, the validity of an electric field driven model becomes questionable after the observations of substrate hot electron injection experiments [16]. Substrate hot electron injection causes a significant degradation in oxide lifetime. An anode hole injection process does not necessarily require I/E dependence, especially when considering the defect generation process in the direct tunneling current regime for ultrathin gate dielectrics. It has been reported that the BD in ultrathin gate dielectrics is thickness and polarity dependent [17-18].

Besides, it is assumed that the tunneling electrons may be the driving force for wear-out and breakdown in ultrathin gate oxide. In the direct tunneling regime, the energy of the tunneling electrons is proportional to the applied gate voltage [40, 41]. Log-normal statistics were used previously to fit the data from accelerated life tests to induce various failure mechanisms such as oxide breakdown and electromigration. But later it has been realized that the Weibull distribution fits more accurately with the data, particularly, at low failure rates in ultrathin gate oxides [42-43]. More importantly, Log-normal statistics do not predict the observed area dependence of the t_{BD} for ultrathin gate oxides. Furthermore, the Weibull shape parameter is experimentally observed to decrease as oxide thickness is decreased. One of the real breakthroughs in the understanding of the statistical nature of ultrathin oxide BD is the idea that a critical number of defects must be generated in the film for triggering the oxide BD known as the electron trap generation model [19, 20]. In this model it has been described that the breakdown of oxide takes place, when the number of defects formed in the oxide reaches a critical value.

Figure 2.3. Schematic illustration of percolation-model based on traps generation and conduction via traps. A breakdown path is indicated by shaded spheres [21].

A link between the anode hole injection model and electron trap generation model has been established on the basis of the percolation theory known as percolation model [21, 22, 44]. The parameters used to fit the experimental data are the trap radius and the fraction of defects effective in initiating the breakdown. Figure 2.3 illustrates the percolation model where defects are generated randomly throughout the volume of the oxide film. As defect generation continues, defects can connect electrically to the cathode (poly-Si gate/Si-substrate) and anode (poly-Si gate/ Si-substrate) shown as the shaded spheres in Fig. 2.3. It is clear that if the oxide thickness is made thinner, a percolation path can result with a lower defect density. A device with larger area would also have a higher probability of having overlapping defects for the same oxide thickness.

The percolation model predicts that only one defect is necessary to initiate BD as oxide thickness approaches the diameter of single defect (~ 0.9 nm) [22]. It is the most widely accepted model. But it should be mentioned that although the percolation model predicts many statistical features of ultrathin oxide BD, the parameters chosen, such as the defect's physical dimensions and density, may not relate to the actual defect's physical dimensions, density and the range of interaction. It has been also

reported that the defect density used in the percolation model differs by a factor of 1,000 when compared to the defect density determined by stress induced leakage current (SILC) measurements [44]. Also, defect generation may not be truly random in some structures where gate edge effects dominate the breakdown [44].

2.2.2 Electrical characterization of device breakdown and circuit failure

Characterizing the integrity and reliability of ultrathin SiO₂ films has become extremely challenging due to the difficulty in detecting soft and noisy breakdown behavior in the current/voltage versus time characteristics. Unlike HBD, which is characterized by a large change in the voltage or current during breakdown transient and a post-breakdown current-voltage (*I-V*) characteristic that is essentially almost ohmic, SBD is detected by a much smaller change in the voltage or current after breakdown and by the post-breakdown *I-V* characteristics which have been described by a power law [45]:

$$V_g = \rho_{eff} I_g^\alpha \quad (2.6)$$

where V_g is the applied gate voltage, ρ_{eff} is the effective oxide resistivity, I_g is the post-breakdown gate leakage current, and $\alpha = 0.32 \pm 0.02$ [45]. SBD was first observed in sub-5.0 nm oxide films [46]. The observed fluctuations in the SBD behavior were explained as multiple tunneling events via electron traps after a critical density of traps developed to trigger breakdown. Sune *et al.* [47, 48] proposed the most successful model to describe the post-SBD conduction. The model uses a quantum point contact (QPC) to represent the conducting filament that has developed

as a result of the percolation of defects. Post-breakdown current versus voltage curves have been successfully fitted to the model using two parameters: the energy barrier height of the constriction (ϕ) and α , which is correlated to the shape of the contact. Another model developed by Alam *et al.* [49] explains that SBD is the result of limited power dissipation available at the instant of dielectric breakdown. As the oxide ages under constant voltage stress, traps are generated via the percolation process. A percolation path forms after a critical number of traps have been generated. So that the traps link the gate electrode to the silicon substrate. The surge of current through the percolation path produces localized joule heating that may result in permanent structural damage if the local power dissipation is high enough [49]. The degree of the hardness of the breakdown is related to the amount of the available power dissipation. It was also mentioned that the occurrence of HBD increases with the increasing gate voltage since the power dissipation is related to the voltage $V(t)$ and the current $I_{perc}(t)$ across the percolation path.

The occurrence of soft breakdown increases as the stress voltage is decreased. It has been reported that the voltage and temperature acceleration parameters obtained from the devices that experienced soft breakdown were different from those obtained from devices that experienced hard breakdown [50]. It was also reported on the basis of statistical analysis that both SBD and HBD share a similar origin [51].

Differentiation of various breakdown hardnesses in ultrathin gate-dielectric and its impact on the device performance has become extremely challenging because very little effect can be observed in the transistor parameters V_T and g_m following SBD [27]. Similar findings were reported on the effect of SBD on the transistor performance if the breakdown spot was not located in the device's source or drain region [28, 29]. It has been reported that HBD and catastrophic failure occurred more

frequently in the device having smaller channel length due to a higher probability of the breakdown at the source and drain regions compared to that of the channel [52]. The higher probability of the breakdown at the source and drain regions in the smaller channel length devices is attributed to the dominance of the source and drain regions over the channel area [52]. It has been also reported that the BD location can be measured electrically by the post-breakdown drain current (I_d), source current (I_s) measurements with $V_g = -1.5$ V for nMOSFETs or $V_g = 1.5$ V for pMOSFETs while all the other terminals grounded [53, 54]. The BD position along the channel length can be evaluated using the sorting function S :

$$S = \frac{\Delta I_d}{(\Delta I_d + \Delta I_s)} \quad (2.7)$$

where ΔI_d and ΔI_s are the differences in the drain current and the source current after the breakdown and prior to the breakdown, respectively. If $S = 0$ and 1 the BD will be at the source extension region and drain extension region, respectively. Equation (2.7) can therefore be used to distinguish between source, channel and drain breakdowns. It has also been reported that BD that occurred over the source/drain extension regions will destroy the device functionality [53].

Kaczer *et al.* [30] performed circuit level study of the impact of BD in devices on the overall functionality of a circuit. He reported that a ring oscillator circuit continued to function even after several devices comprising the circuit experienced BD. The increased leakage current in the ruptured devices affected the frequency of oscillation, standby current and dynamic supply current; however, the logic operation was not destroyed. But it is still an open question as to what level of breakdown

hardness will be considered as SBD (affordable range of hardness), which results in less degradation in the performance of the device and circuit functionality. Some researchers tried to differentiate SBD and HBD with the post-breakdown effective gate resistance R_{geff} [31, 32]:

$$R_{geff} = \frac{V_g}{I_g} \quad (2.8)$$

where the applied $V_g = 1.5$ V and the applied source voltage (V_s) = drain voltage (V_d) = substrate voltage (V_{sub}) = 0 V for nMOSFET. It was reported that for the HBD case, R_{geff} ranges from ~ 1 k Ω to ~ 30 k Ω whereas for the SBD case, R_{geff} is greater than 30 k Ω [31, 32].

Figure 2.4 shows the relationship between the effective gate resistance (calculated using equation (2.8)) and the position of breakdown spots along the channel (calculated using equation (2.7)) [53]. The effective gate resistance drops linearly over the 40 nm wide interval at both source and drain side (see Fig. 2.4). Hence, the source/drain side breakdown has more severe effect on the device performance degradation than the channel breakdown.

Figure 2.4. The effective gate resistance plotted as a function of the breakdown spot position along the channel in three short channel nMOSFETs. The experimental data of the 150 nm, 180 nm and 200 nm channel lengths nMOSFETs are shown by hollow circle, filled square and hollow square respectively [53]. The solid lines are guides for the eye. X-position 0 nm indicates that the breakdown spot is at source.

Figure 2.5. Gate leakage current evolution after the first breakdown event with stressing time in SiO₂/poly-Si gate stack [56].

Figure 2.6. The oxide degradation is a 3 step process: I. The time to creation of a localized conduction path with leakage current ΔI ; II. The progressive wear-out of this path; and eventually III. Saturation due to series resistance [57].

2.2.3 Physical analysis of breakdown phenomenon in ultrathin gate oxide

Even if a circuit survives after a first BD event, because the conductance of the gate current in the affected device is controlled by the effective gate resistance, the continued functionality of the circuit depends on the stability of the leakage path. In ultrathin gate oxide, the occurrence of BD, which is due to the formation of a defect-rich conductive path linking the poly-Si gate and substrate, is followed by a progressive increase in the gate leakage current transient known as “progressive breakdown” (see Fig. 2.5) [45, 55, 56]. From Fig. 2.5, it can be seen that after the first breakdown event the gate leakage current takes 285 s to reach a value of 350 μA . Kaczer *et al.* [57] reported that three phases in the oxide degradation can be distinguished in the ultrathin oxynitride/poly-Si gate stack transistors (Fig. 2.6). First a localized conduction path is formed (Fig. 2.6, I), then this conduction path

progressively wears out (Fig.2.6, II) until the current is limited by a series resistance (Fig. 2.6, III). Catastrophic failure occurs when the leakage current becomes so high that the transistor is no longer functional [57]. Hence, the progressive breakdown provides extra reliability margin for the transistor after a first breakdown event. On the other hand, for a full understanding of the breakdown phenomenon, electrical characterization alone is not sufficient. There is a need to understand the physical nature of the locally damaged region in the gate oxide immediately after BD and the microscopic nature of the associated defects, which one is suspected to lead to destructive breakdown. But, very few reports on the physical analysis of BD phenomenon can be found in the literature. Radhakrishnan *et al.* [23] and Pey *et al.* [24] reported that a localized dielectric-breakdown-induced epitaxy in the vicinity of the breakdown path, dielectric-breakdown-induced migration (DBIM), generation of severe substrate defect, gate oxide burnout, and/or even gate evaporation are commonly seen to be associated with ultrathin gate oxide breakdown.

The physical analysis results show that DBIE is a highly localized microstructural defect and always occurs on the cathode side regardless of the compliance current and hardness of the breakdown. For example, for devices stressed in inversion mode, DBIE only occurs in the poly-Si gate in pMOSFET and at the silicon substrate in nMOSFET as shown in Fig 2.7 (a) and (b), respectively [25].

Figure 2.7. HRTEM lattice image of a DBIE hillock extending from (a) the Si substrate in an nMOSFET, and (b) the poly-Si grain in pMOSFET [59].

Tung *et al.* [25] suggested that the primary driving force for the formation of DBIE in very narrow transistor is an enhanced thermal effect in the very confined narrow gate structure initiated by joule heating due to a high current density surging through a very narrow initial percolation path of the gate breakdown spot in ultrathin gate oxides (G_{ox}). The model was supported by the ANSYS – simulation results, which showed that the breakdown induced localized thermal joule heating in the vicinity of the percolation path is very high and more than the silicon melting point during PBD [58]. The very large thermal effect and large current density present in the vicinity of the breakdown spot of the cathode side accelerate the migration of the

thermally dislodged Si atoms towards the percolation path of the gate oxide during the breakdown transient. Since oxide is a perfect diffusion barrier for Si atoms, the Si atoms are subsequently piled up and re-grown as Si epitaxy at the nucleation site of the oxide interface of the cathode end (see Fig. 2.7).

Figure 2.8. Schematic showing the possible effects of oxide deformation caused by the growth of DBIE on G_{ox} failures. (a) Localized oxide “thinning” occurs when the G_{ox} thickness at DBIE point $T_{1ox} < T_{ox}$, which favors more percolation paths formation in its vicinity. (b) A proposed progression of the growth of the DBIE during a SBD where $t_1 < t_2 < t_3$ (t_1 , t_2 , and t_3 are the time intervals). HBD will occur if DBIE from the cathode grows to an extent that it shorts the anode [26].

Figure 2.9. Dynamic lateral evolution of DBIE towards nearer lightly doped drain (LDD) region during progressive breakdown [61]. The growth of DBIE will gradually skew towards the nearest LDD region due to the relatively smaller channel resistance.

It was also that reported DBIE formation is one of the major concerns for the reliability of ultra thin gate oxide [26]. Pey *et al.* [26] attempted to differentiate the hardness of BD by the growth of dielectric-breakdown-induced epitaxy. They categorized the BD into three stages: SBD (percolation path formation and its dilation due to huge thermal heat in the vicinity of percolation path), SBD+DBIE (gate oxide thinning due to nucleation and growth of DBIE) and HBD+DBIE (catastrophic breakdown due to gate oxide rupture by huge DBIE), which are similar to the three stages of the oxide breakdown revealed by ballistic electron emission spectroscopy [60]. It is also suggested that the DBIE formation is a dynamic process (see Fig. 2.8) and depends on the effective percolation conduction path diameter X_d . If the growth rate of X_d is slower than the DBIE growth rate, the localized gate oxide thickness T_{ox} will be so thin and eventually DBIE will physically breakaway the gate oxide and results in HBD+DBIE. If the rate of X_d increase is much faster than the DBIE growth rate, the lateral expansion of X_d will be fast enough to cope with the gate oxide thinning, resulting in SBD+DBIE without gate oxide being physically ruptured.

Figure 2.10. A plot of the percentage change in the g_m / I_{dsat} versus the gate leakage compliance current limit on which the regions in which various modes of breakdown are shown [61]. The discovery of DBIE allows us to classify the modes of BD into SBD, SBD+DBIE and HBD+DBIE.

The DBIE lateral evolution is always faster towards the nearer lightly doped drain (LDD) region during PBD [61]. Assuming that DBIE is located close to the edge of the device channel, due to the relatively smaller channel resistance, the portion of DBIE nearer to the LDD region will experience a stronger electron flux. Consequently, the portion of DBIE closer to the LDD region will grow with a faster rate than other portions of DBIE. Figure 2.9 shows the dynamic lateral evolution of DBIE during PBD [61]. As a whole, the growth of DBIE will gradually skew towards the nearest LDD region and leads the device to catastrophic failure by making a direct connection between LDD and gate. Lateral evolution of the DBIE towards the nearer LDD region has been fully supported by electrical and physical analysis results (see

Fig. 2.10). It can be seen that the DBIE growth evolves from the channel and shorts the nearer LDD region, resulting in catastrophic failure of the device (see the TEM micrograph of Region HBD+DBIE of Fig. 2.10).

Figure 2.11. General representation summarizing that the degree of microstructural damages induced by dielectric BD in MOSFETs with an ultrathin-SiO_xN_y/poly-Si gate stack is directly related to the gate leakage current [23].

It was also suggested that the DBIE growth at the Si/SiO₂ interface helps to alleviate the thermal runaway effect by consuming the system free energy and by reconfiguring the conductive path formed around the percolation path and in some cases, stop the SBD from evolving into a HBD [62]. It was reported that the DBIE size in the nMOSFETs is about 2 times or more than that of pMOSFETs, when compared under the same conditions of stress voltage, compliance current levels, and

failure locations [59]. The larger DBIEs in the nMOSFETs are attributed to a lower effective resistance (~ 2 times) in the nMOSFETs stressed in inversion mode at the initiation of breakdown as compared to pMOSFETs stressed under same electrical condition. The comparatively lower effective resistance results in high localized heat due to surging of a very high leakage current density through the very narrow percolation path, making favorable conditions for the growth of larger DBIE in nMOSFET.

Recently, it has been found that DBIE can occur under different stressing methodology (i.e., constant-voltage stress and constant-current stress [63]) and at a very low stressing voltage of 2.5 V [64, 65], further indicating that DBIE is a universal BD phenomenon in ultrathin gate oxide. On the other hand, the presence of polarity dependent DBIE has also been verified by conductive atomic force microscopy (C-AFM) [66, 67].

Besides the DBIE formation, several other microstructural damages such as DBIM, severe substrate defects, implosion, poly recrystallization, gate and contact plug burn out take place due to joule heating in the vicinity of breakdown spot [68]. On the basis of microstructural changes, Tung *et al.* [69] defined the different modes of the oxide breakdown and its effect on the device performance. Figure 2.11 shows the sequence of several microstructural damages with the gate leakage current which is correlated with the joule heating in the vicinity of the percolation path [23]. Figure 2.12 shows the predicted localized temperature required for the formation of the observed microstructural damages [68].

Figure 2.12. Sequence of microstructural changes with predicted localized temperature [68]. It is believed that the degree of microstructural damages increases with increasing localized temperature.

2.3 HfO₂ high- κ gate dielectric

For sub-65 node technology, materials whose dielectric constant is above 20 and compatible with complimentary metal-oxide-semiconductor process have been investigated over the past years. Many high- κ materials such as La₂O₃, ZrO₂, Ta₂O₃, HfO₂ etc. have been explored as the alternative gate dielectric to overcome leakage current problem, which is a major concern for ultrathin oxynitride gate dielectric. Figure 2.13 shows the valence and conduction band offsets on silicon substrate of all the possible high- κ candidates [70]. Among the high- κ alternatives, HfO₂ is a very promising candidate because it has good material properties ($\kappa = \sim 25$, energy band gap = 5.7 eV), has demonstrated better device characteristics and is compatible with the polysilicon gate process [5-7, 71-75]. But three major issues evident in numerous

publications [76-91] must be addressed to fabricate useful devices for CMOS circuit application using HfO_2 high- κ gate dielectrics. These are (1) high and unstable threshold voltage, (2) the large capacitive equivalent oxide thickness (CET_{inv}) difference between nMOS and pMOS, and (3) mobility degradation. A model describing V_T -instability has been proposed on the basis of experimental results [78]. It is suggested that a defect band in the HfO_2 layer located above the Si conduction band, which allows efficient charging and discharging of the defects by applying positive and negative bias, respectively, is responsible for the threshold voltage instability. It is believed that the physical origin of the defect band is due to oxygen vacancy and chlorine impurity of water related defects. It is also reported that the V_T -instability is mainly due to the creation of negative U traps by oxygen vacancy [83, 84]. Whereas, Bersuker *et al.* [85] suggested that the electron trapping (which is responsible for low temperature V_T -instability) occurs through a two-step process: resonant tunneling of the injected electron into the pre-existing defects (fast trapping) and temperature-activated migration of trapped electrons to unoccupied traps (slow trapping). On the other hand, Hobbs *et al.* [8, 90, 91] reported that Fermi pinning at the poly-Si/metal oxide interface just below the poly-Si conduction band causes high threshold voltage shift in the MOSFET devices. It is reported that the pinning occurs due to the existence of the interfacial Si-Hf bonds at poly-Si/high- κ interface. Whereas, Shimishi *et al.* [92] suggested that the creation of oxygen vacancy and subsequent electron transfer at poly-Si/high- κ interface is the main root cause of the Fermi level pinning.

Figure 2.13. Calculated conduction band and valence band offsets of various oxides on silicon [70].

On the other hand, it is reported that a residual polarization occurs due to applied voltage in HfO₂ gate dielectric, which remains long even after voltage is removed [93, 94]. This phenomenon is known as dielectric relaxation (DR), resulting in time dependent threshold voltage shift. It has also been reported that, different from SiO₂, the conduction mechanism in the HfO₂ gate dielectric is mainly governed by the Pool-Frankel mechanism, resulting in a large increase in the stress induced leakage current at high temperature and high stress voltage [95].

Mobility degradation is also a major concern for implementing the high- κ gate dielectrics in the next generation of CMOS technology [87-89]. Fischetti *et al.* [88], reported that the mobility degradation in HfO₂ gate stack is due to remote phonon scattering. On the other hand, Hiratani *et al.* [89] suggested that the mobility degradation is due to remote charge scattering.

Figure 2.14. TEM image of poly-Si/high- κ transistor with < 1.2 nm silicon recess. (a) 1.0 nm SiO₂ layer under the high- κ is removed in the all dry-removal process [96] and (b) HRTEM of nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) used in our project showing the evidence of micro-bird's beak.

The processing of HfO₂ gate dielectric device is still a challenge. It has been reported that at higher annealing temperature of 1273 K, the thin HfO₂ film becomes more crystallized, and crystallization makes it leakier due the conduction through the grain boundaries [6]. For rapid introduction of high- κ materials into the current CMOS platform, compatibility of the dielectric layer with the conventional poly-Si gate electrodes is critical. Specifically, at the gate stack patterning level, innovative approaches are required to fabricate either poly-Si or metal gate etch on high- κ dielectrics as well as selective high- κ removal from the source and drain areas [96]. For good device performance, there should be no damage to the silicon substrate, minimal recess in the silicon active area and field oxide, and no high- κ footing extending from the gate structures during etching. The wafer should also be free of resist, residues, and redeposited high- κ material. In the processing of these transistors, the gate patterning step is just followed by a high- κ removal step. Figure 2.14 (a) shows TEM micrograph of a poly-Si gate HfO₂ transistor processed by the new etch

technique developed by Schram *et al.* [96]. Figure 2.14 (b) shows the HRTEM micrograph of the HfO₂ high- κ /poly-Si gate stack MOSFET used in our study.

It was reported that careful design of material system and thermal processing steps can suppress the generation of oxygen vacancy which is considered as one of the major concerns for the Fermi level pinning and V_T -instability of HfO₂ gate stack devices [97]. Callegari *et al.* [98] reported that the mobility of the HfO₂ gate stack MOSFET can be enhanced by interface engineering. Also different annealing conditions have been proposed for better performance of the HfO₂ gate stack devices [74, 75, 80]. Bera *et al.* [99] reported that multistep metallorganic chemical vapor deposition (MOCVD) of HfO₂ can suppress the gate leakage current due to the offset of the grain boundaries and the pinholes from one layer to another.

On the other hand, the reliability study of HfO₂ gate dielectric is getting more attention by the researchers. McPherson *et al.* [100-102] reported that the ultimate breakdown strength (E_{bd}) of a dielectric material decreases with increasing κ and having a relationship of E_{bd} proportional to $\kappa^{-1/2}$. It is suggested that a very high local electric field (Lorentz-relation/Mossotti-field) in the high- κ dielectrics tends to distort/weaken the polar molecular bonds making them more susceptible to bond breakage by standard Boltzmann processes and/or by hole-capture, resulting in lower E_{bd} [100-102]. Kim *et al.* [33, 103] reported that the Weibull slopes β of the BD distribution in ultrathin HfO₂ (which is related to the reliability of the gate dielectric; larger the β value, the better reliability) for SBD and HBD are different, and β for HBD is greater than that of the SBD. It is similar to that of a progressive breakdown of SiO₂ which has different BD statistics in terms of β values [104]. It has also been reported that β of thick HfO₂ is smaller than that of SiO₂ of similar physical thickness. Whereas, β of thinner HfO₂ is similar to that of SiO₂. Furthermore, the BD is intrinsic

and can be explained by the percolation model [34]. It has been suggested that the HfO_2 may have smaller critical defect density (NBD) at BD or larger spacing between the defects where tunneling of trapped electron becomes probable in comparison with SiO_2 [34]. This would result in a smaller β with SiO_2 . On the other hand, Kauerauf *et al.* [105] analyzed β for Al_2O_3 as a function of physical thickness, and indicated that the BD in high- κ layer is dominated by an extrinsic mechanism, and process-induced defects are considered as the root cause.

Degraeve *et al.* [106] reported that the breakdown in HfO_2 high- κ / SiO_2 gate stack is stress polarity dependent due to asymmetric band-diagram. For substrate injection, steep increase in the bulk trap density of HfO_2 is likely to trigger the BD of the HfO_2 -layer, while during gate injection SiO_2 interfacial layer (IL) controls the BD. Similar stress polarity dependent BD has also been reported for other high- κ gate stacks [107, 108]. Garros *et al.* [109] observed a smaller time to breakdown during substrate injection compared to gate injection. Furthermore, for the same equivalent oxide thickness (EOT) the HfO_2 gate dielectric shows higher reliability than SiO_2 [109]. It is also reported that in the HfO_2 / SiO_2 gate stacks, the gate leakage current at low gate voltage is totally dominated by trap assisted conduction, causing no degradation [110]. Whereas, Kim *et al.* [111] reported that the reliability of the HfO_2 gate dielectric is dynamic and having a longer life time during AC stressing compared to that of DC stressing.

On the other hand, it is reported that the dominant carrier in stress induced leakage current is hole, while the electron current is predominant after the soft breakdown of the dielectric film in Hf-based high- κ gate dielectrics [112]. Furthermore, for the SILC condition, the trap generation in the high- κ stack occurs both near the conduction band edge of n^+ poly-Si and the valence band edge of Si

substrate, while the defect sites generated in the high- κ stack after SBD are located at energies near the conduction band edge of n^+ poly-Si [113]. It was also reported that the hole-injection-induced release of hydrogen from Si-H terminations causes interfacial layer breakdown, which accelerates negative bias temperature instability (NBTI) and defects due to electron-trapped oxygen vacancies are the origin of trap-assisted tunneling, causing SILC in the electron current and positive BTI (PBTI) [113]. Whereas, Houssa *et al.* [114] reported that under gate injection, electrons arrive at the Si/SiO₂ interfacial layer-interface with energy $|qV_g|$. If this energy is higher than ~ 1 -1.5 eV, electrons can induce the depassivation of Si₃≡SiH centers, producing electrically active Si₃≡Si• defects, resulting in interfacial layer breakdown.

Figure 2.15. (a) The gate leakage current evolution with stress time for the SiO₂ IL/HfAlO_x gate stacks. The up and down arrows indicate the HBD and the SBD, respectively. (b) Schematics show that the successive multiple soft breakdowns in high- κ gate stacks is due to the breakdowns in the high- κ layer, and the hard breakdown takes place only after the interfacial layer breakdown [116].

Recent research shows that the interfacial layer in the high- κ gate stacks plays a very important role in the degradation of the HfO₂ gate dielectric devices. Young *et al.* [115] reported that voltage stress-induced generation of the defects contributing to

threshold voltage instability in high- κ gate stacks occurs primarily within the interfacial SiO_2 layer. It is also reported that the gradual increase in the gate leakage is due to the occurrence of successive multiple soft breakdowns of the high- κ layer, and hard breakdown occurs only after the interfacial layer breakdown (see Fig. 2.15) [116]. On the other hand, Wang *et al.* [117] categorized the soft breakdown in the Hf-based gate dielectric into two modes-digital soft breakdown and analog soft breakdown. It was reported that the low energy dissipation in the oxide layer, trapping and emission of electrons at the traps located near the breakdown path in the high- κ gate dielectric contribute to the digital soft breakdown. Whereas, the existence of various breakdown paths in the high- κ dielectric film with high density of localized traps owing to the large Joule heating under stress is responsible for the analog soft breakdown [117].

So far, the analysis of the BD phenomenon in HfO_2 is based on pure electrical analysis. Very few reports in the literature describe the physical analysis of the BD phenomenon in HfO_2 gate dielectric. Recently, on the basis of conductive atomic force microscopy (C-AFM) analysis of HfO_2 gate dielectric, Blasco *et al.* [118] reported that the breakdown is a reversible phenomenon, i.e., the BD path can be switched on and off. It is also suggested that the $\text{HfO}_2/\text{SiO}_2$ stacks BD is controlled by the SiO_2 interfacial layer, and the HfO_2 layer has a protective effect during the BD transient, which allows the observation of the reversibility of the BD phenomenon. Furthermore, the C-AFM study also revealed different conduction regimes at different voltage ranges in virgin $\text{HfO}_2/\text{SiO}_2$ gate stacks: in the lower-field regime carrier injection through triangular HfO_2 barrier (and through trapezoidal SiO_2 barrier), whereas in the intermediate field regime the carrier injection is at energies above the HfO_2 barrier, and at large enough fields, breakdown of the gate stacks was observed

[119]. It is also found that the size of breakdown spots in the $\text{HfO}_2/\text{SiO}_2$ stacks are of the same order as the BD spots in SiO_2 -based dielectrics [119].

2.4 Metal gate electrode

An alternative gate structure under consideration is the introduction of metal gate electrodes to replace poly-Si gate electrodes for better performance of HfO_2 high- κ gate dielectric MOSFETs. Metal gate is beneficial for aggressive EOT scaling since there is no impact on the capacitance equivalent thickness (CET) due to poly-silicon gate depletion, and the complete change of the gate stack also significantly impacts the integration challenges for 65 nm and below CMOS technologies. Furthermore, metal gate electrode has added advantage of avoiding unwanted poly-Si/ HfO_2 interaction (which is responsible for the Fermi pinning and V_T -instability) [8, 90, 91, 120]. It is reported that with TiN gate electrode, HfO_2 gate stack has lower EOT value compared to poly-Si gate electrode [121]. It is also reported that the metal gate (TaN gate)/ HfO_2 transistors achieved better performance than the conventional poly-Si gate/ HfO_2 transistors under same processing conditions [96]. Furthermore, Houssa *et al.* [120] reported that the effect of NBTI is less significant in HfO_2/TaN gate stack devices compared to $\text{HfO}_2/\text{poly-Si}$ gate stack. On the basis of simulation results, Kotlyar *et al.* [122] reported that inversion mobility can be improved by the implementation of high- κ /metal gate stacks in place of high- κ /poly-Si gate stacks. Yu *et al.* [123] reported that generation of extrinsic defects (which resulting in metal workfunction instability due to Fermi pinning) upon annealing is less significant for metal gate on HfO_2 compared to metal gate on SiO_2 gate dielectric.

On the other hand, it is reported that the workfunction of metal gate depends on the gate dielectric materials due to dipole formation at the interface of the gate electrode and gate dielectric, and the phenomenon could be explained by metal induced gap states (MIGS) theory [124-126]. Samavedam *et al.* [127] reported that a small change at the metal/dielectric interface could result in significant change on the metal workfunction due to Fermi pinning at interface states. Thus for improved performance of the device, search for suitable metal gate electrode and dielectric material and appropriate processing conditions are major task to make the effective workfunction of metal gate electrode near to nMOSFET and pMOSFET. For the conventional bulk CMOS devices, metal gate must have the workfunction near (< 0.2 eV) the conduction band and valence band edges of Si. For non-bulk devices, the work function is required to be ~ 0.3 eV above and below the mid-gap level [128].

Recently, a “dual metal gate” approach has attracted attention to improve the CMOS performance [129], as opposed to mid-gap metals, such as TaN, TiN to avoid high threshold voltage of the device. It is suggested that for CMOS integration, metals with “tunable” work function is suitable for metal gate applications. Various alloy systems such as metal alloys, silicides, and nitrides have been investigated as the gate electrode for workfunction “tunability” [130-135]. Both alloying and implantation techniques have been considered as possible techniques to tune the workfunction of the metal gate electrode. Furthermore, it is reported that Fermi level pinning can be controlled by dual gate electrode [130-135]. In addition, Narayanan *et al.* [136] reported that CVD deposited dual gate electrode on HfO_2 high- κ gate dielectric provides better hole mobility and excellent device performance.

On the other hand, many researchers suggested that stacked metal layer such as Al/TaN, Ta/TaN, TaN/Ti/HfN/TiN, Ta/HfN/TaN, TiN/TaN, Ti/HfN/TaN,

Ti/Ta/HfN/TaN, HfN/Ti/TaN etc. can be used as the gate electrode for CMOS system for tuning the workfunction by choosing the suitable thickness of the thin metal layers and processing conditions [137-139]. Jeon *et al.* [140] proposed that the work function “tuning” in bi-metal layers are due to a drastic change of the electron density in thin continuous metal layer in direct contact with the bulk metal.

Figure 2.16. Gate leakage current evolution with stress time in high- κ /metal gate stack MOSFETs [35].

Very few reports in the literature discussed about the failure mechanisms in metal gate electrode MOS devices. Recently, Palumbo *et al.* [141] reported that high degradation rate is very common in SiO_2 breakdown with tungsten gate electrode MOS capacitors. It has also been reported that the large abrupt gate leakage current increase associated with BD in high- κ /metal gate stack MOSFETs (see Fig. 2.16) compared to poly-Si gate electrode is an intrinsic property of the metal gate electrode. The results raise a potential limitation for the reliability of metal gate-based devices [35]. Degraeve *et al.* [142] reported the existence of two phases of breakdown in high- κ /metal gate stack transistors; the transistor first suffers progressive/digital soft

breakdown before an abrupt increase in the gate leakage current resulting in catastrophic failure of the transistor (see Fig. 2.17). But the exact mechanism responsible for BD in metal gate stacks remains unclear.

(a)

(b)

Figure 2.17. (a) Example of the wear-out phase ('digital soft breakdown') observed before the final hard breakdown occurs in metal gate stack transistors. (b) The schematic drawing defines the creation time of a breakdown path, t_c , a wear-out phase, t_{pw} , and an abrupt breakdown, t_{HBD} . In ultrathin SiO_xN_y /poly-Si gate stacks, wear-out ended with a gradual current run-away limited by resistance effects (dashed line). In metal gate stack devices, the current run-away phase is always very fast [142].

2.5 Summary

The advantages, concerns and breakdown mechanisms in SiO₂/poly-Si gate stacks, HfO₂ high- κ /poly-Si gate stacks and metal gate stacks are reviewed. It is realized that most of the breakdown models describing the dielectric degradation are based on electrical analysis results, and are not sufficient to explain all the experimental data. In HfO₂ high- κ /poly-Si gate stacks and metal gate stacks, the dielectric degradation is more complicated due to several new intrinsic properties of high- κ and metal gate and its dependency on the processing conditions. Hence, the electrical analysis results are not sufficient to explain the breakdown mechanism in HfO₂ high- κ /poly-Si gate stacks and metal gate stacks. In order to better understand the dielectric degradation and its impact on the device and the circuit performance, physical analysis of the breakdown mechanism(s) is needed.

Chapter 3 EXPERIMENTS

3.1 Introduction

In order to reveal the failure mechanisms in HfO₂ high- κ gate stack MOSFETs, both electrical and physical analysis have been performed. This chapter describes the details of the devices, electrical stressing methods, and electrical and physical analysis equipment used.

3.2 Devices used in study

In this project, *small* gate area (i.e., gate width (W) $\times$ gate length (L) $\leq 1 \mu\text{m}^2$ [143]) SiO_x interfacial layer/HfO₂ high- κ /poly-Si gate stack nMOSFETs, and SiO_x interfacial layer/HfO₂ high- κ /TaN/TiN gate stack n/pMOSFETs were studied. Ultrathin SiO_xN_y and semi-high- κ Si₃N₄ nMOSFETs were also used for comparison. The details of the devices are listed in Table 3.1. Figure 3.1 shows the respective TEM micrographs of the poly-Si and metal gate stack MOSFETs listed in Table 3.1.

(a)

(b)

Figure 3.1. TEM cross-sectional micrographs of SiO_x IL/ HfO_2 high- κ /poly-Si gate stack and SiO_x IL/ HfO_2 high- κ /TaN/TiN gate stack MOSFETs used in our study. (a) SiO_x IL/ HfO_2 high- κ /poly-Si gate stack. (b) SiO_x IL/ HfO_2 high- κ /TaN/TiN gate stack. The inserts show a cross-section of the MOSFETs.

Table 3.1. Details of the devices used in study.

Devices	Device dimensions (gate width (nm) and gate length (nm))	Equivalent oxide thickness (EOT) (nm)	Physical thickness revealed by TEM
Co-silicided nMOSFETs having SiO _x interfacial layer/ HfO ₂ high- κ /poly-Si gate stack	W = 250 - 2000 L = 50 - 500	EOT = 2.1	4.4 nm of HfO ₂ and 0.6 - 0.8 nm of SiO _x interfacial layer
Ni-silicided n/pMOSFETs having SiO _x interfacial layer/ HfO ₂ high- κ / TaN/TiN gate stack	W = 250 - 2000 L = 50 - 500	EOT = 1.7 – 2.36	3.3 nm – 4.8 nm of HfO ₂ and 1.3 - 1.5 nm of SiO _x interfacial layer
Co-silicided nMOSFETs having silicon oxynitride (SiO _x N _y) gate dielectric	W = 150 - 300 L = 150 - 300	EOT = 2.0	2.1 nm
Co-silicided nMOSFETs having silicon nitride (Si ₃ N ₄) gate dielectric	W = 300 and 600 L = 180	EOT = 2.0	2.9 nm

3.3 Electrical characterization of unstressed devices

The equivalent oxide thickness of the various gate stacks listed in Table 3.1 has been measured from the corresponding capacitance-voltage (C - V) characteristics using a CVC5 commercial software with poly-Si depletion and quantum mechanical extraction. Figures 3.2 (a) and (b) show two examples of typical C - V characteristics (measured using a HP 4285 A precision LCR meter) of SiO_x IL/ HfO₂ high- κ /poly-Si gate stack and SiO_x IL/ HfO₂ high- κ / TaN/TiN gate stack MOS capacitors ($W \times L = 100 \times 100 \mu\text{m}^2$), respectively. The measured EOT are listed in Table 3.1.

(a)

(b)

Figure 3.2. C-V characteristics of SiO_x IL/ HfO_2 high- κ /poly-Si gate stack and SiO_x IL/ HfO_2 high- κ /TaN/TiN gate stack MOS capacitors ($W \times L = 100 \times 100 \mu\text{m}^2$). (a) Two SiO_x IL/ HfO_2 high- κ /poly-Si gate stack MOS capacitors. The EOT of these devices is 2.1 nm after poly depletion and quantum mechanical extraction. (b) Two SiO_x IL/ HfO_2 high- κ /TaN/TiN gate stack MOS capacitors. The EOT of these devices is 1.95 nm after quantum mechanical extraction.

In order to verify the performance of the unstressed MOSFETs, the drain/source saturation currents, gate leakage current and transconductance were also measured using either Agilent 4156C precision semiconductor parameter analyzer

connected to a Suss probestation (PA 200) or HP 4156A precision semiconductor parameter analyzer connected to a Cascade Microtech probestation (Model 12000) (see Fig. 3.3). Figures 3.4, 3.5 and 3.6 show the common drain/source saturation currents, gate leakage currents and transconductance of unstressed HfO_2 /poly-Si gate stack and HfO_2 /TaN/TiN gate stack MOSFETs, respectively. It can be seen that the MOSFETs used in the study have high source/drain saturation current (see Fig. 3.4), very low gate leakage current (see Fig. 3.5) and high maximum value of transconductance (see Fig. 3.6). The threshold voltage (measured using maximum transconductance method) of the HfO_2 high- κ /poly-Si gate stack and HfO_2 high- κ /TaN/TiN gate stack MOSFETs are ~ 0.45 V and ~ 0.55 V, respectively. Only HfO_2 high- κ gate MOSFETs having good electrical performance were used in our project for further failure mechanisms study.

(a)

(b)

(c)

Figure 3.3. Equipment used in the MOSFET characterization and stressing. (a) Cascade Microtech probestation (model 12000), (b) semiconductor parameter analyzer HP 4156A, and (c) Temptronic Corporation temperature controller (TP 03000A – 2300 – 2).

(a)

(b)

Figure 3.4. Drain/Source current characteristics of the unstressed SiO_x IL/ HfO₂ high-κ/ poly-Si gate stack and SiO_x IL/ HfO₂ high-κ/ TaN/TiN gate stack nMOSFETs ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$). (a) SiO_x IL/ HfO₂ high-κ/ poly-Si gate stack (EOT = 2.1 nm), (b) SiO_x IL/ HfO₂ high-κ/ TaN/TiN gate stack (EOT = 1.95 nm).

Figure 3.5. I_g - V_g characteristics of the unstressed SiO_x IL/ HfO₂ high-κ/ poly-Si gate stack and SiO_x IL/ HfO₂ high-κ/ TaN/TiN gate stack nMOSFETs ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) shown in Fig. 3.4. The fluctuation in the gate leakage current is due to the system noise as the gate leakage current is very low of the order of 10^{-13} A.

Figure 3.6. I_d - V_g characteristics ($V_d = 0.1$ V, while source and substrate grounded) and transconductance of the unstressed poly-Si and TaN/TiN gate nMOSFETs shown in Fig. 3.4. (a) SiO_x IL/ HfO_2 high- κ / poly-Si gate stack, (b) SiO_x IL/ HfO_2 high- κ / TaN/TiN gate stack.

3.4 Constant voltage stress (CVS)

In this method, MOSFETs were stressed by a constant voltage ($V_{gstress}$) applied to the gate electrode in inversion or accumulation mode at 298 - 423 K using either Agilent 4156C or HP 4156A precision semiconductor parameter analyzer (see Fig. 3.3). In this arrangement, a suitable constant voltage $V_{gstress}$ was applied at the gate of the n/pMOSFETs, while keeping the source, drain and substrate terminals grounded in

the inversion mode or accumulation mode stressing. In some of the accumulation mode CVS stressing, the substrate was grounded, while keeping the source and drains floating. During the stressing, a gate leakage compliance current limit (I_{gl}) setting was used to control the gate leakage current after a gate dielectric breakdown or to control the post-BD gate leakage current evolution. The algorithm developed by our collaborator in IMEC, Belgium shown in Fig. 3.7 was used for the determination of a suitable stressing voltage.

Figure 3.7. Flow chart of $V_{gstress}$ determination.

3.4.1 Determination of average breakdown voltage

As shown in Fig. 3.7 some of the devices are first stressed by a quick voltage ramping starting from 0 V with an increment of 0.1 V in 0.1 s by setting a gate leakage compliance current limit of 10 μ A. The voltage at which 63% of the devices reach the compliance current limit or encounter a breakdown is considered as the

average breakdown voltage (V_{BDavg}). V_{BDavg} can be shown to correspond to the time-to-breakdown ($t_0 \sim 0.1$ s) in the constant voltage stress at V_{BDavg} .

Figure 3.8. Degradation in acceleration factor with V_g in oxide [144].

3.4.2 Determination of $V_{gstress}$

The time-to-BD, t_{BD} , is maintained in the range of 100 to 1000 s. So the stressing voltage should be lower than V_{BDavg} . Hence, we adopted the formula, suggested by Berman *et al.* [10], for the calculation of a suitable stressing voltage.

The formula for the calculation of $V_{gstress}$ is expressed as:

$$\ln t_{BD} = \ln t_0 + \beta (V_{BDavg} - V_{gstress}) \quad (3.1)$$

where t_{BD} is the time-to-BD at $V_{gstress}$, t_0 is the time-to-BD at V_{BDavg} (in our case $t_0 = 0.1$ s) during CVS, and β is the voltage acceleration factor which is dependent on temperature, applied voltage, area and thickness of device. Figure 3.8 was used to estimate the value of β . For our requirement of t_{BD} of 100 - 1000 s, $V_{gstress}$ in the range

of (+/-) 3.0 V – (+/-) 4.5 V is considered as an appropriate voltage for various gate stacks used in our study.

3.5 Successive constant voltage stress (SCVS)

In the SCVS method, a suitable $V_{gstress}$ was applied to the transistors until a breakdown occurred at a relatively low gate leakage compliance current limit of typically less than 10 μ A. Subsequently, the stress was continued by successively (or stepwise) relaxing I_{gl} to higher values while keeping the stress voltage unchanged. The temperature of the stressing was kept at 373 K. This method is useful to study the evolution of different stages of breakdown, the associated microstructural damages, and the effect of the post-BD evolution of the gate leakage current on the device performance.

3.6 Two-step stress

In the two-step stress methodology [55, 144], MOSFETs were stressed under CVS in either inversion or accumulation mode at a high $V_{gstress}$ while keeping I_{gl} of 500 nA – 10 μ A at 373 K. Once the gate leakage current evolves to a pre-set I_{gl} due to a gate oxide breakdown, the stressing was continued at a lower $V_{gstress}$ with a higher I_{gl} . This method is useful to study the breakdown transient during progressive breakdown and the post-BD degradation rate of the gate leakage current at different $V_{gstress}$. Figure 3.9 shows the flow chart of the two-step stress method.

Figure 3.9. Flow chart showing the two-step stress methodology.

3.7 Multiple-stage stress

Multiple-stage stress methodology was used to study the post-BD stability of the breakdown path. In this method, samples were stressed under inversion or accumulation modes CVS with a high $V_{gstress}$ and a low I_{gl} of 500 nA – 10 μA at 373 K. Once the gate leakage current reached the pre-set I_{gl} upon breakdown, the device was stressed subsequently at a lower voltage range of $V_{gstress} = (+/-) 1.6 \text{ V} - (+/-) 2.5 \text{ V}$ ($|\Delta V_{gstress}| = 0.1 \text{ V}$) for a duration of 300-500 s at each subsequent $V_{gstress}$. Figure 3.10 shows the flow chart of the multiple-stage stress methodology.

Figure 3.10. Flow chart showing the multiple-stage stress methodology.

3.8 Electrical characterization

The post-breakdown leakage currents (I_g , I_d , I_s and substrate current (I_{sub})) with time were monitored during various stressing conditions. All the pre- and post-BD I - V characteristics were measured in a temperature range of 298 – 423 K. The post-BD transconductance (i.e., $\Delta I_d / \Delta V_g$), post-BD effective gate resistance (i.e., R_{geff}) @ $V_g = 1.5$ V (equation (2.8)), breakdown location (equation (2.7)), and degradation rate (i.e., dI_g/dt) [55, 145] were measured.

3.9 Physical analysis

It is necessary to know the microscopic nature of the defects/microstructural changes which cause the breakdown or develop during the breakdown event for a better understanding of the failure mechanisms in the HfO₂ high- κ /poly-Si gate stack and HfO₂ high- κ /metal gate stack MOSFETs. TEM/HRTEM analysis of the

breakdown spots was performed after stressing of the devices to study the microscopic nature of microstructural changes physically. EDS/EELS [146, 147] technique was used to study the elemental composition, the chemical composition and the atomic bonding states of the compounds at the breakdown spot.

Figure 3.11. Schematic showing the top view of a MOSFET. It can be seen that for a *narrow* width device, the probability of capturing the BD defects in the final TEM lamella of about 100 nm of thickness after thinning is higher than 90%.

Figure 3.12. FEI Model 4022 2624 3531 FIB was used to prepare the samples for TEM analysis.

3.9.1 TEM/EDS/EELS sample preparation by focus ion beam

For the TEM/EDS/EELS analysis, the thickness of the TEM lamella should be around 100 nm. In order to facilitate the TEM analysis, very *narrow* transistors consisting of widths of 250 nm or less were used. Using this method, the probability of capturing BD defects in the final TEM lamella of about 100 nm of thickness is more than 90 percent (see Fig. 3.11).

Precision TEM sample preparation was used to prepare the TEM lamella of the thickness of about 100 nm. Only focused ion beam (FIB) technique was able to meet this requirement as very small devices located at specific locations were used in our study. The working mechanism of FIB is based on the sputtering of the sample material by highly energized Ga^+ ions in the presence of electric and magnetic field. The Ga^+ ions can be well focused and controlled by the FIB equipment electric and magnetic field. Hence, the minimum beam size can be scaled down to a very narrow range. Figure 3.12 shows the FIB equipment used in our study.

In the precision TEM sample preparation, both “pre-thinning” and “lift-off” methods can be used. In the pre-thinning method, the area containing the transistor of interest is pre-thinned by mechanical polishing to $\sim 30\ \mu\text{m}$. After that, the specimen was mounted onto a copper ring to enhance the sample mechanical hardness. Then the specimen was fixed on a specific FIB sample holder and logged into the FIB machine. FIB was used to further thinning the specimen to the location of interest from both sides of the membrane to get a TEM lamella of thickness of about 100 nm.

Figure 3.13. Electron beam micrographs show FIB thinning of a specimen and detachment of the required TEM lamella from the rest of the specimen during the “lift-off” sample preparation method. (a) Electron beam micrograph shows two transistors, (b) deposition of platinum (Pt) protective layer on the area of interest, (c) FIB thinning of the specimen from both sides to get the required TEM lamella, (d) three cuts of the thinned specimen using FIB to detach the required TEM lamella, (e) TEM lamella detached only from one corner, and (f) the fully detached TEM lamella.

On the other hand, the “lift-off” sample preparation method uses FIB thinning of the specimen from both sides of the target location to a thickness of about 100 nm without pre-mechanical polish. Then the required TEM lamella was detached from the rest of the specimen using FIB. After that, the detached TEM lamella was lifted-off using a tungsten (T-4-10) probe and kept on a carbon film, which is mounted onto a copper ring. Figures 3.13 and 3.14 show the different stages of the “lift-off” sample preparation method. In our study, the samples for the TEM analysis were mainly prepared by the “lift-off” sample preparation method.

Figure 3.14. Optical images showing the process of the lifting-off of the TEM lamella to a copper ring using tungsten (T-4-10) probe. (a) Probe was being approached to the TEM lamella, (b) TEM lamella sucked by the probe, (c) TEM lamella lifted-off by the probe, (d) TEM lamella kept on the carbon film.

3.9.2 TEM/EDS/EELS/Elemental dot mapping analysis

After the FIB sample preparation of MOSFETs suffered gate dielectric breakdown, microstructural analysis was done by a Philips CM 200FEG TEM shown in Fig. 3.15. The linear resolution of the TEM was $1.6 \text{ \AA}$, smaller than the atomic distance between the two silicon atoms in the adjacent $\langle 111 \rangle$ direction ($\sim 3.135 \text{ \AA}$). Thus the analysis of the microstructural defects in the vicinity of the breakdown spot can be as accurate as an atomic layer.

Gatan Image Filter (GIF) mapping was carried out to map the elemental distortion of the species of interests, such as oxygen, cobalt, titanium, tantalum, nickel, hafnium, nitrogen, and silicon in our study. EDS/EELS technique was used to study the chemistry of the microstructural defects at the breakdown spot for better understanding of the failure mechanism.

Figure 3.15. Philips CM 200FEG TEM was used for all the TEM experiments in the project.

(a)

(a)

Figure 3.16. (a) Schematic showing the HfO_2 /poly-Si gate stack nMOSFET having source/drain extension of 20 nm with a 5 nm of HfO_2 gate dielectric protrusion. (b) HRTEM of an unstressed nMOSFET showing a “L-shape”-like profile near a poly-Si edge used in our study.

3.10 Simulation

In order to support the experimental results, computer simulation was carried out using T-SUPREM4 and MEDICI. nMOSFET having 4.4 nm of HfO_2 high- κ ($\kappa=20$) gate dielectric with 0.6 nm of SiO_2 ($\kappa=3.9$) interfacial layer was created using the T-SUPREM4 simulator. The poly-Si (doping of 10^{21} cm^{-3} and dielectric constant of 11.7) gate length of the simulated nMOSFET was kept at 90 nm with a

source/drain extension of 20 nm. In order to simulate the nMOSTET used in our study (see Fig. 3.16), the developed nMOSFET also consists of a “L-shape”-like profile near the poly-Si edge with a 5 nm of HfO₂ gate dielectric protrusion. The SiO₂ spacer of dielectric constant of 3.9 was used.

The effect of the “L-shape”-like profile near the poly-Si edge on the potential and electric field profile at the poly-Si/HfO₂-interface and middle of the interfacial layer was studied under both inversion and accumulation mode CVS using the MEDICI commercial software. The simulation results will be discussed in Chapter 4.

3.11 Summary

Various methodologies of the gate dielectric stressing have been discussed in this chapter. The pre- and post-breakdown device electrical characterization methodologies have also been discussed. The precision TEM/EDS/EELS sample preparation methods are described. The parameters of the high- κ /poly-Si gate stack nMOSFET simulation performed using a T-SUPREM4 simulator are discussed in here.

Chapter 4 FAILURE MECHANISMS/DEFECTS IN HfO₂ HIGH- κ /POLY-SI GATE STACK MOSFETS

4.1 Introduction

It has been reported that the breakdown phenomenon in HfO₂/poly-Si gate stacks, which is considered as the appropriate candidate for future CMOS technologies [5-7, 71-76], and other high- κ gate stacks may be different from the BD phenomenon in ultrathin SiO_xN_y/poly-Si gate stacks [33, 34, 105-111].

Recently, it has been found that *polarity*-dependent dielectric-breakdown-induced epitaxy DBIE (which was revealed by TEM/EDS/EELS/EELS elemental dot mapping analysis) is one of the major universal failure defects responsible for gate dielectric breakdown evolution in SiO_xN_y/poly-Si and Si₃N₄/poly-Si gate stacks [23-26, 61-65, 68, 69]. The hardness of the BD in SiO_xN_y/poly-Si and Si₃N₄/poly-Si has also been categorized as SBD, SBD+DBIE, HBD+DBIE on the basis of the growth of DBIE [26, 61]. Furthermore, it was found that the DBIE growth helps to control the thermal runaway phenomenon and, in some cases, saves the device from catastrophic failure, i.e., stop the SBD from evolving into a HBD [62]. Other structural damage associated with HBD in ultrathin gate dielectrics are DBIM, silicide/poly-Si

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intermixing and regrowth, silicon substrate damage, total epitaxy of transistor, implosion, and contact plug failure [24, 68, 69].

So far all the physical investigations of the breakdown phenomenon have been done on SiO_xN_y/poly-Si and Si₃N₄/poly-Si gate stack MOSFETs. The physical defects associated with gate dielectric breakdown in high- κ /poly-Si gate stacks, however, remain unknown.

In this chapter, the common and new failure mechanisms/defects associated with SiO_x interfacial layer/HfO₂ high- κ /poly-Si gate stack MOSFETs are described and compared to those found in the SiO_xN_y/poly-Si and Si₃N₄/poly-Si gate stacks. A comprehensive breakdown model describing the breakdown mechanism in the HfO₂/poly-Si gate stack MOSFETs is proposed.

4.2 Comparison of common failure mechanisms/defects between HfO₂/poly-Si gate stacks and SiO_xN_y/poly-Si and Si₃N₄/poly-Si gate stacks

4.2.1 Polarity-dependent dielectric-breakdown-induced epitaxy

Figure 4.1 shows the TEM micrograph of a SiO_x/HfO₂ high- κ /poly-Si gate stack nMOSFET stressed in inversion mode CVS with I_{gl} of 50 μ A. It can be seen that the DBIE hillock from the substrate side has ruptured the HfO₂ gate dielectric, creating a direct contact between the silicon substrate and poly-Si gate. Figure 4.2 shows the pre- and post-BD I - V characteristics of the device discussed in Fig. 4.1. Similar post-BD I_{ds} - V_{ds} and I_{sd} - V_{sd} characteristics confirm that the breakdown is near the channel center [69]. Based on the post-BD I_d and I_s current separation

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measurement, the electrically measured breakdown location (measured using equation (2.7)) of $0.59 L$, where L is the effective channel length, correlates well with the physical breakdown location shown in the insert of Fig. 4.1. These electrical and physical analysis results are similar to those obtained from ultrathin SiO_xN_y and Si₃N₄ gate dielectrics (Fig. 4.3 and Refs. 23-26, 61-65, 68, 69).

Figure 4.1. TEM micrograph of a SiO_x/HfO₂ high- κ /poly-Si gate stack nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed in inversion mode CVS (i.e., substrate injection) with $V_{g\text{stress}}$ of 3.6 V and $I_{gl} = 50 \mu\text{A}$ at 373 K. The dotted circle in the insert shows that the breakdown location is near the channel center.

Figure 4.4 shows the HRTEM micrographs of two examples of DBIEs associated with breakdowns in high- κ /poly-Si gate stack transistors under inversion mode CVS. Similar to the DBIEs in ultrathin SiO_xN_y and Si₃N₄ gate dielectrics of poly-Si gate MOSFETs, the Si hillocks nucleate and grow at the cathode end of the stress electrode in the vicinity of the breakdown path. The HRTEM lattice imaging analysis confirms that the epitaxial Si hillocks are extended from the Si crystal of the substrate, which is the cathode electrode during the inversion mode stressing of the device.

(a)

(b)

Figure 4.2. Pre- and post-BD I - V characteristics of the nMOSFET shown in Fig. 4.1. (a) Drain characteristics I_{ds} - V_{ds} , (b) source characteristics I_{sd} - V_{sd} . Symmetrical post-BD drain and source characteristics also indicate that the breakdown is located near the channel center.

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(a)

(b)

Figure 4.3. TEM micrographs of nMOSFETs failed with HBD in inversion mode CVS. (a) A DBIE located near the gate corner of a 2.0 nm SiO_xN_y/poly-Si gate stack ($W \times L = 0.3 \times 0.3 \mu\text{m}^2$) after an inversion stress with a $V_{g\text{stress}}$ of 3.8 V. (b) Si₃N₄/poly-Si gate stack ($W \times L = 0.3 \times 0.18 \mu\text{m}^2$) with EOT of 2.0 nm failed at I_{gl} of 360 μA with $V_{g\text{stress}}$ of 3.8 V. The insert shows the BD spot marked by the dotted circle. The DBIE situated near the corner can be seen.

Unlike HBD in SiO_xN_y/poly-Si and Si₃N₄/poly-Si gate stack MOSFETs (in which there is always a well aligned DBIE to the Si [111] direction [23-26, 61, 68, 69] formed at the breakdown spot, and DBIE makes a direct contact between the silicon

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substrate and poly-Si gate (see Figs. 4.3(a) and 4.3(b))), in some HBD cases of the SiO_x/HfO₂ high- κ /poly-Si gate stacks, only the interfacial layer is ruptured by the silicon epitaxy without any visible damage of the HfO₂ gate dielectric (see Fig. 4.5). It may be due to the higher mechanical strength and relatively high melting point of HfO₂ (~ 3050 K) compared to that of SiO_xN_y (~ 1986 K) and Si₃N₄ (~ 2173 K) gate dielectrics. Therefore, it is mechanically difficult to push up the HfO₂ gate dielectric to form a direct contact between the silicon substrate and poly-Si gate by a DBIE hillock, in the vicinity of the breakdown spot, resulting in only the interfacial layer breakdown. It is also postulated that in these cases, the HfO₂ gate dielectric has probably been ruptured by the silicon epitaxy, but it is not easy to detect in the TEM analysis due to a higher shadowing effect of the thicker surrounding HfO₂ lattice in the vicinity of the breakdown spot.

Figure 4.4. HRTEM micrographs of the breakdown spots of two HBD SiO_x/HfO₂ high- κ /poly-Si gate stack nMOSFETs ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed in inversion mode CVS at 373 K. (a) $V_{g\text{stress}} = 3.8$ V, (b) $V_{g\text{stress}} = 3.3$ V. The DBIE crystal orientation is well aligned with the silicon [111] direction.

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(a)

(b)

Figure 4.5. TEM micrographs of two SiO_x/HfO₂ high- κ /poly-Si gate stack HBD nMOSFETs ($W \times L = 0.25 \times 0.05 \mu\text{m}^2$ and $W \times L = 0.25 \times 0.5 \mu\text{m}^2$) failed with HBD in inversion mode CVS. (a) nMOSFET ($W \times L = 0.25 \times 0.05 \mu\text{m}^2$) failed at $I_{gl} = 1 \text{ mA}$ with $V_{gstress}$ of 3.8 V. The insert shows the BD spot marked by the dotted circle. (b) nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) failed at $I_{gl} = 400 \mu\text{A}$ with $V_{gstress}$ of 3.8 V.

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Figure 4.6 shows the leakage current evolutions of a transistor during accumulation mode stress. Two gate dielectric breakdowns can be seen from the leakage current evolutions characteristics – the first breakdown is near the channel center (i.e., at $0.49 L$ measured using equation (2.7)) and the second breakdown is at the drain side of the transistor (i.e., $0.96 L$) (see Fig. 4.6). A breakdown event was defined by observing a sudden abrupt increase in the gate leakage current during CVS. The corresponding TEM micrograph of the transistor shows two breakdown spots – one near the channel center (i.e., Spot A) and the another at the drain side (i.e., Spot B) of the MOSFET (see Fig. 4.7 (a)). The gate leakage current evolution as shown in Fig. 4.6 corresponds well with the physical analysis results (see Fig. 4.7 (a)). Figure 4.7 (b) shows a HRTEM micrograph of the BD Spot A. It could be seen that the lattice orientation within the HfO₂ gate dielectric in the vicinity of the BD area is the same as that of the poly-Si gate electrode. Figure 4.7 (c) shows a TEM micrograph of BD Spot B. A large DBIE from the poly-Si gate electrode without creating any severe damage in the HfO₂ high- κ gate dielectric can be seen in the spacer region. The root cause may be due to the higher melting point and higher mechanical strength of HfO₂ than the spacer material. Hence, the the DBIE hillock can easily rupture the spacer material than the HfO₂ gate dielectric. It can be also seen that the Co-silicide is missing in the region near by the breakdown Spot B (see Fig. 4.7 (c)). The mechanisms behind the Co-silicide migration will be discussed in Chapter 6.

Figure 4.6. Leakage currents evolution with stress time of a SiO_x/HfO₂ high- κ /poly-Si gate stack nMOSFET failed during accumulation mode CVS with $V_{gstress}$ of -4.0 V. There was no I_{gl} set in this experiment. The dotted circles show two breakdown events (i.e., BD1 and BD2).

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(a)

(b)

(c)

Figure 4.7. TEM micrographs of the nMOSFET shown in Fig. 4.6. (a) Two breakdown spots (labeled as A and B shown in the circles) can be seen over the 0.5 μ m channel length. HRTEM of breakdown spots, (b) Spot A, (c) Spot B. The DBIE hillocks from the poly-Si gate electrode can be observed.

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Figure 4.8 shows the pre- and post-BD I - V characteristics of the nMOSFET shown in Fig. 4.6. Similar to the case of SiO_xN_y/poly-Si and Si₃N₄/poly-Si gate stacks BD [61, 63-65, 68, 69], and the case of the breakdown in inversion mode stress high- κ gate stacks (see Fig. I.1 in Appendix I), an asymmetry between the drain (resistive-like) and source (transistor-like) post-BD I - V characteristics is seen (see Fig. 4.8). The physical results (see Fig. 4.7) correspond well with the electrical results (Fig. 4.8), in which it can be clearly seen that the BD has a larger impact on the drain region characteristics (i.e., Spot B) (see Fig. 4.7 (c)). The transistor-like post-BD I - V characteristics at the source side as shown in Fig. 4.8 (b) indicate that the damage is not catastrophic at Spot A.

The dielectric-breakdown-induced epitaxy formation from the poly-Si gate electrode (i.e., cathode side) in accumulation mode stress (see Figs. 4.7 (b) & 4.7 (c)), and from the Si-substrate electrode (i.e., cathode side) in the inversion mode stress (see Figs. 4.1, 4.4 and 4.5) indicates that the DBIE formation in HfO₂ high- κ gate dielectrics is also *polarity dependent* and nucleates only on the cathode side of the stressed transistor. This observation is identical to those for SiO_xN_y and Si₃N₄ ultrathin gate dielectrics [23-26, 61-65, 68, 69]. Hence, *thermal-electro-migration* effects [25] are again postulated to be the main driving force responsible for the DBIE defect formation in the HfO₂ gate dielectrics during the BD transient. In addition, similar to SiO_xN_y/poly-Si gate stacks [64, 65], DBIE in the HfO₂/poly-Si gate stacks is found at both low and high $V_{gstress}$ (see Figs. 4.1, 4.4, 4.5 and 4.7).

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(a)

(b)

Figure 4.8. Pre- and post-BD I - V characteristics of a nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) shown in Fig. 4.6. (a) I_{ds} - V_{ds} , (b) I_{sd} - V_{sd} .

4.2.2 Dielectric-breakdown-induced migration

Another common failure mechanism seen in oxynitride and high- κ gate stacks is DBIM. Figures 4.9 and 4.10 show three examples of DBIM of Co-silicide in SiO_x/HfO₂/poly-Si gate stack *narrow* nMOSFETs. Similar to the oxynitride gate stack [24, 68], DBIM has been observed during both inversion (Fig. 4.10 (a)) and accumulation modes (Figs. 4.9 and 4.10 (b)) CVS in the high- κ gate stack MOSFETs. Figure 4.9 shows that the migration of cobalt happens only on the source side which is closer to the original breakdown spot and makes a direct contact between the gate and source electrode. The resistive-like post-BD *I-V* characteristics of the source (see Fig. 4.11 (a)) correlate well with the physical analysis results shown in Fig. 4.9 (b). In addition, the negligibly small post-BD *I-V* characteristics of the drain (see Fig. 4.11 (b)) confirm the formation of an amorphous insulating layer over the entire channel region due to a thermal joule heating during the breakdown event, revealed by TEM micrograph of the device shown in Fig. 4.9 (a). On the other hand, all the Co materials from the drain side of the MOSFET shown in Fig. 4.10 (a) have migrated to the source and gate, forming a “Co-based metal gate” and leaving no CoSi₂ on the drain side. Both DBIE and DBIM have been seen together in the planar TEM micrograph of a SiO_x/HfO₂/poly-Si gate stack nMOSFET stressed under accumulation mode CVS (Fig. 4.10 (b)). The mechanism responsible for the DBIM will be discussed in Chapter 6.

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(a)

(b)

(c)

Figure 4.9. (a) TEM, (b) TEM and EELS Co-mapping of source side and (c) TEM and EELS elemental Co-mapping of drain side of a SiO_x/HfO₂/poly-Si narrow nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed in accumulation mode with $V_{g\text{stress}} = -3.8 \text{ V}$ keeping I_{gl} of $300 \mu\text{A}$. A Gatan package commercial software three window is used for elemental mapping. The scale for the elemental mapping is kept identical to TEM micrograph.

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(a)

(b)

Figure 4.10. (a) TEM and EELS elemental Co-mapping of a SiO_x/HfO₂/poly-Si gate stack MOSFET ($W \times L = 0.25 \times 0.05 \mu\text{m}^2$) stressed under inversion mode with $V_{g\text{stress}} = 3.5 \text{ V}$ and $I_{gt} = 300 \mu\text{A}$. A Gatan package commercial software three window is used for elemental mapping. The scale for the elemental mapping is kept identical to TEM micrograph. (b) Planar TEM micrograph of another SiO_x/HfO₂/poly-Si narrow nMOSFET ($W \times L = 2.0 \times 0.5 \mu\text{m}^2$) stressed in accumulation mode CVS with $V_{g\text{stress}} = -3.6 \text{ V}$ and $I_{gt} = 600 \mu\text{A}$. Both DBIE and DBIM co-exist after a breakdown event. The inset shows a larger view, including both source/drain and gate, of the MOSFET.

(a)

(b)

Figure 4.11. Pre- and post-BD I - V characteristics of the nMOSFET shown in Fig. 4.9. (a) I_{sd} - V_{sd} , (b) I_{ds} - V_{ds} .

Figure 4.12. Evolution of the leakage current (I_g , I_s , I_d and I_{sub}) with stressing time of a SiO_x/HfO₂/poly-Si gate stack nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed in inversion mode CVS with $V_{gstress}$ of 3.8 V and I_{gl} of 5 mA. BD1, BD2 and BD3 show 3 BD events of the same MOSFET. A breakdown event was defined by sudden abrupt increase (at least two times of the previous value) in the leakage current during constant voltage stress.

4.3 New failure mechanisms/defects in HfO₂/poly-Si gate stacks

4.3.1 Grain Boundary and Field assisted multiple breakdowns

Figure 4.12 shows the leakage current evolution of a SiO_x/HfO₂/poly-Si gate stack nMOSFET stressed under inversion mode CVS. From the gate leakage current evolution, it can be seen that the transistor suffered three breakdown events. The effective breakdown locations are measured electrically using equation (2.7) and it is found that the first, second and third breakdown locations are at channel center (i.e., $\sim 0.5 L$), drain side (i.e., $\sim 1 L$), and source side (i.e., $\sim 0 L$), respectively (Fig. 4.12). From the TEM micrograph of the same device, three breakdown spots can be observed physically (see Fig. 4.13 (a)). Figure 4.13 (b) shows another example of

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multiple breakdowns in high- κ gate stack MOSFETs stressed under inversion mode CVS. Multiple breakdowns are also found in accumulation mode stressed SiO_x/HfO₂/poly-Si gate stacks (see Figs. 4.6 and 4.7). This phenomenon of multiple breakdowns in *small* gate area (i.e., $W \times L \leq 1 \mu\text{m}^2$ [143]) high- κ gate stacks is different from SiO_xN_y/poly-Si and Si₃N₄/poly-Si gate stack MOSFETs, in which multiple breakdowns are rarely observed [61, 64, 65]. In the SiO_xN_y/poly-Si and Si₃N₄/poly-Si gate stack *small* gate area MOSFETs, the most common mechanism is the evolution of DBIE from the channel to the nearer source/drain (*S/D*) LDD region of a same BD spot, leading the device to catastrophic failure eventually (see Fig. 4.3).

Breakdowns in HfO₂ via grain boundary (GB) and triple points of the annealed polycrystalline HfO₂ high- κ dielectrics are believed to be the main mechanism causing the multiple breakdowns along the transistor channel. Figure 4.14 shows an indirect evidence of the role of grain boundary-assisted breakdown in HfO₂. In Fig. 4.14 (b), the presence of a clearly defined grain boundary next to a DBIE and an amorphized HfO₂ layer provides an indirect support of the role and importance of GB-assisted BD in the HfO₂ film. The *amorphous* HfO₂ layer sandwiched between the DBIE and another *crystalline* HfO₂ grain is the result of a substantial localized thermal heating process.

(a)

(b)

Figure 4.13. (a) TEM micrograph of the device shown in Fig. 4.12. Three BD spots named as A, B and C can be seen over the 0.5 μm channel length. (b) TEM micrograph of another SiO_x/HfO₂/poly-Si gate stack nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed under CVS in inversion mode with $I_{gt} = 5 \text{ mA}$ and $V_{gstress} = 3.3 \text{ V}$. The dotted circles show three BD locations.

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(a)

(b)

Figure 4.14. TEM micrographs of a HBD SiO_x/HfO₂/poly-Si gate stack ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed in inversion mode with $V_{g\text{stress}} = 3.6 \text{ V}$. (a) Two BD locations A and B, are indicated by the dotted circles, (b) HRTEM micrograph of Spot A. Formation of DBIE and amorphization of HfO₂ in the vicinity of grain boundary can be seen, which support the proposed GB-assisted breakdown hypothesis.

It is found that in both inversion and accumulation mode stressing, the multiple BDs were strongly dependent on the gate areas. Only a single BD ($> 90\%$ analyzed) was typically detected for nMOSFETs with relatively small gate area ($W \times L = 0.25 \times 0.05 \mu\text{m}^2$) (Fig. 4.15) as compared to the multiple BDs in relatively larger gate area ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) nMOSFETs (Figs. 4.6, 4.7, 4.13 and 4.14). On the

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other hand, corner breakdowns near the S/D extension are commonly found in both large gate lengths ($0.5\ \mu\text{m}$) and small gate lengths ($0.05\ \mu\text{m}^2$) SiO_x/HfO₂/poly-Si gate stack nMOSFETs ($W = 0.25\ \mu\text{m}$) of inversion and accumulation modes CVS (see Figs. 4.6, 4.7, 4.12, 4.13, 4.14, 4.15 and 4.16). Table 4.1 compares and summarizes the breakdown events and probability of the breakdown location in long- and small-channel length high- κ MOSFETs.

Figure 4.15. TEM micrographs of two HBD SiO_x/HfO₂/poly-Si nMOSFETs ($W \times L = 0.25 \times 0.05\ \mu\text{m}^2$). MOSFET stressed in (a) accumulation mode, (b) inversion mode. The dotted circles indicate the BD location.

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Figure 4.16. TEM micrographs of several SiO_x/HfO₂/poly-Si gate stack nMOSFETs ($W \times L = 0.25 \times 0.05 \mu\text{m}^2$ and $0.25 \times 0.5 \mu\text{m}^2$) suffered corner BD indicated by the dotted circles. Both inversion and accumulation mode failures are shown. The electrically measured breakdown locations (BD_L) using equation (2.7) correspond well with the physical analysis results.

Table 4.1. Summary of the breakdown characteristics in large and small gate area SiO_x/HfO₂/poly-Si gate stack nMOSFETs.

MOSFET size ($W = 0.25 \mu\text{m}$)	BD events (for a given I_{gl} and stress time)	Location of BD revealed by TEM
Large $L = 0.5 \mu\text{m}$	Multiple	~50% near corner
Small $L = 0.05 \mu\text{m}$	Single	> 90% near corner

Figure 4.17. Effective electric field near gate edge reported by Ono *et al.* [148] for a high- κ gate dielectric ($\kappa=19.5$). At $\Delta \sim 5 \text{ nm}$ shown in Fig. 3.16, the effective field strength is $> 5.5 \text{ MV/cm}$ as κ for the spacer material in our case is about 3.9 (i.e., < 9.75 shown in the above figure).

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This non-uniformity in the breakdown location is attributed to two main factors: 1) the presence of grain boundaries in the annealed high- κ film that promotes the grain-boundary assisted breakdown (see Fig. 4.14), and 2) the existence of possibly a much higher effective field strength near the “L-shape” corner at the poly-Si edge [148] due to a large difference in the dielectric constant between the spacer material and the high- κ gate dielectric (see Fig. 4.17). Based on the simulation results reported by Ono *et al.* [148], the effective electric field for a high- κ gate stack with a slight extension of the high- κ film ($\kappa=19.5$) from the gate edge is higher than that without an extension. Due to the presence of the high electric field strength near the “L-shape” corner compared to that of the channel, it is easier to create breakdown paths near the source/drain extension regions if the stress is continued. Hence, in order to prevent the corner breakdown, there is need of fabricating zero extension high- κ film in high- κ MOSFET, if the dielectric constant of the spacer material is much lower than the high- κ film. On the other hand, it is believed that since the size of the annealed HfO₂ grains is about 11 nm [149], the grain-boundary assisted breakdown in the channel area for smaller nMOSFETs is less probable as compared to a larger gate area, leading to a higher percentage of the corner breakdown reported in Table 4.1.

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(a)

(b)

Figure 4.18. Summary of the electrically measured location of the *first* breakdown of SiO_x/HfO₂/poly-Si gate stacks (measured using equation (2.7)). nMOSFETs having gate area of (a) $W \times L = 0.25 \times 0.5 \mu m^2$, and (b) $W \times L = 0.25 \times 0.05 \mu m^2$.

Figures 4.18 (a) and (b) tabulate the electrically measured breakdown locations (measured using equation (2.7)) of the *first* breakdown in MOSFETs of two sizes. The results agree well with that measured by the TEM analysis shown in Table 4.1. It has been observed that the 0.05 μm gate length MOSFETs have less channel

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breakdown than the 0.5 μm gate length MOSFETs (Figs. 4.13 – 4.15, 4.18). This indicates that grain boundaries also play an important role in the breakdown of the SiO_x/HfO₂/poly-Si gate stacks as the small area MOSFETs have less grain boundaries in the channel compared to the large area devices. In contrast, the breakdown location of the SiO_xN_y/poly-Si gate stack nMOSFETs is randomly distributed across the entire channel (see Fig. 4.19 and Refs. 32, 53). Hence, on the basis of the electrical analysis, physical analysis and simulation results, it is revealed that both high electric field strength near the “L-shape” corner at the poly-Si edge and existence of grain-boundaries in the HfO₂ high- κ film play important roles in the breakdown of high- κ gate stack MOSFETs.

Figure 4.19. First *effective* BD location (measured using equation (2.7)) in SiO_xN_y/poly-Si gate stack nMOSFETs ($W \times L = 0.15 \times 0.15 - 0.3 \times 0.3 \mu\text{m}^2$) having EOT of 2.0 nm stressed under CVS of 3.6 V and $I_{gl} = 10 \mu\text{A}$.

4.3.2 HfO₂ high- κ /spacer – interface breakdown

Two types of breakdowns near the source/drain extension (i.e., corner) have been observed in the HfO₂ high- κ /poly-Si gate stack nMOSFETs stressed under accumulation mode CVS. These are 1) the corner breakdowns via the interface of the HfO₂ high- κ /spacer (see Figs. 4.20 and 4.21), and 2) the corner breakdowns via the HfO₂ film itself (see Fig. 4.22). From Fig. 4.20, it can be seen that a breakdown through the interface of the HfO₂/spacer has taken place near the source/drain extension, instead of the HfO₂ high- κ gate film. This new HfO₂/spacer-interface failure mechanism (7 cases out of 13 cases (i.e., > 50%) of breakdown near the *S/D* extensions studied by TEM) only seen in the accumulation mode stressing of nMOSFETs, has been so far observed for both long ($L = 0.5\ \mu\text{m}$) and short ($L = 0.05\ \mu\text{m}$) channel nMOSFETs (Fig. 4.21). In addition, as shown in Fig. 4.22 for two nMOSFETs ($W \times L = 0.25 \times 0.05\ \mu\text{m}^2$) stressed in accumulation mode, the formation of DBIE hillocks from the poly-Si grain (cathode) takes place via the HfO₂ high- κ film itself, instead of the HfO₂/spacer-interface at the source/drain extension regions as shown in Figs. 4.20 and 4.21. The physical analysis results revealed that the probability of breakdown near the *S/D* extensions via the HfO₂/spacer-interface and via HfO₂ film is nearly equal.

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Figure 4.20. TEM and HRTEM micrographs of a narrow SiO_x/HfO₂/poly-Si gate stack nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) failed at I_{gl} of 2 mA during CVS under accumulation mode stress with $V_{gstress} = -3.8\text{V}$. (a) TEM micrograph showing the BD location at the drain extension region. The dotted circle indicates the breakdown spot. (b) HRTEM micrograph of the breakdown spot in (a) showing the breakdown through the HfO₂/spacer-interface, instead of HfO₂ film itself.

On the other hand, the breakdowns near the S/D extension via HfO₂/spacer-interface (seen in Figs. 4.20 and 4.21) have *not* been observed in inversion mode stressing of nMOSFETs (see Figs. 4.23 and 4.24) in all the cases analyzed by TEM (in total 15 cases studied). Figure 4.24 shows the typical HRTEM micrographs of two nMOSFETs ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$ and $0.25 \times 0.05 \mu\text{m}^2$) failed under inversion mode stressing. Similar to Fig. 4.22, in the case of breakdowns near the S/D

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extensions, the DBIE hillocks are formed from the Si-substrate (cathode) via the HfO₂ high- κ film.

Figure 4.21. TEM micrographs of several SiO_x/HfO₂/poly-Si gate stack nMOSFETs suffered corner BDs through HfO₂/spacer-interface at I_{gl} of 2 mA during CVS accumulation mode stressing with $V_{gstress} = -4.0-4.5$ V. (a), (b) and (c) nMOSFETs ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$). (d), (e) and (f) nMOSFETs ($W \times L = 0.25 \times 0.05 \mu\text{m}^2$). The arrows show the breakdowns near the S/D extensions through the HfO₂/spacer-interface.

Figure 4.22. HRTEM micrographs of two narrow nMOSFETs ($W \times L = 0.25 \times 0.05 \mu\text{m}^2$) having HfO₂ gate dielectric failed at I_{gl} of 2 mA during CVS under accumulation mode stress. The arrows show the DBIE hillocks from the poly-Si grain through the HfO₂ film in the source/drain extension regions.

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Figure 4.23. TEM Micrographs of 5 BD spots of the nMOSFETs suffered breakdowns near the *S/D* extensions under inversion mode stress. The arrows indicate the *S/D* extension breakdowns through the HfO₂ film itself.

Figure 4.24. HRTEM micrographs of BD spots of two SiO_x/HfO₂/poly-Si gate stack nMOSFETs suffered *S/D* extension BD through the HfO₂ film under inversion mode stress. (a) nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) failed at $V_{gstress}$ of 3.5 V with I_{gl} of 2 mA. (b) nMOSFET ($W \times L = 0.25 \times 0.05 \mu\text{m}^2$) failed at $V_{gstress}$ of 3.8 V with I_{gl} of 2 mA. The arrows indicate that the DBIE lattice follows the Si-substrate through the HfO₂.

(a)

(b)

Figure 4.25. Simulation data of the potential and electric field profile in the half portion (i.e., either drain or source portion) of a nMOSFET having HfO₂ high- κ /poly-Si gate stack with poly-Si doping of 10^{21} cm^{-3} and 5 nm of HfO₂ extension (see Fig. 3.16), stressed in accumulation mode with $V_{gstress}$ of -4.0 V and $V_d = V_s = V_{sub} = 0$ V. (a) Potential distribution, and (b) the absolute value of the electric field strength.

The T-SUPREM4 and MEDICI simulations as discussed in Chapter 3 have been performed to study the potential and the electric field strength profiles along the poly-Si/high- κ -interface and the middle of the interfacial layer of the nMOSFETs. The simulation results show a much higher electric field strength along both poly-Si/high- κ -interface and the middle of the interfacial layer between the S/D extension

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regions and the gate edge than that in the channel in accumulation mode stressing (see Fig. 4. 25). Ono *et al.* [148] reported that at the interface between the two materials of different dielectric constants, a component of the electric field, which is perpendicular to the interface, is enhanced in the lower dielectric constant material due to a continuity of electric flux density. Hence, very high electric field strength along poly-Si/high- κ -interface between the *S/D* extension regions and the gate edge is attributed to the difference of the dielectric constant between the high- κ film ($\kappa = 20$) and the spacer ($\kappa = 3.9$). It is also believed that the very high electric field strength along the middle of the interfacial layer between the *S/D* extension regions and the gate edge than that in the channel is attributed to an addition of extra 0.7 V voltage difference across the p-n junction between the *S/D* and the silicon substrate during the accumulation mode stressing. In addition, it can also be observed that the electric field strength along the poly-Si/high- κ -interface is lower than that along the middle of the interfacial layer in the channel region (see Fig. 25 (b)). This is due to a smaller dielectric constant difference between the poly-Si ($\kappa = 11.7$) and high- κ gate dielectric ($\kappa = 20$) than that of between the interfacial layer ($\kappa = 3.9$) and high- κ gate dielectric [148]. From the simulated results, it was estimated that the probability of the field assisted *S/D* extension breakdowns (both via HfO₂/spacer-interface and HfO₂ film) will be at least 40 % higher than that of the channel breakdowns. The estimation was made on the basis of our observation that 40 nm of the gate dielectric at the source and drain extensions regions experienced very high electric field strength out of 100 nm of the entire gate dielectric length as shown in Fig. 4.25 (b). This result correlates well with our physical analysis results (i.e., 13 cases of breakdowns near the *S/D* extensions out of 16 cases studied). It is worth mentioning that the high percentage of breakdowns near to the *S/D* extensions compared to the channel may not be detectable

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during stressing, if the source and drain are floated during the accumulation mode stress.

On the other hand, the simulation results show that the electric field strength is similar in magnitude between the channel and *S/D* extension regions along the middle of the interfacial layer in the inversion mode stressing (see Fig. 4.26). Hence, both grain boundaries assisted channel breakdowns (see Fig. 4.14) and field assisted *S/D* extension breakdowns are observed (6 cases of grain boundaries assisted breakdowns and 9 cases of breakdowns near the *S/D* extensions via HfO₂ film out of 15 cases studied by TEM). It is believed that the slightly higher percentage of the breakdowns near the *S/D* extensions (observed by the TEM analysis results) compared to that of the channel is again due to the existence of the very high electric field strength near the poly-Si gate edge along the interface between the high- κ gate dielectric film and poly-Si gate (see Fig. 4.26 (b)).

(a)

(b)

Figure 4.26. Simulation data of the potential and electric field profile in the half portion (i.e., either drain or source portion) of a nMOSFET having HfO₂ high- κ /poly-Si gate stack with poly-Si doping of 10^{21} cm^{-3} and 5 nm of HfO₂ extension (see Fig. 3.16), stressed in inversion mode with $V_{gstress}$ of 3.5 V and $V_s = V_d = V_{sub} = 0 \text{ V}$. (a) Potential distribution, and (b) the absolute value of electric field strength.

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Figure 4.27. Schematics showing the channel potential profiles and the nature of BD during CVS. (a) accumulation mode CVS, and (b) inversion mode CVS.

Figure 4.27 shows the schematics of a proposed model of the HfO₂/spacer-interface failure mechanism in the HfO₂ high- κ gate stacks studied. This new failure mechanism can take place with a higher probability under accumulation mode stressing (i.e., gate injection) due to the presence of the high electric field distributions near the poly-Si gate edge along the interface between the high- κ gate dielectric film and poly-Si gate shown in Fig. 4.25 (b). If the high electric field at the gate edge, coupled with the fact that the HfO₂/spacer-interface is defective compared to the HfO₂ crystalline lattice, this interface would become a preferential breakdown site (see Fig. 4.27 (a)) during the gate injection. On the other hand, even if the electric field is high at the gate edge under inversion mode stressing along the interface between the high- κ gate dielectric film and poly-Si gate (see Fig. 4.26 (b)), there is no preferential HfO₂/spacer-interface breakdown as electrons are injected from the silicon substrate to the poly-Si gate (see Figs. 4.27 (b)). Such gate dielectric/spacer-interface breakdown has never been observed in the conventional SiO_xN_y gate dielectrics [23-26, 61-65, 68, 69], as the gate dielectric material is similar to the spacer materials. On

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the basis of the experimental results and the simulation results, it is believed that, similar to the gate injection in nMOSFETs breakdown via the interface of the HfO₂ gate dielectric and spacer, the interface breakdown may be seen in pMOSFETs during inversion mode stress (i.e., gate injection). Hence, in order to prevent the HfO₂/spacer-interface breakdown, gate engineering to give perfect side wall is needed.

(a)

(b)

Figure 4.28. TEM micrograph of two HBD SiO_x/HfO₂ high- κ /poly-Si gate stack nMOSFETs ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed under CVS in inversion mode. (a) I_{gl} of 5 mA and $V_{gstress}$ of 3.8 V, (b) $V_{gstress}$ of 3.5 V having a compliance current limit of 2 mA. Formation of a “ball-shaped” capping layer above the breakdown spot at the anode electrode of the device can be seen.

4.3.3 “Ball-shaped” Capping layer

Figure 4.28 shows the TEM micrographs of two HBD SiO_x/HfO₂/poly-Si gate stack nMOSFETs ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) failed under inversion mode constant voltage stress. A dielectric breakdown induced “ball-shaped” capping layer on the anode side (i.e., at the poly-Si side in this case) of the MOSFET can be seen in the vicinity of the breakdown spot (see Figs. 4.28 (a) and (b)). The formation of the “ball-shaped” capping layer at the silicon substrate side (i.e., anode electrode) has also been observed in nMOSFETs ($W \times L = 0.25 \times 0.05 \mu\text{m}^2$) stressed under accumulation mode with $V_{gstress}$ of -4.5 V and a compliance current limit of 2 mA (see Fig. 4.29).

Based on a HRTEM/EDS (not shown here)/EELS elemental dot mapping analysis (see Fig. 4.30), a large percentage of hafnium, oxygen and silicon has been observed within the capping layer shown in Figs. 4.28 and 4.29. Figures 4.31 (a) and (b) show the EELS spectra of the oxygen K edges and hafnium O_{2,3} edges of the HfO₂ gate dielectric, respectively. The oxygen K edge of the spacer material (SiO₂) is included in Fig. 4.31 (a) for comparison. We can see that the peaks of the oxygen K edges, which provide the information about the chemical properties of oxygen in a particular compound, are different in the SiO₂ spacer, HfO₂ gate dielectrics and “ball-shaped” capping layer (see Fig. 4.31 (a)). This leads to the conclusion that the oxygen in the capping layer has a different chemical bonding from that in the HfO₂ gate dielectrics as well as in SiO₂. In this particular case, as shown in Fig. 4.31 (a), the oxygen K edge peak at ~547.5 eV, which is present in the capping layer, is almost disappeared in the HfO₂ gate dielectrics. It has also been observed that the oxygen K edge EELS spectrum of capping layer (see Fig. 4.31 (a)) is similar to the oxygen K edge EELS spectrum of HfSiO₄ reported by Craven *et al.* [150]. Based on the oxygen

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K edge EELS chemical analysis, it was found that the capping layer consists of Hf-based compounds, whose chemical properties lie between the HfO₂ and HfSiO₄.

Figure 4.29. TEM micrograph of a HBD SiO_x/HfO₂ high- κ /poly-Si gate stack nMOSFET ($W \times L = 0.25 \times 0.05 \mu\text{m}^2$) stressed in accumulation mode with $V_{g\text{stress}}$ of -4.5 V having a compliance current limit of 2 mA.

In addition, the peaks of the hafnium O_{2,3} edge in the HfO₂ gate dielectrics and capping layer are different (see Fig. 4.31 (b)). The hafnium O_{2,3} edge peak at ~ 50 eV (which is present in the HfO₂ gate dielectrics) disappears in the capping layer while the sharp hafnium O_{2,3} edge peak at ~ 23 eV of the capping layer has a lower intensity than that of the HfO₂ gate dielectrics (Fig. 4.31 (b)). This indicates that the number of Hf second-nearest neighbors around the excited Hf atoms is reduced in the capping layer. Together with the HRTEM/EDS/EELS elemental dot mapping spectra that show only the presence of Hf, O, and Si in the capping layer, it is concluded that the “ball-shaped” capping layer consists of mainly compounds composed of Hf, Si, and O. Apparently, the compounds are not HfO₂ or Hf sub-oxide, HfO_{*x*} with $x < 2$, since

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both Hf and O bonding show significantly different signatures from that of HfO_2 . The alternatives left are HfSi_xO_y and HfSi_x .

Figure 4.30. HRTEM and elemental dot maps of the breakdown spot shown in Fig. 4.28 (a). (a) HRTEM micrograph showing DBIE. EELS elemental dot maps (b) Hafnium, (c) Oxygen, and (c) Silicon. The presence of hafnium, oxygen and silicon can be seen in the “ball-shaped” capping layer. The oxygen and silicon maps are rotated compared to the hafnium map due to rotation of the sample for better focus to get good oxygen signal. A Gatan package commercial software three window is used for elemental mapping. The scale for the elemental mapping is kept identical to TEM micrograph. 99 eV energy window is used for the Si EFTEM.

(a)

(b)

Figure 4.31. EELS spectra of oxygen K edge and Hafnium $\text{O}_{2,3}$ edge at various locations of a nMOSFET shown in Fig. 4.28 (b). (a) Oxygen K edge at SiO_2 spacer, HfO_2 gate dielectric (position 1), and “ball-shaped” capping layer (position 2) as seen in Fig. 4.28 (b). The solid arrows indicate the oxygen K edge peaks. (b) Hafnium- $\text{O}_{2,3}$ edge at position 1 (i.e., HfO_2) and position 2 (i.e., “ball-shaped” capping layer) as seen in Fig. 4.28 (b). The solid arrows indicate hafnium- $\text{O}_{2,3}$ edge peaks.

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Figure. 4.32. Schematics of a comprehensive model for the BD mechanism in HfO₂ high-κ/poly-Si gate stacks stressed in inversion mode. (a) Phase I – percolation path formation, (b) Phase II – percolation path dilation, (c) Phase III – SBD + DBIE + silicide/silicate formation, (d) Phase IV-A – Hard SBD + DBIE + SHIC (e) Phase IV-B –HBD + DBIE + ruptured SHIC.

4.3.4 Self healing insulating cap model

Fig. 4.32 shows a model depicting a proposed model of the breakdown mechanisms in the HfO₂ high- κ /poly-Si gate stacks stressed in inversion mode. The model consists of four phases. In Phase I, the formation of a percolation path can take place within the HfO₂ grains or at the grain boundaries (Fig. 4.32 (a)) due to pre-existing defects and the additional generation of a large amount of defects/traps during stressing. It is believed that after the formation of a percolation path, a huge amount of current density (J) surges through the percolation path and its surrounding. As a result, thermal joule heating, proportional to the $J^2\rho$ (where ρ is the resistivity of percolation path) is generated. Immediately after Phase I, in Phase II, the presence of a huge joule heating accelerates the percolation path dilation, especially along the grain boundary (Fig. 4.32 (b)). Also, the thermally excited and dislodged Si atoms from the cathode in the vicinity of the BD path may be “sucked” into the percolation path as the formation of Si substitutional defects in the HfO₂ gate dielectric requires less energy [151]. This mechanism makes the leakage path within the HfO₂ more conductive, allowing more substantial increase in the leakage current. In addition, in Phase II, the *breaking* of HfO₂ bond and migration of the dislodged Hf and O atoms within the dilated percolation path in the direction of the electron flow could take place as the binding energy of HfO₂ is relatively small (16.5-17.0 eV) [152]. The localized heat created in Phase I and II could further promote *thermochemical* reactions in Phase III (Fig. 4.32 (c)). As the reactions between HfO₂ and Si only needs an enthalpy (ΔH) of typically 50-80 kJ/mole [153], the formation of HfSi_xO_y, HfSi_x and SiO₂ take place favorably in the vicinity of the anode side of the percolation path. Further sub-reactions (i.e., SiO₂+HfO₂→HfSiO₄) are enhanced by the presence of

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SiO_2 as ΔH is -12.4 kJ/mol [153]. This leads to an HfSi_xO_y -rich insulating compound intermixed with HfO_2 , SiO_2 , and HfSi_x . At the same time, on the cathode end, the initial reactions could have been dominated by the presence of the IL (i.e., $\text{SiO}_2 + \text{HfO}_2 \rightarrow \text{HfSiO}_4$), and by the nucleation and growth of DBIE, pushing all the intermixed Hf-compounds along its growth direction (Fig. 4.32 (c)). Once Phase III is allowed to evolve into Phase IV, DBIE is expected to grow very rapidly, creating a very huge up-thrust to all the intermixed compounds towards the anode side, forming a shape similar to a “ball-shaped” capping layer called *self-healing insulating cap* (SHIC), as seen in Fig. 4.32 (d).

Figure 4.33. HRTEM micrograph of a breakdown spot of a $\text{SiO}_x/\text{HfO}_2$ high- κ /poly-Si gate stack nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed in inversion mode with $V_{g\text{stress}} = 3.6$ V. The DBIE crystal orientation is same as that of the Si substrate.

Phase IV can then evolve into Phase IV-A or IV-B. In Phase IV-A, there will be no breakage/crack in SHIC (i.e., “ball-shaped” capping layer) while more HfSi_xO_y is being formed (i.e., *self-healing*), maintaining it as an ultrathin insulator-like layer

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separating DBIE from the poly-Si (Fig. 4.30 (d)). The HRTEM result shown in Fig. 4.33 corresponds well with the existence of SHIC (i.e., “*ball-shaped*” capping layer) in Phase IV-A. Alternatively in Phase IV-B, the SHIC formation may not completely cut off the leakage path and possibly mix with high concentration of HfSi_x, SHIC will be distorted (Fig. 4.32 (e)) and later ruptured due to the extrusion force from the DBIE underneath. The TEM/EELS results shown in Figs. 4.28 and 4.30 confirm the dispersion of the presence of the Hf-related materials. On the other hand, in accumulation mode constant voltage stress, the nature of the Hf-based “*ball-shaped*” capping layer could be slightly different due to the presence of the SiO_x interfacial layer on the anode end, leading to a SHIC probably just consisting of HfSiO₄ after HfO₂ reaction with SiO_x. The relatively high rigidity of the Si substrate is believed to make SHIC gentler and smoother in accumulation mode (Fig. 4.34). Figures 4.29 and 4.34 (b) show two examples of the physically observed DBIE and SHIC in the accumulation mode stress. Table 4.2 summarizes the SHIC model and the variation in the post-BD resistances associated with various BD microstructural changes for HfO₂ and SiO_xN_y gate stacks.

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$$R_{\text{eff}} = R(\text{HfSi}_x\text{O}_y\text{-based SHIC}) + R(\text{Si-epi}) + R_{\text{poly}} + R_{\text{para}}$$

(a)

(b)

Figure 4.34. (a) Schematic of the BD mechanism of HfO₂/poly-Si gate stack stressed in accumulation mode. (b) TEM micrograph shows an example of the formation of “ball-shaped” capping layer as shown in (a) under accumulation mode CVS with $V_{g\text{stress}} = -4.0$ V.

Chapter 4: Failure mechanisms/defects in HfO₂ high- κ /poly-Si gate stack MOSFETs**Table 4.2.** Effects of microstructural evolution associated with BD on resistances in oxynitride and HfO₂ gate stacks.

BD Phases	BD Types	Gate dielectric type	R _{perco}	R _{poly}	R _{para}	R(HfSi _x O _y +HfSi _x) or R(SiO _x)	R (Si-epi)	R(HfSi _x O _y -based SHIC)	R _{geff} (Ω)
Phase I and II	SBD	HfO ₂	√	√	√	X	X	X	10 ⁶ -10 ⁷
		SiO _x N _y	√	√	√	X	X	X	
Phase III	SBD+DBIE	HfO ₂	√	√	√	√	√	X	~ 10 ⁵
		SiO _x N _y	√	√	√	√	√	X	~ 10 ⁵
Phase IV-A	“Hard” SBD +DBIE	HfO ₂	X/√	√	√	X/√	√	√	10 ⁴ -10 ⁵
	HBD+DBIE	SiO _x N _y	X	√	√	√	√	X	10 ³ -10 ⁴
Phase IV-B	HBD+DBIE	HfO ₂	X	√	√	X	√	√	10 ³ -10 ⁴
	HBD+DBIE	SiO _x N _y	Same as phase IV-A						
R _{perco} = resistance of percolation path; R _{poly} = Resistance of poly-Si gate; R _{para} = Parasitic resistances; X = not present; √ = present, X/√ = unclear									

4.3.5 Effect of SHIC on gate leakage current evolution and device performance

Figure 4.35 shows the evolution in the breakdown leakage current of four *small* HfO₂/poly-Si gate stack nMOSFETs during inversion and accumulation mode constant voltage stress. Upon a breakdown event, the breakdown leakage current typically does not reach the pre-set I_{gl} and behaves differently from the conventional SiO_xN_y dielectrics after the initial abrupt transient [61]. For example, the leakage current can stabilize at a relatively constant level, or gradually increase/decrease as a function of the stress time until the next breakdown occurs. The *self-healing* mechanism or the dielectric nature of the Hf-based SHIC (i.e., “*ball-shaped*” capping layer) shown in Figs. 4.28 - 4.34 is believed to be primarily responsible for the

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behavior of the breakdown induced gate leakage current arrested after each abrupt transition. If the Hf-based SHIC contains a large portion of pinhole-like defects i.e., a discontinuous layer, the DBIE (i.e., epitaxial Si) extruded from the cathode side can form a low resistivity electrical path with the poly-Si gate via the pinholes and HfSi_x. Similarly, for a high percentage of HfSi_x in the SHIC, DBIE can also chemically react with HfSi_x. This *chemical reaction induced slow leakage current ascending and breakdown self-healing* process give rise to a gradual increase in the leakage current (i.e., R_{geff} decreases, where R_{geff} is the post-BD effective gate resistance of the nMOSFET (see equation (2.8) and Ref. 61) as shown in S1, S2 and S4 in Fig. 4.35. On the other hand, if HfSi_xO_y in the Hf-based SHIC is dominating over HfSi_x, more subsequent formation of HfSiO₄ is possible via the initial reaction products of Si and HfO₂ i.e., SiO₂ with HfO₂, and poly-Si with HfO₂. The resultant capping layer will be thicker and more resistive i.e., R_{geff} increases. This *chemical reaction induced isolation and self-healing* process causes the leakage current to gradually decrease such as S1 and S3 shown in Fig. 4.35. Another possibility is that the chemical reaction mechanism in the Hf-based SHIC reaches an equilibrium, stabilizing R_{geff} as well as the leakage current at a specific level (see S2 and S4 in Fig. 4.35). In addition, the post-BD drain saturation current (I_{dsat}) recouping phenomenon (see Fig. I.4 in Appendix I) is attributed to a HfSiO₄-rich SHIC layer in which the “defects” in the dielectric layer have been annealed out by the self-healing process, improving its dielectric quality and leading to a higher I_{dsat} .

Figure 4.35. Gate leakage current evolution of HfO₂/poly-Si gate stacks during inversion and accumulation mode stress. The solid arrows, dashed arrows and star-solid arrows indicate the gate leakage current gradual decrease, leakage current ascending and leakage current stabilization respectively.

Figure 4.36. Flow chart for the BD characteristics and microstructural changes during a BD event in HfO₂ gate stacks.

4.4 Summary

The failure defects and mechanisms in SiO_x/HfO₂ high- κ /poly-Si gate stack nMOSFET are studied physically and electrically. Instead of a single progressive BD in *narrow* SiO_xN_y/Si₃N₄ MOSFETs, multiple BDs in single *narrow* high- κ nMOSFETs are commonly observed. In addition to DBIE and DBIM observed in the breakdowns of ultrathin SiO_xN_y and Si₃N₄ gate dielectrics, grain-boundary and field-assisted breakdowns are found to be of critical importance for most of the breakdowns observed in the SiO_x/HfO₂ high- κ /poly-Si gate stack transistors. A new failure mechanism along HfO₂ high- κ /spacer interface is also observed.

On the other hand, the formation of a new microstructural defect called “*ball-shaped*” capping layer at the anode side of the device is found. On the basis of the chemical analysis results (TEM/EELS and EDS), the “*ball-shaped*” capping layer induced by the breakdown in high- κ /poly-Si nMOSFETs is found to be composed of Hf-related compounds, either HfSi_xO_y or/and HfSi_x. The driving force for the formation of the capping layer is a thermally assisted chemical reaction in the vicinity of the breakdown path. A SHIC (i.e., “*ball-shaped*” capping layer) model describing the breakdown mechanism and evolution in HfO₂/poly-Si gate stacks is proposed. Figure 4.36 summarizes all the possible BD evolutions in HfO₂/poly-Si gate stack. The formation of SHIC by a *breakdown induced thermo-chemical reaction and self-healing process* is used to explain the post-BD electrical *I-V* characteristics. Table 4.3 summarizes the new and common failure defects/mechanisms in HfO₂/poly-Si gate stacks as compared to SiO_xN_y/poly-Si and Si₃N₄/poly-Si gate stacks, revealed by physical and electrical analysis.

Chapter 4: Failure mechanisms/defects in HfO₂ high- κ /poly-Si gate stack MOSFETs**Table 4.3.** Summary of the failure defects/mechanisms in HfO₂/poly-Si gate stack compared to SiO_xN_y/poly-Si and Si₃N₄/poly-Si gate stack MOSFETs.

	Failure Mechanisms/defects	Narrow HfO ₂ /poly-Si gate stack	Narrow SiO _x N _y /poly-Si and Si ₃ N ₄ /poly-Si gate stacks
TEM/EDS/ EELS analysis	Multiple breakdowns in small area (i.e., $\leq 1\mu\text{m}^2$) MOSFETs	Yes (see Figs. 4.7, 4.13, 4.14)	No [23-26, 61-65, 68, 69]
	Grain boundary and field assisted BD	Yes (see Figs. 4.13 – 4.16 and 4.20 - 4.24)	No [23-26, 61-65, 68, 69]
	High- κ /Spacer - interface BD	Yes (see Figs. 4.20 and 4.21)	No [23-26, 61-65, 68, 69]
	“Ball-shaped” capping layer and formation of Hf-based compounds assisted by <i>thermochemical</i> reaction	Yes (see Figs. 4.28 - 4.34)	No [23-26, 61-65, 68, 69]
	Amorphization of anode material	Yes (see Fig. I.3 in Appendix I)	No [23-26, 61-65, 68, 69]
	<i>Polarity</i> dependent DBIE	Yes (Figs. 4.1, and 4.4 , 4.5 and 4.7)	Yes [23-26, 61-65, 68, 69]
	DBIM	Yes (Figs. 4.9 and 4.10)	Yes [24, 68]
Electrical analysis	Multiple BDs	Yes (see Figs. 4.6, 4.12 and 4.35)	No [23-26, 61-65, 68, 69]
	I _{dsat} recouping	Yes (see Fig. I.4 in Appendix I)	No [23-26, 61-65, 68, 69]
	Progressive breakdown	Yes (see Figs. 4.6, 4.12 and 4.35)	Yes [45, 55-57, 104]
	Asymmetrical breakdown (i.e., one side transistor-like and other side resistive-like <i>I-V</i> characteristics)	Yes (Figs. 4.8 and I.1 in Appendix I)	Yes [61-65, 68, 69]
	Channel short (i.e., both side resistive-like <i>I-V</i> characteristics)	Yes (see Fig. I.2 in Appendix I)	Yes [61-65, 68, 69]
	Channel center breakdown (i.e., both side symmetrical transistor-like <i>I-V</i> characteristics)	Yes (see Fig. 4.2)	Yes [69]

Chapter 5 FAILURE MECHANISMS/DEFECTS IN HfO₂ HIGH- κ /TaN/TiN GATE STACK MOSFETS

5.1 Introduction

In Chapter 4, we discussed the failure mechanisms in HfO₂ high- κ /poly-Si gate stack MOSFETs. But in the literature, it has been reported that metal gate stacks have a lot of advantages over poly-Si gate stacks in terms of device performance and compatibility with high- κ process [96, 98, 121, 122, 127, 129-140]. Thus the study of the failure mechanisms in metal gate stack devices is significantly important before its implementation into nanoscale CMOS technology.

High degradation rate in the gate leakage current (which results in very high post-BD gate leakage current at nominal operating voltage, once a breakdown event occurs) is commonly observed in the breakdown of SiO_xN_y/tungsten gate stack MOS capacitors [141], and in high- κ /metal gate stack MOSFETs [35]. Kauerauf *et al.* [35] found that the metal gate electrode plays an important role for the abrupt large gate leakage current increase upon breakdown of the high- κ /metal gate stacks.

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On the other hand, it is reported that the static noise margin (SNM) of the static random access memory (SRAM) cells degrades to 50% if the post-breakdown gate leakage current at nominal operating voltage reaches a value of 20 - 50 μ A [154]. Hence, the high degradation rate in the gate leakage current in the metal gate has strong implication on the post-breakdown device/circuit reliability. But the exact mechanism responsible for the fast breakdown transient in the metal gate stacks, and the physical nature of the microstructural defects induced by high- κ breakdown in the metal gate MOSFET remain unclear.

In this chapter, we discuss a metal-like filamentation of breakdown path, resulting in an ultrafast progressive breakdown during substrate injection of the SiO_x/HfO₂/TaN/TiN gate stack n/pMOSFET. We also propose a breakdown model describing the filamentation of the BD path during the substrate injection of the device.

5.2 Filamentation of breakdown path in metal gate MOSFET during substrate injection

5.2.1 Ultrafast progressive breakdown

Figure 5.1 shows the evolution of the gate leakage current with time during breakdown event of 6 metal gate nMOSFETs (labeled as S1 - S6) stressed under inversion mode CVS (i.e., substrate injection). From Fig. 5.1, it can be seen that if the initial I_{gl} is kept at less than 2 μ A, the I_g can recover to the current level prior of the BD, indicating switching “off” of the percolation path (see S1 and S5 in Fig. 5.1). However, upon continuing the stress after the I_g recovery, subsequent switching “on” of the percolation paths can still take place. This phenomenon of the percolation path

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switching “on” and “off” has been consistently observed for many samples as long as $I_{gl} \leq 2 \mu\text{A}$, and could be due to charging and discharging of traps from the percolation path [114]. Similar variation in the gate leakage current in the initial phase of progressive BD, defined as digital breakdown, has been reported by Suehle *et al.* [155] for SiO₂/poly-Si gate stacks. On the other hand, once I_g reaches a value of more than $2 \mu\text{A}$, no I_g recovery could be observed in the metal gate after removing the stress, and I_g surged to the next higher I_{gl} instantaneously (i.e., in less than the milli-second of our system time resolution), similar to those ultrafast progressive BD seen in Refs. 35 and 141. The degradation rate (i.e., dI_g/dt [145]) for $\Delta I_g < 2 \mu\text{A}$ is $10^{-7} - 10^{-6} \text{ A/sec}$, more than 3 - 4 orders of magnitude lower than that for $2 \mu\text{A} < \Delta I_g < \sim 7 \text{ mA}$, further indicating that the BD mechanism above $2 \mu\text{A}$ is different from that of below $2 \mu\text{A}$. Degraeve *et al.* [142] also reported the two stages of progressive breakdown in high- κ /metal gate stack MOSFET.

Figure. 5.1. I_g evolution with time of six SiO_x/HfO₂/Ta₂N₅/TiN nMOSFETs (labeled as S1 - S6) ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed in inversion mode by CVS and SCVS with $V_{gstress}$ of 3.7 V and $I_{gl} = 1 \mu\text{A}$ -7 mA. I_{gl} of $2 \mu\text{A}$ is the threshold for an ultrafast progressive BD in the metal gate used in our study – below $2 \mu\text{A}$ slow progressive BD, and above $2 \mu\text{A}$ ultrafast progressive BD of the devices.

5.2.2 “Unarrested” breakdown

Figure 5.2 (a) shows that the pre- and post-BD I_g - V_g characteristics of *metal* gate nMOSFETs stressed under substrate injection with $I_{gl} \leq 2 \mu\text{A}$ is nearly identical, confirming that the BD is very “soft”, which could be due to switching “off” of the percolation path. Above the $2 \mu\text{A}$ threshold of I_{gl} , the post-BD gate leakage current @ $V_g = 1.5 \text{ V}$ is much higher than the preset I_{gl} of $5 - 10 \mu\text{A}$ @ $V_{gstress} = 3.7 \text{ V}$ for the inversion mode stressed (i.e., substrate injection) TaN/TiN gate nMOSFETs (see Fig. 5.2). Similar phenomenon has been observed for accumulation mode stressed *metal* gate pMOSFETs (i.e., substrate injection for pMOSFETs) (Fig. 5.3). On the other hand, for the case of the gate injection stressed metal gate n/pMOSFETs (i.e., accumulation mode stressing of nMOSFET and inversion mode stressing of pMOSFET), the post-BD I_g @ $|V_g| = 1.5 \text{ V}$ is lower than the preset I_{gl} @ $V_{gstress}$ (see Figs. 5.2 (b) and 5.3). It indicates that during the substrate injection in the *metal* gate devices, the post-BD transient can hardly be “arrested” by the preset I_{gl} , while this is not the case for the gate injection. This phenomenon is different from the HfO₂/*poly-Si* gate stacks discussed in Chapter 4, in which the post-BD transient can be arrested in both accumulation and inversion mode CVS (Fig. 5.4).

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(a)

(b)

Figure 5.2. (a) Pre- and post-BD gate leakage current I_g of five SiO_x/HfO₂ high- κ /TaN/TiN nMOSFETs (labeled as S1, S2, S4, S6, and S8) ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed in the inversion mode (i.e., substrate injection) CVS and SCVS with $V_{g\text{stress}}$ of 3.7 V and $I_{gl} = 2 \mu\text{A} - 7 \text{mA}$. S1, S2, S4 and S6 are shown in Fig. 5.1. S6 was stressed under SCVS with first I_{gl} of $5 \mu\text{A}$, and once I_g hits the $5 \mu\text{A}$, stress was continued with a higher I_{gl} of 7 mA, leading to two post-BD I_g curves of S6 in Fig. 5.2 (a). (b) Comparison of post-BD I_g - V_g characteristics of the other SiO_x/HfO₂ high- κ /TaN/TiN gate stack nMOSFETs ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed under inversion mode ($V_{g\text{stress}} = 3.7 \text{ V}$) and accumulation mode ($V_{g\text{stress}} = -4.5 \text{ V}$) CVS.

The “unarrested” breakdowns (i.e., ultrafast progressive breakdown) during the substrate injection in the *metal* gate n/pMOSFETs above the threshold of $2 \mu\text{A}$ of

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the gate leakage current result in very low post-BD effective gate resistance R_{geff} (see equation (2.8) and Ref. 61) of less than 100 k Ω , which is a major reliability concern. It has been reported that SRAM cell can work only if the post-BD R_{geff} is above ~ 50 k Ω [154]. The ultrafast progressive for $I_g > 2$ μ A is also detrimental to the device lifetime as it has been reported that slow progressive breakdown provides extra lifetimes for device to function [57].

Figure 5.3. Post-BD I_g - V_g characteristics of HfO₂ high- κ /TaN/TiN gate stack pMOSFETs ($W \times L = 0.25 \times 0.5$ μm^2) (EOT=1.71 nm) stressed under inversion mode ($V_{gstress} = -4.2$ V) (i.e., gate injection) and accumulation mode ($V_{gstress} = 3.7$ V) (i.e., substrate injection) CVS.

Figure 5.4. Post-BD I_g - V_g characteristics of HfO₂ high- κ /poly-Si gate stack nMOSFETs (labeled as N1 – N4) (EOT = 2.1 nm) ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed under inversion mode (i.e., substrate injection) ($V_{g\text{stress}} = 3.5 \text{ V}$) and accumulation mode (i.e., gate injection) ($V_{g\text{stress}} = -4.0 \text{ V}$) CVS.

Figure 5.5. Gate leakage current evolution of a TaN/TiN gate nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed under multiple-stage stress (see Chapter 3) with a first $V_{g\text{stress}}$ of 4.1 V and I_{gl} of 5 μA . After a BD occurred at 4.1 V, the device was stressed subsequently with $V_{g\text{stress}}$ of 1.6 - 2.5 V for 500 s at each stressing voltage. The insert shows I_g evolution at the first $V_{g\text{stress}}$ of 4.1 V.

5.2.3 Stable breakdown path

Figure 5.5 shows the I_g evolution during multiple-stage stress of a TaN/TiN gate nMOSFET with $V_{gstress}$ of 1.6 - 2.5 V after a BD occurred with $V_{gstress}$ of 4.1 V and $I_{gl} = 5 \mu\text{A}$. The I_g evolution in the *metal* gate stacks during the post-BD low voltage multiple-stage stress is very stable. Even if the $I_{gl} @ V_{gstress}$ of 4.1 V is 5 μA , the post BD I_g is much higher at lower $V_{gstress}$ of 1.6 V (Fig. 5.5), further indicating that the post-BD transient in the metal gate stacks is “unarrested” by the preset I_{gl} during the substrate injection. On the other hand, for *poly-Si* gate stacks, the initial BD path caused by $V_{gstress} = 3.3 \text{ V}$ and $I_{gl} = 5 \mu\text{A}$ is unstable and shows digital nature at the post-BD lower $V_{gstress}$ of 1.5 - 2.3 V (Fig. 5.6).

Figure 5.6. I_g evolution of a HfO₂/poly-Si gate stack nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed under multiple-stage stress with a first $V_{gstress}$ of 3.3 V and I_{gl} of 5 μA . After a BD occurred at 3.3 V, the device was stressed subsequently with $V_{gstress}$ of 1.6 - 2.3 V for 300 s at each stressing voltage. The insert shows I_g evolution at first $V_{gstress}$ of 3.3 V.

(a)

(b)

Figure 5.7. Post-BD I_{sub} - V_g characteristics in the temperature range of 308–423 K of a TaN/TiN gate nMOSFET (labeled as D2) ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed under inversion mode CVS with $V_{gstress}$ of 3.7 V and $I_{gl} = 10 \mu\text{A}$. (b) Pre- and post –BD I_{sub} - V_g at 373 K of another TaN/TiN gate nMOSFET, S1, shown in Fig. 5.1.

5.2.4 Schottky-like behavior of breakdown path

Figure 5.7 (a) shows the post-BD I_{sub} - V_g characteristics of an inversion mode stressed TaN/TiN gate nMOSFET, D2, with $I_{gl} = 10 \mu\text{A}$ at different temperatures. The post-BD I_{sub} - V_g characteristics show a *Schottky-like* behavior of a possible junction

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between the BD path and p-type substrate. Assuming the BD path is *metal*-like, the corresponding effective Schottky barrier (Φ) height and ideality factor (n) have been calculated by curve fitting of the post-BD I_{sub} - V_g for 7 inversion mode stressed metal gate nMOSFETs (labeled as D1 – D7) with $I_{gl} = 5 \mu\text{A} - 2 \text{ mA}$ (see Fig. 5.8) with the Schottky-diode current-voltage equation expressed as [156]:

$$I = I_{sat} \exp\left(\frac{q V}{n k T}\right) \quad (5.1)$$

$$I_{sat} = A A^{**} T^2 \exp\left(\frac{-\phi}{kT}\right) \quad (5.2)$$

where A is the area, A^{**} is the effective Richardson constant of ($32 \text{ A cm}^{-2} \text{ K}^{-2}$) [157], T is the temperature in K, q is the electronic charge, V is the applied voltage, n is the ideality factor, Φ is the barrier height and k is the Boltzmann's constant. Both n and ϕ for all samples lies between 1.2-1.8 and 0.24 - 0.47 eV, respectively (Fig. 5.8 (b) & 5.8 (c)), indicating that metal filamentation of the BD path. Similar *Schottky*-like behavior of the BD path has only been observed for *metal* gate pMOSFETs under accumulation CVS even at low I_{gl} of $5 \mu\text{A}$ (see Fig. 5.9).

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Figure 5.8. Schottky diode ideality factor n and barrier height Φ measured by using the post-BD $I_{\text{sub}}-V_g$ at different temperature (308 - 423 K) of 7 TaN/TiN gate nMOSFETs (D1 - D7) (EOT = 1.95 nm) ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed under inversion mode CVS with $V_{g\text{stress}}$ of 3.7 V and I_{gl} of 5 μA - 2 mA (D2 is also shown in Fig. 5.7 (a)) with the Schottky-diode equation (see equations (5.1) and (5.2)). (a) Ideality factor with temperature, (b) Arrhenius plot. The slope of the Arrhenius plot gives barrier height and intercept ($\text{Ln}(AA^{**})$) gives the area. (c) Schottky barrier height (measured by the slopes of the plots of Fig. 5.8 (b)) with the calculated BD path diameter obtained from the intercept of the plots of Fig. 5.8 (b).

In addition, if the nMOSFET stressed with $I_{gl} \leq 2 \mu\text{A}$ during the substrate injection, the Φ and n cannot be extracted from the post-BD $I_{\text{sub}}-V_g$ (see Fig. 5.7 (b)) confirming that the BD path is non *metal*-like or is switching “off”. Similarly, the breakdown path in the *metal* gate n/pMOSFETs stressed under the gate injection gives no evidence/presence of the Schottky-like behavior even if I_{gl} is much higher than 5

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μA . Similar behavior has also been reported for *poly-Si* gate stacks, if I_{gl} is lower than $\sim 50 \mu\text{A}$ [158]. It indicates that the *metal-like* filamentation of BD path only takes place during the substrate injection of the metal gate n/pMOSFETs for $I_{gl} \geq 2 \mu\text{A}$, resulting in ultrafast progressive breakdown (see Fig. 5.1). The Schottky-like behavior is also supported and explained in terms of the tunneling equation using the band bending, Boltzmann distribution and Fermi-Dirac distribution. The details are presented in Appendix II.

Figure 5.9. Schottky diode ideality factor n and barrier height Φ measured by using the post-BD I_{sub} - V_g at different temperature (307 – 423 K) of 5 TaN/TiN gate pMOSFETs (labeled as P1 - P5) ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) (EOT = 1.71 nm) stressed under accumulation mode CVS with $V_{gstress}$ of 3.6 - 3.7 V and I_{gl} of 5 - 30 μA using the Schottky diode equation (see equations (5.1) and (5.2)). (a) Ideality factor with temperature, (b) Arrhenius plot, (c) Schottky barrier height with breakdown location .

5.2.5 Quantum point contact-like behavior

Detailed electrical characterization of the breakdown path in the high-κ/metal gate stack clearly shows the presence of a possible *metal*-like filament breakdown path as the post-BD conductance (i.e., dI_g/dV_g [47, 48]) is extremely high and in a similar range once $I_{gl} \geq 5 \mu\text{A}$ (Fig. 5.10). In addition, the negligibly small post-BD conductance verifies that below $2 \mu\text{A}$ of I_{gl} , the breakdown path is *non-metal* like (see Fig. 5.10). The histogram of the post-BD conductance of the *metal* gate nMOSFETs stressed under the substrate injection shows two peaks at 0.15 and 0.4 [$2e^2/h$] (Fig. 5.11). Based on a population of 50 samples, the data indicate that there is quantum confinement [47, 48] of the breakdown path in the metal gate MOSFET. Figure 5.12 (a) shows the post-BD I_g - V_g characteristics of 7 *metal* gate nMOSFETs. Quantum point contact (QPC) barrier height ϕ , shape parameter α and barrier thickness (T_B) were calculated using the post-BD I_g - V_g of the 7 *metal* gate nMOSFETs as shown in Fig. 5.12 (a), with the QPC adiabatic equations expressed as [48]:

$$I = \left(\frac{4e}{\alpha h} \right) \exp(-\alpha \phi) \exp\left(\frac{\alpha e V_g}{2} \right) \quad (5.3)$$

$$T_B = \left(\frac{\alpha h}{2\pi^2} \right) \left(\sqrt{\frac{2\phi}{m_z^*}} \right) \quad (5.4)$$

where I is the current, ϕ is the barrier height, α is shape parameter, h is the Planck's constant, e is the electronic charge, V_g is the gate voltage and m_z^* is $0.19m_o$ (m_o is free electron mass). The calculated results are shown in Figs. 5.12 (b) and (c).

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Figure 5.10. Pre- and post-BD conductance of 9 TaN/TiN nMOSFETs ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed with inversion mode CVS with $V_{g\text{stress}}$ of 3.7 V and $I_{gl} = 2 \mu\text{A} - 2 \text{mA}$.

Figure 5.11. Post-BD conductance of about 50 TaN/TiN gate nMOSFET stressed under inversion mode CVS with $V_{g\text{stress}} = 3.7 \text{ V}$ and $I_{gl} = 5 \mu\text{A} - 2 \text{mA}$. Two peaks at $0.15 [2e^2/h]$ and $0.40 [2e^2/h]$ indicate the quantum confinement of the BD path.

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Figure 5.12. (a) Post-BD I_g - V_g of 7 TaN/TiN gate nMOSFETs shown in Fig. 5.8. Quantum point contact barrier height, barrier thickness and shape parameter α were measured by the post-BD I_g - V_g characteristics shown in (a) with QPC adiabatic equations (5.3) and (5.4). (b) QPC barrier height (measured using equation (5.3)) and barrier thickness (measured using equation (5.4)) with the post-BD conductance. It is observed that the post-BD conductance is inversely proportional to the barrier height and the barrier thickness. (c) T_B with the shape parameter α . (d) The diameter of the constriction area near the narrowest point (measured using equation (5.5)) with barrier height as shown in (b).

After obtaining the QPC ϕ from Fig. 5.12 (b), the approximate diameter of the constriction area at the narrowest point has been calculated by considering the circular infinite quantum well at the constriction and using the expression [159]:

$$\varphi = \frac{h^2}{8\pi^2 m_z^* R^2} [a_{(0,0)}]^2 \quad (5.5)$$

where R is the radius of circular constriction area, and $a_{(0,0)} = 2.40483$ [159]. The results are shown in Fig. 5.12 (d). The QPC-like behavior (Figs. 5.10 - 5.12) of the BD path suggests that the BD path has an *hour-glass* shape with a “necking” of ~ 1 - 3 nm (Fig. 5.12 (d)), as the calculated effective BD path diameters are in the range of 12 - 63 nm at the Schottky interface (Fig. 5.8 (c)).

5.2.6 Physical evidences of metal-like filamentation of breakdown path

5.2.6.1 Non-visible microstructural damages for $I_{gl} \leq 2$ mA

Figures 5.13 (a) and (b) show the TEM micrographs of two TaN/TiN nMOSFETs (S1 and S4) shown in Fig. 5.1, stressed with I_{gl} of 500 μ A and 2 mA respectively. Even though the gate leakage current (Fig. 5.1) shows a high degradation rate and the post-BD R_{geff} of the devices is < 50 k Ω , the devices exhibit no *visible* microstructural damage in the TEM micrographs especially at the interfaces of IL/Si, HfO₂/IL, and HfO₂/TaN. This phenomenon has been confirmed for more than 25 metal gate MOSFETs. This finding is different from the HfO₂/ *poly-Si* gate stack nMOSFETs stressed under inversion mode CVS, in which severe microstructural damages have been observed at relatively low I_{gl} of 50 μ A (Fig. 4.1 in Chapter 4), even if the stress was cut off instantaneously upon I_g reaching I_{gl} .

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Figure 5.13. TEM micrographs of two $\text{SiO}_x/\text{HfO}_2$ high- κ /TaN/TiN narrow nMOSFETs (S3 and S4) shown in Fig. 5.1 ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed under inversion mode CVS with $V_{g\text{stress}}$ of 3.7 V. (a) S3 ($I_{gl} = 500 \mu\text{A}$), and (b) S4 ($I_{gl} = 2 \text{ mA}$). The dotted circles in the inserts show the BD locations ($0.65 L$ for S3 and $0.47 L$ for S4) measured electrically using equation (2.7). No visible physical damage was observed in either MOSFET.

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Figure 5.14. TEM micrographs and elemental dot maps of a HfO₂ high- κ /TaN/TiN gate stack nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed under inversion mode (i.e., substrate injection) SCVS with $V_{g\text{stress}}$ of 3.7 V and I_{gl} of 2 mA. The device was subjected to an additional 1000 s stress after reaching I_{gl} of 2 mA. (a) TEM/EDS shows Ta, N and Hf present at the BD spot. The dotted circle in the insert shows the BD spot, which matches with that measured electrically using equation (2.7) $\sim 0 L$ (i.e., near the S/D extension region). (b) EELS elemental mapping of BD spot - (A) Silicon, (B) Oxygen, (C) Nitrogen. (c) TEM micrograph of the BD location of another TaN/TiN gate nMOSFET stressed under inversion mode CVS with $V_{g\text{stress}}$ of 3.7 V and $I_{gl} = 7$ mA. A Gatan package commercial software three window is used for elemental mapping. The scale for the elemental mapping is kept identical to TEM micrograph.

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5.2.6.2 Ta-based intermix at Si substrate (i.e., cathode side) during substrate injection

Prolonged stressing upon breakdown at $I_{gl} = 2$ mA (i.e., stress was not cut off immediately after gate leakage reaching I_{gl}) and breakdown at very high I_{gl} but less than 2 mA leads to severe microstructural damages during inversion mode stressing of nMOSFETs (see Fig. 5.14). During the additional stress of 1000 s at I_{gl} of 2 mA, and later stressing at a higher I_{gl} of 7 mA, a presence of a Ta-based intermix was observed on the cathode (i.e., Si substrate) side (see Fig. 5.14).

Figure 5.15. TEM micrographs of a HfO₂ high- κ /TaN/TiN gate stack nMOSFET ($W \times L = 0.25 \times 0.5$ μm^2) stressed under accumulation mode (i.e., gate injection) CVS with $V_{g\text{stress}}$ of -4.5 V and $I_{gl} = 20$ μA having the source and drain floated. The insert shows the BD location in the channel.

Figure 5.15 shows the TEM micrograph of the catastrophically damaged metal gate nMOSFET stressed under accumulation mode (i.e., gate injection). From the TEM/EDS (not shown here) analysis of the device, it is observed that there is absence of Ta at the anode (i.e., Si substrate) side during the gate injection (see Fig. 5.15). It is different from the case of severely damaged nMOSFETs stressed under the substrate injection, in which presence of the Ta-based intermixed is found on the Si substrate (i.e., cathode side) (see Fig. 5.14).

Figure 5.16. Flow chart showing the sequence of breakdowns in $\text{HfO}_2/\text{TaN}/\text{TiN}$ gate stack n/pMOSFETs during substrate injection.

5.2.7 Filamentation model

Figure 5.16 shows the flow chart of the sequences of breakdown in TaN/TiN gate n/pMOSFETs stressed under substrate injection. There are mainly two stages of BD. In stage I ($I_g \leq 2 \mu\text{A}$), the percolation path [21, 22, 44] continues to wear-out by the generation of defects during stressing (see Fig. 5.17 (a)). In this stage, the device experiences slow progressive BD/digital BD (see Region A, B, and C of Fig. 5.18(a)). Once the I_g reaches a higher value of about $2 \mu\text{A}$, due to a large electron density surging through the percolation path, localized enhancement of surface plasmon by the highly energetic electrons in the vicinity of the breakdown path/TaN interface takes place as the energy to excite the surface plasmon is proportional to $(1+\kappa)^{-1/2}$ [37,

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38]. Hence, it is much easier to excite surface plasmons at HfO₂ high- κ /TaN interface which require an energy of less than ~ 4.5 eV by considering the κ value of HfO₂ is 20. This is confirmed by the substantial increase in the holes current during the slow progressive BD of $I_g \leq 2$ μ A (Region A, B, and C in Fig. 5.18 (b)) by excitation and decay of surface plasmon. The localized hole current at the high- κ /metal-interface in the vicinity of the BD spot forces the unbound/loosely bounded Ta atoms/ions (as TaN gate is not perfectly stoichiometric [160]) to migrate immediately towards and fill the percolation path in the direction of electric field and form a stable “hour-glass” shaped metal filament (Figs. 5.5 and 5.17 (b)). It is believed that the “hour-glass” shape of the metal filament is due to incoming metal atoms/ions bombardment on the previous metal atoms/ions at the gate dielectric/silicon-interface, resulting in the lateral movement of metals atoms along the interface. Dekker *et al.* [161] and Lodder *et al.* [162] reported that in some metals such as Ta, Ti, Ca, Cr, V, Nb etc., the electromigration also takes place opposite to electron wind direction due to a significantly large contribution of hole current. Once the stable *metal*-like filament is formed, hot electrons could pass through it by suffering negligible amount of electron scattering or energy loss, resulting in an abrupt increase of the gate leakage current I_g (i.e., ultrafast progressive BD) (Figs. 5.1 and 5.18(a)), in which the post-BD transient is “unarrested” using the preset I_{gl} (Figs. 5.2 and 5.3) due to a limitation in the system response time, leading to *Schottky*-like and QPC-like behaviors of the breakdown path (Figs. 5.7 - 5.12). As the electrons may suffer negligibly small inelastic scattering within the *metal*-like BD path, the heat generated in the vicinity of the BD path is insignificant. It leads to minimized microstructural damages. This is the case if the stress is stopped instantaneously after reaching the threshold I_{gl} of 2 mA. Hence, the corresponding physical analysis results show no *visible*

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microstructural damages (Fig. 5.13). However, severe heating could take place due to the presence of high spreading resistance at the anode and cathode end of the *metal*-like BD path leading to huge microstructural changes shown in the Fig. 5.14. The subsequent prolonged stressing at I_{gl} of 2 mA and $I_{gl} \gg 2$ mA in our experiments under the substrate injection in the TaN/TiN n/pMOSFETs further enhanced the localized microstructural changes. In addition, the metal filamentation of the BD path is further supported by the presence of Ta at the substrate region in the vicinity of a BD path for catastrophically damaged nMOSFET stressed in inversion mode; confirming the migration of Ta atoms/ions opposite to electron wind direction (Fig. 5.14). On the other hand, we have not detected the presence of Ta atoms in the substrate region for severely damaged nMOSFETs stressed under the accumulation mode CVS (Fig. 5.15). Thus metal filamentation which leads the device to ultrafast progressive breakdown takes place only during the substrate injection in the metal gate n/pMOSFET.

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(a)

(b)

Figure 5.17. Schematics describing the *metal-like* filament formation of BD path in TaN/TiN gate n/pMOSFETs during substrate injection. (a) Stage I - formation of percolation path due to generation of stressed induced traps. (b) Stage II - “Hour-glass” shaped Ta/Ta⁺- metal filament formation due to localized enhancement of holes current by excitation and decay of surface plasmon in the vicinity of percolation path during slow progressive BD, resulting in ultrafast progressive breakdown.

(a)

(b)

Figure 5.18. (a) I_g evolution of three TaN/TiN gate nMOSFETs stressed under inversion mode CVS. Slow progressive BD at low gate leakage ($\leq 2 \mu\text{A}$) (See Region A, B and C) followed by an ultrafast progressive BD can be seen. (b) Electron-hole ratio during breakdown event of the devices shown in Fig. 5.18 (a). Hole current increases during slow breakdown transient (See Region A, B, and C). The dashed arrows show a sudden decrease in the hole current during ultrafast progressive BD, confirming the metal filamentation.

5.3 Summary

HfO_2 high- κ /TaN/TiN gate stack n/pMOSFETs have been studied. Ultrafast progressive breakdown is polarity dependent and is found only in the case of substrate injection in metal gate n/pMOSFETs. The ultrafast progressive breakdown observed is due to a metal-like filament formation at the breakdown spot during the substrate injection of the TaN/TiN n/pMOSFETs. The progressive BD transient of the metal gate pMOSFET is much slower than nMOSFET in inversion mode stress, which is a nominal operating condition for CMOS transistors. Due to the ultrafast progressive BD in the metal gate nMOSFET, pMOSFET in inversion mode will have a longer progressive transient than that of nMOSFET.

Chapter 6 BREAKDOWN INDUCED MICROSTRUCTURAL DEFECTS IN HIGH- κ / METAL GATE STACK MOSFETS

6.1 Introduction

In Chapter 4, the common and new failure mechanisms/defects associated with HfO₂ high- κ /poly-Si gate stack MOSFETs were discussed and compared to those found in the SiO_xN_y/poly-Si gate stacks. The substrate injection induced metal-like filamentation of the breakdown path in SiO_x IL/ HfO₂ high- κ /TaN/TiN gate stack n/pMOSFETs, resulting in ultrafast progressive breakdown, was studied in Chapter 5. Basically, two stages of BD in the metal gate MOSFETs have been reported during the substrate injection (Fig. 5.1); first the device experienced slow progressive BD/digital soft BD below 2 μ A gate leakage current, followed by an ultrafast PBD.

In this chapter, we study various failure defects associated with the breakdown in the HfO₂ high- κ /TaN/TiN metal gate stack MOSFET. Both common and new post-breakdown failure defects in the HfO₂ high- κ /metal gate stack MOSFETs will be compared to those previously observed microstructural damages in HfO₂ high- κ /poly-Si gate stacks. The sequence of the breakdown induced microstructural defects in the

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metal gate stacks will be also correlated with the gate leakage compliance current limit.

6.2 Common failure defects between metal gate and poly-Si gate stack MOSFETs

6.2.1 Dielectric-breakdown-induced migration

Similar to poly-Si gate MOSFETs (Figs. 4.9 and 4.10 Refs. 24, 68) DBIM is one of the common failure defects observed in metal gate MOSFETs. Figures 6.1 (a) and (b) show that Ni-silicide migration (i.e., DBIM) into the channel from both source and drain side of the TaN/TiN gate nMOSFETs stressed under inversion mode CVS. DBIM is also found in the accumulation mode stressed devices (see Fig. 6.1 (c)). Figure 6.1 (c) shows that Ni-silicide is missing at the drain side and has migrated towards the source upon breakdown of the metal gate nMOSFET. As shown in the insert of Fig. 6.1 (c), the gate dielectric remains intact even in the nickel accumulated area of the channel. DBIM is also seen for Ti- and Co-silicide in SiO_xN_y , Si_3N_4 , and HfO_2 MOSFETs having poly-Si gate (Figs. 4.9 and 4.10, Refs. 24, 68).

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Figure 6.1. (a) TEM micrographs showing nickel Ni migration in an inversion mode stressed HfO₂ high-κ/TaN/TiN nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) with $V_{gstress}$ of 4.2 V and I_{gl} of 5 mA. Ni migrates from both source and drain side into the channel. (b) EELS Ni elemental mapping of the device shown in (a) verifies the Ni migration in the channel. (c) TEM micrographs showing Ni migration in another accumulation mode stressed HfO₂ high-κ/TaN/TiN nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) with $V_{gstress}$ of -4.5 V and I_{gl} of 2 mA. The insert shows no oxide rupturing in the Ni accumulated area of the Si substrate. A Gatan package commercial software three window is used for elemental mapping. The scale for the elemental mapping is kept identical to TEM micrograph.

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On the other hand, from the reliability point of view, DBIM will result in catastrophic failure of the MOSFETs by electrically shorting the transistor gate/drain/source electrodes through the channel and/or the breakdown spot with the gate dielectric. The electrical and physical analysis results reveal that DBIM occurs for all the silicide materials tested (i.e., Ti, Co, and Ni) on both cathode and anode sides of the MOSFETs. However, it took place only in a range of medium to high gate leakage current during constant voltage stress. It is also observed that DBIM is independent of the gate dielectric materials (SiO_xN_y , Si_3N_4 , and HfO_2) as well as gate electrode materials (Ti-, Co-, Ni-silicided, poly-Si gate, and TiN/TaN gate) (see Figs. 4.9 and 4.10 and 6.1, and Refs. 24, 68). Hence, DBIM is a universal failure mechanism independent of stressing conditions of the MOSFETs, gate dielectrics and electrode materials.

In order to discuss the mechanism behind the DBIM, the migration of silicide/silicon interface is considered as a moving boundary problem. The motion of a phase boundary is caused by a net flux of matter across the boundary due the difference in the partial volumes between adjacent phases [163]. The net flux is expressed as the differences of velocity field:

$$\vec{J}_i^E \equiv C_i \cdot (R_{\vec{v}_i} - R_{\vec{v}_E}) = -D_i \nabla n_i + n_i \vec{v}_i \quad (6.1)$$

where $\vec{J}_i^E$ is the diffusive flux of species i (i.e., either the silicide metal M or Si in MSi_x) in (mole or gram) $\text{cm}^{-2} \text{sec}^{-1}$ with respect to the field E , C_i is the concentration of species i , expressed in (mole or grams) per cm^3 , R is the reference frame in which we measure velocities and fluxes and can be arbitrarily chosen, $R_{\vec{v}_i}$ is the average

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velocity of species i , and $R_{\vec{v}_E}$ is a velocity field, i.e., a vector quantity varying with position and time, D_i is the intrinsic diffusion coefficient, n_i is the number of species i per unit volume (either M or Si), ∇n_i is the concentration gradient, and $\vec{v}_i$ is the interface moving velocity. The above equation is equivalent to *Fick's first law*. The overall velocity of the moving boundary can be written as;

$$\vec{v} \equiv \frac{\vec{J}_{Si} + \vec{J}_M}{n} = M^B \Delta G \quad (6.2)$$

where M^B is the mobility of the boundary and ΔG is the corresponding free energy change per atom. Under the influence of both temperature gradient ∇T and electric field E , the flux of M and Si atoms can be expressed as [164];

$$J_{Si} = -D_{Si} \nabla n_{Si} + Z_{Si} \frac{eE}{kT} n_{Si} \frac{D_{Si}}{f_0} - Q_{Si} \frac{\nabla T}{kT^2} n_{Si} \frac{D_{Si}}{f_0} \quad (6.3)$$

$$J_M = -D_M \nabla n_M + Z_M \frac{eE}{kT} n_M \frac{D_M}{f_0} - Q_M \frac{\nabla T}{kT^2} n_M \frac{D_M}{f_0} \quad (6.4)$$

where Z_{Si} and Z_M are the effective valence of Si and M respectively, f_0 is the self-diffusion correlation factor, and Q_{Si} and Q_M are the heat of transport. The moving velocity of the silicide/silicon boundary can now be calculated using equations (6.2)-(6.4).

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Figure 6.2. Schametic showing a MOSFET consisting of a percolation path.

From equations (6.3) and (6.4), it can be seen that there are three main driving forces for silicide migration - the concentration gradient $-\nabla n_i$ (polarity independent), the electrical field E (polarity dependent), and the temperature gradient $-\nabla T$ (polarity independent). DBIM is an intricate balance among all three driving forces. For concentration gradient, $-\nabla n_i$, M moves preferentially from silicide to silicon (poly-Si gate or Si substrate) region due to $-\nabla n_i$, while Si moves from silicon to silicide (see Fig. 6.2). For the electric field E , M and Si both move in the electron wind direction from cathode to anode (see Figs. 4.9 and 4.10 and 6.1 and Refs. 24, 68). Current crowding effect plays a major role in the E field driven atomic flux. For temperature gradient $-\nabla T$, it can be either temperature change induced variation in the solubility of Si and M in silicon or silicide, or the instability of the silicide phases at different temperatures inducing phase transition from one silicide into other silicides.

Now we discuss the effect of a breakdown transient on DBIM. On the basis of our current results and understanding, it may be concluded that a breakdown transient

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has roughly two stages (Figs. 5.1 and Ref. 165). First a slow transient takes place with progressive degradation of the gate dielectric percolation path followed by a final fast transient, which causes the device to suffer HBD. It is observed that during the slow transient, the voltage (i.e., V_0 as shown in Fig. 6.2) at the junction of the percolation path resistance (R_{perc}) and parasitic resistance (R_{para}) (R_{para} is the sum of channel resistances and external resistances), which controls the effective electric field E_{eff} strength across the silicon/silicide junction is very low. This voltage becomes very high during fast transient [165]. Hence, E_{eff} across the silicon/silicide junction, which contributes to electromigration, increases during the breakdown transient due to a continuous decrease in R_{perc} and R_{para} (i.e., increase in V_0 as shown in Fig. 6.2). E as used in equations (6.3) and (6.4), thus, should be replaced by E_{eff} and is a function of R_{perc} and R_{para} instead of a constant. Similarly, during the breakdown transient, the thermal joule heating generates in the vicinity of the breakdown spot due a surging of the leakage current through the percolation path. By careful consideration of each stage above, the local temperature and the influence of temperature gradient $-\nabla T$, can be estimated.

Based on the above discussion and using equations (6.2), (6.3) and (6.4), the boundary movement can be estimated for the pre-breakdown stage, during slow transient soft breakdown stage, during fast transient soft breakdown stage, and the hard breakdown stage. The results are summarized in Table 6.1.

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Table 6.1. Silicide boundary moving velocity at different stages of the breakdown event as predicted by equation (6.2).

Stage	Temp. T (K)	Temp. gradient ΔT (K/100nm)	E -field (mV/100 nm)	Max. metal flux J_M (atoms/s- cm ²)	Max. silicon flux J_{si} (atoms/s-cm ²)	Boundary velocity v (nm/ μ s)
Pre-BD	373	0 to 75	0	2×10^{14}	2×10^{-11}	4×10^{-8}
Slow transient SBD	1687	0 to 1314	0	8×10^{18}	1.6×10^{18}	2×10^{-3}
Fast transient SBD	1687	0 to 1314	50	1.2×10^{21}	4.73×10^{18}	0.24
HBD	1687	0 to 1314	1.9×10^3	4.5×10^{24}	1.25×10^{23}	900

Comparing the four different stages as shown in Table 6.1, it can be seen that the negligible movement of the silicon/silicide boundary in the pre-breakdown stage and very slow movement in the soft breakdown slow transient stage (in this case zero electric field strength is considered across the silicon/silicide junction). The difference in the migration between the pre-breakdown and slow transient SBD stages is due to the local temperature. The breakdown induced local joule heating drives the diffusion and silicide movement (see Table 6.1). In the soft breakdown slow transient stage, which occurs intermittently for a long duration (from a few hours to even years) before the fast transient kicks-in at nominal operating stress voltage, the silicide movement accumulates, then gradually becomes substantial and poises a reliability concern. Such migration is polarity independent and the silicide from both gate and source/drain simply moves toward the breakdown spot during this stage [24, 68]. But in the fast transient SBD stage, a significantly faster migration is introduced when there is a small electrical field (assuming only 50 mV in our calculation) across the

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channel (see Table 6.1). Such electrical field strength becomes very high when R_{perc} becomes comparable to R_{para} during the later stage of SBD leading to fast transient [165]. Table 6.1 shows that slight electric field difference may trigger very fast silicide migration (silicide can migrate up to a few micrometers and into the channel region in a few micro-seconds), resulting in one-sided or two-sided DBIM, which causes catastrophic failure of the device. Such DBIM have been experimentally observed (see Refs. 24, 68 and Figs. 4.9, 4.10 and 6.1). In the final stage HBD, electromigration dominates the migration and the silicide movement is driven by the electrical field (i.e., R_{perc} becomes negligible and V_0 becomes very high across the channel and other high resistive paths). Such DBIM is very commonly seen in metal gate stack MOSFETs, in which ultrafast progressive breakdown (see Chapter 5) takes place during substrate injection (see Figs. 6.1 (a) and (b)). Similar to the electric-field driven DBIM, similar phenomenon has been observed in the study of eFUSE using electromigration in silicide [166, 167].

On the basis of our results and discussions, it can be said that the device experiences hard failure instantaneously, not because of the gate dielectric breakdown, but because of DBIM. This confirms some of our experimental observation discussed previously; i.e., a direct physical short between polysilicon gate and silicon channel does not necessarily lead to device hard failure (Figs. 4.1 and 4.2 and Ref. 69).

Figure 6.3. TEM micrograph of a SiO_x/HfO₂ high- κ /TaN/TiN gate stack nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed under accumulation mode (i.e., gate injection) CVS with $V_{g\text{stress}}$ of -4.5 V and $I_{gl} = 4$ mA, while the source and drain grounded. The arrow shows a corner breakdown along the spacer/high- κ interface.

6.2.2 High- κ /spacer-interface breakdown

Besides DBIM, another common post-breakdown microstructural defect in HfO₂/metal gate stack compared to HfO₂/poly-Si gate stack is the corner breakdown along the spacer/high- κ interface above the source and drain extension regions of MOSFETs during gate injection. Figure 6.3 shows an example of the corner breakdown along the spacer/high- κ interface during a gate injection stressing. This breakdown mechanism was attributed to the enhanced electric-field near the source/drain extension regions compared to the channel (Fig. 4.25) and interface defects along the spacer/high- κ gate dielectrics interface (Fig. 4.27). A model describing the corner breakdown along the spacer/high- κ interface is discussed in Chapter 4. Hence, spacer/high- κ interface engineering is needed to overcome this

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breakdown. Otherwise, it may be a severe problem for pMOSFETs during device operation i.e., inversion mode stress (i.e., gate injection).

6.3 New failure defects in metal gate compared to poly-Si gate MOSFET

6.3.1 Localized Amorphization of Si substrate

Besides the metal-like filamentation of the breakdown path and the presence of Ta-based intermix at the Si substrate during substrate injection of metal gate MOSFETs (Chapter 5), Figs. 5.15 and 6.4 (a) show a polarity dependent localized anode amorphization (i.e., amorphization of Si substrate) as another new failure defect in the vicinity of the breakdown path during gate injection of the metal gate stack nMOSFETs. In particular, the interfacial layer was ruptured as shown in Fig. 5.15. The localized amorphization has been observed in the range of the gate leakage compliance current limit of 20 – 40 μA with a prolong stress of another ~ 1000 s. In this experimental condition, the electron flux reaching the anode electrode of the metal gate nMOSFET (i.e., Si substrate) during the gate injection is very high (10^{26} – 10^{27} electrons $\text{cm}^{-2}\text{s}^{-1}$ by considering the breakdown path diameter of 10 - 20 nm). At the same time, the electron dose received by the silicon substrate is more than 10^{29} electrons cm^{-2} . It is believed that the high dose of the energetic electrons may be able to produce hot phonons having temperature of ~ 1200 K [168, 169] at the silicon substrate. The hot phonons and high electron flux will be able to create lattice distortion and displacement of the silicon atoms, resulting in point defects. The clustering of the point defects [170] leads to the localized amorphization of the Si substrate (Figs. 5.15 and 6.4 (a)) observed during the gate injection of the metal gate

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MOSFETs. It is reported that the amorphization is also possible by very high energy electron irradiation [171]. The anode amorphization has also been seen in HfO_2 /poly-Si gate stacks, but having different microstructural changes (see Fig. I.3 in Appendix I).

Figure 6.4. TEM and HRTEM micrographs of a $\text{SiO}_x/\text{HfO}_2$ high- κ /TaN/TiN gate stack nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed under accumulation mode (i.e., gate injection) CVS with $V_{g\text{stress}}$ of -4.5 V and $I_{gl} = 4$ mA, while the source and drain grounded. (a) TEM micrograph showing the whole channel, (b) HRTEM micrograph of the spot shown by the dotted circle in (a). An amorphization of the Si substrate and delamination of metal gate with HfO_2 can be seen.

6.3.2 Metal high- κ delamination

Figures 6.4 (a) and (b) show a delamination along the TaN/ HfO_2 -interface of a TiN/TaN metal gate stack from HfO_2 high- κ gate dielectric. The post-BD electrical measurements showed an open circuit between the gate and the substrate. In HfO_2 high- κ /poly-Si gate stack, the delamination along the poly-Si/high- κ -interface has never been observed. It is believed that the metal/high- κ delamination is mainly due to four reasons. First, the adhesion of metal on oxide is less compared to the adhesion of poly-Si on oxide [172]. Second, the chemical reaction between metal gates and

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HfO₂ gate dielectric is less evident compared to poly-Si gate with HfO₂ [8, 90, 91, 121, 127]. Hence, the metal gate adheres less strongly with HfO₂ than a poly-Si gate with a HfO₂ gate dielectric. Third, metal/high- κ -interface normally consists of a large number of extrinsic defects [123]. Fourth, the electric field strength at metal/high- κ -interface is higher compared to that of poly-Si/high- κ -interface due to a large difference of the dielectric constant between the metal gate and high- κ gate dielectric [148]. These four mechanisms make metal/high- κ -interface as one of the weakest links in the metal/high- κ gate stack for laminated metal gate structures. Hence, it can be easily lead to delamination along the TaN/HfO₂-interface in metal/high- κ system.

Figure 6.5. Sequence of the post-BD microstructural defects in HfO₂ high- κ /TaN/TiN gate stack nMOSFETs with gate leakage compliance current limit I_{gl} .

6.4 Summary

Besides metal-like filamentation of breakdown path and Ta-based intermix formation on the cathode side in *metal* gate MOSFET during substrate injection,

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localized amorphization and delamination are found in *metal* gate, but *not* in *poly-Si* gate MOSFETs. Figure 6.5 shows the sequences of the post-breakdown microstructural defects in *metal* gate MOSFETs for various I_{gl} . DBIM is found as a universal failure defect. Table 6.2 compares the post-breakdown failure defects observed in *metal* gate to poly-Si gate MOSFETs.

Table 6.2. Summary of post-breakdown failure defects for metal gate stack in comparison to poly-Si gate stack MOSFETs.

Failure Mechanisms/defects	Metal gate stacks	Poly-Si gate stacks
Filamentation	Yes [Chapter 5]	No [Chapter 4, 23-26, 61-65, 68, 69]
Intermixing of gate electrode	Yes [Chapter 5]	No [Chapter 4, 23-26, 61-65, 68, 69]
Localized Amorphization	Yes (Figs. 5.15 and 6.4 (a))	No [Chapter 4, 23-26, 61-65, 68, 69]
Delamination	Yes (Figs. 6.1 (a) and (b))	No [Chapter 4, 23-26, 61-65, 68, 69]
DBIE	Yes	Yes [Chapter 4, 23-26, 61-65, 68, 69]
DBIM	Yes (Fig.6.1)	Yes [Chapter 4, 23-26, 61-65, 68, 69]
Spacer/ high-κ interface BD	Yes (Fig. 6.3)	Yes [Chapter 4, 23-26, 61-65, 68, 69]

Chapter 7 CONCLUSION AND RECOMENDATIONS

7.1 Conclusion

Failure mechanisms/defects in SiO_x IL/HfO₂ high- κ /poly-Si gate stack and SiO_x IL/HfO₂ high- κ /TaN/TiN gate stack MOSFETs have been studied. SiO_xN_y/poly-Si and Si₃N₄/poly-Si gate stack MOSFETs were also studied for comparison. DBIE is a common failure defect of MOSFETs. DBIM mainly driven by the electric field is found as another universal defect that would lead to catastrophic failure during breakdown transient.

In addition to DBIE and DBIM, new failure mechanisms/defects in SiO_x IL/HfO₂ high- κ /poly-Si gate stacks have also been observed as compared to ultrathin SiO_xN_y/poly-Si and Si₃N₄/poly-Si gate stacks. Multiple breakdowns in *small* area ($\leq 1 \mu\text{m}^2$) SiO_x IL/HfO₂ high- κ /poly-Si gate stacks were commonly observed. This is different from *small* area SiO_xN_y/poly-Si and Si₃N₄/poly-Si gate stacks, in which single progressive breakdown is commonly observed. Grain-boundary assisted channel breakdown and field-assisted corner breakdown were found to be responsible for the multiple breakdowns observed in the *small* area SiO_x/HfO₂ high- κ /poly-Si gate

stack transistors. HfO_2 high- κ /spacer-interface breakdown was also observed in high- κ /poly-Si gate stacks stressed under accumulation mode. A model is proposed to describe the high- κ /spacer-interface BD by considering the high- κ /spacer-interface as the most defective site and the existence of a high electric field at the S/D extensions region relative to the channel.

On the other hand, a post-BD “*ball-shaped*” capping layer at the anode side of the device is commonly seen in SiO_x IL/ HfO_2 high- κ /poly-Si gate stack MOSFETs. On the basis of TEM/EELS and EDS analysis, the “*ball-shaped*” capping layer induced by BD in high- κ /poly-Si gate stack nMOSFETs was found to be composed of Hf-related compounds, either HfSi_xO_y or/and HfSi_x . The thermally assisted chemical reactions in the vicinity of the breakdown path are considered as the main driving force for the formation of the “*ball-shaped*” capping layer. A SHIC model describing the breakdown mechanism and evolution in the HfO_2 /poly-Si gate stacks is proposed and verified by the electrical and physical results. The post-BD I - V characteristics are described by SHIC model.

Two stages of breakdown are observed in the SiO_x IL/ HfO_2 high- κ /TaN/TiN gate stack MOSFETs. First the MOSFET suffered a slow progressive breakdown followed by an ultrafast progressive breakdown. The ultrafast progressive breakdown is *polarity* dependent and is found only in the case of substrate injection in metal gate n/pMOSFETs. It is established that the ultrafast progressive breakdown is due to the formation of a metal-like filament in the breakdown path by migration of Ta/Ta⁺ towards the breakdown path in the direction of excessive hole flow generated by a localized excitation and decay of surface plasmons at the high- κ /metal-interface in the vicinity of breakdown spot. A model based on an “hour-glass” shaped metal-like filamentation of breakdown path is proposed which was verified by electrical and

physical analysis results. Due to the *polarity* dependent ultrafast progressive BD in metal gate nMOSFET, pMOSFET in inversion mode will have a longer progressive transient than that of nMOSFET.

Besides metal-like filamentation of breakdown path, Ta-based intermix formation at the Si substrate in *metal* gate nMOSFET during substrate injection is also observed, which is different from *poly-Si* gate MOSFETs. Localized amorphization and delamination were found as other new failure defects in *metal* gate, but *not* in *poly-Si* gate MOSFETs. The Sequence of the post-breakdown microstructural defect formation in *metal* gate MOSFETs has also been established. On the other hand, similar to poly-Si gate MOSFETs, DBIE, DBIM, and Spacer/ high- κ interface breakdowns are also observed in SiO_x IL/HfO₂ high- κ /TaN/TiN gate stack MOSFETs.

7.2 Recommendations

On the basis of the physical and electrical analysis results, it is established that grain boundaries in the polycrystalline HfO₂ gate dielectrics are the weakest links to form breakdown path, resulting in multiple breakdowns in small area MOSFETs. Hence, breakdown study of polycrystalline HfO₂ gate dielectrics with the aid of scanning tunneling electron microscopy (STEM) will be helpful to provide more insight about the grain boundary assisted breakdown. Also, study of the breakdown mechanism in amorphous HfSiO₄ gate dielectric and its comparison to the breakdown mechanism in polycrystalline HfO₂ gate dielectrics will be helpful to study the exact role of grain boundaries on the breakdown of the polycrystalline gate dielectrics.

The existence of a high electric field strength near the “L-shape” corner of poly-Si edge due to differences in the dielectric constants of the high- κ and spacer

materials is a major concern for the breakdown near the S/D extensions. It is also found that the high- κ /spacer-interface is the weakest link for breakdown path creation. Hence, gate stack structure and precise high- κ /spacer-interface engineering may minimize the corner breakdown.

SHIC model is proposed to describe the breakdown in HfO_2 high- κ /poly-Si gate stacks. In the SHIC model, the thermochemical reactions among high- κ , poly-Si gate, IL and silicon substrate and the formation of a “ball-shaped” capping layer consisting of HfSi_xO_y and HfSi_x are discussed. EELS analysis by normal TEM/EELS system (~ 1 eV of resolution) is not sufficient to study the exact chemistry of the “ball-shaped” capping layer. It is believed that monochromator-based STEM/EELS (0.1 - 0.2 eV of resolution) will be able to reveal the exact chemistry of the capping layer, which will provide more insight to understand the effect of SHIC on the gate leakage current evolution and post-BD device performance.

Metal-like filamentation of the breakdown path in metal gate MOSFETs during substrate injection is verified by electrical and physical analysis results. Physically, it is a challenging task to detect a metal-like breakdown path of diameter of about 1 - 4 nm in the dielectric with conventional transmission electron microscope equipped with EELS capabilities having energy resolution of about ~ 1.0 eV. We believe that the nano-diameter metal-like filament can be observed and studied with the aid of monochromator-based STEMs having energy resolution of 0.1 - 0.2 eV.

In addition, the metal-like filamentation of the breakdown path during substrate injection is observed in the PVD deposited TaN/TiN gate stack MOSFETs, which has a non-perfect stoichiometric high- κ /metal gate-interface. Hence, a lot of loosely and unbound Ta atoms/ions are present at the high- κ /metal gate-interface, which may accelerate the process of the metal-like filament formation of the

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breakdown path. So, it will be worth to study FUSI gate stack MOSFETs, which has stoichiometric high- κ /FUSI gate-interface. This may provide new insight for the role of high- κ /metal-interface on the metal-like filamentation of the breakdown path.

Author's Publications

Journal papers:

1. **R. Ranjan**, K.L. Pey, C.H. Tung, D.S. Ang, L.J. Tang, T. Kauerauf, R. Degraeve, G. Groeseneken, S. De Gendt, and L.K. Bera, "Ultrafast progressive breakdown associated with metal-like filament formation of breakdown path in $\text{HfO}_2/\text{TaN}/\text{TiN}$ transistor", *Applied Physics Letters*, Vol. 88, 2006, pg. 122907. Also selected for *Virtual Journal of Ultrafast Science*, Vol. 5, April 2006.
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Appendix I

I Other post-breakdown phenomenon in $\text{SiO}_x/\text{HfO}_2/\text{poly-Si}$ gate stack MOSFETS

I.1 Asymmetrical I - V characteristics

Figure I.1 shows the pre- and post-BD I - V characteristics of a HfO_2 High- κ /poly nMOSFET, which failed during an inversion mode CVS. An asymmetry between the drain side (resistive-like) and source side (transistor-like) post-BD I - V characteristics can be easily seen. From the asymmetry, it can be deduced that the HBD occurred near the drain side. It is also confirmed by the BD-location measurement method reported by R. Degraeve *et al.* [53] (see equation (2.7)). Similar results have been reported for one-sided HBD in SiO_xN_y and Si_3N_4 gate dielectrics [61, 63-65, 68, 69].

(a)

(b)

Figure A.1. Pre- and post-BD I - V characteristics of a $\text{SiO}_x/\text{HfO}_2/\text{poly-Si}$ gate stack nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) failed during CVS at 3.8 V with a compliance current limit I_{gl} of 1mA. Only one BD event was observed. (a) $I_{ds} - V_{ds}$, (b) $I_{sd} - V_{sd}$.

I. 2 Channel short (i.e., both source and drain resistive-like I - V characteristics)

Figure I.2 shows the pre- and post-BD I - V characteristics of a HfO_2 High- κ /poly nMOSFET, which failed during an inversion mode CVS. Both resistive-like source and drain post-BD I - V characteristics can be easily seen. Similar results have

been reported for channel short HBD in SiO_xN_y and Si_3N_4 gate dielectrics [61, 63-65, 68, 69].

(a)

(b)

Figure I.2. Pre- and post-BD I - V characteristics of a $\text{SiO}_x/\text{HfO}_2/\text{poly-Si}$ gate stack nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) failed during CVS at 3.8 V with a compliance current limit I_{gl} of 2mA. (a) $I_{sd} - V_{sd}$, (b) $I_{ds} - V_{ds}$.

I. 3 Amorphization of anode material

Figures I.3 (a) and (b) show the TEM micrographs of amorphization of the anode materials associated with a breakdown event in HfO₂ high- κ /poly-Si gate stack MOSFETs stressed in accumulation and inversion mode, respectively. The joule heating associated with the breakdown is attributed to be the root cause in melting down the Si substrate underneath and poly-Si above the gate stacks respectively, forming an amorphous-like insulating layer.

(a)

(b)

Figure I.3. TEM micrographs of HfO₂/poly-Si gate stacks. (a) nMOSFET ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) stressed in accumulation mode with $V_{g\text{stress}} = -3.8 \text{ V}$ keeping the I_{gl} of $300 \mu\text{A}$. (b) nMOSFET ($W \times L = 0.25 \times 0.05 \mu\text{m}^2$) stressed under inversion mode with $V_{g\text{stress}} = 3.5 \text{ V}$ and $I_{gl} = 300 \mu\text{A}$.

I.4 I_{dsat} Recouping

Figure I.4 (a) shows the pre- and post-BD I - V characteristics of a 500nm gate length $\text{HfO}_2/\text{poly-Si}$ gate stack nMOSFET under successive constant voltage stress by increasing I_{gl} slowly from 50 μA upto 250 μA . One of the notable observations is that the I_{dsat} values for $I_{gl} = 50 \mu\text{A}$ is smaller than that for $I_{gl} = 100 \mu\text{A}$ and 150 μA . This phenomenon was observed in several devices (see Fig. I.4 (b)). Such phenomena have not been observed in the traditional SiO_xN_y and Si_3N_4 gate dielectrics, and are called, in this study, post-BD I_{dsat} recouping. The peak transconductance measured at $V_d = 0.1 \text{ V}$ correlates well with the I_{dsat} recouping (see Fig. I.5 (a)). The correlation of the I_{dsat} recouping with the post-BD effective gate resistance can also be seen (see Fig. I.5 (b)). Hence, we postulate that the I_{dsat} is closely related to the recovery of the breakdown path and possibly the healing of some microstructural damages and broken bonds.

(a)

(b)

Figure I.4. Recouping in the post-BD I_{dsat} of $\text{SiO}_2/\text{HfO}_2/\text{poly-Si}$ gate stack nMOSFETs stressed under SCVS. (a) A typical pre- and post-BD I - V characteristics of an I_{dsat} -recouped nMOSFET ($W \times L = 1.0 \times 0.5 \mu\text{m}^2$) as shown in (a). We can see that the post-BD I_{dsat} -recouping in the range of $I_{gl} = 50$ - $250 \mu\text{A}$ at $100\mu\text{A}$ (3) and $150 \mu\text{A}$ (4). (b) I_{dsat} recouping for 5 nMOSFETs of $L=0.05$ and $0.5\mu\text{m}$, while $W=0.25, 0.5, 1.0$, and $5.0 \mu\text{m}$. D2 is shown in Fig. I.4.

(a)

(b)

Figure I.5. (a) Correlation between I_{dsat} recouping and the peak transconductance, g_m , measured at $V_d = 0.1V$ of a $SiO_x/HfO_2/poly-Si$ gate stack nMOSFET ($W \times L = 1.0 \times 0.5 \mu m^2$) stressed in inversion mode SCVS with $V_{gstress}$ of 3.5 V. (b) The corresponding post-BD effective gate resistance $R_{geff} @ V_g = 1.5 V$ [61] of the device shown in (a).

Appendix II

Derivation of post-breakdown conduction in metal gate stack MOSFETs:

In Chapter 5, the Schottky-like behavior of the post-breakdown leakage current was discussed. In this appendix, we report a possible explanation for such behavior in terms of the tunneling equation. This alternative approach uses band bending, Boltzmann distribution and Fermi-Dirac distribution to support the Schottky-like behavior of the leakage current.

Figure II.1. Energy-band-diagram of a breakdown experienced n-type Si/thin insulating layer/metal electrode stack, similar to hard breakdown experienced metal gate stack pMOSFET. The red arrow indicates the tunneling of charge carrier.

In order to model the post-BD leakage current, a n-type Si/thin insulating layer/metal gate stack is considered (see Fig. II.1). Using MOS theory, the following expressions can be defined during positive bias of the stack [173, 174]:

$$E_{CS} - E_{FS} = \frac{E_g}{2} - q\phi_s \quad (\text{II.1})$$

$$q\phi_B = E_F - E_S \quad (\text{II.2})$$

where E_{CS} is the conduction band edge at the surface, E_{FS} is the Fermi level edge at the surface, E_g is the band gap of silicon, and ϕ_s is the surface potential. During positive bias, the tunneling current has two components: 1) direct current, and 2) reverse current. First we consider the reverse current is zero. Hence, using the Boltzmann distribution, the tunneling current density can be expressed as [174, 175, 176]:

$$J = \frac{4\pi qm}{h^3} \int_{E_{CS}}^{\infty} f(E - E_{FS}) \int_0^{E - E_{CS}} T(E - E_t) dE_t dE \quad (\text{II.3})$$

where m is the effective mass of charge carrier, q is the electronic charge, and h is the Planck's constant. For the hard breakdown case the transmission probability of the charge carrier can be considered as 1. Hence, equation (II.3) can be expressed as:

$$J = \frac{4\pi qm}{h^3} (kT)^2 \exp\left(\frac{E_{FS} - E_{CS}}{kT}\right) \quad (\text{II.4})$$

Using equation (II.1), equation (II.4) can be expressed as in terms of surface potential:

$$J = A^* T^2 \exp\left(\frac{-E_g}{2kT}\right) \exp\left(\frac{q\phi_s}{kT}\right) \quad (\text{II.5})$$

where A^* is $(4\pi qmk^2)/h^3$. Equation (II.5) can be also expressed as in terms of band bending:

$$J = A^* T^2 \exp\left[\frac{-(E_g - 2q\phi_B)}{2kT}\right] \exp\left(\frac{q\psi_s}{kT}\right) \quad (\text{II.6})$$

By considering the case of equilibrium, when there is a balance between the direct current and reverse current, the tunneling current can be expressed as:

$$J = A^* T^2 \exp\left[\frac{-(E_g - 2q\phi_B)}{2kT}\right] \left\{ \exp\left(\frac{q\psi_s}{kT}\right) - 1 \right\} \quad (\text{II.7})$$

It can be seen that equations (II.6) and (II.7) is similar to the Schottky diode equations shown in equations (5.1) and (5.2) and Ref. 156. In equations (II.6) and (II.7), the tunneling current is dependent on the band bending, not on the applied voltage. Using Fermi-Dirac distribution equation (II.6) can be expressed as [177, 178]:

$$J = A^* T^2 F_1 \left(-\frac{E_g - 2q\phi_B}{2kT} + \frac{q\psi_s}{kT} \right) \quad (\text{II.8})$$

where F_1 is the first order Fermi-Dirac integral. In order to model the post-BD gate leakage current, which is obtained experimentally with applied voltage V_g , there is need to correlate the band bending with the applied voltage. Here it is assumed that the band bending at the location of the breakdown is similar to the band bending of a fresh device. To further simplify the problem, the band bending with the applied voltage is expressed as [179]:

$$\psi_s (V_g) = \frac{(E_g - 2q\phi_B)}{\pi} \arctg \left[\frac{\pi V_g / n}{E_g - 2q\phi_B} \right] \quad (\text{II.9})$$

where $\psi_s (V_g \rightarrow \infty) = \frac{E_g}{2} - q\phi_B$, $\psi_s (V_g \rightarrow 0) = \frac{V_g}{n}$ and n is

the ideality factor. It is believed that n is related to the filling up of the surface states. With the appropriate modifications, equations (II.1) – (II.9) are also valid for p-type Si substrate under negative bias.

Figure II.2 shows the relationship between ψ_s and the applied voltage (ψ_s is calculated using equation (II.9) by considering the ideality factor $n = 1$). It can be seen

that in the low voltage region ψ_s is linear function of the applied voltage, but it saturates at high voltage.

Figure II.2. Plot shows the ψ_s versus applied voltage relationship.

Figure II.3 (a) shows that the post-BD I_{sub} fits well with the simulated leakage current using equations (II.6), (II.8) and (II.9). Similar to the post-BD I_{sub} of an accumulation mode stressed metal gate stack pMOSFET, the post-BD substrate current of an inversion mode stressed TaN/TiN gate stack nMOSFET also fits well with the simulated leakage currents (see Fig. II.3 (b)). This study further supports the Schottky-like behavior of the post-BD leakage current of the metal gate n/pMOSFETs during substrate injection as discussed in Chapter 5.

(a)

(b)

Figure II.3. Comparison of the post-BD I_{sub} (measured at 393 K) of $\text{SiO}_x/\text{HfO}_2/\text{TaN}/\text{TiN}$ gate stack n/pMOSFETs ($W \times L = 0.25 \times 0.5 \mu\text{m}^2$) with the simulated leakage currents using equations (II.6), (II.8) and (II.9). (a) pMOSFET stressed under accumulation mode CVS, (b) nMOSFET stressed under inversion mode CVS.

Summary

Post-breakdown conduction in metal gate stack MOSFETs is derived in terms of the tunneling equation considering band bending, Boltzmann distribution and Fermi-Dirac distribution. The tunneling equation shows the T^2 dependence of the leakage current similar to the Schottky-like behavior of the post-BD leakage current of the metal gate stack MOSFETs discussed in Chapter 5. The simulated leakage current using derived tunneling equations fits well with the post-BD leakage current of the $\text{SiO}_x/\text{HfO}_2/\text{TaN}/\text{TiN}$ gate stack n/pMOSFETs.

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