Design of a low-voltage low-power CMOS phase detector for SONET/SDH standards

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**Design of a Low-Voltage Low-Power
CMOS Phase Detector for SONET/SDH
Standards**

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A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Master of Engineering

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ABSTRACT

Due to the exponential growth in the Internet data traffic, the volume of data over the telecommunications network has increased rapidly. The required capacity of the transport (transmission) links must also increase, motivating work on faster communication channels. Among all the available transmission media, optical fiber achieves highest bandwidth with the lowest loss. Thus, the development of telecommunication transport networks has been accelerated, resulting in the Synchronous Optical Network (SONET)/Synchronous Digital Hierarchy (SDH) standards. The SONET OC-192, a standard for 10-Gb/s serial links, has been well established.

The clock and data recovery (CDR) circuit is the most challenging part of building a optical receiver for the SONET OC-192 standard because of the high-speed operation and the random input data stream. Further, the CDR must comply with stringent jitter requirements specified in the standard. The phase detector, being the first stage dealing with incoming high-speed data, is a crucial building block of a CDR circuit. Its characteristics determine the design styles of other block elements in a CDR circuit as well as the entire performance of CDR system critically.

In this project, a new non-sequential linear high-speed phase detector (PD) for SONET OC-192 standard is proposed. The 0.18 μ m CMOS Analog/RF process of Chartered Semiconductor Manufacturing Ltd (CSM) is used throughout the design. The data rate is set to be 10-Gb/s according to the standard. The proposed

PD has reduced the metastable region by avoiding using of D-flipflop (DFF) or D-latch, which are commonly employed in sequential PDs. Its circuit structure is simpler than the half-rate PD achieving 10-Gb/s operation reported so far. Its linear characteristic is desired in CDR block because under locked condition, the zero charge pump output will not generate significant activity at VCO control line and guarantee small jitter operation of the CDR circuit. In addition, the proposed PD also eliminates the problem of half-period skew in normal linear PDs. The post-layout simulation results show that the proposed PD exhibits linear characteristics for low jitter operation and consumes 34.58mW power which is less than the 10-Gb/s half-rate linear PD implemented in the same process. The proposed PD consumes a silicon area of $136\mu\text{m}\times 142\mu\text{m}$.

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1 Introduction

1.1 Motivation

Due to the exponential growth in the Internet data traffic, the volume of data over the telecommunications network has increased at an annually compounded rate of 100% since 1995 in the US and 1997 in Europe [1]. The required capacity of the transport (transmission) links, which connect the network switching nodes, must also increase, motivating work on faster communication channels. Among all the available transmission media, optical fibers gave the highest bandwidth with the lowest loss, serving as an attractive solution for the Internet backbone. The current state of the art for time division multiplexed (TDM) bit streams for optical communication systems is the 10-Gb/s synchronous optical network (SONET) OC-192 technology and its European counterpart, the synchronous data hierarchy (SDH) STM-64 [2].

The rapidly growing volumes of data in optical communication networks have rekindled interests in high-speed optical and electronic devices and systems [3]. The high bit-rate optical receiver is therefore serving as an interface between the optical and electronics worlds. To design a 10-Gb/s single-chip optical receiver for SONET OC-192 standards is not easy. The high-speed operation is the most challenge task for the design work. Furthermore, the data stream received by the optical receiver is both asynchronous and noisy. For subsequent processing, timing information, e.g. a clock must be extracted from the data so as to allow synchronous operations and the data must be “retimed” such that jitter

accumulated during transmission is removed [4]. The task of clock extraction and data retiming (called clock and data recovery or CDR) is particularly difficult at such high-speed operation to meet the stringent jitter requirements defined by SONET OC-192 standards.

To narrow down the scope of the effort, this research was primarily focused on the design of a high-speed phase detector (PD) for 10-Gb/s clock and data recovery circuits compliant with SONET OC-192 standards. The phase detector, being the first stage dealing with incoming high-speed data, is a crucial building block of a CDR circuit. The main function for the PD is to detect and amplify the phase difference between the input high-speed signal and the output of the voltage-controlled oscillator (VCO) employed in the CDR circuit to recover the clock and data. Unlike the normal PDs in phase locked loops (PLL), where the input signals of a PD is periodical, the input signal of a PD in CDR systems is random data, presenting more difficulties in PD design. Further, the characteristics of PD determine the design styles of other block elements in a CDR circuit as well as the entire performance of the CDR system critically.

The majority of 10-Gb/s CDR systems reported have been implemented in technologies in GaAs and SiGe HBT [5][6] to achieve high-speed operation, however, at the expense of large power consumption. In recent years, the complementary metal-oxide-silicon field-effect transistor (CMOS in short) is becoming popular for its low fabrication costs, high integration, simpler structure than BJT and ease of scaling down in dimensions. The reported CMOS 10-Gb/s CDR systems in [7][8], however, have not nearly explored the variety of possible

CDR architectures and the PD designs.

1.2 Objectives

The primary objective of this project is to analyze, design, and simulate a CMOS low-voltage, low-power phase detector for clock and data recovery circuits based on SONET OC-192 standard. The linear characteristic of the phase detector is to be ensured for low jitter operation of the whole CDR circuit. The targeting operating frequency is at 10GHz to handle the 9.95328-Gb/s random serial data according to the standards. In this project, the critical design parameters include low power, small jitter and high speed.

1.3 Major Contributions of the Thesis

A new 10-Gb/s non-sequential linear phase detector for SONET OC-192 clock and data recovery IC is implemented in this thesis. Traditionally, BJT process is employed for realizing such high-speed digital IC; CMOS design has yet been explored for various architectures.

The report focuses on the design and simulation of the proposed non-sequential linear phase detector in the logical representation (schematic); and the design in physical representation (layout) on Chartered 0.18 μ m CMOS Analog/RF technology. The linear characteristic of the proposed phase detector is desired in CDR block for achieving small jitter operation. By avoiding using of D-latches in the design, the proposed phase detector reduces the susceptibility to metastable region, thus achieves larger operating range than the half-rate linear PD

implemented under the same process. In addition, the proposed phase detector also eliminates the problem of half-period skew in normal linear phase detectors. The MOS current mode logic (MCML) is employed to realize GHz logical gates. The post-layout simulation results show that the proposed PD exhibits linear characteristics for low jitter operation and consumes 34.58mW power which is less than the 10-Gb/s half-rate linear PD implemented in the same process.

1.4 Organization of the Thesis

This thesis is organized into eight chapters. Chapter 1 provides an introduction to the problem faced in the design and an outline of the thesis.

Chapter 2 provides some background on the optical receiver and clock and data recovery architectures.

Chapter 3 takes a look at the overview of the phase detector design for the CDR system. Several types of phase detectors for clock and data recovery systems are studied, and the advantages and disadvantages of each type are presented.

Chapter 4 examines the design of the new non-sequential linear phase detector. Detailed analysis, implementation and simulation results will be presented.

Chapter 5 studies the MOS current mode logic circuits (MCML). Several logical gates and latch are designed in MCML.

Chapter 6 gives a brief description of the Chartered™ 0.18μm CMOS technology, the layout considerations involved as well as the steps in designing the layout of the proposed phase detector.

Chapter 7 compares the proposed phase detector against the half-rate linear phase detector built under same process in terms of simplicity and susceptibility to metastable region.

Chapter 8 concludes the thesis with a summary of results and some recommendations for further research in this area.

2 Background and Literature Review

This chapter serves as an introduction to the subject of clock and data recovery (CDR). Beginning with the introduction of optical receiver and basics of CDR, this chapter then analyzes the incoming data for CDR and discusses various clock and data recovery systems.

2.1 High Bit-Rate Optical Receivers

The goal of an optical communication (OC) system is to carry large volumes of data across long distance [9]. Though the optical fibers are capable of transmitting data over long distance for their unique characteristics of wide bandwidth and low cost, the data gets distorted as it travels through the fiber, mostly because of the fiber dispersion. This distortion leads to the closure of the data eyes and reduced signal amplitude due to the loss throughout the fiber. The restoration of the original data at the receiver side therefore must be performed with acceptable bit-error rate (BER).

A popular SONET OC-192 receiver architecture is shown in Figure 2.1. It uses a photodiode or photo detector to convert the incoming high-speed optical pulse of a single channel into electrical current. The detector is followed by a low-noise high-bandwidth transimpedance amplifier (TIA) that converts the current into voltage with a swing large enough for the proceeding blocks. The pulses then pass through a low-pass filter to remove out-of-band noise, thereby improving the

received signal-to-noise ratio (SNR). Additional amplification is then provided by an automatic gain control amplifier (AGC), compensating for variations in the received signal power. The clock required to retune the incoming synchronous data stream is recovered from the received data stream by the clock and data recovery block. A time-division demultiplexer (DEMUX) is then employed in order to separate the 10-Gb/s stream into multiple, lower speed channels. Typical DEMUX ratios are 1:4, 1:8 and 1:16. The lower speed channels are then be further processed by VLSI CMOS circuitry designed to comply with the SONET standards [10].

Figure 2.1: Block level architecture of 10-Gb/s SONET receiver [3]

2.1 Clock and Data Recovery Systems

The core of the receiver is the clock and data recovery (CDR) system. A CDR system extracts timing information from the incoming data and then uses it to retune the received bit stream. Clock recovery, also known as timing recovery, is the process by which a clock at the symbol rate (or multiple of the symbol rate) is recovered from the received data. Data recovery then occurs when the recovered

clock is used to convert the incoming continuous-time signal into a discrete-time stream of received data symbol [11]. Early implementation for OC192 CDR used a narrowband passive filter combined with a nonlinearity to implement the CDR function. Though these systems work well, the narrowband passive filters are expensive and difficult to implement monolithically. For monolithic implementations, a phase-locked loop (PLL) based CDR solution is preferred [6].

As suggested by Razavi [3], the clock recovered by the PLL based CDR must satisfy three important conditions: (1) It must have a frequency equal to the data rate, i.e. 10GHz for 10-Gb/s data rate. (2) It must bear certain phase relationship with respect to the data, allowing optimum sampling of the bits by clock. As indicated by Figure 2.2, if the rising edges of the clock coincide with the midpoint of each bit, then the sampling occurs farthest from the preceding and following data transitions, providing maximum margin for jitter and other timing uncertainties. (3) It must exhibit a small jitter as it is the principal contributor to the retimed data jitter.

Figure 2.2: Optimal sampling

2.1.1 CDR architecture

Figure 2.3 shows a dual-loop receiver CDR architecture that is originated from [12]. It basically consists of a low noise Voltage Controlled Oscillator (VCO), a linear phase detector (PD), a phase-frequency detector (PFD), a lock detector, a 1:16 De-multiplexer (DeMUX), a loop filter (external), a selector, a charge pump, and a frequency divider, which form a dual-loop architecture, i.e. a frequency-locked loop and a phase-locked loop (PLL). The frequency acquisition aid is required because the center frequency of the voltage-controlled oscillator (VCO) in the CDR architecture may vary by a large amount with process and temperature – as much as a factor of two ring CMOS oscillator [9] and the pull-in range of the PLL is very small. The frequency acquisition is done by initially training the VCO to a stable reference clock with a frequency close to $1/N$ of the data rate. Keeping the VCO close to the desired operating frequency will also prevent false locking. When the divided VCO clock frequency and the reference clock agree to within $\pm 0.1\%$, the lock detector automatically switches the circuit to the recovery loop where the phase detector (PD) takes over from the phase-frequency detector (PFD). In this mode, the lock-in time is very short because the VCO frequency is already close to the incoming data rate [12]. In the phase-locked loop, the phase difference between the incoming data and clock signals is captured by the PD and its output is then converted into a control voltage to the VCO by the charge pump and loop filter. The data is retimed by the recovered clock signal through the master-slave D flip-flop (DFF) retimer before being de-multiplexed by later stage.

Figure 2.3: Dual-loop CDR architecture

2.1.2 CDR System Specifications

In the optical communications, the time-domain behavior of phase noise is of great interests because it represents the extent to which the zero crossings of a waveform are corrupted. The deviation of the zero crossings from their ideal position in time or the deviation of each period from their ideal value T_0 (Figure 2.4) is called jitter [3]. Several other definitions of jitter can be found in [13].

Figure 2.4: Jitter definition

The SONET jitter specifications place stringent constraints on the jitter characteristics of the CDR. There are three main ways in which the CDR's jitter properties are specified: jitter generation, jitter tolerance and jitter transfer.

Jitter generation is the process whereby jitter appears at the output port of an individual piece of digital equipment in the absence of an applied jitter at the input [14]. The Bellcore recommended the jitter generation to be less than 0.1 unit intervals (UI) peak to peak, where the a unit interval is the bit period [2]. For OC-192 with a bit period of 100ps, 0.1 UI translates to a maximum peak to peak generated jitter of 10ps.

Jitter transfer function is the ratio between the output jitter and input sinusoidal jitter at various input jitter frequencies. A jitter peaking and a bandwidth component [14] describe the function as shown in Figure 2.5. For SONET OC-192, the jitter bandwidth is specified to be less than 120KHz and the jitter peaking is set to be less than 0.1dB [5]

Figure 2.5: OC-192 Jitter transfer specification

The key performance characteristic of a clock/data recovery circuit is its input jitter tolerance [15]. The input jitter tolerance is the maximum amount of phase jittering on an input data stream tolerable by the circuit that it still recovers the clock and data from the input. The SONET OC-192 CDR jitter tolerance specification is defined by the mask shown in Figure 2.6.

Figure 2.6: OC-192 jitter tolerance specification

2.1.3 Incoming Data Format

Most fibre based optical transmission systems use on/off keying and direct-detection. In on/off keying, the intensity (power/unit area) of the light source is modulated by a binary data signal. The receiver converts the incident optical power into an electrical current (direct detection)/ optical power is a scalar and therefore, the received signal is always greater than zero. In on/off keying (a simple pulse amplitude modulation, PAM scheme) a “zero” is represented by near zero intensity and a “one” is represented by a positive intensity. More complicated multi-level

PAM schemes are generally not used since the optical fibre bandwidth is so large that the system's maximum bit rate is imposed by the receiver (Rx) and transmitter (Tx) electronics. The power control of the light source and the control of the Rx decision thresholds are also greatly complicated in multi-level modulation schemes. Since the fibre bandwidth does not limit the system performance, there is little motivation to make the power, transmission distance, receiver complexity vs. occupied bandwidth trade-off that is made by moving to a multi-level PAM scheme [16].

Non-return-to-zero (NRZ) data is most often employed in high-speed optical communication applications to maximize the data rate within a given channel bandwidth. The name NRZ serves to differentiate it from return-to-zero (RZ) data, which is a related, but more bandwidth intensive scheme. Figure 2.7 shows an example of each data format. For NRZ data, each bit has duration of T_b (called "bit period") which corresponds to a bit rate, $r_b = 1/T_b$, whereas in RZ data format, the signal goes to zero between consecutive bits and it is possible NRZ data sequence with a bit period of $1/2T_b$. As a consequence, RZ data requires twice the bandwidth of NRZ data to transmit the same bit sequence. Therefore RZ data is not commonly used in optical communication systems.

Figure 2.7: NRZ and RZ bit streams with identical bit patterns

NRZ data has two properties that make the task of clock recovery particular difficult. Firstly, the random nature of the data allows arbitrarily long sequence of “ZERO”s or “ONE”s. This property requires the CDR to “remember” the bit rate during such a period, i.e. in the absence of data transitions, the CDR should not only continue to produce clock, but also incur negligible drift in the clock frequency [17]. The second property of NRZ data is that it contains no spectral content at the bit rate (the required clocking frequency). This can be shown from the shape of the NRZ data spectrum. Since the autocorrelation function of a random binary sequence is [18]:

$$\begin{aligned}
 R_x(\tau) &= 1 - \frac{|\tau|}{T_b} \\
 &= 0 \\
 &(|\tau| < T_b)
 \end{aligned}
 \tag{Equation 2.1}$$

the power spectral density equals

$$P_x(\omega) = T_b \left[\frac{\sin(\omega T_b / 2)}{\omega T_b / 2} \right]^2
 \tag{Equation 2.2}$$

Plotted in Figure 2.8, this function vanishes at $\omega = 2m\pi / T_b$. In contrast, RZ has finite power at such frequencies. Due to the lack of spectral component at bit rate of NRZ data, the CDR may lock to spurious signals or simply not lock at all. Thus, a nonlinear operation at the front-end of the circuit needs to occur to create spectral information at the bit rate.

Figure 2.8: Spectrum of NRZ data

2.1.4 Design Challenges

The primary design challenge for CDR IC design is the jitter requirements defined by the standards. There are five sources of jitter can be identified with their origins in the phase-locked loop. (1) Jitter generated from the data traveling on

long lines for large distances. (2) Ripple on the control line of VCO directly translates into jitter through the VCO in an open loop manner. (3) Disturbance of the VCO by the leakage of data transitions through the phase detector is major cause of data-dependent jitter. (4) Oscillation jitter due to the thermal noise of the devices in the VCO. Although this jitter is filtered by the loop dynamics of PLL, for PLL's with small loop bandwidths, a majority of noise remains unfiltered. (5) Noise from the power supply line and substrate is contributing to the jitter. The effect of input jitter can be reduced by a narrow loop bandwidth and the VCO jitter is lowered through the use of large swing and careful design. The fully differential design must be employed to minimize the supply and substrate noise. The phase detector is to be carefully designed such that no significant activity on the VCO control line is generated for minimizing source of jitter in (2) and (3).

As stated in section 2.2.3, NRZ data has two attributes that make the task of clock recovery, especially phase detection, difficult. Thus, the process of phase detection is complicated and requires considerable preprocessing. When there is absence of data transition, i.e. long sequence of "ONE"s or "ZERO"s in the input NRZ data stream, the phase detector must not produce any false phase comparisons. Further, since there is no spectral component at bit rate, the phase detector must incorporate some nonlinear operation to generate spectral information at the clock frequency. Therefore, as elaborated in [3], PDs for random data must provide two essential functions: data transition detection and phase difference detection to cater for the two attributes of NRZ data format.

The current state of art for optical communication is the SONET OC-192 standard which is targeting the bit rate at 9.95328-Gb/s [2]. For such high-speed CDR system, the requirements of tolerance to long run sequence of input data, stringent jitter and bandwidth will be particular difficult to accomplish. In the design of phase detector, the small amount of phase error at such high operating rate would be so crucial that it may cause wrong phase difference to be detected and make the CDR malfunctioning, though this amount of phase error might be negligible at lower operating speed. Further more, in CMOS realization of PLL-based CDR system, difficulties such as slow and noisy devices are to be conquered.

The design of VCO directly impacts on the jitter performance of the CDR system. The phase noise in VCO is the electrical noise produced by the devices of the circuits. If the phase noise performance is poor in VCO, the additional jitter is resulted at the output of clock signal of VCO. Consequently, jittered clock signal injected into the phase detector and the performance of PD will degrade due to its inability to fully turn on the switching transistors in the CML circuits.

2.2 CDR Categories

As mentioned above, in monolithic implementation of CDR systems, the PLL-based CDR solution is preferred. There are two major groups of CDR architectures in the literature, namely, linear CDR and binary CDR. In this section, their differences and characteristics will be briefly introduced.

2.2.1 Linear CDR Systems

The linear CDR system is based on the linear phase detector, which has an rms output voltage that is linearly related to the phase error between the clock and data. Figure 2.9 shows a simplified block diagram of a linear CDR architecture (frequency acquisition loop is eliminated since the PLL structure is focused in the thesis).

Figure 2.9: Linear CDR system

The linear PD produces two output pulses, Dif and Ref signals, whose difference is linear proportional to the phase difference between input data and clock signal. Charge pump is acting as an integrator and loop filter filters unwanted signals and provides the control voltage for VCO. The output clock signal from VCO is running at full rate, i.e. at 10-Gb/s for OC-192 applications.

One obvious advantage of linear CDR system is that it can be designed using linear control theory. Detailed theoretical analysis of jitter transfer, jitter tolerance and jitter generation based on linear PLL theory can be found in [5]. Since the output pulse width of linear PD is linearly proportional to the phase difference, the constant loop gain is resulted during lock transient and minimal charge pump activity is achieved. Therefore, output jitter is also minimized.

2.2.2 Binary CDR Systems

In contrast to the linear CDR systems, the binary phase detector based CDR is categorized into binary CDR systems. As the name implied, the binary PD may have as few as two output states, i.e. either the clock edge is early (before the optimal sampling point) or it is late (after the optimal sampling point). Figure 2.10 shows the basic binary CDR architecture.

The binary CDR is less demanding on the “analog” features of IC technology. The most critical element in the binary CDR is the phase detector, where sub-picosecond time resolution is required [6]. Binary PD produces two digital outputs, UP and DN, to signal if the data is early or late with respect to the VCO clock. Normally, the binary information is spilt into two loops [19]. One loop is the phase-control loop formed with the UP and DN directly modulating the VCO frequency with frequency step $\pm\Delta F_{bb}$ (bb denotes “bang-bang”, other name of the binary PLL architecture) via bang-bang frequency tune input. The other loop is the frequency loop in which the UP and DN outputs are integrated with charge pump and loop filter to control the second tune input of VCO.

Figure 2.10: Binary CDR system

As compared with the architecture of linear CDR, the binary CDR architecture is more complicated, especially in the VCO design since the VCO requires two sets of tune inputs. In the binary CDR system, the linear theory is not applicable any more, therefore the jitter is exhibiting highly nonlinear characteristic. The most undesired feature of the binary CDR is that the binary PD creates significant ripple on the VCO control line and hence great jitter at VCO output is resulted [9].

2.3 Summary

In this chapter, a brief overview of the architectures and specifications of high-bit rate optical receivers was presented. The core block of optical receiver – CDR system was especially highlighted with the discussion in its incoming data format and specifications. Finally, two distinct CDR architectures were reviewed.

In practice, a lot of attentions will be paid to PD and VCO design in a CDR

Background and Literature Review

system because these two block elements are most susceptible to the jitter in the system. In this thesis, we will be focusing on the discussion of PD design. The design of high-speed PD for CDR systems will be elaborated in the following chapters.

3 Overview of PD Design

The phase detector (PD) is employed in the CDR systems to detect and amplify the phase difference between the input data and the clock output from VCO. Since the input data stream is in the format of random NRZ data, the PD therefore must provide two essential functions: data transition detection and phase difference detection [4].

Recently a significant effort has been made on designing high-speed low-power CMOS phase detectors for CDR systems because the performance of CDR is critically dependent on the characteristic of PD. Traditionally, there are two main categories of PDs that are dealing with random data input: linear PD and binary PD. However, with the rapid increasing of data rate in communication systems, these two types of PDs may not be able to work fine at so high data rate at full clock rate even with scaled technology. In recent years, new PDs employing half-rate or $1/8$ rate technique have emerged.

3.1 Linear Phase Detector

A typical example of a linear phase detector is the Hogge phase detector reported in [20]. Figure 3.1 shows the simplified block diagram of a Hogge PD and its output waveforms.

Figure 3.1: Hogge phase detector

DFF1 samples the incoming data by the VCO output *CLK*, producing waveform *B* which is a delayed replica of the input data. Further, the delayed time is just the phase difference between input data and *CLK* signal. Therefore, the pulse width of output $Dif = Data \oplus CLK$ varies linearly with input phase difference and the pulse appears for each data transition, suggesting that the circuit can operate as a linear PD. This type of output is called proportional pulses, which provide phase difference detection. The other output pulse *Ref* is required to eliminate the data pattern dependency. The reason is that the average value of the

Dif pulses is a function of data transition density, failing to uniquely represent the phase difference for various data patterns [4]. For instance, the average value of *Dif* output will remain unchanged if the transition density falls by a factor of two and the phase difference rises by the same factor (Figure 3.2). In other words, two different phase differences may result in the same dc output, leading to false lock. To overcome this ambiguity, the *Ref* pulses are introduced. It is called the reference pulses since it appears on every data transition edge and exhibits a constant pulse width. The *Ref* pulses are produced as follows: the output from DFF1 (signal *B*) is delayed by half clock period through sampling by VCO output $\overline{CLK}$ in DFF2; the delayed signal *A* is therefore XORed with signal *B*; pulses of half clock period is produced for each data transition (*Ref* output).

Under locked condition, the rising edge of *CLK* signal is sampling the midpoint of each bit for optimal sampling of the data stream as mentioned in chapter two, thus *Dif* and *Ref* produce equal pulse widths (Figure 3.3). As a result, the Hogge PD does not generate significant activity on the VCO control line and hence smaller output jitter [21] in the locked condition.

Figure 3.2: Data pattern dependency (a) original waveforms (b) data transition falls by half and phase difference rises by two

While exhibiting a linear characteristic, the Hogge PD entails a number of issues. First, the finite delay through DFF1 introduces a phase offset in the locked condition [20], degrading the clock phase margin. Second, as shown in Figure 3.4, the retiming delay through DFF2 leads to a half-period skew between *Dif* and *Ref* pulses. Consequently, even in locked condition, a charge pump (CP) and a loop filter driven by *Dif* and *Ref* produce a positive ramp while *Dif* is high and a negative ramp while *Ref* is high. The control line of the VCO therefore experiences a “triwave” with a positive net area [22].

Figure 3.3: Waveforms of Hogge PD in phase-locked condition

Figure 3.4: Problem of half-period skew on Hogge PD

3.2 Binary Phase Detector

A typical example of binary phase detector is the Alexander configuration [23] shown in Figure 3.5. It is also known as early-late phase detector.

Figure 3.5: Alexander phase detector

The Alexandra PD employs four flipflops to realize a three-point sampling scheme and two XOR gates to compare the samples. As illustrated in Figure 3.5, DFF1 and DFF2 sample the data inputs on two consecutive rising edges of CLK ,

producing B and A , respectively. DFF3 samples $Data$ input on the falling edge of CLK , and DFF4 delays this sample by half clock period, generating C . As a consequence, if CLK leads $Data$, then $A \neq C = B$, generating a low UP and a high DN . Conversely, if CLK lags $Data$, then $A = C \neq B$, forcing a high level at UP and a low level at DN [9].

The Alexander PD is a bang-bang system, exhibiting a very high gain in the vicinity of $\Delta\phi = 0$ [4]. The drawback of the Alexander PD is that it creates significant ripple on the VCO control line and hence produces great jitter at VCO output [24].

3.3 Half-rate Linear Phase Detector

If the data rate is higher than the maximum tolerable speed of phase detectors and VCOs, a half-rate CDR architecture can be used [25][26]. The idea is to run the VCO at a frequency equal to half of the data rate, thereby relaxing the design of the circuits in the signal path. Half-rate architectures usually demultiplex the data as well [9]. A half-rate linear phase detector was reported in [7] with 10-Gb/s data rate. The simplified half-rate linear phase detector is shown in Figure 3.6.

Figure 3.6: Half-rate linear phase detector

The half-rate linear PD consists of four latches and two XOR gates. The data is applied to the inputs of two sets of cascaded latches (L1-L4), each cascade constituting a flipflop that retimes the *Data*. The *CLK* input is running at half rate. Assuming *Data* leads *CLK* by ΔT and latches L1 and L2 sample *Data* on rising and falling edges of *CLK*, L1 produces a pulse (signal A) width equal to $T_{CLK}/2 + \Delta T$ and L2 generates a pulse (signal B) width equal to $T_{CLK}/2 - \Delta T$. Therefore, $A \oplus B$ produces a pulse of width ΔT for each data, indicating that output $Dif = A \oplus B$ is actually the proportional pulse and the PD can indeed operate as a linear PD. In order to provide the reference pulse to complete the task of phase detection for random data, the other two latches L3 and L4 are required to produce pulse *C* and pulse *D*. The two waveforms are identical except for a phase difference equal to half of the clock period. Thus, $C \oplus D$ produces a constant-width pulse on every data transition, serving as a reference.

While the two XOR operations provide both the proportional and reference pulses for every data transition, the pulses in proportional pulse are only half as wide as those in reference pulse. This is because if the clock edge is strobe in the middle of data eye, i.e. at optimal detection, the proportional pulses are $T_{CLK}/4$ s wide, whereas the reference pulses are $T_{CLK}/2$ s wide. In [7], the amplitude of proportional pulse is scaled up by a factor of two by doubling the corresponding current source in charge pump.

The advantages of the half-rate linear PD are that it allows the circuit to work at high speed and still maintain reliable operation, as well as removal of the dead zone from its characteristics. However, its main drawback is its complexity.

3.4 Half-rate Binary Phase Detector

A binary phase detector employing half-rate technique was also reported recently in [8]. A simplified block diagram of half-rate binary PD and its operating principle is shown in Figure 3.7.

The half-rate binary PD employs three double-edge-triggered flipflops (DETFFs). A DETFF is formed by two latches operating on opposite clock phases along with a multiplexer [8]. Shown in Figure 3.7(a), *Data* input is sampled by *CLK* through a single DETFF. Three types of samples can be identified: those in the immediate vicinity of positive data edges, S_+ ; those in the immediate vicinity of negative data edges, S_- ; and those near no data edges S_0 (Figure 3.7(b)). In Figure 3.7(c), the S_0 samples are discarded and S_+ and S_- samples are examined for early *CLK* and late *CLK* respectively. In order to uniquely determine whether *CLK* is early or late, S_- samples are negated in DETFF3*. Shown in Figure 2.5 (d), *Data* input is retimed by DETFF1 by quadrature phase of *CLK*, thereby a delayed edge of *Data* $Data_Q$ is generated. By doing so, a positive transition on $Data_Q$ means a S_+ sample has already been taken; and a negative transition on $Data_Q$ means a S_- sample has already been taken. From Figure 3.7(a), it can be observed that signal $Q_k (k = 0, \dots, 7)$ contains the S_+ and S_- samples and V_Q signal serves as the retimed replica of *Data*. DETFF3* samples V_I by V_Q , negating S_- on the falling edges of V_Q . As a result, the half-rate binary PD output V_{PD} is positive if the clock is late and negative if it is early.

Figure 3.7: (a) A half-rate binary PD. (b) A DETFF sampling the *Data* by *CLK*. (c) s_0 samples discarded for late and early *CLK*. (d) Detecting the absence of data transition.

The advantage of half-rate binary PD is that it can operate at higher data rate. However, this type of PD is even more complex than half-rate linear PD. Besides, like Alexandra PD, it creates significant ripple on VCO control line and generate potentially great jitter at the VCO output.

3.5 1/8-rate Linear Phase Detector

Since the VCO is the bottleneck to achieve high-speed operation in CDR systems and the reliable operation may not be guaranteed under the process, voltage and temperature variation even with half-rate architectures, Song has suggested the 1/8-rate clock technique for CDR design [27]. In his design, a 1/8-rate linear phase detector is also introduced. It accomplishes the phase error detection with no systematic phase offset.

Figure 3.8: 1/8-rate linear PD

Figure 3.8 depicts the block diagram of the 1/8-rate linear PD. It consists of eight data sampling DFFs, a data and clock transition (DCT) detector and a DCT generator. The DFFs sample the incoming NRZ data stream in each bit at every rising and falling edge of the four half-quadrature clocks. Then, the four DCT signals ($DCT_0 - DCT_3$) are generated in DCT detector; with the incoming four DCT signals, the DCT generator produces the DT and CT signals to determine the phase error between the data and the clock.

Figure 3.9 illustrates the operation of 1/8-rate linear PD. All *DCT* signals go high whenever there is data transition. The falling edges of DCT_0 , DCT_1 , DCT_2 and DCT_3 signals are triggered by rising and falling edges of CLK_3 , CLK_0 , CLK_1 and CLK_2 respectively. Consequently, the *DCT* signals can be described as:

$$DCT_0 = \overline{CLK_3}(Q_1 \oplus Q_3) + CLK_3(Q_0 \oplus Q_2) \quad (\text{Equation 3.1})$$

$$DCT_1 = \overline{CLK_0}(Q_3 \oplus Q_5) + CLK_0(Q_2 \oplus Q_4) \quad (\text{Equation 3.2})$$

$$DCT_2 = \overline{CLK_1}(Q_5 \oplus Q_7) + CLK_1(Q_4 \oplus Q_6) \quad (\text{Equation 3.3})$$

$$DCT_3 = \overline{CLK_2}(Q_7 \oplus Q_1) + CLK_2(Q_6 \oplus Q_0) \quad (\text{Equation 3.4})$$

where Q_k ($k = 0, \dots, 7$) is the output of a data sampling DFF in Figure 3.8. The *DT* and *CT* are generated by toggling four *DCT* signals at every consecutive rising and falling edge. Therefore, *DT* and *CT* appear at every data transition; the pulse width of *CT* output is linearly proportional to the phase error; and *DT* remains unchanged with varying phase error.

Figure 3.9: Operation of 1/8-rate linear PD [27]

The major advantage of the 1/8-rate linear PD is that it has the systematic path in generation both DT and CT outputs. Thus, no systematic phase offset occurs between the clock and data. However, its high-speed operation has yet been approved for 10-Gb/s CDR circuits. Moreover, the extreme complexity is also a drawback.

3.6 Non-sequential Phase Detector

As at high frequencies, the DFF used in Hogge PD has the problem of settling fast enough when sampling the random data. A new non-sequential phase detector for high-speed CDR circuits was also reported in [28] to avoid using of DFFs. It was designed to operate at higher data rates than what is achievable with

Hogge PD. The circuit structure and signal waveforms are shown in Figure 3.10.

The non-sequential PD only consists of XOR gates, AND gates and delay cells. The two delay cells and two XOR gates are used to detect the edges of random data. The *UP* and *DN* outputs are required to drive the charge pump. Signal *A* is generated from *CLK_lead* and $\overline{CLK_{lag}}$ signals. It has fixed relationship with the generated *CLK*, i.e. the rising edges of *CLK* are at the middle of signal *A*. Signals *E* and *F* are generated from the signals *Data*, *Data_delay1* and *Data_delay2*. The falling edges of *F* and the rising edges of *E* are aligned at the dotted lines, which, when the PLL is in lock, is right at the middle of the signal *A*. When PLL is in lock, *UP* and *DN* outputs are generated by using *E* and *F* to cut signal *A* in half. Therefore, *UP* and *DN* outputs have the same pulse widths, leaving VCO control line voltage unchanged when in lock.

This non-sequential PD has the advantage of simplicity and operability at high-speed [28]. However, it does not present acquisition behavior as good as linear PDs do, and it presents large charge pump charging activities [29].

Figure 3.10: Non-sequential PD reported in [28]

3.7 Summary

A detailed literature review on phase detectors for random data is presented in this chapter. Several types of PDs were described, each with its own advantages and disadvantages. For SONET OC-192 applications, it is important to have low

jitter and high-speed PD. According to the above discussion, the linear PD provides the low jitter operation. However, normal linear PD, like Hogge PD cannot achieve such high speed for SONET application. The non-sequential PD can achieve higher data rate, but failed to suppress jitter adequately. The CDR design employing half-rate or 1/8-rate technique is advantageous in achieving high-speed operation, however increasing the design complexity. Therefore, it leads to research on new linear high-speed phase detector design for SONET OC-192 CDR circuits.

4 New Non-sequential Linear Phase Detector Design

In this chapter, the design of a new linear non-sequential phase detector for CDR circuits is presented. Since the performance of DFF deteriorates rapidly at modestly high frequencies, the proposed PD avoids using of DFF to achieve higher operating speed. As described in chapter 3, the half-rate and 1/8-rate technique normally employ complex PD architecture. The proposed PD has much simpler structure with full-rate design.

4.1 Non-sequential Linear Phase Detector Design

To design a linear PD for CDR systems, it must provide two essential functions as mentioned in chapter 3: edge detection and phase detection. We follow the two functions to present the proposed PD design.

Since the incoming data stream is NRZ random data, the edge detection is a must. The simplest way of digital edge detector is illustrated in Figure 4.1. The data sequence and its delayed version are XORed, thereby producing a positive pulse of width ΔT on each data edge. Therefore, the positive pulse at the output of digital edge detector can be viewed as the reference pulse. However, unlike the Hogge PD where the reference pulses are produced after the proportional pulse (Figure 3.1), the digital edge detector output is generated immediately after every data transition.

Figure 4.1: Digital edge detector

For the phase detection, it can be observed the phase difference between the reference pulses and CLK signals just represents the phase error between the input data stream and the CLK (Figure 4.2). In order to capture this amount of phase difference and produce the proportional pulses on every data transition edge, the $\overline{CLK}$ signals are ANDed with the reference pulses, producing the proportional pulses V_p .

Figure 4.2: Generation of proportional pulses

New Non-sequential Linear Phase Detector Design

Based on the above analysis, the new non-sequential linear PD can be designed as depicted in Figure 4.3.

Figure 4.3: Proposed non-sequential linear PD

The proposed non-sequential linear phase detector simply consists of three logical gates and one half-cycle delay cell. The operating principle is illustrated in Fig. 4.3. The delay time in the half-cycle delay cell is set to half of input data bit period. Hence, the output signal *Ref* pulse will have constant pulse width of half data bit period. The data transition edges of the random NRZ data is detected by

the half-cycle delay cell and XOR1 gate. The XOR2 gate is inserted to compensate the delay in the XOR1 gate to minimize systematic offset. The $\overline{CLK}$ signal from VCO of CDR loop is XORed with 0 (GND) in XOR2 gate. Therefore, the output of XOR2 gate is just a delayed version of $\overline{CLK}$. The Ref output and the $\overline{CLK_delay}$ are connected to the two input lines of the AND gate. Hence, the output Dif of the AND gate will only be high when both Ref and $\overline{CLK}$ are high. Consequently, the pulse width of Dif pulse is linearly proportional to the phase difference between $Data$ and CLK , completing the phase difference detection. With both Dif and Ref output signals generated at every data transition edge, the proposed simple phase detector is able to detect the phase difference between the random NRZ data and clock signal and eliminate the data pattern dependency.

In locking state, i.e. when the rising edge of CLK signal aligns with the rising edge of the $Data$ signal, each data transition creates equal width of Dif and Ref , yielding an average zero value for $(Dif-Ref)$. Henceforth, the charge pump output will also be zero. This property of the proposed phase detector is desirable for low jitter operation of the CDR system because the zero charge pump output will not generate significant activity on the VCO control line [21].

4.2 Problem of Half-period Skew

In addition to the desired linear characteristic, the proposed phase detector will also eliminate the problem of half-period skew [9] in normal Hogge phase detector. As explained in section 3.1, the half-period skew problem is due to the retiming delay through the second DFF in Hogge PD, leading to a “triwave” with a

positive net area at the output of charge pump and a loop filter at locking condition. Some modifications proposed in [30] has achieved “triwave” with zero net area in locked condition and alleviated this half-period skew problem. However, the problem is not eliminated and the design has become more complicated with the modifications. In the case of the proposed non-sequential linear PD, there is no retiming delay between *Dif* pulse and *Ref* pulse because they are generated at the same time. The charge pump outputs of for the Hogge PD and the proposed non-sequential PD at locking condition are shown in Figure 4.4 (a) and Figure 4.4 (b) respectively. In the case of Hogge PD, even at lock state, the VCO control line will experience a “triwave” with positive net area, disturbing the VCO on every data transition. For the proposed non-sequential PD, on the contrary, the charge pump output will remain unchanged in lock state, leaving the VCO undisturbed. As a result, the half-period skew problem is avoided in proposed non-sequential PD by generating two output pulses *Dif* and *Ref* at the same time.

Figure 4.4: Problem of half-period skew: (a) Hogge PD and (b) Proposed non-sequential PD

4.3 Simulation Results and Discussion

The proposed non-sequential linear PD was implemented in a 0.18 μm standard CMOS process obtained from Chartered Semiconductor Manufacturing Ltd. The transistors were sized to ensure proper linearity and to achieve a desired voltage swing for high-speed operation.

New Non-sequential Linear Phase Detector Design

It is instructive to plot the input/output characteristic of the proposed phase detector to ensure linearity [7]. This is accomplished by obtaining the average values of PD outputs *Dif* and *Ref* pulses while the phase detector is operating at maximum speed, i.e. at 10GHz. Figure 4.5 shows the simulated behavior as the phase difference between input data and CLK varying from 0° to 360°.

Figure 4.5: Input/output characteristic curve of proposed PD

The *Ref* output exhibits very good linearity in two ranges, i.e. from 5ps to 45ps and from 55ps to 95ps roughly. It achieves the highest average value at 50ps. At this point, the whole CDR system will be in lock condition where rising edges of the *CLK* from VCO coincide with midpoint of each bit, i.e. optimum sampling point. Shown in Figure 4.5, the *Dif* and *Ref* output have approximately the same average value when in lock condition, which is highly desired. The linear characteristic of the proposed phase detector results in minimal charge pump activity and small ripple on the control line in the locking condition. Due to the different circuit structures and different current sources in the MCML XOR and AND gates, there is small amount of discrepancy between *Dif* and *Ref* at 50ps point of lock condition. The dead zone is minimized because both *Dif* and *Ref* pulses are generated in every cycle [31].

The power supply was chosen to be 2.5V to ensure enough voltage gain of proposed phase detector when handling 10-Gb/s data and small jitter generation [7]. Simulations were also carried out at different power supply conditions, i.e. at 1.8V and 2.0V. The results are shown in Figure 4.6 (a) and (b) respectively. It is shown that average values of *Dif* and *Ref* pulses will no longer be equal at optimum sampling point with lower power supply, instead, they two will have the same average values just before and after the optimum sampling point. Therefore, small ripples will be generated on control line in locking condition and jitter will be generated at the output of the CDR system, which is highly undesired. The voltage gain is also reduced at lower power supply level, which can be observed from Figure 4.6.

New Non-sequential Linear Phase Detector Design

(a)

(b)

Figure 4.6: Input/output characteristic curve of proposed PD for (a) $V_{dd}=1.8V$ and (b) $V_{dd}=2.0V$.

In the proposed PD, all the blocks are built with MCML circuits biased at high current density to improve the speed. When the switching transistors are scaled down, the current driving ability will also be scaled since the DC bias current is proportional to the aspect ratio of the transistor, considering only the 1st order effect. Therefore, the switching transistor pair in MCML cannot be fully turned on/off, reducing the voltage gain of the proposed PD.

4.4 Summary

A new linear non-sequential phase detector operating at 10GHz for Clock and Data Recovery Circuits is proposed in this chapter. It simply consists of two delay cells, a XOR gate and an AND gate. It can achieve higher data rates than what is achievable with the Hogge PD [20]. Compared with the half-rate PD achieving 10-Gb/s data rate reported in [7][8], the proposed circuit has a much simpler structure. It is capable of detecting random data by providing proportional pulse and reference pulse outputs. It also has the advantage of eliminating half-period skew problem against Hogge PD. The simulation results show that the proposed PD exhibits linear characteristics for small jitter operation of CDR circuits and the power consumption is much smaller than other PDs reported in the literature.

5 MCML Circuits Design

The detailed circuit implementations of the proposed non-sequential linear PD will be discussed in this chapter. Since the application of the new proposed phase detector is for the Clock and Data Recovery Circuit running at 10-Gb/s data rate, it is crucial to design the building blocks in the new phase detector for such high-speed application.

5.1 MOS Current Mode Logic

The MOS Current Mode Logic (MCML) is adopted for building the high-speed digital logic gates because MCML is capable of faster operation than the conventional CMOS logic and it would be suitable for use in 10-Gb/s systems [32]. Figures 5.1 (a) and (b) show the inverter circuits for CMOS logic and MCML respectively. The CMOS logic has the advantage of low static power consumption, but its operation is relatively slow [33]. For example, the maximum toggle frequency of a conventional 0.18 μm CMOS inverter is only about 3.5GHz. Obviously, it is not applicable for 10-Gb/s CDR systems.

Figure 5.1: Inverter circuits of (a) CMOS logic and (b) MCML

In [32], SPICE simulation of MCML and CMOS logic inverters were performed using 0.18 μm CMOS transistors with a 1.8-V supply voltage. The simulated delay time at different fan-out conditions and power consumption for different operating frequencies are shown in Figure 5.2.

Figure 5.2: Comparison of CMOS logic and MCML. (a) Delay time as a function of fan-out (b) Power consumption as a function of frequency [32]

The CMOS logic inverter is shown to have longer delay time than the MCML inverter for different fan out conditions, which shows that the MCML is faster than CMOS logic. From [34], the propagation delay of CMOS logic is

approximated by:

$$T_{p(CMOS)} \propto \frac{C \times V_{dd}}{\frac{k}{2} \times (V_{dd} - V_{th})^\alpha} \quad (\text{Equation 5.1})$$

where k and α are the process and transistor size dependent parameters, C is the load capacitance on output node, whereas the MCML logic propagation delay is found to be [35]:

$$T_{p(MCML)} \propto \frac{C \times \Delta V}{I_0} \quad (\text{Equation 5.2})$$

where ΔV is the voltage swing and I_0 is the current in the current source transistor MN0 as shown in Figure 5.1. From Equation 5.1 and Equation 5.2, it is observed that $T_{p(CMOS)}$ is proportional to V_{dd} , on the contrary, $T_{p(MCML)}$ is proportional to ΔV . Since smaller input voltage swings are normally adopted for MCML, MCML will have shorter delay compared to CMOS logic.

As shown in Figure 5.2(b), the CMOS logic inverter has lower power consumption than the MCML inverter when the operating frequency is smaller than 2GHz approximately. The CMOS logic inverter will consume much larger power when frequency goes up, while the MCML inverter consumes a constant power. At 10GHz, the MCML inverter only consumes approximately half of the power of the CMOS logic inverter. This can also be proved in the equation-based analysis. For the CMOS logic circuit, its power consumption is mainly determined

by the dynamic power, which is given by the formula [36]:

$$P_{(CMOS)} = C_L V_{dd}^2 f \quad (\text{Equation 5.3})$$

where C_L is the total load capacitance and f is the operating frequency. The power consumption in MCML circuits is constrained by the equation:

$$P_{(MCML)} = V_{dd} I_0 \quad (\text{Equation 5.4})$$

As a result, the power consumption of MCML circuits is of constant value regardless of variation of operating frequency, whereas the power consumption of CMOS logic circuits increases with operating frequency. In gigahertz frequency range, the power consumption of the CMOS logic become larger than that of the MCML [32], as shown in Figure 5.2(b), which shows that MCML is suitable for low-power operation in gigahertz frequency range.

MCML circuits also have the noise advantages over CMOS logic circuits. Firstly, the MCML employs the differential input/output signals, which in turn provides the immunity to common-mode noise. Secondly, shown in Figure 5.1, transistor MN0 behaves as a current source and provides a constant current to the switching NMOS transistors. Hence, with this constant current source, the amount of spiking of supply and substrate voltages are reduced, therefore reducing the supply and substrate noise.

In Figure 5.1, MCML inverter needs five transistors and CMOS logic inverter needs only two transistors. In addition, the MCML requires two lines for each signal. Therefore, a chip area with a given function is about two to four times larger in the MCML than in the CMOS logic. In spite of this disadvantage, the MCML has superior advantages, like shorter delay, lower power consumption and lower noise over CMOS logic at 10GHz operating frequency.

5.2 Design of MCML Circuits

In order to reduce the capacitive loading on the output nodes, the active PMOS loads are replaced by resistive loads (R_L) in our MCML design, as shown in Figure 5.3. The load capacitance at the drain of M1/M2 (including device capacitance) is modeled as C_L .

Figure 5.3: MCML inverter

A first order expression for delay time through an MCML gate is given by [37]:

$$D_{MCML} = \frac{C_L \cdot \Delta V}{I_0} \quad (\text{Equation 5.5})$$

As the MCML circuits are resistively loaded, $\Delta V = R_L \cdot I_0$. Therefore,

$$D_{MCML} = \frac{C_L \cdot \Delta V}{I_0} = \frac{C_L \cdot R_L \cdot I_0}{I_0} = C_L \cdot R_L = \frac{1}{SSBW} \quad (\text{Equation 5.6})$$

Therefore, the delay of a MCML circuit is inversely proportional to the small signal bandwidth ($SSBW$) of the equivalent differential amplifier [37]. The low frequency single ended small signal gain or DC gain can be expressed as:

$$Gain = \frac{1}{2} g_{m1} (R_L // r_{ds1}) \quad (\text{Equation 5.7})$$

If the load resistance is relatively small, the DC gain can be approximated by:

$$Gain = \frac{1}{2} g_{m1} (R_L // r_{ds1}) \approx \frac{1}{2} g_{m1} R_L \quad (\text{Equation 5.8})$$

Therefore, the gain bandwidth product can be expressed as follows:

$$GBW = \frac{g_{m1}}{2C_L} \quad (\text{Equation 5.9})$$

The goal of the MCML circuit design is to create a buffer which has the largest possible bandwidth while still having an acceptable amount of gain. We follow the design methodology described in [37]. First of all, the voltage swing is chosen such that is made as large as possible without forcing the switching transistors into the triode region at any time during the switching cycle. If the differential pair is switched all the way to one side, i.e. $V_{G1} = V_{DD}$ and $V_{G2} = 0V$, for transistor M1 in saturation region, the voltage swing ($\Delta V = R_L \cdot I_0$) must obey the following conditions:

$$V_{DS1} = (V_{DD} - \Delta V) - (V_{DD} - V_{GS1}) \geq V_{Dsat1} \quad (\text{Equation 5.10a})$$

$$\Delta V \leq V_{GS1} - V_{Dsat1} = V_{th1} + V_{eff1} - V_{Dsat1} = \Delta V_{\max} \quad (\text{Equation 5.10b})$$

For long channel transistors, V_{eff} and V_{Dsat} are approximately equal, but for short channel transistors (e.g. $0.18\mu\text{m}$), these two parameters differ greatly especially at relatively high bias currents. This puts the upper limit on the voltage swing. After knowing the voltage swing, the value of I_0 and R_L is to be decided for making up the voltage swing. As suggested by Rogers, the solution is to start with a large value of I_0 and a small value of R_L and then decrease I_0 and increase R_L until the minimum gain specification is met [37].

5.3 MCML Latch

Figure 5.4 shows the schematic of MCML latch. This topology contains a reading pair (M1 and M2) and a latching pair (M3 and M4) driven by opposite

phase of the CLK . When the reading pair of the logic stage begins to change state, the latching pair boosts the current to speed up the output voltage swing. The latching pair provides positive feedback to increase the gain of the stage [38].

Figure 5.4: MCML latch

One critical issue in the MCML latch design is the metastability [37], which would degrade the jitter generation performance in the PD design. Metastability occurs when the time for the latch phase is insufficient for the positive feedback loop to ramp the output voltage from the initial voltage difference ΔV_0 at the beginning of the latch phase to the voltage required for reliable recognition of the digital state ΔV_{logic} . The minimum latch time is approximated by [39]:

$$T_{latch} = \frac{R_L C_L}{g_{m3} R_L - 1} \ln \left(\frac{\Delta V_{logic}}{\Delta V_0} \right) \quad (\text{Equation 5.11})$$

To increase the operation speed of the MCML latch, optimization is usually focused on reducing the size of the latching transistors [40]. In circuit simulation under 0.18 μm CMOS process, a ratio of 1.75 for W_R / W_L is chosen for MCML latch to provide maximum possible operating speed without degrading the metastability operation.

5.4 MCML XOR Gate

Figure 5.5 shows the circuit topology of the MCML XOR gate. It is very similar to the analog multiplier Gilbert cell structure [41]. The upper two differential pairs sample the input A and lower differential pair sample input B . When input B is high, the M1-M2 pair is enabled, therefore, $Q = \bar{A}$ and $\bar{Q} = A$; when input B is low, the M3-M4 pair is enabled, causing $Q = A$ and $\bar{Q} = \bar{A}$. As a result, the output signals $Q = A \oplus B$ and $\bar{Q} = \overline{A \oplus B}$.

Compared with MCML latch, the MCML XOR circuit topology has one obvious advantage that it has no problem of metastability. The reason is that in MCML XOR gate, there are two reading pairs, but no latching pair, which will reduce the possibility getting into the metastable region.

However, in this topology, the signal paths of A and B are not exactly the same, i.e. delay from A to output Q and from B to output Q are not identical,

differential pair of the left-hand Gilbert cell as well as the upper differential pairs of the right-hand Gilbert cell. Therefore, the input capacitance for input A and input B are the same since they have absolutely symmetrical structure. Consequently, the delay time differences between A to Q and B to Q are exactly compensated, and the slight phase error can be minimized.

As it can be observed from Figure 5.6, the obvious disadvantage of the absolutely symmetrical XOR gate is the larger input capacitance, compared to common XOR gate in Figure 5.5. However, this drawback can be mitigated, because (at a given internal output swing and load resistance) each internal gate requires only half of the current of a standard gate [42]. As a consequence, the size of differential pair transistors can be considerably reduced, resulting in a reduction of the input capacitance.

Figure 5.6: Absolutely symmetrical XOR gate

5.5 MCML AND Gate

Figure 5.7 shows the circuit topology of the MCML AND gate. The circuit functions as follows: when B is high, $M6$ is turned off and $M5$ is conducting, thus $Q = A$; when B is low, $M6$ is conducting and $M5$ is turned off, thus $Q = 0$ and $\bar{Q} = 1$.

Figure 5.7: MCML AND gate

5.6 Delay Cell

The half-cycle delay cell in the proposed PD is used to create a half of a bit period delay, i.e. 50ps for 10-Gb/s data rate. It adopts exactly the same circuit topology as the MCML absolutely symmetrical XOR gate in Figure 5.6. The circuit schematic is shown in Figure 5.8. The control voltage V_{BN} is made external to control the delay time over the temperature range and the process corner.

Figure 5.8: Implementation of half-cycle delay cell

5.7 Summary

The detailed circuit implementation of the proposed non-sequential PD is presented in this chapter. The MOS current mode logic (MCML) circuits were adopted in the design since MCML has superior advantages of low power and short delay at GHz operating frequency. The MCML latch, XOR gate and AND gate were analyzed and designed for 10-Gb/s operating speed.

6 Layout Design

A layout is basically a drawing of the mask from which the design of the integrated circuit will be fabricated. The performance of a high-speed digital IC, especially for Gb/s applications, is heavily influenced by its layout. Creating the layout is always as critical as specifying the parameters of the devices. It will determine the behavior of the realized design.

In this chapter, the layout design of the MCML circuits and the proposed non-sequential linear PD will be described. Some consideration on the layout, including the matching resistors and matching transistors, will be discussed. The information is based on Chartered Semiconductor Manufacturing Ltd (CSM) CMOS 6-Metal, 1-Poly, 0.18 μm process.

6.1 Introduction to Chartered Process Design Kit

The Chartered Process Design Kit (PDK) is a complete set of technology files for the Cadence environment that enables the CSM customers to create a custom IC design. It supports current versions of Cadence Analog Design Environment, Schematic Composer, Spectre circuit simulator, Virtuoso Custom Design, Diva physical verification and Assura physical verification. It is provided for Chartered's 0.35 μm , 0.25 μm , 0.18 μm and 0.13 μm Process Technologies [43].

The PDK for 0.18 μm CMOS Analog/RF technology is employed in the

design. It supports the implementation of active devices such as Native and Low V_t transistors, MOS, and BJT; and passive devices such as PN varactors, inductors, insulated metal-to-metal and insulated poly-to-substrate capacitors, resistors and diodes [44].

There are six layers of metal and one layer of poly available for interconnection. The optional features are Salicide block mask to provide non-salicided diffused and poly regions, thicker top metal, and Polyimide layer passivation.

6.2 Layout of Transistors

In a layout, a transistor with a large W/L aspect ratio is drawn either as multiple transistors or as a multifinger transistor. Multiple transistors are identical devices wired in parallel while a multifinger transistor is a single transistor which is split into a number of parallel equal parts arranged in a stack of polysilicon gates within the same active region. The rule of thumb is to choose the width of each finger such that the resistance of the finger is less than the inverse transconductance associated with the finger, i.e., $R_{gi} < 1/g_{mi}$ [45]. Figure 6.1 shows the layout of a multifinger transistor which was employed in this design since most of the transistors are of a large aspect ratio.

Figure 6.1: Layout of a transistor with N fingers

For transistor with a large aspect ratio, the layout should be drawn in matching structures to minimize random mismatches stemming from microscopic fluctuations in dimensions, dopings, oxide thickness, and other parameters that influence component values [46]. Traditionally, there are five types of matching structures commonly used in the layout design: Strip, Common Centroid, ABBA-1, ABBA-2 and ABBA-2 gate separated. The illustration of the configurations of these matching structures is shown in Figure 6.2. Among the five types of matching structures, the ABBA-1 was chosen for the layout design of the proposed PD since it the simplest and least area-consuming structure.

(i) Strip

(ii) Common Centroid

(iii) ABBA-1

(iv) ABBA-2

(v) ABBA-2 Gate-separated

Figure 6.2: Transistor matching structures

Several guidelines should be considered for achieving a good layout for transistors matching. Firstly, we should keep the transistors to be matched close to each other. Secondly, we should place groups of devices around a common geometric center. Thirdly, we should employ identical devices layouts and place them in identical surroundings. Finally, we should orient devices in the same direction.

6.3 Layout of Resistors

For the CSM 0.18 μ m CMOS process, N-well, N+, P+, and poly are available layers for implementing resistors. N+ and P+ resistors have a low sheet resistance (79 Ω /square for N+ and 118 Ω /square for P+) and low accuracy (10% and 25% tolerance for N+ and P+ respectively). N-well layer has a high sheet resistance (780 Ω /square), with a tolerance of about 19%. N-Poly resistor (85 Ω /square) and P-Poly resistor (330 Ω /square) have the highest accuracy.

The considerations for matching resistors are similar to those of matching transistors. It is recommended that the matched resistors are constructed from single material and should be of the same width. Identical geometries should be used for all the resistors in one circuit whenever possible [47]. Matched resistors should be placed in close proximity and dummies should be included in either end of a resistor arrays [46]. Figure 6.3 depicts the layout drawing of matched array resistors A and B. They are cross-connected to achieve matching structure. It is shown that there are four dummy segments placed on the two ends of the resistor array.

Figure 6.3: Resistor layout

6.4 Layout of MCML Circuits

In designing the layout of MCML circuits, the first consideration is the symmetrical drawing since the MCML is heavily relying on the differential signals.

All the transistors were drawn in multifinger structure since they have large aspect ratio. For the biasing transistors or current mirrors, the current matching is important. Therefore, the matching structure ABBA-1 was employed for these transistors. Figure 6.4 shows the layout of a MCML XOR.

Figure 6.4: MCML XOR layout

Detailed layouts of the MCML gates and latch can be found in Appendix A.

6.5 Layout Framework

The layout of the proposed circuits is done using the CadenceTM Virtuoso Layout Editor. The placement of the devices and the interconnections is done by following the design rules guidelines provided by the CharteredTM's PDK for 0.18 μ m CMOS Analog/RF technology.

Still in the CadenceTM Virtuoso Layout Editor, the Design Rule Check (DRC) is performed to the finished layout. This is to ensure that the designers do not overlook and violate any design rules. This is important, as any violations in the design rules will result in almost certainly that the fabricated chip will not work as desired.

An extraction of the layout view is the step following the DRC. This operation takes the mask sequences and attempts to match them with the known sequence for the device. The extraction process will produce the Netlist information for the whole layout and a view that shows the recognized device represented in the schematic symbol format and all the connections together with all the parasitic components that can be extracted from the physical layout view.

The parasitic components, which are extracted from the physical layout view, include the parasitic capacitance due to the same layer coupling, different layer coupling, area overlap, perimeter overlap and coincident edges; and parasitic resistance due to the metal and via interconnects.

The LVS (Layout versus Schematic) operation is performed following the extraction to compare the logical representation in the schematic with the physical representation in the extracted layout. Resistors will be compared for the width and length of each individual bar and its equivalent resistance value. MOS transistors are compared for channel lengths and final device widths. The latter is the sum of transistors' widths when multifingers are used. In addition to the individual device comparison, terminals of each individual component and the connections among those are also compared to those in the schematic view. Upon successful matching, the extracted parasitic components may then be mapped to the schematics. Once the LVS is completed, the circuit is ready for the post-layout simulation.

6.6 Summary

In this chapter, the layout consideration for the transistors, resistors and matched structures were discussed. The layout design of MCML circuits was shown. Finally, the layout framework was described to sum up the whole layout design flow.

7 Comparison and Discussion

This chapter presents the post-layout simulation results for both the proposed non-sequential PD and the half-rate linear PD implemented in CSM standard 0.18 μ m CMOS process.

7.1 Half-rate Linear PD

Up to date, the only 10-Gb/s linear phase detector for SONET OC-192 applications implemented in standard CMOS process is the half-rate linear phase detector reported in [7] (Figure 3.6). To make a fair comparison, the half-rate linear PD was implemented in the same process with the proposed non-sequential PD, i.e. CSM 0.18 μ m CMOS process. The same MCML circuit topology as the proposed PD was also employed for the half-rate linear PD. Further more, the input voltage swings and DC level, the biasing conditions were chosen identically as the proposed PD.

Figure 7.1 shows the post-layout simulation results of the half-rate linear PD characteristic curve. The *Ref* output exhibits a notch when the phase difference is around 40ps. This is the instance when the latches enter the metastable region. As a result, at those instances, the phase difference cannot be captured properly as indicated by the characteristic curve. Due to the same reason, the linear range of the *Dif* curve is limited, only from 30ps-80ps approximately.

Figure 7.1: Half-rate linear PD characteristic curve (post-layout)

7.2 Comparison and Discussion

Figure 7.2 shows the post layout simulation results of the propose non-sequential linear PD characteristic curve. Compared with Figure 7.1, the proposed PD is exhibiting a larger linear range and smaller metastable region. It can be shown that the half-rate linear PD is only working properly when phase difference is from 40ps-80ps roughly, whereas the proposed PD is working well for the phase difference varying from 15ps- 90ps. The reason is that the D-latch employed in the half-rate linear PD is easily to be captured in metastable region at high operating frequencies since it consists of one reading pair and one latching pair. When the phase difference between *CLK* and *Data* is very small, the latching pair is not able to adjust itself to retain the proper voltage swing within required time interval.

However, the proposed non-sequential linear PD avoids using of D-latches, instead it employs the XOR gate consisting of two reading pairs. By this means, the susceptibility to metastable region is highly reduced at high operating speed.

Figure 7.2: Proposed non-sequential linear PD characteristic curve (post-layout)

Table 7.1 compared the proposed PD with other PDs reported in the literature in terms of design complexity. The two CMOS half-rate PDs designed by Jofai are achieving 10-Gb/s operation, however at the expense of design complexity. Take the example of the half-rate linear PD, it consists of 4 latches and 2 XOR gate and power consumption after the post-layout simulation is 39.12mW. While the proposed PD consists of 1 delay cell, 2 XOR gates and 1 AND gate, consuming power of 34.58mW after post-layout simulation under the same process as the half-rate linear PD. The CMOS half-rate binary PD and the non-sequential

PD requires more block elements than the half-rate linear PD, thus we can induce that the power consumption will be larger if they are constructed in the same process.

Table 7.1: Comparison Between Proposed PD and Other PDs Reported in Literature

PD	Linear/Binary	Data rate	Block elements
Half-rate Linear PD in [7]	Linear	10-Gb/s	4 Latches and 2 XOR gates
Half-rate Binary PD in [8]	Binary	10-Gb/s	6 DFFs and 3 Multiplexers
Non-sequential PD in [28]	Binary	2-Gb/s	2 Delay cells, 2 XOR gates and 2 AND gates
Proposed PD	Linear	10-Gb/s	1 Delay cells, 2 XOR gate and 1 AND gate

7.3 Summary

In this chapter, the post-layout simulation results of the proposed non-sequential linear PD are compared with the half-rate linear PD under same process. The proposed PD is exhibiting larger operating range than the half-rate linear PD since it employs the XOR gates, which reduces the susceptibility to metastable region. The simple structure of the proposed PD also gains the advantage of lower power consumption compared with other PDs reported in the literature.

8 Conclusions and Recommendations

This chapter summarizes the major contribution in the design of the 10-Gb/s phase detector for SONET OC-192 standards. The proposed non-sequential linear phase detector is designed to be able to operate at 10-Gb/s with full-rate clock signal. The design of the proposed phase detector is discussed in chapter 4. The detailed implementation of the proposed phase detector using the MOS current mode logic circuits is presented in chapter 5. Chapter 6 describes the layout consideration for the proposed phase detector and finally chapter 7 discusses the comparison between the proposed non-sequential linear phase detector and the half-rate non-linear phase detector. This chapter closes with recommendation for the future work.

8.1 Conclusions

High-speed CDR design must deal with many circuit issues. This thesis focuses on high-speed phase detector design for CDR circuits for SONET OC-192 standard, which requires the data rate to be at 10-Gb/s. The reported CMOS 10-Gb/s PD for CDR applications tends to employ half-rate technique to achieve the high-speed operation. However, they are quite complicated to be implemented. On the other hand, the SONET OC-192 specifies stringent jitter requirements on the CDR circuits, which affects the design of the PD because the jitter performance of the CDR is critically depending on the characteristics of PD. A linear PD is highly desired to achieve small jitter operation since at locking state, the linear PD will produce zero charge pump output that will not generate significant activity on

VCO control line.

In this project, a new non-sequential linear PD for CDR circuits operating at 10-Gb/s is proposed. It avoids the use of DFFs or D-latches, as in the case of Hogge PD and other half-rate PD. Instead, the proposed PD only consists of one half-cycle delay cells, two XOR gate and one AND gate. By this means, the proposed PD achieves larger operating range than the half-rate linear PD [7] since the XOR gate is less susceptible to the metastability than the D-latch. The proposed PD eliminates the problem of half-period skew in the Hogge PD by generate the two pulses at the same time. Thus, at locking condition, the charge pump output will not experience a “triwave” with positive net area, leaving the VCO control line undisturbed. The MCML is adopted to implement the logic blocks in the proposed PD as it is proved to be faster and more power-efficient at 10GHz frequency than the CMOS logic. Absolutely symmetrical XOR gate is employed to achieve equal delay time for both inputs. Built using CSM CMOS 0.18 μm process, the proposed PD is simulated by SPECTRE in CADENCE. The input/output characteristic curve shows that the proposed PD exhibits linear characteristics for low jitter operation of CDR circuits. Because of the simplicity, the proposed PD only consumes 34.58mW power, which is approximately 11% smaller than the half-rate linear PD simulated under same process. The proposed PD consumes a silicon area of $136\mu\text{m}\times 142\mu\text{m}$.

8.2 Recommendations

Although the proposed non-sequential phase detector reported in this thesis achieves better performance at 10-Gb/s operating speed than the half-rate linear phase detector, many issues need to be addressed before the proposed phase detector can be integrated into the Clock and Data Recovery system.

Firstly, the investigation of inclusion of the data recovery process into the phase detector should be done to eliminate the skew between the recovered *CLK* and recovered *Data* at the Clock and Data Recovery block output port. The suggested method could be employing of some other logical gates to realize the function of retiming the incoming data.

Secondly, the power consumption could be further reduced by a lower power supply. However, it may cause the instability of the circuits as described in Chapter 4. One possible method is to integrate a dynamic circuit into the MCML structure to enhance the output swing and reduce the power consumption.

The design could also be migrated into the next generation 0.13 μm CMOS technology. This should allow a degree of margin in designing the circuitry leading to a more robust circuit, which would be more suitable for commercial applications.

Author's Publications

R. Wu, K. S. Yeo, M. A. Do and J. G. Ma, "A new simple linear phase detector for high-speed clock and data recovery circuits", Asia-Pacific Microwave Conference, Korea, Nov. 2003.

R. Wu, K. S. Yeo, M. A. Do, J. G. Ma, X. P. Yu and G. Q. Yan, "A New Simple and Linear PD", submitted to International Symposium on Integrated Circuits, Devices & Systems (ISIC), 2004.

R. Wu, K. S. Yeo, M. A. Do, J. G. Ma, X. P. Yu and G. Q. Yan, "A New Non-sequential Linear CMOS Phase Detector for CDR Applications", submitted to IEE proceedings, Circuits, Devices and Systems.

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Appendix A

MCML XOR Layout

Appendix A

MCML AND Layout

Half-cycle Delay Cell Layout

Appendix A

Proposed Non-sequential Linear PD Layout

Appendix A

Half-rate Linear PD Layout