Fabrication and characterization of InP/InGaAs Metamorphic heterojunction bipolar transistors (HBTs)

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**Fabrication and Characterization of
InP/InGaAs Metamorphic Heterojunction
Bipolar Transistors (HBTs)**

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

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Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

11/05/05
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Summary

High gain metamorphic InP/InGaAs/InP DHBTs (double heterojunction bipolar transistors) on GaAs substrate fabricated using complete NTU in-house process have been demonstrated in this investigation. DC and RF characterization of various MHBTs (metamorphic HBTs), including noise and power measurements, elevated temperature and current stress measurements, evaluation of thermal resistance, and performance comparison of devices grown by different growth techniques have been accomplished. Other important tasks completed include new device design and mask layout, and development of two-micron or less emitter width device process technology. The important findings from this investigation are summarized as follows:

(1) A comparative study of InP-based MHBTs grown by gas and solid-source MBE (molecular beam epitaxy) techniques has been presented. The DC and RF performances of the devices with an emitter size of $1.6 \times 20 \mu\text{m}^2$ and base Be doping concentration of $2 \times 10^{19} \text{ cm}^{-3}$ are summarized. The figures of merit for these two MHBTs have been compared. Results suggest that both the solid-source and the gas-source MBE techniques may offer similar material quality, and hence higher device performances could be achieved by proper optimization of the material growth conditions.

(2) The temperature dependence of the DC characteristics of the metamorphic InP-based DHBT on GaAs substrate has been investigated. The device transport properties of the devices were studied to access the material quality. The experimental results suggest that the band-to-band recombination plays a dominant role in determining the

base current in the studied temperature range of 300 to 400 K, the range where the devices are commonly operated. No trap-related recombination was observed for the base and the collector currents indicating that the metamorphic HBT structures grown by SSMBE offer good material quality.

(3) The stress tests on MHBTs have been carried out under high current density at high junction temperature. Photoluminescence characterization, low frequency noise measurements and electrical tests were performed on MHBT structures. Good correlation obtained between the device degradation during the electrical stress and the optical and low frequency noise measurements may provide important means to assess the device stability for MHBTs. The promising results indicate that, by proper growth optimization of the strain relief buffer layer and the device layer structures, MHBTs on GaAs substrate with electrical stability similar to that of HBTs on InP substrate could be achieved.

(4) Thermal properties of MHBTs grown using a linearly graded InGaP metamorphic buffer have been investigated. Compared to the widely used InAlAs buffer, InGaP offers better thermal properties resulting in a much smaller thermal resistance for the MHBTs. Theoretical calculations of the thermal resistance of devices have been made based on a simple constant heat-spreading model, and the results were found to be consistent with the experimental data. With better thermal conductivity and the flexibility in growth optimization, InGaP metamorphic buffer could be considered as an important alternative to the existing InAlAs and InP schemes.

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Introduction

Metamorphic technology – the growth of the InP-based high electron mobility transistor (HEMT) [1,2] or heterojunction bipolar transistor (HBT) [3,4] layer structures on GaAs substrates has received increasing attention in recent years. It offers many advantages such as the increased substrate size (GaAs is available in larger sizes compared to InP), improved substrate mechanical strength (less brittle), and reduced production cost over the fabrication of devices on InP substrates. Moreover, the availability matured backside fabrication process in the case of GaAs substrates enables the possibility of production of high performance monolithic integrated circuits. InP-based HBTs are, however, attractive for high-speed and medium-power operation due to inherent advantages of their material systems.

Thus, the realization of metamorphic HBTs offers the combined advantages of high performance InP – based device structures and GaAs substrates as illustrated in Fig. 1.1. Applications of metamorphic HBTs (MHBTs) under consideration within the scope of the present investigation are for medium power devices in the microwave/millimeter wave range.

Fig.1.1 Merits of Metamorphic HBTs.

1.1 Motivation

The potential advantages of a bipolar transistor with a wide band-gap emitter were first recognized in a patent application by Williams Shockley in 1948 [5]. The basic theory for this kind of a transistor was further developed by Kroemer in 1957 [6]. Although these advantages of heterojunctions were well recognized, it was not possible to fabricate such junctions with sufficiently high interface qualities for device operation at that time due to technological problems. Hence, it took almost 15 years to demonstrate the first GaAs/AlGaAs HBT grown by liquid phase epitaxy (LPE) at IBM by Dumke et al. in 1972 [7].

Since the mid-70s, two advanced epitaxial techniques, molecular beam epitaxy (MBE) and metal-organic chemical vapour deposition (MOCVD), have been employed for the growth of compound semiconductors. These two growth technologies allow unprecedented control over thickness, (nearly on an atomic layer

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scale) composition (and thus the band structure) as well as doping. These improvements, in turn, allow HBTs to retain the advantages of their Si predecessors, but extend their performances to higher operating frequencies. In addition, a variety of disadvantages of Si bipolar transistors can be overcome. In HBTs, the base can be doped to a very high level, and the base and the emitter can be doped independently. HBTs in the GaAs/AlGaAs material system have been the first beneficiaries for operating at microwave frequencies. Many performance features of HBTs expected in the early days became reality.

During the 1980's, the application of HBT was aimed at radar and military communication systems where the objective was to obtain the fastest circuits possible. At the beginning of the 1990's, more applications were found in the field of wireless and satellite communication systems. The main devices considered were GaAs HBT power amplifiers for cell phones.

Besides GaAs-based HBTs, InP/InGaAs HBTs were first investigated in the early 1980s due to some advantages compared to Si- and GaAs HBTs such as:

- (1) Lower electron effective mass leads to high electron mobility (mobility in InGaAs is 1.6 times that of GaAs and 9 times that of Si). Hence, a short base transit time can be obtained exhibiting higher f_T .
- (2) Higher electron peak velocity results in a shorter collector delay time. It allows a trade-off for thicker collectors with higher breakdown voltage.
- (3) The bandgap energy (E_g) of emitter is much larger than that of the base, such as InP with $E_g=1.35$ eV for the emitter and InGaAs with $E_g=0.76$ eV for the base. This

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allows the base doping to be increased to the limits of dopant incorporation during the growth (10^{20} cm^{-3}), and results in a very low base sheet resistance and a high Early voltage.

- (4) Lower surface recombination velocity, both in InP and InGaAs, is also advantageous for fabricating sub-micron emitter devices for high-speed/high-density IC's without a serious degradation in the current gain.
- (5) Higher substrate thermal conductivity of InP substrate than in the case of GaAs.
- (6) For a given level of the collector doping, InP has a high breakdown field.
- (7) Lower $1/f$ noise than GaAs makes them suitable for low-phase-noise oscillator circuits.
- (8) Lower turn-on voltage offered by the lower bandgap of InGaAs makes them very desirable for operations at low power supply voltages.

Thus, the InP-based device technologies gain operative advantages over GaAs-, Si, and Si/Ge-based semiconductors in terms of speed, better voltage handling capability than SiGe, less power dissipation than GaAs, and superior high-speed performance compared with both the competing materials. Fig.1.2 shows the comparison of the material and electrical properties of Si BJTs, InP HBTs and GaAs HBTs [8]. It illustrates that InP and InGaAs are superior in terms of the current density, the breakdown voltage, and the electron velocity. These characteristics lead to low-voltage operation, improved power output, and higher frequency of device operation respectively. But, InP and GaAs lose out to Si in terms of thermal conductivity.

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In addition, InP-based HBTs are very attractive for applications in optoelectronic integrated circuits due to their capability for the monolithic integration with long-wavelength optical devices [9]. Excellent high-frequency characteristics of InP-based HBTs have been reported with cutoff frequencies greater than 200 GHz [10]. InP-based HBTs are also of great interest for the development of microwave point-to-point links with the emerging 60GHz band and possible 90GHz band applications due to their superior high frequency performance and speed.

Fig.1.2 A comparison of the material and electrical properties of Si BJTs, InP HBTs and GaAs HBTs.

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In terms of InP-based HBTs for military systems and commercial applications, both low noise devices with low power dissipation up to mm-wave and high power devices with good efficiency and linearity in the mm-wave regime are required. InP-based HBTs have demonstrated to be the excellent candidates to fulfill the requirements of low noise and high power density. However, InP-based technology using InP substrate is not well matured compared to GaAs. Moreover, InP substrates are smaller in diameter, significantly expensive and fragile. The challenge is, therefore, to explore the possibility of integrating the InP-based high performance heterostructures on GaAs substrates to develop MHBTs and devices.

Recent advances in the metamorphic growth have resulted in metamorphic high electron mobility transistors (MHEMTs) with excellent DC and microwave characteristics [1,2]. The great success in metamorphic HEMTs has been the motivation to investigate the fabrication and characterization of high performance metamorphic heterojunction bipolar transistors (MHBTs). However, the progress made in realizing the high performance MHBTs has been limited. This is due to a number of factors which include (1) bipolar transistor structure is much more sensitive to defects in the structure than the majority carrier devices such as HEMTs. (2) Material growth and device fabrication of InP-based HBTs on GaAs are more complicated and less mature.

Hwang et al. [11] reported metamorphic InAlAs/In_{0.33}Ga_{0.67}As HBTs on GaAs substrates with a relatively low indium composition (0.33 for InGaAs base) in 1999. Although the use of lower indium composition may ease the material growth, it

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compromises the superior transport properties of InGaAs with higher indium mole fraction. Moreover, the high aluminum mole fraction in the emitter may also cause potential reliability issues. Therefore, fabrication and characterization of InP/In_{0.53}Ga_{0.47}As/InP MHBTs with high indium composition that will equal and even surpass the performance of InP-based lattice-matched HBTs (LHBTs) are of great interest. Recently, InP/In_{0.53}Ga_{0.47}As metamorphic HBTs with high In content were demonstrated for the first time by Wang et al. [3] in 2000.

Despite many desirable features, the InP-based metamorphic HBT technology is less mature and still in its infancy. Studies are limited, and only a few research works have reported on the DC and RF performance of such devices [12,13]. Many technical issues need to be addressed in terms of both growth and fabrication technologies before these devices can be considered for utilization in commercial systems.

Although MHBTs fabricated using gas source MBE and solid source MBE have been reported, it is useful to compare the characteristics of identical device structures grown by different growth techniques to assess the material quality. For the MHBTs with a compositionally graded strain relief buffer layer, the temperature and bias stability become the important issues for practical system applications. However, the device thermal stability related issues such as the degradation of MHBTs under high current density at high junction temperature have not been addressed. Short-term bias-temperature stress tests on MHBTs under high current density at high junction temperature should reveal the stability of the devices.

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One of the important issues in the metamorphic technology is the relatively high thermal resistance of the buffer layer, which may potentially limit the device power performance. Thus, a detailed study on the thermal properties of MHBTs using different metamorphic buffer layers need to be performed. The results will be important in the design of layer structure for MHBTs to achieve better thermal properties.

In this study, double heterojunction $\text{InP}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ HBTs grown on GaAs substrate have been studied systematically, including the structure optimization, new mask set designing, process development and devices characterization. DC and RF characteristics including microwave noise and power performances of the HBTs have been investigated, and the figures of merit of these devices are compared wherever possible. The primary focus of this investigation is on the device fabrication and characterization with little emphasis on the epitaxial growth.

1.2 Objectives

The objective of this investigation is to develop fabrication and characterization technologies for the double heterojunction $\text{InP}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ metamorphic HBTs (MHBTs) on GaAs substrate. The research work will focus on the fabrication and DC and RF characterization of MHBTs, including noise and power measurements, elevated temperature and current stress measurements, evaluation of thermal resistance, and performance comparison of devices grown by different growth techniques.

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1.3 Major contribution of the Thesis

The work presented in this thesis was initiated to comprehensively understand and address the major issues in realizing InP-based metamorphic heterojunction bipolar transistors (MHBTs) on GaAs substrates for high frequency applications. The most important contributions of this work are summarized as following:

- (1) Development of a complete in-house fabrication process technology for MHBTs especially for devices with the emitter width of 2 micrometer or less. It includes layer structure optimization, new device design and mask layout.
- (2) A comparative study of MHBTs grown by gas and solid-source molecular beam epitaxy (MBE) techniques has been carried out. DC and RF characterization including noise and power performances have been evaluated. The results suggest that both the epitaxial growth techniques may offer similar material quality, and hence higher device performances could be achieved by proper optimization of the material growth conditions.
- (3) Detailed investigations on the thermal reliability (300K-400K) of the high gain metamorphic InP/InGaAs/InP HBTs on GaAs substrate have been carried out. The device DC properties were studied to assess the material quality.
- (4) Study of the short-term bias-temperature stress tests on MHBTs under high current density at high junction temperature: Good correlation between the optical and

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low frequency noise measurements, and the device degradation during the electrical stress indicated that the optimization of the strain relief buffer was believed to be the most critical step to achieve high device stability.

(5) Thermal properties of metamorphic InP/InGaAs/InP MHBs using a linearly graded InGaP buffer have been investigated. Based on the experimental data and a theoretical model, InGaP is found to offer better thermal properties resulting in a smaller thermal resistance for the MHBs. Hence, it could be considered as an important alternative to the existing InAlAs and InP metamorphic buffer layers.

1.4 Organization of the Thesis

The motivation and the objectives of this project are described in Chapter 1. The theoretical background related to the device DC and RF figures of merit is reviewed in Chapter 2. Chapter 3 describes the InP-based lattice-matched and metamorphic HBTs fabrication technology developed in this work. In Chapter 4, the HBT layer structures used in this work and the DC and RF performance of the fabricated devices are presented. The designing of the new mask set is also discussed in this chapter. A comparative study of InP-based metamorphic HBTs grown by gas and solid-source molecular beam epitaxy (MBE) techniques is reported in Chapter 5. DC and RF characteristics including microwave noise and power performances of the devices are reported and the figures of merit of these devices are compared. Chapter 6 reports on the DC characterization of metamorphic InP/InGaAs HBTs at elevated temperatures. The device transport properties are studied to assess the material quality. Chapter 7

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studies the device stability performance of the metamorphic InP/InGaAs HBTs under high current and high temperature stress. PL characterization and electrical tests including low frequency noise measurements performed on MHBT structures to address the device stability are described. In Chapter 8, the thermal properties of metamorphic InP/InGaAs/InP MHBTs using a linearly graded InGaP buffer are investigated. Theoretical calculations of the device thermal resistance have been reported based on the simple constant heat-spreading model. Finally, the conclusions of the present work with recommendations for future work are given in Chapter 9.

Chapter 2

Device Physics of HBTs

2.1 Introduction

In this chapter, the basic principles of HBT are discussed. Section 2.2 introduces the operating principles of HBT, and Section 2.3 introduces DC parameters and important figures of merit used in DC and RF characterization of HBTs.

The key part of a HBT is the emitter-base heterojunction with the bandgap of the emitter being larger than that of the base. It is possible to dope the base much higher than the emitter without significantly decreasing the current gain. Hence, an InP-based HBT structure normally consists of a wider band gap material such as InP (1.353 eV) for the emitter and a narrow band-gap material such as InGaAs (0.737 eV) for the base. The use of high base doping density produces the following two positive effects on the transistor performance: (1) a low base resistance resulting in higher $f_{\max}$ and lower $NF_{\min}$, and (2) a very thin base (without running the risk of base punch-through), leading to a short base transit time and thus a high cutoff frequency f_T .

The advantage of DHBTs is the wider bandgap of the collector resulting in a larger Early voltage, which is equivalent to a smaller output conductance, and a

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higher breakdown voltage. Hence, InP is used as the collector for InP DHBTs. However, due to the large conduction band discontinuity between the InGaAs base and the InP collector, InP/InGaAs DHBTs typically suffer from the conduction band spike hindering the electron transport [14]. In order to minimize the conduction band spike, the special collector design so-called composite collector (InGaAs/InP) is used [15,16]. In this structure, the collector consists of two different materials namely the narrow bandgap InGaAs and the wide bandgap InP. Insertion of InGaAs moves the top of the barrier (InP) spatially to below the base conduction band level. For such structures, optimization of the InGaAs layer thickness in the composite collector structure is necessary in order to suppress the current blocking effect without sacrificing the breakdown voltage.

2.2 Operating Principle of the HBT

The Heterojunction Bipolar Transistor (HBT) has three terminals, namely emitter, base and collector, and can be either a single HBT or a double HBT. The emitter and the base are made of different materials, with the bandgap of the emitter being larger than that of the base. For DHBTs, on the other hand, the base and the collector are made of different materials too, thus both the emitter-base junction and the collector-base junction are heterojunctions.

When the emitter-base heterojunction of an HBT is forward-biased, electrons are injected from the emitter into the base. The amount of the forward bias voltage V_{BE} applied to the emitter-base heterojunction governs the magnitude of the electron injection and thus the collector current I_C . Fig. 2.1 shows the energy band diagrams of

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the emitter-base junction of an abrupt HBT. The bandgap of the emitter and the base are E_{GE} and E_{GB} , respectively, and the bandgap difference ΔE_G is $(E_{GE} - E_{GB})$. The emitter and the base materials have different electron affinities, and the bandgap difference is shared between the conduction and the valence band offsets ΔE_C and ΔE_V , respectively. The potential barrier for the electrons is smaller than that for the holes as shown in Fig. 2.1. Thus, the undesired holes injection from the base to the emitter is effectively suppressed and an acceptable current gain can be obtained, even if the base doping is equal to or higher than the emitter doping.

Fig. 2.1 Energy band diagrams of the emitter-base junction for abrupt HBTs.

The emitter injection efficiency G_e has the general form of

$$G_e = \frac{I_n}{I_p} \quad (2-1)$$

where I_n and I_p are the electron and hole diffusion currents crossing the forward-biased emitter-base junction, respectively, and

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$$G_e \propto \frac{N_{DE}}{N_{AB}} \exp \frac{\Delta E_V}{k_B T} \quad \text{for an abrupt heterojunction [17,18]} \quad (2-2)$$

Here, N_{DE} is the emitter doping density, N_{AB} is the base doping density, k_B is the Boltzmann constant, and T is the temperature. Due to the exponential term in Eq. (2-2), it is clear that larger emitter injection efficiency can be obtained in HBTs than in BJTs with comparable emitter and base doping concentrations. The larger emitter injection efficiency automatically leads to a large common-emitter current gain.

Fig. 2.2 Forward active region of operation of a common emitter HBT (npn)

Thus, in the case of a common emitter HBT with forward active mode (shown in Fig. 2.2), the forward biasing of the emitter/base junction causes a large number of electrons to be injected from the emitter into the base. A concentration gradient is

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therefore established in the base, which encourages the electrons to diffuse towards the collector. If the base of the transistor were very wide all the injected electrons would recombine before reaching the collector, and the transistor would merely behave like two back-to-back diodes. However, the essence of the bipolar transistor is that the base is sufficiently narrow, and the majority of the electrons can reach the collector/base junction, where they are swept across into the collector by the large electric field across the reverse biased junction. This is achieved by making the base width comparable to, or smaller than the diffusion length of the electrons in the base. The base current is determined by the number of holes injected from the base into the emitter [19].

However, obtaining a very large current gain is typically not the primary design goal for a microwave transistor. Instead, a more important issue is that an acceptable current gain is achievable with $N_{DE} \ll N_{AB}$, and that the base dopant concentration can be made very high. A high base doping density is desirable for microwave transistor operation. First, it allows for a very thin base without running the risk of having base punch-through. A narrow base, in turn, leads to a smaller base transit time providing a high cutoff frequency (f_T). Second, the high base doping density corresponds to a smaller intrinsic base resistance R_{Bi} , which gives rise to a high maximum frequency of oscillation (f_{max}) and an improved high-frequency noise performance. A low emitter doping density is also beneficial for high-speed operation. It leads to a smaller emitter-base space-charge region capacitance and therefore a smaller emitter-base delay time Γ_{EB} . To realize the above-mentioned advantages,

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HBTs frequently employ base doping density levels exceeding the emitter doping density.

2.3 DC Parameters and Figures of Merit of HBTs

2.3.1 DC Parameters

1) Common-emitter Current Gain

The DC current gain (β) is one of the most important parameters in bipolar transistors. It is the ratio of the collector current (I_C) to the base current (I_B) [20]. I_B consists of various current components as:

$$I_B = I_{BP} + I_{B,surf} + I_{B,cont} + I_{B,bulk} + I_{B,scr} \quad (2-3)$$

They are:

- (0) I_{BP} hole back-injection to emitter current
- (1) $I_{B,surf}$ surface recombination current in the exposed extrinsic base region
- (2) $I_{B,cont}$ interface recombination current at the base contact
- (3) $I_{B,bulk}$ bulk recombination current at the base region
- (4) $I_{B,scr}$ space-charge recombination current in the base-emitter space-charge region

The overall base current mainly consists of four recombination current components as shown in Fig. 2.3, and the holes back-injection to emitter current.

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The current I_{BP} is constituted by the flow of holes injected from the base to emitter. The energy-gap difference between the base-emitter heterojunction in the HBT effectively eliminates this current component.

Fig. 2.3 Schematic diagram showing the location of the four main base recombination currents in HBTs.

The effect of the second component of the base current, $I_{B,surf}$ is negligible in InP HBTs. This is due to very small surface recombination velocity of about 10^3 cm/s for the base materials such as InGaAs.

The excess carrier concentration decreases rapidly from the intrinsic base region towards the extrinsic region. When the base-emitter contact separation is large,

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the excess carrier concentration at the base contact is nearly zero and hence $I_{B,cont}$ is nearly zero. Even in the microwave transistors whose base-emitter contact spacing is small due to base-emitter self-alignment, the number of excess carriers in the contact interface is substantially reduced from its value in the intrinsic region such that $I_{B,cont} < I_{B,surf}$.

The base bulk recombination current $I_{B,bulk}$ is related to the recombination in the quasineutral base and is constituted by the flow of holes to supplement the loss of holes in the quasineutral base due to the recombination. The current can be estimated by [17],

$$I_{B,bulk} = \frac{qn(x_{BE})w_B}{2\tau_n} A_E \quad (2-4)$$

where w_B is the thickness of the quasineutral base, τ_n is the minority electron lifetime in the base and A_E is the emitter area.

The last base current component, $I_{B,scr}$ is the electron-hole recombination current in the emitter-base space-charge region. It is proportional to the emitter area and depends on the base-emitter voltage as:

$$I_{B,scr} \propto \exp \frac{V_{BE}}{2V_T} \quad (2-5)$$

where V_{BE} is the base-emitter applied voltage and V_T is the thermal voltage.

When $I_{B,bulk}$ is the dominant base current component, the current gain can be expressed as :

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$$\beta = \frac{I_C}{I_{B,bulk}} = \frac{\tau_n}{\tau_b} \quad (2-6)$$

where τ_b is the minority carrier transit time across the base. When the base electric field is zero, τ_b is given as:

$$\tau_b = \frac{X_B^2}{2D_{nB}} \quad (2-7)$$

where X_B is the base thickness and D_{nB} is the electron diffusion coefficient in the base.

2) Gummel Plots and Ideality Factors

Gummel Plots illustrate both the collector current I_C and the base current I_B on a logarithmic scale as a function of the forward-bias voltage V_{BE} applied between the base and the emitter terminals, and can be represented as

$$I \sim \exp[qV_{BE}/(nkT)] \quad (2-8)$$

where n is the ideality factor. It can be easily calculated from the $\log I_C$ ($\log I_B$) versus V_{ce} (V_{be}) curve (Gummel plots). For a device with good material quality, both the base and the collector currents are normally approximately ideal (n close to 1) in the medium current level.

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At the low current region, the base current could be larger than its ideal value. This is due to the presence of the defects or surface states giving rise to significant generation-recombination current. The generation-recombination current usually can be recognized by its $\sim 2kT$ ($n \sim 2$) dependence on V_{BE} . In the HBTs, the generation-recombination current adds to the base current and hence degrades the dc current gain. By properly optimizing the material growth and the device fabrication process to reduce the defects and the surface states density, the generation-recombination current component can be largely reduced.

At the high current region, the reduction of the base and the collector currents from their ideal behavior is mainly due to the effect of emitter and base parasitic series resistances. As the currents flow through these parasitic resistors, the voltage drops on these resistors tend to offset the externally applied voltages and thus degrade the base and the collector currents. Proper design of emitter and base doping level and optimization of the fabrication process is important [20].

3) Output Conductance

High voltage gain and device linearity result from low output conductance, g_o given by:

$$g_o = \frac{dI_c}{dV_{ce}} \quad (2-9)$$

Both the base-width modulation by the base-collector voltage (Early effect) and the impact ionization in the collector can cause the increase of device output conductance. Because of the high base doping in the InP HBTs, the early voltage is normally about

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10 to 20 times higher than that for Si bipolar transistors. In the InP/InGaAs SHBTs, high output conductance is mainly due to the high impact ionization rate in the InGaAs. The use of a wide band gap material such as InP as the collector has been found to be the most effective approach to improve the output conductance in InP HBTs [21].

4) Breakdown Voltage

The HBT breakdown voltage involving the collector-base junction, the emitter-base junction, and the collector-emitter junction govern the HBT operating limits such as the linearity and the output power. The breakdown voltages are defined as follows:

Collector-Base Junction Breakdown voltage (Emitter Open), BV_{cbo} : High BV_{cbo} is desired for high device linearity and high-power application. The BV_{cbo} is mainly decided by the collector doping level and its thickness. Thicker and lower doped collector increases the breakdown voltage (avalanche process) at the cost of increased effective transit times.

Emitter-Base Junction Breakdown voltage (Collector Open) BV_{ebo} : This junction, which controls the current gain, is the most sensitive to reverse-bias currents that can damage the device. The breakdown mechanism is a combination of avalanche and Zener tunneling processes. High BV_{ebo} is required only for a few applications.

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Collector-Emitter Breakdown voltage, BV_{ceo} : This voltage is governed by the collector-base breakdown coupled with a feedback multiplication factor of the current gain as the base is driven by a current source. The relationship between BV_{ceo} and BV_{cbo} can be written as:

$$BV_{ceo} = BV_{cbo} (1 - \alpha)^{1/\eta} \approx BV_{cbo} (\beta)^{-1/\eta} \quad (2-10)$$

where α is the common-base current gain. It is apparent that BV_{ceo} is smaller than BV_{cbo} and that there is a trade-off between the current gain and the breakdown voltage BV_{ceo} . Notice that higher β results in lower BV_{ceo} .

2.3.2 Figures of Merit of HBTs

1) Unit current gain cut-off frequency, f_T

For small-signal applications, the cut-off frequency, f_T is defined as the transition frequency at which the common-emitter, short-circuit load, small-signal current gain h_{21} drops to unity (or 0 dB). The current gain is frequency dependent, and its magnitude rolls off at higher frequencies with a slope of -20 dB/decade for any transistor.

The unity current gain cut-off frequency (f_T) of an HBT is given by:

$$f_T = \frac{1}{2\pi\tau_{ec}} \quad (2-11)$$

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where $\tau_{ec} = \tau_{ee} + \tau_b + \tau_c + \tau_{cc}$ is the total HBT emitter-to-collector transit time, $\tau_{ee} = (kT/qI_c) C_{be}$ is the emitter-base charging time, τ_b is the base transit time including the diffusion and the drift terms, τ_c is the collector depletion-layer transit time, and $\tau_{cc} = (kT/qI_c + R_e + R_c) C_{bc}$ is the collector charging time.

At low current densities, the cut-off frequency is determined by the emitter-base and the collector-base charging time. At high current densities, f_T is mainly decided by the base and the collector depletion layer transit times. To maximize f_T , the capacitances C_{be} and C_{bc} and the forward transit times τ_b and τ_c should all be minimized. The simplest way to minimize the capacitance is to use advanced device structures that have small parasitic capacitance. The base transit time can be reduced effectively by reducing the intrinsic base thickness. However, reducing the base thickness alone will lead to a large intrinsic base resistance.

It should be pointed out that, at sufficiently large collector current density, base widening becomes important causing the rapid increase of τ_b , and hence f_T decreases rapidly with the further increase of current density. A simple way to increase the peak f_T of an HBT is to increase its collector doping concentration to shift the f_T roll-off to a higher current, provided that the device breakdown voltages remain acceptable. Moreover, it has been found that, the existence of extreme nonequilibrium electron transport in the base of InP-based HBTs also enhances the microwave performances.

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2) Maximum frequency of Oscillation, f_{MAX} (unity power gain)

The maximum frequency of oscillation or the so-called maximum unity power gain is the maximum frequency at which the transistor still provides a power gain.

The unilateral power gain U of a HBT can be expressed in terms of f_T by

$$U = \frac{\alpha_B^2 \omega_T}{4R_B C_{cb} \omega^2} \quad (2-12)$$

where the angular frequency $\omega = 2\pi f$, $\omega_T = 2\pi f_T$, and α_B is the base transport factor. If the base transport factor is approximately unity, which is the case for properly designed BJTs, and bearing in mind that f_{MAX} is the frequency at which U becomes unity, f_{MAX} for a bipolar transistor can be obtained as:

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_b C_{bc}}} \quad (2-13)$$

The optimization of the $R_b C_{bc}$ charging time constant is critical in designing and fabricating high performance HBTs for microwave applications. However, maximizing f_{MAX} by reducing R_b and C_{bc} is a complex trade off process. Designs that increase f_T at the expense of increasing R_b can result in a decrease in f_{MAX} . While, if C_{bc} is reduced by reducing the collector doping concentration, base widening will set a lower collector current density, which in turn can reduce the maximum f_T of the HBT. Recent experimental results indicate that, reducing C_{bc} by undercutting extrinsic

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collector could be an effective approach for simultaneously increasing both f_T and f_{MAX} in InP HBTs [20].

3) Minimum Noise Figure and Associate Gain

A figure of merit describing the amount of intrinsic noise produced in microwave transistors is the noise figure NF. The noise figure (commonly given in decibel) is defined by [22]:

$$NF [dB] = 10 \log \frac{P_{Si} / P_{Ni}}{P_{So} / P_{No}} \quad (2-14)$$

where P_{Si} and P_{So} are the signal powers at the input and output, and P_{Ni} and P_{No} are the noise powers at the input and output, respectively.

The magnitude of NF is dependent on the matching conditions at the input of a transistor, bias conditions, and frequency. Unfortunately, the matching and the bias conditions required for obtaining the minimum noise figure NF_{min} are different from those for maximum power gain. Therefore, if the transistor is to be operated with the minimum noise, it will possess a power gain considerably lower than MAG, MSG, and U. The power gain obtained from the transistor biased and matched for the minimum noise is called the associated gain G_a .

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4) Output Power and Power-Added Efficiency

The output power P_{out} and the power-added efficiency PAE are two figures of merit relevant to power transistors. For a power transistor, the amount of microwave power that can be delivered to the load is of primary importance whereas the noise figure is of no concern. P_{out} is dependent on the frequency and the type of the amplifier circuit. The output power can be expressed either directly in watts (W) or in dBm according to:

$$P_{out} [\text{dBm}] = 10 \log P_{out} [\text{mW}] \quad (2-15)$$

The output power is frequently reported in terms of power density, and the commonly used figure of merit is the output power per μm^2 emitter area of the device. Despite the fact that these figures of merit are not the measures for the total output power of a certain transistor, they offer a general idea of the power handling capability of the transistor and allow for the comparison of power performances between different transistors or even different types of transistors.

In power amplifiers where the heat dissipation and the battery power consumption are of concern, the power-added efficiency is an important figure of merit. It is defined as:

$$\text{PAE} = \frac{P_{out}(hf) - P_{in}(hf)}{P_{in}(dc)} \quad (2-16)$$

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where $P_{\text{out}}(\text{hf})$ and $P_{\text{in}}(\text{hf})$ are the transistor's microwave output and input powers, respectively, and $P_{\text{in}}(\text{dc})$ is the dc power delivered by the power supply including the power dissipated as heat in the transistor. For microwave power transistors, high output power and power-added efficiency are desirable.

Chapter 3

Device Fabrication Process for InP/InGaAs HBTs

3.1 Introduction

The typical process flow for the fabrication of InP/InGaAs HBTs is illustrated in Fig. 3.1. It consists of emitter ohmic metal deposition, emitter mesa formation, base ohmic metal deposition, base mesa formation, collector ohmic metal deposition and collector mesa formation. This is followed by air-bridge pillar and interconnection process, passivation of devices and finally electrical testing. The process flow is essentially the same for both MHBTs and LHBTs. Development of a high yield fabrication process is one of the important tasks in this investigation. The overall fabrication process is summarized in Appendix A.

Fig. 3.1 The typical process flow for InP/InGaAs HBT fabrication

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Mesa-type isolation is typically employed for InP HBTs, since the low bandgap InGaAs base layer has made it difficult to fabricate planarized devices using ion-implantation isolation. In this work, all the patterning was performed using contact optical lithography and wet etching processes. The key features of each processing step have been described in detail in the following sections.

3.2 Formation of Mesa and Ohmic Contact

An all-wet-etching process was used to create the mesas and trenches. Precise etching control is critical to the success of device fabrication and device performance. For InP/InGaAs HBTs, a mixture of $\text{H}_3\text{PO}_4 : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$ in the ratio of 15:5:200 was used to etch InGaAs which has a strong selectivity for InGaAs over InP. A solution of $\text{HCl} : \text{H}_3\text{PO}_4$ in the ratio of 1:5 was used to etch InP which has high selectivity over InGaAs. The etch rate was observed to be 16 nm/s for InGaAs and about 20 nm/s for InP. By taking advantage of the selective etching capability, suitable undercut of the emitter mesa can be easily achieved which allows for making the base contacts self-align to the emitter mesa without shorting the base-emitter junction. The self-aligned base etching helps to minimize the distance between the emitter and the base thereby reducing the base resistance R_B . Combining the thickness measurement techniques and the surface breakdown characteristics, a highly reliable and repeatable HBT process has been developed for mesa formation. A metallization scheme using Ti/Pt/Au was developed for n- and p-type ohmic contacts. Good electrical and morphological characteristics of the ohmic contact have been achieved with high yield. The details are described as follows:

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3.2.1 Formation of Emitter Ohmic Contact and Emitter Mesa

The formation of emitter ohmic contact and emitter mesa is illustrated in Fig. 3.2 (a). After cleaning the wafer, the image reversal photoresist AZ5214 was coated, and then patterned using the emitter level mask. It was followed by the metallization using E-beam evaporation. The use of the image reversal photoresist is mainly to generate an undercut profile suitable for easy metal lift-off. The undercut profile is necessary for the successful lift-off because it generates discontinuity in the deposited metal for the solvent to penetrate and dissolve the photoresist. The discontinuity also prevents ragged edges due to tearing or peeling of the metal. The image reversal process must be carefully controlled for the device fabrication, especially in the fabrication of small patterns. In order to obtain better lift-off in the case of smaller sized samples, cleaning of the edge for good lithography contact and over development are necessary. Using this procedure, good electrical and morphological characteristics of the ohmic contacts have been achieved with high yield.

Following the development of emitter metal, wet etching steps were performed to define the emitter. The first etching was to remove the highly doped InGaAs cap using $\text{H}_3\text{PO}_4 : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$ and stop the etching on InP. For the selective etch, the etching should be stopped when the color of the wafer is observed to be the same all over the surface. The complete removal of the InGaAs layer can be further confirmed by measuring the step height using a surface profiler. The second etching was followed using a solution of $\text{HCl} : \text{H}_3\text{PO}_4$ in the ratio of 1:5 to selectively etch the InP emitter layer stopping on p+ InGaAs base layer. The key point during the emitter

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etching is to control the emitter undercut by carefully controlling the over etching time of the InP emitter layer. The emitter etching was verified by performing I-V measurements observing the surface breakdown using a pair of tungsten probe tips. The breakdown voltage of the Schottky diode formed on the p+ InGaAs base should be much lower than that on the InP emitter layer.

3.2.2 Formation of Base Ohmic Contact and Base Mesa

The formation of base ohmic contact and base mesa is illustrated in Fig. 3.2 (b). The base lithography was done using the same procedure as the emitter lithography. However, this is a critical step as the alignment needs to be precise and rework is undesirable. Metal deposition and lift-off was done as in the case of the emitter. It is important that the thickness of the metal deposited using E-beam evaporator is controlled well. The thickness of the metal should be less than the thickness of the emitter cap plus the emitter layer. Otherwise, the thicker base metal will make base-emitter short due to the self-aligned base configuration. The next step was to etch the base-collector junction down to the subcollector, after the emitter-base region was covered with the AZ1518 positive photoresist mask. In an InP/InGaAs DHBT, this step is made simple due to the excellent etching selectivity present between InP and InGaAs. The first step was to etch the InGaAs base and the InGaAs setback layer. The second step was to etch InP down to the subcollector. Finally, the photoresist was rinsed away with acetone.

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3.2.3 Formation of Collector Ohmic Contact and Collector Mesa

The formation of collector ohmic contact and collector mesa is illustrated in Fig. 3.2 (c). The procedure is similar to the base and the emitter lithography as discussed before. The thickness of the collector metal used was 50nm/200nm for Ti/Au. The mesa isolation was achieved as follows: the HBT mesa was covered with AZ1518 positive photoresist. The first step was to etch the thin InGaAs etch stop layer in the subcollector. In order to isolate the emitter, the base and the collector, the etch time for this step should be long enough. The InP subcollector was etched down into the semi-insulating substrate for LHBTs or semi-insulating buffer layer for MHBTs. The depth was monitored using the surface profiler, and SEM was employed to confirm that the trenches under the neck of the emitter and the base were etched clear. I-V measurement was conducted to ensure that the subcollector had been etched completely and that the etching had reached the semi-insulation layer. Finally, the photoresist was rinsed away using acetone. Fig. 3.3 shows the SEM micrograph of a triple-mesa structure fabricated by the wet etching process.

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Fig. 3.2 (a) Formation of emitter metal contact and emitter mesa

Fig. 3.2 (b) Formation of base metal contact and base mesa

Fig. 3.2 (c) Formation of collector metal contact and collector mesa

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Fig. 3.3 SEM picture of InP HBT with a triple-mesa structure fabricated by wet etching process.

3.3 Air-bridge Interconnections

An air-bridged interconnect process was developed to connect the emitter, the base and the collector ohmic metal contacts to the thick external metal pads for probing or wire-bonding the devices. Using the air-bridged interconnection process, the issue of mesa step coverage for interconnection metal can be eliminated. Moreover, this process allows us to fabricate mesa-type HBTs with small emitter size without using any dielectric layer for isolation. This process, combined with the non-alloyed Ti/Pt/Au ohmic metallization, yields a very low thermal budget for the device fabrication. Fig.3.4 shows the process sequence for the fabrication of air-bridged interconnections.

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Fig.3.4 Process sequence for the fabrication of air-bridged interconnection

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In this process, the positive photoresist AZ 1518 was spun on the entire wafer. The openings for the pillars to connect to the emitter, the base and the collector contacts were then defined. The photoresist was then reflowed by baking at 110 °C for 15 min. Ti/Au (20nm/80nm) seeding layer was then deposited over the wafer by sputtering or electron-beam evaporation. AZ 5214 photoresist (2.5 µm thick) was then applied, and the air-bridge openings were defined by using the image reversal lithography process. The Ti/Au seeding layer was then removed using buffer HF and gold etchant, respectively. The etchant used for Au was $[I_2 : KI : H_2O = 1:4:40] : H_2O$ in the ratio of 1:3 and the etchant for Ti was $HF : HNO_3 : H_2O$ in the ratio of 1:2:63. In order to have the clear edge during the metal etching, this process was carried out in an ultrasonic bath. The thick Ti/Au layer (1.2 µm) was then deposited followed by lifting-off to finally form the interconnections. Alternatively, the thick interconnection metal (Au) can also be deposited by electroplating. In this case, the Ti/Au seeding layer should be etched after the electroplating. The SEM photograph of a fabricated InP HBT with the air-bridged interconnections is shown in Fig. 3.5. Devices with emitter areas as small as $1.6 \times 20 \text{ } \mu\text{m}^2$ can be fabricated using this air-bridged interconnection process.

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Fig. 3.5 SEM picture of a fabricated InP HBT with air-bridged interconnections.

3.4 Device Passivation

Different dielectric materials such as silicon nitride (SiN), silicon oxide or polyimide can be used for device passivation. The SiN can be deposited by using plasma enhanced chemical vapor deposition (PECVD) technique. Good quality SiN film can be obtained by PECVD with a substrate temperature of 300°C. However, Wang et. al [23] have found that passivation of InP DHBT using PECVD SiN may cause significant degradation in current gain, which could be due to the plasma induced surface damage during the SiN deposition. For InP-based HBTs, polyimide has been found to induce the least degradation compared to SiN_x and SiO₂ [24].

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Hence, a polyimide passivation process using ULTRADEL® 7501 was developed. The film thickness was about 1.5 μm . The polyimide was first cured at 200 °C in N_2 for 1 hour followed by a second curing at 325 °C in N_2 for 30 minutes.

Chapter 4

Device Layer Structure and Mask Design

4.1 Introduction

The successful development of metamorphic heterojunction bipolar transistors (MHBTs) has been the motivation to investigate the material growth, device fabrication and characterization of MHBTs to further improve the device performance. The vertical layer structures and the layout design play an important role in the determination of the high performance of InP/InGaAs HBTs. In this chapter, the material growth and the device layer structures, and the DC and RF characterization results obtained for both MHBTs and LHBTs are described and compared. In order to further enhance the DC and RF performance of the MHBTs, a new mask-layout designed has also been described in detail.

4.2 Material Growth and Device Layer Structure

The growth of InP/InGaAs MHBTs and the reference lattice-matched HBTs (LHBTs) were carried out using gas-source molecular beam epitaxy (GSMBE) technique. The substrates used were 2-inch semi-insulating (100) GaAs substrates for MHBTs and 2-inch semi-insulating (100) InP substrates for LHBTs. Si and Be were used as n- and p-type dopants, respectively. The layer structure used for MHBTs was

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the same as the ones used for the InP/InGaAs LHBTs except for the additional buffer layer in the case of MHBTs. For MHBTs, the buffer layer stack consists of a 1.5 μm linearly graded $\text{In}_x\text{Al}_{1-x}\text{As}$ (x varying from 0 to 0.48) metamorphic buffer layer and a 500 Å InP layer. The metamorphic buffer layer serves two purposes [25,26]: (1) to transform the lattice constant from GaAs substrate to that of the high indium content device active layers, and (2) to trap the dislocations and prevent them from propagating into the active layers.

The surface morphology of the MHBT wafers has been studied by atomic force microscope (AFM). Fig.4.1 shows an AFM image ($5 \times 5 \mu\text{m}^2$) of a typical MHBTs sample. The RMS roughness value of the surface texture obtained by AFM in a $5 \times 5 \mu\text{m}^2$ region was about 2nm.

Fig.4.1 AFM image ($5 \times 5 \mu\text{m}^2$) of a typical MHBT sample.

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The detailed layer structure of the MHBTs is given in Table 4.1. The key features of this structure include a thin InGaAs base (50 nm) doped at $2 \times 10^{19} \text{ cm}^{-3}$ with Be and an InGaAs/InP (450 nm) composite collector with dipole-doped interface, and an InP layer for the subcollector to improve the device breakdown.

Table 4.1 Layer structure of the metamorphic InP/InGaAs DHBT

Layer Structure -MHBTs		
Emitter Cap	InGaAs:Si (2×10^{19})	2000 Å
	InP:Si (2×10^{19})	600 Å
Emitter	InP:Si (3×10^{17})	900 Å
Base	InGaAs:Be (2×10^{19})	500 Å
Collector	InGaAs:Si (5×10^{15})	400 Å
	InGaAs:Be (1×10^{18})	50 Å
	InP:Si (1×10^{18})	50 Å
	InP:Si (5×10^{15})	4000 Å
	InGaAs:Si (8×10^{18})	300 Å
	InP:Si (8×10^{18})	5500 Å
Buffer	InP	500 Å
	AlAs $\rightarrow$ In _{0.52} Al _{0.48} As	1.5 μm
	GaAs	1000 Å
GaAs (100) S. I. Substrate		

The emitter layer consists of a highly doped ($2 \times 10^{19} \text{ cm}^{-3}$) InGaAs cap and a wide bandgap InP layer. The cap layer ensures a low emitter ohmic contact resistance. For the wide bandgap emitter, it has been reported that both InP and InAlAs could be used [27,28], but InP was preferred in this work due to ease of processing. In the case of InP/InGaAs structure, the availability of highly selective etching solutions between InP and InGaAs helps to control the fabrication process.

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The doping and the thickness of InP layer were chosen to minimize the emitter resistance and the emitter-base capacitance while maximizing the reverse breakdown voltage.

From the point of view of f_T , the lower base doping and the thinner base thickness results in higher f_T value. However, the lower base doping can increase the base resistance and reduce f_{max} and power gain. Therefore, a trade-off is necessary. A 50nm Be doped InGaAs layer was used as the base layer in the devices studied. This layer was heavily doped ($2 \times 10^{19} \text{ cm}^{-3}$) to minimize the base resistance and hence improve the device's power gain and f_{max} . The thinner base was employed to minimize the base transit time in order to increase the value of f_T .

The design of the collector layer critically influences the performance potential of the devices. InP was selected for the collector since the use of the wider bandgap InP material could result in a larger Early voltage, which is equivalent to a smaller output conductance, and a higher breakdown voltage. However, due to the large conduction band discontinuity between the InGaAs base and InP collector, InP/InGaAs DHBTs typically suffer from the current blocking effect. To overcome this problem, special collector design such as InGaAs/InP composite collector is used. In this structure, the collector is consisted of two different materials namely the narrow bandgap InGaAs and the wide bandgap InP. A thin layer of InGaAs (40nm) is adjacent to the base layer. A dipole doping (p-type InGaAs with 5nm, and n-type InP with 5nm) is employed at the InGaAs/InP interface to further reduce the current blocking effect. The dipole doping at the InGaAs/InP interface narrows the barrier to

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the point that electrons are able to tunnel through the top part of it. The equilibrium band diagram (from base to collector) shows how the dipole doping at the collector heterojunction alters the barrier to electrons (see Fig.4.2). Thus, in the HBT structure, InGaAs/InP (45/405 nm) composite collector with a dipole-doped interface was used to minimize the conduction band spike hindering the electron transport. A heavily doped ($8 \times 10^{18} \text{ cm}^{-3}$) InP layer was selected for the subcollector to reduce the parasitic collector resistance and improve the device breakdown. The thin InGaAs (30nm) layer serves as the etch stop layer and also provides the collector ohmic contact.

Fig.4.2 Equilibrium band diagram (from base to collector) for the two layer structures showing how the dipole doping at the collector heterojunction alters the barrier to electrons.

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4.3 DC and RF Characterization of InP HBTs

To evaluate the material quality of the MHBTs, comparison of DC performance between MHBTs and LHBTs has been made. Fig.4.3 compares the common emitter I-V characteristics of MHBTs and LHBTs with $5 \times 20 \mu\text{m}^2$ emitter size. The MHBTs shows lower current gain, higher output conductance and higher offset voltage compared to LHBTs. DC parameters of LHBTs and MHBTs are summarized in Table 4.2. The poor performance of MHBTs could be due to the presence of dislocations in the lattice-mismatched epilayers. Fig.4.4 compares the Gummel plots obtained for the MHBTs and LHBTs. The higher ideality factors (Table 4.2) for the MHBTs indicate that further optimization of the material growth is required to improve the material quality. Fig.4.5 compares the DC current gain characteristics of the MHBTs and LHBTs. The MHBTs exhibit a much lower DC current gain in the low collector current region. However, at a higher current of $I_c = 10 \text{ mA}$, the DC gain reaches a value of 106 which is comparable to the referenced LHBTs. Similar LHBTs results have been reported by Liu et al. [29] for LHBTs with the DC current gain of 50, the offset voltage of 0.07V, the ideality factors, (n_c/n_b) of (1.00/1.41) and the breakdown voltage BV_{ceo} of 10V when the base layer was doped at $4 \times 10^{19} \text{ cm}^{-3}$.

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Fig. 4.3 Common emitter I-V characteristics of MHBTs and LHBTs with $5 \times 20 \mu m^2$ emitter size.

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Fig. 4.4 Gummel plots of MHBTs and LHBTs with $5 \times 20 \mu m^2$ emitter size.

Fig.4.5 DC current gain versus collector current of MHBTs and LHBTs.

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For microwave characteristics, on wafer measurements of S-parameters from 1 to 40 GHz using Cascade Microtech Probes and an HP8510 Network Analyzer were used to determine the unity current gain cut-off frequency (f_T) and the maximum oscillation frequency (f_{MAX}) of the devices. Fig. 4.6 shows the current gain ($|H_{21}|$), the maximum available power gain/maximum stable power gain (MAG/MSG) and unilateral power gain as a function of frequency for LHBTs and the MHBTs with $3 \times 5 \mu\text{m}^2$ emitter size. The values of f_T and f_{MAX} were obtained by the extrapolation of $|H_{21}|$ and U using a -20 dB/decade slope. At a collector to emitter (V_{CE}) bias of 2.5 V and a collector current (I_C) of ~3 mA, f_T of 65 GHz, and f_{MAX} of 70 GHz were measured for the LHBTs. The corresponding values obtained for the MHBTs were $f_T = 42$ GHz and $f_{MAX} = 35$ GHz that are found to be comparable to the values obtained for the reference LHBTs. Similar microwave characteristics have been reported for MHBTs using InGaP as the strain relief buffer layer with f_T and f_{MAX} value of 48GHz and 42GHz, respectively [30].

The detailed comparison of DC and RF parameters between LHBTs and MHBTs are listed in Table 4.2. It shows that the MHBTs and LHBTs exhibit comparable DC and RF performances. The difference in performances may be attributed to the buffer layer quality as the device layers grown on the metamorphic buffer are known to exhibit larger surface roughness with high defect density. With continued improvement in the metamorphic growth technique to reduce the surface roughness and the residual strain, the performance of the MHBTs may be expected to be the same as with that of LHBTs.

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(a)

(b)

Fig.4.6 Current gain ($|H_{21}|$), the maximum available power gain/maximum stable power gain (MAG/MSG) and unilateral power gain versus frequency for (a) LHBTs and (b) MHBTs with $3 \times 5 \mu\text{m}^2$ emitter size

Table 4.2 DC and RF parameters of LHBTs and MHBTs

Parameters	LHBT	MHBT
DC gain (maximum)	150	110
BV_{ceo} (V)	11	11
Offset (V)	0.05	0.1
n_c	1.02	1.1
n_b	1.04	1.3
f_T (GHz)	65	42
f_{MAX} (GHz)	70	35

4.4 Mask Design

In order to enhance the RF and microwave performance of InP/InGaAs HBTs, a new nine-level mask set with smaller device structures has been designed for the device fabrication. Trade-offs between the device performance and the process limitation have been taken into account in the mask design. Too complicated design will result in reduced yield and reliability. The determinations of several key geometries in our device design are considered.

Emitter Stripe Width, S_e

The emitter stripe width S_e is a very important geometrical parameter. Selection of S_e has implications on the base resistance, and the emitter and collector capacitances, and hence may affect the device operating frequency as well as the power gain. An optimized maximum frequency of oscillation f_{max} on S_e reported by Gao *et al.* [31] is given by

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$$f_{max} = \frac{1}{2\pi S_e} \sqrt{\frac{nF\sigma_b v_d W_{bop}}{\epsilon\epsilon_o}} \quad (4-1)$$

where σ_b is the base conductivity, v_d is the carrier drift velocity, F is the layout figure of merit, and W_{bop} is the optimum base width. Obviously, the maximum frequency of oscillation increases with the decrease in S_e . In addition, the smaller the value of S_e the smaller will be the base-emitter junction capacitance (C_{be}), which will also improve the device cut-off frequency f_T [32]. Thus, smaller S_e is preferred to improve the device high frequency performance. However, the smallest dimension of the emitter stripe was limited to 1.2 μm in this study due to the current device processing technology capability. Therefore, 1.2 to 2 μm emitter stripe (contact pattern) widths were chosen in the device layout design for comparing the device performance as a function of S_e .

Emitter Finger Length, L_e

The emitter finger length, L_e is primarily determined by the emitter metallization resistance and the junction temperature non-uniformity along the emitter length. Both factors can cause a severe non-uniform distribution of the emitter current along the length. In general, the length and the length-to-width ratio of an emitter finger should not exceed 30 μm and 20-to-1 ratio, respectively in order to minimize the junction temperature and the voltage drop along the length of the finger. From thermal considerations, a power HBT with a larger emitter length results in a higher junction temperature that in turn causes a reduction in the output power density. In the mask design, emitter lengths in the range of 5 to 30 μm were used. The maximum ratio of length-to-width was ~20.

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Emitter Area, A_e

The total emitter area, A_e is determined by the desired output power or the maximum peak collector current. Knowledge of the output power, operating voltage, and the PAE is sufficient to determine this current. In GaAs HBTs, the current crowding effects are reduced substantially by the higher base doping. As calculated by Asbeck and Cheng [33], an emitter utilization factor ($S_{e\text{ eff}}/S_e$) of 95% can be obtained from 2 μm emitter width under 10GHz operating frequency. In this case, the current capability and the output power for HBTs are dependant on the emitter area rather than the emitter periphery. Taking the current non-uniformity into account, the total emitter area A_e is given by [34]:

$$A_e = K \frac{P_{out}}{P_e} \quad (4-2)$$

where P_e is the output power density per unit emitter area, and K is a constant which is larger than unity, depending on the current distribution. In this work, different emitter areas with single and multiple fingers have been included.

Emitter Spacing, S_D

For multi-finger devices, a very important parameter of the layout design is the emitter spacing S_D , the centre distance between two adjacent emitter fingers. A larger S_D results in a higher base resistance and capacitance, both of which degrade the f_{max} and the power gain. On the other hand, a larger S_D reduces the peak value of junction temperature at a given power dissipation. The trade-off on the frequency performance and the junction temperature should be considered in deciding S_D [35]. The smallest dimension for S_D is also limited by the device technology and the processing

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limitations, such as device structures and lithography alignment tolerance, S_D values ranging from $6\mu\text{m}$ to $11\mu\text{m}$ have been used in the layout.

All the key geometric parameters discussed must be optimized as a part of the overall design for high frequency HBTs. In general, the frequency performance, operating voltage and power gain are given importance. Further, trade-offs between the device layout design and the process limitation must also be made to achieve reasonable device performance and yield. Fig.4.7 shows the layout for a self-aligned single emitter HBT with $1.2 \times 20 \mu\text{m}^2$ emitter size. More than 150 HBTs including the structures for process monitoring were laid out in a $6.5 \times 5.0 \text{ mm}^2$ die. The plot of this die is shown in Fig. 4.8.

Fig.4.7 The layout of a self-aligned single emitter HBT with $1.2 \times 20 \mu\text{m}^2$ emitter size.

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Fig.4.8 The plot of a single die-layout on Mentor Graphics IC station.

Chapter 5

Characterization of MHBTs Grown by Gas and Solid Source MBE

5.1 Introduction

InP/InGaAs metamorphic HBTs were first demonstrated by Wang et al. [3] using solid-source molecular beam epitaxy (MBE) techniques in 2000. In that work, InGaP linearly graded buffer was used between the GaAs substrate and the InP based device structure. Using the solid-source MBE technique, Kim et al. [36] have reported very high f_T and f_{MAX} values of 200GHz for MHBTs with C-doped InGaAs base. MHBTs grown by gas-source MBE system using InAlAs linearly graded buffer have been investigated by Lefebvre et al. [37].

In this work, the same MHBTs layer structures grown by two different growth techniques, gas- and solid-source molecular beam epitaxy (MBE), have been studied and the DC and RF performance are compared. The device structures were grown on GaAs substrates and the metamorphic buffer layer used was linearly graded InAlGaAs.

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5.2. Material Growth and Device Structure

The MHBt structures were grown by molecular beam epitaxy (MBE) on semi-insulating (100) GaAs substrates. The samples were grown using Riber gas source MBE and solid source MBE systems. In GSMBE system, arsenic and phosphorus species were generated by cracking gaseous AsH_3 and PH_3 , respectively. In SSMBE system, valved phosphorus (P) cracker cell and the classic arsenic (As) effusion cell were employed to obtain these species. Si and Be were used as the n- and p-type dopants, respectively. The detailed layer structure of the MHBtS studied is given in Table 5.1. Two identical structures using 1.3 μm linearly graded InGaAlAs as the metamorphic buffer were produced using two different MBE growth techniques - solid-source MBE and gas-source MBE. The key features of this structure include a thin InGaAs base (50 nm) with a designed Be-doping concentration of $2 \times 10^{19} \text{ cm}^{-3}$ and an InGaAs/InP (450 nm) composite collector with the dipole-doped interface. The collector thickness and the doping were optimized to improve the device breakdown.

Table 5.1 Layer structure design of the metamorphic InP/InGaAs DHBt

Layer Structure		
Emitter Cap	InGaAs:Si (2×10^{19})	2000 Å
	InP:Si (5×10^{18})	500 Å
Emitter	InP:Si (4×10^{17})	1000 Å
Base	InGaAs:Be (2×10^{19})	500 Å
Collector	InGaAs:Si (1×10^{16})	400 Å
	InGaAs:Be (1×10^{18})	50 Å
	InP:Si (1×10^{18})	50 Å
	InP:Si (1×10^{16})	4000 Å
	InGaAs:Si (8×10^{18})	300 Å
	InP:Si (8×10^{18})	5500 Å
Buffer	InAlAs	3000 Å
	InGaAlAs	1.3 μm
	GaAs	500 Å
GaAs (100) S. I. Substrate		

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Device fabrication consists of emitter, base and collector mesa formation followed by ohmic metallization, air-bridge pillar development, interconnection, and finally passivation of the devices. Ti/Au was used for n- and p-type ohmic contacts. Device isolation was achieved by wet mesa etching, and gold-plated air-bridges were used to connect the emitter, base and the collector contacts to the probe pads. The detailed device fabrication has been discussed in Chapter 3. Devices described in this chapter have been fabricated using the new mask set designed as discussed in Chapter 4. A MHBТ fabricated with $1.6 \times 10 \mu\text{m}^2$ emitter size is shown in Fig. 5.1.

Fig. 5.1 SEM picture of a fabricated InP MHBТ with $1.6 \times 10 \mu\text{m}^2$ emitter size.

5.3 Results and Discussion

Fig.5.2 and Fig. 5.3 compare the common emitter I-V characteristics and DC current gain versus collector current of MHBTs grown by solid- and gas-source MBE techniques, respectively. The MHBTs grown by solid-source MBE exhibit lower current gain, breakdown voltage and offset voltage compared to the MHBTs grown by gas-source MBE. They also exhibit higher ideality factors as indicated by the Gummel plots shown in Fig. 5.4. The detailed results can be found in the Table 5.2.

Fig. 5.2 Common emitter I-V characteristics of MHBTs grown by solid- and gas-source MBE techniques with $1.6 \times 20 \mu\text{m}^2$ emitter size.

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Fig. 5.3 DC current gain versus collector current of MHBTs grown by solid- and gas-source MBE techniques with $1.6 \times 20 \mu\text{m}^2$ emitter size.

Fig. 5.4 Gummel plots of MHBTs grown by solid- and gas-source MBE techniques with $1.6 \times 20 \mu\text{m}^2$ emitter size.

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Fig. 5.5 (a) shows the current gain ($|H_{21}|$), maximum available power gain/maximum stable power gain (MAG/MSG) and unilateral power gain vs. frequency for an MHBTS grown by solid-source MBE. At a collector to emitter bias V_{CE} of 1.5 V and a collector current I_C of ~9 mA, f_T and f_{MAX} of 62 GHz and 72 GHz, respectively were determined for this MHBTS. However, the corresponding values obtained for MHBTS grown by gas-source MBE at the same biasing conditions were found to be lower with $f_T = 57$ GHz and $f_{MAX} = 41$ GHz as shown in Fig. 5.5 (b). The highest f_T and f_{MAX} values of 200GHz has been reported by Kim et al. [36] for MHBTS with a higher base doping concentration of $4 \times 10^{19} \text{ cm}^{-3}$. Moreover, the emitter area of the MHBTS in their study was $3 \mu\text{m}^2$ that is about ten times smaller compared to $32 \mu\text{m}^2$ in this study. However, the values of DC current gain, β and the breakdown voltage, BV_{ceo} are higher in this investigation (Table 5.2) compared to 27 and 6V, respectively [36].

The noise performance is measured using the ATN automated noise-pull system (NP5). Fig.5.6 (a) shows the minimum noise figure (NF_{min}) and the associated gain (G_{ass}) versus frequency in the range of 4 to 18 GHz for a $1.6 \times 20 \mu\text{m}^2$ MHBTS grown by solid-source MBE at $I_C = 0.9$ mA and $V_{CE} = 2$ V. The device exhibits an NF_{min} value of ~1.92dB and a G_{ass} value of ~11dB at 4 GHz. Similar performances were obtained for the devices grown by gas-source MBE as shown in Fig.5.6 (b): an NF_{min} value of ~1.99dB and a G_{ass} value of ~12dB at 4 GHz. These noise results are comparable to the InP LHBTs reported by Hsu and Pavlidis with the NF_{min} value of ~1.55dB at 6GHz [38].

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(a)

(b)

Fig. 5.5 Microwave performance of a MHBТ ($1.6 \times 20 \mu\text{m}^2$ emitter) grown by (a) solid-source MBE and (b) and gas-source MBE.

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(a)

(b)

Fig. 5.6 The minimum noise figure (NF_{min}) and the associated gain (G_{ass}) versus the frequency for a MHBTS grown by (a) solid-source MBE and (b) gas-source MBE with $1.6 \times 20 \mu m^2$ emitter size.

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Microwave power performance of $1.6 \times 20 \mu\text{m}^2$ devices was measured on wafer using ATN load-pull system (LP1) under class-A bias of $I_c = 9 \text{ mA}$ and $V_{ce} = 3 \text{ V}$. When tuned for the maximum power at 8 GHz, a maximum output power of 11 dBm was obtained with a small signal gain of 12 dB and a power-added efficiency (PAE) of 43 % for the MHBTs grown by solid-source MBE, as shown in Fig. 5.7 (a). These values are comparable to the reported results for MHBTs grown on InGaP linearly graded buffer with a maximum output power of 12 dBm, a small signal gain of 10 dB and a power-added efficiency (PAE) of 43 % [30]. The output power in our case is mainly limited by the device on-state breakdown, and can be improved by using a thicker collector layer. MHBTs grown by gas-source MBE also showed similar performance as plotted in Fig. 5.7 (b). A maximum output power of ~35 mW was obtained for four emitter finger MHBTs of $1.6 \times 20 \mu\text{m}^2$ emitter area each when tuned for the maximum power at 8 GHz.

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(a)

(b)

Fig. 5.7 The microwave power performance of a MHBТ grown by (a) solid-source MBE and (b) gas-source MBE with $1.6 \times 20 \mu\text{m}^2$ emitter size.

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The DC and RF performances measured for the devices with the emitter size of $1.6 \times 20 \mu\text{m}^2$ are summarized in Table 5.2. Some variation in terms of DC and RF characteristics were observed between the devices grown by two different growth techniques. It may be noted that the DC current gain is found to be higher and the f_{MAX} lower for MHBTs grown by gas-source MBE. This may be attributed to the variation in the actual base doping concentration in the device, although the designed value of $2 \times 10^{19} \text{cm}^{-3}$ was kept the same during the growth of the two structures.

The difference in the base doping concentration between these two structures has been confirmed by measuring the base sheet resistance using the TLM method. The devices grown by gas-source MBE exhibits higher sheet resistance of $640 \Omega/\text{sq}$ due to the lower doping concentration compared to the layer structures grown by solid-source MBE with a lower sheet resistance of $440 \Omega/\text{sq}$. This is consistent with the higher DC gain measured for the gas-source grown samples. The lower doping concentration in these devices may result in lower base bulk recombination providing higher DC current gain. On the other hand, the higher base resistance may cause the degradation of the device microwave performance such as f_{MAX} as summarized in Table 5.2.

Nevertheless, the figures of merit for these two MHBTs such as the product of DC current gain and the maximum oscillation frequency ($\beta \times f_{\text{MAX}}$) which are governed by the base quality and the base doping concentration, and the product of the common emitter breakdown voltage and the unity current gain cut-off frequency ($BV_{\text{ceo}} \times f_T$)

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which are related to the thickness variation are similar. This suggests that both the solid-source and the gas-source MBE techniques may offer similar material quality for the devices. Hence, higher device performances could be achieved by proper optimization of the material growth conditions and the layer structure.

Table 5.2 DC and RF parameters of MHBTs ($1.6 \times 20 \mu\text{m}^2$)

	Gas-source	Solid-source
DC gain (maximum)	160	90
BV_{ceo} (V)	11	9.3
Offset (V)	0.08	0.05
n_c	1.01	1.01
n_b	1.26	1.45
f_T (GHz)	57	62
f_{MAX} (GHz)	41	72
$BV_{CEO} \times f_T$ (V•GHz)	627	577
$\beta \times f_{MAX}$ (GHz)	6560	6480
Min noise figure @ 4GHz (dB)	1.99	1.92
Power @ 8GHz (dBm)	11	11
PAE @ 8GHz	42%	43%

5.4 Summary

High performance InP-based metamorphic heterojunction bipolar transistors (MHBTs) grown by solid- and gas-source MBE techniques have been fabricated and characterized. DC and RF characteristics including microwave noise and power performances of the devices are reported and the figures of merit of these devices are

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compared. Some differences in the DC and RF performances of MHBTs grown by these two techniques have been observed. However, they are found to be more related to the difficulty in achieving the designed layer parameters rather than the growth technique itself. This suggests that both the solid-source and the gas-source MBE techniques may offer similar material quality, and hence higher device performances could be achieved by proper optimization of the material growth conditions.

Chapter 6 DC Characterization of MHBTs at Elevated Temperature

Chapter 6

DC Characterization of MHBTs at Elevated Temperature

6.1 Introduction

Studies on the temperature dependence of electrical characteristics of devices are important to understand the transport properties and assess the material quality. Investigations on the AlGaAs/GaAs HBTs [39] and the carbon-doped InP/InGaAs HBTs [40] have been reported. Elevated temperature measurements are particularly significant for the metamorphic HBT device structures grown on mismatched substrates. However, there are no reports available on the DC characterization of MHBTs investigated at elevated temperatures.

In this study, a detailed DC characterization of metamorphic InP/InGaAs/InP DHBTs in the temperature range of 300 K to 400 K was carried out and the carrier transport properties were investigated. Our experiments reveal that band-to-band recombination is the dominant mechanism for the base current indicating the good base material quality for the metamorphic HBT structures.

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6.2 Experiments

The growth of InP/InGaAs MHBTS layer was carried out in a Riber 32P MBE system equipped with a Riber KPC250 valved phosphorus (P) cracker cell and a Riber VAC500 valved arsenic (As) cracker cell. The substrates used were semi-insulating (100) GaAs substrates. The detailed growth information can be found elsewhere [12]. The buffer layer consists of a 1000 Å GaAs layer, a 1.5 µm linearly grading In_xGa_{1-x}P (x varying from 0.48 to 1) layer and a 500 Å InP layer.

The detailed layer structure of the MHBTS device is given in Table 6.1. The key features of this structure include a thin InGaAs base (50 nm) doped at 2×10¹⁹ cm⁻³ with Be and an InGaAs/InP (350 nm) composite collector with dipole-doped interface which was used to improve the device base-collector junction breakdown. The devices used for testing were of mesa-type structures with self-aligned base electrodes.

Table 6.1 Layer structure of the metamorphic InP/InGaAs DHBT

Emitter Cap	InGaAs:Si (2 × 10 ¹⁹)	1000 Å
	InP:Si (2 × 10 ¹⁹)	600 Å
Emitter	InP:Si (3 × 10 ¹⁷)	900 Å
Base	InGaAs:Be (2 × 10 ¹⁹)	500 Å
Collector	InGaAs:Si (5 × 10 ¹⁵)	400 Å
	InGaAs:Be (1 × 10 ¹⁸)	100 Å
	InP:Si (1 × 10 ¹⁸)	100 Å
	InP:Si (5 × 10 ¹⁵)	2900 Å
	InP:Si (5 × 10 ¹⁸)	80 Å
	InGaAs:Si (5 × 10 ¹⁸)	4500 Å
Buffer	InP	500 Å
	In _{0.48} Ga _{0.52} P → InP	1.5 µm
	GaAs	1000 Å
GaAs (100) S. I. Substrate		

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The temperature dependence of the device DC characteristics was measured using a Cascade probe station with a thermal chuck and an HP4156 Semiconductor Parameter Analyzer. The temperature was monitored at the surface of the hot plate and the samples were protected by N₂ ambient during the test. Devices with (5×10) μm² emitter size were chosen for the measurements.

6.3 Results and Discussion

Fig.6.1 shows the common emitter I_C - V_{CE} characteristics of a typical MHB device measured at 300K. The common-emitter off-state break down voltage (BV_{CEO}) was higher than 9 V, and the base-collector junction breakdown voltage (BV_{cbo}) was about 13.5 V. The device shows good I-V characteristics with a low leakage current. The off-state current (I_{CEO}) at $V_{CE} = 8$ V was only about 75 μA. This could be attributed to the low junction leakages (Inset of Fig.6.1). In fact, the base-collector (B-C) and the base-emitter (B-E) junction leakage currents for the MHBs were only slightly higher than those measured from the LHBs grown and fabricated using the same facilities and process conditions. The device showed a relatively high output conductance and high offset voltage (0.5 V). Similar results were observed for the referenced LHBs, suggesting that the high output conductance and the high offset voltage are not due to the use of metamorphic structure. The poor output conductance requires optimization of the thickness of InGaAs/InP composite collector [41]. The large offset voltage obtained is due to the asymmetry of the emitter-base and base-collector junction [42]. This can be confirmed by the measurement of the base-emitter and base-collector junction characteristics as given in the inset of Fig. 6.1.

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The devices used for characterization exhibit a peak DC gain, β over 100. Fig.6.2 plots β versus base doping concentration for both the metamorphic and the lattice-matched devices obtained using different growth techniques [43,44,45,46]. The base thickness of the transistors is about 50 nm. The β of the MHBt reported in this work is close to those reported for the lattice-matched HBTs with similar base thickness and doping concentration.

Fig.6.1 Common-emitter characteristics of the MHBt with a $5 \times 10 \mu\text{m}^2$ emitter. Inset: Emitter and collector junction current-voltage characteristics for the same device.

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Fig.6.2 DC current gain versus base doping concentration for metamorphic and lattice-matched HBT devices obtained using different growth techniques.

A plot of the current gain, β versus collector current, I_c at different temperatures is shown in Fig. 6.3. The decrease of β with the increase in temperature occurs only in the low collector current regime. It is similar to reported data for InP/InGaAs LHBTs by Liu et al. [47] where β exhibited a very weak dependence on temperature ranging from about 300K to 470K, decreasing slightly at low current levels and remaining essentially constant at high current levels.

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Fig. 6.3 Current gain, β versus collector current, I_c at different temperatures for the MHBT.

Base-emitter (B-E) and base-collector (B-C) junction characteristics measured at different temperatures are given in Fig.6.4. The temperature dependence behavior was found to be similar for both B-E and B-C junctions. As the temperature is increased, the increase of the junction reverse leakage current can be observed. However, no significant change of bias sensitivity of the leakage current was found which indicates that the dominant transport mechanism for the junction reverse current was not changed in this temperature range. Similar results have also been reported for InP/InGaAs LHBTs [47].

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(a)

(b)

Fig6.4 (a) Base-emitter and (b) base-collector junction characteristics measured at different temperatures.

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To understand the properties of carrier transport in the MHBTs, and further assess the material quality, Gummel plots obtained at different temperatures have been analyzed for a $5 \times 10 \mu\text{m}^2$ device as shown in Fig.6.5. As the temperature is increased, the base-emitter turn-on voltage largely decreases, and the crossover of the base and collector currents remains low. No obvious changes of base and collector ideality factors were observed.

Fig.6.5 Gummel plots for a $5 \times 10 \mu\text{m}^2$ device at different temperatures.

To study the carrier transport in the device, collector and base currents in Gummel plots at different temperatures were extrapolated to $V_{BE} = 0 \text{ V}$ to obtain the values of I_{C00} and I_{B00} [48]. Activation energy plots for the collector and the base current [$\log I_{C00}$ (or $\log I_{B00}$) versus $1/T$] are shown in Fig.6.6. For the collector current, an E_a of 1.1 eV was obtained that may indicate the presence of the electron

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injection by thermionic emission as the value is close to the sum of the bandgap energy for InGaAs ($E_{g \text{ InGaAs}} = 0.75 \text{ eV}$) and the conduction band discontinuity ($\Delta E_C = 0.22 \text{ eV}$). As for the base current, $E_a = 0.8 \text{ eV}$ was obtained which is close to the band gap energy of the InGaAs base, indicating that, in this temperature range, the band-to-band recombination plays a dominant role in determining the base current. No trap-related recombination was observed for the base and the collector currents, which further indicates that the metamorphic HBT structures grown by SSMBE have good material quality and it is comparable to the LHBTs.

Fig.6.6 Activation energy plots for collector and base currents extrapolated to $V_{BE} = 0 \text{ V}$.

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6.4 Summary

In conclusion, the temperature dependence of the DC characteristics for a high gain metamorphic InP/InGaAs HBT on GaAs substrate has been investigated. The device transport properties were studied to assess the material quality. The experimental results suggest that, in the temperature range of 300 to 400 K in which the devices are commonly operated, the band-to-band recombination plays a dominant role in determining the base current. No trap-related recombination was observed for the base and the collector currents indicating that the metamorphic HBT structures grown by solid source MBE can offer good device quality material.

Chapter 7

Study on Device Stability of MHBTs

7.1 Introduction

Metamorphic HEMTs (MHEMTs) biased at low current and voltage for low noise applications have been shown to be reliable, and the mean-time to failure (MTTF) exceeding 10^6 hours at a channel temperature of 125°C has been achieved, which is comparable to that of lattice matched HEMTs on InP substrates [49]. In the case of metamorphic HBTs (MHBTs), DC and microwave performances comparing to that of the lattice-matched InP HBTs (LHBTs) on InP substrate have been demonstrated as discussed in Chapter 4.

However, compared to HEMTs, HBTs could be more sensitive to structural defects as they are minority carrier devices. For example, the early reliability study on AlGaAs/GaAs lasers (which is also a minority carrier device) on Si substrate indicated that the rapid formation and propagation of dark line defect could cause significant degradation of the device performance preventing the stable CW lasing operation, which is critical for practical applications. The fast degradation has been observed at a current density as low as $1\text{kA}/\text{cm}^2$ [50]. The residual strain in the device active layer could accelerate the defect generation and propagation [51]. Thus, for the

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MHBTs with a compositionally graded strain relief buffer layer, the temperature and the bias stability have become the important issues for practical system applications.

In general, the device layers grown on metamorphic buffer exhibit larger surface roughness with high defect density. Monitoring and controlling of the material quality is important to achieve high performance. This is particularly true for the HBT structure. However, unlike HEMT structures where the material quality can be quickly assessed by the conventional hall mobility measurement, characterization techniques for HBT structures are limited. In this work, both the optical and the electrical characterizations such as photoluminescence (PL) and low frequency noise measurements have been performed on different MHBTs under high current density at high junction temperature stress to understand the correlation between these parameters and the device performance. The structural stability of the MHBTs subjected to rapid thermal annealing (RTA) has also been investigated by PL. The experimental results obtained from the optical and electrical characterizations have been correlated.

7.2 Experiments

The MHBTs used in this work were grown by solid-source molecular beam epitaxy (SSMBE) on semi-insulating (100) GaAs substrates. The optimization of the growth condition for the metamorphic buffer layer was targeted to achieve low surface roughness and residual strain. MHBT devices were fabricated using wafers grown with different growth conditions for the metamorphic buffer scheme.

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The devices used for bias-stress tests were mesa type structures with self-aligned base electrodes as discussed in Chapter 3. All the devices exhibited DC performance with the current gain, β in the range of 30 to 60 and a common emitter breakdown voltage of ≈ 9 V.

The bias-temperature stress tests were conducted using an HP4156 semiconductor parameter analyzer with a cascade probe station and a thermal chuck as discussed in Chapter 6. Both MHBTS and the reference LHBTS with $5 \times 10 \mu\text{m}^2$ emitter were chosen for the stress tests. The reference LHBTS used were with the same device layer structure and were fabricated in the same process run. Stress current density of 100 kA/cm^2 was chosen, which is much higher than 25 kA/cm^2 required for normal device operation, to shorten the stress time so that the stress tests could be performed at wafer level without using any package. In this case the results can be obtained in a few hours [52]. The junction temperature (250°C) was estimated using the method suggested by Bovolon [53]. The junction temperature T_j can be determined from:

$$T_j = T_{amb} + R_{th} \cdot I_c \cdot V_{ce} \quad (7-1)$$

where T_{amb} is the ambient temperature, R_{th} is the thermal resistance of the device.

The PL measurements in this work were carried out using a SPEX 750M system with an Ar+ laser excitation source with the excitation power density of $\sim 5 \text{ W/cm}^2$ and the wavelength is 514 nm. The PL spectra were detected using a liquid

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nitrogen cooled germanium detector with a 1200 gr/mm grating spectrometer. The samples measured in a vacuum chamber can be cooled down to 4 K.

7.3 Results and Discussion

Fig.7.1 plots the collector currents of a typical MHBT and the reference LHBT over the stress period of 3600 seconds at a temperature of 150 °C. It can be seen in Fig.7.1 that both the devices show similar degradation behavior where the decrease of the collector current gets saturated within the initial tens of seconds. The initial degradation in the current density may be attributed to the process-induced defects that had already been incorporated in the devices during the material growth or the device fabrication. The decrease of the collector current for the MHBT and the LHBT after 1-hour stress was about 4.9% and 3.8%, respectively.

Fig.7.1 Collector current density as a function of current stress time at a constant I_B for a typical MHBT and a LHBT.

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Fig.7.2 shows the typical Gummel plots before and after the stress. Only a slight increase in the base and the collector currents in the low current and low base-emitter voltage region can be observed. Both the MHBTs and the reference LHBTs show similar behavior indicating that no additional degradation mode can be found for the MHBTs.

Fig.7.2 Comparison of Gummel plots for a MHBT and a LHBT before and after the bias-temperature stress.

Fig.7.3 compares the effect of stress tests on the current gain as a function of collector current for the MHBT and the LHBT. The decrease of β due to the bias-temperature stress occurs only in the low collector current regime. The change of the current gain at collector currents higher than 1mA is negligible. The modification of the common-emitter I-V characteristics for a MHBT induced by the stress is shown in Fig.7.4. Only slight changes on the I-V characteristics can be observed.

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Fig.7.3 Current gain β , versus collector current I_C , for a MHBT and a LHBT before and after stress.

Fig.7.4 Comparison of common-emitter I-V characteristics for the MHBT before and after the stress.

Chapter7 Study on Device Stability of MHBTS

To investigate the impact of optimization of the strain relief buffer and the layer structures on the device bias-temperature stability, MHBTS with the metamorphic buffer layer grown using a different set of growth conditions and layer structures (MHBT_B) have also been chosen for the stress tests. The details layer structure of MHBT_B has been shown in Table 6.1. The growth was carried out in a Riber 32P MBE system equipped with a Riber KPC250 valved phosphorus (P) cracker cell and a Riber VAC500 valved arsenic (As) cracker cell. Si and Be were used as the n- and p-type dopants, respectively. The study was basically initiated to understand the capability of low frequency noise and PL measurements to distinguish the material quality between different devices. Thus, it should be noted that MHBT_B device structure studied was not fully optimized in term of growth conditions because it was the first metamorphic HBT sample grown by solid-source MBE in our lab. The surface roughness of this structure was also higher than that for MHBT_A.

Although the initial current gain for MHBT_B is similar to that of MHBT_A, the MHBT_B typically shows a fast degradation of the collector current (current gain) during the stress. More than 40% decrease in the collector current was observed in the stress duration of 2000 seconds as shown in Fig.7.5. The fast degradation of MHBT_B could be due to the degradation of device junction quality during the stress.

Fig.7.6 shows the comparison of Gummel plots for the MHBT_B before and after the stress. It can be seen that the device exhibits a significant increase in I_B and decrease in I_C that results in the large decrease of the current gain. Moreover, after one hour of stressing, the base ideality factor has increased from ~ 1.4 to ~ 1.7

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indicating the increase in trap-related recombination. A fundamental understanding on the degradation mechanism however requires further studies. It should be pointed out that similar stress tests have been conducted on the metamorphic high electron mobility transistors (MHEMTs) grown on the buffer that is the same as the one used for MHBT_B. However, no significant degradation during the bias-temperature stress has been observed. This result suggests that compared to MHEMTs, the growth of high quality metamorphic buffer is more critical for the stability of MHBTs.

Fig.7.5 Stress current behavior of MHBT_A and MHBT_B.

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Fig.7.6 Comparison of Gummel plots for MHBT_B before and after stress.

Low frequency (LF) noise is one of the important parameters for heterojunction bipolar transistors (HBTs). It has been found that the device LF noise is extremely sensitive to both the surface and the bulk defects in HBTs, which make the LF noise measurements as a tool for monitoring the device quality. Recent studies on GaAs-based single HBTs indicate that the base noise spectral density at low frequency can be correlated to the device long-term reliability, Thus, the LF noise measurement can serve as a cost-effective technique of screening HBTs [54]. In this work, the LF noise characteristics of MHBTs have been reported for the first time. Base noise spectra, $S_{IB}(f)$ measured for the two different MHBT devices in the frequency range of 1 Hz to 2 kHz at the same current density are plotted in Fig.7.7 along with the data for the referenced LHBT for comparison. Both MHBT_A and

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LHBT show similar noise behavior with an $1/f^{0.98}$ dependence in the frequency range of 1 Hz to 2 kHz. The LHBT shows a slightly lower noise level. Much higher noise level with an $1/f^{1.1}$ dependence was observed for MHBT_B. The $1/f$ noise level of MHBT-A is found to be comparable to that measured from the referenced InP LHBTs, which suggests that MHBT device structures with comparable material quality to that of LHBTs could be achieved by using optimized strain relief buffer layer and the layer structures.

Fig.7.7 Comparison of base noise spectrum, $S_{IB}(f)$, for different devices in the frequency range of 1 Hz to 2 kHz. The devices have the emitter size of $100 \mu m^2$.

To investigate whether the difference in the material quality can be detected by PL measurements, low temperature PL measurement was performed on the

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samples. The InGaAs cap layer was removed by selective etching prior to PL measurements to avoid emission from the cap region. Fig.7.8 shows the PL spectra obtained for different wafers. The referenced LHBT structure presents three distinct emissions. The strong emission at 0.77 eV is attributed to the emission from the InGaAs base, and the two broad emissions at the higher energy side of the base emission are related to the emission from the InP/InGaAs emitter-base interfacial layer. This was confirmed by comparing the PL spectra measured from a sample by slowly etching away the InP emitter. The etch solution had high selectivity between InP and InGaAs ensuring that no over etching of InGaAs base occurs. It was found that both broad peaks were disappeared simultaneously when the InP emitter layer was fully removed. Unlike the case of the referenced LHBT, only the two high-energy peaks were observed for MHBTA and MHBTB as shown in Fig 7.8. From the PL spectra obtained from the as-grown samples, it is difficult to make a straightforward justification on the material quality. However, the variation of the optical properties in the samples that underwent RTA processes can be sensed by PL measurements.

Fig.7.9 compares the normalized PL intensities for the three different structures studied. The intensities of the higher energy peak located at ~0.86 eV were used for comparison for all the devices since the strong peak at 0.77 eV from the InGaAs base was only detected for the LHBT. The corresponding emissions from the MHBTS were very weak (Fig.7.8). It can be seen that, after annealing at 650 °C for 10 s, more than 80% decrease in the PL intensity was observed for the MHBTB structure, while LHBT and MHBTA showed ~40% and ~50% decrease in PL intensity, respectively. It is generally admitted that the decrease in the PL intensity is

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associated with the deterioration of the material quality. Larger variation of PL intensity observed on MHBT_B suggests a relatively lower thermal stability for the MHBT_B structure. Similar to the electrical stress tests, the MHBT_B shows a faster degradation compared to the other two samples.

Fig. 7.8 PL spectra obtained at 10 K for different MHBT structures and the referenced LHBt structure.

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Fig.7.9 Comparison of normalized PL intensities for the MHBTA and LHBT structures subjected to RTA for 10 s at different temperatures.

7.4 Summary

Stress tests on MHBTA and reference LHBTs were carried out under high current density at high junction temperature. PL characterization and electrical tests including low frequency noise measurements were performed on MHBTA structures, and particular attention was paid on the device stability. The experimental results show that InP MHBTA grown on GaAs substrate with the optimized strain relief buffer layer are as stable as that grown on lattice-matched InP substrates indicating the absence of defect generation and propagation in the MHBTA. These promising results indicate that, by proper growth optimization of the strain relief buffer layer, MHBTA on GaAs substrate with the electrical stability similar to that of HBTs on InP substrate could be achieved. For the MHBTA with the fast degradation during the electrical stress, accelerated by the increase of junction temperature, a high low- frequency base

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noise was measured. The same structure also showed relatively poor PL properties when subjected to RTA process in the temperature range of 350 to 650 °C. Good correlation between the optical and the low frequency noise measurements, and the device degradation during the electrical stress may provide important means to assess the device stability of MHBTs. The optimization of the strain relief buffer is believed to be the most critical step to achieve high device stability in addition to proper layer structure design.

Chapter 8 Thermal Properties of MHBTs Using Different Metamorphic Buffer Layer

Chapter 8

Thermal Properties of MHBTs Using Different Metamorphic Buffer Layer

8.1 Introduction

As discussed in earlier Chapters, MHBTs on GaAs substrates with good DC and microwave performances comparable to conventional lattice-matched structures on InP can be achieved. However, one of the important issues in the metamorphic technology is the relatively high thermal resistance of the buffer layer, which may potentially limit the device power performance. The thermal resistance of an HBT is determined by the thermal resistance of the layer underneath the collector such as the subcollector, and the buffer layers as well as the substrate. For the MHBTs, the low substrate thermal conductivity of GaAs ($0.44 \text{ W/cm}\cdot\text{K}$) compared to InP ($0.68 \text{ W/cm}\cdot\text{K}$) could result in devices with high thermal resistance. More importantly, ternary or quaternary III-V compounds [55] are widely used as the metamorphic buffers. The significant decrease in the thermal conductivity caused by the alloy-disorder scattering due to the random distribution of group III (and/or V) atoms in the cationic (and/or anionic) sublattices in the ternary or quaternary buffer may play a dominant role in determining the device thermal resistance. Defects and dislocations in a layer may cause Rayleigh scattering of phonons and thereby greatly reduce the

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thermal conductivity of the materials [56,57]. For the metamorphic buffer layer, it remains unknown whether the presence of a large amount of dislocations within the buffer layer significantly reduces the material thermal conductivity.

Different III-V compounds have been considered for strain-relief buffer layers in the development of metamorphic HBTs. Kim et al [58] have compared the thermal properties of MHBTs using $\text{In}_x\text{Al}_{1-x}\text{P}$ and InP as the buffer layer. A much lower thermal resistance has been observed in the metamorphic HBTs using a uniform InP buffer and this could be attributed to the high thermal conductivity of the InP material. The thermal conductivities of other materials such as AlGaAsSb and InAlAs [55], which may potentially serve as metamorphic buffer layer materials for HBTs, have the effective thermal conductivity values of at least three times lower than that of InP. InP metamorphic buffer directly grown on GaAs substrate may provide a significant advantage. However, the direct growth of InP on GaAs may result in certain limitations such as high surface roughness [4] and high defect density [59] in the buffer layer and the device structure.

In this work, the thermal properties of metamorphic InP/InGaAs HBTs on GaAs substrates using a linearly graded InGaP buffer are investigated. The motivations for the use of InGaP as a strain-relief buffer are as follows: (1) Using InGaP instead of InP as the buffer may provide more freedom to improve the metamorphic buffer through compositional grading [60]; (2) As it has been pointed out by Kim *et al* in the case of InAlP [58], the use of InGaP as the metamorphic buffer results in the upper portion of the buffer (the region closed to the collector)

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composed of material with a high indium composition (almost pure InP). This consequently lowers the overall thermal resistance as compared to the conventional InAlAs scheme; (3) A higher thermal conductivity (~ 0.16 W/cm $\cdot$ K) with a factor of 3 to 4 observed in $\text{In}_{0.5}\text{Ga}_{0.5}\text{P}$ [61] compared to other ternary materials such as $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (0.044 W/cm $\cdot$ K) [62] may result in less degradation of thermal properties. As discussed later in this Chapter, InGaP indeed causes a large reduction of device thermal resistance compared to the conventional InAlAs approach. The experimental results are quantitatively interpreted using a simple heat transfer model assuming the thermal conduction through the substrate being the dominant heat transfer mechanism in the given devices.

8.2 Experiments

The InP/InGaAs HBTs used in this work were grown on both semi-insulating (100) InP and GaAs substrates by solid-source molecular beam epitaxy (SSMBE). Silicon and carbon were used for the n- and p-type dopants respectively. The devices were fabricated using a triple-mesa isolation process with self-aligned base electrodes as discussed in Chapter 3. The MHBs on GaAs are with identical layer structures and geometries as that of lattice-matched HBTs (LHBTs) grown on InP substrate except that the linearly graded metamorphic buffer ($\text{In}_x\text{Al}_{1-x}\text{As}$ or $\text{In}_x\text{Ga}_{1-x}\text{P}$) was grown between the sub-collector and the GaAs substrate. The 250 nm InAlAs layer between the subcollector and the metamorphic buffer (or InP substrate) served as a growth buffer as well as an etch stop layer. Both $\text{In}_x\text{Al}_{1-x}\text{As}$ and $\text{In}_x\text{Ga}_{1-x}\text{P}$ buffers showed the typical cross-hatched surface morphology with the RMS roughness of ~ 4

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and 6 nm, respectively. These values are lower than the one (~10 nm) reported for InP metamorphic buffer [59]. Table 8.1 shows the detailed layer structure of the MHBTs and the control sample of lattice-matched InP HBT used for the characterization of the thermal resistance, R_{th} .

Table 8.1 Layer structure of MHBTs on GaAs substrate and referenced LHBTs on InP

Emitter Cap	InGaAs	200 nm	n-type	$2 \times 10^{19} \text{ cm}^{-3}$
	InAlAs	50 nm	n-type	$5 \times 10^{18} \text{ cm}^{-3}$
Emitter	InAlAs	100 nm	n-type	$4 \times 10^{17} \text{ cm}^{-3}$
Base	InGaAs	50 nm	p-type	$\sim 4 \times 10^{19} \text{ cm}^{-3}$
Collector	InGaAs	40 nm	n-type	$1 \times 10^{16} \text{ cm}^{-3}$
	InGaAs	10 nm	p-type	$1 \times 10^{18} \text{ cm}^{-3}$
	InP	10 nm	n-type	$1 \times 10^{18} \text{ cm}^{-3}$
	InP	390 nm	n-type	$1 \times 10^{16} \text{ cm}^{-3}$
Subcollector	InGaAs	30 nm	n-type	$8 \times 10^{18} \text{ cm}^{-3}$
	InP	250 nm	n-type	$8 \times 10^{18} \text{ cm}^{-3}$
InAlAs Buffer	InAlAs	250 nm	Undoped	
Metamorphic Buffer	$\text{In}_{0.52}\text{Ga}_{0.48}\text{P} \Rightarrow \text{InP}$ 1.5 μm	$\text{AlAs} \Rightarrow \text{In}_{0.52}\text{Al}_{0.48}\text{As}$ 1.1 μm	Nil	
Substrate	S. I. – GaAs 650 μm			S. I. – InP 650 μm

The device characterizations were conducted using an HP4156 semiconductor parameter analyzer with a Cascade probe station and a thermal chuck as discussed in Chapter 6. Both the metamorphic and the control lattice-matched devices with a $5 \times 20 \mu\text{m}^2$ emitter were chosen for the measurement of R_{th} . The wafers were unthinned and there were no backside via-holes.

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8.3 Results and Discussion

8.3.1 DC Characterization and Thermal Resistance Measurements

Fig.8.1 compares the common-emitter I - V characteristics of InP MHBTs with a linearly graded $\text{In}_x\text{Al}_{1-x}\text{As}$ or $\text{In}_n\text{Ga}_{1-n}\text{P}$ metamorphic buffer and a LHBT measured at a chuck temperature of 50 °C. The emitter size was $5 \times 20 \mu\text{m}^2$. It can be seen that all the devices exhibit similar I - V characteristics, but both the MHBTs show slightly lower offset voltages. Higher base currents are used for the MHBTs to obtain similar collector current indicating a relatively lower current gain of the MHBTs. Both the metamorphic and the lattice-matched devices show low junction leakage currents with the collector and base junction ideality factors similar to LHBT indicating good material quality. The devices made on the graded InGaP metamorphic buffer show comparable junction leakage (<50 nA) to those on InAlAs metamorphic buffer indicating a high resistivity of the graded InGaP metamorphic buffer. Detailed device DC parameters such as the DC gain, the junction ideality factors (n_c and n_b) and common emitter breakdown voltages (BV_{CEO}) are compared in Table 8.2.

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Fig.8.1 Typical common-emitter I - V characteristics of MHBTs with different metamorphic buffers and a LHBT measured at 50 °C. The emitter size of the devices is $5\times 20\ \mu\text{m}^2$.

Table 8.2 Comparison of device DC parameters

Parameters	LHBT	MHBT InGaP Buffer	MHBT InAlAs Buffer
DC gain, β	52	42	37
BV_{CEO} (V)	9.5	8.3	8.5
n_b	1.3	1.35	1.39
n_c	1.08	1.1	1.06

Different methods have been proposed to determine the steady-state thermal resistance, which can be categorized into pulsed I - V [63,64] and DC I - V [65,66,67,53] methods. Detailed comparison of these methods for GaAs-based HBTs has been

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documented by Scott [68]. The pulse I - V methods for determining the junction temperature are based on the matching of the device DC characteristics with those measured under the pulsed conditions but at elevated device temperatures. For the pulsed I - V method, the system must be able to measure the device I - V characteristics in a time interval well below the smallest time constant of the device so that isothermal or near-isothermal device characteristics can be obtained. This is difficult for small devices. The DC I - V method proposed initially by Dawson *et al* [65] and extended by Liu *et al* [67] later involves monitoring of V_{be} (or β) at different substrate temperatures. However, this approach could become uncertain in the case of low breakdown devices.

Recently Bovolon *et al* [53] have demonstrated an elegant and simple method for determining R_{th} at any operating point. Considering the relatively low breakdown voltage, especially for metamorphic HBTs, Bovolon's method has been used in this study. Although the variation of both β and V_{be} could be used to determine R_{th} in for GaAs HBTs [53], the absence of the negative differential output resistance, which originates from the decrease of the DC gain β with increasing junction temperatures (dissipated power) [69], in our MHBTs and LHBTs as shown in Fig.8.1, rules out the use of β as a temperature-sensitive parameter. Instead of β , the base emitter junction voltage (V_{BE}) was used for probing the variation of junction temperature. The increase of the junction temperature could cause the decrease of the bandgap energy which in turn could reduce the junction voltage, V_{BE} . The self-heating effect in our devices is clearly visible as shown in Fig.8.2. As shown in Fig. 8.2(a), after the device was turned-on, both the MHBTs with different buffers and the LHBT exhibited a negative

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dependence of V_{BE} on V_{CE} (i.e., device power consumption). The variation of V_{BE} with the increase of V_{CE} approximately follows a linear relationship. During the measurement, the base currents were set to 200 μA , 180 μA and 140 μA per step for the MHBTs with InAlAs and InGaP metamorphic buffers and LHBT, respectively, to ensure similar collector currents (dissipated power). The MHBTs showed a faster decrease of V_{BE} with the increase of V_{CE} suggesting that the MHBTs may have a relatively larger increase of the junction temperature with the increase of V_{CE} due to the larger thermal resistance of the metamorphic buffer and GaAs substrate. For a given device, a 20°C increase in the substrate temperature produced about 20 mV decrease of V_{BE} while the variation of I_C was only about 70 μA as shown in Fig. 8.2 (b).

The device thermal resistance (R_{th}) was characterized using the method proposed by Bovolon *et al* [53]. In Fig.8.2 (a), the values of V_{BE} in the linear region of the curve were used for the calculation. R_{th} is given as [70]:

$$R_{th}(P_{DISS1}, T_1) = \frac{\frac{V_{BE}(P_{DISS1}, T_1) - V_{BE}(P_{DISS2}, T_1)}{P_{DISS1} - P_{DISS2}}}{\frac{V_{BE}(P_{DISS1}, T_1) - V_{BE}(P_{DISS1}, T_2)}{T_1 - T_2}} \quad (8-1)$$

where P_{DISS1} is the dissipated power at temperature T_1 and P_{DISS2} is the dissipated power at temperature T_2 .

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Fig.8.2 (a) Illustration of typical V_{BE} versus V_{CE} characteristics of MHB-Ts and LHBT measured at 50°C . (b) Comparison of temperature dependence of I_{CE} - V_{CE} and V_{BE} - V_{CE} characteristics measured for the LHBT.

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The extracted values of R_{th} for the MHBTs using different buffer schemes and the control LHBT in the temperature range of 30 to 150 °C are plotted in Fig.8.3. Both the MHBTs and the LHBT show an increase of R_{th} with the increase in temperature as the thermal conductivity decreases with the increase temperature [71]. The values of R_{th} for LHBT are in the range of 1285 to 1500 K/W which is comparable to the low power dissipation value of 1300-1800 K/W obtained for the device with the similar device layer structures on InP substrate [72]. Indeed, the MHBT using the linearly graded InGaP buffer shows R_{th} in the range of 1600-1800 K/W, which is significantly lower than the one using InAlAs as the strain-relief buffer (2320 to 2615 K/W). Considering the similar device layer structure for the two MHBTs used in this study, the difference in the metamorphic buffer scheme could be the major cause for the different values of R_{th} measured for the MHBTs. The use of InGaP as the strain-relief buffer would provide a clear benefit to the device thermal properties compared to the widely used InAlAs. To gain a better understanding, an analytical model was used to have a quantitative verification on our experimental observation. This is also important for the prediction and the optimization of the layer structure design for the metamorphic devices.

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Fig.8.3 The temperature dependence of R_{th} for the MHBTs using InGaP and InAlAs metamorphic buffers and the referenced LHBt in the temperature range of 30 to 150°C .

8.3.2 Analytical Model and Verification

The heat removal from a planar device on a homogenous substrate has been studied by Joy and Schlig [73]. They have solved the thermal Laplace equation with appropriate boundary conditions leading to a widely accepted compact analytical expression. Although their method has been widely applied to different devices such as Si bipolar transistors and even GaAs HBTs [74], the presence of an inhomogeneous multilayer structure in the substrate region of the HBTs makes the use of this method difficult. In this work, a different approach has been employed to deal with our HBTs consisting of multiple layers. The total thermal resistance of the device can be

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expressed as the sum of a number of partial thermal resistances from a set of thin slabs, as in the case of HBT layer structures. The method, initially used by Licari and Enlow [75] for the calculation of heat transfer in hybrid package systems has recently been successfully applied to study the structural dependence of the thermal resistance of trench-isolated SiGe HBTs [76]. As shown in Fig.8.4, for an HBT made on a substrate with multi-layer structures, the downward transfer of heat flux to the substrate region is considered to be uniformly confined within a virtual boundary with an angle of α . Assuming that the temperature in the base-emitter junction is uniform, and ignoring the interface effect during the thermal transport, the thermal resistance for downward heat transfer through the collector, the sub-collector, the metamorphic buffer and the semi-insulating substrate can be calculated by:

$$R_{th} = \sum_i R_{th,i} = \sum_i \frac{\theta_i d_i}{A_i}, \quad (8-2)$$

where θ_i , d_i , and A_i are the thermal resistivity, the thickness and the area of a specified slab, respectively. If the substrate has a much large planar dimension compared to its thickness, utilizing the constant angle approach yields a value for the R_{th} as:

$$R_{th} = \int_0^w \left(\frac{\theta(z)}{(L_{emit} + 2z \cdot \tan \alpha)(W_{emit} + 2z \cdot \tan \alpha)} \right) dz \quad (8-3)$$

where w is the total thickness including the collector, the sub-collector, the buffer layer, and the substrate. L_{emit} and W_{emit} are the emitter length and the width, respectively and z is perpendicular distance from the collector towards the substrate as

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indicated in Fig.8.4. The variation of the thermal resistivity in a graded ternary metamorphic buffer can be determined by using the conventional quadratic relationship between the material composition and the thermal resistivity as:

$$\theta_{A_xB_{1-x}C}(z) = x(z)\theta_{AC} + [1 - x(z)]\theta_{BC} + k_{(AB)C}x(z)[1 - x(z)], \quad (8-4)$$

where $k_{(AB)C}$ is the bowing factor of the thermal resistivity. The room temperature thermal resistivities of the binary compounds as well as the bowing factor of ternary compounds used for the calculation are listed in Table 8.3. Notice that, except for $k_{(\text{InAl})\text{As}}$, the other data were obtained from previous publications [61,62,77]. For $k_{(\text{InGa})\text{P}}$, there is a larger discrepancy in the reported experimental data [61]. To our knowledge, no experimental values of thermal resistivity (conductivity) of bulk InAlAs and its bowing factor, $k_{(\text{InAl})\text{As}}$, have been reported so far. The value of k for InAlAs given in the table was extracted based on the experimental value of the effective thermal conductivity of $\sim 10 \text{ W/m}\cdot\text{K}$ value reported for a $1.5 \mu\text{m}$ $\text{In}_x\text{Al}_{1-x}\text{As}$ linearly graded metamorphic buffer on GaAs substrate [54]. Nevertheless, the extracted value is close to the one suggested by Spagnolo *et al* [78] that the thermal properties of InAlAs may be scaled by a factor of 1.25 with respect to those of InGaAs, based on the known thermal properties of GaAs, AlAs and InAs.

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Table 8.3 Room Temperature thermal resistivities of III-V binary compounds and bowing parameters for the ternary materials used in this work

Material	Thermal Resistivity, θ (K·cm/W)		Material	Alloy-disorder Bowing, k (K·cm/W)	
GaAs	2.27	Ref. [72]	InGaAs	72	Ref. [56]
InP	1.47	Ref. [72]	InGaP	72	Ref. [56]
AlAs	1.10	Ref. [72]		19.9	Ref. [55]
InAs	3.70	Ref. [72]	InAlAs	60* Ref. [50]	
GaP	1.30	Ref. [72]			

* Estimated

The upward heat transfer through the emitter contact could be estimated based on a first order estimation by considering the heat flow in a horizontal direction from the emitter metal to the emitter pads [79]:

$$R_{th_E_metal} = \frac{L_{emit_pad}}{\kappa_{Au} \cdot W_{emit} \cdot T_{emit}}, \tag{8-5}$$

where $R_{th_E_metal}$ is the thermal resistance of the emitter metal, L_{emit_pad} is the distance from the emitter center to the emitter pad which is around 10 μm for our device, k is the alloy disorder bowing factor, the emitter metal width (W_{emit}) is 5 μm and T_{emit} is the emitter metal thickness. Using $\kappa_{Au} = 3.17 \text{ W/cm-K}$ and an emitter metal thickness T_{emit} of 350 nm, Equation (8-5) gives a thermal resistance of $1.803 \times 10^4 \text{ K/W}$. The thermal flux dissipated through the emitter contact is shunt-connected to the substrate with the downward thermal resistance contributing to the total thermal resistance (in the parallel configuration). However, we note that the upward thermal

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resistance through the emitter metal is quite large (typically, ~ 10 times that of the intrinsic device thermal resistance), which conducts only about 10% of the total heat dissipated. The smaller contribution of the flow of heat through the emitter contact compared to the simulated results by Harrison et al [80] may be due to the different device layout designs. In our devices, the emitter is connected to the contact pad from one end of the emitter finger. The emitter thermal resistance is limited by the heat flow in a horizontal direction. Considering that the uncertainty in the measurement of on-chip temperature can be easily as high as 10%, the contribution from the emitter contact can be neglected for a first-order estimate of the device thermal resistance.

Fig.8. 4 Schematic of an HBT made on a metamorphic buffer. The downward transfer of heat flux in the subcollector and the substrate regions is illustrated to be confined within a virtual boundary with an angle of α .

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Fig.8.5 compares the theoretical calculation with the experimental data for the thermal resistance of LHBT and MHBTs. The angle of heat spreading, α is assumed to be 45° in our calculation. This assumption has been validated by 3-dimensional thermal simulations [74] and agrees with the value recommended in literature [81]. The results show that for the device with InGaP metamorphic buffer, using the bowing factor, $k_{(\text{InGa})\text{P}}$, given by Adachi [62] yields a significant overestimation of the device thermal resistance, while the calculation of thermal resistance based on $k_{(\text{InGa})\text{P}}$ of 19.9 K·cm/W reported by Both and Herrmann [61] shows a better prediction of the experimental data. The simple physical model yields an acceptable accuracy for both the lattice-matched and metamorphic HBTs. Although the presence of defects and dislocations in the substrate may cause the change of the material thermal conductivity, the dislocations in the metamorphic buffer region seem to play a negligible effect on the overall thermal resistance.

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Fig.8.5 Comparison of theoretical calculation with the experimental data for the thermal resistance of MHBTs and the referenced LHBT. The open symbols are experimental data, and the solid symbols are the results from the calculation. For device B with InGaP metamorphic buffer, the data represented by (▲) was calculated using the $k_{\text{InGaP}} = 72 \text{ K}\cdot\text{cm}/\text{W}$ [62], and the data represented by (●) was calculated using $k_{\text{InGaP}} = 19.9 \text{ K}\cdot\text{cm}/\text{W}$ [61].

To understand the importance of the metamorphic buffer layer to the total thermal resistance of the devices, the contributions from each individual layer (from the subcollector to the substrate) for different devices are plotted in Fig.8.6. It is seen that, for the MHBt using an InGaP metamorphic buffer, the metamorphic buffer and the substrate contribute about 50% to the total thermal resistance, which is slightly larger than the referenced InP HBT. However, using a linearly graded InAlAs as a the strain-relief buffer results in a much larger contribution. The contributions from an

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InAlAs metamorphic buffer and GaAs substrate to the total thermal resistance could be more than 70%. It seems that the 250 nm InAlAs buffer placed between the substrate and the subcollector provides a substantial contribution to the device thermal resistance. Replacing this layer by a higher thermal conductivity InP or reducing the thickness of InAlAs layer could improve the device thermal properties. The use of InAlAs and InGaAs in the layer structure design should be avoided if the device thermal property is an important concern.

Fig.8.6 Calculations of contributions from the different layers in MHBTs and LHBT (from subcollector to substrate) to the total thermal resistances. The open symbols with error bar are the experimental data. (Device A: LHBT, Device B: MHBT with InGaP metamorphic buffer, and Device C: MHBT with InAlAs metamorphic buffer)

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8.3.3 Notes on Design and Optimization of Metamorphic Buffer Based on Device Thermal Resistance

Although the use of InP as a metamorphic buffer has demonstrated its advantage on the reduction of thermal resistance, the use of ternary InGaP provides more freedom to use as a graded metamorphic buffer scheme, which could be of great benefit during the growth optimization for improving the material quality such as the surface roughness and the defect density. Compared to InAlAs as a metamorphic buffer layer for MHBTs, InGaP could achieve a much lower thermal resistance without sacrificing the advantages of a graded buffer. Furthermore, the total thermal resistance and the contribution of each layer in the substrate region could be largely affected by the layer structure. For example, the calculated results presented in Fig. 8.6 show that, even though GaAs is used as the substrate for both device B (1.5 μm InGaP metamorphic buffer) and C (1.1 μm InAlAs metamorphic buffer), the thermal resistance contributions from the GaAs substrate are different. This could be clearly illustrated by varying the InP subcollector thickness.

Fig. 8.7 plots the calculated R_{th} of device using InGaP buffer and the contribution of thermal resistances from different layers as a function of the InP subcollector thickness. If the InP subcollector thickness is increased from 0.2 to 1.5 μm , the R_{th} of MHBt could be reduced from ~ 1700 K/W to 1500 K/W, which is closer to the value measured from the referenced lattice-matched InP HBTs (1285 K/W). Considering the layer structure shown in Fig. 8.4, although the increase in InP subcollector thickness slightly increases the thermal resistance contributed from subcollector region, the increase in the effective area for the heat transfer in the

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subsequent low thermal conductivity buffer layers results in a reduction of the total device thermal resistance. Notice that, as the thickness of InP subcollector is increased, contributions to the thermal resistance from GaAs substrate and other layers become smaller. This also explains the experimental observations reported by Kim *et al* that the MHBTs using InP metamorphic buffers exhibit a similar value of R_{th} as the referenced HBTs fabricated on InP substrate [58]. Of course, a thick InP subcollector (or buffer) would complicate the device fabrication and lower the throughput of the epitaxial growth.

Fig.8.7 Calculated R_{th} of device B (MHBT with InGaP metamorphic buffer) and contributions of thermal resistances from different layers as a function of InP subcollector thickness. The experimental result (solid symbol) for the device with a 250 nm InP subcollector is also plotted for reference.

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8.4 Summary

This chapter has presented a detailed study of the thermal properties of metamorphic InP/InGaAs HBTs on GaAs substrates using different metamorphic buffers. Compared to the widely used InAlAs metamorphic buffer, InGaP offers better thermal properties resulting in a much smaller thermal resistance for the MHBTs. Although the use of InGaP as a buffer may slightly degrade the device thermal properties compared to the direct growth of low thermal resistance InP, it provides more freedom for the growth optimization of the metamorphic buffer by using compositional grading. This can be an important alternative to the existing InAlAs and InP schemes concerning growth optimization and thermal properties. Theoretical calculations of device thermal resistance have been made based on the simple constant heat-spreading model, and the results are shown to be consistent with the experimental results. It has been made clear that the smaller thermal resistance measured from the MHBTs using a linearly graded InGaP buffer is due to the small bowing parameters and high thermal conductivity of the binary endpoints. The thermal resistivity of InGaP estimated by Adachi [62] based on the extrapolation of experimental value from InGaAs may largely overestimate the alloy-disorder bowing. Data given by Both and Herrmann [61] provide better prediction for the experimental results. Furthermore, using the model, the contributions of the metamorphic buffer and other layers to the device thermal resistance have been estimated. The results will be important in the design of layer structure for MHBTs to achieve better thermal properties.

Chapter9 Conclusion and Recommendations

Chapter 9

Conclusion and Recommendations

9.1 Conclusion

High gain metamorphic InP/InGaAs/InP DHBTs on GaAs substrate fabricated using complete NTU in-house process has been demonstrated in this investigation. DC and RF characterization of various MHBTs, including noise and power measurements, elevated temperature and current stress measurements, evaluation of thermal resistance, and performance comparison of devices grown by different growth techniques have been accomplished. The important findings from these studies are summarized as below:

(1) A comparative study of InP-based MHBTs grown by gas and solid-source MBE techniques has been presented. The DC and RF performances of the devices with an emitter size of $1.6 \times 20 \mu\text{m}^2$ and base Be doping concentration of $2 \times 10^{19} \text{ cm}^{-3}$ are summarized. The figures of merit for these two MHBTs such as the product of DC current gain and maximum oscillation frequency ($\beta \times f_{\text{MAX}}$) which are governed by base quality and the doping concentration, and the product of the common emitter breakdown voltage and the unity current gain cut-off frequency ($BV_{\text{ceo}} \times f_T$) which are related to the thickness variation were found to be similar. This suggests that both the

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solid-source and the gas-source MBE techniques may offer similar material quality, hence, higher device performances could be achieved by proper optimization of the material growth conditions.

(2) The temperature dependence of the DC characteristics of the metamorphic InP-based DHBT on GaAs substrate has been investigated. The device transport properties for the devices were studied to assess the material quality. The experimental results suggest that the band-to-band recombination plays a dominant role in determining the base current in the studied temperature range of 300 to 400 K, the range where the devices are commonly operated. No trap-related recombination was observed for the base and the collector currents indicating that the metamorphic HBT structures grown by SSMBE offer good material quality.

(3) The stress tests on MHBTs have been carried out under high current density at high junction temperature. Photoluminescence characterization, low frequency noise measurements and electrical tests were performed on MHBT structures. Good correlation obtained between the device degradation during the electrical stress and the optical and low frequency noise measurements may provide important means to assess the device stability for MHBTs. The promising results indicate that, by proper growth optimization of the strain relief buffer layer and the device layer structures, MHBTs on GaAs substrate with electrical stability similar to that of HBTs on InP substrate could be achieved.

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(4) Thermal properties of MHBs grown using a linearly graded InGaP metamorphic buffer has been investigated. Compared to the widely used InAlAs buffer, InGaP offers better thermal properties resulting in a much smaller thermal resistance for the MHBs. Theoretical calculations of the thermal resistance of devices have been made based on a simple constant heat-spreading model, and the results were found to be consistent with the experimental data. With better thermal conductivity and the flexibility in growth optimization, InGaP metamorphic buffer could be considered as an important alternative to the existing InAlAs and InP schemes.

9.2 Recommendations for further research

The focus of the present investigation is mainly on the fabrication and characterization of various MHBs with specific device layer structures with optimized growth conditions. Although the DC and RF characteristics including device stability of the MHBs have been good, higher performances can be achieved by adjusting the layer structure design and scaling the device dimensions using improved fabrication process. Moreover, the application of MHB devices in microwave integrated circuits has not been demonstrated. Because of the time limitation, it was not possible to accomplish given the large magnitude of work involved. Along these lines, the following studies may be pursued to bring the metamorphic HBT technology to greater heights:

(1) Device Layer Structure Optimization

In the present studies, a relatively lower base doping of $2 \times 10^{19} \text{ cm}^{-3}$ was employed using beryllium as the dopant. The dopant concentration can be increased

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to $4 \times 10^{19} \text{ cm}^{-3}$ to reduce the base resistance, and increase the power gain and high frequency performance without the serious problem in terms of Be out diffusion. Higher base doping concentration is also possible if carbon is used. Moreover, compositionally graded InGaAs base layer instead of the uniform base can be designed to achieve transit time reduction.

(2) Process Development

Device layout and epitaxial layer structures have great impacts on device performance. Reducing the emitter size of the MHBTS could enhance the microwave performance of the devices. In this case, a new device fabrication process has to be developed with submicron size emitter width by a combination of dry etching and wet etching for self-alignment structures. Optimization of the combinational etching is necessary to suppress the possible plasma damage to the exposed base area. Present wet etch chemistry may not be suitable for smaller emitter devices; thus a suitable new wet etch chemistry should be developed.

(3) Long-term Reliability of the Metamorphic HBTs

One of the major concerns for the practical implementation of metamorphic device in circuits and systems is the long-term reliability. Although a high temperature and high current stress has been performed on our MHBTS devices, the device long-term reliability and lifetime remain unclear. Further studies need to be carried out to assess the device long-term reliability and understand the device degradation mechanisms. This is critical for device practical applications.

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(4) Demonstration of MHB T MMICs

Although MHB T devices have been developed and fabricated in this study, for demonstration in system applications, circuits operating in the microwave or millimeter wave regime have to be designed and fabricated to establish the device potential. This will include development of suitable passive components, small-signal modeling, and circuit modeling and design.

Author's Selected Publication

Journal papers

1. **Hong Yang**, Hong Wang, K. Radhakrishnan and Chee Leong Tan, "Thermal Resistance of Metamorphic InP-based Heterojunction Bipolar Transistors on GaAs Substrates Using a Linearly Graded In_xGa_{1-x}P Metamorphic Buffer," **IEEE Trans. Electron Devices**, vol.51, no.8, pp.1221-1227, 2004.
2. **Hong Yang**, K. Radhakrishnan and Hong Wang, "A comparative study of Metamorphic InP/InGaAs heterojunction bipolar transistors (MHBTs) grown by gas and solid source molecular beam epitaxy (MBE)," **Journal of Crystal Growth**, vol. 268/3-4, pp. 410-414, 2004.
3. **Hong Yang**, Hong Wang, Geok Ing Ng, Haiqun Zheng and K. Radhakrishnan, "DC characterization of Metamorphic InP/InGaAs Heterojunction Bipolar Transistors at Elevated Temperature," **Jpn. J. Appl. Phys.**, vol.41, Part 1, no.2B, pp. 1136-1138, 2002.
4. Hong Wang, **Hong Yang**, K. Radhakrishnan, Tien Khee Ng and Wai Chye Cheong, "The Influence of Emitter Materials on Silicon Nitride Passivation-Induced Degradation in InP-Based HBTs," **IEEE Trans. Electron Devices**, vol.51, no.1, pp.8-12, 2004.
5. H. Wang, **Hong Yang**, W. P. Neo, K. Radhakrishnan, and C. L. Tan, "Temperature Dependence of Avalanche Multiplication in InP-Based Heterojunction Bipolar Transistors with InGaAs/InP Composite Collector: Device Characterization and Physics Model," **IEEE Trans. Electron Devices**, vol.50, no. 12, pp.2335-2343, Dec. 2003.
6. Hong Wang, Geok Ing Ng, **Hong Yang** and K. Radhakrishnan, " Studies on the Degradation of InP/InGaAs/InP Double Heterojunction Bipolar Transistors Induced by Silicon Nitride Passivation," **Jpn. J. Appl. Phys.**, Vol.41, Patr 1, no. 2B, pp. 1059-1061, 2002.

Conference papers

1. **Hong Yang**, Hong Wang, and K. Radhakrishnan, "Device Stability of Metamorphic InP/InGaAs Heterojunction Bipolar Transistors by Optical and Electrical Characterization," 16th International Conference on Indium and Related Materials (IPRM04), May 2004
2. **Hong Yang**, Hong Wang, and K. Radhakrishnan, " Low-Frequency Noise Characterization of Metamorphic InP/InGaAs Heterojunction Bipolar Transistors on GaAs Substrate," 15th International Conference on Indium and Related Materials (IPRM03), pp.142–144, May 2003.
3. **Hong Yang**, K. Radhakrishnan and Wang Hong, "DC and RF characterizations on InP double heterojunction bipolar transistors (DHBT's) grown by gas source MBE," International Conference on Materials for Advanced Technologies (ICMAT 2003), Dec 2003.
4. **Hong Yang**, K. Radhakrishnan and Wang Hong, "A Comparative Study of Metamorphic InP/InGaAs Heterojunction Bipolar Transistors grown by Gas and Solid Source," by International Conference on Materials for Advanced Technologies (ICMAT 2003), Dec 2003.
5. **Hong Yang**, Hong Wang, and K. Radhakrishnan, "Metamorphic InP/InGaAs Heterojunction Bipolar Transistors Under High-Current and High Temperature Stress," 14th International Conference on Indium and Related Materials (IPRM02), pp.369–372, May 2002.
6. **Hong Yang**, Hong Wang, Geok Ing Ng, Haiqun Zheng and K. Radhakrishnan, "Device Performance and Transport Properties of High Gain Metamorphic InP/InGaAs Heterojunction Bipolar Transistors at Elevated Temperature," 13th International Conference on Indium and Related Materials (IPRM01), pp.200–203, May 2001.
7. Hong Wang, **Hong Yang**, K. Radhakrishnan and Chee Leong Tan, "On the Thermal Resistance of Metamorphic and Lattice-Matched InP HBTs: A Comparative Study," 14th International Conference on Indium and Related Materials (IPRM02), pp.177-180, May 2002.

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Appendix A InP/InGaAs DHBT Process Document

Appendix A

InP/InGaAs DHBT Process Document

Emitter Metal and Emitter Mesa			Completed	
No.	Step	Specification		Remarks
1	Cleaning of sample	Hot acetone 1 min, hot IPA 1 min, DI Water, blow dry, bake at 110°C 5-10min		Baking from__ to __
2	Cleaning of InP HBT mask	Acetone, IPA, mask cleaner 1:4 on ultrasonic 5min, DI water, blow dry, bake at 110°C 30min		Baking from__ to __
3	Resist	AZ 5214 , 30s at 3000r/min, baking at 105°C 1min 45 sec Hot plate	Clean the edge using Acetone in case of the smaller size samples	Baking from__ to __
4	Exposure	e- mesa mask, 3 s, no alignment, baking at 110°C 7min, flood exposure 21s without mask		Baking from__ to __
5	development	AZ developer:DI 1:2, 40-60s, optical inspection		inspection:
6	descum	RIE process peo2.prc, dipping in HCl:DI 1:10 10s		resist thickness:
7	metallisation	E-beam or CHA Ti 50nm/Au 300nm, lift-off in acetone		Metal thickness:
8	etching	H ₂ O 200ml/H ₃ PO ₄ 15ml/H ₂ O ₂ 5ml , etch (InGaAs) HCl:H ₃ PO ₄ 1:5 etch (InP)		Breakdown voltage before etching:____V

Remarks :

Base Metal			Completed	
No.	Step	Specification		Remarks
9	Cleaning of sample	as for emitter mesa		baking from __ to __
10	Cleaning of mask	as for emitter mesa		baking from __ to __
11	Resist	AZ 5214 30s at 3000r/min, baking at 105 °C 1min 45s or 90°C 30min	Clean the edge using Acetone in case of the smaller size samples	baking from __ to __
12	Exposure	3 s, baking at 110°C 7min, flood exposure 21s without mask		baking from __ to __
13	development	AZ351:DI 1:2, 40-60s, optical inspection		inspection:
14	descum	RIE process peo2.prc, dipping in HCl:DI 1:10 10s		photoresist thickness:
15	metallisation	E-beam or CHA Ti 40nm/Au 180nm,	Metal thickness must be less than InGaAs+InP cap+ InP emitter	metal thickness
16	Lift-off	in acetone		real etch depth

Remarks:

Appendix A InP/InGaAs DHBT Process Document

Base Mesa			Completed	
No.	Step	Specification		Remarks
17	Cleaning of sample	as for emitter mesa		baking from __ to __
18	Cleaning of mask	as for emitter mesa		baking from __ to __
19	Resist	AZ 1518 30s at 4000r/min, baking at 105 °C 1min 45s or 90°C 30min	Clean the edge using Acetone in case of the smaller size samples	baking from __ to __
20	Exposure	20s		
21	development	AZ351:DI 1:2, 40-60s, optical inspection		inspection:
22	descum	RIE process peo2.prc, baking at 110° 15min		resist thickness:
23	etching	H ₂ O 200ml/H ₃ PO ₄ 15ml/H ₂ O ₂ 5ml, etch InGaAs HCl:H3PO4 1:5 etching InP to subcollector		Dektek check the thickness: Surface breakdown:
24	resist removal	in acetone		real etch depth

Remarks:

Collector Metal			Completed	
No.	Step	Specification		Remarks
25	Cleaning of sample	as for emitter mesa		baking from __ to __
26	Cleaning of mask	as for emitter mesa		baking from __ to __
27	Resist	AZ 5214 30s at 3000r/min, baking at 105 °C 1min 45s or 90°C 30min	Clean the edge using Acetone for smaller size samples	baking from __ to __
28	Exposure	3 s, baking at 110°C 7min, flood exposure 21s without mask		baking from __ to __
29	development	AZ351:DI 1:2, 40-60s, optical inspection		inspection:
30	descum	RIE process peo2.prc, dipping in HCl:DI 1:10 10s		resist thickness:
31	metallization	E-beam or CHA Ti 50 nm/Au 200 nm,		metal thickness
32	Lift-off	in acetone		real etch depth

Remarks:

Appendix A InP/InGaAs DHBT Process Document

Collector Mesa			Completed	
No.	Step	Specification		Remarks
33	Cleaning of sample	as for emitter mesa		baking from __ to __
34	Cleaning of mask	as for emitter mesa		baking from __ to __
35	Resist	AZ 1518 , 30s at 4000r/min, baking at 105 °C 1min45s or 90°C 30min	Clean the edge using Acetone for small size samples	baking from __ to __
36	Exposure	Collector mesa die, <u>90s</u> , alignment to Emitter metal mask		
37	development	AZ:DI 1:2, 35s, optical inspection,		inspection:
38	descum	RIE process peo2.prc, baking at 110° 15min		resist thickness:
39	Etching	H ₂ O 200ml/H ₃ PO ₄ 15ml/H ₂ O ₂ 5ml, at 17-20°C, etch InGaAs HCl:H ₃ PO ₄ 1:5 overetch substrate 10 s	InGaAs stop layer (subcollector), <u>3min</u> InP subcollector +substrate, 5min <u>Check neck etch</u>	inspection: Measurement:
40	resist removal	in acetone		

Remarks:

Pillar			Completed	
No.	Step	Specification		Remarks
41	Cleaning of sample	as for emitter mesa		baking from __ to __
42	Cleaning of mask	as for emitter mesa		baking from __ to __
43	Resist	AZ 1518 , 30s at 3000r/min, baking at 105°C 1 min 45 sec	Clean the edge for small size samples	baking from __ to __
44	Exposure	15s		
45	development	AZ351:DI 1:2, 40-60s, optical inspection		inspection:
46	descum	RIE process peo2.prc,		resist thickness:
47	Post-bake	110°C 10 min, check resist profile!!!	Corner round	
48	Seeding layer	Dep. Seeding metal using CHA Or sputtering	Ti 20nm/Au 80nm	metal thickness

Remarks:

Appendix A InP/InGaAs DHBT Process Document

Air-bridge Interconnection Metal			Completed	
No.	Step	Specification		Remarks
		After seeding layer deposition, No need clean the samples using Acetone!!!		baking from __ to __
49	Resist	AZ 5214 , 30s at 2000 r/min, baking at 105°C 1min 45 sec	Clean the edge for small size samples	baking from __ to __
50	Exposure	interconnect die, 4s, alignment to Emitter Mesa, baking at 110°C 8 min, flood exposure 32s without mask		baking from __ to __
51	development	AZ351:DI 1:2, 80-100s, optical inspection		inspection:
52	descum	RIE process peo2.prc, dipping in HCl:DI 1:10 10s		resist thickness:
53	Seeding layer etch	I2:KI:H2O(A)=1:4:40 etch Au HF:HNO3:H2O=1:2:63 etch Ti	Ti 10s, 5s after bubbling	Ultrasonic!!
54	Interconnect metal	TiAu 50nm/1000 nm, lift-off in hot acetone	Separate three times for Au growths, reduce the temperature	metal thickness

Remarks:

Passivation			Completed	
No.	Step	Specification		Remarks
55	Cleaning of sample	as for emitter mesa		baking from __ to __
56	Cleaning of mask	as for emitter mesa		baking from __ to __
57	Polyimide promoter	Ultradel A600 , 5s at 500r/min, then 30s at 4000r/min, baking at 105°C 1 min 30 sec		baking from __ to __
58	Polyimide	Ultradel 7501 , 30s at 500r/min, then 60s at 4500r/min, baking at 105°C 3 mins		baking from __ to __
59	Exposure	Pattern by passivation mask, 30s, post-exposure bake 175°C 30 mins in nitrogen purged oven		baking from __ to __
60	development	Ultradel D760 50s, optical inspection		inspection:
61	Hardbake in nitrogen oven	25°C 5 mins, 10°C/min ramp to 200°C and hold for 60 mins, 10°C/min ramp to 325 and hold for 30 mins.		baking from __ to __

Remarks: