Copper-ultra low k porous SiLK integration for deep submicron integrated circuits

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Copper-Ultra Low k Porous SiLK Integration
For
Deep Submicron Integrated Circuits

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A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

2006

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

Date

Yang Lieyong

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SUMMARY

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Conventionally, aluminum and its alloys have been widely used for contacts and interconnections in integrated circuits. However, as the interconnect line widths shrink continuously to deep submicron dimensions, the aluminum metallurgy may become inadequate due to electro-migration. Moreover, the resistivity of Al alloys is higher than that required for future design considerations. As a result, copper is a potential candidate as the interconnection for the integrated circuits of the next generation owing to its lower electrical resistivity and higher resistance to electro-migration. On the other hand, the low k and ultra low k dielectrics have been investigated to replace the conventional dielectric SiO_2 to address the problem of parasitic capacitance and resistance capacitance (RC) delay in ultra large scale integration. In this project, the integration of Cu and Ultra low k (ULK) porous SiLK (Trademark) using different barriers on blanket and patterned wafers has been investigated. This includes characterization of ULK porous SiLK, Ta based barrier on ULK, Ta(N)/SiCN/ULK SiLK structures, and integration of Cu-ULK porous SiLK with different barriers on blanket and patterned wafers. The thermal stability, interaction and electrical properties of different structures were comparatively investigated by using various techniques. The single damascene lines were fabricated of Cu and ULK porous SiLK with different barrier layers in 0.13 μm technology. The line resistance, line-to-line leakage current and breakdown voltage were evaluated at various conditions. Furthermore, effects of plasma treatment and additional SiCN layer on the electrical performance and thermal

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stability of the Cu/barrier/ULK structures were evaluated. Finally, the thickness of SiCN was also optimized. The detailed work can be summarized as follows:

The ULK porous SiLK, which is supplied by Dow Chemical Company with k value around 2.3, was characterized. Samples were annealed at various temperatures in order to study the thermal stability. Atomic force microscopy (AFM), X-ray diffraction (XRD), X-ray reflection (XRR), Fourier transform infra-red (FTIR), C-V and other techniques were employed to evaluate the roughness, porosity, thickness, adhesion, dielectric constant and other properties. The porous SiLK still keeps good properties after being annealed at 500°C for 30 mins, including the surface roughness, thickness, adhesion, porosity and dielectric constant. The abrupt change of electrical and mechanical properties was observed after being annealed at temperatures higher than 500°C. This is because when annealing temperature is higher than the glass transition temperature ($T_g = 490^\circ\text{C}$), the repeating unit in ULK possibly breaks down, and turns into small molecules.

Three kinds of diffusion barrier layers (Ta, TaN and Ta/TaN bi-layer) have been developed for the ULK porous SiLK, and the properties of these films, such as sheet resistance, surface morphology and microstructure, have been investigated. It was found that the Ta film showed body centered cubic (BCC) structure, lower resistivity and clear grain boundary, while the TaN film showed smaller grain size and blur grain boundary due to the incorporation of N.

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To evaluate the thermal stability of barrier/ULK structure, annealing was carried out in two different ways. One is to anneal the samples for only 3 mins at various temperatures, and the other is to anneal at 400°C for different times. For the annealing at different temperatures, the barrier/ultra low k structures were found to lose the integrity at temperatures over 500°C due to the failure of ULK's properties, and significant diffusion was observable near the interfaces of the structures. The Ta/ULK structure shows the smallest sheet resistance but the poorest thermal stability while the TaN on the ULK porous SiLK shows the highest resistance but best thermal stability. The Ta/TaN bi-layer barrier takes the advantage of both Ta and TaN barriers and gives reasonable resistance and thermal stability. The better thermal stability of the TaN and the Ta/TaN bi-layer barriers is mainly due to the amorphous/nano structure and less grain boundaries of the barriers. In addition, the texture discontinuity at the Ta/TaN interfaces in the bi-layer barrier also plays an important role in reducing mutual diffusion of Ta atoms in the Ta barrier and some atoms in the ultra low k porous SiLK.

For the annealing at 400°C for different thermal cycles, it was found the sheet resistance and roughness of the barriers increased with the annealing time, and the Ta-O compound was also detected. However, no abrupt change was observed until the annealing time of 150 mins. The secondary ion mass spectrometry (SIMS) results revealed that the oxygen is rich at the barrier/ULK interfaces, and the diffusion coefficient of Ta from the Ta barrier in porous SiLK is $0.023 \pm 0.001 \text{ nm}^2/\text{s}$, while the

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diffusion coefficient of Ta from the TaN is only $0.0033 \pm 0.0001 \text{ nm}^2/\text{s}$.

The effect of the three kinds of barrier layers on the properties of self-ionized plasma (SIP) Cu films such as sheet resistance, surface morphology and microstructure have also been studied using various techniques. Cu (111), Cu (200) and Cu (220) textures were observed for three barriers.

Two factors were found to cause the Cu/Ta/ULK structure degradation. One is the Ta barrier which has the polycrystalline structure with finer grain (7-10 nm), and can easily enter the porous SiLK with pore size around 10 nm. It also provided fast diffusion paths for C, H, and O atoms in the ULK. The other is the higher affinity of Ta to oxygen, which can easily form oxide, Ta_2O_5 , and causes increase in sheet resistance. The results of the SIMS revealed that the significant increase of the sheet resistance was due to the diffusion of Ta and O to the Cu film. It was also revealed that the annealing at 400°C for more than 120 mins also caused diffusion of Ta and O and even Cu into the ULK. Ta and O diffused faster in the dielectric than in the Cu film. In addition, the out-diffusion of the C and H in the ULK towards Ta and Cu layers was also observed and the H diffusion was found to diffuse faster than C.

For TaN barrier, Ta and N may diffuse separately. At the same time, TaN also diffuse on the surface as molecule, these processes could coexist. Compared with the Ta/ULK, TaN/ULK interface is smooth and well defined as a layer of intermediate intensity

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between TaN and ULK. For the Cu/Ta/TaN/ULK sample, smaller diffusion area appeared at the TaN/ULK interface. At the same time, Ta diffused into Cu layer is also presented.

The diffusion coefficients of Cu in different Barrier/ULK are $0.035 \text{ nm}^2/\text{s}$, $0.04 \text{ nm}^2/\text{s}$ and $0.03 \text{ nm}^2/\text{s}$ at 400°C in Cu/Ta/ULK, Cu/TaN/ULK and Cu/Ta/TaN/ULK, respectively. And the diffusion coefficients of Ta in ULK are $0.05 \text{ nm}^2/\text{s}$, and $0.051 \text{ nm}^2/\text{s}$ at 400°C in the Cu/Ta/ULK and Cu/TaN/ULK structures, respectively. Obviously, the diffusion coefficient of Ta with Cu capped layer is larger than that without Cu layer because the residual stress in Cu and Ta can accelerate the Ta diffusion into ULK.

The thermal stability of the Cu/SiCN/ULK structures were investigated. Comparing with the Ta based barriers in the Cu/Ta(N)/ULK structures, SiCN showed many advantages. These include lower density (3.25 g/cm^3), higher hardness (460 GPa), amorphous structure without grain boundary defects, better thermal stability and no reaction with Cu, ULK and oxygen after being annealed at 400°C for 150 mins. So it can be thought as a good barrier candidate for Cu and ULK integration.

Introducing an additional SiCN barrier layer to the Ta barrier can significantly improve the thermal stability because the amorphous structure of the SiCN not only effectively blocks ULK out-diffusion, but also prevents the Cu, Ta from diffusing into ULK. The thin SiCN film deposited on the ULK surface can also significantly improve

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the surface mechanical property and thermal stability. Similar results can also be observed for the sample with TaN barrier. When SiCN additional layer was added to TaN barrier, the barrier shows much better performance. TEM pictures show fairly smooth interfaces up to 400°C. AFM measurement shows only a small increase in roughness of Cu film surface due to the Cu grain growth. No new phases are detected by XRD investigation at 400°C up to 150 minutes of annealing time.

Plasma treatment seems to cause higher sheet resistance for the as-deposited sample because of more grain defect. However, it also improves the barrier integrity in terms of sheet resistance during annealing and results in lower sheet resistance. It also helps to improve the smoothness of Cu film as can be seen by AFM results due to the surface modification. But it also shows that such treatment has critical drawbacks: 1) it can lead to degradation of the ULK; 2) it also causes surface damage and degrades the thermal stability.

The single damascene Cu lines using three kinds of Ta-based barriers with and without SiCN and plasma treatment for Cu-ultra low k interconnect in 0.13 μm technology have been investigated. The electrical tests indicate that the Cu lines with the TaN and Ta/TaN bi-layer barriers exhibit the smaller leakage current and higher breakdown voltage compared with the Cu lines with Ta barrier. However, the line with Ta barrier has the smallest line resistance while the line with the TaN barrier has the highest.

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It was found that the N_2/H_2 plasma treatment on the ULK surface before depositing barrier and Cu could reduce the line resistance significantly, but also brought more surface defects on the sidewall and larger diffusion length. The larger line-to-line leakage currents and lower breakdown voltages were observed after applying thermal stress. It indicates that the plasma treatment degrades the thermal stability comparing with the untreated samples.

Compared with only the Ta and Ta-based barrier layer structure, introduction of an additional SiCN layer could significantly improve the breakdown voltage, line-to-line leakage and thermal stability. However, it also brought higher line resistance. Four groups of samples with different thicknesses of SiCN layers were comparatively studied. The SiCN layer between 20 nm and 50 nm can give better electrical performance and thermal stability.

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CHAPTER 1 Introduction

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Introduction

1.1 Background

Modern integrated circuit devices contain millions of transistors electrically connected by millions of wires fabricated on the wafer. The wires, or "interconnect", transform a sea of transistors into a functioning device with logic defined by the wire layout. Some of today's advanced logic devices have as many as seven layers of interconnects with minimum wire width and spaces of about $0.13\text{ }\mu\text{m}$ [2, 4, 7, 123]. Essentially all interconnects were fabricated using aluminum as the conductor and silicon dioxide as the dielectric. The performance of integrated circuit devices, historically limited by characteristics of the transistors, has become limited by the electrical characteristics of interconnect. In the past, the interconnect signal delay, characterized by the resistance capacitance (RC) time constant, was negligible. The transistor gate delay, which is proportional to the size of the transistor, limited the speed of logic devices. Scaling down the feature sizes in microelectronic circuits has shown efficiency in improving circuit performance and increasing yield at lower cost per function on chip. Circuit speed increases are primarily due to reduction in transistor gate lengths, resulting in faster transistor switching times. However, by reducing the transistor gate size about 30% every technology node, the industry remarkably doubled the device speed roughly every two years since the first introduction of the microprocessor in the early 1970s. The reduction in transistor dimension has been accompanied by the scaled reduction in interconnect feature size. The reduction in

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conductor cross-sectional area results in increased wire resistance, and the reduction in inter-conductor distance results in increased line capacitance, cross-talk, and power dissipation. In contrast to the past, the RC interconnect delay now exceeds the transistor gate delay for some circuits at the 0.18 μm technology node. So using a high conductivity metal (like copper) for interconnecting lines and a low permittivity dielectric (low k) seems to be one of the most efficient solutions.

1.2 Motivation and objectives

1.2.1 Motivation for Cu/low k

The intrinsic propagation delay of a typical gate in a CMOS technology is defined as the delay associated with an inverter implemented in that technology connected to a gate of its own kind using an ideal delay-free transmission line (Fig. 1.1). This parameter is very useful for predicting the improvement in the speed of scaled digital CMOS circuits. Table 1.1 shows the relationship between intrinsic propagation delay time and scaling factor for three common scaling strategies where $s > 1$ is the scaling factor, U is the general scaling factor [1].

Fig. 1.1. Intrinsic propagation delay time for a CMOS gate. [1]

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Table 1.1. Relationship between intrinsic propagation delay time and scaling factor

PARAMETER	RELATION	FULL SCALING	GENERAL SCALING*	FIXED-VOLTAGE SCALING
W, L, t_{ox}		$1/S$	$1/S$	$1/S$
V_{DD}, V_T		$1/S$	$1/U$	1
$T_p(\text{intrinsic})$	$C_L V / I_{av}$	$1/S$	U/S^2	$1/S^2$
P_{av}	$C_L V^2 / t_p$	$1/S^2$	S/U^3	S

* For General Scaling $1 < U < S$

As can be seen here, for all three strategies the propagation delay time is decreasing as the transistors are scaled down. The total delay of the circuit however is somewhat different from the intrinsic propagation delay because there is also some delay associated with the interconnect lines. To take this effect into account the interconnecting line is modeled as a distributed resistor (R) and capacitor (C) as shown in Fig. 1.2.

Fig. 1.2. Distributed resistors and capacitor model of an interconnecting line [1]

Using the values of the distributed capacitor and resistor shown in Fig. 1.2, the total RC product of the interconnecting line is:

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$$RC = k\rho\varepsilon_0 \times \frac{L^2}{d \cdot t} \quad (1.1)$$

Where d , t , and L are dielectric thickness, interconnecting line thickness and interconnecting line length respectively and the latter one is usually proportional to total chip dimensions for global interconnecting lines.

With this ideal case formulation, the RC product of the interconnecting line would be independent of the scaling factor, S , because L^2 and $d \cdot t$ would scale with the same rate. In reality, however, total chip dimensions are not scaled down with the same scaling factor as device dimensions. In fact, as better processing methods are introduced (allowing better yield factors) chip dimensions are scaled up. Also because of the fringing phenomenon shown in Fig. 1.2, the distributed capacitor is not scaled down as fast as the distributed resistor is scaled up. These two effects cause a net increase in the RC product and consequently in the delay of the interconnecting lines as the minimum feature sizes are scaled down.

Based on the above discussion, as the minimum feature sizes get smaller, the percentage contribution of the interconnecting lines gets bigger. Consequently, it is predicted that for modern CMOS circuits the interconnect delay will be the predominant part in speed prediction calculations. One potential solution to this problem is using bigger transistors for deriving long interconnecting lines. To evaluate the effectiveness of this method the total delay of an inverter connected to a load using a real interconnecting line shown in Fig. 1.3 is derived to be [1]:

$$T_{delay} = 0.67R_{Tran}(C_j + C_{int} + C_L) + 0.67R_{int}C_L + 0.38R_{int}C_{int} \quad (1.2)$$

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Where R_{tran} is the resistance of the transistor in its on state which is a function of transistor dimensions. R_{int} , C_{int} , C_j and C_L are distributed resistor and capacitor of the interconnecting line, parasitic capacitor of the transistor and the load capacitor respectively. The last term in Equation (1.2) is the dominant part of the interconnect delay in modern CMOS chips and as can be seen, it is independent of the transistor dimensions (R_{tran}). This shows that using bigger transistors for deriving the interconnecting lines will be of little help in modern CMOS technologies.

Fig. 1.3. A CMOS inverter gate connected to a load using a real interconnecting line with all parasitic components

By expanding the last term in Equation (1.2) using Eq. (1.1), the Total Interconnecting Delay (TID) is found to be proportional to $k\rho L^2$. The square relationship of TID to L implies that breaking the interconnect line using repeaters will decrease TID by changing this square dependency to a nearly linear dependency [1]. This is in fact an effective way of reducing TID but it requires more active devices which directly translate to higher power consumption and larger chip area. A more interesting solution which does not have these drawbacks is reduction of R and k , which is in fact done in Copper-Low- k interconnect technology. For example, using Copper as the interconnecting metal with resistivity of $1.6 \mu\Omega\text{cm}$ compared to Al with resistivity

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of $3.3 \mu\Omega\text{cm}$ and *Perfluorocyclobutane* as dielectric with dielectric constant of 2.3 compared to 4.1 for SiO_2 , TID can be improved by a factor of 3.7 [123, 124]. Compared to the speed improvement that can be achieved from one generation to the other in modern CMOS technologies, this will be a huge improvement and a more sufficient motivation for Cu/Low- k interconnects research activities.

Fig. 1.4. RC delays as a function of the metal thickness for different interconnects

schemes: Al with low- k , Cu with SiO_2 , Cu with low- k and Cu with air (from Ref. [3]). Note that the RC decreases with the increase of metal thickness.

There is also another motivation for using Cu as the interconnecting metal. As minimum feature sizes get smaller and working frequencies go higher, the current densities get larger in modern CMOS technologies. This can cause some reliability problems. These problems are mostly caused by electro-migration of Al which can decrease life-time. It is proven that Cu has a much better electro-migration behavior

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compared to Al. By using Cu as the interconnecting metal, better reliability is then expected in modern CMOS technologies [2-3].

1.2.2 Technological issues

1.2.2.1 Problems with Cu Interconnection

Interconnection in integrated circuits is usually performed by depositing and patterning a metal layer on top of a dielectric material. The metal which is used for this purpose should be compatible with IC process technology and at the same time should show a small amount of resistivity. So far, Al is shown to give a good trade-off between these two requirements. Although Cu can give a resistivity of almost half of that of Al, it has some IC-compatibility problems.

A. The difficulties in etching

There is, in fact, no good recipes available for Cu etch. If Reactive Ion Etching (RIE) is used for Cu etch a lower etch rate (compared to Al) will be achieved which also suffers from rough side-wall and poor etch profile. This is mainly because the reaction between Cu and Chlorine takes place at low temperatures (just like Al) but its by-product is not volatile. Consequently Cu films are corroded instead of etched. This problem even gets more severe as copper does not provide a self protective layer (as Al does) and corrosion can attack inside [4]. Due to those difficulties a new damascene metallization method has been proposed and is being used for Cu metallization. In this damascene process the dielectric is first deposited and the interconnect trenches and via footprints are etched in it. Copper is then deposited on the wafer which fills these

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trenches and via. After a Chemical-Mechanical Polishing (CMP) step, the remaining Cu which forms via and interconnects is encapsulated by depositing another layer of dielectric.

For a long time, Chemical Vapor Deposition (CVD) had been tried for Cu deposition in damascene processes. It is shown, however, that using CVD for Cu deposition is not effective for filling narrow trenches and usually results in voids. For this reason CVD is not used for Cu deposition today. Instead, metal electroplating techniques are employed. It is shown that metal electroplating tends to have a greater deposition rate at narrow trenches filling them completely without forming any voids.

There are two damascene processes: single damascene and dual damascene. A single damascene process is a process in which interconnect via footprints and interconnecting lines are fabricated separately by dielectric fill, metal etch deposition and metal CMP. In a dual damascene process, however, Interconnect trenches and via footprints are filled simultaneously. This makes this process a simpler and consequently more cost-effective one. For this reason dual damascene process is more attractive and in fact an active area of research [2].

The process starts by depositing a layer of dielectric which serves as an isolation layer between two interconnect layers. An etch stop layer is then deposited on top of its layer. After patterning and etching of via footprints on this etch stop layer, another layer of dielectric is deposited on the wafer and the surface is covered by an anti reflective layer which helps for later lithographic process. The top dielectric layer is then patterned and etched down to the etch-stop layer at interconnect positions and all

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the way down to the lower interconnect layer at via positions. These trenches are filled by Cu deposition in the next process step. At the end, all Cu interconnects and via are encapsulated by deposition of another layer of dielectric after a CMP process removes excess copper from wafer surface [7].

B. Contamination

Copper contamination can be divided into two categories: Contamination in the same wafer and cross contamination between two wafers. Cross contamination can be avoided by having two separate clean-room facilities; one for Cu-interconnect wafers and one for non-Cu-interconnect wafers. This approach, however, is too expensive to be practical.

In practice some precautions are usually taken to avoid Cu Contamination. For instance, the embedded Cu features on the front side of the wafer are fully encapsulated and the backside is sealed to avoid spreading of Cu particles in other furnaces. Also some cleaning steps are normally added after CMP to ensure a Copper-free surface and a sufficient edge exclusion of Cu seed [5].

C. The Adhesion of Cu to SiO₂ and diffusion in SiO₂

Copper shows a poor adhesion behavior to SiO₂. This problem can be avoided if a dielectric material other than SiO₂ is used. If SiO₂ is to be used with copper, a buffering layer should be deposited between these two. It is usually tried that this layer serves also as the diffusion barrier layer [3]. Copper has a huge diffusion constant in silicon

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and Cu ions are quite mobile in SiO₂ layer. This enables them to migrate through the SiO₂ layer and reach the active area [5]. Looking at the deep acceptor levels of Cu, it is not surprising that Cu can easily increase the leakage currents and eventually ruin all active devices if it reaches the active area. A diffusion barrier should surround the interconnect lines to block diffusion of Cu to active area. The physical dimension of the final interconnecting line is bigger than the actual dimensions of the Cu line. The total resistor of the line will be:

$$R = \rho_{Cu} \cdot \frac{L}{W_w \cdot t_w} \quad (1.3)$$

where L is the length of the line and other dimensions are shown in Fig. 1.5.

The effective resistivity of the line, ρ_{eff} , is defined by the following equation:

$$R = \rho_{eff} \cdot \frac{L}{W_i \cdot t_i} \quad (1.4)$$

From Equation (1.3) and Equation (1.4), we will have

$$\rho_{eff} = \rho_{Cu} \cdot \frac{W_i \cdot t_i}{W_w \cdot t_w} \quad (1.5)$$

which is in fact larger than the resistivity of pure Cu. For practical dimensions the value of ρ_{eff} is around 2.4 $\mu\Omega\text{cm}$. this is greater than that of pure Cu (1.6 $\mu\Omega\text{cm}$) but is still much better than that of Al.

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Fig. 1.5. Using a diffusion barrier for Cu interconnects

1.2.2.2 Problems with low- k Materials

The usual dielectric used in IC industry is SiO_2 . This is mainly due to easy fabrication steps and compatibility with other materials used in normal fabrication technology. There are several criteria which are important in selection of a low- k material to be used instead of SiO_2 . Dielectric constant is of course the most significant one. In addition, thermal stability and isotropic dielectric properties are also important. The dielectric should be stable enough to tolerate high temperatures due to other processing steps as well as due to the normal operation of the chip without significant change in its electrical properties. Isotropic dielectric property should be taken into account because in modern IC technologies lateral parasitic capacitance between interconnecting lines is as important as the vertical one between two layers of interconnection [6].

There are also some reliability concerns related to the low- k dielectric material. The material should provide good integrity and gap fill behavior. Although having voids and gaps in the dielectric are decreasing its effective permittivity, they are not

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usually favorable because they seriously affect long-term reliability. Last but not least, is the electrical isolation. This includes break down voltage and leakage current. There should also be a good adhesion property between the low- k material and other layers, specially the copper layer [6].

Although there are a lot of materials that can show a permittivity lesser than that of SiO_2 , these practical considerations limit the number of candidates.

1.2.3 Objective and Scope:

Due to the previous problems, the main objective of this project is to study the Ultra low k (ULK) dielectric, characterizing and optimizing it for Deep Sub-micron Integrated Circuit (DSIC) application. Now, there are a large variety of dielectric candidates. In this project, the correlation of structure and properties as well as effects of integration processes on structure and properties of ULK porous SiLK will be studied.

A) Characterization of ultra low k

The electrical, thermal, mechanical, chemical and structural properties of the porous ULK film will be characterized using all possible means available. These will primarily include k value, adhesion, surface roughness, chemical component, structure and porosity.

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B) Investigation of the thermal stability of Cu/barrier/ultra low k structures in blanket wafer

There are two major issues in copper/ultra low k integration: one is the poor adhesion between copper and dielectric, the other is copper diffusion in the dielectric. In this part, the effect of barrier layer, such as widely used Ta and TaN, on adhesion and copper diffusion will be studied. The thermal stability and interfacial properties of Cu/Ta (or/and TaN)/ULK film stacks will also be evaluated in blanket structure. In addition, the copper adhesion improvement with ultra low k film as well as copper diffusion reduction in ULK film will be studied by surface modifications of ULK film or introducing an additional dielectric barrier layer SiCN.

C) Single damascene integration of Cu/barrier/ultra low k

The single damascene Cu line (metal 1) was fabricated in 0.13 μm technology node. The electrical properties and reliability of Cu/barrier/ultra low k structure in patterned wafer are evaluated by measuring the line resistance, line-to-line leakage and breakdown voltage at various conditions. The failure mechanism was also analyzed.

D) Develop new process to improve the electrical properties and reliability of Cu/barrier/ultra low k structures

Two methods will be developed to improve the reliability and electric performance of the Cu/barrier/ULK structure. One method is to modify the ULK surface using forming gas plasma N_2/H_2 treatment before barrier was deposited. The other method is

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depositing a thin SiCN film on the ULK surface before Ta barrier was deposited. The thermal stability, electrical properties, microstructure and other properties will be evaluated.

1.3 Major contribution of the thesis

The integration of Cu and ULK porous SiLK on blanket and patterned wafers has been investigated. This includes characterizations of materials, development of new processes and integration of Cu using single damascene (SD) structures in 0.13 μm technology. The materials studied in this project include ULK porous SiLK, three kinds of metal diffusion barriers (Ta, TaN and Ta/TaN bi-layer), dielectric diffusion barriers (SiCN), Cu seed layer. The thermal stability, interaction, electrical and physical properties were comparatively investigated by employing various technologies. The single damascene lines were fabricated of Cu and ULK porous SiLK with different barrier layers in 0.13 μm technology. The line resistance, line to line leakage and breakdown voltage were evaluated at various conditions. Furthermore, two methods, plasma treatment and introducing additional SiCN barrier layer, were developed to improve the electrical performance and thermal stability of Cu/barrier/ULK structure. Finally, the thickness of SiCN was also optimized by comparing the electrical performance with different SiCN thickness.

1.3.1 ULK Porous SiLK

The ULK porous SiLK, which is supplied by Dow Chemical Company with k value around 2.3, was characterized. Samples were annealed at various temperatures in order

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to study the thermal stability. Atomic force microscopy (AFM), X-ray diffraction (XRD), X-ray reflection (XRR), Fourier transform infra-red (FTIR), C-V and other equipments were employed to evaluate the roughness, porosity, thickness, adhesion, dielectric constant and other properties. The porous SiLK still keeps good properties after annealing at 500°C for 30 mins, including the surface roughness, thickness, adhesion, porosity and dielectric constant.

1.3.2 Diffusion barriers

Three kinds of diffusion barrier layers (Ta, TaN and Ta/TaN bi-layer) have been developed for the ULK porous SiLK, and the properties of these films such as sheet resistance, surface morphology and microstructure have been investigated. It was found that the Ta film shows body centered cubic (BCC) structure with lower resistivity and clear grain boundary. However, the TaN film shows smaller grain size and blur grain boundary due to the incorporation of N.

After being annealed at different temperatures, the barrier/ULK structures were found to lose the integrity at temperatures over 500°C due to the failure of ULK's properties, and significant diffusion was observable near the interfaces of the structures. The Ta/ultra low k porous SiLK shows the smallest sheet resistance but the poorest thermal stability while the TaN on ULK polymer shows the highest resistance but best thermal stability. The Ta/TaN bi-layer barrier takes the advantage of both Ta and TaN barriers and gives reasonable resistance and thermal stability.

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After being annealed at 400°C for different times, the sheet resistance and roughness of the barriers increase with the annealing time, the Ta-O compound was also detected. However, no abrupt change was observed till the annealing time of 150 mins. The SIMS results revealed that the oxygen is rich at the barrier/ULK interfaces, and the diffusion coefficient of Ta from the Ta barrier in porous SiLK is $0.023 \pm 0.001 \text{ nm}^2/\text{s}$, while the diffusion coefficient of Ta from the TaN in porous SiLK is only $0.0033 \pm 0.0001 \text{ nm}^2/\text{s}$.

1.3.3 SIP Cu layer

The effect of the three kinds of barrier layers underneath on the properties of self-ionized plasma (SIP) Cu films have also been studied using various techniques. It was found Cu (111), Cu (200) and Cu (220) textures were observed for three barriers. The results of the SIMS revealed that the significant increase of the sheet resistance was due to the diffusion of Ta and O to the Cu film. It was also revealed that the annealing at 400°C for more than 120 mins also caused diffusion of Ta and O and even Cu into the ultra low k porous SiLK. And the Ta and O diffused faster in the dielectric than in the Cu film. In addition, the out-diffusion of the C and H in the dielectric towards Ta and Cu layers was also observed and the H diffusion was found to diffuse faster than C.

1.3.4 Single damascene integration of Cu and ULK

The single damascene Cu line using three kinds of barriers (Ta, TaN and Ta/TaN) with and without SiCN and plasma treatment for Cu-ultra low- k interconnect in 0.13 μm technology has been investigated. The electrical tests indicate that the Cu lines with

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TaN and Ta/TaN bi-layer barriers exhibit smaller leakage current and higher breakdown voltage comparing with the Cu lines with Ta barrier. However, the line with Ta barrier has the smallest line resistance while the line with the TaN barrier has the highest.

It was found that the N_2/H_2 plasma treatment on the ULK surface before depositing barrier and Cu could reduce the line resistance significantly, but it also brought more surface defects on the sidewall and larger diffusion length. Compared with only the Ta and Ta-based barrier layer structure, introduction of an additional SiCN layer could significantly improve the breakdown voltage, line to line leakage and thermal stability. This is because the thin SiCN layer not only effectively blocks diffusion of elements on both sides, but also significantly improves the mechanical property of ULK. However, as the breakdown voltage and thermal stability increased with SiCN thickness increasing, it also brought higher line resistance. Four groups of samples with different thickness of SiCN layer were comparatively studied. The SiCN layer between 20 nm and 50 nm can give better electrical performance and thermal stability.

1.4 Organization of the thesis

Because the research of this project was carried out just following the back-end-of-line process step by step, the organization of this thesis shows the same order as the process. The details are showed as follows:

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Chapter 1 briefly introduces the background of Cu interconnects, provides many problems for the Cu integrated Circuit and solutions. It also shows the motivation and objective, major contributions and organization of this thesis.

Chapter 2 reviews the theory of dielectric, the development of ULK first, followed by the characterization of the UKL porous SiLK. It includes the dielectric constant, thickness, porosity, adhesion, micro-structure, chemical-bond at different annealing temperatures.

Chapter 3 presents the study of the three diffusion barriers (Ta, TaN and Ta/TaN) and their properties. In this chapter, we mainly focus on how sheet resistance, surface roughness and micro-structure vary with annealing temperature and annealing time. The diffusion coefficient of Ta in ultra low k for Ta and TaN barrier was also estimated from the SIMS results.

Chapter 4 discusses the thermal stability of Cu/barrier/ULK structures. The interaction between Cu, Ta-based barriers and ULK has been presented, and failure mechanism was discussed. The diffusion coefficient of Cu in different barriers was also calculated.

In chapter 5, the thermal stability of the Cu/SiCN/ULK structure on blanket wafers was evaluated, and then the properties of Cu/Ta(N)/SiCN/ULK structures were comparatively studied.

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Chapter 6 describes the effect of plasma treatment on the thermal stability of Cu/Ta(N)/ULK structures on blanket wafer.

Chapter 7 presents the integration of Cu and ULK in single damascene structure for deep submicron integrated circuit (0.13 μm) applications. The electrical parameters of the metal lines which include line resistance, line to line leakage and breakdown voltage were evaluated for different structures under various conditions.

The last chapter summarizes the conclusion and recommendations for the future work.

CHAPTER 2 Characterization of ULK porous SiLK

CHAPTER 2

Characterization of ULK porous SiLK

2.1 Introduction of low k and ultra low k dielectrics

Recent developments in microelectronics technologies have created a great demand for low dielectric constant materials. As we know that internet is the fastest growing industry of the 21st century, the low dielectric constant materials are one of the keys components of the internet devices that perform transmission, communication and storage functions. The world wide market in the 21st century for computer and other high performance memories will be a few hundred billions dollars per year. The interlayer dielectric materials with a very low dielectric constant will play a crucial role in the future generation for integrated circuits devices particularly for ultra large scale integration (ULSI) and high speed IC packaging. The shrinking metal spacing ($\sim 0.18 \mu\text{m}$ and below) in current IC devices is an indicator for a demand of low dielectric constant materials. Silicon dioxide which has a dielectric constant of about 4.0, is currently used in microelectronics packaging. However, materials with a much lower dielectric constant are in demand for the next generation of interconnects to reduce the transmission delay time in integrated circuits that would allow faster intra-chip and inter-chip communications. The aim of ultra fast chip speed can be achieved by reducing the resistance of interlayer metal and by lowering the dielectric constant of interlayer dielectric material. With this emerging view, currently semiconductor industries are considering to produce copper/SiO₂ interconnects and to move towards integrating low dielectric constant materials with copper instead of aluminum

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interconnects. The copper/low dielectric integration approach has been targeted for 0.13 μm generation microelectronics packaging technology to increase chip speed and reduce the number of metal levels and manufacturing costs.

2.1.1 Designing for ULK dielectrics

Though the successful integration of low k (2.7) spin-on deposition (SOD) and CVD films for the 0.13 μm generation has largely been accomplished, companies face significant materials and integration challenges at the 100 nm node and beyond. Because few fully dense spin-on or CVD materials with $k < 2.5$ satisfy the diverse requirements for successful integration. The materials need to meet a demanding list of electrical, mechanical, and chemical requirements to deliver the desired electrical performances, to enable compatibility with fabrication unit operations for high-volume manufacturing at high yield, and to ensure high device reliability in end use. Important low- k film properties include thickness and uniformity, dielectric constant, refractive index, adhesion, chemical resistance, thermal stability, pore size and distribution, coefficient of thermal expansion, glass transition temperature, film stress, and its copper diffusion coefficient [124]. Recent research efforts have focused on the preparation of porous materials, where the dielectric constant, k , scales with the host matrix density. Two main factors that affect the host matrix k are electronic and nuclear polarizability and density.

A) Polarizability

Dielectric constant depends on the summation of the polarizability from the electronic, ionic and polar components of the material (shown in Fig. 2.1). The

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electronic component refers to the oscillation of electrons in chemical bonds and/or in the extended supra-molecular structure. The latter two components constitute the nuclear response and are important at lower frequencies ($< 10^{13}$ Hz), while the electronic response dominates at higher frequencies (4.74×10^{14} Hz). At typical device operating frequencies, currently $< 10^9$ Hz, all three components contribute to the dielectric constant and must be minimized for optimum performance.

Fig. 2.1. Polarization phenomena which influence the dielectric constant.

The choice of a host matrix with low polarizability is aided by examining polarizabilities and the associated bond enthalpies for the atomic building blocks in the host material [13]. For instance, single C-C and C-F bonds have the lowest electronic polarizability, making fluorinated and nonfluorinated aliphatic macromolecules potential candidates for low k applications. Conversely, electronic polarizability is higher for materials containing a large number of carbon-carbon double and triple bonds because of the increased mobility of p electrons. Importantly, in practice, there is a trade-off in achieving a low dielectric constant and high bond strength (which leads to

CHAPTER 2 Characterization of ULK porous SiLK

thermal stability). Low-polarizability single bonds are among the weakest, while fluorinated aliphatic structures display poor adhesion, low hardness, and reactivity toward Ti- and Ta-based liners. In contrast, aromatic *p* bonding configurations have significantly higher bond strengths. Dow Chemical's SiLK material is an example of a cross-linked poly-aromatic matrix that largely eliminates the nuclear polarizability component and features high bond strength and, thus, excellent thermal resistance [18,19]. The chemical vapor deposition (CVD) and polymerization of small molecules containing o-ethynyl-substituted aromatics had been previously demonstrated elsewhere [19]. The high energy content of such systems made handling of the monomers somewhat hazardous. By incorporation of two or more o-ethynyl or o-phenylethynyl-substituted aromatic fragments in a compound of higher molecular weight, a spin-coatable material could be prepared that did not have such a high energy content and was thus safer to handle. These monomers can be partially polymerized in solvent to further control the exotherm and form oligomers that have excellent gap-fill and planarization properties. Once cured on the wafer, a cross-linked poly-naphthalene structure is formed that exhibits excellent thermal stability. The approach that was commercially implemented as SiLK dielectric involves the synthesis of cross-linked poly-phenylenes by the reaction of poly-functional cyclopentadienone- and acetylene-containing materials (Fig. 2.2) [20]. Polyphenylenes are known to have excellent thermal stability [21]. Typically, however, polyphenylenes need to be substantially substituted in order to achieve solubility and thus processability. By preparing the polyphenylenes from cyclopentadienone- and acetylene- containing monomers, the initial oligomers formed are soluble without undue substitution and can thus be processed. Further reaction on wafer converts the oligomers to cross-linked polymers that have properties suitable for use as interlayer dielectrics. The cyclopentadienones

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react with the acetylenes in a 4+2 cycloaddition reaction followed by the expulsion of CO to form a new aromatic ring. The multifunctional nature of the monomers leads to cross-linked polyphenylene systems after full cure.

Fig. 2.2. Formation of cross-linked polyphenylene by the reaction of polyfunctional cyclopentadienone- and acetylene substituted monomers [20]

Permanent and transition dipoles in the low k material contribute to its nuclear polarizability. The response is dominated by polar functionality, such as hydroxyl and carbonyl groups. Unfortunately, these groups can attract water ($k = 78.5$) via hydrogen bonding interactions, which can drastically elevate the dielectric constant. This suggests that an optimal low k material should be devoid of polar functionality containing oxygen or nitrogen that attracts and binds water.

B) Managing density

The matrix dielectric constant can also be lowered by decreasing its density. Researchers achieve lower density by incorporating low molecular weight atoms and/or

CHAPTER 2 Characterization of ULK porous SiLK

adding more free volume to the structure. For example, the lower dielectric constant of non-polar organic polymers (~2.0-2.8) compared to SiO₂ (3.9-4.2) is partly due to the presence of lighter C and H atoms vs. Si and O, as well as the low packing density (~1.0 g/cm³) compared to the dense tetrahedral silica network (~2.4 g/cm³). The incorporation of non-polar and space-occupying groups such as methyl, ethyl and phenyl (R groups) will also increase free volume in a silica network, Optimized loading of R groups in a random silsesquioxane or silica network results in steric congestion, which interferes with polymer chain packing and attractive forces, which could lead to crystallization or areas of higher density. The result is a reduction in dielectric constant from 2.9 for HSQ to 2.5-2.8 for MSQ and other R-substituted silsesquioxane-based SOD. A natural extension of the strategy is the introduction of nanometer-sized pores into the material. Porosity's effect on dielectric constant can be predicted using the Bruggeman effective medium approximation (EMA) model [12]:

$$f_1 \frac{k_1 + k_e}{k_1 + 2k_e} + f_2 \frac{k_2 - k_e}{k_2 + 2k_e} = 0 \quad (2.1)$$

where $f_{1,2}$ represents the fraction of the two components, $k_{1,2}$ the dielectric constant of the components, and k_e the material's effective k . The simple EMA model assumes two components to the film — the solid wall material and voids — and provides the basis for ellipsometric measurement of film thickness, density, and index of refraction on porous or multi-component thin films. Using this model, one can predict dielectric constant as a function of porosity for SiO₂ ($k = 4.0$) and a $k = 2.5$ host materials. These results infer that, by initially choosing a host matrix with a lower k value than SiO₂, significantly less porosity is needed to achieve the lowest target k value.

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C) Level of porosity

Advantages of minimizing the porosity needed to obtain a low k value include greater mechanical strength and greater thermal conductivity of the interlayer dielectric (ILD). To decrease potential for cracking and delamination — and thus ensure device structure integrity — pore sizes should be as small as possible, though some sources recommend no greater than 20% of the smallest feature size [13]. Engineers prefer to work with closed-cell architecture because of increased mechanical strength and resistance to absorption and diffusion of process chemicals. Studies show that Young's modulus decreases with increasing porosity, an important concern in CMP processing [13]. Thermal conductivity also decreases with increasing porosity [13], as the propagation of thermal energy flow through the matrix is interrupted by the nano-scopic voids. This suggests that the ILD material should have sufficient thermal conductivity or a circuit architecture that is optimized to avoid joule heating.

The synthetic chemist can take a variety of approaches in the preparation of ultra-low k SODs with controlled incorporation of porosity. The initial and most widely used approach relies on the incorporation of a thermally degradable material (porogen) within a host thermosetting matrix [23]. Upon heating, the matrix material cross-links, and the porogen undergoes phase separation from the matrix to form nano-scopic domains. Subsequent heating leads to porogen decomposition and diffusion of the volatile by-products out of the matrix. Under optimized processing conditions, a porous network results in which the pore size directly correlates with the original phase-separated morphology. This template-porogen-based approach forms the basis for the National Institute of Standards and Technology (NIST)/IBM/Dow Chemical joint project on porous dielectrics, which began in 1999. The two most prominent materials

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derived from the ultra-low-k portion of this venture are Dow Chemical's porous SiLK and IBM's DendriGlass materials. The template strategy offers versatility and extendibility of the host matrix from one generation to the next, since the matrix material remains constant and only the loading of porogen varies. The approach is applicable to a wide range of materials, both inorganic to organic, and to a range of porogen structures. The critical feature of a template approach is the design and structure of the polymeric porogen. On the nanometer scale, the porogen must phase separate from the thermosetting matrix and decompose entirely, leaving no residue. Dow designed porous SiLK featuring a k value of 2.0 and pore sizes < 20 nm. As with inorganic and hybrid systems, the porogens should be homogeneously dispersed within the cross-linked matrix without gross phase separation, which leads to large pores and open-cell architectures after porogen decomposition. With organic hosts, porogen decomposition must occur below the host's glass transition temperature (T_g). Otherwise, the void structure may collapse in the softer and more rubber-like environment.

2.1.2 Low k and ULK materials available

The candidates for future low-k ILDs fall into two classes of materials. The first one is comprised of a set of inorganic, silica-based oxides:

- Doped SiO_2 (F-doped, with composition SiO_xF_y and abbreviated as FSG for fluorosilicate glass; or C-doped)
- Hydrogen silsesquioxane ($\text{HSiO}_{3/2}$, abbreviated as HSQ). Related materials with composition $\text{RSiO}_{3/2}$, where R is a side group other than H, are also under investigation.
- Xerogels (porous SiO_2)

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- Air gap structures (metal wiring where the spaces between metal lines are only partially filled with SiO₂, and thus contain voids).

The second class of prospective ILD's involves a variety of organic polymers, for example:

- Non-fluorinated (benzocyclobutene, parylene-N, FLAR2.0, SiLK, Black Diamond, Coral, various polyimides, etc.)
- Fluorinated (perfluorinated cyclobutene, parylene-f, FLARE1.0, teflon, fluorinated amorphous carbon, etc.).

Two main deposition processes are developed for the low k dielectrics. All low-k CVD and spin-on materials have strengths and weaknesses. Proponents of CVD approaches, most notably carbon-doped siloxanes (OSGs) with k ranging to below 2.5, claim reuse of existing toolsets and simpler integration due to the silicon dioxide-like structure of CVD siloxanes. OSGs also represent the most limited departure from the standard SiO₂ dielectric. Alternatively, manufacturers of spin-on materials and spin-on dielectric (SOD) tracks contend better extendibility to future generations, especially in the sub-2.5 μ m range when porous low-k materials likely will be used. Today, porous versions of many low-k spin-ons are available for testing, whereas porous CVD low-k materials have yet to be demonstrated. Some spin-on materials may also require a smaller pore volume to attain ultra low k ($k < 2.2$) than CVD films, which may contribute to higher mechanical integrity, better film stability and easier integration. Companies on both sides claim about 80% of the overall low-k inter-level dielectric (ILD) market. Both sides also tout a lower cost-of-ownership [15]. Table 2.1 categorizes the majority of materials offered to the industry for consideration. The materials need to meet a demanding list of electrical, mechanical, and chemical

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requirements to deliver the desired electrical performances, to enable compatibility with fabrication unit operations for high-volume manufacturing at high yield, and to ensure high device reliability in end use. Most of the offerings are not ideal in at least one important criterion for the application. For example, the Si-based systems (SiCOH, porous silica, silsesquioxane) lack sufficient toughness at the targeted low-dielectric-constant; F-containing systems are incompatible with common metal liners; Some of the organic polymer systems are mechanically unsuitable at process temperatures because of low glass transition temperature (T_g); and the thermal stability of benzocyclobutene (BCB) and some other polymer systems do not meet the process temperature requirements. The scarcity of efficacious candidates prompted the Semiconductor Industry Association to identify the criticality of low k materials development and implementation.

In this work, the ultra low k porous SiLK was chosen as the interlayer dielectric. Its k value is around 2.3, which deeply depends on the porosity, and the glass temperature (T_g) is about 490°C. Porous SiLK is developed by Dow Chemical Company for answering the integration challenges of the 65 nm node and beyond. The family of SiLK semiconductor dielectric resins has been formulated not only to deliver the highest-quality low k dielectric available, but to ease integration now and into the future. It combines an industry leading low k value ($k = 2.2$) with superior material properties and uncomplicated integration with existing manufacturing proven technology. Smallest, closed-cell pore sizes enable continuous Tantalum barriers and low CTE, combining to surpass attributes offered by any other low- k material. SiLK resin is already proven at 130nm and 90nm, demonstrating performance, integration properties and reliability. Porous SiLK resin provides a proven path to extend the

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learning and financial investment to 65nm, 45nm and beyond [125-128]. This is the main reason to choose this particular dielectric for integration with Cu. So the objective of this project is to characterize the ultra low k , mainly on its thermal stability, and investigating the changes in mechanical, electric properties under annealing at various temperatures, then optimizing the process parameter for future Cu metallization of integrated circuits.

Table 2.1. Classes of dielectric materials evaluated for on-chip interconnect fabrication [19].

Materials	Dielectric constant	Deposition process
Silicon dioxide	3.9-4.5	PECVD
Fluorosilicate glass (FSG)	3.2-4.0	PECVD
Polyimides	3.1-3.4	Spin-on
H-silsesquioxane	2.9-3.2	Spin-on
Organosilicate glass (SiCOH)	2.7-3.3	PECVD
Parylene-N	2.7	CVD
Benzocyclobutene polymers	2.7	Spin-on
Fluorinated polyimides	2.5-2.9	Spin-on
Methyl-silsesquioxane	2.6-2.8	Spin-on
Poly(arylene ether)	2.8-2.9	Spin-on
Aromatic thermosets	2.6-2.7	Spin-on
Parylene-F	2.4-2.5	CVD
Teflon AF	2.1	Spin-on
Porous silica(aerogel and xerogel)	1.1-2.4	Spin-on

2.2 Thermal stability of ULK porous SiLK

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2.2.1 Introduction

A significant reduction in RC delay can be achieved by introducing a low permittivity polymer into the interconnect structure. Heat resistant, non-polar or slightly polar polymers are potential candidates for Inter-Metal Dielectric (IMD) in future devices. Therefore, some dozens of polymers are under investigation to prove their utility as IMD material. However, the introduction of polymers as IMD materials affords the investigation of a lot more properties than the dielectric constant. It must be considered that polymers exhibit lower Young's module, lower thermal conductivity, lower thermal stability, and higher coefficient of thermal expansion (CTE). The anisotropic thermal, electrical, and mechanical properties of some of the polymers cause additional problems. Nevertheless, for most polymers, thermal stability is the crucial point. Metallization is responsible for the thermal budget in backend-of-line processes. Depending on the number of metal layers, the polymer dielectric must withstand 400-450°C several times (10-15 times) for half an hour without changing the properties. So, firstly, the thermal stability of ultra low k porous SiLK was evaluated, and measurements of the dielectric constant and the mechanical and electrical properties were carried out before and after thermal treatment.

2.2.2 Sample preparation

The (100)-oriented p-type silicon (8 in-dia) wafers were chosen as substrates. A 600 nm-thick porous SiLK layer was coated on the substrate directly by spin-on technology. Porous SiLK resin is a solution of a low-molecular-weight aromatic thermosetting polymer. The polymer molecular weight and solution concentration were tuned to

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enable precise and convenient deposition by spin-on technology, a technique universally used by the industry for the deposition of photoresist materials. The low-molecular-weight polymer will flow to fill gaps smaller than 0.2 μm and planarize underlying topology, a requirement of some interconnect fabrication schemes [19, 125-128]. The film was baked at 320°C for 90s on a hot plate under nitrogen immediately to remove solvent and to form the oligomeric film. The baked layer was further cured at temperature of 430°C for 30 mins in N_2 ambient [11]. At last, the nanometer pore can be achieved. Firstly, the thickness and refract index were measured by optical probe. We select 49 points on the sample, and the average thickness is 603.2 nm, and the refract index (RI) is 1.55, less than that of dense SiLK 1.63 ($k = 2.65$) due to the lower density [19].

Fig. 2.3 and Fig. 2.4 are the cross sectional SEM and TEM images of the porous SiLK respectively. From the SEM image, we can see the uniform thickness. From the TEM image, the pore structure and size can be observed. The matrix (pore wall) connects with each other and pore size ranges from 10 nm to 20 nm.

Fig. 2.3. SEM of porous SiLK (thickness 600 nm)

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Fig. 2.4. TEM of porous SiLK

To study the thin film's thermal stability, samples were annealed at temperatures ranging from 300°C to 600°C for 30 mins under Ar ambient by furnace. The time for temperature increasing and decreasing is 3 mins and 5 mins respectively.

2.2.3 Dielectric constant

The dielectric constant was determined by the standard C-V measurement using a mercury probe system at lower frequencies (0.1 KHz). Fig. 2.5 shows k value as a function of annealing temperature. The minimum k value is 2.01 after annealing at 400°C for 30 mins. From the figure, it is seen that firstly, k value decreases a little with increasing annealing temperature. There are two possibilities for the decreasing in k value. When the samples were annealed, the pore wall is decomposed, so the pore will be conjunct with the close pores and form a bigger one, which results in higher porosity and lower k value. The other possibility may be that samples absorb a little water vapor ($k = 78.5$) after being exposed in air ambient, which increases k value. High temperature annealing removes the vapor, so the k value drops. When the annealing temperature is more than 500°C, higher than the glass transition (490°C), k value

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becomes much higher. The surface color also changes from brown to green, at last to gray, which suggests the reflective index changed.

Fig. 2.5. Impact of annealing temperature on porous SiLK permittivity.

To explain the result, let's go back to the depositing process. SiLK resin is a solution of a low-molecular-weight aromatic thermosetting polymer. The polymer turns into an insoluble film after curing. The selected repeating unit and cross-link chains in the polymer can optimize the combination of T_g and mechanical roughness with lower dielectric constant. When annealing temperature is too high, the repeating unit possibly breaks down, and the polymer structure might also be destroyed and turned into small molecules. These result in higher k value. The theory of plastic or polymer behavior in high temperature is presented in Ref [90, 91, 110], and our XRD & FTIR experiment results also show the long chain molecular breakdown and removal of some bonds when being annealed in temperature beyond its T_g . Another reason is that porosity and its size in the film decrease under higher annealing temperature (shown in Fig. 2.9), which results in high k value.

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2.2.4 Thickness

The thickness of the thin film is a very important physical parameter. When measuring the dielectric constant by C-V standard measurement, the thickness of the film must be input correctly and accurately, otherwise, the result will not be credited. However, the thickness will change significantly because the pore wall decomposes and pores collapse when being annealed at high temperature. Generally, the thickness can be measured by the surface profilometer. Fig. 2.6 shows the thickness changing with annealing temperature. From the curve, we can see the thickness drop slowly till annealing at 500°C (from 600 nm to 520 nm), and the significant change happened at 550°C (from 520 nm to 390 nm), which means the film failed after being annealed at this temperature. From the manufacturing standpoint, the thickness specification limit of film is normally set as $\text{Target} \pm 10\%$ [153, 154]. So if the thickness drifts 20%, it means the film failure. In this case, the thickness changes from 520 nm to 390 nm, and the reduction is about 25%.

Fig. 2.6. Thickness changing with annealing temperature

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2.2.5 Density and porosity tests used X-ray reflection (XRR)

The density and porosity of porous SiLK can be measured by X-ray reflection (XRR). At an x-ray wavelength of a few tenths of a nanometer, the refractive index of most materials is less than one. Hence, there exists a critical angle below which total external reflection of the radiation takes place.

Fig. 2.7. X-Ray reflectivity geometry. Here θ is the incident and reflected angle, and 2θ is the scattering angle.

This critical angle, θ_c , can be approximated as $(\rho_e \lambda^2 / \pi)^{0.5}$, where ρ is the electron density in the material, λ is the x-ray wavelength, and $r_e = 2.818 \text{ fm}$ is the classical electron radius. All the angles used within the context of X-ray reflectivity are defined as grazing angles measured from the surface parallel. At any incident angle below θ_c total reflection occurs. In a typical specular X-ray reflection (SXR) measurement, the reflected intensity is collected as a function of the incident angle as it is continuously varied through the critical angle. By modeling SXR the result with a one-dimensional Schrodinger equation, the details of the electron density depth profile can be deduced. Free-surface roughness, interfacial roughness, and density variations in the thickness

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direction can also be determined using computer modeling to create electron-density depth profiles that best fit the experimental data. The information reported here from SXR is an average over a lateral dimension of a few micrometers as dictated by the coherence length of the x-ray beam [37,38].

The XRR curves were measured using the Siemens D5005 x-ray diffractometer. The Cu Ka X-ray of 1.54 Å operated at 40 kV and 40 mA. The data was collected with the grazing incident angle equal to the detector angle, and the angle ranged from 0° to 2°. Hence, there exists a critical angle below which total external reflection of the radiation takes place [38]. This critical angle θ_c can be approximated by:

$$\theta_c = \lambda \sqrt{\frac{N_A r_o}{\pi} \rho_{eff} \frac{X_C Z_C + X_H Z_H + X_O Z_O}{X_C M_C + X_H M_H + X_O M_O}} \quad (2.2)$$

where $r_o = \frac{e^2}{4\pi\epsilon_o mc^2}$ is the classical electron radius, m is the electron mass, and N_A is the Avogadro number. Z_j is atomic number of element j , and M_j is molar mass. In this work, the polymer was made of C, H and O, so $Z_C = 6$, $Z_H = 1$, $Z_O = 8$, and $M_C = 12$, $M_H = 1$, $M_O = 16$. Fig. 2.8 gives out the spectra of X-ray reflectivity of porous SiLK being annealed at various temperatures, then we can get the critical angle according every curve (list in Table 2.2).

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Fig. 2.8. X-ray reflectivity curves showing critical angle changing with annealing temperatures.

There is no independent information about the wall density and porosity. The porosity of the film must be determined from the SXR data with estimation of the wall material density. If one assumes that the density of the material between the pores is that of a typical thermal oxide, 2.25 g/cm^3 , then the corresponding porosity will be 75.6% by volume. If one assumes that the density of the material between the pores is that of a typical hydrogen silsesquioxane spin-on glass material, 2.00 g/cm^3 , then the corresponding porosity will be 72.6% by volume.

Table 2.2. Critical angle of porous SiLK after being annealed at various temperatures

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Annealing temperature	Porous SiLK critical angle θ_c (deg)	Si critical angle θ_c (deg)
As deposited	0.136	0.197
300°C	0.132	0.199
400°C	0.133	0.197
500°C	0.136	0.197
550°C	0.142	0.198

The validity of the above wall density assumptions can be tested by using a complementary experimental technique. The mass density of the thin film as a whole is simply a product of the connecting material density between the pores, ρ_w , and the volume fraction occupied by the material, $1-P$ (P is porosity). From the SXR and composition data, we have thus determined only the average film mass density. The remaining objective is to apply a second independent technique to obtain another measurable quantity also related to both ρ_w and P . With two measurements containing ρ_w and P in different forms, one can solve the simultaneous equations and deduce the value of ρ_w and P experimentally. In this work, we have known the chemical composition of porous SiLK, and X_c , X_H , X_o is 0.6, 0.39, and 0.01 respectively. So the average mass density can be calculated using equation (2.2). In this work, we used the simplest description of a porous material; a two-phase model where one phase comprises the voids and the other comprises the connecting material. The material between the voids (the pore wall materials) is assumed to be uniform in density. So the

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relationship among the average mass density ρ_{eff} , wall materials density ρ_w and porosity P can be expressed as:

$$\rho_{eff} = \rho_w(1 - P) \quad (2.3)$$

Fig. 2.9 shows the relative porosity P changing with the annealing temperature. At first the P value increases. The reason is because when being annealed at low temperatures, the pore wall is decomposed, so the pore will be conjunct with the neighboring pores and forms a bigger one, which results in porosity increasing. When annealing at higher temperatures, the porosity decreased significantly. The T_g of this porous polymer film was known to be about 490°C. The decreased porosity above this temperature could be due to the softening of the polymer matrix and the viscoelastic flow of polymer chains. This flow might have caused the pore to be rearranged or collapse.

Fig. 2.9. Porosity of porous SiLK versus annealing temperatures.

TEM is performed to observe the pore size and distribution. Fig. 2.10(a) shows the TEM images of as-deposited thin film of porous SiLK. From the figure, we can see the

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pore size ranging from 10 to 15 nm, and the uniform distribution. Fig. 2.10(b) shows the TEM image of the thin film annealed at 550°C for 30mins. We can see the pore size is much bigger than that of as-deposited film, from 20 to 30 nm. However, due to the un-uniformity distribution, the k value has a slight higher than that of as-deposition. The interface between porous SiLK and Si can also be seen clearly. When annealed at 550°C for 30 mins, no diffusion happened at the interface, and the boundary still keeps good.

Fig. 2.10. TEM images of porous SiLK. (a) as-deposited (b) annealed at 550°C for 30 mins

2.2.6 Adhesion

The adhesion can be measured by scratch test equipment. Firstly, the sample was sticked on the hold by glue, and then a diamond tip is used to scratch the surface. The press force ranges from 0.03 N to 28 N till to get the failure point. At last optical review was preformed to confirm the failure point. Fig. 2.11.a (red line) and Fig. 2.11.b (point F) both show the failure point, and where the force is equal to 6.875 N. Fig.

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2.11.c shows the adhesion force increasing with the annealing temperature increasing. However, when the annealing temperature is higher than 550°C, the uniformity of the thin film is not good, and the deviation is very larger with different measurements. The film in some areas can be easily stripped from the substrate with very small force, only 2.37 N, which deeply relates with the property of the thin film. When being annealed at high temperature, parts of the thin film have been carbonized.

Fig. 2.11. Scratch test showing failure point detected by acoustic and optical (a)

acoustic (b) optical (c) adhesion changing with annealing temperatures

2.2.7 Surface morphology

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The roughness can be evaluated by atomic force microscopy (AFM). The AFM measurements were performed with a Nanoscope III, (Dimension 3000, Digital Instruments) in contact mode using silicon tip. Root mean square (RMS) of roughness values was obtained using Nanoscope software.

Fig. 2.12 shows the surface morphology at various annealing temperatures ranging from 300°C to 600°C for 30 mins. No significant changes were observed below 500°C, and the surface still keeps smooth as shown in Fig. 2.12.a-d. However, when the sample is annealed up to 500°C, higher than T_g (glass transition temperature, about 490°C for porous SiLK), the roughness is increasing with temperatures, but no compressive buckling of the stressed layer is observed.

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Fig. 2.12. AFM images of porous SiLK at various annealing temperatures for 30 mins.

(a) as-doposited; (b) annealed at 300°C, (c) 400°C, (d) 500°C, (e) 550°C, (f)

600°C. Fig. 2.13 shows RMS value changing with annealing temperatures. The scanning areas are 5×5 μm, and we choose three points to measure in every sample, and then calculate the average. From the figure we see that annealing at 400°C can get smooth surface. Furthermore, the different scanning area gets same conclusion, which proves good uniformity of the spin-on film.

Fig. 2.13. RMS changing with annealing temperatures on scanning area of 5×5 μm.

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2.2.8 X-ray diffraction and FTIR results

The analysis of the elemental composition of thin films is often aided through the diffraction techniques, which can uniquely identify crystalline phase near a solid surface. X-ray diffraction is most suitable to films thicker than a few hundred angstroms. To limit the penetration of the beam and enhance the diffraction pattern of the film with respect to the substrate glancing angle geometries are used. Individual crystalline phases are identified by their characteristic diffraction patterns. Such X-ray patterns also reveal information on the orientation and size distribution of the crystallites.

The basis of X-ray diffraction is the Bragg equation, which describes the condition for constructive interference for X-ray scattering from atomic planes of a crystal. The condition for constructive interface is:

$$2d \sin \theta = n\lambda \quad (2.4)$$

where λ is the wavelength of the incident radiation.

The x-ray diffraction measurements were performed to analysis the phase structure of the ULK SiLK. With grazing incident angle 6° , XRD patterns were detected from $2\theta = 20^\circ$ to 80° with scan speed of 4° min^{-1} and scan step 0.05° . Four peaks were observed for the as-deposited sample as shown in Fig. 2.14(a), which means the film is made of nano-crystal. However, with increasing annealing temperature, the intensity of peaks becomes weak because parts of nano-crystal change into amorphous. The peaks abruptly disappear after annealing up to 550°C . It is because the polymer bond has been

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broken down and the film became amorphous. However, no chemical transformation occurs at the interface because no new phases were detected by X-ray diffraction.

Fig. 2.14. A series of X-ray diffraction patterns showing the difference when being annealed at various temperatures for 30 mins. ($\omega = 6^\circ$).
(a) as-deposited; (b) 400°C , (c) 500°C , (d) 550°C , (e) 600°C .

Fig. 2.15 shows the comparison of FTIR spectra of annealed porous SiLK at various temperatures. After being annealing at 500°C , the peaks of CH stretch from phenyl ring (wavenumber 2964), CH rock from furan (wavenumber 1258), CH bending (d(CH)) from Phenyl- (wavenumber 1023,801) and CH from furan (wavenumber 1262) become weaker than those of as-deposited film. When the annealing temperature is 600°C , all characteristic peaks almost disappear. Many chemical bonds break down and H release from the thin film, which results in higher k value.

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Fig. 2.15. Spectra of FTIR of porous SiLK after being annealed at different temperatures.

2.3 Effect of annealing time on the properties of ULK

In the previous section, we mainly discussed the properties of ULK affected by annealing temperature. However, in the industry back end of microchip fabrication, no thermal treatment higher than 450°C was carried out in metallization, which is responsible for the several thermal budget in back end of line process. But annealing at < 450°C for several thermal cycles was usually needed. For instance, in this work, A 600 nm thick porous SiLK layer was coated on the substrate directly by spin-on technology, and then baked at 320°C for 90 s on a hot plate under nitrogen immediately to remove solvent and to form the oligomeric film. The baked layer was further cured at 430°C for 30 mins in N₂ ambient. Under this temperature, the porogen will be separated from the thermosetting matrix and decompose entirely, leave no radius [11]. At last, the nanometer pore can be achieved. The global interconnects at least undergo

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several cycles of thermal treatment. Therefore, it is necessary to investigate the properties of ULK changing with annealing time.

Samples with 600 nm thick ULK was annealed at 400°C for several thermal cycles in high vacuum, and each cycle is 30 mins. The C-V measurement and AFM results show there is no significant change in the dielectric constant and surface roughness. The k value changed from 2.3 to 2.32, only 0.8% increment after being annealed for 150 mins. At the same time, the surface roughness also changed from 1.225 nm to 1.318 nm, and 7.5% increment. It is reasonable because the polymer show good thermal stability when the annealing temperature is lower than its T_g [11]. Longer time annealing has been done by one M.Eng candidate in our group. He annealed the samples in nitrogen (N_2) ambient at 450 °C for different periods of time (from 1 to 9 hours). X-ray reflectivity (XRR), Fourier-transmission-infra-red (FTIR), X-ray photoelectron spectroscopy (XPS) were applied for characterization of the atomic structure / porosity of the dielectric films, while deep-level-transient-spectroscopy (DLTS) technique was used for the defects characterization of the material. Minimum value of the mass density at the 5 hours of annealing was originated by a competition among reduction of the film thickness and increase of pore size at the annealing. Defect peaks with densities up to $10^{16} \text{ eV}^{-1} \text{ cm}^{-3}$ have been detected at the 0.3 – 0.5 eV below the conduction band bottom [114].

2.4 Summary

This chapter presents investigations on the spin-on thin film, porous SiLK, which has lower dielectric constant (about 2.3). Samples were annealed at various

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temperatures in order to study the thermal stability. AFM, XRD, XRR, C-V and other techniques were employed to evaluate the electrical and mechanical properties, such as roughness, porosity, thickness, adhesion, dielectric constant and so on. It was revealed that the porous SiLK could still keep good properties after annealing at 500°C for 30 mins. For the annealing above 500°C, the abrupt change of electrical and mechanical properties was observed. This is because when annealing temperature is higher than the glass transition temperature, the repeating unit in ULK possibly breaks down, and the polymer structure might also be destroyed and turned into small molecules.

CHAPTER 3 Comparative studies of Ta, TaN and Ta/TaN bi-layer barriers for ULK porous SiLK

CHAPTER 3

Comparative studies of Ta, TaN and Ta/TaN bi-layer barriers for ULK porous SiLK

3.1 Review of barriers for Cu

The benefits of an interconnect technology depend on the properties of the metal and the interlayer dielectric (ILD). From the previous analysis, it is clear that Cu/low k dielectric will replace Al/SiO₂ for the future integration circuits. However, the practical feasibility of a certain metal/ILD combination ultimately rests to a large extent on the characteristics of the interface between the metal and ILD. The use of Cu as the metal, either with SiO₂ or a low k dielectric as ILD, presents a unique challenge primarily because the Cu/ILD interface is in general much less strong than the corresponding Al/ILD interface. In the context of metal/ILD interface issues, three properties of copper are especially important and pose a much greater problem than with aluminum.

- (1) Cu adheres poorly to most ILD materials because it does not interact strongly with them.
- (2) Cu oxidizes easily, and its oxidation is not self-limiting,
- (3) Cu diffuses readily through undoped SiO₂.

Cu is of course an extremely undesirable impurity in Si, as it forms a generation/recombination center for free charge carriers. For instance, diffusion parameters for Cu diffusion in Si are found as follows [37]:

$$D_o = 4.7 \times 10^{-3} \text{ cm}^2/\text{s} \quad E_a = 0.43 \text{ eV}, \quad 300 \leq T \leq 700^\circ \text{C}$$

and

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$$D_o = 4.0 \times 10^{-2} \text{ cm}^2/\text{s}, \quad E_a = 1.0 \text{ eV}, \quad 800 \leq T \leq 1100^\circ \text{C}$$

Furthermore, sputtered Cu on Si form copper silicides at the Cu/Si interface after being annealed at 200°C for 30 mins [38], so that copper silicides layer with high resistivity induces a time delay and Joule heat generation.

The data on Cu diffusion through low k ILDs such as doped SiO₂ and polymers are incomplete at this time, but it is likely that Cu diffusion will be a serious problem there, too. Consequently, Cu must be used with a thin interlayer film (barrier) between it and ILD. This additional layer must correct the three problematic properties of Cu mentioned above; it must provide the “glue” to insure good metal/ILD adhesion, it must protect the Cu from oxidation, and it must act as a barrier for the diffusion of Cu into the ILD.

Another constrain on the diffusion barrier arises from electrical considerations. Given the low electrical resistance of copper, the barrier material will by necessity have a much higher resistance than the Cu itself. Hence the barrier must be thin enough so as not to have a negative impact on the via resistance and the overall electrical conduction properties of the metal wiring. At the same time, the barrier must be thick enough to prevent the diffusion of copper. As the widths of metal lines, and thus barrier thickness are continually being decreased, in parallel to the downscaling of feature sizes, the demands on the barrier stability are becoming ever more stringent.

Suitable barrier materials against Cu diffusion and undesirable interaction between Cu and either Si or SiO₂ have been developed. These include Ta [39], Ta-Si-N [40], Ti, TiN [41], W [42] and TaN [43]. However, the quality and properties of the Cu film are

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sensitive to the barrier materials on which the Cu film is deposited. Among these materials, Tantalum is presently one of the most widely used copper diffusion barrier materials in copper metallization because it shows not only relatively high melting temperature ($T_m = 3270$ K) but also is known to be thermodynamically stable with respect to Cu [44]. Some paper reported the ionized metal plasma (IMP) Ta and Ta-base compound for SiO₂ and other low k dielectric. In this chapter, we will present the SIP (self-ionized plasma) Ta, TaN and Ta/TaN bi-layer for the ultra low k porous SiLK. SIP PVD was introduced by Applied Materials. They refer to this source as self-ionized plasma, and the internal of re-coil in their IMP source to ionize the sputtered metal atoms is not needed. The source operates at relatively low pressures with a target-to-substrate distance that is increased above the distance used in conventional magnetron sputtering sources. The term self-ionized plasma probably refers to the phenomenon in which some of the sputtered metal atoms that are ionized by the source return to the target with enough energy to sputter other metal-atoms. These additional electrons ionize more of the sputtered metal atom, which keep the plasma self-sustaining and produces more metal-ions. The phenomenon is apparently an efficient way of ionizing metal-atoms that have small ionization energy [129]. SIP offers a cost-effective, single-chamber PVD solution for Ta, TaN and liner/barrier for intermediate to advanced devices. SIP extends PVD performance to sub-0.25 μ m geometries with >7:1 aspect ratio features. Its high bottom coverage (>25%) is twice the bottom coverage of standard PVD-results in high throughput and low Cost of Ownership [130].

3.2 Properties of as-deposited SIP Ta, TaN and Ta/TaN bi-layer barriers on porous SiLK

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Ta, TaN and Ta/TaN bi-layer of 25 nm thickness were deposited separately onto porous SiLK(600 nm)/Si substrates using SIP technology. The as-deposited films were characterized using various analysis techniques. These include AFM for surface morphology and roughness, XRD for crystallographic orientation, and four-point probe for sheet resistance.

3.2.1 Sheet resistance

The purpose of the 4-point probe is to measure the resistance of any semiconductor material. It can measure either bulk or thin film specimen, each of which consists of a different expression. The 4-point probe setup consists of four equally spaced tungsten metal tips with finite radius (as shown in Fig. 3.1). Each tip is supported by springs on the other end to minimize sample damage during probing. The four metal tips are part of an auto-mechanical stage which travels up and down during measurements. A high impedance current source is used to supply current through the outer two probes; a voltmeter measures the voltage across the inner two probes (See Fig. 3.1) to determine the sample resistance. Typical probe spacing is ~ 1 mm.

Fig. 3.1. Schematic of four-point probe configuration

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For a very thin layer (thickness $t \ll s$) we get current rings instead of spheres [131, 139]. Therefore the expression for the area $A = 2\pi xt$. The derivation is as follows:

$$R = \int_{x_1}^{x_2} \rho \frac{dx}{2\pi xt} = \int_s^{2s} \frac{\rho}{2\pi t} \frac{dx}{x} = \frac{\rho}{2\pi t} \ln(x) \Big|_s^{2s} = \frac{\rho}{2\pi t} \ln 2 \quad (3.1)$$

Consequently, for $R = V/2I$, the sheet resistance for a thin sheet is:

$$\rho = \frac{\pi t}{\ln 2} \left(\frac{V}{I} \right) \quad (3.2)$$

Note that this expression is independent of the probe spacing. Furthermore, this latter expression is frequently used for characterizing semiconductor layers, such as a diffused N^+ region in a p-type substrate. In general, the sheet resistance $R_s = \rho/t$ can be expressed as:

$$R_s = a \left(\frac{V}{I} \right) \quad (3.3)$$

where the factor a is a geometric factor. In the case of a semi-infinite thin sheet, $a = 4.53$, which is just from the derivation. The factor a will be different for non-ideal samples.

Table 3.1 shows the sheet resistance and roughness of the three barriers deposited on the porous SiLK/SiO₂/Si substrate. For comparison, the data published for the barriers directly deposited on Si substrate are also included. As shown in the table, the resistivity of Ta, TaN and Ta/TaN bi-layer barriers deposited on the ULK porous polymer are 55, 272 and 84 $\mu\Omega\text{cm}$, respectively. Because the film's thickness is only 25 nm, there are more defects in the film. Some grain states are in amorphous and quasi-amorphous, and the crystalline grain is also small, so the measured result is higher than the general value [45]. α -Ta is 30 $\mu\Omega\text{cm}$, and TaN is approximately 200 $\mu\Omega\text{cm}$. The Ta has the smallest resistance while the TaN has the largest. The resistance

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value of the Ta/TaN bi-layer is understandable as the Ta layer is on the top and dominates the conduction. Compared to the resistance data deposited on Si substrate, the resistance values of the Ta and TaN deposited on the ULK is slightly greater likely due to the difference in the smoothness of the substrates. In addition to the resistance, Table 3.1 also shows the surface roughness of the three kinds of barriers deposited on the ULK. They are 7.3, 6.9 and 7.7 nm respectively. These data are much greater than that deposited on Si due to the difference of the smoothness of the substrate.

Table 3.1. Resistivity and roughness of Ta, TaN and Ta/TaN deposited on Si and ULK porous SiLK

	α -Ta		TaN		Ta/TaN bi-layer	
Substrate	Si	ULK	Si	ULK	Si	ULK
Resistivity ($\mu\Omega\text{cm}$)	15-60 [Ref. 45 & 46]	55	200-250 [Ref. 47]	272	-	84
Roughness (nm)	-	7.3	0.33	6.9	0.54	7.7

3.2.2 Surface morphology

Fig. 3.2 shows the surface morphology scanned by AFM. The scanning area is $5 \times 5 \mu\text{m}$. Five points were measured and the mean roughness of Ta, TaN, Ta/TaN are 7.3 nm, 6.9 nm, 7.7 nm respectively (as shown in Table 3.1). There is no significant difference among them. To get more detail of the microstructure, we improved the resolution, and selected the scanning area of $2 \times 2 \mu\text{m}$. The comparison of Ta and TaN are shown in Fig. 3.2(d-e). The grain boundary of Ta film can be observed clearly, which is in general considered as extended defects acting as fast diffusion paths [48,49].

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However, the TaN film shows smaller grain size and blur grain boundary due to the incorporation of N [58].

Fig. 3.2. AFM image of: (a) Ta 5×5 μm; (b) TaN 5×5 μm; (c) Ta/TaN 5×5 μm; (d) Ta 2×2 μm; (e) TaN 2×2 μm

3.2.3 Microstructure of Ta, TaN and Ta/TaN deposited on porous SiLK

The textures of the Ta, TaN and Ta/TaN bi-layer barrier films were examined by XRD analysis and the results are shown in Fig. 3.3. For the Ta barrier, three characteristic peaks were observed. They are centered at 38.5°, 55.6°, 69.6°. They

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correspond to Ta (110), Ta (200), and Ta (211), respectively, which are the features of α -Ta [50]. This observation is the same as the recently reported one by Tokei et al [51]. However, in our case, the Ta and the ULK can be uniformly deposited so that the α phase of the Ta barrier is detectable in most of the 8 inch wafer. The mechanism of α phase formation will be discussed in section 3.2.4.

With addition of N_2 gas flow, TaN thin film can be deposited on the substrate by SIP. From Fig. 3.3(b), we can see the peak TaN (111) width is boarder than that of Ta peaks, which means that the TaN film may be quasi-amorphous as it is a mixture of amorphous and some fine grain, which can be verified from our XRD results and there is a very broader and smaller peak in XRD patterns as shown in Fig. 3.3. The grain size is smaller than Ta. The reason is that nitrogen atoms are incorporated into the Ta lattice, and the structure will shift from crystalline to amorphous. The grain size becomes smaller. It is non-columnar nano-crystalline structure, which is quite favorable for barriers. The TaN microstructure was also discussed in section 3.2.4.

For the bi-layer barrier, the peaks observed are exactly the same as that observed in the Ta layer except the difference in the peak intensities. That is, the Ta layer deposited on the TaN layer also has α phase. Since the bi-layer barrier has the TaN deposited on the ULK, followed by the Ta layer on the top, and the TaN layer should have a structure shown in Fig. 3.3(b). This observation clearly indicates that the Ta deposited on TaN have the same phase as that directly deposited on the ULK.

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Fig. 3.3. XRD patterns of as-deposited (a) Ta, (b) TaN, and (c) Ta/TaN bi-layer films.

The grain size t can be estimated from the XRD results by the Scherrer equation [50]

$$t = \frac{0.9\lambda}{B \cos \Theta_B} \quad (3.4)$$

where λ is the wavelength of the X-ray source, 0.154 nm in the present case, $2\Theta_B$ is Bragg angle, and B is the full width at half maximum (FWHM) at $2\Theta_B$. The calculated grain size values for Ta (110), Ta (200), and Ta (211) are 10.6 nm, 12.4 nm and 8.6 nm, respectively, but for TaN (111), the grain size is only 4.6 nm.

3.2.4 Mechanism of Ta and TaN texture formation

We can see from Fig. 3.3 that the Ta film has BCC (Body Centered Cubic) structure. In general, using R.F. magnetron sputtering it is possible to deposit two kinds of Ta film. One is α -Ta, and the other is β -Ta. They have different structure and sheet resistance, which can be distinguished by XRD and four-point probe [50]. The α -Ta is of BCC structure. It grows in a crystalline state with grain size of several microns. The

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β -Ta is of tetragonal structure. It is typical for columnar-grown grains (shown in Fig. 3.4). In addition, the resistance of α -Ta is lower than that of β -Ta.

Fig. 3.4. Tetragonal β -Ta unit cell according to Moseley and Seabrook, seen from the (001) (left) and (010) directions (right). The cell dimensions are $1.019 \times 1.019 \times 0.531$ nm. The atoms can be thought of as forming two (pseudo-) hexagonal planes with different orientations, while eight atoms lie halfway between the hexagonal planes. The grey atoms form the hexagonal plane at $z = 0$, the light atoms the hexagonal plane at $z = c/2$, and the black atoms lie in the 'intermediate' planes at $z = c/4$ and $3c/4$ (the c -axis is taken in the z -direction) [64].

In general, the Ta films directly deposited on Si, SiO_2 and other low k materials substrates in the pure Ar plasma are of high resistivity metastable tetragonal phase (β -Ta). Extensive studies have been made on correlations between the properties of the Ta films and the deposition conditions, substrate nature, and impurities incorporated. Hieber and Mayer demonstrated that evaporated Ta films initially start as β -Ta and transform into α -Ta as the film thickness is increased to several hundred nanometers

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[52], Shewartz and Feit showed the defects of impurities on inhibiting the beta to alpha phase transition [53]. In addition Thornton and Hoffman [54], and Jankowski [55] all demonstrated that Ta films sputter-deposited at low pressures were intrinsically compressively stressed (α -Ta) and Ta films deposited at high pressures were intrinsically tensile stressed (β -Ta).

As generally accepted, Ta films sputtered onto silicon based substrates prefer to nucleate and grow into tetragonal beta Ta phase. However, the α -Ta film is desirable because of its smaller resistivity compared with that of β -Ta film [50]. We also found that the texture of PVD Cu seed layer shows a strong preferred Cu (111) orientation when the Cu seed layer was deposited onto the low-resistivity alpha Ta film, whereas a more random orientation of crystallographic planes was observed in the case the Cu deposited onto β -Ta. The strong Cu (111) texture in the Cu seed layer will promote a similar texture in the electroplated plane layer and hence reduce electro-migration effects in the Cu line.

In recent years, people have been searching harder for the method of direct deposition of α -Ta on the Si-based substrate and several methods have been successfully developed. The α -Ta could be obtained by changing some conditions, such as the bias to the substrate, substrate temperature [56], plasma parameters, and phase transformation [56, 57] or by using epitaxial related growth mechanism promoted by lattice matched cubic under-layer such as Ti, Nb, Al, Cr, Ta₂N and W [58-59]. However, disadvantages arising from the above process conditions include the deposition onto temperature sensitive dielectric materials, which eliminates high

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temperature deposition as well as problems of process control and reliability arising from the controlled introduction of film contaminants. As barrier thicknesses shrink below 10nm, the introduction of base layers or ‘sandwiched’ structures will become increasingly impractical, especially if reactive sputter deposition is involved such as in the case of a TaN/Ta structure. In our case, the Ta films deposited directly on the ultra low k porous SiLK without any special treatment was cubic structure with $\rho = 55 \mu\Omega.cm$. So it is useful to find the mechanism of cubic Ta formation on the ultra low k porous SiLK.

Peter Klaver and Barend Thijsse [64] reported the results of classical molecular-dynamics simulations of BCC and β -phase Ta thin films. The various inequivalent atomic positions in β -Ta have substantially different individual cohesion energies. They are shown in Fig. 3.5 along with the different relaxed vacancy formation energies at these positions. For comparison, in BCC Ta the cohesion energy is 8.09 eV and the relaxed vacancy formation energy is 2.86 eV. The average atomic cohesion energy of the β -phase is 8.01 eV, 0.08 eV less than the value for the BCC phase. A difference of 0.08 eV may be somewhat large for a structure which is still stable in experiment at up to 1000 K [64]. That is why Ta films sputtered onto silicon based substrates prefer to nucleate and grow into tetragonal beta Ta phase and the phase transformation from β to α -Ta can be observe after annealed.

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Fig. 3.5. View of a β -Ta crystal along (001) direction with atoms shaded according to their cohesion energy E_c (negative of the potential energy). The top plane is a hexagonal plane. Also indicated are the relaxed vacancy formation energies E_v at different atomic sites. The atom marked '1' is the atom in the centre of the unit cell in Fig. 3.4. Type-3 atoms have been marked with small white circles. A few hexagons have been drawn to indicate the orientation of the hexagonal planes [64].

The unexpected formation of the low resistivity Ta phase, when deposited directly on the porous SiLK substrate at room temperature, is thought to be related to the chemical nature of the dielectric and interaction between the dielectric and the Ta film during initial stages of film growth. This interaction and hence the phase formation of the Ta film and its resistivity can be controlled by the Ta deposition conditions such as wafer bias.

In this case, the alpha Ta deposition condition is listed as follows:

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Temperature: Room temperature; Wafer bias: 150 V; Process pressure: 1.90~2.0 mT;
DC power: 20 kW; Ar flow: 30 sccm.

However, only beta Ta phase can be achieved when Ta is deposited on the SiO₂ at the same condition. Obviously, the Ta phase is depended on the substrate properties. Generally, the Ar plasma was applied to treat the substrate surface before Ta deposition, which is also called 'pre-clean'. Because the hardness of SiO₂ (6-7 GPa) is larger than that of porous SiLK (0.25-0.38 GPa), surface atoms of porous SiLK are created more than that of SiO₂ after treatment by Ar plasma. Here, the surface atoms are those atoms which lack five or more nearest or next nearest neighbors [64]. In the discussion of chapter 2, we know the porous SiLK is mainly made of C, H, and O, and the chemical compositions of porous SiLK, X_c , X_H , X_o are 0.6, 0.39, and 0.01 respectively. Small amounts of carbon introduced into the near surface-region of the porous SiLK layer during pre-clean is a possible candidate to facilitate formation of α -Ta during the early stages of film growth as identified in the early work by Schwartz et al [65,66]. In the literature, several references can be found that report the formation of Ta-C bonds at the interface when Ta is deposited on substrates containing carbon [105], due to the high formation of the Ta-C bond ($\Delta_f H^0(TaC) = -34.44$ kcal/mol) [106]. The pre-cleaning plasma has introduced radicals and new carbonyl bonds on the surface. Upon metallization, this would definitely enhance the adhesion due to the formation of metal-carbon bonds. Energetic ions (Ta) can break C-C or C-H bonds, and the free radicals resulting under these conditions can only react with other surface radicals or with other chains in the chain transfer reactions. Therefore, they tend to be stable. After Ta is deposited on the surface, they thereby have an opportunity to react and form Ta-C bonds [105-107, 134-136]. This thin TaC layer can work as the lattice matched cubic

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under-layer and then promotes the α -Ta formation. The formation detail and microstructure of TaC has been reported by K. W. Gerstenberg [106] and T. Laurila [137]. It is cubic structure. In Pg 59, we have reviewed some papers on the promoted epitaxial growth by lattice matched cubic under-layer such as Ti, Nb, Al, Cr, Ta₂N and W [58, 59]. In this case, the TaC existing at the interface of Ta and ULK can be proved by SIMS results and the similar XRD patterns were also observed from the cubic α -Ta deposited on other cubic underlayer [50, 58, 59]. The formation of the C-Ta bond is the key reason for the improvement for metal/ULK adhesion [105]. So at the interface between the ULK and the α -Ta film, a transition layer with high intermixing forms. A considerable number of Ta atoms are dispersed in the ULK matrix, either un-reacted or in the form of Ta-C crystallites [106, 107].

After we discussed the mechanism of alpha Ta formation, we will introduce the TaN microstructure formation in the following. In this case, TaN was also prepared by SIP technique by introducing N₂ and Ar gas mixture. Many researches have studied the phase composition and microstructure of the as-deposited TaN films and their dependence on N content [70-72]. The phases sequentially formed by sputtering tantalum under increasing amounts of nitrogen partial flows include nitrogen-incorporated cubic Ta (α -Ta(N)), hexagonal Ta₂N and NaCl-type TaN. The effectiveness of these barrier layers in terms of chemical inertness for Cu metallization appears to follow a direction reverse to the phase formation order, that is from TaN, Ta₂N, α -Ta(N) to β -Ta [58]. Riekkinen et al. reported that the hexagonal TaN phase could be formed by introducing the N₂ partial flow 5% [70]. Yang et al. also reported that the FCC TaN phase was formed as N₂ partial flow increasing up 15% in the sputtering gas [71]. In our case, the N₂ gas flow was fixed at 20% in the sputtering gas

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mixture. As shown in Fig. 3.3 b), the diffraction peaks at the angles of 37° could be assigned to FCC TaN (111) [71]. As far as the formation of the cubic TaN is concern, according to Wakasugi et al. [72], both hexagonal and cubic (FCC) TaN have triangle basic lattices of Ta in (001) and (111), respectively. The directions of the triangles orient differently from each other. The lattice constant of the FCC TaN is smaller than hexagonal close-packed (hcp) TaN [72] and it is required to rearrange the direction of triangle lattices and reduce the Ta-metal planes distance for the formation of cubic TaN. When N atoms impinge on the sites, the N atoms screen the interaction between metal planes. The Ta atoms has a degree of freedom of displacement with rotation and /or translation and the tightening of the N-Ta bonding may occur to reduce the inter-planar spacing. Therefore, the increase of N allows the possibility of the structure to change into cubic from hexagonal [72]. M. Hecker [113] studied the influence of N content on microstructure and thermal stability of Ta-N thin film on Si substrate. R Hubner [112] and T Riekkinen [47] reported the structure, stability and properties of TaN on SiO₂. All conclusions shows there are no significant difference of TaN properties on Si and SiO₂ substrates. With N content increasing, the TaN will change from hcp-Ta₂N (5% N₂ flow), hexagonal TaN (10% N₂ flow) to FCC TaN (15% N₂ flow).

3.3 Effect of annealing temperature on the barrier properties

3.3.1 Introduction

Heat treatment is an important and indispensable link in the fabrication of semiconductor devices, because it gives rise to interface diffusion and reaction that significantly improve the device contacts by the formation of metal silicides and /or

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carbides/graphite in metal/Si and SiC systems. On the other hand, it results in a degradation of electron device and limitation of the microminiaturization of electron devices due to possible agglomeration and lateral diffusion of the metal film. So the thermal stability is a very important item to evaluate the barrier function. Many researchers have studied the Cu/Ta(N)/SiO₂ structures, particularly their phase control, electrical properties and reliability [60-63]. In this section, we report the electrical, interfacial and structural properties as well as thermal stability of Ta, TaN and Ta/TaN bi-layer barriers deposited on the ultra low k porous SiLK.

3.3.2 Experimental procedures

To study the properties and the thermal stability of the three kinds of barriers, Ta, TaN and Ta/TaN, on the ULK, the barriers with a thickness of 25 nm were deposited separately onto ULK (600 nm)/SiO₂/Si substrates by SIP technology. After the as-deposited structures were characterized using various techniques, they were annealed at temperatures ranging from 450°C to 600°C for 3 mins in high vacuum by rapid thermal process (RTP). The times for temperature raising and dropping are 1 mins and 5 mins, respectively. The annealed samples were then evaluated by four-point probe, AFM, XRD and TEM. The AFM was performed with a scanning probe microscope (SPM-9500J2, SHIMADZU) in contact mode using silicon tip. The XRD measurements were carried out with a Philip X-pert using a grazing incident angle of 2°. The θ -2 θ scanning was from 20-90° with scanning speed of 3° per minute and a scan step of 0.05°. So we can get the sheet resistance, roughness and character peaks changing with the annealing temperature, then optimizing the process for Ta(N)/ULK/Si structure and selecting the favorable barrier for porous SiLK.

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3.3.3 Results and discussion

Fig. 3.6 shows the sheet resistance as a function of the annealing temperatures. After thermal treatment, the sheet resistance of the TaN/ULK structure almost has no change till an annealing at 550 °C, and the increase after this temperature is not very significant. For the Ta barrier, the sheet resistance increases slowly up to 500 °C, and abruptly then after. The bi-layer barrier, however, follows the trend of Ta up to 500°C and is then close to the value of the TaN above this temperature.

Fig. 3.6. Sheet resistances of three kinds of barriers deposited on ULK porous SiLK as a function of annealing temperature.

There are two factors that affect the sheet resistance after annealing. One is diffusion. Some of Ta atoms in the metal layer can diffuse into the polymer, which reduces the thickness of the Ta film. Similarly, some atoms in the polymer, such as C, H, O, can easily diffuse into Ta film to form resistive Ta oxide and carbides with increasing annealing temperature. This explanation can be verified by our XRD and SIMS results, as shown in Fig. 3.13a & b. A large amount of O can be detected at the surface of the

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Ta and the interface between Ta and ULK. The large O concentration at the interface is likely because the porous SiLK probably absorbs vapors after being exposed in air. However, fewer O atoms are detected in the Ta layer. After being annealed, the O concentration rises with annealing time, as shown in Fig. 3.13(b). This indicates that the O atoms diffuse into Ta lattice slowly along the grain boundaries as well as the ULK porous SiLK. As the annealing time increases, more and more O atoms diffuse into the Ta barrier and form Ta₂O₅, which coincides with the XRD results. The Ta sheet resistance increases because Ta oxide has higher resistivity [48]. For the thickness change, it can be verified by the TEM results, as shown in Fig. 3.9 a. For the TaN film, the nitrogen in the film mostly accommodates near the grain boundaries, which reduces intermixing. Therefore, the sheet resistance changes very little even after being annealed at 600°C. The change of the sheet resistance of the Ta/TaN bi-layer is slightly more than that of TaN but much less than that of the Ta. This is mainly due to the presence of TaN in the bi-layer structure. In addition, the crystal discontinuity in the bi-layer structure also plays a role in reducing intermixing.

The other factor is the surface roughness. Iacopi has studied the relationship between sheet resistance and surface roughness for metal/porous material structure [67]. As annealing temperature increases, there are more open pores at the interface formed, and the mechanic property of the polymer also changes significantly, so the residual stress in the barrier layers can be easily released by extruding the substrate, which causes rougher interface. Many metal atoms can enter the open pores, and the thickness of barrier also becomes thinner, which leads to the sheet resistance increasing. For the metal atoms entering the open pores and the thickness of Ta becoming thinner can be observed from TEM results as shown in Fig. 3.9a. Iacopi *et al* [107] reported the

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sealing properties of the Ta(N) layers on top of porous low k films are evaluated by ellipsometric porosimetry, and the strong correlation between sheet resistance and substrate surface roughness was also presented. It is similar to our experimental results.

The surface of three kinds of barriers after annealed at 550°C for 3 mins appears frosted. The AFM inspections in top-down (Fig. 3.7) and cross section TEM (Fig. 3.9) mode reveal buckling of the whole barrier/ULK film. This relaxation mode was identified as wrinkling (short wavelength instability) with rigid base [108]. Thin compressed films can relax through buckling till a compromise is reached between the stress release by expanding out of the nominal plane and the elastic stresses generated by film bending. Huang [142] reported the wrinkling of an elastic film on a viscous layer. Their study provides a theoretical model for the wrinkling process. The elastic film is modeled with the nonlinear theory and the flow of the viscous layer is modeled with the theory of lubrication. Similar phenomena can be observed from our AFM results, so we suspected the elastic stresses generated by film bending. On the other hand, thin film can buckle at still lower load if unconstrained. This can happen for either free standing films or for films deposited onto viscous or viscoelastic (high compliant) substrates, as reported by Sridhar *et al* [91, 109]. Relaxation in such a mode is thus possible for lower critical stresses provided the polymer undergoes a transition from elastic to visco-elastic behavior. This can take place through creep phenomena already at temperatures that are fractions of the polymer T_g . when the ULK film is under conditions of high stress and temperature, and enough energy can be available to initiate a viscous flow through motion of the chains. Segments of polymer chains tend to pack parallel to one another, and since the covalent bonds along the chain are much

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stronger than the van der Waals bonds between the chains, a gliding motion between the chains is favored [90, 110].

Fig. 3.7. Surface morphology of three kinds of barrier layers after being annealed at 550°C for 3 mins. (a) Ta/ULK (b) TaN/ULK (c) Ta/TaN/ULK.

Fig. 3.8(a-c) shows the XRD patterns of Ta, TaN and bi-layers Ta/TaN on ULK after annealing at various temperatures. As seen from Fig. 3.8(a), the intensity of the Ta peaks becomes lower and the width becomes broadened significantly as the annealing temperature increases. This is due to the diffusion of C and O atoms into the Ta film, which results in formation of amorphous Ta oxide carbide and Ta consumption. The C and O atoms diffused into Ta film can be confirmed by SIMS results (Fig. 3.13) and the intermixing area can also be observed in TEM results (Fig. 3.9). No peak of TaC and TaO are observed from the XRD results because in this case the TaC and TaO exist in amorphous not polycrystalline structure due to the lower annealing temperature. If the annealing temperature is higher, their structure will transfer from amorphous into polycrystalline and the peaks can be captured by XRD [43, 44, 49, 61]. It should be pointed out that in the Ta/ULK XRD pattern, the peak centered at 55.6° is a combined result of two textures. One is the Ta (200) peak, and the other is the substrate Si. It is because the incident glancing incidence angle is 2° , the X-ray can penetrate the Ta and

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ULK film to the Si substrate. With annealing temperature increasing, the Si information becomes stronger due to the reduction of the diffraction from the Ta/ULK structure. For the TaN/ULK XRD pattern, as we discussed in section 3.2.4, its microstructure is significantly dependent on N concentration. For the as-deposited TaN film, in this case FCC structure is obtained and TaN (111) peak was observed. However, after being annealed, the N released from TaN film, and at the same time, the microstructure is changed from FCC TaN to Ta₂N. The structure of Ta₂N is hexagonal; with nitrogen randomly occupying the interstitial site while Ta occupying the lattice sites. As indicated in the diffraction diagrams, annealing at 450°C results in the commencing formation of Ta₂N, which peaks at 55.5° [111, 112, 113]. Of course, this peak also includes the information of Si. After being annealed at 600°C, the TaN (111) peak disappeared (as shown in Fig. 3.8 (b)). This means that TaN almost is completely changed into Ta₂N. For the Ta/TaN bi-layer barrier, the peak centered at 55.5°C includes the information of Ta (200), Ta₂N (200) and Si. The peak centered at 38.5° is still strong after being annealed at 600°C although the Ta peak in the Ta/ULK and TaN peak in the TaN/ULK both become lower. These observations clearly indicate that the lattice discontinuity at the Ta/TaN interfaces plays an important role in reducing the diffusions. As a result, only the Ta and TaN layers near the ULK are affected significantly while the texture of the metal film on top side is less affected.

As for the grain size, annealing makes them smaller. For example, after being annealed at 600°C for 3 mins, the grain size of Ta (110) is reduced to 5 nm. The reduction of the grain size is likely a result of mutual diffusion of C, O and Ta atoms, which results in formation of amorphous TaO_x or TaC_x and Ta consumption.

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Fig. 3.8. XRD patterns of the samples after being annealed at indicated temperatures (a) Ta/ULK, (b) TaN/ULK, and (c) Ta/TaN/ULK.

To directly observe the interaction at the interfaces, the cross-sectional TEM images of the three structures with different barriers, after being annealed at 550°C for 3 mins, were examined, and the results are shown in Fig. 3.9. As seen from the images, the Ta/ULK shows the widest interface between the barrier and the ULK, while the TaN/ULK has the narrowest interface. For the Ta/TaN bi-layer/ULK structure, the interface is much narrower than that of Ta/ULK but slightly wider than that of TaN/ULK structure. These observations are in good agreement with the change in sheet

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resistance and the XRD results. The buckling interface also corresponds to the wrinkling surface morphology.

Fig. 3.9. TEM images of three samples after being annealed at 550°C for 3min: a) Ta/ULK b) TaN/ULK and c) Ta/TaN bi-layer /ULK.

3.4 Effect of annealing time on the barrier properties

3.4.1 Introduction

In the previous section, we mainly discussed the properties of barrier/ULK structures after being annealed at different temperature. It is believed that significant change happened after being annealed at 500°C which is higher than the T_g (490°C) of porous SiLK. However, as discussed in chapter 2, the industry microchip fabrication and interconnects in the wafer process undergo at least several cycles (depending on the number of metal layers). Therefore it is necessary to investigate how the properties of the barrier/ULK systems change with annealing time. In chapter 2, we have discussed the properties of porous SiLK which do not change significantly after being annealed at

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400°C for 150 mins. In this section, we will discuss the effect of annealing time on the properties of Ta/ULK and TaN/ULK structures on blanket wafers.

3.4.2 Experiment procedures

The samples studied are Ta/ULK/SiO₂/Si and TaN/ULK/SiO₂/Si structures. The Si substrates used are 8-inch p-type Si (100) wafers. Firstly, 200 nm SiO₂ is deposited by plasma enhanced chemical vapor deposition (PECVD), and then 600 nm porous SiLK is deposited on the SiO₂ by spin-on technology. Two kinds of barriers, Ta, and TaN, with a thickness of 25 nm were deposited separately onto porous polymer (600 nm)/SiO₂/Si substrates by SIP technology in Ar and Ar+N₂ mixing gas, respectively.

The samples were annealed at 400°C in high vacuum of 10⁻⁶ Pa for several thermal cycles by RTP. Every thermal cycle is 30 mins. The electrical and physical properties of the structures were characterized after each cycle. The characterization techniques include four-point probe for sheet resistance, AFM for surface morphology, XRD for crystal structure, and SIMS for diffusion profile. The XRD measurements were performed with Philip X-pert using a grazing incident angle of 1°. The 2 θ scanning was carried out from 2 θ = 20-80° with scanning speed of 3° per minute and scan step 0.05°. The depth profile of different elements in the Ta/ULK/ SiO₂/Si and TaN/ULK/ SiO₂/Si was studied using a CAMECA IMS-6f instrument. The Cs⁺ primary beam extracted at 4 kV was made incident on the sample at 2 kV, thus yielding a net impart energy of 2 keV. The primary beam was rastered across the sample surface over an area of 250×250 μm^2 and the central circular area of 60 μm diameter of the rastered portion was assessed by the mass spectrometer. The samples were rotated during measurements

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in order to reduce the effect of roughness.

3.4.3 Results and discussion

3.4.3.1 Sheet resistance

The sheet resistance is a very important parameter for the thin film. It is used not only to estimate the microstructure of the film, but also to monitor the intermixing and diffusion between the barrier and the underlying ULK layer. The Ta films were reported to exhibit two different crystallographic phases, stable bulk BCC structure (α -phase) with smaller resistivity (typically 30 $\mu\Omega\text{cm}$) and metastable tetragonal structure (β -phase) with larger resistivity (more than 200 $\mu\Omega\text{cm}$) [50-55]. The Ta film used in our work has α phase with a sheet resistance of about 22 Ω/square or a bulk resistivity of 55 $\mu\Omega\text{cm}$. The sheet resistance of TaN is dependent on the nitrogen content. In this work, the sheet resistance of TaN is 94.7 Ω/square , corresponding to a bulk resistivity of 272 $\mu\Omega\text{cm}$, which is slightly higher than the reported 250 $\mu\Omega\text{cm}$ [50].

After thermal treatment at 400°C for different periods of time, the Ta and TaN sheet resistances as a function of annealing time are shown in Fig. 3.10. As shown in the figure, the sheet resistance of Ta has no significant change after being annealed for 30 mins. It then increases abruptly after being annealed for 60 mins and more. For the TaN barrier, however, the sheet resistance shows significant change only after being annealed for 120 mins. It is clear that TaN barrier has better thermal stability as compared to Ta, but it also shows the larger sheet resistance values.

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Fig. 3.10. Sheet resistance changing with annealing time for Ta/ULK and TaN/ULK structures.

3.4.3.2 Surface morphology

The surface morphology of the as-deposited Ta and TaN has been described in section 3.2.2. After thermal treatment at 400°C for 30 mins, the roughness of the two structures increases drastically, and it then increases slowly after further annealing, as shown in Fig. 3.11. This can be understood from the difference between the mechanical properties of the barriers and the ULK porous SiLK as well as the growth of the grains during thermal annealing. The ULK can experience a transition into viscous flow at temperatures which are only fraction of the material T_g and may thus fall within the typical temperature ranges for damascene processing. In particular, the Ta film with an intrinsic compressive stress of about 2 GPa deposited onto a blanket ULK can undergo stress relaxation through wrinkling, allowed by the transition of the polymer into viscous behavior around 280°C [90]. Polymeric materials are prone to creep, as their structure allows a gliding motion between material chains [91]. The mismatch

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coefficient of thermal expansion (CTE) of Ta and the ULK are 5.2 ppm/K and 60 ppm/K. The mismatch introduces higher stress in Ta layer, where relaxation is allowed by the compliance of porous dielectrics. This causes the roughness increasing significantly after being annealed. The same phenomena can also be observed from the AFM and TEM results presented in section 3.4.3.4. Therefore, the growth of the grains and the release of the stress during thermal annealing will cause greater roughness. For the TaN/ULK structure, it has similar change in roughness as Ta/ULK structure (as shown in Fig. 3.11).

Fig. 3.11. Roughness of Ta/ULK and TaN/ULK as a function of annealing time at 400°C.

3.4.3.3 XRD results

Fig. 3.12 shows the XRD patterns of Ta/ULK and TaN/ULK structures after being annealed at 400°C for different periods of time. For the as-deposited Ta/ULK structure, three characteristic peaks of Ta film are observed, as shown in Fig. 3.3. They are centered at 38.5°, 55.6°, and 69.6°, corresponding to Ta (110), Ta (200), and Ta (211), respectively. These are the features of α -Ta [50]. With increased annealing time, the

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peak intensity of Ta (110) decreases and the width also becomes broad (as shown in Fig. 3.12(a)). The Ta₂O₅ peak can be detected by XRD after being annealed for 60 mins, and it is intensified with increased annealing time. The observation of the Ta₂O₅ compound coincides with the increase of the sheet resistance because Ta oxide has higher resistivity [48].

Compared with Ta/ULK, TaN/ULK shows a broad TaN(111) peak due to the incorporation of N into Ta lattice. The lower intensity and broad peak width shown in the TaN XRD pattern suggest a smaller grain size, which is in good agreement with the corresponding AFM images. The same peak of Ta₂O₅ appears after the sample is annealed at 400°C for 120 mins (Fig. 3.12(b)). This observation also coincides with the increase of the sheet resistance in the TaN/ULK structure. As discussed in section 3.3.3, due to the release of N, the TaN film transferred from FCC structure to hexagonal Ta₂N structure, so the Ta₂N (200) peak appeared after being annealed for 30 mins. The increment of peak intensity with annealing time increasing suggested that this transform benefits from the longer annealing time. Both the N diffusion and the subsequent Ta₂N formation can alter the original barrier properties, like electrical resistivity or adhesion characteristics. The thermal stability is also affected due to the changed microstructure [112]. Note that this peak does not include the information of Si substrate due to the smaller glancing incidence angle ($\omega = 1^\circ$).

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Fig. 3.12. X-ray diffraction patterns from samples after being annealed at 400°C for different periods of time. (a) Ta/ULK ; (b) TaN/ULK.

3.4.3.4 SIMS results

The physical diffusion of the elements between the barrier and the ULK can be examined by SIMS analysis. Fig. 3.13 and Fig. 3.14 present the depth profile of Ta/ULK and TaN/ULK, respectively. As shown in Fig. 3.13(a), the Ta curve shows a sharper change at the interface, which indicates very low inter-diffusion between Ta and ULK porous SiLK for the as-deposited film. The peak of Ta at the Ta/ULK is broad because the yield of secondary ions is enhanced in the Ta/O interface by matrix effects [48]. A large amount of O can be detected at the surface of the Ta and the interface between Ta and ULK. The large O concentration at the interface is likely the porous SiLK probably absorbs vapors after being exposed in air. However, fewer O atoms are detected in the Ta layer. After being annealed, the O concentration rises with annealing time, as shown in Fig. 3.13(b). This indicates that the O atoms diffuse into Ta lattice slowly along the grain boundaries as well as the ULK porous SiLK. As the annealing time increases, more and more O atoms diffuse into the Ta barrier and form

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Ta₂O₅, which coincides with the XRD results. After being annealed for 150 mins, significant Ta and O diffuse into ULK.

Fig. 3.13. SIMS depth profile of Ta (25 nm)/ULK (600 nm), a) as-deposited; b) being annealed at 400°C for 150 mins.

For the TaN/ULK structure, O atoms are also detected at the TaN surface and the interface with ULK porous SiLK in the as-deposited sample, as shown in Fig. 3.14. The intensity of the O signal in the barrier layer also increases with the annealing time, but much slower than in the Ta barrier. This observation can be used to explain why the Ta₂O₅ can be observed after being annealed for 120 mins. It is also seen in the figure that the Ta and N have similar trends in the diffusion into the ULK polymer and the

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detected Ta diffusion is much slower than in the Ta/ULK structure. This observation indicates that most of the Ta in the TaN/ULK structure diffuses into the ULK in the form of TaN rather than elemental Ta.

Fig. 3.14. SIMS depth profile of TaN (25 nm)/ULK (600 nm), a) as-deposited,

b) being annealed at 400°C for 150 mins.

It can be noticed that at the TaN/ULK interface of the as-deposited TaN/ULK sample the decrease of Ta concentration is more gradual (Fig. 3.14(a)), which indicates that parts of TaN have diffused into the ULK for the as-deposited samples. It is likely because the TaN with smaller grain size (4.6 nm) and amorphous structure can easily enter the open pores near the interface (around 10 nm). However, after being annealed for 150 mins, no significant diffusion is observed due to the lower diffusion coefficient of TaN in the ULK porous SiLK.

3.4.3.5 Diffusion coefficient of Ta in ULK

Generally, Fick's diffusion law can be used to calculate the diffusion constant. Fick's diffusion theory was published in 1855 and was based on the analogy between material transfer in a solution and heat transfer by conduction. Fick's first law describes

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the relationship between the flux J per unit area, $\frac{\partial C}{\partial x}$ the concentration of the diffusing species given in units of per unit volume, and a quantity D called the diffusion coefficient or diffusivity given in units of area/time, as the following:

$$J = -D \frac{\partial C(x,t)}{\partial x} \quad (3.6)$$

Fick's second law of diffusion can be derived by considering the diffusion across an elemental volume and using the law of conservation of matter, so that one can obtain:

$$\frac{\partial C(x,t)}{\partial t} = D \frac{\partial^2 C(x,t)}{\partial x^2} \quad (3.7)$$

if D is considered independent of position and time. There are two most frequently used solution for Eq.(3.7) [139], depending on boundary conditions namely surface concentration constant and the diffusing amount constant. In this work, it is assumed that the amount of Ta atoms from the surface of the samples will be constant throughout the process. The following apply:

- a) Before diffusion, all diffusing atoms in the solid are uniformly distributed with concentration C_s .
- b) The value of x at the surface is zero and increased into the solid.
- c) The time is zero at the instance before diffusion process starts.

From these assumptions, the boundary conditions are simplified to:

- a) $C = 0, t = 0$ at $0 < x \leq \infty$
- b) $C = C_s, t > 0$ (constant surface concentration) at $x = 0$
- c) $C = 0$ at $x = \infty$

The solution of Eq.(3.7) [139] that will satisfy the condition above is:

$$C(x,t) = C_s \operatorname{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) \quad (3.8)$$

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where C_s is the interface concentration, D is the constant diffusivity, x is the distance, t is the diffusion time (in this case $t = 150$ mins), and $erfc$ is the complementary error function.

To quantitatively compare the diffusion of Ta and TaN into the porous SiLK in the Ta/ULK and TaN/ULK structures, the diffusion coefficients of Ta and TaN are extracted from the SIMS data. The reference point is defined as the barrier/ULK interface while the diffusion depth is defined as the distance from the interface to the point where the counts of Ta or TaN have three-orders of magnitude reduction [69]. Fig. 3.15 shows the depth profiles of Ta and TaN in the ULK porous SiLK. The dots in the figure are the extracted counts from SIMS results for the sample annealed for 150 mins, while the solid line is from the simulation based on the diffusion Eq.(3.8). The diffusion coefficient of Ta in porous SiLK is $0.023 \pm 0.001 \text{ nm}^2/\text{s}$, while the diffusion coefficient of TaN is $0.0033 \pm 0.0001 \text{ nm}^2/\text{s}$, which is much less than that of Ta in the Ta/ULK structure. It should be noted that for TaN barrier, Ta and N may diffuse separately, and at the same time, TaN can also diffuse in form of molecules. So the Ta information in the TaN SIMS results may include the two parts.

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Fig. 3.15. Experimental and simulation data of Ta diffusion in ULK from Ta/ULK and TaN/ULK structures after being annealed at 400 °C for 150 mins a) Ta (25 nm)/ULK; b) TaN (25 nm)/ULK.

3.5 Summary

Three kinds of diffusion barrier layers (Ta, TaN and Ta/TaN bi-layer) have been developed for the ULK porous SiLK, and the properties of these films such as sheet resistance, surface morphology and microstructure have been investigated. It was found that the Ta film shows body centered cubic (BCC) structure, lower resistivity, and clear grain boundaries. However, the TaN film shows smaller grain size and blur grain boundary due to the incorporation of N.

For the annealing at different temperatures, the barrier/ultra low k structures were found to lose the integrity at temperatures over 500°C due to the failure of ULK's

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properties, and significant diffusion was observed near the interfaces of the structures. The Ta/ULK structure shows the smallest sheet resistance but the poorest thermal stability while the TaN on the ULK porous SiLK shows the highest resistance with better thermal stability. The Ta/TaN bi-layer barrier takes the advantage of both Ta and TaN barriers and gives reasonable resistance and thermal stability. The better thermal stability of the TaN and the Ta/TaN bi-layer barriers is mainly due to the amorphous/nano structure and less grain boundaries of the barriers. In addition, the texture discontinuity at the Ta/TaN interfaces in the bi-layers barrier also plays an important role in reducing mutual diffusion of Ta atoms in the Ta barrier and some atoms in the ULK porous SiLK.

For the annealing at 400°C for different thermal cycles, it was found that the sheet resistance of the Ta barrier increased significantly after being annealed for 60 mins while that of TaN increased for 120 mins due to Ta₂O₅ compound formation as revealed by X-ray diffraction and secondary ion mass spectrometry. The better integrity of the TaN compared Ta is due to N incorporation, which degrades the diffusion of Ta and O. The diffusion coefficient of Ta in the porous polymer is $0.023 \pm 0.001 \text{ nm}^2/\text{s}$, while the diffusion coefficient of TaN is only $0.0033 \pm 0.0001 \text{ nm}^2/\text{s}$.

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4.1 Introduction

The transition from aluminum to copper interconnects introduces new processes and materials into semiconductor manufacturing, e.g., dual damascene process flow, Cu electroplating and new diffusion barrier materials. Electroplating is an attractive deposition method for copper with the need for a conformal seed layer. Particular properties including low thickness concurrent with coherence, low electrical resistivity, smooth surface and good adhesion to the barrier layer are required. The seed layer can be provided by several deposition techniques, which can be divided into two general categories: (1) physical vapor deposition (PVD) (evaporation, sputtering etc.); and (2) chemical vapor deposition (CVD), electrolytic etc. However, these methods suffer from some problems in depositing copper. PVD deposition is limited by the shadow effect. Due to the high growth temperatures of CVD processes, CVD-Cu films are subjected to greater film stress. PVD seed layers all show a very strong (111) texture with no traceable existence of (200) texture while CVD seeds show far more random orientation of grain textures. Although no noticeable variation of texture with varying seed thickness is observed in both cases, AFM roughness measurements reveal that the surface becomes rougher as the thickness is increased for both PVD and CVD seed layers. Furthermore, the CVD seeds have much rougher surface than the PVD ones.

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X-ray analysis of electroplated films demonstrates that the films plated on smooth and strongly textured PVD seeds have very strong (111) texture, while the films on rough and weakly-textured CVD seeds form much more random texture [74].

In this work, the Cu layer was deposited by SIP technology. SIP PVD technology allows thin conformal barrier/seed films, ensuring minimal overhang while enabling a wide process window for Electrochemical Plating (ECP) gap fill in high aspect ratio via structures.

As discussed in chapter 3, the interaction of copper with contacting materials in multilevel metallization schemes is an important issue that needs to be addressed before it can be utilized in IC devices. Especially copper diffusion in dielectrics may give rise to unanticipated yield or reliability problems. Furthermore, any movement of copper into the substrate through drift or diffusion could degrade device leakage current. Copper is a deep-level dopant in silicon and forms several acceptor and donator levels within the forbidden band gap. Those deep levels act as generation-recombination centre and can induce leakage current [73]. Hence a diffusion/drift barrier is necessary to prevent copper movement into the Si-substrate and inter-level dielectric. In the field of metallic barriers, Ta and Ta-based alloys such as Ta [39], Ta-Si-N [40], TaN [43] as well as Ti, TiN [41], W [42] were investigated successfully.

In this chapter, we will evaluate the properties of SIP Cu layer deposited on three

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kinds of barrier layers for Cu and ULK porous SiLK systems. The SIP Cu properties such as sheet resistance, surface morphology and microstructure on different barrier layers have also been investigated by various techniques. Furthermore, we will discuss the driving force for Cu motion and therefore the failure mechanism for different barrier layers.

4.2 Experimental procedure

The samples studied are the Cu/Ta/ULK/SiO₂/Si, Cu/TaN/ULK/SiO₂/Si, Cu/Ta/TaN/ULK/SiO₂/Si structures, respectively. The Si substrates used are 8-inch p-type Si(100) wafers. Firstly, a SiO₂ layer of 200 nm was deposited, followed by a 600 nm thick ULK porous SiLK deposited by spin-on technology. The tantalum or tantalum nitride film was deposited onto the ULK/SiO₂/Si substrate at room temperature using SIP technology in Ar or Ar+N₂ ambient. The Cu film of about 150 nm was deposited at -40°C by the same technique without breaking the vacuum.

The samples were annealed in high vacuum of 10⁻⁶ Pa for several thermal cycles at 400°C by RTP and each cycle was 30 mins. Then the electrical and physical properties were examined at end of each cycle using various techniques.

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4.3. Results and discussion

4.3.1 Sheet resistance

Fig. 4.1 shows the sheet resistance as a function of annealing time. The measured sheet resistances of Cu/Ta/ULK, Cu/TaN/ULK, and Cu/Ta/TaN/ULK as-deposited structures are 0.104, 0.103, and 0.108 Ω/sq , respectively. So there is no significant difference among those samples with different barriers. It is expected that the measured sheet resistance of Cu/barrier/ULK is dominated by the Cu film since it has much smaller sheet resistance (0.1 Ω/sq) and much thicker (150 nm) than the Ta barrier layer (150 Ω/sq and 25 nm), and the TaN barrier layer (800 Ω/sq and 25 nm). The sheet resistance of Cu/Ta/ULK increases linearly with the increasing annealing time up to 120 mins. And after annealing at 400°C for 150 mins, there is an abrupt rise. For Cu/TaN/ULK structure, the sheet resistance increases slowly and it remain almost unchanged after being annealed for 90 mins and more. For the structure with Ta/TaN bilayer barrier, the sheet resistance increases slightly after being annealed for 30 mins and then there is no further increase observed after that. The variation percentage of the sheet resistance is defined as the difference of the sheet resistance between annealed and the as-deposited samples, divided by the value of the as-deposited samples, as described below [68]:

$$\frac{\Delta R_s}{R_s} \% = \frac{R_{s, \text{annealed}} - R_{s, \text{as-deposited}}}{R_{s, \text{as-deposited}}} \times 100\% \quad (4.1)$$

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The variation percentages of Cu/Ta/ULK, Cu/TaN/ULK and Cu/Ta/TaN/ULK structures is 68%, 25.4% and 7.5%, respectively after being annealed for 150 mins, which indicates the structure with Ta/TaN bilayer has better stability.

Fig. 4.1. Sheet resistance changes of Cu/barrier/ULK porous SiLK structures as a function of annealing time.

4.3.2 Surface morphology

Generally, three factors affect the sheet resistance of copper thin films [48, 129]: copper grain size, diffusion and oxidation. Fig. 4.2 shows the surface morphologies of three samples with different barrier layers: as-deposited and annealed for 150 mins. For the as-deposited films, the surface is relatively smooth with finer grain size. The roughness are 4.23 nm, 4.76 nm and 5.26 nm, respectively. After being annealed for 150 mins, almost all grains grow up significantly (shown in Fig. 4.2 (d-f)), and the

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roughness also rises abruptly for three samples. They become 41 nm, 48 nm, and 63 nm, respectively. The growth driven may have arisen from the stress of Cu films. High thermal-excursion can cause large stress in the Cu films. That is, as the temperature is increased, the thermal expansion of the copper is greater than that of surrounding dielectric material. This Cu expansion thus induces compressive-stress in the copper film that causes the film to re-crystalline and relaxes through dislocation motion. However, upon cooling the copper contracts and goes into tensile stress that is much higher under ambient temperature conditions than that in the as-deposited film, which causes higher surface roughness [123].

The grain boundary defects can also be observed. Besides the Cu grain growth, another reason is mismatch of the coefficient of thermal expansion (CTE) of different layer materials, which introduces higher stress in Cu and Ta layer. The relaxation of stress also leads to interface roughness increasing. The TEM cross section showed the rougher interface of Cu/Ta/ULK, Cu/TaN/ULK and Cu/Ta/TaN/ULK (As shown in Fig. 4.8). Generally, the bigger grain can cause the sheet resistance to decrease. At the same time, it also makes the surface rougher. Iacopi has studied the relationship between sheet resistance and surface roughness for metal/porous material structure [67], and its result showed that the sheet resistance will increase with the surface roughness linearly. So the finally measured sheet resistance results were decided by the two effects.

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As-deposited:

After being annealed at 400°C for 150mins:

Fig. 4.2. Surface morphology of Cu film deposited on different barrier layers for as-deposited and after being annealed. (a,d) Cu/Ta/ULK; (b,e) Cu/TaN/ULK; (c,f) Cu/Ta/TaN/ULK.

4.3.3 XRD results

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XRD was employed after each cycle of annealing and the results are shown in Fig. 4.3. From the XRD results, there was no new phase formed during the annealing. Although there was no new peak formed, we could not conclude that there was no interaction between the layers as annealing time increases. The main phases detected before and after annealing were: Cu (111), Cu (200), Cu (220). In the as-deposited structure, Cu (111), Cu (200) and Cu (220) textures were observed. The intensity of the Cu (220) peak is the highest and that of the Cu (200) is the lowest. However, with the annealing time increasing, the Cu (220) peak becomes lower while the Cu(111) peak becomes higher and finally dominates the structure of the Cu film. There was no new compound observed.

In Fig. 4.3 (a), we could also see a slight shift of Ta (110) peak after annealing. This peak shift was suspected to be due to the inter-diffusion between Ta and ULK where O atoms from ULK take interstitial positions of the bcc Ta lattice. The dissolved oxygen in the Ta tetrahedral interstices would slightly distort the Ta from BCC to body-centered tetragonal (BCT) structures, which shifts its peak towards the lower angle direction [64, 120]. Another possible source of O atoms was the ambient of Ta deposition.

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Fig. 4.3. X-ray diffraction patterns of three samples after being annealed at 400°C for different periods of time. (a) Cu/Ta/ULK, (b) Cu/TaN/ULK and (c) Cu/Ta/TaN/ULK

Generally, the strong Cu (111) texture in the Cu seed layer will promote a similar texture in the electroplated plane layer and hence reduce electro-migration effects in the Cu line [65]. Furthermore, as Lee [74] reported, the grain size and texture of plated top

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layer is highly dependent on the roughness and texture of the underlying seed layers, and the surface roughness of the seed layer is related to the texture of the layer itself. The films plated on smooth and strongly textured seed layers can achieve a median grain size larger than 1 μm and a strong (111) texture. And the grain size even can extend to 20 μm for some samples. The films on rough and weakly textured seed layers have grains of 0.08-0.15 μm and weak (111) texture. Some films show bimodal grain size distributions, which is possibly an indication of secondary grain growth occurring during deposition. So it is important to check how the texture and grain size of the Cu layer change with annealing.

Fig. 4.4 shows how the intensity ratio Cu(111)/Cu(220) increases with annealing time for three kinds of barriers. These results indicate that the annealing process can promote the Cu growth along the preferred Cu (111) orientation. However, the ratios Cu(111)/Cu(220) are largest for the structures with Ta/TaN barrier. It can be explained from the XRD results. All Ta (110) and TaN (111) texture can promote the Cu (111) texture [50,72]. From the Fig. 4.3, one can see that with annealing time increasing, the intensity of TaN (111) peak (Fig. 4.3(b)) becomes weak due to the microstructure transform. The intensity of Ta (110) peak (Fig. 4.3(a)) decreases fast after being annealed for 30 mins, and almost disappears after being annealed for 90 mins. But for the Ta/TaN bi-layer, it shows stronger Ta (110) peak after being annealed for 90 mins, so its ratio increases faster than others. Yuan [50] and Kstuhiko [72] reported that Ta (110) and TaN (111) can promote the Cu (111) texture. From XRD results as shown in

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Fig. 4.3, one can observe that the Ta (110) peak in Cu/Ta/TaN/ULK is higher than that in Cu/Ta/ULK after being annealed for 90 mins. This means that the Ta (110) texture in Cu/Ta/TaN/ULK is more stable than that in Cu/Ta/ULK due to the TaN underlayer existing. So the increase in the Cu(111)/Cu(220) for Ta/TaN barrier is larger. The ratio of Cu (111)/Cu (220) of three samples increases because the intensity of Cu (111) increases faster than that of Cu (220) due to the barrier condition.

Fig. 4.4 The intensity ratio of Cu(111)/Cu(220) changing as a function of annealing time for three samples

The grain size t can be estimated from the XRD results by Equation (3.4). The calculated grain size values for Cu (111) and Cu (220) for the Cu/Ta/ULK and Cu/TaN/ULK structures are shown in Fig. 4.5. As seen from the figure, the copper grain size slightly increased with the annealing time, as is usually observed after annealing. The slight increase in the grain size should cause a slight decrease of the

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sheet resistance rather than increase although the change due to the grain growth may not be significant. Furthermore, the grain size of Cu (111) is slightly smaller than that of Cu (220). But there is no significant difference in the Cu (220) grain size for the samples with different barrier layers, that is, no tightly relationship between the Cu (220) grain size and barrier layer because it is the random orientation. However, for the Cu (111) texture, it has larger grain size on TaN barrier than that on Ta barrier, which indicates that the Cu (111) would grow fast on TaN (111) than on Ta (110).

Fig. 4.5 Extracted grain size of phase Cu (111) and Cu (220) from XRD results.

4.3.4 SIMS results

SIMS technique was utilized to find the depth profile of several elements which include Cu, Ta, O, N, C and H. As we know, SIMS is an effective and highly sensitive

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characterization tool in detecting the performance of Ta-based diffusion barriers in Cu/Si structure, especially to observe the low levels of copper diffusion [75,76]. The depth profiles of the as-deposited Cu/barrier/ULK structure for three different barriers are presented in Fig. 4.6(a,c,e). The Cu and Ta curves show a sharp change in the interfaces. The significant amount of oxygen is also shown at the barrier/ULK interface, but few O atoms were detected in the Cu layer. This phenomenon could be explained with interstitial diffusion mechanism. Cu with FCC structure has four octahedral interstices with a radius of 0.529 Å while Ta with BCC structure possesses 12 tetrahedral interstices having a radius of 0.415 Å per unit cell. The atomic radius of oxygen is 0.64 Å and the available interstitial sites accommodating oxygen in Ta are three times more than in Cu, indicating that the solubility of oxygen in Ta is much higher than in Cu. Although the activation energy for oxygen diffusion in Cu (~ 16.0 kcal/mol) is lower than that in Ta (~ 26.7 kcal/mol), the concentration of the oxygen in both layers is determined by the combination effects of available interstices and activation energy as well as temperature and structure [120]. In these samples, the lower solubility of oxygen in Cu may be the dominant factor that lowers the oxygen concentration in Cu. The SIMS result also indicates that oxygen has been incorporated into Ta matrix for the as-deposited film. The O at the Ta and ULK interface is likely due to the absorption of the ULK SiLK when it is exposed to air.

After being annealed at 400°C for 150 mins, the Cu curves from 3 samples show the change in the slope (as shown in Fig. 4.6.(b,d,f)), which indicate Cu diffusion. At the

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same time, Ta not only diffused into the ULK, but also out diffused into Cu layer. The O intensity changed synchronously with the Ta change due to the higher solubility of oxygen in Ta than that in Cu, which suggested the formation of Ta-O chemical bonds (for the TaN barrier, it should be Ta-O-N). They are not crystalline structure because no new peak was observed in the XRD spectra. Laurila reported that the interfacial oxide layer is formed between Cu and Ta, which works as an additional barrier layer and retards the diffusion of Cu up to much higher temperatures [69]. However, the interfacial oxide layer between Cu and Ta not only results in higher resistance, but also induces reliability problems so it is thought that oxygen atoms might play an important role for the thermal stability of Cu/barrier/ULK structure. It is necessary to find out the source of oxygen. The first source is the underlying ULK. The porous polymer probably absorbed a trace amount of vapor after being exposed in air for long time, which could diffuse into and react with the Ta layer with annealing time increasing. Secondly, oxygen atoms can be incorporated from the annealing ambient. Most of the oxygen atoms will be at the surface of the Cu layer and some may penetrate the Cu layer along the Cu grain boundary because Ta has higher affinity to oxygen [77]. The oxygen profile, as measured by SIMS after annealing, showed the diffusion of oxygen from both Cu surface and ULK, as shown in Fig. 4.6(b,d,f). In addition, it is also observed that H has greater diffusion compared with C although the H diffusion is not as fast as O. These observations indicate that the increased sheet resistance in the structure is mainly due to the O in the Cu film and at surface although the Ta diffused

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into the Cu film also plays a role. The strong diffusion can also be verified by TEM to be shown in Fig. 4.8(a,b,c).

It should be noted here that for the Cu/TaN/ULK sample, the longer trail of Ta is shown at the TaN/ULK interface. We have explained it in the chapter 3. For the as-deposited Cu/Ta/TaN/ULK sample, the depth profile shows clearly that the N is defined in TaN layer. However, after being annealed for 150 mins, the N atoms diffuse out of the TaN film into the adjacent Ta. The Ta and N distributions across the whole barrier region are nearly equal, which has a good agreement with the previous XRD results. As indicated in the XRD diagrams, annealing results in the formation of Ta₂N due to the N release [112].

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Fig. 4.6. SIMS depth profiling spectra of the as-deposited (a,c,e) and the annealed (400°C for 150 min) (b,d,f) for Cu/Ta/ULK, Cu/TaN/ULK, Cu/Ta/TaN/ULK structures, respectively.

From the SIMS depth profile, the diffusion coefficient of Cu in Barrier/ULK and the diffusion coefficient of Ta into the ULK polymer can be estimated using the diffusion equation (which has been discussed in chapter 3),

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The experimental (dot) and simulated (solid line) data of Cu diffusion in Barrier/ULK are presented in Fig. 4.7(a). The diffusion coefficients of Cu are 0.035 nm²/s, 0.04 nm²/s and 0.03 nm²/s in Cu/Ta/ULK, Cu/TaN/ULK, and Cu/Ta/TaN/ULK respectively. The different diffusion coefficients are likely due to the stress difference between Cu and barriers. Li [85] reported that the nitrogen composition incorporated into Ta barrier layer causes larger tensile strain between TaN and Cu. However, the Cu film deposited on the Ta/TaN bi-layer barrier showed the smallest stress due to relaxation of strain in the bi-layer barrier. So the diffusion coefficient of Cu is the largest in TaN/ULK the smallest in Ta/TaN/ULK structures.

The diffusion coefficient of Ta from different barriers diffusing into the ULK can also be estimated in the same way. The experimental (dot) and simulated (solid line) data of Ta diffusion in ULK for different barrier layers are presented in Fig. 4.7(b), and the diffusion coefficients of Ta are 0.05 nm²/s, 0.051 nm²/s in the Cu/Ta/ULK and Cu/TaN/ULK, respectively. Obviously, the diffusion constant of Ta with Cu capped layer is larger than that without Cu layer (shown in Chapter 3).

With Cu cap layer, the inter-diffusion between Cu and Ta would occur during the annealing, which can be observed as shown in the TEM results (Fig. 4.8). Ma *et al.* [121] demonstrated amorphization in 0.9 nm thick Cu/3.6 nm thick Ta layers during annealing at 450°C. They suggested that the excess interfacial free energy is relatively larger and may elevate the free energy to a state close to that of the amorphous alloy.

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The inter-diffusion and amorphization between Cu and Ta probably results in such Ta film thinning, which leads to a complete rearrangement and disintegration of the barrier [122]. At the same time, it also enhances the inter-diffusion between Ta and ULK. So there is larger intermixing appeared at the Ta and ULK interface for the samples with Cu than that without Cu. In addition, the residual stress in Cu and Ta can accelerate the Ta diffusing into ULK.

Fig. 4.7. Experimental and simulated data of (a) Cu diffusion in Barrier/ULK and (b) Ta diffusion in the ULK porous SiLK. The experimental data are extracted from the SIMS results of the sample after being annealed.

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4.3.5 TEM results

Fig. 4.8 shows the TEM images of three structures after being annealed at 400°C for 150 mins. For the Cu/Ta/ULK structure (Fig. 4.8(a)), the interface of Ta/ULK is very rough, and the reaction region of 30 nm thick is observed at the interface. It suggested that the diffusion and intermixing mainly occurs between Ta and ULK. Generally, the grain boundaries in the polycrystalline Cu and Ta can be thought as the fast diffusion paths. The Ta grains are from 7 to 10 nm [50]. They can easily enter the underlying porous ULK with pore size around 10 nm. On the other hand, C, H, O atoms in the ULK with smaller volume and lower mass can also easily diffuse into Ta barrier layer along the grain boundary defects, and even penetrate the barrier layer and reach the Cu/Ta interface (as shown in SIMS results). The diffusion of Ta into Cu is more difficult due to the lower annealing temperature. It was reported that the faster diffusion of Ta into Cu along the grain boundaries seems to start in the range 550-600°C [49]. The effective barrier thickness decreased significantly owing to the diffusion or intermixing of the Ta and the element in the underlying ULK. However, the Ta layer is not completely consumed by the reactions. It is evident that the reaction between Ta and ULK and the Cu oxidizing at the surface are the main cause of the observed changes in electrical measurement.

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For TaN barrier, Ta and N may diffuse separately, at the same time, TaN can also diffuse on the surface as molecule, and these processes could coexist. Compared with Ta/ULK, the TaN/ULK interface is smooth and better defined. It could be explained by different surface diffusions of Ta and TaN on the ULK. If surface diffusion is high (Ta on ULK) then the deposited barrier can penetrate the porous film by pore walls without forming a sealing layer on the top surface. On the other hand, if surface diffusion is low (TaN on ULK) then the TaN forms a continuous layer on the top surface without penetrating deep into the porous film [118, 119]. For the Cu/Ta/TaN/ULK sample, smaller diffusion region appeared at the TaN/ULK interface. At the same time, Ta diffused into Cu layer is also presented.

(a)

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(b)

(c)

Fig. 4.8. TEM images of (a) Cu/Ta/ ULK, (b) Cu/TaN/ULK and (c) Cu/Ta/TaN/ULK structures after being annealed at 400°C for 150 mins

4.4 Summary

In summary, this section reports the thermal stability of SIP Cu layer deposited on different barrier layers (Ta, TaN and Ta/TaN bi-layer). It was found that the variation percentages of sheet resistance for Cu/Ta/ULK, Cu/TaN/ULK and Cu/Ta/TaN/ULK structures are 68%, 25.4% and 7.5%, respectively, after being annealed for 150 mins. Cu (111), Cu (200) and Cu (220) textures were observed for all samples. It was found

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there are two reasons to degrade the thermal stability of Cu/Ta/ULK structure. One is that the barrier Ta has the polycrystalline structure with finer grain (7-10 nm), which can easily enter the porous polymer with pore size around 10 nm. It also provided many grain boundaries as the fast diffusion paths for C, H, and O atoms in the ULK out-diffusion. The other is that Ta has higher affinity to oxygen and forms stable oxide, Ta₂O₅, which causes increase in sheet resistance. The results of the SIMS revealed that the significant increase of the sheet resistance is due to the diffusion of Ta and O to the Cu film. It was also revealed that the annealing at 400°C for more than 120 min also caused diffusion of Ta and O and even Cu into the ultra low k porous polymer, and the Ta and O diffused faster in the dielectric than in the Cu film. In addition, the out-diffusion of the C and H in the dielectric towards Ta and Cu layers was also observed and the H diffusion rate was found to be faster than C.

For TaN barrier, Ta and N may diffuse separately, and at the same time, TaN may also diffuse in the form of molecules. Compared with Ta/ULK, the TaN/ULK interface is smooth and better defined due to its lower surface diffusion on ULK. For the Cu/Ta/TaN/ULK sample, smaller diffusion region appeared at the TaN/ULK interface. At the same time, Ta diffused into Cu layer is also presented.

The diffusion coefficients of Cu are 0.035 nm²/s, 0.04 nm²/s and 0.03 nm²/s in the Cu/Ta/ULK, Cu/TaN/ULK and Cu/Ta/TaN/ULK structures. And the diffusion coefficients of Ta in ULK are 0.05 nm²/s and 0.051 nm²/s in the Cu/Ta/ULK and

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Cu/TaN/ULK structures, respectively. Obviously, the diffusion constant of Ta with Cu cap layer is larger than that without Cu layer because of the inter-diffusion and amorphization between Cu and Ta. In addition, the residual stress in Cu and Ta can accelerate the Ta diffusion into ULK.

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5.1 Introduction

Generally, there are two kinds of barriers. One is the metallic barrier, and the other is the dielectric barrier. It is known that plasma deposited Si_3N_4 acts as the hard mask. In addition, it is also Cu drift barrier [78]. However, the high dielectric constant k of Si_3N_4 ($k = 8$) motivates the development of other PECVD materials. Recently, other SiC-based dielectrics are used as hard mask due to their lower k value. They have good resistance to wet chemicals, aggressive etch and chemical mechanical polishing. Moreover, they also work as the barrier layers to block Cu diffusion because of their amorphous structures, higher crystalline temperature and lower density. Many papers reported that the SiC-based dielectric barriers such as SiCOH [69], SiCH [78] and SiCN [92, 93] have good properties to block Cu diffusion. The SiC-based dielectrics applied in the wafer process can be divided into three types according to their deposition process. The details are shown in Table 5.1. Among them, although SiCO has the lowest k value, the O atoms may cause some reliability problems during the integration. If O atoms exist in the dielectrics, they will diffuse into the Ta and Cu layer and react with Ta or Cu to form TaO or CuO during annealing because Ta and Cu have higher affinity with O [49, 61]. Tomi [48] also reported that the diffusion of Cu through the Ta layer could not proceed until the Ta matrix had dissolved the interfacial oxide.

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The oxide compounds result in large resistance due to their higher resistivity, which results in RC delay, thermal and stress issues. Another consideration is the electro-migration. If CuO exists at the surface or interface, the electro-migration will fail earlier because Cu ion or Cu atoms move faster in CuO layer than in Cu layer [48]. For SiCH, its k value is highest. Comparing with SiCO and SiCH, SiCN not only has lower k value, but also with oxygen-free, so, in this work, we mainly study the $\text{Si}_{0.49}\text{C}_{0.34}\text{N}_{0.17}\text{H}$ (we use SiCN in this thesis).

SiC possesses a lower band gap (approx. 2.8 eV) comparing with SiN and is characterized by excellent mechanical performance [170,171] and CN contributes high hardness, partial electrical conductivity and high elastic rebound [172] due to a fullerene-like microstructure [173,174]. Therefore, by changing the phase content and by controlling the short-range order it is possible to tune the properties of SiCN films to specific applications. SiCN films have been prepared by various techniques, which include pyrolysis of polymer precursors [166], chemical vapor deposition (CVD) at elevated temperatures [162], bias-assisted hot filament CVD [175], radio frequency plasma-enhanced CVD (PECVD) [176,177], microwave PECVD [178,179], electron cyclotron resonance PECVD [167, 168], pulsed laser deposition [164,169], ion beam sputtering [163,180], and reactive magnetron sputtering [165,181,182]. PECVD technique offers an attractive opportunity to fabricate amorphous hydrogenated SiCN films at intermediate substrate temperatures (200-300°C) and it provides high quality films with good adhesion, good coverage of complicated substrate shapes and high

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deposition rate [176,177]. The mechanical, electrical properties and thermal stability were respectively reviewed as shown in the following.

Mechanical properties of SiCN

P. Jedrzejowski et al [160] reported mechanical properties, such as hardness, Young's modulus, friction coefficient and stress, of the SiCN films fabricated by PECVD from SiH₄/CH₄/N₂/Ar gas mixtures at a temperature of 400°C. Films deposited under optimized conditions exhibited a hardness >30 GPa, Young's modulus >190 GPa, elastic rebound of 85% and a compressive stress of approximately 1 GPa. The high compressive stress enables multi-level integration with tensile bulk low k materials [160].

Thermal stability of SiCN

SiCN remains thermally stable to 1600 degrees and higher, and has an oxidation rate nearly 10 times slower than that of polycrystalline silicon carbide and silicon nitride according to Raj [161], an expert in high temperature research of metals and ceramics. The remarkable properties of SiCN derive from their amorphous structure in contrast to the crystalline structure of silicon nitride and silicon carbide. The crystalline materials contain grain boundaries, which weaken their high temperature mechanical properties. The SiCN materials remain predominantly amorphous, allowing them to retain their properties to very high temperatures. SiCN also has an ultra low coefficient of thermal expansion, which would impart outstanding thermal shock resistance.

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According to Applied materials and Novellus reports [183], SiCN shrinkage is less than 0.3% after 2 hours at 425°C, and no measurable change in k after 2 hours at 425°C. Lastly, SiCN exhibits almost zero deformation at very high temperature. Carbon is an outstanding material for building high temperature systems, except that it burns in air above about 800 degrees C, and the SiCN materials have all the good attributes of carbon except that they do not burn at temperatures approaching 2000 degrees C [161].

Electrical properties of SiCN

SiCN shows excellent electrical properties as a dielectric Cu barrier and etch stop film used as a low k alternative to silicon nitride in damascene applications [183]. With a dielectric constant of <5.0 , this film provides significant reductions in the effective capacitance of the dielectric stack. Advanced SiCN is an extension of SiCN and further reduces the dielectric constant to <4.0 , while maintaining SiCN performance characteristics. The leakage current of SiCN is less than 1 nA/cm^2 under 0.5 MV/cm , and 2 nA/cm^2 at 1 MV/cm [183].

The pure silicon carbide film had a dielectric constant approximately 3.8, and the dielectric constant of nitrogen-containing films, SiCN, was higher. The increase of dielectric constant is due to the appearance of SiN bonds in SiC films. The tetrahedral structure of SiC is distorted with the addition of SiN bonds which enhances polarization and improves the barrier function [93]. Although the pure SiC has lower k value, the

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leakage current of pure SiC is much larger than that of SiCN because the bonding energy of SiN is higher than SiC bond [93]. According to Chen's report [93], the bonding energy of SiN (101.8 eV) is higher than SiC (100.6 eV) bond and the carrier would be difficult to transport through the SiCN films. As a result, the leakage currents of SiCN films are smaller than SiC ones. In this case, the mechanism of leakage current is Poole-Frenkel (P-F) emission [141] which is due to field-enhanced thermal excitation of trapped electrons in the insulator into conduction band. The current density is given by:

$$J = J_0 \exp\left(\frac{\beta_{PF} E^{1/2} - \phi_{PF}}{k_B T}\right) \quad (5.1)$$

Where $\beta_{PF} = \left(\frac{e^3}{4\pi\epsilon_0\epsilon}\right)^{1/2}$, e the electronic charge, E the applied field, ϵ_0 the dielectric constant of free space, ϵ the relative dielectric constant, and ϕ_{PF} the contact potential barrier. As reported by Chen [157], the energy gap values of 3.81 and 4.66 eV are obtained for $\text{Si}_{35}\text{C}_{26}\text{N}_{39}$ and $\text{Si}_{38}\text{C}_5\text{N}_{57}$ films, respectively, corresponding to Si-rich SiCN structures. The energy gap value progressively decreases with increasing C content in the film. Therefore, the ϕ_{PF} of SiCN is larger than that of SiC due to larger energy gap and the leakage current of SiCN is also smaller than that of SiC.

Why introduce SiCN in Cu/ULK structure

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In chapter 4, we mainly discussed the Ta, TaN and bi-layer Ta/TaN barriers in Cu/barrier/ULK porous SiLK structures. In our work, we found that there are some disadvantages for the Ta based barriers: 1) the polycrystalline Ta with grain size around 7-10 nm can easily enter the pores in the ULK. Moreover, some atoms in the ULK, such as C, H, can easily diffuse into Ta and Cu film along the grain boundary defects. 2) Ta has higher affinity to oxygen, so the formation of an amorphous TaO_x layer at the Cu/Ta interface is more likely, which not only causes higher resistance, but also brings some reliability problems [77]. 3) The coefficient of thermal expansion (CTE) is 5.2 ppm/K for Ta, and 60 ppm/K for ULK. Moreover, the Ta film has the compressive stress. The CTE mismatch between Ta and ULK causes rougher interface, which degrades the electrical performance significantly.

Excellent copper diffusion barrier properties, as well as high resistance to moisture, allow SiCN to be easily integrated into Cu/dual damascene devices. In addition, SiCN's high compressive stress enables multi-level integration with tensile bulk low k materials. Therefore, inclusion of SiCN film in the Cu-porous low k integration should be of positive influence on the improvement of electrical performance of the interconnects. Furthermore, when it is used together with FSG or Black Diamond, SiCN enables capacitance reductions of 25% and 35%, respectively, relative to USG/SiN schemes [183].

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Table 5.1. All kinds of SiC-based dielectric-cap layer deposited by PECVD [153]

	Dielectric-cap layer			
	SiN	SiCO	BLOk™-1	BLOk™-2
Gases/ flow (sccm)	SiH ₄ / 500	C0 ₂ /3000	He/200	He/400
	NH ₃ /4000	4MS/500	3MS/80	3MS/150
	N ₂ /1600		NH ₃ /160	
Power (W)	HFRF- 570	HFRF- 500	300	460
	LFRF- 430	LFRF- 400		
Pressure(Torr)	2.6	2.5	3	8.7
k value	7.0±0.2	4.4±0.2	4.6±0.2	4.9±0.2
Composition	----	Si _{0.39} C _{0.35} O _{0.26} :H	Si _{0.49} C _{0.34} N _{0.17} :H	Si _{0.53} C _{0.47} :H

Notes:

- 3MS is tri-methyl-silane, Si(CH₃)H. Three -CH₃ groups instead -H in SiH₄ composite the Si(CH₃)H.
- Equation for PECVD SiCN:

Equation for PECVD SiCO:

5.2 Properties of SiCN barrier on blanket wafer

5.2.1. Experimental procedure

The samples studied are Cu/SiCN/ULK/SiO₂/Si structures. The Si substrates used are 8-inch p-type Si (100) wafers. Firstly, 200 nm SiO₂ and 50 nm SiC were deposited by PECVD, and then 300 nm ULK porous SiLK was deposited on the wafer by spin-on technology. Amorphous SiCN layer with thickness of 50 nm was deposited as barrier

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layer by PECVD. Finally, the Cu film of 150 nm was deposited on the SiCN directly by SIP at a deposition temperature -40°C .

To evaluate the thermal stability, the samples were annealed at 400°C in high vacuum of 10^{-6} Pa for several thermal cycles by RTP. Every thermal cycle is 30 mins. Then the electrical and physical properties were investigated by same techniques as presented in last chapter.

5.2.2 Results and discussion

Fig. 5.1 shows the sheet resistance of Cu/SiCN/ULK structures as a function of annealing time. The measured sheet resistance should be dominated by the copper thin films. As shown in Fig. 5.1, the sheet resistance decreased with annealing time. The variation percentage of sheet resistance, defined by Equation (4.1) decreased by 15.8% after being annealed for 150 mins in comparison of a 68% for the Cu/Ta/ULK structure.

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Fig. 5.1. Sheet resistance changes of Cu/SiCN/ULK as a function of annealing time

To find out the mechanism behind the change in sheet resistance of the structures, the roughness, grain size, and texture of Cu film are examined. This is because they are the possible factors that can affect the electrical conduction of the Cu films. Fig. 5.2 shows the AFM results of the as-deposited and after being annealed at 400°C for 150 mins. For the as-deposited sample, the roughness is 0.67 nm, which is lower than 4.23 nm of the Cu/Ta/ULK. It indicates that the Cu deposited on SiCN has much smoother surface than that deposited on Ta. With annealing time increasing, the roughness also increased due to grain growth. The roughness becomes 7.6 nm after being annealed at 400°C for 150 mins, which is also lower than 41 nm of the Cu/Ta/ULK samples after being annealed at the same conditions. The growth of the grains should be the main cause for the decreased sheet resistance. The as-deposited Cu on SiCN/ULK is highly defective and the resistivity is high due to the lower deposition temperature. This film

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is not stable because of high defect density. It trends to reduce the defect level by re-crystallization during annealing. The grains grow larger by consuming defective grains, leaving defects mainly in the grain boundaries and interfaces. The stress in copper film also changes from compressive stress to tensile stress after being annealed. For the Cu/Ta/ULK structure, however, besides the grain growth, there are oxidation and diffusion which cause the sheet resistance increase.

Fig. 5.2. Surface morphology of Cu/SiCN/ULK a) as-deposited, b) annealed at 400°C for 150 mins.

XRD analysis can identify the intermixing and new phase formation. Fig. 5.3 shows the XRD spectra of the Cu/SiCN/ULK structure after being annealed for different periods of time. As discussed in last chapter 4, for the Cu/Ta/ULK structure, the Cu (111), Cu (200) and Cu (220) textures were observed in as-deposited structure, and the

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Cu (220) texture dominates. The intensity of Cu (220) is two times that of the Cu (111) intensity (as shown in Table 5.2). However, with annealing time increasing, the intensity of Cu(220) decreased, and the Cu(111) texture dominated after being annealed for 150 mins.

For the Cu/SiCN/ULK structure, however, the Cu (220) texture dominates for the as-deposited and the annealed samples (as shown in Fig. 5.3). The $I(220)/I(111)$ ratio increased from 10.4 to 12.4 as the annealing time increased to 150 mins. The increment of ratio is due to the weakening (111) texture and stronger (220) texture during the thermal annealing [115]. These observations suggest that the texture of the Cu film is strongly affected by the underlying material. For the polycrystalline Ta barrier, there is a strong (111) texture in the Cu layer. However, for the amorphous SiCN barrier, a strong Cu (220) texture dominates and other textures are lower.

Orientation in thin film is controlled by a number of factors. According to Tsuji [155] report, the substrate type and the substrate surface condition have marked influences on the texture of as-deposited Cu films. For the amorphous structure, the high atomic density of the underlayer is a possible factor promoting the strong (111) texture of the overlaid Cu films. He also showed the correlation between the intensity of Cu (111) and the density of substrate, and the peak of Cu (111) increases with substrate density increasing. B Okolo [144] reported Cu films deposited on amorphous Si_3N_4 substrates exhibit a stronger (111) fiber texture than that of SiO_2 substrates

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because the density of Si_3N_4 (2.93 g/cm^3) is larger than that of SiO_2 (2.29 g/cm^3). So it is easy to understand why only a weaker Cu (111) peak is observed when Cu is deposited on amorphous SiCN (2.0 g/cm^3) comparing with that of SiO_2 and Si_3N_4 substrates [156]. That is, the weak Cu(111) peak is believed to be mainly due to the smaller density of the SiCN underlayer.

Fig. 5.3. A series of X-ray diffraction patterns of Cu/SiCN/ULK after being annealed at various periods of time. ($\omega = 1^\circ$)

The grain size t can be estimated from the XRD data, and the results are shown in Table 5.2. It is clear that the grain size increases with the annealing time. This is in good agreement with the AFM results.

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Table 5.2. comparison of Cu properties for two structures after being annealed for different periods of time

	Cu/Ta/ULK			Cu/SiCN/ULK		
Annealing time (mins)	$\frac{I_{Cu(220)}}{I_{Cu(111)}}$	Grain size Cu(111) (nm)	Grain size Cu(220) (nm)	$\frac{I_{Cu(220)}}{I_{Cu(111)}}$	Grain size Cu(111) (nm)	Grain size Cu(220) (nm)
As-deposited	2.20	20.83	23.92	10.40	21.92	25.71
30	0.83	21.71	25.98	10.86	22.21	27.63
90	0.81	22.82	26.66	11.94	24.80	27.91
150	0.60	24.54	26.84	12.41	32.43	28.34

Fig. 5.4 shows the TEM images of the structure after being annealed at 400°C for 150 mins. The clear and smooth interfaces can be observed in the Cu/SiCN/ULK TEM image, which confirms that no significant diffusion occurred even after being annealed at 400°C for 150 mins. It indicates the amorphous SiCN barrier layer shows better performance. It has higher hardness, without grain boundary defects, so it can prevent the Cu diffusion and block the ULK out-diffusion even after being annealed at 400°C for 150 mins.

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Fig. 5.4. TEM images of Cu/SiCN/ULK after being annealed at 400°C for 150 mins.

5.3 Improvement of thermal stability of Cu/Ta(N)/ULK by inducing additional SiCN layer

5.3.1 Introduction

From the discussion in section 5.2, SiCN can be thought as a good barrier candidate for Cu and ULK integration due to its lower density (3.25 g/cm^3), higher hardness (460 GPa), amorphous structure without grain boundary defects, better thermal stability and no reaction with Cu, ULK and oxygen after being annealed at 400°C for 150 mins.

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Unfortunately, the poor adhesion between Cu and SiCN limits the application. It can not withstand the CMP pressure and tends to peel after CMP process. So a buffer layer is needed between the Cu and SiCN to improve the adhesion. Ta and Ta-based layers can be used as the buffer layer to improve the adhesion between Cu and SiCN. It is well known that there is stronger adhesion between Ta and Cu. In addition, Ta also has tendency to react with C at the surface of SiCN to form the Ta-C bond, which is helpful for the adhesion improvement. Iacopi reported the detailed reaction between Ta and SiCH [107]. The carbidic bonds on the dielectric surface are weakened (mainly C-H like, since the covalent Si-C bonds are much stronger) due to charge delocalization effects induced by the presence of neighboring Ta metal atoms. Moreover, the ion bombardment energy released during the PVD deposition further favors the breaking of these bonds, and can lead to cross-linking of the top layers of the matrix through the formation of a C-C bond across the chains. Like schematically shown in Fig. 5.5, the same process also happened for the Ta/SiCN interface, which is proved by the following integration process.

Fig. 5.5. Mechanism leading to local cross-linking enhancement of dielectric matrices containing CH_x functional groups. The presence of TaC crystallites or unreacted Ta, together with ion bombardment from the PVD deposition,

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resulting in weakening and eventual breaking of C-H bonds. Cross linking among two neighboring polymer chains can take place [107].

Therefore, in this work, we try to deposit SiCN combined with Ta or TaN barrier for Cu/ULK integration. The thermal stability is comparatively investigated of Cu/Ta/SiCN/ULK and Cu/TaN/SiCN/ULK structures on blanket wafer by employing four points probe, AFM, XRD and TEM.

5.3.2 Experiment procedure

The samples studied were the Cu/Ta/SiCN/ULK/SiO₂/Si (sample A) and Cu/TaN/SiCN/ULK/SiO₂/Si (sample B) structures. The Si substrates used were the 8-inch p-type Si (100) wafers. Firstly, a SiO₂ layer of 200 nm was deposited and followed by a 310 nm porous ULK deposited by spin-on technology. The samples were deposited amorphous SiCN layer with thickness 20 nm by PECVD, and the equation for PECVD SiCN was shown as following:

And then Ta film was deposited onto the SiCN/ULK/SiO₂/Si substrate at room temperature using SIP technique. The Cu film of about 150 nm was finally deposited at -40°C by the same technique without breaking the vacuum. For the

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Cu/TaN/SiCN/ULK/SiO₂/Si structure, the preparation procedure is almost same as that of Cu/Ta/SiCN/ULK/SiO₂/Si structure except the metal barrier layer.

To evaluate the thermal stability, the blanket samples were annealed in high vacuum of 10⁻⁶ Pa for several thermal cycles at 400°C by RTP and each cycle was 30 minutes. Characterization was carried out using same techniques as before.

5.3.3 Results and discussion

5.3.3.1 Sheet resistance

Fig. 5.6 shows the sheet resistance versus annealing time for the two structures. The sheet resistance for as deposited sample A is 0.137 ohm/sq. It is slightly higher than the sample without SiCN layer because the β phase Ta is formed when Ta is deposited on the SiCN layer directly. This can be proved by the XRD results (as shown in Fig. 5.9). After being annealed for 150 mins, the sheet resistance decrease to 0.105 ohm/sq, and the variation percentage is -23.7%. This indicates that the sample with SiCN has better thermal stability in terms of sheet resistance. The drop of the sheet resistance with increased annealing time is caused by the decrease of the defeat density and the grain growth of the Cu film.

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For the sample B, the same trends as the sample A can be observed because the information mainly come form the Cu layer. Compared with sample A, sample B has slightly higher sheet resistance due to the TaN layer, which has higher resistivity than Ta. After being annealed for 150 mins, the sheet resistance of sample B also drops because of the decrease of the defeat density and grain growth of the Cu film. The variation percentage is -21.3%.

Fig. 5.6. Sheet resistance vs annealing time for sample A and sample B at 400°C.

5.3.3.2 Surface morphology

From Fig. 5.7, it could be seen that the RMS values of sample A did not vary significantly throughout the annealing process. The RMS value of the as-deposited sample was 0.85 nm. After being annealed for 150 mins, the RMS value increased to

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2.15 nm. Moreover, the surface morphology of the sample A was much smoother compared with the Cu/Ta/ULK structure without SiCN layer. SiCN has high hardness, and it could withstand the stress from Ta and Cu during thermal annealing. It was also amorphous and therefore could prevent the diffusion of element in the ULK into the barrier. This may explain the smoothness of Cu film when SiCN was incorporated.

Fig. 5.7. Surface morphology of Sample A before and after being annealed for 150 mins.

For sample B (shown in Fig. 5.8), the RMS value of the as deposited sample is 0.89 nm. After being annealed for 150 mins, the RMS value increases to 2.32 nm. The surface morphology of the samples B is also smoother than that of the Cu/TaN/ULK sample (RMS values: 4.76 nm for as-deposited, 76.38 nm after being annealed for 150 mins) due to the same reason.

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Another factor for improvement the thermal stability with additional barrier SiCN layer is due to the lower surface diffusion of SiCN on the ULK. Yanovitskaya *et al* [119] simulated deposition of TaN on low k films by a Monte Carlo model. It provided the explanation for the sealing behavior of TaN on porous low k films. The minimal barrier thickness needed for complete sealing of the porous films is a function of activation energy. The minimal thickness for Ta and TaN barrier is around 25 nm, but for the SiCN barrier, the thickness is around 10 nm, or even less. The following electrical testing results can also prove it.

As-deposited sample B

RMS value: 0.89 nm

After being annealed for 150 mins

RMS value: 2.32 nm

Fig. 5.8. Surface morphology of sample B before and after being annealed for 150 mins.

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5.3.3.3 Microstructure

For the sample A, the XRD measurements results show that the Cu (111), Cu (200) and Cu (220) peaks exist in the as-deposited sample (Fig. 5.9). However, after being annealed, the only phase detected is Cu (220). It is noted that the Ta microstructure is different from that in the Cu/Ta/ULK structure. The peaks appeared are Ta (200), Ta (202) and Ta (513), respectively, which are the feature of tetragonal β phase [50], while the Ta deposited on the ULK directly shows the BCC α phase. And the Ta (110), which is the characteristic peak of BCC α phase, is thought to be the growth promoter of Cu (111). In the Cu/Ta/SiCN/ULK structure, Ta does not directly contact with ULK due to the additional SiCN layer, which results in tetragonal β phase not BCC α phase Ta. Consequently, formation of Cu (111) was deterred. The lower intensity and broader peaks of Ta indicates that the Ta film has finer grains. We also observed that the intensity of Cu (220) had increased after annealing, thereby indicating the enhanced crystallization of Cu (220).

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Fig. 5.9. XRD patterns of Sample A after being annealed at 400°C for different periods of times.

For the sample B (as shown in Fig. 5.10), the only phase detected before and after annealing was Cu (220). And the intensity of Cu (220) had increased after annealing, thereby indicating the enhanced crystallization of Cu (220). Compared to the Cu/TaN/ULK structure, the preferred orientation had also changed from Cu (111) to Cu (220). This is because the TaN deposited on SiCN has different texture from that deposited on the ULK porous SiLK. The TaN (111) peak does not appear in the XRD patterns, which indicates the TaN is amorphous when it is deposited on the SiCN. As reported by Riekkinen [47] and Nie [140], the character peak of FCC TaN centered at 35.4° becomes dominant when it is deposited on the SiO₂ substrate. However, in this

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case, same deposition condition is used to deposit TaN on ULK and SiCN respectively, but no peak appeared in TaN/SiCN structure. According to our previous results, if the grain size is larger than 4.6 nm, a very broad peak can be captured by XRD. Here no peak appearing in XRD measurement means its grain size is smaller than 4.6 nm and its structure is amorphous or close amorphous. So the Cu grows on the amorphous TaN in the random texture (220). It is obvious that the introduction of an additional SiCN layer will affect the Cu and TaN textures.

Fig. 5.10. XRD patterns of sample B after being annealed at 400 °C for different periods of time.

5.3.3.4 TEM

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Fig. 5.11.a shows the TEM image of Sample A after being annealed at 400°C for 150 mins. It could be observed that there was a smooth interface between ULK and SiCN, and no significant reaction and diffusion appeared at this interface. And no Ta or Cu diffusion is observed in ULK region. However, at the Ta/SiCN interface, it shows the sign of intermixing. At some places, the Ta diffusion into Cu layer can also be observed. Fig. 5.11.b shows the TEM images of sample B after being annealed at 400°C for 150 mins. Similar results can be observed except the difference in the metal barrier.

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Fig. 5.11. TEM images of a) sample A and b) sample B after being annealed at 400°C for 150 mins.

5.4 Summary

The effect of SiCN on the thermal stability of the Cu/barrier/ULK structures was investigated. Comparing with the barrier Ta and Ta based in the Cu/barrier/ULK structure, the SiCN barrier showed many advantages: lower density (3.25 g/cm³), higher hardness (460 GPa), amorphous structure without grain boundary defects, better thermal stability and no reaction with Cu, ULK and oxygen after being annealed at 400°C for 150 mins. So it can be thought as a good barrier candidate for Cu and ULK integration.

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Introducing an additional SiCN barrier layer to the Ta barrier can significantly improve the thermal stability because the amorphous structure of the SiCN not only effectively blocks ULK out-diffusion, but also prevents the Cu, Ta from diffusing into ULK. The thin SiCN film deposited on the ULK surface can also significantly improve the surface mechanical property and thermal stability. Similar results can also be observed for the sample with TaN barrier. When SiCN additional layer was added to TaN barrier, the barrier shows much better performance. TEM pictures show fairly smooth interfaces up to 400°C. AFM measurement shows only a small increase in roughness of Cu film surface due to the Cu grain growth. No new phases are detected by XRD investigation at 400°C up to 150 minutes of annealing time.

CHAPER 6 Effect of plasma treatment on the thermal stability of Cu/Barrier/ULK porous SiLK structures

CHAPER 6

Effect of plasma treatment on the thermal stability of

Cu/Barrier/ULK porous SiLK structures

6.1 Introduction

Plasma is an environmentally safe method of organic removal and surface modification. When plasma gas interacts with the surface of polymers, four primary effects can occur: the removal of organic materials, CASING (CASING is an acronym referring to the use of inert gas as the plasma for treatment on polymer surfaces) or cross-linking via activated species of inert gases, ablation, and surface chemical restructuring. Surface chemical restructuring, by adding polar functional groups to the surface structure, greatly increases the surface energy and associated adhesion to other materials. Ablation roughens the surface increasing the total contact area between the adhesive and the subsurface. As we know, many wafer processing steps need plasma treatment during wafer process. The plasma pretreatment is used to remove oxides and etch residues that contaminate the metal surface at the bottom of via. In this work, the ULK surface firstly was treated by N_2/H_2 plasma, then Ta or TaN barriers with Cu layer were deposited. Hydrogen plasma is considered as a promising technique for the dry resist stripping as oxygen plasma is found to cause significant damage to some ultra low-k materials [132]. The plasma etch gas combinations of (N_2+H_2) were chosen based on certain criterion as explained below. The combinations chosen are the conventional

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gas mixtures widely used in etching processes of various dielectric films in the Cu/low-k dual damascene interconnects technology development. This selection criterion will enable to simulate the effect of the ULK material when this plasma etch gas mixtures are applied during the actual pattern transfer process, e.g., trench, via and dual damascene etching. The plasma exposure time of the individual gas mixtures was adjusted such that approximately the same thickness of the ULK film was removed [133]. The thermal stability of the structures was then investigated and compared with that without plasma treatment using various techniques.

6.2 Experiment procedure

The samples studied were the Cu/Ta/Plasma-treatment/ULK (sample A) and Cu/TaN/Plasma-treatment/ULK (sample B) structures. Samples used were the 8-inch p-type Si (100) wafers. Firstly, a 200 nm of SiO₂ film was deposited and followed by a 310 nm porous ULK deposited by spin-on technology. The samples were treated by forming gas N₂/H₂ plasma for 20 second at 135°C, and then Ta film was deposited onto the ULK/SiO₂/Si substrate at room temperature using SIP technique. The Cu film of about 150 nm was deposited at -40°C by the same technique without breaking the vacuum. For the Cu/TaN/plasma-treatmentULK/SiO₂/Si structures samples (sample B), the preparation procedure is almost same as that of sample A except the different barrier layer.

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To evaluate the thermal stability, the blanket samples were annealed in high vacuum of 10^{-6} Pa at 400°C for 5 thermal cycles by RTP and each cycle was 30 minutes. Characterization was carried out using various techniques.

6.3 Results and discussion

6.3.1 Sheet resistance

Fig. 6.1 shows that as the annealing time increased, the sheet resistance of the sample A decreased in contrary to the increasing trend of the untreated Cu/Ta/ULK sample. The sheet resistance for the as deposited sample A is about 0.128 ohm/sq, which is higher than that of Cu/Ta/ULK due to smaller grain size and more grain defects. Stanley Wolf [129] reported the film resistivity is a strong function of grain size, and annealing of Cu films also reduce their resistivity by up to 20% due to grain growth [134]. Thin films with larger grains generally have a smaller resistivity than those with smaller grains. This is because in films with larger grains there are fewer grain boundaries – which cause carrier scattering, and thus degrade conductivity. In this case, for the as-deposited Cu/Ta/ULK film, it is highly defective and its resistivity is also high due to lower deposition temperature. It trends to reduce the defect level by re-crystallization during annealing. The grains grow larger by consuming defective grains, leaving defects mainly in the grain boundaries and interface [85]. However, after being annealed for 150 mins, the value of sheet resistance of sample A is only 0.1 ohm/sq, and the variation percentage of sample A is -19%. One possible explanation is

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that the hydrogen ions produced during plasma treatment would react with oxygen and prevent the formation of oxides [80]. The drop of sheet resistance with increased annealing time was thought to be caused by a decrease of the defect density and the grain growth of the copper film [81].

For sample B, the same trends as the sample A can be observed. Comparing with sample A, the sample B has higher sheet resistance due to the TaN barrier. After being annealed for 150 mins, the sheet resistance also drops because of the decrease of the defect density and the grain growth of Cu film. The variation percentage of sample B is -21.3%.

Fig. 6.1. Sheet resistance vs annealing time for sample A and sample B with and without plasma treated at 400°C.

6.3.2 Surface morphology

It is observed from Fig. 6.2 that the surface roughness of sample A has remained relatively constant. The result also shows much smoother surface with much lower

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RMS values (2.99 and 3.34 nm for the as-deposited and the annealed for 150 mins respectively) compared with the untreated sample Cu/Ta/ULK (4.23 and 41.23 nm, as shown in Fig. 4.2.a&d). These results suggest that the introduction of hydrogen during the plasma treatment had improved the surface morphology. Choi [80] reported that hydrogen radicals would enhance the reflow of Cu which resulted in smoother Cu film. Cu reflow was the movement of Cu atoms resulting from gradients of a chemical potential due to the curvature of the metal surface.

Fig. 6.2. Surface morphology of Cu film deposited on plasma treated Ta (sample A) for the as-deposited and annealed samples.

From the AFM results of sample B presented in Fig. 6.3, it could be observed that the RMS values remained relatively constant, which are significant lower than that of untreated Cu/TaN/ULK samples. This meant that the surface roughness was improved by the plasma treatment.

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Fig. 6.3. AFM results of Cu film deposited on plasma treated ULK with TaN barrier (sample B) for the as-deposited and annealed samples.

6.3.3 Microstructure

Like the untreated sample Cu/Ta/ULK structure, the XRD results of sample A did not show any new phases after being annealed at 400°C for 150 mins. The main phases detected before and after annealing are Cu (111), Cu (200), Cu (220) and Ta (110). However, unlike the untreated sample Cu/Ta/ULK, there was less phase shift of Ta (110) comparing with the untreated sample. As we assumed that the peak shift was due to the incorporation of O atoms impurity, the plasma treatment seemed to remove at least some of the impurity [80]. This may also explain the improvement in sheet resistance shown earlier.

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In the experiment, it was also observed that the peak intensity ratio of Cu (111)/Cu (200) increases after plasma treatment. However, the short and broad peaks of Ta (220) and Ta (211) don't exist after annealing. Moreover, there was a decrease in peak intensity of Cu (111) as annealing time increases. This may be due to the inter-diffusion in the Cu/Ta/ULK sample.

Fig. 6.4. XRD results of sample A after being annealed at 400°C for various periods.

Like the untreated Cu/TaN/ULK sample, the XRD results of sample B show no new phases formed after being annealed at 400°C. The main phases detected before and after annealing are Cu (111), Cu (200), and Cu (220). For the TaN barrier, its peak is broad, which indicates an amorphous structure. The intensities of Cu (111), Cu (200) and Cu (220) have basically no change even after being annealed for 150 mins.

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Fig. 6.5. XRD results of sample B after being annealed at 400 °C for different periods of time.

6.3.4 TEM results

The TEM results of sample A after being annealed at 400°C for 150 mins (Fig. 6.6.a) show that diffusion has occurred at the Cu, Ta and ULK interfaces. The reaction, diffusion area and rougher interface can be observed. These results supported the findings from the XRD measurements that there were still inter-diffusion between the barrier and ULK. This shows that the role of plasma treatment is mainly to remove impurity which leads to improvement in sheet resistance rather than improving the barrier capability against diffusion. Moreover, comparing TEM results between

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untreated and plasma treated samples, it seems that the diffusion between Ta and ULK was more severe in the plasma treated sample. This may be because the plasma treatment has introduced radicals and new carbonyl bonds on the surface, which enhances the reaction between Ta and ULK. On the other hand, more defects are created at the ULK surface by the plasma treatment. However, the carbide bonds on the dielectric surface are weakened (mainly C-H like) due to charge delocalization effects induced by the presence of neighboring Ta metal atoms. Moreover, the plasma energy released during treatment further favors the breaking of these bonds, and can lead to cross-linking of the top layers of the matrix through the formation of a C-C bond across the chains, which can improve the surface mechanical property of ULK, so the surface roughness changes less till after being annealed for 150 mins. Further study to find the optimal condition used for plasma treatment was required.

Fig. 6.6.b presents the TEM images of sample B after being annealed at 400°C for 150 mins. The inter-diffusion between the TaN barrier and ULK is severe, and the diffusion length from the TaN barrier to ULK is around 66 nm, which is larger than that of untreated Cu/TaN/ULK. It indicates the rougher ULK surface caused by the plasma treatment provides larger contact area with the barrier layer, which offers more possibility for the reaction between TaN and ULK. Cu has also penetrated the TaN at some places.

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Fig. 6.6. TEM image of a) Sample A and b) sample B after being annealed at 400°C for 150 mins.

6.4 Summary

Plasma treatment seems to cause higher sheet resistance for the as-deposited sample because of more defects associated with the treatment and annealing results in lowering the sheet resistance. It helps to improve the smoothness of Cu film as can be seen by AFM results due to the surface modification. Such treatment also has critical drawbacks: 1) it can lead to degradation of the ULK; 2) it also causes surface damage and degradation of the thermal stability.

Similar results can also be observed for blanket TaN samples. Plasma treated TaN blanket samples also show some improvements compared to untreated TaN. The peak

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intensities of Cu (111) and Cu (220) are relatively stable after being annealed for 150 mins, whereas for untreated TaN we notice the increase in Cu (111) peak and the decrease in Cu (220) peak. AFM results of Cu films also show much smoother surface. The sheet resistance of plasma treated TaN after being annealed for 150 mins is also lower ($0.112 \text{ } \Omega/\text{sq}$) compared to that of untreated TaN ($0.127 \text{ } \Omega/\text{sq}$). However, TEM results for plasma treated TaN at 400°C shows that severe diffusion has occurred.

CHAPTER 7 Single damascene integration of Cu and ultra low k porous SiLK

CHAPTER 7

Single damascene integration of Cu and ultra low k porous SiLK

7.1 Introduction

In the last five chapters (chapter 2 to chapter 6), I have presented studies of ultra low k porous SiLK, Ta and Ta-based diffusion barrier layers, the SIP Cu seed layer deposited on different barrier layers, effects of plasma treatment on the thermal stability of Cu/barrier/ULK structures, and effects of an additional SiCN barrier layer prior to Ta deposition. To better evaluate the performance of ULK porous SiLK, Ta and Ta-based barrier layer, SIP Cu seed layer as well as the plasma modification, it is necessary to apply them to the interconnect technology for deep submicron integrated circuits using damascene structures. In this chapter, the electrical performance and thermal stability of single damascene (SD) structures for 0.13 μm technology fabricated at different conditions will be presented. These include comparative studies of electrical performance and thermal stability of Cu/barrier/ULK structures with different barriers, plasma treatment and effects of an additional barrier layer SiCN on electrical performance and thermal stability and optimization of the thickness of SiCN layer.

7.2 Integration process of Cu and ULK for 0.13 μm technology

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Single damascene structures with different barriers were fabricated on 8-inch p-type (100) oriented silicon wafers. After all wafers were cleaned using standard procedures, a SiO₂ film of 500 nm was first deposited, followed by a layer of SiC of 50 nm as etch stop layer and 300 nm of porous ULK was deposited by spin-on technology for metal 1 trench, then a dual CVD hard mask consisting of 50 nm SiC and 200 nm SiO₂ were deposited. The SD structures were formed after patterning, etching and clean. Fig. 7.1 presents the trench pattern of a 0.18 μm structure after etching.

Fig. 7.1. SEM trench pattern after etch

After the SD patterns were formed, the Ta and Ta-based barrier were deposited by self ionized plasma (SIP) technology firstly, then 150 nm Cu seed layer was deposited using the same technology, followed by electrical chemical plating (ECP) Cu gap-fill and chemical mechanical polishing (CMP). Finally, an aluminum (Al) of 750 nm, a TaN (25 nm) as well as passivation layer (SiC/SiO₂) were deposited and etched to form

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bond pads for electrical test. Fig. 7.2 shows the detail of metal line formation for 0.13 μm technology.

Fig. 7.2. Formation of metal layer in single damascene structures for 0.13 μm technology

To study the leakage current and line resistance, the bridging/continuity structures, as schematically shown in Fig. 7.3, were fabricated. There are three Cu lines in the figure. They are comb 1, comb 2 and serpentine lines (sandwiched between comb structures), respectively. The leakage current was measured by applying a voltage between the serpentine line and one of the comb lines (1 or 2) while the line resistance

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was measured by applying a voltage to the two serpentine pads. The serpentine line is 0.192 m long, which is the product of $640 \times 300 \mu\text{m}$ (640 lines and each $300 \mu\text{m}$), and $0.35 \mu\text{m}$ thick. The line width varies from $0.16 \mu\text{m}$ to $0.26 \mu\text{m}$, and the line spacing between the serpentine and the comb lines also varies from $0.16 \mu\text{m}$ to $0.26 \mu\text{m}$.

Fig. 7.3. Schematic diagrams of bridging/continuity structures, which contains comb 1, comb 2 and serpentine line.

7.3 Effect of metal barriers (Ta, TaN, Ta/TaN) in the Cu/barrier/ULK porous SiLK structures on the electrical performance and thermal stability

In chapter 3, we comparatively investigated the thermal stability and properties of three kinds of barriers (Ta, TaN, and Ta/TaN) on blanket wafer. In this section, the integration of Cu and ULK with three kinds of barriers has been implemented for $0.13 \mu\text{m}$ technology. The electrical performance, such as line resistance, line-to-line leakage and breakdown voltage, will be evaluated. To compare the electrical performance of different barriers, the samples were divided into three groups after formation of SD

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structure (shown in Fig. 7.2 (b)): the first group has Ta barrier (group A). The second group has TaN barrier (group B). The third group has Ta/TaN bi-layer barrier (group C). All samples were merged, and then 150 nm Cu seed layer was deposited by the same technology, followed by ECP Cu gap-fill and CMP. Finally, an Al of 750 nm, a TaN (25 nm) as well as passivation layer (SiC/SiO₂) were deposited and etched to form bond pads for electrical test.

7.3.1 Line resistance

The serpentine line in the Bridging/continuity structures (shown in Fig. 7.3) with a length of 0.192 m was used for the measurement of line resistance at room temperature. In order to look at the effect of line width, three kinds of line width 0.18, 0.20, and 0.22 μm were tested. Fig. 7.4 shows the comparison line resistance of group A, B, and C samples with different line widths. As shown in Fig. 7.4(c), the line resistance has no significant difference for three groups of samples with line width of 0.22 μm . The resistance values are 44596, 47135 and 46273 Ω for group A, B, and C, respectively. From the Equation (1.4), we expect that when the line width W_l is reduced to 0.18 μm , the line resistance will increase. The measured line resistance values of group A, B and C are 58051, 95090, and 55506 Ω , respectively. For group B, the line resistance is significantly higher than that of groups A&C at 0.18 μm because TaN has larger resistance than that of Ta and Ta/TaN, which has been discussed in chapter 3.

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Fig. 7.4. Comparative line resistance of three groups of samples for different line widths. a) 0.18 μm ; b) 0.20 μm ; c) 0.22 μm ;

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7.3.2 Line-to-line leakage

One comb line and the central serpentine line in the Bridging/continuity structures were chosen to measure the line-to-line leakage current. Both the line width and spacing we have chosen in this work are 0.24 μm . The leakage currents at room temperature at 1 V are shown in Fig. 7.5. As seen from the figure, the currents of group B&C samples are slightly different, and the main distribution is between 1 to 3×10^{-12} A. But the leakage currents of group B show a tighter distribution and smaller values for measured 24 dies. Group A samples show larger leakage values than that of group B&C, and the main distribution is around 1 to 3×10^{-11} A. The results are easily understood as discussed in chapter 3. TaN is a better barrier because of smaller grain size and blur grain boundary due to the incorporation of N. But Cu can penetrate Ta barrier through the grain boundary defects in the barrier layer. For the Ta/TaN bi-layer barrier, it takes the advantage of both Ta and TaN barriers and gives reasonable resistance and thermal stability. It also shows good capability to block Cu diffusion due to the thin TaN layer.

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Fig. 7.5. Line-to-line leakage current distributions of three groups of samples with a line width of 0.24 μm and spacing of 0.24 μm .

TEM was performed to observe the trench sidewalls of three groups of as-fabricated samples. Fig. 7.6 (a) shows the sidewall of group A trench. Clear interaction region at the interface of Ta and ULK was observed (as shown in the circle). For the Ta barrier with polycrystalline structure, though it can effectively block Cu diffusion into the ULK dielectrics, it is difficult to prevent the finer C, H, O atoms in the ULK dielectric from out-diffusing into barrier and Cu layer because the grain boundary in Ta barrier can be the fast diffusion path for those smaller atoms. On the other hand, the Ta with grain size around 7-10 nm can easily enter the pore in ULK with pore size (10 nm).

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The TEM image of the group B sample was shown in Fig. 7.6(b). The TaN on the sidewall was about 7 nm thick, and no significant interaction region as in group A samples can be observed due to its better barrier function. The smaller interaction region was also observed in Fig. 7.6(c) for group C samples. The greater interaction region at the Ta/ULK interface may explain why this group has the largest leakage current. The barrier thicknesses on the sidewall are around 8, 7 and 7.5 nm for Ta, TaN and Ta/TaN barriers. The difference is probably due to the step coverage rate.

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Fig. 7.6. TEM images of trench for three groups. a) Group A, b) Group B, c) Group C.

7.3.3 Thermal stability of three groups of samples after thermal treatment

To compare the thermal stability of the three groups of samples, burn-in at 200°C for 40 hours and thermal stress at 150°C were applied. Those conditions are standard reliability test conditions [153, 154]. For the high temperature storage test, it is required

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no 20% drift for critical parameter when it is stored at 200°C. For the high temperature operation life test, the criteria are no 20% drift when measuring at 150°C.

For the burn-in experiments, the comparative data were shown in Fig. 7.7. The leakage currents of group B samples have increased with the mean leakage values around 10^{-11} A. It is because during the burn-in process, most N atoms were released from TaN film. At the same time, the microstructure was changed from FCC TaN to Ta₂N. Both the N diffusion and the subsequent Ta₂N formation can alter the original barrier properties, which results in the increase of the leakage current. The leakage currents of group C samples not only show a more spread distribution, but also increase 2 to 3 orders of magnitude as compared to that of as-fabricated samples. The leakage currents of group A samples show very significant degradation after burn-in. Some leakage values of the 24 measured dies were higher than 10^{-8} A. The mechanism of leakage current has been presented in Section 7.5.3. It has similar mechanism for three kinds of barrier structures Cu/Ta, Cu/TaN and Cu/Ta/TaN. As shown in Table 7.1, the median leakage value of Ta/TaN is comparable with that of Ta, but it is larger than that of TaN after burn-in at 200°C for 40 hours. It is in a good agreement with our blanket results as presented in Chapter 3. The bi-layer Ta/TaN barrier takes the advantage of both Ta and TaN barriers and gives reasonable resistance and thermal stability.

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Fig. 7.7. Comparison of line-to-line leakage current distributions of three groups of samples with a line width of 0.24 μm and a line spacing of 0.24 μm after burn-in.

Under thermal stress of 150°C, the leakage currents of group A, B and C samples all increased about ten times as that of as-fabricated samples. The leakage currents of group B&C samples are around 10^{-11} A, which is much lower than that of group A samples (around 10^{-10} A). For group A, the leakage currents of the 3 dies at wafer edge are higher than 10^{-5} A, and the leakage currents of some dies at wafer edge in group C samples are around 10^{-5} A, which is mainly due to the poor within wafer uniformity of PVD deposition. Although the leakage degradation happened after burn-in and under thermal stress of 150°C, the leakage mechanisms are different. We will discuss the detail in the section 7.5.3.

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Fig. 7.8. Comparison of line-to-line leakage current distribution of three groups of samples with a line width of $0.24\ \mu\text{m}$ and a line spacing of $0.24\ \mu\text{m}$ at 150°C .

The breakdown voltages of the three groups of samples were also measured in the same structure as used for leakage current measurement by increasing the applied voltage for the as-fabricated, after burn-in at 200°C for 40 hours and at 150°C respectively. For each group, 10 dies were measured, and we only show one curve has a breakdown voltage similar to the average value. Fig. 7.9 presents the comparative breakdown voltages of the three groups of as-fabricated samples. As seen from the figure, the breakdown voltages of the groups A, B and C are 42.3, 45.1 and 45.2 V

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respectively. The breakdown voltage of the group A is a little lower than that of groups B&C, but no significant difference.

Fig. 7.9. Comparative breakdown voltages of the as-fabricated samples for three groups with a line width of 0.24 μm and a line spacing of 0.24 μm .

After burn-in, the breakdown voltages of group B&C are 22.6 V and 22.1 V respectively. There are no significant differences. However, compared with the as-fabricated samples, the breakdown voltages of group B&C degrade significantly after burn-in. The group A samples not only has the smallest breakdown voltage, but also the highest leakage current. These observations indicate the TaN barrier has the best thermal stability.

The breakdown voltages of three groups of samples measured at 150°C are presented in Fig. 7.11. The breakdown voltage of group A is 25.4 V, which is

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significantly lower than that of the as-fabricated (42.3 V). The degradation is probably due to the Poole-Frenkel (PF) emission in which the trapped electrons in the ULK are excited into the conduction band [93]. The breakdown voltage of group C is 35.6 V, which is about 10 V less than that of the as-fabricated. However, the breakdown voltage of the group B samples did not drop significantly.

Fig. 7.10. Comparative breakdown voltages of three groups of samples with a line width of 0.24 μm and a line spacing of 0.24 μm after burn-in at 200°C for 40 hours.

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Fig. 7.11. Comparative breakdown voltages of three groups of samples with a line width of 0.24 μm and a line spacing of 0.24 μm measured at 150°C.

7.4 Electrical characterization of Cu/Ta/TaN/ULK structures with plasma treated on patterned wafer

As discussed in the last section and chapter 3, the bi-layer Ta/TaN on ULK takes the advantage of both Ta and TaN barriers and shows reasonable resistance and thermal stability. In chapter 6, we discussed the effect of plasma treatment on the thermal stability of blanket wafer. In this section, the effect of plasma treatment on the electrical performance and thermal stability is comparatively studied on patterned wafer for the Cu/ULK SD metal lines with the bi-layer Ta/TaN barrier. The line resistance, line-to-line leakage and breakdown voltage were evaluated.

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After the formation of the SD structure, the sample was treated by forming gas N_2/H_2 plasma at 135°C for 20 second, the bi-layer Ta/TaN barrier with thickness of 25 nm was deposited by SIP technology firstly, and then the 150 nm Cu seed layer, followed by ECP Cu gap-fill and CMP. Finally, an Al of 750 nm, a TaN (25 nm) as well as passivation layer (SiC/SiO₂) were deposited and etched to form bond pads for electrical test.

7.4.1 Line resistance

Fig. 7.12 shows the line resistance of 3 groups of samples with and without plasma treatment. The line widths of three groups of samples are 0.22, 0.20 and 0.18 μm . It is seen that the line resistances of the plasma treated samples always are lower than that of the untreated samples for all line widths. It indicates that the forming gas (N_2/H_2) plasma treated played a prominent role in preventing the Ta from being oxidized, which strongly affects line resistance in 0.13 μm and below technology. On the other hand, the plasma may etch away some atoms and make the line deeper and wider, which reduces the line resistance (as shown in Fig. 7.13). However, the spread distribution of line resistance values indicates that the process for the plasma treated samples is not stable.

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Fig. 7.12. Comparative line resistances of the samples with (open box) and without (filled box) plasma treated. The samples tested have three line widths, 0.18, 0.20 and 0.22 μm.

TEM was performed to observe the trench structure and sidewall interface of the as-fabricated plasma treated samples. The TEM images were shown in Fig. 7.13. The voids were clearly observed in some trenches, which contribute to the larger line-to-line leakage current, lower breakdown voltage and worse thermal stability. The void formation can be explained as follows: When the forming gas N_2/H_2 plasma is used to treat the ULK surface, it etches trench sidewall and bottom, and causes rougher ULK surface. This will bring some problems. First, when the barrier and SIP Cu seed layer were deposited onto the rougher surface directly, the uniformity of Ta/TaN and Cu thin film will be significantly affected by the rougher substrate. So the voids were created when using electrical plating Cu to fill the trench. Secondly, the defects created by

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plasma treated provide much higher probability for the C, H, O atoms in ULK out-diffusion into barrier as well as Cu, Ta diffusing into ULK when the thermal and electrical stress are applied.

Fig. 7.13. TEM images of trench for the plasma treated samples.

7.4.2 Line-to-line leakage

The leakage currents data of the samples with and without plasma treatment are shown in Fig. 7.14. As seen from the figure, for the as-fabricated samples, the leakage currents of untreated samples show a narrower distribution for the measured 24 dies. Several dies of plasma treated samples exhibit higher leakage current values (more than 10^{-5} A). For the burn-in samples, the leakage currents of untreated samples still keep the narrow statistical distribution with values around 10^{-10} A. The leakage currents of the plasma treated samples not only show wide distribution, but also are increased by 2 to 4 orders of magnitude as compared to the as-fabricated samples. It is because the plasma

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treatment brings more surface defects on the ULK sidewall, which may enhance diffusion and cause higher leakage current.

Fig. 7.14. Comparison of line-to-line leakage current distribution of three groups of samples with a line width of $0.24\ \mu\text{m}$ and a line spacing of $0.24\ \mu\text{m}$ with and without burn-in at 200°C for 40 hours, respectively.

The breakdown voltages of the plasma treated and untreated samples were also measured by increasing the applied voltage before and after burn-in at 200°C for 40 hours. Fig. 7.15 presents the comparative breakdown voltages of the plasma treated and untreated samples under different conditions. For the as-fabricated samples, the breakdown voltages of the plasma treated and untreated samples are 26 V and 45.2 V respectively, which suggests the plasma treatment may cause the electrical performance

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degradation. After burn-in, the breakdown voltage of the plasma treated samples is 12.1 V, but the breakdown voltage of untreated samples is 22.1 V. These data clearly indicate that plasma treated causes higher leakage current and lower breakdown voltage.

Fig. 7.15. Comparative breakdown voltages of the plasma treated and untreated samples with a line width of 0.24 μm and a line spacing of 0.24 μm with and without burn-in at 200°C for 40 hours, respectively.

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7.5 Effect of SiCN barrier on the electrical performance of Cu lines in the Cu/Ta/TaN/ULK structures

From the chapter 5, we know that the samples with additional SiCN layer combined with Ta or TaN barrier can significantly improve the thermal stability on the blanket wafer because the amorphous SiCN layer not only effectively blocks the out-diffusion of the elements in the ULK, but also prevents the Cu, Ta from diffusing into ULK. Moreover, the thin SiCN layer deposited on the ULK surface can also significantly improve the mechanical property and thermal stability. In this section, we will compare the electrical performance of samples with and without SiCN barrier on the patterned wafers. Two groups of single damascene metal lines were fabricated. One group only has with Ta/TaN bi-layer barrier (group A), the other group has SiCN and bi-layer Ta/TaN as the barrier (group B). Finally, the line resistance, line-to-line leakage, breakdown voltage and leakage mechanism, were comparatively studied.

7.5.1 Line resistance

Fig. 7.16 shows the line resistances of group A and B with different line widths. The line resistance has no significant difference between group A and B when the line is 0.22 μm thick. The values are 46273 and 47062 Ω for group A and B, respectively. For a line width of 0.18 μm , the line resistance of group A slightly increases due to the line width scaling, and the value is 55506 Ω . However, the line resistance value of

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group B becomes 389 k Ω , which is significantly higher than that of group A at 0.18 μm . This is because the additional layer SiCN causes reduction of the metal line width, which leads to the increase of the line resistance.

Fig. 7.16. Comparative line resistance of two groups of samples with different line widths. (group B (open box), group A (filled box))

Fig. 7.17 presents the sidewall of group B trench of the as-fabricated samples. From the graph, we can observe the thickness of SiCN around 10 nm. There is no significant intermixing observed. For the group A samples, as shown in Fig. 7.6.c, the small intermixing area appeared on the sidewall, which is believed to degrade the electrical performance. When the additional amorphous SiCN barrier layer is introduced between Ta/TaN and ULK, which has no grain boundary defects, it improves the electrical performance and thermal stability significantly. The thickness of SiCN at the bottom is

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around 15.5 nm, and 9.5 nm at the sidewall when a 50 nm SiCN was deposited on the top. Hence, the step coverages of the bottom and sidewall are 31% and 19% respectively. However, for the Ta/TaN barrier, the thickness at the bottom and sidewall is 14.8 nm and 7.2 nm when a 25 nm Ta/TaN was deposited on the top, and the step coverages of bottom and sidewall are 58% and 28%.

Fig. 7.17. TEM images of trench for group B, a) Sidewall, b) bottom of the trench.

7.5.2 Line-to-line leakage

The leakage currents of the two groups of samples are shown in Fig. 7.18. The main distribution of group B samples is around 8×10^{-12} A. But the leakage currents of group A samples exhibit higher values, which are around 8 to 9×10^{-11} A, which is ten times as that of group B. For the samples after burn-in, the leakage currents of group B samples are even smaller than that of the as-fabricated samples. Its statistical

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distribution is around 9×10^{-12} A. But the leakage currents of group A samples have 2 orders degradation, and the mean leakage value is 8 to 9×10^{-19} A.

Fig. 7.18. Comparative line-to-line leakage current statistical distribution of the two groups of samples with a line width of $0.24 \mu\text{m}$ and a line spacing of $0.24 \mu\text{m}$ before and after burn-in at 200°C for 40 hours, respectively.

The breakdown voltages of the two groups of samples were also measured in the same structure. Fig. 7.19 presents the comparative breakdown voltage of the two groups under different conditions. For the as-fabricated samples, the breakdown voltages of groups A&B are 45.2 and 64.1 V respectively. It indicates that the group B samples can stand higher electrical field because of the additional thin SiCN barrier

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layer. After burn-in, the breakdown voltages become 53.2 V for the group B samples only 22.1 V for the group A samples. These data clearly indicate that group B samples have better thermal stability and better electrical performance than the group A samples.

Fig. 7.19. Comparative breakdown voltages of the two groups of samples with a line width of 0.24 μm and a line spacing of 0.24 μm before and after burn-in at 200°C for 40 hours.

7.5.3 Leakage current and breakdown mechanism for ULK

To explain those results of leakage current, the dielectric breakdown mechanism

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should be discussed. A simplified picture of dielectric breakdown has two components: a physical mechanism that describes how microscopic defects are generated in the dielectric under stress conditions and a statistical model that describes how the accumulation of these microscopic defects finally leads to dielectric breakdown, which is a macroscopically detectable event. The percolation model [94] is such a statistical model and has found wide acceptance. According to this model, microscopic defects are created under electrical stress randomly distributed in the dielectric. These microscopic defects are assumed to be electrically conductive. As the degradation continues, these defects accumulate in the dielectric until a critical defect density is reached. At this point a conducting path is created between the electrodes, which results in an abrupt increase of the leakage current through the dielectric. The current density in the conduction path is normally high that the dielectric around the conducting path thermally degrades or even melts and creates a hard breakdown, which means a permanent low resistance short between the electrodes. For the oxide dielectric, the model is well supported by experiment data [95]. However, the mechanism of electrical transport in polymer is still in dispute. Tu [97] reported that polyimide has a narrow valence band with a bandwidth of about 0.25 eV. It implies that the holes in polymer are strongly localized and would not contribute much too electrical conduction. Although the metal electrode may inject holes, these holes because of their localization would immediately form a positive charge layer very near the electrode to suppress further injection. So the electrical conduction is mainly due to the electron transport. Polymer consists of polymer chains of repeated units. Electrons may migrate along the

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chain (intra-molecular transfer), as well as between the chains (intermolecular transfer). Polymer falls into the class of donor-acceptor polymers [98]. It is likely that electrons may move via a hopping process under electric fields from acceptor to next acceptor.

For porous dielectrics with large surface due to open pores lying at the surface, two leakage paths are possible. Surface leakage is originated from the internal surfaces of voids and bulk leakage is related to the defect states in the band gap of IMD. Surface leakage is important in high porosity materials especially above the percolation threshold. For low k materials with closed pore and narrow pore size distribution, it is expected that the bulk leakage influence to be more significant. The bulk leakage current in dielectrics is due to injection of carriers into the bands or hopping of carriers between localized states within the band gap. Hopping refers to a thermally assisted tunneling process. The localized states (looked as traps) are formed in the band gap because of a lack of long range order in the microstructure. According to Kao's electrical breakdown model [99], each electron trapping evolves the energy of the order of 2–5 eV depending on the trap energy level for large band-gap materials. The band gap of ULK is about 7 eV. This range of energies evolved is possible, and this energy will be dissipated in the material in the form of breaking bonds and hence, creating defects and new traps. This indicates clearly that the electrical conduction at high fields is filamentary. It can be imagined that if the total current flows mainly through the filament the current density and the energy stored in it would be much more than the energy required causing thermal instability. The destructive breakdown is initiated by

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thermal instability and following by the creation of low-density regions which provide large mean free paths for subsequent impact ionization leading to a sharp increase in current at the breakdown field [97].

Besides the nature properties of ULK dielectric, the metallic intermixing also contributes to the dielectric electrical properties degradation. Gonella et al [100] reported the Cu induced degradation model for dielectrics: defects generation within the dielectrics is enhanced by drifting or diffusing Cu ions during their displacement; these defects allow the electronic current to increase gradually, during the stress. Once the defect density locally reaches a level such that a critical path is generated between the electrode and the substrate, electrons flow directly from the cathode to the anode, a discharge takes place leading to the fatal breakdown. It can be used to explain the leakage current and breakdown voltage degradation for the group A samples after burn in because the thermal stress caused largely Cu and Ta diffusing into the ULK, which can be proved by TEM results (shown in Fig. 7.6.c).

Based on the above discussion, the electrical behavior of group B samples can be understood easily because of additional SiCN barrier layer, which can efficiently prevent Cu, Ta from diffusing into ULK and lower the Cu induced degradation as discussed in chapter 5.

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7.6 Comparative studies of metal lines in Cu/TaN/ULK and Cu/TaN/SiCN/ULK structures

As discussed in the last section, the SiCN combined with Ta/TaN barrier can significantly improve the electrical performance and thermal stability of the single damascene structure. In this section, the Cu/TaN/ULK structure will be discussed. Here, we define the sample with Cu/TaN/SiCN/ULK structure as group A, and the samples with Cu/TaN/ULK structure as group B.

7.6.1. Results and Discussion

Three structures with line width of 0.18, 0.20, and 0.22 μm were tested to get the relationship of line resistance with line width. From Fig. 7.20, it is found that the line resistance increased with line width shrinking due to electron scattering at Cu/barrier-metal interface for the narrow-line Cu interconnects [87]. The distribution also became widely spread because the step coverage degraded for the high A/R structure. Comparing the two groups of samples, the mean value of group A samples (open box) is larger than that of group B samples (filled box). The difference also increased with line width shrinking because introducing additional layer SiCN with thickness around 10 nm. Since the additional layer SiCN reduced the Cu line width compared with group B samples with the same trench.

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Fig. 7.20. Comparison of line resistance of two groups of samples with a line width of 0.24 μm and a line spacing of 0.24 μm for different line widths. (group A (open box), group B (filled box))

The leakage current measured from 20 dies of each group of samples was presented in the form of cumulative percentage in Fig. 7.21. As shown in the figure, the leakage current of the two groups of samples without thermal treated is 1.08×10^{-12} A and 1.89×10^{-12} A respectively. The leakage also showed almost negligible deviation among the measured 20 dies. Burn-in at 200°C for 40 hours was carried out to evaluate the thermal stability of two groups of samples. The comparative data are also shown in Fig. 7.21. For the burn-in samples, the leakage of group A samples still showed a stable statistical distribution around 4.89×10^{-12} A. The slightly lower leakage value could be due to removal of the residual gas and vapor from the device during burn-in process.

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However, the leakage of group B samples had a significant degradation after burn-in, the leakage value of the 24 measured dies was higher than 10^{-11} A. It was noted that the leakage value increased about of 1 order compared with that of the as-fabricated samples.

Fig. 7.21. Comparison of line-to-line leakage current statistical distribution of two groups of samples with line width $0.24\ \mu\text{m}$ and line spacing $0.24\ \mu\text{m}$ before and after burn-in at 200°C for 40 hours;

Fig. 7.22 showed the breakdown voltage of the two groups of samples under different conditions. The breakdown voltages of the as-fabricated for group A and B samples are $69.2\ \text{V}$ and $45.8\ \text{V}$ respectively. After burn-in, the breakdown voltage of group A samples slightly decreased to $66.7\ \text{V}$, while it significantly drops to $22.6\ \text{V}$ for the group B samples. The reason has been discussed in section 7.3.

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Fig. 7.22. Comparative breakdown voltage of two groups of samples with line width 0.24 μm and line spacing 0.24 μm before and after burn-in at 200°C for 40 hours.

Fig. 7.23 shows that the SiCN and TaN layer at the sidewall are 12 nm and 6 nm thick respectively. The pores in the sidewalls were better sealed with SiCN better than the TaN barriers. Furthermore, the thin SiCN layer could also block the C, H, and O in the ULK dielectrics into the metal barrier and Cu because of its amorphous structure and good mechanical properties. It is obvious that group A samples have better thermal stability and electrical performance as compared with group B samples,

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Fig. 7.23. TEM images of trench sidewall of group B samples.

Therefore, as an additional dielectric barrier layer SiCN with thickness around 10 nm was deposited on the sidewalls prior to TaN metal barrier deposition by PECVD. It was found that the leakage current decreased by 1 order of magnitude and breakdown voltage increased 200% compared with the samples without SiCN layer after burn-in at 200°C for 40 hours.

7.7 Optimization of the thickness of the SiCN barrier layer

7.7.1 Introduction

From the results of last two sections, it is obvious that introducing an additional thin barrier SiCN layer between the ULK and Ta-based barrier can significantly improve

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the electrical performance and thermal stability of the single damascene metal line. This is because the amorphous SiCN layer not only blocks out-diffusion of element in the ULK film, but also prevents Cu, Ta(N) from diffusing into the ULK. However, with the SiCN thickness increasing, the line resistance also increases significantly, especially when the line width shrinks. Hence, the thickness of the SiCN layer needs to be optimized. In this section, four groups of samples with different SiCN thickness (0, 10 nm, 20 nm and 50 nm respectively) will be comparatively studied.

7.7.2 Experiment

Single damascene (SD) structures with different thicknesses of the SiCN layer were fabricated on 8-inch p-type (100) oriented silicon wafers. After all wafers were cleaned using standard procedures, a SiO₂ film of 500 nm was first deposited, followed by a 50 nm thick SiC as etch stop layer, and 300 nm of porous ULK for metal 1 trench. Then, a dual CVD hard mask composed of 50 nm SiC and 200 nm SiO₂ were deposited. The SD structures were formed after patterning, etching and clean. The samples were divided into four groups which had different thickness of SiCN layer deposited. The thicknesses of the SiCN layer in groups A, B, C and D samples are equivalent to 0, 10, 20, and 50 nm on the top respectively. As discussed in the section 7.5, the step coverages of SiCN at the bottom and sidewall are 31% and 19%, respectively. Hence, the estimated thicknesses on the sidewall are approximately 0, 2, 4 and 10 nm, respectively. The four groups of samples were then merged for a Ta barrier; a 150 nm

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Cu seed layer, followed by ECP Cu gap-fill and CMP. Finally, an Al of 750 nm, a TaN (25 nm) as well as passivation layer (SiC/SiO₂) were deposited and etched to form bond pads for electrical test.

7.7.3. Results and discussion

7.7.3.1 Line resistance

The Bridging/continuity structures with the serpentine line length of 0.192 m, were used for the measurement of line resistance on 42 dies at room temperature. In order to get the effect of A/R ratios of two kinds of line width, 0.18 and 0.22 μm , were tested. Fig. 7.24 shows the comparison line resistance of the four groups of samples with different line widths. As shown in Fig. 7.24.b, the line resistance has no significant difference among samples in groups A, B, and C when the dimension of line is 0.22 μm . The average resistance values are 46932, 44831 and 46935 Ω , respectively. However, it is obvious that the line resistance of the group D samples is slight higher than that of other samples at the same dimension, which is 54318 Ω , indicating an increase with the SiCN thickness. When the line width is shrunk to 0.18 μm , the average resistances for samples of groups A, B, and C are higher than that with the width of 0.22 μm , but have no significant difference among them. However, the line resistance of the group D samples becomes 1021 K Ω , which is about 17 times as that of other samples at the same line width. The results indicate that the line resistance increases with the decrease of line width, and additional barrier SiCN layer caused higher line resistance when its

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thickness is 50 nm or more, but there are no significant different if its thickness is 20 nm or lower.

Fig. 7.24. Comparison of line resistance of four groups of samples for different line widths. a) 0.18 μm ; b) 0.22 μm

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7.7.3.2 Line-to-line leakage current

The leakage current measured at room temperature and 1 V bias is shown in Fig. 7.25 (a). On the graph, the leakage current of the group C and D samples shows a narrow distribution with values around 10^{-12} A, indicating no significant difference for the samples with 20 nm and 50 nm thickness SiCN. However, for sample A and B, the distribution is broader, and some dies have been breakdown. The leakage current values are around 10^{-10} A, which are higher than that of sample C and D. It means that a 10nm SiCN layer is not thick enough to block diffusions. To compare the thermal stability of the four groups of samples, burn-in at 200°C for 40 hours was applied. The comparative data are shown in Fig. 7.25 (b). For the burn-in samples, the leakage current of the group D samples still keeps the narrow better statistical distribution. The current after burn in becomes less (From 10^{-12} to 10^{-13} A). This is likely due to the removal of some defects during burn in. For the group C samples, the majority of the samples have the leakage current unchanged while 13 of the measured 35 dies have the worse leakage current compared to that without burn in. The groups A and B samples show a more border distribution of leakage current after burn in. The values of 2 to 4 orders of magnitude are higher than that without burn in.

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Fig. 7.25. Comparison of line-to-line leakage current of four groups of samples with line width of $0.24\ \mu\text{m}$ and line spacing $0.24\ \mu\text{m}$ measured under different conditions. a) as-fabricated; b) after burn-in at 200°C for 40 hours.

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The breakdown voltages of the four groups of samples were also measured in the same structure as that for line-to-line leakage current. Fig. 7.26 shows the comparative breakdown voltages. For the as-fabricated samples, the breakdown voltages of groups A, B, C and D are 43.2, 47.9, 61.8 and 62.2 V respectively increasing with the SiCN thickness. The group D samples can stand higher electrical field because of its thicker SiCN layer. The breakdown voltage of group C samples is very close to that of group D samples though its SiCN thickness is only 20 nm. However, when the thickness of SiCN is reduced further, its value is close that of sample A. This indicates that the 10 nm SiCN is not enough to improve the breakdown leakage. After burn-in at 200°C for 40 hours, the breakdown voltages of groups A, B, C and D become 15.1, 19.1, 44.2, and 57.5 V. That is, there is little degradation for group D samples and slightly more degeneration for group C samples. However, the breakdown voltages of groups A and B are 15.1, 19.1 V after burn in correspond to about 50% degeneration. These data clearly indicate that group C and D samples have better thermal stability and better electrical performance than that of group A and B samples.

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Fig. 7.26. Comparison of breakdown voltage of four groups of samples with line width

0.24 μm and line spacing 0.24 μm measured under different conditions. a)

As-fabricated; b) After burn-in at 200°C for 40 hours.

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7.8 Summary

The single damascene Cu line using three kinds of Ta and Ta-based barrier (Ta, TaN and Ta/TaN) with and without SiCN and plasma treatment for Cu-ultra low- k interconnect in 0.13 μm technology has been investigated. Comparing the single damascene Cu lines with three kinds of barriers (Ta, TaN and Ta/TaN), the electrical tests indicates that the Cu lines with the TaN and bi-layer Ta/TaN barriers exhibits the smaller leakage current and higher breakdown voltage compared with the Cu lines with Ta barrier. However, the line with Ta barrier has the smallest line resistance while the line with the TaN barrier has the highest.

Applying forming gas N_2/H_2 plasma treated on the ULK surface can reduce the line resistance significantly, especially for the in 0.13 μm or below Cu damascene technology. But it also shows that such treated has critical drawbacks: 1) it can lead to degradation of the ULK; 2) it also causes surface damage and degradation of the thermal stability of all structure.

When an additional dielectric barrier layer SiCN of around 10 nm thick was deposited on the sidewalls prior to the TaN metal barrier deposition by PECVD, it was found that the leakage current decreased by 1 order of magnitude and the breakdown voltage increased 200% compared with the samples without SiCN layer after burn-in at 200°C for 40 hours.

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By comparing with only one Ta barrier layer structure, it was confirmed that introducing an additional SiCN barrier layer combined with Ta barrier can significantly improve the breakdown voltage, line-to-line leakage and thermal stability. However, it also brings higher line resistance. By considering these pros & cons, a 20 nm SiCN layer may be proper for the Cu-ULK porous SiLK interconnects of 0.13 μm technology and beyond.

Table 7.1 Summary of electrical parameters of three kinds of samples in different conditions

		Cu/Ta(N)/ULK			Cu/Ta(N)/SiCN/ULK			Cu/Ta(N)/ULK plasma treatment	
		Ta	TaN	Ta/TaN	Ta	TaN	Ta/TaN	TaN	Ta/TaN
As-fabricated	Line Resistance (0.22 μm) (Ω)	44569	47135	46273	52468	66798	53712	231	196
	Line to line leakage (A)	2.80E-11	1.89E-12	4.20E-12	2.00E-12	1.08E-12	1.50E-12	3.20E-11	2.90E-11
	Breakdown voltage (V)	42.3	45.1	45.2	62.2	69.1	64.2	19.9	15.3
After burn-in at 200 C for 40 hours	Line to line leakage (A)	1.90E-10	5.00E-11	2.90E-10	4.20E-13	4.89E-12	1.70E-13	3.10E-08	1.00E-08
	Breakdown voltage (V)	15.1	22.6	22.1	57.5	66.7	53.2	14.7	12.1
thermal stress at 150 C	Line to line leakage (A)	8.90E-11	3.30E-11	7.00E-12	5.00E-11	5.20E-11	3.00E-12	1.10E-07	4.20E-09
	Breakdown voltage (V)	25.4	41	35.5	35	41.6	48.6	18.6	19.7

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CHAPTER 8

Conclusions and Recommendations for Future Research

8.1 Conclusion

The integration of Cu and ULK porous SiLK using different barriers on blanket and patterned wafers has been investigated. This includes characterizations of ULK porous SiLK, Ta based barriers on ULK, Ta(N)/SiCN/ULK SiLK structures, and Cu/Ta(N)/SiCN/ULK structures on blanket and patterned wafers. The thermal stability, interaction and electrical properties of different structures were comparatively investigated by using various techniques. The single damascene lines were fabricated of Cu and ULK porous SiLK with different barrier layers in 0.13 μm technology. The line resistance, line to line leakage and breakdown voltage were evaluated at various conditions. Furthermore, effects of plasma treatment and additional SiCN layer on the electrical performance and thermal stability of the Cu lines were evaluated. Finally, the thickness of SiCN was also optimized. The important conclusions acquired from these studies can be summarized as follows:

1) The ULK porous SiLK, which is supplied by Dow Chemical Company, with k value around 2.3, was characterized. Samples were annealed at various temperatures in order to study the thermal stability. It was revealed that the porous SiLK could still retain its properties after annealing at 500°C for 30 mins. For the annealing above 500°C, the abrupt change of electrical and mechanical properties was observed. This is because when annealing temperature is higher than the glass transition temperature, the

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repeating unit in ULK possibly breaks down, and the porous SiLK structure might also be destroyed and be turned into small molecules.

2) Three kinds of diffusion barrier layers (Ta, TaN and bi-layer Ta/TaN) deposited on ULK porous SiLK were investigated. It was found that the Ta film shows BCC structure, with lower resistivity, clear grain boundary. And the TaN film shows smaller grain size and blur grain boundary due to the incorporation of N.

3) After being annealed at different temperatures, the barrier/ULK structures were found to lose the integrity at temperatures over 500°C due to the failure of ULK's properties, and significant diffusion was observable near the interfaces of the structures. The Ta/ULK porous SiLK shows the smallest sheet resistance but the poorest thermal stability while the TaN on the ULK porous SiLK shows the highest resistance but the best thermal stability. The bi-layer Ta/TaN barrier takes the advantage of both Ta and TaN barriers and gives reasonable resistance and thermal stability. The better thermal stability of the TaN and the bi-layer Ta/TaN barriers is mainly due to the amorphous/nano structure and less grain boundaries of the barriers.

4) After being annealed at 400°C for different times, it was found that the sheet resistance of the Ta barrier increased significantly after being annealed for 60 mins while that of TaN increased for 120 mins due to Ta₂O₅ compound formation as revealed by X-ray diffraction and secondary ion mass spectrometry. The better integrity of the TaN compared to Ta is due to N incorporation, which degrades the diffusion of Ta and O. The diffusion coefficient of Ta in the porous SiLK is $0.023 \pm 0.001 \text{ nm}^2/\text{s}$, while the diffusion coefficient of TaN is only $0.0033 \pm 0.0001 \text{ nm}^2/\text{s}$.

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5) The effect of the three kinds of barrier layers ULK porous SiLK on the properties of the self-ionized plasma (SIP) Cu films have also been studied using various techniques. Cu (111), Cu (200) and Cu (220) textures were observed for all samples. After being annealed, it was found there are two reasons to degrade the thermal stability of Cu/Ta/ULK structure. One is that the barrier Ta has the polycrystalline structure with finer grains (7-10 nm), which can easily enter the porous SiLK with pore size around 10 nm. It also provided many grain boundaries as the fast diffusion paths for C, H, and O atoms in the ULK out-diffusion. The other factor is that Ta has higher affinity to oxygen and formed one stable oxide, Ta_2O_5 , which causes increase in sheet resistance. The results of the SIMS revealed that the significant increase of the sheet resistance is due to the diffusion of Ta and O to the Cu film. It was also revealed that the annealing at 400°C for more than 120 min also caused diffusion of Ta and O and even Cu into the ULK porous SiLK, and the Ta and O diffused faster in the dielectric than in the Cu film. In addition, the out-diffusions of the C and H in the dielectric towards Ta and Cu layers were also observed and the H diffusion was found to diffuse faster than C.

6) For TaN barrier, Ta and N may diffuse separately, and at the same time, TaN may also diffuse in the form of molecules. Compared with Ta/ULK, the TaN/ULK interface is smooth and better defined due to its lower surface diffusion on ULK. For the Cu/Ta/TaN/ULK sample, smaller diffusion region appeared at the TaN/ULK interface. At the same time, Ta diffused into Cu layer is also presented.

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7) The diffusion coefficients of Cu in different Barrier/ULK are $0.035 \text{ nm}^2/\text{s}$, $0.04 \text{ nm}^2/\text{s}$ and $0.03 \text{ nm}^2/\text{s}$ corresponding to Cu/Ta/ULK, Cu/TaN/ULK, and Cu/Ta/TaN/ULK respectively. And the diffusion coefficients of Ta in ULK are $0.05 \text{ nm}^2/\text{s}$ and $0.051 \text{ nm}^2/\text{s}$ for Cu/Ta/ULK and Cu/TaN/ULK, respectively. Obviously, the diffusion constant of Ta with Cu capped layer is larger than that without Cu layer because the inter-diffusion and amorphization between Cu and Ta. In addition, the residual stress in Cu and Ta can accelerate the Ta diffusion into ULK.

8) The effect of SiCN on the thermal stability of the Cu/barrier/ULK structures was investigated. Comparing with the barrier Ta and Ta based in the Cu/barrier/ULK structure, the barrier SiCN showed many advantages: lower density (3.25 g/cm^3), higher hardness (460 GPa), amorphous structure without grain boundary defects, better thermal stability and no reaction with Cu, ULK and oxygen after being annealed at 400°C for 150 mins. So it can be thought as a good barrier candidate for Cu and ULK integration.

9) Introducing an additional SiCN barrier layer to the Ta barrier can significantly improve the thermal stability because the amorphous structure of the SiCN not only effectively blocks ULK out-diffusion, but also prevents the Cu, Ta from diffusing into ULK. The thin SiCN film deposited on the ULK surface can also significantly improve the surface mechanical property and thermal stability. Similar results can also be observed for the sample with TaN barrier. When SiCN additional layer was added to TaN barrier, the barrier shows much better performance. TEM pictures show fairly smooth interfaces up to 400°C . AFM measurement shows only a small increase in roughness of Cu film surface due to the Cu grain growth. No new phases are detected by XRD investigation at 400°C up to 150 minutes of annealing time.

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10) Plasma treatment seems to cause higher sheet resistance for the as-deposited sample because of more grain defect. However, it also improves the barrier integrity in terms of sheet resistance during annealing and results in lower sheet resistance. It also helps to improve the smoothness of Cu film as can be seen by AFM results due to the surface modification. But it also shows that such treatment has critical drawbacks: 1) it can lead to degradation of the ULK; 2) it also causes surface damage and degraded the thermal stability.

11) The single damascene Cu lines using three kinds of Ta-based barriers with and without SiCN and plasma treatment for Cu-ULK interconnect in 0.13 μm technology have been investigated. The electrical tests indicate that the Cu lines with the TaN and bi-layer Ta/TaN barriers exhibit the smaller leakage current and higher breakdown voltage compared with the Cu lines with Ta barrier. However, the line with Ta barrier has the smallest line resistance while the line with the TaN barrier has the highest.

12) It was found that the N_2/H_2 plasma treatment on the ULK surface before depositing barrier and Cu could reduce the line resistance significantly, but it also brought more surface defects on the sidewall and larger diffusion length. The larger line to line leakage current and lower breakdown voltage were observed after applying thermal stress. It indicates the plasma treatment degrades the thermal stability comparing with the untreated samples.

13) Compared with only the Ta and Ta-based barrier layer structure, introduction of an additional SiCN layer could significantly improve the breakdown voltage, line to

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line leakage and thermal stability. However, as the breakdown voltage and thermal stability increased with increasing SiCN thickness, it also brought higher line resistance. Four groups of samples with different thicknesses of SiCN layer were comparatively studied. The SiCN layer between 20 nm and 50 nm can give better electrical performance and thermal stability.

8.2 Recommendations for Future research

The integration of Cu and ULK porous SiLK is developed in this work for 0.13 μm technology, and the single damascene structure is studied. For the technologies of 90 nm or below, following topics should be studied in the future:

1) Dual Damascene structure will be fabricated for Cu and ULK

To achieve multi-level Cu interconnects, the dual damascene structure is necessary to be fabricated using Cu and ULK, and it includes via fabrication, deposition in higher A/R ratio trench or via, free void gap-filled. Some new processes need to be developed, these include etching, cleaning, CMP, etc.

2) Electro-migration test

Compared to Al, Cu shows higher EM resistivity, but it can easily diffuse into low k or ultra low k dielectrics. After introducing the ULK porous SiLK into the Cu interconnects, the EM test should be performed to evaluate the Cu/ULK reliability with

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different barrier layers, especially, with additional SiCN barrier layer. It is necessary to know how it affects the EM results.

3) Development of new process for integration

In this work, copper metallization for patterned wafer is carried out for 0.13 μm technology. For the 90 nm or below integrated circuits, new processes Cu/ULK porous SiLK integration need to be developed. And the thermal stability and reliability of the new structures for the new generation of ICs need to be systematically studied.

Author's Publication

Journal Papers:

1. **L.Y Yang**, D.H Zhang, C.Y Li, S.Y Wu, P.W Lu and P.D Foo, "Improving electrical performance of Cu/porous ultra low k dielectrics single damascene lines". **IEE Electronic Letter**, Vol.40, No.12, 2004, P729-730
2. **L.Y. Yang**, D.H. Zhang, C.Y Li, and P.D Foo, "Comparative study of Ta, TaN and Ta/TaN bilayer barriers for Cu-ultra low k porous polymer integration", **Thin Solid Film 462-463 (2004) P176-181**.
3. **L.Y. Yang**, D.H. Zhang, C.Y. Li, R. Liu , A.T.S. Wee, P.D. Foo, "Comparative study of Ta and Ta(N) in the barrier/ultra low k polymer structures for deep submicron integrated circuits" **International Journal of Nanoscience, Vol. 3, Nos. 4-5 (2004) 471-479**
4. **L.Y. Yang**, D.H. Zhang, C.Y. Li, R. Liu, A.T.S. Wee, P.D. Foo, "Characterization of Cu/Ta/ultra low k porous polymer structures for multilevel Interconnects" **Thin Solid Film 462-462 (2004) P182-185**.
5. **L. Y. Yang**, D.H. Zhang, C. Y. Li, K. Prasad and P.D. Foo, "Comparative study of TaN and SiC barriers in the Cu/barrier/Ultra low k structures", **Microelectronics Engineering, (To be published)**
6. D.H. Zhang, **L.Y. Yang**, C.Y. Li, R. Liu, A.T.S. Wee and P.D. Foo, "Thermal stability of Cu/Ta/ultra low k porous polymer structures for multilevel Interconnects" **International Journal of Nanoscience, Vol. 3, Nos. 4-5 (2004) 481-487**

7. **L.Y. Yang**, D.H. Zhang, C.Y. Li, Lu Peiwei and P.D. Foo, “SiCN and Ta/TaN barriers for Cu/ULK integration in 0.13 μ m Technology”, **Proceeding of The Society Photo-optical Instrument Engineering (SPIE) 2004.**

Conference:

1. **L.Y. Yang**, D.H. Zhang, P.D. Foo, C.Y. Li, Wu Shaoyu, “Study on the thermal stability of porous SiLKTM”, November 19-20, 2002 VMIC conference, Singapore
2. **L.Y. Yang**, D.H. Zhang, C.Y. Li, Lu Peiwei and P.D. Foo, “SiCN and Ta/TaN barriers for Cu/ULK integration in 0.13 μ m Technology”, The 5th International Conference on Thin Film Physics and Application (TFPA2004) May 31-June 2, 2004 Shanghai, China.
3. **L. Y. Yang**, D.H. Zhang, C. Y. Li, K. Prasad and P.D. Foo, “Comparative study of TaN and SiC barriers in the Cu/barrier/Ultra low k structures”, The 2nd International Conference on Technological Advances of Thin Films & Surface Coatings and The 1st International Conference on Nanotechnology, 13-17 July, 2004, Singapore.

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