High speed microwave transmission system for a low earth orbit micro-satellite platform

Yeap, Yean Wei

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**HIGH SPEED MICROWAVE TRANSMISSION
SYSTEM FOR A LOW EARTH ORBIT MICRO-
SATELLITE PLATFORM**

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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

2007

HIGH SPEED MICROWAVE TRANSMISSION SYSTEM
FOR A LEO MICRO-SATELLITE PLATFORM

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2007

High Speed Microwave Transmission System For A Low Earth Orbit Micro-Satellite Platform

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
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Yeap Yean Wei

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Summary

Before determining the architecture of a transmitter, considerations such as power consumption, cost, complexity, targeted performance and applications of the transmitter must be carefully studied. In this thesis, the direct up-conversion and the double up-conversion transmitter architectures are briefly discussed and an **X-band direct up-conversion module** was developed. The practical design considerations of a high power amplifier such as the DC bias network, devices' and PCBs' heat dissipation and groundings, etc., are highlighted. Taking into account all the practical design considerations, the **X-band high power and high gain cascade power amplifier modules** were designed and it has been shown that the modules consume 10W DC power less than the subsystem specifications, without compromising the RF performance. The power amplifier modules designed has a gain of 33dB, Power Added Efficiency (PAE) of 16%, Error Vector Magnitude (EVM) of less than 4% and Phase Error (PE) of less than 1.5° at an output power of 38dBm. Instead of using a conventional coupler, which has high insertion loss and large physical dimensions, a **novel and simple X-band power divider** was designed to detect the forward output power from an amplifier. By using this power divider, the RF circuits of the cascade power amplifier engineering modules occupied only 85% of the dimension provisioned. Without significant redesign effort, a few methods on how to overcome the cavity resonance of the high power cascade amplifier are also reported.

Besides, a **novel technique on how to design an S-band high power amplifier based on a small signal S-parameter analysis** and a passive load pull are demonstrated. This technique is ideally suitable for designer who wants to design power amplifier when a full load pull system is unavailable. Based on this technique, a

power amplifier was successfully designed with a gain of 12dB, PAE of better than 40%, EVM of less than 5%, PE of less than 1.5% at an output power of 34dBm.

Finally, **a novel approach on how to design a linear power amplifier** without the sophisticated PA linearization is presented. The proposed technique shows how the linearity of a medium power amplifier can be improved. The amplifier designed has a gain of 12dB, PAE of better than 30%, EVM of less than 1.5%, PE of less than 0.8% at an output power of 27dBm.

The novel approaches/techniques demonstrated has accelerated the development of the RF modules in the Satellite Engineering Centre of NTU.

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Abbreviations

ADAM	Advanced Data Acquisition & Messaging
ADCS	Attitude Determination & Control System
ADS	Advance Design Systems
aka	also known as
Amp	Amplifier
BPF	Band Pass Filter
BPSK	Binary Phase Shift Keying
C	Capacitance/Capacitor
CAN	Control Area Network
CCSDS	Consultative Committee for Space Data Systems
COTS	Commercially Off-The-Shelf
CREST	Centre for REsearch in Satellite Technologies
CRISP	Centre for Remote Imaging, Sensing and Processing
CW	Continuous wave
dBc	dB relative to the carrier power
dBm	Decibels relative to 1 mW ($10\log(\text{power}/1\text{mW})$)
DRO	Dielectric Resonator Oscillator
DUT	Device Under Test
ECSS	European Cooperation for Space Standardization
EIRP	Effective Isotropic Radiated Power
EM	Engineering Model
ESA	European Space Agency
ESR	Equivalent Series Resistance
EVM	Error Vector Magnitude
FEC	Forward Error Correction
FET	Field Effect Transistors
GaAs	Gallium-Arsenide
GPS	Global Positioning System
HPA	High Power Amplifier
IF	Intermediate Frequency
IRIS	10m Resolution Multi-spectral Visible Band Optical Instrument
ISRO	Indian Space Research Organization
LAN	Local area network

LEO	Low Earth Orbit
LPF	Low Pass Filter
LO	Local Oscillator
LVDS	Low Voltage Differential Signal
MAN	Metropolitan Area Network
Mbps	Mega bits per second
Msp/s	Mega symbols per second
MMIC	Monolithic Microwave Integrated Circuit
NASA	National Aeronautics and Space Administration
NTU	Nanyang Technological University of Singapore
OBC	On-Board Computer
P1dB	Power at 1dB compression point
PA	Power Amplifier
PE	Phase Error
PAE	Power Added Efficiency
PAN	Personal area network
PLL	Phase Lock Loop
PPU	Parallel Processing Unit
PSLV	Polar Satellite Launch Vehicle
PSU	Power Supply Unit
QPSK	Quadrature Phase Shift Keying
R	Resistance/Resistor
RAMDISK	Solid State Memory Unit
RCE	Relative Constellation Error
RMS	Root Mean Square
SEL	Single Event Latchup
SMD	Surface Mount Device
SNR	Signal to Noise Ratio
SSPA	Solid State Power Amplifier
SWR	Standing Wave Resonance
TTC/TT&C	Telemetry, Tracking & TeleCommand
VNA	Vector Network Analyzer
VSA	Vector Signal Analyzer
VSG	Vector Signal Generator
XBT	X-Band Transmitter

1. Introduction

The X-Sat is a Low Earth Orbit (LEO) micro-satellite earth surface observation and imaging mission, currently being developed in the Centre for Research in Satellite Technologies (CREST), Singapore. It has a nominal mass of 100kg and is designed to have a lifespan of three years. It will be launched into a 685 km high sun synchronous orbit using the Polar Satellite Launch Vehicle (PSLV) of Indian Space Research Organization (ISRO) in early 2008 [1].

1.1. Motivation

Microwave communication is the only way of communication between the X-Sat micro-satellite and the ground station once the micro-satellite is successfully placed into the orbit. In the X-Sat, the Telemetry, Tracking & teleCommand (TT&C) System is the primary communication system used to receive commands from ground controller and send telemetries back to the controller. In addition to the TT&C system, the micro-satellite will be carrying a high speed X-band transmission system (XBT), which will be used for near-real time data downlink at a data rate of up to 50Mbps, to the ground station. Although there are many commercial off-the-shelf (COTS) components that can be used to develop a microwave transponder or transmitter, besides the requirements of meeting the link budget specifications, stringent launch vehicle and space environment specifications, there are challenges remained in the RF module design to completely fulfill the bandwidth, power, efficiency, linearity and cost of the development. As the micro-satellite is located at a distance of 685km away from the earth surface, the transmitted signal suffers extremely high propagation loss when it reaches the ground station. Consequently these transmitters must employ progressively larger power amplifiers (PA) to boost a

low power signal to the large output power prior to transmission. The PA not only consumes a major fraction of power used by the satellite, it also generates unwanted noise and non-linear distortion with increasing output power [3] [4]. Since linear amplification is required when the signal contains both amplitude and phase modulation [2], the PA and all the driver stages must “backoff” its output power. This consequently leads to very low power efficiency of the PA. Besides the PA, some of the building blocks in a transmitter such as modulators, oscillators, mixers, and low-level amplifiers also introduced the non-linear characteristics. The accumulated non-linear distortion will drastically degrade the overall transmitter performance if the non-linearity is not minimized. Therefore, each RF block, especially the high power amplifier (HPA) that exhibits strong non-linear behaviors, must preserve its linearity to an acceptable output level without scarifying much on the power efficiency. Thus the non-linear impairments to the digitally modulated signal can be reduced. As a result, the need for high efficiency and linearity are the main drivers in the design of a RF power amplifier.

1.2. Objectives

The main objectives of this project are to design and develop high performance RF modulator and PAs, which will become parts of the RF modules in the TT&C transmitter and XBT of the X-Sat. Three different PAs, which have different output power level, matching network and operating frequency, have been designed to investigate their individual performance and characteristics. The work includes:

- ❖ Design of a direct QPSK modulator module operating at 8.3GHz. It involves PCB layout design, integration and development of the module. It also involves test setup of vector signal generator (VSG) and vector signal analyzer (VSA) for

the phase noise measurement of the local oscillator (LO), power measurement and relative constellation error (RCE) analysis.

- ❖ Design of an X-band HPA module with a minimum gain and output power of 33dB and 38dBm respectively [5]. Two single-stage internally matched amplifiers, an isolator and a power divider will be evaluated separately before cascading and integrating them into a module. The practical design considerations such as proper bias network design, sufficient groundings and heat sinking of devices and PCB will be taken into account. The non-linear impairments and effects of operating the HPA near to its output 1-dB compression point will be studied based on the RCE analysis.
- ❖ Design of a single stage S-band HPA with a minimum gain and output power of 11dB and 34.5dBm respectively [6]. The input and output matching networks of the HPA will be initially matched for power gain based on the small signal S-parameter provided by the manufacturer. A passive load pull measurement will be setup by using a sliding screw tuner, a VSG and a power meter. When biasing the HPA at a condition recommended by the manufacturer, the load impedance of the HPA device will be measured using a vector network analyzer (VNA). To achieve optimum output power, the output matching networks will be redesigned to match the measured load impedance.
- ❖ Design of a single stage linear S-band medium PA with a minimum gain and output power of 12dB and 25dBm respectively [6]. Similar passive load pull technique discussed above will be applied to accomplish the design. Next the biasing condition of the medium PA will be readjusted for optimum linearity and efficiency.

1.3. Major Contributions of the Thesis

There are four main contributions from this work:

- ❖ In the XBT, the directional coupler, isolator and switch are usually placed after the HPA. The losses due to these components will decrease the efficiency of the HPA. Since these devices are unavoidable, the only solution is to minimize the insertion loss. A novel low loss power divider is designed to replace the directional coupler. This power divider is also physically smaller than a directional coupler. It has been shown, by using this power divider, the RF circuits of the solid state power amplifier (SSPA) module occupied only 85% of the dimension provisioned.
- ❖ Cavity resonance may occur when the RF circuits are placed in an enclosure. The absorber can be used to overcome this problem but a series of qualification tests are needed to examine its suitability for space application. This may incur additional cost and module development time. Without a complete redesign or rework effort, the detachable metal blocks has been proven to be effective in overcoming the cavity resonance.
- ❖ For the HPA device that requires impedance matching, a design approach that is based on the passive load pull technique is presented. This approach highlights how the small signal S-parameter can be used to locate and to match the load impedance. If the complete load pull system is unavailable for PA characterization, this approach becomes a very useful design reference. This is especially effective when the device is cascaded with other microwave circuits. Characterization of the HPA device is impossible using this method, however,

this approach demonstrates the flexibility of using just a VNA and a slide screw tuner to design the matching networks of a HPA.

- ❖ To shorten the development time and to avoid having additional circuitries required for linearizing a PA, a novel approach of designing a linear amplifier is presented. This approach highlights how a PA can be further optimized for linearity, after performing passive load pull, to yield the highest efficiency and linear output power by varying the bias condition.

1.4. Organization of the Thesis

The thesis is organized as follows:

Chapter 1 begins with an introduction to the motivation behind this work. This is followed by an outline of objectives and major contributions of this thesis. Lastly, the organization of the thesis is included to give an overview of this thesis.

Chapter 2 commences with a brief overview of the various subsystems in the X-Sat, with more in depth discussion on the antenna systems and RF modules of the XBT and the TT&C transceiver. A few factors that might be affecting the performance of microwave transmission system and the downlink budget analyses are also included. This is followed by a discussion on the proposed configurations for this research work, which includes the direct QPSK modulator module and the HPA amplification chain proposed for the XBT and TT&C transmitter.

Chapter 3 starts with an introduction on the formation of QPSK signal in theory, followed by the development of the X-band direct up-conversion modulator and finally the experimental results.

In Chapter 4, the design and development of the X-band PAs are reported. The Chapter begins with a review of the PA characteristics and design considerations before the design of single stage PAs, power divider, detector circuit, cascade amplifier and final SSPA Engineering Model are presented. The methods of overcoming cavity resonance and simulation of electromagnetic field distributions in the SSPA Engineering module are discussed before presenting the experimental results of each circuit designed.

Chapter 5 and Chapter 6 cover the design of S-band PA based on small signal S-parameters analysis. Chapter 5 starts with a review of the complex conjugate impedance matching and subsequently a detail description of the proposed technique, which include the design procedures and the experimental results. In Chapter 6, the design concept of how to design a linear medium PA is presented before detailing the design procedures and experimental results.

Chapter 7 presents the conclusion and the recommendations for future research work.

2. Background and Literature Review

The X-Sat mission led by the CREST of NTU is a collaborative flagship project between NTU and the DSO National Laboratories. The X-Sat is designed with three mission objectives. The primary mission objective of the X-Sat mission is the earth observation and environmental monitoring in the South East Asian region, realized using a 10m resolution multi-spectral visible band optical instrument known as IRIS payload. The secondary payload is the Advanced Data Acquisition and Messaging (ADAM), a mobile communication system which provides two way low-rate data communications with remote low power terminals, ideally suitable for a variety of land, maritime and aeronautical mobile applications. The third payload is the Parallel Processing Unit (PPU), designed and developed to demonstrate on-board data processing, such as image data classification and compression in a small satellite. The IRIS payload will perform earth imaging and observation during two daytime-passes over Singapore, which data will be transmitted within the same orbit. ADAM and PPU will operate in the orbits that are not used by the primary payload [7].

2.1 Brief Overview of the X-Sat Subsystems

The subsystems in X-Sat micro-satellite are ADAM, Attitude Determination & Control System (ADCS), IRIS imaging system, Global Positioning System (GPS), On-Board Computer (OBC), PPU, Power Supply Unit (PSU), Telemetry, Tracking & TeleCommand (TT&C) and X-Band Transmitter (XBT). As shown in Fig. 1, these subsystems are connected to each other and interfaced via On-Board Data Handling (OBDH) systems that consist of OBC, solid state memory unit – RAMDisk and the Control Area Network (CAN) bus. Some critical subsystems such as the PSU, XBT, and CAN buses are designed with full redundant units. The secondary units will be used when the primary units fail to operate. The OBC is the

core subsystem supporting all the data transfer. The GPS, PSU and TT&C are provided with dedicated serial data links to the OBC. There are also dedicated high speed data links connecting the XBT, IRIS and PPU to the OBC.

Fig. 1: X-Sat Subsystems, bus systems and data links.

The TT&C subsystem provides the primary means of communication between the micro-satellite and the ground station. The OBC controls and directs the designated subsystems to operate when telecommands are received by the TT&C subsystem. The OBC also monitors the health of the micro-satellite, tracks the satellite position and transfers telemetries back to the TT&C system. Under some circumstances, the TT&C may direct the PSU to cut off power supply to certain subsystems without intervention from the OBC when a telecommand is received from the ground station to do so. Currently the TT&C ground station for the X-Sat mission control and operation is situated at the TechnoPlaza of NTU.

The OBC will gather imaging data taken by the high resolution multi-spectral camera, or images stored on the RAMDisk (images processed by the PPU in the previous orbits) for transmission to the ground station via the XBT. The images will be received by a 13m reception dish antenna located at the Centre for Remote Imaging, Sensing and Processing (CRISP), Singapore, for data processing and archiving.

2.2 The X-Sat Communication Systems

The X-Sat communication systems comprise of the dual redundant S-band TT&C transceivers and X-band transmitters subsystems. The TT&C subsystem provides full duplex communications between the ground station and micro-satellite during all mission phases, including contingency operations [6]. Hence the antenna pattern of the TT&C subsystem must be near omni-directional and the processing electronics must support high flight dynamics to ensure highly reliable communication between the micro-satellite and the ground station. For the XBT, it operates only during image data downlink. It supports downlink data rate of up to 50 Mbps for near instantaneous data downlink during the same orbit pass while imaging operation is being carried out or downlink of images stored in the RAMDisk.

Before detailing the specifications and architectures of the TT&C and the XBT communication subsystems, an overview of two typical architectures of the microwave transmission system will be discussed next.

2.2.1 Architectures of Typical Microwave Transmission System

The architecture of a transmitter is usually designed based on the system and performance requirements such as the output power, modulation and coding schemes. Generally the building blocks in a transmitter include oscillators, mixers, filters, matching networks, combiners, and isolator, antenna, driver and power amplifiers, etc. In this thesis, two most relevant architectures, the direct up-conversion and double up-conversion will be discussed. Other transmitter architectures such as stage bypassing, Kahn, envelope tracking, outphasing, and Doherty can be found in the reference [2].

2.2.1.1 Direct Up-conversion Architecture

Fig. 2 shows the block diagram of a typical direct up-conversion transmitter. The data can be phase, amplitude or frequency modulated directly on a carrier frequency. Low phase noise local oscillator (LO) should be used so that the RCE (see section 2.3.1) in the modulated signal can be kept to minimum. The spurious and harmonics generated are normally filtered by a BPF prior to power amplification. A LPF is placed after HPA to filter out harmonics generated, if any. The direct up-conversion process generates modulated signals close to the LO frequency. At the output of the transmitter, the modulated signal that has been amplified to very large amplitude may potentially leak into the LO (PLL frequency synthesizer) if the LO is not properly shielded or isolated. In this case, both the leakage signal and the Voltage Controlled Oscillator (VCO) signal will appear simultaneously at the input of the PLL phase detector. Consequently the phase comparator will not be able to stabilize the phase difference and the PLL will be knocked out of lock. There is also a potential that the leakage signal is re-modulated, impairing the quality of the digital signal.

Fig. 2: Typical direct up-conversion transmitter.

2.2.1.2 Double Up-conversion Architecture

Unlike direct up-conversion, the double up-conversion transmitter requires two LO sources as shown in Fig. 3. The baseband modulation is similar to the direct up-conversion architecture but the modulated signal is subsequently up-converted to a higher frequency. Obviously this architecture will be more expensive and consume

more power since two LO sources are required. This architecture is more complex but stable in term of performance. The main advantage is that high power interference from the HPA output to the PLL frequency synthesizer is less because the centre frequencies are different. However, the second stage mixer may introduce additional non-linear distortion to the modulated signal.

Fig. 3: Typical double up-conversion transmitter.

One of the design challenges of this architecture is to determine the right IF and LO frequencies. When a mixer is used to convert signals from one frequency to another, in addition to the desired output frequency signal, it also produces inter-modulated, sum and difference signals due to the nonlinear mixing of the input signals (IF and LO) frequency and the output signal (RF) frequency [8]. Hence, it is important to ensure the unwanted mixing components are located far from the desired frequency and can be easily filtered out with a BPF. Conventionally the mixing components can be identified by using graphical manner by referring to the up-converter spurious products chart described in [9]. Today, the designer can use design software such as Agilent Advance Design System (ADS) or Applied Wave Research Microwave Office, to predict the mixing products of a mixer by using behavioural model available in the software. An example of using ADS to predict the mixing components is shown in section 2.2.2.2.2.

2.2.1.3 Determining the Architecture of a Transmitter

At L-band or S-band, direct up-conversion architecture is preferred since high quality modulators at these frequency bands are cheap and commonly available in

the market. On the contrary, at Ka or Ku-band, double or multiple up-conversions is preferred due to unavailability of commercial I/Q modulator package. Sometimes, implementing direct up-conversion architecture at very high frequency is even more expensive than the double up-conversion. Therefore when deciding the architecture of a transmitter, besides the considerations highlighted in Table 1, other considerations such as operating frequency, the availability and reliability of commercial package, cost and time of development has to be taken into account.

	Direct Up-conversion	Double Up-conversion
Number of LO	1	2
Power Consumption	Lower	Higher
Cost	Lower	Higher
Complexity	Simple	Complex
Performance	- Leakage signal along the transmitter path may lead to system failure. - Require isolators along the path and shielding of LO.	- More stable as two different frequencies are used.
Application	- For transmitter with low transmit power.	- For transmitter with very high transmit power. - Require high system performance and reliability.

Table 1: Comparison of the direct and double up-conversion architectures.

When planning the RF power budget of a transmitter, the input level to the devices that exhibit non-linear characteristic (i.e. amplifier and mixer) should not force these devices to operate at the saturating condition. Saturating these devices may result in increasing RCE of the modulated signal as shown in [10]. The RCE can be minimized by “back-offing” the output power of these devices [11] but this will reduce the efficiency of the device, especially the HPA. Therefore, there is a trade-off between the linearity and output power of a HPA (will be presented in the following chapters).

2.2.2 The X-band Transmitter (XBT) Subsystem

This section details the specifications and the architecture of the XBT subsystem.

2.2.2.1 XBT Subsystem Specifications

❖ *Centre Frequency*

According to the ITU Radio Regulations, the frequency allocated for space-to-earth remote sensing applications and earth exploration is 8215MHz-8400MHz [12]. The centre frequency of the defined band is $(8215+8400)/2=8307.5\text{MHz}$. However a non-standard frequency source that provides fractional value will increase the cost of the subsystem (i.e. the local oscillator). Therefore the centre frequency of XBT is fixed at 8.3GHz [5].

❖ *Operating Centre Frequency Range*

The primary mission operation necessitates a maximum data rate of 50Mbps that is desired for transmitting the image data in the same orbit. For such a high rate system, the RF channel bandwidth required is at least 25MHz with QPSK modulation. The centre frequency of the transmitter is fixed at 8.3GHz under normal operation. For contingency operation, additional two non-overlapping channels are provisioned, centred at 8.275GHz and 8.325GHz respectively. Therefore the operating centre frequency ranges from 8.275GHz to 8.325GHz [5].

❖ *Modulation and Coding Scheme*

QPSK modulation has been chosen to have compatibility with the existing X-band reception system at the CRISP, where the X-Sat payload data shall be gathered. There is no coding scheme applied at this transmitter.

❖ *Bandwidth*

With three non-overlapping channels ($8.275\text{GHz} \pm 12.5\text{MHz}$, $8.3\text{GHz} \pm 12.5\text{MHz}$ and $8.325\text{GHz} \pm 12.5\text{MHz}$), the overall RF bandwidth required is 75MHz [5].

❖ *Transmit Power and Link Margin*

Typical output power at the last stage power amplifier is 38dBm. The nominal link margin shall be 3dB above the required E_b/N_o of 9.6dB (BER of 10^{-5}) [5].

❖ *Downlink Data Rate*

Downlink data rates are selectable at 12.5, 25 and 50Mbps. Low data rate is useful to support low rate downlink along the orbital pass if the conical beam antenna is used while high data rate is desirable for near real time downlink using switched beam antenna [5].

2.2.2.2 Architecture of the XBT Subsystem

The XBT downlink subsystem comprises of dual redundant RF modules connecting to the switched beam antenna and conical antenna respectively, as shown in Fig. 4. The primary and secondary data sources for the XBT are the IRIS camera and RAMDisk. For near real time downlink, the camera would stream the images using low voltage differential signal (LVDS) to the XBT. Otherwise, the OBC will stream the images stored in the RAMDisk.

Fig. 4: Block diagram of the XBT subsystem interfaces.

2.2.2.2.1 X-band Antenna Systems

To support high rate and near real-time downlink to the ground station in the same orbit, high EIRP is needed. Higher EIRP can be achieved by re-orientate the whole

micro-satellite to point towards the ground station. However this would take up valuable imaging time. For the X-Sat, the unique solution was to put eight patch antennas on an inclined platform (at an angle of $\sim 45^\circ$). Once the satellite is ready for image download, the attitude determination software would compute which of the eight antennas is able to provide optimal link margin to the ground station. The transmitter output power would be switched to the selected antenna. This antenna system is known as “Switched Beam Antenna” [5]. It consists of eight antenna elements, each element is a 2×2 array circular polarized patches with a boresight of $\pm 30^\circ$. The estimated antenna gain pattern is shown in Fig. 5. These antenna elements are placed on an octagonal shaped structure, as shown in Fig. 6.

Fig. 5: Antenna pattern of X-band conical beam antenna.

Fig. 6: Structure of the X-band antenna system.

Since the 8-sided antenna is rather big, it would not be feasible to duplicate this antenna for redundancy. Instead a conical beam antenna is provided in the middle of the inclined platform [5]. It is used as a fall back options to support comparatively lower data rates. The conical beam antenna consists of sequentially rotating (phase) patch elements arranged in a circle. It has a wide illumination angle with a null near the boresight region [13], providing an omni coverage. The estimated gain pattern is shown in Fig. 7. This type of antenna can be used to compensate the free space propagation loss for satellite which is moving from horizon-to-horizon [13]. The conical beam antenna has a lower antenna gain than switched beam antenna, with a peak gain of approximately 5dBi.

Fig. 7: Antenna pattern of X-band conical beam antenna.

2.2.2.2.2 X-band RF Modules

As shown in Fig. 8, the RF modules of the XBT comprise the QPSK Modulator Module, Up-Converter Module, and Solid State Power Amplifier (SSPA) Module. As the output power from the HPA is about 10W, the double up-conversion architecture is preferred for the XBT. The I/Q data received from the IRIS camera or RAMDisk is first modulated at 2.2GHz. The local oscillator is a phase lock loop (PLL) frequency synthesizer. The modulated signal is up-converted to 8.3GHz using

a double balanced mixer and a phase-locked Dielectric Resonator Oscillator (DRO) at 6.1GHz, followed by high power amplification. Digital attenuator is added to control the transmit power level. The DRO is chosen as it has very high frequency stability and extremely low phase noise.

Fig. 8: Block diagram of RF modules in the XBT.

Determining the suitable IF and LO frequencies is vital so that the inter-modulated components generated by the mixer can be easily filtered out using a BPF. The IF frequency is determined at sub 2GHz band because there are a lot of commercial components available at this frequency band. To up-convert the IF to RF at 8.3GHz, any combination of IF + LO frequency can be selected as long as the spurious can be filtered out. To illustrate this scenario, two combinations of IF and LO frequencies are examined, IF + LO of 2.1GHz + 6.2GHz (known as “Mix1”) and 2.2GHz and 6.1GHz (known as “Mix2”). It is assumed that the mixer has a conversion loss of 6dB and is perfectly matched to 50Ω. The schematic diagram shown in Fig. 9 is simulated with Harmonic Balance simulator in ADS. Fig. 10 shows that both combinations of IF + LO frequencies produce desired RF at 8.3GHz. However the spurious of “Mix2” are just 100MHz away from RF. If “Mix2” is selected, a high order BPF will be required to filter out the spurious. Consequently, the specification of the BPF will be more stringent, resulting in higher cost of development and insertion loss. To avoid this, “Mix1” is a more appropriate choice of IF and LO.

Fig. 9: Schematic diagram of an ideal up-converter.

Fig. 10: Output spectrum at "VRF" of Fig. 9.

2.2.3 The Telemetry, Tracking & teleCommand (TT&C) Subsystem

This section highlights the specifications and the architecture of the TT&C subsystem, focusing mainly on the transmitter of the TT&C.

2.2.3.1 TT&C Subsystem Specifications

❖ Centre Frequency

According to the ITU Radio Regulations [12], the earth-to space and space-to-earth radio frequency bands allocated for radio communication services are

2.025-2.12GHz and 2.2-2.3GHz respectively. For the TT&C of the X-Sat, the receive and transmit centre frequencies are specified at 2.036GHz and 2.211GHz respectively [6].

❖ *Operating Centre Frequency Range*

Although the implementation uses a PLL frequency synthesizer as the LO, the centre frequency of the transmitter and receiver is fixed during the operation. In the case of emergency, the operating frequency might be changed, if necessary [6].

❖ *Modulation and Coding Scheme*

Based on the Consultative Committee for Space Data Systems (CCSDS)'s recommendation, at the transmitter, the telemetry downlink uses a direct Binary Phase Shift Keying (BPSK) modulation. Forward Error Correction (FEC) codes such as Convolution (CC) and Reed Solomon (RS) are applied in the downlink. At the receiver, the telecommand received is coded with Bose, Ray-Chaudhuri, Hocquenghem (BCH) code and is phase modulated on a 16kHz BPSK sub-carrier [6].

❖ *Bandwidth*

According to the TT&C subsystem specifications [6], the transmitter and receiver RF bandwidth is specified at 5MHz, which is the nominal bandwidth of a patch antenna. The TT&C subsystem does not deliver as high data rate as the XBT. It is only required to support maximum downlink rate of 1Mbps. Hence, the bandwidth of 5MHz is sufficient to support transmission of 1Mbps BPSK modulated signal.

❖ *Transmit Power and Link Margin*

Typical output power at the last stage power amplifier is 34.5dBm. The nominal link margin shall be 3dB above the required E_b/N_o of 9.6dB (BER of 10^{-5}) [56].

❖ *Uplink/Downlink Data Rate*

The uplink rate received by the receiver is fixed at 4kbps. The downlink rate transmitted by transmitter is selectable at 125kbps or 1Mbps.

2.2.3.2 Architecture of the TT&C Subsystem

The TT&C subsystem receives commands from the ground station operators and transmits the satellite status and other mission data to the ground station. The TT&C subsystem comprises of the S-band antenna system, RF transceivers (S-band receivers and transmitters) and CCSDS processors. As shown in Fig. 11, the data from each CCSDS processor is connected to the RF transceivers respectively. The outputs of the transceivers are connected to separate pair of antennas. Hence there are eight antenna patches in the TT&C antenna system. The specifications of uplink and downlink subsystems are conformed to the CCSDS's recommendations [14].

Fig. 11: Block diagram of the TT&C subsystem interfaces.

2.2.3.2.1 S-band Antenna System

The TTC antenna system should provide omni-directional coverage so as to allow the ground station to command and retrieve critical system parameters from the satellite at its normal or off-pointing orientation. Due to the limited bandwidth of patch antennas (nominal bandwidth of 5MHz), separate antenna pairs for transmit and receive would be used. In order to achieve omni-directional coverage and to support a tumbling attitude during contingency operations, each transmit and receive antenna comprises of a nadir main beam antenna (in the direction of the camera bore sight) and a null filling antenna at the zenith face of the satellite [6], as shown in Fig. 12. The null filling antenna is fed with power that is 10dB lower with respect to the main beam. With this configuration, the TT&C is able to optimize the link margin by optimum pointing under normal mode of operation and contingency operation when the satellite pointing direction is not optimally stabilized.

Fig. 12: The location of the TT&C antennas on the X-Sat.

The transmit and receive antenna should have a minimum antenna gain of better than -10dBi over 90% of the sky. This requirement is desired to support non-stabilized communication operations. In addition, the gain of the antenna has to be higher than

0dBi for $\pm 60^\circ$ of the boresight of the IRIS camera to support high-speed telemetry data transfer to the ground station while simultaneous imaging operations with off pointing are being carried out [6].

2.2.3.2.2 S-Band Transmitter

The S-band transmitter of the TT&C comprises three modules as shown in Fig. 13: Phase Lock Loop Frequency Synthesizer Module, BPSK Modulator Module and the SSPA Module. The downlink data rate is 125kbps for contingency operations or 1Mbps for normal operations.

Fig. 13: Block diagram of RF modules in the S-band transmitter.

The S-band transmitter employs the direct up-conversion architecture. More components are added in order to fulfil the subsystem requirements. Data from the CCSDS processor is directly modulated at BPSK and further amplified at 2.211GHz. The digital attenuator is added so that the RF power level can be adjusted accordingly. Realizing that the modulated signal may potentially leak to the Phase Lock Loop (PLL) frequency synthesizer, isolators have been added before and after the HPAs. When placing the entire RF circuits into the housing, the HPA output should be placed far away from the frequency synthesizer. To further protecting the frequency Synthesizer, this module must be well shielded and isolated using buffer amplifiers.

The main challenge with S-band transmitter is that its operating frequency is very close to the receiver frequency. The wideband noise generated by the transmitter must be adequately suppressed so as not to blind the receiver. Bandpass filtering within the HPA module and careful design of the antenna system should provide over 50 dB of output noise power suppression to suppress the transmitter noise floor into the thermal noise floor. A bandpass filter is added prior to the last stage of PA for this purpose. It is not cascaded after the PA so that the HPA efficiency can be preserved.

2.2.3.2.3 S-Band Receiver

The receivers' primary function is to track the uplink residual carrier for Doppler frequency shift and down-convert received signal to the 16 kHz command sub-carrier to the CCSDS processor for demodulation. Both the S-band receivers are active at all times. The receiver input port supports a dynamic range of -70dBm to -120dBm to accommodate horizon-to-horizon variations in link margin as well as different sizes of ground station antenna [6].

2.3 Factors Affecting the Performance of X-Sat Microwave Transmission System

To assess the performance of a digital microwave transmission system, a few figures of merit based on relative constellation error (RCE) will be discussed. Factors such as the heat dissipation of module, components used and orbital/altitude perturbation that might affect the performance of the transmission system will also be covered. Taking into account the coding/modulation schemes, noise temperature, Effective Isotropic Radiated Power (EIRP), free space and atmospheric losses, the satellite downlink budget is estimated by simple numerical calculations.

2.3.1 Non-linearity of Microwave Devices

The performance of a microwave communications system depends on the transmitter, the receiver and the air interface over which the communications take place [15] [16]. Most of the microwave communications systems use complex techniques to place bit streams on RF carrier before transmitting and recover the digitally modulated signals propagate through the radio channel. Errors occur anywhere throughout the transmitter or receiver which can impair the signal or data integrity. Therefore, in order to develop a high performance communication, any impairment that can cause signal degradation within the transmitter and receiver must be minimized.

To reduce the complication during troubleshooting, identification of possible impairments within a communication system should be carried out on the transmitter or receiver separately. In this context, the performance of the X-Sat microwave transmitters, the TT&C transmitter and X-band transmitter, will be addressed.

Poor quality transmission can be seen as low signal quality which may result in a high bit-error rate (BER) at the receiver [15]. The RCE is a measure of the constellation cluster variance due to any impairment or transmitter imperfections measured relative to the ideal constellation point locations, as shown in Fig. 14. Expressed in another way, it is the residual noise and distortion remaining after an ideal version of the signal has been stripped away [17]. Typical parameters used to analyze RCE are Root Mean Square (RMS) Error Vector Magnitude (EVM), Root Mean Square (RMS) magnitude error, Root Mean Square (RMS) phase error, frequency error, I/Q offset, gain imbalance, quadrature error, etc. In this thesis, the RMS EVM (EVM) and RMS phase error (PE) would be used for gauging the RF performance.

Fig. 14: Error Vector Magnitude (EVM) and related quantities [18]

A successful transmitter design depends on the ability to locate sources of error. Typical sources of error in a transmitter include gain or phase imbalances, interfering or spurious signals, jamming, noise, symbol timing errors, amplitude or phase nonlinearities, carrier frequency offset, etc [18]. By knowing the types of errors that may occur, the causes of these errors can be traced back to a component, device, or subsystem of the microwave communications system. In the XBT & TT&C transmitter, the cumulative distortions from each RF component shall be less than 10% at typical operating output power of 38dBm [5] and 34dBm respectively [6].

2.3.2 Downlink Forward Error Correction (FEC)

A concatenated coding scheme consisting of Reed Solomon (RS) code and Convolution Code (CC) is recommended by the CCSDS for telemetry channel coding [19]. In this scheme, the CC is used in the inner code and RS code is used for the outer code. These FEC codes are used not only to reduce bursty errors, they are able to detect and correct errors in the presence of additive white Gaussian noise (AWGN). The total coding gain of these applying these codes is approximately 7dB for a BER of 10^{-5} [20]. In the contrary, no coding is used at the XBT because the existing CRISP X-band reception system does not have specific FEC decoder.

2.3.3 Noise in the Microwave Transmission System

Noise is regarded as a disturbance that affects a desired signal and may distort the information carried by the signal. In the X-Sat transmission system, potential impairments in the transmitting signal could be due to noises generated by non-linearities in the amplification devices which produce intermodulation noise, antennas' side lobes and polarization discrimination, etc. However most satellite transmission systems are designed in such a way as to limit interference and most of the modules are shielded inside aluminum chassis with a thickness of 3mm, therefore the thermal noise is predominant. The thermal noise power is given by

$$P_{\text{Noise}} = K \times T \times B \quad (1)$$

Where K is the Boltzmann's constant (1.38×10^{-23} W/Hz/K)

T is the temperature in Kelvin

B is the RF carrier bandwidth in Hz

2.3.4 Heat Dissipation

In the X-Sat, the temperature distribution in a micro-satellite is achieved via passive thermal balance design. Such design maintains the temperature within the satellite from 0 to 55°C throughout its orbit. Most of the electronic components residing inside the spacecraft operate well from -30 to 80°C. However the HPA devices, especially, generate excessive heat when it is powered up. The heat must be efficiently dissipated to prolong the lifespan of the devices and to maintain the power efficiency of the transmission system. Some steps have been taken for better heat dissipation during the module design. First, thermally and electrically conductive epoxy will be applied between the contact of the HPA device and the module. Secondly, high power subsystems such as the HPA modules are attached to the base plate region where the thermal capacity is high. Thus the heat dissipation is

the most efficient. Basically the concept is to use the entire metal structure of the X-Sat for heat sinking and distribution in the space.

Unfortunately the structure of the micro-satellite is not finalized yet and the heat conduction analysis of the satellite structure has not been carried out analytically or experimentally. As a result, a heatsink (125mm x 250mm x 50mm) will be placed below the amplifier module during test and measurement. Since the SSPA module consumes a lot of power and generates a lot of heat, the module will not be power up at all time. It will be powered up for less than 10 minutes during imaging downlink.

2.3.5 Components Selection

The commercially off-the-shelf (COTS) products are getting common for the space application. For a low cost mission and short micro-satellite's lifespan, many of the components in the communication system used are COTS products. The COTS components may be advantageous in terms of cost, power consumption, availability and processing capability. However, unlike dedicated military or space grade components, not all COTS components are able to survive in the space environments with low pressure and extreme temperature changes, as well as withstanding the random vibration and g-force loading introduced by the launch vehicle. Besides, there is risk of component damage due to Single Event Latchup (SEL) induced by high-energy particles flux radiation in the LEO environment.

Due to this reason, considerations such as heritage (used in previous satellite missions), and test results (performed by other laboratories for space applications) of components selected need to be taken into account [21]. Suitable COTS parts can be found from the ESA, NASA parts selection list [22] or data sources from the European Cooperation for Space Standardization (ECSS) [23]. For most of the RF

components used in the X-Sat are based on heritage and recommendation from NASA and ESA. In addition, selecting commercial parts with known SEL performance is preferred. Where information is not available, especially for active component, Gallium Arsenide (GaAs) parts are extensively used; otherwise, bipolar parts would be favored over CMOS [24]. Gallium Arsenide (GaAs) devices are relatively hard to high energy particle radiation in space because of their relatively short minority carrier lifetimes and high majority carrier concentrations [25]. As for MMICs, since they usually have low density in the chip areas, the probability of hit by high energy particles is further reduced. To prevent single-event upsets or latchups and temperature fluctuation that may cause electronics to run slower or stop operating, important environmental tests such as thermal cycling, vacuum test and vibration test must be carried out for all the components selected.

2.3.6 Orbital/Altitude Perturbations on the Radio Communication

The polar sun-synchronous circular orbit is a common choice for LEO remote sensing satellites [26]. At this orbit, the effects of orbit (position) and attitude (pointing) perturbations of a spacecraft are less significant than the geostationary communication satellite. It is because the on-board antennas of LEO satellite are usually low in gain. The loss in link margin due to pointing error of spacecraft or gimbaled spacecraft antenna is normally not very significant.

It is recognized that to compensate for the small variation in satellite position, ground stations are usually required to have some kind of tracking capability to realign the antenna towards the satellite. For reasonably accurate ground station antenna pointing, up-to-date two-line-elements, which is a standard mathematical model used to describe a satellite's orbit, could be used to track the satellite's

position. For more reliable tracking, auto-tracking using conical scan, multi-horn monopulse system, step back or hill climbing system could be used instead [27].

2.3.7 Ground Based System Interferences

The frequencies used by the microwave systems are reserved for X-Sat by the Telecommunication Authority, the Infocomm Development Authority of Singapore (IDA). Emitting radio at reserved bands in Singapore is illegal and the Authority will take action against the intruder. At international level, the IDA are actively involving in the frequency coordination at the World Radio Conference (WRC) and ITU. Hence ground based systems interferences are likely to be very minimum.

2.3.8 Downlink Budget

Link budget is normally calculated to determine if the signal has sufficient strength to propagate to the other end of the transmission chain. Downlink budget is presented here to estimate the required output power from each transmitter to ensure reliable microwave communication. The basic parameters required for the analyses are discussed in equations (2) to (6) and graphically represented in Fig. 15. The downlink budget for the X-band and S-band transmitters will be calculated next.

Fig. 15: Parameters required for link budget analyses.

❖ Effective Isotropic Radiated Power (EIRP)

The EIRP is the apparent power transmitted from the micro-satellite towards the ground station in dBW.

$$\text{EIRP} = P_t \times G_t \quad (2)$$

Where P_t is the transmit power sent to the transmitting antenna in dBW

G_t is the gain of the transmitting antenna in dBi

❖ Free Space Loss

The free space is the basic transmission loss in signal strength between two antennas, given by [28]

$$\text{Loss}_{\text{free-space}} = 20 \log (4\pi d/\lambda) \quad (3)$$

Where d is the transmission path length in m

λ is the wavelength in m

❖ Other Losses

In addition to the free space loss, signal transmitted from the micro-satellite will also suffer losses due to antenna polarization mismatch (polarization loss), connectors and cable (feeder loss), rain attenuation, air moisture, scattering, refraction (atmospheric loss), etc.

❖ Received Power

Based on Friis transmission equation [29] [30], the power received by the ground station antenna, P_r , is given by

$$P_r = \text{EIRP} + G_r + 20 \log [\lambda/(4\pi d)] \quad (4)$$

Where P_r is the power received by receiving antenna in dBW

G_r is the gain of receiving antenna in dBi

❖ Received E_b/N_o

The E_b/N_o is classically defined as the ratio of Energy per Bit (E_b) to the Spectral Noise Density (N_o). It is the measure of signal to noise ratio for a digital communication system. The received E_b/N_o is given by [31]

$$\text{Received } E_b/N_o = \text{Received Power} - 10 \log (\text{data rate}) - 10 \log (k) \quad (5)$$

Where k is the Boltzman's constant, 1.38×10^{-23}

❖ Link Margin

Link margin is defined as the difference between the signal to noise ratio available at the receiver and the signal-to-noise ratio needed at the receiver in an additive white Gaussian channel. The link margin is given by [31]

$$\text{Link margin} = \text{Received } E_b/N_o - (E_b/N_o)_{\text{required}} \quad (6)$$

2.3.8.1 XBT Downlink Budget Analysis

Based on the XBT specifications (section 2.2.2) and equations (2)-(6) discussed, the link budget analyses for the XBT using switched beam and conical beam antennas are calculated at different elevation angles of the ground station, as shown in Table 2 and Table 3 respectively. Since the switched beam antenna is placed at a skewed angle of about 45° from the satellite Z-axis, this antenna is estimated to have its peak gain at the ground station elevation angle of 45° . With eight patches, the switched beam antenna can provide sufficient link margin to support downlink at any data rates to the ground station under nominal condition. For the conical beam antenna that provides omni coverage, it is only able to support low rate downlink along the orbital pass due to its inherent low antenna gain. The link margin at elevation of 90° is insufficient for high rate downlink since its gain at the nadir is very low, as shown in Fig. 7. During heavy rain, when the elevation angle of the ground station is less than 5° , data downlink might not be possible due to insufficient link margin.

Parameter	Units	Switched Beam Antenna					
Ground station Elevation	degree	90.0	70.0	50.0	30.0	10.0	5.0
Frequency	GHz	8.3	8.3	8.3	8.3	8.3	8.3
HPA transmit output power	dBW	8.0	8.0	8.0	8.0	8.0	8.0
Feeder Losses	dB	2.5	2.5	2.5	2.5	2.5	2.5
Antenna Gain	dBi	-0.7	7.0	10.8	10.0	5.1	3.6
TX EIRP	dBW	4.8	12.5	16.3	15.5	10.6	9.1
Range	km	685.0	724.3	865.6	1212.9	2122.6	2528.9
Free Space Loss	dB	167.5	168.0	169.6	172.5	177.4	178.9
Atmospheric Losses	dB	0.5	0.5	0.5	0.5	0.5	0.5
Polarization Loss	dB	0.4	0.4	0.4	0.4	0.4	0.4
Other Losses	dB	5.0	5.0	5.0	5.0	5.0	5.0
GS antenna G/T (13m dish)	dB/K	35.0	35.0	35.0	35.0	35.0	35.0
GS Received power	dBW	-133.7	-126.4	-124.2	-127.9	-137.6	-140.6
Convert data rates to dB-Hz							
1) 12.5mbps	dB-Hz	71.0	71.0	71.0	71.0	71.0	71.0
2) 25mbps	dB-Hz	74.0	74.0	74.0	74.0	74.0	74.0
3) 50mbps	dB-Hz	77.0	77.0	77.0	77.0	77.0	77.0
GS Received Eb/No							
1) 12.5mbps	dB	24.0	31.2	33.4	29.8	20.0	17.0
2) 25mbps	dB	20.9	28.2	30.4	26.8	17.0	14.0
3) 50mbps	dB	17.9	25.2	27.4	23.8	14.0	11.0
Required BER		10^{-5}	10^{-5}	10^{-5}	10^{-5}	10^{-5}	10^{-5}
Required Eb/No (QPSK)	dB	9.6	9.6	9.6	9.6	9.6	9.6
Link Margin (nominal)							
1) 12.5mbps	dB	14.4	21.6	23.8	20.2	10.4	7.4
2) 25mbps	dB	11.3	18.6	20.8	17.2	7.4	4.4
3) 50mbps	dB	8.3	15.6	17.8	14.2	4.4	1.4
Link Margin (worst case)							
Rain Attenuation	dB	3.0	3.0	3.0	3.0	3.0	3.0
1) 12.5mbps	dB	11.4	18.6	20.8	17.2	7.4	4.4
2) 25mbps	dB	8.3	15.6	17.8	14.2	4.4	1.4
3) 50mbps	dB	5.3	12.6	14.8	11.2	1.4	-1.6

Table 2: Estimation of XBT downlink budget using switched beam antenna.

Parameter	Units	Conical Beam Antenna					
Ground station Elevation	degree	90.0	70.0	50.0	30.0	10.0	5.0
Frequency	GHz	8.3	8.3	8.3	8.3	8.3	8.3
HPA transmit output power	dBW	8.0	8.0	8.0	8.0	8.0	8.0
Feeder Losses	dB	2.5	2.5	2.5	2.5	2.5	2.5
Antenna Gain	dBi	-14.0	-0.3	2.8	4.0	3.0	2.0
Tx EIRP	dBW	-8.5	5.2	8.3	9.5	8.5	7.5
Range	km	685.0	724.3	865.6	1212.9	2122.6	2528.9
Free Space Loss	dB	167.5	168.0	169.6	172.5	177.4	178.9
Atmospheric Losses	dB	0.5	0.5	0.5	0.5	0.5	0.5
Polarization Loss	dB	0.4	0.4	0.4	0.4	0.4	0.4
Other Losses	dB	5.0	5.0	5.0	5.0	5.0	5.0
GS antenna G/T (13m dish)	dB/K	35.0	35.0	35.0	35.0	35.0	35.0
GS Received power	dBW	-146.9	-133.7	-132.2	-133.9	-139.8	-142.3
Convert data rates to dB-Hz							
1) 12.5mbps	dB-Hz	71.0	71.0	71.0	71.0	71.0	71.0
2) 25mbps	dB-Hz	74.0	74.0	74.0	74.0	74.0	74.0
3) 50mbps	dB-Hz	77.0	77.0	77.0	77.0	77.0	77.0
GS Received Eb/No							
1) 12.5mbps	dB	10.7	23.9	25.5	23.7	17.9	15.4
2) 25mbps	dB	7.7	20.9	22.5	20.7	14.9	12.3
3) 50mbps	dB	4.7	17.9	19.4	17.7	11.9	9.3
Required BER		10^{-5}	10^{-5}	10^{-5}	10^{-5}	10^{-5}	10^{-5}
Required Eb/No (QPSK)	dB	9.6	9.6	9.6	9.6	9.6	9.6
Link Margin (nominal)							
1) 12.5mbps	dB	1.1	14.3	15.9	14.1	8.3	5.8
2) 25mbps	dB	-1.9	11.3	12.9	11.1	5.3	2.7
3) 50mbps	dB	-4.9	8.3	9.8	8.1	2.3	-0.3
Link Margin (worst case)							
Rain Attenuation	dB	3.0	3.0	3.0	3.0	3.0	3.0
1) 12.5mbps	dB	-1.9	11.3	12.9	11.1	5.3	2.8
2) 25mbps	dB	-4.9	8.3	9.9	8.1	2.3	-0.3
3) 50mbps	dB	-7.9	5.3	6.8	5.1	-0.7	-3.3

Table 3: Estimation of XBT downlink budget using conical beam antenna.

2.3.8.2 TT&C Downlink Budget Analysis

Since the TT&C subsystem is operating at S-band and the downlink data rate is lower than XBT, it has better downlink margin. Considering the worst scenario, the antenna gain is -10dBi over 90% of the sky, it is shown in Table 4 that the downlink margin at low data rate is sufficient along the orbital pass but high rate downlink can only be supported when the ground station elevation angle is greater than 30°.

Parameter	Units	TT&C Antenna System					
Ground station Elevation	degree	90.0	70.0	50.0	30.0	10.0	5.0
Frequency	GHz	2.2	2.2	2.2	2.2	2.2	2.2
HPA transmit output power	dBW	4.0	4.0	4.0	4.0	4.0	4.0
Feeder Losses	dB	1.5	1.5	1.5	1.5	1.5	1.5
Antenna Gain	dBi	-10.0	-10.0	-10.0	-10.0	-10.0	-10.0
Tx EIRP	dBW	-7.5	-7.5	-7.5	-7.5	-7.5	-7.5
Range	km	685.0	724.3	865.6	1212.9	2122.6	2528.9
Free Space Loss	dB	156.0	156.5	158.1	161.0	165.9	167.4
Atmospheric Losses	dB	0.5	0.5	0.5	0.5	0.5	0.5
Polarization Loss	dB	0.4	0.4	0.4	0.4	0.4	0.4
Other Losses	dB	5.0	5.0	5.0	5.0	5.0	5.0
GS antenna G/T (6.1m dish)	dB/K	16.0	16.0	16.0	16.0	16.0	16.0
GS Received power	dBW	-153.4	-153.9	-155.5	-158.4	-163.3	-164.8
Convert data rates to dB-Hz							
1) 125kbps	dB-Hz	51.0	51.0	51.0	51.0	51.0	51.0
2) 1Mbps	dB-Hz	60.0	60.0	60.0	60.0	60.0	60.0
GS Received Eb/No							
1) 125kbps	dB	24.2	23.7	22.2	19.2	14.4	12.8
2) 1Mbps	dB	15.2	14.7	13.1	10.2	5.3	3.8
Required BER		10 ⁻⁵	10 ⁻⁵	10 ⁻⁵	10 ⁻⁵	10 ⁻⁵	10 ⁻⁵
Required Eb/No (QPSK)	dB	9.6	9.6	9.6	9.6	9.6	9.6
RS-CC Coding Gain	dB	7.0	7.0	7.0	7.0	7.0	7.0
Link Margin (nominal)							
1) 125kbps	dB	21.6	21.1	19.6	16.6	11.8	10.2
2) 1Mbps	dB	12.6	12.1	10.5	7.6	2.7	1.2
Link Margin (worst case)							
Rain Attenuation	dB	3.0	3.0	3.0	3.0	3.0	3.0
1) 125kbps	dB	18.6	18.1	16.6	13.6	8.8	7.2
2) 1Mbps	dB	9.6	9.1	7.5	4.6	-0.3	-1.8

Table 4: Estimation of TTC downlink budget.

2.4 Motivation

For a low-cost LEO mission, using COTS HPA module is definitely not a cost-effective solution. The motivations of this research work is to develop a direct QPSK modulator module integrated with COTS discrete parts as alternative configuration for the XBT Modulator Module and Up-converter Module, and design high efficiency linear HPAs, which will fulfill the system specifications outlined in

section 2.2 and demonstrate better performance than the requirements by using three discrete amplifier devices operating at X-band and S-band respectively.

The factors affecting the performance of the transmission system (discussed in section 2.3) will also be taken into account. In particular the emphases will be on minimizing the non-linear distortion on the digitally modulated signal, improving the power efficiency of HPAs and effectively dissipating excessive heat produced by the amplifiers.

2.5 Proposed Direct Up-conversion and HPA Configurations

In this section, the proposed direct up-conversion QPSK modulator and HPA configuration will be discussed. The power budget planning of the RF amplification chain and components selected will be discussed.

2.5.1 Direct Up-conversion Configuration

As shown in Fig. 16, the X-band direct up-conversion QPSK modulator module consists of an X-band QPSK modulator (Remec MIQ56SMD-1) and a hermetically-shielded phase locked Dielectric Resonator Oscillator (DRO). A phase lock DRO is used because the operation does not require changing of operating frequency. Besides, the DRO has excellent frequency stability and extremely low phase noise. Otherwise a frequency synthesizer could be used instead. The baseband data stream, I/Q, will be generated from the Vector Signal Generator (VSG). The main focus of this development is to design the metallic housing, integrate all the parts into the housing and examine the RCE due to the non-linear distortion introduced by the modulator.

Fig. 16: Block diagram of proposed X-band direct up-conversion module.

2.5.2 HPA Configuration for the XBT

Based on the downlink budget analyses presented in section 2.3.8.1, either using a conical or switched beam antennas, the required output power from the last stage HPA has to be higher than 8dBW (equivalent to 38dBm). According to the XBT specifications [5], the typical output power available from the Up-converter Module is 10dBm (up to 15dBm). According to above requirements, Fig. 17 shows the RF amplification chain proposed in this research work.

Fig. 17: Block diagram of proposed HPA module of the XBT.

The module consists of an isolator, a RF detector and two HPAs devices, which are hermetically sealed package and internally matched to 50Ω at the input and output. The PA1 (TMD0708-02, see Appendix A for data sheet) is a GaAs MMIC

manufactured by Toshiba. During the development, a better alternative, Fujitsu FMM5057VF GaAs MMIC (see Appendix B for data sheet), which has better power efficiency than TMD0708-02 is found. Therefore, the TMD0708-02 was used in first cascade amplifier module and later replaced by FMM5057VF in the Engineering Model. The PA2 (see Appendix C for data sheet) is a GaAs FET manufactured by Fujitsu. As discussed in section 2.3.5, GaAs devices are preferred because it is relatively hard to high energy particle radiation. An isolator, with RF power rating of 10W, is added to prevent the module from damage due to large reflected power from the antenna module. The RF detector is also added to provide telemetry of the XBT transmit power. Since only forward power will be monitored, a power divider is designed instead of a directional coupler because this divider has lower insertion loss and physically smaller. Due to lower insertion loss of the divider, the power efficiency of the HPA module will be improved.

As the power gain of the devices may vary, two cases of power budget (min and typical amplifier gain at 1-dB compression point) are shown in Fig. 17. Generally, this configuration is sufficient to amplify the signal to 39dBm even the gain from both PAs is minimum. Note that the losses due to the PCB substrate and DC block capacitors are not included in the calculation. The housing must be carefully designed so that the devices can be well shielded and heat can be efficiently dissipated. The amplifiers, isolator and power dividers will be evaluated individually prior to cascading them.

2.5.3 HPA Configuration for the TT&C Transmitter

Based on the downlink budget analyses presented in section 2.3.8.2, the required output power from the last stage HPA has to be higher than 4dBW (equivalent to

34dBm). According to the TT&C specifications [6], the typical output power available from the Modulator Module is 12 dBm (up to 16dBm). According to above requirements, Fig. 18 shows the RF amplification chain proposed in this research work. Since most of the PA devices operating at S-band require impedance matching, the focus of this research work is to design matching networks for PA1 and PA2 to achieve the required power, as well as obtaining high power efficiency and linearity.

Fig. 18: Block diagram of proposed HPA module of the TT&C transmitter.

The PA1 (see Appendix D for data sheet of FLL177ME) and PA2 (see Appendix E for data sheet of FLL357ME) are hermetically shielded GaAs FET manufactured by Fujitsu. Similarly, two cases of power budget (min and typical amplifier gain at 1-dB compression point) are shown in Fig. 18. This configuration is sufficient to amplify the signal to 34dBm even the gain from both PAs is minimum.

3. Development of X-band Up-conversion Module

3.1. Introduction

During preliminary design review, a reviewer from the ISRO suggested to the CREST to develop direct up-conversion architecture operating at 8.3GHz as an alternative to the double up-conversion architecture for XBT. As a result, an X-band direct up-conversion module was developed as a backup solution.

A typical QPSK modulator, as shown in Fig. 19, consists of a phase shifter, two mixers for I and Q signal modulation, and a summer. Essentially a QPSK modulator is as if two BPSK modulators combined in parallel. Ideally the 'I' data stream modulates with a carrier, $+\cos \omega t$ (in phase with the reference oscillator), to form $+\cos \omega t$ (0°) and $-\cos \omega t$ (180°). The 'Q' data stream modulates with a carrier, $-\sin \omega t$ (90° out of phase with the reference carrier), to form $+\sin \omega t$ (90°) and $-\sin \omega t$ (270°). The summer combines these quadrature signals to yield four output phases, which angular separation between any two adjacent phases is always 90° on a RF carrier.

Fig. 19: Block diagram of a QPSK modulator.

3.2. Design of a Direct Up-conversion QPSK Modulator Module

In this design, the direct X-band Up-conversion Module is developed by assembling a passive wideband QPSK modulator (MIQ56SMD-1) and a phase locked Dielectric Resonator Oscillator (DRO) manufactured by Remec and Lucix respectively. The DRO requires a DC supply of 12V at 0.35A. The drawing of the housing is available at Appendix F. The assembled module is shown in Fig. 20.

Fig. 20: Assembled X-band direct up-conversion module.

3.3. Setup of Equipment

First, the phase noise of the DRO was measured using Agilent PSA E4440A. To begin the RCE analysis of the modulated signal, the module I/Q inputs are connected to the Agilent VSG (PSG E8267D) I/Q ports respectively while the module RF output is connected directly to the Agilent VSA (PSA E4440A) input. Table 5 shows the properties of the baseband I/Q and demodulation parameters set at the VSG and VSA. The baseband filter type selected is based on the XBT specifications. The measured and reference filters set are based on the recommendations from the VSA software.

Parameters	PSG 8267D VSG Baseband I/Q setting	PSA E4440A VSA Demodulation setting
Frequency	-	8.3 GHz
Modulation Type	QPSK	QPSK

Symbol Rate	25Msps	25Msps
Filter Type	Root Nyquist	-
Measured Filter	-	Root Nyquist
Reference Filter	-	Nyquist
Filter Alpha	0.35	0.35

Table 5: VSG and VSA demodulation parameters and settings

3.4. Result and Discussion

The phase noise of the DRO measured is shown in Fig. 21. The DRO output power is about 13dBm at 8.3GHz. When the RCE was initially measured, it is found that the quality of the modulation is very poor. Connecting the module output to a spectrum analyzer, it is shown in Fig. 22 that there is leakage of LO carrier. The impairment is identified, which is due to insufficient grounding of the I/Q modulator as the ground contact of the package to the housing relies merely on the four screws shown in Fig. 23.

Fig. 21: Measured phase noise of Lucix DRO.

Fig. 22: Initial measurement at RF output of X-band direct up-conversion module.

Fig. 23: Cross-section view of X-band direct up-conversion module.

To overcome this problem, the ground surface of SMD package was then epoxied onto the PCB using electrically conductive epoxy, EPO-TEKH20E, as shown in Fig. 24. After the epoxy was cured, the PCB was reassembled as a complete module shown in Fig. 20. It is shown in Fig. 25 that there is no LO leakage observed at the output spectrum after the improvement.

Fig. 24: Modulator package was epoxied directly onto the PCB.

Fig. 25: LO leakage disappears at output of the direct up-conversion module.

The measurement was carried out with a fixed LO power from the DRO (~13dBm) and the baseband power was varied from -1dBm to +6dBm. Fig. 26 shows the EVM and PE measured with respect to the output channel power measured, before and after the grounding improvement. The EVM and PE is quite poor when LO leakage exists. The EVM and PE increase with increasing output power as the device is operating closer to the device P1dB.

Fig. 26: Performance of X-band direct up-conversion module before and after grounding improvement.

3.5. Conclusion

Proper grounding of microwave devices is always crucial to ensure optimum device operation. Ground contact between PCB and microwave device can be improved by using electrically conductive epoxy. The idea of performing direct QPSK modulation at X-band has been proven and demonstrated in this chapter. In the next chapter, an X-band PA module design will be presented.

4. Design and Development of X-band Power Amplifiers

As outlined in Fig. 17 of section 2.5.2, the Solid State Power Amplifier (SSPA) module consists of two HPAs (Toshiba MMIC TMD0708-02 (aka HPA1) and Fujitsu GaAs FET FLM7785-12F (aka HPA2)), a power divider and an isolator. Each component will be evaluated individually before cascading them. The first cascade amplifier was designed with TMD0708-02 and FLM7785-12F. However a better MMIC, Fujitsu FMM5057VF, was found after completion of first cascade amplifier. Hence the TMD0708 was replaced by FMM5057VF in the Engineering Model. To reduce the nonlinear distortion introduced by the amplifier, one of the solutions is to back-off the output power. However this will reduce the efficiency of the amplifier. It is indeed a trade-off between minimizing nonlinear distortion and achieving high Power Added Efficiency (PAE). Nevertheless the first objective is to design a stable and high performance module before deciding the performance trade-off.

4.1. General Characteristics of an Amplifier

❖ Gain

Gain is defined as the ratio of the output signal, P_2 , from an amplifier to the input signal, P_1 . In term of dB, it is given by

$$\text{Gain} = \log_{10}\left(\frac{P_2}{P_1}\right) \text{ dB} \quad (7)$$

Where P_1 and P_2 are the input and output powers respectively.

❖ Power at 1-dB Compression Point (P1dB)

An amplifier maintains a constant and linear gain for low-level input signals. However, at higher input levels, the amplifier goes into saturation and its gain decreases as shown in Fig. 27. At the point where the input signal is amplified by 1

dB less than the small signal gain, the 1 dB Compression Point has been reached.

Output P1db is given by

$$P_{1dB_{output}} = P_{1dB_{input}} + (\text{Gain} - 1) \text{ dBm} \quad (8)$$

Fig. 27: Variation of output power with input power.

❖ Saturated Power (P_{sat})

The amplifier is said to reach its saturation point when the output power from the amplifier remains unchanged with increasing input power. If the input power is increased to an extreme value, the amplifier will be destroyed.

❖ Power Added Efficiency (PAE)

The power added efficiency (PAE) is defined as the ratio of the difference of the output (P_{OUT}) and input power (P_{IN}) to the DC power (P_{DC}) consumed, given by

$$PAE = (P_{OUT} - P_{IN})/P_{DC} * 100\% \quad (9)$$

4.2. Design Considerations

At the initial stage of prototyping, the major constraints faced were insufficient power gain, low output power at P1dB and oscillation. The reasons are identified and some of the design considerations are listed below.

4.2.1. Selection of HPA Devices and Materials

The satellite microwave transmission system should be designed to withstand the launch vehicle requirements (i.e. random vibration and g-force loading) and the

stringent space environment of the low earth orbit (i.e. the thermal and radiation effects). Therefore the components and materials used for the sub-circuits have to be carefully selected. As discussed in section 2.3.5, the components and materials selected are primarily based on the recommendation listed by the NASA or ESA.

GaAs FET amplifier devices are selected because these HPA devices show greater linearity and operate well at elevated temperature [32]. All the amplifier packages selected are hermetically sealed so that they do not outgas in the space. The lumped elements used are ceramic capacitor and resistor manufactured by ATC Inc. When selecting a PCB substrate, issues like dielectric constant (ϵ_r) control, material loss, electrical and mechanical thermal stability, manufacturability and cost have been taken into considerations. A few choices of low loss Roger PCB substrates are shown in Table 6. All these materials are approved for spacecraft applications [33]. FR4 is not considered as it is very lossy ($\tan \delta$ of 0.02) at X-Band. RT/Duroid 5870 and RT/Duroid 5880 were not considered because the thermal conductivity are not as good as RO4003/RO4350/Duroid6002. Since the price of RT/duroid6002 is far more expensive than RO4003/RO4350, both RO4003/RO4350 could be used. For all the X-band prototypes, RO4003 is selected because it has slightly lower dissipation factor. The RO4003 substrate has a thickness of 0.508 mm and copper thickness of 0.034mm. RO4350 is the best alternative substrate after RO4003.

Properties	RO4003C [34]	RO4350B [34]	RT/Duroid 5870 [35]	RT/Duroid 5880 [35]	RT/Duroid 6002 [36]
Dielectric Constant (ϵ_r)	3.38±0.05	3.48±0.05	2.33±0.02	2.2±0.02	2.94±0.04
Dissipation Factor at 10GHz ($\tan \delta$)	0.0027	0.0037	0.0012	0.0009	0.0012
Thermal Conductivity (W/m/K)	0.64	0.62	0.22	0.2	0.6

Table 6: Choices of PCB substrates.

4.2.2. Heat Dissipation

For efficient heat dissipation, the HPA devices and PCBs have to be mounted directly on an aluminium plate. Table 7 shows the initial observation recorded. The power gain drops drastically as the temperature increases. This phenomenon is particularly severe for HPA2. The first prototype of HPA2 was developed on a small piece of metal plate. When it was first powered on, the power gain measured was approximately 6dB and drop to 2dB after 30 seconds. A temperature of 120°C was measured on the surface of HPA device. As a result, thicker aluminium plate was used in the subsequent prototype. As discussed in section 2.3.4, the HPA modules will be attached to the base plate of the X-Sat for heat dissipation. Proper heat dissipation is also essential during test and measurement.

Aluminium Thickness (mm)	Gain (dB)	P1dB (dBm)	HPA Device Temperature (°C)
8	3 - 6	< 37	>120
45	5 - 7	> 37	<70

Table 7: Performance of HPA2 with respect to the thickness of the heat sink measured at room temperature (no epoxy applied).

4.2.3. HPA Device and PCB Grounding

The PCB ground contact of the first few prototypes relied merely on the screws. It is found that the amplifiers oscillate occasionally. However pressing on certain area of the PCB, the oscillation disappeared. Therefore the PCB and HPA device ground was then epoxied directly onto the metallic housing using thermally and electrically conductive silver epoxy, EPO-TEKH20E. This is to ensure proper electrical contact (DC and RF ground) and thermal conduction (heat sinking) of the HPA device and PCB ground plane to the aluminium housing. The chosen epoxy requires thermal curing of 20 minutes at 120°C. Higher temperature would shorten the time. However the temperature set should not exceed the absolute HPA device temperature.

It has been found that the HPA without epoxy has insufficient ground contact, and leading to lower power gain and output P1dB measured, as shown in Table 8. In the worst case, the HPA device may become unstable and start to oscillate.

Epoxy Applied	Gain (dB)	P1dB (dBm)	Other Observations
No	3 - 7	< 38	Oscillation
Yes	> 9	> 40	-

Table 8: Performance of HPA2 measured at room temperature before and after the HPA device and PCB were epoxied.

4.2.4. DC Block Capacitor

The Equivalent Series Resistance (ESR) of the capacitor has to be as small as possible to minimize the coupling loss [37]. The self-resonant frequency of the DC block capacitor should not fall near the operating frequency [38]. ATC 600F series capacitor is selected since it has very low insertion or coupling loss and high resonant frequency. The easiest way to determine the suitability of a capacitor is to measure the insertion loss of the capacitor. Since the S-parameters of each capacitor value are available from the ATC website, any simulation tool can be used to predict the insertion loss and resonant frequency of a capacitor.

4.2.5. DC Bias Network

It is important to evaluate the performance of the bias network. Improper design of a DC bias network may lead to oscillations if the RF signal leaks to the DC supply. Hence it is worthwhile to evaluate the bias network before designing the HPA. The objective of the bias circuit design is to minimize the insertion loss while having high RF isolation to the DC source. The bias network is usually designed by using a high impedance quarter-wavelength transformer with either a radial stub [39] or chip capacitors [40]. The bias network consists of a quarter-wavelength

$$Z_c = \frac{1}{2\pi f C} = \frac{1}{2\pi f (15 \times 10^{-6})} = \frac{0.0106}{f_{(MHz)}} \quad (10)$$

60

As part of the investigation, the biasing network was epoxied onto an aluminium block as shown in Fig. 29. The circuit was simulated in ADS2003 and measured using the Anritsu VNA. The simulated and measured results were plotted in the same graph for comparison in section 4.6 (Results).

Fig. 29: Photo of the bias network.

4.3. Design and Development

4.3.1. Design of Single Stage Toshiba & Fujitsu HPAs

Taking all the practical considerations discussed, the HPAs were first designed and evaluated separately. Both internally matched MMIC, Toshiba TMD0708 and Fujitsu FMM5057VF, were designed. As discussed earlier in section 2.5.2, the FMM5057VF is an alternative to TMD0708 found during the development. The TMD0708 was used in the initial development but was replaced by FMM5057VF later. The design of HPA1 is simpler as the bias pins were isolated from the RF pin as shown in Fig. 30 and Fig. 31. Based on the properties of RO4003 substrate discussed in section 4.2.1, the 50Ω Line width calculated from the “Agilent LineCal” software is 1.14mm. As discussed in section 4.2.5, the bypass capacitor, in the range of 1uF to 20uF, should be placed at the input of every DC point. The TMD0708 is biased at V_{DS} of 10V, I_{DS} of 1.7A and V_{GS} of -5V, I_{GS} of 30mA while FMM5057VF is biased at V_{DS} of 10V, I_{DS} of 1.1A and V_{GS} of -5V, I_{GS} of 5mA.

Fig. 30: The layout and photo of HPA1 (TMD0708-02).

Fig. 31: The layout and photo of HPA1 (FMM5057VF, alternative for HPA1).

Since the RF and DC paths of HPA2 device share the same pin, the bias network evaluated in 4.2.5 was incorporated into the design as shown in Fig. 32. According to manufacturer's recommendation, a 50Ω resistor is added in series at the gate input for more reliable operation of the GaAs FET. DC block capacitor was added at the input and output of the HPA. HPA2 is biased at V_{DS} of 10V, I_{DS} of 2.9A and V_{GS} of $-0.5V$, I_{GS} of 1mA.

Fig. 32: The layout and photo of HPA2.

To avoid oscillation and device transient burnout, it is important to turn-on and turn-off the HPA devices in a proper sequence. The limits defined in the device data sheet have to be respected. The below sequences prevent exceeding these limits [41]:

Turn-on procedure:

- 1) Ensure V_{gs} and V_{ds} is set to 0V before switch on.
- 2) Decrease V_{gs} to the pinchoff voltage.
- 3) Increase V_{ds} slowly to the recommended V_{ds} value.
- 4) Increase V_{gs} to obtain quiescent drain current recommended by the device manufacturer.
- 5) With the bias conditions properly set, apply RF drive.

Turn-off procedure:

- 1) Turn off the RF drive.
- 2) Decrease V_{gs} down to the pinchoff voltage.
- 3) Decrease V_{ds} down to 0V
- 4) Increase V_{gs} to 0 V.

The measurement of single stages HPA are presented in section 4.6 (Results).

4.3.2. Design of Microwave Power Divider

The directional coupler is usually used to couple forward and reverse power at the output of a HPA. Since the SSPA unit only requires telemetry of the forward power, the coupler can be replaced by a simple power divider circuit. **This novel power divider is modified and realized based on the bias network.** Without changing the layout, it can be designed to have a coupling ratio of 30dB to 35dB.

To illustrate how this can be achieved, the schematic shown in Fig. 28 will be re-simulated with and without the 15uF bypass capacitor. Without the capacitor, the ratio of leakage power from Term1 to Term3 is approximately 30dB at 8.3GHz (coupled ratio is therefore 30dB). Placing a high capacitance tantalum will further reduce the leakage power ratio to approximately 35dB (coupled ratio will be 35dB in this case) as shown Fig. 33. Thus the leakage power from Term1 to Term3 is similar to the forward coupled power in a conventional 4-port coupler. The design concept is to control the amount of leakage power to Term3 by using a quarter wavelength transformer (as if an inductor) and a radial stub (as if a capacitor). When using a tantalum capacitor, the leakage power ratio can only be adjusted by 5dB. To further increase or decrease the leakage power ratio by 10dB or more, the stub dimension and transformer length must be re-optimized. Changing these dimensions will shift the resonant frequency.

Fig. 33: Leakage ratio from Term1 to Term3 with and without the bypass capacitor.

With this topology, the insertion loss of the divider is significantly lower than a conventional coupler because the insertion loss of the divider is independent of the coupling ratio. The only disadvantage of such configuration is that the “coupled”

power ratio is not flat across a wideband of frequency. It is because the stub and quarter wavelength transformer are narrowband and frequency dependant elements. For the current application, it is not a serious concern since the objective is to ensure that the divider contributes the lowest insertion loss. The layout of the power divider is shown in Fig. 34. The hardware is similar to the one shown in Fig. 29. The measured result is presented in the section 4.6 (Results).

Fig. 34: Layout of the power divider.

4.3.3. RF Detector Circuit

As shown in Fig. 17, the detector circuit that converts the RF power into DC voltage is incorporated at the divider output. The RF detector selected in this work is a surface mount Schottky mixer diode, HSMS-8202 (see Appendix H for data sheet), manufactured by Agilent Technologies. The approach used is the self-biased (zero bias) single diode detector [42] as shown in Fig. 35. Such detector could be realized either by placing it in series or in shunt. In this research work, the Schottky diode was shunted across the microstrip line to the ground.

Fig. 35: Detector circuit.

The diode will convert the RF power coupled from the divider output to a DC voltage. Different RF power level from the HPA output will generate an equivalent DC level to the CAN module. Hence the DC voltage is a telemetry that represents the forward RF power of the XBT. A capacitor is placed in series to block the converted DC from flowing back to the divider. A DC feed through filter (similar to LPF) is added to ensure that there is no analogue signal at the output.

4.3.4. Design of Isolator

As discussed in section 2.5.2, an isolator is placed after the power divider so that the HPA device can be protected from damage if there is any reverse power from the antenna module. As shown in Fig. 36, the design is rather straightforward. The measurement is presented in section 4.6 (Results).

Fig. 36: The layout and photo of the isolator.

4.3.5. Development of Toshiba & Fujitsu Cascade Amplifier Module

This cascade amplifier was developed before a better alternative for HPA1 is found. In this design, the HPA1 (Toshiba TMD0708-02) was cascaded at the input of HPA2 (FLM7785-12F) and a 35dB power divider and RF detector circuit were cascaded at the output, as shown in Fig. 37. All the PCBs and HPA devices were epoxied to the aluminium housing. Isolation walls were added between the HPAs to avoid cavity resonance when the module is covered with a metallic cover. The DC feed-through filters were used at every DC point to attenuate noise, if any, generated by the power supply. Measurement is presented in section 4.6 (Results).

(a) Housing layout before integration

(b) Complete cascade HPAs

Fig. 37: X-band Toshiba and Fujitsu cascade HPA.

4.3.6. Development of SSPA Engineering Model

The SSPA Engineering Model is slightly different from the cascade amplifier module presented in the previous section. The Toshiba MMIC is now replaced by the Fujitsu MMIC, FMM5057VF. Replacing this device will further improve the module PAE because the new device consumes 0.5W lesser DC power. In addition to this replacement, an isolator will be cascaded after the HPA2 to form a complete SSPA Engineering Model.

Fig. 38 shows the layout of the SSPA unit designed in ADS layout. Since the housing dimension of the SSPA module is specified at 70 mm x 145mm x 17mm,

the PCB is intentionally extended at the input to meet the requirements. The drawings of the module housing and isolation wall are available at Appendix I. With operating frequency going higher into the microwave and millimeter-wave band, the cavity resonance effects become a common problem when the standing wave resonance (SWR) peaks at certain points. For this design, more isolation walls and blocks are added to avoid cavity resonance. The walls in the grey colour are fixed while blocks shaded in yellow are detachable blocks. If the cavity resonance happens, the detachable blocks can be installed into the module to solve the problem. The completed module is shown in Fig. 39.

Fig. 38: PCB layout of SSPA EM.

Fig. 39: Inner view of SSPA EM developed.

When the SSPA was first powered up, a resonant frequency of 7.55GHz is observed on the VSA even without feeding test signal at the input. However, if the cover was removed, nothing was observed on the VSA. It has been identified that the cavity resonance is caused by the HPA1 because resonant frequency was detected only when the HPA1 compartment was covered. Furthermore, the resonant frequency could still be observed on the VSA when the DC supply to HPA2 was cut off.

4.4. Cavity Resonance of Microwave Circuits in Enclosed Housing

The effect of cavity resonance is mainly due to the module height and the housing structure. The standing wave has the characteristic such that the E and H fields are 90° out of phase with each other. The impedance will therefore fluctuate wildly across the cavity causing unknown (usually bad) effects on circuitry including the introduction of instability to active devices [43]. It is hard to simulate the impact of cavity because not all the component properties can be accurately defined, especially the active components. A more practical approach is to examine and identify the cavity resonance on the actual hardware. Relocating a particular circuit element to a different position in the cavity can often fix the problem but it involves an investment in engineering redesign time and possible manufacturing delays.

A few simpler approaches are demonstrated in the next section to overcome this problem. The whole module was then imported into the CST Microwave Studio, a 3D electromagnetic simulator, for EM simulation. The objective of the simulation is to visualize the field distributions inside the module.

4.4.1. Practical Approaches

I) Microwave Absorber

Pasting microwave absorber on the module cover is the quickest and easiest solution to get rid of cavity resonant as shown in Fig. 40. The absorber placement is determined based on the cut-and-paste trial and error method. This solution might incur additional cost to purchase space grade absorber or to conduct qualifying tests for the absorber and adhesive material. In addition, the output power is a few dB lower due to the wave absorption. Fig. 57 shows that the SSPA output power is only up to 38dBm at input power of 8dBm whereas the output power hits 39dBm when using isolation blocks. Fig. 58 shows that the relative EVM and PE measured degrade with increasing output power.

Fig. 40: Absorber was pasted on the cover of HPA1 compartment.

II) Detachable Isolation Block

The concept of using isolation block is to disrupt the standing wave via intelligent positioning of the blocks. It is difficult to determine a priori where the optimum blocks placement would be because the isolation blocks act to damp the resonance sometimes, other times they act to shift the SWR peaks to a less detrimental location. As a result, this approach might require more time to determine the optimum placement of the blocks.

To begin the study, the detachable blocks made were installed accordingly as shown in Fig. 39. It is found that the resonant frequency shifts to a higher frequency with the existence of these blocks. The existing position of the blocks was not effective in damping the resonance. An attempt to place four copper blocks at the corner of HPA1 compartment, as shown in Fig. 41, was able to get rid of the problem. However this solution might require engineering redesign effort.

Fig. 41: Damping cavity resonance using copper blocks.

Since most cavities are somewhat rectangular in shape [43], two isolation blocks extending over the HPA devices were manufactured to reduce the cavity size of each compartment, as shown in Fig. 42. This method effectively damps the resonance but unfortunately another problem arises. When CW was fed into the SSPA input, the output carrier was coupled with spurious, as shown in Fig. 59. This has resulted in extremely high EVM and PE of the modulated signal. It has been identified that the DC supplied to HPA1 was interfered by the input RF. To filter out the spurious, the optimized arrangement is to detach the first isolation block and add another two tantalum capacitors to the bias network of HPA1, as shown in Fig. 43. The optimized SSPA module was enclosed with screws as

shown in Fig. 44. To validate the consistency and performance of the SSPA EM developed, another similar module was developed. The performances of the first optimized SSPA and the second SSPA are shown in section 4.6 (Results).

Fig. 42: Damping cavity resonance using aluminium blocks that extend over the HPA devices.

Fig. 43: Inner view of the optimized SSPA EM.

Fig. 44: Outer view of the optimized SSPA EM.

4.4.2. Verification via Electromagnetic Field Plots

The SSPA housing exported to the design environment of CST Microwave Studio is shown in Fig. 45. The heights of the HPA devices were modelled according to the information given in the data sheet. The substrate is defined based on the properties of RO4003. The “red dots” are the discrete ports, used to generate signal to the RF traces. In fact, the model is identical to the module developed in Fig. 43, except the lumped components, solder and connectors are not included in the simulation. The simulation was carried out using “Time Solver”. To shorten the simulation time, the metallic housing was defined as Perfect Electrical Conductor. The settings used in the simulation are listed in Appendix J. The simulation took about 10 hours to complete the computation. The electric and magnetic energy densities simulated are shown in Fig. 46 and Fig. 47 respectively.

Fig. 45: Model imported to CST Microwave Studio.

Fig. 46: Electric Energy Density at 8.3GHz.

Fig. 47: Magnetic Energy Density at 8.3GHz.

Majority of the electric and magnetic energy are concentrating at the output of HPA2 as shown in Fig. 46 and Fig. 47. Looking at the side view of the module, part of the energy is actually blocked by the isolation block that was installed over HPA2 device. Due to strong E and H energy concentrated at this region, the standing wave will fluctuate wildly across the cavity if no isolation block is used. If this happens, cavity resonance may potentially occur. Besides, it is also found that some energy exists at the bias line of HPA1. Both observations may explain the phenomenon encountered on the SSPA module. After added the isolation block over HPA2 device, the cavity resonance disappeared but the output carrier was coupled with spurious. As shown in Fig. 46, the spurious is due to electric energy leaked to the input bias line. After added a capacitor at the bias line, the SSPA module operates as usual.

4.5. Test Setup for RCE Study

To generate and analyze the digitally modulated signals, two types of instruments, the Agilent VSG (PSG E8267D) and the Agilent VSA (the PSA E4440A) were used for testing X-band HPA. The PSA E4440A VSA (up to 26.5GHz) was used because it has demodulation bandwidth of up 80MHz. The PSG 8267D VSG can generate vector RF up to 44GHz. The VSG I/Q modulation and VSA demodulation settings are listed in Table 5. The actual power set at the VSG and measured at the PSA was re-measured using Agilent power meter, 53147A, to ensure accuracy of data taken. As a reference, the average EVM and PE of 25Msps QPSK RF generated by the PSG E8267D is 1.6%, 0.65° at 8.3GHz. To remove the impairments introduced by the VSG, the relative EVM and PE are defined as:

$$\text{Relative EVM} = \text{EVM}_{\text{Measured at DUT output}} - \text{EVM}_{\text{Introduced by the VSG}} \quad (11)$$

$$\text{Relative PE} = \text{PE}_{\text{Measured at DUT output}} - \text{PE}_{\text{Introduced by the VSG}} \quad (12)$$

4.6. Results

4.6.1. Measurement of DC Bias network

Fig. 48 shows that the simulated and measured insertion loss of the bias circuit (in Fig. 29) is approximately 0.4dB and the return loss is better than -20dB. Note that the insertion loss measured includes the losses introduced by the connectors.

Fig. 48: Simulated and measured S-parameter of the DC bias network.

4.6.2. Measurement of Single Stage Toshiba & Fujitsu HPAs

The small signal gain of for TMD0708, FMM5057VF and FLM7785-12F measured using VNA is 23.3dB, 25.1dB and 9.5dB respectively. The HPAs were initially tested with CW at 8.3GHz to estimate their P1dB. The P1dB and PAE of the HPAs are shown in Fig. 49, Fig. 50 and Fig. 51. It can be seen that the output power of FMM5057VF is slightly higher than the Toshiba MMIC. At output power of 34dBm, the PAE of this FMM5057VF MMIC is 3% better as the DC power consumption is 0.5W lesser. The numerical data of the measurement is available at Appendix K.

Fig. 49: Output power and PAE of HPA1 (TMD0708) at 8.3GHz tested with CW.

Fig. 50: Output power and PAE of HPA1 (FMM5057VF) at 8.3GHz tested with CW.

Fig. 51: Output power and PAE of HPA2 at 8.3GHz tested with CW.

4.6.3. Measurement of Microwave Power Divider

The measured insertion loss of the power divider is less than 0.4dB with approximately 35dB of “coupled” power at 8.3GHz.

Fig. 52: Measured insertion loss, return loss and coupled ratio of the X-band power divider with 15uF tantalum.

4.6.4. Measurement of Isolator

The insertion loss and isolation of the isolator measured is approximately 0.7dB and 35dB at 8.3GHz respectively.

Fig. 53: S-Parameter of the isolator measured.

4.6.5. Measurement of Toshiba & Fujitsu Cascade Amplifier and Discussion

The cascade amplifier consumes approximately 44W of DC power. It was first tested with CW. The output P1dB of 40.7dBm at 8.3GHz was measured with an overall PAE of 27% as shown in Fig. 54 (a). The cascade HPA has a linear gain of approximately 34dB. The detected DC voltage level corresponds linearly to the output power as shown in Fig. 54 (b). It is also worthwhile to mention that the HPA has low 2nd and 3rd harmonic levels, at least -50dBc at output power 40.5dBm, as shown in Fig. 55. Hence low pass filter is not necessary at the output.

Fig. 54: Performance of the Toshiba and Fujitsu cascade HPA tested with CW at 8.3GHz.

Fig. 55: Output spectrum measured at the output of Toshiba and Fujitsu cascade HPA.

To examine the RCE of modulated signal introduced by the cascade HPAs, the 25Msps QPSK test signal was generated from PSG E8267D VSG instead of CW. Fig. 56 (a) shows the output channel power and PAE measured when tested with 25Msps QPSK signal. If the output power is below 37dBm, driving at the same input power, the same output power level is measured for CW or modulated signal. However, it is found that the power measured is approximately 1dB less than that of CW when the output power is near to the P1dB (~38.5dBm). In Fig. 56 (b), it is shown that the corresponding relative EVM and PE increase with the output power.

Fig. 56: Performance of cascade Toshiba and Fujitsu HPA tested with 25Msps QPSK signal at 8.3GHz.

The drawback of achieving higher output power is increased distortion of the modulated signal. Figures are plotted separately for clearer distinction of EVM, PE, PAE and output power with reference to the input power.

4.6.6. Measurement of SSPA Engineering Model

4.6.6.1. Measurements Taken while Troubleshooting Cavity Resonance

Fig. 57 and Fig. 58 show the performance measured when absorber was pasted at the cover of HPA1 compartment. Fig. 59 shows the spurious observed on the spectrum analyzer after installed 2 isolation blocks extending over the HPA devices.

Fig. 57: Pout and PAE of SSPA EM measured with absorber.

Fig. 58: EVM and PE of SSPA EM measured with absorber.

Fig. 59: Output carrier with spurious.

4.6.6.2. Measurement of Optimized SSPA Engineering Model

Comparing the power level in Fig. 56 (a) and Fig. 60, the output power of the engineering model is approximately 0.7dB lower due to the insertion loss of the power divider and isolator. Depending on the system requirement, one can decide the trade-off between the tolerable impairment and desired output power based on result shown in Fig. 61. Fig. 62 shows that the DC voltage measured at the output of the detector. Each RF power level is corresponded to a DC level. At the output power of 38.5dBm, Fig. 63 shows that the 2nd and 3rd harmonics are at least 60dBc below the desired frequency.

Fig. 60: Pout and PAE of the optimized SSPA EM.

Fig. 61: EVM and PE of the optimized SSPA EM.

Fig. 62: DC voltage detected with respect to Pout of the optimized SSPA EM.

Fig. 63: Output spectrum measured at the output of the optimized SSPA EM.

The second module has slightly better performance than the previous module as shown in Fig. 64 to Fig. 66. Note that the DC voltage measured at the output of the detector in both models is different since the coupled power from the power divider varies. It is because tantalum capacitor was not added in the power divider circuit for the first EM (coupling ratio is therefore $\sim 30\text{dB}$) while tantalum capacitor was added in the second EM (coupling ratio is $\sim 35\text{dB}$). The purpose is to find out the DC voltage difference with respect to different coupling ratio. Most importantly, the DC level detected should linearly correspond to a RF power so that the actual output power can be estimated accordingly.

Fig. 64: Pout and PAE of second SSPA EM.

Fig. 65: EVM and PE of second SSPA EM.

Fig. 66: DC voltage detected with respect to Pout of second SSPA EM

Although the manufacturer specifies typical P1dB of FLM7785-12F at 41.5dBm, most of the FLM7785-12F device has P1dB lower than 41dBm at 8.3GHz, as shown in Fig. 67.

Fig. 67: Manufacturer's test data of two FLM7785-12F GaAs FET.

4.7. Conclusion

The evaluation of bias network is recommended to ensure minimum insertion loss at the frequency band of interest. If broadband coupling response is not required, the X-band power divider presented could be used since the insertion loss is lower than a conventional coupler. As the power divider only requires a quarter wavelength transformer and a radial stub, the layout of the circuit can be flexibly designed within a small area, as shown in Fig. 43. From equation (9), it can be seen that the PAE is linearly proportional to the P_{OUT} . The P_{OUT} from the SSPA module using this

power divider will be higher than the module using a conventional coupler. As a result, the PAE of the SSPA module using this novel power divider will also be improved.

Although 3D electromagnetic simulation takes substantial time to complete the computation, the 3D electric and magnetic fields distribution created within a metallic enclosure is rather useful for troubleshooting the effect of cavity. It is also worthwhile to mention that the model was simplified to shorten the simulation time. In order to fully understand the behavior of cavity resonance within this enclosure, a more precise module, which includes the models for discrete components, should be created. This could be one interesting topic for future research.

Besides, the HPA should be measured with modulated signal instead of CW in order to fully understand the non-linear behaviors introduced by the HPA. It has been shown that the RCE of the amplified QPSK signal increases when the amplifier is operating near to its P1dB. Therefore, the trade-off between the tolerable impairment of the modulated signal and PAE should be made based on the system requirements. All numerical test data is available in Appendix K for reference. In the next chapter, the design of HPA operating at S-band will be presented.

5. Design of S-band HPA Based on Small Signal S-parameters Analysis

5.1. Introduction

As shown in Fig. 18, the HPA module of the TT&C transmitter consists of two HPAs. In this chapter, the final stage S-band HPA were designed using a Fujitsu GaAs FET, FLL357ME. The goal of this HPA design is to achieve 11dB of gain and output power of 34.5dBm at 2.211GHz. Unlike X-band HPA, the HPA device is not internally matched to 50Ω . The challenge is to design the input and output impedance matching circuits. Since large-signal S-parameters of a HPA device are normally not provided by the manufacturer, one of the practical methods is to characterize the device is through load and source pull before designing the impedance matching network. However the design basically cannot be accomplished without the load pull system. Furthermore a commercial load pull system is extremely expensive.

In this chapter, **a simpler and novel approach is demonstrated on how to design HPA without a complete load pull facility**. When the Fujitsu PA device was first tested without matching network, the power gain measured was 6dB less than the device specification at 2.211GHz. By using conjugate impedance matching technique, the HPA is first matched for gain. This is followed by load pull of the pre-matched HPA using slide screw tuner to locate the load impedance. Based on the load impedance measured, the output matching network of the HPA is redesigned and tuned to achieve output power of 3.5W at 2.211GHz.

The PCBs substrate used for this S-band HPA prototypes is Roger RO4350, having a thickness of 0.762mm and relative permittivity, ϵ_r of 3.48. As discussed in 4.2.1, RO4350 has quite identical properties to RO4003. Since RO4003 was temporarily

out of stock during the research period, RO4350 was used. All PCBs were milled using Quick Circuit System, from T-Tech, Inc instead of chemical etching to reduce development cost.

5.2. Concept of Complex Conjugate Impedance Matching

An amplifier can be constructed as shown in Fig. 68. Normally the small signal S-parameter of the amplifier is provided by the manufacturer. The input and output matching networks are needed to match the active device to the source and load impedance.

Fig. 68: Typical configuration of a single-ended amplifier.

By using complex conjugate impedance matching techniques, maximum power gain of an amplifier can be achieved. Equations below explain how an amplifier could be matched to both input and output ports impedance simultaneously. For a complex conjugately matched source,

$$\Gamma_{in} = \Gamma_s^* = S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1 - \Gamma_L S_{22}} \quad (13)$$

Similarly, for a complex conjugately matched load,

$$\Gamma_{out} = \Gamma_L^* = S_{22} + \frac{S_{21}S_{12}\Gamma_s}{1 - \Gamma_s S_{22}} \quad (14)$$

Equations (13) and (14) have to be satisfied at the same time for simultaneous impedance matching. Solving both equations simultaneously, the matched source and load reflection coefficients, Γ_{sM} and Γ_{LM} , are given by [44]

$$\Gamma_{SM} = \frac{B1 \pm \sqrt{B1^2 - 4(|C1|)^2}}{2 \cdot C1} \quad (15)$$

$$\Gamma_{LM} = \frac{B2 \pm \sqrt{B2^2 - 4(|C2|)^2}}{2 \cdot C2} \quad (16)$$

Where

$$B1 = 1 + (|S11|)^2 - (|S22|)^2 - (|\Delta|)^2 \quad (17)$$

$$B2 = 1 - (|S11|)^2 + (|S22|)^2 - (|\Delta|)^2 \quad (18)$$

$$C1 = S11 - \Delta \cdot S22^* \quad (19)$$

$$C2 = S22 - \Delta \cdot S11^* \quad (20)$$

$$\Delta = S11 \cdot S22 - S12 \cdot S21 \quad (21)$$

Note: the plus sign is used when $B_{1,2} < 0$ and the minus sign when $B_{1,2} > 0$.

After calculated the reflection coefficients, the impedance matching networks can be designed by using the single stub tuning approach, as shown in Fig. 69. The shunt stub can be opened-circuited or short-circuited. Open-ended shunt stub is preferred because no “vias” are required and it is easier to fabricate. With the aid of RF design software, the impedance matching networks can be easily designed if the device S-parameter is provided by the manufacturer. Usually the line impedance of $\lambda_1, \lambda_2, \lambda_3$ and λ_4 is 50Ω . Only the lengths of these lines need to be determined and optimized.

Fig. 69: Impedance matching using single stub matching technique.

Stability is another important criterion in an amplifier design. If the S-parameter of an amplifier is available, an easy method to examine the stability of an amplifier is to calculate the Rollet stability factor, K. The K is given by [44] in equation 22. If K is bigger than 1, the amplifier is unconditionally stable and vice versa.

$$K := \frac{1 - (|S_{11}|)^2 - (|S_{22}|)^2 + (|\Delta|)^2}{2 \cdot |S_{12} \cdot S_{21}|} \quad (22)$$

With condition $|\Delta| < 1$

5.3. Design Procedures

The performance of the HPA device, GaAs FET FLL357ME, was first verified under small signal, which tested without any matching network as shown in Fig. 70. The DC bias circuit was designed based on the proposed bias network shown in [40] to minimize the physical dimension of the PCBs. Biasing the HPA at V_{DS} of 10V, I_{DS} of 0.72A and V_{GS} of -1V, the S-parameters provided by the manufacturer and measured are plotted on the same graph in Fig. 76 for comparison. It can be seen that the S-parameters measured and provided by the manufacturer are well matched. It is also shown that the HPA device was poorly matched because the gain measured was a few dB lower than the device specification. The K Stability Factor measured is greater than 1 implying that the HPA is unconditionally stable from 1 to 3 GHz.

Fig. 70: FLL357ME HPA tested with 50 ohms lines at the input and output.

5.3.1. Design of Amplifier for Maximum Gain

Based on the small signal S-parameters provided by the manufacturer (with test data of P1dB at 34.98dBm), the HPA was designed for maximum gain at 2.211GHz by using the complex conjugate impedance matching technique. Fig. 71 shows the matching circuits simulated and optimized in ADS. As recommended by the manufacturer, a 100Ω resistor is added at the gate bias. The layout and photo of the HPA designed is shown in Fig. 72. The small signal S-parameters simulated and measured with VNA are shown in Fig. 77. The gain measured at 2.211 GHz is improved from 5.9dB to 12.8dB. The RCE study of this HPA is also presented in section 5.5 (Results).

Fig. 71: Schematic of the FLL357ME HPA matched for max small-signal gain.

Fig. 72: Layout and photo of the FLL357ME HPA matched for max small-signal gain.

5.3.2. Achieving Maximum Power via Passive Load Pull

Although the gain of the HPA has been achieved but the P1dB of the HPA was only 33.38dBm, due to the fact that impedance matched for maximum transducer gain might not be matched to the load impedance for optimum output power. To locate the actual load impedance needed for optimum output power, the Maury Microwave slide screw tuner (model 2640D1) was connected at the output of the HPA prior to the power meter. The complete setup is shown in Fig. 73. A driver amplifier was used to ensure that the test input power to the HPA is consistent at 23dBm at 2.211GHz.

Fig. 73: Setup for passive load pull.

The procedure of the design is as follows:

Step 1: The HPA was biased at $V_{DS}=10V$, $0.54A$, $V_{GS}=-1.3V$ (manufacturer's recommendation). Driving the HPA with the appropriate test power, the tuning stubs and slider of the tuner were adjusted until maximum power was observed on power meter.

Step 2: Find out the phase delay of the SMA connector at the design frequency using VNA. The phase delay of the SMA connector is approximately 32.23° at 2.211GHz. Apply the reference plane on VNA to de-embed the effect of the SMA connectors and then connect the output matching circuit of the HPA together with the tuner to the VNA as shown in Fig. 74. With the effect of the SMA connector de-embedded, the measured load impedance of the HPA device was found to be approximately 6.51 Ohm at 2.211GHz, denoted in blue in Fig. 80.

Fig. 74: Setup to measure the required output load impedance for the HPA device.

Step 3: Record the load impedance displayed on the Smith Chart at the design frequency. Based on the load impedance measured, optimize the output matching network for this load impedance using design software. In Fig. 80, it can be seen

that the amplifier was initially matched to $20.94+3.37j$ Ohm when it is matched for maximum power gain. By optimizing the lengths of the output matching elements, TL24 and TL25 (in Fig. 71), the matched impedance is shifted from $20.94+3.37j$ Ohm to 6.51 Ohm at 2.211GHz. When performing single-stub tuning [44] in ADS, varying the lengths of TL24 and TL25 is as if transforming the impedance from one point to another on a Smith chart. Optimized length for TL24 and TL25 is 3.92mm and 15.7mm respectively. It is shown in Fig. 80 that the output matching circuit has been matched to the measured load impedance.

Step 4: The output matching network optimized for optimum output power was then integrated into the final HPA design. The final HPA layout and photo is shown in Fig. 75. The P1dB measured is 35.35dBm, closed to the manufacturer's specification of 34.98dBm.

Fig. 75: Layout and photo of FLL357ME HPA circuit optimized for output power.

Based on the same optimized output matching network as in Fig. 75, another HPA device from the same manufacturer (with test data of P1dB at 35.37dBm) was used for the second HPA circuit. The output power of the HPA tested with CW was 34.6dBm. By repeating step 1 to 3, it has been found that for the second HPA device, the optimum load impedance was 10.6ohm instead of 6.51ohm (optimum load impedance for the first HPA device). Connecting the PCB at the HPA output to a 50 ohm termination, the load impedance of the second HPA circuit was

6.32ohm initially as shown in Fig. 81. Since the load impedance measured is higher, the length of the open circuit stub should be shortened. The length of the stub was trimmed by approximately 3.5mm and the load impedance measured on the smith chart was $11.48 -j 4.6\text{ohm}$. Through optimization in ADS, the length of TL25 (in Fig. 71) should be shortened from 15.7mm to 12.2mm for second HPA device. If lower impedance is required, the open circuit stub can be extended by soldering a small piece of copper tape to the rectangular patches next to the stub. The measurement and RCE study of this second HPA are presented in section 5.5.

5.4. Equipment Setup for RCE Study

To understand the non-linear distortion introduced by the amplifier, the VSG E4438C and the VSA E4404B with modulation analysis personality installed were used to generate and analyze the digitally modulated signals. These equipment are different from those used for X-band HPA testing. Although the demodulation bandwidth of E4404B VSA is limited to 10MHz but it has a simpler configuration comparing to the PSA E4440A. The PSG 8267D VSG can generate vector RF up to 44GHz but the VSG E4438C (up to 6GHz) can generate better quality of vector RF. For comparison purpose, the average EVM and PE of 25Msps QPSK vector RF generated by the PSG 8267D is 1.6%, 0.65° at 8.3GHz and 0.6%, 0.2° at 2.211GHz by the E4438C VSG. To remove the impairments introduced by the VSG, the relative EVM and PE are defined in equations (11) (12). The parameters set on the VSG and VSA are listed in Table 9.

Parameters	VSG E4438C Baseband I/Q setting	E4404B VSA Demodulation setting
Frequency	2.211GHz	2.211GHz
Modulation Type	BPSK	BPSK
Symbol Rate	1Msps	1Msps
Filter Type	Root Nyquist	-
Measured Filter	-	Root Nyquist
Reference Filter	-	Nyquist

Filter Alpha	0.35	0.35
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Table 9: Parameters set on the VSG and VSA for S-band PA testing.

5.5. Results

Fig. 76 shows the measured and simulated S-parameters of the amplifier designed with 50 ohms lines at the input and output (no matching circuit).

Fig. 76: Comparison of FLL357ME S-parameters and K value measured and provided by manufacturer.

5.5.1. Measurements of Amplifier Designed for Maximum Gain

Fig. 77 shows the small signal S-parameters simulated and measured for HPA matched for maximum power gain.

Fig. 77: Simulated and measured S-parameters of the FLL357ME HPA matched for maximum small signal gain.

As shown in Fig. 78 (a), the P1dB of the HPA measured at 2.211GHz is approximately 33.4dBm when tested with CW. Comparing the output power measured with modulated BPSK signal to that of CW, the power level is approximately 1dB lower. The EVM and PE measured are shown in Fig. 79.

Fig. 78: P1dB and PAE of FLL357ME HPA matched for maximum small signal gain at 2.211GHz.

Fig. 79: EVM and PE of FLL357ME HPA measured with BPSK signal. (Matched for maximum small signal gain at 2.211GHz)

5.5.2. Measurements of Amplifier Matched for Max Power (via Load Pull)

Fig. 80 shows the load impedance of first HPA device matched at different conditions. This explains why the P1dB measured for the HPA optimized for small signals (33.38dBm) is below the specification due to mismatch of load impedance.

Fig. 80: Measured and simulated load impedances for optimum output power and max transducer gain.

For the second HPA devices, it is shown in Fig. 81 that the original output matching circuit was matched to $6.32 + j0.39$ Ohm. After the length of the stub was trimmed by approximately 3.5mm, the output matching circuit was matched to $11.48 - j4.6$ Ohm, as shown on the smith chart (Fig. 81).

Fig. 81: Load impedance of 2nd FLL357ME device measured before and after tuning.

After trimming the output open circuit stub of the second HPA, the measured P1dB tested with CW is now 35.42dBm with a PAE of 52 percent, as shown in Fig. 82 (a). Fig. 82 (b) shows the output power and PAE tested with modulated BPSK signal. The power is slightly lower than that of CW. Even though high output power and PAE are achieved, but the EVM and PE also increase significantly as shown in Fig. 83. Depending on the system specifications, one can decide the trade-off between the tolerable impairment and desired output power based on the result shown. All numerical test data is available in Appendix L.

Fig. 82: P1dB and PAE of second FLL357ME HPA matched for power at 2.211GHz.

Fig. 83: EVM and PE of FLL357ME HPA measured with BPSK signal. (Matched for power at 2.211GHz)

5.6. Discussion

Table 10 summarizes the performance of the measured and manufacturer's test data for the two HPA devices evaluated. The test data provided by the manufacturer are normally tested with CW. Therefore the measured data tested with CW are comparable to the manufacturer's data. It is also useful to note that the optimum load impedances for maximum power are different from device to device.

Measurement	1 st HPA device performance	2 nd HPA device performance
PAE at P1dB (%)	37.7	52.13
P1dB (dBm)	33.45	35.42
G1dB (dB)	12.00	11.40
Load Impedance Measured	6.51	10.6
Manufacturer's Test Data		
P1dB (dBm)	34.98	35.37
G1dB (dB)	11.73	12.10

Table 10: Comparison of test data from manufacturer and the measured results of the two FLL357ME HPA devices measured with CW.

5.7. Conclusion

HPA designed using complex conjugate impedance matching technique yields maximum power gain but not maximum power of a HPA device. However, it has been shown how to leverage on this technique to achieve the power gain before optimizing it for optimum output power. The approach described here is easier to implement with minimal effort even without the complete load pull system. In the next chapter, similar design approach will be used to design a medium PA to achieve better linearity under predetermined conditions.

6. Design of Linear S-band Medium PA with High PAE

6.1. Introduction

To ensure that the last stage S-band HPA amplifies the signal to the desired output level, a medium power driver amplifier is required as shown in Fig. 18. The goal of the driver amplifier design is to achieve gain of 12dB and output power of 25dBm at 2.211GHz. There are many commercially available medium PAs, which do not need sophisticated matching circuit. However, it has been shown that driving the amplifier near to P1dB will introduce significant distortion to the modulated signal in the previous chapters. By using a medium PA with higher P1dB may solve the problem but the HPA device will definitely consume more DC power. In this chapter, a novel approach on how to design a linear medium PA easily without sophisticated PA linearization is presented.

First, the performance of two internally matched commercial medium PA: 1) WJ Communications gain block, WJAH102, with a gain of 12dB and P1dB at 25dBm 2) Hittite HBT MMI, HMC454ST89, with a gain of 12.5dB and P1dB at 27dBm, were measured. Next the performances of both medium PA were compared to the medium PA (GaAs FET FLL177ME) designed based on the novel approach. The PCB substrate used for this medium PA is Roger RO4003, similar to the substrate used for X-band HPA circuits.

6.2. Design Concept

The medium PA device, Fujitsu GaAs FET FLL177ME, is first designed for maximum power according to the steps described in the previous chapter. Then the drain current of the PA device is adjusted to locate the PA load impedance, which

gives the highest linear output power. Basically, the drain current is controlled by the applied gate voltage as shown in Fig. 84. The V_{DS} is fixed at 10V, when the gate voltage varies, the drain current and the load impedance vary too. As the output matching circuit is already fixed, changing the gate voltage will vary the load impedance of the PA device. This approach is as if fine tuning the load impedance for better linearity.

Fig. 84: I_{DS} vs V_{DS} curve for FLL177ME device.

6.3. Design Procedures

To understand the non-linear characteristics of the amplifiers, both WJAH102 and HMC454ST89 medium PA were tested using modulated BPSK signal. The modulated signal and demodulation settings are similar to that of Table 9. Fig. 91 and Fig. 92 show the output power and PAE measured for respective medium PAs and the plot of EVM and PE against the input test power. It is again shown that the amplifier operating near P1dB region distort the modulated signal significantly.

Fig. 91 (b) and Fig. 92 (b) show that the EVM $< 2\%$ and PE $< 1^\circ$ when the amplifiers are operating greater than 4dB down from the P1dB. Deducing from the RCE measurements of these two commercial medium PAs, in order to achieve low non-linear distortion (EVM $< 2\%$ and PE $< 1^\circ$), it is therefore recommended to use PA device with P1dB that is 5dB higher than the actual output power requirement. In

this case, Fujitsu FLL177ME is selected, which has a minimum output power of 31.5dBm. FLL177ME has a linear gain of 8.7dB without impedance matching.

6.3.1. Design of Medium PA Pre-matched for Power Gain

Based on small signal S-parameters provided by the manufacturer, the PA device was first matched for power gain at 2.211GHz by applying conjugate impedance matching technique. The schematic of the PA pre-matched for gain is shown in Fig. 85. The DC bias circuit was designed based on the proposed bias network in [40]. It can be seen in Fig. 86 that the gain simulated is well matched at 2.211GHz.

Fig. 85: Schematic of the pre-matched medium PA.

Fig. 86: S-Parameters simulated for Medium PA matched for maximum gain.

The layout and prototype developed is shown in Fig. 87. The performance of the pre-matched PA is shown in Fig. 93. As expected, since the PA is only matched for gain, the P1dB is lower leading to greater EVM and PE measured as the input power increases.

Fig. 87: PCB layout and photo of the pre-matched medium PA.

6.3.2. Design of Medium PA Matched for Optimum Output Power

Following the design steps described in section 5.3.2, the Maury Microwave slide screw tuner was cascaded after the pre-matched PA to locate the optimum load impedance of the medium PA. When performing load pull, the gate voltage can be varied accordingly to limit or lower the drain current and record the optimum load impedance at 2.211GHz. By using small the signal S-parameter simulation in ADS, the output matching network was optimized to match to the measured load impedance. The lengths of TL21 and TL22 were optimized from 10.34mm and 15.4mm (in Fig. 85) respectively to 11.96mm and 6.35mm (in Fig. 88). Fig. 89 shows the small signal S-parameters simulated from the optimized medium PA. It can be seen that the gain reduces by 2dB and the output matching (S_{22}) reduces to -5dB. These changes were expected because the medium PA has been matched for optimum output power instead of maximum power gain.

Fig. 88: Schematic of medium PA FLL177ME matched to optimum load impedance.

Fig. 89: S-Parameters simulated based after optimized for better linearity.
Output is not match after tuning.

The layout and prototype of the optimized medium PA is shown in Fig. 90. Additional rectangular patches were added next to the output shunt stub for on-board tuning, if necessary. With the optimized output matching network, the overall performance of the medium PA improves significantly as shown in Fig. 94. The medium PA biased at V_{GS} of -1.4V has higher linear gain and output power than V_{GS} of -2V. However, the medium PA biased at V_{GS} of -2V introduces less non-linear distortion and has higher PAE.

Fig. 90: PCB of medium PA FLL177ME matched to optimum load impedance.

To validate the consistency of the performance of medium PA based on such design approach, another medium PA device from the same manufacturer was developed. The measured result is shown in Fig. 95.

6.4. Results

6.4.1. EVM Measurement of Two Commercial Medium PAs

Fig. 91: Performance of WJAH102 measured at 2.211GHz.

(a) P_{out} and PAE (P_{1dB} at ~26.5dBm)

(b) EVM and PE

Fig. 92: Performance of HMC454ST89 measured at 2.211GHz.

6.4.2. Performance of Medium PA Pre-matched for Power Gain

(a) Output power and PAE

(b) EVM and PE

Fig. 93: Performance of pre-matched medium PA (FLL177ME).

6.4.3. Performance of Medium PA Matched for Optimum Output Power

Fig. 94: Performance of optimized medium PA FLL177ME biased at V_{GS} of -1.4V and -2V and measured at 2.211GHz.

Fig. 95: Performance of 2nd optimized medium PA FLL177ME biased at V_{GS} of -1.4V and -2V and measured at 2.21 GHz.

6.5. Discussion

Fig. 95 shows that the linear gain and output power for the second medium PA is slightly higher and the EVM and PE measured remain consistent. Therefore, it can be concluded that both medium PA biased at -1.4V has high output power and gain with degraded linearity. With slight degradation of output power and gain, both PA biased at V_{GS} of -2V has a better linearity, with EVM less than 2% and PE less than 1° at output power of approximately 29.5dBm and PAE of 47%.

Table 11 summarizes the performance of all the medium PAs tested with 1Mps modulated BPSK signal. It is shown that the maximum linear power of FLL177ME is approximately 2 to 3 dB below the P1dB.

Measurements	WJ AH102	Hittite HMC454ST89	Fujitsu FLL177ME (1)	Fujitsu FLL177ME (2)
P1dB (dBm)	25.30	26.22	31.45	31.51
PAE at Pout of 25dBm (%)	18.1	32.9	29.1	29.5
DC Power at 25dBm (W)	1.7 (10V, 0.17A)	0.95 (5V, 0.19A)	1.1 (10V, 0.11A)	1.1 (10V, 0.11A)
Linear Gain (dB)	12.1	12.5	11.7	14.7
Max. Linear Pout (dBm)*	22.50	24.10	29.95	29.77
PAE at Max. Linear Pout (%)	9.05	28.3	46.73	50.93

* Max. Linear Pout is defined as measured EVM <2% and PE <1° for medium PA

Table 11: Performance comparison of the medium PAs measured at 2.211GHz.

6.6. Conclusion

To achieve an output power of 25dBm, the design started of with WJAH102 and HMC454ST89 operating at P1dB of 25dBm and 27dBm respectively. The EVM measured was >5% at 25dBm. If we operate the amplifiers 4dB down or more from the P1dB, the EVM improved to <2%. A new amplifier based on FLL177ME, with

minimum P1dB of 31.5dBm was developed. Operating the FLL177ME with 5dB back off from P1dB, the PAE is almost the same as HMC454ST89 but the EVM improved to <1.5%. Based on this design approach, it has been shown how a linear medium PA can be achieved easily without linearizing the amplifier. All numerical test data is available in Appendix M.

7. Conclusion and Recommendations

In a low-cost LEO satellite mission, the subsystems are usually developed using COTS components with heritage instead of using high grade or space qualified components. Due to limited power supply, volume and mass of a micro-satellite, the on-board RF module are usually designed such that the space occupation of the circuitries are small to reduce the module mass and the DC power consumption is as low as possible. This principle has been extensively applied in the designs accomplished in this project.

The project focuses on developing the RF sub-circuits in the XBT and TT&C subsystems. The developments of the subsystems are usually built upon previous mission. The basic design parameters of these subsystems are derived directly from the mission requirements such as near real time high speed downlink in the XBT and omni-directional reception and transmission in the TT&C subsystem. The subsequent requirement of transmit power are derived from the link margin, data rate, bandwidth and operating frequency. To fulfil the requirements of X-Sat microwave link budget, the PAs play an important role in amplifying the signal to the required output power. Traveling wave tube amplifier (TWTA) and SSPA are the most commonly used in high rate transmitter of LEO satellite. As presented in the downlink budget analyses, the required output power is approximately 10W for XBT and 3W for TT&C transmitter. At these output power level, the SSPA is easier to develop and more cost effective than TWTA.

The thesis starts with a discussion on the microwave transmission systems of X-Sat and factors affecting their performance. The direct up-conversion is a common architecture used in most of the wireless PAN/LAN/MAN today as only one LO is required. The information is directly modulated and transmitted on single carrier

frequency. In the double up-conversion architecture, the information is first modulated on a carrier frequency and subsequently up-converted to a higher frequency prior to transmission. The pros and cons of both architectures are highlighted. Using a commercial I/Q modulator package and a phase locked DRO, an **X-band direct QPSK up-conversion module** is developed (in Chapter 3).

Non-linear microwave circuits such as HPA, mixer and modulator introduce non-linear distortions. In the thesis, the impairments introduced by the modulator and HPA were investigated based on the measured numerical figures of RMS EVM (EVM) and RMS phase error (PE). **As a good reference for the RF designer, the modulated signal should be used to test the non-linear RF sub-circuits instead of CW because it has been shown that the actual impact can only be observed under this test condition.**

To ensure sufficient link budget of a microwave link, the HPA is one of the essential sub-circuits in amplifying the modulated signal prior to the transmission. In the design of a high frequency HPA, the goal is to achieve sufficient power gain, output power and high PAE at the desired frequency. However, to achieve optimum electrical performance from a HPA, there are many design considerations that need to be taken into account such as impedance matching, DC bias network design, grounding and heat sinking of the HPA device. Nowadays most semiconductor manufacturers produce internally matched HPA devices at X-band to shorten the development time. Even though the device is internally matched, ignorance of these design blocks mentioned above may lead to the device breakdown or oscillations. The degradations are primarily owing to insufficient device grounding and severe RF signal leakage to the bias network. In Chapter 4, the **bias network and a novel simple microwave**

power divider were designed with primary requirement of **low insertion loss** at the operating frequency and as **small physical dimension** as possible. Taking the practical design considerations into account, a 2W MMIC HPA and a 10W HPA were designed and evaluated separately prior to integrating them with a RF detector circuit and an isolator at the HPA output. Next, two **high power and high gain cascade HPA modules** were developed. Due to lower insertion loss of the novel power divider, the **PAE of the full SSPA module** also improved. The HPA housing dimension is particularly vital as improper design may lead to the cavity resonance. **As a good reference for the HPA designer, a few practical approaches on how to damp the cavity resonance and the verification of cavity resonance via electromagnetic simulation are also reported.**

On the contrary, the HPA device operating at S-band is usually not matched to 50 ohm. Large-signal S-parameters are usually used to design the impedance matching networks. Since the large-signal S-parameters of the HPA device are normally not provided by the manufacturer, the characteristics of a HPA device can be accurately extracted from load pull measurement as described in [45]. However the setup and measurement procedures are rather tedious and time consuming. In addition, the output load impedance of the HPA device is also not consistent from a chip to another. Even though the large-signal S-parameter for a device can be accurately extracted with load pull experiment, the matching network designed will not necessarily match to the desired output load impedance for another device. Further constraints are that the test power generated from a commercial VNA is normally low (10dBm) while maximum input power to the VNA is limited to 1W (30dBm). Therefore additional equipment is needed to extract the large-signal S-parameter.

In Chapter 5, **a novel and flexible technique is demonstrated on how to design a HPA based on small signal S-parameters**. The approach is to firstly match a commercial HPA device for gain by using small signal S-parameters provided by the manufacturer, followed by passive load pull to achieve 3.5W of output power and PAE of over 50%. Based on this approach, it is shown that the output load impedance can be easily located on the smith chart for subsequent on-board tuning. **Even without a complete load pull system, this novel approach is easy and flexible to implement with minimal effort** especially when the device is cascaded with other microwave circuit. Characterization of HPA device is impossible using this method. However, it has been shown how a HPA can be designed and implemented with just a VNA and a slide screw tuner.

The fundamental requirements in a PA design are to achieve high output power at 1dB compression point (P_{1dB}), reasonable power gain and excellent PAE at the design frequency. However the challenge arises when the designer has to simultaneously match the amplifier for gain and power while minimizing non-linear distortion. It is shown that the non-linearity of PA distorts the quality of a modulated signal. Sometime, the linearization of a PA is implemented to minimize non-linear distortion while maintaining good PAE. Hence the PA design often involves the trade-off between linearity and power efficiency. The PA linearization using feedforward techniques [46]-[49] can be very tedious and time consuming. Hence, **a novel practical approach on how to achieve high power and good PAE of a class AB medium PA is shown in Chapter 6 without performing PA linearization**. Given an output power requirement of 25dBm, a PA device that has P_{1dB} of 5dB higher than the specification should be selected. The PA device with higher P_{1dB} is selected so that the device is matched for high output power at the beginning. After it is matched

for power, the PA is operated at lower drain current. In Chapter 6, a simple design trade-off is shown on how to minimize non-linear distortion of a medium PA and achieving excellent PAE, without significant degradation on the power gain and output power. The medium PA device selected has a minimum P1dB of 31.5dBm. The medium PA design is accomplished based on the small signal S-parameters analysis mentioned above. The medium PA device is first matched for gain, followed by passive load pull of the pre-matched amplifier using sliding screw tuner to achieve high output power. It is shown that the PA operating at lower drain current introduces minimum distortion to the modulated signal based on the figures of merit of EVM and PE measured. Therefore, linearization of PA can be avoided with this method. For PA with greater output power, the proposed approach can be applied but it is recommended to epoxy the PCBs and HPA devices directly onto the aluminium housing using thermally and electrically conductive epoxy.

In this research project, **a few simple and novel approaches/techniques have been demonstrated and proven with the real hardware** on how to design a power divider, impedance matching of amplifiers as well as optimizing it for linear output power. Most of the RF sub-circuits were successfully designed. They have been used and further developed into complete modules in the Satellite Engineering Centre, CREST. The X-band SSPA modules developed is the engineering model for XBT; The design of S-band medium PA, FLL177ME, and the last stage HPA, FLL357ME, have been cascaded as S-band HPA module in the TT&C system.

7.1. Recommendations for Further Research

- ❖ Owing to the the structure of micro-satellite was not completely defined during this research period, the heat conduction from the SSPA module to the satellite chassis were not studied analytically or experimentally. As the X-band SSPA module dissipates a large amount of heat, a heatsink (125mm x 250mm x 50mm) was placed under the module during the measurement. Under such test condition, the performance of the SSPA does not degrade significantly over a period of 3-5 minutes at room temperature. However, further study should be carried out analytically using finite element analysis tools or experimentally using thermal vacuum chamber to investigate the heat conduction of SSPA module mounted on a representative satellite chassis.

- ❖ Although the desired RF performance of the X-band SSPA module was achieved, the temperature cycle and vibration tests were not carried out because the test specifications and methodologies are still under development during this research period. To examine whether the SSPA Engineering Model could be further developed into a Qualifying Model, one area of future work is to carry out environmental tests after the test methodologies have been defined and agreed by the Thermal and Structural Design Group.

- ❖ Even though a number of simulations have been shown, a system level simulation was not carried out because the non-linear models of the HPA devices were not available in the ADS library. Small signal S-parameters of an amplifier or passive component can be easily represented by the touchstone file format. However the power at compression region and non-linear characteristics of the PA cannot be captured in the touchstone format. Furthermore, modelling of a

HPA device requires extensive measurements at different drive power and bias conditions over a frequency range to accurately extract all the parameters and associated parasitic. Another area of future work is to model the amplifier behaviours in ADS. Driving BPSK or QPSK signal to the input of HPA model, it would be interesting to compare the results reported in this thesis and simulated from Ptolemy in ADS.

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Appendix A: Data Sheet of Toshiba TMD0708-02

TOSHIBA

**MICROWAVE SEMICONDUCTOR
TECHNICAL DATA**

POWER GaAs MMIC

TMD0708-2

Features:

- HIGH POWER
 $P_{1dB} = 33 \text{ dBm}$ at 7.1 to 8.5 GHz
- BROAD BAND INTERNALLY MATCHED
- HIGH GAIN
 $G_{1dB} = 22 \text{ dB}$ at 7.1 to 8.5 GHz
- HERMETICALLY SEALED PACKAGE

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

CHARACTERISTICS	SYMBOL	UNIT	RATINGS
DRAIN SUPPLY VOLTAGE	V_{DD}	V	15
GATE SUPPLY VOLTAGE	V_{GG}	V	-10
INPUT POWER	P_{in}	W	0.1
PLANE TEMPERATURE	T_f	$^\circ\text{C}$	-30 ~ +80
STORAGE TEMPERATURE	T_{stg}	$^\circ\text{C}$	-65 ~ +175

RF CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

CHARACTERISTICS	SYMBOL	CONDITION	UNIT	MIN.	TYP.	MAX.
Output Power at 1 dB Gain Compression Point	P_{1dB}	$V_{DD1} = V_{DD2} = V_{DD3} = 10\text{V}$	dBm	32.0	33.0	—
Power Gain at 1 dB Gain Compression Point	G_{1dB}	$V_{GG} = -5 \text{ V}$ $f = 7.1\text{--}8.5 \text{ GHz}$	dB	20.0	22.0	—
Drain Current	$I_{DD} *$		A	—	1.70	2.00
Input VSWR	V_{SWRi}		—	—	—	3.0

* $I_{DD} = I_{DD1} + I_{DD2} + I_{DD3}$

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★ The information contained herein may be changed without prior notice. It is therefore advisable to contact TOSHIBA before proceeding with the design of equipment incorporating this product.

Appendix B: Data Sheet of Fujitsu FMM5057VF

FMM5057VF

7.1-8.5GHz Power Amplifier MMIC

FEATURES

- High Output Power: 34.0dBm(typ.)
- High Linear Gain: 26.0dB(typ.)
- Low VSWR
- Broad Band: 7.1 ~ 8.5GHz
- Impedance Matched $Z_{in}/Z_{out} = 50\Omega$
- Small Hermetic Metal-Ceramic Package(VF)

DESCRIPTION

The FMM5057VF is a MMIC amplifier that contains a four-stage amplifier, internally matched, for standard communications band in the 7.1 to 8.5GHz frequency range. Fujitsu's stringent Quality Assurance Program assures the highest reliability and consistent performance.

ABSOLUTE MAXIMUM RATINGS (Case Temperature $T_c=25^\circ\text{C}$)

Item	Symbol	Rating	Unit
DC Input Voltage	V_{DD}	12	V
DC Input Voltage	V_{GG}	-7	V
Input Power	P_{in}	14	dBm
Storage Temperature	T_{stg}	-55 to +125	$^\circ\text{C}$

Recommended Operating Condition

Item	Symbol	Condition	Unit
DC Input Voltage at $T_c=25^\circ\text{C}$	V_{DD}	10	V
Input Power at $T_c=25^\circ\text{C}$	P_{in}	12	dBm
DC Input Current at $T_c=25^\circ\text{C}$	I_{DD}	≤ 1200	mA
Operating Case Temperature	T_c	-40 to +85	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS (Case Temperature $T_c=25^\circ\text{C}$)

Item	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Frequency Range	f		7.1 - 8.5			GHz
Output Power at 1dB G.C.P.	P_{1dB}	$V_{DD}=10V, V_{GG}=-5V$ $f=7.1 \text{ to } 8.5\text{GHz}$	32.0	34.0	-	dBm
Power Gain at 1dB G.C.P.	G _{1dB}		23.0	26.0	-	dB
Gain Flatness	ΔG		-	2.4	4.0	dB
Input VSWR	VSWR _i		-	2 : 1	2.5 : 1	-
Output VSWR	VSWR _o		-	2 : 1	-	-
DC Input Current	I_{DD}	$V_{DD}=10V, V_{GG}=-5V$	-	1100	1200	mA
DC Input Current	I_{GG}		-	5.0	15.0	mA
Channel Temperature Rise	ΔT_{ch}		-	50	-	$^\circ\text{C}$

CASE STYLE: VF

Note: G_{1dB} is referenced to Linear G₀ measured at $P_{in}=3\text{dBm}$.

G.C.P.: Gain Compression Point

ESD	Class 0	- 199 V
-----	---------	---------

Note: Based on EIAJ ED-4701 C-111A(C=100pF, R=1.5k Ω)

FMM5057VF

7.1-8.5GHz Power Amplifier MMIC

OUTPUT POWER vs. FREQUENCY

VDD=10V, VGG=-5V

OUTPUT POWER, POWER ADDED EFFICIENCY vs. INPUT POWER

VDD=10V, VGG=-5V

IMD vs. OUTPUT POWER

VDD=10V, VGG=-5V

VSWR vs. FREQUENCY

VDD=10V, VGG=-5V

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FMM5057VF

7.1-8.5GHz Power Amplifier MMIC

OUTPUT POWER, POWER ADDED EFFICIENCY
vs. INPUT POWER

OUTPUT POWER, POWER ADDED EFFICIENCY
vs. INPUT POWER

DRAIN CURRENT vs OUTPUT POWER

OUTPUT POWER vs. GATE VOLTAGE

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FMM5057VF

7.1-8.5GHz Power Amplifier MMIC

■ Package Out Line

Appendix C: Data Sheet of Fujitsu FLM7785-12F

FLM7785-12F

C-Band Internally Matched FET

FEATURES

- High Output Power: $P_{1dB} = 41.5\text{dBm}$ (Typ.)
- High Gain: $G_{1dB} = 8.5\text{dB}$ (Typ.)
- High PAE: $\eta_{add} = 34\%$ (Typ.)
- Low $IM_3 = -46\text{dBc}$ @ $P_o = 30.5\text{dBm}$
- Broad Band: 7.7 ~ 8.5GHz
- Impedance Matched $Z_{in}/Z_{out} = 50\Omega$
- Hermetically Sealed

DESCRIPTION

The FLM7785-12F is a power GaAs FET that is internally matched for standard communication bands to provide optimum power and gain in a 50 ohm system.

Fujitsu's stringent Quality Assurance Program assures the highest reliability and consistent performance.

ABSOLUTE MAXIMUM RATING (Ambient Temperature $T_a = 25^\circ\text{C}$)

Item	Symbol	Condition	Rating	Unit
Drain-Source Voltage	V_{DS}		15	V
Gate-Source Voltage	V_{GS}		-5	V
Total Power Dissipation	P_T	$T_C = 25^\circ\text{C}$	57.6	W
Storage Temperature	T_{stg}		-65 to +175	$^\circ\text{C}$
Channel Temperature	T_{ch}		175	$^\circ\text{C}$

Fujitsu recommends the following conditions for the reliable operation of GaAs FETs:

1. The drain-source operating voltage (V_{DS}) should not exceed 10 volts.
2. The forward and reverse gate currents should not exceed 32.0 and -5.6 mA respectively with gate resistance of 50Ω .

ELECTRICAL CHARACTERISTICS (Ambient Temperature $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Saturated Drain Current	I_{DSS}	$V_{DS} = 5\text{V}, V_{GS} = 0\text{V}$	-	5400	8100	mA
Transconductance	g_m	$V_{DS} = 5\text{V}, I_{DS} = 2400\text{mA}$	-	5000	-	mS
Pinch-off Voltage	V_p	$V_{DS} = 5\text{V}, I_{DS} = 240\text{mA}$	-0.5	-1.5	-3.0	V
Gate Source Breakdown Voltage	V_{GSO}	$I_{GS} = -300\mu\text{A}$	-5	-	-	V
Output Power at 1dB G.C.P.	P_{1dB}	$V_{DS} = 10\text{V},$ $I_{DS} = 0.65 I_{DSS}$ (Typ.), $f = 7.7 \sim 8.5\text{GHz},$ $Z_S = Z_L = 50\text{ohm}$	40.5	41.5	-	dBm
Power Gain at 1dB G.C.P.	G_{1dB}		7.5	8.5	-	dB
Drain Current	I_{dsr}		-	3500	4500	mA
Power-added Efficiency	η_{add}		-	34	-	%
Gain Flatness	ΔG		-	-	± 0.6	dB
3rd Order Intermodulation Distortion	IM_3	$f = 8.5\text{GHz}, \Delta f = 10\text{MHz}$ 2-Tone Test $P_{out} = 30.5\text{dBm S.C.L.}$	-44	-46	-	dBc
Thermal Resistance	R_{th}	Channel to Case	-	2.3	2.6	$^\circ\text{C/W}$
Channel Temperature Rise	ΔT_{ch}	$10\text{V} \times I_{dsr} \times R_{th}$	-	-	80	$^\circ\text{C}$

CASE STYLE: IK

G.C.P.: Gain Compression Point, S.C.L.: Single Carrier Level

FLM7785-12F

C-Band Internally Matched FET

POWER DERATING CURVE

OUTPUT POWER & IM₃ vs. INPUT POWER

OUTPUT POWER vs. FREQUENCY

OUTPUT POWER vs. INPUT POWER

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FLM7785-12F

C-Band Internally Matched FET

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Appendix D: Data Sheet of Fujitsu FLL177ME

FLL177ME

L-Band Medium & High Power GaAs FET

FEATURES

- High Output Power: $P_{1dB}=32.5\text{dBm}$ (Typ.)
- High Gain: $G_{1dB}=12.5\text{dB}$ (Typ.)
- High PAE: $\eta_{add}=46\%$ (Typ.)
- Proven Reliability
- Hermetically Sealed Package

DESCRIPTION

The FLL177ME is a Power GaAs FET that is specifically designed to provide high power at L-Band frequencies with gain, linearity and efficiency superior to that of silicon devices. The performance in multitone environments for Class AB operation make them ideally suited for base station applications. This device is assembled in hermetic metal/ceramic package.

Fujitsu's stringent Quality Assurance Program assures the highest reliability and consistent performance.

ABSOLUTE MAXIMUM RATING (Ambient Temperature $T_a=25^\circ\text{C}$)

Item	Symbol	Condition	Rating	Unit
Drain-Source Voltage	V_{DS}		15	V
Gate-Source Voltage	V_{GS}		-5	V
Total Power Dissipation	P_t	$T_C = 25^\circ\text{C}$	7.5	W
Storage Temperature	T_{stg}		-65 to +175	$^\circ\text{C}$
Channel Temperature	T_{ch}		175	$^\circ\text{C}$

Fujitsu recommends the following conditions for the reliable operation of GaAs FETs:

1. The drain-source operating voltage (V_{DS}) should not exceed 10 volts.
2. The forward and reverse gate currents should not exceed 9.6 and -1.0 mA respectively with gate resistance of 200Ω .
3. The operating channel temperature (T_{ch}) should not exceed 145°C .

ELECTRICAL CHARACTERISTICS (Ambient Temperature $T_a=25^\circ\text{C}$)

Item	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Saturated Drain Current	I_{DSS}	$V_{DS} = 5\text{V}, V_{GS} = 0\text{V}$	-	600	900	mA
Transconductance	g_m	$V_{DS} = 5\text{V}, I_{DS} = 400\text{mA}$	-	300	-	mS
Pinch-off Voltage	V_p	$V_{DS} = 5\text{V}, I_{DS} = 30\text{mA}$	-1.0	-2.0	-3.5	V
Gate Source Breakdown Voltage	V_{GSO}	$I_{GS} = -30\mu\text{A}$	-5	-	-	V
Output Power at 1dB G.C.P.	P_{1dB}	$V_{DS} = 10\text{V}$ $I_{DS} \approx 0.6I_{DSS}$ (Typ.), $f = 2.3\text{GHz}$	31.5	32.5	-	dBm
Power Gain at 1dB G.C.P.	G_{1dB}		11.5	12.5	-	dB
Power-added Efficiency	η_{add}		-	46	-	%
Thermal Resistance	R_{th}	Channel to Case	-	15	20	$^\circ\text{C/W}$

CASE STYLE: ME

G.C.P.: Gain Compression Point

FLL177ME

L-Band Medium & High Power GaAs FET

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Appendix E: Data Sheet of Fujitsu FLL357ME

FLL357ME

L-Band Medium & High Power GaAs FET

FEATURES

- High Output Power: $P_{1dB}=35.5\text{dBm}$ (Typ.)
- High Gain: $G_{1dB}=11.5\text{dB}$ (Typ.)
- High PAE: $\eta_{add}=46\%$ (Typ.)
- Proven Reliability
- Hermetically Sealed Package

DESCRIPTION

The FLL357ME is a Power GaAs FET that is specifically designed to provide high power at L-Band frequencies with gain, linearity and efficiency superior to that of silicon devices. The performance in multitone environments for Class AB operation make them ideally suited for base station applications. This device is assembled in hermetic metal/ceramic package.

Fujitsu's stringent Quality Assurance Program assures the highest reliability and consistent performance.

ABSOLUTE MAXIMUM RATING (Ambient Temperature $T_a=25^\circ\text{C}$)

Item	Symbol	Condition	Rating	Unit
Drain-Source Voltage	V_{DS}		15	V
Gate-Source Voltage	V_{GS}		-5	V
Total Power Dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	15	W
Storage Temperature	T_{stg}		-65 to +175	$^\circ\text{C}$
Channel Temperature	T_{ch}		175	$^\circ\text{C}$

Fujitsu recommends the following conditions for the reliable operation of GaAs FETs:

1. The drain-source operating voltage (V_{DS}) should not exceed 10 volts.
2. The forward and reverse gate currents should not exceed 19.4 and -2.0 mA respectively with gate resistance of 100Ω.
3. The operating channel temperature (T_{ch}) should not exceed 145 $^\circ\text{C}$.

ELECTRICAL CHARACTERISTICS (Ambient Temperature $T_a=25^\circ\text{C}$)

Item	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Saturated Drain Current	I_{DSS}	$V_{DS} = 5\text{V}, V_{GS} = 0\text{V}$	-	1200	1800	mA
Transconductance	g_m	$V_{DS} = 5\text{V}, I_{DS} = 800\text{mA}$	-	600	-	mS
Pinch-off Voltage	V_p	$V_{DS} = 5\text{V}, I_{DS} = 60\text{mA}$	-1.0	-2.0	-3.5	V
Gate Source Breakdown Voltage	V_{GSO}	$I_{GS} = -60\mu\text{A}$	-5	-	-	V
Output Power at 1dB G.C.P.	P_{1dB}	$V_{DS} = 10\text{V}$ $I_{DS} \approx 0.6I_{DSS}$ (Typ.), $f = 2.3\text{GHz}$	34.5	35.5	-	dBm
Power Gain at 1dB G.C.P.	G_{1dB}		10.5	11.5	-	dB
Power-added Efficiency	η_{add}		-	46	-	%
Thermal Resistance	R_{th}	Channel to Case	-	7.5	10	$^\circ\text{C/W}$

CASE STYLE: ME

G.C.P.: Gain Compression Point

FLL357ME

L-Band Medium & High Power GaAs FET

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Appendix F: Housing Dimension for the Modulator Module

Appendix G: Measurement Result for X-band Direct Up-conversion QPSK Modulator Module

Test conditions:

DRO: 12V, 0.35A.

Ambient temperature: ~ 25°C

Baseband Power (dBm)	Module Output Power (dBm)	EVM (%) (Improved)	PE (°) (Improved)	EVM (%) (Initial)	PE (°) (Initial)
-0.94	-3.9	13.4	1.1	27	5.6
0.12	-3	13.3	1	27.5	6
0.98	-2.1	13.1	0.95	28	5.8
1.92	-1.2	13	1	28.4	6.1
2.85	-0.3	13	1.1	28	6.5
3.98	0.6	13	1.4	28.6	7
4.92	1.4	13.1	1.9	29	7.8
5.8	2.1	13.4	2.6	28.4	8.8

Appendix H: Data Sheet of HSMS-8202 Schottky Diode

Surface Mount Microwave Schottky Mixer Diodes

Technical Data

HSMS-8101 Single
HSMS-8202 Series Pair
HSMS-8207 Ring Quad
HSMS-8209 Crossover Quad

Features

- Optimized for use at 10-14 GHz
- Low Capacitance
- Low Conversion Loss
- Low RD
- Low Cost Surface Mount Plastic Package

Plastic SOT-23 Package

Package Lead Code Identification (Top View)

Plastic SOT-143 Package

Description/Applications

These low cost microwave Schottky diodes are specifically designed for use at X/Ku-bands and are ideal for DBS and VSAT downconverter applications. They are available in SOT-23 and SOT-143 standard package configurations.

Note that Agilent's manufacturing techniques assure that dice found in pairs and quads are taken from adjacent sites on the wafer, assuring the highest degree of match.

Absolute Maximum Ratings^[1], $T_A = +25^\circ\text{C}$

Symbol	Parameter	Unit	Min.	Max.
P_T	Total Device Dissipation ^[2]	mW	—	75
P_{IV}	Peak Inverse Voltage	V	—	4
T_J	Junction Temperature	$^\circ\text{C}$	—	+150
T_{STG}, T_{op}	Storage and Operating Temperature	$^\circ\text{C}$	-65	+150

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. Measured in an infinite heat sink at $T_{CASE} = 25^\circ\text{C}$. Derate linearly to zero at 150°C per diode.

ESD WARNING:

Handling Precautions Should Be Taken To Avoid Static Discharge.

DC Electrical Specifications, $T_A = 25^\circ\text{C}$

Symbol	Parameters and Test Conditions	Units	HSMS-8101		HSMS-8202		HSMS-8207		HSMS-8209	
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{BR}	Breakdown Voltage $I_R = 10\ \mu\text{A}$	V	4		4		4		4	
C_T	Total Capacitance $V_R = 0\ \text{V}$, $f = 1\ \text{MHz}$	pF		0.26		0.26		0.26		0.26
ΔC_T	Capacitance Difference $V_R = 0\ \text{V}$, $f = 1\ \text{MHz}$	pF		—		0.04		0.04		0.04
R_D	Dynamic Resistance $I_F = 5\ \text{mA}$	Ω		14		14		14		14
ΔR_D	Dynamic Resistance Difference $I_F = 5\ \text{mA}$	Ω		—		2		2		2
V_F	Forward Voltage $I_F = 1\ \text{mA}$	mV	250	350	250	350	250	350	250	350
ΔV_F	Forward Voltage Difference $I_F = 1\ \text{mA}$	mV		—		20		20		20
Lead Code			1		2		7		9	
Package Marking Code in White where x is date code			R1x		2Rx		R7x		R9x	

RF Electrical Parameters, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Units	Typical
L_c	Conversion Loss at 12 GHz	dB	6.3
Z_{IF}	IF Impedance	Ω	150
SWR	SWR at 12 GHz		1.2

Note:

DC Load Resistance = 0 Ω ; LO Power = 1 mW.

SPICE Parameters

$I_S = 4.6\ \text{E-}8$	$E_G = 0.69$	$TT = 0$
$R_S = 6$	$C_{JO} = 0.18\ \text{E-}12$	
$N = 1.09$	$P_B (V_J) = 0.5$	
$B_V = 7.3$	$M = 0.5$	
$I_{BV} = 10\text{E-}5$	$FC = 0.5$	

Linear Equivalent Circuit

Self Bias

	1 mA	2.5 mA
R_j	263	142

Appendix I: Drawing of the SSPA Module

Main Chassis

Module Cover

Isolation Block 1 (To Cover HPA1)

Isolation Block 2 (To Cover HPA2)

Appendix J: Simulation Setting in CST Microwave Studio

1) Simulation Frequency Range: 0-10 GHz

2) Mesh Properties

The screenshot shows the 'Mesh Properties' dialog box. The 'Mesh type' is set to 'Hexahedral'. Under 'Mesh density control', 'Lines per wavelength' is 28, 'Lower mesh limit' is 28, and 'Mesh line ratio limit' is 40. The 'Automatic mesh generation' checkbox is checked. The 'Mesh summary' section shows: Min. mesh step: 0.057, Max. mesh step: 1.07476, Meshcells: 1,765,788, Nx: 292, Ny: 149, and Nz: 42. Buttons on the right include OK, Apply, Cancel, Update, Specials..., Simplify Model..., and Help.

3) Background Properties

The screenshot shows the 'Background Properties' dialog box. Under 'Material properties', 'Material type' is 'Normal', 'Epsilon' is 1.0, 'Thermal type' is 'Normal', and 'Thermal cond. (W/K/m)' is 0.024. The 'Surrounding space' section has 'Apply in all directions' checked, and 'Distance' is 5. Buttons at the bottom include OK, Apply, Close, and Help.

4) Transient (Time) Solver Properties

Appendix K: Test Data of the XBT HPA and SSPA Module

Test conditions:

Ambient temperature: $\sim 25^{\circ}\text{C}$

Single Stage Amplifier (TMD0708-02) Tested with CW

Pin (dBm)	Pout (dBm)	Gain (dB)	Vds (V)	Ids (A)	Vgs (V)	Igs (A)	PAE (%)
0	23.75	23.75	10	1.35	-5	0.03	1.73
1	24.75	23.75	10	1.36	-5	0.03	2.16
2	25.75	23.75	10	1.38	-5	0.03	2.68
3	26.75	23.75	10	1.38	-5	0.03	3.38
4	27.75	23.75	10	1.38	-5	0.03	4.25
5	28.75	23.75	10	1.39	-5	0.03	5.31
6	29.75	23.75	10	1.40	-5	0.03	6.64
7	30.74	23.74	10	1.42	-5	0.03	8.23
8	31.62	23.62	10	1.45	-5	0.03	9.87
9	32.50	23.50	10	1.49	-5	0.03	11.76
10	33.15	23.15	10	1.52	-5	0.03	13.39
11	33.60	22.60	10	1.57	-5	0.03	14.37
12	33.89	21.89	10	1.62	-5	0.03	14.88
13	34.27	21.27	10	1.77	-5	0.03	14.86

Single Stage Amplifier (FMM5057VF) Tested with CW

Pin (dBm)	Pout (dBm)	Gain (dB)	Vds (V)	Ids (A)	Vgs (V)	Igs (A)	PAE (%)
1.00	26.28	25.28	10.00	1.21	-5.00	0.01	3.48
2.00	27.22	25.22	10.00	1.21	-5.00	0.01	4.33
3.00	28.48	25.48	10.00	1.22	-5.00	0.01	5.74
4.00	29.40	25.40	10.00	1.23	-5.00	0.01	7.03
5.00	30.32	25.32	10.00	1.24	-5.00	0.01	8.62
6.00	31.20	25.20	10.00	1.26	-5.00	0.01	10.39
7.00	31.92	24.92	10.00	1.29	-5.00	0.01	11.98
8.00	32.70	24.70	10.00	1.33	-5.00	0.01	13.90
9.00	33.48	24.48	10.00	1.37	-5.00	0.01	16.15
10.00	34.15	24.15	10.00	1.41	-5.00	0.01	18.31

Single Stage Amplifier (FLM7785-12F) Tested with CW

Pin (dBm)	Pout (dBm)	Gain (dB)	Vds (V)	Ids (A)	Vgs (V)	Igs (A)*	PAE (%)
22.00	32.00	10.00	25.40	2.54	-0.5	0	5.62
23.00	33.05	10.05	25.40	2.54	-0.5	0	7.16
24.00	34.10	10.10	25.40	2.54	-0.5	0	9.13
25.00	35.12	10.12	25.50	2.55	-0.5	0	11.51
26.00	36.15	10.15	25.60	2.56	-0.5	0	14.54
27.00	37.05	10.05	25.80	2.58	-0.5	0	17.71
28.00	37.92	9.92	26.00	2.60	-0.5	0	21.40
29.00	38.71	9.71	26.20	2.62	-0.5	0	25.33
30.00	39.45	9.45	26.60	2.66	-0.5	0	29.36
31.00	40.20	9.20	26.80	2.68	-0.5	0	34.37
32.00	40.50	8.50	25.70	2.57	-0.5	0	37.49
33.00	40.71	7.71	23.80	2.38	-0.5	0	41.10
34.00	40.78	6.78	22.20	2.22	-0.5	0	42.59
33.50	40.77	7.27	22.80	2.28	-0.5	0	42.55

* Gate current is less than 1mA. Therefore the power consumption at device gate is negligible.

Toshiba and Fujitsu Cascade Amplifier Tested with CW

Pin (dBm)	Pout (dBm)	Gain (dB)	TMD0708-02				FLM7785-12F			PAE (%)
			Vds (V)	Ids (A)	Vgs (V)	Igs (I)	Vds (V)	Ids (A)	Vgs (V)*	
-2	32.77	34.77	10	1.34	-5	0.03	10	2.35	-0.5	5.10
-1	33.77	34.77	10	1.34	-5	0.03	10	2.5	-0.5	6.18
0	34.76	34.76	10	1.34	-5	0.03	10	2.58	-0.5	7.60
1	35.73	34.73	10	1.34	-5	0.03	10	2.59	-0.5	9.48
2	36.68	34.68	10	1.34	-5	0.03	10	2.61	-0.5	11.74
3	37.63	34.63	10	1.35	-5	0.03	10	2.65	-0.5	14.43
4	38.56	34.56	10	1.36	-5	0.03	10	2.72	-0.5	17.52
5	39.41	34.41	10	1.38	-5	0.03	10	2.82	-0.5	20.70
6	40.13	34.13	10	1.41	-5	0.03	10	2.93	-0.5	23.65
7	40.71	33.71	10	1.45	-5	0.03	10	2.89	-0.5	27.03
8	40.9	32.9	10	1.49	-5	0.03	10	2.91	-0.5	27.85
9	40.73	31.73	10	1.49	-5	0.03	10	2.45	-0.5	29.89
10	40.7	30.7	10	1.57	-5	0.03	10	2.36	-0.5	29.76
11	40.68	29.68	10	1.65	-5	0.03	10	2.32	-0.5	29.32
12	40.67	28.67	10	1.7	-5	0.03	10	2.3	-0.5	29.02

* Gate current is less than 1mA. Therefore the power consumption at device gate is negligible.

Toshiba and Fujitsu Cascade Amplifier Tested with 25Msps QPSK Signal

Input			TMD0708-02				FLM7785-12F			Output			Relative Error			
Pin (dBm)	EVM (%)	PE (°)	Vds (V)	Ids (A)	Vgs (V)	Igs (A)	Vds (V)	Ids (A)	Vgs (V)*	Pout (dBm)	EVM (%)	PE (°)	EVM (%)	PE (°)	Gain (dB)	PAE (%)
2	1.55	0.6	10	1.38	-5	0.03	10	2.51	-0.5	36.87	2.82	1.05	1.27	0.45	34.87	12.5
3	1.55	0.6	10	1.38	-5	0.03	10	2.56	-0.5	37.42	3.3	1.2	1.75	0.6	34.42	14.01
4	1.55	0.6	10	1.39	-5	0.03	10	2.62	-0.5	38.03	3.95	1.37	2.4	0.77	34.03	15.84
5	1.55	0.6	10	1.4	-5	0.03	10	2.68	-0.5	38.52	4.5	1.63	2.95	1.03	33.52	17.42
6	1.55	0.6	10	1.43	-5	0.03	10	2.73	-0.5	39.02	5.3	2	3.75	1.4	33.02	19.17
7	1.55	0.6	10	1.46	-5	0.03	10	2.77	-0.5	39.47	6.3	2.6	4.75	2	32.47	20.91
8	1.55	0.6	10	1.49	-5	0.03	10	2.7	-0.5	39.87	8.2	3.5	6.65	2.9	31.87	23.15
9	1.55	0.6	10	1.5	-5	0.03	10	2.2	-0.5	39.82	7.9	3.1	6.35	2.5	30.82	25.91

* Gate current is less than 1mA. Therefore the power consumption at device gate is negligible.

SSPA Engineering Model with Absorber, Tested with 25Msps QPSK Signal

Input			FMM5057VF				FLL7785-12F			Output			Relative Error			
Pin (dBm)	EVM (%)	PE (°)	Vds (V)	Ids (A)	Vgs (V)	Igs (A)	Vds (V)	Ids (A)	Vgs (V)	Pout (dBm)	EVM (%)	PE (°)	EVM (%)	PE (°)	Gain (dB)	PAE (%)
-3.1	1.6	0.65	10	1.04	-5	0.01	10	2.55	-0.5	31.1	1.65	0.66	0.05	0.01	34	3.59
-2.08	1.6	0.65	10	1.05	-5	0.01	10	2.53	-0.5	32.1	1.7	0.7	0.1	0.05	33.98	4.53
-1	1.6	0.65	10	1.05	-5	0.01	10	2.52	-0.5	33	1.9	0.74	0.3	0.09	33.8	5.59
0	1.6	0.65	10	1.05	-5	0.01	10	2.52	-0.5	33.9	2.1	0.8	0.5	0.15	33.7	6.87
1	1.6	0.65	10	1.06	-5	0.01	10	2.53	-0.5	34.9	2.5	0.95	0.9	0.3	33.7	8.6
2	1.6	0.65	10	1.07	-5	0.01	10	2.55	-0.5	35.7	3	1.1	1.4	0.45	33.5	10.3
3	1.6	0.65	10	1.08	-5	0.01	10	2.6	-0.5	36.4	3.7	1.3	2.1	0.65	33.2	11.9
4	1.6	0.65	10	1.1	-5	0.01	10	2.66	-0.5	37.2	4.3	1.6	2.7	0.95	33	14.0
5	1.6	0.65	10	1.13	-5	0.01	10	2.74	-0.5	37.7	5	1.87	3.4	1.22	32.5	15.2
6	1.6	0.65	10	1.16	-5	0.01	10	2.82	-0.5	38.2	5.7	2.1	4.1	1.45	32	16.6
7	1.6	0.65	10	1.2	-5	0.01	10	2.89	-0.5	38.6	6.5	2.3	4.9	1.65	31.4	17.7
8	1.6	0.65	10	1.22	-5	0.01	10	2.94	-0.5	38.9	7	2.5	5.4	1.85	30.7	18.6

* Gate current is less than 1mA. Therefore the power consumption at device gate is negligible.

Complete SSPA Engineering Model 1, Tested with 25Msps QPSK Signal

Input			FMM5057VF				FLL7785-12F			Output			Relative Error			
Pin (dBm)	EVM (%)	PE (°)	Vds (V)	Ids (A)	Vgs (V)	Igs (A)	Vds (V)	Ids (A)	Vgs (V)*	Pout (dBm)	EVM (%)	PE (°)	EVM (%)	PE (°)	Gain (dB)	PAE (%)
-3.1	1.6	0.65	10	1.04	-5	0.01	10	2.66	-0.6	31.1	1.65	0.65	0.05	0	34	3.48
-2.08	1.6	0.65	10	1.05	-5	0.01	10	2.64	-0.6	32.1	1.7	0.7	0.1	0.05	33.98	4.393
-1	1.6	0.65	10	1.05	-5	0.01	10	2.63	-0.6	33.05	1.9	0.74	0.3	0.09	33.85	5.483
0	1.6	0.65	10	1.05	-5	0.01	10	2.62	-0.6	34	2.2	0.8	0.6	0.15	33.8	6.842
1	1.6	0.65	10	1.06	-5	0.01	10	2.62	-0.6	35	2.53	0.95	0.93	0.3	33.8	8.59
2	1.6	0.65	10	1.07	-5	0.01	10	2.64	-0.6	36	3.1	1.15	1.5	0.5	33.8	10.73
3	1.6	0.65	10	1.08	-5	0.01	10	2.68	-0.6	36.7	3.7	1.4	2.1	0.75	33.5	12.43
4	1.6	0.65	10	1.1	-5	0.01	10	2.74	-0.6	37.35	4.4	1.65	2.8	1	33.15	14.14
5	1.6	0.65	10	1.13	-5	0.01	10	2.82	-0.6	37.95	5.25	1.9	3.65	1.25	32.75	15.78
6	1.6	0.65	10	1.17	-5	0.01	10	2.89	-0.6	38.4	6	2.2	4.4	1.55	32.2	17.03
7	1.6	0.65	10	1.2	-5	0.01	10	2.95	-0.6	38.8	6.7	2.4	5.1	1.75	31.6	18.27
8	1.6	0.65	10	1.22	-5	0.01	10	3.01	-0.6	39.2	7.3	2.5	5.7	1.85	31	19.65

* Gate current is less than 1mA. Therefore the power consumption at device gate is negligible.

Complete SSPA Engineering Model 1, Tested with 25Msps QPSK Signal

Input			FMM5057VF				FLL7785-12F			Output			Relative Error			
Pin (dBm)	EVM (%)	PE (°)	Vds (V)	Ids (A)	Vgs (V)	Igs (A)	Vds (V)	Ids (A)	Vgs (V)*	Pout (dBm)	EVM (%)	PE (°)	EVM (%)	PE (°)	Gain (dB)	PAE (%)
-3.1	1.6	0.65	10	1.01	-5.3	0.01	10	2.52	-0.55	33.72	1.74	0.65	0.14	0	36.62	6.67
-2.08	1.6	0.65	10	1.02	-5.3	0.01	10	2.52	-0.55	34.64	1.95	0.68	0.35	0.03	36.52	8.22
-1	1.6	0.65	10	1.02	-5.3	0.01	10	2.53	-0.55	35.53	2.3	0.74	0.7	0.09	36.33	10.1
0	1.6	0.65	10	1.03	-5.3	0.01	10	2.54	-0.55	36.4	2.7	0.83	1.1	0.18	36.2	12.2
1	1.6	0.65	10	1.04	-5.3	0.01	10	2.57	-0.55	37.2	3.44	1	1.84	0.35	36	14.5
2	1.6	0.65	10	1.05	-5.3	0.01	10	2.6	-0.55	37.85	4.25	1.27	2.65	0.62	35.65	16.7
3	1.6	0.65	10	1.06	-5.3	0.01	10	2.63	-0.55	38.35	5	1.52	3.4	0.87	35.15	18.5
4	1.6	0.65	10	1.07	-5.3	0.01	10	2.66	-0.55	38.8	5.6	1.85	4	1.2	34.6	20.3
5	1.6	0.65	10	1.09	-5.3	0.01	10	2.67	-0.55	39.15	6.2	2.16	4.6	1.51	33.95	21.9
6	1.6	0.65	10	1.11	-5.3	0.01	10	2.67	-0.55	39.37	6.7	2.5	5.1	1.85	33.17	22.9
7	1.6	0.65	10	1.14	-5.3	0.01	10	2.59	-0.55	39.5	7	2.6	5.4	1.95	32.3	23.9
8	1.6	0.65	10	1.17	-5.3	0.01	10	2.51	-0.55	39.7	7.5	2.75	5.9	2.1	31.5	25.3

* Gate current is less than 1mA. Therefore the power consumption at device gate is negligible.

Appendix L: Test Data of the S-band HPA, FLL357ME

Test conditions:

Ambient temperature: ~ 25°C

Amplifier Matched for “Gain”, Tested with CW

Pin (dBm)	Pout (dBm)	Gain (dB)	Vds (V)	Ids (A)	Vgs (V)*	PAE (%)
12	25.45	13.45	10	0.71	-1	4.72
13	26.44	13.44	10	0.67	-1	6.28
14	27.44	13.44	10	0.65	-1	8.15
15	28.43	13.43	10	0.63	-1	10.56
16	29.43	13.43	10	0.63	-1	13.29
17	30.42	13.42	10	0.62	-1	16.96
18	31.35	13.35	10	0.61	-1	21.34
19	32.17	13.17	10	0.59	-1	26.59
20	32.83	12.83	10	0.57	-1	31.91
21	33.38	12.38	10	0.55	-1	37.31
22	33.85	11.85	10	0.54	-1	42.00
23	34.16	11.16	10	0.53	-1	45.41

* Gate current is less than 1mA. Therefore the power consumption at device gate is negligible.

Amplifier Matched for “Gain”, Tested with 1Msps BPSK Signal

Pin (dBm)	Pout (dBm)	Gain (dB)	Vds (V)	Ids (A)	Vgs (V)*	Relative EVM (%)	Relative PE (°)	PAE (%)
12	24.54	12.54	10	0.58	-1	0.85	0.38	4.63
13	25.5	12.50	10	0.58	-1	0.85	0.38	5.77
14	26.46	12.46	10	0.57	-1	0.9	0.38	7.32
15	27.37	12.37	10	0.57	-1	1.09	0.36	9.02
16	28.23	12.23	10	0.57	-1	1.54	0.36	10.97
17	29.02	12.02	10	0.56	-1	2.4	0.46	13.36
18	29.72	11.72	10	0.55	-1	3.24	0.43	15.90
19	30.35	11.35	10	0.54	-1	4.08	0.46	18.60
20	30.82	10.82	10	0.53	-1	4.7	0.5	20.90
21	31.36	10.36	10	0.52	-1	5.27	0.53	23.88
22	31.72	9.72	10	0.49	-1	5.95	0.58	27.09
23	31.52	8.52	10	0.31	-1.4	6.95	0.9	39.34

* Gate current is less than 1mA. Therefore the power consumption at device gate is negligible.

Amplifier Matched for “Power”, Tested with CW

Pin (dBm)	Pout (dBm)	Gain (dB)	Vds (V)	Ids (A)	Vgs (V)*	PAE (%)
12	24.4	12.4	10	0.47	-1	5.52
13	25.41	12.41	10	0.47	-1	6.97
14	26.39	12.39	10	0.47	-1	8.73
15	27.42	12.42	10	0.47	-1	11.07
16	28.42	12.42	10	0.47	-1	13.94
17	29.4	12.4	10	0.48	-1	17.10
18	30.39	12.39	10	0.48	-1	21.48
19	31.39	12.39	10	0.48	-1	27.04
20	32.38	12.38	10	0.5	-1	32.60
21	33.37	12.37	10	0.52	-1	39.36
22	34.23	12.23	10	0.55	-1	45.27
23	34.9	11.9	10	0.58	-1	49.84
24	35.42	11.42	10	0.62	-1	52.13
25	35.66	10.66	10	0.64	-1	52.58

* Gate current is less than 1mA. Therefore the power consumption at device gate is negligible.

Amplifier Matched for “Power”, Tested with 1Msps BPSK Signal

Pin (dBm)	Pout (dBm)	Gain (dB)	Vds (V)	Ids (A)	Vgs (V)*	Relative EVM (%)	Relative PE (°)	PAE (%)
6	19.46	13.46	10	0.63	-1	0.85	0.39	1.34
7	20.4	13.4	10	0.63	-1	0.94	0.45	1.66
8	21.36	13.36	10	0.62	-1	0.84	0.39	2.10
9	22.33	13.33	10	0.62	-1	0.88	0.41	2.63
10	23.32	13.32	10	0.61	-1	0.81	0.36	3.36
11	24.3	13.3	10	0.6	-1	0.82	0.38	4.28
12	25.28	13.28	10	0.6	-1	0.84	0.39	5.36
13	26.25	13.25	10	0.59	-1	0.84	0.39	6.81
14	27.26	13.26	10	0.59	-1	0.84	0.38	8.59
15	28.25	13.25	10	0.59	-1	0.82	0.39	10.79
16	29.24	13.24	10	0.59	-1	0.81	0.38	13.55
17	30.24	13.24	10	0.59	-1	0.98	0.43	17.06
18	31.25	13.25	10	0.59	-1	1.72	0.73	21.53
19	32.23	13.23	10	0.59	-1	2.7	1.1	26.98
20	33.04	13.04	10	0.59	-1	3.69	1.38	32.44
21	33.73	12.73	10	0.59	-1	4.5	1.34	37.87
22	34.34	12.34	10	0.59	-1	5.24	1.4	43.36
23	34.79	11.79	10	0.57	-1	5.88	1.5	49.36
24	34.61	10.61	10	0.49	-1.7	8.77	1.7	53.87
25	34.5	9.5	10	0.46	-1.7	10.2	2.1	54.39

* Gate current is less than 1mA. Therefore the power consumption at device gate is negligible.

Appendix M: Test Data of the Medium PA, FLL1777ME

Test conditions:

Ambient temperature: ~ 25°C

WJ AH102 Amplifier Tested with 1Mbps BPSK Signal

Pin (dBm)	Pout (dBm)	Gain (dB)	Vds (V)	Ids (A)	Relative EVM (%)	Relative PE (°)	PAE (%)
6	18.18	12.18	10	0.2	1.37	0.28	3.09
7	19.05	12.05	10	0.2	1.46	0.3	3.77
8	20.01	12.01	10	0.19	1.45	0.29	4.94
9	20.96	11.96	10	0.19	1.52	0.37	6.15
10	21.9	11.9	10	0.19	1.72	0.47	7.63
11	22.87	11.87	10	0.19	2.06	0.7	9.53
12	23.8	11.8	10	0.18	2.95	1.12	12.45
13	24.62	11.62	10	0.18	4.77	1.61	14.99
14	25.3	11.3	10	0.17	7.41	2.25	18.45
15	25.73	10.73	10	0.16	10.63	3.2	21.41
16	25.93	9.93	10	0.14	13.76	4.06	25.14
17	26	9	10	0.13	16.08	4.35	26.77
18	25.95	7.95	10	0.12	17.73	5.83	27.54

Hittite HMC454ST89 Amplifier Tested with 1Mbps BPSK Signal

Pin (dBm)	Pout (dBm)	Gain (dB)	Vds (V)	Ids (A)	Relative EVM (%)	Relative PE (°)	PAE (%)
6	18.5	12.5	5	0.15	0.59	0.25	8.91
7	19.5	12.5	5	0.15	0.61	0.26	11.22
8	20.5	12.5	5	0.15	0.74	0.32	14.12
9	21.48	12.48	5	0.15	0.91	0.4	17.69
10	22.42	12.42	5	0.15	1.15	0.5	21.94
11	23.35	12.35	5	0.16	1.54	0.57	25.46
12	24.22	12.22	5	0.17	2.1	0.55	29.22
13	25	12	5	0.18	2.95	0.47	32.92
14	25.67	11.67	5	0.18	4.05	0.48	38.21
15	26.22	11.22	5	0.19	5.32	0.66	40.75
16	26.66	10.66	5	0.2	6.79	1.19	42.36
17	26.95	9.95	5	0.2	8.59	1.95	44.53
18	27.09	9.09	5	0.2	10.33	2.56	44.86

First FLL177ME Amplifier Tested with 1Mbps BPSK Signal, Vgs at -2V

Pin (dBm)	Pout (dBm)	Gain (dB)	Vgs (V)	Vds (V)	Ids (A)	EVM (%)	PE (°)	PAE (%)
6	17.47	11.47	-2	10	0.05	0.88	0.45	10.37
7	18.44	11.44	-2	10	0.06	0.91	0.42	10.80
8	19.46	11.46	-2	10	0.06	0.92	0.38	13.67
9	20.48	11.48	-2	10	0.07	0.93	0.34	14.82
10	21.5	11.5	-2	10	0.08	0.99	0.3	16.41
11	22.56	11.56	-2	10	0.09	1.03	0.29	18.63
12	23.63	11.63	-2	10	0.1	1.05	0.27	21.48
13	24.7	11.7	-2	10	0.11	1.09	0.25	25.02
14	25.78	11.78	-2	10	0.12	1.19	0.25	29.44
15	26.85	11.85	-2	10	0.14	1.33	0.24	32.32
16	27.93	11.93	-2	10	0.16	1.49	0.25	36.32
17	28.96	11.96	-2	10	0.18	1.24	0.22	40.94
18	29.99	11.99	-2	10	0.2	1.18	0.28	46.73
19	30.91	11.91	-2	10	0.23	3.09	0.69	50.16
20	31.23	11.23	-2.1	10	0.23	4.92	1.18	53.36
21	30.92	9.92	-2.4	10	0.21	4.72	1.42	52.86
22	30.55	8.55	-2.8	10	0.19	4.33	1.57	51.40

First FLL177ME Amplifier Tested with 1Mbps BPSK Signal, Vgs at -1.4V

Pin (dBm)	Pout (dBm)	Gain (dB)	Vgs (V)	Vds (V)	Ids (A)	EVM (%)	PE (°)	PAE (%)
6	21.43	15.43	-1.4	10	0.21	0.7	0.32	6.43
7	22.41	15.41	-1.4	10	0.21	0.79	0.38	8.06
8	23.39	15.39	-1.4	10	0.21	0.91	0.43	10.09
9	24.36	15.36	-1.4	10	0.21	1.15	0.58	12.62
10	25.29	15.29	-1.4	10	0.21	1.54	0.8	15.62
11	26.22	15.22	-1.4	10	0.22	2.04	1.07	18.46
12	27.14	15.14	-1.4	10	0.22	2.45	1.3	22.81
13	28.05	15.05	-1.4	10	0.23	2.79	1.51	26.88
14	28.94	14.94	-1.4	10	0.24	2.77	1.49	31.60
15	29.77	14.77	-1.4	10	0.25	2.7	1.33	36.67
16	30.57	14.57	-1.4	10	0.27	2.87	0.93	40.76
17	31.29	14.29	-1.4	10	0.29	4.15	0.51	44.68
18	31.6	13.6	-1.5	10	0.28	4.99	0.63	49.37
19	31.49	12.49	-1.8	10	0.26	4.89	0.9	51.15
20	31.27	11.27	-2.1	10	0.24	4.96	1.18	51.65
21	30.96	9.96	-2.4	10	0.22	4.88	1.45	50.98
22	30.59	8.59	-2.7	10	0.2	4.35	1.52	49.35

Second FLL177ME Amplifier Tested with 1Mbps BPSK Signal, Vgs at -2V

Pin (dBm)	Pout (dBm)	Gain (dB)	Vgs (V)	Vds (V)	Ids (A)	EVM (%)	PE (°)	PAE (%)
6	20.63	14.63	-2	10	0.07	1.19	0.28	15.95
7	21.63	14.63	-2	10	0.08	1.26	0.25	17.57
8	22.64	14.64	-2	10	0.08	1.07	0.52	22.17
9	23.68	14.68	-2	10	0.09	1.04	0.47	25.04
10	24.69	14.69	-2	10	0.1	1.03	0.41	28.44
11	25.74	14.74	-2	10	0.12	1.06	0.38	30.20
12	26.8	14.8	-2	10	0.13	1.2	0.37	35.60
13	27.86	14.86	-2	10	0.15	1.36	0.35	39.40
14	28.87	14.87	-2	10	0.16	1.16	0.3	46.61
15	29.77	14.77	-2	10	0.18	1.33	0.33	50.93
16	30.68	14.68	-2	10	0.21	3.1	0.68	53.79
17	31.38	14.38	-2	10	0.23	5.33	1.12	57.56
18	31.55	13.55	-2	10	0.23	6.64	1.55	59.38
19	31.26	12.26	-2	10	0.21	7.01	2.01	59.86
20	30.89	10.89	-2	10	0.19	6.82	2.35	59.34
21	30.47	9.47	-2	10	0.18	6.41	2.6	54.91
22	30.06	8.06	-2	10	0.16	5.88	2.68	53.46

Second FLL177ME Amplifier Tested with 1Mbps BPSK Signal, Vgs at -1.4V

Pin (dBm)	Pout (dBm)	Gain (dB)	Vgs (V)	Vds (V)	Ids (A)	EVM (%)	PE (°)	PAE (%)
6	22.63	16.63	-1.4	10	0.19	0.84	0.42	9.43
7	23.69	16.69	-1.4	10	0.19	1.04	0.55	12.05
8	24.7	16.7	-1.4	10	0.19	1.35	0.74	15.20
9	25.71	16.71	-1.4	10	0.2	2.01	1.13	18.22
10	26.7	16.7	-1.4	10	0.2	2.73	1.55	22.89
11	27.73	16.73	-1.4	10	0.21	3.3	1.87	27.64
12	28.74	16.74	-1.4	10	0.22	3.55	2.02	33.29
13	29.68	16.68	-1.4	10	0.23	3.26	1.78	39.52
14	30.5	16.5	-1.4	10	0.24	3	1.2	45.70
15	31.2	16.2	-1.4	10	0.26	4.06	0.64	49.49
16	31.73	15.73	-1.4	10	0.28	5.58	0.56	51.77
17	31.74	14.74	-1.7	10	0.26	6.29	1.07	55.49
18	31.55	13.55	-2.1	10	0.24	6.71	1.54	56.91
19	31.24	12.24	-2.4	10	0.22	6.84	1.92	56.86
20	30.85	10.85	-2.7	10	0.2	6.98	2.35	55.81
21	30.42	9.42	-3	10	0.18	6.48	2.6	54.20
22	29.98	7.98	-3.3	10	0.16	5.83	2.64	52.31