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High Performance Organic Semiconducting Device and Physics

Qin Fang

School of Chemical and Biomedical Engineering

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CHAPTER 1 INTRODUCTION AND OBJECTIVE OF THE RESEARCH

1.1 Backgroundz

Organic semiconducting material-based organic electronics have extensively studied over the last twenty years. It offers several advantages over the traditional inorganic semiconductor technologies. First, organic electronics are compatible with low-cost mass manufacturing process such as direct printing, embossing and other solution-based processes, which makes them favorable to applications in markets where cost is the key factor. Second, organic electronics can use a variety of substrates including plastics for remarkable mechanical flexibility. Another distinguishing factor is the multiple functionalities that organic materials can sustain when synthesized with carefully designed chemical structures, which may allow the fabrication of multifunctional organic devices using extremely simple device structures. Organic field effect transistor (OFET) is one of the mainstream devices in this area for considerable attentions. Since the first organic field effect transistor was reported in 1986[1], there has been a very impressive progress in both the synthesis of novel semiconducting materials[2-6] and the development of new fabrication techniques[7-9]. This kind of electrical devices has great potential for different applications, especially for new products that rely on their unique characteristics, such as electronic newspapers[10, 11], radio-frequency identifications

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tags[12, 13], large-area flexible displays[11](Figure 1.1) and various chemical and biological sensors[14, 15].

Figure 1.1 Organic emissive displays in the present and the future. (a), A full color 13-inch diagonal small-molecular-weight OLED display based on OTFT backbones, Image courtesy of Sony Corp. (b), A conceptual view of a future organic electronic flexible pen display, Image courtesy of Universal Display Corp [7].

1.2 Objective and Significance

The main challenge in organic electronics is that both fundamental theories and fabrication techniques of the OFET devices are extremely immature. Thus, although OFETs can offer great advantages as discussed above, there is a great need to develop novel approaches for high performance device and to study their physics for deep scientific insight that could guide us to further enhance the performance and stability for realization of practical applications.

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In our research, we use different organic materials to fabricate devices on silicon wafer based structures. Our objective is to fabricate high-performance, solution-processible and stable OFETs through systemically investigating the semiconducting materials and optimizing device fabrication process; then further exploring some fundamental physical mechanisms and scientific insights underlying the device operation, such as charge transport channel, interface energy matching, bias-stress effects and thermal stability. In this study, for the first time we fabricate solution processed high performance OFET devices from environmentally friendly solvent, and investigate OFET stability under both high temperature and long time bias-stress of the specific organic semiconductor we used. Studies of these fundamental mechanisms provide us useful information to develop the strategies for design and optimization of electrically stable materials and high performance devices.

1.3 Scope of Research

This thesis presents research work on two families of high mobility p-type organic semiconductors and their OFETs, one of them is synthesized by our research group. Chapter 2 is a brief background introduction of OFET technology. The current status of the synthetic organic semiconductor materials, fabrication methods of OFET devices and their operations is reviewed. A progress report on OFET devices made from different materials including their performances, e.g. charge carrier mobility, drain current, on/off ratio, and channel dimension effect is presented.

Chapter 3 discusses the experimental methods I used to fabricate and characterize the semiconducting materials and the OFET devices in this work. Specifically, the methods

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of semiconductor characterization, device substrates preparation, thin film growth, surface modification, and electrical characterization are described.

Chapter 4 reports the OFET based on Poly (3, 3'''-didodecyl quarter thiophene) (PQT-12). The material is characterized with different techniques including UV-visible spectrum, Raman spectrum, XRD detection and electrochemical methods. Different types of self-assembled organosilane monolayers (SAMs) are deposited on dielectric surface to enhance the device performance. Experiments for temperature effect on the device are conducted to understand more the charge transport mechanism and environmental stability. Long term bias-stress effect and its recovery process are also investigated.

Chapter 5 covers the characterization of a novel p-type semiconducting polymer Poly (2, 6-bis (3-alkylthiophen-2-yl) dithieno [3, 2-b; 2', 3'-d] thiophene) (PBTDDT-12) and the fabrication and optimization of its OFET device. A high field-effect mobility of 0.28cm/Vs and an *on/off* ratio of 10^7 at ambient temperature and atmosphere are obtained. Uniformly distributed nanoparticle dispersion of this material in the environmentally friendly solvent---hexane is achieved through ultrasonic agitation and is used to fabricate high performance OFET devices. The thermal stability of this material is discussed at the end of this chapter.

Chapter 6 provides conclusions of this thesis work and a brief discussion of directions for future works on semiconducting materials and OFET technologies.

CHAPTER 2 LITERATURE REVIEW

2.1 Introduction

Following the initial demonstration of field-effect conduction in small organic molecules[5, 16, 17], and conjugated polymers[6, 18, 19], the community of industrial and academic research groups that are interested in using organic molecules as the active components in field-effect transistor (FET) devices has been growing steadily, particularly over the last four to five years. One of the main technological attractions is that all the layers of an OFET can be deposited and patterned at room temperature by a combination of low-cost solution-processing and direct-write printing, which makes them ideally suitable for the realization of flexible large-area electronic [8, 20, 21]. As a result of using organic semiconductors with better inherent mobility and stability, better understanding of the requirements for gate dielectrics, and by more controlled manufacturing processes, many applications, such as active-matrix electronic-paper displays, low-cost radio frequency identification tags and sensing devices, can be realistically put into market within the next three to five years.

2.2 Device Fabrication Methods

Organic field effect transistors are initially fabricated by matured photolithography, most of which are actually produced on oxidized silicon with source and drain contacts

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patterned. However, to adapt to the demands for low-cost and easy-fabrication techniques, there is a trend of patterning the source and drain electrodes using other methods. An elegant and promising route to low-cost fabrication of organic integrated circuits is the direct printing of various elements constituted OFETs.

Figure 2.1 shows cross-sectional view of two common geometries for OFETs. Both cases utilize a semiconducting layer that is electrically connected to source and drain electrodes. A thin insulating film isolates these electrodes and the semiconductor from the underlying gate electrode. The source and drain electrodes can be deposited on top of the semiconductor (top-contact OFET; Figure 2.1a), or the semiconductor can be deposited on top of the electrodes (bottom-contact OFET; Figure 2.1b). The region between the source and drain electrodes is known as the channel of the transistor.

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Figure 2.1 Schematic illustrations of two layouts of OFETs. (a).Geometry often referred to as “top-contact” because the source/drain electrodes lie on top of the semiconductor. (b). “Bottom-contact” device.

2.2.1 Screen printing

Screen printing is a simple patterning method that uses a blade to squeeze ink through predefined screen masks. It is a purely additive method in which an ink is deposited and patterned in one single step. The resolution depends on the properties of the ink, the substrate and the mask. It is generally difficult to form features smaller than 100 μ m with

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this method. Transistors with printed gate, drain, and source electrodes were first described by Garnier and coworkers[22]. More recent work demonstrates high-performance plastic transistors in which all of the essential components were screen printed[23]. Figure 2.2 shows the work principle of a screen printer and the transistor architecture it fabricated.

Figure 2.2 Printing principles of screen printed transistors and their device architectures.

2.2.2 Roll-to-roll printing

Starting with a roll of plastic substrate, the organic materials forming the devices' active regions are first deposited from the liquid phase, and then a metal "strike layer" is

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deposited. The film is then passed between rollers with an embossed pattern representing the ultimate electrode scheme required on their surfaces. These rollers can be used to directly pattern the electrodes. In final step, the strike layer metal is removed by dry etching, completing the device[7]. The sheets are eventually coated to eliminate degradation from exposure to the environment, and packaged to suit the desired application. This approach can be used to fabricate large-scale circuit with very low cost per unit area, but there are also some problems need to be solved such as, how the cylindrical stamps can be constructed and used for rapid patterning with reduced distortions. Figure 2.3 shows a schematic diagram of continuous roll-to-roll manufacture of organic electronic devices

Figure 2.3 Conceptual diagram of continuous and low-cost manufacture of organic electronic devices. [24]

2.2.3 Microcontact printing

Microcontact printing is one of the most commonly used soft lithography methods[25]. In

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the microcontact printing process, molecular transfer results from the contact-induced chemical change of the surface occurs. The nanoscale interaction between the substrate and the stamp enables transfer of materials from a stamp to a substrate. The resolution of microcontact printing is associated with the modulus of the elastomer used for the preparation of the stamp. Feature sizes as small as a few tens of nanometers can be microcontact printed[26]. This method has been used to pattern Au and Ag drain and source electrodes of OFETs[7]. It was also used to pattern solution-deposited semiconductor by microcontact printing different hydrophilic and hydrophobic patterns where the semiconductor is selectively deposited only on the hydrophilic regions[27]. Recently, microcontact printing is used to print a hydrophobic silane layer on a flexible plastic substrate[28]. The subsequent electroless plated Ni gate electrodes were only deposited at regions without the silane layer. Flexible integrated circuits were also demonstrated by this method. Figure 2.4 shows the schematic diagram of a direct microcontact patterning of OFET source and drain electrodes.

Figure 2.4 Illustration of the microcontact printing process in both subtractive way and additive way to pattern source and drain electrodes.[24]

2.2.4 Embossing

Embossing can be divided into two kinds: hot-embossing and Uv-embossing. It is a pattern transfer technique using the microstructured metallic or rigid plastic mold to imprint liquid polymers which are subsequently hardened by heat or Uv irradiation. In Uv transfer embossing[9], the mold is used as a printing template and the Uv resin is used as an adhesive rather than a structure material. The process selectively glues an ink from the template onto a substrate using the Uv resin. The ultimate resolution capability of this process depends solely on the master template. It is suitable for rapidly patterning large area substrates. Conducting polymer electrodes, thin film metal foil and graphite ink were molded into drain and source electrodes for OFETs[29]. Figure 2.5 shows an OFET of which source and drain electrodes made by embossing method, the big advantage of this method is that it has a very good resolution which upto several hundred nanometers. Vertical channel polymer field effect transistors on flexible poly (ethylene terephthalate) substrate were fabricated using this method, in which the critical channel length is only 0.7 to 0.9 micrometers[21].

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Figure 2.5 Fabrication process of an OFET source and drain electrode using embossing method.

2.3 Device Operation Mode

The basic function of a field-effect transistor is to modulate the current flowing in a conducting channel between two source and drain electrodes by means of a variable voltage applied at a third electrode, the gate, as shown in figure 2.6. Consider a plane-parallel condenser whose plates are a metal and a p-type organic semiconductor, in which holes are majority carriers. When no potential is applied to the plates, the free carriers are homogeneously distributed within the entire layer of the organic semiconductor. Owing to their low density, the conductance of this layer is very small and the current between

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the source and drain electrodes is very low. Now, when polarizing the gate negatively, an excess of holes would be attracted at the surface of the p-type semiconductor and concentrated there within a very thin layer. The density of charge carriers in this thin layer is largely increased, allowing a significant conductivity to be created in this conducting channel. On the other hand, when applying a positive bias on the gate, a depletion of charge carriers occurs in the semiconductor, which, under sufficiently high gate voltage, can be extended over the whole thickness of the semiconducting layer. Thus the external voltage applied to the gate allows either the accumulation of charge carriers at the semiconductor-insulator interface or the depletion of this interface, leading to a modulation of the charge carrier density in this conducting channel. This modulation of the carrier density is read by two other electrodes, source and drain (figure 2.6). A field-effect transistor (FET), is thus a three-electrode unipolar device that allows one to monitor, through the gate bias, the conductance of a thin channel at the semiconductor-insulator interface.

Figure 2.6 Schematic diagram of a bottom-contact thin film field effect transistor, with the organic semiconductor deposited onto the gate insulator and the previously patterned source and drain electrodes.

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The critical parameters of FETs are the channel width, W , the channel length, L , and the capacitance per unit area C_i of the insulator layer of thickness d , $C_i = \epsilon\epsilon_0/d$. Two main regimes are observed when plotting the drain current as a function of the drain voltage, at constant gate voltage (Fig 2.7). At low drain voltage, the current follows Ohm's law; it is therefore proportional to both the gate and drain voltages. As the drain voltage increases, the voltages drop at drain decreases to a point at which it falls to zero. At this point, which occurs when the drain voltage approach the gate voltage, there is a pinch off of the channel, and the channel current becomes independent of the drain bias. This regime is called the saturation regime. The gradual transition from the linear to the saturation regime is clearly shown in figure 2.7 (a).

The basic equation relating the drain current I_d to the applied gate voltage V_g and to the drain voltage V_d for the linear regime is

$$I_{Dlin} = \frac{W}{L} C_i \mu (V_g - V_{th}) V_d \quad (2.1)$$

Where μ is the field-effect carrier mobility, V_{th} is the threshold voltage.

An important parameter of such a device is the transconductance, g_m , which is used to calculate the linear field-effect mobility, μ .

$$g_m = \frac{\partial I_d}{\partial V_g} = \frac{W}{L} C_i \mu V_d \quad (2.2)$$

For higher values of V_d , after pinch-off of the channel, the saturation regime is described by

$$I_{Dsat} = \frac{W}{2L} C_i \mu (V_g - V_{th})^2 \quad (2.3)$$

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Equation (2.1) to (2.3) show that the value of the carrier mobility is a critical parameter defining semiconductors, for it directly controls the level of current output of these devices. Mobility is known as the average drift velocity of carriers per unit electric field in a homogeneous semiconductor and therefore is directly related to the switching speed of the device.

Besides the drain current obtained, I_d , reaching the regime of tenths of microamps, another very important characteristic of such OFETs concerns the dynamic range, or I_{on}/I_{off} ratio, which is defined as the ratio of the current in the “ON” and “OFF” states. This ratio preferred to be as high as possible for practical applications where OFETs operates like a switch, see figure 2.7(b).

Threshold voltage V_{th} is another common characteristic of transistors. It is defined as the voltage that the transistor enters the accumulation mode which is the “ON” state. It is given by the equation:

$$V_{th} = \frac{qdp_o}{C_i} \quad (2.4)$$

Where q is the absolute electron charge, d as the thickness of the organic semiconductor layer, p_o is the charge carrier density at zero voltage. But in experiment analysis, we usually use the extrapolated point of the x -axis from the slope of the plot $\sqrt{|I_d|}$ versus V_g as the threshold voltage of the device; see figure 2.7(b) inset.

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Figure 2.7 (a) Plot of drain current I_d versus drain voltage V_d at different gate voltages V_g from a bottom-contact OFET using PQT-12 as the semiconductor, 100nm thermally grown SiO_2 as the gate insulator, a heavily doped n-type Si wafer as the gate, and gold as source and drain electrodes. (b) Plot of I_d versus V_g at $V_d = -35$ V for the same device, inset is the square root of I_d versus V_g diagram used to decide the threshold voltage. The

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field-effect mobility μ calculated in the saturation regime is $0.087 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and I_{on}/I_{off} ratio is 10^6 .

2.4 Active Materials

The initial studies on organic materials addressed both fundamental issues of the semiconducting and conducting properties and also the great potential presented by a new generation of devices. At present, a number of organic conductor and semiconductor classes has been discovered, which is based on the principal of π -conjugated small molecules and polymers. These results have generated an exciting library of systems that allow the organic electronic solid-state community to draw important relations between molecular structure and structural organization in the solid state, film morphology, and ultimately, electrical performance. The goal of this part is to review fundamental chemical aspects behind the structural design, realization, and charge transport properties, as well as the recent achievements of many organic semiconductors for field-effect transistor (FET) applications.

2.4.1 Semiconductors

Semiconducting materials based on organic molecules and polymers have been the focus of intense investigation for the past 50 years. These structures comprising molecular and polymeric units exhibit the common feature of ' π -conjugated bonds', which give rise to delocalized filled and empty π -orbitals that greatly impact the optical and electrical

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properties. In contrast to inorganic semiconductors, the solid-state structures of these materials are based on weak interactions, principally van der Waals and dipole-dipole interactions, between neighboring molecules/polymer chains imparting properties from conductors to insulators.

To achieve acceptable performance, organic semiconductors must satisfy general criteria relating both the injection and current-carrying characteristics, in particular: (i) the highest occupied/lowest unoccupied molecular orbital (HOMO/LUMO) energies of the individual molecules (perturbed by their placement in a crystalline solid) must be at levels where holes/electrons can be induced at accessible applied electric fields; (ii) the crystal structure of the material must provide sufficient overlap of frontier orbitals to allow efficient charge migration between neighboring molecules; (iii) the solid should be extremely pure since impurities act as charge carrier traps; (iv) the molecules should be preferentially oriented with the long axes approximately parallel to the FET substrate normal since the most efficient charge transport occurs along the direction of π - π intermolecular stacking; and (v) the crystalline domains of the semiconductor should cover the area between the Source and Drain contacts uniformly, hence the film should possess a single-crystal-like morphology [30].

Figure 2.8 and Figure 2.9 shows the chemical structure of some p-type (hole-transporting) and n-type (electron-transporting) semiconductors, with Table 1 reviews their achievement of OFET performance in detail.

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Figure 2.8 Commonly used *p*-type organic semiconductors. F8T2 (poly[9,9-dioctylfluorene-co-bithiophene]); MDMO-PPV (poly[2-methoxy-5-(3,7-dimethyloctyloxy)-1,4-phenylenevinylene]); P3HT (regioregular poly[3-hexylthiophene]); PTAA (polytriarylamine); PVT (poly[2,5-thienylene vinylene]); DH-5T (α,ω -dihexylquinquethiophene); DH-6T (α,ω -dihexylsexithiophene); phthalocyanine; pentacene; α -6T (α -sexithiophene).

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Figure 2.9 Commonly used *n*-type organic semiconductors. NDI (naphthalenediimide); F16CuPc (perfluorocopperphthalocyanine); perylene; PTCDA (3,4,9,10-perylene-tetracarboxylic dianhydride); PDI (*N,N*-dimethyl 3,4,9,10-perylene tetracarboxylic diimide); C₆₀; PCBM, (methanofullerene [6,6]-phenyl C₆₁-butyric acid methyl ester)[31].

Table 1 Highest field-effect mobility (μ) values measured from OFETs as reported in literatures annually from 1986 to 2007.

Year	Mobility	Material	Deposition	W/L*	Ion/Ioff*	Ref
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			Method		ere nce	
1986	10^{-5}	Polythiophene	Solution	NR	10^3	[1]
1988	10^{-4}	Polyacetylene	Solution	750	10^5	[32]
1988	10^{-3}	Phthalocyanine	Vacuum	3	NR	[33]
1992	0.027	Hexathiophene	Vacuum	100	NR	[34]
1992	2×10^{-3}	Pentacene	Vacuum	NR	NR	[34]
1995	0.038	Pentacene	Vacuum	1000	140	[35]
1995	0.3	C ₆₀	Vacuum	25	NR	[3]
1996	0.045	Poly(3-hexylthiophene)	Solution	20	340	[2]
1996	0.62	Pentacene	Vacuum	11	10^3	[36]
1997	1.5	Pentacene	Vacuum	2.5	10^8	[37]
1997	0.05	Bis(dithienothioophene)	Vacuum	500	10^8	[38]
1998	0.1	Poly(3-hexylthiophene)	Solution	20	10^6	[20]
1998	0.23	Dihexyl-quaterthiophene	Vacuum	1.5	NR	[39]
1998	0.15	Dihexyl-anthradithiophene	Vacuum	1.5	NR	[5]
2000	0.1	n-decapentafluoroheptyl-methylnaphthalene-1,4,5,8-tetracarboxylic diimide	Vacuum	1.5	10^5	[4]
2002	0.6	N,N'-dioctyl-3,4,9,10-perylene tetracarboxylic	Vacuum	10	10^5	[40]

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diimide						
2003	0.001	CuPc	Vacuum	165	2.3×10^4	[41]
2003	0.002	Methanofullerene[6,6]- phenyl-C61-butyric acid methyl ester (PCBM)	Solution	140	NR	[41]
2003	0.53	C ₆₀	Vacuum	40	10^8	[17]
2004	0.73	Poly(3-hexylthiophene)	Solution	12	NR	[42]
2004	0.1	PTCDI-C5	Vacuum	10	10^5	[43]
2004	0.004	C ₆₀	Vacuum	250	10^5	[44]
2004	0.2	PCBM	Solution	23	10^3	[45]
2004	0.1	Poly(3-hexylthiophene)	Solution	200	10^5	[46]
2005	0.63	C ₆₀	Vacuum	40	10^4	[47]
2005	0.015	Poly(3,3''-dialkyl- terthiophene) (PQT-12)	Solution	50	10^5	[19]
2005	0.51	Pentacene	Vacuum	40	10^5	[48]
2005	0.06	C ₆₀ -fused(C ₆₀ MC12)	Solution	250	1.6×10^5	[49]
2005	0.02	PCBM	Solution	250	7×10^4	[49]
2006	0.15	PQT-12	Solution	54	10^7	[50]
2006	0.7	Thieno[3,2-b]thiophene	Solution	400	10^6	[6]
2007	0.28	PBTDDT-12	Solution	1600	10^7	[51]

*: W is the device channel width, L is the channel length, I_{on}/I_{off} is the current ratio between device “on” state and “off” state.

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2.4.2 Dielectrics

From the equation 2.1 to 2.3, it becomes immediately evident that for the manufacture of high-quality OFETs, the organic semiconductor is not the only critical component. It is also very important to incorporate a suitable gate insulator. The requirements that a gate insulator material for OFETs must satisfy are rather stringent, with most applicable to gate inorganic transistor insulators as well[52]. The crucial parameters are the maximum possible electric displacement D_{max} the gate insulator can sustain,

$$D_{max} = \epsilon_0 k E_B$$

Where k is the dielectric constant, E_B is the dielectric breakdown field; ϵ_0 is the vacuum dielectric constant; and the capacitance per area C_i is

$$C_i = \epsilon_0 (k / d)$$

With “ d ” as the insulator thickness; the capacitance magnitude is governed not only by the “ k ” value but also by the film thickness “ d ” for which a pinhole-free film should be achieved, and thus may reflect the deposition procedure as well as intrinsic materials properties.

The major motivation to search for SiO_2 alternatives is to significantly reduce the OTFT operating voltage. In fact, while the carrier mobility of organic semiconductors have now approached or surpassed those of amorphous silicon, this has generally been achieved at very large source-drain or source-gate biases, typically greater than 30 V. OFET operation employing such large biases will incur excessive power consumption. Furthermore, note that in such devices, the semiconductor carrier mobility is gate-bias dependent and it increases when the gate voltage increased. Therefore, according to

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equation 2.1, 2.3, a viable approach to substantially increasing the drain current while operating at low biases is to increase the capacitance of the dielectric materials.

The second motivation is that OFET gate insulators must fulfill demands specific to organic electronics, which include low-cost and low-temperature manufacturing of organic electronic circuits[10, 28]. OFET gate insulators should ideally be compatible with flexible substrates and be processible or printable from solution, but should also be insoluble in the solvent used for deposition of the organic semiconductor (in the case of bottom-gate structures), and should be compatible with the gate line-deposition process (in the case of top-gate configurations). The confluence of these three important goals has stimulated new research approaches, which can be divided in three major classes: high- k inorganic, polymers, and self-assembled small molecules. Figure 2.10 shows the chemical structure of commonly used organic dielectric materials [7].

Figure 2.10 Chemical structures of commonly used organic dielectrics. PVP, (poly(4-vinyl phenol)); PS, (polystyrene); PMMA, (polymethyl-methacrylate); PVA, (polyvinyl

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alcohol); PVC, (polyvinylchloride); PVDF, (polyvinylidenefluoride); P α MS, (poly[α -methylstyrene]); CYEPL, (cyano-ethylpullulan); BCB, (divinyldimethylsiloxane-bis(benzocyclobutene)) [7].

2.4.3 Conductors

For conductors, conducting polymers are most desirable because of their mechanical flexibility and processability. Commonly used ones are poly (3, 4-ethylenedioxythiophene)/poly (styrene sulfonate) (PEDOT: PSS)[21], polyaniline (PANI)[53], various polypyrroles (PPy)[54], as well as graphite-based inks [55] (Fig. 2.11). However, the conductivities and electrical/thermal stability of conducting polymers are still lower than required, especially for interconnecting lines over large areas. Recently, people has developed methods to use the gold nanoparticles[55] and silver nanoparticles[50] to form thin conducted film from solution in low temperature. This provided us a simple approach to a printable metal conductor for microelectronics, which exhibit high electrical conductivity similar to that of a vacuum-deposited metal conductor yet worked far more efficiently as electrodes in organic TFTs.

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Figure 2.11 Chemical structures of some conducting polymers used in OFETs: PEDOT: PSS (poly [3, 4-ethylenedioxythiophene]/ poly [styrene sulfonate]), PANI (polyaniline), Ppy (poly [N-methylpyrrole]) [30].

CHAPTER 3 RESEARCH METHODOLOGY

3.1 Introduction

Characterization methodology of organic semiconductor materials and their devices is of great importance. To systematically study OFETs, we use different advanced equipment and methods in our experiments. In this research, some methodologies are innovatively used and even further developed for high performance devices and precise characterizations.

3.2 Characterization of organic semiconductor

3.2.1 UV-visible spectrophotometry

Ultraviolet-visible spectrophotometry uses light in the visible and adjacent near ultraviolet (UV) and near infrared (NIR) ranges. In this region of energy, polymeric molecules undergo electronic transitions. This spectroscopy is routinely used in the quantitative determination of highly conjugated organic compounds.

In our experiment, the equipment used was HITACHI, U-2800. It has a detection range from 200nm to 1100nm of wavelength. By this method, we verify the successful deposition of organic layer and for semiconductor materials, the onset point of absorption can be used to decide the band gap (difference of energy between HOMO and LUMO).

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3.2.2 Electrochemical method

A simple method for quickly assaying the HOMO and LUMO of a semiconductor material is the robust technique of cyclic voltammetry. In solution, an organic semiconductor can have electrons added or removed by changing the potential of a working electrode. The technique of cyclic voltammetry uses three electrodes to control and measure the flow of electrons (current) which are added (removed) to (from) molecules as a function of potential. The working electrode sweeps potential, the ground counter electrode provides a second terminal for the current flow, and a third electrode serves as a “reference”. When the working electrode is swept negatively, electrons are added to the molecule (reduction) and an increase in the current is observed. As the voltage is swept positively, the added electrons come back off the molecule, and eventually, at a high positive voltage, electrons are removed from the molecule by oxidation.

In our experiment, the CHI 660B (CH Instruments, Austin, TX) was used as our electrochemical workstation. Other experiment conditions were like:

Electrolyte: 0.1 M (Bu_4NPF_6) dissolved in anhydrous acetonitrile;

Working electrode: Glass carbon;

Counter electrode: Platinum

Reference electrode: Ag/AgCl

Organic materials were measured in thin film states, which were prepared by dropping a solution of semiconductor on glass carbon electrode and drying for 5 hours in vacuum at room temperature.

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3.2.3 Raman spectroscopy

Raman spectroscopy is a spectroscopic technique used in condensed matter physics and chemistry to study vibrational, rotational, and other low-frequency modes in a system. It relies on inelastic scattering of monochromatic light, usually from a laser. The laser light interacts with phonons or other excitons in the system, resulting in the energy of the laser photons being shifted up or down. The shift in energy gives information about the phonon modes in the system. Here in our study, Raman spectra were collected with a scanning Raman microscope “CRM 200” (WITec, Germany) in backscattering geometry. The Raman system was equipped with an Ar⁺ laser (LASOS, LGN7812) with the excitation source at 488 nm and a charge couple device (CCD) detector. The highest grating was adopted to reach a resolution of less than 2 cm⁻¹.

3.2.4 X-ray diffraction

The crystal structures of the organic semiconductors were characterized by X-ray diffraction (XRD, D/max-2400 Rigaku, Japan) with Cu K α radiation ($\lambda = 1.54178 \text{ \AA}$) operating at 50.0 kV and 200.0 mA.

X-ray diffraction (XRD) is a versatile, non-destructive technique that reveals detailed information about the chemical compositions and crystallographic structures of natural and synthetic materials. A polymer can be considered partly crystalline and partly amorphous. The crystalline parts give sharp narrow diffraction peaks and the amorphous components give very broad peaks. The ratio between these intensities can be used to calculate the amount of crystallinity in a material. And normally, we believe the higher

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percentage of the crystalline parts in a semiconductor, the higher mobility it can achieve in an OFET device [55].

3.2.5 Differential scanning calorimetry

Differential scanning calorimetry (DSC) is a thermoanalytical technique in which difference in the amount of heat required to increase the temperature of a sample and reference is measured as a function of temperature. By observing this difference in heat flow, the physical transformation of the material such as melting, crystallization and glass transition point can be determined. In our study, DSC analysis was conducted on a TA Instruments DSC 2910 at a heating rate of 5 °C per min under nitrogen atmosphere.

3.2.6 Atomic force microscopy

The Atomic force microscopy (AFM) experiments were performed with a Nanoman multimode scanning probe microscope (Veeco, Santa Barbara, CA) operated at ambient conditions. Si tips with a resonance frequency of approximately 300 kHz and a scan rate of 1 Hz were used. All AFM measurements were done in the tapping mode, which enable the acquisition of topographical and phase images at the same time. Phase images are especially useful for direct visualization of the organic polymer samples. The contrast in phase image comes from the phase shift of the oscillating cantilever relative to the driving signal when it interacts with the sample. The phase contrast essentially arises from the difference of energy dissipation during tip-sample interaction. This enables it to

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differentiate areas with different viscoelastic properties.

3.2.7 Scanning Tunneling Microscopy

Scanning tunneling microscopy (STM) is the most potent tool for studying the microscopic structure of molecules adsorbed onto a solid substrate. By employing the quantum tunneling mechanism, it is able to obtain sub-molecular or even atomic resolution images of self-organized molecular structures. STM measurements were performed at the *n*-tetradecane/substrate interface at room temperature in the constant current mode using a Pico LE SPM system (Molecular Imaging). STM tips were prepared from Pt/Ir (90:10) wire by mechanical cutting. HOPG substrates were freshly cleaved prior to deposition. A small amount of the sample was dissolved in *n*-tetradecane (Aldrich, 99+ %) prior to droplet deposition onto the HOPG substrates before imaging.

3.3 Device fabrication and thin film growth

Organic field effect transistors used in our experiment were constructed in a bottom-contact common top-gate configuration. The fabrication process consists mainly four parts: (1). Substrate preparation; (2) Semiconductor solution preparation; (3). Thin film deposition process and (4) Post-annealing treatment; thin film growth is one of the most important steps in making an optimal OFET. Important parameters that should be controlled are the deposition methods, substrate modifications, solvent evaporation rates and annealing temperatures. These parameters play an important role in determining

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structural defects, molecular alignment, and charge trapping density as well as crystal grain size; all of which are important for OFET operation.

3.3.1 Substrate preparation

The field effect transistor substrate was made using heavily doped N-type silicon wafers as the common gate electrode and a 100nm thermally oxidized SiO₂ layer as the gate dielectric. Then gold source and drain electrodes were patterned in a bottom contact configuration using conventional photolithography method. A 10nm layer of titanium was used acting as an adhesion layer for the gold on SiO₂. Here we employ the ring-type geometry of source and drain electrodes in order to eliminate the parasitic leakage path from source to drain electrodes, as showed in Figure 3.1.

Figure 3.1 Schematic diagrams and the real picture of the ring-type source and drain patterned substrate.

All substrates were cleaned with standard procedure before use. Blend sulphuric acid with hydrogen peroxide at the ratio of 7:3 then heated to 80 degree on the hot plate. Soak

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the silicon wafer in the solution for 30 minutes. When finished, rinse the wafer with overflowing DI water completely. For some of the experiment, where deposition of silane is needed, the wafer was exposed to oxygen plasma treatment before use, this is to increase the surface energy of the wafer and thus facilitate the covalent bond between silane and the silicon dioxide surface.

3.3.2 Semiconductor solution preparation

The semiconducting polymers used in our experiment can be easily dissolved in normal organic solvents like chlorobenzene, dichlorobenzene, chloroform, toluene, etc. But the performances of the devices vary with the solvents; possibly result from different solubility and the interaction between the solvent and the material. Hence, optimization of the experimental condition was conducted. Beside normal solution, nanoparticle dispersion of the material in environmental friendly solvent was also prepared. The nanoparticle dispersion was formed by adding polymer PBTDTT-12 powder into pure hexane solvent, and then went through nearly 1 hour ultrasonic agitation treatment at 50 °C until the mixture became a purple dispersion.

3.3.3 Film deposition

Both spin coating and solution casting are commonly used methods for solution deposition. In the spin coating method, the solvent dries relatively fast allowing less time for molecular ordering compared to that in solution casting. But the film uniformity is

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usually better for spin coated films. These films can be annealed afterward to improve molecular ordering as discussed later.

For solution deposition, semiconductor concentration, solvent evaporation rate, solubility of the semiconductor and the spin rate for spin coater play important roles in the quality of the resulting semiconductor films.

Here in our experiment, we chose to use the solution casting method because after modification of dielectric and electrode, the surface of the device substrate was hydrophobic, which was not suitable for high speed spin coating.

3.3.4 Post-deposition annealing

Post-deposition annealing is commonly used to improve device performance after deposition[6, 19, 46, 56]. The reasons cause this improvement are the fully evaporation of the residue solvent and more importantly, the reorganization of the organic molecular and thus the thin film morphology change. When spun from solution, good semiconducting molecules exhibited a great tendency to form π - π stacking in view of their intrinsically excellent self-organization capability. However, because of the competition between the crystallization and substrate pulling, only nanosized crystallites containing a small number of stacked molecules were formed. But after being heated to certain temperature, normally the phase transition point, mobility of the molecules is substantially greater, the backbone of the molecules is disrupted and the reorganization of the π - π stacking arrays occurred. The polymer molecules are thus able to rearrange to form long-range ordered π - π stacking structure upon slow cooling to room temperature overnight[19]. This ability to form long-range order allowed adequate morphological

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development. The morphology change leads to a much larger grain size and smoother grain boundary, which eventually lead to a more efficient charge transport in the conducting channel and achievement of high mobility of the semiconductor material.

3.4 Electrical characterization

OFET electrical characterization was performed in a probe station built by Cascade Microtech (USA). Triaxial electrical feedthroughs allow current sensitivity down to the sub-femtoamp level. The build-in microscope allows viewing the electrodes nanostructures on device substrates clearly so as to locate the precise location as where the probe should be placed. The roll-out chuck in the chamber is able to move in all three axes to locate samples. For performing variable temperature measurements, the probe-station is equipped with a thermochuck system (TPO3000, Temptronic, USA), which can change the temperature of detection chamber from -60°C to 200°C. Gases (e.g. oxygen; nitrogen) can be bled into the chamber, and the subsequent pressure is monitored with a cold cathode ion gauge.

Current and voltage were applied and measured using Agilent E5270B 8-Slot Precision Measurement Mainframe. The E5270B offers a flexible solution for parametric characterization of semiconductor devices, with voltage measurement resolution down to 0.5 microvolt and current measurement resolution down to 0.1 femtoamps. Three different source/monitor unit (SMU) types are available to meet a variety of parametric measurement challenges: a medium power SMU (MPSMU), a high power SMU (HPSMU), and a high resolution SMU (HRSMU). An optional auto-sense and switch unit

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(ASU) works with the HRSMU to provide 100 amps of current measurement resolution. The ASU enables switching between SMU-based measurement (current-voltage) and capacitance meter based measurement (capacitance-voltage) without having to change any cables. Data from the E5270B was acquired via a GPIB interface to a PC computer running a powerful LabView driver program called ICS.

The current-voltage detection setup of an OFET device is showed in figure3.3. One SMU was connected to a tungsten pin which breakthrough the semiconductor thin film and precisely touch the source electrode, another was connected to drain electrode at the same way. Finally, the high doped silicon gate electrode was contacted with the metal chuck surface directly, a vacuum pump make sure the contact was tight that no significant resistance existed between interfaces.

For a working transistor device, as mentioned in previous chapter, normally two characteristic curves need to be tested: the output curve and the transfer curve. For output test, a constant zero voltage was applied to source electrode and a sweeping mode negative voltage was applied to drain electrode since PQT-12 was a p-type semiconductor, a negative bias voltage can make it work under accumulation mode. And a stepped negative gate voltage was also applied to induce the electrical field. At the same time, all currents from source, drain and the gate were monitored and recorded. The output characteristic of a transistor was used to determine the gate modulation of semiconductor channel conductivity, as well as the linear and saturation region of device. The transfer test was divided into two parts, one was in the linear region and another was in saturation region. The difference between those two was the value of constant voltage applied to drain electrode, which was determined from the output curve. The source

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electrode was still grounded. And for the gate electrode, this time a DC voltage was swept from positive to negative. The transfer characteristic can give the information about ON/OFF ratio and the threshold voltage of the device.

All electrical detections were performed in a dark ambient atmosphere.

Figure 3.2 Probe station

Figure 3.3 Illustration of the electrical measurement setup. Source and drain probes need to breakthrough the organic film for spin coated semiconductor, gate probe was on metal chuck surface.

3.5 Protocol developed for fabrication of OFETs

3.5.1 Surface modification of the dielectric layer with SAMs

In the field-effect device structures, the conduction channel exists at the interface between organic thin films and SiO₂ gate insulators. Here, we used organosilane self-assembled monolayers (SAMs) growing on SiO₂ insulator to control the device performance.

The device has to be cleared of organic residue from the photolithography process before different self-assembled silane monolayers can be deposited using the following steps:

- (1) First, the silicon wafer was cleaned by standard procedures and then heated to around 110 °C for 20mins by a hotplate to get rid of water molecules, thus facilitate the SiO₂ surface modification by silane.
- (2) Second, SiO₂ surface was modified by immersing the clean wafer substrate in toluene solution of different silanes at 60 °C for one hour. The concentrations of all silanes were kept at 10mM.
- (3) Cooled the device to room temperature and then completely rinsed with toluene and 2-isopropanol; afterwards, blowed to dry by nitrogen gas.

Water contact angle characterization and XRD were used to confirm the successful deposition of silanes, details can be found in the preliminary result part.

The semiconductor material was then deposited on top of the SAMs by solution casting onto the whole OFET substrates.

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3.5.2 Temperature dependence of the device performance

An important aspect for the commercialization of any new device technology is stability. Although we have made great progress in OFET device fabrication and its performance in the last decade, there is still considerable skepticism about whether molecular materials possess adequate stability to meet the extreme working conditions required for any type of practical devices. In the real application, we need to consider the huge amount of heat dissipation during the working of circuit, which would elevate the environmental temperature and affect the OFETs performance. Therefore, we investigated the device degradation under high temperature and the causing effect..

The effect of temperature on the stability of the OFET was investigated with the use of the Temptronic Thermochuck. The device used in this experiment was fabricated almost the same as the one in SAMs modification, except this time the organosilane used was always octyltrichlorosilane (OTS-8). At first, a high performance OFET device was fabricated, and then tested under different temperatures. The temperatures at which the I-V characteristics obtained were 40 °C, 60 °C, 80 °C, 100 °C, 140 °C, 160 °C, 180°C and 200 °C. The drain current, threshold voltage as well as the mobility change versus the test temperature were investigated.

For PQT-12 based devices, a further investigation was conducted by fabricating a series of devices in same method but annealed at different temperatures. The temperature under which the device annealed were room temperature, 60 °C, 80 °C, 100 °C, 140 °C and 160 °C. Afterwards, all devices were tested under normal conditions, e.g. room temperature at ambient environment. This experiment was aimed at helping to determine the radical reactions causing the performance change under enhanced temperature.

3.5.3 OFETs device stability based on bias-stress effect

Study of the electrical stability of polymeric OFETs is essential to their adoption in practical applications. Although gate-bias stress is an important electrical characteristic for determining the lifetime of OFETs in applications such as displays, there is no fundamental understanding of how to design a semiconductor material free from bias stress[30].

In our experiment, we investigated the long-time bias-stress effect on PQT-12 based devices. Bias stress effect was an important phenomenon in disordered organic semiconductors based devices. It often manifests itself as a decay of the output current caused by the prolonged operation of the transistor. This was the first time a multiple bias condition and long time (up to 24 hours) stress investigation on this material. At first, six high-performance OFETs with PQT-12 as the semiconductor material were fabricated with the same procedure in Chapter 3.5.2. All devices were fabricated under strictly same conditions to eliminate the environmental factors on performance. Then, tested the device before applying any bias, collected the standard curve. Afterwards, a constant bias applied on both gate and drain electrode for several seconds, collected the output as well as the transfer curve again for comparison. Continued the stress again for 2 to 3 minutes, collected the output and transfer curve as before. Continued this procedure till stress time up to several hours and repeated this electrical detection process for six bias conditions, as showed in table 2.

Table 2 Different bias stress intensities

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Device	Bias Condition	
	Drain Voltage (V)	Gate Voltage (V)
1	-40	-40
2	-20	-40
3	-10	-40
4	-5	-20
5	-40	-20
6	-40	-5

Studies of gate-bias stress will be essential for materials to determine their operating range and to optimize dielectric layer. It is doubtful that bias stress can be completely eliminated but its mitigation by materials and device design in combination with driving conditions is a necessity.

CHAPTER 4 ORGANIC FIELD EFFECT TRANSISTOR BASED ON POLY (3, 3''-DIALKYL-TERTHIOPHENE) (PQT-12) AND ITS DEVICE PHYSICS INVESTIGATION

4.1 Characterization of semiconductor material

Regio-regular polythiophene, poly (3, 3'''-dialkylquaterthiophene), PQT-12 (Fig 3.1), is one of the organic materials that provides both high field effect mobility and proper resistance to adverse environmental effects [50]. It has an electronic structure favorable for charge transport with ability to self-organize from solution to form proper structural order in the solid state, which gives good mobility just from solution deposition.

Therefore, the first stage of my research was based on this material; PQT-12 was used as the active semiconductor to investigate the interface match and OFET device stability.

Figure 4.1 Chemical structure of PQT-12

4.1.1 UV-visible spectrophotometer

According to formula

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$$E = h\nu = \frac{hc}{\lambda}$$

Where h is the planks constant, ν is the frequency of the photon, c is the velocity of light and λ is the wavelength of the photon, we can calculate the band gap energy from the onset point of the light absorption. For PQT-12, the value is around 1.79ev. And thin film spin coated from the nanoparticle dispersion in dichlorobenzene onto a quartz slide exhibited well defined vibronic splitting at $\lambda_{max} = 545$ nm, and 585 nm, reflecting the high structural order in the thin film.

Figure 4.2 UV-visible spectrum of PQT-12 on quartz slides

4.1.2 Electrochemical cyclic voltammetry

Cyclic voltammetry (CV) is a well-tried method for the determination of oxidation and reduction potentials of different polymers[57], which allows calculation of their

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HOMO/LUMO levels. These values give valuable information, e.g. which semiconductor material can or should preferably be combined with which source and drain conductors for the promising fabrication of OFETs. According to the empirical equation $E_{HOMO/LUMO} = [-exp(E_{onset} (vs. Ag/AgCl) - E_{onset} (Fe/Fe^{+} vs. Ag/AgCl))] - 4.8\text{eV}$ [58] (including the ferrocene value -4.8eV with respect to the vacuum level, which is defined as being zero), the HOMO/LUMO levels can be estimated from the $E_{onset}^{ox}/E_{onset}^{red}$ values.

HOMO of PQT-12: 5.24eV

LUMO of PQT-12: 3.16eV

Electrochemical band gap: 2.08eV

Figure 4.3 Cyclic voltammograms of the electrochemical oxidation and reduction of PQT-12 thin film in 0.1 M Bu_4NPF_6 anhydrous acetonitrile at a sweep rate of 20mV/s.

4.1.3 Raman spectrophotometer

We investigated the Raman spectrum of PQT-12 on both silicon dioxide substrates and gold substrates with different concentrations, see figure 4.4. The substrates and

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concentrations have no effect on the position of characteristic scattering peaks of Raman spectrum, but the intensity of the scattering increases with concentrations.

Figure 4.4 Raman spectrum of PQT-12 thin film of different substrate and concentrations

4.1.4 X-ray diffraction

PQT-12 is a microcrystalline polymer. It can form highly ordered lamellar domains with two-dimensional sheets of conjugated polymeric backbones and with con-facial π - π interchain stacking separated by layers of alkyl side chains. From the width of X-ray diffraction peaks, the typical crystallite size has been estimated to be on the order of 50-150nm, these microcrystalline domains are separated by regions with more disordered microstructures.

XRD of thin film sample of PQT-12 exhibit two diffractions at $2\theta = 4.97$ and 10.10° , revealing an interchain d spacing of 17.7 Å and a π - π stacking distance of 8.7 Å (Figure 4.6). The d spacing was calculated from Bragg's law:

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Figure 4.5 XRD of silane modified substrate, the inset shows the XRD of bare silicon dioxide without any modification.

Figure 4.6 XRD of PQT-12 on different SAMs modified substrates, a small amount of peak shift can be observed.

4.2 Effect of organosilane modification

OFET performance depends largely on the semiconductor/dielectric interface[59]. The purpose of this part of work is to show that the performance of OFETs can be improved by controlling the chemistry of the dielectric/polymer interface. We chose to use SiO₂ as the substrate isolator because of its well-characterized properties (dielectric constant, breakdown voltage, and surface roughness) and ease of chemical modification. Derivatizing the dielectric surface with organosilane self-assembled monolayers (SAMs) prior to the deposition of semiconductor leads to a significant change on the device performance.

1. The organosilanes we chose to use and the according device performances are:

(1). Octadecyltrichlorosilane (OTS-18)

(2). Dichloro (methyl) phenylsilane

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(3). Trimethoxymethylsilane

(4). Phenyltrimethoxysilane

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(5). Octyltrichlorosilane (OTS-8)

(6). Hexamethyldisilazane (HMDS)

(7). (3-Mercaptopropyl) trimethoxysilane (MPTS)

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(8). Chlorotrimethylsilane

(9). (3-Aminopropyl) trimethoxysilane (APTS)

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The effect of SAMs modification on the transistor devices performance are summarized in Table 3.

Table 3 SAMs modified device performance

No	Silane	Mobility [cm^2/vs]	Threshold Voltage [V]	ON/OFF
1	Octadecyltrichlorosilane	0.059	9.96	$10^{5.5}$
2	Dichloro (methyl) phenylsilane	0.016	9.96	$10^{5.5}$
3	Trimethoxymethylsilane	0.027	17.92	10^6
4	Phenyltrimethoxysilane	0.0012	14.10	10^5
5	Octyltrichlorosilane	0.087	13.68	10^6
6	Hexamethyldisilazane	0.048	18.21	10^5
7	(3-Mercaptopropyl) trimethoxysilane	0.004	21.40	10^3
8	Chlorotrimethylsilane	0.016	19.92	10^6
9	(3-Aminopropyl) trimethoxysilane	0.0002	22.32	10^4

2. The water contact angle detection

From the water contact angle results (table 4), we find that the original hydrophilic surface of silicon dioxide changes to a hydrophobic one, confirms the successful growth of organosilanes. This is because the $-\text{OH}$ terminal group of SiO_2 has been changed to $-\text{CH}$, phenyl or some other groups by the silane monolayer.

Table 4 Water contact angle detection

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(Reported contact angles are the average of at least 4 measurements.)

Sample No.	Water (degree)	Organic solvent (degree)
Bare SiO ₂	28.36	20.09
SAMs 1	95.76	8.22
SAMs 2	79.87	10.88
SAMs 3	109.48	11.98
SAMs 4	83.85	17.49
SAMs 5	121.70	14.57
SAMs 6	139.48	11.98
SAMs 7	56.56	6.25
SAMs 8	56.14	5.04
SAMs 9	86.14	8.13

3. AFM of both silane- modified substrate and the organic semiconductor layer on top of it.

Silane No.1: Hexamethyldisilazane (HMDS)

Roughness of the substrate: **1.793 nm**

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Figure 4.7 From left to right, in the first row is the top view, phase view and 3D view of the HMDS substrate; in the second row is the top view, phase view and 3D view of the PQT-12 layer.

Silane No. 2: Dichloro (methyl) phenylsilane (DMPS)

Roughness of the substrate: **3.24nm**

Figure 4.8 From left to right, in the first row is the top view, phase view and 3D view of the DMPS substrate; in the second row is the top view, phase view and 3D view of the PQT-12 layer.

Silane No.3: Octyltrichlorosilane (OTS-8)

Roughness of the substrate: **0.528nm**

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Figure 4.9 From left to right, in the first row is the top view, phase view and 3D view of the OTS-8 substrate; in the second row is the top view, phase view and 3D view of the PQT-12 layer.

All the SAMs are confirmed to be successfully assembled and the coverage is very high and even.

The according electrical performance of transistor devices made on those modified substrate is showed in figure 4.10. We can see that the drain current is positively proportional to the dielectric surface roughness.

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Figure 4.10 Drain current from three different substrates, the value of the drain current is positively proportional to the dielectric surface roughness detected by AFM.

Self-assembled organosilane monolayer has been demonstrated to influence both the field effect mobility and threshold voltage of OFETs. In addition, SAM-coated dielectrics have been shown to have a strong effect both on the morphology of thin films of organic polymers and on the electrical performance of OFETs.

4.3 Temperature dependent annealing and device stability

4.3.1 Introduction

In this study, we anneal and test the device under different temperatures, investigate the device degradation under high temp, and then suggest the reason cause this phenomena.

Variable temperature OFET measurements can be used to determine the temperature dependence of the mobility in a semiconductor thin film. The temperature dependence of the mobility can yield information about the conduction mechanism and trap states in the semiconductor.

4.3.2 Experimental results

1. OFET devices annealing under different temperature.

(1).Annealing temperature: room

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(2). Annealing temperature: 80 degree

(3). Annealing temperature: 100 degree

(4). Annealing temperature: 120 degree

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(5). Annealing temperature: 140 degree

(6). Annealing temperature: 160 degree

2. Effects of enhanced testing temperature

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Figure 4.11 Drain current versus drain voltage at $V_G = -40$ V under different temperatures.

Figure 4.12 Square root of drain current versus gate voltage at saturation regime ($V_D = -35$ V)

Figure 4.13 Mobility and threshold voltage change with temperature. Both parameter decreases dramatically between 120 and 140 °C.

4.3.3 Discussion

The annealing process is very important to OFET performance. For PQT-12, the device annealed at the 120 to 140 °C gives the best performance. This is because the Differential Scanning Calorimeter (DSC) of PQT-12 showed liquid crystalline characteristics with two endotherms at ~120 °C and ~140 °C, corresponding to the crystalline-to-liquid crystalline and liquid crystalline-to-isotropic phase transitions, respectively. At the crystal-to-liquid crystal phase transition temperature above 110 °C, the mobility of the molecules is substantially greater, and the reorganization of the π - π stacking arrays occurred, leading to the formation of mosaic crystal domains. Increasing the temperature up to the melting region (at 148 °C) disrupted the π - π stacking between polymer backbones and completely relaxed the molecules; the polymer molecules were thus able to rearrange to form long-range ordered π - π stacking structure upon slow cooling to room

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temperature overnight[19]. This ability to form long-range order allowed adequate morphological development.

The mobilities of semiconductor are dependent on the operating temperature. As illustrated in figure 4.13, the mobility would decrease as temperature increases. The other two important parameters—threshold voltage and On/Off ratio of the device are also investigated. Figure 4.13 shows that the threshold voltage gradually shifts to the negative direction with the temperature increasing up to 480K and figure 4.12 shows that On/Off ratio are lower as the temperature increasing. These phenomena could be explained by the stability of the organic material in air, which has been extensively studied in terms of the effects of oxygen and humidity[60, 61]. In the normal ambient, although PQT-12 shows more resistance to environmental influence than other polymer semiconductors, it is still demonstrated that oxygen can react with PQT-12 which increases its doping level, thus increases the *Off* current of the transistor. And water molecules could form a dipole layer at the insulator-semiconductor interface making the transistor harder to be turned off. This could explain our results. When the temperature is increased, oxygen could more effectively react with the PQT-12. On the other hand, the concentration of water molecules reduces with the increasing temperature, thus resulting in the negative shift of the threshold voltage and decreasing On/Off ratio.

New electronic states near the top of the highest occupied molecular orbital (HOMO) can also be generated by the enhance temperature. Therefore, the shape of the transfer characteristics of the transistor is affected. As the device turn on, charge must fill the new states. Because these are shallow trap states, they contribute only practically to the output current through thermal excitation into conducting states. The result is broader

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sub-threshold area than an unstressed device, which also leads to a V_{th} shift, and a reduced apparent mobility as shown in figure 4.12.

4.4 Long-term bias stress effect and recovery

It is important to minimize the device instability in order to facilitate the development of reliable devices and applications. It has been observed by many authors that the electrical performance of organic field effect transistor devices can change significantly with time due to the electrical instabilities of the device[62-65]. The examination of the bias stress effect in the OFET is one of the appropriate methods to investigate and understand the cause of the device degradation. For the measurement, negative gate and drain bias are applied to the device with different intensities. Device characteristics are measured at various time intervals.

4.4.1. Bias- stress effect

Bias stress can be due to either a structural degradation of the semiconductor material—which leads to a decrease of the effective carrier mobility μ , or to trapping of mobile charges in non-conducting states—which leads to a threshold voltage shift but no change in mobility when all the traps are filled. From figure 4.14 and figure 4.15, we find that for semiconductor material PQT-12, the mechanism underlying the stress effect should be due to the trapping of mobile charges. Trapping can occur in the semiconductor, in the gate dielectric or at the dielectric-semiconductor interface. The electrostatics of thin-film transistors dictate that all the induced charge is located within 5nm of the dielectric –

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semiconductor interface, Therefore, the physical phenomena associated with bias stress should occur near this interface.

Different trapping processes lead to changes of transfer curves before and after electrical stressing. Carriers trapped in localized states at the dielectric –semiconductor interface form an immobile charge density distribution which shields the gate voltage. When the gate voltage overcomes this electrostatic screening, the device characteristics are identical to those of a pristine device. This type of degradation gives rise to a V_{th} shift in the direction of the gate bias but no change in overall shape of the transfer characteristics and the carrier mobility, as shown in figure 4.15. The V_{th} shift is equal to N_{trap}/C_i , where N_{trap} is the density of trapped charge, C_i is the capacitance per unit area.

Figure 4.14 Time dependence of the output drain current of a PQT-12 OFET after a drain voltage = -40V and gate voltage = -20V is applied.

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Figure 4.15 Time dependence of the threshold shift of a PQT-12 OFET after a drain voltage = -40V and gate voltage = -20V is applied.

Figure 4.16 Time dependence of the threshold shift of a PQT-12 OFET after a constant gate voltage (left) or a constant drain voltage (right) are applied, measured at different drain voltages (left) or different gate voltages (right) as shown, respectively.

4.4.2 UV illumination recovery process

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Devices subjected to bias stress recover to their original state within hours when re-annealed at vacuum environment. Recovery is much faster, however, when the OFET is subjected to illumination. Figure 4.17 shows the result of recovery and it is observed that after a short time of exposure to above band-gap UV illumination, the device restore to its original state. At the end of the recovery process, the transfer characteristic is essentially identical to that of the unstressed device. The progressive threshold voltage recover depends on the intensity and duration of the optical irradiation. The cycles of stress and recovery by illumination are repeated many times with no sign of changes in behavior. We discussed earlier that bias stress is due to the presence of a trapped sheet of charge near the interface; hence the recovery reflects the removal of this charge---holes and electrons which are thermally excited to form interface states.

Figure 4.17 The recovery of threshold voltage of a device subjected to bias stress by above band-gap UV illumination.

CHAPTER 5 POLY (2, 6-BIS (3-ALKYLTHIOPHEN-2-YL) DITHIENO [3, 2 -B; 2', 3'-D] THIOPHENE) (PBTDDT-12): A NEW HIGH-PERFORMANCE P-TYPE ORGANIC SEMICONDUCTOR FOR THIN FILM TRANSISTORS

5.1 Introduction

A newly synthesized p-type semiconducting polymer---poly (2, 6-bis (3-alkylthiophen-2-yl) dithieno [3, 2-b; 2', 3'-d] thiophene) (PBTDDT-12) is characterized with different techniques and OFET devices based on this material are fabricated. The rationale for this semiconducting polymer design is based on the following considerations: (i) the relatively large and planar structure of DTT moieties on the polymer backbone would promote strong π - π stacking and facilitate charge carrier transport via hopping mechanism; (ii) the large resonance stabilization energy of DTT units would also suppress electron delocalization along the backbone and reduce the effective π - π conjugation length, thus giving rise to a lower HOMO level, and higher stability against oxidative doping; (iii) the regioregular placement of long alkyl side-chains along the polymer backbone would enable solution process and encourage molecular self-organization via intermolecular inter-digitations.

5.2 Material synthesis and characterizations

5.2.1 Synthesis route

As shown in Figure 5.1, the polymer is prepared via Stille coupling polymerization of 2,6-bis-trimethyl-stannanyl-dithieno[3,2-b;2',3'-d]thiophene [67] with 5,5'-Dibromo-4,4'-dialkyl-[2,2'] bithiophene [68] in good yields. It is purified by sequential Soxhlet extraction with hexane and ethanol. The isolated polymer product is soluble in THF, CHCl_3 , chlorobenzene, *etc.* Gel-permeation chromatography analysis of the product, PBTDDT-12 ($\text{R}=\text{n-C}_{12}\text{H}_{25}$), in THF solution showed a number-average molecular weight of 7900 with a polydispersity (M_w/M_n) of 1.3 against polystyrene standards. All reagents were used as received from Sigma-Aldrich. A typical experimental procedure was as follows:

Into a Schlenk flask was added 2,6-Bis-trimethylstannanyl-dithieno[3,2-b;2',3'-d]thiophene (1 equivalent), 5,5'-Dibromo-4,4'-didodecyl-[2,2']bithiophene (1 equivalent), tri(o-toyl) phosphine (8 mol% equivalent), tris(dibenzylideneacetone)dipalladium (2 mol% equivalent) and dry chlorobenzene (30 ml) under nitrogen protection. The flask was securely sealed and stirred for 48 h at 120°C. After cooling to room temperature, the reaction mixture was precipitated into a mixture of methanol (100 ml) and concentrated hydrochloric acid (4 ml) and stirred for 16 h. The precipitate was collected, and Soxhlet extracted with hexane and ethanol for 48 h each, and dried under vacuum. The bulk product yield by this procedure was 89%. Anal. Calc. For $\text{C}_{40}\text{H}_{56}\text{S}_5$ C 68.91%, H 8.10%, S 22.99%; Found C 69.1%; H 8.2%; S 22.7% $^1\text{H-NMR}$ (300MHz, CDCl_3) δ 7.32 (s, 2H), 7.05 (s, 2H), 2.79 (br, 4H), 1.69 (br, 4H), 1.26 (br, 36H), 0.87 (t, 6H)

Figure 5.1 Synthesis of poly (2, 6-bis (3-alkylthiophen-2-yl) di- thieno [3, 2-b; 2', 3'-d] thiophene) (PBTDTT-12)

5.2.2 UV-vis spectrometer

The UV-vis spectrum of the dilute solution of PBTDTT-12 in chlorobenzene shows absorption peaks at 489, 558, and 605 nm with distinct vibronic splitting characteristics (Figure 5.2). The spectral absorptions of PBTDTT-12 thin film are slightly red shifted, exhibiting well-defined vibronic splitting at absorption maxima 520, 558, and 605 nm, reflecting the higher structural order in the thin film. The similarity of the absorption spectral patterns between the thin film and solution suggests that the polymer sample in the solution exists predominantly as a nanoparticle form, possessing similarly ordered structures as in the thin film. Light-scattering measurements on polymer solution in chlorobenzene indicate a suspension of nanoparticles with particle size around 90 nm.

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The suspension of PBTDTT-12 nanoparticles is very stable because when the dilute solution is heated above 60°C, the absorption spectrum of PBTDTT-12 still shows the vibronic splitting characteristic, and no gelation occurs when the solution is cooled to room temperature.

Figure 5.2 UV-vis absorption spectra of PBTDTT-12: Trace (a): absorptions of a solution cast film of PBTDTT-12 (red dash dot line); (b) absorptions of dilute solution of PBTDTT-12 in chlorobenzene at 25°C (black solid line); (c) absorptions of dilute hot solution of PBTDTT-12 in chlorobenzene above 60°C (green dashed line).

5.2.3 X-ray diffraction

The XRD spectrum of a powdered sample of PBTDTT-12 exhibits two diffractions at $2\theta = 4.7$ and 24.5° ; these correspond respectively to interchain d-spacing of 19.4 Å and stacking distance of 3.6 Å, and reflect a high degree of ordering and crystallinity. When the powdered sample is annealed at 160°C, a more distinctive, highly crystalline XRD

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pattern is observed (Figure 5.3). On the other hand, the XRD pattern of the thin film of PBTDDT-12 on an octyltrichlorosilane (OTS-8) modified silicon wafer substrate is featureless prior to annealing but shows a strong primary diffraction peak at $2\theta = 4.2^\circ$ and second order at 8.6° after annealing at 160°C , reflecting an inter-chain distance of $20.9\text{ \AA}$. The annealed film lacks the prominent annealed powder π - π stacking peak at $2\theta = 24.5^\circ$, which indicates that the highly ordered lamellar π - π stacks are oriented normal to the substrate. The HRTEM image clearly shows crystal lattices of PBTDDT-12 domain, where the (010) fringes have a d-spacing of $3.7\text{ \AA}$, corresponding to the face-to-face π - π stacking distance. The electron diffraction analysis also indicates π - π stacking distance of $3.7\text{ \AA}$.

Figure 5.3 XRD spectra of PBTDDT-12: (a) powder pellet at room temperature; (b) powder pellet annealed at 160°C ; (c) thin film at room temperature; (d) thin film annealed at 160°C ; (e) HRTEM image of crystalline domains in a PBTDDT-12 film on carbon grid; and (f) SAED of PBTDDT-12 film on carbon grid.

5.2.4 Electrochemical cyclic voltammetry

Cyclic voltammetric measurements of a thin film of PBTDDT-12 in 0.1 M $\text{Bu}_4\text{PF}_6/\text{CH}_3\text{CN}$ solution showed a multi-electron oxidation process with an onset oxidation potential at about 0.1 eV higher than that of PQT-12, indicating a greater stability against oxidative doping, and a quasi-reversible reductive process (Figure 5.4). The electrochemical band gap was calculated to be 2.3 eV, a little larger than that estimated from the onset of its UV-vis absorption.

Figure 5.4 Cyclic voltammetry spectra of PBTDDT-12: oxidative process (black line) and reductive process (red line)

5.2.5 Differential scanning calorimetry

The DSC thermogram of PBTDTT-12 does not show any obvious phase transition behavior between 25°C and 300°C.

Figure 5.5 DSC of PBTDTT-12 during the two heating/cooling scans at 5°C/min.

5.2.6 Scanning Tunneling Microscopy (STM)

The molecules were deposited onto Highly Oriented Pyrolytic Graphite (HOPG) surfaces and were investigated by STM. STM measurements were performed at the n-tetradecane/substrate (liquid/solid) interface in the constant current mode. Figure 5.6 showed the STM images at different data scales, it can be seen that the molecules of PBTDTT-12 form both crystalline grains and amorphous parts. Inside the crystalline grain, the alkyl chain ordered into inter-digital structures.

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Figure 5.6 STM of PBTDDT-12: (a). Data scale = 300 nm x 300 nm, $I_t = 0.070$ nA, $V_t = -0.300$ V; (b). Data scale = 100 nm x 100 nm, $I_t = 0.075$ nA, $V_t = -0.280$ V; (c). Data scale = 30 nm x 30 nm, $I_t = 0.070$ nA, $V_t = 0.307$ V; (d). Data scale = 15 nm x 15 nm, $I_t = 0.075$ nA, $V_t = 0.307$ V.

5.3 Field effect transistor fabrication and optimization

For the OFETs device application of a new class semiconducting polymer, all the system parameters should be optimized to acquire satisfactory electrical properties. In this part, a series of optimization experiments were conducted for the PBTDTT-12 based transistor devices. Four parameters were investigated: (1). Organic solvents used for the thin film deposition; (2). Concentrations of PBTDTT-12 in the solution; (3). Surface modification of both the dielectric and the electrodes, (4). annealing temperatures for the device.

5.3.1 Solvent effect

Six different solvents with different boiling points, relative polarities and densities were used as medium for thin film deposition. Their individual physical and chemical characteristics are listed in table 5.

Table 5 Characteristic properties of the organic solvents (boiling point, polarity, etc.)

Solvent	Formula	Boiling Point (°C)	Density (g/ml)	Solubility in H ₂ O(g/100ml)	Relative Polarity
Dichlorobenzene	C ₆ H ₄ Cl ₂	174	1.25	8	2.7
Chlorobenzene	C ₆ H ₅ Cl	131.7	1.1066	0.05	2.7
Chloroform	CHCl ₃	61.5	1.498	0.80	4.1
Toluene	C ₇ H ₈	110.6	0.867	0.05	2.4
P-xylene	C ₈ H ₁₀	138.3	0.861	1.00	2.5
Hexane	C ₆ H ₁₄	69.0	0.655	0.014	0.1

The solubility of the PBTDTT-12 varies with solvents. Dichlorobenzene, chlorobenzene and chloroform give good solubility as they are for other organic semiconductors; and the

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solution exhibit a dark purple color at ambient environment. The solubility in toluene is a little worse than the above three solvents, and the solution gives a dark yellow color. For p-xylene, PBTDDT-12 can only be partially dissolved; big concrete polymer particles can be observed at ambient environment. And the environmentally friendly solvent-hexane, gives no solubility at all. This is expected because during the synthesis of the material, it went through Soxhlet extraction with hexane process. But after heating the solution/mixture to higher temperature along with ultrasonic agitation, they all mix into well dissolved solutions. For the one in hexane, we find the semiconductor forms bright purple color nanoparticle dispersion. This nanoparticle dispersion in an environmentally friendly solvent will be discussed in detail later (see chapter 5.3).

The electrical performances of OFET devices fabricated from these solutions are compared in figure 5.7. Chlorobenzene gives the best result which has both the maximum drain current and *on/off* ratio. We contribute this result to the good solubility of the semiconducting material in this solvent and the relative high boiling point of this solvent. The evaporation rate of the solvent after deposition would be lower due to the high boiling point, which give the semiconductor thin films more time to form an ordered π - π stacking and thus increase the charge carries mobility. The overall performance comparison is: Chlorobenzene > Dichlorobenzene > Hexane > Chloroform > Toluene. The worse performance of dichlorobenzene compared to chlorobenzene maybe because of the crystallinity of the material in the thin film formed, chlorobenzene generate bigger crystal grain than dichlorobenzene[66]. This speculation need to be confirmed by AFM experiment. Although we tried a number of times, the devices made from p-xylene solution never works.

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Figure 5.7 Summary of the electrical performances of the OFET devices made from different solvents: (a) drain current of the devices at $V_g = -40$ V; (b). *on/off* ratio at the saturation regime of the devices.

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5.3.2 Concentration effect

The concentration of the semiconductor in the solution reflects the charge carriers' density. Lower concentration will cause the pin-hole effect of the thin film in the conducting channel, which would block the charge hopping from one delocalized orbital to another. However, higher concentration would affect the self-organization of the polymer molecule; resulting a more amorphous thin film.

It is found that the device performance increase as the concentration of PBTDTT-12 increase from 0.5 mg/ml to 5.0mg/ml in chlorobenzene, and then decrease as concentration went to 6.0mg/ml and even worse when it is 8.0mg/ml. This experiment result demonstrates that performance is optimized at the point of 5.0mg/ml.

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Figure 5.8 Summary of the electrical performances from different concentrations of PBTDDT-12. (a). maximum drain currents of the devices at $V_g = -40$ V; (b). Transfer curves of the devices at saturation regime (inset: *on/off* ratio)

5.3.3 Annealing treatment

Because the DSC data shows no peak of phase transition between 25°C and 300°C, we only can deduce the annealing temperature from the chemical structure of this material. PBTDDT-12 has a dithieno [3, 2-*b*: 2', 3'-*d*] thiophene (DTT) based backbone structure, which means the annealing temperature usually higher than 120°C. Based on experience and other semiconductors, we choose three conditions to test: 120°C, 160°C and 180°C.

The result shows that the device annealed at 160 degree has both the maximum drain current and the *on/off* ratio value. The leakage current also reduces at least one order of magnitude at this annealing temperature.

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Figure 5.9 Summary of the electrical performances from different annealing temperatures. (a). drain currents of the devices at $V_g = -40$ V; (b). *On/off* ratio of the devices at saturation regime;

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5.3.4 Surface modification

Surface treatment is an important way to improve OFET performance. Capping SiO_2 surface with octyltrichlorosilane (OTS-8) not only removes Si-OH trapping centers, but also leads to the larger grain growth and improved crystalline ordering (see chapter 4.2).

Treating the Au surface with a self-assembled monolayer (SAM) of octanethiol can significantly reduce the contact resistance between the electrodes and the semiconductor layer, as showed in figure 5.10. The nonlinear behavior of the drain current at low drain voltage before modification is successfully eliminated after the grafting of SAMs. Therefore, charge injections from the electrodes to semiconductor thin film are more efficient. The device mobility without modification is 0.107, and increase to 0.28 after the modification.

Figure 5.10 Characteristic of drain current at different gate voltages before (a) and after (b) gold electrodes modification.

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5.3.5 Conclusion

In summary, the best fabrication conditions for PBTDTT-12 based bottom-contact OFETs are listed at table 6.

Table 6 The optimized conditions for PBTDTT-12 based OFET fabrication

Active material: PBTDTT-12				
Solvent	Concentration	Dielectric Modification	Electrode Modification	Annealing Temperature
Chlorobenzene	5mg/ml	OTS-8 silane	Octanethiol	160 °C

Figure 5.11 exhibits the characteristic p-type OFET behavior of an optimized PBTDTT-12 device. The output characteristics display very good saturation behavior with no obvious contact resistance. The saturation current is 3.5 mA at the gate and the source-drain voltages of -40 V. The transfer characteristic shows a near-zero turn-on voltage and a threshold voltage of -14.2 V; The mobility derived from the saturated portions of the I - V curves is as high as $0.28 \text{ cm}^2/\text{Vs}$, and the current on/off ratio is over 10^7 .

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Figure 5.11 I-V characteristics of an illustrative OFET device using PBTDTT-12 semiconductor: (a) output curves at different gate voltages; (b) Transfer curve in saturated regime at constant source-drain voltage of -40 V and square root of the absolute value of the drain current as a function of gate voltage. The field-effect mobility μ

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calculated in the saturation regime is $0.28 \text{ cm}^2/\text{vs}$ and I_{on}/I_{off} ratio is over 10^7 . All measurements are conducted at ambient environment.

In conclusion, we have created a new class of solution-processible polymeric semiconductors, PBTDTT-12, which has well self-assembly ability and controlled effective $\pi - \pi$ conjugation length. In OFET application, a series of optimization experiment is conducted. This material demonstrates high mobility and high current on/off ratio properties.

5.3 OFETs based on environmentally friendly solvent - Hexane

Despite the continuous progress on semiconducting materials synthesis and OFET device fabrication methods, there still a large gap before this technology step into commercialization. One of the limitations is that for almost all the solution processible semiconducting polymer nowadays, toxic solvents like chloroform, chlorobenzene which has extensive phenyl group and halogen elements are required to achieve good performance. Those solvents would cause major environmental contamination as well as serious damage to people's health.

Here in this part of work, we demonstrate that with proper ultrasonic agitation treatment, PBTDTT-12 can form uniformly distributed nanoparticle dispersion in the environmentally friendly solvent---hexane. Bottom contact OFET devices made from this dispersion exhibit a high field mobility of $0.162 \text{ cm}^2/\text{Vs}$, and a large current On/Off ratio as 10^6 at ambient environment.

5.3.1 Preparation of the nanoparticle dispersion and its characterization

The nanoparticle dispersion is formed by adding PBTDTT-12 powder into pure hexane solvent, and then goes through nearly 2 hour ultrasonic agitation treatment at 50 °C until the mixture becomes a purple dispersion. Light-scattering measurements reveal that PBTDTT-12 particles are uniformly distributed in hexane solvent and the size is about 494nm with a variation of 10nm. The Uv-vis spectrum of the nanoparticle dispersion in hexane shows strong absorption peaks at 519 (shoulder), 558, and 605nm with distinct vibronic splitting characteristic of high structural ordering. No peak shift can be observed as the particle concentration increase, see figure 5.12, demonstrate that this nanoparticle dispersion is very stable under ambient environment.

Figure 5.12 UV-vis absorption spectrum of PBTDTT-12 in hexane: Trace a: solution after filtering the nanoparticle dispersion through a 0.2 μm PTFE filter; Trace b, c, d, is the nanoparticle dispersion with increased concentration, specifically, $d > c > b$.

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The X-ray diffraction pattern of the thin films drop casting from the nanoparticle dispersion onto silicon wafers which have been modified with OTS-8 silane exhibit a primary diffraction peak at $2\theta = 4.42^\circ$, corresponding to a d-spacing of $19.97 \text{ \AA}$, which is result from the ordering of the alkyl side-chain. After post-annealing to 160°C , the thin film sample exhibits a more distinctive and high crystalline pattern, with the second and third order diffractions at $2\theta = 8.95^\circ$, $2\theta = 13.67^\circ$ can be observed, respectively.

Figure 5.13 XRD spectrum of PBTDDT-12 casting from hexane dispersion: (a). as casting at room temperature; (b). after annealing to 160 degree.

AFM of the thin film casting from the nanoparticle dispersion exhibit unique patterns and demonstrate the annealing effect. As casting at room temperature, the thin film shows small crystal grains with aggregation effect and high surface roughness. Impurities and trapping molecules absorbed from the ambient environment tend to accumulate at grain boundaries and further increase the energy barriers for hoping. But after annealing at 160°C

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°C, larger and interconnected webs are formed. These large continuous domains are responsible for the higher motilities.

Figure 5.14 AFM morphology of the PBTDTT-12 thin film casting from the nanoparticle dispersion in hexane. Image dimension: 2 μm x 2 μm . (A) Top view and 3D view of the film casting at room temperature; (b). Top view and 3D view of the film after annealing at 160 degree.

5.3.2 Electrical properties of the OFET based on the nanoparticle dispersion

Bottom contact OFET devices fabricated from PBTDTT-12 nanoparticle dispersion in hexane under ambient conditions yield excellent transistor properties (figure 5.15). The

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output characteristics showed no noticeable contact resistance, very good saturation behavior even at small channel length, and clear saturation currents that are quadratic to the gate bias. The saturation current is more than -0.7 mA at the gate, and source/drain voltages equal to -40 V. After annealing at 160 °C, the mobility of the device can be as high as $0.162 \text{ cm}^2/\text{Vs}$ and I_{on}/I_{off} ratio is over 10^6 .

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Figure 5.15 I-V characteristics of an exemplary OFET device using PBTDTT-12 nanoparticle dispersion in hexane: (a) output curves at different gate voltages; (b) Transfer curve in saturated regime at constant source-drain voltage of -40 V and square root of the absolute value of the drain current as a function of gate voltage. The field-effect mobility μ calculated in the saturation regime is $0.162 \text{ cm}^2/\text{Vs}$ and I_{on}/I_{off} ratio is over 10^6 . All measurements are conducted at ambient environment.

In conclusion, we have demonstrated that through proper ultrasonic agitation treatment, a high mobility p-type semiconductor material PBTDTT-12 can uniformly dispensed in hexane solvent and self assembled into ordered structure with high crystallization. Excellent OFET performance characteristics can be getting from this material. To the best of our knowledge, this is the first time an environmental friendly solvent is used to build an OFET and achieved relatively high performance.

5.4 Thermal stability of the PBTDTT-12 based OFET

A major challenge in OFET research is the development of practical OFET materials that ensure not only high performance but also high stability in the operational environment. The thermal-stability of OFET devices means that not only highly ordered molecular structure but also the air-stability should be remained at high temperature since high temperature would inevitably promote severe oxygen doping. It seems to be a common trouble for the most polymers to maintain highly ordered molecular structures at rather high temperatures due to their intrinsic phase transition properties upon heating. The

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thermal property of PBTDDT-12 (as shown in Fig. 5.4) has been disclosed by DSC thermogram, which does not show any obvious phase transition behavior between 25°C and 300°C, implying PBTDDT capable of avoiding such problem.

An in-situ temperature dependent experiment is conducted on the OFET devices based on this material. It is found that the current will continuous increase at the linear region but start to decrease a little at saturation region (figure 5.16 (a)). We conclude this is due to the bias stress effect which can be supported by the transfer curve figure 5.16 (b). From the transfer curve, we observe that after 120 degree, exactly the temperature where the saturation current start to reduce, the slope of the square root of drain current versus gate voltage stop to change. The enhanced temperature only manifests itself in the parallel shift of threshold voltage but not change in the mobility. This behavior is corresponding to the bias stress effect we observed in figure 4.15.

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Figure 5.16 In situ temperature dependent measurements of OFET devices based on PBTDTT-12. (A) Drain current versus drain voltage at $V_g = -40$ V at different temperature; (B) Transfer curve of square root of drain current versus gate voltage at different temperature.

The FET devices based on PBTDTT-12 as active layer keep stable FET characteristics all along with the increase of operational temperature. The in-situ measurements of FET performances at the temperature as high as 200°C demonstrates a mobility of $\mu_{\text{sat}} = 0.22$ cm²/Vs together with an on/off ratio of 10^6 , as showed in figure 5.17. The output characteristics still remain very good saturation behavior at 200°C. The transfer curve shows that the threshold voltage shifts a little positively to -4.1 V. It is an exciting result since all the data are collected entirely under the atmosphere conditions without any precautionary measures in excluding oxygen, light and moisture during device fabrication and characterization, indicative of PBTDTT-12 possessing a super thermal stability and air-stability against oxygen doping at high temperatures.

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Figure 5.17 I-V characteristics of the OFET device based on PBTDDT-12 semiconductor measured at 200°C. (A) Output curves at different gate voltages and (B) transfer curve in

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saturated regime at constant source-drain voltage of -40 V and square root of the absolute value of the drain current as a function of gate voltage.

CHAPTER 6 CONCLUSIONS AND OUTLOOK

This project is initiated with the aim of developing high-performance, solution-processible and stable organic field effect transistors. Two classes of high mobility p-type organic semiconductors, Poly (3, 3'''-didodecyl quarter thiophene) (PQT-12) and Poly (2, 6-bis (3-alkylthiophen-2-yl) dithieno [3, 2-b; 2', 3'-d] thiophene) (PBTDDT-12) are investigated. The polymers are characterized in detail with different techniques including UV-visible spectra, XRD, AFM and STM microscopy, as well as electrochemical methods to understand their physical and chemical properties. A number of fundamental issues of the OFET devices physics are studied and for scientific insights are explored to improve the OFET performance:

1. The role of the surface modification by organosilane self-assembled monolayers (SAMs) on SiO₂ gate insulator for PQT-12 based OFET is studied in this work. We use nine different organosilanes to modify the surface of dielectric layer for the correlation between the surface energy and the device performance. The results demonstrate that SAMs affect the field effect mobility, the threshold voltage of the device and the morphology of the PQT-12 thin film. The silane monolayer modifies the roughness of dielectric layer and their structures to direct the lamellar ordering of the semiconductor layer. Suitable SAMs could reduce the charge injection barrier and facilitate the charge transportation at the interface and lead to significant improvement of the device performance.

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2. The post annealing process of the deposited organic semiconductor thin film and device degradation under elevated temperatures are studied. We demonstrate that annealing at phase transition point can effectively increase the device mobility. Because at those temperatures, semiconductor molecules have the freedom to rearrange into a long-range ordered π - π stacking structure, thus to reduce the energy barrier for the charge carriers hopping from one crystalline domain to another, eventually leading to a more efficient charge transport in the conducting channel. For device degradation under elevated temperatures, we discover that reduced mobility and on/off ratio and the negative shift of threshold voltage are due to the oxygen and moisture in the environment. Oxygen in the air reacts with semiconductor material would increase its doping level, thus increase the off current of the transistor, in which water molecules form a dipole layer at the insulator-semiconductor interface. This layer offsets the gate bias and makes the transistor harder to be turned off. When the temperature increases, oxygen could more effectively react with the semiconductor. On the other hand, the partial pressure of water vapor reduces with the increasing temperature, thus resulting in the negative shift of the threshold voltage and the decrease of on/off ratio.

3. Electrical instability from the bias-stress effect is investigated. It is discovered that prolonged gate and drain bias-stress induces a continuous decrease in the drain current and a negative threshold voltage shift but no change in mobility. Furthermore, the change of threshold voltage is eventually saturated as the operation time pass by. This effect can be ascribed to trapping of mobile charges located within the dielectric-semiconductor interface. Those trapped charges form an immobile charge density distribution that shields the gate voltage. When the gate voltage overcomes this electrostatic screening, the

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device characteristics are identical to those of a pristine device. The shift of charge-transport curve can be recovered subjected to an above band gap UV illumination.

For the OFET application of the new class semiconducting polymer PBTDDT-12, which is synthesized in our group, a number of optimization experiments are conducted to acquire the best device performance. The best fabrication conditions for PBTDDT-12 based bottom-contact OFETs are listed at table 6. The field-effect mobility of the resulted OFET is $0.28 \text{ cm}^2/\text{Vs}$ and I_{on}/I_{off} is over 10^7 . This result is among the best reported to date for solution-processed OFETs and thus affirms that PBTDDT-12 is an excellent polymeric semiconductor.

We demonstrate that through proper ultrasonic agitation treatment, PBTDDT-12 can form uniformly distributed nanoparticle dispersion in an environmentally friendly solvent---hexane, and self assembled into ordered structures with high crystallization. Excellent OFET performance characteristics ($\mu=0.162 \text{ cm}^2/\text{Vs}$ and $I_{on}/I_{off}=10^6$) can be getting from this dispersion. To the best of our knowledge, this is the first time an environmentally friendly solvent is used to build an OFET device and achieved good electrical performance. An *in-situ* temperature-dependent experiment is conducted on the OFET devices based on this material. It is found that the device can even work at the temperature as high as 200°C without performance degradation. This is an exciting result since all the data are collected without any precaution to oxygen and moisture in the environment, indicating that PBTDDT-12 possesses super thermal stability and air-stability against oxygen doping at high temperatures.

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The performance of OFETs has been improved substantially during the past 10-15 years due to the introduction of novel materials and the development of new fabrication methods. However, the structure-property issues in organic semiconductors are still unclear and need to be studied in the future work. Understanding of the fundamental excitations and processes at a microscopic level involved in charge transport and injection is still very superficial. Moreover, the developed organic materials are limited, especially for n-type semiconductors, which are very important to make bipolar devices for the application of complementary logic circuit. Dielectric material is another crucial component for OFETs. In general, organic dielectric materials have relatively low dielectric constants compared with inorganic materials. Exploration of high performance dielectric materials would be very important for the realization of organic electronic circuits.

In summary, there are great challenges in R&D to make OFETs for practical applications in spite of their excellent performances achieved in recent years. The bright and promising future of organic field-effect transistors are worthy of prolonged investigations.

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