CMOS building blocks for 10+Gb/s clock data recovery circuit

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2007

Liu, H. (2007). CMOS building blocks for 10Gb/s clock data recovery circuit. Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/39032>

<https://doi.org/10.32657/10356/39032>

0529967

CMOS Building Blocks for 10+Gb/s Clock Data Recovery Circuit

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A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

2007

Abstract

The design of a clock data recovery (CDR) circuit is the most challenging part of building a high-speed optical transceiver because of the complexity of this block. In this dissertation, the design of a half-rate high speed CDR is described, following a top-down design procedure. VHDL-AMS, which is the acronym of the *VHDL (VHSIC Hardware Description Language) for Analog and Mixed-Signal*, is used to implement the behavioral model of the whole system in the early and mid-stage of the design process.

As both wireless and optical communications systems move towards high-data rate application, low noise high frequency voltage-controlled oscillators (VCOs) are becoming more important in the design of the receiver and transmitter blocks. Ring oscillator has long been perceived as capable of permitting easy implementation and occupying smaller die area as compared with its inductor-capacitor (LC) counterparts. Ring oscillator is also well known to be able to cover a wide tuning range, and to generate quadrature signals, by simply using even-number of differential delay stages.

In this dissertation, the design and experimental results of two novel ring oscillators are described. One of the proposed VCO attains the high speed and wide tuning range with acceptable noise level by using push-pull inverter as the secondary input of the multiple-loop ring oscillator. Experimental results prove the capability of the VCO to operate at

high frequencies. Implemented in 0.18- μm CMOS process, the oscillator presents a tuning range of 6.3 to 7 GHz with a relatively constant tuning gain across the whole tuning range.

The other proposed VCO achieves low-noise, low voltage tuning gain without impairing the wide tuning range by utilizing coarse/fine-tuning technique. The frequency and phase noise performance of the coarse/fine-tuning oscillator are analyzed in detail. The analysis is also verified by the physical implementation. The fabricated oscillator in 0.13- μm technology is measured to cover a frequency range of 7.3 to 7.9 GHz, and exhibits a typical phase noise of -103.4 dBc/Hz at 1 MHz from 7.64 GHz center frequency.

By modifying the proposed ring oscillator from three stages to four stages, in-phase and quadrature (IQ) clock signals are obtained to be used in the half-rate CDR circuit. A half-rate bang-bang phase detector is used for higher speed data processing as well as to avoid the marginal performance of the full-rate 10-Gb/s CDR system implemented in 0.18- μm CMOS technology. Since the lock-in range of data-tracking loop in CDR system is very limited while the VCO usually has a wide tuning range to accommodate the process drift, the frequency-locked loop is usually necessary to extend the lock-in range of the CDR system. An analog lock detector is designed for use in the CDR which employs frequency-locked loop. The post-layout simulation of the CDR indicates that the design can operate at input data rate of 13-18 Gb/s.

Acknowledgements

I like to express my deepest appreciation to my supervisor, Associate Professor Goh Wang Ling, for her support, guidance and friendship through my three years of research. Her vast knowledge and experience were essential for me to complete my research. A/P Goh has not only assisted me in my research project, but also helped me to develop a positive attitude towards solving difficulties in my life.

I would also like to extend my gratitude to Associate Professor Siek Liter, for his constructive instruction and continuous supports throughout the development of my research. It would be impossible to achieve these research results without the consistent support from A/P Siek.

Special thanks go to Associate Professor Zhang Yue Ping for his valuable advices and discussions on my research project. In particular, I want to acknowledge Mr. Yeoh Wooi Gan and Dr. Lin Fujiang of Institute of Microelectronics, Singapore, for their support in chip prototyping and test.

Final Year Project students, Tan Poh Kong and Jimmy Tang, are gratefully acknowledged for their contributions in this research project. My fellow students at the Centre for Integrated Circuits and Systems, including Phyu Myint Wai, Jia Lin, Yu Xiaopeng and Lim Wei Meng, are also acknowledged for their friendship and technical discussions. I also want to express my appreciation to all the technicians in the Centre for Integrated Circuits and Systems and IC Design Lab, for their technical support and assistance.

Finally, I like to express my gratitude for my parents, brothers, and sister for their love, support and encouragement.

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List of Symbols and Abbreviations

BER	Bit Error Rate
CMOS	Complementary Metal-Oxide-Semiconductor
CDR	Clock Data Recovery
CMU	Clock Multiplication Unit
DAE	Differential Algebraic Equation
DCSL	Differential Current Steering Logic
DEMUX	Demultiplexer
ESD	Electrostatic Discharge
FEC	Forward Error Correction
FoM	Figure-of-Merit
ISF	Impulse Sensitivity Function
LFSR	Linear Feedback Shift Register
LTI	Linear Time-Invariant
MCML	MOS Current Mode Logic
MiM	Metal-insulator-Metal

NMF	Noise Modulation Function
NRZ	NonReturn-to-Zero
ppm	parts per million
PDA	Portable Digital Assistant
PFD	Phase/Frequency Detector
PLL	Phase-Locked Loops
PSD	Power Spectrum Density
PTPFD	Precharge Type PFD
PRBS	Pseudo-Random Bit Sequence
PWL	Piece-Wise Linear
rms	root mean square
SONET	Synchronous Optical NETwork
SDH	Synchronous Digital Hierarchy
STS	Synchronous Transport Signal
STM	Synchronous Transport Module
TIA	TransImpedance Amplifier
UI	Unit Interval
VHDL	VHSIC Hardware Description Language
VHSIC	Very-High-Speed Integrated Circuit
VHDL-AMS	VHDL-Analog and Mixed-Signal
VCO	Voltage-Controlled Oscillator
WLAN	Wireless Local Area Network

Chapter 1

Introduction

1.1 Research Background and Motivation

Ever since its introduction in the mid-1980s as a synchronous transmission system that could directly extract low-speed signals from multiplexed high-speed traffic, synchronous optical network (SONET) [1] has emerged as the technology of choices for optical communication networks. Today's carrier backbone networks are supported by SONET and synchronous digital hierarchy (SDH) transmission technologies. SONET is the standard used in the United States and SDH is the standard used outside the United States. The SONET/SDH specification outlines the frame format, multiplexing method, and synchronization method between the equipment, as well as the specifying optical interface. In the core network, the carriers offer services such as telephone, dedicated leased lines, and Internet protocol (IP) data, which are continuously transmitted. The individual data is not

Table 1.1: Synchronous Transport Signal and Synchronous Transport Module

SONET	SONET	SDH	Both
North America	North America	European STM	Line rates
STS level	OC level	level	(Mbps)
STS-1	OC-1	N/A	51.84
STS-3	OC-3	STM-1	155.52
STS-12	OC-12	STM-4	622.08
STS-48	OC-48	STM-16	2488.32
STS-192	OC-192	STM-64	9553.28
STS-768	OC-768	STM-256	39813.72

transmitted on separate lines. Instead, they are multiplexed for higher speeds, and transmitted on SONET/SDH networks, at up to 10 gigabits per second (Gb/s). Table 1.1 shows the line rates of the SONET and SDH systems. The base rate for SONET is 51 Mbps. Synchronous transport signal (STS-n) refers to the SONET signal in the electrical domain, and optical carrier (OC-n) refers to the SONET signal in the optical domain. The base rate for SDH is 155 Mbps. Synchronous transport module (STM-n) refers to the SDH signal level in both the electrical and optical domains.

In recent years, wireless local area network (WLAN) has evolved as one of the major means for end-users to access the network. Based on the new WLAN standards, i.e., IEEE 802.11a/b/g, the mobile network has witnessed wide applications for devices, such as the mobile handsets, PDAs and personal computers accessing the internet. In addition, with the

convergence of voice, video and data (e.g., triple-play access networks), Ethernet connections are now being used for the delivery of mission-critical services. This further increases the data traffic through the network backbone between base stations and the network.

With ever increasing data traffic through the network and hence the increasing demand on bandwidth, various high speed communication technologies have converged into the multi-gigabit domain. With the rapid development of optical fiber technology and digital processors, the receiver and transmitter have also become the bottleneck as an interface between them.

Depicted in Figure 1.1 is a fiber optic transceiver, consisting of a transmitter and a receiver. In the transmitter path, parallel low-speed data sequences are combined in the multiplexer (MUX) to generate a serial high-speed data stream. The clock multiplication unit (CMU) provides the clock signal for the multiplexer and hence, to a large extent, it determines the jitter performance of the transmitter. The CMU operates by using an integer-N phase-locked loop (PLL) to phase lock the internal voltage-controlled oscillator (VCO) to an external reference clock via a frequency divider [2]. The high-speed serial data signal from the multiplexer is then boosted by the laser driver to a level that the laser diode can handle. The laser diode ultimately emits the data signal to the fiber channel.

In the receiver end, the high-speed optical data signal traveling through the fiber is fed to the receiver after being converted into an electrical signal by the photodiode and transimpedance amplifier (TIA). The clock and data recovery (CDR) circuit extracts the high-frequency clock from the data signals and consequently provides the timing information for the decision circuit to re-sample the jittered data. The CDR is operating in such a

way that its output clock's rising/falling edges fall in the middle of the data eye, so that the sampling occurs at the optimum point. This will improve the signal-to-noise ratio (SNR) of the receiver. The retimed data is subsequently deserialized into multiple parallel channels at a much lower speed by the demultiplexer (DEMUX), so that they can be processed by the network processor. The network processor will then perform the required data processing tasks such as forward error-correction (FEC) encoding/decoding and other functions. The divided CDR clock signals provide the timing information for the demultiplexer.

CDR circuit is amongst the most critical analog/mixed-signal building blocks in the optical receiver system. It defines the performance of the overall system. The design of the CDR circuit is also the most complicated part of implementation of an optical transceiver. A common method to implement a CDR involves a phase-locked loop (PLL), to adjust the frequency and phase for data sampling in the decision circuit. Figure 1.2 shows the block diagram of a common PLL-based CDR. The phase detector (PD) compares the clock with the random input data transitions, to provide output pulses representing the phase error. The charge pump (CP) sinks or sources current from/to the loop filter according the PD output pulses. The filtered voltage controls the VCO to provide the output clock and sampling signals.

The VCO is probably the most important block in a PLL system. As a high-speed block within the PLL circuit, the VCO usually burns a large portion of the overall power consumption. The noise performance of the VCO directly impacts the jitter and phase noise performance of the whole system. Two common methods to design a VCO for PLLs are

Figure 1.2: Block diagram of a PLL-based CDR.

LC-based oscillator and ring oscillator. LC-based oscillators are usually perceived as capable of generating clean frequencies with low power consumption as compared to the ring oscillator. LC oscillators also have some obvious disadvantages. They occupy much larger die area. Inductors especially pose a significant barrier to integration and miniaturization. Most LC oscillators have narrow frequency covering range and at least two of them have to be coupled in order to generate the In-phase (I) and the Quadrature (Q) signals. This implies that the die area would be further enlarged. The ring oscillators, on the other hand, are well-known for occupying a much lesser area as well as being capable of easy integration. Multi-phase clock is easily obtained by simply deploying even number of delay stages. Ring oscillator also has a wide tuning range and this permits it to cope with the process drift during fabrication. Unlike their LC-based counterparts that oscillate through self-resonance of passive inductors and capacitors, the highest frequency of the ring oscillators is limited by the delay contributed by each delay stage, and that is ultimately limited

by the parasitic resistance and capacitance involved in the stage. For the same technology, it is therefore difficult to generate comparable high frequency as LC oscillators by employing ring oscillators. Meanwhile, the ring oscillators provide poorer phase noise performance since every active device contributes to the overall noise. Nevertheless, when comparing with applications such as frequency synthesis of Wireless LAN (WLAN) transceiver, the noise and power requirements of the CDR in SONET transceiver and data link/storage systems [3] are often less stringent. This is also in accordance with the fact that transistors have replaced inductors wherever possible since the "wireless revolution" in the 80s [4].

The challenges in the design of a high-speed low-noise/jitter CMOS voltage-controlled ring oscillator to be used in PLLs such as CDR circuits and the design of a high data-rate CDR circuit, have provided the key motivations for this research.

1.2 Objectives

The CDR circuit employed in SONET OC-192 communication systems has to process the Nonreturn-to-Zero (NRZ) data inputs working in a speed of 10 Gb/s. This implies that the PLL has to provide a 10 GHz output clock (at full-rate architecture) or a 5 GHz output clock (for half-rate architecture) to fulfill the mission. The oscillator used in the PLL must therefore be capable of operating beyond 5 GHz. The objective of this research is to explore on the frequency limitation of the CMOS ring oscillator as well as to design a high-speed CMOS ring VCO, with acceptable noise level for use in CDR system.

1.3 Major contribution of the Thesis

In this work, different architectures of voltage-controlled ring oscillator have been thoroughly studied. Novel delay cells for multi-gigahertz ring oscillators have been proposed and implemented in standard CMOS process. One of the ring oscillator designs presented adapts the coarse/fine-tuning scheme to yield a lower tuning gain, without impairing the ability to cover a wide frequency range. The frequency and phase noise characteristics are analyzed and predicted using small-signal analysis. The results obtained agree well with the experimental results. Another ring oscillator is also proposed for single voltage tuning. Its modified version for multi-phase clock generation is then integrated into a CDR system for verification. The top-down design procedure is applied in the design of the CDR circuit by using the analog/mixed-signal modeling language VHDL-AMS. This allowed a tremendous saving of the design period. Post-layout simulation proves that the circuit can operate at an input data rate from 13 to 18 Gb/s, with a typical power dissipation of 600 mW for an input bit rate at 16 Gb/s.

1.4 Organization of the Thesis

In Chapter 2, CDR system is reviewed in terms of its jitter specifications: jitter transfer, jitter generation and jitter tolerance. Different CDR architectures are also discussed and analyzed. This is followed by a brief description of the CDR building blocks, detailing mainly the different types of phase detectors. Since CMOS VCO is one of the main research objects in this thesis, review on VCO especially ring oscillator is also carried out in

this chapter. Different ring oscillator types are introduced with a brief explanation on the oscillator fundamentals. Existing oscillator noise models and some of the techniques for improving the oscillator frequency are also reviewed in Chapter 2. A novel delay cell for multiple-loop ring oscillator is demonstrated for operation in the 7-GHz range in Chapter 3. A push-pull inverter is added into the delay cell as the secondary signal path to boost the operating frequency and to improve the phase noise performance. Chapter 4 demonstrates the design of a high-frequency low-noise multiple-loop ring oscillator with coarse- and fine-tuning control. The frequency and phase noise characteristics of the design is analyzed in detail. The experimental results of a prototype chip that was implemented to verify and validate the theoretical results are also discussed. Chapter 5 describes the design of a half-rate CDR circuit where a modified version of the ring oscillator discussed in Chapter 3 is adopted to provide the necessary multi-phase clock signals. Different blocks, including novel lock detector and phase/frequency detector (PFD) are also proposed in this chapter. Finally, in Chapter 6, a brief summary of the introduced work is presented along with discussions on the major contributions of this work and the future directions.

Chapter 2

Clock and Data Recovery System

It is clear that the clock and data recovery system is the most critical block at the receiving path of the optical communication system for its high requirements on both the speed and the noise performance. From speed point of view, the CDR has to realize both the high-frequency-in and the high-frequency-out functions. The CDR receives distorted high speed data, outputs retimed high speed data as well as recovered high frequency clock. From noise performance point of view, the CDR's input is jittered and distorted after transmission through channels, while the output of the CDR needs to ensure clean clock to provide the timing information to the receiver. The input data is asynchronous since there is no accompanying clock signal. Different pulse patterns of input data stream also impose difficulty onto the proper function of CDR. Due to these requirements on the speed and noise as well as the complexity of the functionality, it is very important to choose the right CDR architecture and design to meet the jitter specifications.

2.1 CDR Jitter Specifications

Noise, distortion and signal attenuation in communication channels cause timing jitter in data signals. A CDR circuit extracts the clock signal from the input data stream and re-sample the noisy data. The jitter in the input data is hence transferred to the output clock. Due to the nonlinearity and internal noise, the CDR itself also generates timing jitter. Because of the jitter in the recovered clock phase, bit errors may occur on the recovered data. Bit error rate (BER) is therefore one of the major specifications of a digital communication system. SONET has a comprehensive set of jitter measurement standards. There are three types of important jitter characteristics in SONET receiver design: jitter tolerance, jitter transfer function (bandwidth and jitter peaking) and jitter generation [5], [6].

2.1.1 Jitter Tolerance

Jitter tolerance is a measure of the performance of how much peak-to-peak sinusoidal jitter can be added to the incoming data before causing data errors due to misalignment of the data and the recovered clock. The jitter tolerance test setup is shown in Figure 2.1, in which case the input data generator is phase-modulated with a sinusoidal signal. At each jitter frequency, the sine wave modulation amplitude is increased until the BER penalty is equal to that caused by 1dB optical attenuation. The SONET CDR jitter tolerance specification is defined as a mask that relates the maximum amount of phase modulation that can be corrected by the loop to the frequency offset with respect to the data rate, as illustrated in Figure 2.2. In this case, for 10 Gb/s data rate, the CDR should be able to track a minimum

Figure 2.1: Jitter tolerance test setup.

Figure 2.2: Jitter tolerance mask.

of 0.15 unit interval (UI) of the input jitter at 4 MHz jitter frequency.

2.1.2 Jitter Transfer

Jitter transfer specification deals with the closed-loop transfer function of the CDR system. The system specifications define the 3-dB bandwidth and the peaking in the transfer function. The maximum value of the jitter transfer function must be kept less than 0.1 dB, which is intended to control jitter peaking in long repeater chains. A large bandwidth would be

beneficial to suppress the VCO phase noise, while a small bandwidth is used if the input clock noise dominates. The bandwidth is chosen as a tradeoff to minimize the sum of these noise contributions. An approximation for the jitter transfer bandwidth and jitter peaking of a PLL-based CDR with linear phase detector is given by De Vito equations [7] as

$$\omega_{3dB} = R_1 \cdot I_{CP} \cdot K_{VCO}, \quad (2.1)$$

$$J_{peaking} = 1 + \frac{1}{\omega_{3dB} R_1 C_1} \quad (2.2)$$

where R_1 and C_1 is the loop filter resistor and capacitor, respectively, K_{VCO} is VCO gain in rad/s and I_{CP} is charge pump current.

The relationship between the jitter transfer function $J_{Tran}(s)$ and the jitter tolerance $J_{Tol}(s)$ characteristics is given by [8]

$$J_{Tol}(s) = \frac{1}{1 - J_{Tran}(s)} \quad (2.3)$$

The jitter transfer test setup is shown in Figure 2.3. A sine wave phase-modulated data is applied to the CDR. The CDR then recovers the input clock signal from the data and the jitter of the recovered clock is measured. The frequency of the sinusoidal jitter is changed and the measurement is repeated so as to plot the transfer function.

2.1.3 Jitter Generation

The jitter generation is a measure for the jitter generated by the CDR circuit. For SONET applications, the peak-to-peak (p.p.) jitter should be less than 0.1 UI. To test CDR for compliance to the jitter generation specification, an input data stream with very low jitter is

Figure 2.3: Jitter transfer test setup.

input to the CDR, and the jitter of the recovered clock and data is measured. The jitter generation is often tested with several pseudo-random bit sequence (PRBS) patterns generated with linear feedback shift register (LFSR), where the LFSR has a length of 7 or 23.

2.2 CDR Architectures

Depending on the VCO frequency and PD clock speed, the architecture of CDRs can also be sorted into full-rate [9, 10, 11, 12] and sub-rate (particularly half-rate) [13]. In full-rate CDRs, the rising or falling edge of one whole VCO clock period samples one bit of input data (see Figure 2.4a), while in the sub-rate CDRs, the clock signals of multiple phases are employed in the PD so that a chain of flip-flops can capture the data stream at a lower rate, alleviating the speed requirements of circuits. For instance, quadrature clocks are necessary for use in half-rate CDR. For LC-type VCOs, two LC banks are often coupled to each other to generate the quadrature clock outputs. Even number of stages can be used in ring type VCO to obtain the quadrature clock. In half-rate circuit, data is sampled by both the rising and the falling edges of the clock, the duty cycle mismatch results in bimodal jitter, since the duty cycle distortion pushes both edges away from the mid point of the data [14]. As

Figure 2.4: (a) Full-rate and (b) half-rate data recovery.

compared to a half-rate CDR, the VCO in a full-rate CDR has a simpler structure.

Full-rate CDR has the advantage of structural simplicity and operational robustness to various data patterns, while half-rate CDR offer the benefit of lower power consumption by reducing the clocking frequency, and lower complexity if the CDR is not required to generate a full-rate output since the first level of demultiplexing is automatically performed [14].

The PLL-based CDR architectures can also be grouped as two categories, according to their phase detectors (PD) characteristics: linear type and binary (bang-bang) type. Linear phase detectors for CDR design are mostly based on the Hogge phase detector [15], and binary phase detectors are based on the Alexander [17] phase detector. Linear type CDR has a linear characteristic since the average voltage difference between the 'up' and 'down' signals of the PD output is linearly proportional to its input phase error between the data and clock signals. Therefore linear PLL theory can be applied to analyze the jitter transfer

characteristics [20]. As compared to the linear type PD, the binary type PD produces two digital outputs, UP and DOWN, to signal if the data is early or late with respect to the VCO clock. When the loop is locked, the clock will vary around the data transition due to the random jitter on both the clock and data signals. In contrast, the linear phase detector output is close to zero when the loop is locked. The binary CDR is also hard to analyze since the gain of the binary PD is a function of the amount of jitter present in the system. The ring oscillator is recommended for binary CDR, to reduce the delay in the PLL loop and therefore the jitter generation in the CDR. Such recommendation is also due to the VCO phase noise being less critical in a binary CDR because of the relatively wide PLL bandwidth (usually 4 to 8 MHz).

Shown in Figure 2.5 is the block diagram of a CDR incorporating a parallel R and C as the loop filter which makes the loop second order. The transfer function of the CDR can be expressed as:

$$H(s) = \frac{K_{PD}I_{CP}K_{VCO}/C}{s^2 + \frac{1}{RC}s + K_{PD}I_{CP}K_{VCO}/C} = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (2.4)$$

Solving for the loop natural frequency ω_n , it can be shown that

$$\omega_n = \sqrt{K_{PD}I_{CP}K_{VCO}/C} \quad (2.5)$$

and the damping factor

$$\xi = \frac{1}{2R\sqrt{K_{PD}I_{CP}K_{VCO}/C}} \quad (2.6)$$

K_{PD} , K_{VCO} and I_{CP} are the gains of phase detector, VCO and charge pump current, respectively. For $\xi \geq 0.5$, the loop jitter transfer function does not produce any jitter peaking. However, this configuration does suffer from the problem of static phase error.

Figure 2.5: A second order CDR.

Since the resistor keeps discharging the capacitor in the loop filter, a static phase error must exist between the input data and the VCO clock signal, so that the phase detector can compensate for the resistor discharging. This static phase error is proportional to the difference (Δf) between the free-running VCO frequency and the input frequency, and inversely proportional to the PLL open loop gain K . While the frequency difference Δf varies with the process, the static phase error may become hard to predict. The loop gain K can be increased to reduce the phase error, but this will lead to a smaller ξ , which is not desirable for the CDR system.

In [7], the dual-path loop is utilized to incorporate an additional capacitor in the slow tracking frequency loop along with the fast tracking phase loop, as seen in Figure 2.6. By using a much larger C_2 and a smaller charge pump current I_{CP2} , the slow tracking loop performs the VCO tuning after the initial compensation for R_1 discharging by the phase detector in the first stage, to gradually result in a zero voltage over C_1 . On the other hand, since the time constant of the slow track loop is designed to be very large, it has negligible effect on the PLL dynamics during the locked state and the jitter performance is still dictated by the phase tracking loop. While this architecture does solve the problem of

Figure 2.6: Block diagram of dual-path loop CDR.

the static phase error that is inherent in the previously discussed second order loop CDR, most designs simply use a second order loop filter to ease the design process.

Since the Non-Return-to-Zero (NRZ) data makes the clock recovery difficult for CDR, i.e., arbitrarily long consecutive sequences of 1s or 0s limit the capture range of the PLL and allow the frequency to drift, and the NRZ data contains no spectral content at the bit rate, a frequency reference is necessary to guarantee lock in the case of large oscillator frequency covering range. Alongside with the single-loop CDR architecture as shown in Figure 1.2, technique to provide reference clock to the system to form another frequency-locking loop [10, 11, 12], [21, 23] are therefore increasingly common. This allows the VCO process-variation to be dynamically trimmed out, avoiding false locking. The purpose for addition of another frequency loop to the original PLL is also to cater to the limited pull-in range of the PLL for data recovery [12]. This problem is especially severe when the VCO range is too wide.

As illustrated in Figure 2.7, the CDR employs a two-loop approach: one loop for data

Figure 2.7: CDR with frequency acquisition loop.

phase tracking, and another loop for VCO frequency training. The frequency loop activates during the startup to use the external reference clock to train the VCO. When the frequency difference is less than a particular amount, the lock detector senses the small difference and switches over the selector so that the phase tracking loop takes over. Conversely, if the CDR clock frequency is out of tolerance, the CDR will toggle back to the frequency acquisition mode.

2.3 CDR Building Blocks

Phase detector and VCO are two of the most critical building blocks of the CDR. The phase detector provides the timing information about the spacing between the input data and the clock, which is further used to control the phase and frequency of VCO. As discussed earlier in Section 2.2, the phase detectors for CDR design can be divided into two groups:

Figure 2.8: A Hogge phase detector.

linear ([15], [24], [25], [16], [20]), and binary ([17]-[19]).

2.3.1 Linear phase detector

Presented in Figure 2.8 is the block diagram of Hogge phase detector [15]. Recognizing that a D flip-flop (DFF) produces a delayed replica of the input data, the result of the exclusive-OR the D_{in} and output of FF1, Q1, contains pulses whose width represents the phase difference between D_{in} and CLK. Hence, one can find that the circuit produces a pulse for each data transition, providing the edge detection, and the width of the output pulses varies linearly with the input phase difference [24]. Note that the retimed data at Q1 is delayed by half a clock cycle, $T_{CLK}/2$, and XORED with itself, pulses of width $T_{CLK}/2$ are produced at *Reference* for each data transition, which can be used as reference signal. Under locked condition, *Reference* and *Error* produce equal pulse widths.

A CDR system utilizing a linear PD exhibits a constant loop gain during lock transient and minimum charge pump activity after the loop locks. Hence, the VCO control voltage is relatively quiet. The difficulty in the design of high speed linear PD, however, lies in

Figure 2.9: An Alexander phase detector.

generating pulses which occupy a very small fraction of clock period at the PD outputs at a speed near the limit of the technology [25].

2.3.2 Binary phase detector

Figure 2.9 depicts the early-late detection method employed in the Alexander PD [17].

The early-late information is provided based on the following rules:

- If $S1 \oplus S2 = 0$ and $S2 \oplus S3 = 1$, the clock is early.

- If $S_1 \oplus S_2 = 1$ and $S_2 \oplus S_3 = 0$, the clock is late.
- If $S_1 \oplus S_2 = S_2 \oplus S_3$, no data transition is present.

The flipflops, FF1 and FF2, sample their D inputs at the rising clock edges and generate S_3 and S_1 respectively. FF3 samples the input data on the falling edge of CLK, and FF4 delays the sample by half a clock cycle, producing S_2 . The comparison of the flipflop outputs S_1 , S_2 and S_3 is launched at the second rising edge of CLK so that the XOR gates always generate valid outputs simultaneously.

As a binary system, the Alexander PD exhibits a very high gain at the vicinity of the zero phase offset between the input data and clock. As a result, a CDR system with this PD locks such that S_1 coincides with the data zero crossings and the falling edge of CLK automatically samples the data in the middle of the bit period.

Modified version of the Alexander PD had also been reported in the literature. In [21], a novel PD with simple architecture is designed. As shown in Figure 2.10, this PD consists of three master-slave flipflops. FF1 and FF2 sample the data on the falling and rising edges of clock, respectively, producing outputs that contain information on whether the clock leads or lags the incoming data. Flipflop FF3 then samples the output of FF2 by using FF1 output as the clock to generate binary signal to indicate the phase relationship between the clock and data. This design features a simplified physical design and reduced signal loading. But long sequences of 0s or 1s will deteriorate the proper function since the retimed data is treated as clock for FF3.

In contrast with the speed problem inherent in linear PDs, the greatest challenge of binary PDs lies in its creating significant ripple on the control line in the locked condition.

Figure 2.10: Bang-bang type phase detector used in [21].

This is because of the high gain in the vicinity of zero phase offset, thereby producing large jitter at the VCO output. The design used in [25] combines both linear and bang-bang PD by employing master-slave sample-and-hold technique to overcome the speed limitation of the linear PD and the high activity problem of binary PD.

2.3.3 Half-rate phase detector

A half-rate PD uses a clock with a frequency that is half the baud rate of the input data. The key concept behind the half-rate PD is the utilization of the in-phase and quadrature phases of the clock signals. Illustrated in Figure 2.11 is a half-rate solution for binary type PD. The implementation incorporates three flipflops, sampling the data by the multiphases of the clock. Some other half-rate binary PDs have also been implemented [14], [22]. A modified binary version of Anderson's PD [26] has been used in [14]. This PD suffers from complicated logics and therefore the increased delays in the PLL loop.

Figure 2.11: Bang-bang type half-rate phase detector.

2.3.4 Voltage-controlled oscillator

The VCO generates the recovered clock in the PLL-based CDR system. Although LC oscillator generates less noise than ring oscillator, the latter is often preferred over the former in the CDR applications. This is attributed to the wide PLL bandwidth which permits minimum phase noise contribution [13], [21], [25], [27], [28]. Another reason for choosing the ring oscillator over their LC counterpart is that the tuning range of LC oscillator is usually small, which makes compensation on process variations difficult.

The principle of oscillator as well as the operations of LC and ring oscillators is discussed in the following section. Some design techniques and challenges for high-speed ring oscillator are also reviewed in detail, along with the description of two widely accepted phase noise models for oscillator.

2.4 CMOS Ring Oscillator

In this section, the oscillator is reviewed in detail, especially the techniques and architectures that enable high speed ring oscillator operation. The section begins with an overview of the oscillator principles, following by the presentation of the general operation scheme of the LC oscillator. Since the focus of this thesis is on ring oscillator and its application, the ring oscillator is reviewed in depth. Finally, some existing phase noise models are also described.

2.4.1 Oscillator Principles

An oscillator outputs periodic signals. As such, it must entail a self-sustaining mechanism that allows its noise to grow and eventually become a periodic signal. An oscillator is basically a feedback network. Shown in Figure 2.12, the model is constructed from an amplifier block and a frequency-selective network connected in a positive-feedback loop.

Simple analysis of this system shows the transfer function to be written as follows

$$H(s) = \frac{Y(s)}{X(s)} = \frac{A(s)}{1 - \beta(s)A(s)} \quad (2.7)$$

where $A(s)$ is the s-domain transfer function of the amplifier block and $\beta(s)$ is the transfer function of the frequency-selective network.

The system has to sustain its oscillation even in the absence of an input signal, which means the open loop gain $A(j\omega_0)\beta(j\omega_0)$ should be equal to one at the frequency of oscillation ω_0 . Hence the magnitude of the loop gain should be equal to unity and the phase shift around the loop should be zero or an integer multiple of 2π as defined in Eqs. (2.8) and

Figure 2.12: Positive feedback s-model of oscillator.

(2.9). This is known as the Barkhausen criterion.

$$|A(j\omega_0)\beta(j\omega_0)| = 1 \quad (2.8)$$

$$\angle(A(j\omega_0)\beta(j\omega_0)) = 2n\pi \quad (2.9)$$

Note that the Barkhausen criterion only guarantees that the oscillation can be sustained after excitation, but it does not guarantee the oscillator's kick-start. A simple intuitive explanation can be given as follows [40]. Suppose the circuit is excited such that a certain signal has occurred at a certain node of the circuit. If the phase of the loop gain is zero or multiple of 2π , the signal will just go through the loop and return in phase, adding directly to the original signal. If the magnitude of the loop gain is smaller than unity, the feedback signal will be smaller than the original signal and the excitation will die. If the magnitude of the loop gain is larger than one, the feedback signal will be larger than the original signal and so the excitation will be amplified and the oscillator is started. In practice, the loop gain is designed to be slightly larger than unity for the oscillator to start. After successful excitation by the oscillator itself, the gain of the loop will drop to unity. This is attributed to the fact that as the signals get larger, the transistors' gain drop at larger signal and also due

to the hard-limiting of the power supply, a steady-state oscillatory signal can be ensured.

2.4.2 CMOS Integrated Oscillators

Integrated oscillators for high frequency applications are mainly implemented in ring oscillator and LC based oscillator. The circuit operations of these two oscillators are discussed in the following subsections.

I. LC Oscillator

As discussed in Chapter 1, LC oscillators have the best noise and frequency performance when compared with other type oscillators because of the use of passive resonant network with high Q factors. On the other hand, the disadvantages of LC-VCOs include large chip area for the on-chip inductors and a narrow frequency tuning range. An LC resonator contains an inductor and a capacitor as energy-storage elements and resistors as the lossy components. Ideally, the resonator will resonate at a frequency that is determined by $\omega_n = 1/\sqrt{LC}$. However, the oscillation will die out due to the tank loss as modeled by the two parasitic resistors, R_L and R_C . Hence, the loss in the tank has to be compensated for in order to sustain the oscillation. This can be done by introducing a negative resistance, $-G_m$, into the tank as illustrated in Figure 2.13. To provide the necessary negative transconductance for the lossy resonator, a cross-coupled differential pair is usually used. The implementation depicted in Figure 2.14 is a popular LC oscillator structure.

The varactors of LC oscillator can be implemented in a reversed biased diode junction,

Figure 2.13: LC tank with negative conductance compensation.

Figure 2.14: Popular LC-VCO structure with cross-coupled transistors to provide negative transconductance.

where the variable capacitance is obtained by a depletion capacitance, whereby the capacitance drops roughly as the square root of the bias voltage. Diode varactors, however, have obvious disadvantages such as low Q (often < 20) and low tuning range ($\pm 20\%$). A more popular option of the varactor implementations is the MOS varactor. MOS varactors are easily integrated in CMOS technology but has a relatively low Q factor.

Integrated spiral inductors and bonding wire inductors are usually used in LC oscillator. The bonding wire inductor can achieve a much higher Q factor (typically larger than 40) than the spiral inductors. Its disadvantages include difficult integration and the lack of accurate control over the inductance value. Spiral inductors are usually implemented using the top metal layer (in order to minimize the series resistance and the coupling to the substrate) in spiral shape (a patterned ground shield is often used). Spiral inductors have a moderate Q (5-10), but they are completely integrated. Addition of inductors in CMOS process, however, introduces problems such as eddy currents in the substrate and magnetic coupling.

II. Ring Oscillator

Ring oscillators, on the other hand, are suitable for monolithic system design using any digital CMOS process. A ring oscillator is realized by connecting a number of delay stages in series. The number of stages N must be odd for single-ended configuration. However, N can be even number if differential delay stages are employed as long as the connection at one of the stages is reversed in polarity to obtain an extra phase shift of 180° . The phase delay of each stage is dependent on the delay stage configuration and the number of stages.

Figure 2.15: A simple three-stage single-ended ring oscillator.

Figure 2.16: Four-stage differential ring oscillator with last stage reversed to provide the 180° dc phase shift.

For example, for a simple single-ended three-stage oscillator (Figure 2.15), each stage contributes 60° of frequency-dependent phase shift and 180° of dc phase shift, providing a total of 360° [42]. While for a four-stage differential ring oscillator (Figure 2.16), $\pi/4$ of ac phase shift is generated by each stage, and an extra dc phase shift of π is obtained by reversing the connection of the last stage and the first stage.

The linear model of the three-stage oscillator is depicted in Figure 2.17. So the transfer function can be written as

$$H(j\omega_0) = \left(\frac{-G_m R}{1 + j\omega_0 RC} \right)^3. \quad (2.10)$$

As discussed above, each stage contributes 60° . With unity loop gain at oscillation frequency ω_0 , Eq. (2.10) can be reexpressed as

$$\left(\frac{-G_m R}{1 + j\omega_0 RC} \right)^3 = 1, \quad (2.11)$$

Figure 2.17: Linear model of a three-stage ring oscillator.

and

$$\tan^{-1}(\omega_0 RC) = 60^\circ. \quad (2.12)$$

Therefore, we have

$$G_m R = 2. \quad (2.13)$$

In this case, the oscillator can oscillate and the output waveforms of the three stages are 60° out of phase with each other.

2.4.3 High-Speed Ring Oscillator Design Techniques and Challenges

As discussed in the previous section, the ring oscillator is more suitable for monolithic design and is much easier to implement than the LC oscillators. However, its Achilles heel involves poor phase noise and especially limitation on its highest achievable frequency. This section shall briefly discuss on some of the different techniques that have been exploited to improve on the frequency and the noise performance of the ring oscillators.

The frequency of the ring oscillator is directly dependent on the total delay around the whole loop. Generally there are two methods to improve the operating speed, i.e., to reduce

Figure 2.18: Two-stage ring oscillator.

the total loop delay. The first technique involves using minimum delay stages. For single-ended oscillators, a minimum of three stages have to be used while for the differential design, a minimum of two stages are required. Another way to increase the oscillation frequency is to minimize the delay of a single stage by modifying the stage design.

In [41], a two-stage ring oscillator is designed to achieve a high frequency using the $0.5\text{-}\mu\text{m}$ CMOS technology. The schematic of the delay cell is shown in Figure 2.18. In this design, a positive feedback PMOS pair is used to maintain the oscillation while the diode-connected PMOS pair and a tail current source transistor are used for frequency tuning. Consists of two delay cells, the oscillator covers a frequency range of $0.66\text{--}1.27\text{ GHz}$ using a 2.5-V supply voltage.

Other two-stage ring oscillator designs have also been reported. A double differential gain stage is presented in [43] to supply the required extra phase and gain in the two-stage oscillator design (see Figure 2.19). The current mirror load doubles the gain of the

Figure 2.19: Double differential delay stage from [43].

differential amplifier by folding the small signal current at one side and by combining it with the small signal current of the other side.

The oscillation frequency can also be improved by utilizing special architecture to reduce the delay of each single delay stage. The array oscillator proposed in [29] is one of such techniques. This design is structured as a two-dimensional array of dual-input inverting buffers. Each delay buffer has a ring input and a coupling input which are used to form a single loop oscillator and to couple to another single loop, respectively. The dual-input buffer stage is presented in Figure 2.20. Both the ring and coupling input transition times determine when the output transition will occur. The coupling input may lead or lag the ring input, just that the early coupling input reduces the buffer delay while the late coupling input increases the buffer delay. Therefore, care has to be taken when connecting the coupling loop so as to improve the oscillation frequency.

Figure 2.20: Maneatis dual-input buffer stage with symmetric load, ring and coupling inputs.

Similar to the array oscillator design in [29], Sun also proposes his sub-feedback ring oscillator design in [34], [44]. The concept behind the design is basically very similar to the Maneatis array ring oscillator. A special case of application of these two techniques is reported in [35], where a coupled two-stage ring oscillator is presented by connecting two two-stage ring oscillators together. This means that the single-loop consists of two buffer stages and the coupling loop (or sub-feedback loop) also consists of two buffer stages. The simple delay stage and the coupling top architecture make it possible for attaining ultra-wide frequency coverage, with operating frequency as high as 9 GHz.

2.4.4 Existing Phase Noise Models of Oscillator

A number of approaches have been proposed in the literature to analyze the phase noise of VCO, including early model developed by Leeson [45] and later models by Razavi [46], and Hajimiri [47]. Among these three models, the first two were developed based on the linear time-invariant (LTI) analysis and work well in LC oscillator and small signal ring oscillator. They are not suitable in the analysis of most ring oscillators that experience large signal operation, but they do provide a basic understanding of the oscillator noise. In contrast with the Leeson model, nonlinearity and cyclostationary effects are taken into consideration in Hajimiri model. Hence, this model achieves better accuracy on the prediction and analysis of the large signal ring oscillators, at the cost of more complicated calculation. The following subsections briefly review both the Leeson and the Hajimiri models.

I. Leeson's Phase Noise Model

In [45], Leeson developed an equation to describe the oscillator phase noise without any formal proof, which turned out to be the most widely known noise model. The single-sideband noise is expressed as

$$\mathcal{L}(\Delta\omega) = S_{\Delta\theta}(\Delta\omega) \left[1 + \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \right] \quad (2.14)$$

where $\left[1 + \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \right]$ is the noise shaping function, $S_{\Delta\theta}(\Delta\omega)$ is the spectrum of the input noise and defined as

$$S_{\Delta\theta}(\Delta\omega) = \frac{\alpha}{\Delta\omega} + \frac{2FkT}{P_s} \quad (2.15)$$

Figure 2.21: Phase noise PSD in an oscillator vs. frequency offset.

The input noise spectrum comprises of two parts: low frequency component ($\alpha/\Delta\omega$) due to the flicker noise terms, and the additive component ($2FkT/P_s$) due to the white noise terms. Other parameters used include center frequency ω_0 , offset frequency $\Delta\omega$, loaded quality factor Q , flicker noise constant α , excess empirical noise factor F and the signal level at oscillator active element input P_s .

Leeson model predicts the oscillator output noise in three different regions in terms of the offset frequency. As illustrated in Figure 2.21, in the first region, $(\omega_0/2Q\Delta\omega)^2 \gg 1$. Hence Eq. 2.14 can be simplified to

$$\mathcal{L}(\Delta\omega) = S_{\Delta\theta}(\Delta\omega) \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \quad (2.16)$$

In region I of Figure 2.21, phase noise is dominated by both the flicker noise and thermal noise sources and proportional to $1/\Delta\omega^3$, corresponding to a 30 dB/decade drop. The second region, that is region II, starts from the $1/f$ noise bandwidth f_1 and extends up to half of the feedback loop bandwidth, $f_2 = \omega_0/2Q$, where the $1/f$ noise effect no longer

predominates and that thermal noise sources dominate the phase noise output. The phase noise equation in this region can be simplified to

$$\mathcal{L}(\Delta\omega) = \frac{2FkT}{P_s} \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2. \quad (2.17)$$

In region II, the output noise is proportional to $1/\Delta\omega^2$, which corresponds to 20 dB/decade drop. This region extends from a few hundreds of KHz to tens or hundreds of MHz. Hence it is the most important region since many communication systems specify the noise requirement in this range.

For offset frequency above the feedback loop half-bandwidth, where $\left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \ll 1$, Eq. (2.14) reduces to

$$\mathcal{L}(\Delta\omega) = \frac{2FkT}{P_s}. \quad (2.18)$$

As a result, the input white noise is directly transferred to the output, thereby appearing as a flat noise region.

II. Hajimiri's Phase Noise Model

Leeson's equation is valid based on some restrictive assumptions. This makes its application limited, catering only to a selected class of oscillators. Besides, the noise factor at the operating power level and the input noise signal power have to be made known. This makes the model impractical for general oscillator noise analysis. A general phase noise model had been introduced by [47], which is capable of making accurate prediction about the phase noises of different types of oscillators. The model uses time-variant methodology through an impulse response approach for determine the excess phase of an oscillator. Since this model involves a lot of derivations and formulas, only some core concepts of

Figure 2.22: Effect of current noise injection on phase shift in oscillator node at different instants. (a) impulse applied near peak of the voltage, and (b) impulse applied at zero crossing.

the methodology are discussed in this part. The complete flow of calculation based on this methodology is applied on the proposed ring oscillator, which is described in detail in Chapter 5.

1. Impulse Sensitivity Function (ISF)

When a current impulse is injected into one of the oscillator nodes, both the amplitude and the phase shift at the node will change immediately. The amplitude effect will diminish as the oscillation progresses. This is because of the inherent automatic level constraint mechanism in the oscillator. However, the phase shift resulting from the injected charge will exist permanently, which will eventually become the jitter. The phase shift is proportional to the ratio of the injected charge and the maximum charge swing on that node, i.e., $\phi(t) \propto \Delta q / q_{max} = i(t)t / V_{max}C_{tot}$, where V_{max} is the maximum voltage swing on the node of interest and C_{tot} is total capacitance at that node. Note that the resulted phase shift from the injected charge is time dependent, as depicted in Figure 2.22. If the impulse is applied

near the peak of the voltage, maximum amplitude change will result but there will be very small phase shift. On the other hand, if the impulse is injected at zero crossing, maximum excess phase will be produced. Because of the periodical behavior of the system, the time dependence of the excess phase is also periodical, with the same period as the system. This leads to the unit impulse response for excess phase that can be expressed as

$$h_\phi(t, \tau) = \frac{\Gamma(\omega_0 \tau)}{q_{max}} u(t - \tau) \quad (2.19)$$

where $u(t)$ is the unit step, q_{max} is the maximum charge displacement on the node. $\Gamma(x)$ is called the *impulse sensitivity function* (ISF), which is defined as a dimensionless, frequency- and amplitude-independent periodic function with a period 2π that describes the amount of phase shift resulting from an injection of charge impulse at time $t = \tau$. ISF strongly depends on the output waveform shape. Figure 2.23 depicts the output waveform and the ISF of a typical ring oscillator.

Acknowledging the fact that the ISF is periodic, the output excess phase $\phi(t)$ can be calculated using superposition integral, and ISF can be expanded in a Fourier series, as

$$\phi(t) = \frac{1}{q_{max}} \int_{-\infty}^{\infty} \Gamma(\omega_0 \tau) i(\tau) d\tau \quad (2.20)$$

$$\Gamma(\omega_0 \tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 \tau + \theta_n) \quad (2.21)$$

where $i(t)$ is the input noise current injected into the circuit, c_n are the real valued Fourier coefficients and θ_n is the phase of the n th harmonic. Therefore,

$$\phi(t) = \frac{1}{q_{max}} \left[\frac{c_0}{2} \int_{-\infty}^t i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^t i(\tau) \cos(n\omega_0 \tau) d\tau \right] \quad (2.22)$$

This equation implies that only noise close to the harmonics of ω_0 and of DC can result in excess phase.

Figure 2.23: (a) Output waveform and (b) ISF of a typical ring oscillator.

2. Phase Noise Prediction

An equation that relates the oscillator output voltage Power Spectrum Density (PSD) to the excess phase variations is derived in [47]. An injected current at $n\omega_0 + \Delta\omega$ results in a pair of equal sidebands at $\omega_0 \pm \Delta\omega$ with a sideband power relative to the carrier given by

$$P_{SBC}(\Delta\omega) = 10 \cdot \log \left(\frac{I_n c_n}{4q_{max} \Delta\omega} \right)^2 \quad (2.23)$$

Based on Eq. 2.23, the single-sideband phase noise of an arbitrary oscillator in the $1/f^2$ region of the phase noise spectrum is derived as

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log \left(\frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{4 \cdot \Delta\omega^2} \right) \quad (2.24)$$

where $\mathcal{L}(\Delta\omega)$ represents phase noise spectral density in dB below the carrier per unit bandwidth due to the source on one node at an offset frequency $\Delta\omega$, $\overline{i_n^2}/\Delta f$ represents the white

PSD of input noise current, Γ_{rms} is the rms value of $\Gamma(x)$ and can be obtained from

$$\sum_{n=0}^{\infty} c_n^2 = \frac{1}{\pi} \int_0^{2\pi} |\Gamma(x)|^2 dx = 2\Gamma_{rms}^2 \quad (2.25)$$

The phase noise spectrum in the $1/f^3$ portion is expressed as

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log \left(\frac{c_0^2}{q_{max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{8 \cdot \Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega} \right) \quad (2.26)$$

It is also found that the $1/f^3$ phase noise corner due to internal noise sources is not equal to the $1/f$ device noise corner. Instead, it is smaller by a factor equal to $c_0^2/2\Gamma_{rms}$. Since c_0 depends on the waveform as $c_0 = \frac{1}{\pi} \int_0^{2\pi} \Gamma_{eff}(x) dx$ (where Γ_{eff} is the effective ISF [47]), it can be significantly reduced if the oscillation waveform exhibits certain symmetry property.

3. Some Design Implications from the Model

The Hajimiri model presents some important implications to the oscillator design.

First, increasing the maximum charge displacement q_{max} across the node capacitances reduces the phase noise at the cost of more dissipated power.

Second, noise power around the harmonics of the oscillation frequency is converted to the vicinity of the oscillation frequency corrupting the output signal, whereas noise power at other frequencies is mostly diminished in the system because of the averaging.

Third, as discussed previously, maximum value of ISF is observed around the waveform zero crossings. If the rise and fall times of the waveform are of significant difference, the ISF will have a large dc value. As a result, the close-in phase noise due to low-frequency noise sources will be larger. Hence, the symmetry of each half-circuit is important to reduce the close-in noise upconversion. Sharper signal transitions result in minimized ISF peak

value and therefore help to reduce the phase noise for ring oscillators.

To conclude, the operating principle of oscillator and some general architecture of LC and ring oscillator have been discussed in this chapter. Some existing techniques for improving on the ring oscillator frequency have also been reviewed. Two new ring oscillators are to be presented in the following two chapters, which analyze the ring oscillator in frequency and phase noise.

Chapter 3

Design of A 7-GHz Multiloop Ring

Oscillator in 0.18- μm CMOS Technology

In a PLL circuit, the VCO is probably the most important block in terms of operating speed and power consumption, since it limits the achievable frequency of the PLL and consumes a large amount of power in the circuit. Requirements for low phase noise, sufficient tuning range and acceptable power consumption therefor impose challenges in the design of VCOs.

As having been discussed in the previous chapters, the implementation of VCO can be categorized into two areas: ring oscillator and LC tank oscillator. LC oscillators are widely adopted in the wireless communication applications for their ease of achieving high frequency with low phase noise and power consumption. As compared to LC oscillator, the ring oscillator is much easier to implement and manifests a wider tuning range. It also occupies a much smaller area than the LC tank. The ring oscillator is also especially

attractive for multiphase or quadrature clock generation that is required in data sampling and clock data recovery systems. The bottlenecks of ring oscillator involve its poor phase noise performance and the achievable highest frequency since the ring oscillator operates by deploying the parasitic capacitances instead of the passive components in their LC-based counterparts. In this context, to explore circuit techniques for high frequency ring oscillator with acceptable phase noise performance has motivated the research of this work.

In this chapter, a novel delay cell for multiloop ring oscillator is demonstrated for operation in the 7-GHz range. A push-pull inverter is added into the delay cell as the secondary signal path to boost the operating frequency and to improve the phase noise performance.

3.1 Existing Ring Oscillator For Multi-Loop Architecture

The frequency of a conventional single-loop ring oscillator is limited by the smallest delay provided by the basic inverter delay cell. Hence, there is a necessity to apply other architectural techniques to boost the maximum frequency of the ring oscillators. Various techniques have been explored to attain the smallest possible delay per stage.

In [29], the dual-input array oscillator is for the first time proposed by Maneatis. By coupling several rings together, the array oscillator is able to break the dependence of the oscillation frequency on the number of buffers. The delay stage employed in the array oscillator has two inputs: the ring input and the coupling input. The coupling input is made possible by simply splitting the input devices in half. It should be noted that there is no requirement on the strength or linearity of the coupling input for the dual-input buffers.

Figure 3.1: Block diagram of 4-stage quadrature differential ring oscillator in [34].

The multiple-feedback-loop ring architecture is proposed in [30]. Double-feedback-loop and triple-feedback-loop current-controlled oscillators are implemented by using differential current steering logic (DCSL). The auxiliary loops are constructed simply by adding additional input transistors. The dual-delay-path technique is also proposed and utilized in [32], and reanalyzed as multi-pass oscillator in [33]. The most significant difference amongst the designs reported in [29], [30] and [32], [33] is that the latter two use PMOS to form the additional input paths instead of splitting the NMOS to construct multiple input signal paths as stated in [29] and [30]. A ring oscillator utilizing similar technique is also proposed in [31]. The new negative skewed delay cell is built by inserting a conceptual negative delay element at one of the two transistor inputs of the inverter. As compared to other designs which deploy differential delay stages, this negative skewed delay stage simply adopts an inverter that comprises a single PMOS and a single NMOS.

In [34], a method to increase the operating frequency of ring oscillators by creating sub-feedback loop is presented. The sub-feedback loop is established as a fast loop against

Figure 3.2: Topology of a three-stage multiloop ring oscillator.

the low loop by a normal feedback loop. Other similar ring oscillator architectures can also be found in the literature, such as the coupled ring oscillator [35].

It is important to point out that all the above discussed frequency-enhancement techniques share a common characteristic of reducing the stage delay by the conventional single loop, i.e., all of them depend on the use of additional shorter loop or loops that are essentially formed by inter-coupled feedback stages to increase the frequency. In this chapter, the proposed ring oscillator utilizes the same technique and is therefore named multiple-loop ring oscillator. Basically, all of these techniques are fundamentally similar and can be traced back to the array oscillator architecture introduced by Maneatis in [29].

3.2 Circuit Design

Illustrated in Figure 3.2 is the general topology of a three-stage multiloop ring oscillator. For this case, two operating loops, the primary loop (represented by the solid line) and the secondary loop (represented by the thin line), are involved. It can be seen that the primary

Figure 3.3: Typical delay cells accommodate multiloop technique. (a) NMOS input transistors split for secondary entry; (b) PMOS introduced for secondary entry.

loop is formed by all the three stages and works as a normal single-loop ring oscillator, while the secondary loop is constructed by two stages and provides an additional entry to the input/output transfer function. The extra entry helps to decrease the slew time of the output nodes, at the rising edge or falling edge depending on the secondary input devices.

From the earlier discussion of multiloop oscillators in section 4.1, it can be seen that the additional loop is formed by either splitting the input NMOS transistor or by introducing an additional PMOS input transistor, along with some other necessary frequency-tuning and bias current devices. In the designs reported in [29], [30] and [35], the input NMOS transistors are split for primary (V_{P+} and V_{P-}) and secondary (V_{S+} and V_{S-}) input entries and this is illustrated in Figure 3.3(a). The slew time at the falling edge is reduced since the secondary input transistors provide an early sink current to pull down the output nodes. Figure 3.3(b) shows a typical delay cell that makes use of the PMOS transistors as the

Figure 3.4: A three-stage implementation using delay cell in Figure 3.3b.

secondary input. Based on the same understanding, the slew rate at the rising edge of the designs reported in [32]-[34] can be faster since the secondary input PMOS transistors can help to source current to the output nodes. A three-stage ring oscillator implementation by using the above delay cell in Figure 3.3b is shown in Figure 3.4 which illustrates the connection of primary and secondary transistors.

In order to further increase the slew rate, the push-pull inverter is adopted in the proposed delay cell, as illustrated in Figure 3.5. Due to the fact that both early sink current and source current can be provided by the inverter, both the low-to-high and the high-to-low propagation delays will be reduced, resulting in higher frequency than that achieved by delay cell that involves active load inverter. In this circuit, N1 and N2 form the input pair of the primary loop, while inverters INV1 and INV2 serve as the input pair of the secondary loop. PMOS P1/P2 forms the load of the delay cell. Since the input voltage at V_{S+} is earlier than V_{P+} , the secondary input inverter will be already sourcing current to the load capacitor at the output node, $OUT-$, thus the low-to-high delay is decreased.

In order to avoid the loss of oscillation at the extreme cases of frequency tuning, extra

Figure 3.5: Delay cell of the proposed multiple-loop ring oscillator.

transistors, P3 and P4, are added in shunt with the controllable load P1 and P2. In this design, the gates of P3 and P4 are connected to GND to bias the transistors into the triode region of operation. This will provide enough current for charging the output node even when the control voltage approaches V_{dd} , to shut P1/P2 down completely.

The cross-coupled NMOS transistor pair is introduced for two purposes: (1) to prevent the differential output nodes from converging at the same voltage of V_{dd} or GND and (2) to reduce the slew time of the output nodes, from low to high and from high to low due to the positive feedback of the cross-coupled pair, to yield a better oscillator phase noise performance [37]. Note however that the improvement of robustness and phase noise is at the expense of lower frequency since it becomes more difficult for the output nodes to change their status due to the positive feedback latch. Thus, the cross-coupled latch

Figure 3.6: Simulation results comparison between the single-loop, active PMOS load and push-pull inverter ring oscillators.

may also be regarded as the load, whereby it causes the delay cell to be insensitive to the common-mode noise.

Based on the proposed delay cell, a single-loop three-stage ring oscillator and a modified ring oscillator which utilizes only the PMOS load as the secondary input are also simulated, to allow comparison with the original design using a push-pull inverter as the secondary input. All three oscillators are sized to consume the same amount of power for fair comparison. The schematic simulation results are given in Figure 3.6. The single loop ring oscillator can be tuned from 5.9 GHz to 7.5 GHz while the tuning range of the oscillator that uses PMOS load is 6.9 GHz to 7.96 GHz. The proposed oscillator that involves push-pull inverter is noted to cover an improved frequency range of 8.23 GHz to 9.3 GHz, which implies a frequency enhancement of 24% and 17% from the previous two circuits,

Figure 3.7: Simulation result illustrating the phase relationship between two inputs and the output.

respectively. This verifies the discussion presented earlier in this section. Figure 3.7 illustrates the simulated waveform of the proposed oscillator which depicts the phase relation between the primary/secondary inputs and the output.

It should be noted however that the speed in the proposed oscillator is improved at the expense of a lower swing amplitude. This is a reasonable outcome since the power is kept constant among the three circuits compared, while the average dynamic power consumed by ring oscillator is proportional to the operating frequency, load capacitance and square of the voltage swing, i.e., $P_{avg} \propto C_L V_{SW}^2 f$. The three circuits are designed to have the same device size so the parasitic load capacitance difference can be ignored. Intuitively, it can also be appreciated that the improved frequency is at the cost of higher power consumption if the same amplitude is to be sustained. This is because of the time overlap when both PMOS and NMOS transistors are switched on [31].

Figure 3.8: Die photograph of the proposed ring oscillator.

3.3 Experimental Results

To validate the performance of the proposed ring oscillator, a prototype chip has been fabricated using Chartered Semiconductor Manufacturing 0.18- μm one-poly six-metal CMOS process. Given in Figure 3.8 is the die microphotograph of the fabricated oscillator with a chip dimension of $440\ \mu\text{m} \times 430\ \mu\text{m}$ (including the pad frame). The core oscillator occupies only $140\ \mu\text{m} \times 100\ \mu\text{m}$. On-wafer probing was performed for the measurement. Ground-Signal-Ground (GSG) RF probe is used to measure the circuit. As illustrated in Figure 3.9, the oscillator demonstrates a measured frequency tuning range of 6.24 to 7.04 GHz when the control voltage changes from 1.3 to 0.3 V, with a relatively constant tuning gain of 750 MHz/V over the whole tuning range. The measured frequency deviation from

Figure 3.9: The measured frequency tuning characteristics of the fabricated ring oscillator.

the simulated result may be attributed to the interconnect line capacitance as well as the transistor resistive and capacitive parasitics. The current dissipation of the total chip is 60-71 mA, of which 20 mA is consumed by the two-stage CML buffer, with a supply voltage of 1.8 V.

The phase noise measurement is implemented by using an HP8563E spectrum analyzer. Figure 3.10 is a typical phase noise measurement plot with a phase noise result of -107.7 dBc/Hz at 10 MHz offset from the 6.25 GHz operating frequency. The noise is flat around 60MHz. Basically it means that the noise floor is as high as -120 dBc/Hz, which is contributed mainly by the circuit. The unfiltered power supply is also believed to contribute to some extent to the high noise floor. The measured corresponding output power spectrum with -10.07 dBm output power is plotted in Figure 3.11. The performance of the proposed ring oscillator is summarized in Table 3.1.

Figure 3.10: The measured phase noise of -107.7dBc/Hz at 10 MHz offset from the center frequency of 6.25 GHz.

Figure 3.11: The measured output spectrum at the center frequency of 6.3 GHz.

Table 3.1: Performance summary of the proposed ring oscillator

Technology	Chartered 0.18- μm 1P6M CMOS
Voltage Supply	1.8 V
Current	VCO core: 40 mA (@6.3GHz)
Consumption	Buffer: 20 mA
Tuning Range	6.24-7.04 GHz
Phase Noise	-107.7 dBc/Hz
at 10MHz offset	from 6.25 GHz
Chip Area	440 μm $\times$ 430 μm

3.4 Performance Comparison

The performance of the presented ring oscillator is compared with some reported ring oscillators in Table 3.2. The Figure-of-Merit (FoM) can be expressed as follows:

$$FoM = \mathcal{L}(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{dc}}{1\text{mW}}\right) \quad (3.1)$$

where $\mathcal{L}(\Delta f)$ is the measured phase noise at an offset of Δf from the carrier of f_0 and P_{dc} is the measured power dissipation of the oscillator in mW. From Table 3.2, it is evident that the presented design is able to achieve good results that are comparable to the recently reported ring oscillator designs. The design in [38] also uses 0.18- μm CMOS technology and is able to achieve comparable speed as the proposed design. However, it has inferior phase noise performance and consumes more power. The oscillator proposed in [35] covers a wider tuning range and achieves higher frequency than the presented work. This is unfortunately at a cost of much higher power consumption and poorer phase noise.

Table 3.2: Comparison of the implemented VCO with published designs

Reference	Tuning Range (GHz)	Technology μm	Power (mW)	Phase Noise (dBc/Hz)@ Δf , f_0	FoM (dBc/Hz)
[32]	0.75-1.2	0.6 CMOS	30	-117@600KHz, 906 MHz	-165.8
[33]	1.1-1.86	0.18 CMOS	-	-105.5@1MHz, 1.81 GHz	-
[35]	2.5-9	0.18 CMOS	135	-82@1MHz, 5 GHz	-135
[38]	4.3-6.1	0.18 CMOS	80	-85@1MHz, 5 GHz	-140
[39]	0.1-3.5	0.18 CMOS	16	-106@4MHz, 3.5 GHz	-153
This Work	6.24-7.04	0.18 CMOS	72	-107.7@10MHz, 6.25 GHz	-145.1

3.5 Summary

A novel delay cell of a CMOS voltage-controlled ring oscillator for operation in the 7-GHz range is demonstrated in this work. Push-pull inverter is engaged as the secondary input in the multiple-loop ring oscillator to boost the circuit’s operating frequency. Experimental results had proved the capability of the VCO to operate at high frequencies with a relatively constant tuning gain across the whole tuning range. Due to the introduction of the push-pull inverter as the secondary input as well as the cross-coupled transistor pair, both the rising and the falling times at the output nodes is significantly reduced, resulting in a faster operating speed and a lower phase noise. These characteristics are highly attractive for use in high-speed optical communication and in clock generation systems.

Chapter 4

Design and Implementation of Multi-GHz Ring Oscillator With Coarse and Fine Frequency Tuning

4.1 Overview of Coarse/Fine-Tuning VCO Design

Oscillators are required to cover multi-rate band for some systems such as the optical network (9.95 Gb/s for SONET/SDH, 10.71 Gb/s for Optical Transport Networks). On the other hand, due to the need for large frequency tuning range, a very high gain is necessary at a decreased supply voltage of deep-submicron CMOS processes. This will translate into high sensitivity to noise at its control input, which then seriously degrades the noise performance of the voltage-controlled oscillator and the phase-locked loop.

Various methods using the coarse/fine tuning have been developed to maintain the wide

tuning range as well as the moderate gain. For LC-tuned oscillators, a commonly used method is to adopt the digitally switched capacitor array to provide the coarse tuning steps, along with the continuous fine frequency tuning [48], [49]. Some other LC VCOs also make use of the analog coarse-tuning to suppress the VCO gain while achieving the large tuning range [50], [51]. For ring VCOs, however, very few circuits have been designed for this purpose. In [53], two delay cells are used to construct the coarse/fine-tuning VCOs. The coarse and fine tuning are implemented through controlling the tail current of the whole circuit. This will unfortunately increase the risk of the up-conversion of flicker noise from the tail current source transistors.

In this chapter, a new delay cell for 10-GHz frequency operation that is equipped with both coarse- and fine-tuning is proposed. The multiloop technique is adopted to push the circuit's operating frequency to the maximum. The fine-tuning is implemented by adjusting the current flowing through the positive feedback cross-coupled NMOS pair that is introduced for self-balancing. In contrary to the digital coarse tuning, the coarse tuning engaged in this work is implemented in an analog manner, to minimize the design complexity of the PLL circuit. For digital coarse tuning in VCOs, either external control of the digital input bits or internal on-chip calibration circuit is needed in the PLL loop. In the case of external control of the digital bits that are applied to the VCOs/PLLs, the frequency tuning characteristics has to be known beforehand. This is somehow impracticable due to the process drift during fabrication. This method also increases the number of pads and hence the die area. For the latter method, the calibration circuit is usually complicated and requires many digital supporting blocks. The advantages of the digital coarse tuning with

Figure 4.1: Three-stage multiloop ring oscillator.

calibration circuit lie in its fast and accurate settling [54].

4.2 Design of the coarse/fine-tuning ring oscillator

The proposed ring oscillator delay cell utilizes the multiloop technique. Illustrated in Figure 4.1 is a general architecture of a three-stage multiloop-pass ring oscillator. As mentioned in Section 3.1, the primary loop works as a normal differential ring oscillator, while the secondary loop provides an additional entry to the input/output transfer function. This extra entry can help to decrease the slew time of the output nodes, from low to high, since the secondary inputs are fed from the outputs that are a few stages prior to the current stage. The circuit schematic of the proposed delay cell and the full VCO circuit indicating primary and secondary connections are depicted in Figure 4.2 and Figure 4.3, respectively. In this circuit, N1 and N2 form the input pair of the primary loop, while PMOS P5 and P6 serve as the input pair of the secondary loop. PMOS P1/P2 forms the load of the delay cell. When

Figure 4.2: Proposed delay cell, with coarse- and fine- frequency tunings.

V_{P+} is lower than V_{tn} , transistor N1 shuts off. Since the input voltage at V_{S+} is earlier than V_{P+} , the secondary input transistor will be already conducting, to source current to the load capacitor at the output node, $OUT-$. As a result, the time for the output node to rise from low to high is decreased.

The tail current source transistors are avoided in this delay cell so as to reduce the noise upconversion and maximize the output swing as well. In order to avoid the loss of oscillation at the extreme cases of frequency tuning, extra PMOS loads, P3 and P4, are added in shunt with the controllable load P1 and P2. Coarse-tuning is accomplished by varying the load through changing the gate voltage of P1/P2. On the other hand, fine-tuning can be achieved by adjusting the amount of tail current flowing through the cross-coupled positive feedback transistors, N3 and N4. By properly choosing the transistor dimension and current of the cross-coupled transistors, the noise contributed and the noise

Figure 4.3: Full circuit schematic of the proposed oscillator.

upconversion from its tail current transistor can be minimized. The cross-coupled pair can also be regarded as the load and this load causes the delay cell to be insensitive to the common-mode noise.

4.3 Frequency Characteristic Analysis

4.3.1 Small-Signal Model of the Oscillator

The ring oscillator design involves many tradeoffs, especially the power, frequency and noise performance. Due to the nonlinearity that is contributed by the large signal operation and the complexity due to the involvement of too many transistors, the ring oscillator poses difficulties when it comes to the analysis of the frequency characteristics. Although there exist some methods to predict the operating frequency of the ring oscillator, they are either too complicated or structure-limited and cannot be applied to all oscillator structures.

In our analysis, in order to gain an insight to the frequency operation and the tuning of the circuit, a simple method reported by [44] is engaged as a starting point of the frequency characteristic analysis. The small signal model discussed in this section assumed the oscillation amplitude to be small and the waveform shape is sinusoidal. The first-order approximation of each gain stage is shown in Figure 4.4, where g_{mp} and g_{ms} represent the transconductances from the primary input to the output, and from the secondary input to the output, implemented by using N1/N2 and P5/P6, respectively. g_{mc} is the equivalent transconductance between the differential outputs which is constructed by the cross-coupled latch N3 and N4. R and C are the equivalent resistance of the PMOS load and

Figure 4.4: First-order model of the proposed ring oscillator gain stage.

the equivalent capacitance seen at each differential output, respectively. We define θ as the phase difference between the output node and the primary input node, and ϕ as that between the output node and the secondary input node. Thus for each half stage, the following equations may be derived:

$$V_{OUT-} = V_{P+} e^{-j\theta} \quad (4.1)$$

$$V_{OUT-} = V_{S+} e^{-j\phi} \quad (4.2)$$

$$V_{OUT-} = V_{OUT+} e^{-j\pi} \quad (4.3)$$

Use KCL at the output node, OUT-,

$$V_{OUT-} = \frac{R}{1 + j\omega RC} (-g_{mp} V_{P+} - g_{ms} V_{S+} - g_{mc} V_{OUT+}) \quad (4.4)$$

Substituting (4.2) and (4.3) into (4.4) and rearranging V_{OUT-} and V_{P+} , we get

$$V_{OUT-}(1 + j\omega RC + g_{ms}Re^{j\phi} + g_{mc}Re^{j\pi}) = -g_{mp}RV_{P+} \quad (4.5)$$

Therefore the transfer function $H(j\omega)$ can be written as

$$\begin{aligned} H(j\omega) &= \frac{V_{OUT-}}{V_{P+}} \\ &= \frac{-g_{mp}R}{(1 + g_{ms}R \cos \phi - g_{mc}R) + j(\omega RC + g_{ms}R \sin \phi)} \end{aligned} \quad (4.6)$$

Since the phase of $H(j\omega)$ is $-\theta$, so

$$\begin{aligned} \angle H(j\omega) &= -\tan^{-1} \left(\frac{\omega RC + g_{ms}R \sin \phi}{1 + g_{ms}R \cos \phi - g_{mc}R} \right) \\ &= -\theta \pm \pi \end{aligned} \quad (4.7)$$

Taking tangent at both sides and rearrange in terms of ω , the relationship between the oscillation frequency and the small-signal model's parameters can be obtained.

$$\omega = \frac{\tan \theta}{RC} + \frac{g_{ms}(\cos \phi \tan \theta - \sin \phi)}{C} - \frac{g_{mc} \tan \theta}{C} \quad (4.8)$$

From the above equation, it can be easily denoted that the first term represents the primary loop operating frequency, and is determined by the time constant and the number of delay stages, n , since θ is defined by n . The second term in the equation illustrates the effect of the oscillation frequency attributed by the secondary loop. In order to improve the oscillator speed, the term, $\cos \phi \tan \theta - \sin \phi$, has to be positive. This is because $\pi < \theta \leq 3\pi/2$ (i.e., $\theta = 3\pi/2$ when $n = 2$, θ approaches π when n increases), which implies that $\tan \theta$ is always a positive value. Thus, the secondary loop has to be properly connected

to ensure that the above term is positive. On the other hand, a larger g_{ms} will result in a greater frequency improvement. But this improvement is nonlinear since larger secondary input transistors leads to extra capacitance at the output node. The third term in Eq. (4.8), however, corresponds to the frequency change that is contributed by the cross-coupled NMOS pair. We can see that the introduction of the cross-coupled pair slows down the circuit speed by a factor that is proportional to the transistor transconductance. Hence, decreasing the transistor size or the drain current will reduce the slow-down effect.

For qualitative analysis, the cross-coupled NMOS pair can also be viewed as a latch, which makes it more difficult for both the differential outputs to change their status. Although this pair slows down the circuit operating speed, it is still essential since they can help to prevent the differential outputs from converging at the same voltage level. This convergence shall bring the differential stage back to a single-ended stage. The positive feedback caused by the cross-coupled pair also reduces the slew time of the output nodes, from low to high or from high to low, which results in a better oscillator phase noise performance [37]. Meanwhile, an additional channel to fine-tune the oscillator is also obtained by controlling the current flowing through them.

From Eqs. (4.6) and (4.7), and according to the Barkhausen criterion of oscillation, the minimum required dc gain of each stage can be written as

$$g_{mp}R \geq \left| \frac{1 + g_{ms}R \cos \phi - g_{mc}R}{\cos \theta} \right| \quad (4.9)$$

which is the minimum requirement to be considered in the design process.

Based on the above qualitative analysis, the transistors are sized for operation in the

Table 4.1: Transistor sizes of the proposed 3-stage ring oscillator delay cell (μm)

	N1	N3	N5	P1	P3	P5
W/L	40/0.18	2/0.18	12/0.5	20/0.18	20/0.18	15/0.18

Where V_x and V_x' indicate negative and positive outputs, respectively.

Figure 4.5: Small-signal model of the proposed 3-stage multi-pass ring oscillator.

Figure 4.6: Phase relationship of the differential stages in the ring VCO.

10-GHz frequency range. The length of the tail current source transistor of the cross-coupled pair is increased to $0.5 \mu\text{m}$ without changing the W/L ratio. Thus, the $1/f$ noise is minimized to the greatest possible extent. The final sizes are tabulated in Table 4.1. The secondary loop is connected as that shown in Figure 4.5. Figure 4.6 illustrates the phase relationship between the three stages. It can be seen that for this connection scheme, $\theta = 4\pi/3$ and $\phi = 5\pi/3$, which give the necessary positive value for the second term in Eq. (4.8).

4.3.2 Oscillator Frequency Prediction

As mentioned in Subsection 4.3.1, R and C represent the equivalent resistance and capacitance seen from each output node. In this subsection, the calculation of R and C will be discussed in order to predict both the VCO frequency and the tuning characteristics.

To simplify the calculation, the cross-coupled pair along with the tail transistor will

Figure 4.7: Operation regions illustration of P1/P2.

be ignored to derive the equivalent resistance and capacitance without weakening the effectiveness of the calculation. Since the oscillator is in reality experiencing a full-swing oscillation, the equivalent resistance should be a function of time. For the PMOS P3/P4 seen in Figure 4.2, since $|V_{gs}| = V_{DD}$, the transistors are assumed to be operating in the linear region throughout the entire cycle. The corresponding resistance can therefore be expressed as

$$\begin{aligned}
 R_{P3}(t) &= \frac{1}{k(V_{DD} - |V_{tp}| - (V_{DD} - V_{OUT-}(t)))} \\
 &= \frac{1}{k(V_{OUT-}(t) - |V_{tp}|)}
 \end{aligned} \tag{4.10}$$

where k represents $\mu_p C_{ox} W/L$. Hence, an accurate R_{P3} can be evaluated by averaging the above equation across one cycle.

For P1/P2, it is not trivial to calculate the conductance since the working region depends

not only on $V_{OUT-}(t)$ but also on the gate voltage, V_{coarse} . The working region can be schematically illustrated in Figure 4.7. Similar to the case of P3/P4, the following equation can be derived to evaluate R_{P1} :

$$R_{P1} = \left\{ \begin{array}{ll} \frac{1}{k(V_{out-} - V_{coarse} - |V_{tp}|)} & \text{if } V_{out-} > V_{coarse} + |V_{tp}| \\ \frac{1}{0.5\lambda k(V_{DD} - V_{coarse} - |V_{tp}|)^2} & \text{otherwise} \end{array} \right\} \quad (4.11)$$

When evaluating the effective conductance of the two pairs input transistors, the gate and drain voltages are assumed to be fixed at zero-crossing differential voltage, V_{CM} , since it is unpractical to calculate the time-varying resistance.

The equivalent load capacitance C can be broken down into two parts: parasitic capacitance of current stage C_L and the gate capacitance from next stage C_{in} , and is expressed as

$$\begin{aligned} C &= C_L + C_{in} \\ &= [(C_{db} + C_{gd})_{P1} + (C_{db} + C_{gd})_{P3} + (C_{db} + (1 + |\cos \phi|)C_{gd})_{P5} \\ &\quad + (C_{db} + (1 + |\cos \theta|)C_{gd})_{N1}] \\ &\quad + [(C_{gb} + (1 + |\cos \phi|)C_{gd})_{P5} + (C_{gb} + (1 + |\cos \theta|)C_{gd})_{N1}] \end{aligned} \quad (4.12)$$

where the gate-drain capacitances of the input transistors are multiplied by a factor of $1 + |\cos \phi|$ and $1 + |\cos \theta|$, respectively, with consideration for the Miller effect.

Figure 4.8 presents the calculated g_{ds} of P1/P2 and the overall conductance seen from the output node that vary with V_{coarse} . The load capacitance C is calculated to be 285 fF when V_{coarse} is set to 0 V.

Figure 4.8: Conductance (g_{ds}) of P1/P2 and the overall conductance seen from the output node vs. V_{coarse} .

4.4 Simulation of Oscillator Frequency

The validity of the analysis presented in the previous section can be verified using simulations. The frequency simulation is performed on the VCO by using SpectreRF in Cadence. The simulation and the calculated frequency results using Eq. (4.8) are both illustrated in Figure 4.9. In both cases, V_{fine} is fixed at 1.8 V. The large discrepancy between the predicted value and the simulation result at the lower frequency end of Figure 4.9 may be due to the parasitic load capacitance that has in fact risen when V_{coarse} is tuned high, whereas in calculations C is fixed at the calculated value when $V_{coarse} = 0$ V.

The fine tuning characteristic of the oscillator is plotted in Figure 4.10, with coarse tuning control voltage V_{coarse} ranging from 0 V to 1.3 V at a 0.1 V interval. A sudden transition is noted when the fine control voltage is set to around 0.7 V. In this region, the

Figure 4.9: Comparison of simulated and analytical frequency characteristics with the coarse tuning.

Figure 4.10: Frequency against fine control voltage with coarse control voltage ranging from 0 V to 1.3 V at 0.1 V intervals.

VCO gain escalates to a range of 650-900 MHz/V but within a narrow frequency band. On average, the fine tuning gain varies from 220 MHz/V to 160 MHz/V when the coarse control voltage is increased.

4.5 Phase Noise Analysis

Phase noise analysis through appropriate noise model can help the designer to make informed decisions on the tradeoffs that are involved in the ring oscillator in terms of power, area and noise performances. Since the circuit of Figure 4.2 is symmetrical, a half-circuit of the delay cell may be considered for noise analysis. The phase noise prediction is based on the Hajimiri-Lee noise model [37].

As discussed in Section 2.4.4, in [37], the phase noise of an oscillator in the regions of $1/f^3$ and $1/f^2$ are respectively defined as follows:

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log \left(N \cdot \frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{4 \cdot \Delta\omega^2} \right) \quad (4.13)$$

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log \left(N \cdot \frac{c_0^2}{q_{max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{8 \cdot \Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega} \right) \quad (4.14)$$

N in the above equations is the number of noise stages, i.e., $N = 6$ for a 3-stage differential ring oscillator. The quantity Γ_{rms} is the *rms* value of the ISF, c_0 is twice the dc value of the ISF function and is defined as $1/\pi \cdot \int_0^{2\pi} \Gamma(x) dx$. The ISF is plotted by measuring the excess phase shift a few tens of cycles after injecting a current impulse into the node of interest across one period of the oscillation. The duration of the impulse should be set small enough so as to improve on the accuracy of the calculated ISF. $\overline{i_n^2}/\Delta f$ is the noise current PSD of the active devices.

The power densities of the noise sources in the oscillator are required for the calculation of the phase noises [i.e., using Eqs. (4.13) and (4.14)]. The oscillator system is itself periodically time varying. Likewise, the random noise sources involved in the oscillator also change with time in a periodic manner, which is referred to as *cyclostationary noises* [37]. As for our proposed oscillator design, the noise power of the primary input transistors, N1/N2, and the secondary input transistors, P5/P6, are all modulated by the gate source overdrives since the gate voltages vary with time. For PMOS transistors, P1/P2 and P3/P4, although the gate voltages are fixed to dc values, the drain voltages vary with time which also modulate the drain induced noise power. The cyclostationary noise can be treated as a stationary noise that is applied to the system, with an effective ISF given by

$$\Gamma_{eff}(x) = \Gamma(x) \cdot \alpha(x) \quad (4.15)$$

where $\alpha(x)$ is known as the *Noise Modulation Function (NMF)* and can be obtained from device noise characteristics. By applying this expression to Eqs. (4.13) and (4.14), they can be rewritten as

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log \left(N \cdot \frac{\Gamma_{rms,eff}^2}{q_{max}^2} \cdot \frac{\overline{i_{n0}^2}/\Delta f}{4 \cdot \Delta\omega^2} \right) \quad (4.16)$$

$$\mathcal{L}\{\Delta\omega\} = 10 \cdot \log \left(N \cdot \frac{c_{0,eff}^2}{q_{max}^2} \cdot \frac{\overline{i_{n0}^2}/\Delta f}{8 \cdot \Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega} \right) \quad (4.17)$$

The calculated ISF, Noise Modulation Functions (NMFs) and effective ISFs are all presented in Figure 4.11. Since N3/N4 and the tail transistor N5 contribute much less noise than the rest of the transistors, they are neglected in our analysis. The noise current PSD of the active devices in the ring oscillator can be modeled as

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{\overline{i_{n,d}^2}}{\Delta f} + \frac{\overline{i_{n,g}^2}}{\Delta f} = 4kT\gamma_{gd0} + 4kT\delta g_g \quad (4.18)$$

Figure 4.11: ISF, NMF and effective ISF of P1/P3/P5/N1 at $V_{coarse} = 0.5V$. N3/N4/N5 are neglected since they contribute much less noise than others.

where $\overline{i_{n,d}^2}/\Delta f$ and $\overline{i_{n,g}^2}/\Delta f$ represent the drain and gate induced noises of the MOS devices, respectively. γ and δ model the excessive noise of the short channel devices. $\gamma = 2.5$ and $\delta = 2\gamma = 5$ are chosen for the 0.18- μm process that is engaged in this work. g_{d0} is the channel conductance at zero V_{ds} . The gate conductance g_g can be approximated to be [55]

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \quad (4.19)$$

The calculated parameters when $V_{coarse} = 0.5$ V are tabulated in Table 4.2. Since the thermal noise dominates the overall phase noise performance of the circuit, the thermal noise contributions by the four transistors are also listed in the table for comparison. Although the largest transistor N1 contributes nearly half of the thermal noise, N1 has to be large enough to provide sufficient dc gain of the delay stage, so as to maintain oscillation at high frequency.

The calculated phase noise of our proposed oscillator is -100.2 dBc/Hz at 1-MHz offset from the center frequency of 10.39 GHz. This is only of 0.5 dB difference from the simulated -99.7 dBc/Hz, that is obtained from Cadence SpectreRF. The performance of the proposed 10-GHz ring VCO is summarized in Table 4.3. The current consumptions vary from 31 mA to 40 mA when the oscillation frequency is tuned from 9.3 GHz to 11.4 GHz.

Table 4.2: Calculation Results for Phase Noise Analysis

	Γ_{rms}	c_0	$\overline{i_n^2}/\Delta f$	Thermal Noise Contribution
P1	0.154	0.0564	3.5753E-22	9%
P3	0.2611	-0.0041	5.292E-22	29.5%
P5	0.275	-0.0027	1.347E-22	10.4%
N1	0.2035	-0.0868	14.88E-22	51.1%

Table 4.3: Performance summary of the proposed VCO

	Analytical	Simulation
Voltage supply	1.8 V	1.8 V
Current	-	31-42 mA
Tuning range	9.6-11.6 GHz	9.3-11.4 GHz
Phase noise ($V_{coarse}=0V,@1MHz$)	-100.0 dBc/Hz	-99.6 dBc/Hz
Phase noise ($V_{coarse}=0.5V,@1MHz$)	-100.2 dBc/Hz	-99.7 dBc/Hz
Phase noise ($V_{coarse}=1.3V,@1MHz$)	-100.3 dBc/Hz	-99.8 dBc/Hz

Figure 4.12: The simplified cross-sectional view of NMOS transistor in triple-well technology.

4.6 Implementation of proposed coarse/fine-tuning ring oscillator in 0.13- μm CMOS technology

4.6.1 Circuit implementation

To validate the performance of the proposed ring oscillator, the circuit was fabricated in a standard one-poly six-metal 0.13- μm triple-well digital CMOS technology. The cut-off frequency f_T of NMOS transistor in this technology is over 90 GHz. The triple well process offers a better performance in terms of noise isolation and bulk control as compared to conventional P-Well technology. As illustrated in the simplified cross-sectional view in Fig. 4.12, the buried deep N-Well isolates the bulk of NMOS from the common P-substrate, thereby effectively minimizes the noise coupling from P-substrate to NMOS bulk.

Table 4.4: Transistor Sizes of the proposed 0.13- μm CMOS ring oscillator delay cell (μm)

	N1	N3	N5	P1	P3	P5
W/L	35/0.13	5/0.13	20/0.4	15/0.13	15/0.13	15/0.13

Figure 4.13: The calculated (a), Impulse Sensitivity Function (ISF); (b), Noise Modulation Function (NMF); and (c), effective ISF of transistors N1, P1, P3 and P5.

According to the analysis in previous sections, the transistors are sized as shown in Table 4.4. The length of the tail current transistor of the cross-coupled latch is increased to 0.4 μm to minimize the $1/f$ noise impact originated from the ripple appearing in the fine-tuning voltage. The calculated ISF, NMFs and effective ISFs are all illustrated in Figure 4.13. The calculated phase noise of our proposed oscillator is -102.5 dBc/Hz at 1-MHz offset from the center frequency of 7.5 GHz.

A two-stage buffer has also been designed to drive the bondpads and the probe. An inverter buffer stage is inserted between the VCO and the 50- Ω output buffer to isolate the ring oscillator stages from the output load.

Figure 4.14: The die photograph of the ring oscillator.

4.6.2 Experimental results of the proposed 0.13- μm CMOS ring oscillator

Figure 4.14 shows the die photograph of the fabricated oscillator with a chip dimension of $500\ \mu\text{m} \times 320\ \mu\text{m}$ (including the pad frame). The core oscillator occupies only $180\ \mu\text{m} \times 50\ \mu\text{m}$. On-wafer probing was performed for the measurement.

Two additional pads (marked as TS in Figure 4.14) were added to cater to troubleshooting in the event of failure such as to kick start its oscillation. Two differential internal nodes of the VCO are connected to these two pads at the cost of a lower operating frequency since additional parasitic capacitances introduced by the pads into the oscillator loop make an influential impact on the circuit's operating frequency.

The coarse- and fine-tuning characteristics were measured and the results are plotted in Figures 4.15 and 4.16, respectively. As seen in Figure 4.15, the oscillator is able to

Figure 4.15: Measured coarse frequency tuning characteristics of the 0.13- μm CMOS ring oscillator when V_{fine} is fixed at 0 V.

Figure 4.16: Measured fine frequency tuning characteristics of the 0.13- μm CMOS ring oscillator.

Figure 4.17: Phase noise measurement result at 7.64 GHz.

operate from 7.44 to 7.86 GHz when V_{fine} is fixed at 0 V and with V_{coarse} tuned. The coarse tuning range shifts to 7.28 to 7.6 GHz when V_{fine} is fixed at 1.2 V, where the cross-coupled latch is tuned on. It is noted from Figure 4.15 that the coarse frequency tuning gain is about 380 MHz/V when $V_{fine} = 0$ V. Figure 4.16 illustrates the fine tuning characteristics with varied coarse control voltages. A lowered fine frequency tuning sensitivity is denoted at around 115 MHz/V. The fine tuning sensitivity can be further reduced by using smaller W/L sizes for the cross-coupled latch. In contrast, the coarse tuning gain can be increased by using larger W/L sizes of transistors P1/P2.

The phase noise measurement is characterized using the HP8563E spectrum analyzer. Figure 4.17 presents a typical phase noise measurement result of -103.4 dBc/Hz at 1 MHz offset from the 7.64 GHz operating frequency, at $V_{coarse} = 0.5$ V and $V_{fine} = 0.8$ V. The

Figure 4.18: Output power spectrum at an operating frequency of 7.42 GHz.

Table 4.5: Comparison with other ring oscillator designs

Reference	Tuning Range (GHz)	Technology	Power (mW)	Phase Noise (dBc/Hz@ Δf , f_0)	FOM (dBc/Hz)
[53]	2.4	0.35- μ m CMOS	-	-97@1MHz, 2.4 GHz	-
[44]	0.75-1.2	0.6- μ m CMOS	30	-117@600KHz, 906 MHz	-165.8
[39]	0.1-3.5	0.18- μ m CMOS	16	-106@4MHz, 3.5 GHz	-153
[56]	9.8-11.5	30 GHz BiCMOS	75	-94.3@2MHz, 11.5 GHz	-151
[38]	4.3-6.1	0.18- μ m CMOS	80	-85@1MHz, 5 GHz	-140
[57]	5.3-9.3	47 GHz SiGe	54	-74.3@1MHz, 9.3 GHz	-136.4
This Work	7.3-7.9	0.13- μ m CMOS	60	-103.4@1MHz, 7.64 GHz	-163.3

Table 4.6: Performance summary of the fabricated VCO

Technology	0.13- μm CMOS with 1P6M
Die Size	500 μm $\times$ 320 μm
Tuning Range	7.2 - 7.9 GHz
Tuning Sensitivity	Coarse: 380 MHz/V Fine: 115 MHz/V (average)
Supply Voltage	1.5 V
Current Consumption	61 mA (40 mA by VCO core)
Phase Noise@1MHz offset	-103.4 dBc/Hz (from 7.64 GHz)

corresponding output power spectrum with -7.2 dBm output power is plotted in Figure 4.18. At a supply voltage of 1.5 V, the power dissipation of the total chip is 113 mW, and 60 mW is consumed by the VCO core.

Results of other ring oscillator designs are also tabulated in Table 4.5 for comparison. The Figure-of-Merit (FoM) is expressed as

$$FoM = \mathcal{L}(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{mW}}{1mW}\right) \quad (4.20)$$

where $\mathcal{L}(\Delta f)$ is the measured phase noise at an offset of Δf from the carrier f_0 and P_{mW} is the measured power dissipation of the oscillator in mW. From the table, it is evident that our proposed design is able to achieve good results that are comparable to those recently reported ring oscillator designs. The performance of the ring oscillator is summarized in Table 4.6. In addition to providing a coarse/fine tuning scheme, the presented oscillator also achieves a competitive phase noise performance as compared to other designs. The

tuning sensitivity of this oscillator can be as low as 115 MHz/V while that of other designs is as high as a few GHz/V. The disadvantage of the fabricated design over other designs is its narrow coarse tuning range, but this can be rectified by increasing the size ratio between load transistors P2/P2 and P3/P4 (see Figure 4.2).

Chapter 5

Design of a 10+ Gb/s Half-Rate

Bang-Bang Type CDR System

This chapter describes the design and simulation results of a CMOS clock data recovery system. The circuit incorporates a four-stage multi-loop voltage-controlled ring oscillator and a half-rate binary phase detector. The CDR architectures and its design issues will be presented in the section to follow. Details on the design of the building blocks, the behavioral simulation results performed using VHDL-AMS, and the transistor-level simulation results will all be discussed at a later section.

5.1 CDR Architecture

The choice of the CDR architecture is primarily determined by the speed limitation of the technology as well as the power dissipation of the system. In a full-rate CDR circuit for 10

Gb/s application, the phase detector compares the phase of the incoming 10 Gb/s data with the phase of 10 GHz clock generated by the VCO. The VCO here is heavily loaded as it has to drive the phase detector, the decision circuit and the frequency divider in a dual-loop architecture. If a 0.18- μm CMOS technology is to be used, the full rate CDR architecture may pose severe difficulties in 10 Gb/s operation. It is therefore desirable to employ a half-rate architecture instead, requiring the VCO to run at only 5 GHz. This will ensure a better reliability for the operation of the CDR.

Because of the limited pull-in range of the CDR phase locking loop, a frequency-aided loop is often a must to deal with the wide VCO frequency range and the process variation's effect on the VCO free-running frequency. For a wideband VCO, thousands of samples are also required to lock onto the incoming data stream without the frequency-aided loop. In this work, we choose the architecture discussed earlier in Section 2.2 and redraw it in Figure 5.1. This structure features a large frequency acquisition range while maintaining a precise control of the clock phase to achieve the jitter tolerance requirement. The reference frequency is chosen to match the expected clock frequency range. The additions of the reference clock and the lock-detection circuit ensure that the VCO maintains a certain operating frequency, and help to provide a more predictable lock time in startup conditions. Since the frequency loop is shut off when the VCO frequency is close enough to the data rate, it does not contribute much to the jitter performance of the overall system as long as stability is maintained.

During power-up or when the input data signal has been lost, the CDR locks to the reference clock. Once the VCO frequency is within a particular amount of the desired value, the

Figure 5.1: CDR with frequency acquisition loop.

CDR is switched to data-locking mode, where the half-rate Alexander-type phase detector is switched in and the phase/frequency detector is switched out. A linear phase detector is not used in our design. This is because at 10-Gb/s data rates accurate phase measurements are extremely difficult to achieve with reasonable power. Circuit imperfections cause the Hogge phase detector characteristic to deviate from the ideal odd-function characteristic, resulting in static phase error, which will ultimately degrade bit error rate performance. Due to the speed limitations of the technology, the output of the binary phase detector varies with the phase offset when clock is close to the data transition [58]. This means the phase detector output has a slope instead of a vertical step when the phase offset is small. This slope determines the bandwidth of the CDR when the loop is in lock. Because the characteristics of binary phase detector exhibits a strong dependence on the data pattern

and data signal integrity, the finite slope of the phase detector, or the effective gain, and the eventual loop bandwidth are all dependent on the input data pattern and jitter. As an example, when the jitter on the input data is increased, the phase detector effective gain will reduce proportionally and so is the open loop bandwidth which makes the CDR acts slower.

The CDR employs the second-order loop filter. The filter elements are determined by the transfer characteristics of the system. C1 is implemented off-chip to save the die area and for convenient adjustment of the loop bandwidth. C2 is much smaller compared with C1. Low jitter peaking is achieved by over-damping the phase tracking loop.

Although the data-tracking loop is nonlinear, it is still possible and necessary to derive some useful analytical formulas to analyze the jitter performance and loop dynamics of the CDR loop. Since the loop filter C1 is typically large, the oscillator control voltage tracks $I_{cp}R1$, which results in triangular variation of the VCO output phase. Due to the fact that the loop is overdamped, the PLL jitter transfer JTRANS(f) approaches a single-pole low-pass-type response with the bandwidth inversely proportional to the input jitter amplitude. The slew-limited -3dB bandwidth of the system can be approximated as [59]:

$$F_{3dB}(\phi_{in,p}) = DF \cdot \frac{\Delta F_{bb}}{2\phi_{in,p}} \quad (5.1)$$

where F_{3dB} is the 3-dB bandwidth of the CDR jitter transfer function; $\phi_{in,p}$ is the peak value of input jitter; DF is the average data transition density factor; ΔF_{bb} is the bang-bang frequency step given by:

$$\Delta F_{bb} = I_{cp}RK_{VCO} \quad (5.2)$$

where I_{cp} is the charge-pump current, R is the filter resistor value and K_{VCO} is the VCO

Figure 5.2: Jitter tolerance of a bang-bang CDR loop.

gain.

The entire jitter transfer function is also approximated to be

$$\frac{\phi_{out,p}}{\phi_{in,p}}(s) = \frac{1}{1 + \frac{s}{\omega_{3dB}}}. \quad (5.3)$$

The jitter tolerance performance of bang-bang CDR loop is derived as illustrated in Figure 5.2, where $\omega_1 = K_{VCO}I_{cp}R/2$ and $\omega_2 = 0.63\pi/RC_1$ [59].

In order to satisfy the SONET tolerance mask, the jitter transfer bandwidth defined in 5.1 should be set above 4 MHz at a jitter amplitude of $Jitter_{pp} = 0.15$ UI (i.e., 15 ps_{pp} for 10 Gb/s application) and minimum DF .

The *jitter generation* in a binary CDR system is proportional to the frequency step and the delay through the PLL loop, expressed as the number m of clock periods required to propagate signal from the phase detector output to its input:

$$JG_{pp} \propto m \cdot \Delta F_{bb}. \quad (5.4)$$

Both Equations (5.1) and (5.3) are used as first-order approximation to estimate the required filter values and charge-pump current. These values are fed into the behavioral models for transient simulation to ensure stability, and will be further optimized with transistor-level simulations.

5.2 Building Blocks of the Designed CDR System

5.2.1 Phase Detector Design for high speed CDR

The phase detector architecture used in this work is a fully-symmetrical half-rate Alexander-based phase detector from [7]. As shown in Figure 5.3, the phase detector is fully differential and utilizes clock phases of 0° , 90° , 180° and 270° to sample the data, producing D0, D90, D180 and D270 signals. When the CDR is in lock state, the quadrature clock edges (Q and QB) are aligned with the data transitions. Hence, the in-phase clock edges (I and IB) sample the data at the optimum point of the data eyes. Therefore, D0 and D180 are the recovered demultiplexed data. By using another multiplexer (MUX) controlled by clock I and IB, the full-speed data is obtained by sampling D0 and D180.

In order to maintain a symmetrical architecture and hence equal clock-to-q delays, four DFFs and XORs are used to generate two pairs of Up and Down signals (UP1/DN1 and UP2/DN2). The delay of the circuits can be compensated by the multiplexer clock signal. The phase detector logic is illustrated as Figure 5.4. When the clock is early (i.e., Q leads data transition), $UP1 = D0 \oplus D90 = 0$ and $DN1 = D90 \oplus D180 = 1$. When the clock is late, $UP1 = D0 \oplus D90 = 1$ and $DN1 = D90 \oplus D180 = 0$. When there is no data transitions, D0

Figure 5.3: Block diagram of half-rate binary phase detector used in CDR. A retimer is included here.

Figure 5.4: Logic operation of phase detector: (a) clock is early; (b) clock is late.

= D90 = D180, UP = DN = 0.

All the cells in the phase detector are built using common-mode logic (CML) circuit and all the signals are differential so as to improve on the speed and also to improve on PSRR and CMRR. Among all the blocks shown in the phase detector, the DFF is one of the most critical parts. The DFFs not only have to process the data sampling that is of high speed, but also to cope with the small data and clock input swing caused by heavy loading. In this DFF, resistive loads are used instead of PMOS transistors so as to reduce the capacitive loading on the output nodes. Tail current source transistors have been omitted to help widen the output voltage swing, which also simplify the circuit design and enhance the speed as well [40].

A series of optimization simulations were launched to find the transistor sizes and resistor values for optimum speed and power consumption. Since the biasing tail current transistor is removed in this circuit, the transistors are not working in the saturation region

Figure 5.5: DFF with 500 Ω resistive load used in the phase detector of 5.3.

for the entire cycle. Hence, the linear circuit analysis cannot be conveniently employed for analysis. However there are still some fundamental guidelines for designing this kind of CML buffer. First of all, the load resistor should be small in order to reduce the RC delay and increase the bandwidth [60]. Secondly, the output swing should be large enough to drive the following stage. It is known that the output node of the differential pair varies from V_{dd} to $V_{dd} - I_{ss}R$, where I_{ss} represents the tail current by assuming the current switching takes place, and R is the load resistor [60]. In order to obtain a large enough voltage swing, the tail current that can be provided must be also large enough after the load resistor is determined. The process of optimization is actually a process of tradeoff between speed and power. An optimum value of 500 Ω is eventually determined for use in this DFF which results in sufficiently small propagation delay as well as acceptable power consumption.

Out of the same consideration, CML circuits with the resistive loads are also used in the XOR and MUX gates of the phase detector. The resistor loads value used in these two gates is 400 Ω .

Figure 5.6: XOR gate with 400 Ω resistive load used in the phase detector of 5.3.

Figure 5.7: MUX gate with 400 Ω resistive load.

Figure 5.8: Charge pump with cascode current source and unity gain buffer.

This half-rate binary phase detector has less propagation delay which is vital for the jitter generation. Its three-state behavior also decreases the data dependent jitter for long periods of data without any transitions.

5.2.2 Charge pump circuit for CDR

The charge pump circuit is shown in Figure 5.8. Transistor P1 is controlled by the phase detector 'UPB' signal and transistor N1 is controlled by the 'DN' signal. They serve to provide the required net current, to source to or sink from the loop filter. A dummy branch

Table 5.1: Device sizes of charge pump

Device size	W/L ($\mu\text{m}/\mu\text{m}$)
N1-N2	2.7/0.18
N3-N4	1.4/0.18
N5-N8	30/1
N9	6/1
P1-P2	7/0.18
P3-P4	3.5/0.18
P5-P6	80/1

consisting of transistors P2 and N2, controlled by complementary phase detector pulses, are added to remedy the charge disturbance induced. Once the switches P1 and N1 are turned off, P2 and N2 are turned on to prevent the nodes n1 and n2 from being charged and discharged, respectively. Complementary switches P3, P4 and N3, N4 are used in this charge pump to provide complementary charges, so as to minimize the effect of charge injection and clock feed-through on the output node [61]. The sizes of these dummy switches are chosen to be half that of the primary switches, assuming that the channel charge will flow equally to the drain and source when the switches P1, P2 and N1, N2 are turned off. The transistor sizes of the charge pump are listed in Table 5.1.

By using wide-swing cascode current sources [63], the output impedance is increased for effective current injection. Although cascode current source devices consume some voltage headroom and consequently narrow the output dynamic range of the charge pump

because of the voltage drop across each device, it does not pose a problem to the voltage-tuning range since the frequency coverage of VCO is wide enough. The overdrive voltage of the wide-swing cascode current source transistors N5-N8, V_{ov} , is chosen to be around 0.15 V. The channel length of the current source transistors is chosen to be 1 μm in order to minimize the short channel effect. As a result, the dimension of the transistors N5-N9 can be calculated from a source current of 100 μA . The bias voltage for the PMOS cascode current source transistors comes directly from the biasing circuit, which also results in a same overdrive voltage. In addition, a rail-to-rail unity-gain buffer is used to maintain the same voltage potential for node n3 and the output node, minimizing the charge sharing between nodes n1 and n2.

As illustrated in 5.9, the unity-gain buffer utilizes a biasing current of 10 μA . The amplifier is a rail-to-rail input op amp with both PMOS and NMOS input transistors. The biasing current is chosen to be 10 μA , which determines proper sizing of biasing transistors N5-N7, P5-P6. The gain of the first stage A_{v1} alone is important as it determines the noise performance of the opamp. A_{v1} is chosen to be 3. Hence $(W/L)_{P1}$ is constrained to be less than $1/3 \cdot (W/L)_{N1}$ assuming $\mu_n/\mu_p = 3$. The factor B, which is the size ratio $B = (W/L)_{P3} / (W/L)_{P1}$, is increased to $B = 2$ to increase the slew rate as well as the GBW. The choice of B is a tradeoff between current consumption and GBW/slew rate. Design procedures presented in [62] is followed to fine tune the transistor size for enough phase margin. Table 5.2 lists the transistor size of the buffer.

The sourcing and sinking characteristics of the charge pump is simulated and depicted in Figure 5.10. From the figure, one can see that both the sourcing PMOS transistor and the

Figure 5.9: The unity-gain buffer used in the charge pump.

Table 5.2: Device sizes of the unity-gain buffer in the charge pump

Device size	W/L ($\mu\text{m}/\mu\text{m}$)
N1-N2	10/0.5
N3-N4	20/0.5
N5-N7	6/1
P1-P2	3/0.5
P3-P4	12/1
P5-P6	18/1
P7-P8	30/0.5

Figure 5.10: Charge pump net output current, source current and sink current at output node with respect to the output voltage.

sinking NMOS transistor perform very well in their saturation region, so that their currents match perfectly when the output voltage ranges from nearly 0.3 V to 1.4 V.

5.2.3 Multi-GHz Voltage-Controlled Oscillator

The voltage-controlled ring oscillator was chosen in this design because of its ability to provide a wide tuning range to encompass the process and temperature variations. The VCO used in this CDR is based on the multi-loop ring oscillator design discussed in Chapter 4. Because the quadrature clock signals are needed for half-rate binary CDR, four delay stages are used in the oscillator to generate the necessary multi-phase clocks. As evident

Figure 5.11: Topology of the quadrature output multi-loop voltage-controlled ring oscillator.

in Figure 5.11, care has been paid to the connection of the secondary loop to boost the operating speed instead of decreasing it [44].

The delay stage is depicted in Figure 5.12. N-type transistors N1/N2 and N5/N6 form the primary and secondary input, respectively. As discussed in previous chapters, transistors N3/N4 are used for maintaining oscillation and improving jitter performance. P-type transistors P1/P2 are used for frequency control, and so, this VCO has a negative frequency tuning gain.

Buffers are used to isolate the oscillator from the data transitions that are coupled through the phase detector. They also serve to isolate the heavy loading from the phase detector, frequency divider and output pads. All four stages in the ring oscillator are loaded

Figure 5.12: The schematic of the delay stage used in the VCO.

by almost identical buffers so as to ensure equal rise and fall times, and hence improving on the jitter performance.

The post-layout simulation result of the VCO operating frequency with all the buffer loading is described in Figure 5.13. High linearity of tuning range is observed from 0.1 V to nearly 1.2 V. The tuning range when the V_{ctrl} is tuned from 0.1 V to 1.5 V is 9.38 to 6.37 GHz. The average tuning gain in the linear range is 2.6 GHz/V.

Figure 5.13: The post layout tuning characteristics of the VCO.

5.2.4 Frequency-Locked Loop

The mere purpose of engaging the frequency-lock loop is to train the VCO frequency. Its performance is therefore not as critical as compared to that of the data-tracking loop. The PFD and the frequency divider used in the frequency-locked loop are described in this subsection.

As depicted in Figure 5.14, the precharge type logic is used to build the PFD. This is due to its much smaller propagation delay and the ability to attain higher operating frequency than those traditional PFDs using RS-type flip-flops. The smaller propagation delay and the higher operating frequency resulted from the critical reset path consists of only three gate delays for the PFDs using the precharge type flip-flops as opposed to the six gate delays required in conventional PFDs using RS flip-flops. Another advantage of this modified Precharge Type PFD (PTPFD) is that both the UP and DN output signals are

Figure 5.14: The modified precharge type PFD used in the frequency-lock loop.

simultaneously logically high for a minimum amount of time that is sufficiently long to eliminate the dead zone and reasonably short to minimize the perturbation on the loop filter during charge pump short circuit [64]. The PFD was optimized for the operating frequency in this CDR system and the transistor sizes are also provided in Figure 5.14.

Although consuming high power, the MOS Current Mode Logic (MCML) circuit [65], [66], is commonly used to achieve a high operating frequency [67]. The CML circuit was therefore chosen in this work to implement a frequency divider that can operate beyond 5 GHz frequency. The divide-by-64 divider was constructed by cascading six divide-by-2 CML stages. The first stage is most critical because it operates in the maximum frequency. The schematic of the divide-by-2 stage is presented in Figure 5.15. To increase the maximum toggle frequency, the current source is omitted [68]. The sizes of the transistors are listed as follows: PMOS load transistor 15/0.18, clock NMOS transistors 25/0.18 and the rest NMOS transistors 15/0.18, where all are in μm . The RFCMOS model provided by Chartered was used for design and simulation. A nominal output swing of 0.7 V was chosen first for transistor sizing. Since the sizing of MCML latch is not straightforward, simulations based on some rough estimation were carried out for sizing the MCML latch. The clock NMOS transistor in the first divide-by-2 stage was chosen to be larger than the rest to provide a large current for high frequency operation. The rest of the NMOS transistors also need to be sized to ensure enough gain [69]. The post-layout simulation result of the divider running from 8-GHz clock of VCO is shown in Figure 5.16.

Figure 5.15: The schematic of the divide-by-two divider stage.

Figure 5.16: Post-layout simulation result of the divide-by-64 divider that is running at 8-GHz input clock from VCO.

Figure 5.17: The block diagram of the proposed analog lock detector.

5.2.5 Analog Lock Detector

The lock detector monitors the frequency difference between the divided VCO clock and the reference clock, and de-asserts the lock-detection (LD) signal when the VCO is operating within a particular amount of desired frequency (usually 500 to 2000 ppm). This enables the phase-locking loop, which pulls the VCO frequency in the remaining amount and also acquires phase lock. Once locked, if the input frequency error exceeds the amount, the LD signal will be re-asserted, and the control will then return to the frequency loop, to reacquire and maintain a stable clock signal at the output.

There are mainly two types of lock detectors: analog type [78] and digital type. The analog lock detector used in [78] utilizes an exclusive-NOR gate to detect the system lock, but the circuit is only applicable to CDR systems with linear PD. Different from conventional digital lock detector, a new analog lock detector is designed and described in detail in this subsection. The lock detector is designed based on the concept presented in [70]. The block diagram of the analog lock detector is given in Figure 5.17. Detection of a locked condition is accomplished in the lock detector through an XOR gate in the first step. The

XOR gate generates pulses that represent the phase difference between the divided VCO clock and the reference clock. When the loop is frequency locked, the output of the XOR gate, 'XOR', will be at logic low and the voltage is then fixed at about 0.8 V through properly chosen load resistor and tail current in the XOR gate. Therefore, the output voltage of the lock detector capacitor C_{LD} , V_C , is discharged to 0.8 V through the resistors R_{LD1} and R_{LD2} . When the divided VCO clock deviates from the reference clock by a certain amount, the pulses appearing on the XOR gate output will charge the capacitor through R_{LD2} only since the diode across R_{LD1} is forward biased, which results in a higher voltage level across the LD capacitor. By choosing a reference voltage level (V_{ref}) that is slightly higher than 0.8 V at the negative input of the comparator, the function of the lock detection can be accomplished. When the phase difference is within the toleration, which means $V_C < V_{ref}$, the comparator outputs a logic 0. The logic level is passed through two inverters to reach a larger driving capability.

The time constant in the path that discharges the lock-detector capacitor is given by $T_{discharge} = (R_{LD1} + R_{LD2}) \times C_{LD}$, while the charging of the lock-detector capacitor may be defined as $T_{charge} = R_{LD2} \times C_{LD}$. The resistors are chosen such that the charging (VCO loss of lock) is much faster than discharging (VCO in lock), i.e., $R_{LD1} \gg R_{LD2}$. This implies that the lock detector can rapidly reacts to the VCO loss of lock to pull the frequency-acquisition loop back to re-acquire the desired VCO frequency. In our design, in order to improve the accuracy, R_{LD2} is set to 150 Ω and R_{LD1} is chosen as $R_{LD1} = 40R_{LD2} = 6 \text{ K}\Omega$. Hence, the discharging time constant is about 40 times that of the charging phase. A typical range of the lock-detector capacitor value for a frequency of 100 MHz is about 1

Figure 5.18: The schematic of the analog lock detector.

pF [70].

The detailed circuit is presented in Figure 5.18. The load resistor values and the tail source current in the XOR gate (Figure 5.18(a)) are chosen to be $10\text{ K}\Omega$ and $100\text{ }\mu\text{A}$, respectively. This results in a voltage drop of 1 V across the load resistor which means the lower end of the XOR output voltage is of 0.8 V for a power supply of 1.8 V . The core part of Figure 5.18(b) is a comparator with hysteresis. The cross-coupled PMOS load transistors are sized slightly larger than the diode-connected PMOS load to obtain a small hysteresis. The differential output is converted to single-ended following by two normal inverter buffers. The biasing current for the comparator is $10\text{ }\mu\text{A}$.

After launching a series of simulations, the reference voltage is set to 0.82 V to present a detection accuracy of 2000 ppm (0.2%) for an operating frequency of 156 MHz . Figure 5.19 shows the output waveform of the post-layout simulation of the lock detector with different input phase offsets. The 'delay' in the figure represents the phase difference between the reference clock and the divider output whose periods are both of 6.4 ns . From the figure, one can see that the lock detector outputs a logic 1 when the phase difference is smaller than 12 ps , but changes to 0 when the 'delay' is equal to 14 ps . Therefore, an accuracy of 1875 ppm ($12\text{ ps}/6.4\text{ ns} = 0.1875\%$) is achieved, and this accuracy is high enough to narrow the frequency gap between the VCO and the expected frequency down to a value that is much smaller than the pull-in range of the data-tracking loop [71].

Figure 5.19: Lock detector output waveform of the post-layout simulation running with different input phase offsets.

Figure 5.20: The output buffer.

5.2.6 Clock and Data Output Drivers

The high-speed clock and data output drivers are CML differential logic drivers as shown in Figure 5.20. The common mode voltage of the input to the first buffer stage is fixed at around 1.0 V by using an RC network to minimize the dc offset impact on the output buffers' gain. A large resistor value is chosen for R so as to reduce the thermal noise. The final stage of the multistage buffer uses a $50\text{-}\Omega$ on-chip resistive termination resistor to meet signal integrity and the return loss specifications.

5.3 Behavioral Modeling of CDR Using VHDL-AMS

A behavioral modeling approach allowing systematic design of the PLL can give the designer a grasp of the fundamentals by using coarse models at the early stage of the design. This provides insight to the lower order effects by gradually increasing the level of detail as the design develops. Accurate design specifications for the actual blocks can be obtained by transistor-level simulators such as Spectre and Eldo, and the corresponding results can

be back-annotated onto the behavioral models for further verification. The development process for the back-annotation may not necessarily be a straightforward top-down approach. This is because the lower level details can impact the overall performance and necessitate a review of some of the prior design assumptions or a further refinement in the models. Several iterations up and down the different levels are inevitable until a satisfactory result is obtained.

On the other hand, traditional transistor-level simulators take a long time to compute the dynamic response of the PLL-based CDR system mainly for the two following reasons. First, the high speed operation of the phase detector and the high frequency output of VCO (in multi-GHz range) imposes an even higher simulation sample frequency (often in a few tens GHz or even hundreds of GHz range). Second, the overall PLL dynamics have a bandwidth that is typically three to four orders of magnitude lower in frequency (often a few MHz bandwidth). For example, it usually takes 4 days to a week to simulate a PLL-based 10 Gb/s CDR before it can lock for a traditional simulator (usually less than 10 μ s transient running time). This makes it impractical to iterate a lot of simulations to verify the system design and optimization. All these necessitate a behavioral modeling and simulation at different stages of the system design.

5.3.1 What is VHDL-AMS

The VHDL-AMS, which was approved as a superset of VHDL in March 1999, is a mixed-signal HDL standard that supports designers in the construction of complex analog and mixed-signal models. This language represents a major innovation for systems and design

engineers involved with analog and mixed-signal electronics. With its unique features such as Differential Algebraic Equations (DAEs), discontinuity handling and processing, and the ability to communicate between discrete-event and continuous-time systems, VHDL-AMS allows a very rich model expressiveness for describing analog, digital and mixed signal behavior of an electronic circuit [72]-[77]. It provides an industry-standard platform for the design of mixed-signal systems-on-a chip development of component models and the integration of mixed-signal electronics into large-scale systems.

5.3.2 VHDL-AMS Modeling of CDR

A VHDL-AMS models library has been developed to model the PLL-based CDR system. There are two description modes for the input and/or output signals of each PLL blocks, a bit digital signal or an analog electrical terminal. During simulation, the digital signals call the digital event-driven kernel while the analog terminals call the analog continuous-time kernel. The advantage of event-driven simulation is the reduction of CPU time, but the settling time of any transition can only be modeled with analog electrical terminal. In order to best reflect the real circuit's response and also to save the simulation time, all ports in the developed models are defined as digital ports whenever possible. As an example, the output of the charge pump, loop filter and VCO are all defined as electrical terminals, while the others are defined as digital signals.

The phase detector is modeled in the exact same way as it is designed in the gate level. D-flipflop, XOR and MUX are also modeled, to implement the structural model of the phase detector. As for lock detector modeling, a common implementation of the digital

lock detector is to use two gray-code or binary counters to detect the locked and unlocked state of the PLL, by comparing the frequency between the reference frequency and divided frequency. This implementation allows accurate tolerance between the two frequencies and is easier to be implemented in HDL language as compared to analog implementation. Therefore, in this model library, we chose to build the digital lock detector by utilizing two counters.

Although the pulse-swallow type divider is commonly used in PLL-based frequency synthesizers, a simple divide-by-16 or divide-by-64 divider is more often used in CDRs [10]. Since a divide-by-64 divider is employed in our CDR system, a simple model is built in addition to the pulse-swallow integer-N frequency divider to fulfill this function. The divider is implemented using a 6-bit binary down counter.

The transistor-level simulation result of the VCO frequency is back annotated to the VHDL-AMS model. Considering the nonlinear tuning characteristics of the real VCO, the piece-wise linear (PWL) method is used to construct the VCO tuning curve in the behavioral model.

Table 5.3 lists the block models, with a brief description of each block. Typical values of the loop parameters are shown in Table 5.4. The response of the loop to a large input phase step is given in Figure 5.21. A 17.8 Gb/s PRBS data sequence is pumped into the loop. The input reference clock frequency is 139.5 MHz. Because of the relatively small frequency loop bandwidth as compared to the large comparison frequency, cycle-slipping can be seen when the frequency loop is trying to pull the VCO to the expected frequency. The loop is in lock at 16.4 μ s, after which the data-tracking loop takes over and generates

Table 5.3: Models library for CDR modeling.

Model Name	Description Level	Comments
Phase Detector	structural	half-rate, binary
PFD	behavioral	common tri-state
Charge Pump	behavioral	
Lock Detector	structural	digital
Loop Filter	structural	2nd-order
VCO	behavioral	PWL gain setting
Integer-N Divider	structural	pulse-swallow type
Divide-by-64	behavioral	
PRBS Generator	behavioral	7-bit
Jitter Module	behavioral	for noise modeling

Table 5.4: CDR loop parameters for behavioral modeling.

I_{CP}	100 μ A
R1	30 Ω
C1	1 nF (off-chip)
C2	63 pF (on-chip)
K_{VCO}	2.6 GHz/V ($0 \leq V_{ctrl} \leq 1.1$) 0.68 GHz/V ($1.1 \leq V_{ctrl} \leq 1.5$)

Figure 5.21: Transient response of the CDR loop to a 17.8 Gb/s PRBS data sequence.

a 2 mV ripple on the control line. From the eye diagram of the recovered clock, the ripple causes a jitter (peak-to-peak) of 2 ps, as shown in Figure 5.22.

5.4 Layout Issues

Extensive isolation and decoupling between the analog and digital parts in a high speed mixed analog/digital circuit are necessary in the layout of the design. Layout techniques were implemented in this work to reduce cross-talk and provide power supply and ground isolation. Separate power supply and ground pads are used for analog and digital blocks. To reduce substrate noise propagation from the digital to the analog subcircuits, guard-rings are used around each analog blocks. Within every analog subcircuit, that is the charge

Figure 5.22: Eye diagram of the recovered clock.

pump, VCO and biasing circuit, each transistor is also equipped with a guard-ring. An N-well region connected to analog power supply is placed underneath each n-poly resistor used in the design to reduce the amount of substrate noise injection into these devices. Transistors in analog block are drawn in interdigitized configuration to improve the matching. To prevent the signals from coupling to each other, all the critical signals are shielded at the cross points with metal layers, which is connected to ground.

The final layout of the CDR is shown in Figure 5.23. Note that a $30\ \Omega$ poly resistor and 63 pF Metal-insulator-Metal (MiM) capacitor have also been integrated on chip. All the I/O pads, except for those connected to high speed I/O (data input, recovered data out and clock out), are connected to ESD protection circuits. The CDR core circuit occupies an die area of $0.7\text{mm} \times 0.72\text{mm}$, while the whole chip area including the pad frame is $1.2\text{mm} \times 1.2\text{mm}$.

Figure 5.23: Layout of the CDR circuit.

Figure 5.24: Post-layout transient response of the CDR circuit.

5.5 Circuit Simulation Results

Post-layout simulation is carried out to verify the functions of the CDR system. A 16 Gb/s data with '01010101' pattern is pumped into the phase detector. Likewise, a reference clock of 125 MHz is injected into the PFD. An initial value of the control voltage V_{ctrl} is selected for fast simulation convergence. The transient simulation result is as shown in Figure 5.24. As evident in the figure, the data-tracking loop is switched in at $t = 2.7\mu\text{s}$ after the frequency-locked loop attained lock. A 2 mV ripple is observed on the control voltage and this is because of the inherent bang-bang characteristic of the binary phase detector. A smaller ripple can be assured if a larger off-chip C_1 is used during the measurement. 1nF off-chip capacitor is used for simulation since the larger the capacitor is, the longer time the simulation takes.

The jitter transfer characteristics of the CDR circuit are predicted using Eq.(5.1) through Eq.(5.3). Figure 5.25 plots the approximated jitter transfers for different input jitter amplitudes. The calculated jitter transfer bandwidths for input jitter amplitudes of 0.25 UI, 0.5

Figure 5.25: Predicted jitter transfer of CDR circuit for different input jitter amplitude.

UI and 1 UI are 7.8 MHz, 3.6 MHz and 1.8 MHz, respectively.

Running at 16 Gb/s input data rate, the entire chip consumes a power of 600 mW at a power supply of 1.8 V, where most of which is dissipated by the VCO (92 mW), PD (98 mW), divider (95 mW) and buffers (310 mW). The post-layout simulations prove that the chip is able to run at an input bit rate of 13 to 18 Gb/s.

Chapter 6

Conclusion

6.1 Contribution

This thesis describes a wide range of techniques employed in high speed PLL. The investigation covers mainly on the high frequency CMOS ring oscillator and its application in CDR system. Existing techniques to improve the voltage-controlled ring oscillator's operating speed, including the interpolation and multi-loop methods, are discussed. Two noise models for oscillator noise analysis, namely the linear-time-invariant (LTI)-based Leeson model and the Hajimiri model, are briefly reviewed to provide an insight into the oscillator's phase noise PSD shape and noise sources. Two ring oscillators have been designed and fabricated for high speed application. Both oscillators are able to cover a frequency range of 7-GHz. A CDR circuit which employs the ring oscillator design has also been developed. The post-layout simulation indicated that the CDR can operate up to a data rate of 16 Gb/s.

The main contributions of this thesis can be summarized as follows.

1. A novel delay cell of a CMOS ring oscillator for operation in the 7-GHz range is demonstrated. The experimental results proved that the VCO is able to operate at high frequencies with a relatively constant tuning gain across the entire tuning range. Due to the introduction of the push-pull inverter as the secondary input as well as the cross-coupled transistor pair, both the rising and the falling times at the output node are significantly reduced. This allows the realization of a very much improved operating speed. Fabricated using 0.18- μm CMOS technology, the oscillator is tunable from 6.24 to 7 GHz. The measured phase noise is about -107.7 dBc/Hz at 10 MHz offset from 6.25 GHz center frequency. The oscillator only occupies a die area of 0.189 mm^2 .

2. A new VCO that is equipped with both the coarse- and fine-tuning is presented. Different from the conventional design that achieves fine-tuning by splitting the tail current source of the delay cell, which consequently deteriorates the phase noise performance of the oscillator due to the noise upconversion from tail current transistors, the proposed approach implements the function by adjusting current flowing through the positive feedback cross-coupled NMOS pair. This pair with optimized dimensions for minimal $1/f$ noise and thermal noise allows the upconverted noise of the fine-tuning devices to have minimum impact on the VCO's overall noise performance. The frequency and phase noise performance of the proposed VCO had been analyzed in detail.

Experimental results proved that the capability of the coarse/fine-tuning ring oscillator. Implemented in 0.13- μm logic CMOS process, the oscillator is measured to cover a frequency range of 7.3 to 7.9 GHz and exhibits a phase noise of -103.4 dBc/Hz at 1 MHz

from the center frequency of 7.64 GHz. The average fine tuning gain of the oscillator is only 115 MHz/V.

3. The design of a high-speed PLL-based CDR with half-rate bang-bang phase detector is presented last in this thesis. The behavioral modeling using the VHDL-AMS has been engaged to speed up the design and verification process of the system. Different blocks, including PD, VCO and lock detector, have been designed to fulfill the stringent requirements of 10+ Gb/s input bit rate. Transient simulation was carried out to verify the function of the CDR. Post-layout simulation shows that the chip can work at an input bit rate of 13 to 18 Gb/s, with a power dissipation of 600 mW for 16 Gb/s input data rate. The jitter transfer bandwidth is approximated to be 7.8 MHz for an input jitter amplitude of 0.25 UI.

6.2 Future Work

The chip will be sent for fabrication to physically verify the proper functioning of the system. PCB shall be designed to mount the fabricated CDR circuit for measurement. Jitter performance measurement, i.e., the jitter transfer and the jitter tolerance, shall be carried out as one of the most important future work.

Another future research topic may be the utilization of the coarse/fine-tuning oscillator proposed in Chapter 4 in CDR circuit, to improve the jitter performance of the system. Since the VCO gain required is quite large in order to achieve a given tuning range, the ripple on the control voltage due to the phase detector activity creates large jitter at the output. This conflict between the requirements of a wide tuning range and a low VCO

Figure 6.1: CDR using coarse/fine-tuning VCO to reduce impact of ripple by binary PD on jitter performance.

sensitivity can be resolved using the coarse/fine-tuning approach engaged previously in the VCO. As illustrated in Figure 6.1, the fine tuning of the VCO is involved in the data-tracking loop while the coarse tuning is controlled by the frequency-training loop. Since the frequency loop remains relatively quiet after phase lock, the high sensitivity of the coarse control does not lead to high jitter. A zero is not necessary in the frequency loop because the VCO is merely a gain element in the frequency domain. After the CDR is in lock, the frequency loop has ignorable effect on the operation of the data loop because of the tri-state characteristics of PFD. The coarse/fine-tuning ring oscillator presented in Chapter 4 can therefore be utilized in this loop architecture. This configuration avoids the use of the lock detector to identify the frequency difference between the VCO and the expected

frequency, and the MUX that is used to choose the pulses from the phase detector and the PFD, which significantly simplifies the implementation of the CDR architecture.

While recent advances in IC technology make fabrication processes very suitable for digital designs, more and more research efforts have been focused on the digital and all-digital PLL designs. The advantages of all-digital PLL include small-area and low-voltage as well as its scalability and easy redesign with process changes or shrinks. Recently, several digital and all-digital phase-locked loops (PLLs) for different applications and analysis methodology as well as design procedure for ADPLL have been reported [79]-[81]. Some digital CDR designs can also be found in literature [82]-[83]. Despite all these digital CDR designs, there is no an existing systematic analysis and corresponding design procedure for a binary digital CDR system. Hence our research effort could be put on this potential topic.

Publications

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