Synthesis, characterisation and device application of silicon nanocrystals

Ng, Chi Yung

2007

Ng, C. Y. (2007). Synthesis, characterisation and device application of silicon nanocrystals.
Doctoral thesis, Nanyang Technological University, Singapore.

<https://hdl.handle.net/10356/39044>

<https://doi.org/10.32657/10356/39044>

9530236

Synthesis, Characterization and Device Application of Silicon Nanocrystals

Ng Chi Yung

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfilment of the requirement for the degree of
Doctor of Philosophy

2007

To my parents

Acknowledgements

First and foremost, I would like to express my gratitude to my thesis advisor, A/Prof Chen Tu Pei. The successful completion of this thesis was made possible through his generous support. He not only dedicates his time to guide me throughout the entire course of research but also supported my application for other Ph.D. scholarships during my study. Without this invaluable contribution of time and energy from him, I would not be able to reach the fruition. I would also like to convey my appreciation to Dr. Alastair D. Trigg from the Institute of Microelectronics, Singapore for his suggestions and supports especially with equipment and material characterizations.

Special thanks to Temasek Holdings for granting me the Singapore Millennium Foundation (SMF) Ph.D. Scholarship. It helped me to continue my Ph.D. research for four years. It is indeed a boost to me to have their recognition for contributions and achievements in research. I would also like to thank IEEE Electron Device Society (EDS) for awarding me the IEEE EDS Graduate Student Fellowship for the year 2006.

I would like to thank my fellow colleagues and technicians who have created fond memories at my laboratory in the School of Electrical and Electronic Engineering, NTU. The insight, entertainment and friendship that they have brought to me have made my life at NTU an unforgettable one.

Finally, I would like to express my deepest appreciation to my family especially my parents for their care, love, understanding, encouragement and support throughout these years. Without their patience and continuous support, all my achievements will not be possible.

Summary

It is the intent of this work to investigate the physics and device applications of silicon nanocrystals embedded in dielectric film. Silicon nanocrystals embedded in SiO_2 film have been synthesized using ion-implantation. Metal-oxide-semiconductor field-effect-transistors (MOSFET) embedded with silicon nanocrystal as charge storage node has also been fabricated. The electrical characteristics of the structure are obtained using the conventional current-voltage (I-V) and capacitance-voltage (C-V) techniques. To identify the size of the silicon nanocrystal, X-ray Diffraction (XRD) and cross-section Transmission Electron Microscopy (TEM) measurements have been conducted.

Reviews of other techniques to synthesize the silicon nanocrystal have been summarized, including chemical vapor deposition, sputtering, pulse laser deposition and etc. Besides these, the size distribution of the silicon nanocrystal produced by ion-implantation (as shown in this work) is compared with other techniques as obtained from the literature.

The charge decay and charge transport in silicon nanocrystal has been studied by Electrostatic Force Microscopy (EFM) technique. This technique allows sub-micron visualization of charge transport and charge decay characteristic in nanocrystal. It is found that charge decay in the silicon nanocrystal is influenced by the nanocrystal distribution. In addition, the influence of neighboring trapped charge on the charge decay is significant. A charge decay model is provided to understand the charge decay in the nanocrystals.

An approach to study the static dielectric constant of silicon nanocrystal based on Maxwell-Garnett Effective Medium Approximation (EMA) and C-V

measurements has been developed. The dielectric constant of nanosize silicon is significantly suppressed compared to that of bulk silicon. The result is in good agreement with other theoretical calculation. A detailed picture on the influence of silicon nanocrystal implantation energy and implantation dosage on the total MOS capacitance is presented.

The effect of thermal annealing on the stability of flatband voltage of MOS capacitor embedded with silicon nanocrystal has been studied. Different annealing temperature, annealing time and temperature ramping rate have a serious implication on the flatband voltage shift of the device. Calculation reveals that the number of remaining Si ions trapped inside the SiO_2 is only about $\sim 0.1\%$. However, it can affect the flatband voltage stability.

The electrical properties of single layer silicon nanocrystal embedded in SiO_2 film and silicon nanocrystal distributed throughout the SiO_2 film have been investigated. Single electron trapping in the nanocrystal is observed. Appropriate models are provided to explain the difference between the two distributions.

Furthermore, silicon nanocrystal-based nonvolatile memory devices have been fabricated based on conventional $2\text{-}\mu\text{m}$ complementary MOS technology. The electrical characteristics of the devices have been characterized. The influence of tunnel oxide thicknesses on the memory performances is evaluated. The impact of different programming mechanism on the memory performance and the retention characteristics has also being investigated.

Two inventions on the silicon nanocrystal-based volatile memory and nonvolatile memory are being disclosed. These two inventions have the potential as an emerging memory device. Discussion is provided on the observed phenomena.

Table of Content

Acknowledgementsiii

Summaryiv

List of Figurexi

List of Table.....xxi

Chapter 1 1

Introduction..... 1

1.1 Brief introduction to nanoelectronics and nanocrystal..... 1

1.2 Future Semiconductor Memory Technology and Market Trends6

1.3 Silicon Nanocrystal: an overview 8

1.4 Motivation 8

1.5 Objective 10

1.6 Scope of research and approach 10

1.7 Major contributions in this thesis 11

1.8 Thesis outline 13

Chapter 2 15

Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview..... 15

2.1 Introduction 15

2.2 Ion implantation 16

2.3 Other fabrication techniques 18

2.3.1 Chemical Vapor Deposition 18

2.3.2 Aerosol synthesis 20

2.3.3	Sputtering.....	21
2.3.4	Pulse Laser Deposition	21
2.3.5	Mechanical ball milling and spin-coating.....	22
2.3.6	Comparison on the nanocrystal fabrication technique.....	22
2.4	Fabrication of SiO ₂ thin film with silicon nanocrystal.....	24
2.5	Non-electrical characterization of nanocrystal.....	27
2.5.1	Transmission Electron Microscopy (TEM).....	27
2.5.2	X-Ray Diffraction (XRD).....	28
2.5.3	Secondary Ion Mass Spectroscopy (SIMS)	29
2.5.4	Stopping Range of Ions in Matter (SRIM) Simulation.....	30
2.5.5	Scanning Electron Microscopy (SEM).....	31
2.5.6	Results.....	31
2.6	Electrical characterization of nanocrystal	37
2.6.1	Capacitance-voltage and current-voltage characteristics.....	37
2.7	Physical Properties	41
2.7.1	Coulomb blockade and Single-electron charging effect.....	41
2.7.2	Dielectric Constant of Silicon Nanocrystal	44
2.8	Applications of nanocrystals embedded in dielectric films.....	46
2.8.1	Nano-memory devices	46
2.8.2	Single-electron devices	47
Chapter 3		52
Charge Transport and Charge Decay.....		52
3.1	Overview	52
3.2	Atomic Force Microscopy (AFM)	53
3.2.1	Electrostatic Force Microscopy (EFM)	54

3.3	Probes Selection	57
3.4	EFM Characterization of nc-Si	58
3.5	Voltage dependence of the charging effect	62
3.6	Visualizing charge transport in silicon nanocrystal	65
3.7	Influence of neighboring charges	67
3.8	Effect of nanocrystal's depth distributions on charge injection and charge decay	71
Chapter 4		80
Static Dielectric Constant of Silicon Nanocrystal		80
4.1	Motivation	80
4.2	Introduction	81
4.3	Distribution of nanocrystal inside the SiO ₂	83
4.4	Effective Medium Approximation (EMA) method	85
4.5	Influence of implantation energy and dosage	89
4.6	Comparison with theoretical calculation	92
4.7	Effective dielectric constant	95
4.8	Influence of SiO ₂ thickness	97
Chapter 5		99
Electrical Characteristics of Nanocrystal Embedded in Dielectric Film		99
5.1	Introduction	100
5.2	Single layer of nanocrystal embedded in SiO ₂ thin film	101
5.2.1	Annealing effect on the flatband voltage shift	101
5.2.1.1	Conventional furnace annealing	102
5.2.1.2	Rapid Thermal Annealing (RTA)	104

5.2.2	Remaining ions due to annealing effect.....	106
5.2.3	Reduction of flatband voltage shift by electron injection.....	109
5.2.4	Charging effect in single-layer nc-Si.....	111
5.2.5	Current transport in single-layer nc-Si	117
5.2.6	Retention characteristics of single-layer nc-Si	119
5.3	Nanocrystal distributed throughout the SiO ₂ thin film.....	120
5.3.1	Fabrication	120
5.3.2	Capacitance-voltage characteristics.....	122
5.3.3	Current-voltage characteristics	128
Chapter 6		133
Non-Volatile Memory Devices Based On Silicon Nanocrystal		133
6.1	Introduction	134
6.2	Basic principles	136
6.3	Programming and erasing options.....	139
6.3.1	Fowler-Nordheim (FN) programming	139
6.3.2	Channel-hot-electron (CHE) programming	141
6.3.3	Fowler-Nordheim (FN) Erasing	142
6.4	Comparison of various semiconductor memory technologies	144
6.5	Advantages of nanocrystal-based memory devices.....	146
6.6	Nanocrystal-based non-volatile memory devices	150
6.7	Influence of tunnel oxide thicknesses	155
6.8	Impact of programming mechanism.....	160
Chapter 7		172
Alternative Memory Structures using nc-Si.....		172

7.1	Introduction	172
7.2	Introduction to conventional 1T1C-DRAM	173
7.3	Invention of a silicon nanocrystal-based 1T-DRAM	176
7.4	Invention of a two terminal memory devices	185
Chapter 8		192
Conclusion and Recommendation		192
8.1	Conclusion.....	192
8.1.1	Charge transport and charge decay	192
8.1.2	Dielectric constant of nc-Si	193
8.1.3	Single-layer nc-Si embedded in SiO ₂ thin film	194
8.1.4	Nanocrystal embedded throughout the SiO ₂ thin film.....	195
8.1.5	Flash memory based on silicon nanocrystal	196
8.1.6	Silicon nanocrystal-based 1T-DRAM	197
8.1.7	Two-terminal memory devices based on silicon nanocrystal	197
8.2	Recommendation.....	199
8.2.1	Fabrication of silicon nanocrystal.....	199
8.2.2	Single electron tunneling	199
8.2.3	Flash memory devices based on silicon nanocrystal in high-K dielectric film	200
8.2.4	Modeling of silicon nanocrystal memory device.....	200
List of Publications		201
Bibliography		207
Appendix A.....		236

List of Figure

Fig. 1.1	Size of biological and semiconductor objects.	3
Fig. 1.2	Transistor size trend for different technology node (Re-plotted using data from Refs. [3] and [12]).	3
Fig. 1.3	Taxonomy of solid-state nanoelectronic devices (Re-plotted using data from Ref. [13]).	5
Fig. 1.4	Future technology and demand trend for memory devices.	7
Fig. 1.5	Potential market revenues for all products based on semiconductor devices (Re-plotted using data from Ref. [24]).	7
Fig. 2.1	Illustration of Si^+ implantation process followed by high temperature annealing to form nc-Si.	18
Fig. 2.2	The density of nanocrystal can be controlled by varying the deposition time (Extracted from Ref. [65]).	19
Fig. 2.3	AFM image of nc-Si produced by CVD technique. The scan size is $1\text{ }\mu\text{m} \times 1\text{ }\mu\text{m}$.	20
Fig. 2.4	Schematic illustration of three most important factors during the fabrication of nc-Si for device applications [56].	23
Fig. 2.5	Schematic illustration of single-layer of nc-Si embedded in SiO_2 thin film.	25
Fig. 2.6	Schematic illustration of nc-Si distributed throughout the entire SiO_2 thin film with peak nc-Si concentrations close to the SiO_2 surface.	25

Fig. 2.7	Schematic illustration of wide distributions of nc-Si embedded in SiO ₂ thin film.	26
Fig. 2.8	Effect of Si ⁺ implantation into SiO ₂ at energies increasing from 1 to 5 keV (Extracted from Ref. [55]).	28
Fig. 2.9	Plan-view TEM measurements of nc-Si (Extracted from Ref. [72]).	28
Fig. 2.10	Cross-section high resolution TEM measurements on the sample with nc-Si.	32
Fig. 2.11	XRD profile of the SiO ₂ embedded with nc-Si.	33
Fig. 2.12	Si ⁺ SIMS profile.	33
Fig. 2.13	Comparison of SIMS measurements and SRIM simulation of Si ⁺ implanted into SiO ₂ thin film at energy of 1 keV.	35
Fig. 2.14	Top view SEM image shows the presence of silicon nanocrystal / nanoparticles at the SiO ₂ surface.	36
Fig. 2.15	Hysteresis observed during reversible C-V measurement (a). Pure SiO ₂ does not exhibit hysteresis effect (b).	38
Fig. 2.16	Reversible drain current (I _d) measurements for both sample without nc-Si (a) and with nc-si (b).	40
Fig. 2.17	Illustration of the total electron energy in the quantum dot / nanocrystal for various gate voltages applied.	42
Fig. 2.18	Energy band diagram of a nanocrystal containing (a) N electrons with a CB gap, and (b) N+1 electron without a CB gap.	43
Fig. 2.19	Plot of size-dependent static dielectric constant vs the radius of the silicon sphere based on Lannoo and Wang and Zunger models.	45

Fig. 2.20	Silicon nanocrystals as memory devices (Extracted from Ref. [46]).	46
Fig. 2.21	(a) Schematic diagram of Si single-electron device with self-aligned floating gate, and (b) the cross-section along a'-a line (Extracted from Ref. [109]).	48
Fig. 2.22	Drain current vs gate voltage for (a) and (b) device with floating dot and (c) device without floating dot (Extracted from Ref. [109]).	50
Fig. 2.23	Step-like threshold voltage shift of a single-electron device (Re-plotted using data from Ref. [123]).	51
Fig. 3.1	Comparison of the attractive and repulsive forces.	55
Fig. 3.2	Frequency Modulation (FM) mode for the EFM study (Extracted from Ref. [133]).	56
Fig. 3.3	Lift mode operation during the EFM measurements.	57
Fig. 3.4	Setup for the EFM experiment. Half of the total charges in nc-Si, Q is reflected as image charges ($-\frac{1}{2} Q'$) at the EFM tip.	60
Fig. 3.5	EFM images. (a) uncharged nc-Si sample; (b) nc-Si sample charged at +4 V; (c) nc-Si sample charged at -4 V; and (d) SiO ₂ sample (i.e., without nc-Si) charged at +4 V.	63
Fig. 3.6	3D EFM images of initially deposited charge as a function of voltage bias.	64
Fig. 3.7	EFM images of decay of charge trapped in nc-Si.	66
Fig. 3.8	Increase of the area of the charge cloud due to charge diffusion.	66
Fig. 3.9	(a) Blockage of charge diffusion by neighboring charges with the same charge sign; (b) acceleration of charge diffusion by	

	neighboring charges with the opposite sign; and (c) decay time as a function of both the number and charge sign of the neighboring charged spots. “+” represents positive charge while “-” represents negative charge.	70
Fig. 3.10	a) nc-Si distributions in SiO ₂ film; and (b) schematic illustration of charge injection from the EFM tip to the nc-Si and charge diffusion through the nc-Si.	72
Fig. 3.11	3D EFM images taken at various time after charge injection for sample A and sample X.	74
Fig. 3.12	(a) Determination of the size of charge cloud from the pseudo-voigt fittings to the experimental data of the resonance-frequency shift versus position; and (b) Size of charge cloud as a function of decay time. The charge injection is carried out at -4 V	75
Fig. 3.13	Charge decay characteristics for sample X and sample A. The initial charge (Q_0) and the characteristic decay time (τ) can be obtained from the fitting based on $Q(t)=Q_0\exp(-t/\tau)$.	77
Fig. 3.14	Influence of neighboring charges on the characteristic decay time.	79
Fig. 4.1	Comparison of C-V characteristics between the MOS structures with and without the nc-Si embedded in the oxide. The both structures have identical oxide thickness.	81
Fig. 4.2	nc-Si distribution in a 30 nm gate oxide obtained from SRIM simulation. (a) Partial distribution under the ion implantation energy of 2 keV; and (b) full distribution under the implantation energy of 8 keV.	84

- Fig. 4.3 Sub-layer model used in the studies for partial distribution (a) and full distribution (b) of nc-Si in the gate oxide. 86
- Fig. 4.4 Calculated MOS capacitance as a function of ϵ_{nc-Si} . The intercept between the calculated and the measured capacitance yields the dielectric constant of the nc-Si embedded in the SiO₂. 89
- Fig. 4.5 Influence of Si⁺ implantation energy on the MOS capacitance. The gate oxide thickness is 30 nm, and the implantation dosage is $1 \times 10^{16} \text{ cm}^{-2}$. 90
- Fig. 4.6 Influence of Si⁺ dosage on the MOS capacitance. The gate oxide thickness is 30 nm, and the implantation energy is 8 keV. 91
- Fig. 4.7 TEM image of nc-Si embedded in a 30 nm gate oxide. (a) Partial distribution under the implantation energy of 2keV; and (b) full distribution under the implantation energy of 10 keV. 93
- Fig. 4.8 Depth distribution of the effective dielectric constant of the gate oxide. (a) Partial distribution under the implantation energy of 2 keV; and (b) full distribution under the implantation energy of 8 keV. 96
- Fig. 4.9 Total MOS capacitance of SiO₂ film with and without nc-Si as a function of different SiO₂ thickness. As the SiO₂ thickness increases, the capacitance difference between SiO₂ with and without nc-Si reduces. 97
- Fig. 5.1 Single layer nc-Si embedded in SiO₂ (a) and nc-Si embedded throughout the entire SiO₂ (b). 100

Fig. 5.2	Comparison of the C-V characteristics between two annealing temperatures (850 °C and 1000 °C). The annealing time is 20 minutes for both samples.	102
Fig. 5.3	Flatband voltage shift as a function of both annealing temperature and annealing time for conventional furnace annealing.	104
Fig. 5.4	Flatband voltage shift for the sample annealed by rapid thermal annealing (RTA) process.	105
Fig. 5.5	Number of trapped Si ions as a function of annealing temperature and annealing time for conventional furnace annealing.	107
Fig. 5.6	Number of trapped Si ions as a function of annealing temperature and annealing time for rapid thermal annealing.	107
Fig. 5.7	Reduction of flatband voltage shift by electron injection from the gate.	110
Fig. 5.8	Cross-sectional high resolution TEM image of sample 2.	112
Fig. 5.9	Hysteresis behaviors in C-V measurement of sample 1 (a), sample 2 (b) and the pure SiO ₂ sample (c).	113
Fig. 5.10	Flatband voltage shift as a function of the applied positive (a) and negative (b) gate voltage. The duration of the application of a gate voltage is 1 s.	115
Fig. 5.11	Current-voltage characteristics of sample 1, sample 2 and the pure SiO ₂ sample.	118
Fig. 5.12	Schematic illustrations of the two regions of the sample with nc-Si.	118

Fig. 5.13	Charge retention characteristics of the nc-Si structure. Electron trapping in the nc-Si is achieved by the application of +25 V gate voltage for 1 s.	119
Fig. 5.14	Si SIMS profile for the MOS structure with nc-Si distributed throughout the gate oxide.	121
Fig. 5.15	Cross-section TEM measurements for the MOS structure.	122
Fig. 5.16	Changes in MOS capacitance due to charging/discharging in nc-Si. (a) charging at +4 V for 320 s and discharging at -2 V for 160 s; (b) charging at -4 V for 320 s and discharging at +2 V for 160 s; and (c) comparison of the MOS capacitance between the MOS structure without nc-Si and the MOS structures with nc-Si after charging (charging at either + or -4 V).	124
Fig. 5.17	Equivalent circuit of the MOS structure with nc-Si embedded in the gate oxide. C_{nc-Si} represents the equivalent capacitance of the nc-Si, C'_{ox} represents the equivalent capacitance of the remaining SiO ₂ , and C_D represents the equivalent capacitance of the Si surface region, respectively.	126
Fig. 5.18	Changes in MOS capacitance due to charging at +4 V for 320 s and the discharging under UV illumination for 5 minutes.	127
Fig. 5.19	Changes in MOS capacitance due to charging at +4 V for 320 s and the discharging under low temperature annealing at 100 °C for 10 minutes.	127
Fig. 5.20	Reduction and recovery in the gate current after the electrical stress at +4 V for 320 s and the UV illumination for 5 minutes,	

	respectively. The I-V characteristic of pure SiO ₂ is included for comparison.	129
Fig. 5.21	Recovery in the gate current after thermal annealing at 100 °C for 10 minutes.	129
Fig. 5.22	A proposed model on the effect of charging and discharging of the nc-Si on the current conduction in the gate oxide.	131
Fig. 6.1	Memory type.	135
Fig. 6.2	Basic operating principle of a floating-gate non-volatile memory device.	137
Fig. 6.3	Illustration of a nanocrystal-based memory device.	138
Fig. 6.4	Electron flow during the FN programming.	140
Fig. 6.5	Electron flow during the CHE programming (Re-plotted using data from Ref. [160]).	141
Fig. 6.6	Energy band diagram for a charge stored in the floating gate.	142
Fig. 6.7	Electron flow during the FN erasing.	143
Fig. 6.8	The memory window of the device is determined from the threshold voltage differences between the programmed state and the erased state (Re-plotted using data from Ref. [160]).	144
Fig. 6.9	All the charges stored in the FG will leak to the channel due to isolated defect at the tunnel oxide (a). For nanocrystal-based memory, only the charge stored in the specific nanocrystal will leak away (b).	148
Fig. 6.10	(a) SRIM simulation of the nc-Si distribution; and (b) Cross-section TEM image of nc-Si embedded in the gate oxide of the memory devices.	151

Fig. 6.11	Threshold voltage shift as a function of program time and erase time under different program voltage or erase voltage.	152
Fig. 6.12	Endurance characteristics at various temperatures.	153
Fig. 6.13	Data retention characteristics at various temperatures. The devices have been cycled for 1000 P/E cycles at +12 V / -12 V with a pulse width of 1 ms.	154
Fig. 6.14	Transfer characteristics of the devices with $t_{\text{tunn}} = 7$ nm (a) and $t_{\text{tunn}} = 3$ nm (b). The $I_{\text{On}} / I_{\text{Off}}$ ratio is higher for $t_{\text{tunn}} = 7$ nm.	156
Fig. 6.15	Endurance characteristics for the thinner tunnel oxide ($t_{\text{tunn}} = 3$ nm) (a) and the thicker tunnel oxide ($t_{\text{tunn}} = 7$ nm) (b) at room temperature and 85 °C.	158
Fig. 6.16	Retention characteristics for the thinner tunnel oxide ($t_{\text{tunn}} = 3$ nm) (a) and the thicker tunnel oxide ($t_{\text{tunn}} = 7$ nm) (b) at room temperature and 85 °C.	159
Fig. 6.17	Illustration of the FN (a) and CHE (b) programming and the FN erasing (c).	162
Fig. 6.18	Transfer characteristics of the programmed and erased states under the programming / erasing operation of FN / FN (a) or CHE / FN (b). The programming / erasing time is 1 μ s.	164
Fig. 6.19	Memory window as a function of magnitude of programming / erasing voltage for the FN / FN and the CHE / FN operations.	165
Fig. 6.20	Endurance characteristics for the CHE / FN and FN / FN at room temperature (a) and at 85 °C (b).	167
Fig. 6.21	Retention characteristics for the CHE / FN and FN / FN at room temperature (a) and at 85 °C (b).	168

Fig. 6.22	Gate current before and after 10^4 programming / erasing cycles for the FN / FN (a) and the CHE / FN (b).	171
Fig. 7.1	Circuit representation of a 1T1C-DRAM.	174
Fig. 7.2	(a) Schematic cross section of the 1T-DRAM structure; and (b) profile of the implanted Si ions obtained from the SRIM simulation.	179
Fig. 7.3	Cross-section TEM measurement of the 1T-DRAM sample.	180
Fig. 7.4	Transfer characteristics of the 1T-DRAM after programming and erase operations.	181
Fig. 7.5	Measurement of the threshold voltage as a function of the programming time for the application of gate voltage of -12 V.	182
Fig. 7.6	Endurance performance of the 1T-DRAM.	183
Fig. 7.7	Retention characteristic of the 1T-DRAM at room temperature after the programming at -12 V for 3 ns.	184
Fig. 7.8	Top, schematic cross section (a) and charge-induced shifts in C-V (b) and I-V (c) characteristics of a conventional nc-Si memory device. Bottom, schematic cross section (d) and charge-induced changes in C-V (e) and I-V (f) characteristics of the nc-Si memory structure reported in this study.	186
Fig. 7.9	Bistability in capacitance (a) and resistance (b). Both the capacitance and resistance are measured at 0.5 V.	188
Fig. 7.10	Switching from a discharged state to a charged state by charging at +8 V (a); and Switching from a charged state to a discharged state by discharging at -8 V.	190

List of Table

Table 2.1	Comparison of the size of silicon nanocrystal produced by different techniques.	23
Table 4.1	Comparison between the measured and calculated MOS capacitance for various samples. The calculation is based on Eq. (4.3) for the partial distribution and Eq. (4.4) for the full distribution.	94
Table 6.1	Summary of comparison between semiconductor-memory technologies (Re-plotted using data from Ref. [48]).	145
Table 6.2	Critical problems faced by conventional Flash memory (Re-plotted using data from Ref. [48]).	146

Chapter 1

Introduction

This thesis presents a research study conducted at the School of Electrical and Electronic Engineering, Nanyang Technological University. In this work, the physical properties and electrical characteristics of semiconductor nanocrystal (i.e., silicon nanocrystal) embedded in a dielectric film are explored. This chapter introduces the background and the purpose of this work. Details of the work are presented in the following chapters.

1.1 Brief introduction to nanoelectronics and nanocrystal

The incorporation of nanotechnology into our daily life is inevitable with the usage of mobile phone, computers, television and electronic portable devices. We are enjoying a healthier, happier and more convenient life through the advent of new materials and semiconductor technology, information technology (IT) and artificial intelligence. Nanotechnology is a collection of technologies that modifies, controls, analyzes and uses materials at the nanoscopic level [1, 2]. With the emergence of nanotechnology into the main stream of electronics such as memory devices, micro-electromechanical system (MEMS), light emitting devices (LED) and quantum-electronic lasers, we are already living in a world using nanoelectronics for our daily life. Fig. 1.1 shows the size of biological and semiconductor features. Almost all of us use personal computers; the size of each

Chapter 1: Introduction

of the transistors inside the centre processing unit (CPU) is already in the sub-micrometer regime. The minimum feature size of the transistor in the CPU has been scaled down extensively for the past 3 decades [3]. Indeed, the chipsets in some of our daily-used consumable products over the past few years are also in the regime of sub-micrometer to nanometer regime. The sizes of transistors in our microprocessor as well as other chipsets are already hundreds of nanometer in length, which is smaller than our red blood cell and also many bacteria as shown in Fig. 1.1. The impact of shrinking the size of the transistor toward the nano regime has been reviewed by Geer et al. [4], and Bohr et al. [3]. Furthermore, it is believed that nanotechnology will eventually shift to the molecular level as well as towards DNA electronics [5, 6]. For example, Yale / Rice team has demonstrated a reconfigurable switch that falls into the category of molecular electronics [7]. The HP/UCLA team has also demonstrated an array of configurable switches, each consisting of a monolayer of redox-active rotaxanes sandwiched between metal electrodes [8]. Besides, Seeman et al. demonstrated DNA constructions as a possible mean of building general purpose computing devices [9, 10]. Certainly, the challenges such as maintaining the yield will be a major issue too [11]. There is no doubt that nanoelectronic devices will dominate in the next generation solid-state devices.

Chapter 1: Introduction

Fig. 1.1 Size of biological and semiconductor objects.

Fig. 1.2 Transistor size trend for different technology node (Re-plotted using data from Refs. [3] and [12]).

Chapter 1: Introduction

Nanoelectronics research is focusing on semiconductor structures and devices at the extremes of miniaturisation. Future nanoelectronic devices can be divided into two main categories. The first category continuously minimizes the size of conventional transistors to achieve faster switching speed. As shown in Fig. 1.2, the size of the transistor will continue to scale smaller towards the 45 nm and 30 nm technology node [12]. In the second category the small feature size is used to introduce quantum effects to create new types of devices. Solid-state nanoelectronic devices are believed to be one of the most promising devices for future applications. Fig. 1.3 shows the taxonomy of solid-state nanoelectronics devices [13]. Solid-state nanoelectronics can be divided into 3 main categories of (a) quantum dots, (b) resonant tunneling devices, and (c) single-electron transistors (SET). Nanocrystal-based memory devices and optoelectronic devices are potential research areas and can be grouped into the area of either the quantum dots or the SET. The size of nanocrystalline silicon is only ~ 5 nm, which is also a good candidate for single-electron transistor research. These three areas are interesting, both from the aspect of fundamental research, as well as device applications.

Fig. 1.3 Taxonomy of solid-state nanoelectronic devices (Re-plotted using data from Ref. [13]).

Over the past two decades, much research has gone into creating and characterizing semiconductors of extremely small size. When the dimensions of the crystal fall below 5 nm, the physical and electronic properties of the crystal change radically even though the chemical composition remains unchanged [14]. These crystals, known as nanocrystals or quantum dots, contain tens to thousands of atoms. Semiconductor nanocrystals can be described as a state of matter intermediate between molecular and bulk crystalline. Their small size and high optical activity make them very interesting for optical, electronic, and photonic applications [15, 16]. As the nanocrystal is reduced in size, the physical properties will change (i.e., band gap becomes larger) [17, 18]. Besides, the Coulomb blockade effect in nanocrystals is very interesting, especially for memory devices [19].

Chapter 1: Introduction

1.2 Future Semiconductor Memory Technology and Market Trends

Modern memory devices demand high-density, low power and high speed through advanced process technology development and smart design techniques. Future devices demand even higher performance. The needs for mass storage have grown massively particularly for mobile and portable applications (i.e., mobile phone, portable handheld, notebook, camera, heart pacer, wrist-watch and etc.). With the prevalence of digital telecommunication systems, there is an increase in demand for Flash memory, which is on the way to be the next-generation storage medium. Previous limitations of speed, density, power, performance and size must be overcome through the pursuit of differentiated value-added research and development. For example, to produce future non-volatile memory devices (details are explained in Chapter 6), different design and new materials are needed. On the other hand, dynamic random access memory devices (DRAM) are required for networking applications and communications with high speed, low power and unlimited program / erase cycle usage. Fig. 1.4 shows the future memory technology and demand trend for different areas such as personal computers (PCs), server, networking, communication fields and graphics [20-22]. Nanotechnology-based memory devices are necessary to accommodate all the above-mentioned features and requirements to support the future demands of memory devices. Fig. 1.5 shows the future market potential and sales for all semiconductor devices / products. We can observe that the two largest sales are the logic and the memory, at present and projected for the next 5 years. The memory sales has a huge potential market with the projection of over 80 Billion USD of sales revenue at year 2006 [23].

Chapter 1: Introduction

Fig. 1.4 Future technology and demand trend for memory devices.

Fig. 1.5 Potential market revenues for all products based on semiconductor devices (Re-plotted using data from Ref. [24]).

Chapter 1: Introduction

1.3 Silicon Nanocrystal: an overview

What is silicon nanocrystal? Silicon nanocrystal consists of a few tens to a few tens of thousands of silicon atoms aligned in crystalline form. For example, a silicon nanocrystal (nc-Si) with a mean core diameter of 1.0 nm, has about 35 silicon atom aligned in crystalline form [25]. Silicon nanocrystal has a typical dimension of 1 – 10 nm. SiO₂ films containing nc-Si have recently attracted much attention as they are very interesting from the pure physics as well as applied physics point of view. Silicon nanocrystal has unique charge storage ability that can be used for memory devices and single-electron memory devices. In addition, nc-Si embedded in SiO₂ dielectric films are also among the possible candidates for the application of Si-based optoelectronic ICs. With the size of nc-Si within the regime of < 10 nm, it is possible to investigate the Coulomb blockade effect at room temperature, electrical properties and optical properties for electronic and optoelectronic devices [26].

The formation of nc-Si using different fabrication techniques and conditions will result in a different nc-Si size distributions and density in the SiO₂ thin films. This requires much extensive research to fully explore the unique properties of the nc-Si.

1.4 Motivation

Continuous scaling of the device's length on the conventional silicon (Si) technology and the significant improvement of the performance of everyday appliances such as cell phones and computers has attracted many researchers around the globe to explore the physics and science of Si devices. In recent years,

Chapter 1: Introduction

research have been carried out to investigate the properties of Si nanostructures as well as various designs proposed to allow large quantities of devices to be fabricated on one single wafer [27]. However, there are many issues to be solved such as the performance expectation of new materials, new designs and new concepts of device operations. Furthermore, the reliability of these new materials are yet to be investigated.

The semiconductor market is and will continue to be dominated by logic and memory. Therefore research on nanoelectronics for memory devices will continue to be driven by the needs of an ever more demanding market. For some memory devices, the need to store information for a very long period of time is essential. Flash memory devices that allow hundreds of thousands of program and erase cycles, long retention time (i.e, ~10 years) and high density are needed. This type of non-volatile memory device (NVM) is often known as floating-gate (FG) [28]. Floating-gate memories contribute substantially to the semiconductor industry today and are vital for both code execution and data storage in portable electronic devices. However, when continuously shrinking the device dimensions, the device faces some reliability challenges. Semiconductor nanocrystal Flash memories are expected to have superior electrical characteristics which can resolve the limitations imposed by the conventional FG memories [19].

To develop the nanocrystal-based Flash memory, extensive research must be carried out to understand the physics and device behavior of semiconductor nanocrystals, particularly silicon nanocrystals (nc-Si), as discrete charge storage nodes. Nanocrystal charge storage nodes behave differently from single layer polysilicon charge storage layers. With the crystal size down to several nanometers, Coulomb blockade effects as well as other quantum effects become significant.

Chapter 1: Introduction

Therefore, proper understanding on the physical properties (i.e., electrical properties, size effect, carrier transport, and decay characteristics) and the device applications of nc-Si embedded in SiO₂ are important for future design and development and eventually manufacturing of products to meet customer specifications.

1.5 Objective

The objective of this Ph.D. work is to synthesize silicon nanocrystal (nc-Si) and to investigate the physical properties and memory application of nc-Si embedded in a SiO₂ matrix.

1.6 Scope of research and approach

The scope of research and approach in this Ph.D. thesis is as follows:

- 1) Investigate the charge transport and charge decay of silicon nanocrystal embedded in SiO₂ thin film. This can be done with Electrostatic Force Microscopy (EFM) which has an image resolution down to nanometers. The measurement of charging and discharging of silicon nanocrystal embedded in dielectric film and the mapping of charge transport during the charge decay of a single nanocrystal are carried out with the EFM.
- 2) Investigate the electrical properties (i.e., capacitance, flatband voltage shift and retention characteristics) of MOS structure containing a single layer nc-Si using the conventional capacitance-voltage (C-V) measurements. This investigation allows us to understand the charging and discharging of nc-Si when the sample is biased with different voltages. In addition the study of

Chapter 1: Introduction

the sample's current-voltage (I-V) characteristics will be carried out using the conventional I-V measurements.

- 3) Investigate the electrical properties (i.e., C-V and I-V characteristics) of MOS structure with nc-Si distributed throughout the SiO₂ using the conventional C-V and I-V measurements. The electrical properties are different from that of a SiO₂ containing a single layer of nc-Si. Appropriate model to describe the C-V and I-V characteristics of the MOS structure will be provided.
- 4) Fabrication of metal-oxide-semiconductor field effect transistor (MOSFET)-based Flash memory device with nc-Si as the charge storage node. The device will be fabricated using conventional CMOS 2- μ m technology and the nc-Si will be formed using very low energy Si-ion implantation followed by high temperature annealing.
- 5) Investigate the memory characteristics (i.e., threshold voltage shift, program / erase endurance, and retention characteristics.) of the nc-Si-based Flash memory cell at room and hot temperature.

1.7 Major contributions in this thesis

The major achievements of this research are listed as below:

- 1) Visualized the charge transport in silicon nanocrystal embedded in SiO₂ matrix by using Electrostatic Force microscopy (EFM) method [29, 30].
- 2) Examined the influence of nanocrystal's depth distributions on the charge decay characteristics [31].

Chapter 1: Introduction

- 3) Proposed an approach to understand the increase of total capacitance of SiO_2 embedded with silicon nanocrystal based on the Effective Medium Approximation (EMA) for the first time [32].
- 4) Determined the static dielectric constant of silicon nanocrystal from the C-V measurements [33].
- 5) Investigated the influence of annealing temperature and annealing duration on the flatband voltage shift of SiO_2 embedded with single layer of silicon nanocrystal [34].
- 6) Investigate the charging effect and gate leakage current in a single layer silicon nanocrystal embedded in SiO_2 thin film [35].
- 7) Investigated the novel and interesting electrical behaviors of SiO_2 embedded with silicon nanocrystal distributed throughout the entire SiO_2 thin film with peak nc-Si concentration in the SiO_2 surface region [36-38].
- 8) Designed, fabricated, and characterized the memory characteristics of silicon nanocrystal-based non-volatile memory devices [39].
- 9) Investigated the influence of tunnel oxide thickness on the performance of the nc-Si memory devices [40, 41].
- 10) Investigated the impact of programming mechanism on the performance and reliability of nc-Si memory devices [42].
- 11) Proposed a novel one-transistor volatile memory device based on silicon nanocrystal, which has a fast programming speed and very long retention time. It can replace the conventional one-transistor one-capacitor DRAM.
- 12) Proposed novel two-terminal memory devices based on silicon nanocrystal, which allow for fabrication of high-density memory array.

Chapter 1: Introduction

1.8 Thesis outline

In this thesis, the electrical properties and Flash memory devices based on ion-beam synthesized silicon nanocrystal embedded in SiO_2 films are presented. Chapter 1 provides a brief overview of silicon nanocrystal and the objective and scope of research. Chapter 2 discusses the fabrication of silicon nanocrystals using ion-implantation techniques and the electrical and non-electrical characterization of silicon nanocrystals embedded in SiO_2 matrix. The electrical characterization includes conventional current-voltage and capacitance voltage measurements. The non-electrical characterization includes Transmission Electron Microscopy (TEM), X-ray Diffraction (XRD), Secondary Ion Mass Spectroscopy (SIMS) and Stopping Range of Ions in Matter (SRIM), and Scanning Electron Microscopy (SEM) measurements, which provide the information of the size of the nanocrystals and their depth distributions. Some discussions on the potential applications of nc-Si are provided in this chapter.

Chapter 3 focuses on understanding the mechanisms of charge transport and charge decay in silicon nanocrystals embedded in SiO_2 matrix. The study of charge transport and charge decay in silicon nanocrystal is carried out using electrostatic force microscopy (EFM). The influence of different nanocrystal distributions on the charge decay is also presented.

In Chapter 4, the study of the static dielectric constant of silicon nanocrystals embedded in SiO_2 matrix is presented. The presence of nanocrystals in SiO_2 will affect the total capacitance of the material. The static dielectric constant is determined from the total capacitance of the SiO_2 film based on the effective medium approximation (EMA) method. The results are proven to be reliable by comparing them with values from literature.

Chapter 1: Introduction

Chapter 5 discusses the electrical behaviors of two different nc-Si distributions inside the SiO_2 (i.e., a single layer of nc-Si and nc-Si distributed throughout the entire SiO_2). For the former case, the effects of annealing temperature, annealing time and temperature ramping rate on the flatband voltage shift of silicon nanocrystal embedded in SiO_2 close to the SiO_2 surface are presented. The amount of remaining Si ions trapped in the SiO_2 is then determined. The charge trapping properties of such a structure including single electron tunneling effects is observed. For the latter case, the capacitance-voltage characteristics and tunneling current are studied. A model to describe the C-V and I-V characteristics of such structure is provided.

Chapter 6 deals with the fabrication and characterization of non-volatile memory structures based on nc-Si. The nc-Si are synthesized with very low energy ion-implantation followed by annealing in N_2 ambient. The memory characteristics are investigated at different operating temperature. On the other hand, the impact of tunnel oxide thicknesses and programming mechanism on the memory's performance are discussed too.

Chapter 7 describes the inventions of the 1T-DRAM and two-terminal non-volatile memory devices based on silicon nanocrystal. It is hoped that this invention can replace conventional memory devices.

Finally, Chapter 8 summarizes the research works of this thesis and provides recommendations for future work.

Chapter 2

Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

In this chapter, the common techniques used to synthesize silicon nanocrystal on the SiO_2 surface or inside the SiO_2 are discussed. Emphasis is placed on the ion-implantation process by using Si ion implantation followed by annealing at high temperature. A brief introduction of other methods to produce nc-Si will be included. Some discussions will be provided on their relative merits and shortcoming. Further on, characterization techniques will also be presented to understand the properties of these nanocrystals. To characterize the silicon nanocrystal embedded in SiO_2 thin films, electrical and non-electrical measurements are performed on the samples. Finally, some discussions are provided on the potential applications based on nanocrystal embedded in dielectric film.

2.1 Introduction

Since the first core memory in electronics was proposed by Kahng and Sze in 1967 [43], various device structures have been proposed and extensive research has been conducted on these memory devices, including the erasable-programmable read-only memory (EPROM) [44] and electrically alterable read-

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

only memory (EAROM) [45]. With the invention of nanocrystal-memories in 1995 by IBM [46, 47], it has been forecasted as one of the most promising memory devices to replace conventional floating-gate (FG) memory devices [48]. Moreover, nanocrystal-based memory technology is fully compatible with the complementary-metal-oxide-semiconductor (CMOS) process, it is easy for industry to migrate from conventional FG memory devices to nanocrystal-based memory devices.

Fabricating devices with small critical features is a challenge even with the most advanced lithography and processing equipment. Currently, CMOS is the cheapest technology used by the semiconductor industry. However, to integrate nanocrystals technology successfully into an existing CMOS manufacturing platform, some challenges exist and several stringent requirements must be met. For example, to integrate nanocrystals into memory devices, low defect densities, size, shape, density and separation are important parameters to be controlled. This has yet to be proved using the existing state of the art CMOS technology.

2.2 Ion implantation

Ion implantation his a common technique in conventional microelectronic devices fabrication. Dopants such as boron, phosphorous, or arsenic are implanted into the silicon wafers in CMOS fabrication [49-51]. As pointed out by Bala et al. [52], the major advantages of ion implantation are the masking flexibility, throughput, extendibility to larger wafers, and ability to form impurity profiles that are not possible with simple diffusion process. However, ion implantation systems are very complex and can create problems such as defects, thus limiting product yield. Many researchers has tried to investigate the implantation of Si ions into

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

dielectric films [39, 53-55]. In a typical process, Si ions are implanted into thermally grown SiO₂ films at a specific energy. For example, Si ions are implanted at energy of 30 keV into a 100 nm thick thermally grown SiO₂ layer on Si (100) wafers. The concentration and the depth distribution of the profile depends on the implantation energy and the implantation dosage [55]. Recently, with developments in fabrication equipment, it is possible to implant various ion species including Si⁺ with very-low and ultra-low energy (i.e., 0.65 keV to 2 keV) into very thin SiO₂ films [40, 56, 57]. To remove the defects created during the ion implantation, additional annealing at high temperature must be carried out.

High temperature annealing typically at ~1000 °C to ~1100 °C, for 0.1 hr to 5 hr is needed, to precipitate silicon nanocrystals (as shown in Fig. 2.1). The annealing process may be carried out in N₂ ambient, H₂ + N₂ ambient, or O₂ ambient [56]. The annealing also serves to recover the defects and damages produced by the ion-implantation process. Hydrogen passivation of nc-Si has been performed by Cheylan et al. [58]. Besides, Wang et al. has studied the effect of hydrogen passivation on the microstructure of nc-Si embedded in SiO₂ film [59]. Fig. 2.1 illustrates the Si⁺ implantation and subsequent annealing at high temperature to induce the nanocrystal formation.

This technique offers the advantage of being fully compatible with the CMOS process and is able to control the nc-Si size and distribution by adjusting the implantation energy and silicon ion dose [60]. The ion implantation process provides good homogeneity and good reproducibility of the profiles. For example, nc-Si distributed inside the SiO₂ film with a narrow distributions is very useful for nanocrystal-based Flash memories [56]. On the other hand, photoluminescence studies on the nc-Si produced by ion-implantation has been shown by Torre et al.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

recently [61]. This shows that the nc-Si distributions can be controlled easily using ion-implantation technique.

Fig. 2.1 Illustration of Si⁺ implantation process followed by high temperature annealing to form nc-Si.

2.3 Other fabrication techniques

2.3.1 Chemical Vapor Deposition

Chemical vapor deposition (CVD) is another commonly used technique to fabricate silicon nanocrystals. In this technique, silane (SiH₄) is thermally decomposed at 550 - 650 °C to nucleate the nanocrystals on the Si substrate. The pressure during the CVD process varies from 0.12 - 0.7 Torr [62-64]. The entire process includes nanocrystal incubation, nucleation, growth, and deposition which all take place in the same chamber, as shown in Fig. 2.2. The density of the nanocrystal (/cm²) is controlled by the deposition time [65]. This technique is also CMOS compatible. However, the nanocrystal size fluctuations is large as being reported by Nakajima et al. [66] and individual nanocrystal cannot be fabricated

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

with monolayers precision. To improve the nanocrystal size distribution, thermal oxidation of the nanocrystal after the initial deposition step can be carried out. This oxidation step can result in a lower trap density at the nanocrystal-oxide interface [19]. Recently, some works have been carried out by Zacharias group to produce well dispersed nc-Si [67, 68] and superlattices of passivated nc-Si embedded in SiO₂ thin film [69].

Fig. 2.3 shows atomic force microscopy (AFM) images of a sample containing silicon nanocrystals grown by CVD technique. The size of the nc-Si varies from 30 - 50 nm.

Fig. 2.2 The density of nanocrystal can be controlled by varying the deposition time (Extracted from Ref. [65]).

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

Fig. 2.3 AFM image of nc-Si produced by CVD technique. The scan size is $1\ \mu\text{m} \times 1\ \mu\text{m}$.

2.3.2 Aerosol synthesis

A spherically shaped silicon nanocrystal can be formed by pyrolytic decomposition of diluted silane (SiH_4) gas at $\sim 950\ ^\circ\text{C}$ [70]. Initially these particles are formed by homogeneous gas-phase nucleation and grown by coagulation. Then, thermal oxide can be grown on the particles to form an insulating shell [71]. The oxidation step has an additional advantage of sharpening the particle size distribution and decrease the size of the nanocrystal. The main advantage of this technique is the ease of control of fabrication process, nanocrystal size and size distribution, and good process integration as mentioned by Ostraat et al. [72]. The main drawback of this technique is that this technique is not proven for large scale manufacturing.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

2.3.3 Sputtering

Another technique to produce nc-Si is by sputtering. In this technique, the nc-Si can be produced by bombarding the Si target with energetic ions, typically Ar^+ . By independently varying the power applied to each magnetron in either balanced or unbalanced configurations, an entire spectrum of mixed compositions and microstructures is possible. When Ar gas is injected into the field formed by high voltage applied on the electrodes, Ar ions will be accelerated and collide on the cathode surface. Atoms of the cathode material will be sputtered and deposited on the substrate surface forming ultra-fine particle films. Some characterization (i.e., electrical and optical) have been performed on the nc-Si produced using this method as shown in references [73-76].

2.3.4 Pulse Laser Deposition

Pulse Laser Deposition (PLD) is a technique similar to sputtering technique. It is also commonly known as laser ablation technique. In this technique, a Si target is ablated by a pulse laser beam in an inert gas ambient. The ablated Si particles are deposited on the substrate surface. An annealing process, carried out in O_2 ambient leads to the formation of nc-Si embedded in SiO_2 [16, 77, 78]. The annealing effect on the structure of nc-Si produced by PLD method has been extensively studied by Makino et al. [16]. Orii et al. synthesized silicon nanoparticles via PLD of a silicon target. Size of nc-Si between 3 to 6 nm has been produced [79]. The advantage of using this technique to produce nc-Si is that the density of the nc-Si can be controlled precisely compared to that of using the CVD method.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

2.3.5 Mechanical ball milling and spin-coating

In this technique, crystalline Si powder is mechanically milled at ambient temperature to extract different weight of Si powder. After the milling process the extracted Si powders were mixed in tetraethylorthosilicate (TEOS) solution. Then the mixture is was spun onto the Si substrate as sol-gel film [80]. The main advantage of using this technique is that the sample can be produced at a relatively lower production cost. However, controlling the size of the nanocrystal is a difficult task. Further more, there is a high possibility of agglomeration of nanocrystal, which results in a non-uniform distribution of nanocrystal in the TEOS film.

2.3.6 Comparison on the nanocrystal fabrication technique

All these techniques have their own advantages and disadvantages. The purpose of all synthesizing methods is to achieve size-controlled silicon nanocrystals. Except for the size of nc-Si, as for the purpose of potential device applications, researchers need to pay attention to the size distribution and depth distribution of nc-Si in dielectric films. These three important factors (i.e., inter-nc-Si distance (a), size of nc-Si (b) and depth distribution (c)) have a significant impact on potential devices based on nc-Si. They are illustrated in Fig. 2.4. Previous mentioned methods (for example CVD, sputtering, PLD and aerosol synthesis) normally result in a relatively broad size distribution of synthesized nc-Si. By using ion implantation technique, size control can be realized varying the ion implant energy and silicon dosage [81] or by subsequent oxidation of nanocrystals [66, 82]. Recently a general review on the synthesis and size control

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

of silicon nanocrystal via different techniques has been provided by Heitmann et al. [83].

Fig. 2.4 Schematic illustration of three most important factors during the fabrication of nc-Si for device applications [56].

Table 2.1 Comparison of the size of silicon nanocrystal produced by different techniques.

Techniques	Size of nc-Si (nm)	References
Ion implantation	4 - 8	[55, 56, 84]
CVD	8 - 30	[63, 85]
Sputtering	10 - 50	[73]
Aerosol synthesis	3 - 10	[70, 71]
PLD	2 - 20	[16]
Ball Milling	8 - 50	[80]

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

Table 2.1 shows the comparison of the silicon nanocrystal size as obtained from the literature review. It is observed that ion-implantation method can control the nc-Si at a relatively narrow size range as compared to that using other methods. With such advantages, ion-implantation method is employed for all the fabrications done in this work.

2.4 Fabrication of SiO₂ thin film with silicon nanocrystal

All the samples used in this study are fabricated using standard CMOS process in the Micro-Fabrication Laboratory (MFL) at Nanyang Technological University, Singapore. Three few nc-Si distributions in the SiO₂ thin film have been investigated in this study:

- Single-layer of nc-Si embedded in the SiO₂ thin film (as shown in Fig. 2.5), Si⁺ ions are implanted into the SiO₂ by very-low energy ion-implantation (typically 1 – 5 KeV).
- nc-Si distributed throughout the entire SiO₂ thin film with peak nc-Si concentrations close to the SiO₂ surface. The implantation energy follows the case of wide distributions, but there is an additional SiO₂ etching step after the annealing process. (as shown in Fig. 2.6).
- Wide distributions of nc-Si in the SiO₂ (as shown in Fig. 2.7). The implantation energy varies from 5 keV to ~14 keV. After the implantation step, all these samples will be annealed in N₂ ambient at high temperature to form nc-Si.

Details of the fabrication processes for each of the 3 distributions are listed in Appendix A.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

Fig. 2.5 Schematic illustration of single-layer of nc-Si embedded in SiO₂ thin film.

Fig. 2.6 Schematic illustration of nc-Si distributed throughout the entire SiO₂ thin film with peak nc-Si concentrations close to the SiO₂ surface.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

Fig. 2.7 Schematic illustration of wide distributions of nc-Si embedded in SiO₂ thin film.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

2.5 Non-electrical characterization of nanocrystal

2.5.1 Transmission Electron Microscopy (TEM)

Transmission electron microscopy (TEM) is a destructive technique used to provide high resolution structural information in either plan view or cross section of a sample. TEM measurements reveal the crystallinity and orientation of a sample. Normally, the samples for TEM measurements are typically prepared by thinning the samples down to ~200 nm thick. The samples are imaged in vacuum using very high energy (~100 - 200 keV) electrons. During such high energy imaging, the spatial resolution of the sample imaged can be as small as 0.2 nm. Besides, this technique can be used to image a variety of samples such as insulators, conductors and semiconductors.

Cross-section TEM technique has been widely used to image nanostructure materials as well as nanoparticles embedded in dielectric film. Qin et al. [86] has performed cross-section TEM to observe the size of nanocrystal silicon after some thermal treatment. Seifarth et al. [73] has also performed TEM measurements to observe the lattice planes of polycrystalline silicon in SiO₂ matrix. Assayag et al. [87] used TEM to determine the distance between the nc-Si layer and the Si substrate. Similarly, Bonafos et al. [55] has performed TEM measurements on SiO₂ sample with different energy of Si⁺ implantations, as shown in Fig. 2.8. Wang et al. [88, 89] used TEM to observe the coalescence and the orientation of nc-Si embedded in SiO₂. Besides, plane-view TEM measurements of nc-Si on SiO₂ surface has been demonstrated by Ostraat et al. [72] as shown in Fig. 2.9. Both the cross-section TEM measurements and plane-view TEM measurements are widely used to deduce the size of nc-Si [90-93].

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

Fig. 2.8 Effect of Si⁺ implantation into SiO₂ at energies increasing from 1 to 5 keV (Extracted from Ref. [55]).

Fig. 2.9 Plan-view TEM measurements of nc-Si (Extracted from Ref. [72]).

2.5.2 X-Ray Diffraction (XRD)

X-ray diffraction (XRD) is a technique used to determine the size of a crystalline structure. The mean nc-Si size (*D*) embedded inside a SiO₂ matrix can be estimated from x-ray diffraction measurement with the Scherer’s equation [94]

$$D = \frac{0.9\lambda}{\Delta\theta \cos(\theta_B)} \tag{2.1}$$

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

where λ is the wavelength of the x-ray, θ_B is the Bragg angle and $\Delta\theta$ is the full width of the half maximum (FWHM) of the Bragg peak after correction for instrumental broadening. The correction of instrumental broadening can be calculated by using the following equation [95]:

$$\Delta\theta^2 = \Delta\theta_M^2 - \Delta\theta_{Si}^2 \quad (2.2)$$

where $\Delta\theta_M$ is the measured FWHM of the peak and $\Delta\theta_{Si}$ is the FWHM of polycrystalline Si standard (instrumental broadening).

XRD technique has been used by Pedersen et al. [96] to observed the crystalline structure of Y_2O_3 . The average grain size for other materials like the nanostructure Strontium Titanate ($SrTiO_3$) [97] and Germanium nanocrystals [98] have also been determined using XRD technique. Liu et al. [37] and Chen et al. [99] had performed XRD and TEM measurements to confirm the size of nc-Si embedded in a SiO_2 matrix. Similarly Wang et al. [100] and Seifarth et al. [73] had performed XRD to determine the size and orientation of nc-Si embedded in SiO_2 matrix. This shows that XRD method is useful to determine the size of nc-Si embedded in SiO_2 .

2.5.3 Secondary Ion Mass Spectroscopy (SIMS)

When the SiO_2 sample is implanted with Si ions, it is essential to obtain the profile of the implanted Si ions. This can be achieved by using Secondary Ion Mass Spectroscopy (SIMS) measurements. SIMS is widely used to trace elements in solid materials, especially the doping depth profile in Si substrate [50]. In a typical SIMS analysis, the samples are sputtered by a focused energetic primary ion beam which is rastered over a square area, usually $\sim 100 \mu m \times 100 \mu m$.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

Secondary ions formed during the sputtering process are accelerated away from the sample surface by a nominal sample voltage of ~ 4.5 kV. A fraction of the secondary ions is accepted for analysis by a mass spectrometer and is collected in the rastered region. The secondary ions are energy focused by an electrostatic analyzer, and mass-filtered by a magnetic sector analyzer. After passing through the analyzers, the ions are detected.

Chen et al. [101] used SIMS technique to determine the concentration of nitrogen in ultra-thin SiO_2 film. Murrell et al. [51] performed SIMS to understand the effect of rapid thermal annealing on the diffusion of Boron in Si(100) wafers. Recently, Marstein et al. [102] used SIMS to characterize the distribution of implanted Ge ions in the SiO_2 . With the capability of SIMS measurements, determine the depth profile of implanted Si ions in thin SiO_2 film should be easy.

2.5.4 Stopping Range of Ions in Matter (SRIM) Simulation

Stopping Range of Ions in Matter (SRIM) simulation can also be used to calculate the depth profile of implanted Si^+ in the SiO_2 thin film. SRIM simulation is based on a quantum mechanical treatment of ion-atom collisions. It is a theoretical method of forecasting the profile of implanted ions [103]. It has a very friendly user interface, and has default parameters for all ions in all materials up to an ion energy of 1 GeV. It has been shown by Liu et al. [104] to efficiently predict the depth profile of Si ions in SiO_2 . Many efforts have also been carried out to study the distributions of implanted Si^+ in SiO_2 films using SRIM simulations [105-108]. This method is proven to be reliable to predict the Si^+ distributions in SiO_2 films, and comparable to SIMS measurements.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

2.5.5 Scanning Electron Microscopy (SEM)

Scanning Electron Microscopy (SEM) is a non-destructive technique used to map the surface of a thin film or material. Sample to be viewed by SEM is placed in a vacuum chamber. Electron beam is produced from the filament of the electron gun in the vacuum chamber. The beam forms a line that continuously sweep across the sample at high speed. There are hundred of possible approaches made possible by electron gun, x-ray fluorescence, primary, secondary or backscattered electrons. SEM technique can be used to predict the size of silicon nanocrystal synthesized via CVD method. In contrast to TEM measurements, SEM measurement does not tell the crystallinity. Even though SEM do not have the resolution as good as TEM, it is still possible to observe the existence of particles on a surface of a thin film. Moreover, the sample preparation is much simpler than TEM.

SEM technique is commonly used to observed the final structure of a nano-scale device, such as a single-electron memory [109, 110], silicon nanostructures [111] or even the cross section of a DRAM [112]. Besides, SEM technique has been used by Ji and Anderson [113] to study the morphology of nc-Si deposited on top of SiO₂ film at different temperature. Suzuki et al. [114] uses SEM to observe the cross-sectional structure of the silicon nanocrystallites synthesized using PLD technique.

2.5.6 Results

TEM measurements are used in this study to measure the size of the nc-Si embedded in SiO₂. Fig. 2.10 shows the cross-section TEM image of silicon

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

nanocrystal embedded in SiO_2 . This high-resolution image demonstrates the presence of nanocrystals in the SiO_2 and also reveals the size of the crystalline Si. The average nanocrystal diameter is ~ 4 nm with a density of $\sim 3 \times 10^{12} \text{ cm}^{-2}$ estimated from the TEM image. This image shows excellent nc-Si / SiO_2 interface quality.

Fig. 2.10 Cross-section high resolution TEM measurements on the sample with nc-Si.

XRD measurements are performed on the fabricated samples too. Fig. 2.11 shows the XRD measurement on one of the sample embedded with nc-Si, similar to the sample used for TEM measurements as shown in Fig. 2.11. The mean size of the nc-Si obtained from the 3 times XRD measurement with the Scherer's equation is 4.5 ± 0.3 nm. Here, $\lambda = 1.54 \text{ \AA}$, $\theta_B = 55.7^\circ$ and $\Delta\theta = 0.0576$ (radian). Thus the

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

estimated nc-Si size is ~4 nm. The time involved to do the XRD measurements is much faster compared to the use of TEM measurements.

Fig. 2.11 XRD profile of the SiO₂ embedded with nc-Si.

Fig. 2.12 Si⁺ SIMS profile.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

In this study, SIMS is used to determine the depth profiles of excess Si^+ implanted into the SiO_2 film. Cs^+ is used as the primary beam to sputter off the atomic layer of the SiO_2 sample. Fig. 2.12 shows a typical Si SIMS depth profile in SiO_2 film. During the SIMS measurements, $^{28}\text{Si}^+$ are detected. The background was subtracted to obtain the $^{28}\text{Si}^+$ profile as shown in Fig. 2.12. The Si^+ implantation was carried out at 8 keV with an implant dosage of $1 \times 10^{16} \text{ cm}^{-2}$. There is a Gaussian-like distribution of Si^+ distributed from the surface to $\sim 30 \text{ nm}$ in the SiO_2 .

Fig. 2.13 shows the comparison of implanted Si profiles between SIMS measurements and SRIM simulations. Both SIMS and SRIM results give an acceptable Si depth profile, distributed from the surface to a depth of $\sim 40 \text{ nm}$ with the peak being located at about 15-18 nm. The consistency between these two methods enables the accurate determination of the depth profile of nanocrystal in dielectric film, both experimentally and theoretically. SRIM simulation is used extensively to determine the Si^+ profile and the detail will be discussed in Chapter 4.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

Fig. 2.13 Comparison of SIMS measurements and SRIM simulation of Si^+ implanted into SiO_2 thin film at energy of 1 keV.

SEM measurement is used to reveal the nc-Si produced by LPCVD technique. Fig. 2.14 shows the top view SEM measurements of nc-Si on SiO_2 thin film. The mean diameter for the nc-Si is $\sim 10 \pm 2$ nm. The density of the nc-Si is $\sim 3 \pm 1 \times 10^{11} \text{ cm}^{-2}$.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

Fig. 2.14 Top view SEM image shows the presence of silicon nanocrystal / nanoparticles at the SiO_2 surface.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

2.6 Electrical characterization of nanocrystal

DC electrical measurements are performed with a HP4156A semiconductor parameter analyzer at room temperature, and capacitance measurement is performed with a HP 4284A LCR meter at 1 MHz.

2.6.1 Capacitance-voltage and current-voltage characteristics

Electrical property is very important in identifying the operating condition and behavior of nc-Si embedded in SiO₂ dielectric films. The two main electrical characteristics of nc-Si embedded in SiO₂ dielectric films are capacitance-voltage (C-V) characteristic and current-voltage (I-V) characteristic. The C-V characteristic of nc-Si embedded in SiO₂ is different from pure SiO₂. Fig. 2.15 shows a typical C-V characteristic of nc-Si embedded in SiO₂. During the C-V measurement, the voltage is swept from accumulation state to depletion state; and from the depletion state to accumulation state. A hysteresis effect [64] can be observed after the reversible measurements. The hysteresis effect represents a shift in the flatband voltage (V_{fb}) or threshold voltage (V_{th}) during the reversible C-V or I-V measurements. This is a charge trapping event. In contrast, the control sample (i.e., pure SiO₂) does not exhibit any hysteresis effect. This effect has been observed and reported by many researchers [40, 56, 90]. More detailed studies on the electrical properties of different nc-Si distributions in the SiO₂ will be presented in Chapter 5.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

Fig. 2.15 Hysteresis observed during reversible C-V measurement (a). Pure SiO_2 does not exhibit hysteresis effect (b).

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

The I-V characteristic for nc-Si embedded SiO_2 is another important issue to be discussed. The I-V characteristic of SiO_2 embedded with nc-Si exhibits hysteresis effect [115]. This hysteresis effect can realize the program and erase application in memory devices where shift in the flatband voltage to positive and negative value is achieved by applying the gate voltage in reverse order. For drain current (I_d) versus gate voltage (V_g) characteristic, hysteresis effect can be observed clearly with the reversible voltage sweep. Fig. 2.16b shows the shift in the drain current with reversible gate voltage applied.

This small hysteresis effect observed in Fig. 2.16b during drain current versus gate voltage measurement is due to the shift of the flatband voltage. In contrast, the control sample (without nc-Si) has no shift in the flatband voltage as shown Fig. 2.16a. This shows that nc-Si embedded in SiO_2 samples can be used as charge storage node in memory devices.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

Fig. 2.16 Reversible drain current (I_d) measurements for both sample without nc-Si (a) and with nc-si (b).

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

2.7 Physical Properties

2.7.1 Coulomb blockade and Single-electron charging effect

When the size of a Flash memory is very small (i.e., typically in the range of $< 50 \text{ nm} \times 50 \text{ nm}$), some intriguing features such as single-electron / single-hole charging phenomenon at room temperature become very significant. Understanding the physics behind this phenomenon is indeed important. The single-electron charging phenomenon is a manifestation of the Coulomb blockade (CB) effect. The CB effect is due to the discrete changes in the charging energy of an ultra-small capacitor [116]. These ultra-small capacitors can also be an isolated conducting island as shown in Fig. 2.17. This discrete change in the charging energy of the capacitor is due to the electrostatic and quantum interaction between single particles. For example, when one electron gains entry into a quantum dot / nanocrystal, another electron needs to overcome the Coulombic repulsion from the initial electrons that already reside in the quantum dot / nanocrystal. To overcome the Coulombic repulsion, external electric field can be applied to the control gate as shown in Fig. 2.17. Analytically, one can express the electrostatic energy of N number of electrons trapped in the quantum dot / nanocrystal as [117]

$$E(N) = QV_g + \frac{Q^2}{2C} \quad (2.3)$$

where $Q = -Ne$ is the stored charge in the quantum dot / nanocrystal, V_g is the external applied gate voltage, e is the elementary charge unit and C is the capacitance of the quantum dot / nanocrystal. Due to the repulsion interaction between the electrons and the quantum dot / nanocrystal, the total charge Q is represented as negative, while Eq. (2.3) represents the attractive interaction between the Q and the positive gate bias.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

The charging energy associated to a single electron trapped into the quantum dot / nanocrystal can be presented as

$$\Delta E = \frac{e^2}{2C} \quad (2.4)$$

which can be related to the second term in Eq. (2.3). For example, the capacitance of the quantum dot / nanocrystal can be of order 10^{-18} F when the size is $\sim 1-5$ nm. As such, the charging energy of the quantum dot / nanocrystal can be a few hundreds of meV. This charging energy is larger than that of the thermal energy at room temperature (~ 26 meV). Thus, this charging energy is not easily affected by thermal effects and the influence of the program voltages on the total charges trapped in the quantum dot / nanocrystal is very significant.

Fig. 2.17 Illustration of the total electron energy in the quantum dot / nanocrystal for various gate voltages applied.

In a semiconductor nanocrystal, the charging energy is also strongly influenced by size quantization effects that arise from the wave nature of the highly confined electrons. This quantization energy level imposes an additional energy burden of ΔE to the classical CB energy when a new energy level is occupied by an

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

electron due to the size effect. The charging energy will become $\Delta E_I = \Delta E + e^2/2C$ whenever a new energy level is occupied by an electron [117].

Fig. 2.18 Energy band diagram of a nanocrystal containing (a) N electrons with a CB gap, and (b) $N+1$ electron without a CB gap.

Fig. 2.18 shows two energy band diagrams that illustrate the single-electron charging in a nanocrystal / quantum dot sandwiched between two SiO_2 thin films. For the SiO_2 on the right hand side, it is connected to a metal. The black dots represent electrons. The energy levels due to size quantization are depicted as lines in the nanocrystal, and the dots represent electrons. When the Fermi level is not aligned to the energy level of nanocrystal, there is a CB gap (E_{CB}). Fig. 2.18a shows the situation of N electrons in the nanocrystal. When the metal is biased with negative voltage, electron will be trapped into the nanocrystal quantized level when both the nanocrystal energy level and the Fermi level of the metal are aligned. Upon the entry of the $(N+1)^{\text{th}}$ electron in the nanocrystal, a CB gap develops between the $(N+1)$ and the $(N+2)$ levels.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

2.7.2 Dielectric Constant of Silicon Nanocrystal

Reduction of the static dielectric constant becomes significant as the size of the quantum confined physical systems, such as quantum dots / nanocrystal and nanowires, approaches the nanometer range. A reduced static dielectric constant increases the Coulomb interaction energy between electrons, holes, and ionized shallow impurities in quantum confined structures [118]. Wang and Zunger have carried out an empirical pseudopotential calculation of the size-dependent static dielectric constant ϵ of silicon quantum dots [119]. Lannoo et al. has applied a semiempirical linear combination of atomic orbitals (LCAO) technique to calculate the static dielectric constant for silicon quantum dots as related to porous silicon [120, 121]. The static dielectric constant can be written as [118]:

$$\epsilon = 1 + \frac{\epsilon_B - 1}{1 + (\Delta\epsilon_a / E_g)^2} \quad (2.5)$$

where ϵ_B is the dielectric of bulk silicon, E_g is the bandgap of bulk silicon, and

$\Delta\epsilon_a = \left(\frac{\pi E_F}{k_F r} \right)$, where E_F is 12.6 eV, r is the radius of the silicon quantum dot and k_F

is the free isotropic energy band with all valence electrons up to an energy E_F . Fig. 2.19 shows the size-dependant static dielectric constant of silicon nanocrystal based on the models from Refs. [119, 120]. Significant suppression of the dielectric constant of silicon compared to the bulk silicon of 11.9 can be observed when the size of the silicon quantum dot is reduced to < 10 nm.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

Fig. 2.19 Plot of size-dependent static dielectric constant vs the radius of the silicon sphere based on Lannoo and Wang and Zunger models.

The reduction of static dielectric constant with decreasing size is still under debate. Among the different mechanisms proposed for dielectric suppression of nanoscale materials, most are related to: (i) opening of the band gap, which lowers the polarizability [119], and (ii) the breaking of polarizable bonds at the surface [122].

2.8 Applications of nanocrystals embedded in dielectric films

2.8.1 Nano-memory devices

Embedded nanocrystals in the dielectric films can be implemented as memory devices. Silicon nanocrystals exhibit charging and discharging effect, allowing the devices to read, write and erase information stored in nc-Si as shown in the previous section. With different voltage polarities applied on the gate, charging and discharging of nc-Si can be realized. Once the nc-Si are charged, flatband voltage will shift accordingly. If the nc-Si are discharged, flatband voltage will shift back to its initial value. As the memory application using conventional floating gate structure begin to reach it's limitation in technology scaling, memory devices based on nc-Si embedded in dielectric films have great potential to overcome the current limitations. Fig. 2.20 shows a cross-section of nanocrystal-based memory device and the functions of write, read, and erase [46]. This type of nanocrystal-based memory devices have been demonstrated by several groups, mainly using the CVD method to synthesize the nanocrystals [62-64].

Fig. 2.20 Silicon nanocrystals as memory devices (Extracted from Ref. [46]).

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

2.8.2 Single-electron devices

The design concepts used in conventional semiconductor technology cannot be scaled down infinitely; thus new concepts must be found. In recent years, physical transport properties based on the Coulomb blockade of tunneling of single charge quanta (Single Electron Tunneling, SET) have become favor for implementing electronics at the nano-meter scale.

Single-electron devices may overcome the physical limitations of MOS transistors. MOS exploits the field effect described by classical transport equations for the charge carriers. The finite length of space charge layers, tunneling effects and fluctuations of the doping concentrations, thus limit MOS devices. The single electron devices exploit the Coulomb blockade in very small metallic capacitors, where quantum tunneling through insulating layers is essential. Thus these devices can be made much smaller than MOS transistors [109, 115, 123, 124]. If room temperature operation is considered, typical capacitances should be in the range of 0.1 to 1 attoFarad, corresponding to feature sizes of 1 to 10 nm.

A typical structure of single-electron transistor based on Si quantum dot / nanocrystals is shown in Fig. 2.21. This single-electron device is fabricated based on self-aligned process, which consists of a MOSFET with narrow channel and a Si quantum dot / floating dot embedded between the channel and the gate.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

Fig. 2.21 (a) Schematic diagram of Si single-electron device with self-aligned floating gate, and (b) the cross-section along a'-a line (Extracted from Ref. [109]).

Hysteresis can be observed from the reversible drain current measurements as shown in Fig. 2.22. In contrast, there is no hysteresis effect for the control sample. According to Nakajima et al. [109], the threshold voltage shift can be approximated by

$$\Delta V_t = e / (C_{gc} + C_{gt}) \quad (2.6)$$

where e is the electron charge, C_{gc} is the capacitance between the control gate and the narrow channel wire, and C_{gt} is the capacitance between the control gate and the floating dot.

The discrete increase in the threshold voltage indicating single electron trapping into the Si quantum dot can be observed clearly in single-electron

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

transistor as reported by Wu et al. [123]. This effect is attributed to the Coulomb blockade effect as the second electron needs to have higher charging voltage to overcome the Coulomb energy arising from the first electron trapped in the quantum dot. After each additional electron is trapped, the threshold voltage shifts a certain amount due to the screening of electron. This leads to the step-like threshold voltage shift as shown in Fig. 2.23.

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

Fig. 2.22 Drain current vs gate voltage for (a) and (b) device with floating dot and (c) device without floating dot (Extracted from Ref. [109]).

Chapter 2: Synthesis, characterization, physical properties, and applications of silicon nanocrystal: an overview

Fig. 2.23 Step-like threshold voltage shift of a single-electron device (Re-plotted using data from Ref. [123]).

This chapter has discussed the fabrication and characterization techniques for silicon nanocrystal. Some discussions are provided on the physical properties as well as device applications based on silicon nanocrystal.

Chapter 3

Charge Transport and Charge Decay

In this work, the charging and discharging of silicon nanocrystal (nc-Si) embedded in SiO₂ matrix are explored using the electrostatic force microscopy (EFM) technique. By using this technique, the charging and discharging of nc-Si can be studied down to sub-micrometer regime. It is found that the distribution of nc-Si in the SiO₂ has a significant effect on the total amount of stored charge during the charging process. It is also observed that the charge decay mechanism varies for different distributions of nc-Si in the SiO₂. Detailed discussions of these effects will be presented.

3.1 Overview

The ability to detect charges at the level of a single electron is attracting many researchers' interest and becomes more and more important for nanoscale materials and devices. The use of capacitance-voltage (C-V) measurement is a common method to estimate the amount of stored charge in a material by examining the flatband voltage (V_{fb}) shift after the sample is biased with a constant voltage / pulse voltage for certain durations [125, 126]. However, the total area used in the C-V measurements is relatively large (e.g., $2.5 \times 10^{-9} \text{ m}^2$). In this case, C-V measurements are not able to detect localized storage of a few electrons, and difficult to observe Coulomb blockade phenomena as well as single-electron

Chapter 3: Charge Transport and Charge Decay

tunneling effect due to large area involved. C-V measurements can only give macroscopic device information which represents the averaged property over an area but not the local variation on the nanometer scale. With the introduction of scanning probe techniques, characterization of nanostructure materials (i.e., area of investigation is $< 1 \mu\text{m}^2$), and force imaging of a very small sample's area can make possible. In particular, by using the electrostatic force microscopy (EFM) method, the area of the study can be smaller than $1.0 \times 10^{-12} \text{ m}^2$. This technique has been proven useful for direct imaging of surface potential variations and forces due to storage of charge on the nanometre scale [127]. Compared with conventional C-V measurements, EFM provides better resolution and better data interpretation down to the sub-micrometer scale.

3.2 Atomic Force Microscopy (AFM)

The three most common modes of operation of an atomic force microscopy (AFM) are (a) contact [128], (b) non-contact [127], and (c) intermittent contact or tapping [129]. Each of these three modes can be used for different purposes of investigations. In contact mode operation, the tip of the cantilever is touching the surface of the sample. Surface topography (i.e., surface roughness) is normally measured using this mode of operation. For the non-contact mode operation, surface to bulk sample capacitance and the dc surface voltages can be measured [130]. For tapping mode, the tip of the cantilever is intermittently touching the surface of the sample. Surface topography can be measured using the tapping mode. Damage on the sample's surface during the contacts between the tip and the sample can be reduced by using tapping mode compared to that using the contact

Chapter 3: Charge Transport and Charge Decay

mode. Extensive reviews on the theories and operations of AFM have been done by Hofer et al. [131] and Giessibl et al. [132].

3.2.1 Electrostatic Force Microscopy (EFM)

EFM is a mode of AFM in which the cantilever is connected to an independent voltage source. This independent voltage source is used to create an electrostatic field between the tip and the sample. An electric field is induced between the tip and the sample when the tip is biased with a constant voltage. In the EFM mode there is a small deflection of the cantilever tip caused by the electrostatic force between the conductive tip and region on sample vertically underneath the cantilever tip. It is this deflection which is sensed. When a voltage occurs between a sample and the EFM tip, the electrostatic force F can be written as:

$$F = \frac{1}{2} \frac{dC}{dz} V^2 \quad (3.1)$$

where dC/dz is the first derivative of the tip to sample capacitance with respect to the tip to surface distance z and V is the externally applied potential difference between the tip and the sample. When there is a vertical gradient of the electrostatic force between the tip and the sample, the total capacitance C will change.

EFM is commonly performed in frequency modulation (FM) mode. When the EFM operates in FM mode, the cantilever tip will oscillate at a nominal resonance frequency. When there is an attractive force gradient between the sample and the cantilever tip, the tip is attracted to the sample. Thus, the total resonance frequency of the tip shifts to a lower resonance frequency. When there is

Chapter 3: Charge Transport and Charge Decay

a repulsive force gradient resulting from the sample to the cantilever tip, the tip will repulse further away from the sample. As a result of the repulsive gradient, the resonance frequency of the tip will shift to a higher resonance frequency. This principle is illustrated in Fig. 3.1.

Fig. 3.1 Comparison of the attractive and repulsive forces.

Chapter 3: Charge Transport and Charge Decay

Fig. 3.2 Frequency Modulation (FM) mode for the EFM study (Extracted from Ref. [133]).

The EFM relies on the vertical force gradient from the sample detected at the cantilever tip. The detection of changes in the cantilever resonant frequency is known as frequency modulation (FM). Fig. 3.2 shows the diagram of how the frequency modulation functions and the signal enhancement and feedback allowing gradient detection. This signal will be transferred to the NanoScope software and the force gradient images will be displayed on the screen.

The EFM images were acquired together with the surface topography in a two-pass procedure. In the first pass, a line scan of the sample topography was obtained during normal tapping-mode imaging with no voltage applied to the tip (shown in Fig. 3.3 (1)). During the second pass, the tip was lifted to a distance above the sample surface (i.e., $\sim 10 - 15$ nm), a dc bias was applied to the tip and the lifted tip rescanned above the line traced during the first pass (as shown in Fig. 3.3 (2)). This method is commonly known as lift mode operation. Fig. 3.3 shows

Chapter 3: Charge Transport and Charge Decay

the two-pass operation during the EFM measurements. The topography data are obtained during the first pass, while the electrostatic data are obtained during the second pass measurements. During the EFM measurements, higher the quality factor enhances the data collection and reduces the noise from the tip oscillation.

Fig. 3.3 Lift mode operation during the EFM measurements.

3.3 Probes Selection

To conduct EFM measurements, the EFM probe should be carefully chosen in order to optimize the detection of the weak electrostatic force. The probe should be electrically conductive, have a small spring constant and a high quality factor of oscillation. In general tips used for conventional atomic force microscopy (AFM), usually silicon or silicon nitride are not conductive. For EFM measurements, a conductive tip is necessary while still having a suitable geometry to acquire sample topography data. There are various commercially available probes with different tip radius and sensitivity. In this study, the cantilever tips coated with Pt alloy were obtained from commercial vendors [134] having a resonant frequency of ~ 65 kHz, spring constants of ~ 2 N/m and the radius of ~ 20 nm.

Chapter 3: Charge Transport and Charge Decay

3.4 EFM Characterization of nc-Si

To enable SiO₂ with embedded nc-Si to work as a non-volatile memory device, understanding the charge transport in the material system is indeed important. By using conductive atomic force microscope (AFM) method [135, 136], localized charging effect in nc-Si has been shown to exhibit good charge retention. The charging of Cobalt (Co) nanoclusters and silver nanocrystals has been characterized with electrostatic force microscopy (EFM) recently [137, 138]. The EFM is an accurate tool for the local and nondestructive investigation of nanostructure material. EFM is used to investigate the charge transport in nc-Si due to its potential for probing electrostatic properties with high sensitivity and good spatial resolution [139]. EFM is very sensitive and the electric field due to charges as few as a few electrons (1 to 3) can be measured at room temperature [140-142]. Ultimately, the EFM has proven single-charge detection too [143]. Hence, it is a good tool to study the charge injection, charge decay and charge transport of SiO₂ film embedded with nc-Si.

To study the charge transport of nc-Si embedded in dielectric film, EFM is employed to measure the total force acting on the EFM tip due to the Coulomb interaction between the sample and the EFM tip. During EFM imaging, the tip is scanned over the sample surface with a constant height. The presence of excess charge on the sample gives rise to an image charge on the substrate and on the tip as well. As such, half of the total charge on the dielectric film is reflected on the tip (as shown in Fig. 3.4). The amount of stored charge in nc-Si can be estimated based on the force arising from the Coulomb interactions between the charge Q of the sample and the image charge on the tip. There are many available models to describe the force detected at the cantilever tip due to the different sample structure,

Chapter 3: Charge Transport and Charge Decay

surface effect as well as tip to sample distance and operation modes [15, 138, 144-146]. For example, as pointed out by Melin et al. [143], the model to interpret the force due to the charging of nanocluster on SiO₂ surface is different from the model for a nanocluster embedded inside the SiO₂ film. All the available models in the literature review strongly depend on the structure's composition. In our case, the total electrostatic force on the tip can be written as [29]:

$$F(z) = \frac{1}{\left(z + \frac{d}{\varepsilon}\right)^2} \left(\frac{-\varepsilon_0 A V^2}{2} + \frac{d Q V}{\varepsilon} - \frac{d^2 Q^2}{2 \varepsilon^2 \varepsilon_0 A} \right) \quad (3.2)$$

where z is the distance between the tip and the sample, d is the SiO₂ film thickness, ε is dielectric constant of SiO₂, ε_0 is the permittivity in vacuum, Q is the charges trapped in the nc-Si, A is the area of the charged region and V is the EFM DC bias. The measurement of force is based on the shift in the tip cantilever resonance frequency with respect to its nominal frequency. This shift is related to the Coulomb force gradient detected by the EFM tip and can be written as [130]:

$$\frac{2k\Delta f}{f_0} = \frac{\partial F(z)}{\partial z} \quad (3.3)$$

where Δf is the shift of resonance frequency, f_0 is the nominal frequency, and k is the cantilever spring constant estimated from the lever geometry. The total charge Q is then estimated with the Eqs. (3.2) and (3.3).

Fig. 3.4 Setup for the EFM experiment. Half of the total charges in nc-Si, Q is reflected as image charges ($-\frac{1}{2} Q'$) at the EFM tip.

For the samples used in this study (hereafter known as sample X), nc-Si distributed from the surface to a depth of ~ 20 nm with the peak concentration at a depth of ~ 10 nm as determined from the SRIM simulations. The nc-Si distribution can be represented with an nc-Si surface layer in the SiO_2 film, and the surface layer thickness is ~ 20 nm which is much smaller than the SiO_2 film thickness of 750 nm.

To carry out the study on the charge transport in nc-Si, the sample containing nc-Si must be charged first. In order to charge the nc-Si, charges were injected into the sample via contact-mode EFM. The tip is lowered until the tip is touching the surface of the sample (tip height above the sample surface = 0 nm) and the feedback control of the tip had been disengaged before the voltage was applied. A negative or positive bias is applied to the tip for certain durations with the sample stage grounded. For visualizing the charge inside the nc-Si, tapping-

Chapter 3: Charge Transport and Charge Decay

mode EFM was used to map the total charge variation on the sample. The EFM images were acquired together with the surface topography in a two-pass procedure. In the first pass, a line scan of the sample topography was obtained during normal tapping-mode imaging with no additional dc bias applied to the tip. During the second pass, the tip was lifted to ~ 15 nm above the sample surface. A dc bias ($V = -1$ V) is applied to the tip and lifted tip rescanned above the line traced in the first pass. This magnitude of -1 V was chosen so that no additional charging effect will occur during the mapping of the charge cloud on the sample. As the tip moved along the sample at a fixed height (z), it responds to the presence of electrostatic forces from the sample. The Coulomb forces between these charges and the tip caused a resonant frequency shift in the cantilever oscillation. During the second pass measurements, there will be a peak in the electrostatic data when there are charges in the specific area of the sample. In the rest of this chapter, only the EFM images are shown as the shift of the resonance frequency is interested but not the surface topography.

Chapter 3: Charge Transport and Charge Decay

3.5 Voltage dependence of the charging effect

Fig. 3.5 shows EFM images of pure SiO₂ and the SiO₂ with nc-Si after the application of either -4 V or +4 V for 10 s. The virgin sample with nc-Si before the voltage biasing is shown in Fig. 3.5a. Localized charging of the samples with nc-Si is evident from the dark spot Fig. 3.5b or a bright spot Fig. 3.5c in the EFM images. In contrast, the pure SiO₂ does not exhibit any charging effect Fig. 3.5d. Both the pure SiO₂ sample and the virgin sample with nc-Si do not have any bright or dark spot, indicating no charge trapping. The dark spot reflects a total positive charge while the bright spot reflects a total negative charge. The size of the spots (i.e., the charges deposited on the SiO₂ film with nc-Si) was ~250 nm in diameter. The EFM image of the charges appears as a protrusion on the surface due to the electrostatic interaction between the image charge on the grounded tip and the charge in the sample.

If the voltage biased at the tip varies but the voltage bias time is fixed, different amount of charges will be stored on the nc-Si. This phenomena is shown in Fig. 3.6. Total charges are calculated based on Eq. (3.2) and Eq. (3.3). As shown in this figure, a higher positive voltage bias induced more charges (Q) in nc-Si and the number of positive charges deposited increased linearly with the positive voltage applied. For negative voltage applied, the higher the negative voltage, the larger the number of negative charge ($-Q$) will be stored in the nc-Si. The number of negative charges deposited also increased linearly with the negative voltage applied. The voltage effect can be also observed in the 3D EFM images of the initial charges deposited as a function of voltage bias. A larger convex bright spot is observed for the sample charged with larger negative voltage while a larger concave spot is observed for the sample charged with larger positive voltage.

Chapter 3: Charge Transport and Charge Decay

Fig. 3.5 EFM images. (a) uncharged nc-Si sample; (b) nc-Si sample charged at +4 V; (c) nc-Si sample charged at -4 V; and (d) SiO₂ sample (i.e., without nc-Si) charged at +4 V.

Chapter 3: Charge Transport and Charge Decay

Fig. 3.6 3D EFM images of initially deposited charge as a function of voltage bias.

Chapter 3: Charge Transport and Charge Decay

3.6 Visualizing charge transport in silicon nanocrystal

To understand the charge transport in nc-Si, charge decay from the dielectric film is monitored with a series of snap shots of EFM images recorded in real time after constant voltage injection. The contrast of the bright or dark spots observed in the EFM image diffuses over time, as shown in Fig. 3.7, indicating dissipation of the injected charge. After a long time, the contrast disappeared indicating that the trapped charge decays to the background level. The charge dissipation is also evident from the reduction of the resonance frequency shift. The dissipation of the trapped charges is actually due to the diffusion of the trapped charges to the neighboring uncharged nc-Si in the surrounding area. The charge diffusion leads to the increase in the area of the charge cloud (i.e., the area of the charged spot) together with the reduction in the brightness (or darkness) of the charged spot. One typical example is shown in Fig. 3.8. The increase of the area of the bright spot (electron trapping) with time can be clearly seen in this figure. At the same time, there is a reduction in the brightness of the spot with time. This is due to the charge diffusion from the charged nc-Si to the surrounding uncharged nc-Si. A wider charge cloud is observed with a reduction in the brightness of the charging spot. The increase in the charging spot size shows that charges diffuse from charged nc-Si to the surrounding uncharged nc-Si. At the same time, reduction in the resonance frequency during decay indicates a reduction in the total charges. To further investigate the transport of charges within nc-Si, the initial charge was dissipated to the background level before a new bias was applied on the same spot. An increased in the total charge cloud area after the 2nd bias has been observed. This shows that the previous charge trapping in nc-Si is still significant.

Chapter 3: Charge Transport and Charge Decay

Fig. 3.7 EFM images of decay of charge trapped in nc-Si.

Fig. 3.8 Increase of the area of the charge cloud due to charge diffusion.

Chapter 3: Charge Transport and Charge Decay

3.7 Influence of neighboring charges

To study the influence of neighboring charges on the charge decay, one charged spot, two charged spots with a spacing of 300 nm, and three charged spots on a straight line with a spacing of 300 nm were created. For the cases of 2 charged spots, the charge in one spot has the sign (positive or negative) either the same as or opposite to that of another spot. For the cases of 1 and 3 charged spots, each spot is negatively charged. Such arrangement can give us a clear picture of the influence of neighboring charges on the charge diffusion. To have quantitative information of charge decay, the charge Q was determined with Eqs. (3.2) and (3.3), and the charge decay with time is shown in Fig. 3.9.

Firstly, the influence of the neighboring charges with the same charge sign has been studied by applying -4 V bias for 10 s for each spot to create 1 to 3 charged spots, and the results are shown in Fig. 3.9a. Note that for the negative bias each spot is negatively charged. As shown in Fig. 3.9a, the charge decay for the all cases is found to follow the exponential law

$$Q(t) = Q_o \exp\left(-\frac{t}{\tau}\right) \quad (3.4)$$

where Q_o is the initial charge, t is the time after charge injection, and τ is the characteristic decay time. The characteristic decay time is 310, 346 and 657 s for 1, 2, and 3 charged spots, respectively. The increase in the characteristic decay time with the spot number clearly shows the blockage of charge diffusion by the neighboring charges with the same sign. In contrast, the neighboring charge with opposite sign can speed up the charge decay. As shown in Fig. 3.9b, in the case of 2 charged spots, one spot is negatively charged at -4 V for 10 s (the bright spot), and the other spot is positively charged (the dark spot), and the charge decay

Chapter 3: Charge Transport and Charge Decay

measurement is conducted for the negatively charged spot. For comparison, the charge measurement is also conducted for the 1-spot case in which the spot is negatively charged at -4 V for 10 s. As can be seen in Fig. 3.9b, the characteristic decay time for the 2-spots case is 256 s, which is significantly shorter than that of the 1-spot case (310 s). This indicates that the charge neutralization caused by the neighboring charge with opposite sign leads to a faster decay of the trapped charge. Fig. 3.9c shows the charge-charge interaction model, in which the negative charge-negative charge interaction has longer decay characteristic, while negative charge-positive charge interaction has shorter decay characteristics. This figure clearly shows that charge-charge interaction affects the charge decay characteristic significantly.

Fig. 3.9 (continue next page)

Fig. 3.9 (a) Blockage of charge diffusion by neighboring charges with the same charge sign; (b) acceleration of charge diffusion by neighboring charges with the opposite sign; and (c) decay time as a function of both the number and charge sign of the neighboring charged spots. "+" represents positive charge while "-" represents negative charge.

3.8 Effect of nanocrystal's depth distributions on charge injection and charge decay

In order to study the effect of nanocrystal's depth distributions, two samples with different nanocrystal depth profiles are prepared. Fig. 3.10a shows the nc-Si distributions in SiO₂ matrix for the two samples obtained from the SRIM simulations. The peak concentrations of nc-Si are located very close to the SiO₂ surface (hereafter known as sample A) and at the depth of ~16 nm underneath the surface (hereafter known as sample X), respectively. For sample X, most of the nanocrystals distribute in the region of ~5 – 30 nm underneath the SiO₂ surface. To inject charges into these nanocrystals, the charges need to overcome the barrier of SiO₂ with a distance of at least 5 nm. In contrast, for sample A, most of the nanocrystals distribute from the surface to a depth of ~20 nm with its peak concentration located very close to the surface, and thus charge injection is much easier to occur. Therefore, for a given charge injection time, the injected charge number of sample A should be larger than that of sample X. As the injected charges will diffuse into neighboring uncharged nc-Si, the size of the injected charge cloud of sample A should be also larger than that of sample X. These situations are illustrated in Fig. 3.10b, and they have been confirmed in this experiment and will be discussed further.

Fig. 3.10 a) nc-Si distributions in SiO₂ film; and (b) schematic illustration of charge injection from the EFM tip to the nc-Si and charge diffusion through the nc-Si.

Chapter 3: Charge Transport and Charge Decay

The 3D EFM images of sample X and sample A as a function of decay time after the injection at -4 V for 10 s is shown in Fig. 3.11. The size (i.e., the diameter) of charge cloud can be determined from pseudo-voigt fitting to the shift of the resonance frequency versus the position obtained from the EFM measurement based on 10 % of the peak height, as shown in Fig. 3.12a. The decay time dependence of the size of the charge cloud for the two samples is shown in Fig. 3.12b. For sample A, the size of the charge cloud does not change with the decay time and is $\sim 1.25 \mu\text{m}$ for decay time longer than 3 minutes. Therefore, the initial size of the charge cloud (i.e., when decay time = 0) is expected to be $\sim 1.25 \mu\text{m}$. For sample X, the size of charge cloud increases with the decay time linearly. The linear relationship indicates that the speed of the lateral charge diffusion is constant. The initial size of the charge cloud for sample X can be estimated from the linear relationship with decay time = 0, and it is $0.54 \mu\text{m}$ as mentioned early. The influence of the nc-Si distribution on the size of charge cloud can be clearly seen in Fig. 3.12b. The size for sample X is smaller than that for sample A. However, it increases with decay time linearly. In contrast, the size for sample A does not change with decay time. These results are explained in the following. For sample A with most of the nanocrystals distributing in the surface region, lateral charge diffusion occurs easily during the charge injection, leading to a larger charge cloud; however, after the injection, there is no more lateral diffusion as the injected charges can easily dissipate on the surface, and thus the size of the charge cloud remains unchanged during the decay period. For sample X with most of the nanocrystals distributing in the region at least $\sim 5 \text{ nm}$ away from the surface, the charge injection is relatively difficult, and thus the charge cloud is smaller; after

Chapter 3: Charge Transport and Charge Decay

the injection, the injected charges diffuse in all directions, leading to the increase in the size of the charge cloud with decay time.

Fig. 3.11 3D EFM images taken at various time after charge injection for sample A and sample X.

Chapter 3: Charge Transport and Charge Decay

Fig. 3.12 (a) Determination of the size of charge cloud from the pseudo-voigt fittings to the experimental data of the resonance-frequency shift versus position; and (b) Size of charge cloud as a function of decay time. The charge injection is carried out at -4 V

Chapter 3: Charge Transport and Charge Decay

The charge decay characteristics for sample X and sample A after the injection at -4 V for 10 s is shown in Fig. 3.13. As shown in Fig. 3.13, the charge decay follows an exponential law, i.e., $Q(t) = Q_0 \exp(-t/\tau)$ where Q_0 is the initial charge (i.e., the injected charge), τ is the characteristic decay time and t is the time after charge injection. The fitting to the experimental data of charge versus decay time with the exponential law yields the initial charge (Q_0) and the characteristic decay time (τ). The initial charge is 84 electrons for sample X and 1103 electrons for sample A, while the characteristic decay time is 310 s for sample X and 155 s for sample A. The initial charge of sample A is much larger than that of sample X, indicating that the charge injection into sample A is easier and more efficient; however, the characteristic decay time of sample A is shorter than that of sample X, which can be explained by the easy charge dissipation on the surface of sample A. The reason for these results is that in sample A, the existence of a large amount of nc-Si in the surface region made the charge injection easier, and exposing the nc-Si in air (i.e., humid environment) speeded up the charge dissipation. These results are consistent with the above discussions on the sizes of the charge clouds.

The difference in the total decay time of sample X and sample A can be interpreted as a consequence of Coulomb blockade energy for charging the nc-Si. For a negative trapped charge to tunnel out from a nc-Si in sample X, the negative charge must overcome a potential barrier of $\Phi_X = \Phi_{nc} - e\chi_{SiO_2} - E_o$, where Φ_{nc} is the nc-Si potential barrier, χ_{SiO_2} is the SiO₂ affinity and $E_o = e^2/(2C_{nc})$ is the single-electron charging energy of nc-Si. The situation is different for sample A, where there is no SiO₂ potential barrier to be overcome. The negative charge only

Chapter 3: Charge Transport and Charge Decay

need to overcome a potential barrier of $\Phi_A = \Phi_{nc} - E_o$. The decay τ dependant to the tunneling probability $T \sim \exp(-2d \frac{\sqrt{2me\Phi}}{\hbar})$, where Φ is the potential barrier needed to overcome, and d is the barrier thickness [137]. In the present case, Φ_A is larger than Φ_X . Thus the characteristic decay time for sample X is larger than that of sample A.

Fig. 3.13 Charge decay characteristics for sample X and sample A. The initial charge (Q_0) and the characteristic decay time (τ) can be obtained from the fitting based on $Q(t) = Q_0 \exp(-t/\tau)$.

Similarly to the experiment shown in section above [3.7], the influence of neighboring charges on the charge decay is very significant. One additional charge cloud close to the charge cloud under test (i.e., the EFM measurement is conducted

Chapter 3: Charge Transport and Charge Decay

on this charge cloud) is being created. The charge cloud under test is negative and is formed by the charge injection at -4 V for 10 s; while the additional charge cloud is either negative or positive and is formed by the charge injection at -4 V or $+4$ V for 10 s, respectively. As pointed out earlier, the initial size of the charge cloud under test just after the charge injection are ~ 1.25 μm and ~ 0.54 μm for sample A and sample X, respectively. Therefore, the center of the additional charge cloud is set to locate ~ 1 μm and ~ 0.3 μm away from the center of the charge cloud under test for sample A and sample X, respectively. Note that the time interval between the end of charge injection of the charge cloud under test and the start of the charge injection of the additional charge cloud is ~ 2 s, which is too short to have a significant impact on the decay study. The influence of the neighboring charges on the characteristic decay time is shown in Fig. 3.14. For sample X, a negative or positive neighboring charge leads to a longer or shorter characteristic decay time, respectively. This means that the negative neighboring charge resists the charge dissipation of the negative charge cloud under test while the positive neighboring charge accelerates the charge dissipation. However, for sample A, the neighboring charges have no significant influence on the charge decay. The difference between the two samples is consistent with the early discussions on the influence of the nc-Si distribution on the charge diffusion. For sample A, as mentioned earlier, there is no lateral charge diffusion during the decay period because the injected charges can easily dissipate on the surface, and therefore the neighboring charges have no significant influence on the charge decay. For sample X, there is a strong lateral charge diffusion during the decay period. As the neighboring charges can either accelerate or resist the lateral charge diffusion, they have a significant influence on the charge decay.

Fig. 3.14 Influence of neighboring charges on the characteristic decay time.

The charging and discharging of silicon nanocrystal (nc-Si) embedded in SiO_2 matrix has been explored using the EFM technique. Detailed discussions on the charge decay characteristics have been presented in this chapter.

Chapter 4

Static Dielectric Constant of Silicon Nanocrystal

The introduction of silicon nanocrystal into SiO_2 matrix will definitely affect the material properties as well as the electrical properties. In this chapter, it is observed that the introduction of silicon nanocrystal will affect the total capacitance of the Metal-oxide-semiconductor (MOS) structure. By using Maxwell-Garnett effective medium approximation (EMA) approach, the influence of the nanocrystal distributions, volume fraction as well as the dielectric constant will affect the total capacitance of the structure. Detail discussions are provided on the approach used in this study as well as the comparison of the result with other theoretical calculations. Some discussions are provided for the reduction of the static dielectric constant of nanocrystalline silicon.

4.1 Motivation

It is observed that the total capacitance for the sample implanted with nanocrystal is slightly larger than that compared to a sample without nanocrystal. Fig. 4.1 shows the increment of total capacitance at strong accumulation for the MOS structures with and without the nc-Si distributed in the oxide. Ng et al. has observed the increase of capacitance at accumulation during the investigation of ion-beam synthesized Si nanocrystal in SiO_2 [147]. As can be seen in this figure, the inclusion of the nc-Si in the oxide leads to a significant increase in the MOS

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

capacitance (i.e., the capacitance under strong accumulation). This indicates that the dielectric constant of the nc-Si is larger than the dielectric constant of SiO₂. Besides the increase in the capacitance, Fig. 4.1 also shows that the inclusion of the nc-Si leads to a flatband voltage shift. The shift is due to the charge trapping in the nc-Si during the C-V measurement and the difference in the work function between the nc-Si and the SiO₂. These effects will not be discussed in this thesis.

Fig. 4.1 Comparison of C-V characteristics between the MOS structures with and without the nc-Si embedded in the oxide. The both structures have identical oxide thickness.

4.2 Introduction

In recent years, research on silicon nanocrystal (nc-Si) embedded in SiO₂ thin film has been carried out intensively due to its potential applications in memory devices as well as opto-electronic devices. An example of optoelectronic device is the Si light emitting diode (LED) based on Si nanocrystal. The Si LED will be used in Si optoelectronic integrated circuits for inter- and intra-chip data

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

communications. One promising technique for incorporating nc-Si into SiO₂ is to use Si ion implantation followed by high temperature annealing. With this technique the nc-Si synthesis is fully compatible with the mainstream complementary metal-oxide-semiconductor (CMOS) process and the distribution of the nc-Si can be easily controlled as discussed in Chapter 2. When the nc-Si is embedded in the SiO₂ film, the dielectric properties of the film will be different from that of the pure SiO₂ film. Therefore, for flash memory devices with the nc-Si embedded in the gate oxide [40, 148, 149], the inclusion of the nc-Si will definitely affect the gate capacitance. The effect of the nc-Si on the MOS capacitance has been observed experimentally [147]. The change in the MOS capacitance due to the influence of the nc-Si will then affect the device's electrical characteristics. Obviously, a precise knowledge on the influence of the nc-Si on the MOS capacitance is very useful in the design and modeling of the memory devices. However, a quantitative study on the influence of the nc-Si on the gate capacitance is still lacking. On the other hand, as the nc-Si is an isolated nanoscale structure with a size of less than ~5 nm embedded in the SiO₂ matrix, its physical properties should be different from that of bulk crystalline Si. Thus, understanding the dielectric properties of the nc-Si is undoubtedly important to the fundamental physics. In addition, if the dielectric properties of the nc-Si are known, the dielectric properties of a SiO₂ thin film containing the nc-Si can also be obtained based on an appropriate effective medium approximation (EMA), and the information is useful to the device applications of the nc-Si.

In this chapter, an approach to the calculation of the MOS capacitance for any nc-Si distribution in the gate oxide for the circumstances that the nc-Si does not form conductive percolation tunneling paths connecting the gate to the

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

substrate [36] has been developed. The approach is based on the calculation of the effective dielectric constant of the gate oxide in the nc-Si distributed region with a sub-layer model of nc-Si distribution and the Maxwell-Garnett effective medium approximation (EMA). The MOS capacitance calculated using this approach has been compared to the capacitance measurement for a number of samples with various gate oxide thicknesses, implantation energies and dosages, and an excellent agreement has been achieved for all the samples. A detailed picture of the influence of implantation energy and implantation dosage on the MOS capacitance has been obtained.

4.3 Distribution of nanocrystal inside the SiO₂

The distribution of the nc-Si in the gate oxide can be obtained from the Stopping and Range of Ions in Matter (SRIM) simulation or from the Secondary Ion Mass Spectroscopy (SIMS) measurements. There are two cases of nc-Si distribution in the gate oxide: partial and full distributions in the gate oxide. For the partial distribution, the oxide can be divided into two regions, the nc-Si distributed region and the pure SiO₂ region (i.e., without nc-Si). One example of the partial distribution which has been achieved with the ion implantation energy of 2 keV for a 30 nm gate oxide is shown in Fig. 4.2a. For the full distribution, nc-Si is distributed in the entire gate oxide. Note that for the full distribution the nc-Si concentration should not be too high to avoid the formation of conductive percolation tunneling paths connecting the gate to the substrate. The electrical characteristics of such structure will be discussed in Chapter 5. Fig. 4.2b shows one example of the full distribution achieved with the ion implantation energy of 8 keV for a 30 nm gate oxide. The SRIM simulation shows that for a 30 nm gate

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

oxide that the full distribution can be achieved with implantation energy higher than 7 keV.

Fig. 4.2 nc-Si distribution in a 30 nm gate oxide obtained from SRIM simulation. (a) Partial distribution under the ion implantation energy of 2 keV; and (b) full distribution under the implantation energy of 8 keV.

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

4.4 Effective Medium Approximation (EMA) method

As mentioned earlier, the distribution of the implanted nc-Si can be obtained from the SRIM profile. From the nc-Si SRIM profile, the depth distribution of the nc-Si volume fraction in the SiO₂ can be obtained. The volume fraction can be expressed as:

$$v(x) = \frac{QI(x)}{N_{Si} \int_0^{d_{max}} I(x) dx} \quad (4.1)$$

where Q is the dosage of implanted Si ions, N_{Si} is the silicon density, d_{max} is the maximum depth of the Si implantation profile (i.e., the width of the nc-Si distributed region. Note that d_{max} is equal to the gate oxide thickness for the case of full distribution), and $I(x)$ is the Si SRIM intensity. The information of the volume fraction is required for the calculation of the effective dielectric constant of SiO₂ containing nc-Si, as discussed below.

As the nc-Si volume fraction varies with the depth in the oxide, the effective dielectric constant of the oxide is not uniform and should vary with the depth also. The nc-Si distributed region (note that its width is equal to d_{max} of Eq. (4.1)) can be virtually divided into m ($m = 30, 40$, and 100 for $30, 40$, and 100 nm of SiO₂ thickness, respectively, in the present study.) sub-layers with equal thickness of $\frac{d_{max}}{m}$ nm (namely sub-layer 1, sub-layer 2,..., sub-layer m) starting from the surface to the depth of d_{max} as shown in Fig. 4.3. The nc-Si volume fraction within a sub-layer is approximately constant. Thus the effective dielectric constant, ϵ_i ($i = 1, 2, \dots, m$) of the i^{th} sub-layer can be calculated with the Maxwell-Garnett effective medium approximation (EMA), as given by [84, 99, 150-152]

$$\frac{\epsilon_i - \epsilon_{SiO2}}{\epsilon_i + 2\epsilon_{SiO2}} = v_i \frac{\epsilon_{nc-Si} - \epsilon_{SiO2}}{\epsilon_{nc-Si} + 2\epsilon_{SiO2}} \quad (4.2)$$

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

where v_i ($i = 1, 2, \dots, m$) is the volume fraction of the nc-Si in the i^{th} sub-layer, ϵ_{nc-Si} is the static dielectric constant of nc-Si, and ϵ_{SiO_2} is the dielectric constant of pure SiO_2 .

Fig. 4.3 Sub-layer model used in the studies for partial distribution (a) and full distribution (b) of nc-Si in the gate oxide.

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

After determining the dielectric constant of the nc-Si, the effective dielectric constant ε_i ($i = 1, 2, \dots, m$) of each sub-layer of the nc-Si distributed region can be calculated with Eq. (4.2). With the depth distribution of the effective dielectric constant taken into account, the MOS capacitance in the accumulation regime is calculated, as described below. For the case of partial nc-Si distribution in the gate oxide as shown in Fig. 4.3a, the MOS capacitance (C) per unit area can be expressed as

$$\frac{1}{C} = \sum_{i=1}^m \left[\frac{m\varepsilon_i\varepsilon_0}{d_{\max}} \right]^{-1} + \left[\frac{3.9 \times \varepsilon_0}{T_{\text{oxide}} - d_{\max}} \right]^{-1} \quad (4.3)$$

where T_{oxide} is the gate oxide thickness, and ε_0 is the permittivity in vacuum. On the other hand, for the case of full nc-Si distribution in the gate oxide as shown in Fig. 4.3b, the MOS capacitance is given by

$$\frac{1}{C} = \sum_{i=1}^m \left[\frac{m\varepsilon_i\varepsilon_0}{T_{\text{oxide}}} \right]^{-1} \quad (4.4)$$

It should be pointed out that the above calculations of the MOS capacitance (i.e., Eqs.(4.3) and (4.4)) are valid only for the circumstances that the nanocrystals themselves are not charged and discharged in response to the small AC signal applied during a capacitance measurement. If there is a high concentration of nanocrystals distributed throughout the gate oxide, these nanocrystals can form conductive percolation tunneling paths connecting the substrate to the gate [38]. Thus they can be charged and discharged easily under the influence of the AC signal. In this case, a nanocrystal acts like a capacitor, and therefore the MOS capacitance should be calculated based on an equivalent circuit that takes the contribution of the nanocrystal capacitance into account [36].

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

As the volume fraction (v_i) of nc-Si in each sub-layer and ϵ_{SiO_2} are known, the dielectric constant (ϵ_i) of each sub-layer can be calculated with Eq. (4.2) for a given $\epsilon_{\text{nc-Si}}$, and then the MOS capacitance (C) can be calculated with Eq. (4.4) (note that the distribution of nc-Si is a full distribution for this sample). Fig. 4.4 shows the calculated MOS capacitance as a function of $\epsilon_{\text{nc-Si}}$ which varies from 3.9 (dielectric constant of SiO_2) to 11.9 (dielectric constant of bulk crystalline silicon). As can be seen in this figure, the capacitance increases with the $\epsilon_{\text{nc-Si}}$. From the curve of the capacitance versus the $\epsilon_{\text{nc-Si}}$ shown in Fig. 4.4, one can easily find the value of $\epsilon_{\text{nc-Si}}$ corresponding to the measured MOS capacitance of the structure with the nc-Si distributed in the oxide. The value obtained is 9.8, and it is actually the dielectric constant of the nc-Si embedded in the oxide. As expected, the dielectric constant of the nc-Si is much larger than that of pure SiO_2 but significantly smaller than that of bulk crystalline Si.

Fig. 4.4 Calculated MOS capacitance as a function of ϵ_{nc-Si} . The intercept between the calculated and the measured capacitance yields the dielectric constant of the nc-Si embedded in the SiO_2 .

4.5 Influence of implantation energy and dosage

Fig. 4.5 also shows the influence of implantation energy on the MOS capacitance. The capacitance is calculated at various implantation energies ranging from 1 keV to 11 keV for the fixed implantation dosage of $1 \times 10^{16} \text{ cm}^{-2}$ and the gate oxide thickness of 30 nm. According to the SRIM output, 30 nm gate oxide with partial distribution that corresponds to implantation energies lower than 7 keV, while the full distribution is achieved with implantation energies higher than 7 keV. For the partial distribution, as the implantation energy increases, the width (d_{max}) of the nc-Si distributed region increases, but the effective dielectric constant, ϵ_i ($i = 1, 2, \dots, m$) decreases as the nc-Si volume fraction (v_i) decreases when d_{max} increases for a constant implantation dosage. Thus the overall effect of implantation energy on the MOS capacitance for the partial distribution is that the MOS capacitance

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

first decreases with the implantation energy and then it increases slowly when the energy is larger than ~ 2 keV, as shown in Fig. 4.5. For the full distribution, when the implantation energy is larger than 7 keV, some of the Si ions are implanted into the Si substrate, and thus the effective dielectric constant, ϵ_i ($i = 1, 2, \dots, m$) decreases as the nc-Si volume fraction (v_i) decreases with the implantation energy. Therefore, as given by Eq. (4.4), the MOS capacitance decreases with the implantation energy. This is also depicted in Fig. 4.5.

Fig. 4.5 Influence of Si⁺ implantation energy on the MOS capacitance. The gate oxide thickness is 30 nm, and the implantation dosage is $1 \times 10^{16} \text{ cm}^{-2}$.

Fig. 4.6 shows the MOS capacitance calculated with Eq. (4.4) as a function of the implantation dosage. The gate oxide thickness is 30 nm, the implantation energy is fixed at 8 keV which corresponds to the full distribution, and the ϵ_{nc-Si} value used is 9.7. For comparison, the measured MOS capacitances for the implantation dosages of $3 \times 10^{14} \text{ cm}^{-2}$, $2 \times 10^{15} \text{ cm}^{-2}$ and $1 \times 10^{16} \text{ cm}^{-2}$ are also

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

included in Fig. 4.6. As can be seen in the figure, there is a good agreement between the calculation and the measurement. Fig. 4.6 shows that the MOS capacitance increases with the implantation dosage and the increase becomes significant when the dosage is higher than $\sim 3 \times 10^{14} \text{ cm}^{-2}$. The increase of the MOS capacitance is due to the increase of the effective dielectric constant as a result of the increase in the nc-Si volume fraction with the dosage.

Fig. 4.6 Influence of Si^+ dosage on the MOS capacitance. The gate oxide thickness is 30 nm, and the implantation energy is 8 keV.

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

4.6 Comparison with theoretical calculation

The screening dielectric constant of nc-Si can be theoretically calculated with the formula below [119]:

$$\varepsilon_{nc-Si}(D) = 1 + \frac{\varepsilon_b - 1}{1 + \left(\frac{1.38}{D}\right)^{1.37}} \quad (4.5)$$

where ε_b is the dielectric constant of bulk crystalline silicon (note that in ref. [119], the two constants, 1.37 and 1.38 used in Eq. (4.4) are obtained under the assumption of $\varepsilon_b = 11.4$. This ε_b value is slightly different from the widely-used value, 11.9 (ref. [153])) and D is the diameter of nc-Si in the unit of nm. Fig. 4.7 shows the cross-section TEM measurements of the sample embedded with nc-Si for both the partial and full distribution. The mean nc-Si size is 4.5 nm as determined from the x-ray diffraction (XRD) measurement and TEM measurements. The ε_{nc-Si} calculated with Eq. (4.5) is 9.7 under the assumption of $D = 4.5$ nm. This ε_{nc-Si} value is consistent with that from the optical study reported in ref. [18]. Most importantly, the calculated MOS capacitance based on this ε_{nc-Si} value is in excellent agreement with the measured capacitance, indicating that the ε_{nc-Si} value is correct.

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

Fig. 4.7 TEM image of nc-Si embedded in a 30 nm gate oxide. (a) Partial distribution under the implantation energy of 2keV; and (b) full distribution under the implantation energy of 10 keV.

Table 4.1 summarizes the comparison between the measured capacitance and the capacitance calculated using $\epsilon_{nc-Si} = 9.7$ with Eq. (4.3) for the partial distribution or Eq. (4.4) for the full distribution. The agreement between the measurement and the calculation can easily be described by the ratio $R = \text{calculated capacitance} / \text{measured capacitance}$. As can be seen in the table, the R

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

value is very close to 1 (in the range from 0.982 to 1.002) for all the samples. This indicates that the calculation is in excellent agreement with the measurement.

Table 4.1 Comparison between the measured and calculated MOS capacitance for various samples. The calculation is based on Eq. (4.3) for the partial distribution and Eq. (4.4) for the full distribution.

nc-Si distribution	SiO ₂ thickness (nm)	Implantation energy (keV)	Dosage (cm ⁻²)	Measured capacitance (F/m ²)	Calculated capacitance (ε _{nc-Si} =9.7) (F/m ²)	$R = \frac{\text{calculated cap.}}{\text{measured cap.}}$
Partial distribution	30	2	1×10 ¹⁶	1.209×10 ⁻³	1.209×10 ⁻³	1.000
	30	5	1×10 ¹⁶	1.211×10 ⁻³	1.211×10 ⁻³	1.000
	100	28	8×10 ¹⁶	3.907×10 ⁻⁴	3.913×10 ⁻⁴	1.002
Full distribution	30	8	3×10 ¹⁴	1.153×10 ⁻³	1.153×10 ⁻³	1.000
	30	8	2×10 ¹⁵	1.169×10 ⁻³	1.163×10 ⁻³	0.995
	30	8	1×10 ¹⁶	1.209×10 ⁻³	1.21×10 ⁻³	1.001
	30	10	3×10 ¹⁶	1.335×10 ⁻³	1.328×10 ⁻³	0.995
	40	18	5×10 ¹⁶	1.033×10 ⁻³	1.014×10 ⁻³	0.982

It is obvious from the above discussions that the dielectric constant of nc-Si is significantly reduced from its bulk value. There are a number of studies on the reduction of the dielectric constants of nanoscale systems [118, 119, 122, 154, 155]. Originally, the reduction in the dielectric constant of small quantum dots (such as the nanocrystal here) was attributed to the bandgap increase inside the quantum dots. However, it was only recently argued by Delerue et al. [122] that the reduction is due to the breaking of polarizable bonds at the surface and is not due to the opening of the bandgap induced by the confinement. This argument is supported by the following two latest studies [156, 157]. Based on the first-

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

principle calculation of the microscopic dielectric response function for quantum dots, Cartoixà et al. [156] have found that the reduction of the macroscopic dielectric constants is a surface effect. Giustino et al. [157] have also shown that for Si slabs of finite size the decrease of the permittivity with slab thickness is related to surface rather than bulk effects.

4.7 Effective dielectric constant

The EMA method has been proven to be reliable in predicting the dielectric constant of nc-Si embedded in SiO₂ matrix. It is also clear from the above discussions that the increase in the MOS capacitance is due to the increase in the effective dielectric constant of the gate oxide as a result of the introduction of the nc-Si into the gate oxide. As the nc-Si volume fraction is a function of the depth, the effective dielectric constant varies with the depth also. The depth distribution of the effective dielectric constant in the gate oxide was calculated based on Eq. (4.2). Fig. 4.8 shows the effective dielectric constant as a function of the depth in a 30 nm gate oxide for the partial distribution (Fig. 4.8a) and the full distribution (Fig. 4.8b). For the case of partial distribution, the sample was implanted with $1 \times 10^{16} \text{ cm}^{-2}$ of Si⁺ at 2 keV. There is a large increment of 1.12 in the effective dielectric constant at the peak position of the nc-Si distribution as compared to the dielectric constant of pure SiO₂. The effective dielectric constant is the same as the dielectric constant (3.9) of pure SiO₂ when the depth is larger than ~15 nm as there is no nc-Si in the region. For the case of full distribution, the sample was implanted with $1 \times 10^{16} \text{ cm}^{-2}$ of Si⁺ at 8 keV. The effective dielectric constant at the peak position of the nc-Si distribution is larger than the dielectric constant of pure SiO₂

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

by 0.36. For both the partial and full distributions, the depth distribution of the effective dielectric constant approximately follows the nc-Si distribution.

Fig. 4.8 Depth distribution of the effective dielectric constant of the gate oxide. (a) Partial distribution under the implantation energy of 2 keV; and (b) full distribution under the implantation energy of 8 keV.

4.8 Influence of SiO₂ thickness

The influence of SiO₂ thickness on the MOS capacitance with and without nc-Si is shown in Fig. 4.9. The ϵ_{nc-Si} is fixed at 9.7 assuming the size of the nc-Si is always a constant value of ~ 4.5 nm. The volume fraction of the nc-Si is also assumed to be a constant. When the SiO₂ thickness is 16 nm, it is observed that there is a difference of 2.13×10^{-4} F/m² between the capacitance of pure SiO₂ and the capacitance of SiO₂ embedded with nc-Si. As the SiO₂ thickness increases, the difference in the MOS capacitances reduces. This is mainly due to the increase of T_{oxide} but no changes in the capacitance of the nc-Si + SiO₂ layer. Even though the variation in MOS capacitance is small, this effect cannot be neglected. For example, when the SiO₂ thickness is 30 nm, there is still a 5.7×10^{-5} F/m² difference between the SiO₂ and the SiO₂ with nc-Si. Such differences will become more significant when the nc-Si dosage increases.

Fig. 4.9 Total MOS capacitance of SiO₂ film with and without nc-Si as a function of different SiO₂ thickness. As the SiO₂ thickness increases, the capacitance difference between SiO₂ with and without nc-Si reduces.

Chapter 4: Static Dielectric Constant of Silicon Nanocrystal

This model is not valid for the sample embedded with nc-Si distributed throughout the entire SiO_2 with very high concentration of nc-Si [36-38]. For this nc-Si distributed throughout the entire SiO_2 , there are many nc-Si tunneling paths connected between the surface of the SiO_2 to the Si substrate. Charges can easily tunnel through these nc-Si tunneling paths and respond to the ac signal during the C-V measurements, leading to large increment in the total measured capacitance. A detailed discussion on the electrical characteristics of such structure is presented in section 5.3.

This chapter has investigated the static dielectric constant of nc-Si embedded in SiO_2 matrix by using EMA method. This method is proven reliable by comparing the results with other theoretical calculations. Indeed, the introduction of nc-Si in the SiO_2 affects the effective dielectric constant of the film and the total capacitance of the film.

Chapter 5

Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

The electrical characteristics of two different distributions of silicon nanocrystals in SiO₂ thin films are investigated. In the first case, there is a single layer silicon nanocrystal synthesized by very low energy ion implantation. The distribution of nanocrystal is located very close to the SiO₂ surface. The electrical properties (i.e., flatband voltage shift) under different annealing temperature, annealing durations and temperature ramping rates are investigated. From the flatband voltage shift, the total remaining Si ions trapped in the sample can be deduced. The memory characteristics of this single layer nanocrystal close to the SiO₂ surface are also investigated. This simplified structure exhibit memory effect with positive and negative charge trapping characteristics. The structure is found to be a good candidate for memory device applications with good charge retention up to 10⁵ s. In the second case, the silicon nanocrystal is distributed throughout the entire SiO₂ thin film. Some interesting phenomena (i.e., large capacitance and large tunneling current) are observed for this structure. An equivalent circuit to this structure is proposed to explain the charging effect.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

5.1 Introduction

The electrical properties (i.e., flatband voltage shift, tunneling current, and retention characteristics) of metal oxide semiconductor (MOS) capacitor embedded with silicon nanocrystal (nc-Si) are indispensable realms to be explored. In this chapter, conventional methods of current-voltage (I-V) measurements and capacitance-voltage (C-V) measurements are being used to characterize the electrical properties of an MOS structure with nc-Si. The influences of nc-Si distributions (i.e., (a) single-layer of nc-Si and (b) nc-Si distributed throughout the SiO₂) are discussed separately. Fig. 5.1 illustrates the two different distributions of nc-Si in the SiO₂. In section 5.2.1, we will discuss the annealing effect on the electrical properties of single layer nc-Si in SiO₂ film. The current-voltage characteristic of the structure will be explained briefly. In section 5.3, the electrical characteristics of nc-Si embedded throughout the entire SiO₂ will be discussed.

Fig. 5.1 Single layer nc-Si embedded in SiO₂ (a) and nc-Si embedded throughout the entire SiO₂ (b).

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

5.2 Single layer of nanocrystal embedded in SiO₂ thin film

5.2.1 Annealing effect on the flatband voltage shift

One of the promising techniques for the incorporation of nc-Si in SiO₂ films is Si ion implantation into SiO₂ films grown by thermal oxidation of a Si substrate as discussed in details in Chapter 2. With this technique, Si nanocrystals with a size less than ~ 5 nm can be formed by subsequent thermal annealing in the Si-rich SiO_x ($x < 2$) films resulting from the Si ion implantation [104]. Memory effects of nc-Si embedded in SiO₂ thin films synthesized with low to very-low energy Si⁺ implantation followed by subsequent annealing have been demonstrated by several research groups [108, 158]. Different annealing conditions including annealing temperature and annealing time have been reported in different studies [87, 158, 159]. There are two important issues. The first issue being the optimization of the annealing temperature to form nanocrystal and to reduce the flatband voltage shift to a minimum value. The second issue concerns the remaining Si ions trapped in the SiO₂ matrix. Although the Si ions can be removed by a high temperature annealing, there may be still be some Si ions remaining if the annealing temperature is not high enough or annealing time is not long enough [160]. The remaining Si ions affect the flat-band voltage, and they can cause instability in the flat-band voltage as the Si ions can be neutralized by the injected electrons during the memory operation. Ironically, although increasing the annealing temperature and prolonging the annealing time can eliminate the ions, too high a thermal budget is harmful, and thus an optimized annealing process is required. There are no detailed studies currently reported on the remaining Si ions and their effect on the performance and the stability of the memory devices. In the present work, a study on the annealing effect on the flatband voltage as well as on

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

the instability of the flatband voltage due to the remaining Si ions has been conducted. Two types of annealing processes will be discussed, namely conventional furnace annealing and rapid thermal annealing.

Fig. 5.2 Comparison of the C-V characteristics between two annealing temperatures (850 °C and 1000 °C). The annealing time is 20 minutes for both samples.

5.2.1.1 Conventional furnace annealing

The C-V characteristics of two different samples annealed at 850 °C and 1000 °C respectively, for 20 mins are shown in Fig. 5.2. The C-V curves were obtained by sweeping the voltage to the negative direction (i.e., from the depletion to the accumulation). The two samples show a flatband voltage difference of ~ 2.3 V. This indicates that thermal annealing has a strong impact on the flatband voltage. The flatband voltage of the sample annealed at 850 °C is more negative than that of the sample annealed at 1000 °C. This shows that thermal annealing leads to the reduction of positive charges trapped in the SiO₂ matrix. The positive

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

charges are the Si ions that are trapped in the SiO₂ during the Si ion implantation. They can be released by a high temperature annealing.

Fig. 5.3 shows the flatband voltage shift as a function of both the annealing temperature and annealing time for conventional furnace annealing. The annealing experiments were carried out with either a constant annealing time or a constant annealing temperature. From this figure, it is clearly observed that the effect of the Si ions on the flatband voltage and the reduction of the Si ions by annealing in high temperature. For the former case, the annealing time is set at 20 mins and the annealing temperature varies from 500 °C to 1100 °C. For the latter case, the annealing temperature is set at 1000 °C and the annealing time varies from 20 mins to 100 mins. The flatband voltage shift (ΔV_{fb}) is measured with respect to the flatband voltage of a 30 nm pure SiO₂ sample. In this figure, it is observed that the as-implanted sample also experiences some annealing effect during the deposition of platinum electrodes.

At annealing temperatures > 900 °C, no further reduction in the flatband voltage shift is observed, and the ΔV_{fb} is ~ -0.1 V. This shows that the annealing temperature has reached a saturation point and no further reduction in the flatband voltage shift can be obtained. For the case of annealing temperature fixed at 1000 °C, an almost constant ΔV_{fb} ranging from -0.2 V to -0.1 V is observed for annealing time longer than 20 minutes, as shown in Fig. 5.3. The dependence of the flatband voltage shift on both the annealing temperature and annealing time shown in Fig. 5.3 clearly indicates that annealing at 900 °C for 20 minutes is sufficient since a higher annealing temperature or a longer annealing time does not reduce the flatband voltage shift further. This has important implication for memory device fabrication when excess thermal budget must be avoided. Indeed,

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

previous works by Priolo group have suggested that the annealing temperature below 900 °C is insufficient to precipitate all the Si nanocrystals produced by CVD method [161-163].

Fig. 5.3 Flatband voltage shift as a function of both annealing temperature and annealing time for conventional furnace annealing.

5.2.1.2 Rapid Thermal Annealing (RTA)

The flatband voltage shift of implanted Si ions in the SiO₂ thin film annealed by rapid thermal annealing (RTA) process is further investigated. The RTA process is used frequently in CMOS processing especially for dopant activation after ion implantation [51, 164]. Fig. 5.4 shows the flatband voltage shift as a function of different annealing temperature and annealing time using the rapid thermal annealing (i.e., ramping rate = ~40 °C/ s). For the as-implanted sample, the

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

flatband voltage shift is still very large (~ -37 V). There is a gradual reduction of flatband voltage shift as the annealing time increases from 20 s to 100 s when the sample is annealed at 900 °C. There is still a large flatband voltage shift (~ -22 V) even though the sample has been annealed at 900 °C for 100 s using the RTA process. Besides, it is found that the flatband voltage shift is still very high even though the sample is being annealed at 1000 °C for 20 s. The flatband voltage shift is ~ -13 V. Compared to the samples annealed using the conventional furnace annealing at 900 °C for 20 mins, the flatband voltage shift due to the remaining Si ions inside the SiO₂ has been reduced to a minimum value. It is clear that the RTA process is unable to remove the remaining Si ions inside the SiO₂.

Fig. 5.4 Flatband voltage shift for the sample annealed by rapid thermal annealing (RTA) process.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

5.2.2 Remaining ions due to annealing effect

To get a quantitative analysis on the effect of annealing on the flatband voltage shift, the amount of remaining ions in the device has to be determined. The number of trapped Si ions can be determined from the flatband voltage shift. The distribution of the charge density $\rho(x)$ due to the trapped Si ions in the SiO₂ thin film is assumed proportional to the distribution of the implanted Si in the SiO₂ thin film, i.e., $\rho(x) = Af(x)$ where A is a coefficient depending on thermal annealing and $f(x)$ is the distribution of the implanted Si. The distribution of the implanted Si can be determined from the stopping and range of ions in matter (SRIM) simulation or from Secondary Ion Mass Spectroscopy (SIMS) measurements. The number of remaining Si ions, N is found to be

$$N = \frac{(C_{ox}\Delta V_{fb})}{1.6 \times 10^{-19}} \frac{T_{ox} \int_0^{T_{ox}} f(x) dx}{\int_0^{T_{ox}} xf(x) dx} \quad (5.1)$$

where T_{ox} is the SiO₂ thickness, and $C_{ox} (= \frac{\epsilon_r \epsilon_0}{T_{ox}})$ where ϵ_r is the dielectric constant of SiO₂ and ϵ_0 is the permittivity in vacuum) is the gate oxide capacitance per unit area.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

Fig. 5.5 Number of trapped Si ions as a function of annealing temperature and annealing time for conventional furnace annealing.

Fig. 5.6 Number of trapped Si ions as a function of annealing temperature and annealing time for rapid thermal annealing.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

Fig. 5.5 shows the number of trapped Si ions as a function of different annealing temperature and annealing time. These samples were annealed using the conventional furnace annealing process. The as-implanted sample has $\sim 1.5 \times 10^{14}$ ions/cm² of Si ions trapped in the SiO₂. This means that only $\sim 0.2\%$ of the implanted ions (note that the implant dose is 8×10^{16} ions/cm²) remains in the SiO₂ thin film for the as-implanted sample. For the sample annealed at 900 °C for 20 minutes, thermal annealing has reduced the number of the trapped ions to the lowest value (i.e., $\sim 1 \times 10^{12}$ ions/cm²). At higher annealing temperature (i.e., 1000 °C or 1100 °C for 20 mins), there is no further reduction in the number of trapped Si ions. When the annealing time (at 1000 °C) is increased, there is also no further reduction in the number of trapped Si ions.

Fig. 5.6 shows the remaining trapped Si ions in the SiO₂ when the sample is annealed with RTA process. For the sample annealed at 1000 °C for 20 s, the remaining Si ions is found to be $\sim 5.1 \times 10^{13}$ ions/cm², which is 50 times larger than that of the sample annealed using the conventional furnace annealing. Similarly to the sample annealed at 900 °C, the remaining trapped Si ions is about 86 to 125 times larger when the annealing time reduces from 100 s to 20 s. This indicates that it is difficult to eliminate the Si ions by using the RTA process.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

5.2.3 Reduction of flatband voltage shift by electron injection

On top of the annealing process, the flatband voltage shift can be further reduced by electron injection from the gate under a negative gate voltage, indicating that the trapped Si ions can be neutralized by the injected electrons. Fig. 5.7 shows the flatband voltage shift as a function of the electron injection time at the gate voltage of -5 V for the samples annealed at different temperatures and different annealing time. For the as-implanted sample, the electron injection in the first 60 s causes a dramatic reduction from -37.8 V to -4.8 V in the flatband voltage shift; however, further electron injection does not change the flatband voltage shift, indicating that some trapped ions ($\sim 1.9 \times 10^{13}$ ions/cm²) cannot be neutralized by the injected electrons. For the sample annealed at 700 °C for 20 minutes, there is also a small amount of trapped ions of 2×10^{12} ions/cm² that cannot be neutralized by the electron injection. For the sample annealed at 900 °C for 20 minutes, as discussed earlier the thermal annealing has reduced the number of the trapped ions to the lowest limit (i.e., 1×10^{12} ions/cm²), and therefore the electron injection does not lead to a significant change in the flatband voltage shift.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

Fig. 5.7 Reduction of flatband voltage shift by electron injection from the gate.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

5.2.4 Charging effect in single-layer nc-Si

After investigating the annealing effect on the flatband voltage shift, it is interesting to investigate the electrical characteristics of single layer nc-Si embedded in SiO₂ matrix. Recently it has been demonstrated that the synthesis of nc-Si with very-low-energy ion implantation can be used to fabricate nanocrystal-based flash memories [40]. With a low-energy ion-implantation, the nc-Si can be confined in a very narrow layer embedded in the gate oxide. To investigate the memory effect of nc-Si, a common practice is to form the structure of gate / control oxide / nc-Si layer / tunnel oxide / Si substrate. In the present study, the above structure is simplified by using a single very-low-energy ion implantation into a SiO₂ thin film to eliminate the deposition of the control oxide [165]. In the simplified structure, the nc-Si is distributed in a narrow layer in the gate oxide near the gate.

Two samples with nc-Si embedded in the SiO₂ are used in this study. Si ions are implanted into the 30 nm SiO₂ thin film at 2 keV with the implantation dosage of 8×10^{16} and $1 \times 10^{16} \text{ cm}^{-2}$ for sample 1 and sample 2 respectively. Thermal annealing was carried out for all implanted samples in N₂ ambient at 1000 °C for 1 hour to induce nc-Si formation. As revealed by the cross-sectional high-resolution transmission electron microscope (HRTEM) image shown in Fig. 5.8, the nc-Si size is ~5 nm, and the nc-Si is confined in a narrow layer with a layer thickness which is about the same as the nc-Si size.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

Fig. 5.8 Cross-sectional high resolution TEM image of sample 2.

Fig. 5.9 shows the hysteresis effect in the C-V measurement from -8 V to +6 V and then from +6 V to -8 V. In contrast to the control sample (i.e., without Si ion implantation) which does not show any hysteresis effect, both sample 1 (with a Si^+ dosage of $8 \times 10^{16} \text{ cm}^{-2}$) and sample 2 (with a Si^+ dosage of $1 \times 10^{16} \text{ cm}^{-2}$) show a large hysteresis effect. The hysteresis window is approximately $\sim 1.8 \text{ V}$ for sample 1 and $\sim 0.6 \text{ V}$ for sample 2, respectively, showing that a higher Si^+ dosage leads to a larger hysteresis effect. On the other hand, an increase in the capacitance at positive gate voltage is also observed for both sample 1 and sample 2 when the gate voltage is scanned from +6 V to -8 V, as shown in Fig. 5.9. A higher Si^+ dosage leads to a larger increase in the capacitance. The increase in the capacitance is due to the contribution of uncharged or neutral nanocrystals near the surface of SiO_2 to the total capacitance of the MOS structure [36, 37]. This effect has been discussed in detail in Chapter 4.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

Fig. 5.9 Hysteresis behaviors in C-V measurement of sample 1 (a), sample 2 (b) and the pure SiO_2 sample (c).

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

The rising of the capacitance on the right hand side of curve in Fig. 5.9 is due to the existent of uncharged nc-Si in the SiO₂. These uncharged nc-Si in the SiO₂ can easily respond to the small ac signal during the C-V measurements at 1 MHz. For a pure SiO₂ MOS capacitor without nc-Si, the depletion charge fails to respond to the small ac signal during the C-V measurement, thus the total capacitance at depletion is small as shown in Fig. 5.9c. In contrast, for a SiO₂ embedded with nc-Si, the uncharged nc-Si can easily respond to the C-V measurement, thus contributes to the rising of the capacitance at depletion.

The sample with nc-Si exhibits a memory effect in terms of flatband voltage shift (ΔV_{fb}). As shown in Fig. 5.10, the application of a positive gate voltage causes a positive flatband voltage shift (i.e., $\Delta V_{fb} > 0$), while the application of a negative gate voltage leads to a negative flatband voltage shift (i.e., $\Delta V_{fb} < 0$). This indicates that the application of a positive or negative gate voltage results in electron or hole trapping in the nc-Si, respectively. For both electron and hole trapping, the flatband voltage shift strongly depends on the nc-Si concentration. For example, the application of +25 V for 1 s, ΔV_{fb} is 5.85 V for sample 1 while it is only 0.60 V for sample 2. On the other hand, the magnitude of ΔV_{fb} for positive gate voltage is larger than that for negative gate voltage, showing that electron tunneling into the nc-Si is easier than hole tunneling into the nc-Si.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

Fig. 5.10 Flatband voltage shift as a function of the applied positive (a) and negative (b) gate voltage. The duration of the application of a gate voltage is 1 s.

From Fig. 5.10, a step-like ΔV_{fb} can be observed for both positive and negative gate voltage. For the nc-Si with a size of ~ 5 nm in this study, the Coulomb charging energy of the nc-Si is estimated to be ~ 70 meV which is larger than the thermal energy (26 meV) at room temperature [65]. Therefore, Coulomb

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

blockade effect could occur at room temperature. The threshold voltage shift (ΔV_{th}) due to electron trapping in nc-Si is given by

$$\Delta V_{th} = \frac{npq}{\epsilon_{ox}} \left(t_{cfl} + \frac{\epsilon_{ox} t_{nc}}{2\epsilon_{Si}} \right) \quad (5.2)$$

where n is the nanocrystal number density, p is the average number of electrons stored per nanocrystal, q is the electronic charge, ϵ_{ox} and ϵ_{Si} represent the permittivity of the oxide and Si, respectively, t_{cfl} represents the thickness of the control oxide, and t_{nc} is the linear dimension of the nanocrystal well. For nanocrystals that are 5 nm in dimension, a nanocrystal density of $2.5 \times 10^{12} \text{ cm}^{-2}$, and a control oxide thickness of 6 nm, the threshold voltage shift is $\sim 0.8 \text{ V}$ for one electron per nanocrystal. This value is comparable with the experimentally observed step-like ΔV_{fb} which is $\sim 0.5 - \sim 1 \text{ V}$. On the other hand, the coulomb gap voltage for addition of a single electron to a nanocrystal can be calculated with the formula of e/C_{Σ} , where C_{Σ} is an approximation to the nanocrystal capacitance [166, 167]. From the calculation, the coulomb gap voltage is found to be $\sim +1.8 \text{ V}$, which is also comparable to the experimental observation that every increment of $\sim 2 \text{ V}$ of the gate voltage leads to a step-like ΔV_{fb} . The step-like ΔV_{th} (threshold voltage shift) behavior has also been observed in nc-Si structures by other researchers [168, 169]. A more direct way to observe the single-electron effect is the measurement of the oscillation in the drain current of a MOSFET with nc-Si embedded in the gate oxide [170]. However, such a measurement requires the transistor size to be very small (typically in the order of 10^{-16} m^2).

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

5.2.5 Current transport in single-layer nc-Si

Fig. 5.11 shows the gate current as a function of gate voltage for pure SiO₂ sample, sample 1 and sample 2. As shown in this figure, the introduction of nc-Si into the gate oxide leads to a reduction in the onset voltage of Fowler-Nordheim (FN) tunneling, and the onset voltage decreases with the nc-Si concentration. This can be explained in the following.

For sample 1 and sample 2, nc-Si distributes from the SiO₂ surface to a depth of ~10 nm in the 30 nm gate oxide. Therefore, as shown in Fig. 5.12, the gate oxide can be virtually divided into two regions: Region 1 is a pure SiO₂ layer with a thickness T_1 (~20 nm) and Region 2 is a nc-Si –distributed region with a thickness T_2 (~10 nm). When FN tunneling occurs at the interface of gate oxide / substrate, it is determined by the electric field (E_1) in Region 1 (i.e., the pure SiO₂ region). For the FN tunneling to occur, E_1 must be at least equal to the onset electric field ($E_{\text{SiO}_2}^{\text{onset}}$) for FN tunneling for pure SiO₂. Note that the $E_{\text{SiO}_2}^{\text{onset}}$ is a constant for pure SiO₂. The gate oxide voltage ($V_{\text{ox}}^{\text{onset}}$) required to achieved the $E_{\text{SiO}_2}^{\text{onset}}$ can be described by

$$V_{\text{ox}}^{\text{onset}} = E_{\text{SiO}_2}^{\text{onset}} T_1 + I^{\text{onset}} R_2 \quad (5.3)$$

where I^{onset} is the FN tunneling current at the electric field of $E_{\text{SiO}_2}^{\text{onset}}$, and R_2 is the resistance of Region 2. When there is nc-Si distributed in Region 2, the nc-Si can form conductive percolation tunneling paths [37, 46] which reduces the value of R_2 . In other words, the presence of nc-Si in Region 2 leads to a lower R_2 , and the R_2 decreases as the nc-Si concentration increases. Therefore, it can be concluded based on Eq. (5.3) that the onset voltage of FN tunneling is lowered in the presence of nc-Si and it decreases with the nc-Si concentration.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

Fig. 5.11 Current-voltage characteristics of sample 1, sample 2 and the pure SiO_2 sample.

Fig. 5.12 Schematic illustrations of the two regions of the sample with nc-Si.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

5.2.6 Retention characteristics of single-layer nc-Si

It is also important to investigate the charge retention in the nc-Si. A gate voltage of +25 V is applied for 1 s on both sample 1 and 2. Then C-V measurements are carried out to measure the flatband voltage shift as a function of waiting time. The result is shown in Fig. 5.13. There is no obvious change in the flatband voltage shift for both sample 1 and 2 in the time frame of the measurement (10^5 s). Therefore, the actual charge retention time is expected to be much longer than 10^5 s. This indicates that the ~ 6 nm SiO_2 between the metal gate and the nanocrystal layer is sufficient to hold the charge trapped in the nanocrystal.

Fig. 5.13 Charge retention characteristics of the nc-Si structure. Electron trapping in the nc-Si is achieved by the application of +25 V gate voltage for 1 s.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

5.3 Nanocrystal distributed throughout the SiO₂ thin film

Charging and discharging in nc-Si are indeed very important as they are directly related to data storage/retention in the memory cells. For memory applications, the nanocrystals are normally confined in a narrow layer embedded in the gate dielectrics near the Si substrate. In section 5.2, the electrical properties of nc-Si confined in a narrow layer without the deposition of control oxide have been discussed. It is interesting to consider the electrical behavior of other distributions of nc-Si in the SiO₂. In this section, the charging and discharging in the nc-Si that distributes throughout the gate dielectric especially with the nc-Si peak concentration located near the gate will be examined. For MOS structures with such nc-Si distribution, charging and discharging of the nc-Si are expected to be easy and thus they will have a significant impact on the electrical characteristics of the MOS structures. Indeed, for such MOS structures, some interesting phenomena have been observed.

5.3.1 Fabrication

To fabricate the MOS structures with nc-Si distributed throughout the gate oxide with its peak concentration located near the gate, a 30 nm SiO₂ film was thermally grown on P-type (100) Si wafers in dry oxygen at 950 °C. Then Si⁺ ions with the dose of $3 \times 10^{16} \text{ cm}^{-2}$ were implanted to the SiO₂ at 14 keV. From the SRIM simulations, the peak concentration was estimated to be at the depth of about 20 nm. Thermal annealing was carried out at 1000 °C in N₂ ambient for 1 hour to induce nc-Si formation. The annealing can also eliminate the damage/defects caused by the ion implantation. Formation of nc-Si was clearly

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

observed by transmission electron microscope (TEM) studies. The mean size of the nc-Si is about 5 nm as determined from x-ray diffraction measurement. The oxide layer was thinned in a diluted 2 % HF solution. About 17 nm of SiO₂ layer was removed such that the peak concentration of nc-Si is located close to the oxide surface. A 20 nm aluminum layer was then deposited to form the gate electrode. The backside of the wafer was coated with a layer of aluminum with the thickness of about 1- μ m after removing the backside oxide. Finally, metal alloy process was conducted at 425 °C in N₂ ambient to form ohmic contacts. Fig. 5.14 shows the secondary ion mass spectroscopy (SIMS) profile for the nc-Si in the gate oxide of the MOS structures. The peak concentration of nc-Si was found to be located near the gate. Fig. 5.15 shows the cross-section TEM measurements of the MOS structure.

Fig. 5.14 Si SIMS profile for the MOS structure with nc-Si distributed throughout the gate oxide.

Fig. 5.15 Cross-section TEM measurements for the MOS structure.

5.3.2 Capacitance-voltage characteristics

A MOS capacitor with a gate oxide thickness of 15 nm and a gate area of $100 \times 100 \mu\text{m}^2$, has a capacitance of ~ 24 pF under strong accumulation at -3 V if there is no nanocrystal embedded in the gate oxide (Fig. 5.16c). However, as can be seen in Fig. 5.16a or Fig. 5.16b, with the nc-Si distributed throughout the gate oxide, the virgin capacitance (i.e., the capacitance before charge trapping in the nc-Si) is much larger than this value (~ 45 times larger). This can be explained by the use of equivalent capacitance as follows: Charge could be stored in the three elements of the MOS structures, i.e., the nanocrystals, the remaining gate oxide

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

capacitor and the Si depletion layer. The corresponding capacitances of the elements are denoted by C_{nc-Si} , C'_{ox} and C_D , respectively.

To investigate the charging and discharging effect of nc-Si, a constant voltage of +4 V or -4 V is applied to the gate for 320 s to the sample. It is observed that the MOS capacitance reduces dramatically to a very low level (< 700 fF), as shown in Fig. 5.16. The polarity of the gate voltage (either positive or negative) does not have a significant effect on the reduction of the capacitance. Obviously, the capacitance reduction can be explained in terms of the charge trapping in the nc-Si. With charge trapping in the nanocrystals, the nanocrystal capacitance C_{nc-Si} should decrease as the number of uncharged nanocrystals responding to the small AC signal in the C-V measurement is reduced. If all the chargeable nanocrystals are charged up, then C_{nc-Si} should approach zero. Thus the MOS capacitance is very small as it is now determined by the remaining gate oxide capacitance C'_{ox} (< 700 fF).

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

Fig. 5.16 Changes in MOS capacitance due to charging/discharging in nc-Si. (a) charging at +4 V for 320 s and discharging at -2 V for 160 s; (b) charging at -4 V for 320 s and discharging at +2 V for 160 s; and (c) comparison of the MOS capacitance between the MOS structure without nc-Si and the MOS structures with nc-Si after charging (charging at either + or -4 V).

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

The reduction in the capacitance can be understood with the equivalent circuit consisting of the nc-Si capacitance (C_{nc-Si}), the remaining pure SiO₂ capacitance (C'_{ox}) and the capacitance of silicon surface region (C_D), as shown in Fig. 5.17. The total capacitance (C_{total}) of the system can be represented by

$$C_{total} = \frac{C_D (C_{nc-Si} + C'_{ox})}{C_D + (C_{nc-Si} + C'_{ox})} \quad (5.4)$$

As the value of C_D is very large, the overall capacitance relies on the C_{nc-Si} and C'_{ox} , i.e., $C_{total} \approx (C_{nc-Si} + C'_{ox})$. As the remaining gate oxide capacitance is very small, the total capacitance is determined by the nc-Si capacitance. Due to the existence of a high concentration of nc-Si in the gate oxide close to the gate, the remaining gate oxide capacitance C'_{ox} should be much smaller than the conventional gate oxide capacitance (C_{ox}) without the nc-Si (C'_{ox} is found to be less than ~ 700 fF). On the other hand, as the Si nanocrystals distribute throughout the gate oxide with their peak concentration located close to the gate, they respond easily to the small AC signal in the C-V measurement if they are uncharged or neutral (i.e., no charges trapped in them). The virgin C_{nc-Si} (i.e., the nc-Si capacitance before charge trapping) should be very large due to the existence of a high concentration of nc-Si. However, if the nc-Si is charged up, then the C_{nc-Si} becomes very small, and thus the total capacitance is very small, as shown in Fig. 5.16a.

The charges trapped in the nc-Si can also be released by ultra-violet (UV) illumination or low temperature annealing. As shown in Fig. 5.18, the application of +4 V for 320 s reduces the MOS capacitance to an extremely low value (< 700 fF); however, after 5 minutes of exposure to the UV light at the wavelength of 365 nm, the capacitance increases dramatically to a higher level than the virgin capacitance. This indicates that the UV illumination can release not only the

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

charges that are trapped in the nc-Si during the application of the charging voltage but also the initial charges that are trapped in the nc-Si prior to the application of the voltage (note that the C-V measurement at -3 V may have already caused some charge trapping in the nc-Si). UV illumination experiment was carried out on SiO₂ sample without nc-Si for 5 mins. No reduction or increment in the total capacitance for the SiO₂ sample without nc-Si.

On the other hand, similarly to the UV illumination, a low temperature annealing can also lead to the release of the trapped charges and thus a recovery of the MOS capacitance. Fig. 5.19 shows the recovery of the MOS capacitance after annealing at 100 °C for 10 minutes (a slight increase in the capacitance after the annealing indicates that some initial charges have been released also during the annealing).

Fig. 5.17 Equivalent circuit of the MOS structure with nc-Si embedded in the gate oxide. C_{nc-Si} represents the equivalent capacitance of the nc-Si, C'_{ox} represents the equivalent capacitance of the remaining SiO₂, and C_D represents the equivalent capacitance of the Si surface region, respectively.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

Fig. 5.18 Changes in MOS capacitance due to charging at +4 V for 320 s and the discharging under UV illumination for 5 minutes.

Fig. 5.19 Changes in MOS capacitance due to charging at +4 V for 320 s and the discharging under low temperature annealing at 100 °C for 10 minutes.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

5.3.3 Current-voltage characteristics

It is also interesting to investigate the I-V characteristics of the MOS structure with nc-Si distributed throughout the SiO₂. Fig. 5.20 shows the I-V characteristic of the MOS structure with the nc-Si distributed in the gate oxide. The I-V characteristic is very similar to a typical hard-breakdown [171-173] I-V characteristic of a pure SiO₂ film as both exhibit a power-law behavior. Similar to the situation of post breakdown in a pure SiO₂ film, the power-law behavior in the MOS structure with nc-Si can be explained based on the percolation model [172, 173] of the tunneling paths formed by the uncharged nc-Si distributed in the gate oxide. With the existence of a high concentration of nc-Si in the SiO₂ matrix, the device exhibits a high leakage current.

To investigate the charging and discharging effect of nc-Si, a virgin device was stressed at constant +4 V for 320 s. After the constant-voltage stress, the I-V measurements were conducted again. The current is also found to drop dramatically to a level (a reduction of about 6 orders) similar to that of a virgin pure SiO₂ thin film as shown in both Fig. 5.20 and Fig. 5.21. As observed in Fig. 5.18 (i.e., capacitance drop due to charging in nc-Si), the reduction of current magnitude is due to the charging of nc-Si. After the recovery process by the UV illuminations or thermal annealing at 100 °C, the current increases to the magnitude similar to the virgin I-V characteristics as shown in Fig. 5.20 and Fig. 5.21.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

Fig. 5.20 Reduction and recovery in the gate current after the electrical stress at +4 V for 320 s and the UV illumination for 5 minutes, respectively. The I-V characteristic of pure SiO₂ is included for comparison.

Fig. 5.21 Recovery in the gate current after thermal annealing at 100 °C for 10 minutes.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

The trapped charges in the nc-Si can be released under UV illumination or low-temperature annealing, and the discharged nc-Si can form conductive tunneling paths leading to an increase in the current, as shown in Fig. 5.22c. The discharge by UV illumination is evident from the recovery of the C-V and I-V characteristics after 5 minutes of UV exposure, as shown in Fig. 5.18 and Fig. 5.20. Actually, there is an “over recovery”, i.e., an increase in both the capacitance and the current after the UV illumination as compared to that of the virgin situation. This means that some charges trapped in the nc-Si of the virgin sample, which may be due to the charge trapping during the C-V or I-V measurements, are also discharged by the UV illumination. Similarly, the trapped charges in the nc-Si can also be discharged by low-temperature annealing. Fig. 5.19 and Fig. 5.21 show the recovery of both the capacitance and the current after the annealing at 100 °C for 10 minutes. As shown in Fig. 5.19, an “over recovery” in the current is observed. This indicates that the initial charges trapped in the nc-Si of the virgin sample can be released by the annealing. However, as shown in Fig. 5.20, an “under recovery” in the current is observed (note that the samples of Fig. 5.19 and Fig. 5.20 are identical but not the same). This means that for this sample not all charges trapped in the nc-Si during the electrical stress are released by the annealing. Another observation from Fig. 5.21 is that there is an instability in the current (i.e., the current jumps up or drops during the I-V measurement) after the annealing. This is due to the change in the conductive paths as a result of the discharging/charging of the nc-Si during the I-V measurement.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

Fig. 5.22 A proposed model on the effect of charging and discharging of the nc-Si on the current conduction in the gate oxide.

Chapter 5: Electrical Characteristics of Nanocrystal Embedded in Dielectric Film

Note that the influence of charge trapping in the nanocrystals on C-V characteristics for the nc-Si distributed throughout the SiO_2 is very different from the situation where nanocrystals are being confined in a narrow layer embedded in the gate oxide (i.e., either the nanocrystal distributed very near to the SiO_2 surface as discussed earlier in section 5.2 or the conventional structure of SiO_2 layer / nanocrystal layer / SiO_2 layer). In the latter case, the charge trapping in the nanocrystals leads to a shift of the C-V curve (i.e., a change in the flat-band voltage) [126, 174, 175], but it does not change the capacitance magnitude under accumulation or inversion. In contrast, for nc-Si distributed throughout the SiO_2 , the charge trapping leads to a dramatic reduction in the capacitance magnitude, but no obvious flat-band voltage shift can be seen as the MOS capacitance is reduced to an extremely low level. The difference between the two cases highlights the importance of the nc-Si distribution.

The electrical characteristics of single-layer of nc-Si and nc-Si distributed throughout the SiO_2 film have been presented in this chapter.

Chapter 6

Non-Volatile Memory Devices Based On Silicon Nanocrystal

Non-volatile memory devices based on silicon nanocrystal as charge storage is being fabricated based on the industrial-standard 2- μm complementary metal-oxide-semiconductor (CMOS) process. Silicon nanocrystals are formed by Si ions implantation and subsequently annealed in N_2 ambient at 1000 $^{\circ}\text{C}$. The basic principles of memory devices will be reviewed and the programming / erasing mechanisms will be discussed. Besides, challenges faced by the conventional floating-gate memory devices and the advantages of nanocrystal-based memories are also presented. The memory characteristics of nanocrystal-based memory devices are being investigated at different operating temperature. Furthermore, nanocrystal-based memory devices with two tunnel oxide thicknesses are fabricated and the performance of memory devices is investigated. Finally, the impact of different programming mechanisms (i.e., Fowler-Nordheim (FN) programming or channel-hot-electron (CHE) programming) on the performance and reliability of the memory devices will be discussed.

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

6.1 Introduction

There has been a distinct growth of semiconductor memory devices development since the last few decades, driven by desktop computing, mobile phones, communication, automotive and other types of electronic portable equipment (i.e., digital camera, mp3 audio player, mobile PC, and others). The embedded memory storage in these portable equipments is highly desirable. With the improvement of fabrication technique, smaller memory devices can be fabricated inside these portable equipments, together with the core processing unit. According to the latest survey [24], about 20 % of the semiconductor market is in semiconductor memories, which can be divided into three branches: (i) the volatile memories (i.e., SRAM or DRAM), (ii) the non-volatile memories (i.e., EPROM, EEPROM, or Flash), and (iii) one-time programmable (i.e., ROM), where these three were based on the CMOS technology [176]. Moreover, in the coming years, portable systems will demand even more non-volatile memories that either featuring high density, high writing throughput for data storage application; or with fast random access for code execution in place [23]. Fig. 6.1 illustrates the above mentioned semiconductor memory branches.

Starting from the year 2000, Flash memory can be considered a mature technology, where more than 800 million units of 16Mb equivalent NOR flash devices were sold in the same year. The volume of Flash market is forecasted to be above \$20 billion, reaching the DRAM market amount [24]. In the past, different type of Flash memory and architectures have been proposed and realized for production. The two most common Flash memories are the NOR Flash [177] and the NAND Flash [178, 179]. Both the NOR and NAND Flash memory are basically a floating-gate MOS transistor, i.e., a transistor with a gate that is

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

completely surrounded by dielectrics, the floating-gate (FG) and electrically governed by a capacitively coupled control gate (CG). The FG acts as the storing electrode for the memory device; where charges were injected into the FG and were maintained in the FG to allow the modulation of the threshold voltage. Currently, the FG Flash technology has reached 70 nm with $0.025\text{ }\mu\text{m}^2$ cell size for 8Gb NAND Flash memory [180], and $0.049\text{ }\mu\text{m}^2$ cell size for NOR Flash memory [181].

Fig. 6.1 Memory type.

With the continuing decreases in the size of the FG, Flash memory devices based on FG technology suffer some problems such as performance degradation and retention time, which will be discussed later in section 6.5. As such, in 1995, silicon nanocrystal-based memory devices was proposed by IBM [47] to be a potential candidate to replace the conventional FG Flash memory. Nanocrystal has some unique properties due to the quantum size effect that permits charge storage in it. This enables nanocrystal to act as charge storage for a MOSFET containing

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

nanocrystal in the dielectric film. Details about the advantages of nanocrystal-based Flash memory devices will be discussed in section 6.5.

6.2 Basic principles

What exactly is a Flash memory device? Flash is classified as memory that is able to store and retain digital information under certain conditions. The retained data can be read repeatedly and remain stored for up to ~10 years. Fig. 6.2 illustrates the basic operating principle of a non-volatile memory devices based on the charge storage in the floating gate of a MOSFET. A positive voltage is applied at the gate, grounding all the other three terminals. Electrons will tunnel from the channel to the floating gate (note that the floating gate is either polysilicon or nitride layer) and stored inside the floating gate. The threshold voltage (V_{th}) due to the trapped charges is given by [182]

$$V_{th} = 2\Phi_f + \Phi_{ms} - \frac{Q_f}{C_{OX}} - \frac{Q_D}{C_{OX}} - \frac{Q_T}{\epsilon_{OX}} d_2 \quad (6.1)$$

where Φ_{ms} is the work function difference between the poly-gate and the bulk Si material, Φ_f is the Fermi potential of the semiconductor at the surface, C_{OX} is the capacitance of the insulator layer, Q_f is the fixed charge at the SiO_2 interface, Q_D is the charge in the silicon depletion layer, Q_T is the charge stored in the polysilicon and ϵ_{OX} is the dielectric constant of SiO_2 and d_2 is the thickness of the control oxide. The V_{th} shift (ΔV_{th}) is caused by the storage of the charge Q_T (either of electrons or holes) and is given by

$$\Delta V_{th} = -\frac{Q_T}{\epsilon_{OX}} d_2 \quad (6.2)$$

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

Fig. 6.2 Basic operating principle of a floating-gate non-volatile memory device.

For nanocrystal-based memory devices (as shown in Fig. 6.3), the threshold voltage shift due to the trapping of either electrons or holes in the nanocrystal can be realized as [46]:

$$\Delta V_{th} = \frac{qn_{nc-Si}}{\epsilon_{OX}} \left(t_{ctrl} + \frac{\epsilon_{OX}}{2\epsilon_{Si}} t_{nc-Si} \right) \quad (6.3)$$

where t_{ctrl} is the thickness of the control oxide under the polysilicon gate, t_{nc-Si} is the mean size of the nanocrystal, ϵ_{OX} and ϵ_{Si} is the dielectric constant of SiO_2 and Si, respectively, q is the magnitude of the electronic charge, and n_{nc-Si} is the density of the nanocrystal.

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

Fig. 6.3 Illustration of a nanocrystal-based memory device.

Fabrication of nanocrystal-based memory device is fully compatible with the CMOS process. The main difference between a FG-based memory device and a nanocrystal-based memory device is the gate stack region. As mentioned earlier, for FG memory device, charges are trapped in a continuous layer of polysilicon or nitride layer, while for the nanocrystal-based memory device, charges are trapped in isolated nanocrystalline silicon.

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

6.3 Programming and erasing options

There are a few types of commonly used programming method for FG-NVMs, such as by using channel-hot-electron (CHE) injection [177, 183], Fowler-Nordheim (FN) tunneling [182], channel initiated secondary electron injection (CHISEL) [184-186], source-side injection (SSI) [187, 188] or drain avalanche hot electron (DAHE) [189]. In this work, only two types of programming mechanism (FN and CHE) are being used in this study and their details will be discussed.

6.3.1 Fowler-Nordheim (FN) programming

Flash memory devices can be programmed using the FN injection mechanism. To program the Flash memory using FN injection, a large positive bias is applied at the polysilicon control gate, grounding all three other terminals. Fig. 6.4 shows the band diagram of the device under the FN programming. A simple expression for the FN tunneling is given below [190, 191]

$$J = A E_{ox}^2 \exp(-B/E_{ox}) \quad (6.4)$$

where J is the current density of the FN tunneling current through the oxide layer, E_{ox} is the oxide field, and A and B are two constants given by

$$A = \frac{q^3}{8\pi\hbar m_{ox}\Phi_b} \quad (6.5)$$

$$B = \frac{4}{3} \frac{(2m_{ox})^{1/2}}{q\hbar} \Phi_b^{3/2} \quad (6.6)$$

where q is the electronic charge, m_{ox} is the effective mass for electrons (or holes) in the oxide layer, h is the Planck constant, $\hbar$ the reduced Planck constant, and Φ_b the tunneling barrier height for electrons or holes. It should be noted that the above expression for FN tunneling was derived for a triangular potential barrier under the

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

low-temperature approximation. The image force will modify the triangular potential barrier [192]. In addition, other effects such as the temperature dependence of the FN tunneling current [193, 194], the barrier height variation with the oxide thickness [195, 196], and the dependence of the effective mass on oxide thickness [197, 198], may need to be taken into account. Several approximate expressions have been proposed to take into account the temperature dependence [192, 193] and the image force effect [192]. For simplicity, the above simple expression, i.e., Eqs. (6.4) – (6.6) for the analysis of the FN tunneling current is quite adequate for most of the calculations for Flash memory devices. Since the energy barrier at Si-SiO₂ interface is ~3.1 eV for electrons and ~4.8 eV for holes, the FN current is dominated by tunneling electrons. To achieve current levels sufficient for programming of Flash memory devices ($\sim 10^7$ A/m²), the value of the injection field has to be > 7 MV/cm.

Fig. 6.4 Electron flow during the FN programming.

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

6.3.2 Channel-hot-electron (CHE) programming

Channel-hot-electron (CHE) means the highly energetic electrons induced by the high electric field. To program the Flash memory using CHE method, positive bias is applied at the gate and drain respectively, grounding both the source and bulk. The large positive bias at the drain creates sufficient horizontal electric field for current to flow from the source to the drain terminal. Under the influence of the vertical field, a fraction of these horizon electrons will be accelerated and injected into the floating gate near the drain region. Fig. 6.5 shows the band diagram of the flash memory device under CHE programming. The SiO_2 material has a barrier of ~ 3.1 eV. The first SiO_2 energy barrier between the floating gate and the channel prevents electrons from leaking to the channel. The second barrier between the floating gate and the control gate prevent electrons from escaping to the metal gates.

Fig. 6.5 Electron flow during the CHE programming (Re-plotted using data from Ref. [160]).

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

To program the memory device, positive bias is applied at the gate or at both the gate and drain terminal as shown in Fig. 6.4 and Fig. 6.5. Electrons will tunnel across the tunnel oxide and get trapped in the FG. When no voltage is biased at the gate or the voltage bias is set at 0 V, the trapped charge remains at the FG as shown in Fig. 6.6.

Fig. 6.6 Energy band diagram for a charge stored in the floating gate.

6.3.3 Fowler-Nordheim (FN) Erasing

In this study, all the memory devices are erased by using FN mechanism. A negative bias is applied at the gate terminal, grounding all three other terminals (i.e., drain, source and bulk terminal). Electrons trapped in the FG or nanocrystal will tunnel to the channel under the negative electric field. Fig. 6.7 shows the energy band diagram of the device under the FN erasing. One important difference between CHE and FN is that the former can only be used to program Flash

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

memory, but it cannot remove the electrons from the nanocrystal. As such, FN erasing mechanism is used throughout this study.

Fig. 6.7 Electron flow during the FN erasing.

Fig. 6.8 shows a typical transfer characteristic of a Flash memory device after the programming and the erasing operation. It is observed that is a memory window (i.e., threshold voltage shift) between these two I-V curves. To determine the memory state of the memory device, the sensing is carried out by measuring the current magnitude at a specific voltage. When the measured current is high (typically 20-30 μA), it represents an erased state of “0”. When the current measurement is low, it represents a programmed state of “1”.

Fig. 6.8 The memory window of the device is determined from the threshold voltage differences between the programmed state and the erased state (Re-plotted using data from Ref. [160]).

6.4 Comparison of various semiconductor memory technologies

Table 6.1 summarizes and compares the technologies of some of the semiconductor memories which are currently available and emerging devices. Each of the semiconductor memory (either volatile or non-volatile) has its own advantages and disadvantages. It is observed that scaling issue has been the critical challenge for current FG Flash EEPROM memory devices. Besides, the devices also have limited number of operation cycles ($10^4 - 10^5$), large operation voltage and slow operation time. This gives rise to the importance of new material or new structure that can replace the Flash EEPROM memory devices. From Table 6.1, it is observed that nano floating-gate memory has characteristics similar to the conventional Flash EEPROM memory devices. Besides, nano floating-gate memory devices can be programmed at relatively shorter time, lower operation

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

voltage, while maintaining the non-volatile characteristics. As such, nano floating-gate / nanocrystal-based memory may be a suitable candidate to replace the Flash EEPROM.

Table 6.1 Summary of comparison between semiconductor-memory technologies (Re-plotted using data from Ref. [48]).

Storage mechanism	Present Day Technologies		Phase Change memory	Nano floating Gate memory	Single / few electron memories	Molecular memories
Device type	DRAM	Flash EEPROM	Ovonic Unified memory	Nanocrystal	SET	Bi-stable switch
Availability	2004	2004	~2006	>2006	>2007	>2010
Cell size (F ²)	10	4-8	~6	4	~6	Not known
Write time	<15 ns	~1 ms	< 100 ns	< 30 ns	< 50 ns	~10 ns
Endurance (cycles)	Unlimited	10 ⁴ -10 ⁵	> 10 ¹³	10 ⁶	Not known	10 ²
Retention	64 ms	>10 years	>10 years	10-20 years	~100 s	~1 month
Advantage	- Density - Economy	- Non-volatile - Multi-bit cells	- Non-volatile - Low power - Multi-bit cells	- Non-volatile - Fast read and write - Multi-bit cells	- Density - Low power	- Density - Low power - 3D potential
Challenges	Scaling	Scaling	- Large current -New material and integration	Material quality	Dimension control for room-temperature operation	- Volatile - Thermal stability
Maturity	Production	Production	Development	Research	Research	Research
Voltage (V)	1.8-5	12-20	2	8-10	2	Not known

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

Table 6.2 Critical problems faced by conventional Flash memory (Re-plotted using data from Ref. [48]).

Year	2004	2005	2006	2007	2010	2013	2016
Flash technology, F (nm)	100	90	80	70	50	35	25
Gate Length (μm)	0.21-0.23	0.2-0.22	0.2-0.22	0.19-0.21	0.17-0.19	0.14-0.16	0.12-0.14
NOR Highest W/E voltage	8-10	7-9	7-9	7-9	7-9	7-9	7-9
NAND highest W/E voltage	18-20	18-20	17-19	17-19	17-19	16-18	16-18
NOR tunnel oxide thickness (nm)	9-10	8.5-9.5	8.5-9.5	8.5-9.5	8-9	8-9	8-9
NAND tunnel oxide thickness (nm)	8-9	8-9	7.5-8	7.5-8	6-7	6-7	6-7
NOR control oxide thickness (nm)	11-13	10-12	9-11	9-11	8-10	6-8	6-7
NAND control oxide thickness (nm)	12-14	12-14	11-13	10-13	10-12	9-11	9-11

White-Manufacturable solution exist; and being optimized

Yellow-Manufacturable solution are known

Red-Manufacturable solution are NOT known

6.5 Advantages of nanocrystal-based memory devices

Table 6.2 summarizes the challenges faced by the conventional FG memory devices when the dimension of the devices (i.e., gate length, tunnel oxide thickness, control oxide thickness and etc.) becomes smaller and smaller. The biggest challenge is to maintain the non-volatibility of the memory device as well as to have 10⁵ cycles of program / erase capability. Charge leakage problem

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

becomes critical when the tunnel oxide thickness reduces. The leaking of trapped charge in the FG will shift the V_{th} to a smaller value. If the memory window as shown in Fig. 6.8 is small, slight reduction in the V_{th} will change the memory state from “1” to “0”.

As compared to FG Flash device, nanocrystal charge storage offers several advantages as reviewed by DeBlauwe et al. [199]. The main advantage is the potential to use thinner tunnel oxides without sacrificing non-volatility. The reduction of the tunnel oxide thickness is the key to lower the operating voltages and higher operating speeds. This can improve scalability results and make the storage more robust and fault-tolerant. Besides, nanocrystal-based memories are fully CMOS compatible. The fabrication process is more simplified than stacked-gate FG Flash as it avoids the dual-poly process. Further more, nanocrystal-based memories have excellent immunity to stress induced leakage current (SILC) and oxide defect due to the distributed nature of the charge storage in the nanocrystal layer. The absence of drain to FG coupling has also made nanocrystal-based memories suffer less drain-induced-barrier-lowering (DIBL) and therefore have intrinsically better punchthrough characteristics. On the other hand, the nanocrystal layer can be as thin as ~ 5 nm thick (with each nanocrystal size of ~ 5 nm) while still maintaining good charge retention characteristic. This is comparatively better to FG Flash as the FG layer suffers charge loss due to the reduction of the FG layer thickness. As shown in Fig. 6.9a, all the charges trapped in the FG will leak to the Si substrate if there is a single defect in the tunnel oxide. In contrast, for the nanocrystal-based memory, charge loss will occur only at the specific nanocrystal underneath the defect in the tunnel oxide, as shown in Fig. 6.9b.

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

On the other hand, nanocrystal memory has deeper electron storage traps (~ 3 eV) compared to nitride traps (1-2 eV) improves electron retention within the nanocrystal. Coulomb blockade (CB) effect due to the small size of nanocrystal is another advantage for nanocrystal memory. The CB effect in the nanocrystal eventually blocks the addition of an extra electron into the nanocrystal if the energy level is fully occupied with electrons. Under zero electric field (no bias applied), these electrons that are trapped at the energy level will require higher thermal energy to tunnel to the Si channel. This situation is different compared to that of using the FG as charge storage node.

Fig. 6.9 All the charges stored in the FG will leak to the channel due to isolated defect at the tunnel oxide (a). For nanocrystal-based memory, only the charge stored in the specific nanocrystal will leak away (b).

Many works have been carried out by researchers on nanocrystal-based memory devices. The pioneer work by Tiwari et al. demonstrated a nc-Si memory device using CVD method [47]. Next, Hanafi et al. used ion implantation technique at a medium implantation energy and medium implantation dosage to

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

produce silicon and germanium nanocrystals memories with long retention time at room temperature [200]. Further more, Atwater group used aerosol technique to produce nanocrystal based non-volatile memory devices and investigated the memory performances at room temperature [72, 201]. Less work has been carried out to investigate the performances of the nanocrystal-based memory devices at different operating temperature, different programming mechanism as well as memory devices with different tunneling oxide thicknesses. In this work, the nc-Si based memory device is synthesized using very-low energy ion implantation at high dosage of Si ions. The memory performances (i.e., endurance and retention characteristics) are investigated at room and hot temperatures. Next, the performances of nc-Si based memory device with different tunnel oxide thickness are investigated. The impacts of different programming mechanisms on the memory performances are also being investigated.

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

6.6 Nanocrystal-based non-volatile memory devices

As mentioned earlier, nanocrystal-based non-volatile memory devices has the potential to overcome the limitation of current polysilicon-based floating-gate memory devices. For this reason, many researches have been carried out in this area by using different techniques such as CVD [62], sputtering [73], and ion-implantation [54] to precipitate nanocrystals. Discussions on the fabrication process have been presented in Chapter 2, section 2.2 and 2.4, respectively. In this section, the characterization of silicon nanocrystal-based non-volatile memory devices based on very-low energy Si ions implantation technique is being highlighted.

The n-channel MOSFETs with the gate oxide containing the nc-Si are fabricated with a conventional 2- μm CMOS process. A 20 nm SiO_2 film is thermally grown on p-type Si(100) wafers in dry oxygen at 950 °C. Si^+ ions with a dose of $5 \times 10^{16} \text{ cm}^{-2}$ are implanted at 2 keV into the oxide. The Stopping and Range of Ions in Matter (SRIM) simulation shows that the implanted Si distributes from the surface to a depth of ~ 13 nm in the 20 nm thermal oxide, suggesting the existence of a tunnel oxide of ~ 7 nm. Additional 20 nm SiO_2 is deposited on top of the previously grown oxide by low pressure CVD (LPCVD) to form a 20 nm control oxide. Then thermal annealing is carried out at 1000 °C in N_2 ambient for 1 hour to induce nc-Si formation. Fig. 6.10a shows the SRIM simulations of nc-Si distribution in the gate oxide. The cross-section TEM image (Fig. 6.10b) of the memory device clearly shows the existence of the nc-Si layers. It also confirms the existence of ~ 7 nm tunnel oxide layer. The program/erase (P/E) operations are carried out with Fowler-Nordheim (FN) tunneling under a positive and negative gate voltage (all other terminals are grounded), respectively.

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

Fig. 6.10 (a) SRIM simulation of the nc-Si distribution; and (b) Cross-section TEM image of nc-Si embedded in the gate oxide of the memory devices.

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

Fig. 6.11 Threshold voltage shift as a function of program time and erase time under different program voltage or erase voltage.

Fig. 6.11 shows the P/E behaviors under different gate voltages with various pulse widths ranging from 10 μs to 1 s. The threshold voltage shifts strongly depend on the magnitude and the duration of the program and erase operations. A threshold voltage window of $\sim 0.5 \text{ V}$ can be achieved under +12 V / -12 V for 1 ms. A larger threshold voltage window and a shorter program and erase time can be achieved with a thinner tunneling oxide. In the following discussions,

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

the memory characteristics are measured with the P/E voltage of +12 V / -12 V and P/E time of 1 ms.

The endurance characteristic of the memory device is shown in Fig. 6.12. At room temperature, only a small drift of 0.1 V in the threshold voltage for both the program and erase operations are observed after 10^5 P/E cycles, showing a good endurance. At the temperature of 150 °C, the threshold voltage shifts after 10^5 P/E cycles is still less than 0.2 V for both the program and erase operations. The drift-up in the threshold voltage is attributed to the electron trapping in the control oxide. The nanocrystal layer may not be able to capture all the injected electrons from the substrate and some of the injected electrons are trapped in the control oxide [65]. Incomplete removal of the trapped electrons from both the control oxide and the nc-Si during the erase operation will lead to an increase in the flatband voltage. Fig. 6.12 clearly shows that this effect is enhanced by a higher operation temperature.

Fig. 6.12 Endurance characteristics at various temperatures.

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

The retention characteristics of the memory devices are shown in Fig. 6.13. The threshold voltage for both the program and erase states are monitored after 1000 P/E cycles. There is no obvious change in the threshold voltage for up to 10^4 s of waiting time. The long-time extrapolation gives a 10-year memory window of ~ 0.3 V for operation temperature up to 100 °C, fulfilling the requirement of 10-year retention at 85 °C. However, the retention characteristics for the program state degrade (i.e., the threshold voltage decreases with waiting time) at 150 °C after 10^4 seconds of waiting time, as shown in Fig. 6.13. The decrease of threshold voltage may be due to the escaping of the trapped electron at a higher temperature. At 150 °C the threshold voltage for the erase state saturates at ~ 1.7 V after 10^4 seconds of waiting time.

Fig. 6.13 Data retention characteristics at various temperatures. The devices have been cycled for 1000 P/E cycles at +12 V / -12 V with a pulse width of 1 ms.

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

6.7 Influence of tunnel oxide thicknesses

Flash memory with the nc-Si as a charge storage has been fabricated and the characteristics and performance of the devices have been investigated in the previous section 6.6. In this section, the performance of the nc-Si-based memory devices with two tunnel oxide thickness is evaluated. The memory devices have a tunnel oxide (t_{tunn}) of either 3 nm or 7 nm. The room temperature low-voltage transfer characteristics of both the samples are shown in Fig. 6.14. For memory device with thick tunnel oxide, the program state is obtained by applying +12 V for 1 ms (Fig. 6.14a), while the program state for sample with thin tunnel oxide is obtained by applying +12 V for 1 μ s (Fig. 6.14b). For the thick sample, the transistor has an on/off current ($I_{\text{On}} / I_{\text{Off}}$) ratio larger than 10^8 and the sub-threshold slope of ~ 110 mV/dec for both the program and erase states. For the thin sample, the transistor has an $I_{\text{On}} / I_{\text{Off}}$ ratio larger than 10^7 and the sub-threshold slope of ~ 110 mV/dec for the erase state and ~ 130 mV/dec for the program state. Obviously, a thicker tunnel oxide leads to a larger $I_{\text{On}} / I_{\text{Off}}$ ratio. The increase of sub-threshold slope for the program state of thin sample is mainly due to the localized charge effect in the nc-Si as well as the fringing field effect [202]. However, for the thick sample, the localized charge effect and fringing field effect are not significant due to the thicker tunnel oxide. As such, the sub-threshold slopes for both the program and erase states of sample 1 remain the same. On the other hand, at the driving current of 1 μ A, a memory window of 0.51 V is obtained for the sample with thick tunnel oxide while a memory window of 1 V is obtained for the sample with t_{tunn} of 3 nm. This indicates that the memory window can be increased by reducing the tunnel oxide.

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

Fig. 6.14 Transfer characteristics of the devices with $t_{\text{tunn}} = 7 \text{ nm}$ (a) and $t_{\text{tunn}} = 3 \text{ nm}$ (b). The $I_{\text{On}}/I_{\text{Off}}$ ratio is higher for $t_{\text{tunn}} = 7 \text{ nm}$.

For the thinner tunnel oxide ($t_{\text{tunn}} = 3 \text{ nm}$), direct tunneling (DT) mechanism is a favorable mechanism to inject electrons (“program” operation) from the channel into the nc-Si or expel the trapped electrons (“erase” operation) from the nc-Si into the channel. Similarly, for the thicker tunnel oxide ($t_{\text{tunn}} = 7 \text{ nm}$), FN mechanism is favourable for the program and erase operations. Under a positive or negative gate voltage, electrons are injected into or tunnel out the nc-Si

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

either by the DT (for the thinner oxide) or FN (for the thicker oxide) mechanism, respectively.

Fig. 6.15 shows the endurance characteristics of the memory device for $t_{\text{tunn}} = 3 \text{ nm}$ (a) and $t_{\text{tunn}} = 7 \text{ nm}$ (b). For $t_{\text{tunn}} = 3 \text{ nm}$, the endurance measurement is conducted with P/E pulses of +12 V / -12 V at 1 μs . For $t_{\text{tunn}} = 7 \text{ nm}$, the endurance measurement is conducted with P/E pulses of +12 V / -12 V at 1 ms. At both room temperature and the hot temperature (85 °C), the device with $t_{\text{tunn}} = 3 \text{ nm}$ exhibits a memory window (i.e., the threshold-voltage difference between the program and erase operations) of $\sim 1 \text{ V}$. However, for the device with $t_{\text{tunn}} = 7 \text{ nm}$, the application of the same voltage for 1 ms can yield a memory window of only $\sim 0.5 \text{ V}$. At room temperature, only a small drift of 0.1 V in the threshold voltage for both the program and erase operations is observed after 10^5 P/E cycles, showing a good endurance for the both tunnel oxides. At the hot temperature of 85 °C, the threshold voltage shift after 10^5 P/E cycles is still less than 0.2 V for the device with $t_{\text{tunn}} = 7 \text{ nm}$, which is considered acceptable. The drift-up in the threshold voltage is attributed to the electron trapping in the control oxide as discussed previously in section 6.6. The nc-Si has a smaller capture cross-section as compared to the polysilicon floating gate and hence portion of the injected electrons from the channel are captured by the nc-Si while the rest are trapped in the control oxide [65]. Incomplete removal of the trapped electrons from the control oxide and the nc-Si during the erase operation leads to an increase in the flatband voltage. This effect is enhanced by a hot temperature. Besides, the threshold voltage drift-up is more significant for the thicker tunnel oxide.

Fig. 6.15 Endurance characteristics for the thinner tunnel oxide ($t_{\text{tunn}} = 3 \text{ nm}$) (a) and the thicker tunnel oxide ($t_{\text{tunn}} = 7 \text{ nm}$) (b) at room temperature and 85°C .

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

Fig. 6.16 Retention characteristics for the thinner tunnel oxide ($t_{\text{tunn}} = 3 \text{ nm}$) (a) and the thicker tunnel oxide ($t_{\text{tunn}} = 7 \text{ nm}$) (b) at room temperature and 85 °C.

The retention characteristics of the memory devices are shown in Fig. 6.16. The threshold voltage measurements are carried out at both room temperature and 85 °C. The threshold voltage for both the program and erase states are monitored after 1000 P/E cycles. For the retention measurements at the hot temperature, the

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

device is left at 85 °C at all time while measuring the threshold voltage. There is no obvious change in the threshold voltage for up to 10^4 s of waiting time for $t_{\text{tunn}} = 7$ nm at both temperatures, and an extrapolated 10-year memory window of ~ 0.3 V is obtained for operation temperatures up to 85 °C. This fulfills the requirement of 10-year retention at 85 °C by the International Technology Roadmap for Semiconductors (ITRS) [48]. For the device with $t_{\text{tunn}} = 3$ nm, ~ 70 % of the stored charge will be lost after 10 years, as shown in Fig. 6.16a. However, for the thicker tunneling oxide ($t_{\text{tunn}} = 7$ nm), only ~ 20 % of the charge will be lost after 10 years as shown in Fig. 6.16b. The poorer charge retention for the thinner tunnel oxide is due to the fact that the trapped electrons are easier to tunnel out through a thinner oxide. Therefore, although the reduction of the tunnel oxide thickness can enhance the charging efficiency, it will result in a poorer retention performance.

6.8 Impact of programming mechanism

Conventional Flash memory devices can be programmed by using channel-hot-electron (CHE) injection [202-204] or Fowler-Nordheim (FN) tunneling [179, 182], but they are usually erased by FN tunneling regardless of the programming mechanisms [179, 182, 204]. For the Flash memory based on nc-Si, the programming / erasing operations by the FN / FN mechanism [39, 57, 148] or the CHE / FN mechanism have been reported [65, 148, 149, 205]. However, there are no detailed studies reported on the impact of the programming mechanisms on the performance and reliability of the nc-Si-based Flash memory devices. In this section we examined the influence of the programming mechanisms including the FN and CHE on the memory window, endurance and charge retention of the fabricated memory devices.

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

To program the memory devices, electrons are injected into the nc-Si from the channel by either the CHE or FN mechanisms. Fig. 6.17 illustrates the two programming mechanisms: FN injection (a), CHE injection (b); and the erasing mechanism (c). For the FN programming, a positive voltage is applied to the gate (i.e., $V_g > 0$) while the other three terminals are grounded. For the CHE programming, a positive voltage is applied to both the gate and the drain (i.e., the gate voltage $V_g =$ the drain voltage $V_d > 0$) while both the source and substrate are grounded as shown in Fig. 6.17b. To erase the memory devices, the electrons trapped in the nc-Si are expelled by the FN mechanism. For the FN erasing, a negative voltage is applied to the gate (i.e., $V_g < 0$) while all the other terminals are grounded as shown in Fig. 6.17c. In the following discussions, “FN / FN” and “CHE / FN” denote the operations of FN programming / FN erasing and CHE programming / FN erasing, respectively.

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

Fig. 6.17 Illustration of the FN (a) and CHE (b) programming and the FN erasing (c).

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

Fig. 6.18a shows the shift of transfer characteristics of the device at room temperature under the FN / FN ($V_g = +10$ V for programming and $V_g = -10$ V for erasing) for 1 μ s. For comparison, the transfer characteristics under the CHE / FN ($V_g = V_d = +10$ V for programming and $V_g = -10$ V for erasing) for 1 μ s are shown in Fig. 6.18b. As can be seen from the figure, the FN / FN leads to a memory window of ~ 0.75 V, while the CHE / FN yields a memory window of ~ 1 V. It is observed that a larger memory window is always achieved by the CHE / FN than by the FN / FN for the same voltage magnitude and time of programming / erasing. This situation is also clearly demonstrated in Fig. 6.19 which shows the memory window as a function of the program / erase voltage at room temperature for both the CHE / FN and the FN / FN. The programming / erasing time is fixed at 1 μ s. It is evident from this figure that the CHE / FN leads to a larger memory window as compared to the FN / FN for any P/E voltage. A larger memory window is actually the consequence of a larger threshold voltage shift caused by programming (i.e., a larger V_{th} at the programmed state) and a lower threshold voltage after erasing (i.e., a lower V_{th} at the erased state) in the CHE / FN operation, as discussed in the following.

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

Fig. 6.18 Transfer characteristics of the programmed and erased states under the programming / erasing operation of FN / FN (a) or CHE / FN (b). The programming / erasing time is 1 μs .

Fig. 6.19 Memory window as a function of magnitude of programming / erasing voltage for the FN / FN and the CHE / FN operations.

The CHE programming causes a larger threshold voltage shift as compared to the FN programming as shown in Fig. 6.19. Under the CHE programming, the channel hot electrons are generated by the lateral electric field near the drain junction. The generated hot electrons are injected into the nanocrystals and the gate oxide both near the drain junction, leading to local charge trapping near the drain. This situation is similar to that observed for conventional NVMs [202-204]. In contrast, under the FN programming, electrons are injected from the Si substrate into the nanocrystals and the gate oxide over the channel, leading to charge trapping with an almost uniform lateral distribution over the whole channel. The difference in the distribution of trapped charges between the two programming mechanisms can explain the larger threshold voltage shift caused by the CHE programming. In the present study, the threshold voltage is measured by reading the drain current with the source grounded (i.e., forward reading). With this

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

measurement configuration, the threshold voltage is sensitive to the charge trapping near the drain, and it is larger for a larger amount of localized charge trapping near the drain. Therefore, the CHE programming can yield a larger threshold voltage shift as it can cause more charge trapping near the drain. On the other hand, as discussed later, the FN programming has more electrons trapped in the control oxide as compared to the CHE programming. The threshold voltage shift due to the electron trapping in the control oxide should not be large because the trapped electrons are far away from the channel. This may be also partially responsible for the relatively smaller threshold voltage shift caused by the FN programming.

It is also evident in Fig. 6.20 that the threshold voltage after erasing (i.e., the V_{th} at the erased state) in the CHE / FN operation is lower than that in the FN / FN operation. As discussed above, in the CHE / FN operation, the CHE programming leads to the localized charge trapping near the drain. However, during the FN erasing the entire nc-Si layer is erased. In other words, the trapped charges in the region near the drain are removed, but at the same time electron tunneling from the nc-Si of all other regions to the Si substrate can occur under the influence of the uniform oxide electric field produced by the negative gate bias. This over erase leads to a lower V_{th} at the erased state. Actually, the over erase is evident from the fact that the initial V_{th} before any programming / erasing) is ~ 1.75 V but the V_{th} decreases to ~ 1.65 V after a CHE programming. In contrast, in the FN / FN operation, both the charging trapping and the charge erasing are laterally uniform, and thus there is no over erase occurring.

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

Fig. 6.20 Endurance characteristics for the CHE / FN and FN / FN at room temperature (a) and at 85 °C (b).

Fig. 6.20 also shows the endurance characteristics of the memory device. For the endurance measurement, the voltage magnitude and duration of programming / erasing are 10 V and 1 μ s, respectively, for both FN / FN and CHE / FN. At room temperature, the threshold voltage (V_{th}) starts to drift up after 10⁴ and 10⁵ program / erase (P/E) cycles for the FN / FN and the CHE / FN, respectively. After 10⁶ P/E cycles, the FN programming shows a V_{th} drift-up of

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

~ 0.13 V, while the CHE programming shows a drift-up of only ~ 0.05 V. At the hot temperature of 85°C , the V_{th} drift-up is more significant, and 0.25 V and 0.13 V drift-up after 10^6 P/E cycles are observed for the FN / FN and the CHE / FN, respectively. The more significant V_{th} drift-up in the FN/ FN operation indicates that the FN programming leads to more electrons trapped in the control oxide than the CHE programming.

Fig. 6.21 Retention characteristics for the CHE / FN and FN / FN at room temperature (a) and at 85°C (b).

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

Fig. 6.21 shows the retention characteristics of the memory devices at room temperature (Fig. 6.21a) and at 85 °C (Fig. 6.21b). The retention measurement was carried out after 1000 P/E cycles. It is observed from the figure that the charge retention for the CHE programming is better than that for the FN programming. For the programmed state at room temperature, ~50 % and ~70 % charge losses after 10 years are expected for the CHE and FN programming, respectively. The better charge retention is related to the localized charge trapping caused by the CHE programming. As discussed earlier, the trapped charges are distributed uniformly in the entire nc-Si layer for the FN programming, but the charge trapping is highly localized near the drain for the CHE programming. As such, the cross section (or area) for electron tunneling out from the nc-Si to the channel during the retention experiment should be much smaller for the latter case. This means that the charge lost is less in the case of CHE programming. For the V_{th} at the erased state at room temperature, for the case of FN / FN it remains unchanged with time, showing no charge transfer during the retention experiment. However, for the case of CHE / FN, it starts to increase at the time of 10^4 seconds from ~1.65 V with a trend to the initial value (i.e., the V_{th} before any programming / erasing) of ~1.75 V, indicating the recovery from the over erase that has been discussed previously. At room temperature, the expected memory window after 10 years is ~0.5 V for the CHE / FN, which meets the retention requirement of NVMs. However, it is only ~0.2 V for the FN / FN. At the hot temperature of 85 °C, the retention capability degrades significantly for both the CHE / FN and the FN / FN due to the enhancement of thermal tunneling of electrons from the nc-Si, but for

Chapter 6: Non-volatile Memory Devices Based On Silicon Nanocrystal

the CHE / FN the expected memory window after 10 years is still larger than 0.3 V which could be sufficient for proper memory functioning.

It is also observed that the CHE programming leads to fewer damages to the gate oxide and the oxide / Si interface. Fig. 6.22 shows the gate leakage currents before and after 10^4 P/E cycles for both the FN programming (Fig. 6.22a) and the CHE programming (Fig. 6.22b). For the FN programming, a significant stress-induced leakage current (SILC) is observed after 10^4 P/E cycles. The SILC at low gate voltage ($< \sim 3$ V) is attributed to the displacement current associated with the interface traps and oxide traps near the interface that are generated by the FN injection, while the SILC at high gate voltage ($> \sim 3$ V) can be explained in terms of the oxide-trap-assisted tunneling [206]. In contrast to the FN programming, the CHE programming leads to an insignificant SILC after 10^4 P/E cycles. The interface trap generation caused by CHE is highly localized in the drain region. However, FN stress causes uniform interface trap generation. During the CHE or FN programming, these electron trapped can release the hydrogen from the nc-Si / SiO₂ interface as well as oxide / silicon interface. After 10^4 program / erase cycles, the number of hydrogen released from the nc-Si / SiO₂ interface due to FN stress is larger than that due to the CHE stress. Besides, DiMaria et al. has pointed out that the FN programming has higher probability of defect generation in the oxide, which could be the possible reason that the FN programming induced higher leakage current in the gate oxide [207]. Therefore, it is evident that the CHE programming produces less damage to the oxide and the interface and thus has a better reliability than the FN programming.

Fig. 6.22 Gate current before and after 10⁴ programming / erasing cycles for the FN / FN (a) and the CHE / FN (b).

Non-volatile memory devices based on silicon nanocrystal has been fabricated. The memory characteristics (programming / erasing, endurance and retention) have been investigated and presented in this chapter.

Chapter 7

Alternative Memory Structures using nc-Si

In this chapter, the invention of 1T-DRAM based on silicon nanocrystal and the invention of two-terminal memory devices based on silicon nanocrystal, both embedded in SiO₂ matrix are discussed. Discussions are provided on the memory effect, endurance characteristic and retention characteristics of 1T-DRAM and the two-terminal memory devices. These two inventions are potentially useful for future volatile and nonvolatile memory devices.

7.1 Introduction

Research on the emerging memory technology is aiming at the development of new volatile and nonvolatile memories to replace the current main-stream volatile and nonvolatile memory devices. Indeed, current volatile and nonvolatile memory devices face the tough challenges of operation and scaling limitation (i.e., low programming speed, high programming voltage, good retention characteristics and etc). According to the ITRS [48], there are a few emerging memory devices (i.e., phase change memory, magnetic random access memory, molecular memories and few electron memories) which have the potential to replace the two main-stream memories. However, there are still some challenges behind the fabrication process as well as the memory operations. Some discussions have been provided in Chapter 6. The potential of silicon nanocrystal-based

Chapter 7: Alternative Memory Structures using nc-Si

nonvolatile memory to replace the conventional floating-gate flash memory has been discussed in detail in Chapter 6. In this chapter, the invention of silicon nanocrystal-based one-transistor memories for future volatile and nonvolatile memory device applications is presented. The electrical properties of each of the memory device will be presented.

7.2 Introduction to conventional 1T1C-DRAM

The Dynamic Random Access Memory (DRAM) is the highest volume semiconductor memory of all time for the past one decade because of its low cost and high density attributes [208]. Its cell is the smallest of the RAM cells which makes the chip small and cost effective. However, with the introduction of Flash memory (as discussed in Chapter 6), the total memory area of a DRAM cell doubles as compared to that of a NAND Flash memory. DRAMs use a large capacitor to store charge as data. In contrast, charge storage occurs at the floating gate for a Flash memory device. The separate capacitor for charge storage connecting to the transistor in a DRAM cell constitutes a larger total area. The major advantage of DRAM is the short programming time. For example, the programming time of a DRAM is ~ 15 ns, compared to ~ 0.1 ms in a Flash memory. As the technology is scaled down to the deep submicron region, the capacitance of a DRAM must remain in the 20-30 fF range for adequate protection against soft and hard error and the data retention time must remain in the millisecond range. To maintain the capacitance of the DRAM, the required area of the capacitor has been stacked above the access transistor or trenched beneath it, adding significant cost to the process. Besides, the ability to retain the data up to 64 ms becomes more difficult as the dimension of the device becomes smaller.

Chapter 7: Alternative Memory Structures using nc-Si

Fig. 7.1 Circuit representation of a 1T1C-DRAM.

Fig. 7.1 shows the circuit representation of the current 1T1C-DRAM. The first generation of a Si-based DRAM was manufactured in 1970, consisting of three transistors (3T) and one capacitor (1C) cell. Significant development and improvement on the memory cell were carried out and the design has been reduced to 1T1C-DRAM. Dennard has invented the first generation of 1T1C-DRAM [209]. This 1T1C-DRAM has paved the way to become the current fast access and high density DRAM. The evolution development and the future direction of DRAMs have been reviewed extensively by Nitayame et al. [210] as well as Dennard et al. [211].

The basic structure of a Si-based 1T1C-DRAM consists of a select MOSFET and a MOS capacitor. The gate terminal of the MOSFET is connected to the word line (WL) of the memory array, the drain terminal of the MOSFET is connected to a Bit line (BL) of the memory array, and the source terminal of the MOSFET is connected to the MOS capacitor.

Charging and discharging of the MOS capacitor in a 1T1C DRAM cell are achieved by allowing current to flow through the channel of the MOSFET into the

Chapter 7: Alternative Memory Structures using nc-Si

MOS capacitor. The mechanism of introducing charge into the capacitor is termed as programming. In the case of a p-type substrate in the MOSFET transistor, the substrate is grounded. To program the MOS capacitor with a binary 1, a 5 V pulse is biased at both the BL and the WL, respectively. Therefore, the channel of the transistor is formed and the transistor is turned on (assuming the threshold voltage of the MOSFET is ~ 1 V). Charge flows into the MOS capacitor and stores inside the capacitor. To erase the memory cell, a 5 V pulse and a 0 V pulse are applied at the gate and the drain terminal respectively. Charge will flow out from the MOS capacitor to the BL, making the memory cell a binary 0.

7.3 **Invention of a silicon nanocrystal-based 1T-DRAM**

Since the invention of one-transistor-one-capacitor 1T1C-DRAM cell in the late 1960s [209], the technology has been advancing continuously and is now approaching the sub-100 nm generation. To go beyond the sub-100 nm generation, there are many challenges and scaling issues [210]. According to the international technology roadmap of semiconductor (ITRS) 2004 for 1T1C-DRAM, the programming time is ~ 15 ns while the retention time is ~ 64 ms [48]. It has been proposed by Tiwari et al. [47] to utilize a structure based on silicon nanocrystal (nc-Si) as a quasi-non-volatile memory, but the programming time of the structure is 100 ns which is too slow for DRAM applications. Recently, a new memory structure with a very short programming time of ~ 3 ns was proposed [212]. However such a structure is based on the expensive silicon on insulator (SOI) technology, and the retention time is less than 10 s. In this work, a true one-transistor-DRAM (1T-DRAM) using nc-Si as a charge storage node is demonstrated based on gate injection mechanism for the first time. The 1T-DRAM has a programming time faster than that of the 1T1C-DRAM and reliability characteristics compatible with most DRAM applications. Most importantly, the retention time of the 1T-DRAM is much longer than that of the 1T1C-DRAM, which could tremendously reduce the power dissipation required for data refreshment.

Except for the additional steps of the nc-Si synthesis, n-channel MOSFETs with the gate oxide containing the nc-Si are fabricated with a conventional 2 μm CMOS process. A 40 nm SiO_2 thin film was thermally grown in dry oxygen at 950 $^\circ\text{C}$ on a p-type Si(100) wafer. Si^+ ions with a dose of $5 \times 10^{16} \text{ cm}^{-2}$ were then implanted into the SiO_2 thin films at the energy of 18 keV and additional 5×10^{16}

Chapter 7: Alternative Memory Structures using nc-Si

cm^{-2} Si^+ ions were implanted at 2 keV. Thermal annealing was carried out in N_2 ambient at 1000 °C for 1 hour.

Fig. 7.2a shows the schematic cross section of the 1T-DRAM structure. The silicon nanocrystals were distributed throughout the gate oxide. The average size of the nanocrystal is found to be ~ 4 nm as obtained from transmission electron microscopy (TEM) measurement. In contrast to the nc-Si-based Flash memory which consist of control oxide / nc-Si layer / tunnel oxide [40], this structure has nc-Si distributing throughout the gate oxide with a specially designed non-uniform distribution. Fig. 7.2b shows the profile of the implanted Si ions based on the Stopping and Range of Ions in Matter (SRIM) simulation. As shown in Fig. 7.2b, the nc-Si distribution in the gate oxide can be divided into two distinct regions, i.e., the “ Δ ”-implanted region and the uniformly-implanted region. The “ Δ ”-implanted region extends from the SiO_2 surface to the depth of ~ 12 nm with the peak of nc-Si concentration located at the depth of ~ 5 nm, while the uniformly-implanted region is located at a depth of ~ 12 nm to the SiO_2 / Si interface. Note that the peak concentration in the “ Δ ”-implanted region is much higher than the concentration in the uniformly-implanted region. The “ Δ ”-implanted region is created for the purpose of fast programming / erasing based on the gate injection mechanism, while the uniformly-implanted region can increase the memory window, as explained in the followings.

In a conventional nc-Si-based Flash memory with the structure of control oxide/nc-Si layer/tunnel oxide, electrons are injected into the nc-Si from the inversion layer of the Si substrate, and thus the delay due to the formation of the inversion region will limit the programming speed. In contrast, in the present 1T-DRAM, electrons are injected directly from the n^+ -polysilicon gate to the nc-Si in

Chapter 7: Alternative Memory Structures using nc-Si

the “ Δ ”-implanted region under Fowler-Nordheim (FN) injection at a negative gate bias. Therefore, the programming speed could be fast enough for a DRAM application. To increase the threshold voltage shift due to the electron trapping in nc-Si during the programming (i.e., to increase the memory window), it is desirable to have electron trapping in nc-Si located close to the interface of SiO_2 / Si substrate. For this purpose, the uniformly-implanted region is created. The memory window can be increased by increasing the nc-Si concentration in this region. A fast charging in this region by electron injection from the gate is realized by the formation of the tunneling paths of the uncharged nc-Si in both this region and the “ Δ ”-implanted region. Therefore, the 1T-DRAM structure has a high programming speed while having a sufficient memory window. On the other hand, the erase operation can be realized by electron tunneling out of the nc-Si to the gate under a positive gate bias, and a fast erase can also be achieved based on the reasons similar to those for the programming. The fast programming/erasing is a tradeoff with the retention time. With the nc-Si distributed throughout the gate oxide, the retention time should be much shorter than that of a conventional nc-Si-based Flash memory where the nc-Si is confined in a very narrow layer isolated by SiO_2 . However, as the magnitude of the positive gate voltage under “Read” operation is much lower than that required for the erase operation, the charge retention time should be long enough for DRAM applications. As discussed below, the 1T-DRAM used in the present study has a retention time of ~ 300 s which is much longer than that of a 1T1C-DRAM. Fig. 7.3 shows the cross-section TEM measurements on the samples. The injection oxide is ~ 3 nm, which allow fast programming time as discussed earlier. A “ Δ ”-implanted region can be clearly

Chapter 7: Alternative Memory Structures using nc-Si

observed in Fig. 7.3 as a layer of nc-Si, while the nc-Si is not that significant in the uniformly-implanted region.

Fig. 7.2 (a) Schematic cross section of the 1T-DRAM structure; and (b) profile of the implanted Si ions obtained from the SRIM simulation.

Fig. 7.3 Cross-section TEM measurement of the 1T-DRAM sample.

Fig. 7.4 shows the measured transfer characteristics of the 1T-DRAM after programming and erasing operations. The programming and erasing operations are carried out at the gate voltage of -12 V and +12 V, respectively, with all other terminals (source, drain and bulk) grounded. Note that the programming-voltage polarity used here is opposite to that of the conventional NAND Flash memory cell. The programming time is 3 ns while the erase time is 30 ns. The difference in the threshold voltage between the programming and the erase, i.e., the memory window is ~ 0.3 V as determined from the measurement. Since the measurement

Chapter 7: Alternative Memory Structures using nc-Si

setup time is ~ 10 s, the memory window determined from the measurement is significantly smaller than the initial memory window of the moment when the programming has just been completed. The estimated initial memory window is ~ 0.5 V, as shown in Fig. 7.4. It should be pointed out that a memory window of ~ 0.2 V is sufficient to determine the two memory states of ‘0’ (programmed) and ‘1’ (erased). It is also worth to note that both the programming voltage and programming time can be reduced when the memory structure is further optimized and the device dimensions are scaled down by using an advanced CMOS technology such as the 90 nm technology (it should be kept in mind that the 1T-DRAM structure used in the present study is fabricated with a 2- μm CMOS technology). Nevertheless, the programming time of the 1T-DRAM here is still 33 times shorter than that of the nc-Si-based quasi-non-volatile memory [47] and 5 times shorter than that of the 1T1C-DRAM memory.

Fig. 7.4 Transfer characteristics of the 1T-DRAM after programming and erase operations.

Chapter 7: Alternative Memory Structures using nc-Si

Fig. 7.5 shows the measured threshold voltage as a function of the programming time for the application of a -12 V gate voltage. As the measurement setup time is ~ 10 s, the actual initial threshold voltage immediately after the programming is about ~ 0.2 V larger than the measured ones shown in Fig. 7.4. For programming time shorter than ~ 50 ns, the threshold voltage shift increases with programming time; however the threshold voltage shift becomes saturated when the programming time is longer than ~ 50 ns. The measured memory window is ~ 0.3 V (the estimated initial memory window is ~ 0.5 V) for the programming time of 3 ns. It increases to ~ 1.0 V for the programming time of 50 ns and is saturated at ~ 1.1 V for a longer programming time. Therefore, the 1T-DRAM has a memory window large enough for a DRAM application even when the programming time is shorter than 3 ns.

Fig. 7.5 Measurement of the threshold voltage as a function of the programming time for the application of gate voltage of -12 V.

Chapter 7: Alternative Memory Structures using nc-Si

The endurance performance of the 1T-DRAM is shown in Fig. 7.6. The endurance measurement is conducted with programming / erasing pulses of -12 V / +12 V with a pulse width of 1 μ s. Due to the limitation of the measurement facility, the endurance performance is measured up to 10^{10} programming / erasing cycles. As shown in Fig. 7.6, there is no trend observed for the drift in the threshold voltage within 10^{10} cycles. Therefore, it is expected that the actual endurance performance should be much better than 10^{10} cycles.

Fig. 7.6 Endurance performance of the 1T-DRAM.

Fig. 7.7 shows the retention characteristic of the 1T-DRAM at room temperature after the application of a -12 V gate voltage for 3 ns. The initial memory window immediately after the programming is ~ 0.5 V, and the memory window decreases to 0.2 V after 300 s. As a memory window of 0.2 V is sufficient to determine the two memory states of '0' (programmed) and '1' (erased), we can conclude that the memory states of the 1T-DRAM can be maintained for 300 s. For DRAM applications, the 1T-DRAM having a retention time of 300 s is a huge

Chapter 7: Alternative Memory Structures using nc-Si

improvement over a conventional 1T1C-DRAM which has a typical retention time of 64 ms [48]. This means that as compared to the conventional 1T1C-DRAM, the 1T-DRAM requires much lesser power dissipation for data refreshment. This is particularly important when memory density becomes higher and higher and for portable electronic devices.

Fig. 7.7 Retention characteristic of the 1T-DRAM at room temperature after the programming at -12 V for 3 ns.

Standard 1T1C-DRAM array architecture has a single memory cell area between 18 to 26 F^2 where F is the technology minimum feature size, and the layout of the DRAM array follows the common open bitline architecture [213]. In contrast, the layout of the 1T-DRAM can adapt the NAND Flash array architecture with an effective cell size of 4.5 F^2 [214]. Therefore, it is expected that the 1T-DRAM can allow a higher density of DRAM manufacturing and it can have an ultimate sub-nanosecond programming time when the feature size is down to sub-100 nm scale.

Chapter 7: Alternative Memory Structures using nc-Si

7.4 Invention of a two terminal memory devices

In a metal-oxide-semiconductor field-effect transistor (MOSFET) memory based on nc-Si, the nc-Si is normally confined in a narrow layer embedded in the gate dielectrics near the Si substrate [57, 126], as shown in Fig. 7.8a. A thin tunneling oxide separates the nc-Si from the Si substrate, and a thicker oxide (i.e., the control oxide) separates the nc-Si from the control gate. Electrons tunneling into (corresponding to the charged or programmed state) or off (corresponding to the discharged or erased state) the nc-Si through the tunneling oxide lead to a shift in the flatband voltage (Fig. 7.8b) and thus a shift in the threshold voltage of the MOSFET [57, 126, 158, 165, 215]. When a sensing voltage (V_{sense}), which should fall in-between the threshold voltages of the charged and discharged states is applied to the control gate, the two memory states can be distinguished from the detection of the on or off of the MOSFET by measuring the drain current (Fig. 7.8c). Detailed discussions on electrical properties of nanocrystal embedded in SiO_2 thin film, floating-gate Flash memory, and nanocrystal-based non-volatile memory devices have been presented in Chapter 5 and Chapter 6 respectively. In this chapter, it is shown that in contrast to the above operation of a conventional nc-Si memory, memory states can be represented by the bistability in capacitance and resistance of the simple nc-Si memory structure shown in Fig. 7.8d. The memory structure reported here is a two-terminal metal-oxide-semiconductor (MOS) structure with the nc-Si distributed throughout the gate oxide (rather than confined in a narrow layer as in a conventional nc-Si memory). Some discussions on the electrical properties of such structure have been discussed in Chapter 5, sections 5.3.2 and 5.3.3. Detailed discussion on how to realize the possibility of a two-terminal memory structure will be presented.

Chapter 7: Alternative Memory Structures using nc-Si

Fig. 7.8 Top, schematic cross section (a) and charge-induced shifts in C-V (b) and I-V (c) characteristics of a conventional nc-Si memory device. Bottom, schematic cross section (d) and charge-induced changes in C-V (e) and I-V (f) characteristics of the nc-Si memory structure reported in this study.

The detailed discussion on the fabrication process of this structure is explained in Chapter 5, section 5.3.1. The area of the memory structure in this study is $100 \times 100 \text{ } \mu\text{m}^2$. An unusual memory effect, i.e., the bistability in capacitance and resistance of the MOS structure as a result of charging and discharging in nc-Si has been observed. Fig. 7.8e shows the capacitance-voltage (C-V) characteristics of the charged and discharged states. In contrast to the situation that a conventional nc-Si memory exhibits a shift in the C-V characteristic between charged and discharged states (Fig. 7.8b), there is a large change in the capacitance magnitude rather than a flatband voltage shift between the two states. At a sense voltage of -0.5 V, the capacitance of the discharged and

Chapter 7: Alternative Memory Structures using nc-Si

charged states is 560 pF and 586 fF, respectively, showing a capacitance ratio of $\sim 10^3$ between the two states. On the other hand, the current-voltage (I-V) characteristic of each state is well defined, and it follows a power law, i.e., $I = aV^b$ where a and b are two parameters determined by the charging in the nc-Si, as shown in Fig. 7.8f. The DC resistance of the MOS structure shows a huge difference between a charged state and a discharged state. As shown in Fig. 7.8f, the current at 0.5 V is 9.3×10^{-12} A (corresponding to a resistance of $5.4 \times 10^{10} \Omega$) and 1.8×10^{-4} A (corresponding to a resistance of $2.8 \times 10^3 \Omega$) for the charged and discharged states, respectively. This means that the resistance ratio of the charged state to the discharged state is 1.9×10^7 . With such high capacitance or resistance ratios, memory states (i.e., the charged and discharged states) can be easily distinguished at low sense voltage. Specifically, the huge difference in resistance between the two states indicates that the memory structure is an excellent switch with well-distinguished on and off states.

Fig. 7.9 Bistability in capacitance (a) and resistance (b). Both the capacitance and resistance are measured at 0.5 V.

The capacitance and the resistance are directly related to the charge trapping / detrapping in the nc-Si. The amount of the trapped charges and the trapping sites are not necessarily the same for every charging/discharging operation since charge trapping / detrapping is a random process. Therefore, the capacitance and the resistance are not necessarily the same for every charging / discharging operation. However, the difference in the capacitance or resistance between a charged state and a discharged is always large enough such that the two

Chapter 7: Alternative Memory Structures using nc-Si

memory states are distinguishable. For example, as shown in Fig. 7.9a, although there is a small difference in the capacitance between the first discharged state and the repeated discharged state, both states can be well distinguished from the charged state.

On the other hand, the charged and discharged states can be retained for at least a few hours at low voltage (for example less than 1 V), as there is no significant change in the capacitance and resistance of the charged or discharged states observed during the time frame limited by the measurement facility. Fig. 7.9 shows the time-domain measurement of the capacitance and resistance corresponding to the charged and discharged states at the measurement voltage of 0.5 V. It is evident from the figure that the application of 0.5 V for 1000 s cannot change the memory states at all. This is particularly important, as the memory states can be easily detected at a low sense voltage (such as 0.5 V). This shows that the memory device has the potential to become a nonvolatile memory device. On the other hand, the total memory area of this structure is smaller than that of a MOSFET. Hence it allows high-density memory array fabrications.

Fig. 7.10 Switching from a discharged state to a charged state by charging at +8 V (a); and Switching from a charged state to a discharged state by discharging at -8 V.

The memory states can be changed by a charging or discharging operation at a relatively high voltage. A charging operation is required for switching a discharged state to a charged state, whereas a discharging operation is required for switching a charged state to a discharged state. The charging and discharging operation can be carried out with either positive or negative voltage. The charging or discharging time for a successful switching strongly depends on the magnitude

Chapter 7: Alternative Memory Structures using nc-Si

of the voltage, and it is also affected by the memory structure. For the memory structure used in this study, the voltage should be larger than 2 V. With the voltage of 8 V, the charging time is ~ 9 s, while the discharging time is ~ 18 s, as shown in Fig. 7.10. It is believed that the charging / discharging time can be dramatically reduced if the memory structure is optimized in terms of the device dimensions and the concentration and distribution of the nc-Si (note that the area of the current structure, which is $100 \times 100 \mu\text{m}^2$, is too large for a real memory device based on the effect reported here, but such a large area is necessary for the capacitance measurement).

This chapter discussed about the invention of a 1T-DRAM based on silicon nanocrystal and the invention of a two-terminal memory devices based on silicon nanocrystal.

Chapter 8

Conclusion and Recommendation

8.1 Conclusion

This chapter briefly summarizes the overall work presented in this thesis. This thesis has addressed the synthesis of silicon nanocrystal, physical properties (i.e., charging and discharging effect, charge transport, charge decay, volume fraction, dielectric constant, flatband voltage shift, and gate tunneling current) as well as device applications based on silicon nanocrystal (nc-Si) embedded in SiO₂ thin film (i.e., Flash memory based on nc-Si, nc-Si-based 1T-DRAM, and nc-Si-based two-terminal memory device). These studies enhanced the understanding on the properties of nc-Si. Finally, some suggestions are provided for future work.

8.1.1 Charge transport and charge decay

The charging and discharging effect of silicon nanocrystal embedded in SiO₂ matrix has been investigated via electrostatic force microscopy (EFM) technique. This technique provides resolution down to sub-micrometer resolution and the mapping of charge decay phenomena (i.e., either of charge decaying to the surrounding nanocrystal, or decaying to the surface of SiO₂) in real-time. It is observed that the charge injection and charge decay are seriously affected by the distributions of nc-Si inside the thin film. Moreover, it is found that the trapped

Chapter 8: Conclusion and Recommendation

charge in the neighboring nanocrystals affects the characteristic decay time. During the charge injection, larger charge cloud is observed for nc-Si distributed near the SiO₂ surface, as compared to nc-Si distributed deep inside the SiO₂. This indicates that during the charge injection process, electrons / holes are easily tunnelled into the nc-Si and from the nc-Si to the surrounding nc-Si for the premier case. For the latter case, there is a SiO₂ barrier to be overcome before trapping can occur. During charge decay, neighboring charge polarities do not affect the charge decay characteristics for nc-Si distributed near SiO₂ surface. In contrast, for nc-Si located deep inside SiO₂, the neighboring charge polarity has seriously affected the charge decay characteristics. From this study, the charge decay model is provided for both nc-Si distributions.

8.1.2 Dielectric constant of nc-Si

The static dielectric constant of isolated silicon nanocrystal embedded in SiO₂ thin film has been investigated by employing Maxwell-Garnett Effective Medium Approximation (EMA) and capacitance-voltage measurement. In addition, an approach to the calculation of the Metal-Oxide-Semiconductor (MOS) capacitance for any nc-Si distribution in the gate oxide has been developed. From the nanocrystal volume fraction as a function of depth, the distribution is divided into multi sub-layers. Then the dielectric constant of each of the sub-layers is calculated and the total capacitance is obtained. For the nc-Si with a mean size of ~4.5 nm, the dielectric constant so determined is 9.8, being consistent with a theoretical prediction. This value is significantly lower than the static dielectric constant (11.9) of bulk crystalline Si, indicating the significance of nc-Si size effect. On the other hand, a detailed picture of the influence of implantation energy

Chapter 8: Conclusion and Recommendation

and implantation dosage on the MOS capacitance has been presented through modeling and experiment. Excellent agreement between the measurement and the modeling has been achieved. This is very important to the future design and modeling of the memory devices.

8.1.3 Single-layer nc-Si embedded in SiO₂ thin film

The formation of silicon nanocrystals (nc-Si) takes place through a thermal chemical reaction that involves high temperature annealing in N₂ ambient. It is noticeable that different annealing temperature, annealing time and ramping rate (i.e., conventional furnace annealing or rapid thermal annealing) can seriously affect the initial flatband voltage of the device. This study is very useful to the fabrication of memory devices based on Si nanocrystals. It is observed that conventional furnace annealing at 900 °C for 20 mins is sufficient to reduce the flatband voltage shift to a minimum value. However, rapid thermal annealing (RTA) at 1000 °C for 20 s is still not sufficient. From this experiment, the number of excess Si ions in the SiO₂ matrix and the percentage of Si ions left inside the SiO₂ after the high temperature annealing process can be calculated. It is found that the remaining Si ions seriously affect the stability of the flatband voltage.

The electrical characteristics of single-layer nanocrystal near the SiO₂ surface have been investigated. The silicon nanocrystal is synthesized via Si ions implantation and subsequently annealed in N₂ ambient for 1000 °C for 1 hour. A common practice is to form the structure of gate / control oxide / nc-Si layer / tunnel oxide / Si substrate. In this study, the above structure is simplified to eliminate the deposition of the control oxide. From the flatband voltage shift under positive and negative voltage bias for 1 s, a step-like behavior is observed. Further

Chapter 8: Conclusion and Recommendation

more, the influence of nc-Si concentration on the flatband voltage shift is also being investigated. For larger nc-Si concentration, the flatband voltage shift under the same biasing voltage is larger. It is also found that the introduction of nanocrystal into the gate oxide leads to a reduction in the onset voltage of Fowler-Nordheim (FN) tunneling, and the onset voltage decreases with the nc-Si concentration. The explanation to this effect has been provided. Finally, it is observed that this simplified structure shows good charge retention characteristics with no charge loss after 10^5 s of waiting time, suggesting that this structure is a good candidate for memory device applications.

8.1.4 Nanocrystal embedded throughout the SiO₂ thin film

In contrast to the conventional situation in which charge trapping in nc-Si confined in a narrow layer embedded in the gate oxide leads to a shift in C-V characteristic, charge trapping in nc-Si distributed throughout the gate oxide with its peak concentration located close to the gate leads to a dramatic reduction in the MOS capacitance. The virgin capacitance of this MOS structure is > 40 times larger than that of a pure SiO₂ thin film with the same SiO₂ thickness. The charging of nc-Si can be easily carried out with a constant-voltage stress, leading to a reduction of both the capacitance and tunneling current. On the other hand, an UV illumination or low-temperature annealing can cause the discharging of nc-Si, leading to the recovery of both the capacitance and tunneling current. The influence of the charging /discharging on the capacitance can be explained with the equivalent circuit proposed in this work. The dramatic change (increase or decrease) in the current is explained in terms of the formation or breaking of the

Chapter 8: Conclusion and Recommendation

conductive percolation paths as a result of discharging or charging of nc-Si, respectively.

8.1.5 Flash memory based on silicon nanocrystal

Non-volatile memory devices based on silicon nanocrystal as charge storage has been fabricated based on the industrial-standard 2- μm complementary metal-oxide-semiconductor (CMOS) process. Silicon nanocrystals are formed by Si ions implantation and subsequently annealed at 1000 °C in N₂ ambient. The memory characteristics of nanocrystal-based memory devices are being investigated at different operating temperatures. It is found that the memory devices perform well at both room and hot temperature, with up to 10⁵ program / erase cycles and a projected 10-years charge retention characteristics. However, for very-high temperature operation (i.e., 150 °C), the performance and retention characteristics degraded.

Moreover, nanocrystal-based memory devices with two different tunnel oxide thicknesses have been fabricated. The performance and retention characteristics of the memory devices are investigated. Larger threshold voltage shift is observed under same biasing voltage for the sample with thinner tunnel oxide thickness. However, the retention characteristics of the memory devices with thinner tunnel oxide (i.e., ~3 nm) is worse than that of the memory devices with thicker tunnel oxide (i.e., ~7 nm). For the thick and thin tunnel oxides, the device is expected to show ~20 % and ~70 % charge loss after 10 years, respectively. In addition, the impact of different programming mechanisms (i.e., Fowler-Nordheim (FN) programming or channel-hot-electron (CHE) programming) on the performance and reliability of the memory devices is also being presented. It is

Chapter 8: Conclusion and Recommendation

shown that as compared to the FN programming, the CHE programming has a larger memory window, better endurance and longer retention time. In addition, the CHE programming does not produce significant stress-induced leakage current, which is significant for the FN programming. This suggests that the CHE programming produces fewer damages to the gate oxide and the oxide / Si interface than the FN programming. Explanations to the difference between the CHE programming and the FN programming are given.

8.1.6 Silicon nanocrystal-based 1T-DRAM

For the first time a true 1T-DRAM based on nc-Si is demonstrated. The programming of the 1T-DRAM is 5 times faster than that of the 1T1C-DRAM. The 1T-DRAM exhibits a good endurance of more than 10^{10} program / erase cycles. More importantly, its retention time is ~ 300 s, which is a huge improvement over the 1T1C-DRAM that has a typical retention time of 64 ms. With the very long retention time, the power dissipation required for data refreshment will be reduced tremendously. The memory array architecture for the 1T-DRAM can adapt a common NAND Flash architecture, allowing a high memory density. Besides, it is also expected that the programming time of the 1T-DRAM can be ultimately reduced to the sub-nanosecond range when the minimum feature size is in the sub-100 nm scale.

8.1.7 Two-terminal memory devices based on silicon nanocrystal

In this work, the memory effect as a result of charging / discharging in nc-Si distributed throughout the gate oxide has been demonstrated. For such nc-Si distribution, the resistance and capacitance of the system exhibit bistability which

Chapter 8: Conclusion and Recommendation

can be controlled by charging and discharging the nc-Si. Memory states (i.e., the charged and discharged states) can be easily distinguished at low sense voltage. For example, at 0.5 V, the resistance ratio of the charged state to the discharged state can be $\sim 10^7$, while the capacitance ratio of the discharged state to the charged state can be $\sim 10^3$. Such a memory effect provides the possibility of a simple memory structure with only two terminals. Explanations to the observed phenomena are provided.

Chapter 8: Conclusion and Recommendation

8.2 Recommendation

There are several approaches and directions in which the research described in this thesis can be extended and contributions be made in the field of nanotechnology silicon.

8.2.1 Fabrication of silicon nanocrystal

It will be useful to fabricate and characterize the silicon nanocrystal using other techniques as discussed in Chapter 2. The new results can be compared to the existing results based on Si ions implantation as presented in this work. The relationship between the synthesis method, nanocrystal size, density and distributions should also be investigated.

8.2.2 Single electron tunneling

Based on the experimental observation in Chapter 5, section 5.2.4, a better understanding on the single electron tunneling and Coulomb blockade effect is very important to realize a single electron device. Room temperature and cold temperature (i.e., ~ 4 K or 77 K) experiments can be carried out to understand the physics and current transport of nanoscale silicon. The experiment is important to further understand the charging effect such as adding / removing only one electron to / from one nanocrystal.

Chapter 8: Conclusion and Recommendation

8.2.3 Flash memory devices based on silicon nanocrystal in high-K dielectric film

In Chapter 6, it is observed that the retention time of ~ 3 nm tunnel oxide is a serious issue. To allow faster memory operation, the tunnel oxide must be reduced without degrading the charge retention characteristics. Even though the retention characteristics of the silicon nanocrystal-based Flash memory with a tunnel oxide of ~ 7 nm is good, it is important to investigate the performance and retention characteristics of the device with thinner tunnel oxide, or by using different material (i.e., high-K materials) as the tunnel oxide. Utilizing high-K dielectric film as the tunnel oxide, it is believed that when the tunnel oxide thickness is thinned down, the programming of the memory devices can be achieved within a shorter programming pulse while maintaining a retention characteristics [216]. Further more, utilizing high-K dielectric film as the control oxide will allow thinner control oxide layer and possibility of lower operating voltage. A detail work on the silicon nanocrystal-based Flash memory device based on high-K dielectric as the tunnel oxide will be useful.

8.2.4 Modeling of silicon nanocrystal memory device

Work involving modeling and simulation of SiO_2 embedded with silicon nanocrystal will be useful. Taking into account the effects of quantum confinement and Coulomb blockade effect, the memory characteristics of silicon nanocrystal can be modeled [217, 218]. There is still a lack of study in the modeling and simulation of nanocrystal-based memory device. If the modeling work can be carried out by comparing the simulation with the experimental data, the result will be very interesting.

List of Publications

Journals:

1. **C.Y. Ng**, T.P. Chen, L. Ding, Q. Chen, Y. Liu, P. Zhao, A.A. Tseng, and S. Fung, "Si ions-induced instability in flatband voltage of Si⁺-implanted gate oxide", *IEEE Trans. Electron Dev.*, vol. 53, pp. 1280-1282, 2006.
2. **C.Y. Ng**, T.P. Chen, L. Ding, M. Yang, J.I. Wong, P. Zhao, X.H. Yang, K.Y. Liu, M.S. Tse, A. Trigg and S. Fung, "Influence of Si nanocrystal distributed in the gate oxide on the MOS capacitance", *IEEE Trans. Electron Dev.*, vol. 53, pp. 730-736, 2006.
3. **C.Y. Ng**, T.P. Chen, M. Yang, J.B. Yang, L. Ding, C.M. Li, A. Du, and A. Trigg, "Impact of programming mechanisms on performance and reliability of non-volatile memory devices based on Si nanocrystal", *IEEE Trans. Electron Dev.*, vol. 53(4), pp. 663-667, 2006.
4. **C.Y. Ng**, T.P. Chen, L. Ding, S. Fung, A. Trigg, and A.A. Tseng, "Memory characteristics of MOSFETs with densely-stacked silicon-nanocrystal layers in the gate oxide synthesized by low-energy ion beam", *IEEE Electron Dev. Lett.*, vol. 27, pp. 231-233, 2006.
5. **C.Y. Ng**, T.P. Chen, L. Ding, Y. Liu, M.S. Tse, S. Fung, and Z.L. Dong, "Static dielectric constant of isolated silicon nanocrystals embedded in a SiO₂ thin film", *Appl. Phys. Lett.*, vol. 88, pp. 063103, 2006.
6. **C.Y. Ng**, T.P. Chen, M.S. Tse, V.S.W. Lim, S. Fung, and A. A. Tseng, "Influence of silicon-nanocrystal distribution in SiO₂ matrix on charge injection and charge decay," *Appl. Phys. Lett.*, vol. 86, pp. 152110-1 - 152110-3, 2005.

List of Publications

7. **C.Y. Ng**, T.P. Chen, H.W. Lau, Y. Liu, M.S. Tse, O.K. Tan, and V.S.W. Lim, "Visualizing Charge Transport in Silicon Nanocrystals Embedded in SiO₂ Films with Electrostatic Force Microscopy", *Appl. Phys. Lett.*, vol. 85, pp. 2941-2943, 2004.
8. **C.Y. Ng**, G.S. Lum, S.C. Tan, T.P. Chen, L. Ding, O.K. Tan, and A. Du, "An electrical study of behaviors of Si nanocrystals distributed in the gate oxide near the oxide/substrate interface of a MOS structure", *Thin Solid Films*, vol. 504, pp. 32-35, 2006.
9. **C.Y. Ng**, T.P. Chen, D. Sreeduth, Q. Chen, L. Ding and A. Du, "Silicon nanocrystal-based non-volatile memory devices", *Thin Solid Films*, vol. 504, pp. 25-27, 2006.
10. **C.Y. Ng**, T.P. Chen, Y. Liu, M.S. Tse, and D. Gui, "Modulation of Capacitance Magnitude by Charging/Discharging in Silicon Nanocrystals Distributed throughout the Gate Oxide in MOS Structures", *Electrochemical and Solid-State Lett.*, vol. 8, pp. G8-G10, 2005.
11. **C.Y. Ng**, Y. Liu, T.P. Chen, and M. S. Tse, "Charging/discharging induced premature breakdown/recovery in Si Nanocrystals embedded in SiO₂ matrix", *Smart Mater. Struct.*, vol. 15, pp. S43-S46, 2005.
12. **C.Y. Ng**, H.W. Lau, T.P. Chen, O.K. Tan, and V. S. W. Lim, "Dissipation of charges in SiO₂ dielectric films: An Electrostatic Force Microscopy Study," *Int. J. Nanoscience*, vol. 4, pp. 709-715, 2005.
13. **C.Y. Ng**, T.P. Chen, P. Zhao, L. Ding, Y. Liu, S. Fung, and A.A. Tseng, "Electrical characteristics of Si nanocrystal distributed in a narrow layer in the gate oxide near the gate synthesized with very low energy ion beams ", *J. Appl. Phys.*, vol. 99, pp. 106115, 2006.

List of Publications

14. **C.Y. Ng**, T.P. Chen, and A. Du, "A study of the influence of tunnel oxide thickness on the performance of flash memory based on ion-beam synthesized silicon nanocrystals," *Phys. Status Solidi (a)*, vol. 203, pp. 1291-1295, 2006.
15. **C.Y. Ng**, T.P. Chen, J.I. Wong, M. Yang, T.S. Khor, C.L. New, C.M. Li, A.D. Trigg, and S. Li, "Performance of silicon nanocrystal non-volatile memory devices under various programming mechanisms", accepted by *Journal of Nanoscience and Nanotechnology*.
16. Y. Liu, T.P. Chen, **C.Y. Ng**, M.S. Tse, S. Li, S. Fung, and P. Zhao, "Influence of charge trapping in Si nanocrystals embedded throughout the gate oxide in MOS structures on I-V and C-V characteristics", *Electrochemical and Solid-State Lett.*, vol. 7, pp. G134-G137, 2004.
17. Y. Liu, T.P. Chen, **C.Y. Ng**, M.S. Tse, P. Zhao, Y.Q. Fu, and S. Zhang, "Time-domain Capacitance Modulation due to Charging/Discharging in Si Nanocrystals Embedded in Gate Dielectric", *Nanotechnology*, vol. 16, pp. 1119-1122, 2005.
18. Y. Liu, T.P. Chen, **C.Y. Ng**, L. Ding, M.S. Tse, S. Fung, A.A. Tseng, "Influence of Si-Nanocrystal Distribution in the Gate Oxide on the Charging Behaviors in the Capacitance Characteristics", *IEEE Trans. Electron Dev.*, vol. 53, pp. 914-917, 2006.

List of Publications

Conferences:

1. **C.Y. Ng**, Y. Liu, T.P. Chen, and M. S. Tse, "Charging/discharging induced premature breakdown/recovery in Si Nanocrystals embedded in SiO₂ matrix," in Proceedings of SPIE (BioMEMS and Nanotechnology) vol. 5275, pg. 18-23, 2004.
2. **C.Y. Ng**, H.W. Lau, T.P. Chen, O.K. Tan, V.S.W. Lim, "Dissipation of charges in Silicon Nanocrystals embedded in SiO₂ dielectric films; An Electrostatic Force Microscopy Study", presented at the 1st International Conference on Nanotechnology (Nanotech 2004), 13-17 July 2004, Meritus Mandarin, Singapore, 2004.
3. **C.Y. Ng**, T.P. Chen, and M.S. Tse, "Electrical Characteristics of Ion-Beam Synthesized Si Nanocrystals In SiO₂ Matrix", in Proceedings of ISIC 2004, pg. 281-283, 2004.
4. **C.Y. Ng**, T.P. Chen, V.S.W. Lim and M.S. Tse, "Study of Charge Storage In Si Nanocrystals Embedded In SiO₂ Matrix By Electrostatic Force Microscopy", in Proceedings of ISIC 2004, pg. 75-77, 2004.
5. **C.Y. Ng**, T.P. Chen, V.S. W. Lim, and M.S. Tse, "Real Time Evolution of Charge Decay Characteristics in Silicon Nanocrystals", in Proceedings of ICSE 2004, pg. 160-163, 2004.
6. **C.Y. Ng**, L. Ding, and T.P. Chen, "Charge Trapping and Charge Decay in Silicon Nanocrystals", in Proceedings of Nanotech 2005, vol. 2, pg. 50-53, 2005.
7. Y. Liu, T.P. Chen, **C.Y. Ng**, and L. Ding, "Influence of Si nanocrystal distribution on electrical characteristics of MOS structures", in Proceedings of Nanotech 2005, vol. 3, pg. 146-149, 2005.

List of Publications

8. **C.Y. Ng**, T.P. Chen, D. Sreeduth, Q. Chen and L. Ding, “Silicon Nanocrystal based non-volatile memory devices”, presented at the 3rd International Conference on Materials for Advanced Technologies (ICMAT), Singapore, 3-8 July, 2005.
9. **C.Y. Ng**, G.S. Lum, S.C. Tan, T.P. Chen, L. Ding, O.K. Tan and A. Du, “An electrical study of behaviors of Si nanocrystals distributed in the gate oxide near the oxide / substrate interface of a MOS structure”, presented at the 3rd International Conference on Materials for Advanced Technologies (ICMAT), Singapore, 3-8 July, 2005.
10. **C.Y. Ng**, T.P. Chen, and A. Du, “A study of the influence of tunnel oxide thickness on the performance of flash memory based on ion-beam synthesized silicon nanocrystals”, presented at the Trends in Nanotechnology (TNT) 2005, Oviedo, Spain, 29 August - 02 September 2005.
11. **C.Y. Ng**, M. Yang, J.I. Wong, and T.P. Chen, “*Static dielectric constant of SiO₂ embedded with silicon nanocrystals*”, 2006 NSTI Nanotechnology Conference and Trade Show, Boston, 7-11 May 2006, Proceedings of Nanotech 2006, Vol. 1, 435-438, 2006.
12. **C.Y. Ng**, J.I. Wong, M. Yang and T.P. Chen, “*Instability in flatband voltage of SiO₂ embedded with silicon nanocrystals*”, 2006 NSTI Nanotechnology Conference and Trade Show, Boston, 7-11 May 2006, Proceedings of Nanotech 2006, Vol. 1, 812-814, 2006.

List of Publications

USA Patent Filling

1. T.P. Chen, Y. Liu, **C.Y. Ng**, and M.S. Tse, “Two-terminal solid-state memory device and two-terminal flexible memory device based on nanocrystals or nanoparticles”, USA Patent Pending (submitted 2005).
2. T.P. Chen and **C.Y. Ng**, “A silicon nanocrystal-based one-transistor-DRAM with fast programming speed and very long retention time”, USA Provisional Patent Application 2005.

Bibliography

- [1] D. Chin, "Nanoelectronics for an Ubiquitous-Information Society," in *ISSCC Dig. Tech. Papers*, vol. 1, pp. 22-26, 2005.
- [2] D.G. Gordon, M.S. Montemerlo, J.C. Love, G.J. Opiteck, and J. C. Ellenbogen, "Overview of Nanoelectronic Devices," in *Proceedings of the IEEE*, vol. 85, pp. 521-540, 1997.
- [3] M. T. Bohr, "Nanotechnology Goals and Challenges for Electronic Applications," *IEEE Trans. Nanotechnology*, vol. 1, pp. 56-62, 2002.
- [4] D. Geer, "Nanotechnology: The Growing Impact of Shrinking Computers," in *IEEE Pervasive Computing*, vol. 5, 2006, pp. 7-11.
- [5] T. Kawai, "Nanotechnology toward DNA electronics," presented at International Microprocesses and Nanotechnology, 2001.
- [6] C. Peterson, "Taking technology to the molecular level," in *Computer*, vol. 33, 2000, pp. 46-53.
- [7] J. Chen, M.A. Reed, A.M. Rawlett, and J. M. Tour, "Large On-Off Ratios and Negative Differential Resistance in a Molecular Electronic Device," *Science*, vol. 286, pp. 1550-1552, 1999.
- [8] C.P. Collier, E.W. Wong, M. Belohradsky, F.M. Raymo, J.F. Stoddart, P.J. Kuekes, R.S. Williams, and J. R. Heath, "Electronically Configurable Molecular-Based Logic Gates," *Science*, vol. 285, pp. 391-394, 1999.
- [9] J. Zheng, P.E. Constantinou, C. Micheel, A.P. Alivisatos, R.A. Kiehl, and N.C. Seeman, "2D Nanoparticle Arrays Show the Organizational Power of Robust DNA Motifs," *Nano Lett.*, vol. 6, pp. 1502-1504, 2006.

Bibliography

- [10] G. Wu and N.C. Seeman, "A Method of Multiplying with DNA," *Nature Computing*, vol. 5, pp. 427-441, 2006.
- [11] K. C. Ang, "Yield challenges in nanotechnology," in *Proc. 12th IPFA*, pp. 1, 2005.
- [12] R. Chau, "Si and Non-Si Nanotechnologies and their Benchmarking," presented at 2005 IEEE VLSI-TSA International Symposium on VLSI Technology, 2005.
- [13] J. C. Ellenbogen, "A Brief Overview of Nanoelectronic Devices," in *Proc. of the IEEE*, 1998.
- [14] A. P. Alivisatos, "Perspectives on the Physical Chemistry of Semiconductor Nanocrystals," *J. Phys. Chem*, vol. 100, pp. 13226-13239, 1996.
- [15] T.D. Krauss and L. E. Brus, "Electronic properties of single semiconductor nanocrystals: optical and electrostatic force microscopy measurements," *Mat. Sci. Engineering B*, vol. 69-70, pp. 289-294, 2000.
- [16] T. Makino, Y. Yamada, N. Suzuki, T. Yoshida, and S. Onari, "Annealing effects on structures and optical properties of silicon nanostructured films prepared by pulsed-laser ablation in inert background gas," *J. Appl. Phys.*, vol. 90, pp. 5075-5080, 2001.
- [17] V. I. Klimov, *Semiconductor and Metal Nanocrystals: Synthesis and Electronic and Optical Properties*: Marcel Dekker, Inc., New York, 2004.
- [18] L. Ding, T.P. Chen, Y. Liu, C.Y. Ng, Y.C. Liu, and S. Fung, "Thermal annealing effect on the bandgap and dielectric functions of silicon nanocrystals embedded in SiO₂ matrix," *Appl. Phys. Lett.*, vol. 87, pp. 121903, 2005.

Bibliography

- [19] J. D. Blauwe, "Nanocrystal Nonvolatile Memory Devices," *IEEE Trans. Nanotechnology*, vol. 1, pp. 72-77, 2002.
- [20] C. G. Hwang, "Semiconductor Memories for IT Era," in *ISSCC Dig. Tech. Papers*, vol. 1, pp. 24-27, 2002.
- [21] P. P. Gelsinger, "Microprocessors for the new millennium: Challenges, opportunities, and new frontiers," in *Proc. ISSCC*, pp. 22-25, 2001.
- [22] G. Weinberger, "The new millennium: wireless technologies for a truly mobile society," in *Proc. ISSCC*, pp. 20-24, 2000.
- [23] C. G. Hwang, "Insights on memory technology and the market," in *IEEE Circuits and Devices Magazine*, vol. 17, 2001, pp. 12-18.
- [24] Databeans, "2005 Semiconductor Market Share," 2005.
- [25] M. Luppi and S. Ossicini, "Ab initio study on oxidezed silicon clusters and silicon nanocrystals embedded in SiO₂: Beyond the quantum confinement effect," *Phys. Rev. B*, vol. 71, pp. 035340, 2005.
- [26] J.Y. Jeong, S. Im, M.S. Oh, H.B. Kim, K.H. Chae, C.N. Whang, and J. H. Song, "Defect vs. Nanocrystal Luminescence Emitted in Si-Implanted SiO₂ Layers," *Jpn. J. Appl. Phys.*, vol. 37, pp. 6981-6983, 1998.
- [27] K. Yano, T. Ishii, T. Sano, T. Mine, F. Murai, T. Hashimoto, T. Kobayashi, T. Kure, and K. Seki, "Single-Electron Memory for Giga-to-Tera Bit Storage," presented at Proceedings of the IEEE, 1999.
- [28] C. M. Hu, *Nonvolatile semiconductor memories, technologies, design and application*: IEEE Press, New York, 1991.
- [29] C.Y. Ng, T.P. Chen, H.W. Lau, Y. Liu, M.S. Tse, O.K. Tan, and V. S. W. Lim, "Visualizing Charge Transport in Silicon Nanocrystals Embedded in

Bibliography

- SiO₂ Films with Electrostatic Force Microscopy," *Appl. Phys. Lett.*, vol. 85, pp. 2941-2943, 2004.
- [30] C.Y. Ng, H.W. Lau, T.P. Chen, O.K. Tan, and V. S. W. Lim, "Dissipation of charges in SiO₂ dielectric films: An Electrostatic Force Microscopy Study," *Int. J. Nanoscience*, vol. 4, pp. 709-715, 2005.
- [31] C.Y. Ng, T.P. Chen, M.S. Tse, V.S.W. Lim, S. Fung, and A. A. Tseng, "Influence of silicon-nanocrystal distribution in SiO₂ matrix on charge injection and charge decay," *Appl. Phys. Lett.*, vol. 86, pp. 152110-1 - 152110-3, 2005.
- [32] C.Y. Ng, T.P. Chen, L. Ding, Y. Liu, M.S. Tse, S. Fung, and Z. L. Dong, "Static dielectric constant of isolated silicon nanocrystals embedded in a SiO₂ thin film," *Appl. Phys. Lett.*, vol. 88, pp. 063103, 2006.
- [33] C.Y. Ng, T.P. Chen, L. Ding, M. Yang, J.I. Wong, P. Zhao, X.H. Yang, K.Y. Liu, M.S. Tse, A.D. Trigg, and S. Fung, "Influence of Si Nanocrystal Distributed in the Gate Oxide on the MOS Capacitance," *IEEE Trans. Electron Dev.*, vol. 53, pp. 730-736, 2006.
- [34] C.Y. Ng, T.P. Chen, L. Ding, Q. Chen, Y. Liu, P. Zhao, A.A. Tseng, and S. Fung, "Si Ion-Induced Instability in Flatband Voltage of Si⁺-Implanted Gate Oxides," *IEEE Trans. Electron Dev.*, vol. 53, pp. 1280-1282, 2006.
- [35] C.Y. Ng, T.P. Chen, P. Zhao, L. Ding, Y. Liu, A.A. Tseng, and S. Fung, "Electrical characteristics of Si nanocrystal distributed in a narrow layer in the gate oxide near the gate synthesized with very-low-energy ion beams," *J. Appl. Phys.*, vol. 99, 2006.
- [36] C.Y. Ng, T.P. Chen, Y. Liu, M.S. Tse, and D. Gui, "Modulation of Capacitance Magnitude by Charging/Discharging in Silicon Nanocrystals

Bibliography

- Distributed throughout the Gate Oxide in MOS Structures," *Electrochemical and Solid-State Lett.*, vol. 8, pp. G8-G10, 2005.
- [37] Y. Liu, T.P. Chen, C.Y. Ng, M.S. Tse, S. Li, S. Fung, and P. Zhao, "Influence of charge trapping in Si nanocrystals embedded throughout the gate oxide in MOS structures on I-V and C-V characteristics," *Electrochemical and Solid-State Lett.*, vol. 7, pp. G134-G137, 2004.
- [38] C.Y. Ng, Y. Liu, T.P. Chen, and M. S. Tse, "Charging/discharging of silicon nanocrystals embedded in SiO₂ matrix induced reduction/recovery in total capacitance and tunneling current," *Smart Mater. Struct.*, vol. 15, pp. S43-S46, 2005.
- [39] C.Y. Ng, T.P. Chen, L. Ding, and S. Fung, "Memory Characteristics of MOSFETs With Densely Stacked Silicon Nanocrystal Layers in the Gate Oxide Synthesized by Low-Energy Ion Beam," *IEEE Electron Dev. Lett.*, vol. 27, pp. 231-233, 2006.
- [40] C.Y. Ng, T.P. Chen, D. Sreeduth, Q. Chen, L. Ding, and A. Du, "Silicon nanocrystal-based non-volatile memory devices," *Thin Solid Films*, vol. 504, pp. 25-27, 2006.
- [41] C.Y. Ng, T.P. Chen, and A. Du, "A study of the influence of tunnel oxide thickness on the performance of flash memory based on ion-beam synthesized silicon nanocrystals," *Phys. Status Solidi (a)*, vol. 203, pp. 1291-1295, 2006.
- [42] C.Y. Ng, T.P. Chen, M. Yang, J.B. Yang, L. Ding, C.M. Li, A. Du, and A. Trigg, "Impact of Programming Mechanisms on the Performance and Reliability of Nonvolatile Memory Devices Based on Si Nanocrystals," *IEEE Trans. Electron Dev.*, vol. 53, pp. 663-667, 2006.

Bibliography

- [43] D. Kahng and S. M. Sze, "A floating gate and its application to memory devices," *Bell Syst. Tech. J.*, vol. 46, pp. 1283-1295, 1967.
- [44] H. Pein and J. D. Plummer, "A 3D sidewall flash EPROM cell and memory array," *IEEE Trans. Electron Dev.*, vol. 40, pp. 2126-2127, 1993.
- [45] S. Hijiya, T. Ito, T. Nakamura, N. Toyokura, and H. Ishikawa, "Electrically alterable read-only memory cell with graded energy band-gap insulator," in *IEDM Tech. Dig.*, vol. 26, pp. 590-593, 1980.
- [46] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E.F. Crabbe, and K. Chan, "A silicon nanocrystals based memory," *Appl. Phys. Lett.*, vol. 68, pp. 1377-1379, 1996.
- [47] S. Tiwari, F. Rana, K. Chan, H. Hanafi, W. Chan, and D. Buchanan, "Volatile and Non-Volatile Memories in Silicon with Nano-Crystal Storage," in *IEDM Tech. Dig.*, pp. 521-524, 1995.
- [48] S. I. Association, "International Technology Roadmap for Semiconductors," <http://public.itrs.net>, 2004.
- [49] K. Lee, J.H. Sim, Y. Li, W.T. Kang, R. Malik, R. Rengarajan, R. Chaloux, S. Bernstein, and P. Kellerman, "Shallow n+/p+ junction formation using plasma immersion ion implantation for CMOS technology," in *Symp. on VLSI Tech.*, pp. 21-22, 2001.
- [50] S. Biswas, C. Mulcahy, P. Banks, and E. Collart, "Accurate characterization of dose and shape of ultra low energy arsenic (1keV and 2keV) implants by SIMS," in *Proc. 14th Int. Conf. Ion Implantation Technology*, pp. 244-247, 2002.
- [51] A.J. Murrell, E.J.H. Collart, M.A. Foad, and D. Jennings, "Process interactions between low-energy ion implantation and rapid-thermal

Bibliography

- annealing for optimized ultrashallow junction formation," *J. Vac. Sci. Technol. B*, vol. 18, pp. 462-467, 2000.
- [52] K. Bala, J. Hoepfner, and B. E. Kareh, "Ion Implantation Issues in Microelectronic Device Manufacturing," presented at Proc. 45th Electronic Components and Technology, 1995.
- [53] P. Normand, D. Tsoukalas, E. Kapetanakis, J.A.V.D. Berg, D.G. Armour, J. Stoemenos, and C. Vieu, "Formation of 2-D Arrays of Silicon Nanocrystals in Thin SiO₂ Films by Very-Low Energy Si⁺ Ion Implantation," *Electrochemical and Solid-State Lett.*, vol. 1, pp. 88-90, 1998.
- [54] O.G. Varona, B. Garrido, S. Cheylan, A.P. Rodriguez, A. Cuadras, and J. R. Morante, "Control of tunnel oxide thickness in Si-nanocrystal array memories obtained by ion implantation and its impact in writing speed and volatility," *Appl. Phys. Lett.*, vol. 82, pp. 2151-2153, 2003.
- [55] C. Bonafos, M. Carrada, N. Cherkashin, H. Coffin, D. Chassaing, G.B. Assayag, A. Claverie, T. Muller, K.H. Heinig, M. Peregp, M. Fanciulli, P. Dimitrakis, and P. Normand, "Manipulation of two-dimensional arrays of Si nanocrystals embedded in thin SiO₂ layers by low energy ion implantation," *J. Appl. Phys.*, vol. 95, pp. 5696-5672, 2004.
- [56] E. Kapetanakis, P. Normand, D. Tsoukalas, K. Beltsios, J. Stoemenos, S. Zhang, and J. V. D. Berg, "Charge storage and interface states effects in Si-nanocrystal memory obtained using low-energy Si⁺ implantation and annealing," *Appl. Phys. Lett.*, vol. 77, pp. 3450-3452, 2000.
- [57] P. Dimitrakis, E. Kapetanakis, D. Tsoukalas, D. Skarlatos, C. Bonafos, G.B. Assayag, A. Claverie, M. Perego, M. Fanciulli, V. Soncini, R. Sotgiu, A. Agarwal, M. Ameen, C. Sohl, and P. Normand, "Silicon nanocrystal

Bibliography

- memory devices obtained by ultra-low-energy ion-beam synthesis," *Solid-State Electron.*, vol. 48, pp. 1511-1517, 2004.
- [58] S. Cheylan and R. G. Elliman, "Effect of hydrogen on the photoluminescence of Si nanocrystals embedded in a SiO₂ matrix," *Appl. Phys. Lett.*, vol. 78, pp. 1225-1227, 2001.
- [59] Y.Q. Wang, R. Smirani, and G. G. Ross, "Effect of hydrogen passivation on the microstructure of silicon nanocrystals in SiO₂," *Physica E: Low-dimensional Systems and Nanostructures*, vol. 23, pp. 97-101, 2004.
- [60] M. Carrada, N. Cherkashin, C. Bonafos, G. Benassayag, D. Chassaing, P. Normand, D. Tsoukalas, V. Soncini, and A. Claverie, "Effect of ion energy and dose on the positioning of 2D-arrays of Si nanocrystals ion beam synthesised in thin SiO₂ layers," *Mat. Sci. Engineering B*, vol. 101, pp. 204-207, 2003.
- [61] J.D.L. Torre, A. Souifi, A. Poncet, C. Busseret, M. Lemiti, G. Bremond, G. Guillot, O. Gonzalez, B. Garrido, J.R. Morante, and C. Bonafos, "Optical properties of silicon nanocrystal LEDs," *Physica E*, vol. 16, pp. 326-330, 2003.
- [62] G. Dalba, N. Daldosso, P. Fornasini, R. Grisenti, L. Pavesi, F. Rocca, G. Franzo, F. Priolo, and F. Iacona, "Chemical composition and local structure of plasma enhanced chemical vapor-deposited Si nanodots and their embedding silica matrix," *Appl. Phys. Lett.*, vol. 82, pp. 889-891, 2003.
- [63] A. Salonidou, A.G. Nassiopoulou, K. Giannakopoulos, A. Travlos, V.I. Sougleridis, and E. Tsoi, "Growth of two-dimensional arrays of silicon nanocrystals in thin SiO₂ layers by low pressure chemical vapour

Bibliography

- deposition and high temperature annealing/oxidation. Investigate of their charging properties," *Nanotechnology*, vol. 15, pp. 1233-1239, 2004.
- [64] D.N. Kouvatsos, V.I. Sougleridis, and A. G. Nassiopoulou, "Charging effects in silicon nanocrystals within SiO₂ layers, fabricated by chemical vapor deposition, oxidation, and annealing," *Appl. Phys. Lett.*, vol. 82, pp. 397-399, 2003.
- [65] R.A. Rao, R.F. Steimle, M. Sadd, C.T. Swift, B. Hradsky, S. Straub, R. Merchant, M. Stoker, S.G.H. Anderson, M. Rossow, J. Yater, B. Acred, K. Harber, E.J. Prinz, B.E. White Jr., and R. Muralidhar, "Silicon nanocrystal based memory devices for NVM and DRAM applications," *Solid-State Electron.*, vol. 48, pp. 1463-1473, 2004.
- [66] A. Nakajima, Y. Sugita, K. Kawamura, H. Tomita, and N. Yokoyama, "Microstructure and optical absorption properties of Si nanocrystals fabricated with low-pressure chemical-vapor deposition," *J. Appl. Phys.*, vol. 80, pp. 4006, 1996.
- [67] M. Zacharias, J. Heitmann, R. Scholz, U. Kahler, M. Schmidt, and J. Blasing, "Size-controlled highly luminescent silicon nanocrystals: A SiO/SiO₂ superlattice approach," *Appl. Phys. Lett.*, vol. 80, pp. 661-663, 2002.
- [68] J. Shen, T.Z. Lu, M. Alexe, O. Kidun, and M. Zacharias, "Controllable Charge Density in the Si Nanocrystals Nonvolatile Memory," *Integrated Ferroelectrics*, vol. 78, pp. 271-279, 2006.
- [69] J. Heitmann, F. Muller, M. Zacharias, and U. Gosele, "Silicon Nanocrystals: Size Matters," *Adv. Mat.*, vol. 17, pp. 795-803, 2005.

Bibliography

- [70] K.A. Littau, P.J. Szajowski, A.J. Miller, A.R. Kortan, and L. E. Brus, "A luminescent Si nanocrystals colloid via a high temperature aerosol reaction," *J. Phys. Chem.*, vol. 97, pp. 1224-1227, 1993.
- [71] M.L. Ostraat, J.W. DeBlauwe, M.L. Green, L.D. Bell, H.A. Atwater, and R. C. Flagan, "Ultraclean two-stage aerosol reactor for production of oxide passivated silicon nanoparticles for novel memory devices," *J. Electrochem. Soc.*, vol. 148, pp. G265, 2001.
- [72] M.L. Ostraat, J.W. DeBlauwe, M.L. Green, L.D. Bell, M.L. Brongersma, J. Casperson, R.C. Flagan, and H. A. Atwater, "Synthesis and characterization of aerosol silicon nanocrystal nonvolatile floating-gate memory devices," *Appl. Phys. Lett.*, vol. 79, pp. 433-435, 2001.
- [73] H. Seifarth, R. Grotzschel, A. Markwitz, W. Matz, P. Nitzsche, and L. Rebohle, "Preparation of SiO₂ films with embedded Si nanocrystals by reactive r.f. magnetron sputtering," *Thin Solid Films*, vol. 330, pp. 202-205, 1998.
- [74] T. Torchynska, F.G.B. Espinoza, Y. Goldstein, E. Savir, J. Jedrzejewski, L. Khomenkova, N. Korsunska, and V. Yukhimchuk, "Nature of visible luminescence of co-sputtered Si-SiO_x systems," *Physica B*, vol. 340-342, pp. 1119-1123, 2003.
- [75] M. Allegrini, C. Ciofi, A. Diligenti, F. Fuso, A. Nannini, V. Pellegrini, and G. Pennelli, "Photoluminescence from ion-beam cosputtered Si/SiO₂ thin films," *Solid State Comm.*, vol. 100, pp. 403-406, 1996.
- [76] V.G. Baru, A.P. Chernushich, V.A. Luzanov, G.V. Stepanov, L.Y. Zakharov, K.P. Donnel, L.V. Bradley, and N. N. Melnik, "Optical

Bibliography

- properties of Si nanocrystals prepared by magnetron sputtering," *Appl. Phys. Lett.*, vol. 69, pp. 4148-4150, 1996.
- [77] L. Patrone, D. Nelson, V.I. Safarov, M. Sentis, W. Marine, and a. S. Giorgio, "Photoluminescence of silicon nanoclusters with reduced size dispersion produced by laser ablation," *J. Appl. Phys.*, vol. 87, pp. 3829-3837, 2000.
- [78] X.Y. Chen, Y.F. Lu, Y.H. Wu, B.J. Cho, M.H. Liu, D.Y. Dai, and W. D. Song, "Mechanism of photoluminescence from silicon nanocrystals formed by pulsed-laser deposition in argon and oxygen ambient," *J. Appl. Phys.*, vol. 93, pp. 6311-6319, 2003.
- [79] T. Orii, M. Hirasawa, and T. Seto, "Tunable, narrow-band light emission from size-selected Si nanoparticles produced by pulsed-laser ablation," *Appl. Phys. Lett.*, vol. 83, pp. 3395, 2003.
- [80] H.W. Lau, O.K. Tan, Y. Liu, C.Y. Ng, T.P. Chen, and D. Lu, "Defect-Induced Photoluminescence from Tetraethylorthosilicate Thin Films Containing Mechanically Milled Silicon Nanocrystals," *J. Appl. Phys.*, vol. 97, 2005.
- [81] T. Fisher, V.P. Koch, K. Shcheglov, M.S. Brandt, and F. Koch, "Continuously tunable photoluminescence from Si^+ -implanted and thermally annealed SiO_2 films," *Thin Solid Films*, vol. 276, pp. 100-103, 1996.
- [82] A. Nakajima, Y. Sugita, K. Kawamura, H. Tomita, and N. Yokoyama, "Si Quantum Dot Formation with Low-Pressure Chemical Vapor Deposition," *Jpn. J. Appl. Phys.*, vol. 35, pp. L189-L191, 1996.

Bibliography

- [83] J. Heitmann, F. Muller, M. Zacharias, and U. Gosele, "Silicon Nanocrystals: Size Matters," *Advance Materials*, vol. 17, pp. 795-803, 2005.
- [84] L. Ding, T.P. Chen, Y. Liu, C.Y. Ng, and S. Fung, "Optical Properties of Silicon Nanocrystals Embedded in a SiO₂ Matrix," *Phys. Rev. B*, vol. 72, pp. 125419, 2005.
- [85] C.F. Lin, W.T. Tseng, and M. S. Feng, "Formation and characteristics of silicon nanocrystals in plasma-enhanced chemical-vapor-deposited silicon-rich oxide," *J. Appl. Phys.*, vol. 87, pp. 2808-2815, 2000.
- [86] X. G. H. Qin, H. Lu, J. Liu, X. Huang, K. Chen, "Observation of Coulomb-blockade in a field-effect transistor with silicon nanocrystal floating gate at room temperature," *Solid State Comm.*, vol. 111, pp. 171-174, 1999.
- [87] G.B. Assayag, C. Bonafos, M. Carrada, A. Claverie, P. Normand, and D. Tsoukalas, "Transmission electron microscopy measurements of the injection distances in nanocrystal-based memories," *Appl. Phys. Lett.*, vol. 82, pp. 200-202, 2003.
- [88] Y.Q. Wang, R. Smirani, and G. G. Ross, "Nanotwinning in Silicon Nanocrystals Produced by Ion Implantation," *Nano Lett.*, vol. 4, pp. 2041-2045, 2004.
- [89] Y.Q. Wang, R. Smirani, G.G. Ross, and F. Schiettekatte, "Ordered coalescence of Si nanocrystals in SiO₂," *Phys. Rev. B*, vol. 71, pp. 161310(R), 2005.
- [90] Y. Kim, K.H. Park, W.C. Choi, T.H. Chung, H.J. Bark, J.Y. Yi, and J. Jeong, "Charge retention effect in metal-oxide-semiconductor structure containing Si nanocrystals prepared by ion-beam-assisted electron beam deposition," *Mat. Sci. Engineering B*, vol. 83, pp. 145-151, 2001.

Bibliography

- [91] Y.H. Kwon, C.J. Park, W.C. Lee, D.J. Fu, Y. Shon, T.W. Kang, C.Y. Hong, H.Y. Cho, and K. L. Wang, "Memory effects related to deep levels in metal-oxide-semiconductor structure with nanocrystalline Si," *Appl. Phys. Lett.*, vol. 80, pp. 2502-2504, 2002.
- [92] J.U. Schmidt and B. Schmidt, "Investigation of Si nanocluster formation in sputter-deposited silicon sub-oxides for nanocluster memory structures," *Mat. Sci. Engineering B*, vol. 101, pp. 28-33, 2003.
- [93] M. Ehbrecht, H. Ferkel, and F. Huisken, "Generation, analysis, and deposition of silicon nanocrystals up to 10 nm in diameter," *Z. Phys. D*, vol. 40, pp. 88-92, 1997.
- [94] R. Govindaraj, R. Kesavamoorthy, R. Mythili, and B. Viswanathan, "The formation and characterization of silver clusters in zirconia," *J. Appl. Phys.*, vol. 90, pp. 958-963, 2001.
- [95] B. D. Cullity, *Elements of X-ray diffraction*, 2nd ed. Indiana: Addison-Wesley, 1997.
- [96] H. Pedersen, F. Soderlind, R.M. Petoral Jr., K. Uvdal, P.O. Kall, and L. Ojamae, "Surface interactions between Y_2O_3 nanocrystals and organic molecules-an experimental and quantum-chemical study," *Surface Science*, vol. 592, pp. 124-140, 2005.
- [97] Y. Hu, O.K. Tan, W. Cao, and W. Zhu, "A low temperature nano-structured $SrTiO_3$ thick film oxygen gas sensor," *Ceramics International*, vol. 30, pp. 1819-1822, 2004.
- [98] Y.X. Jie, X. Wu, C.H.A. Huan, A.T.S. Wee, Y. Guo, T.J. Zhang, J.S. Pan, J. Chai, and S. J. Chua, "Synthesis and Characterization of Ge Nanocrystals

Bibliography

- Immersed in Amorphous SiO_x Matrix," *Surf. Interface Anal.*, vol. 28, pp. 1950-199, 1999.
- [99] T.P. Chen, Y. Liu, M.S. Tse, O.K. Tan, P.F. Ho, K.Y. Liu, D. Gui, and A. L. K. Tan, "Dielectric functions of Si nanocrystals embedded in a SiO₂ matrix," *Phys. Rev. B*, vol. 68, pp. 153301, 2003.
- [100] K. Wang, H. Chen, and W. Z. Shen, "AC electrical properties of nanocrystalline silicon thin films," *Physica B*, vol. 336, pp. 369-378, 2003.
- [101] S.M. Chen and F. S. Y. Ip, "Nitrogen in ultra-thin gate oxides: its profile and functions," *Solid-State Electron.*, vol. 43, pp. 1997-2003, 1997.
- [102] E.S. Marstein, A.E. Gunnaes, U. Serincan, R. Turan, A. Olsen, and T. G. Finstad, "Nanocrystal and nanocluster formation and oxidation in annealed Ge-implanted SiO₂ films," *Surf. Coatings Technology*, vol. 158-159, pp. 544-547, 2002.
- [103] J.F. Ziegler, J.P. Biersack, and U. Littmark, *The Stopping and Range of Ions in Solids*. New York: Pergamon, 1985.
- [104] Y. Liu, T.P. Chen, Y.W. Fu, M.S. Tse, J.H. Hsieh, P.F. Ho, and Y. C. Liu, "A study on Si nanocrystal formation in Si-implanted SiO₂ films by x-ray photoelectron spectroscopy," *J. Phys. D, Appl. Phys.*, vol. 36, pp. L97-L100, 2003.
- [105] T. Muller, K.H. Heinig, and W. Moller, "Nanocrystal formation in Si implanted thin SiO₂ layers under the influence of an absorbing interface," *Mat. Sci. Engineering B*, vol. 101, pp. 49-54, 2003.
- [106] T. Muller, K.H. Heinig, and W. Moller, "Size and location control of Si nanocrystals at ion beam synthesis in thin SiO₂ films," *Appl. Phys. Lett.*, vol. 81, pp. 3049-3051, 2002.

Bibliography

- [107] T. Gebel, J.V. Borony, H.-J. Thees, M. Wittmaack, K.-H. Stegemann, and W. Skorupa, "Non-volatile memories based on Si⁺-implanted gate oxides," *Microelectronic Engg.*, vol. 59, pp. 247-252, 2001.
- [108] J.V. Borony, T. Gebel, K.-H. Stegemann, H.-J. Thees, and M. Wittmaack, "Memory properties of Si⁺ implanted gate oxides: From MOS capacitors to nvSRAM," *Solid-State Electron.*, vol. 46, pp. 1729-1737, 2002.
- [109] A. Nakajima, T. Futatsugi, K. Kosemura, T. Fukano, and N. Yokoyama, "Room temperature operation of Si single-electron memory with self-aligned floating dot gate," *Appl. Phys. Lett.*, vol. 70, pp. 1742-1744, 1997.
- [110] B.J. Hinds, T. Yamanaka, and S. Oda, "Charge Storage Mechanism in Nano-Crystalline Si Based Single-Electron Memories," presented at Mat. Res. Soc. Symp. Proc., 2001.
- [111] A. Kuller, W. Eck, V. Stadler, W. Geyer, and A. Golzhauser, "Nanostructuring of silicon by electron-beam lithography of self-assembled hydroxybiphenyl monolayers," *Appl. Phys. Lett.*, vol. 82, pp. 3776-3778, 2003.
- [112] E. Adler, J.K. DeBrosse, S.F. Geissler, S.J. Holmes, M.D. Jaffe, J.B. Johnson, c.W. Koburger III, J.B. Lasky, B. Lloyd, G.L. Miles, J.S. Nakos, W.P. Noble Jr., S.H. Voldman, M. Armacost, and R. Ferguson, "The evolution of IBM CMOS DRAM technology," *IBM J. Res. Develop.*, vol. 39, pp. 167-188, 1995.
- [113] C. Li and W. A. Anderson, "Metal-Induced Grown Si Nanostructures for Large-Area-Device Applications," *IEEE Trans. Electron Dev.*, vol. 50, pp. 1885-1889, 2003.

Bibliography

- [114] N. Suzuki, T. Makino, Y. Yamada, T. Yoshida, and S. Onari, "Structures and optical properties of silicon nanocrystallites prepared by pulsed-laser ablation in inert background gas," *Appl. Phys. Lett.*, vol. 76, pp. 1389-1391, 2000.
- [115] A. Dutta, Y. Hayafune, and S. Oda, "Single Electron Memory Devices Based on Plasma-Derived Silicon Nanocrystals," *Jpn. J. Appl. Phys. Part II*, vol. 39, pp. L855-L857, 2000.
- [116] H. Grabert and M. H. Devoret, *Single Charge Tunneling, Coulomb Blockade Phenomena in Nanostructures*: Plenum, New York, 1992.
- [117] A. Thean, "Computer Modeling of Silicon Quantum Dot Floating-Gate Flash Memory Devices," University of Illinois at Urbana-Champaign, 2001.
- [118] R. Tsu, D. Babic, and J. L. Ioriatti, "Simple model for the dielectric constant of nanoscale silicon particle," *J. Appl. Phys.*, vol. 82, pp. 1327-1329, 1997.
- [119] L.W. Wang and A. Zunger, "Dielectric constants of silicon quantum dots," *Phys. Rev. Lett.*, vol. 73, pp. 1039, 1994.
- [120] M. Lannoo, C. Delerue, and G. Allan, "Screening in Semiconductor Nanocrystallites and Its Consequences for Porous Silicon," *Phys. Rev. Lett.*, vol. 74, pp. 3415-3418, 1995.
- [121] G. Allan, C. Delerue, M. Lannoo, and E. Martin, "Hydrogenic impurity levels, dielectric constant, and Coulomb charging effects in silicon crystallites," *Phys. Rev. B*, vol. 52, pp. 11982-11988, 1995.
- [122] C. Delerue, M. Lannoo, and G. Allan, "Concept of dielectric constant for nanosized systems," *Phys. Rev. B*, vol. 68, pp. 115411-1 - 115411-4, 2003.

Bibliography

- [123] W. Wu, J. Gu, H. Ge, C. Keimel, and S. Y. Chou, "Room-temperautre Si single-electron memory fabricated by nanoimprint lithography," *Appl. Phys. Lett.*, vol. 83, pp. 2268-2270, 2003.
- [124] Y. Ono and Y. Takahashi, "Electron pump by a combined single-electron field-effect transistor structure," *Appl. Phys. Lett.*, vol. 82, pp. 1221-1223, 2003.
- [125] C.Y. Ng, G.S. Lum, S.C. Tan, T.P. Chen, L. Ding, O.K. Tan, and A. Du, "An electrical study of behaviors of Si nanocrystals distributed in the gate oxide near the oxide/substracte interface of a MOS structure," *Thin Solid Films*, vol. 504, pp. 32-35, 2006.
- [126] D.N. Kouvatsos, V.I. Sougleridis, and A. G. Nassiopoulou, "Charging effects in silicon nanocrystals embedded in SiO₂ films," *Mat. Sci. Engineering B*, vol. 101, pp. 270-274, 2003.
- [127] Y. Martin, C.C. Williams, and H. K. Wickramasinghe, "Atomic force microscope-force mapping and profiling on a sub 100-A scale," *J. Appl. Phys.*, vol. 61, pp. 4723-4729, 1987.
- [128] G. Binnig, C.F. Quate, and C. Gerber, "Atomic Force Microscope," *Phys. Rev. Lett.*, vol. 56, pp. 930-933, 1986.
- [129] Q. Zhong, D. InnissK. Kjoller, and V. B. Elings, "Fractured polymer/silica fiber surface studied by tapping mode atomic force microscopy," *Surf. Sci. Lett.*, vol. 290, pp. L688-L692, 1993.
- [130] P. Girard, "Electrostatic force microscopy: principles and some applications to semiconductors," *Nanotechnology*, vol. 12, pp. 485-490, 2001.

Bibliography

- [131] W.A. Hofer, A.S. Foster, and A. L. Shluger, "Theories of scanning probe microscopes at the atomic scale," *Rev. Mod. Phys.*, vol. 75, pp. 1287-1331, 2003.
- [132] F. J. Giessibl, "Advances in atomic force microscopy," *Rev. Mod. Phys.*, vol. 75, pp. 949-983, 2003.
- [133] Veeco, "Dimension 3100 Manual," 2004.
- [134] M. Imaging. 4666 S. Ash Avenue, Tempe, Arizona 85282, U.S.A.
- [135] E.A. Boer, L.D. Bell, M.L. Brongersma, H.A. Atwater, M.L. Ostraat, and R. C. Flagan, "Charging of single Si nanocrystals by atomic force microscopy," *Appl. Phys. Lett.*, vol. 78, pp. 3133-3135, 2001.
- [136] E.A. Boer, M.L. Brongersma, H.A. Atwater, R.C. Flagan, and L. D. Bell, "Localized charge injection in SiO₂ films containing silicon nanocrystals," *Appl. Phys. Lett.*, vol. 79, pp. 791-793, 2001.
- [137] D.M. Schaadt, E.T. Yu, S. Sankar, and A. E. Berkowitz, "Charge storage in Co nanoclusters embedded in SiO₂ by scanning force microscopy," *Appl. Phys. Lett.*, vol. 74, pp. 472-474, 1999.
- [138] R.M. Nyffenegger, R.M. Penner, and R. Schierle, "Electrostatic force microscopy of silver nanocrystals with nanometer-scale resolution," *Appl. Phys. Lett.*, vol. 71, pp. 1878-1880, 1997.
- [139] T.D. Krauss and L. E. Brus, "Charge, polarizability and photionization of single semiconductor nanocrystals," *Phys. Rev. Lett.*, vol. 84, pp. 638, 2000.
- [140] C. Schonenberger and S. F. Alvarado, "Observation of Single Charge Carriers by Force Microscopy," *Phys. Rev. Lett.*, vol. 65, pp. 3162-3164, 1990.

Bibliography

- [141] N. Shimizu, M. Ikeda, E. Yoshida, H. Murakami, S. Miyazaki, and M. Hirose, "Charging states of Si quantum dots as detected by AFM/Kelvin probe technique," *Jpn. J. Appl. Phys. Part I*, vol. 39, pp. 2318, 2000.
- [142] B.D. Terris, J.E. Stern, D. Rugar, and H. J. Mamin, "Contact Electrification Using Force Microscopy," *Phys. Rev. Lett.*, vol. 63, pp. 2669-2672, 1989.
- [143] T. Melin, H. Diesinger, D. Deresmes, and D. Stievenard, "Electric force microscopy of individually charged nanoparticles on conductors: An analytical model for quantitative charge imaging," *Phys. Rev. B*, vol. 69, pp. 035321-1 - 035321-8, 2004.
- [144] J. Lambert, C. Guthmann, and M. S. Jean, "Relationship between charge distribution and its image by electrostatic force microscopy," *J. Appl. Phys.*, vol. 93, pp. 5369-5376, 2003.
- [145] L.J. Klein, C.C. Williams, and J. Kim, "Electron tunneling detected by electrostatic force," *Appl. Phys. Lett.*, vol. 77, pp. 3615-3617, 2000.
- [146] E.A. Boer, L.D. Bell, M.L. Brongersma, and H.A. Atwater, "Models for quantitative charge imaging by atomic force microscopy," *J. Appl. Phys.*, vol. 90, pp. 2764-2772, 2001.
- [147] C.Y. Ng, T.P. Chen, and M. S. Tse, "Electrical characteristics of ion-beam synthesized Si nanocrystals in SiO₂ matrix," in *Proc. ISIC-2004*, pp. 281-283, 2004.
- [148] G. Ammendola, V. Ancarani, V. Triolo, M. Bileci, D. Corso, I. Crupi, L. Perniola, C. Gerardi, S. Lombardo, and B. DeSalvo, "Nanocrystal memories for FLASH device applications," *Solid-State Electron.*, vol. 48, pp. 1483-1488, 2004.

Bibliography

- [149] R. Muralidhar, R.F. Steimle, M. Sadd, R.A. Rao, C.T. Swift, E.J. Prinz, J. Yater, L. Grieve, K. Harber, B. Hradsky, S. Straub, B. Acred, W. Paulson, W. Chen, L. Parker, S.G.H. Anderson, M. Rossow, T. Merchant, M. Paransky, T. Huynh, D. Hadad, K.M. Chang, and B. E. White, "A 6 V embedded 90 nm silicon nanocrystal nonvolatile memory," in *IEDM Tech. Dig.*, pp. 601-604, 2003.
- [150] H.-Ch. Weissker, J. Furthmuller, and F. Bechstedt, "Validity of effective-medium theory for optical properties of embedded nanocrystallites from ab initio supercell calculations," *Phys. Rev. B*, vol. 67, pp. 165332-1 - 165332-5, 2003.
- [151] L.N. Dinh, L.L. Chase, M. Balooch, W.K. Siekhaus, and F. Wooten, "Optical properties of passivated Si nanocrystals and SiO_x nanostructures," *Phys. Rev. B*, vol. 54, pp. 5029-5037, 1996.
- [152] T.P. Chen, Y. Liu, M.S. Tse, P.F. Ho, G. Dong, and S. Fung, "Depth profiling of Si nanocrystals in Si-implanted SiO₂ films by spectroscopic ellipsometry," *Appl. Phys. Lett.*, vol. 81, pp. 4724-4726, 2002.
- [153] S. M. Sze, *Semiconductor Devices Physics and Technology*: John Wiley and Sons, New York, 1987.
- [154] D. R. Penn, "Wave-Number-Dependent Dielectric Function of Semiconductors," *Phys. Rev.*, vol. 128, pp. 2093-2097, 1962.
- [155] L.W. Wang and A. Zunger, "Pseudopotential calculations of nanoscale CdSe quantum dots," *Phys. Rev. B*, vol. 53, pp. 9579-9582, 1995.
- [156] X. Cartoixa and L. W. Wang, "Microscopic Dielectric Response Functions in Semiconductor Quantum Dots," *Phys. Rev. Lett.*, vol. 94, pp. 236804-1 - 236804-4, 2005.

Bibliography

- [157] F. Giustino and A. Pasquarello, "Theory of atomic-scale dielectric permittivity at insulator interfaces," *Phys. Rev. B*, vol. 71, pp. 144104, 2005.
- [158] B. Garrido, S. Cheylan, O.G. Varona, A.P. Rodriguez, and J. R. Morante, "The effect of additional oxidation on the memory characteristics of metal-oxide-semiconductor capacitor with Si nanocrystals," *Appl. Phys. Lett.*, vol. 82, pp. 4818-4820, 2003.
- [159] Y. Liu, T.P. Chen, C.Y. Ng, M.S. Tse, P. Zhao, Y.Q. Fu, S. Zhang, and S. Fung, "Random capacitance modulation due to charging/discharging in Si nanocrystals embedded in gate dielectric," *Nanotechnology*, vol. 16, pp. 1119-1122, 2005.
- [160] A. Thean and J. P. Leburton, "Flash memory: towards single-electron," *IEEE Potentials*, vol. 21, pp. 35-41, 2002.
- [161] F. Iacona, C. Bongiorno, C. Spinella, S. Boninelli, and F. Priolo, "Formation and evolution of luminescent Si nanoclusters produced by thermal annealing of SiO_x films," *J. Appl. Phys.*, vol. 95, pp. 3723-3732, 2004.
- [162] A. Irrera, F. Iacona, I. Crupi, C.D. Presti, G. Franzo, C. Bongiorno, D. Sanfilippo, G.D. Stefano, A. Piana, P.G. Fallica, A. Canino, and F. Priolo, "Electroluminescence and transport properties in amorphous silicon nanostructures," *Nanotechnology*, vol. 17, pp. 1428-1436, 2006.
- [163] N. Daldosso, G. Das, G. Dalba, S. Larcheri, R. Grisenti, G. Mariotto, L. Pavesi, F. Rocca, F. Priolo, G. Franzo, A. Irrera, M. Miritello, D. Pacifici, and F. Iacona, "silicon nanocrystal nucleation as a function of the annealing temperature in SiO_x films," *MRS Proceedings* vol. 770, pp. 11.3, 2003.

Bibliography

- [164] V. E. Borisenko, *Rapid Thermal Processing of Semiconductor*. New York: Plenum Press, 1997.
- [165] P. Normand, E. Kapetanakis, P. Dimitrakis, D. Tsoukalas, K. Beltsios, N. Cherkashin, C. Bonafos, G. Benassayag, H. Coffin, A. Claverie, V. Soncini, A. Agarwal, and M. Ameen, "Effect of annealing environment on the memory properties of thin oxides with embedded Si nanocrystals obtained by low-energy ion-beam synthesis," vol. 83, pp. 168-170 2003.
- [166] E. Kapetanakis, P. Normand, D. Tsoukalas, and K. Beltsios, "Room-temperature single-electron charging phenomena in large-area nanocrystal memory obtained by low-energy ion beam synthesis," *Appl. Phys. Lett.*, vol. 80, pp. 2794-2796, 2002.
- [167] T. Baron, P. Gentile, N. Magnea, and P. Mur, "Single-electron charging effect in individual Si nanocrystals," *Appl. Phys. Lett.*, vol. 79, pp. 1175-1177, 2001.
- [168] L. Guo, E. Leobandung, and S. Y. Chou, "A room-temperature silicon single-electron metal-oxide-semiconductor memory with nanoscale floating-gate and ultranarrow channel," *Appl. Phys. Lett.*, vol. 70, pp. 850-852, 1997.
- [169] S. K. Sung, D.H. Kim, J.S. Sim, K.R. Kim, Y.K. Lee, J.D. Lee, S.D. Chae, B.M. Kim, and B. G. Park, "Single-Electron MOS Memory with a Defined Quantum Dot Based on Conventional VLSI Technology," *Jpn. J. Appl. Phys. Part I*, vol. 41, pp. 2606-2610, 2002.
- [170] G. Molas, B. DeSalvo, G. Ghibaudo, D. Mariolle, A. Toffoli, N. Buffet, R. Puglisi, S. Lombardo, and S. Deleonibus, "Single electron effects and

Bibliography

- structural effects in ultrascaled silicon nanocrystal floating-gate memories," *IEEE Trans. Nanotechnology*, vol. 3, pp. 42-48, 2004.
- [171] T.P. Chen, M.S. Tse, and X. Zheng, "Snapback behavior of the postbreakdown I-V characteristics in ultrathin SiO₂ films," *Appl. Phys. Lett.*, vol. 78, pp. 492-494, 2001.
- [172] T.P. Chen, M.S. Tse, X. Zheng, and S. Fung, "On the switching behavior of post-breakdown conduction in ultra-thin SiO₂ films," *Semiconductor Sci. Technology*, vol. 16, pp. 793-797, 2001.
- [173] T.P. Chen, M.S. Tse, C.Q. Sun, and S. Fung, "Post-Breakdown Conduction Instability of Ultrathin SiO₂ Films Observed in Ramped-Current and Ramped-Voltage Current-Voltage Measurements," *Jpn. J. Appl. Phys. Part I*, vol. 41, pp. 3047-3051, 2002.
- [174] S. Banerjee, S. Huang, and S. Oda, "Operation of Nanocrystalline-Silicon-Based Few-Electron Memory Devices in the Light of Electron Storage, Ejection, and Lifetime Characteristics," *IEEE Trans. Nanotechnology*, vol. 2, pp. 88-92, 2003.
- [175] S. Huang, S. Banerjee, R.T. Tung, and S. Oda, "Quantum confinement energy in nanocrystalline silicon dots from high-frequency conductance measurement," *J. Appl. Phys.*, vol. 94, pp. 7261-7265, 2003.
- [176] R. Bez, E. Camerlenghi, A. Modelli, and A. Visconti, "Introduction to Flash Memory," in *Proceedings of the IEEE*, vol. 91, pp. 489-502, 2003.
- [177] I. Motta, G. Ragone, O. Khouri, G. Torelli, and R. Micheloni, "High-Voltage Management in Single-Supply CHE NOR-Type Flash Memories," in *Proceedings of the IEEE*, vol. 91, pp. 554-568, 2003.

Bibliography

- [178] J.D. Choi, J.H. Lee, W.H. Lee, K.S. Shin, Y.S. Yim, J.D. Lee, Y.C. Shin, S.N. Chang, K.C. Park, J.W. Park, and C. G. Hwang, "A 0.15 μm NAND Flash Technology with 0.11 μm^2 Cell Size for 1 Gbit Flash Memory," *In IEDM Tech. Dig.*, 2000.
- [179] J.D. Lee, J.H. Choi, D. Park, and K. Kim, "Data Retention Characteristics of Sub-100 nm NAND Flash Memory Cells," *IEEE Electron Dev. Lett.*, vol. 24, pp. 748-750, 2003.
- [180] T. Hara, K. Fukuda, K. Kanazawa, N. Shibata, K. Hosono, H. Maejima, M. Nakagawa, T. Abe, M. Kojima, M. Fujiu, Y. Takeuchi, K. Amemiya, M. Morooka, T. Kamei, H. Nasu, W. Chi-Ming, K. Sakurai, N. Tokiwa, H. Waki, T. Maruyama, S. Yoshikawa, M. Higashitani, T. D. Pham, F. Yupin, and T. Watanabe, "A 146-mm/sup 2/ 8-gb multi-level NAND flash memory with 70-nm CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 161-169, 2006.
- [181] C. Park, S. Sim, J. Han, C. Jeong, Y. Jang, J. Park, J. Kim, K. Park, and K. Kim, "A 70nm NOR Flash Technology with 0.049 μm^2 Cell Size," *in VLSI Tech. Digest Technical Paper*, pp. 238-239, 2004.
- [182] W.D. Brown and J. E. Brewer, *Nonvolatile Semiconductor Memory Technology, A Comprehensive Guide to understanding and Using NVSM Devices*: Piscataway, NJ: IEEE Press, 1998.
- [183] D. R. Nair, N. R. Mohapatra, S. Mahapatra, S. Shukuri, and J. D. Bude, "Effect of P/E cycling on drain disturb in flash EEPROMs under CHE and CHISEL operation," *IEEE Trans. Dev. Materials Reliability*, vol. 4, pp. 32-37, 2004.

Bibliography

- [184] D. R. Nair, S. Mahapatra, S. Shukuri, and J. Bude, "Multi-level programming of NOR flash EEPROMs by CHISEL mechanism," 2004.
- [185] S. Mahapatra, S. Shukuri, and J. Bude, "CHISEL flash EEPROM. I. Performance and scaling," *IEEE Trans. Electron Dev.*, vol. 49, pp. 1296-1301, 2002.
- [186] N. R. Mohapatra, D. R. Nair, S. Mahapatra, V. Ramgopal Rao, S. Shukuri, and J. D. Bude, "CHISEL programming operation of scaled NOR flash EEPROMs-effect of voltage scaling, device scaling and technological parameters," *IEEE Trans. Electron Dev.*, vol. 50, pp. 2104-2111, 2003.
- [187] A. T. Wu, T. Y. Chan, P. K. Ko, and C. Hu, "A novel high-speed, 5-volt programming EPROM structure with source-side injection," *In IEDM Tech. Dig.*, vol. 32, pp. 584-587, 1986.
- [188] C. Kuo-Tung, C. Wei-Ming, C. Swift, J. M. Higman, W. M. Paulson, and C. Ko-Min, "A new SONOS memory using source-side injection for programming," *IEEE Electron Device Lett.*, vol. 19, pp. 253-255, 1998.
- [189] D. Ielmini, A. Ghetti, S. Beltrami, A. S. Spinelli, A. L. Lacaita, and A. Visconti, "Experimental and Monte Carlo analysis of drain-avalanche hot-hole injection for reliability optimization in Flash memories," *In IEDM Tech. Dig.*, pp. 7.1.1-7.1.4, 2003.
- [190] M. Depas, B. Vermeire, P. W. Mertens, R. L. V. Meirhaeghe, and M. M. Heyns, "Determination of Tunneling Parameters in Ultra-thin Oxide Layer Poly-Si/SiO₂/Si Structures," *Solid-State Electron.*, vol. 38, pp. 1465-1471, 1995.
- [191] C.Y. Ng, T.P. Chen, Y. Liu, C.Q. Sun, and S. Fung, "Influence of nitrogen on tunneling barrier heights and effective masses of electrons and holes at

Bibliography

- lightly-nitrided SiO₂/Si interface," *J. Appl. Phys.*, vol. 96, pp. 5912-5914, 2004.
- [192] A. Hadjadj, G. Salace, and C. Petit, "Fowler-Nordheim conduction in polysilicon (n⁺)-oxide-silicon (p) structures: Limit of the classical treatment in the barrier height determination," *J. Appl. Phys.*, vol. 89, pp. 7994-8001, 2001.
- [193] G. Pananakakis, G. Ghibaudo, R. Kies, and C. Papadas, "Temperature dependence of the Fowler-Nordheim current in metal-oxide-degenerate semiconductor structures," *J. Appl. Phys.*, vol. 78, pp. 2635-2641, 1995.
- [194] G. Salace, A. Hadjadj, C. Petit, and M. Jourdain, "Temperature dependence of the electron affinity difference between Si and SiO₂ in polysilicon (n⁺)-oxide-silicon(p) structures: Effect of the oxide thickness," *J. Appl. Phys.*, vol. 85, pp. 7768-7773, 1999.
- [195] A. Hadjadj, G. Salace, and C. Petit, "Fowler-Nordheim conduction in polysilicon (n⁺)-oxide-silicon (p) structures: Limit of the classical treatment in the barrier height determination," *J. Appl. Phys.*, vol. 89, pp. 7994-8001, 2001.
- [196] G. Pananakakis, G. Ghibaudo, R. Kies, and C. Papadas, "Temperature dependence of the Fowler-Nordheim current in metal-oxide-degenerate semiconductor structures," *J. Appl. Phys.*, vol. 78, pp. 2635-2641, 1995.
- [197] S. Horiguchi and H. Yoshino, "Evaluation of interface potential barrier heights between ultrathin silicon oxides and silicon," *J. Appl. Phys.*, vol. 58, pp. 1597-1600, 1985.

Bibliography

- [198] R. Luduke, E. Cartier, and A. Schenk, "Determination of the energy-dependent conduction band mass in SiO₂," *Appl. Phys. Lett.*, vol. 75, pp. 1407-1409, 1999.
- [199] J. DeBlauwe, "Nanocrystal nonvolatile memory devices," *IEEE Trans. Nanotechnology*, vol. 1, pp. 72, 2002.
- [200] H.I. Hanafi, S. Tiwari, and I. Khan, "Fast and Long Retention-Time Nanocrystal Memory," *IEEE Trans. Electron Dev.*, vol. 43, pp. 1553-1558, 1996.
- [201] J. DeBlauwe, M. Ostraat, M.L. Green, G. Weber, T. Sorsch, A. Kerber, F. Klemens, R. Cirelli, E. Ferry, J.L. Grazul, F. Baumann, Y. Kim, W. Mansfield, J. Bude, J.T.C. Lee, S.J. Hillenius, R.C. Flagan, and H. A. Atwater, "A novel, aerosol-nanocrystal floating-gate device for non-volatile memory applications," in *IEDM Tech. Dig.*, pp. 683-686, 2000.
- [202] E. Lusky, Y.S. Diamand, G. Mitenberg, A. Shappir, I. Bloom, and B. Eitan, "Investigation of Channel Hot Electron Injection by Localized Charge-Trapping Nonvolatile Memory Devices," *IEEE Trans. Electron Dev.*, vol. 51, pp. 444-451, 2004.
- [203] E. Lusky, Y.S. Diamand, I. Bloom, and B. Eitan, "Characterization of Channel Hot Electron Injection by the Subthreshold Slope of NROM Device," *IEEE Electron Dev. Lett.*, vol. 22, pp. 556-558, 2001.
- [204] B. Eitan, P. Pavam, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, "NROM: A novel localized trapping, 2-bit nonvolatile memory cell," *IEEE Electron Dev. Lett.*, vol. 21, pp. 543-545, 2000.
- [205] S. Lombardo, B. DeSalvo, C. Gerardi, and T. Baron, "Silicon nanocrystal memories," *Microelectronic Engg.*, vol. 72, pp. 388-394, 2004.

Bibliography

- [206] M.L. Green, E.P. Gusev, R. Degraeve, and E. L. Garfunkel, "Ultrathin (<4 nm) SiO₂ and SI-O-N gate dielectric layers for silicon microelectronics: Understanding the processing, structure, and physical and electrical limits," *J. Appl. Phys.*, vol. 90, pp. 2057-2121, 2001.
- [207] D.J. DiMaria, "Electron energy dependence of metal-oxide-semiconductor degradation," *Appl. Phys. Lett.*, vol. 75, pp. 2427-2428, 1999.
- [208] B. Prince, *Emerging Memories - Technologies and Trends*: Kluwer Academic Publishers, 2002.
- [209] R. H. Dennard, "Field-effect transistor memory," 1968.
- [210] A. Nitayama, Y. Kohyama, and K. Hieda, "Future Directions For DRAM Memory Cell Technology," in *IEDM Tech. Dig.*, pp. 355-358, 1998.
- [211] R. H. Dennard, "Evolution of the MOSFET dynamic RAM - A personal view," *IEEE Trans. electron Dev.*, vol. 31, pp. 1549-1555, 1984.
- [212] S. Okhonin, M. Nagoga, J.M. Sallese, and P. Fazan, "A Capacitor-Less 1T-DRAM Cell," *IEEE Electron Dev. Lett.*, vol. 23, pp. 85-87, 2002.
- [213] L. C. Tran, "Beyond Nanoscale DRAM and Flash - Challenges and Opportunities for Research in Emerging Memory Devices," in *Proc. IEEE Microelectronics and Electron Devices*, pp. 35-38, 2004.
- [214] F. Masuoka, M. Momodomi, Y. Iwata, and R. Shirota, "New Ultra High Density EPROM and Flash EEPROM with NAND structure cell," in *IEDM Tech. Dig.*, pp. 552-555, 1987.
- [215] I. Kim, S. Han, K. Han, J. Lee, and H. Shin, "Si nanocrystal memory cell with room temperature single electron effects," *Jpn. J. Appl. Phys.*, vol. 40, pp. 447-451, 2001.

Bibliography

- [216] E. Spitale, D. Corso, I. Crupi, S. Lombardo, and C. Gerardi, "Improvement of the P/E window in nanocrystal memories by the use of high-k materials in the control dielectric," *Microelectronics Reliability*, vol. 45, pp. 895-898, 2005.
- [217] E.S. Hasaneen, E. Heller, R. Bansal, W. Huang, and F. Jain, "Modeling of nonvolatile floating gate quantum dot memory," *Solid-State Electron.*, vol. 48, pp. 2055-2059, 2004.
- [218] A. Campera and G. Iannaccone, "Modelling and simulation of charging and discharging processes in nanocrystal flash memories during program and erase operations," *Solid-State Electron.*, vol. 49, pp. 1745-1753, 2005.

Appendix A

Fabrication steps for single-layer silicon nanocrystal embedded in SiO₂ thin film.

Step	Step Name	Description
0	Starting Wafer	P<100>, boron doped, 9-12 Ω-cm
1	Oxide growth	
1a	Preclean	Clean Recipe: 1. H ₂ SO ₄ /H ₂ O ₂ (4:1), 100 ± 5°C 10mins 2. Quick Dump Rinse 6 cycles 3. H ₂ O:HF(20:1), 12 s 4. Quick Dump Rinse 6 cycles 5. IPA Dry
1b	Oxidation	Multiple wafers: thickness = 300 ± 25 Å 5mins. Diluted dry Oxidation, 950°C 75mins. Dry Oxidation, 950°C 1mins. Diluted Dry Oxidation, 950°C 20mins. Anneal, N ₂ , 950°C
2	Si ⁺ implantation	Si-28, 7 degree, c/w 4 Quarter Imp (Energy range: 1 – 2 KeV) Wafer #1: 1 KeV, Dose: 1×10 ¹⁶ cm ⁻² Wafer #2: 1 KeV, Dose: 8×10 ¹⁶ cm ⁻² Wafer #3: 2 KeV, Dose: 2×10 ¹⁵ cm ⁻² Wafer #4: 2 KeV, Dose: 1×10 ¹⁶ cm ⁻²
3	Annealing	N ₂ ambient Various temperature: 500°C - 1100°C for 20mins
4	Patterning	Coating photo-resist Align and expose to UV (wavelength=365nm) Develop photo-resist and hard bake
5	Metal Deposition	Evaporation of Aluminum for 20mins
6	Strip Photo-resist	O ₂ ashing Nanostrip clean: 60°C for 10mins
7	Backside Metal Deposition	Aluminum = 1μm Front side wafers coated with photo-resist H ₂ O:HF(20:1) for 30 s Strip Photo-resist Metal Deposition
8	Metal Alloy	N ₂ 425°C for 20mins N ₂ +H ₂ 425°C for 25mins N ₂ 425°C for 2mins

Appendix A

Fabrication steps for wide distributions of silicon nanocrystal embedded in SiO₂ thin film.

Step	Step Name	Description
0	Starting Wafer	P<100>, boron doped, 9-12 Ω-cm
1	Oxide growth	
1a	Preclean	Clean Recipe: 1. H ₂ SO ₄ /H ₂ O ₂ (4:1), 100 ± 5°C 10mins 2. Quick Dump Rinse 6 cycles 3. H ₂ O:HF(20:1), 12 s 4. Quick Dump Rinse 6 cycles 5. IPA Dry
1b	Oxidation	Multiple wafers: thickness = 300 ± 25 Å 5mins. Diluted dry Oxidation, 950°C 75mins. Dry Oxidation, 950°C 1mins. Diluted Dry Oxidation, 950°C 20mins. Anneal, N ₂ , 950°C
2	Si ⁺ implantation	Si-28, 7 degree, c/w 4 Quarter Imp (Energy range: 5 – 10 KeV) Wafer #5: 5 KeV, Dose: 2×10 ¹⁵ cm ⁻² Wafer #6: 5 KeV, Dose: 1×10 ¹⁶ cm ⁻² Wafer #7: 8 KeV, Dose: 2×10 ¹⁵ cm ⁻² Wafer #8: 8 KeV, Dose: 1×10 ¹⁶ cm ⁻² Wafer #9: 10 KeV, Dose: 3×10 ¹⁶ cm ⁻²
3	Annealing	N ₂ ambient Various durations: 1000°C for 30-60mins
4	Patterning	Coating photo-resist Align and expose to UV (wavelength=365nm) Develop photo-resist and hard bake
5	Metal Deposition	Evaporation of Aluminum for 20mins
6	Strip Photo-resist	O ₂ ashing Nanostrip clean: 60°C for 10mins
7	Backside Metal Deposition	Aluminum = 1μm Front side wafers coated with photo-resist H ₂ O:HF(20:1) for 30 s Strip Photo-resist Metal Deposition
8	Metal Alloy	N ₂ 425°C for 20mins N ₂ +H ₂ 425°C for 25mins N ₂ 425°C for 2mins

Appendix A

Fabrication steps for silicon nanocrystal distributed throughout the entire in SiO₂ thin film.

Step	Step Name	Description
0	Starting Wafer	N<100>, Phosphorous doped, 9-12 Ω-cm
1	Oxide growth	
1a	Preclean	Clean Recipe: 1. H ₂ SO ₄ /H ₂ O ₂ (4:1), 100 ± 5°C 10mins 2. Quick Dump Rinse 6 cycles 3. H ₂ O:HF(20:1), 12 s 4. Quick Dump Rinse 6 cycles 5. IPA Dry
1b	Oxidation	Multiple wafers: thickness = 300 ± 25 Å 5mins. Diluted dry Oxidation, 950°C 75mins. Dry Oxidation, 950°C 1mins. Diluted Dry Oxidation, 950°C 20mins. Anneal, N ₂ , 950°C
2	Si ⁺ implantation	Si-28, 7 degree, c/w 4 Quarter Imp (Energy range: 14 KeV) Wafer #10: 14 KeV, Dose: 3×10 ¹⁶ cm ⁻²
3	Annealing	N ₂ ambient Various durations: 1000°C for 30-60mins
4	Oxide Etch	Wet etching H ₂ O:HF(50:1) for 90 s (etch rate 10 nm/mins) Quick Dump Rinse 6 cycles IPA Dry
5	Patterning	Coating photo-resist Align and expose to UV (wavelength=365nm) Develop photo-resist and hard bake
6	Metal Deposition	Evaporation of Aluminum for 20mins
7	Strip Photo-resist	O ₂ ashing Nanostrip clean: 60°C for 10mins
8	Backside Metal Deposition	Aluminum = 1μm Front side wafers coated with photo-resist H ₂ O:HF(20:1) for 30 s Strip Photo-resist Metal Deposition
9	Metal Alloy	N ₂ 425°C for 20mins N ₂ +H ₂ 425°C for 25mins N ₂ 425°C for 2mins