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A High-Speed CMOS Pipelined Subranging ADC

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in fulfillment of the requirement for the degree of
Doctor of Philosophy

2006

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

28, Oct, 2006

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ABSTRACT

ABSTRACT

This dissertation presents a new 10-bit subranging analog-to-digital converter (ADC) dedicated for high-speed low-power application. The proposed architecture includes one coarse ADC plus two interleaved fine ADCs incorporating with pipeline and doubling sampling techniques. Contrasting to conventional subranging architectures, the system maximizes the throughput via elimination of extra idle time and eliminates a sample-and-hold (S/H) circuit. Besides, a new sliding feedback capacitor technique, using time constant reduction concept, is proposed to enhance the speed of coarse ADC. A synchronized switch is introduced to minimize the sample-time mismatches so as to reduce nonlinearity arising from interleaving action. Other well-established circuit techniques like bottom-plate sampling, distributed sampling, autozeroing, and interpolation are employed for complete ADC design. The critical building blocks such as the preamplifier for core ADC and source followers for design of input buffer for high-speed ADC testing are thoroughly analyzed to show the origin of nonlinearity. The realistic HSPICE simulations using Level 49 BSIM3 models are used to confirm the second-order analysis. The prototype ADC is fabricated in 0.35 μm CMOS process and achieves 52 dB SNDR for a 10MHz input frequency at 150MS/s. Without calibration, the measured differential nonlinearity (DNL) is ± 0.5 LSB and the integral nonlinearity (INL) is ± 0.9 LSB. The ADC occupies an active area of 2.7 mm^2 , consuming only 178 mW at a single 3V supply. The Figure of Merit (FOM) of the proposed ADC is the best among other high-speed subranging ADCs and compares favorably with other state-of-art ADC architectures, thus validating it can achieve very good optimal performance parameters and meet the ultimate objectives of this research work.

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CHAPTER 1

INTRODUCTION

An introduction of analog-to-digital converter (abbreviated ADC or A/D converter) is given in this chapter. First, a general background pertaining to high-speed ADC is presented, including design motivations and difficulties. Next, the objectives of this research project are presented, which is followed by the contributions. Finally, the organization of this thesis is stated at the end of this chapter.

1.1 Background

The rapid development of integrated circuit is derived mainly from successive improvement in device miniaturization and the concomitant increase in device density and circuit complexity on a single chip. Functionality per chip has grown in accordance with Moore's law, an historical observation made by Intel executive Gordon Moore. Moore's law states that functionality as measured by the number of transistors per square millimeter of silicon doubles every one and a half years. At the same time, transistors become faster, making ever-increasing clock rates in digital circuits. So far, digital circuits have achieved speed of up to many hundreds of MHz or even GHz while

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consuming acceptable power with the continuous advance of semiconductor technology and scaling of devices. This trend seems to continue for at least another decade without slowing down. Thus, in the near future, the processing power of digital circuits will continue to increase at an accelerating pace. On the other hand, the analog circuit does not benefit significantly from precision point of view in the tremendous progress of microelectronics.

Fig. 1.1 Interface between Physical World and a Digital Signal Processor

For these reasons, more and more applications, which have been traditionally implemented in analog domain, are being replaced with digital signal processing (DSP) techniques whenever possible, such as digital audio and wireless cellular phones. However, the input or output signals of a system still remain analog representations when interfacing with the real world, which blocks entire digital realization. Fig. 1.1 shows a typical application system. The physical world is in analog domain because many signal sources are in analog form, for example the speakers in mobile phones, analog input signal in computer monitors, the RF signals in space and at the antenna. Thus, analog-to-digital converters and digital-to-analog converters (DAC or D/A converter) provide a link between the digital signal processor and the analog signals. A/D converter converts an

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analog signal into a digital quantity with a prescribed number of bits, whereas D/A converter is used to reproduce the analog signal after digital signal processing.

The digital signal processing has developed rapidly over the past 20 years. New DSP architectures allow complex algorithms to be implemented at high computation. Under this scenario, analog-digital interface must be able to match the resolution and the speed of the DSP. The present trend pushing the border of digital conversion towards the transmit-and-receive terminal leads to ever increasing demands on specifications, namely speed and resolution. This causes the practical limitations such as the speed and accuracy in the high-speed operation of the data converters. In general, the implementation of A/D converter is more difficult than D/A converter in terms of speed, resolution and power consumption. Thus, analog-to-digital converters continue to play a vital role that dictates the performance of the whole system. Therefore, it is extremely necessary to conduct advanced research on investigating A/D conversion algorithms, architectures and circuits to overcome the above limitations.

Using sub-micron technologies, it is possible to integrate millions of transistors either on a smaller number of chips or the ultimate goal of system on chip (SOC). Hence, the trend of ADC design implicates that A/D converter will serve as an embedded core with other parts of the system having a lot of digital circuitry. Bipolar and CMOS in silicon are the two mainstream semiconductor technologies. Bipolar transistors can operate at higher frequencies than CMOS counterpart with relatively larger transconductance g_m . However, digital circuits in bipolar technology are power hungry,

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prohibiting very large scale integration. Therefore, bipolar technology is suitable for pure analog integration with relatively high operating speed (such as RF circuits) or relatively high power (such as asymmetric digital subscriber line (ADSL) drivers) applications. CMOS technology has offered very large scale integration for both high-density digital circuits (such as DSP and memory) and analog circuits (including amplifiers, filters, A/D and D/A converters) to meet low-cost low-power objective. Another advantage of MOS technology is the implementation of quality switch, which is very useful for sample-data circuits, such as switched-capacitor filters and A/D & D/A converters. With the emergence of new CMOS technologies having smaller feature sizes (such as $0.25\mu\text{m}$, $0.18\mu\text{m}$ or below), not only do they exhibit smaller switch errors, they can operate at increasingly high-speed (5GHz) environment, which is comparable to some bipolar counterparts. BiCMOS technology is the combination of the above two, which has both CMOS and bipolar transistors. It benefits both merits of CMOS and bipolar technologies but at the expense of higher manufacturing cost due to required extra processing steps. For reasons of low cost, low power consumption and high integration density, CMOS technologies become the mainstream technologies for mixed-signal system design. It is of particular challenge that if such CMOS A/D converters are fabricated in a standard CMOS technology (not having small feature size of $0.25\mu\text{m}$ or below) whilst achieving good resolution at a sampling rate of 100 MHz or above.

Table 1.1 shows some applications of high speed A/D converter. For modern communication, there is at least 10 bits resolution but it is hardly to find a sampling rate higher than 100MHz. It is not easy to achieve in typical submicron CMOS process. On

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the contrary, when resolution is lower than 10 bits, a number of ADCs [1]-[2] has been reported with sampling rate up to hundreds of MHz. Although the need for increasing conversion rate and resolution can be relieved with the advanced process, the costs tend to be higher, and it is not always favorable for analog design due to strong second-order effects. In this way, the increasing demand for speed and resolution sometimes beyond what the advance process can provide. Thus, there is a need to investigate the ADC architecture that offers the most optimum trade off solution, which can be assessed through figure of merit.

Table 1.1 Application for High-Speed A/D Converters [3]

Application	Hard Disks	Flat panel displays	Imaging	Communications	
				Base Station	Wireline, Modems
Resolution	6bit	8bit	10bit	10-12bit	12-14bit
Sampling Rate	>500MHz	>100MHz	>30MHz	>50MHz	>5MHz

The ADC architecture is one of the key system design considerations. The choice or research of ADC architecture is strongly related to the design specifications and applications. This is translated to the system design that should provide strategic emphasis on particular performance parameters as the ultimate goal. Each of the well-established ADC architectures has its own place in the resolution – bandwidth picture as illustrated in Fig. 1.2. Of particular interest, the speed-resolution trade off of high-speed

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ADCs can be roughly divided into three groups: Flash, folding/two step/subranging, pipelined architectures.

Fig. 1.2 Speed-Resolution Trade Off with Various ADC Architectures [4],[5]

Fig. 1.3 Power/Fs vs CMOS Technology

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The performance of the A/D converters is enhanced with the evolution of CMOS process technology. Fig. 1.3 summarizes the relationship between the power consumption per sampling rate (Power/ F_s) against the channel length in CMOS technology [1]-[2],[6]-[43]. The Power/ F_s decreases with the scaling of CMOS technology under the same resolution. In addition, the higher the resolution, the larger the power consumption per sampling rate.

In addition to technology and architectures, the circuit techniques also play an important role in the design of A/D converter. Since ADC is a sampled-data system, it requires the use of circuit techniques that can handle discrete-time analog signals. Depending on whether the analog signals are voltages or currents, the circuits are often divided into voltage mode [40],[44] or currents mode circuits [44],[45]. The switched-capacitor (SC) technique is usually used for voltage mode circuits whilst the switched-current (SI) technique is used for current mode circuits. A sample-and-hold (S/H) circuit is often needed in most of the ADC system, which samples the input signal and stores the signal value for a certain amount of time when a hold command is given. There are a number of effects (such as acquisition time, linearity, pedestal error, feedthrough error, etc.) that will degrade the performance of a S/H circuit.

For ADC design, operational amplifier (opamp) and comparators are the fundamental building blocks. Opamps appear in sampling circuits, analog subtractors, gain stages and pipelined circuit etc, with each application imposing a different set of requirements on their speed, gain, linearity, noise, dynamic range and power

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consumption. It is common to find single-stage opamp or multi-stage opamp. Single-stage opamp topology is often the fastest and most power-efficient structures in high-speed ADC applications, but at the cost of lower DC gain which greatly limits the accuracy as well as linearity. In general, multi-stage opamp topology can achieve higher DC gain but requiring somewhat more power to achieve the same bandwidth as that of single-stage opamp. Multi-stage opamp architectures are not well suited for high-speed high-accuracy ADC due to extra zero and pole. Thus, the amplifier topology is the critical block in the ADC design because of directly impacting on performance parameters such as speed, power, accuracy and linearity. Along with amplifier, the high-speed comparator plays another important role in the high-speed ADC design. In particular, flash and two-step architectures require great attention to constraints imposed on the overall system by the large number of comparators. Most such converters utilize voltage comparison, rather than current comparison because distributing a voltage to a large number of comparators is easier. The natural choice to design a comparator is to use an amplifier, so called amplifier-type comparator. To have a fast comparison, latch-type comparator is a common choice, which manually incorporates positive feedback to attain virtually infinite gain and fast speed. Despite of this advantage, there are many practical issues such as gain, offset, kickback noise encountered in the comparator design. All these parameters will affect the performance of ADC. Thus, the comparator is another key building block that must be addressed strictly for successful ADC design.

The trend in ADC design has always been towards higher speed, higher accuracy and lower power target. Non-ideal effects such as offset mismatch, nonlinearity, and

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finite intrinsic gain limit the raw resolution to approximately 6 bits in CMOS technology and 10 bits in bipolar technology [46]. For higher resolution objective, it is often necessary to establish the correction means. Techniques like auto-zero [47], averaging [48], trimming [46] and error correction logic [46] are popular. For this reason, the ADC in this project will address reliable correction techniques for meeting the design objective whilst maintaining simplicity and reducing hardware overhead.

Fig. 1.4 Unity Current Gain Frequency (F_t) vs Channel Length of CMOS process [49]

Although the performance of ADC can be improved through proper architecture incorporating with circuit techniques and correction means, there still exists challenges in the ADC design. First, the implementation of high-speed A/D converter in a CMOS technology will make the design more difficult due to the small g_m of MOS transistor when compared with their counterpart in bipolar process. Together with poor MOSFET device matching, it is hard to achieve similar speed and resolution as compared to bipolar A/D converter. Fig. 1.4 shows that the typical unity current gain frequency (F_t) of NMOS device increases with decreasing channel length. Although continuous device scaling

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improves the speed of MOSFETs, it creates another problem in MOSFET device miniaturization: parameter fluctuation, which causes offset and nonlinearities issues. As device dimensions continue to shrink, random fluctuations in device parameters become more pronounced such that they dictate device performance. In other words, the smaller a device becomes, the less robust its performance is to small processing variations. Consequently, within the chip, there can be a significant variation in the device threshold voltage and aspect ratio, which raises the challenge to the ADC design that of increasing the speed through scaled technologies whilst yet not jeopardizing the circuit sensitivity. In addition, the source and drain series resistances cannot be ignored with the device minimization. In long-channel devices, it is common to ignore the source and drain region resistances with respect to the channel resistance. However, as a device is scaled to ultra submicron dimensions, the source–drain series resistance can become appreciable relative to the channel resistance. As a result, the current drive or speed of the device is degraded, thus adding design constraints to the high-speed ADC.

Fig. 1.5 Power Supply Scaling as a Function of Process Scaling [4],[5]

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Besides, the development of ADC has followed a trend of descending supply voltage [5]. There are two drivers for voltage scaling: technology and power. Refer to Fig. 1.5, the shrinking technology feature size leads to lower break down voltages and thus supply voltage scaling is mandatory. For a long time, the power supply has been 5V. The migration to a 3.3V supply has started another trend that almost every new process generation has a lower nominal supply voltage than its predecessor. For example, the 0.25 μm process generation utilizes a 2.5V supply. Potential high power consumption of ADC gives another rationale for reducing power supply. It is also because if the power consumption is high, expensive packaging is required. In practical application example, low power ADC benefits product life and reliability. As a result, market continues to demand high-speed ADC with power dissipation as low as possible. Despite reducing the power supply as one of the popular approaches to decrease the power consumption, the supply voltage scaling presents another challenge of ADC design. Not only does it lower the circuit speed, it also decreases the signal-to-noise ratio and limit the signal swing, thus restricting the operation of opamps and MOS switches. All these effects will deteriorate the performance of ADC. In this issue, the power efficiency of an ADC can be assessed with figure of merit for performance index. Therefore, the above observation underscores the importance of research and development to improve A/D conversion algorithms and circuits for future applications.

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1.2 Objectives

The objectives of the project are as follows:

- 1) To investigate system architecture and circuit techniques for designing a new high-speed CMOS A/D converter that permits an optimum tradeoff solution among speed, resolution and power consumption using typical submicron CMOS technology for high-speed low-power design.
- 2) To perform the second-order analysis for the critical design building blocks that affect the proposed ADC significantly.
- 3) To design, simulate, layout and test the proposed ADC.
- 4) To compare the new ADC with other state-of-art works.

1.3 Major Contributions of this Thesis

A number of contributions have been made. The contributions of this thesis are summarized as follows:

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- 1) The design of a 150 MS/s 10 bits pipelined subranging analog-to-digital converter (ADC) dedicated for high-speed low-power application.
- 2) In system design contribution, an internal pipelined scheme incorporating with the double sampling and interleaving techniques is proposed. It enables the ADC to sample the input signal on consecutive clock without adding a sample-and-hold (S/H) circuit whilst yet maximizing the throughput through elimination of idle time.
- 3) In circuit design contribution, a new sliding feedback capacitor technique is proposed in the multistage preamplifier design, which results in enhancing the speed of the coarse ADC.
- 4) The thesis contributes the analysis of non-ideal effects on the preamplifier which is identified as the critical building block for high-speed comparator in the ADC design.
- 5) The thesis contributes the large-signal analysis of nonlinear MOS source followers, which gives significant insight and understanding on how the non-ideal effects impacting on the nonlinearity of input buffer and provides useful guidelines for designing the quality input interface of the ADC for meeting stringent testing purpose.

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1.4 Organization of the Report

The thesis is organized as follows. Chapter 1 introduces the background of the project, which describes motivations and design challenge for the design of a high-speed ADC with standard sub-micron CMOS process. The objectives and contributions of this project are also presented. Chapter 2 reviews a number of high-speed ADC architectures and gives the limitations of each type. Chapter 3 proposes the new subranging ADC architecture together with its system design issues. In Chapter 4, the design of comparator is discussed and a high-speed multistage preamplifier with a new sliding capacitor technique is proposed. Chapter 5 gives the design of comparison block which includes coarse and fine comparison block. Its nonlinearity is analyzed to understand the fundamental limitations. Chapter 6 describes the design of other circuit building blocks such as reference ladder, clock generator, ROM and decoding circuits. Chapter 7 deals with the design of I/O interface circuit which is based on the study of different source followers for input buffer interface design so as to achieve the purpose of ADC testing. In Chapter 8, the floor plan of ADC and critical layout issues are discussed. Chapter 9 presents the results and discussions for preamplifier, sample insensitive interleaved design, buffer design and complete ADC. The concluding remarks and recommendations for the future work are given in Chapter 10.

CHAPTER 2

REVIEW OF HIGH SPEED ADC ARCHITECTURES

In this chapter, a number of ADC architectures suited for high-speed operation are reviewed. They are flash, pipelined, folding and subranging ADCs. Their speed-resolution-power trade off are studied. In addition, the performance of recently published ADCs and their figure of merit (FOM) are also compared.

2.1 Flash ADC Architecture

Flash A/D conversion is the fastest conversion technique. Many research works [6]-[13] about this architecture have been published. It uses the most straightforward way to perform the A/D conversion by comparing the input signal with different reference levels directly. Fig. 2.1 shows the block diagram of an N-bit flash ADC. The two-input comparator is connected with analog input and reference voltage respectively. The reference voltages for the comparators are generated using a resistor ladder. The positive (V_{REF+}) and the negative (V_{REF-}) reference voltage of resistor ladder determines the full-scale signal range and each reference level needs to be one LSB apart from each other.

CHAPTER 2 REVIEW OF HIGH SPEED ADC ARCHITECTURES

For N-bit resolution, 2^N-1 comparators simultaneously evaluate the analog input with the proper reference voltage and generate the digital output as a thermometer code, where all the bits below the comparator whose reference is the first to exceed the signal value are ones, while the bits above are all zeros. The thermometer codes from these comparators are encoded to N-bit binary word in digital output by the encoding circuitry.

The most important advantage of the flash architecture is its high throughput rate. The speed is very fast since the input signal is directly connected to the inputs of the comparators, and it only needs one clock cycle per conversion. Thus, the speed is only limited by the comparator. Consequently, the fastest ADCs reported so far are realized with this architecture [14]-[15]. Flash ADC has very low latency because it needs only one clock cycle per conversion. Moreover, since references are made by a resistor string, they are monotonic, resulting in low differential nonlinearity.

However, the hardware complexity of this architecture increases exponentially with the resolution because it needs a 2^N-1 comparators circuits for N-bit resolution, which is the major drawback when N is large. This also means that the power consumption and the chip area increase exponentially with the resolution. Hence, high-resolution flash ADCs are not practical. The second drawback is that the input must drive large capacitive load. Thus, large signal distortion may occur due to the nonlinearity of the input capacitance. The third disadvantage is that mismatch in the resistor reference ladder as well as unequal offset voltages of comparators, which will increase the DNL. Furthermore, the feedthrough of the analog input to the resistor ladder, location-

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dependent reference node time constants, incoherent timing of comparators over a large area also limit the resolution of flash ADC.

Fig. 2.1 N-bit Flash ADC

These drawbacks limit the flash architecture for high resolution applications [46]. Although circuit techniques such as employing auto-zero to reduce offset, adding preamplifier [50] before a latch to relax the resolution requirement for comparator, and incorporating interpolation [51] to reduce the input capacitance load, they cannot significantly reduce the exponentially increased hardware in the flash conversion or push it to even higher resolution. Typically, resolutions are reported for seven bits or below with a sampling rate of several hundred megahertz. Even gigahertz rates seem to be

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within the reach of state-of-the-art CMOS technologies [14]-[15]. Recently, flash ADCs have been used widely in disk drive read channel circuits [2] and local area network interfaces.

2.2 Pipelined Architecture

One popular way to avoid the exponentially increased hardware is to use pipelined architecture [52]-[55]. A typical pipelined ADC architecture is shown in Fig. 2.2. The whole operation is separated into several stages, and each stage consists of a S/H circuit, a k-bit flash ADC, a reconstruction DAC, a subtractor and a residue amplifier. With the aid of S/H, pipelining technique is applied among stages to achieve higher operation with the linear increased hardware. The analog input is applied to the first stage whilst other stages sample the output from the previous stage. Each stage quantizes to k bits digital codes using a flash ADC architecture. The codes are then converted to analog signal by k-bit DAC and subtracted from the sampled signal. The residue is then amplified and passed to the following stages. The output register combines the output bits from each stage and gives the final digital codes. Stage 1 gives MSBs whilst stage M gives the LSBs. The later the stage is, the less significant the bits are because of the gain factor in each stage.

Pipeline A/D converter takes M cycles to process each input signal, a new sample can be entered in the pipelined chain upon each clock. The pipelined architecture offers a

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number of advantages. First, the throughput rate is high because it is determined by the speed of only one stage in the pipeline. Second, the inter-stage residue amplification relaxes the precision required for subsequent stages. Third, the complexity is only proportional to M , which consumes small area, low power dissipation and low input capacitance. Hence, the power and hardware of pipelined converters grow almost linearly with the number of bits. Finally, the overlap and digital correction [56] can be used to overcome large offsets in the comparators.

Fig. 2.2 Pipeline ADC

The primary drawback of the conventional pipelined topology is the need for high precision inter-stage sample-and-hold amplifier (SHA) and residue amplifier, especially at the front end, where the accuracy requirements are most stringent. The precision

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typically mandates the use of operational amplifiers, imposing potential severe trade-offs among speed, voltage swing, gain, and power dissipation. The implementation using high-gain high-bandwidth amplifier becomes increasingly more difficult with the increase of speed and decrease of power supply. In addition, precise DAC and linear subtraction are also needed, which present challenges for the design. Although these difficulties can be relieved partly by advanced process, the cost is expensive. For relaxing the design requirements, another method is to employ sophisticated error correction scheme [57]-[62], but it is at the cost of high power dissipation and larger silicon area. Typically, the resolutions are reported for 8~12 bits with a sampling rate of several ten megahertz in CMOS process. The sampling rate of pipelined ADC can be further improved to hundred megahertz with the aid of interleaving technique. A 200 MSample/s 10 bits pipelined ADC [38] has been reported with four interleaving channels. However, the harmonic distortion is increased due to the non-ideal effects in multi-channel interleaving action.

2.3 Folding and Interpolating Architecture

Another approach to reduce the number of comparators as well as increasing the resolution is resorting to the folding ADC [63]-[66] as shown in Fig. 2.3. The folding converter consists of a coarse converter and a fine converter. The fine converter has an extra analog preprocessing block that folds the input back into range so that it permits more precise estimate on the input signal without a prior knowledge of the input subrange

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values. A folding A/D converter coarsely quantizes the incoming signal by a coarse ADC to generate the MSBs. The fine ADC with the folding circuit operates simultaneously with the coarse quantizer [25] as well as provides conversion to LSBs. As a result, the input signal is concurrently processed by the coarse flash converter, folding circuitry and fine flash converter. This arrangement obviates the need for a S/H between the coarse and fine quantizer by forming the residue signal without going through an A/D-D/A combination, which leads to faster operation. Generalizing this relationship, if the fine and coarse converter resolve the same number of bits, the number of comparators required is greatly reduced to $2 \cdot 2^{N/2}$ when compared with the flash ADC.

Fig. 2.3 Folding ADC

As mentioned before, one of the critical disadvantages of the flash topology is the large input capacitance. This problem can be alleviated by applying interpolation as shown in Fig. 2.4. The idea is that if V_{in} crosses $(V_{r,j} + V_{r,j+1})/2$, V_{o3} crosses zero, thus

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increasing the resolution by a factor of two. In essence, interpolation adds zero crossings to the set of input/output characteristics of a flash stage.

Fig. 2.4 Interpolation ADC

The interpolation A/D converter [67] makes use of input amplifier. The output of preamplifier can be interpolated by resistors. The architecture that combines folding and interpolation is popular because of its simplicity and speed. However, a well-known problem in this architecture is that the folding frequencies of the internal signals are equal to the multiplication of the frequency of the input signal times the folding rates, which is much higher than the frequency of the incoming signal. Thus, the bandwidth required for folding circuit is the folding rate times that of the maximum input frequency, thereby imposing strong trade off among speed, gain, and power consumption. In this aspect,

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folding converters are not as fast as pure flash converters because of the speed-limited folding circuitry [67]. As a result, the performance typically begins to degrade at relatively low signal frequencies. As a consequence, in high speed systems, the folding factor is typically 2~4. The problem can be alleviated by using an S/H circuit in front of the converter. However, it may defeat the speed advantage. In distributed track-and-hold approach [64], each differential pair in the folding amplifier has its own preamplifier with track-and-hold circuit, which has less stringent specifications than a front-end S/H circuit would have. Consequently, a higher speed can be achieved. Another problem of folding ADC is its nonlinearity due to the deviation of actual folding characteristic from a straight line, especially in high speed application.

Fig. 2.5 CMOS Folding Amplifier with Differential Current Output

Folding ADC is implemented primarily in bipolar technology. The smaller offset, high speed switching and exponential I-V characteristics of bipolar transistor allow higher resolution. On the contrary, in CMOS technology, large offsets, low device

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transconductance and short-channel effect make it difficult to increase resolutions. A CMOS implementation of the folding amplifier is shown in Fig. 2.5 [63]. It produces a four-times-folded differential current signal with five differential pairs. The interpolation between two folders can be realized with a resistor ladder.

The resolution of the folding-and-interpolating ADCs reported has typically been in the 8 to 10 bits region and the sampling rates from some dozens of MHz to a hundred MHz. A sampling rate as high as 400-MS/s has been achieved [66] but with 6-bit resolution using 0.5 μm CMOS technology. With the employment of background self-calibration to cancel the offsets of the folding amplifiers, the resolution of CMOS realizations can reach 10 bits. In addition, techniques such as averaging [48],[63], and self calibration [64] are commonly used to reduce offset sensitivity, but they add the complexity significantly.

2.4 Two-step Subranging ADC Architecture

In order to avoid the limitation of pipeline and folding architecture in high speed application, subranging architecture enables potentially faster conversion [41],[68]. The simple example of a 4-bit subranging ADC is shown in Fig. 2.6, which comprises of a 2-bit coarse flash ADC and a 2-bit fine flash ADC. The same reference resistor ladder provides both coarse and fine reference voltages. The coarse conversion generates the 2-

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bit MSBs as well as controls a multiplexer (MUX) to select the proper segment of reference ladder for fine conversion. Then, the input voltage compares with the selected reference voltages and generates the 2-bit LSBs of the ADC output to complete the digital output code.

Fig. 2.6 4-bit Conventional Subranging ADC

In two-step subranging, the number of comparators can be reduced from $2^N - 1$ to $2(2^{N/2} - 1)$, assuming that the number of bits determined in each sub-ADC is the same. Thus, it gives a significant reduction in power, die area, and input capacitance. More importantly, there is neither precise linear subtraction nor high-speed high-gain amplifier is required. In addition, SHA and exact gain stages are also not needed, which not only save power but also relieving the requirement for gain stage design. Therefore, this gives the possibility of subranging ADC achieving 10-bit resolution with high speed whilst yet no trimming and calibration are needed for obtaining acceptable INL and DNL values.

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Recently, a 10-bit subranging ADC incorporating with S/H circuit has been reported [43]. However, it cannot attain the high speed objective because of the use of high-gain high-bandwidth amplifier in the S/H circuit. One way to relax this limitation is to use bottom-plate sampling technique, which is widely used in high speed subranging ADC due to the elimination of high-gain high-bandwidth amplifier [46],[69]. With interleaving techniques, an ADC can be sampled at 100 MS/s with 8-bit resolution [39] in a 0.4 μm CMOS technology.

2.5 Time-Interleaved Architecture

In the architectures discussed above, the conversion rate is still limited by the settling time and accuracy requirements. When even higher conversion speed is desired, parallelism needs to be applied to further enhance the throughput rate. Time interleaving technique was used in four-channel [70],[38] as well as two-channel ADC [71]-[73]. Fig. 2.7 shows a system view of the architecture for time-interleaved A/D converter. If N channels are used, each channel is operated at frequency of F_S/N , where F_S is the system overall sampling frequency. Each channel incorporates a SHA that tracks for T/N seconds and holds for $(N-1)T/N$ seconds. Thus, each sub-ADC is allocated $(N-1)T/N$ seconds for one conversion. The front-end S/H must be sufficiently faster than the A/D conversion of ADC. An analog multiplexer and a digital multiplexer are used at the input and the output of the system. The throughput of the system is increased by N times at the cost of increasing hardware.

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Fig. 2.7 Time Interleaved ADC

The most critical problem that needs to be solved in this technique is on how to improve the matching between channels, such as offset mismatch, gain mismatch and sample-time mismatch [74]-[75]. This directly affects the highest resolution and the distortion [75].

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2.6 Study of Previous Works

It is desirable to understand the power efficiency of the ADC in the context of power, technology and performance. According to [76], ADC is evaluated in the form of a power figure of merit. It is given by:

$$FOM = \frac{2^B f_s}{Pf_t}$$

where P is power dissipation, B is number of bits, f_s is sample rate and f_t is effective device unity current gain frequency. The higher the number in FOM, the better power efficiency the ADC is.

Table 2.1 shows the recent research for high-speed ADC with different CMOS process technologies. It is observed that their conversion rate is larger than 100 MHz. The resolution is between 6-bit to 10-bit. It is obvious that there is always a trade off between the conversion rate and resolution. For example, the one [14] with 1300 MS/s conversion rate only attains 6-bit resolution, whilst another one with 10-bit resolution [20][31]-[32],[38] only has conversion rate in range of 100 MS/s ~200 MS/s. Besides, the power consumption increases with the increase of the conversion rate and resolution. For example, when conversion rate is higher than 1 GS/s [11], the power consumption can reach 1150 mW, but when the resolution increases to 10-bit [20] at 100 MS/s, the power consumption only needs 310 mW.

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Table 2.1 Performance of High-Speed ADCs

Reference	Conversion rate	Resolution	Power-Supply	Power-Consumption	CMOS Process	Architecture	FOM
[6]-Tsukamoto-1996	200MS/s	6b	3V	110mW	0.5um	Flash	5.8
[7]-Tsukamoto-1998	400MS/s	6b	3V	190mW	0.35um	Flash	4.99
[8]-Yoon-1999	500MS/s	6b	3V	330mW	0.6um	Flash	6.06
[2]-Mehr-1999	500MS/s	6b	3.3V	225mW	0.35um	Flash	5.26
[9]-Tamba-1999	500MS/s	6b	3.3V	400mW	0.4um	Flash	3.2
[12]-Yoo-2001	1GS/s	6b	2.5V	66.87mW	0.25um	Flash	24.5
[10]-Sushihara-2000	800MS/s	6b	3.3V	400mW	0.25um	Flash	3.28
[11]-Uyttenhove-2000	1GS/s	6b	3.3V	1155mW	0.35um	Flash	2.05
[13]-Nagaraj-2000	700MS/s	6b	3.3V	187mW	0.25um	Flash	10.4
[15]-Geelen-2001	1.1GS/s	6b	3.3V	300mW	0.35um	Flash	8.69
[14]-Choi-2001	1.3GS/s	6b	3.3V	545mW	0.35um	Flash	5.65
[1]-Dalton1998	200MS/s	6b	5V	380mW	0.6um	Flash	2.1
[24]-Yu-2001	900MS/s	6b	2.5V	450mW	0.25um	Pipelined	3.28
[27]-Kim-2001	200MS/s	8b	3V	210mW	0.35um	Pipelined	9.03
[20]-Nairn2000	100MS/s	10b	3V	310mW	0.35um	Pipeline	12.2
[31]-Yoo 2004	120MS/s	10b	2.5V	208mW	0.25um	Pipeline	15.15
[32]-Moon 2004	100MS/s	10b	1.8V	67mW	0.18um	Pipeline	25.5
[38]-Sumanen 2001	200MS/s	10b	3V	280mW	0.5um	Parallel-Pipeline	36
[35]-Yoon-2000	125MS/s	8b	3.3V	110mW	0.35um	Folding	10.77
[39]-Taft2001	100MS/s	8b	2.2V	75mW	0.4um	Subranging	13.1
[40]-Wang2000	150MS/s	8b	3.3V	395mW	0.6um	Subranging	6.07

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Obviously, for low resolution (≤ 6 bits), the flash architecture is typically the best choice. Even gigahertz rates can be achieved using the state-of-the-art CMOS technologies. It is clearly that the fastest architecture can provide 6–7-bit resolution range with a sampling rate of several hundred MHz or above GHz.

Pipelined architecture can be used in a very wide resolution range, typically from 8 to 10 bits and up to 15 bits with dedicated calibration schemes [26],[32],[77]. For high-speed ADC with hundreds MHz conversion rate, the resolution is in the range of 6 ~ 10 bits. However, the die area, power consumption increases greatly with the increase of sampling frequency and resolution. Although the sampling rate can be improved by interleaving technique, the linearity [38] is degraded due to the mismatch among differential channels. Moreover, the area and hardware increase N times for N channels interleaving, which is regarded as a penalty.

Subranging and folding ADCs can be realized without linear precision subtraction and the circuit area is typically quite small. However, the speed of the folding ADC is limited by the folding circuit despite of the fact that it can achieve higher resolution than subranging ADC through calibration [78]. For sampling rate of 100 MS/s and above, the resolution is limited to 8 bits. However, for subranging ADC, 8 bits resolution can be observed for sampling frequency higher than 100 MS/s using only typical CMOS technology to achieve lower power consumption and lower power supply, hence higher FOM. Therefore, in view of sampling rate, technology and power consumption, the

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subranging ADC is identified as one of the good choices for compromising the performance parameters in high-speed ADC design using standard sub-micron CMOS technologies. There is a strong potential to enhance the subranging ADC design approach despite of the medium value of FOM in the comparison table. Therefore, it leads to the investigation of improved subranging ADC design as one of the main objectives in this research work.

CHAPTER 3

PROPOSED PIPELINED SUBRANGING ADC ARCHITECTURE

In this chapter, the limitations of conventional subranging ADCs are reviewed. In order to overcome the drawbacks, a new subranging analog-to-digital converter (ADC) dedicated for high-speed low-power application is presented. In system design, an internal pipelined scheme incorporating with the double sampling and interleaving techniques allows the ADC sample input signal on consecutive clock without adding a sample-and-hold (S/H) circuit, thus maximizing the throughput with elimination of idle time. Finally, the overall block diagram of proposed ADC is given.

3.1 Review of Subranging ADC Architectures

As discussed in Chapter 2, the subranging ADC architecture allows for higher resolutions than the flash architecture due to the reduced number of comparators. However, the speed of conventional subranging ADC is decreased because of the two steps operation. It is imperative to compare the sequence of the operation of flash ADC and subranging ADC.

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Fig. 3.1 Comparison of Flash and Subranging ADCs with S/H

The conventional flash ADC, subranging ADC and their time base events are shown in Fig. 3.1(a), Fig. 3.1(b) and Fig. 3.1(d) respectively. For flash ADC, it samples the input signal for half of the clock cycle and performs the conversion in the other half clock cycle. While in subranging ADC, the S/H samples the input which is used for both coarse conversion and fine conversion. The S/H can sample another input signal only after the coarse conversion (CC) and fine conversion (FC) have been carried out. Although the coarse conversion can be as fast as a flash ADC, the fine conversion needs extra time, which limits the throughput of whole ADC. This shortcoming can be relaxed through using conventional pipelined subranging architecture as shown in Fig. 3.1(c). Another S/H is added between the Coarse ADC and Fine ADC, which performs

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the sample-and-hold function for the input signal in the fine conversion. Consequently, the front-end S/H can sample the input signal in every clock cycle without waiting for the fine conversion as illustrated in Fig. 3.1(d). Since the S/H circuit requires high-gain high-bandwidth amplifier, this scheme still limits the subranging ADC to operate in high-speed precision application.

Fig. 3.2 Subranging ADCs without S/H

One way to alleviate the use of S/H circuit in the subranging ADCs is to utilize the bottom-plate sampling technique [39], in which the time base of events function is performed by the front-end amplifier. The architectures together with the timing in previous works are shown in Fig. 3.2. Fig. 3.2(a) shows the conventional subranging ADC without S/H circuit. Despite of the fact of the speed can be improved by elimination of the S/H circuit, its conversion cycle still includes three parts: sample, coarse conversion and fine conversion as depicted in Fig 3.2(d), which is the same as the conventional subranging ADC with S/H in Fig. 3.1(a). Obviously, the extra period for fine conversion is still needed, thus an idle time exists in the coarse ADC and fine ADC. Recently, a unified subranging architecture has been reported [39] as shown in Fig. 3.2(b), using the same comparator block to evaluate both MSB and LSB, resulting in good matching characteristic. However, its timing is the same as the conventional one, thus the speed cannot be further improved. With interleaving technique, a sampling rate as high as 100 MS/s with 8-bit resolution has been achieved [39]. The subranging ADC incorporating with the internal pipelining techniques [42] is reported to increase the throughput. Shown in Fig. 3.2(c), the fine ADC is divided into three stages and the pipelining scheme is applied among stages as illustrated in Fig. 3.2(d). It is very effective to decrease the fine clock cycle since the signal passed through only one amplifier stage in half of the clock period. Consequently, the conversion time is shortened by decreasing the fine clock. However, this scheme cannot eliminate the idle time in the coarse and fine ADC and the extra fine clock is needed when compared with the flash ADC. In addition to above limitation, the throughput of the subranging ADC is also limited by the speed of the fundamental analog building block such as amplifier stages. Therefore, the objective of this research is to investigate and design a

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subranging ADC that alleviates the potential shortcomings of the previous works, but with properly managed tradeoffs among speed, power consumption and silicon area.

3.2 Proposed ADC Architecture

From the comparison of previous subranging ADCs without S/H, it is shown that an idle time exists in fine and coarse ADC. In order to remove the idle time, a new subranging ADC architecture is proposed, with a simplified diagram as depicted in Fig. 3.3. There are one coarse ADC and two interleaved fine ADCs (Fine ADC1 and Fine ADC2) to process the signal. The coarse ADC and the Fine ADCs are all divided into four stages for pipelining operation.

Fig. 3.3 Simplified Proposed ADC Architecture

The detail block diagram of the proposed ADC, which is based on the conventional subranging ADC, is depicted in Fig. 3.4. The ADC includes one modified 5-bit coarse ADC, and two interleaved 5-bit fine ADCs (Fine ADC1 and Fine ADC2). Contrasting to the example in Fig. 2.6, the 5-bits coarse ADC is divided into 2 portions: a 2-bit coarse pre-comparison block and a 3-bit coarse post-comparison block. The 2-

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bit coarse pre-comparison block is a simple flash ADC with 3 comparators, which quickly compares the input with the reference voltages. It generates the first 2 MSBs and roughly determines the coarse reference by controlling the coarse multiplexer (CMUX) to select correct coarse segments. Then, the coarse post-comparison block compares the input with the selected reference voltage and generates another 3-bit MSBs. Three additional comparators on each end are used to generate signals for error correction logic to perform increment or decrement the 2 MSBs in the event of an error in the coarse pre-comparison. These 5-bit MSBs control the fine multiplexer (FMUX) so as to select the proper resistor segment from the reference ladder for fine conversion. Finally, two interleaved fine ADCs (Fine ADC1 and Fine ADC2) compare the input voltage with the fine reference voltages to generate 5-bit LSBs. With a demultiplexer, the total 10-bit output is achieved, which represent the input voltage relative to the reference voltages. In the first stage of each interleaved fine ADC, one redundant amplifier is connected to the taps of the neighboring reference segment. They can be used to correct the error in the 5 MSBs of coarse conversion as well as to relax the comparator accuracy requirements in the coarse ADC. As can be seen in Fig. 3.4, the coarse post-comparison has four stages (stage 1, 2, 3, 4) and the fine ADC also has four stages (stage 5, 6, 7, 8). Each coarse ADC or fine ADC is based on the three-stage amplification plus the comparison in the final stage.

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Fig. 3.4 Proposed ADC Architecture

3.3 System Timing

The timing diagram in Fig. 3.5 illustrates the processing steps of four ADC input samples in detail. One coarse ADC, incorporating with two interleaved fine ADCs, deals with the input signals. The fine clock period is the double of the coarse clock period. When the fine ADC1 is in the sample phase, the fine ADC2 is in the amplify phase, and vice versa. In order to increase the speed, an internal pipelined scheme [42] is adopted among stages in the coarse and fine ADCs. Each stage samples or amplifies a signal and provides the output for the following stage. The input signal is pipelining processed stage by stage, a new signal can be sampled into ADC as soon as one signal passes through the stage 1. At any time, all the stages process different signal concurrently. Thus, a throughput of one output per clock cycle is achieved through the use of pipelining and interleaving techniques.

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Fig. 3.5 The Pipelined Timing Diagram of Proposed Subranging ADC

Let us consider the 1st signal as an example to explain the signal processing function. During the clock interval 1, the 1st input signal is sampled by the stage 1 of coarse ADC and stage 5 of fine ADC1 simultaneously. At the end of this interval, the coarse pre-comparison block quickly compares the input voltage with the reference voltages, which is used to choose the coarse reference segment for coarse post-comparison as well as to generate 2MSBs. During the clock interval 2, the voltage difference between the sampled 1st signal and the coarse reference voltages selected by the coarse pre-comparison is amplified by the stage 1, and its output is sampled by the stage 2. Then, the voltage difference is further amplified by the stage 2 and the stage 3 in the interval 3 and 4 respectively, and compared by the stage 4 during the clock interval 5 as well as generates 3MSBs. Thus, the total 5MSBs select the fine reference segment for fine comparison. In the following clock, the 1st input signal sampled by the

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fine ADC1 is compared with fine reference voltages. Similar with the coarse ADC, the 1st input is pipeline processed by the fine ADC according to fine clock shown in Fig. 3.5. Finally, the 5-bit LSBs are achieved so that the 10-bit digital output of 1st input signal is complete. The processing of the second input signal begins from the third interval, one clock cycle after the beginning of the processing of the 1st input signal. The interleaved fine ADC2 deals with the fine conversion for the second signal.

It is important to note that there is no idle time for both coarse ADC and fine ADC. The ADC deals with one input signal every clock cycle. Its speed only depends on the speed of single stage. The clock cycle of the coarse and fine ADC is shortened since the internal pipelining technique is adopted, thus higher speed can be achieved. Therefore, the proposed arrangement can maximize the throughput and fully utilize the circuit when compared to previous subranging ADCs.

3.4 Building Block in Proposed ADC

Fig. 3.6 Block Diagram of ADC

The overall block diagram of proposed ADC is shown in Fig. 3.6, which consists of core ADC circuit and input/output interface circuit. The core ADC includes the comparison block, clock generator, resistor ladder and digital logic circuit. The key building block of ADC is the comparator bank which consists of one coarse pre-comparison, one coarse post-comparison bank and two fine comparison banks. The speed and resolution of these comparator banks will govern the performance of ADC directly. Every component in the comparator bank should be designed carefully. A new sliding feedback capacitor technique will be proposed as the multistage preamplifier for the comparator design, which aims at further increasing the speed of coarse ADC. A high-speed ROM together with the logic circuit is then followed at the output of comparator. A clock generator is needed to provide the necessary clock signals for distributing to the whole ADC. A reference generator is designed to provide a number

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of reference voltages for comparators. Its design and layout approach would be considered carefully in order to get reference voltage with good accuracy. The accuracy for ADC depends directly on the reference voltage of resistor ladder and the quality of input signal applied to ADC. In order to maintain the accuracy of reference and input voltage in testing environment, the input interface circuit should provide high-drive and low-distortion characteristics for high-speed ADC. In other words, the linearity of the input interface should be better than the linearity of the whole ADC so as to alleviate the accuracy lost from them. Finally, the output interface should support proper digital interface logic level and provide sufficient drive ability in delivering the high-speed digital information to the external instrument.

3.5 Summary

The limitation of subranging ADC architecture in previous works is discussed and a new CMOS subranging ADC architecture has been presented in this chapter. In the proposed ADC, one coarse ADC deals the input signal with two interleaved fine ADC. Internal pipelined scheme is applied to both coarse and fine ADCs. The above arrangement allows the whole ADC process the input signal every clock cycle without any idle time, which alleviates the problem in previous research works. Thus, the throughput of ADC is maximized and the building block is fully used. In addition, the input interface is carefully designed in order to maintain high quality input signal whilst the output interface ensures the ADC to deliver proper digital output to the external environment.

CHAPTER 4

STUDY OF MULTISTAGE PREAMPLIFIERS FOR COMPARATOR DESIGN

In this chapter, the multistage preamplifiers for comparator design are studied. A new multistage preamplifier based on the use of a new sliding feedback capacitor technique is presented, which increase the speed of comparator without compromising the accuracy. It is suitable for high-speed comparator design. Second-order analysis has been conducted to understand the dominant nonlinear sources.

4.1 Introduction

In analog-to-digital converters, the comparator plays a crucial role on the overall performance. When dealing with high-speed applications, the comparator design tends to address simplicity in an architectural solution, which often comprises a preamplifier followed by a latch [44],[50] as shown in Fig. 4.1. The problems encountered by the comparator are therefore translated to the preamplifier specification and implementation, aiming at achieving good resolution, high sampling rate, low power consumption and small silicon area.

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Fig. 4.1 Input Offset Storage based Multistage Preamplifier.

Although a single preamplifier stage [46] may meet certain constraints such as speed, power and area, it is also difficult to optimize accuracy among other performance parameters because of finite gain and potential high input offset. As a consequence, this leads to the reported multistage preamplifier topologies [50],[43] incorporating the offset reduction technique. However, these well-known multistage preamplifier topologies have their distinct advantages for use in the comparators targeted for different application-specific ADCs. Despite the gain parameter and accuracy parameter have been improved as a common ultimate goal, there is also a penalty on the operation speed and exists other limitation in view of different architectures. Therefore, the objectives of this chapter are to investigate and propose a new multistage preamplifier that alleviates the potential shortcomings from the previous works.

4.2 Multistage Preamplifiers with Offset Reduction

4.2.1 Multistage Preamplifier with Input Offset Storage

Fig. 4.2 illustrates a multistage preamplifier with input offset storage approach [50]. The structure is simple and it supports rail-to-rail common mode input. In the reset mode, the respective switch (S_1, S_2, S_3) around each amplifier (A_1, A_2, A_3) is closed, and the offset is stored on the respective capacitor (C_1, C_2, C_3) in series to the corresponding input. In the amplification mode, any difference between the sampled input V_{in} and the reference voltage V_r is amplified by the gain, $A_{v1}A_{v2}A_{v3}$, of the preamplifier. The effective input-referred offset can be derived as

$$V_{OS} = \frac{V_{OS3}}{A_{v1}A_{v2}(1 + A_{v3})} + \frac{V_{OSL}}{A_{v1}A_{v2}A_{v3}} \quad (4.1)$$

where V_{OSL} is the input offset of latch, $V_{OS1}, V_{OS2}, V_{OS3}$ and A_{v1}, A_{v2}, A_{v3} are the respective input offset and voltage gain for the individual gain stage in the preamplifier.

(a) Topology

(b) Timing

Fig. 4.2 Input Offset Storage based Multistage Preamplifier.

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As can be seen from (4.1), the input-referred offset is reduced substantially via the product of three gain factors. However, the amplification phase is performed when all the feedback switches are off. It needs a long clock period because a signal must be passed through three stages in half a clock period. Hence, the operation speed will be greatly limited by the effective time constant of the complete amplifier. More importantly, when the active load, like CMOS inverter as an example, is utilized to implement the gain stage, the bandwidth will be reduced significantly.

Fig. 4.3 Pipeline Operation of Alternative Cascade Structure

These drawbacks can be overcome by the variant structure [42] as depicted in Fig. 4.3. The switch around amplifier is closed and opened alternatively between one amplifier and the next amplifier in pipelined operation. When stage 1 and stage 3 are in reset phase, stage 2 is in the amplification phase. When stage 1 and stage 3 are in amplification phase, stage 2 is in reset phase. In this pipeline operation, the difference between the sampled input and the reference voltage are amplified in the amplifier A_1

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and stored in the capacitor C_2' with the reset-mode amplifier A_2 , while the previous processing signal is transferred to the latch via the amplifier A_3 being arranged in switched-capacitor configuration.

Despite the latency, this pipeline scheme is very effective for increasing the throughput because the signal must be passed through only one amplifier stage in half of the clock period. Since each gain stage is implemented by switched-capacitor technique [39], the gain factor, now defined by the capacitor ratio, is stabilized. However, the improvement of the amplifier time constant through the capacitor ratio is counteracted by the increase of capacitive loads via the illustration of all the capacitors associated with the stage 1 amplifier in Fig. 4.4(a).

(a) Stage 1st Reset Phase and Amplification Phase

(b) Equivalent Circuit in Amplification Mode

Fig. 4.4 Operation of Stage 1 Amplifier and Its Equivalent Circuit in Amplification Phase

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Refer to Fig. 4.4(a), the gain of each stage can be defined as the ratio of input capacitance to feedback capacitance, thus, the closed-loop gain of stage 1 is

$A_{1c} = \frac{C_{1f}'}{C_{1f}}$. From node X and Y in Fig. 4.4(b), the time constant can be derived as [79]:

$$\tau_{amp} = \frac{C_{1f}'}{G_m} + \frac{C_{Leq}}{G_m} \quad (4.2)$$

and the effective capacitive load at the output of A_1 , node Y, is

$$C_{Leq} = C_2'(1 + C_{1f}'/C_{1f}) \quad (4.3)$$

From (4.2), the amplifier time constant comprises two time constant terms, the first term is proportional to input capacitance whilst the second term is a linear function of effective capacitive load. It is important to note that the time constant can be reduced via increasing device conductance parameter but constrained by power and sizing budget. The capacitance depends on design parameter, but it is also linkage with the architecture. It can be seen that high input capacitance and high effective capacitive load in (4.3) would degrade the operation speed significantly.

4.2.2 Multistage Preamplifier with Output Offset Storage

A multistage preamplifier with output offset storage approach is shown in Fig. 4.5. In the reset mode, the respective switch (S_1 , S_2 , S_3 and S_4) is closed and hence the

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amplifier offsets are stored on the respective output capacitor (C_1, C_2, C_3). In the amplification mode, any difference between the sampled input and the reference voltage is amplified by $A_{V1}A_{V2}A_{V3}$ times. The effective input-referred offset becomes

$$V_{OS} = \frac{V_{OSL}}{A_{V1}A_{V2}A_{V3}} \tag{4.4}$$

where V_{OSL} is the input offset of latch and A_{V1}, A_{V2}, A_{V3} are the gain defined for the three amplifier stage respectively.

Fig. 4.5 Output Offset Storage based Multistage Preamplifier

From equation (4.4), the input-referred offset is small. However, the input common-mode range is constrained by the direct input structure. Although this preamplifier would be faster than that of the input storage preamplifier due to absence of input capacitor, the summed amplifier time constant limits the operation speed.

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4.3 Proposed Multistage Preamplifier

4.3.1 Topology and Operation

A slide-capacitor multistage preamplifier is proposed in Fig. 4.6(a), which is based on the pipeline operation [42]. Instead of fixed feedback capacitor for each amplifier stage, the three amplifier stages share two feedback capacitors C_{1f} and C_{2f} which are regarded as the sliding capacitors. The switches S_{a1} , S_{a1}' , S_{b1} , S_{b1}' , S_{c1} and S_{c1}' are controlled to configure C_{1f} across the input and output of stage 1, 2 or 3 under respective slide-mode control signals $\phi a1$, $\phi b1$, $\phi c1$. For an example, during $\phi a1$, C_{1f} is configured as a feedback element across stage 1 through turning on switches S_{a1} and S_{a1}' . This is a similar process for another sliding capacitor C_{2f} under configuration switches S_{a2} , S_{a2}' , S_{b2} , S_{b2}' , S_{c2} , S_{c2}' by respective control signals $\phi a2$, $\phi b2$ and $\phi c2$.

The timing of the proposed multistage preamplifier is shown in Fig. 4.6(b). The clock signals $\phi a1$, $\phi b1$, $\phi c1$ with C_{1f} and the clock signals, $\phi a2$, $\phi b2$, $\phi c2$ with C_{2f} perform the multistage amplifying. The input signal sampled by C_1 are amplified by proposed preamplifier with interleaved C_{1f} and C_{2f} . The operation of C_{1f} and C_{2f} is the same. Denote the open-loop gain of three amplifiers as A_1 , A_2 and A_3 , and the closed-loop gain of each stage as A_{1c} , A_{2c} and A_{3c} .

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Consider C_{1f} as an illustrative example in Fig. 4.6(c), in phase ϕ_{a1} & ϕ_1 , C_{1f} is in the feedback loop of the stage 1. The input V_{in} is sampled by the input capacitor C_1 , and the feedback capacitor C_{1f} is discharged. In phase ϕ_{a1} & ϕ_2 , the voltage difference between the input voltage V_{in} and reference voltage V_{ref} is amplified by the stage 1 as well as the charge is stored in the feedback capacitor C_{1f} . Its output is sampled by the stage 2. In phase ϕ_{b1} , C_{1f} is connected to the stage 2, and the output of the stage 1 is amplified by the stage 2. Contrasting to the conventional operation in which feedback capacitor is discharged in this period, the charge stored in C_{1f} is not discharged but transferred to the stage 2. In phase ϕ_{c1} , C_{1f} is worked as the feedback capacitor of the stage 3 and the charge stored in C_{1f} at stage 2 is transferred to the stage 3. The voltage difference is further amplified in the stage 3 and its output is applied to the latch for comparison. Then, the charge stored in C_{1f} , related to the first signal, is discharged in next ϕ_{a1} & ϕ_1 , thus C_{1f} can be ready to process a new signal. With the interleaved-capacitors C_{1f} and C_{2f} , the proposed preamplifier can handle one input signal for every clock cycle.

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(a) Topology

(b) Timing

(c) Operation

Fig. 4.6 Proposed Multistage Preamplifier with Sliding Feedback Capacitor

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Table 4.1 shows the voltage change of node 1, 2, 3, 4, 5 and 6 in Fig. 4.6 (a) (V_1 , V_2 , V_3 , V_4 , V_5 and V_6) at time instant A, B, C and D in Fig. 4.6(b), which illustrate the processing of input signal V_{in1} . At the instant A, stage 1 is in the reset phase. The voltage at node 1 and 2 (V_1 , V_2) are equal to the virtual ground of amplifier, V_b . At time instant B, stage 1 is the amplification phase, the voltage difference between the input voltage V_{in1} and reference voltage V_{ref} is amplified by A_{1c} . Thus, the voltages at node 1 and 2 are $V_b + \frac{A_{1c}(V_{ref} - V_{in1})}{A_1}$ and $V_b + A_{1c}(V_{ref} - V_{in1})$. At the same time, the stage 2 is in the reset phase and the voltage at node 3 and 4 are V_b . At time instant C, the voltage $A_{1c}(V_{ref} - V_{in1})$ is further amplified by A_{2c} . Thus, the voltage at node 3 and 4 are $V_b + \frac{A_{1c}A_{2c}(V_{ref} - V_{in1})}{A_2}$ and $V_b + A_{1c}A_{2c}(V_{ref} - V_{in1})$. Similarly, the voltage at node 5 and 6 are $V_b + \frac{A_{1c}A_{2c}A_{3c}(V_{ref} - V_{in1})}{A_3}$ and $V_b + A_{1c}A_{2c}A_{3c}(V_{ref} - V_{in1})$ at time instant D respectively. As a result, the difference of input voltage V_{in1} and reference voltage V_{ref} is amplified by three stages.

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Table 4.1 Signal Processing in Proposed Multistage Preamplifier

	A	B	C	D
V1	V_b	$V_b + \frac{A_{1c}}{A_1}(V_{ref} - V_{in1})$	V_b	$V_b + \frac{A_{1c}}{A_1}(V_{ref} - V_{in2})$
V2	V_b	$V_b + A_{1c}(V_{ref} - V_{in1})$	V_b	$V_b + A_{1c}(V_{ref} - V_{in2})$
V3		V_b	$V_b + \frac{A_{1c}A_{2c}}{A_2}(V_{ref} - V_{in1})$	V_b
V4		V_b	$V_b + A_{1c}A_{2c}(V_{ref} - V_{in1})$	V_b
V5	V_b		V_b	$V_b + \frac{A_{1c}A_{2c}A_{3c}}{A_3}(V_{ref} - V_{in1})$
V6	V_b		V_b	$V_b + A_{1c}A_{2c}A_{3c}(V_{ref} - V_{in1})$

4.3.2 Timing Constant Analysis

The unique operation of the proposed scheme is that, the charges stored in the feedback capacitor C_{1f} and C_{2f} are not discharged after amplification phase. It is reused for the processing of same signal in the following stage and it is only discharged before the processing of a new input signal. The reuse of the charge stored in the feedback capacitor gives a potential possibility to increase the speed. When C_{1f} is worked as the feedback capacitor in the stage 1, and the voltage difference between the input voltage V_{in} and reference voltage V_{ref} is amplified by A_{1c} . Thus, the voltages at

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node 1 and 2 are $V_b + \frac{A_{1c}(V_{ref} - V_{in})}{A_1}$ and $V_b + A_{1c}(V_{ref} - V_{in})$, where V_b is the virtual ground of amplifier and A_1 is the open-loop gain. Since $A_1 \gg A_{1c}$, the voltage at node 1 can be approximated as V_b . Hence the charge stored in C_{1f} is $A_{1c}C_{1f}(V_{ref} - V_{in})$. In the following period, C_{1f} is connected to the stage 2 as feedback capacitor. According to the principle of conservation of electric charge, the nodal equation at node 3 can be achieved:

$$[0 - A_{1c}(V_{ref} - V_{in})]C_2 - A_{1c}C_{1f}(V_{ref} - V_{in}) = -A_{1c}A_{2c}C_{1f}(V_{ref} - V_{in}) \quad (4.5)$$

Then, the closed-loop gain of the stage 2 can be expressed as

$$A_{2c} = \frac{A_{1c}A_{2c}(V_{ref} - V_{in})}{A_{1c}(V_{ref} - V_{in})} = \frac{C_2 + C_{1f}}{C_{1f}} = 1 + \frac{C_2}{C_{1f}} \quad (4.6)$$

Hence, the input capacitor is:

$$C_2 = (A_{2c} - 1)C_{1f} = A_{2c}C_{1f}\left(1 - \frac{1}{A_{2c}}\right) \quad (4.7)$$

This is contrasting to the input capacitance in conventional operation, $C_2 = A_{2c}C_{1f}$, smaller input capacitance is needed in the proposed operation without losing the closed-looped gain. From (4.7), the input capacitor in proposed preamplifier is $\frac{1}{A_{2c}}$ times smaller than the normal input capacitor under the same closed-loop gain and feedback capacitor. According to (4.2) and (4.3), time constant of proposed preamplifier is reduced due to the smaller sampling capacitance. Similarly, the sampling capacitance of stage 3 is $C_3 = A_{3c}C_{1f}\left(1 - \frac{1}{A_{3c}}\right)$. Although the input capacitance

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of the stage 1 is $C_1 = A_{1c} C_{1f}$, which is the same as the normal operation, the capacitive load is reduced due to the smaller input capacitance of the stage 2 according to (4.3). As a result, faster speed can be attained in the proposed preamplifier whilst maintaining gain.

The time constant reduction is summarized in Table 4.2, where the reduction factor denotes time constant reduction when compared with the conventional scheme with fixed capacitors to define the gain in each gain stage. For typical gain stages having gain between 2-5, the time constant can be reduced from 17.2% to 72.5% in the new scheme. Moreover, 1/3 area of feedback capacitor is saved in the proposed preamplifier by sharing two feedback capacitors in three amplifiers, as well as it saves up to 1/3 area of input sampling capacitor according to the gain. In final remark of actual layout consideration, the use of complex clock and time circuits causes about 1.6% increase of the total layout area of the core ADC as a penalty.

Table 4.2 Reduction of Time Constant in Proposed Multistage Preamplifier

	Stage 1	Stage 2	Stage 3
Stage Gain	Reduction Factor1	Reduction Factor2	Reduction Factor3
$A_{1c}, A_{2c}, A_{3c} = 2$	37.5%	72.5%	72.5%
$A_{1c}, A_{2c}, A_{3c} = 3$	23.7%	46.7%	46.7%
$A_{1c}, A_{2c}, A_{3c} = 4$	20.9%	37.5%	37.5%
$A_{1c}, A_{2c}, A_{3c} = 5$	17.2%	31.5%	31.5%

4.3.3 Distortion Analysis

Since the preamplifier is the most critical analog building block in this subranging ADC design, its linearity has a direct impact on the performance of ADC in terms of SNDR, DNL and INL. Shown in Fig. 4.7, the proposed preamplifier is implemented using a pseudo-differential structure for common-mode noise rejection and suppression of even harmonics. Despite of the differential architecture, there is unavoidable nonlinearity due to second-order effects. To examine the effects, the gain stages are identified to contribute the nonlinear error because of the nonlinear g_m and g_{ds} in amplifier. Switch charge injection is another critical error source, which can degrade the linearity of sample-data analog circuits in a form of signal-dependent charge injection. Among the switches employed in the preamplifier, the charge injection of the reset switches (S_{1+} , S_{2+} , S_{3+}) is signal independent, thus contributing only dc effect, and the signal-dependent charge injection arising from the input switch (S_{i1+} and S_{i2+}) can also be minimized via proper timing delay [67]. However, the signal-dependent charge injection of switches (such as S_{a1+} , S_{a1+}' , S_{a2+} , S_{a2+}' and so on) associated with the feedback capacitors C_{1f} and C_{2f} cannot be ignored, its influence on the amplifier output is analyzed in Appendix D.

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Fig. 4.7 Differential Preamplifier with Mismatching

In deep sub-micron CMOS technology, the mismatch effect appears as one of the dominant errors in high-speed differential switched-capacitor circuits because of relative higher sensitivity in switch pairs using small channel length and in capacitor ratios using small capacitors. It is important to noted that mismatch between identical designed components in a pair can be observed as the relative sense. Regardless of the component value, one component parameter is chosen as the reference. If the reference is normalized as unity, the other identical designed component parameter can be modeled with the mismatch value of $(1 + \alpha)$, where α represents the mismatching factor. Based on the assumption, this leads to the mismatched differential preamplifier in Fig. 4.7 for nonlinear analysis. The switches associated with the feedback capacitors in the upper branch are regarded as references. The complementary switches in the mirror side can be treated as the mismatched components. Hence, the reference channel areas of the switches associated with feedback capacitors in the upper branch (such as S_{a1+} , S_{a1-} , S_{a2+} , S_{a2-} and so on) are assumed WL whereas the mismatch area for the

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corresponding switch in the lower branch (such as S_{a1-} , S_{a1-}' , S_{a2-} , S_{a2-}' and so on) are given as $WL(1 + \alpha_{iWL})$, where α_{iWL} represents the mismatching factor for stage i . For simplicity, α_{WL} is chosen from the maximum value of the mismatching factors α_{1WL} , α_{2WL} and α_{3WL} in the three stages because these coefficients are close to each other. For ease of analysis, it can be assumed as $WL(1 + \alpha_{WL})$ and treated as the worst case mismatch area for each stage. In a similar treatment, the input and feedback capacitors in the upper differential branch can be modeled as C_1 , C_2 , C_3 , C_{1f} , C_{2f} respectively for the references, their corresponding mismatch components are defined as $C_1(1 + \alpha_C)$, $C_2(1 + \alpha_C)$, $C_3(1 + \alpha_C)$, $C_{1f}(1 + \alpha_{C_f})$ and $C_{2f}(1 + \alpha_{C_f})$ in the lower differential branch, where α_C and α_{C_f} are defined as the worst case mismatching factors for input and feedback capacitors. Furthermore, the variation of C_{ox} and γ is ignored because their contribution to the non-ideal effects is not as strong as the two former mismatch effects as discussed above. Besides, the mismatch in open-loop amplifier gain can also be neglected because the feedback loop degenerate the mismatch effect.

The second-order analysis is performed to obtain the closed-form expressions for the second and third harmonics. If the sampling frequency is made much higher than the fundamental signal component, the second and third harmonic components in a non-linear sample-data circuit, these components can be approximated by their continuous-time counterparts in reasonable accuracy. As a result, the second and third harmonic distortion at the output of the differential preamplifier are derived as follow (see Appendix D):

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$$HD_2 \cong \frac{1}{2} \frac{a_{1f}^2 b_{1f}^2 c_{2f} - a_{1f}'^2 b_{1f}'^2 c_{2f}'}{a_{1f} b_{1f} c_{1f} + a_{1f}' b_{1f}' c_{1f}'} V_p \cong \frac{1}{4} \frac{a_{1f}^2 b_{1f}^2 c_{2f} - a_{1f}'^2 b_{1f}'^2 c_{2f}'}{a_{1f} b_{1f} c_{1f}} V_p \quad (4.8)$$

$$HD_3 = \frac{1}{4} \frac{a_{1f}^3 b_{1f}^3 c_{3f} + a_{1f}'^3 b_{1f}'^3 c_{3f}'}{a_{1f} b_{1f} c_{1f} + a_{1f}' b_{1f}' c_{1f}'} V_p^2 \cong \frac{1}{4} a_{1f}^2 b_{1f}^2 \frac{c_{3f}}{c_{1f}} V_p^2 \quad (4.9)$$

$$\text{with } a_{1f} \cong \frac{C_1}{C_{1f}}, a_{1f}' \cong \frac{C_1}{C_{1f}} (1 + \alpha_c - \alpha_{c_f}), b_{1f} \cong \frac{C_2}{C_{1f}} + 1, b_{1f}' \cong \frac{C_2}{C_{1f}} (1 + \alpha_c - \alpha_{c_f}) + 1,$$

$$c_{1f} \cong \frac{C_3}{C_{1f}} + 1, c_{1f}' \cong \frac{C_3}{C_{1f}} (1 + \alpha_c - \alpha_{c_f}) + 1,$$

$$c_{2f} \cong \frac{\frac{C_3}{C_{1f}} (2 + \frac{C_3}{C_{1f}}) K_{A3a2}}{(1 + \frac{C_3}{C_{1f}} + K_{A3a1})^2} - \frac{\gamma C_{ox} WL}{16(2\Phi_f + V_b)^{3/2} C_{1f}},$$

$$c_{2f}' \cong \frac{\frac{C_3}{C_{1f}} (1 + \alpha_c - \alpha_{c_f}) \left[2 + \frac{C_3}{C_{1f}} (1 + \alpha_c - \alpha_{c_f}) \right] K_{A3a2}}{\left[1 + \frac{C_3}{C_{1f}} (1 + \alpha_c - \alpha_{c_f}) + K_{A3a1} \right]^2} - \frac{\gamma C_{ox} WL}{16(2\Phi_f + V_b)^{3/2} C_{1f}} (1 + \alpha_{WL})$$

$$c_{3f} \cong \frac{\frac{C_3}{C_{1f}} (2 + \frac{C_3}{C_{1f}}) K_{A3a3}}{\left(1 + \frac{C_3}{C_{1f}} + K_{A3a1} \right)^2} - \frac{\frac{C_3}{C_{1f}} (2 + \frac{C_3}{C_{1f}}) K_{A3a2}^2}{\left(1 + \frac{C_3}{C_{1f}} + K_{A3a1} \right)^3} - \frac{(1 + \frac{C_3}{C_{1f}}) K_{A3a2}}{1 + \frac{C_3}{C_{1f}} + K_{A3a1}} \frac{\gamma C_{ox} WL}{16 C_{1f} (2\Phi_f + V_b)^{3/2}} + \frac{\gamma C_{ox} WL}{32 C_{1f} (2\Phi_f + V_b)^{5/2}}$$

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$$c_{3f}' \cong \frac{\frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f}) \left[2 + \frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f}) \right] K_{A3a3}}{\left[1 + \frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f}) + K_{A3a1} \right]^2} - \frac{\frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f}) \left[2 + \frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f}) \right] K_{A3a2}^2}{\left[1 + \frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f}) + K_{A3a1} \right]^3} - \frac{\left[1 + \frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f}) \right] K_{A3a2}}{\left[1 + \frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f}) + K_{A3a1} \right]} \frac{\gamma C_{ox} WL(1 + \alpha_{WL})}{16 C_{1f} (2\Phi_f + V_b)^{3/2}} + \frac{\gamma C_{ox} WL(1 + \alpha_{WL})}{32 C_{1f} (2\Phi_f + V_b)^{5/2}}$$

where V_p is the amplitude of the input signal, a_{1f} , b_{1f} , c_{1f} are responsible for the linear closed-loop gain of stage 1, stage 2, stage 3 whilst c_{2f} and c_{3f} denote the second and third order nonlinear coefficient of stage 3 respectively, a_{1f}' , b_{1f}' , c_{1f}' , c_{2f}' , c_{3f}' are the corresponding mismatching coefficients in lower branch of differential preamplifier with reference to the coefficients in the upper branch a_{1f} , b_{1f} , c_{1f} , c_{2f} , c_{3f} . V_b is the virtual ground of amplifier, K_{A3a1} is the linear gain factor of amplifier for the stage 3, and K_{A3a2} , K_{A3a3} denote the second and third order nonlinear coefficient of amplifier for the stage 3.

From (4.8), the second harmonic distortion (HD2) is only caused by the mismatch of identically designed components in the differential circuit, especially the mismatch of linear closed-loop gain of the stage 1, 2, 3 and the second order nonlinear coefficient of the stage 3. It can be seen that HD2 is sensitive in terms of the mismatch in capacitor ratios and switch size. HD2 is increased with the increase of mismatching.

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The HD2 can be very small for case of good matching. From (4.9), the mismatch does not affect the third harmonic distortion (HD3) significantly since the first product term $a_{1f}^3 b_{1f}^3 c_{3f}$, having the same polarity, is close to the second product term $a_{1f}^2 b_{1f}^2 c_{3f}'$. Besides, the value of HD3 mainly depends on the linear closed-loop gain factors a_{1f} , b_{1f} , c_{1f} for the stage 1, 2, 3 respectively and the third order nonlinear coefficient, c_{3f} , of the stage 3. The nonlinearity of the preamplifier will be validated by the simulation result in Chapter 9.

CHAPTER 5

COMPARISON BLOCK

In this chapter, the comparison blocks for coarse ADC and fine ADC are presented. For coarse ADC, the coarse comparison block is separated into the pre-comparison and post-comparison block. For fine ADC, the fine comparison block incorporating with the double sampling technique allows the ADC sample input signal on consecutive clock without adding a sample-and-hold (S/H) circuit. The use of interleaved technique further enhances the speed of the fine ADC. In addition, a synchronized switch is introduced to minimize the sample-time mismatches in the interleaved architecture. Finally, the circuit design of building blocks such as comparator, amplifier and latch is also presented in this chapter.

5.1 Coarse Comparison Block

5.1.1 Pre-Comparison

As discussed in Chapter 3, the 5-bits coarse ADC is divided into 2 portions: a 2-bit pre-comparison and a 3-bit post-comparison. The 2-bits pre-comparison is implemented by a simple flash ADC with 3 high-speed comparators as illustrated in Fig. 5.1. The input voltage (V_{in}) is quickly compared with three reference voltages (V_{r1} ,

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V_{r2} and V_{r3}) and generate the first 2-bits. The purpose of this pre-comparison in coarse ADC is to make a very fast decision on the reference voltage segment for the 3-bit coarse post-comparison. It roughly determines the coarse reference by controlling the coarse multiplexer (CMUX) to select correct coarse segments. Since the error correction being applied in post-comparison relaxes the accuracy required in the coarse pre-comparison, no technique such as offset cancellation is used.

Fig. 5.1 Pre-Comparison for Coarse ADC

The comparator used in the pre-comparison directly impacts the speed of the overall converter. Fig. 5.2 shows the high-speed comparator [40] utilized in the pre-comparison with differential input signals. It consists of two differential input pairs (M_1 and M_2 , M_3 and M_4), cross-coupled inverters (M_5 and M_7 , M_6 and M_8), four reset switches (S_1 - S_4), two equalization switch (S_5 and S_6) and two biasing transistor (S_7 and S_8). When CK is low, S_7 and S_8 are off, resulting in zero biasing current. All the reset switches (S_1 - S_4) are on, so the four internal nodes (A , B , C , and

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D) are pulled up to V_{DD} with the aid of two equalization switches (S_5 and S_6). The comparator is in the reset mode at this period. When CK goes high, S_7 and S_8 turn on and two differential input pair compare the differential input voltage, V_{in+} and V_{in-} , with the corresponding reference voltage, V_{r+} and V_{r-} , respectively. At the same time, all the reset and equalization PMOS switches are off, the cross-coupled inverters (M_5 - M_8) regeneratively amplify the difference between the inputs to rail-to-rail levels. The digital outputs are buffered by inverters and then fed to the control circuit.

Fig. 5.2 A High Speed Comparator

This comparator offers three important advantages over other topologies. First, the static power dissipation is zero. When CK is low, no static current flows through the circuit. When CK is high, the cross-coupled inverters (M_5 and M_7 , M_6 and M_8) ensure that the current is zero because only one transistor in each inverter is on. Second, the comparator requires only a single-phase clock, greatly simplifying the

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routing of the clock across the chip. Third, the effect of the offsets due to the cross-coupled transistors is reduced by the dynamic gain of the input stage. This is because when CK goes high, nodes A , B , C , and D have been precharged to V_{DD} in the previous phase and $M_5 - M_8$ are off. The input difference is therefore amplified by $M_1 - M_4$ until V_A and V_B drop below V_{DD} by V_{THN} . At this moment, M_7 and M_8 turn on but M_5 and M_6 are still off. The amplification then continues until M_5 and M_6 turn on and M_5 and M_6 contribute a small regenerative gain, thus initiating the final regeneration. Therefore, the offset of M_7 and M_8 are reduced by the gain of amplification by $M_1 - M_4$ whilst the offset of M_5 and M_6 are reduced by the gain of amplification by $M_1 - M_4$, M_7 and M_8 .

5.1.2 Post-Comparison

Shown in Fig. 5.3, the proposed sliding capacitor multistage preamplifier is implemented in the post-comparison of coarse ADC. Its design is presented in Chapter 4 and its distortion is analyzed as well. The bottom-plate sampling, incorporating with the input offset storage, can reduce the input-referred offset greatly. The proposed sliding capacitor technique further improves its speed. The followed latch is used to amplify the input difference to digital level which is fed to the digital circuit. Since the coarse ADC requires high speed and relative low accuracy when compared with the fine ADC, interpolation is not used in the coarse post-comparison block. In addition, pseudo-differential structure is used for better linearity and noise rejection.

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Fig. 5.3 Post-Comparison Block of Coarse ADC

5.2 Fine Comparison Block

A section of fine comparison block is depicted in Fig. 5.4. The comparator in the fine ADCs consists of three-stage preamplifier followed by a regenerative latch, the input-referred offset of latches can be reduced by the gain of preamplifier effectively. Multiplex double sampling at the front end is used to double the sampling speed, which will be discussed in detail in next section. In order to reduce the number of the comparators, a capacitive interpolation is used in the fine ADC. Not only does the interpolation reduce the front-end loading on the input signal and the reference voltages, it also reduces power consumption and die area. In addition, the interpolation attenuates the front-end sources of differential nonlinearity (DNL) [42], the charge injection mismatch in the input sampling switches and the resistor mismatch in the reference ladder.

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Fig. 5.4 Fine Comparison Block

The circuit techniques such as bottom-plating sampling, auto-zero technique and pipelining scheme [46] are combined to achieve fast comparison. Through bottom-plating sampling, not only does it alleviate the restriction imposed by S/H, it also avoids the design for high-performance buffer and saves power. Auto-zero technique is used to cancel the offset of CMOS amplifier. Pipeline scheme is employed among the stages as discussed before. Another important aspect of these comparison blocks is that it does not require a precise gain in any stage. The differential implementation provides greater immunity to digital noise and better charge injection cancellation. Such a

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combined strategy leads to the solution for the design of high-speed high-resolution comparison block.

Fig. 5.5 Amplifier in Multistage Preamplifier

As can be seen in the coarse post-comparison block and fine comparison block, the gain stage in the multistage preamplifier is implemented by amplifier with capacitive feedback. For this amplifier, no high gain is required but high speed is needed in order to meet the speed requirement of the ADC. Due to a large number of amplifiers are needed, the amplifier should be as simple as possible at the same time. All the amplifiers in the gain stage for the coarse and fine ADCs are implemented using the topology of a common source amplifier [39]. As shown in Fig. 5.5, the single stage amplifier consists of one NMOS transistor with a current source as an active load. In order to properly process the input signal, the design of the amplifiers requires special attention to several issues. First, the input-referred offset of the circuit must be as small as possible although it can be alleviated by the auto-zero techniques. The offset arises from the mismatch between the pseudo-differential input transistors and mismatch between the current sources. The mismatch of the pseudo-differential pair typically can be minimized by proper layout. The mismatch of the current sources is reduced significantly by using a wider channel length. The second issue relates to the gain of the

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amplifier. There is no precise stage gain (or closed-loop gain) required in this ADC. Thus, high open-loop gain is not necessary for this amplifier. The gain is chosen to be around several ten as a trade-off between gain, linearity, and speed. Finally, the amplifiers do not require a wide input common-mode range due to the capacitive coupling. However, due to the charge injection that results in lower input common mode voltage, a reasonable input common mode voltage in the design should be needed for achieving good linearity.

(a) Schematic

(b) Timing

Fig. 5.6 Latched Comparator

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A regenerative latch similar to [43] is used in both the comparison blocks, which is located after the multistage preamplifier. As shown in Fig. 5.6(a), it is composed of a differential input pair (M_1 , M_2), CMOS flip-flop circuit and a SR latch. The CMOS flip-flop consists of a n-channel cross-coupled transistor pair (M_4 , M_5), a p-channel cross-coupled transistor pair (M_6 , M_7), n-channel transfer switch pair (M_8 , M_9) and three resetting switches (M_{10} , M_{11} , M_{12}). It is noted that ϕ_1 , ϕ_2 are the non-overlapping clocks that control the operation of the latched comparator.

As shown in Fig. 5.6(b), the dynamic operation of this circuit includes two time intervals: reset time interval (between t_1 and t_2) and regeneration time interval (between t_3 and t_4). During ϕ_2 , the resetting switch M_{12} is closed and the comparator is in the reset mode. Current flows through M_{12} and the previous two logic state voltages at node A and B are equalized. In the meantime, as the n channel flip-flop is reset, the p channel one is also reset by the two closed precharge transistors which charge nodes C and D to the positive power supply voltage. At this period, transistors M_8 and M_9 isolate the n-channel flip-flop from the p-channel flip-flop. After the input stage settles on its decision, a voltage proportional to the input voltage difference is established between nodes A and B in the end. This voltage will act as the initial imbalance for the following regeneration time interval.

When ϕ_2 goes low, switch M_{12} is opened and the regeneration is started. The regeneration includes two steps. The first step of regeneration is within the short time slot between ϕ_2 getting low and ϕ_1 getting high. M_8 and M_9 are opened at this

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period. The second regeneration step starts when ϕ_1 gets high and M_8 and M_9 are closed. The n-channel flip-flop and the p-channel flip-flop regenerates the voltage difference between nodes A and B, C and D, which is soon amplified to a voltage swing nearly equal to the power supply voltages. The following SR latch is used to drive the voltage at C and D to full complementary digital output levels at the end of the regenerative mode. This complementary digital output will remain in the previous stage in the reset mode. There is no slew-rate problem in the regenerative period. The first regeneration step is very important, not only in raising the regeneration speed but also in reducing the total input offset voltage. The differential errors, caused by the charge injection from M_8 and M_9 , the mismatches in the p-channel flip-flop, the two precharge transistors and the SR latch, are divided by the amplification gain in the first regeneration step. They are referred to the input as an equivalent offset voltage. However, their contribution to the total equivalent input offset voltage can be neglected if the gain is large enough.

5.3 Multiplex Double Sample Comparator

In this ADC, the bottom-plate sampling is used to avoid the design of S/H circuit. Fig. 5.7(a) shows the input stage of coarse ADC using the conventional bottom-plate sampling structure and its timing waveforms are illustrated in Fig. 5.7(c). In phase ϕ_1 , the input signal is sampled in the input capacitance C_1 , while the voltage difference between the input signal and reference voltage is amplified in phase ϕ_2 . The input capacitor of coarse ADC samples the input signal every clock cycle of ϕ_1 . From the

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timing diagram in Fig. 3.5, a sampled input signal needs to be held in the fine ADC until it is quantized by the coarse ADC, thus this sampling input capacitor in the fine ADC can only be used to sample another signal after the processing of the previous sampled signal. With interleaving, two sampling capacitor in fine ADC1 and fine ADC2 only can sample the input signal every other clock cycle according to the timing diagram in Fig. 3.5, which is only the half of the sampling speed of coarse ADC. Obviously, in order to sample one input signal every clock cycle, the sampling speed of fine ADC must be doubled. One way to solve this problem is to implement four interleaved ADCs for fine conversion. However, it is at the cost of double the fine comparison block as well as creates idle time in the interleaved fine ADCs, which increase power and silicon area. Another way to solve this problem is to incorporate multiplex double sampling technique with fine ADC. Since the bottom sampling is adopted, the first stage of fine ADC can be modified as shown in Fig. 5.7(b). There are two sampling capacitors in each interleaved fine ADC, which is different with the conventional bottom-plate sampling approach with one sampling capacitor. Thus, four sampling channels for the fine ADC are achieved whilst only a small increase in the circuit complexity. The four input capacitors, CF_1 , CF_2 , CF_3 and CF_4 , sample the input signal in turn with multiplex clock signals ϕ_{f1_1} , ϕ_{f1_2} , ϕ_{f2_1} and ϕ_{f2_2} , then hold it. The multiplex double sampling technique allows each interleaved ADC samples a new input before processing of previous sampled input. In order to hold the input signal without affecting by the sampling of another input, the switches (S_{15} , S_{16} , S_{17} and S_{18}) are added between the sampling capacitor and the input of amplifier. The respective switch is on when the corresponding input capacitor is in the sample phase, amplify phase and off phase when it in the hold phase. As a result, the combination of

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interleaving and double sampling technique in the fine comparison block allows the ADC to process the input signal on consecutive clock without an extra S/H circuit.

(a) Sampling in Post-Comparison in the Coarse ADC

(b) Sampling in Fine Comparison in the Fine ADCs

(c) Timing Diagram

(d) Synchronized Switch

Fig. 5.7 Multiplex Double Sampling

5.4 Sample-time Insensitive Interleaved ADC

In general, applying the interleaving technique in fine ADC is an effective way to increase throughput, however, it creates several error sources such as offset mismatch, gain mismatch and timing mismatch in time-interleaved ADC. Regarding the offset mismatch, it can be reduced by the gain of preamplifier in individual ADC through auto-zero technique [67]. Hence, the input-referred offset error is quite small and of little concern. Regarding the gain mismatch, it is not important in the subranging ADC because the accuracy is not depended on the accurate gain of amplifier [40]. Regarding the timing mismatch, the sample times for the two interleaved channels are hard to be synchronized exactly due to non-ideal digital clock circuitry.

Refer to Fig. 5.7, the sample instant is defined by the falling edge of the clock ϕ_1 , ϕ_1 and ϕ_2 , which control the reset switch S_1 , SF_1 and SF_2 respectively. Thus, different clocks cause the sample time error. Similar to the timing skew insensitive double-sampling S/H circuit [38], the error due to interleaved clock in the double bottom-plating sampling can also be minimized. By modifying the single switch, the ADC can be made insensitive to sample-time error by using a synchronized clock to control the sample-time of interleaved ADC. As shown in Fig. 5.7 (d), the single switch, driven by the clock signals S_1 , SF_1 and SF_2 , is now connected in series with switch S_m , which is controlled by a synchronized clock, ϕ_m , whose falling edge is a little bit early than ϕ_1 , ϕ_1 and ϕ_2 . Thus, the sample-time of interleaved ADC is

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decided by one clock, which minimizes the error due to the mismatch of sample time. Also, it makes the circuit insensitive to the signal-dependent charge injection of the input switch which is connected with the input voltage [67].

Fig. 5.8 Timing Mismatch

Fig. 5.8 shows the timing instants mismatch of an A/D converter. Assume the input signal is $x(t) = \cos(\omega_0 t + \theta)$. The ideal sampling speed is $1/T$ and sampling instants are at the multiples of T . Δt is the sampling time mismatch between two channels. The output can be expressed as [80]

$$y[n] = \cos\left\{\omega_0\left[nT + \frac{\Delta t}{2} - (-1)^n \frac{\Delta t}{2}\right] + \theta\right\} \quad (5.1)$$

From (5.1), the interleaved ADC samples the input at a rate of $1/T$, and there is a phase modulation $\omega_0(-1)^n \frac{\Delta t}{2}$. This phase modulation contributes an undesired tone in the frequency domain. The larger the Δt , the more the nonlinearity is. The effectiveness of the scheme will be validated by the simulation results in Chapter 9.

CHAPTER 6

OTHER CIRCUIT DESIGNS

Except the comparator block discussed in the previous chapter, ADC also includes other circuits to support the operation of whole ADC. In this chapter, the design of ADC building blocks such as reference ladder, clock generator, digital error correction and encode circuit are discussed.

6.1 Reference Ladder

In the ADCs, the accuracy of the reference level for comparator sets the limit to the achievable resolution of the A/D conversion process. Any error present in the reference resistor string will be directly translated into an A/D conversion error such as differential nonlinearity error (DNL) and integral nonlinearity error (INL) and so on. The simplest way for reference voltage generation for comparator is to use a resistor string as shown in Fig. 6.1. The reference voltage for each comparator can be generated from one of the 2^n identical resistor cells connected between two reference voltages at the end of the resistor string.

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Fig. 6.1 Reference Ladder

In order to get accurate reference voltage, the design of the resistor ladder requires special attention to several issues. First, the matching property of the resistor is one of the limiting factors. In some of 8~10 bits subrange [81]-[82], two-step [83], and pipeline [84] ADCs, the resistor has been used to generate a DAC output to form a residue for the following stage. The matching of resistor string elements and the operation speed was proven by the 10-bit 50 MHz DAC [85][86]. For the resistor string matching requirement of n -bit and assume that the resistor values are normally distributed with mean R and standard deviation σ_R , the mean and the variance of the n -bit resistor string (RS_n) that consists of 2^n resistors connected in series can be described as:

$$mean(RS_n) = 2^n R \tag{6.1}$$

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$$\text{var}(RS_n) = 2^n \sigma_R^2 \quad (6.2)$$

Since the worst deviation from the ideal value occurs at the mid-point of the resistor string, one can model this as two big segments of resistors. (6.2) can be written such that each segment matching of a resistor string can be represented as normal distribution with

$$\begin{aligned} \text{mean}(RS_{n/2}) &= 2^{n/2} R \\ \text{var}(RS_{n/2}) &= 2^{n/2} \sigma_R^2 \end{aligned} \quad (6.3)$$

The deviation must be less than $\pm 1/2$ LSB of N -bit ADC from the gain accuracy requirement. Assuming that the each segment of the resistor string can be represented as a mean value and a standard deviation, this resistor matching condition can be described as

$$\frac{1}{2} \left(1 - \frac{1}{2^N}\right) \leq \left| \frac{2^{n-1} R \pm 2^{(n-1)/2} \sigma_R}{2^{n-1} R \pm 2^{(n-1)/2} \sigma_R + 2^{n-1} R \pm 2^{(n-1)/2} \sigma_R} \right| \leq \frac{1}{2} \left(1 \pm \frac{1}{2^N}\right) \quad (6.4)$$

To maximize the effect of mismatch, one part of the segment has a positive sign while the other has a negative sign in the variation. With this assumption, (6.4) becomes

$$\frac{\sigma_R}{R} = 2^{(n-1)/2 - N} \quad (6.5)$$

where n is the resolution and N is the linearity in bits [82]. For example, if 10-bit resolution and 10-bit linearity is needed, $\frac{\sigma_R}{R}$ should be $< 3.1\%$. For the 0.35 μm CMOS

process, the poly resistor matching parameter is $\frac{\sigma_R}{R} = \frac{12\% \mu\text{m}}{\sqrt{WL}}$, therefore it is possible

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to satisfy the 3.1% matching requirement by choosing the appropriate WL for the reference resistor in this ADC design.

Another non-ideal effect of reference ladder is transient bowing. It arises in CMOS A/D converter wherein the comparators employ switched capacitors at their input. CMOS comparator often incorporates offset cancellation for resolutions of 8 bits or above. As illustrated in Fig. 6.1, a CMOS inverting amplifier operates as a comparator [39]. In the sampling mode, S_1 and S_3 are on and S_2 is off. Thus, V_{in} is sampled on C_{in} . During comparison, only S_2 is on but the inverter generates an output voltage proportional to the difference between the V_{in} and V_{ref} . Since C_{in} is switched between the V_{in} and V_{ref} every clock cycle, this effect is equivalent to a resistive path between V_{in} and V_{ref} , introducing ac bowing along the ladder. In addition, the accuracy of the reference voltage is also limited by the settling time. For high speed operation, the sampling capacitor is switched to a tap point, thus creating the voltage glitch. This transient has to settle down to a given accuracy within a given period of time. The worst case setting time occurs at the middle tap, where the equivalent R value is half of the total resistance plus the switch resistance. Thus, the resistance of reference resistor must provide adequate bias current to the fast-settling comparator, so the voltage reference because source or sink quite a large current.

6.2 Clock Generator

The clock generator for producing non-overlapping clock signals can be realized with a simple typical circuit as shown in Fig. 6.2. It is based on the falling edge

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of the input clock passes immediately through one NOR gate, while the rising edge has first to propagate through the other NOR gate and the cascaded delay element. The resulted non-overlapping signals CLK1 and CLK2 have a non-overlapping time equal to the sum of the delays at the NOR gate and the delay element. The delay element is usually realized with an even-numbered chain of inverters. The main advantage of this circuit stems from its simplicity and robustness. In high-speed ADC, the non-overlap time becomes larger than necessary one because of the inverter-based buffer included and the margin added to accommodate the process and temperature variations. Furthermore, the duty cycle of the generated clock signals is inherited from the input clock, requiring it to be close to 50%.

Fig. 6.2 A simple clock generator

(a)

(b)

Fig. 6.3 (a) Timing Requirement for Coarse and Fine ADCs
(b) Generation of fine clock by coarse clock

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Since the ADC includes one coarse ADC and two interleaved fine ADCs, the speed of each fine ADC is only half of the speed of coarse ADC. That means the clock cycle of fine ADC is double of that of the clock cycle of coarse ADC. These two fine clocks should be symmetrical as shown in Fig. 6.3(a), to minimize the mismatch between two interleaved ADCs. Normally, the fine clock is accomplished by a frequency divider [87], producing FCLK with a nominal duty cycle of 50% even if the duty cycle of CCLK1 and CCLK2 deviates from 50%. Then, FCLK₁ and FCLK₂ are generated by the non-overlap circuit as shown in Fig. 6.3 (b). In reality, the devices in the non-overlap circuit or the frequency divider suffer from substantial mismatches and process variation. This introduces large timing errors between FCLK₁ and FCLK₂ at high speed operation. Since a 10-bit ADC sampling a 150-MHz signal cannot tolerate timing mismatches greater than 12 ps roughly, the frequency division does not provide the required accuracy in this design.

The problem of timing mismatch can be considerably relaxed if a single coarse clock drives both FCLK₁ and FCLK₂. Fig. 6.4 illustrates how this is accomplished by synchronizing the falling edge. Four switches, S11, S12, S21 and S22, and two control signals, Ctr1 and Ctr2, are added to the system. Non-overlapping coarse clock, Cclk1 and Cclk2, is provided to the two channels through the four switches. The actual sequence of operation is as follows: During Ctr1, the falling edge of Cclk1 is routed to Fclk1 through switch S11 and the rising edge of Cclk2 to Fclk2 through switch S22. During Ctr2, the falling edge of Cclk1 is rerouted to Fclk2 and the rising edge of Cclk2 to Fclk1. This concept can be easily extended to more channels for the synchronization of more signals.

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Fig. 6.4 (a) Timing of Clock Edge Synchronization
(b) Implementation

The timing mismatch is now equal to the propagation delay mismatch between two switches S11 and S21, a value that can be very small even with mismatch between the sizes of the switches. The timing of Ctr1 and Ctr2 is quite relaxed as they contain the falling edge of Cclk1 and the rising edge of Cclk2 with enough margin. Thus, Ctr1 and Ctr2 can be produced by a simple non-overlapping clock for fine ADC even under the process variation.

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6.3 Digital Error Correction

In order to relax the offset requirement for comparator, the simple digital error correction scheme has been introduced [46]. The digital error correction scheme for coarse ADC is illustrated in Fig. 6.5 as an example. After the coarse conversion, the MSB is generated and they determine the input voltage, V_{in} , in the range between V_{r-1} and V_r . However, V_{in} may not be absolutely in this range due to the non-ideal effect in coarse comparator, and so wrong decision on reference segment may occur. Thus, V_{in} is compared with a larger reference range extend to the two side of selected reference segment, which include the upper overlap range where the reference voltage is higher than V_r and the lower overlap range where the reference voltage is smaller than V_{r-1} as shown in Fig. 6.5. Once the fine comparison is completed, the LSB are generated. They are used determine where V_{in} is located in. Thus, the correction of MSB can be expressed as

$$MSB = \begin{cases} MSB + 1 & V_{in} > V_r \\ MSB & V_{r-1} < V_{in} < V_r \\ MSB - 1 & V_{in} < V_{r-1} \end{cases} \quad (6.6)$$

From (6.6) and Fig. 6.5, if V_{in} lies in the selected reference range between V_{r-1} and V_r , there is no need for the correction on the MSB. If V_{in} is in the upper overlap range, or in the lower overlap range, the MSB should be adjusted by adding 1 or subtracting 1 through the correction logic separately. The digital error correction scheme relaxes the accuracy requirement for coarse ADC. The penalty using a digital error correction is that it requires a redundant comparator and correction logic.

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Fig. 6.5 Error Correction

6.4 Encode Circuit

As discussed before, the output of the comparator is based on thermometer code. For V_{ref} larger than V_{in} , it will have a logic 1 output but vice versa for V_{ref} less than V_{in} . An encode circuit is needed to get binary digital output. As shown in Fig. 6.6, the encode circuit include two parts. An AND gate circuit is used to detect the transition of the comparator outputs from 1s to 0s, with asserted logic 1 output. All other AND gate outputs will be logic 0, resulting in simpler encoding. Each AND gate has three inputs instead of two inputs. The addition input is used to remove the bubble error where alone 1 occur within the string of 0s (or a 0 within the string of 1s) due to the comparator metastability, noise, cross talk, limited bandwidth and so forth. These bubbles usually occur near the transition point of the thermometer code. There must be

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one 1 above two 0s in determining the transition pointing the thermometer code. As a result, the bubble error can be removed with little extra complexity.

Fig. 6.6 Encode Circuit

Although the AND gate performs the function of a priority encoder, determining the position of the highest comparator to produce a logic 0 output, the block that reduces the thermometer code from 2^N logic signals to an N-bit word usually implemented by a ROM. The AND gates in the thermometer decoder, by producing just one active output signal, deliver a unique address to ROM for each quantization level of ADC. In CMOS technology, there are a number of options which can be used to implement the ROM, which is grouped into static ROM and dynamic ROM. The dynamic ROM is chosen for the purpose of high speed and low power consumption. A 3 bit ROM is illustrated in Fig. 6.7 as an example. To reduce the static power while

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reducing the total number of transistors, a single-clocked PMOS pullup can be used for each bit line. It requires precharge the bit line to the high level prior to enable the thermometer code to be presented to the encoder inputs. As shown in Fig. 6.7, when CLK is low, M_{n1} , M_{n2} , M_{n3} turn off and M_{p1} , M_{p2} , M_{p3} precharge the output node B_1 , B_2 , B_3 to VDD. When CLK goes high, M_{p1} , M_{p2} , M_{p3} turn off and M_{n1} , M_{n2} , M_{n3} turn on. The NMOS transistors, M_1 - M_{12} , is controlled by input data $D_0 \sim D_6$ which are the output of AND gate and pull down the corresponding bit line. For instance, if only D_4 is 1, B_2 and B_3 are pull down to 0 by M_3 and M_4 when CLK is high. Thus, 100 binary code is obtained. The binary output $B_1 B_2 B_3$ is then evaluated and fed to the following register array and eventually the output driver.

Fig. 6.7 3-bits ROM Design

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6.5 Biasing Circuit

Fig. 6.8 Biasing Circuit

Fig. 6.8 depicts the biasing circuit. It consists of an n-channel current mirror pair M1-M2 and a resistor R1 to derive the biasing current through self-biased high-swing p-channel cascode current mirror (M3-M6). The gate voltages of M3 and M4 are obtained from the diode-connected transistor M7, in which the current is derived from the bias loop via current mirror transistor M8.

In order to ensure that the circuit can operate in desired operation condition, a start-up circuit is added to the biasing circuit, which includes transistors M9-M12. Before power up, all currents in the bias loop are zero, M11 will be off. During power on process, M12 operates at triode region and serves as an active load, the gates of M9 and M10 will be pulled high due to the very high impedance arising from the off state of M11. Transistors M9 and M10 then turn on, forcing currents to conduct in current mirror pairs to start up the bias loop. Once the loop has been started, M11 will turn on, sinking all of the current from M12 to ground via M11. The gate bias of M9 and M10 is then pulled low, and thereby turning them off so they no longer affect the bias loop.

CHAPTER 7

I/O INTERFACE DESIGN

Except the core ADC, the I/O interface design is taken special consideration for relieving the testing problem caused by the package, PCB board and other testing components. In this chapter, the characteristics of different source followers are studied and thorough analyzed, and the application of the appropriate source follower for the design of analog input interface is presented. Besides, the digital output interface circuit is also discussed.

7.1 Introduction

After design, layout and fabrication, the ADC will be packaged. There exists many parasitics associated with the package. For example, the simple dual-in-line package (DIP), with a die mounted in its center cavity and bonded to the pads on the perimeter of the cavity, it exhibits parasitics such as bonding wire self-inductance, trace self-inductance, trace-to-ground capacitance, trace-to-trace mutual inductance and trace-to-trace capacitance. Thus, the connection between the circuit and the external world are far from ideal. These parasitics associated with the package and connections to the chip introduce testing difficulties in the evaluation of actual performance of high-speed ADC for embedded applications. Therefore, care must be taken to maintain the

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performance of ADC in the presence of lead and package inductance and capacitive loading.

For high-speed ADC testing, the focus is concerned with the quality analog input interface and digital output interface. An understanding of the input structure of the ADC is necessary in order to permit proper design. For switched-capacitor-based ADCs in CMOS processes, they typically connect the switched capacitor circuit directly to the analog input, thereby generating transient current pulses. These transients may significantly degrade performance if the settling time of the op amps are not sufficiently fast, which result in some degradation in the ADC performance. Normally, ADCs may adopt external drive amplifier to provide a buffer for the analog input signal. However, the bond-wire and package inductance of several nanohenries are always present and much larger values are often created, which increase the challenge for external input driving circuit, especially with high input frequency at high sampling frequency. It was found from SPICE simulations that ADC chip with package could display oscillation at frequencies in hundred of megahertz range, with a number of combinations of parasitic inductance (as low as several nanohenries but larger values made the problem even worse) and capacitive loading. One way to relieve this problem is to use an internal buffer to drive the input signal. The transient response of this internal driver circuitry can have a significant affect on the perceived performance of high-speed ADC. In order to obtain the optimal performance from the ADC, the buffer used to drive the A/D converter should have better linearity than the intrinsic A/D converter. The bandwidth should be sufficient as to not to cause attenuation at higher frequencies due to gain distortion. The transient currents and voltages at the output of the amplifiers should sufficiently settle before the A/D converter being instructed to

sample its input signal. Therefore, the internal buffer must be carefully designed so that its distortion performance is better than that of the ADC.

In addition to analog interface, the digital output interface should also be designed carefully. In order to drive the high capacitive loading due to the package with high-speed data transfer, an output stage with high drive ability is needed. These high-speed digital outputs with rail-to-rail signal swing may couple back transients via various parasitic capacitive paths, thus causing the test chip and PCB board in very noisy environment. External capacitive loading at PCB board and external logic circuits exacerbate this problem. Thus, the output interface must have characteristic having high speed, high drive ability whilst minimizing the potential digital noise as low as possible.

7.2 Study of Source Followers for Buffer Design

7.2.1 Background

Buffer with feedback can achieve high linearity [88]. However, bandwidth is limited due to frequency compensation, and it is not suitable for high-speed operation. Although an adaptive-biased buffer [89] exhibits high slew rate, reasonably low distortion with improved bandwidth, the circuit is quite complex. Alternatively, an open-loop buffer is desirable for high-speed applications due to its high stability at broad bandwidth. The source follower is one of the simplest structures to implement a high-speed internal buffer in CMOS process [40][90] technology on the basis of its intrinsic simplicity together with high bandwidth characteristic. However, they suffer

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from several non-ideal effects, including body effects, channel-length modulations, signal-dependent capacitive effects and frequency-dependent distortions arising from the capacitive load. These non-ideal factors will create a tradeoff among linearity, bandwidth and power consumption that present a significant design challenge. The cascode approach [89] is proven to yield high linearity but it may not be suitable for use in modern VLSI deep-submicron CMOS processes with low supply voltages. Therefore, the focus is to investigate different types of source followers that allows for wide-bandwidth, low-distortion operation for ADC input buffer design at a single 3V supply.

The distortion analysis of a standard MOS source follower has been reported in [91]. This analysis is based on nonlinear parameters, g_m and g_{ds} , in a low-frequency small-signal model. Further distortion analysis using the methods of [92]-[93] extends the peculiar small-signal model with additional frequency-dependent capacitive effects, enabling the analysis of high-frequency distortion in analog integrated circuits. When the signal amplitude is increased to sufficiently high levels, the large-signal analysis approach introduced in the foundation work by [94] may be suitable because it deals directly with the nonlinear large-signal current source. Despite the fact that the analysis [94] is conducted on a low-frequency basis, the high-frequency distortion behavior of PMOS source follower (PSF) and NMOS source follower (NSF) has been addressed in recent research efforts by [95]. Thus, the ultimate goal is to analyze and investigate the high-frequency harmonic distortion performance of the source followers using a large-signal approach. This is essentially important because the input signal to the ADC could be a large signal.

In view of the complexity introduced by including every parasitic of the large-signal model [96] in second-order analysis, a simplified approach has been adopted in this work to eliminate non-dominant parasitic elements so that the ultimate model is amenable for hand analysis without losing much accuracy. This analysis is crucial because it provides significant insight and understanding as to how the process and design parameters impact the linearity of source followers under high-frequency large-signal conditions.

7.2.2 Large Signal Models and Assumptions

Fig. 7.1 shows a complete large-signal model for an MOS transistor [96]. The primary purpose of the diodes is to model the dc leakage currents which are small enough to be ignored in dc analysis. For ac consideration, the parasitic resistors and capacitors are key elements that determine the frequency response of the MOS transistor. In typical CMOS sub-micron technology like the 0.35 μm CMOS standard process, it can be estimated that the maximum time constant is 3.25 ps for a 10 pF capacitive load (using an example of a practical NMOS transistor layout with channel width $W = 200 \mu\text{m}$). Consequently, when operating in the range of a few hundred MHz with the given technology, neglecting r_D and r_S does not cause significant inaccuracy in the prediction of the harmonics of the source followers. For parasitic capacitors consideration, C_{GB} can be neglected due to the shield of the inverted channel. C_{GD} is treated as a parasitic capacitor with a constant value when the transistor operates in the saturation region. C_{GS} in conjunction with the lumped output capacitive load, contributes to a feed-forward effect. However, as far as the output follows the input in

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source follower design and the effective output capacitive load is made dominant, C_{GS} can be ignored for simplification, without introducing unacceptable levels of error. Although the non-linear junction capacitances, C_{BD} and C_{BS} , are subject to signal-dependent bias, their capacitances can be treated as nominal capacitances based on nominal biasing voltage for simplified analysis. Taking into account the dominant elements mentioned, a simplified large-signal model that is suitable for the large-signal analysis of source followers is depicted in Fig. 7.2. In contrast to the voltage-controlled current source in the small-signal model, the current source I_d is a large-signal current source and the model includes second-order effects such as body effect, channel-length modulation and so forth. All the transistors in the source followers are assumed to operate in saturation region.

All the equations presented in the following paragraphs refer to the NMOS transistor. In general, the subscript n denotes NMOS based parameters whilst p denotes the PMOS based counterparts. Prior to the analysis, we describe the assumptions relating to the other dominant second-order effects as follows.

Fig. 7.1 Complete Large-Signal Model for MOS Transistor

Fig. 7.2 Simplified Large-Signal Model for Analysis of Source Follower

Body effect occurs when the bulk potential is not equal to the source potential in an MOS transistor. This is a significant effect because of the increasing value of threshold voltage that arises through bulk modulation and the generation of a dominant second harmonic that dictates the total harmonic distortion (THD) in a large-signal condition. The threshold voltage for an NMOS transistor can be approximated as

$$V_{thn} \cong V_{thn0} + K1_n (\sqrt{2\Phi_{fn} + V_{SB}} - \sqrt{2\Phi_{fn}}) \quad (7.1)$$

where V_{thn0} is the threshold voltage when bulk is connected to source, $K1_n$ is the first-order body coefficient and Φ_{fn} is the Fermi level.

In addition, the channel length modulation causes error in low-frequency gain and generates harmonics. It is particularly pronounced for short channel transistors. For accurate hand analysis, the drain current using the non-ideal square law equation [98] for NMOS transistors is assumed as follows:

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$$I_d = \frac{k'_n W}{2L_{eff} A_{bulkn}} (V_{GS} - V_{thn})^2 (1 + \lambda_n V_{DS}) \quad (7.2)$$

with $A_{bulkn} \cong 1 + \frac{A_{0n} K l_n}{2\sqrt{2\Phi_{fn} + V_{SB}}}$ and $k'_n \cong \mu_{0n} C_{ox}$, where μ_{0n} is the mobility of NMOS

device, C_{ox} is the gate capacitance per unit area, A_{bulkn} represents the bulk charge factor due to the non-uniform depletion region along the channel and A_{0n} is the bulk charge coefficient. For ease of hand analysis, λ_n is simplified from the BSIM3 model equations [98] as follows:

$$\lambda_n = \frac{1}{V_A} \cong \frac{1}{V_{Asat} + V_{ACLM}} \quad (7.3)$$

with $V_{Asat} = E_{sat} L_{eff} + V_{dsat}$, $V_{ACLM} = \frac{1}{P_{CLMn}} \frac{A_{bulkn} E_{sat} L_{eff} + (V_{gs} - V_{th})}{A_{bulkn} E_{sat} l_n} (V_{ds} - V_{dsat})$ and

$l_n = \sqrt{\frac{\epsilon_{si} T_{ox} X_{jn}}{\epsilon_{ox}}}$, where P_{CLMn} is the correction factor for channel length modulation,

X_{jn} is the junction depth, and E_{sat} corresponds to the critical electrical field at which the carrier velocity becomes saturated. Since $E_{sat} L_{eff} \gg V_{dsat}$,

$A_{bulkn} E_{sat} L_{eff} \gg (V_{gs} - V_{th})$ and $V_{ds} \gg V_{dsat}$ in this application, (7.3) can be simplified

as

$$\lambda_n = \frac{1}{V_{Asat} + V_{ACLM}} \cong \frac{1}{E_{sat} L_{eff} + \frac{1}{P_{CLMn}} \frac{L_{eff}}{l_n} V_{ds}} \quad (7.4)$$

7.2.3 Analysis of Source Followers

7.2.3.1 Harmonic distortion Analysis

The linearity of a circuit can be evaluated by the harmonic distortion. The second harmonic distortion is most significant under the large-signal condition [95]. It is typically at least several times larger than other distortion terms, so its value can be approximated as the total harmonic distortion. According to the power series expansion in [94],[97], the input-output function of a nonlinear system is normally expressed as

$$V_i = f(V_o) = \sum_{n=0}^{\infty} \frac{f^{(n)}(V_o = V_{oQ})}{n!} (V_o - V_{oQ})^n = \sum_{n=0}^{\infty} b_n (v_o)^n \quad (7.5)$$

with $b_0 = f(V_o = V_{oQ})$, $b_1 = f'(V_o = V_{oQ})$ and $b_2 = \frac{f''(V_o = V_{oQ})}{2}$, where the input voltage V_i is a function of the output voltage V_o . Since the constant b_0 is the dc input voltage, (7.5) can be written as

$$v_i = \sum_{n=1}^{\infty} b_n (v_o)^n = b_1 v_o + b_2 v_o^2 + b_3 v_o^3 + \dots \quad (7.6)$$

To find the harmonic distortion, (7.6) can be rearranged [99] as

$$v_o = \sum_{n=1}^{\infty} a_n (v_i)^n = a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \dots \quad (7.7)$$

According to (7.6) and (7.7), it can be related that $a_1 = \frac{1}{b_1}$ and $a_2 = -\frac{b_2}{b_1^3}$. Let

$v_i = V_m \sin \omega t$, where V_m is the peak amplitude of input signal. We have

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$v_o = a_1 V_m \sin \omega t + a_2 (V_m \sin \omega t)^2 + \dots$. Thus, the second harmonic distortion of a nonlinear system is obtained as [100]:

$$HD_2 \equiv \frac{1}{2} \frac{a_2}{a_1} V_m = \frac{1}{2} \frac{b_2}{b_1^2} V_m \quad (7.8)$$

A. NMOS Source Follower (NSF)

The NMOS source follower in Fig. 7.3 consists of an NMOS input transistor and an NMOS current source that drives a capacitive load C_L . The composite input signal V_i consists of the dc biasing voltage V_{IQ} and the ac signal v_i , whereas the composite output signal V_o consists of the dc biasing voltage V_{OQ} and the ac signal v_o . For n-well CMOS process, the bulks of NMOS transistors M_{1n} and M_{2n} are shared with the same substrate. As a result, the NSF suffers from a body effect. Distortion analysis [94] based on a low-frequency model is well established to reveal a nonlinear bulk modulation term. However, this may not be adequate for broad bandwidth source followers, in which both capacitive load current as well as bulk charge effects contribute additional distortion terms.

Fig. 7.3 NMOS Source Follower (NSF)

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Fig. 7.4 Simplified Large-Signal Model of NMOS Source Follower

Using the input and output notations while applying the simplified large-signal model (Fig. 7.2) to NSF in Fig. 7.3 yields the equivalent circuit of Fig. 7.4(a). With further simplification, Fig. 7.4 (a) in turn leads to Fig. 7.4(b), where the equivalent capacitive load is $C_{Leqn} = C_L + C_{BS1n} + C_{BD2n} + C_{GD2n}$. The ac current passing through the capacitive load C_{Leqn} is $j\omega C_{Leqn}(V_o - V_{OQ})$. It will be significant when the circuit operates at high frequency. As a result, the input transistor M_{1n} conducts a summed current of $I = I_n + I_{cn}$, with I_n and I_{cn} representing the dc biasing current and the frequency-dependent capacitive load current respectively. Using (7.2) and the prior defined terms in Fig. 7.4, the relationship between the currents in the transistors and capacitive load can be approximated as

$$I_n = I - I_{cn} \cong \frac{1}{2} \frac{k'_n (W/L_{eff})_{1n} (V_{GS1} - V_{thn})^2}{A_{bulkn}} - j\omega C_{Leqn} (V_o - V_{OQ}) \quad (7.9)$$

with $V_{thn} \cong V_{thn0} + K1_n (\sqrt{2\Phi_{fn} + V_o} - \sqrt{2\Phi_{fn}})$, $A_{bulkn} \cong 1 + \frac{A_{0n} K1_n}{2\sqrt{2\Phi_{fn} + V_o}}$. It is noted that

the channel length modulation is ignored because the nonlinearities arising from the

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body effect are dominated in NSF. From the definition of $V_{GS1} = V_i - V_o$, (7.9) can be rewritten in a form as

$$V_i = f(V_o) = V_o + V_{thn0} + K1_n (\sqrt{2\Phi_{fn} + V_o} - \sqrt{2\Phi_{fn}}) + \Delta V_n \sqrt{A_{bulkn} \left[1 + \frac{j\omega C_{Leqn}}{I_n} (V_o - V_{oQ}) \right]} \quad (7.10)$$

where $\Delta V_n = \sqrt{\frac{2I_n}{k'_n (W/L_{eff})_{1n}}}$ is the fundamental first-order gate over-drive voltage of

the input transistor. As can be seen in the fourth item of (7.10), the second-order effect contributed by the bulk charge factor A_{bulkn} and the frequency-dependent capacitive item becomes a multiplication function for the gate over-drive voltage. It is reasonable because the capacitive current modulates the gate-over drive voltage at high frequency. From (7.8) and (7.10), the second harmonic distortion of NSF is approximated as [see Appendix A]:

$$HD_{2_NSF} \cong \frac{\frac{-K1_n}{16(2\Phi_{fn} + V_{oQ})^{3/2}} + \frac{\Delta V_n A_{bulkn-Q}^{1/2}}{16} \left(\frac{\omega C_{Leqn}}{I_n} \right)^2 + \frac{\Delta V_n K1_n A_{0n}}{32 A_{bulkn-Q}^{1/2} (2\Phi_{fn} + V_{oQ})^{3/2}} \left[\frac{3}{2(2\Phi_{fn} + V_{oQ})} - \frac{j\omega C_{Leqn}}{I_n} \right]}{\left[1 + \frac{K1_n}{2(2\Phi_{fn} + V_{oQ})^{1/2}} \right]^2} V_m \quad (7.11)$$

where $A_{bulkn-Q}$ is defined as the bulk charge factor when $V_o = V_{oQ}$. In the numerator of (7.11), there are three non-ideal terms arising from second-order effects. The first body effect term is caused by the fundamental modulation of the threshold voltage. The second gate-overdrive term is linked to the capacitive load, with frequency-dependent characteristics. The third term is related to the cross-product term contributed by the interaction between the first and second terms. Thus, the third term is usually small

when compared to the others. At low frequencies, the second distortion term is relatively small and the harmonic distortion is dominated by the body effect term,

$$\frac{-K1_n}{16(2\Phi_{fn} + V_{oQ})^{3/2}}. \text{ However, with increasing frequency, the magnitude of the second}$$

frequency-dependent distortion term in (7.11) becomes more pronounced. As this

significant term $\frac{\Delta V_n}{16} A_{bulk_n-Q}^{1/2} \left(\frac{\omega C_{Leqn}}{I_n} \right)^2$ has the opposite sign to that of the major

$$\frac{-K1_n}{16(2\Phi_{fn} + V_{oQ})^{3/2}} \text{ term, the frequency-dependent distortion tends to counteract the}$$

body effect distortion at high frequency. Therefore, minimum harmonic distortion can be obtained at an optimum spot frequency.

B. PMOS Source Follower (PSF)

When dealing with the circuit of a PMOS source follower, it can be seen that most designs [95],[101] have utilized a body-tied PMOS input transistor to remove the bulk modulation based distortion and to improve the precision issue.

Fig. 7.5 PMOS Source Follower (PSF)

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Fig. 7.6 Simplified Large-Signal Model of PMOS Source Follower

Fig. 7.5 shows a conventional PSF in an n-well CMOS process which includes a PMOS input transistor and a PMOS current source. By applying the simplified large-signal model of Fig. 7.2 and introducing extra bulk-well capacitance to PSF in Fig. 7.5, we get Fig. 7.6(a). Fig. 7.6(b) is derived by further simplification where the equivalent capacitive load is $C_{Leqp} = C_L + C_{BD1p} + C_{BD2p} + C_{GD2p} + C_{w1p}$, and C_{w1p} is the bulk-well capacitance of M_{1p} . Similar to NSF, the current passing through the capacitive load C_{Leqp} cannot be ignored at high frequency. Hence, the input transistor M_{1p} conducts a current of $I = I_p - I_{cp}$, where I_p and I_{cp} represent the dc biasing current and the frequency-dependent capacitive load current respectively. It is noted that I_{cp} is equal to $j\omega C_{Leqp}(V_o - V_{OQ})$ whereas I_p is $I_{p0}[1 + \lambda_{2p}(V_{DD} - V_o)]$ due to the channel length modulation of M_2 , where I_{p0} represents the biasing current at quiescent point. In Fig. 7.6(b), the relationship between the currents in the transistors and the capacitive load can be established as

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$$I_{p0}[1 + \lambda_{2p}(V_{DD} - V_o)] = I + I_{cp} \cong \frac{1}{2} \frac{k'_p (W/L_{eff})_{1p} (V_{SG1} - V_{thp0})^2}{A_{bulkp}} (1 + \lambda_{1p} V_o) + j\omega C_{Leqp} (V_o - V_{OQ}) \quad (7.12)$$

where $\lambda_{1p} \cong \frac{1}{E_{sat} L_{1peff} + \frac{L_{1peff}}{P_{CLMp}} V_o}$ and $\lambda_{2p} \cong \frac{1}{E_{sat} L_{2peff} + \frac{L_{2peff}}{P_{CLMp}} (V_{DD} - V_o)}$ are the

channel length modulation factors for M_1 and M_2 respectively and

$$A_{bulkp} \cong 1 + \frac{A_{op} K1_p}{2\sqrt{2}\Phi_{fp}}. \text{ From the definition of } V_{SG1} = V_o - V_i, \text{ the input voltage on the}$$

basis of (7.12) can be expressed as

$$V_i = f_p(V_o) = V_o - V_{thp0} - \Delta V_p \sqrt{\frac{A_{bulkp}[1 + \lambda_{2p}(V_{DD} - V_o)] - \frac{j\omega C_{Leqp}}{I_{p0}}(V_o - V_{OQ})}{1 + \lambda_{1p} V_o}} \quad (7.13)$$

where $\Delta V_p = \sqrt{\frac{2I_{p0}}{k'_p (W/L_{eff})_{1p}}}$ is the first-order gate-overdrive voltage of the input

transistor. Like the gate-overdrive terms (7.10) in NSF that include the usual bulk charge factor and frequency-dependent capacitive term, the multiplication function is further complicated with additional channel-length modulation factors as observed in the third item in (7.13). Using routine analysis to find the respective coefficients for b_1 and b_2 , and applying the second harmonic distortion definition (7.8), the second harmonic distortion of PSF can be simplified as [see Appendix B]:

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$$\begin{aligned}
HD_{2_PSF} \cong & \frac{\Delta V_p \sqrt{A_{bulkp}}}{16} V_m \left\{ \frac{4}{P_{CLMp}} \frac{L_{1peff}}{I_p} (E_{sat} L_{1peff} \lambda_{1pQ}) (\lambda_{1pQ}^2 - \lambda_{2pQ}^2 \frac{\lambda_{2pQ}}{\lambda_{1pQ}} \frac{L_{2peff}^2}{L_{1peff}^2}) \right. \\
& + (\lambda_{2pQ} E_{sat} L_{2peff})^2 (3\lambda_{1pQ}^2 \frac{L_{1peff}}{L_{2peff}} - \lambda_{2pQ}^2) + (\lambda_{1pQ} E_{sat} L_{1peff})^2 (3\lambda_{1pQ}^2 - \lambda_{2pQ}^2 \frac{L_{2peff}}{L_{1peff}}) \\
& \left. + (\frac{\omega C_{Leqp}}{I_{p0}})^2 + 2 \frac{j\omega C_{Leqp}}{I_{p0}} E_{sat} L_{1peff} (\lambda_{1pQ}^2 - \lambda_{2pQ}^2 \frac{L_{2peff}}{L_{1peff}}) \right\}
\end{aligned} \tag{7.14}$$

Note that λ_{1pQ} , λ_{2pQ} are the constant values for λ_{1p} and λ_{2p} respectively when $V_o = V_{OQ}$. The appearance of the squared lambda terms stems from the double differentiation of (7.13) to obtain the coefficient b_2 according to (7.5) and the definition of (7.8). From (7.14), the second harmonic distortion of PSF is now governed by the channel length modulation and frequency-dependent factor. At low frequency, the frequency-dependent terms are negligible such that the channel length modulation terms become dominant. The harmonic distortion of PSF is expected to attain a low value because of the subtraction from the finite channel length modulation terms $\alpha_i \lambda_{1pQ}^2 - \beta_j \lambda_{2pQ}^2$ arising from two PMOS transistors, where α_i and β_j denote the respective constants for individual squared lambdas. It is also observed that the HD_{2_PSF} is basically the sum of all corresponding difference of squared lambda terms having first-order coefficient $(E_{sat} L_{1peff} \lambda_{1pQ})$ and higher-order coefficients $(E_{sat} L_{1peff} \lambda_{1pQ})^2$ and $(E_{sat} L_{2peff} \lambda_{2pQ})^2$. The PSF exhibits better linearity than the NSF because the lambda-based terms are smaller than bulk modulation terms at low frequency. However, at higher frequency, the dominant frequency-dependent term $(\frac{\omega C_{Leqp}}{I_{p0}})^2$ will swamp the finite values of the lambda-based terms, and so the harmonic distortion increases monotonically with frequency.

C. Cascade-Complementary Source Follower (CCSF)

A cascaded source follower structure can be implemented in two possible forms: a cascade of PSF and NSF or a cascade of NSF and PSF. Their usual common goal is to alleviate the level shift problem arising from a single source follower stage. However, based on the analytical results of the prior NSF, a possibility arises of optimizing low-distortion CCSF – one that has never been reported so far. Intuitively, the new linearization method is achieved by generating the intentional body effect and frequency-dependent effect from the bulk-modulated PSF (M_{1p} , M_{2p}), with the bulks being tied to the supply instead of being self-tied to the respective source in the first stage. This will compensate for those of the nonlinear terms of NSF (M_{1n} , M_{2n}) with the common substrate serving as the bulk in the second stage as shown in Fig. 7.7. The NSF in CCSF is arranged in the final stage because it has higher drive ability and bandwidth than its PSF counterpart.

Fig. 7.7 Cascade-Complementary Source Follower (CCSF)

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Fig. 7.8 Large-Signal Model of CCSF

The equivalent circuit of Fig. 7.7 is illustrated in Fig. 7.8(a) and its simplification using a large-signal model is shown in Fig. 7.8(b). It is noted that the equivalent capacitive load for NSF is $C_{Leqn} = C_L + C_{BS1n} + C_{BD2n} + C_{GD2n}$ and the equivalent capacitive load for PSF is $C_{Leqp} = C_{BS1p} + C_{BD2p} + C_{GD2p} + C_{GD1n}$. The capacitive load of NSF is usually dominated by the linear load C_L whereas the capacitive load of PSF is governed by the sum of nonlinear junction capacitances. As can be seen in Fig. 7.7 and Fig. 7.8(b), the input transistor M_{in} conducts a summed current of $I = I_n + I_{cn}$. The composite signal V_x consists of the dc biasing voltage V_{xQ}

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and the ac signal v_x . Hence, similar to (7.10), the input-output relationship of NSF can be expressed as

$$V_x = V_o + V_{thn0} + K1_n(\sqrt{2\Phi_{fn} + V_o} - \sqrt{2\Phi_{fn}}) + \Delta V_n \sqrt{A_{bulkn} \left[1 + \frac{j\omega C_{Leqn}}{I_n} (V_o - V_{OQ}) \right]} \quad (7.15)$$

For PSF, the input transistor M_{1p} conducts a current of $I = I_p - I_{cp}$. Similar to (7.13), the input-output relationship of PSF can be expressed as

$$V_i = V_x - V_{thp0} - K1_p(\sqrt{2\Phi_{fp} + (V_{DD} - V_x)} - \sqrt{2\Phi_{fp}}) - \Delta V_p \sqrt{A_{bulkp} \left[1 - \frac{j\omega C_{Leqp}}{I_p} (V_x - V_{XQ}) \right]} \quad (7.16)$$

where A_{bulkn} is given in the prior NSF analysis and $A_{bulkp} \cong 1 + \frac{A_{0p}K1_p}{2\sqrt{2\Phi_{fp} + V_{DD} - V_x}}$ for

PMOS transistor. Since the expansion of the square root based V_x terms in (7.16) would be small, it can be replaced with the first-order approximated V_x term from (7.15), with

$$V_x \cong V_o + V_{GS_Q} \quad \text{and} \quad V_{GS_Q} = V_{thn0} + K1_n(\sqrt{2\Phi_{fn} + V_{OQ}} - \sqrt{2\Phi_{fn}}) + \Delta V_n \sqrt{A_{bulkn}}.$$

Substituting the V_x (7.15) into the first term of (7.16) and the approximated V_x term into the square root terms of (7.16), we obtain

$$\begin{aligned} V_i = & V_o + V_{thn0} + K1_n(\sqrt{2\Phi_{fn} + V_o} - \sqrt{2\Phi_{fn}}) + \Delta V_n \sqrt{A_{bulkn} \left[1 + \frac{j\omega C_{Leqn}}{I_n} (V_o - V_{OQ}) \right]} \\ & - V_{thp0} - K1_p(\sqrt{2\Phi_{fp} + [V_{DD} - (V_o + V_{GS_Q})]} - \sqrt{2\Phi_{fp}}) - \Delta V_p \sqrt{A_{bulkp} \left[1 - \frac{j\omega C_{Leqp}}{I_p} (V_o + V_{GS_Q} - V_{XQ}) \right]} \end{aligned} \quad (7.17)$$

From our routine analysis as described before, the second harmonic distortion of CCSF can be expressed as [see Appendix C]:

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$$\begin{aligned}
& -\frac{K1_n}{16(2\Phi_{fn} + V_{OQ})^{3/2}} + \frac{\Delta V_n A_{bulkn-Q}^{1/2}}{16} \left(\frac{\omega C_{Leqn}}{I_n} \right)^2 \\
& + \frac{\Delta V_n K1_n A_{0n}}{64 A_{bulkn-Q}^{1/2} (2\Phi_{fn} + V_{OQ})^{3/2}} \left(\frac{3}{(2\Phi_{fn} + V_{OQ})} - \frac{2j\omega C_{Leqn}}{I_n} \right) \\
& + \frac{K1_p}{16[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS-Q})]^{3/2}} - \frac{\Delta V_p A_{bulkp-Q}^{1/2}}{16} \left(\frac{\omega C_{Leqp}}{I_p} \right)^2 \\
& - \frac{\Delta V_p K1_p A_{0p}}{64 A_{bulkp-Q}^{1/2} [2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS-Q})]^{5/2}} \left(\frac{3}{[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS-Q})]} - \frac{2j\omega C_{Leqp}}{I_p} \right) \\
HD_{2_CCSF} \cong & \frac{\left(\frac{3}{[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS-Q})]} - \frac{2j\omega C_{Leqp}}{I_p} \right)}{\left(1 + \frac{K1_n}{2(2\Phi_{fn} + V_{OQ})^{1/2}} + \frac{K1_p}{2[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS-Q})]^{1/2}} \right)^2} V_m
\end{aligned} \tag{7.18}$$

From (7.18), similar to NSF, the CCSF includes nonlinearities due to the bulk modulation of threshold voltage, the gate-overdrive term with the frequency-dependent effect via capacitive load and the non-dominant cross-product term linked to the former items. All items in the numerator caused by the NSF have their corresponding counterparts with opposite signs generated by the PSF. The low distortion optimization strategy can be formulated by (i) minimizing the summed value of the dominant

frequency-independent pair, $-\frac{K1_n}{16(2\Phi_{fn} + V_{OQ})^{3/2}}$ and

$+\frac{K1_p}{16[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS-Q})]^{3/2}}$, by finding the optimum V_{OQ} , and by (ii)

minimizing the summed value of the dominant frequency-dependent pair

, $+\frac{\Delta V_n A_{bulkn-Q}^{1/2}}{16} \left(\frac{\omega C_{Leqn}}{I_n} \right)^2$ and $-\frac{\Delta V_p A_{bulkp-Q}^{1/2}}{16} \left(\frac{\omega C_{Leqp}}{I_p} \right)^2$, by finding the optimum

C_{Leqp} or C_{Leqn} for balance cancellation.

From the above analysis, the linearity of PSF exhibits highest value at low frequency in absence of body effect but it drops at high frequency because the frequency-dependent item $\left(\frac{\omega C_{Leqp}}{I_{p0}}\right)^2$ dominates at high frequency as observed in

(7.14). For NSF analytical result in (7.11), its nonlinearity arising from body effect is high for all frequencies but the presence of the frequency-dependent component

$\frac{\Delta V_n}{16} A_{bulkn-Q}^{1/2} \left(\frac{\omega C_{Leqn}}{I_n}\right)^2$ will reduce the body effect component $\frac{-K1_n}{16(2\Phi_{fn} + V_{OQ})^{3/2}}$ at

high frequency. For CCSF analytical result in (7.18), the THD will be definitely lower than the NSF but not the PSF at low frequency due to incomplete cancellation between

the n-channel body effect term $-\frac{K1_n}{16(2\Phi_{fn} + V_{OQ})^{3/2}}$ and the p-channel body effect

term $+\frac{K1_p}{16[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS-Q})]^{3/2}}$. However, for proper design, the linearity of

CCSF can outperform than that of PSF at high frequency range because the linearity of PSF degrades significantly at high frequencies. The harmonic distortion of the various source followers will be validated by the simulation results in Chapter 9.

7.2.3.2 Large Signal Transfer Function

Based on the input and output signals defined as $V_i = V_{IQ} + v_i$ and

$V_o = V_{OQ} + v_o$, $V_i = f(V_o)$ can be rewritten as

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$$v_i = -V_{IQ} + f(V_o) \cong -V_{IQ} + f(V_o = V_{OQ}) + f^{(1)}(V_o = V_{OQ})v_o \quad (7.19)$$

Since, $f(V_o = V_{OQ}) = V_{IQ}$, the large signal transfer function can be expressed as

$$H = \frac{v_o}{v_i} \cong \frac{1}{f^{(1)}(V_o = V_{OQ})} \quad (7.20)$$

For NSF, according to (7.10) and (7.20), the large-signal transfer function of NSF becomes

$$H_{NSF} \cong \frac{1}{1 + \frac{K1_n}{2(2\Phi_{fn} + V_{OQ})^{1/2}} - \frac{\Delta V_n}{8A_{bulkn-Q}^{1/2}} \frac{K1_n A_{0n}}{(2\Phi_{fn} + V_{OQ})^{3/2}} + \frac{\Delta V_n A_{bulkn-Q}^{1/2}}{2} \frac{j\omega C_{Leqn}}{I_n}} \quad (7.21)$$

For PSF, according to (7.13) and (7.20), the large-signal transfer function is

$$H_{PSF} \cong \frac{1}{1 + \frac{\Delta V_p \sqrt{A_{bulkp}}}{2} \left\{ \lambda_{2pQ}^2 E_{sat} L_{2peff} + \lambda_{1pQ}^2 E_{sat} L_{1peff} + \frac{j\omega C_{Leqp}}{I_{p0}} \right\}} \quad (7.22)$$

For CCSF, from (7.17) and (7.20), the large-signal transfer function is obtained as

$$H_{CCSF} \cong \frac{1}{1 + \frac{K1_n}{2(2\Phi_{fn} + V_{OQ})^{1/2}} + \frac{K1_p}{2[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS-Q})]^{1/2}} + \frac{\Delta V_n}{2A_{bulkn-Q}^{1/2}} \left(\frac{-K1_n A_{0n}}{4(2\Phi_{fn} + V_{OQ})^{3/2}} + A_{bulkn-Q} \frac{j\omega C_{Leqn}}{I_n} \right) + \frac{\Delta V_p}{2A_{bulkp-Q}^{1/2}} \left(\frac{-K1_p A_{0p}}{4[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS-Q})]^{3/2}} + A_{bulkp-Q} \frac{j\omega C_{Leqp}}{I_p} \right)} \quad (7.23)$$

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From (7.21), the voltage gain of the NSF is smaller than 1, and the gain error is a complex number. The real portion is mainly contributed by the body effect term

$\frac{K1_n}{2(2\Phi_{fn} + V_{OQ})^{1/2}}$ that is independent of frequency, whereas the imaginary portion is

caused by the frequency-dependent term $\frac{\Delta V_n A_{bulkn-Q}^{1/2}}{2} \frac{j\omega C_{Leqn}}{I_n}$ that is significant at

high frequency. Thus, the large-signal gain exhibits dc gain error at low frequency and it rolls off at high frequency. Due to the minute channel length modulation terms in (7.22), the low-frequency gain of PSF is much closer to 1 than that of NSF in (7.21). As in the NSF, the channel length modulation term is responsible for the real portion whilst the frequency-dependent term is responsible for the imaginary portion. When operation frequency is increased to high levels, the frequency-dependent term in the imaginary portion becomes significant. From (7.23), the low frequency gain error of CCSF is larger than that of the NSF in (7.21) and PSF in (7.22) due to the summation of the body effects in NSF and PSF. This can be regarded as a disadvantage of the scheme. At high frequencies, the gain decreases because the frequency-dependent effect becomes apparent. The gain of the various source followers will be verified by the simulation results in Chapter 9.

If the gain of source follower is less than 1, calibration is needed in the testing. First, the gain error can be detected from the relationship between input and output through a reference source follower being built in the chip because it tracks with other source followers within the same chip. Then, the input signal can be processed to compensate the gain error.

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7.2.3.3 Power Supply Rejection Ratio (PSRR)

Consider positive PSRR in single supply operation, the PSRR of PSF and NSF is better than the PSRR of CCSF. It is because the bulk of the PMOS input at the first stage of CCSF is connected with VDD, which make the PSF at the first stage is sensitive to the variation of power supply. This is also regarded as one of disadvantages of the CCSF.

Although the CCSF seems to exhibit worst PSRR among the three source follower schemes, in differential operation, the PSRR of CCSF will be improved significantly due to identically-designed structure despite of bulk-to-supply configuration.

7.3 Input Interface Design

The accuracy for ADC depends directly on maintaining the precision of input signal being applied to the core ADC. In order to attain the accuracy of input voltage, precision buffers with high drive ability are needed. With the increase of sampling frequency and input frequency, the requirements for external driving amplifiers become more and more strict due to parasitic capacitors and inductors associated with packaging and bonding. To relax the drawbacks, an internal buffer is designed to drive the input of core ADC.

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From the analysis of source followers, the NSF offers the most bandwidth efficiency due to the high transconductance of NMOS transistor, the CCSF offers the most significant optimized THD performance due to the compensation and the PSF provide the lowest gain error due to the bulk being tied to source of the main transistor. In the internal buffer design, the PSF circuit architecture is chosen on the basis of its predictable ac gain for a broad range of operation frequency. The internal buffer, as shown in Fig. 7.9, consists of two PSFs for pseudo-differential input signal, one replica buffer and one amplifier. V_{in+} , V_{in-} and V_{in+}' , V_{in-}' are external differential input voltage and differential input applied to ADC. V_r is the common mode voltage of differential signal V_{in+} and V_{in-} . V_{cm} is the common mode voltage of V_{in+}' and V_{in-}' . Two main PSFs are used to drive the differential input of ADC and its characteristics together with non-ideal analysis have already been discussed before. The replica buffer is just a scale down version of the main PSFs, which aims at stabilizing the common mode voltage of differential input by the feedback loop with amplifier. The output of amplifier is connected to the gate of biasing transistor so as to control the biasing currents. Any variation of output common mode voltage from V_{cm} will cause the change of the output voltage of amplifier, hence the biasing current is adjusted to stabilize the common mode voltage of differential input to V_{cm} again.

Fig. 7.9 Internal Input Buffer

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7.4 Output Interface Design

The digital output of ADC is difficult for driving the test instrument directly due to involvement of huge PAD size and power of the output interface design based on the current CMOS technology. The design of the digital output interface is therefore geared to the medium driving level such that it can interface with external buffers with powerful driving capability for further digital signal processing. Besides, the CMOS buffer or TTL buffer is difficult to deal with the digital data which have sampling rate higher than 100MHz. The speed problem encountered in TTL/CMOS buffer can be solved by ECL approach. The main advantage of ECL buffer over a CMOS/TTL buffer is its high-speed transmission, thus it is very suitable for a system which requires very fast data or signal processing. ECL logic technologies also offer a number of advantages for reducing system clock skew over the alternative CMOS and TTL technologies. In addition, the smaller signal swing benefits for the high speed design despite of degradation of noise margin, which does not produce large data-dependent current glitches on the chip power line. Since the use of positive supply in this ADC, PECL buffer, is the best choice for simplifying the circuit design. Fig. 7.10 shows the typical ECL level with 3.3V supply. The high voltage level is around 2.3V~2.4V whilst the low voltage level is around 1.5V~1.6V. The signal swing is around 0.8V, which is much smaller than the signal swing of CMOS or TTL logic

Fig. 7.10 Typical ECL Level with 3.3V power supply

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As a result, the translation between ADC digital output data in CMOS logic and ECL level in the external buffer is justified. Thus, the output levels of the digital output buffer are compatible to that of ECL logic. As illustrated in Fig. 7.11, the output stage is an open-drain PMOS device producing a current of about 8 mA. The current is drawn from an off-chip termination resistor of $100\ \Omega$, generating a voltage swing of 800 mV, a value sufficient for driving off-chip ECL buffers. The small voltage swings allow sharp edges in the output data waveforms even with the large capacitance due to the traces on the printed-circuit (PC) board. One dedicated ground pad is used for all of the output drivers to ensure that the large ground bounce does not disturb the sensitive analog sections.

Fig. 7.11 Output Stage

CHAPTER 8

ADC LAYOUT

After the architecture, circuit design and simulations, the ADC will be proceeded to layout phase. Since ADC is a mixed-signal system, there are quite a number of layout considerations. It is mainly because the accuracy of ADC would be greatly affected if the layout design is not properly addressed. In this chapter, the top-level floor plan of ADC is understood first. Different layout issues are then discussed separately in view of the whole ADC.

8.1 Floor Plan

In this ADC design, the two interleaved fine ADCs deal with the signal from coarse ADC. The digital circuit controls the analog signal processing and it processes signal after the comparators. The high-speed digital control signals in the ADC must travel through the analog sections due to the nature of mixed-signal circuit. These issues underscore the importance of careful layout to suppress various noise coupling and other non-ideal effects. Therefore, the top-level floor plan layout of the ADC must address

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issues such as: (i) routing of critical paths, (ii) power and ground isolation, (iii) noise coupling from the digital sections to the analog sections and so forth.

Fig. 8.1 Floor Plan of the ADC

During the layout process, the floor plan serves as a guide for placement, location and shape of building blocks. Fig. 8.1 shows the complete floor plan of the ADC. The coarse ADC is placed in the left top part and two interleaved fine ADCs are located in the right of the chip. The coarse pre-comparison block is just below the coarse post-comparison block, which is close to the center of the ADC. The reference resistor ladder in the center of the die is a continuous piece of polysilicon without bends or corners. Coarse ADC and fine ADCs are located on the two side of the reference ladder and share

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the same reference ladder. The internal buffer is located at the left side of the chip. In order to reduce the delay between sampled input signal by the coarse ADC and fine ADCs, the analog differential input signals, V_{in+} and V_{in-} , enter from the left side of the chip, go through the internal buffer and are routed between ADC blocks from the center of the chip. A clock generation circuit is placed at lower left part of the center so that it readily reaches the coarse and fine ADCs. To ensure proper timing, the distribution of the clock signals to the coarse ADC and to the two interleaved fine ADCs has to be symmetrical. This means that the wiring between the critical nodes must have the same resistance and the same parasitic capacitance. All signal lines are built with stacked metal wires to minimize the parasitic resistance so as to avoid limiting the settling time constant. Digital outputs leave the chip from the right sides of the chip. Three different power lines are used in this layout, one for the quiet analog section, one for the digital section, and one for the noisy analog section.

8.2 Layout Considerations

In addition to floor plan, a proper layout is essential for a well-performing circuit. The chip area can be minimized by a carefully planned layout. Device properties such as matching, noise and high-frequency performance also rely on good layout approaches. In this design, a standard $0.35\mu\text{m}$ CMOS N-well process is being used.

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8.2.1 Matching Issues

The matching of resistor ladder determines the integral linearity of the ADC. Three effects are considered to have an impact on relative accuracy: geometry (which is determined by shape), width, and length. The mismatching due to deterministic errors caused by bends, lithography, and etching are minimized by using an identical basic resistor cell for all matched resistors. In addition, better matching can be obtained by increasing width and length of a resistor basic cell, because most of the randomness stems from the perimeter due to lithography. Another matching problem stems from contacts interconnecting string resistors. The widely varying contact resistance becomes important to get a good matching in a low resistor string especially in high-resolution converters. Further, the contacts should be avoided in the current path because it can lead to contact alignment error by mask tolerance.

Fig. 8.2 Reference Resistor Ladder

According to the discussion above, the layout of resistor ladder is illustrated in Fig. 8.2. A strip of polysilicon without corner and bend are used as resistive material due to its less process variation. In order to achieve good matching, all resistors in the resistor

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ladder are built of the same basic resistor element. The width of the resistors was chosen at much larger than the minimum size. The connection of the ladder to the comparator inputs, as shown in Fig. 8.2, is done by sensor lead, which is simply taps connecting into the side of the resistor. Accurate voltage sensing across resistors requires special techniques. In order to ensure that there is no current flowing through the metal to poly contacts and that their resistance does not affect the accuracy of the ladder, these sensor lead should be as narrow as possible. Thus, the length of the resistor is determined by the distance between the leads and not by their width [102]. In addition, the body of the resistor should be extended beyond either sense lead by a distance at least equal to the resistor width and preferably by at least twice this width to ensure accurate voltage sensing. Dummy resistors were used in order to create almost identical surroundings of the resistors. To reduce the noise coupled from the substrate, the resistor ladder is put in an n-well being biased at the analog power supply, thus shielding the plate of the resistor from the substrate.

Matching is also a critical issue for many analog circuits in the ADC design such as differential pairs, current mirror, multichannel circuit and so forth. In order to reduce the offset due to the mismatching, common-centroid technique was adopted for all the input transistor of differential pairs. Fig. 8.3 shows the simplest common-centroid layout for two transistors. The idea is to decompose each transistor into two halves that are placed diagonally opposite of each other and connected in parallel. To achieve greater matching characteristic, dummy transistors were added.

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Fig. 8.3 Common Centroid Layout of Differential Transistor Pair

Although no accurate gain is needed in each gain stage, the gain matching characteristic between differential circuits is needed. Since the stage gain is determined by the capacitor ratio, the matching in the capacitor is very important. For better matching property, the capacitors are split into identical pieces. To reduce the noise coupled from the substrate, the plate of the capacitor is shielded from the substrate by an n-well. To minimize the cross talk among different comparators, capacitors in different comparators are put in separate n-well. There are a lot of comparators used in this ADC, and so the matching issue among different comparator channels must be considered. It is impossible to use common-centroid technique among so many comparators. For this reason, each comparator was laid out individually and arranged in the same environment.

In addition, the matching of biasing circuits for different comparators is needed. The distribution of biasing currents and voltages across ADC entails a number of important issues since it is a large chip. As shown in Fig. 8.4, the distribution of electrical

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biasing parameter is preferred with current domain rather than voltage domain. The reference current is routed to each comparator and performed with the current mirror operation locally. The interconnect resistance in series with the current source does not affect the current, which is an advantage over voltage distribution where the voltage drop on these resistance will greatly deviate from the reference source. Thus the circuit sensitivity arising from mismatch of biasing circuits is minimized.

Fig. 8.4 Distribution of Current to Reduce the Effect for Interconnect Resistance

8.2.2 High Speed Issues

The speed is limited by the RC constant. The parasitic capacitance consists of the parasitic associated with the active part of the transistor and the layout-dependent parasitic capacitances between the transistor terminals. Fig. 8.5 shows the parasitic capacitance of long interconnects, which introduce delay and dispersion.

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Fig. 8.5 Delay and Dispersion of a Signal

To minimize the parasitic capacitance from drain and source to bulk, the area of the drain and source diffusions should be minimized, which is also beneficial for the reducing the total area. To minimize the parasitic capacitance due to connection among different components, the components should be arranged as compact as possible. Besides, the metal 3 and metal 4 has the smaller parasitic capacitance since it is far away from the substrate when compared with metal 1 and 2. It is especially useful for high-speed signals with long routing path.

In addition to parasitic capacitance, the parasitic resistance exists in series with the gate, drain and source. To minimize the gate resistance, the gate connection should be as short as possible and the metal should be used instead of poly. Simultaneously, whenever possible, contacts should be added to reduce the contact resistance. The long signal lines should be built with stacked metal wires to minimize the parasitic resistance. Finally, a transistor should be surrounded as closely as possible by a metal ring with substrate contacts to get a low enough bulk resistance. This helps reduction in the disturbances or injection noise from other parts of the circuits.

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8.2.3 Low Noise Issues

Since the ADC contains both analog and digital parts, special care must be taken to avoid the noisy digital section from affecting the performance of the analog section. The digital noise can be coupled into circuit from several aspects such as digital circuit, power supply, substrate, and so on. The noise floor of the ADC may be greatly degraded if the layout efforts have not been addressed properly. Therefore, the noise isolation is considered as follows.

Fig. 8.6 An Example Guard Ring for Sensitive Circuits

In order to prevent the digital circuitry from injection noise to the sensitive analog circuitry, the analog part is keeping as far as possible from the digital circuitry. Moreover, the guard ring is used to shield the digital and analog circuitry from its environment separately as shown in Fig. 8.6. The analog and digital layouts were isolated through the use of guard rings and sufficient grounding. This is necessary to reduce noise

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through substrate coupling. Fig. 8.7 shows the cross section using substrate contacts (P+) and n-well to reduce this effect.

Fig. 8.7 Cross Section of Guard Rings to Reduce Substrate Noise Coupling from Digital Circuits to Analog Circuits

To prevent the digital circuitry from injecting noise to analog circuit through power supply, three supply rails are separated, which are named V_{DDD} , $GNDD$, $VDDA$, $GNDA$, $VCCA$ and $GNDC$ respectively. V_{DDD} , $GNDD$ and $VDDA$, $GNDA$ are for digital circuit and analog circuit separately. The additional power supply, $VCCA$ and $GNDC$, provides power for internal buffer circuit. All the individual power supply line will be connected to the pads in a star configuration as illustrated in Fig. 8.8. The width of power lines were determined by the maximum current and the maximum voltage drop that can be allowed. Finally, if the extra chip space is available, on-chip decoupling capacitors can be added to reduce ripple of the supply voltage, which is vital in embedded mixed-signal applications.

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Fig. 8.8 Power Supply Distribution

It is important to note that analog input line cannot cross digital line. If this has to happen, make sure they cross each other at right angles. Besides, an empty stripe can be provided between the cross section so that the digital control signals can run through analog signal path without interfering it and without losing the speed due to the increasing of the parasitic capacitance. The noise can also be coupled from the lateral metal path. The usual means of reducing this problem is to place the lines carrying analog signals reasonably far away from the line carrying digital signals. Moreover, a dummy line placed between the analog and digital lines biased at a “quiet” voltage achieves a horizontal shielding as shown in Fig. 8.9.

Fig. 8.9 Shielding the Analog and Digital Signal by a Ground Line

Fig. 8.10 Shielding a Sensitive Line by the Lower and Upper Layers

Another shielding technique is shown in Fig. 8.10. The sensitive line is surrounded by a grounded shield consisting of a higher and a lower metal layer and hence fully isolated from external line. In order to reduce the mutual coupling between different digital output due to parasitic capacitance and inductance, ground is inserted between every digital output pad and pin as illustrated in Fig. 8.11.

Fig. 8.11 Shielding the Output by Ground

In order to minimize the effect of substrate noise, the following methods are applied. First, differential operation is used throughout the circuit, making the analog section less sensitive to common mode noise. Second, digital signals and clocks are

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distributed in complementary form, thereby reducing the net amount of the coupled noise. Third, each of the analog blocks, such as gain stage, op amp and biasing circuit, is surrounded by a metal ring with plenty of bulk contacts to reduce the bulk noise effect. Since an n-well process was used, the digital and analog PMOS transistors were naturally isolated by separate wells. The NMOS transistors, however, interact via common, low-resistance p substrate if possible.

In summary, the high-level floor plan, system and circuit layouts are another complementary critical factors for successful ADC design. It should be planned very carefully so as to avoid non-ideal environmental attributes and imperfect fabrication that cause significant degradation of high-performance ADC.

CHAPTER 9

RESULTS AND DISCUSSIONS

In this chapter, the simulation results of preamplifier, buffer design and sample insensitive interleaved design are discussed. The experimental results obtained from the fabricated prototype in a 0.35 μm CMOS technology are described.

9.1 Simulation Result of Preamplifier

9.1.1 Speed

Three multistage topologies being designed with identical power consumption, on the basis of Fig. 4.2, Fig. 4.3 and Fig. 4.6, were simulated using Level 49 BSIM3 models from the 0.35 μm CMOS process. All the gain stage amplifiers in the three designs are implemented using a common source amplifier [39]. Fig. 9.1 shows the simulated results of different step responses at the respective differential output of each gain stage in the three multistage differential preamplifiers.

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(a) First Stage Differential Output

(b) Second Stage Differential Output

(c) Third Stage Differential Output

Fig. 9.1 Step Responses of the Three Preamplifiers

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As can be seen from the output waveforms, not only does the proposed preamplifier exhibit higher slew rate, it also achieves faster settling characteristic due to the benefit of small capacitive load for reducing amplifier time constant. Compared with the settling time among the structures I, II and III at 1% accuracy, the settling times are obtained as 7ns, 3ns and 2.5ns, respectively. It has confirmed that the proposed preamplifier would offer an alternative structure for high-speed comparator design.

9.1.2 Nonlinearity

In nonlinearity aspect, FFT analysis is used to indicate the linearity. The frequencies chosen for the sampling clock and the input signal are 150 MHz and 10 MHz, respectively. Fig. 9.2 shows the simulation and calculation results of the harmonic distortions in the output of preamplifier, with -10% to 10% mismatch in channel area of switch (α_{WL}) and capacitor ratio ($\alpha_C - \alpha_{C_f}$). As observed in Fig. 9.2(a), HD2 is increased with the increase of mismatching factor but it displays at about -90dB even at 10% mismatch, indicating that the mismatch in the channel area of switch does not degrade HD2 significantly. However, HD2 is relatively more sensitive in terms of the mismatch in capacitor ratios as depicted in Fig. 9.2(b). It can be observed that HD2 increases with increasing mismatching factor of capacitor ratio but its value tends to be comparable with HD3 when $\alpha_C - \alpha_{C_f} > 5\%$. Regarding HD3 components in the both mismatch cases as shown in Fig. 9.2(a) and Fig. 9.2(b), they exhibit quite a flat response, almost independent of mismatching factors. The hand-calculated HD2 and HD3 in Fig. 9.2(a) are combined to form the approximate THD as

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a function of the mismatch factor, α_{WL} . The hand-calculated THD is close to the simulated THD, which is based on the HD2 and HD3 spectral components obtained in Fast Fourier Transform. When taken into account of the spectral harmonic components from HD2 to HD7 for representing the simulated THD, the approximated THD values, based on hand-calculated HD2 and HD3, are close when $\alpha_{WL} < \pm 5\%$. They deviate further at high mismatching factor as deduced from the simulated THD curve, which appears in a V-shaped form. This confirms that higher-order harmonics are actually function of the channel area mismatch. These high-order harmonics are not modeled in the current analysis. Regarding the THD performance against the variation of the mismatch in capacitor ratio, $\alpha_C - \alpha_{C_f}$, both the hand-calculated HD2 and HD3 components in Fig. 9.2(b) are combined to form the approximated THD in Fig. 9.2(d). It is observed that the second-order predicted THD values are close to those of simulated THD results, on the basis of either 2-harmonic or 6-harmonic computation from the spectral components. This is translated to the implication that higher-order harmonics are not really a function of the capacitor ratio mismatch.

Table 9.1 shows the simulation result of the total harmonic distortion (THD) of preamplifier with and without mismatching cases. For matched case, the THD attains the value of -65 dB. For the worst case mismatch of 10% in switch area and 10% in capacitor ratio, the THD drops to -50 dB. Therefore, it confirms that the mismatch among differential circuit components has made significant impact on the linearity of multistage preamplifier. It should be minimized through careful layout plan.

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Fig. 9.2 Comparison of Simulated and Hand-Calculated HD and THD in Preamplifier under Mismatch

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Table 9.1 Comparison of THD in Preamplifier under Different Mismatch Factors

Linearity Parameter	Without Mismatch	With $\alpha_{WL} : 5\%$ Mismatch $\alpha_C - \alpha_{C_f} : 5\%$	With $\alpha_{WL} : 10\%$ Mismatch $\alpha_C - \alpha_{C_f} : 10\%$
THD (dB)	-65 dB	-58.4 dB	-50 dB

9.2 Simulation Result of Sample Insensitive Interleaved Design

As discussed in Chapter 5, the sample time error in the interleaved ADC will affect the linearity of the whole ADC very much. From (5.1), the larger the Δt , the more the nonlinearity is. For an input frequency of 10 MHz, Fig. 9.3(a) shows the output spectrum of ADC with sample time error. It can be seen that there are some unexpected tones in the spectrum, thus decreasing the linearity of ADC. Fig. 9.3(b) shows the same output spectrum of ADC with introducing the series switch in Fig. 5.7(d). Better linearity is achieved due to the minimization of sample time error by a synchronized series switch.

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(a)

(b)

Fig. 9.3 The Output Spectrum of ADC
(a) with sample-error (b) with sample-error correction

9.3 Simulation Result of Source Followers

In order to verify the second-order analytical result and compare the relative linearity performance, the THD of NSF, PSF and CCSF were simulated using realistic Level 49 BSIM3 models from 0.35 μ m CMOS process technology. With a sinusoid input signal, the harmonic distortion can be found from Fourier analysis. The process

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and design parameters, used in hand calculations to predict the second harmonic distortion results, are shown in Appendix E. As the second-order distortion component is much larger than the third and fourth harmonics under large signal conditions, the second harmonic is very close to the THD. The THD is therefore used to denote the linearity of the three source followers in simulation whilst maintaining reasonable accuracy.

9.3.1 The Performance of Source Followers

For low-frequency verification, the input frequency was chosen such that the frequency-dependent distortion components are not of any significant impact and the harmonic distortion is governed by the frequency-independent nonlinearities. According to the prior analysis, these frequency-independent nonlinear terms are function of quiescent operation points. Fig. 9.4 shows the variation of the THD of NSF, PSF and CCSF against different V_{OQ} at 10 MHz. In relation to the NSF, the THD is

decreased because the major bulk modulated component $\frac{-K1_n}{16(2\Phi_{fn} + V_{OQ})^{3/2}}$ decreases

with increasing V_{OQ} as revealed in (7.11). For the PSF, the distortion characteristic appears as a V-shaped function against the change of V_{OQ} . This observation is consistent with the observation in (7.14) that it results from the mutual subtraction of the bias-dependent channel length modulation terms (λ_{1pQ} , λ_{2pQ}) from the input transistor and biasing transistor, with the degree of subtraction controlled by V_{OQ} . For the CCSF, the minimum THD can also be observed at a particular output quiescent

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voltage bias point because of the involvement of a PSF that has a similar V-shaped function,. The optimum distortion point arises from the cancellation between PMOS and NMOS based body effect terms, with dominant components denoted as

$$\frac{-K1_n}{16(2\Phi_{fn} + V_{oQ})^{3/2}} \text{ and } \frac{K1_p}{16[2\Phi_{fp} + (V_{DD} - V_{oQ} - V_{GS_Q})]^{3/2}} \text{ in (7.18). This allows the}$$

CCSF to get low distortion at low frequencies.

Fig. 9.4 THD versus V_{oQ} at 1 V_{pp} Input, 1 pF Load and 10 MHz Input Frequency

For high-frequency verification, all the source followers should start with optimum quiescent bias prior to investigating the high-frequency distortion characteristics. Because there is no formal optimal bias point in NSF as described above, the V_{oQ} is preferably set at half the supply voltage. The V_{oQ} of the PSF and CCSF are based on the optimized values according to Fig. 9.4. The simulated high-frequency THD characteristics of PSF, NSF and CCSF together with the calculated results are illustrated in Fig. 9.5. For PSF, THD exhibits the highest linearity at low frequency because of the elimination of the body effect and because there is negligible contribution from the high-frequency nonlinear factor. However, the linearity degrades

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progressively with increasing the input frequency. This confirms that the dominant frequency-dependent term $(\frac{\omega C_{Leqp}}{I_{p0}})^2$ overrides the minute channel length modulation

terms in (7.14). For NSF, although it displays the relative higher nonlinearity at low frequency due to a strong body effect, the nonlinear effect is progressively compensated with the increase in frequency. The view that the frequency-dependent

distortion component $\frac{\Delta V_n}{16} A_{bulkn-Q}^{1/2} \left(\frac{\omega C_{Leqn}}{I_n} \right)^2$ compensates the dominate body effect

distortion component $\frac{-K1_n}{16(2\Phi_{fn} + V_{OQ})^{3/2}}$ in (7.11) is validated. As a consequence, the

NSF displays better THD result than that of PSF at a specific high frequency range. For CCSF, the THD is lower than that of the NSF because the n-channel body effect term is compensated by the p-channel body effect term via the optimized V_{OQ} in Fig. 9.4. Due

to the potentially incomplete cancellation between the cross-product terms as observed in (7.18), the residual values that contribute to the THD will be higher than that of the PSF. This explains why the THD value lies between NSF and PSF, starting from a low frequency range. For high-frequency distortion compensation based on the design

values of $\Delta V_n = 1.4$ V, $A_{bulkn-Q} = 1.48$, $C_{Leqn} = 1.05$ pF, $I_n = 1$ mA, $\Delta V_p = 0.19$ V, $A_{bulkp-Q} = 1.2$, $C_{Leqp} = 0.092$ pF and $I_n = 0.1$ mA in the CCSF, it turns out that

$$\frac{\Delta V_n A_{bulkn-Q}^{1/2} \left(\frac{\omega C_{Leqn}}{I_n} \right)^2}{16} \cong \frac{\Delta V_p A_{bulkp-Q}^{1/2} \left(\frac{\omega C_{Leqp}}{I_p} \right)^2}{16}, \text{ and so the THD stays constant}$$

from low frequency to high frequency.

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Fig. 9.5 THD Characteristic of CCSF at High Frequency and Its THD Comparison with NSF and PSF based on 1 V_{pp} Input, 1 pF Load and Optimal V_{oQ} among 3 schemes

For verification of the large-signal transfer functions, Fig. 9.6 compares the simulated frequency responses of the various source followers with the hand-calculated second-order analytical results. As in the simulated results, all the predicted curves show a rolling off characteristic at high frequencies but they also exhibit different low-frequency gain values. The low-frequency gain of PSF is much closer to the ideal case of unity. This is since the gain offset comes mainly from the channel length modulation terms which are relatively smaller than the nonlinear body effect terms in the NSF. The CCSF has displayed the lowest gain because of the summed body effects from both the NSF and PSF in the cascaded structure.

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Fig. 9.6 Large-Signal Transfer Function of Various Source Followers at 1 V_{pp} Input and 1 pF Load

The comparison of NSF, PSF and CCSF is summarized in Table 9.2. All the schemes permit the THD value to be less than 60 dB but with different frequency ranges. The CCSF offers the most significant optimized THD performance because it allows the circuit to operate with sustained low distortion in a wide frequency range. Nevertheless, the NSF offers the most bandwidth efficiency because the p-channel source followers limit the operation frequencies of both the PSF and CCSF. The PSF offers the best precision among others. The discrepancies between the simulated and calculated results are mainly due to the use of simplified large-signal model (Fig. 7.2), simplified HSPICE BSIM3 model equations and the assumptions made for simplifying the derivation.

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Table 9.2 Performance Comparison of NSF, PSF and CCSF

Condition: $V_{dd} = 3V$, Load = 1 pF and 1 V _{pp} input	NSF	PSF	CCSF
Frequency range for optimized THD < - 60dB at optimal V_{OQ}	Sim: 75–100MHz Cal: 90–110MHz	Sim: 0–35MHz Cal: 0–45MHz	Sim: 0–140MHz Cal: 0–160MHz
Low-frequency gain	Sim: 0.848 Cal: 0.863	Sim: 0.954 Cal: 0.987	Sim: 0.705 Cal: 0.721
Large-signal -3dB bandwidth	Sim: 1500 MHz Cal: 1800 MHz	Sim: 870 MHz Cal: 1170 MHz	Sim: 860 MHz Cal: 1100 MHz
THD for frequency range in 10M~100M	Sim: -54~-61 dB Cal: -51~-62 dB	Sim:-44~-74 dB Cal:-47~-77 dB	Sim: -65~-67 dB Cal: -68~-71 dB
Power consumption	3 mW	3 mW	3.3 mW

9.3.2 Simulation Result of Internal Input Buffer

The PMOS source follower is implemented in the design of internal input buffer as shown in Fig. 7.9. Fig. 9.7 shows the simulation result of the output of buffer with 5 pF capacitive load at 1V_{pp} input. It is can be seen that the THD is around -60 dB at 75 MHz (which is the maximum input frequency) which satisfies the requirement of 10 bit resolution. In addition, the calculation result agrees very well with the simulation result.

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Fig. 9.7 THD of Internal Input Buffer

9.4 ADC Measurement Results

9.4.1 Testing Setup and PCB design

A) Testing Setup

Testing a 10-bit converter at sampling rates greater than 100 MHz entails many challenges, requiring considerable efforts in the design of the test board and the setup. The practical issues such as the parasitics of typical packages, the routing of PCB board and the distortion of source etc, must be considered. The setup for testing ADC is shown in Fig. 9.8. Complete evaluation of ADC requires the use of FFTs to fully characterize the devices AC performance.

Refer to Fig. 9.8, there are two signal generators in this testing, and they are synchronized by the 10MHz sync signal. One signal generator is used to provide the analog input whereas another one provides the clock signal. For accurate dynamic parameter measurement, the input signal source must have lower noise and lower distortion than the data converter under tested. The clock signal generator must have

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very low jitters from sample-to-sample. To further suppress the harmonic distortion components and noise from the input signal generator, high quality low-pass or band-pass filters are applied between the output of generator's output and the ADC input drive source.

Fig. 9.8 System Configuration for testing ADC

A high-speed logic analyzer can be used to capture the ADC output data, and interfaces easily to the ADC evaluation board. Thus, a logic analyzer is chosen as the buffer memory in this ADC testing. The digital output data of the ADC is collected by a logic analyzer and loaded into a personal computer for analysis subsequently. Once the ADC data is inside the PC, software such as Matlab can be used to characterize the results of both static and dynamic tests. INL and DNL are measured at low input frequencies (at a sampling rate of 150 MHz), while SNDR and SFDR are obtained for input frequencies up to the Nyquist rate.

B) Evaluation Board design

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(a) Function Diagram

(b) Prototype

Fig. 9.9 Evaluation Board

The evaluation board is used as a means for interfacing to the ADC. It is designed to allow ease of access to the ADC inputs and outputs while also providing a good layout (including all necessary references, buffer amplifiers, and decoupling). The evaluation board permits the ADC output data to be captured on a parallel output connector. A block diagram of the evaluation board is shown in Fig. 9.9 (a).

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As can be seen, a RF transformer provides a clean single-to-differential input signal conversion. The external ECL buffers are used to read out the digital data from ADC with the clock rate of 150 MHz. Also, the external ECL buffers drive the input channels of the logic analyzer with reasonable rise time, fall time and voltage swings. Besides, external analog buffers are established to drive the reference inputs of the ADC.

An evaluation or characterization board for fast data converters must incorporate high-speed PCB layout techniques. Fig. 9.9(b) shows the prototype of evaluation board. Some basic rules should be followed in order to get the real performance of ADC. First, multilayer boards with separate ground and power planes produce the highest level of signal integrity. Surface mount components are chosen to achieve minimum trace length, inductance, and capacitance. In high-speed ADC testing, special attention must be given to power supply decoupling. For example, fast slewing signals into relatively low impedance loads produce high speed transient currents at the power supply pins of op amp. The transient currents, in turn, produce corresponding voltages across any parasitic impedance which may exist in the power supply traces. These voltages, in turn, may couple to the amplifier output because of the op amp's finite power supply rejection at high frequencies.

A two-capacitor decoupling scheme is chosen to ensure a low impedance path to ground at all transient frequencies. The highest frequency transients are shunted to ground by the 0.1 μ F ceramic capacitors. They are located as close to the power supply pins as possible to minimize any series inductance and resistance. Since the devices are surface mount components, there is minimum stray inductance and resistance in the

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path to the ground plane. The lower frequency transient currents are shunted to ground by the 10 μ F tantalum capacitors.

Consider the use of a split ground plane arranged to match the physical location of analog and digital grounds on the ADC's package. The impedance of the two ground planes must be kept as low as possible. To avoid possible damage or latch up, their AC and DC voltage differences (or both) must be less than 0.3V. These grounds should be joined at a single point, so that noisy digital ground currents do not interfere with the analog ground plane. The ideal location of this connection can be determined experimentally, as the point along the gap between the two ground planes that produces optimum results. This connection can be achieved with a low value surface-mount resistor of 1 to 5 Ω , a ferrite bead, or a direct short. As an alternative (if the ground plane is sufficiently isolated from noisy digital systems such as the downstream output buffer and DSP), all ground pins can share the same ground plane.

In order to isolate the analog signal from the digital signal, these high-speed digital signal traces are routed far away from sensitive analog traces. In order to get low noise clock, the clock input should be routed away from actual analog inputs signal lines.

Keep all signal lines short and free of 90° turns. The length of line for 10 bits digital output must be matched in order to make the delay difference as small as possible. In addition, impedance matching should be considered according to the device used. The input and output signal traces are 50 Ω microstrip transmission lines.

9.4.2 Measurement Results

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Fabricated in a 0.35 μm double-poly four-metal CMOS technology, Fig. 9.10 shows the die photograph of proposed ADC, which occupies 2.7 mm^2 active area. The reference resistor ladder is a continuous piece of polysilicon without bends or corners in the center of the die. The coarse ADC and fine ADCs are on the two side of the reference ladder and share the same reference ladder. The chip dissipates 178 mW at a 3V single supply.

Fig. 9.10 Microphotograph of the Proposed High-Speed Subranging ADC

Fig. 9.11 presents the measured differential nonlinearity (DNL) and integral nonlinearity (INL) at a sampling rate of 150 MS/s, which is obtained from code density tests. The maximum DNL is less than ± 0.5 LSB, and the maximum INL is ± 0.9 LSB. The dynamic performance of ADC was measured in frequency domain. Fig. 9.12

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presents a typical measured output spectrum for a 10 MHz input frequency with 150 MS/s. The 10 MHz fundamental component is evident along with the second and third harmonics, exhibiting 52 dB signal-to-distortion ratio. For even harmonic, the mismatch in the differential circuit lead to imperfect cancellation of second harmonic distortion. For the other non-harmonic distortion, even there is no mismatch in the interleaved ADC, there are still those harmonic due to the nonlinearity.

Fig. 9.11 Measured Results of DNL and INL

Fig. 9.12 Spectrum of FFT on the Measured Signal

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The SFDR and SNDR as a function of input frequency are plotted in Fig. 9.13. The solid line represents the simulated result whereas the dotted curve denotes the measured result. The measured SFDR and SNDR exhibit 57 dB and 52 dB respectively at 10MHz input signal frequency. Both the SFDR and SNDR decrease with the increase of input frequency. When the input frequency reaches 70 MHz, the SFDR and SNDR decrease to 46 dB and 40 dB, respectively. The simulated SFDR and SNDR follow the similar trend of the measured SFDR and SNDR respectively. The deviation of simulated result and measured result is due to the substrate noise in the real chip.

(a) SFDR

(b) SNDR

Fig. 9.13 SFDR and SNDR at Different Input Frequencies

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(a) SFDR

(b) SNDR

Fig. 9.14 SFDR and SNDR with the Variation of Power Supply and Temperature

Fig. 9.14 shows the simulation result of SFDR and SNDR, with the variation of power supply and temperature. It can be seen that the SFDR and SNDR decrease with the increase of input frequency. The SFDR and SNDR improve for higher supply and lower temperature but they degrade at lower supply and higher temperature. Table 9.3 summarizes the overall performance of ADC.

Table 9.3 Performance Summary of the Measured Results

Technology	0.35μm CMOS
Supply voltage	3 V
Sampling Rate	150 MS/s
Resolution	10 bits
DNL	±0.5 LSB
INL	±0.9 LSB
THD at Fin=10MHz	-55 dB
SNDR at Fin=10MHz	52 dB
SFDR at Fin=10MHz	57 dB
Input Range	1 V _{pp}
Reference Range	1 V _{pp}
Core ADC Power	178 mW
Active Area	2.7 mm ²

9.4.2 Comparison with State-of-the-Art ADCs

Table 9.4 shows the comparison between this work and state-of-the-art ADC with 8~10 bits resolution and sampling rate higher than 100 MHz. The figure of merit (FOM) is calculated from $FOM = \frac{2^B f_s}{Pf_i}$ as discussed in Chapter2. It can be seen that the FOM of this work is 32.7, which is the highest among subranging ADCs. Besides, its FOM is higher than most of the ADCs and close to the 10 bit 200 MS/s ADC [38]. The performance comparison between this work and the best of different architectures are shown in Table 9.5. The Folding ADC [Yoon-2000] and subranging ADC [Taft 2001] have lower speed, lower resolution and lower FOM when compared with this work. Although the pipelined ADC [Sumanen 2001] has higher sampling rate and FOM

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of 36, its THD is 48 dB when input frequency is 10 MHz due to the four channels interleaving, hence limiting the SNDR. Compared with 52 dB SNDR at 10 MHz input frequency in this work, the proposed ADC has better trade off among speed, resolution and power consumption.

Table 9.4 Performance Comparison of High-Speed ADC

Reference	Conversion rate	Resolution	Power-Supply	Power-Consumption	CMOS Process	Architecture	FOM
[27]-Kim-2001	200 MS/s	8b	3 V	210 mW	0.35 μm	Pipelined	9.03
[20]-Nairn2000	100 MS/s	10b	3 V	310 mW	0.35 μm	Pipeline	12.2
[31]-Yoo 2004	120 MS/s	10b	2.5 V	208 mW	0.25 μm	Pipeline	15.15
[32]-Moon 2004	100 MS/s	10b	1.8 V	67 mW	0.18 μm	Pipeline	25.5
[38]-Sumanen 2001	200 MS/s	10b	3 V	280 mW	0.5 μm	Parallel-Pipeline	36
[35]-Yoon-2000	125 MS/s	8b	3.3 V	110 mW	0.35 μm	Folding	10.77
[39]-Taft2001	100 MS/s	8b	2.2 V	75 mW	0.4 μm	Subranging	13.1
[40]-Wang2000	150 MS/s	8b	3.3 V	395 mW	0.6 μm	Subranging	6.07
This Work	150 MS/s	10b	3.0 V	178 mW	0.35 μm	Subranging	32.7

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Table 9.5 Comparision of Different ADC Architectures Having Best performance

	[35]-Yoon-2000	[38]-Sumanen 2001	[39]-Taft2001	This Work
Architecture	Folding	Parallel-Pipelined	Subranging	Subranging
Sampling Rate	125 MS/s	200 MS/s	100 MS/s	150 MS/s
Resolution	8 b	10 b	8 b	10 b
CMOS Technology	0.35µm	0.5µm	0.4µm	0.35µm
Supply voltage	3.3 V	3 V	2.2 V	3 V
DNL	0.7/-0.5 LSB	±0.8 LSB	0.4/-0.43 LSB	±0.5 LSB
INL	1.5/-1.2 LSB	±0.9 LSB	0.41/-0.6 LSB	±0.9 LSB
THD		-48 dB at fin=10MHz	51.1 dB at fin=10MHz	-55 dB at fin=10MHz
SNDR	41 dB at fin=10MHz			52 dB at fin=10MHz
SNR			47.4 dB at fin=10MHz	53.5 dB at fin=10MHz
Core ADC Power	110 mW	280 mW	75.2 mW	178 mW
Number of Interleaving Channels	No Interleaving	4 Channels Interleaving	2 Channels Interleaving	1.5 Channels Interleaving
Active Area	0.8 mm ²	7.4 mm ²	0.9 mm ²	2.7 mm ²
FOM	10.77	36	13.1	32.7

In summary, although most of ADCs in Table 9.4 are implemented in pipelined architecture, the proposed subranging ADC is proven as a promising architecture for the design of high performance ADC.

CHAPTER 10

CONCLUSIONS AND RECOMMENDATIONS

This dissertation presents the design work and experimental results of a high-speed pipelined subranging ADC with a standard sub-micron CMOS process. The concluding remarks are given. Finally, the future research work is discussed for further improvement of the ADC.

10.1 Conclusions

In this thesis, the architectures to implement high-speed CMOS ADCs have been studied. They are flash, pipelined, folding and subranging ADCs. Their advantages and disadvantages are discussed. By comparing these ADC architectures, the subranging architecture is chosen for reason of optimum performance parameters for high-speed ADC design. The structure limitations of different subranging ADCs are then critically reviewed. In order to avoid the drawbacks, a new subranging ADC dedicated for high-speed low-power application is proposed.

In proposed system design, an internal pipelined scheme incorporating with the double sampling and interleaving techniques allows the ADC sample input signal on consecutive clock without adding a sample-and-hold (S/H) circuit, thus maximizing the

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throughput with elimination of idle time. This improves from the prior-art subranging ADC architectures which usually suffer from an extra idle time.

In proposed circuit design, a new multistage preamplifier for high-speed comparator design is presented. It is based on the use of a new sliding feedback capacitor technique on a multistage preamplifier so as to increase the speed of comparator without compromising the accuracy. Except with the slightly increase in complexity of timing, the proposed preamplifier can attain good resolution at high-speed operation whilst offering a rail-to-rail input common mode range and maintaining identical power consumption with the prior-art multistage preamplifiers. This gives significant benefit for low-power high-speed circuit implementation.

The detail implementation for achieving fast and precise comparison block is presented. Several circuit techniques are applied jointly: (i) Distributive sampling is used to eliminate the need of sample-and-hold circuit, (ii) Auto-zero is used to suppress the amplifier offset, (iii) Capacitive interpolations in different circuit topologies are used to reduce the input capacitance, the number of the amplifiers to achieve high resolution as well as low power consumption ultimately without jeopardizing the speed issue, (iv) Double sampling technique is implemented at the front end of fine ADCs and (v) A synchronized switch is introduced to minimize the sample-time mismatches in the interleaved architecture.

In circuit analysis perspective, the second-order analysis has shown that the dominant nonlinear effect in the proposed preamplifier are signal-dependent charge injection with mismatch of the switch area, nonlinearity of closed-loop gain factors and

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mismatch of closed-loop gain factors in the pseudo-differential structure, which dictate the ADC performance. Comparative simulations have validated the proposed structure.

In addition to the core ADC, the input and output interface must be carefully designed in order to solve the problems caused by signal integrity issues, parasitics due to packaging and PCB, interface logic levels and driving issues with respect to the external interfaces. The investigation of harmonic distortion of different source followers (NSF, PSF and CCSF) for internal input buffer design is thoroughly analyzed using a simplified large-signal model in conjunction with Level 49 BSIM3 model equations and assumptions. Based on the analysis and simulation results, the PSF is identified as the most suitable input buffer for high-speed ADC testing on the basis of its precision and distortion level.

Since the ADC is a mixed-signal system, there are many issues to be considered prior to the layout. The floor plan of whole ADC together with careful layout considerations aims at maintaining the good performance of the proposed subranging ADC. Finally, the simulation results of preamplifier and input buffer have correlated with the analytical results. Fabricated in a 0.35 μm CMOS process technology, the ADC was measured successfully.

10.2 Recommendations for Future Research

With the technology scaling in CMOS fabrication, the process technologies of ADCs will be scaled down to provide the interface to the digital signal processors. This turns out that the supply voltage will be decreased to avoid that the electric field in the device gets too high, which cause reliability problem. The reduced power supply voltage increases the challenging issues for ADC design. This will lead to further architectural modification plus special circuit techniques to alleviate the problems in the context of the fine process technologies.

Technology scaling benefits for increasing speed, density and functionality in mixed-signal systems. Hence, it is possible for the ADC to implement even more complex digital algorithms such as digitally self-calibrated pipelined ADCs [103]. Similar types of algorithms can also be investigated for mismatch calibration or nonlinearity compensation so that they permit more robust analog structures for improving performance ultimately.

At low-voltage circuit-level design, it is difficult to design high-speed high-swing opamp as well as to provide sufficient bias margin for the MOS switches in switched-capacitor circuits. Current solutions include multistage amplifier architectures and bootstrapped switch techniques, but at a cost of increased complexity, speed tradeoff and reliability issue of thin oxide transistor. This leads to the research with the focus on improving the bandwidth of multistage amplifier through the use of cost-effective frequency compensation technique as an example and devising new

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bootstrapped switch structure with economic implementation as well as addressing the reliability issues.

Interleaving is a very effective method to increase the speed of ADC. In future, it is still a very important technique and the speed of ADC can be greatly improved by more parallelism. Unfortunately any mismatch, such as offset mismatch, gain mismatch and sample time mismatch, among the time interleaved channels will give rise to the distortion. For high-frequency signal, the most difficult mismatch error to be encountered is the sample time mismatch between the clock signals to the S/H circuit. Although many calibration techniques have been reported to reduce these mismatch among time interleaved ADC at the cost of speed and complexity, they may not be so effective when the channel number is increased. Therefore, more research works need to be done on increased parallelism plus calibration in order to push the ADC to another level of high speed and high resolution.

Author's Publications

Author's Publications

1. X. P. Fan and P. K. Chan, "A 150MS/s 10-bit CMOS Pipelined Subranging ADC," submitted to review under *IEEE Trans. Journal*.
2. X. P. Fan and P. K. Chan, "Analysis and Design of Low-Distortion CMOS Source Followers," *IEEE Trans. on Circuits & Systems, Part I*, vol. 52, no. 8, pp. 1489-1501, Aug. 2005.
3. X. P. Fan and P. K. Chan, "A CMOS high-speed multistage preamplifier for comparator design," *Proceedings of IEEE ISCAS 2004*, vol. 1, pp. 545-548, May 2004.
4. X. P. Fan and P. K. Chan, "A CMOS duty cycle corrector for high-speed phase-locked loop," *the 10th International Symposium on Integrated Circuits, Devices and Systems*, Sept. 2004.
5. X. P. Fan, P. K. Chan and L. Siek, "A highly Linear switch for high speed switched-capacitor circuits", *IEEJ International Analog VLSI Workshop*, pp. 1-4, Sept. 2002.

Bibliography

Bibliography

Bibliography

- [1] D. Dalton, G. Spalding, H. Reyhani, T. Murphy, K. Deevy, M. Walsh, and P. Griffin, "A 200-MSPS 6-Bit Flash ADC in 0.6 μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 45, pp. 1433-1444, Nov. 1998.
- [2] I. Mehr and D. Dalton, "A 500-MSample/s 6-Bit Nyquist-Rate ADC for Disk Drive Read-Channel Application," *IEEE J. Solid-State Circuits*, vol. 34, pp. 912-920, July 1999.
- [3] H. Clemens, "Nyquist Rate A/D Converters—A General Overview", *workshop on A/D Converter for telecommunication*, Oct 2001
- [4] M. Steyaert, K. Uyttenhove, "Speed-Power-Accuracy Trade-off In high-speed Analog-to-digital converters: Now and in the future", *Workshop on Advances in Analog Circuit Design*, April 2000
- [5] Plassche, R. J. Van de, *Analog Circuit Design: high speed analog to digital converters, mixed signal design, PLL's and synthesizers*, Kluwer Academic Publisher, 2000.
- [6] S. Tsukamoto, I. Dedic, T. Endo, K. Kikuta, K. Goto, and O. Kobayashi, "A CMOS 6-b 200-MSample/s, 3V Supply A/D Converter for a PRML Read Channel," *IEEE J. Solid-State Circuits*, vol. 41, pp. 1831-1836, Nov. 1996.
- [7] S. Tsukamoto, W. G. Schofield, T. Endo, "A CMOS 6-b 400-MSample/s ADC with Error Correction," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1939-1947, Dec. 1998.
- [8] K. Yoon, S. Park and W. Kim, "A 6b 500MSample/s CMOS Flash ADC with a background Interpolated Auto-Zeroing Technique," *Dig. Tech. Papers International Solid-State Circuits Conference*, pp. 326–327, Feb. 1999.

Bibliography

- [9] Y. Tamba and K. Yamakido, "A CMOS 6b 500MSample/s ADC for a Hard Disk Drive Read Channel," *Dig. Tech. Papers International Solid-State Circuits Conference*, pp. 324–325, Feb. 1999.
- [10] K. Sushihara and H. Kimura, Y. Okamoto, K. Nishimura and A. Matsuzawa, "A 6b 800MSample/s CMOS A/D Converter," *Dig. Tech. Papers International Solid-State Circuits Conference*, pp. 428–429, Feb. 2000.
- [11] K. Uyttenhove, A. Marques and M. Steyaert, "A 6-bit 1GHz Acquisition Speed CMOS Flash ADC with Digital Error Correction," *Proceeding of Custom Integrated Circuits Conference*, pp. 249–252, May 2000.
- [12] J. Yoo, K. Choi and A. Tangel, "A 1-GSPS CMOS flash A/D converter for system-on-chip applications," *Proceeding of IEEE Computer Society Workshop on VLSI*, pp. 135-139, 19–20, April. 2001.
- [13] K. Nagaraj; D.A. Martin, , M. Wolfe, R. Chattopadhyay, S. Pavan,; J. Cancio, and T.R. Viswanathan,, "A 700M Sample/s 6 b read channel A/D converter with 7 b servo mode," *Dig. Tech. Papers International Solid-State Circuits Conference*, pp. 426–427, 476, Feb. 2000.
- [14] M. Choi and A. A. Abidi, "A 6b 1.3GSample/s A/D Converter in 0.35 μ m CMOS," in *Dig. Tech. Papers International Solid-State Circuits Conference*, pp. 126–127, Feb. 2001.
- [15] G. Geelen, "A 6b 1.1GSample/s CMOS A/D Converter," *Dig. Tech. Papers International Solid-State Circuits Conference*, pp. 128–129, Feb. 2001.
- [16] H. Moon, M. K. Song, J. W. Kim and K. H. Kim "A 10bit 30MSPS CMOS A/D Converter for a High Performance Video Application," *IEEE Trans. on Consumer Electronics*, vol 43, pp. 1301–1304, Nov. 1997.
- [17] K. Bult, A. Buchwald. and J. Laskowski, "A 170mW 10b 50MSample/s CMOS ADC in 1mm²," *Dig. Tech. Papers International Solid-State Circuits Conference*, pp. 137–138, Feb. 1997.

Bibliography

- [18] H. C. Choi, H. J. Park, S. S. Hwang, S.K. Bae, J. W. Kim and P. Chung, "A 1.5V 10-bit 25MSPS Pipelined A/D Converter", *IEEE Asia Pacific Conference on ASIC*, pp. 170 – 173, Aug. 1999.
- [19] H. C. Choi, H. J. Park, S.K. Bae, J. W. Kim and P. Chung, "A 1.4V 10-bit 20MSPS Pipelined A/D Converter", *IEEE International Symposium on Circuits and System*, pp. 439 – 442, May 2000.
- [20] D. G. Naim, "A 10-bit, 3V, 100MS/s Pipelined ADC", *Proceedings of the IEEE Custom Integrated Circuits Conference*, , pp.257 – 260, May 2000.
- [21] L. Singer, S.A. Ho, M. Timoko and D. Kelly, "A 12b 65MSample/s CMOS ADC with 82db SFDR at 120MHz," *Dig. Tech. Papers International Solid-State Circuits Conference*, pp. 38–39, Feb. 2000.
- [22] Y. D. Jeon, B. L. Jeon, S. C. Lee, S. M. Yoo and S. H. Lee, "A 12b 50MHz 3.3V CMOS Acquisition Time Minimized A/D Converter," *Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 613 - 616 , Jan. 2000.
- [23] I. Mehr and L. Singer, "A 55mW, 10-bit, 40-Msample/s Nyquist_Rate CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 35, pp. 318–325, Mar. 2000.
- [24] B. Yu and W. C. Black, "A 900MS/s 6b Interleaved CMOS Flash ADC," *IEEE Custom Integrated Circuits Conference*, pp. 149–152, May 2001.
- [25] M. J. Choe, B. S. Song and K. Bacrania, "A 8-b 100-MSample/s CMOS pipelined folding ADC," *IEEE J. Solid-State Circuits*, vol. 36, pp. 184–194, Feb. 2001.
- [26] J. Ming and S. H. Lewis, "A 8-b 80-MSample/s Pipelined Analog to Digital Converter," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1489–1497, Oct. 2001.
- [27] S. Kim and M. Song, "A 8-bit 200MSPS CMOS A/D Converter for Analog Interface Module of TFT-LCD Driver," *IEEE International Symposium on Circuits and System*. 36, pp. 528–531, May 2001.

Bibliography

-
- [28] K. Bult and A. Buchwald, "An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1 mm²," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1887–1895, Dec. 1997.
 - [29] A. Abo and P. Gray, "A 1.5-V 10-bit 14.3-MS/s CMOS pipeline analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 34, pp. 599–605, May 1999.
 - [30] H. V. D. Ploeg and R. Remmers, "A 3.3-V, 10-b, 25-MSample/s Two-Step ADC in 0.35- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1803–1811, Dec. 1999.
 - [31] S. M. Yoo; J. B. Park; S. H. Lee and U. K. Moon, "A 2.5-V 10-b 120-MSample/s CMOS Pipelined ADC based on Merged-Capacitor switching," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Express Briefs*, vol. 51, pp. 269–275, May 2004.
 - [32] J. P. Li and U. K. Moon, "A 1.8-V 67-mW 10-bit 100-MS/s pipelined ADC using time-shifted CDS technique," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1468–1476, Sept. 2004.
 - [33] H. H. Kim and K. S. Yoon, "A 12-bit Current-Mode Folding/Interpolation CMOS A/D Converter with Multipliers," *IEEE Proceeding of TENCON*, vol. 1, pp. 278–281, Sept. 1999.
 - [34] M. Choe and B. Song, "An 8-b 100-MSample/s CMOS pipelined folding ADC," *Dig. Tech. Papers, Symposium on VLSI Circuits*, pp. 81 – 82, June 1999.
 - [35] K. Yoon, J. Lee, D. K. Jeong and W. Kim, "An 8-bit 125-Ms/s CMOS Folding ADC for Gigabit Ethernet," *Dig. Tech. Papers, Symposium on VLSI Circuits*, pp. 212 – 213, June 2000.
 - [36] H. Pan, M. Segami, M. Choi, J. Cao, A. Abidi, "A 3.3-V 12-b 50-MS/s A/D Converter in 0.6- μ m CMOS with over 80-dB SFDR," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1769–1780, Dec. 2000.
 - [37] T. H. Kim, J. J. Sung, S. H. Kim, W. Joo, S. B. You and S. Kim, "A 10-bit, 40Msapmes/s Cascading Folding and Interpolaaing A/D Converter with Wide

Bibliography

- Range Error Correction,” *IEEE Asia Pacific Conference on ASIC*, pp. 57-60, Aug. 2000.
- [38] L. Sumanen, M. Waltari, K. Halonen, “A 10-bit 200 MS/s CMOS Parallel Pipeline A/D Converter,” *IEEE J. Solid-State Circuits*, vol. 36, pp. 1048–1055, Jul. 2001.
- [39] R. C. Taft and M. R. Tursi, “A 100-MS/s 8-b CMOS subranging ADC with sustained Parametric Performance from 3.8V Down to 2.2V,” *IEEE J. Solid-State Circuits*, vol. 36, pp. 331–338, March 2001.
- [40] Y. T. Wang, B. Razavi, “An 8-Bit 150-MHz CMOS A/D Converter,” *IEEE J. Solid-State Circuits*, vol. 35, pp. 308–317, Mar. 2000.
- [41] H. van der Ploeg, G. Hoogzaad, H. A. H. Termeer, M. Vertregt and R. L. J. Rooves, “A 2.5V 12b 54MSample/s 0.25 μ m CMOS ADC in 1mm²,” *Dig. Tech. International Solid-State Circuits Conference*, pp. 132–133, Feb. 2001.
- [42] K. Kusumoto and A. Matsuzawa, “A 10-b 20-MHz 30-mW Pipelined Interpolating CMOS ADC,” *IEEE J. Solid-State Circuits*, vol. 28, pp. 1200–1206, Dec. 1993.
- [43] B. P. Brandt and J. Lutsky, “A 75-mW 10-b 20-MS/s CMOS subranging ADC with 9.5 effective bits at Nyquist,” *IEEE J. Solid-State Circuits*, vol. 34, pp. 1788–1953, Dec. 1999.
- [44] M. Gustavsson, J. Jacob Wikner and N. Nick. Tan, *CMOS Data Converters for Communications*, Kluwer Academic Publishers, 2000.
- [45] N. Tan, *Switched-Current Design and Implementaion of Oversampling A/D Converters*, Kluwer Academic Publishers, 1997.
- [46] B. Razavi, *Principles of Data Conversion System Design*, IEEE Press, 1995.
- [47] C. C. Enz, and G. C. Temes, “Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization,” *Proceedings of the IEEE*, vol. 84, pp. 1584-1614, Nov. 1996.

Bibliography

- [48] K. Kattmann and J. Barrow, "A technique for reducing differential nonlinearity errors in flash A/D converters", *Dig. Tech. Papers International Solid-State Circuits Conference*, pp. 170–171, Feb. 1991.
- [49] Chartered Semiconductor --- <http://www.charteredsemi.com/>
- [50] B. Razavi and B. A. Wooley, "Design techniques for high-speed, high-resolution comparators"; *IEEE J. Solid-State Circuits*, vol. 27, pp. 1916-1926, Dec. 1992.
- [51] H. Kimura, A. Matsuzawa, T. Nakamura and S. Sewada, "A 10-b 300-MHz Interpolated-Parallel A/D Converter," *IEEE J. Solid-State Circuits*, vol. 28, pp. 438–446, Apr. 1993.
- [52] S. Hosotani, T. Miki, A. Maeda and N. Yazawa, "An 8-bit 20-MS/s CMOS A/D Converter with 50-mW Power Consumption", *IEEE J. Solid-State Circuits*, vol. 25, pp. 167–172, Feb. 1990.
- [53] B. L. Jeon and S. H. Lee, "A 10b 50MHz 320mW CMOS A/D Converter For Video Application," *IEEE Transaction on Consumer Electronic*, vol. 45 no. 1, pp. 252-258, Feb. 1999.
- [54] K. Nagaraj, H. S. Fetterman, J. Anidjar, S. H. Lewis and R. G. Renninger, "A 250-mW, 8-b, 52-Msamples/s Parallel-Pipelined A/D Converter with Reduced Number of Amplifiers," *IEEE J. Solid-State Circuits*, vol. 32, pp. 312–320, Mar. 1997.
- [55] W. C. Song, H. C. Choi, S. U. Kawk and B. S. Song, "A 10-b 20-Msamples/s Low-Power CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 30, pp. 514–521, May 1995.
- [56] S. H. Lewis, H. S. Fetterman, G. F. Gross, Jr., R. Ramachandran and T. R. Viswanathan, "A 10-b 20-Msample/s Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 27, pp. 351–358, Mar. 1992.
- [57] H. S. Lee, D. A. Hodges and P. R. Gray, "A Self-Calibrating 15 Bit CMOS A/D Converter," *IEEE J. Solid-State Circuits*, vol. SC-19, pp. 813–819, Dec. 1984.

Bibliography

- [58] Y. M. Lin, B. Kim and P. R. Gray, "A 13-b 2.5-MHz Self-Calibrated Pipelined A/D Converter in 3- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 26, pp. 628–635, Apr. 1991.
- [59] S. H. Lee and B.-S. Song, "Digital-Domain Calibration for Multistep Analog-to-Digital Converters," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1679–1688, Dec. 1992.
- [60] I. E. Opris, L. D. Lewicki and B. C. Wong, "A Single-Ended 12-bit 20 Msample/s Self-Calibrating Pipeline A/D Converter," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1898–1903, Dec. 1998.
- [61] U. K. Moon and B. S. Song, "Background Digital Calibration Techniques for Pipelined ADCs," *IEEE Trans. Circuits and Systems-II*, vol. 44, pp. 102–109, Feb. 1997.
- [62] J. M. Ingino and B. A. Wooley, "A Continuously Calibrated 12-b, 10-MS/s, 3.3-V A/D Converter," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1920–1931, Dec. 1998.
- [63] B. Nauta and A. G. W. Venes, "A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1302–1308, Dec. 1995.
- [64] A. G. W. Venes and R. J. van de Plassche, "An 80-MHz, 80-mW 8-b CMOS Folding A/D Converter with Distributed Track-and-Hold Preprocessing," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1846–1853, Dec. 1996.
- [65] P. Vorenkamp and R. Roovers, "A 12-b, 60-MSample/s Cascaded Folding and Interpolating ADC," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1876–1886, Dec. 1997.
- [66] M. P. Flynn and B. Sheahan, "A 400-Msample/s. 6-b CMOS Folding and Interpolating ADC," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1132–1938, Dec. 1998.

Bibliography

- [67] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, Inc, 1997.
- [68] A. G. Dingwall and V. Zazzu, "An 8-MHz CMOS subranging 8-Bit A/D converter," *IEEE J. Solid-State Circuits*, vol. SC-20, pp. 1138–1143, Dec. 1985.
- [69] R. van de Plassche, *Integrated Analog-to-Digital and Digital-to-Analog Converters* Kluwer Academic Publishers, 1994.
- [70] C. S. G. Conroy, D. W. Cline and P. R. Gray, "An 8-b 85-MS/s Parallel Pipeline A/D Converter in 1- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 28, pp. 447–454, Apr. 1993.
- [71] M. Yotsuyanagi and T. Etoh, K. Hirata, "A 10-b 50-MHz Pipelined CMOS A/D Converter with S/H," *IEEE J. Solid-State Circuits*, vol. 28, pp. 292–300, Mar. 1993.
- [72] K. Nakamura, M. Hotta, L. R. Carley and D. J. Allstot, "An 85 mW, 10 b, 40 Msample/s CMOS Parallel-Pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 30, pp. 173–183, Mar. 1995.
- [73] K. Y. Kim and N. Kusayanagi, A. A. Abidi, "A 10-b, 100-MS/s CMOS A/D Converter," *IEEE J. Solid-State Circuits*, vol. 32, pp. 302–311, Mar. 1997.
- [74] K. C. Dyer, D. Fu, S. H. Lewis and P. J. Hurst, "An Analog Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1912–1919, Dec. 1998.
- [75] D. Fu, K. C. Dyer, S. H. Lewis and P. J. Hurst, "A Digital Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1904–1911, Dec. 1998.
- [76] P. R. Gray, High speed CMOS A/D Converters, Lecture Notes, UC Berkeley.
- [77] S. U. Kwak, B.-S. Song and K. Bacrania, "A 15-b, 5-Msample/s Low-Spurious CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1866–1875, Dec. 1997.

Bibliography

- [78] M. J. Choe, B. S. Song and K. Bacrania, "A 13-b 40-MSample/s CMOS pipelined folding ADC with Background Offset Trimming," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1781–1789, Dec. 2000.
- [79] B. Razavi, "*Design of Analog CMOS Integrated Circuits*", McGRAW-Hill, 2001.
- [80] S. M. Jamal, D. Fu, M. P. Singh, P. J. Hurst and S. H. Lewis, "Calibration of sample-time error in a two channel time-interleaved analog-to digital converter", *IEEE Trans. on Circuit and System: Part I*, vol.51, no.1, pp. 130-139, Jan. 2004.
- [81] A. G. F. Dingwall and V. Zazzu, "An 8-MHz CMOS subranging 8-bit A/D converter," *IEEE J. of Solid-State Circuits*, vol. SC-20, no. 6, pp 1138-1143, Dec. 1985.
- [82] J. Doernberg, P. R. Gray, and D. A. Hodges, "A 10-bit 5-Msample/s CMOS two-step flash ADC," *IEEE J. of Solid-State Circuits*, vol.24(no.2), pp. 241- 249, April 1989.
- [83] R. Petschacher, B. Zojer, B. Astegher, H. Jessner, and A. Lechner, "A 10-b 75-MSPS subranging A/D converter with integrated sample and hold," *IEEE J. of Solid-State Circuits*, vol. 25, no. 6, pp 1339-1346, Dec. 1990.
- [84] S. H. Lewis and P. R. Gray,, "A pipelined 5-Msample/s 9-bit analog-todigital converter," *IEEE J. of Solid-State Circuits*, vol. SC-22 (no. 6), pp. 954-961, Dec. 1987.
- [85] S. Brigati, G. Caiulo, F. Maloberti, and G. Torelli, "Active compensation of parasitic capacitances in a 10 bit 50 MHz CMOS D/A converter," in *Proc. of IEEE Custom Integrated Circuits Conf.*, pp. 507-510, 1994.
- [86] M. J. M. Pelgrom, "A 10-b 50-MHz CMOS D/A converter with 75- Omega buffer," *IEEE J. of Solid-State Circuits*, vol. 25, no. 6, pp 1347-1352, Dec. 1990.
- [87] I. A. Yong, J. K. Greason, and K. L. Wong, "A PLL Clock Generator with 5 to 110 MHz of Lock Range for Microprocessors," *IEEE J. Solid-State Circuits*, vol.27, no. 2, pp. 1599-1607, Nov .1992.

Bibliography

- [88] B. Hernes, O. Moldsvor and T. Saether, "A -80 dB HD3 opamp in 3.3 V CMOS technology using tail current compensation", *Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on*, Vol. 1, pp.216-219, May 2001.
- [89] Kh. Hadidi and A.Khoei, "A highly linear cascode-driver CMOS source follower buffer," *Proceedings of IEEE International Conference On Electronics, Circuits, and Systems*, pp.1243-1246, Oct 1996.
- [90] M. A. M. Zin, H. Kobayashi, K. Kobayashi and J. I. Ichimura, "A high-speed CMOS track/hold circuit", *Proc. of IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, vol. 3, pp. 1709–1712, Sept. 1999.
- [91] P. Wambacp and W. Sansen, "*Distortion Analysis of Analog Integrated Circuits*", Kluwer Academic Publisher, 1998.
- [92] G. Palumbo and S. Pennisi, "*Feedback Amplifiers: Theory and Design*", Kluwer Accademic Publisher, January 2002.
- [93] G. Palumbo and S. Pennisi, "High-frequency harmonic distortion in feedback amplifiers: Analysis and Applications", *IEEE Trans. on Circuits and Systems: Part I*, vol. 50, no. 3, pp. 328-340, March 2003.
- [94] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, "*Analysis and Design of Analog CMOS Integrated Circuits*", John Wiley & Sons, Inc, 2001.
- [95] P. Cost, C. Fiocchi, U. Gatti and F. Maloberti, "High-performance BiCMOS output buffer design strategies", *Proc. of IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 2, pp.168–171, May 1999.
- [96] P. E. Allen and D. R. Holberg, "*CMOS Analog Circuit Design*", Oxford University Press, 2002.
- [97] P. Wambacq, G. Giles and P. R. Kinget, "High-frequency distortion analysis of analog integrated circuits", *IEEE Trans. on Circuits & Systems: Part II*, vol. 46, no. 3, pp 335-344, March 1999.
- [98] "*Hspice User's Manual*". Meta-Software, 2000.

Bibliography

- [99] K. Simons, "The decibel relationship between amplifier distortion products", *Proc. IEEE*, vol. 58, pp. 1071–1086, July 1970.
- [100] R. Meyer and A. Wong, "Blocking and desensitization in RF amplifier", *IEEE J. Solid-State Circuits*, vol. 30, pp. 944–946, Aug. 1995.
- [101] K. Hadidi, J. Sobhi, A. Hasankhaan, D. Muramatsu and T. Matsumoto, "A novel highly linear CMOS buffer", *Proc. of IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pp. 369–371, vol. 3, Sept. 1998.
- [102] A. Hastings, *The Art of Analog layout*, Prentice Hall, 2001
- [103] M. Waltari, L. Sumanen, T. Korhonen and K. Halonen, "A Self-Calibrated Pipeline ADC with 200MHz IF-sampling Frontend," *2002 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 314–315, Feb. 2002.

Appendix

Appendix

Appendix

Appendix A: Detailed Deviation of HD₂ for NSF

$$\begin{aligned}
 V_i &= f(V_o) \\
 &= V_o + V_{thn0} + K1_n (\sqrt{2\Phi_{fn} + V_o} - \sqrt{2\Phi_{fn}}) + \Delta V_n \sqrt{A_{bulkn} \left[1 + \frac{j\omega C_{Leqn}}{I_n} (V_o - V_{OQ}) \right]} \quad (A.1)
 \end{aligned}$$

The coefficients, b_1 and b_2 , are

$$\begin{aligned}
 b_1 &= f'(V_o = V_{OQ}) \\
 &= 1 + \frac{K1_n}{2(2\Phi_{fn} + V_{OQ})^{1/2}} + \frac{\Delta V_n}{2A_{bulkn-Q}^{1/2}} \left(\frac{-K1_n A_{0n}}{4(2\Phi_{fn} + V_{OQ})^{3/2}} + A_{bulkn-Q} \frac{j\omega C_{Leqn}}{I_n} \right) \quad (A.2)
 \end{aligned}$$

$$\begin{aligned}
 b_2 &= \frac{f''(V_o = V_{OQ})}{2} \\
 &= \frac{-K1_n}{8(2\Phi_{fn} + V_{OQ})^{3/2}} + \frac{\Delta V_n}{4} \left[\frac{-1}{2A_{bulkn-Q}^{3/2}} \left(\frac{K1_n A_{0n}}{4(2\Phi_{fn} + V_{OQ})^{3/2}} - A_{bulkn-Q} \frac{j\omega C_{Leqn}}{I_n} \right)^2 \right. \\
 &\quad \left. + \frac{1}{A_{bulkn-Q}^{1/2}} \left(\frac{3K1_n A_{0n}}{8(2\Phi_{fn} + V_{OQ})^{5/2}} - \frac{K1_n A_{0n}}{2(2\Phi_{fn} + V_{OQ})^{3/2}} \frac{j\omega C_{Leqn}}{I_n} \right) \right] \quad (A.3)
 \end{aligned}$$

$$\text{In (A.2), } \frac{\Delta V_n}{8A_{bulkn-Q}^{1/2}} \frac{K1_n A_{0n}}{(2\Phi_{fn} + V_{OQ})^{3/2}} \ll 1 + \frac{K1_n}{2(2\Phi_{fn} + V_{OQ})^{1/2}} \quad \text{and}$$

$$\frac{\Delta V_n}{2} A_{bulkn-Q}^{1/2} \frac{j\omega C_{Leqn}}{I_n} \ll 1 + \frac{K1_n}{2(2\Phi_{fn} + V_{OQ})^{1/2}} \quad \text{in the range of hundreds of MHz. In}$$

$$\text{(A.3), } \frac{-\Delta V_n}{16A_{bulkn-Q}^{3/2}} \left(\frac{K1_n A_{0n}}{4(2\Phi_{fn} + V_{OQ})^{3/2}} \right)^2 \text{ is smaller than other items. Finally, the}$$

second harmonic distortion can be expressed as

Appendix

$$\begin{aligned} HD_{2_NSF} &= \frac{1}{2} \frac{b_2}{b_1^2} \\ &\approx \frac{\frac{-K1_s}{16(2\Phi_{fs} + V_{oQ})^{3/2}} + \frac{\Delta V_s A_{bulbs_Q}^{1/2}}{16} \left(\frac{\omega C_{Leqn}}{I_s} \right)^2 + \frac{\Delta V_s K1_s A_{os}}{64 A_{bulbs_Q}^{1/2} (2\Phi_{fs} + V_{oQ})^{3/2}} \left[\frac{3}{(2\Phi_{fs} + V_{oQ})} - \frac{2j\omega C_{Leqn}}{I_s} \right]}{\left[1 + \frac{K1_s}{2(2\Phi_{fs} + V_{oQ})^{1/2}} \right]^2} V_n \end{aligned} \tag{A.4}$$

Appendix

Appendix B: Detailed Deviation of HD₂ for PSF

$$V_i = f_p(V_o) = V_o - V_{thp0} - \Delta V_p \sqrt{\frac{A_{bulkp}[1 + \lambda_{2p}(V_{DD} - V_o)] - \frac{j\omega C_{Leqp}}{I_{p0}}(V_o - V_{OQ})}{1 + \lambda_{1p}V_o}} \quad (B.1)$$

The coefficients, b_1 and b_2 , are

$$b_1 = f'(V_o = V_{OQ})$$

$$= 1 + \frac{\Delta V_p \sqrt{A_{bulkp}}}{2} \left\{ \sqrt{\frac{1}{T_{2p}T_{1p}}} (\lambda_{2pQ}^2 E_{sat} L_{2peff} + \frac{j\omega C_{Leqp}}{I_{p0}}) + \sqrt{\frac{T_{2p}}{T_{1p}^3}} \lambda_{1pQ}^2 E_{sat} L_{1peff} \right\} \quad (B.2)$$

$$b_2 = \frac{f''(V_o = V_{OQ})}{2}$$

$$= -\frac{\Delta V_p \sqrt{A_{bulkp}}}{16} \left\{ \sqrt{\frac{1}{T_{2p}^3 T_{1p}}} \lambda_{2pQ}^4 E_{sat}^2 L_{2peff}^2 - 2 \sqrt{\frac{1}{T_{2p} T_{1p}^3}} \lambda_{1pQ}^2 \lambda_{2pQ}^3 E_{sat}^2 L_{1peff} L_{2peff} \right.$$

$$- 3 \sqrt{\frac{T_{2p}}{T_{1p}^5}} \lambda_{1pQ}^4 E_{sat}^2 L_{1peff}^2 + 4 \sqrt{\frac{1}{T_{2p} T_{1p}}} \lambda_{2pQ}^3 \frac{E_{sat} L_{2peff}^2}{P_{CLMp} I_p} - 4 \sqrt{\frac{T_{2p}}{T_{1p}^3}} \lambda_{1pQ}^3 \frac{E_{sat} L_{1peff}^2}{P_{CLMp} I_p} \quad (B.3)$$

$$+ \sqrt{\frac{1}{T_{2p}^3 T_{1p}}} \left(\frac{j\omega C_{Leqp}}{I_{p0}} \right)^2 + 2 \sqrt{\frac{1}{T_{2p}^3 T_{1p}}} \lambda_{2pQ}^2 E_{sat} L_{2peff} \frac{j\omega C_{Leqp}}{I_{p0}}$$

$$\left. - 2 \sqrt{\frac{1}{T_{2p} T_{1p}^3}} \frac{j\omega C_{Leqp}}{I_{p0}} \lambda_{1pQ}^2 E_{sat} L_{1peff} \right\}$$

where $T_{2p} = 1 + \lambda_{2pQ}(V_{DD} - V_{OQ})$, $T_{1p} = 1 + \lambda_{1pQ}V_{OQ}$. Note that λ_{1pQ} , λ_{2pQ} are the constant values for λ_{1p} and λ_{2p} respectively when $V_o = V_{OQ}$.

$$\text{In (B.2), } \frac{\Delta V_p \sqrt{A_{bulkp}}}{2} \left\{ \sqrt{\frac{1}{T_{2p}T_{1p}}} (\lambda_{2pQ}^2 E_{sat} L_{2peff} + \frac{j\omega C_{Leqp}}{I_{p0}}) + \sqrt{\frac{T_{2p}}{T_{1p}^3}} \lambda_{1pQ}^2 E_{sat} L_{1peff} \right\} \ll 1$$

in the range of hundreds of MHz. Since λ_{1pQ} , $\lambda_{2pQ} \ll 1$, $T_{2p} \cong 1$ and $T_{1p} \cong 1$ in (B.3),

the second harmonic distortion can be simplified as

Appendix

$$\begin{aligned}
 HD_{2_PSF} &\cong \frac{1}{2} \frac{b_2}{b_1^2} \\
 &\cong \frac{\Delta V_p \sqrt{A_{bulkp}}}{16} V_m \left\{ \frac{4}{P_{CLMp}} \frac{L_{1peff}}{l_p} (E_{sat} L_{1peff} \lambda_{1pQ}) (\lambda_{1pQ}^2 - \lambda_{2pQ}^2 \frac{\lambda_{2pQ}}{\lambda_{1pQ}} \frac{L_{2peff}^2}{L_{1peff}^2}) \right. \\
 &\quad + (\lambda_{2pQ} E_{sat} L_{2peff})^2 (3\lambda_{1pQ}^2 \frac{L_{1peff}}{L_{2peff}} - \lambda_{2pQ}^2) + (\lambda_{1pQ} E_{sat} L_{1peff})^2 (3\lambda_{1pQ}^2 - \lambda_{2pQ}^2 \frac{L_{2peff}}{L_{1peff}}) \\
 &\quad \left. + (\frac{\omega C_{Leqp}}{I_{p0}})^2 + 2 \frac{j\omega C_{Leqp}}{I_{p0}} E_{sat} L_{1peff} (\lambda_{1pQ}^2 - \lambda_{2pQ}^2 \frac{L_{2peff}}{L_{1peff}}) \right\} \quad (B.4)
 \end{aligned}$$

Appendix

Appendix C: Detailed Deviation of HD₂ for CCSF

$$\begin{aligned}
V_i &= V_o + V_{thn0} + K1_n (\sqrt{2\Phi_{fn} + V_o} - \sqrt{2\Phi_{fn}}) \\
&+ \Delta V_n \sqrt{A_{bulkn} \left[1 + \frac{j\omega C_{Leqn}}{I_n} (V_o - V_{OQ}) \right]} \\
&- V_{thp0} - K1_p (\sqrt{2\Phi_{fp} + [V_{DD} - (V_o + V_{GS_Q})]} - \sqrt{2\Phi_{fp}}) \\
&- \Delta V_p \sqrt{A_{bulkp} \left[1 - \frac{j\omega C_{Leqp}}{I_p} (V_o + V_{GS_Q} - V_{XQ}) \right]}
\end{aligned} \tag{C.1}$$

with $V_{GS_Q} = V_{thn0} + K1_n (\sqrt{2\Phi_{fn} + V_{OQ}} - \sqrt{2\Phi_{fn}}) + \Delta V_n \sqrt{A_{bulkn}}$. The coefficients, b_1 and b_2 , are

$$\begin{aligned}
b_1 = f'(V_o = V_{OQ}) &= 1 + \frac{K1_n}{2(2\Phi_{fn} + V_{OQ})^{1/2}} + \frac{K1_p}{2[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS_Q})]^{1/2}} \\
&- \frac{\Delta V_n}{8A_{bulkn_Q}^{1/2}} \frac{K1_n A_{0n}}{(2\Phi_{fn} + V_{OQ})^{3/2}} - \frac{\Delta V_p}{8A_{bulkp_Q}^{1/2}} \frac{K1_p A_{0p}}{[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS_Q})]^{3/2}} \\
&+ \frac{\Delta V_n}{2} A_{bulkn_Q}^{1/2} \frac{j\omega C_{Leqn}}{I_n} + \frac{\Delta V_p}{2} A_{bulkp_Q}^{1/2} \frac{j\omega C_{Leqp}}{I_p}
\end{aligned} \tag{C.2}$$

$$\begin{aligned}
b_2 = \frac{f''(V_o = V_{OQ})}{2} &= \frac{-K1_n}{16(2\Phi_{fn} + V_{OQ})^{3/2}} \\
&+ \frac{\Delta V_n}{8} \left[\frac{-1}{2A_{bulkn_Q}^{3/2}} \left(\frac{K1_n A_{0n}}{4(2\Phi_{fn} + V_{OQ})^{3/2}} \right)^2 + \frac{3K1_n A_{0n}}{8A_{bulkn_Q}^{1/2} (2\Phi_{fn} + V_{OQ})^{5/2}} \right] \\
&+ \frac{\Delta V_n}{16} A_{bulkn_Q}^{1/2} \left(\frac{\omega C_{Leqn}}{I_n} \right)^2 + \frac{K1_p}{16[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS_Q})]^{3/2}} \\
&- \frac{\Delta V_p}{8} \left[\frac{-1}{2A_{bulkp_Q}^{3/2}} \left(\frac{K1_p A_{0p}}{4[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS_Q})]^{3/2}} \right)^2 + \frac{3K1_p A_{0p}}{8A_{bulkp_Q}^{1/2} [2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS_Q})]^{5/2}} \right] \\
&- \frac{\Delta V_p}{16} A_{bulkp_Q}^{1/2} \left(\frac{\omega C_{Leqp}}{I_p} \right)^2 + \frac{\Delta V_n}{8} \left(\frac{-1}{4A_{bulkn_Q}^{1/2} (2\Phi_{fn} + V_{OQ})^{3/2}} \frac{K1_n A_{0n}}{I_n} \frac{j\omega C_{Leqn}}{I_n} \right) \\
&- \frac{\Delta V_p}{8} \left(\frac{-1}{4A_{bulkp_Q}^{1/2} [2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS_Q})]^{3/2}} \frac{K1_p A_{0p}}{I_p} \frac{j\omega C_{Leqp}}{I_p} \right)
\end{aligned} \tag{C.3}$$

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$$\text{In (C-2), } \frac{\Delta V_n}{8A_{bulkn-Q}^{1/2}} \frac{K1_n A_{0n}}{(2\Phi_{fn} + V_{OQ})^{3/2}}, \frac{\Delta V_p}{8A_{bulkp-Q}^{1/2}} \frac{K1_p A_{0p}}{[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS-Q})]^{3/2}} \ll 1$$

$$\text{and } \frac{\Delta V_n}{2} A_{bulkn-Q}^{1/2} \frac{j\omega C_{Leqn}}{I_n}, \frac{\Delta V_p}{2} A_{bulkp-Q}^{1/2} \frac{j\omega C_{Leqp}}{I_p} \ll 1 \text{ in the range of hundreds of}$$

$$\text{MHz. In (C.3), } \frac{-\Delta V_n}{16A_{bulkn-Q}^{3/2}} \left(\frac{K1_n A_{0n}}{4(2\Phi_{fn} + V_{OQ})^{3/2}} \right)^2 \text{ and}$$

$$\frac{-\Delta V_p}{16A_{bulkp-Q}^{3/2}} \left(\frac{K1_p A_{0p}}{4[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS-Q})]^{3/2}} \right)^2 \text{ are smaller than other items. Finally,}$$

the second harmonic distortion can be expressed as

$$\begin{aligned} HD_{2_CCSF} &\cong \frac{1}{2} \frac{b_2}{b_1^2} \\ &= -\frac{K1_n}{16(2\Phi_{fn} + V_{OQ})^{3/2}} + \frac{\Delta V_n A_{bulkn-Q}^{1/2}}{16} \left(\frac{\omega C_{Leqn}}{I_n} \right)^2 \\ &\quad + \frac{\Delta V_n K1_n A_{0n}}{64 A_{bulkn-Q}^{1/2} (2\Phi_{fn} + V_{OQ})^{3/2}} \left(\frac{3}{(2\Phi_{fn} + V_{OQ})} - \frac{2j\omega C_{Leqn}}{I_n} \right) \\ &\quad + \frac{K1_p}{16[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS-Q})]^{3/2}} - \frac{\Delta V_p A_{bulkp-Q}^{1/2}}{16} \left(\frac{\omega C_{Leqp}}{I_p} \right)^2 \\ &\quad - \frac{\Delta V_p K1_p A_{0p}}{64 A_{bulkp-Q}^{1/2} [2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS-Q})]^{3/2}} \left(\frac{3}{[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS-Q})]} - \frac{2j\omega C_{Leqp}}{I_p} \right) \\ &\cong \frac{\left\{ 1 + \frac{K1_n}{2(2\Phi_{fn} + V_{OQ})^{1/2}} + \frac{K1_p}{2[2\Phi_{fp} + (V_{DD} - V_{OQ} - V_{GS-Q})]^{1/2}} \right\}^2}{V_m} \end{aligned} \quad (C.4)$$

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Appendix D: Nonlinear Analysis of Preamplifier

I. Assumptions

The harmonic analysis of discrete-time signal in a nonlinear sample-data circuit and system is not straightforward. The continuous-time approach can be used to approximate the specific sample-data spectral components if the sampling frequency is made much higher than the component frequency of interest. Due to high sampling rate, the aliasing effect to these frequencies is insignificant. Hence, the continuous-time counterparts can represent the corresponding spectral components with reasonable accuracy. More importantly, the ratio of the continuous-time harmonic components will be similar to that of sample-data harmonics because the harmonic distortions are evaluated in relative sense. In this application, the fundamental signal frequency and its second and third harmonics are assumed less than the sampling clock frequency. Therefore, the approximated continuous-time analysis provides an easier method to evaluate the nonlinearity of the switched-capacitor preamplifier.

II. Analysis

Fig. A illustrates the stage 1 of the mismatched differential preamplifier, where A_1 is the gain of amplifier. The voltage difference between the input and reference voltage is defined as $v_i = V_{ref+} - V_{in+} = -(V_{ref-} - V_{in-})$. The upper branch is analyzed to demonstrate the nonlinearity effect. When the switches S_{a1+} and S_{a1-} are on as shown

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in Fig. A(a), the stage 1 is in the amplification phase. According to the principle of conservation of electric charge, the nodal equation at node 1 can be achieved:

$$(0 - v_i)C_1 = -\frac{v_{ol+}}{A_1}C_1 + \left(-\frac{v_{ol+}}{A_1} - v_{ol+}\right)C_{1f} \quad (D.1)$$

Thus, v_{ol+} can be expressed as

$$v_{ol+} = \frac{C_1}{\frac{1}{A_1}C_1 + \left(1 + \frac{1}{A_1}\right)C_{1f}} v_i = \frac{C_1}{C_{1f}} \frac{A_1}{1 + \frac{C_1}{C_{1f}} + A_1} v_i \quad (D.2)$$

Fig. D.1 Stage 1 of the differential preamplifier with Mismatching

The gain of amplifier, A_1 , includes the linear component as well as the nonlinear components. Thus, A_1 can be expressed as $K_{A1a1} + K_{A1a2}v_i + K_{A1a3}v_i^2$, where K_{A1a1} is the linear coefficient whilst K_{A1a2} and K_{A1a3} are the second and third order

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nonlinear coefficient, which can be characterized through simulation of amplifier.

Hence, (D2) can be rewritten as

$$v_{ol+} = \frac{C_1}{C_{1f}} \frac{A_1}{1 + \frac{C_1}{C_{1f}} + A_1} v_i = \frac{C_1}{C_{1f}} \frac{K_{A1a1} + K_{A1a2}v_i + K_{A1a3}^2 v_i^2}{1 + \frac{C_1}{C_{1f}} + K_{A1a1} + K_{A1a2}v_i + K_{A1a3}^2 v_i^2} v_i \quad (D.3)$$

The binomial expression of $(1+x)^a$ is given by

$$(1+x)^a = 1 + ax + \frac{a(a-1)}{2!} x^2 + \frac{a(a-1)(a-2)}{3!} x^3 + \dots \quad \text{By expanding}$$

$$\frac{K_{A1a1} + K_{A1a2}v_i + K_{A1a3}^2 v_i^2}{1 + \frac{C_1}{C_{1f}} + K_{A1a1} + K_{A1a2}v_i + K_{A1a3}^2 v_i^2} \text{ term using binomial expansion, } v_{ol+} \text{ can be}$$

described in term of the source signal v_i through closed-loop nonlinear coefficients,

a_{1f} , a_{2f} and a_{3f} as follow:

$$v_{ol+} = a_{1f}v_i + a_{2f}v_i^2 + a_{3f}v_i^3 + \dots \quad (D.4)$$

$$\text{with } a_{1f} = \frac{C_1}{C_{1f}} \frac{K_{A1a1}}{1 + \frac{C_1}{C_{1f}} + K_{A1a1}} \cong \frac{C_1}{C_{1f}}, \quad a_{2f} = \frac{C_1}{C_{1f}} \frac{(1 + \frac{C_1}{C_{1f}})K_{A1a2}}{(1 + \frac{C_1}{C_{1f}} + K_{A1a1})^2} \text{ and}$$

$$a_{3f} = \frac{C_1}{C_{1f}} \left[\frac{(1 + \frac{C_1}{C_{1f}})K_{A1a3}}{(1 + \frac{C_1}{C_{1f}} + K_{A1a1})^2} - \frac{(1 + \frac{C_1}{C_{1f}})K_{A1a2}^2}{(1 + \frac{C_1}{C_{1f}} + K_{A1a1})^3} \right]$$

Note that the coefficient a_{1f} is responsible for the linear closed-loop behavior of the stage 1, whereas a_{2f} and a_{3f} denote the second and third order nonlinear coefficient respectively.

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At this juncture, the nodal voltages at 1, 2 are $V_b - \frac{v_{ol+}}{A_1}$ and $V_b + v_{ol+}$ respectively,

where V_b is the virtual ground. Hence, the charges stored in C_{1f} is $(v_{ol+} + \frac{v_{ol+}}{A_1})C_{1f}$.

When the switches, S_{a1+} and S_{a1+}' , are turned off, the charges stored in their channels are injected onto the two plates of C_{1f} as shown in Fig. A(b). Thus, Δq_{ch+} and $\Delta q_{ch+}'$ are

$$\Delta q_{ch+} = -\frac{1}{2} \left[V_{DD} - V_b - V_{th0} - \gamma \left(\sqrt{2\Phi_f + V_b - \frac{v_{ol+}}{A_1}} - \sqrt{2\Phi_f} \right) \right] C_{ox} WL \quad (D.5)$$

$$\Delta q_{ch+}' = -\frac{1}{2} \left[V_{DD} - V_b - v_{ol+} - V_{th0} - \gamma \left(\sqrt{2\Phi_f + V_b + v_{ol+}} - \sqrt{2\Phi_f} \right) \right] C_{ox} WL \quad (D.6)$$

where Φ_f is the Fermi level. Using binomial expression to expand and $\sqrt{2\Phi_f + V_b + v_{ol+}}$ in (D6), the effective charge stored C_{1f} can be written as

$$Q_{cap+} = (v_{ol+} + \frac{v_{ol+}}{A_1})C_{1f} + \Delta q_{ch+}' - \Delta q_{ch+} = K_{q1}v_{ol+} + K_{q2}v_{ol+}^2 + K_{q3}v_{ol+}^3 + \dots \quad (D.7)$$

$$\text{where } K_{q1} = \left(1 + \frac{1}{A_1} \right) \left\{ C_{1f} + \frac{1}{2} \left(1 + \frac{\gamma}{2\sqrt{2\Phi_f + V_b}} \right) C_{ox} WL \right\} \quad (D.8)$$

$$K_{q2} = \left(1 - \frac{1}{A_1^2} \right) \frac{-\gamma}{16(2\Phi_f + V_b)^{3/2}} C_{ox} WL \quad (D.9)$$

$$K_{q3} = \left(1 + \frac{1}{A_1^3} \right) \frac{\gamma}{32(2\Phi_f + V_b)^{5/2}} C_{ox} WL. \quad (D.10)$$

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Since $C_{1f} \gg \frac{1}{2} \left(1 + \frac{\gamma}{2\sqrt{2\Phi_f + V_b}} \right) C_{\alpha} WL$, (D8) can be approximated as

$K_{q1} = (1 + \frac{1}{A_1}) C_{1f}$ Form (D7), the charge in the feedback capacitor is not a linear

function of v_{o1+} . It also includes v_{o1+}^2 and v_{o1+}^3 items, which relate to the second order and third order nonlinear effect respectively.

Fig. D.2 Amplification Phase in Stage 2 and 3

In the following period, C_{1f} is connected to the stage 2 as the feedback capacitor as shown in Fig. B(a). According to the principle of conservation of electric charge at node 3, the following nodal equation can be achieved:

$$(0 - v_{o1+})C_2 - Q_{cap+} = -\frac{v_{o2+}}{A_2} C_2 + (-\frac{v_{o2+}}{A_2} - v_{o2+})C_{1f} \quad (D.11)$$

Thus, the output voltage of the stage 2 is

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$$v_{o2+} = \frac{C_2 v_{o1+} + Q_{cap+}}{\frac{1}{A_2} C_2 + (1 + \frac{1}{A_2}) C_{1f}} \cong \frac{C_2}{\left[1 + \frac{1}{A_2} \left(1 + \frac{C_2}{C_{1f}}\right)\right] C_{1f}} v_{o1+} + \frac{Q_{cap+}}{\left[1 + \frac{1}{A_2} \left(1 + \frac{C_2}{C_{1f}}\right)\right] C_{1f}} \quad (D.12)$$

Substitute (D.7) into (D.12) and replace A_2 in (D.12) by $K_{A2a1} + K_{A2a2}v_i + K_{A2a3}v_i^2$, where K_{A2a1} is the linear gain of amplifier in the stage 2, and K_{A2a2} K_{A2a3} denote the second and third order nonlinear coefficient of the stage 2 respectively. Similarly, using binomial expression, (D.12) can be rewritten as:

$$v_{o2+} = b_{1f} v_{o1+} + b_{2f} v_{o1+}^2 + b_{3f} v_{o1+}^3 + \dots \quad (D.13)$$

$$\text{where } b_{1f} = \frac{C_2}{C_{1f}} \frac{K_{A2a1}}{1 + \frac{C_2}{C_{1f}} + K_{A2a1}} + \frac{1 + K_{A2a1}}{1 + \frac{C_2}{C_{1f}} + K_{A2a1}} \quad (D.14)$$

$$b_{2f} = \frac{C_2}{C_{1f}} \frac{(1 + \frac{C_2}{C_{1f}}) K_{A2a2}}{(1 + \frac{C_2}{C_{1f}} + K_{A2a1})^2} + \frac{\frac{C_2}{C_{1f}} K_{A2a2}}{(1 + \frac{C_2}{C_{1f}} + K_{A2a1})^2} - \frac{\gamma C_{ox} WL}{16(2\Phi_f + V_b)^{3/2} C_{1f}} \frac{K_{A2a1}}{1 + \frac{C_2}{C_{1f}} + K_{A2a1}} \left(1 - \frac{1}{K_{A2a1}^2}\right) \quad (D.15)$$

$$b_{3f} = \frac{C_2}{C_{1f}} \left[\frac{(1 + \frac{C_2}{C_{1f}}) K_{A2a3}}{(1 + \frac{C_2}{C_{1f}} + K_{A2a1})^2} - \frac{(1 + \frac{C_2}{C_{1f}}) K_{A2a2}^2}{(1 + \frac{C_2}{C_{1f}} + K_{A2a1})^3} \right] + \left[\frac{\frac{C_2}{C_{1f}} K_{A2a3}}{(1 + \frac{C_2}{C_{1f}} + K_{A2a1})^2} - \frac{\frac{C_2}{C_{1f}} K_{A2a2}^2}{(1 + \frac{C_2}{C_{1f}} + K_{A2a1})^3} \right] - \frac{(1 + \frac{C_2}{C_{1f}}) K_{A2a2}}{(1 + \frac{C_2}{C_{1f}} + K_{A2a1})} \frac{\gamma C_{ox} WL}{16 C_{1f} (2\Phi_f + V_b)^{3/2}} + \frac{K_{A2a1}}{1 + \frac{C_2}{C_{1f}} + K_{A2a1}} \left(1 + \frac{1}{K_{A2a1}^3}\right) \frac{\gamma C_{ox} WL}{32 C_{1f} (2\Phi_f + V_b)^{5/2}} \quad (D.16)$$

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Because $1 + \frac{C_2}{C_{1f}} \ll K_{A2a1}$, thus (D.14) (D.15) (D.16) can be rewritten as

$$b_{1f} \cong 1 + \frac{C_2}{C_{1f}}, b_{2f} \cong \frac{\frac{C_2}{C_{1f}} (2 + \frac{C_2}{C_{1f}}) K_{A2a2}}{(1 + \frac{C_2}{C_{1f}} + K_{A2a1})^2} - \frac{\gamma C_{ox} WL}{16(2\Phi_f + V_b)^{3/2} C_{1f}} \text{ and}$$

$$b_{3f} \cong \frac{\frac{C_2}{C_{1f}} (2 + \frac{C_2}{C_{1f}}) K_{A2a3}}{(1 + \frac{C_2}{C_{1f}} + K_{A2a1})^2} - \frac{\frac{C_2}{C_{1f}} (2 + \frac{C_2}{C_{1f}}) K_{A2a2}^2}{(1 + \frac{C_2}{C_{1f}} + K_{A2a1})^3} \\ - \frac{(1 + \frac{C_2}{C_{1f}}) K_{A2a2}}{(1 + \frac{C_2}{C_{1f}} + K_{A2a1})} \frac{\gamma C_{ox} WL}{16C_{1f} (2\Phi_f + V_b)^{3/2}} + \frac{\gamma C_{ox} WL}{32C_{1f} (2\Phi_f + V_b)^{5/2}}$$

In order to simplify the analysis, assume the nonlinear effect of charge injection in the stage 3 is identical with the stage 2. Similarly, v_{o3+} is:

$$v_{o3+} = c_{1f} v_{o2+} + c_{2f} v_{o2+}^2 + c_{3f} v_{o2+}^3 + \dots \quad (D.17)$$

$$\text{where } c_{1f} \cong 1 + \frac{C_3}{C_{1f}}, c_{2f} \cong \frac{\frac{C_3}{C_{1f}} (2 + \frac{C_3}{C_{1f}}) K_{A3a2}}{(1 + \frac{C_3}{C_{1f}} + K_{A3a1})^2} - \frac{\gamma C_{ox} WL}{16(2\Phi_f + V_b)^{3/2} C_{1f}}$$

$$c_{3f} \cong \frac{\frac{C_3}{C_{1f}} (2 + \frac{C_3}{C_{1f}}) K_{A3a3}}{(1 + \frac{C_3}{C_{1f}} + K_{A3a1})^2} - \frac{\frac{C_3}{C_{1f}} (2 + \frac{C_3}{C_{1f}}) K_{A3a2}^2}{(1 + \frac{C_3}{C_{1f}} + K_{A3a1})^3} \\ - \frac{(1 + \frac{C_3}{C_{1f}}) K_{A3a2}}{(1 + \frac{C_3}{C_{1f}} + K_{A3a1})} \frac{\gamma C_{ox} WL}{16C_{1f} (2\Phi_f + V_b)^{3/2}} + \frac{\gamma C_{ox} WL}{32C_{1f} (2\Phi_f + V_b)^{5/2}}$$

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and K_{A3a1} is the linear gain amplifier in the stage 3, and K_{A3a2} K_{A3a3} denote the second and third order nonlinear coefficient of amplifier in the stage 3. Replacing (D.4) and (D13) into (D17), v_{o3+} can be expressed as a function of v_i :

$$v_{o3+} = d_{1f} v_i + d_{2f} v_i^2 + d_{3f} v_i^3 \quad (D.18)$$

where $d_{1f} = a_{1f} b_{1f} c_{1f}$, $d_{2f} = a_{2f} b_{1f} c_{1f} + a_{1f}^2 c_{1f} b_{2f} + a_{1f}^2 b_{1f}^2 c_{2f}$ and

$$d_{3f} = a_{3f} b_{1f} c_{1f} + 2a_{1f} a_{2f} c_{1f} b_{2f} + 2a_{1f} a_{2f} b_{1f}^2 b_{2f} + a_{1f}^3 c_{1f} b_{3f} + 2a_{1f}^3 b_{1f} b_{2f} c_{2f} + a_{1f}^3 b_{1f}^3 c_{3f}$$

Because $a_{1f}, b_{1f}, c_{1f} \gg a_{2f}, b_{2f}, c_{2f} \gg a_{3f}, b_{3f}, c_{3f}$, thus d_{2f} and d_{3f} can be

approximated as $d_{2f} \cong a_{1f}^2 b_{1f}^2 c_{2f}$ and $d_{3f} \cong a_{1f}^3 b_{1f}^3 c_{3f}$.

where $a_{1f}, b_{1f}, c_{1f}, c_{2f}$ and c_{3f} are:

$$\begin{aligned} a_{1f} &\cong \frac{C_1}{C_{1f}}, \quad b_{1f} \cong \frac{C_2}{C_{1f}} + 1, \quad c_{1f} \cong \frac{C_3}{C_{1f}} + 1, \\ c_{2f} &\cong \frac{\frac{C_3}{C_{1f}} (2 + \frac{C_3}{C_{1f}}) K_{A3a2}}{(1 + \frac{C_3}{C_{1f}} + K_{A3a1})^2} - \frac{\gamma C_{ox} WL}{16(2\Phi_f + V_b)^{3/2} C_{1f}} \\ c_{3f} &\cong \frac{\frac{C_3}{C_{1f}} (2 + \frac{C_3}{C_{1f}}) K_{A3a3}}{(1 + \frac{C_3}{C_{1f}} + K_{A3a1})^2} - \frac{\frac{C_3}{C_{1f}} (2 + \frac{C_3}{C_{1f}}) K_{A3a2}^2}{(1 + \frac{C_3}{C_{1f}} + K_{A3a1})^3} \\ &\quad - \frac{(1 + \frac{C_3}{C_{1f}}) K_{A3a2}}{(1 + \frac{C_3}{C_{1f}} + K_{A3a1})} \frac{\gamma C_{ox} WL}{16C_{1f} (2\Phi_f + V_b)^{3/2}} + \frac{\gamma C_{ox} WL}{32C_{1f} (2\Phi_f + V_b)^{5/2}} \end{aligned}$$

Similarly, the complementary output of stage 3, v_{o3-} , can be expressed as:

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$$v_{o3-} = d_{1f}'(-v_i) + d_{2f}'(-v_i)^2 + d_{3f}'(-v_i)^3 \quad (D.19)$$

With $d_{1f}' = a_{1f}' b_{1f}' c_{1f}'$, $d_{2f}' \cong a_{1f}'^2 b_{1f}'^2 c_{2f}'$ and $d_{3f}' \cong +a_{1f}'^3 b_{1f}'^3 c_{3f}'$. The nonlinear coefficient a_{1f}' , b_{1f}' , c_{1f}' , c_{2f}' and c_{3f}' is the corresponding coefficient of a_{1f} , b_{1f} , c_{1f} , c_{2f} and c_{3f} in mismatched differential preamplifier.

$$a_{1f}' \cong \frac{C_1}{C_{1f}}(1 + \alpha_c - \alpha_{c_f}), \quad b_{1f}' \cong \frac{C_2}{C_{1f}}(1 + \alpha_c - \alpha_{c_f}) + 1, \quad c_{1f}' \cong \frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f}) + 1,$$

$$c_{2f}' \cong \frac{\frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f})[2 + \frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f})]K_{A3a2}}{[1 + \frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f}) + K_{A3a1}]^2} - \frac{\gamma C_{ox} WL}{16(2\Phi_f + V_b)^{3/2} C_{1f}}(1 + \alpha_{WL})$$

and

$$c_{3f}' \cong \frac{\frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f})[2 + \frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f})]K_{A3a3}}{[1 + \frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f}) + K_{A3a1}]^2}$$

$$- \frac{\frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f})[2 + \frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f})]K_{A3a2}^2}{[1 + \frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f}) + K_{A3a1}]^3}$$

$$- \frac{[1 + \frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f})]K_{A3a2}}{[1 + \frac{C_3}{C_{1f}}(1 + \alpha_c - \alpha_{c_f}) + K_{A3a1}]} \frac{\gamma C_{ox} WL(1 + \alpha_{WL})}{16C_{1f}(2\Phi_f + V_b)^{3/2}} + \frac{\gamma C_{ox} WL(1 + \alpha_{WL})}{32C_{1f}(2\Phi_f + V_b)^{5/2}}$$

Therefore, the differential output of preamplifier can be expressed as:

$$v_{o3} = v_{o3+} - v_{o3-} = (d_{1f} + d_{1f}')v_i + (d_{2f} - d_{2f}')v_i^2 + (d_{3f} + d_{3f}')v_i^3 \quad (D.20)$$

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Apply a sinusoidal input $v_i = V_p \cos(\omega t)$, the second and third harmonic distortion due

to mismatch are

$$HD_2 \cong \frac{1}{2} \frac{d_{2f} - d_{2f}'}{d_{1f} + d_{1f}'} V_p \cong \frac{1}{2} \frac{a_{1f}^2 b_{1f}^2 c_{2f} - a_{1f}'^2 b_{1f}'^2 c_{2f}'}{a_{1f} b_{1f} c_{1f} + a_{1f}' b_{1f}' c_{1f}'} V_p \cong \frac{1}{4} \frac{a_{1f}^2 b_{1f}^2 c_{2f} - a_{1f}'^2 b_{1f}'^2 c_{2f}'}{a_{1f} b_{1f} c_{1f}} V_p \quad (D.21)$$

$$HD_3 \frac{1}{2} \frac{d_{3f} - d_{3f}'}{d_{1f} + d_{1f}'} V_p = \frac{1}{4} \frac{a_{1f}^3 b_{1f}^3 c_{3f} + a_{1f}'^3 b_{1f}'^3 c_{3f}'}{a_{1f} b_{1f} c_{1f} + a_{1f}' b_{1f}' c_{1f}'} V_p^2 \cong \frac{1}{4} a_{1f}^2 b_{1f}^2 \frac{c_{3f}}{c_{1f}} V_p^2 \quad (D.22)$$

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Appendix E: Process and Design Parameters

Table E.1 Process parameters used in hand calculations

NMOS Parameter	Process	Value	PMOS Parameter	Process	Value
$k_n'(\mu A/V^2)$		217	$k_p'(\mu A/V^2)$		66
$V_{thn0}(V)$		0.5 V	$V_{thp0}(V)$		0.69 V
$K1_n(V^{1/2})$		0.5	$K1_p(V^{1/2})$		0.6
$\mu_{0n}(m^2/V\text{ sec})$		$4.758*10^{-2}$	$\mu_{0p}(m^2/V\text{ sec})$		$1.482*10^{-2}$
$T_{ox}(m)$		$7.575*10^{-9}$	$T_{ox}(m)$		$7.754*10^{-9}$
P_{CLMn}		0.695	P_{CLMp}		3.184

Table E.2 Design parameters used in hand calculations

Design Parameter	PSF	NSF	CCSF	
	PMOS bulk tied to source		PSF with PMOS bulk tied to V_{dd}	NSF in CCSF
At supply $V_{dd} = 3V$				
Biasing Current	1 mA	1mA	0.1 mA	1 mA
Input Transistor (W)	500 μm	200 μm	40 μm	200 μm
Input Transistor (L_{eff})	0.49 μm	0.45 μm	0.49 μm	0.45 μm
Biasing Transistor (W)	60 μm	60 μm	10 μm	60 μm
Biasing Transistor (L_{eff})	0.49 μm	0.45 μm	0.49 μm	0.45 μm
Bulk-well Capacitance	0.25 pF	—	—	—

Appendix

Appendix F: Terminology in ADC

Analog to digital converter are characterized in a number of different ways to indicate the performance capability, cost and ease of use. Some of the most important characteristics of ADCs are introduced below.

I. Static Performance

i) Resolution

When an analog signal is digitized, it is represented by a finite number of discrete voltage levels. The resolution is the number of discrete levels that are used to represent the signal. A high resolution ADC divides the input range into a larger number of subranges than a low resolution converter. Resolution is usually defined as the base 2 logarithm of subranges the ADC input range divide into. This quantity is referred to as the number of bits resolved by the ADC. Hence, the input voltage can be expressed as:

$$V_{IN} = V_{FSR} \left(\frac{D_1}{2^1} + \frac{D_2}{2^2} + \frac{D_3}{2^3} + \dots + \frac{D_N}{2^N} \right) \quad (F.1)$$

Where V_{IN} is the input signal, V_{FSR} is the full-scale range, N is the resolution of ADC and $D_1 \dots D_N$ are the N bit digital output. Thus, for a fixed full scale input range a high resolution ADC can resolve smaller signals than a low resolution ADC is able to resolve. To more accurately replicate the analog signal, the resolution must be increased.

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ii) DNL and INL

Most ADCs are intended to have a transfer characteristic that approximates a straight line. As the resolution increase, the input-output characteristic of the ADC better approximates a straight line. The transfer characteristic for an ideal version of such an ADC progresses from low to high in a series of uniform steps. The transfer characteristic of a practical ADC steps which is not perfectly uniform and this deviation generally contributes to further nonlinearity as shown in Fig. F.1. Two kind of nonlinearities are used to characterize this deviation.

Differential nonlinearity (DNL) is defined as the difference between an actual step width and the ideal value of 1LSB ($LSB = \frac{V_{FSR}}{2^n}$). For an ideal ADC, in which the differential nonlinearity coincides with $DNL = 0LSB$, each analog step equals 1LSB and the transition values are spaced exactly 1LSB apart. DNL is specified after the static gain error has been removed. It is defined as follows:

$$DNL(LSB) = \frac{V_{D+1} - V_D}{V_{LSB}} - 1 \text{ where } 0 < D < 2^{N-2} \quad (F.2)$$

Where V_D and V_{D+1} is the physical value corresponding to the digital output code D and D+1, N is the ADC resolution, and V_{LSB} is the ideal spacing for two adjacent digital codes. As an example, when using an ADC, as the analog input voltage increases, if the next code transition occurs at a voltage 1.5 LSB away from the previous transition, the DNL error is 0.5 LSB. If it occurs at 0.5 LSB away, the DNL error is -0.5 LSB.

Integral nonlinearity (INL) is described as the deviation, in LSB or percent of full-scale range (FSR), of an actual transfer function from a straight line. The INL

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specification is measured after both static offset and gain errors have been nullified, and can be described as follows:

$$INL(LSB) = \frac{V_D - V_0}{V_{LSB}} - D \quad \text{when } 0 < D < 2^{N-1} \quad (F.3)$$

V_D is the analog value represented by the digital output code D , N is the ADC's resolution, V_0 is the minimum analog input corresponding to an all-zero output code, and V_{LSB} is the ideal spacing for two adjacent output codes.

Fig. F.1 INL and DNL

II. Dynamic Performance

i) Signal to Noise Ratio (SNR)

The signal to noise is the ratio of signal to noise floor in the output of the ADC. One way to measure SNR is to plot the spectrum of the output of the ADC. The SNR is calculated by measuring the difference between the signal peak and the noise floor. For a waveform perfectly reconstructed from digital samples, SNR is the ratio of an rms (root mean square) full-scale analog input to its rms quantization error. Actually, SNR is diminished by many noise sources in addition to quantization noise. The actual SNR for a sinusoidal input signal can therefore be described as

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$$SNR(dB) = 20 * \log_{10} \frac{A_{signal[rms]}}{A_{total_noise[rms]}} \quad (F.4)$$

where $A_{SIGNAL}[rms]$ represents the rms amplitude for the analog input signal, and $A_{TOTAL_NOISE}[rms]$ is the rms sum of all noise sources (thermal noise, quantization noise, etc.) that limit the converter's dynamic performance.

ii) SNDR

The signal to noise plus distortion ratio (SNDR) is often used to measure the degradation due to the combined effect of noise, quantization errors, and harmonic distortion. It describes the quality of an ADC's dynamic range, expressed as the ratio of the maximum amplitude output signal to the smallest increment of output signal that the converter can produce. When a sinusoidal signal of a single frequency is applied to a system, the output of the system generally contain a signal component at the input frequency. Due to distortion, the output also contains signal components at harmonics of the input signal. Furthermore, the ADC adds noise to the output, and this noise generally present to some degree at all frequencies. The SNDR of the ADC is defined as the ratio of the signal power in the fundamental to the sum of the power in all of the harmonics and noise. Mathematically, SNDR is described as

$$SNDR(dB) = 20 * \log_{10} \frac{A_{signal[rms]}}{A_{noise+HD[rms]}} \quad (F.5)$$

where $A_{SIGNAL}[rms]$ depicts the rms output signal level and $A_{NOISE+HD}[rms]$ describes the rms sum of all spectral components below the Nyquist frequency, excluding DC.

iii) spurious-free dynamic range (SFDR)

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Another way to define dynamic range is the spurious free dynamic range (SFDR). Spurious-free dynamic range is the ratio of rms amplitude of the fundamental (the maximum signal component) to the rms value of the largest distortion component in a specified frequency range. In well-designed systems, this spur should be a harmonic of the fundamental. SFDR is important because noise and harmonics restrict a data converter's dynamic range. Thus, SFDR can be expressed as:

$$SFDR(dB) = 20 * \log_{10} \frac{A_{f_{IN}[rms]}}{A_{HD_MAX[rms]}} \quad (F.6)$$

or

$$SFDR(dB) = 20 * \log_{10} \frac{A_{f_{IN}[rms]}}{A_{SPUR_MAX[rms]}} \quad (F.7)$$

where $A[f_{IN}]$ is rms value of input signal, $A_{HD_MAX}[rms]$ is the rms value of the largest-amplitude harmonic and $A_{SPUR_MAX}[rms]$ is the largest spurious signal component ($A_{SPUR_MAX}[rms]$) observed over the entire Nyquist band. The term spurious-free dynamic range is usually applied for cases in which the harmonic distortion and spurious signals are regarded as undesirable spurs in the output spectrum of a sampled pure-sinusoidal input tone.

iv) Total Harmonic Distortion (THD)

THD is the rms sum of all harmonics in the output signal's Fast Fourier Transform (FFT) spectrum. All harmonics are included by definition, but the first three (in most cases) represent the major contribution to output distortion in a given converter. In communications and RF/IF applications, THD is often a more important

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figure of merit for ADCs than are the DC-nonlinearity specifications that describe the converter's static performance. THD is given by

$$THD(dB) = 20 * \log_{10} \frac{\sqrt{A_{HD_2[rms]}^2 + A_{HD_3[rms]}^2 + \dots + A_{HD_N[rms]}^2}}{A_{fIN[rms]}} \quad (F.8)$$

where $A_{fIN[rms]}$ is the rms fundamental amplitude, and $A_{HD_2[rms]}$ through $A_{HD_N[rms]}$ represent the rms amplitudes of the 2nd to Nth-order harmonics.