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**NANYANG
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**DEVELOPMENT OF A BROADBAND TUNABLE
FILTER**

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SCHOOL OF ELECTRICAL AND ELECTRONIC
ENGINEERING
2006**

DEVELOPMENT OF A BROADBAND TUNABLE FILTER

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SUMMARY

Ultra Wide Band (UWB) wireless systems can potentially transmit hundreds of Mbits/s for wireless personal area networks. But UWB system is inherently broadband from 3 to 10 GHz, and has to co-exist with the existing systems. So filters employed at the front-end of the UWB communication systems to minimize interferences from existing narrow band systems for 3-10 GHz will be the key component in the transceiver design. To achieve both low cost and at microwave operation, SiGe/Si design is desirable.

In this project, active bandpass and active notch filters for UWB application have been designed and their performances have been investigated. For the filter design, the most important part is the resonator, which determines the frequency response of the filter. Normally the resonator is composed of inductances and capacitances. To realize frequency tuning, either the inductance or the capacitance should be tunable. So there are two ways to realize frequency tuning: using varactor or using active inductor based on the gyrator concept. Furthermore, due to dielectric losses in the SiGe substrate and the resistance of the metallization, the Quality Factor of the resonator normally is not high enough. So a Q-Enhancement circuit may be needed to maintain a high Q performance. However, by introducing the Q-Enhancement circuit, the circuit will dissipate more DC (direct current) power and hence the noise figure (NF) of the total circuit will suffer.

The bandpass filter in this work employs differential structure. And the resonators in this filter use gyrator inductors. Simulation of the current schematic

shows this filter can work over a frequency band from 2.25 GHz to 5.90 GHz, with a tunable Q-factor from 7.3 to 55.6. This filter is designed in IBM 0.25 μ m BiCMOS (Bipolar and CMOS), with the power supply of 2.5V.

Three types of notch filters are designed in this project. The first one employs differential structure, and uses varactor for frequency tuning. This filter is designed in IBM 0.25 μ m BiCMOS, with the power supply of 3.3V. The filter has been fabricated and measured.

The second notch filter is realized in differential structure. It achieves the bandstop response by reversing a bandpass resonator. Simulation of the schematic design shows this filter can work over a frequency band from 2.9 GHz to 5.9 GHz, with a tunable Q-factor from 126 to 250. This filter is designed in IBM 0.13 μ m CMOS/RF (Complementary Metal Oxide Semiconductor/Radio Frequency) process, with the power supply of 1.5V.

The third notch filter is realized in a single-end structure due to size considerations. Its basic structure is the same as the first notch filter, except that it employs a gyrator active inductor for tuning rather than a varactor. Both schematic and layout design of the filter has been completed. Post layout simulation shows this filter has a frequency tuning range from 2.8GHz to 6.0GHz with a quality factor from 45.4 to 67.0. This filter is designed in IBM 0.13 μ m CMOS/RF process, with the power supply of 1.5V.

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LIST OF ABBREVIATIONS

AC	Alternating Current
ADC	Analog-to-Digital converter
BiCMOS	Bipolar and CMOS
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
ESD	Electrostatic Discharge
ESM	Electronic Support Measures
FCC	Federal Communications Commission
FET	Field Effect Transistor
GaAs	Gallium Arsenide
IC	Integrated Circuit
IFF	Identify-friend-or-foe
IIP3	Input IP3
IM	intermodulation
IP3	third intercept point
LNA	Low Noise Amplifier
LPD	Low Probability of Detection
MEMS	Micro-Electro-Mechanical Systems
MESFET	Metal Semiconductor Field Effect Transistor
MMIC	Microwave Monolithic Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSW	Magnetostatic Wave
NF	Noise Figure
NIC	Negative Impedance Circuit
NMOS	N-channel Metal Oxide Semiconductor
OIP3	Output IP3
PCB	Printed Circuit Board
PLTS	Physical Layer Test System

List of Abbreviations

PMOS	P-channel Metal Oxide Semiconductor
PSD	Power Spectra Densities
RF	Radio Frequency
SAW	Surface Acoustic Wave
UWB	Ultra Wide Band
VNA	Vector Network Analyzer
WLAN	Wireless Local Area Network
YIG	Yttrium Iron Garnet

Chapter 1 Introduction

1.1 Motivation

Ultra Wide Band (UWB) radio is a relative new wireless RF technology developed to transfer signals at high data rate over very short distance at very low power densities. Its general features can be summarized as [1]:

- Ultra-short duration pulse and ultra-wide bandwidth.
- Ultra low power spectral densities (PSD).
- Base-band communications.
- Excellent multi-path immunity.
- Relatively simple and less costly than existing narrow-band radio systems.

Typically UWB systems may transmit and receive signals modulated by ultra-short duration pulses with long intervals between them [2]-[3], which covers a extremely wide spectrum bandwidth (from 3.1 to 10.6 GHz) [4], so that they transfer data by spreading the RF energy very narrowly over this ultra broad frequency range [2]. Moreover UWB radio is a carrier-free (base-band) technology. In UWB systems, no up/down conversion is needed, so the complexity, power, size and cost of the transceiver will be greatly reduced [5]. As a low cost and low power solution, UWB techniques can be potentially deployed into a lot of military and commercial applications, such as radar/localization, identify-friend-or-foe (IFF) systems, short range indoor communications, etc [6].

Since UWB technique is inherently broadband and covers a highly populated frequency range (from 3.1 to 10.6 GHz), it has the potential to interfere,

and be interfered, by existing narrow band wireless systems in the same band [4]. On February 2002, Federal Communications Commission (FCC) permits the operation and marketing of UWB technology but it must co-exist with existing wireless systems [4]. On the other hand, UWB radio should not be interfered by existing narrow band wireless systems; hence although there is a lot of research problems remained to be solved, such as very broad band low noise amplifier (LNA), ultra high speed, high resolution Analog-to-Digital converter (ADC), etc, the major problem of UWB systems is the interference from other existing narrow band wireless communication systems. So the front-end filter design for UWB transceiver is the most important potential problem to be attempted. Furthermore, considering the ultra broad frequency coverage of UWB radio, a front-end filter with extremely wide tuning range is desired, which makes the filter design a highly challengeable mission.

1.2 Objectives

Typically, only passive filters are employed for the front-end design in typical communication systems, due to their low loss, good linearity and high quality performances over the active devices, while the active devices have their own merits. Compared to passive circuits, active circuits have the advantages of smaller size [7], because it permits the realization of filters in MMICs (Microwave Monolithic Integrated Circuits) by replacing transmission lines and power combiners/dividers with appropriate MOSFET (Metal Oxide Semiconductor Field Effect Transistor) and BJT (Bipolar Junction Transistor) configurations and lumped RLC elements. Most of the active devices have tuning capability, which has significant importance in UWB transceivers design.

Normally front-end filters are realized in two processes: SiGe/Si and GaAs. Although SiGe/Si does not have high performance in terms of passive components, substrate loss and noise performance as compared to GaAs, the SiGe/Si process is much less expensive, and it enables a highly integrated radio frequency integrated circuit (RFIC) [8]-[9].

So in this work, the objective is targeted on design and investigation of both bandpass and bandstop microwave active tunable filters with active inductors/varactors in BiCMOS and CMOS/RF processes. A frequency tuning capability from 3.1 to 10.6GHz and a noise figure less than 3dB are required for the front-end filter performance. That is because frequency tuning is a very important aspect for UWB applications, while noise figure is the most critical requirement of the receiver front-end design. Both the gyrator active inductor and the varactor will be employed in these filters for frequency tuning. The quality factor of all these filters should be tunable, so Q-Enhancement circuits will be implemented in these filters. To improve noise figure, a low noise amplifier (LNA) may be included in the filter design. Because these filters are realized in active devices, they have poorer linearity compared to passive filters. And this will also be investigated and discussed in the work.

To fulfill the objective:

- In Chapter 3, an active inductor based on the gyrator concept and Q-Enhancement circuit is designed. The frequency tuning capability of the active inductor is investigated.

- In Chapter 4, a differential bandpass filter employing the active inductor presented in chapter 3 is designed. A LNA may be included before the filter to improve the noise performance.
- In Chapter 5, a differential bandstop filter with varactor tuning is designed. And its tuning capability is investigated and compared to the bandpass filter in Chapter 4.
- In Chapter 6, another differential bandstop filter with the active inductor presented in Chapter 3 is designed. A LNA is included in front of the notch filter to improve its noise performance.
- In Chapter 7, a single-ended bandstop filter tuning by the active inductor presented in Chapter 3 is designed and investigated. A LNA is also utilized to improve the noise figure.
- In Chapter 8, the notch filter in Chapter 5 is fabricated and tested measurement results are presented and investigated.

1.3 Major Contributions of the Thesis

In this work, an active gyrator inductor in both BJT and CMOS processes has been developed and investigated for tunable filter design. A bandpass and two notch filters are designed with this active inductor. Their performances are investigated. Another notch filter employing a varactor for frequency tuning is also designed and investigated. Furthermore, since these filters are realized in BiCMOS or CMOS process, it is inherently low cost and easy to be integrated in the transceiver system.

The major contributions of the thesis are shown below:

- An active inductor based on the gyrator concept with a tuning range from 3.1 to 6.6 GHz is designed. The tuning range is larger than the active inductor in the report works [10], [11]-[12]. Compared to the active inductor in [7] & [13], this inductor doesn't have a superior performance, but it is realized in CMOS process, which is much less expensive than the GaAs process in [7] & [13].
- Employing this active inductor, a bandpass filter in Chapter 4 and two notch filters in Chapter 6 and 7 are designed with a 3GHz plus tuning range (about 3 to 6 GHz). This tuning range is not enough for UWB system, which require a tuning range from 3.1 to 10.6GHz. However, these filters are still useful in UWB applications, since they successfully covers the frequency band of WLAN (wireless local area network), the largest interference jamming the UWB radio.
- By utilizing a LNA stage before the filter, the bandpass filter in Chapter 4 achieves a noise figure less than 3dB, which satisfies the minimum requirement of the UWB receiver.
- The notch filter in Chapter 7 has a 4 to 5 dB noise figure. This result may not be enough for UWB applications but still better than lots of report works (see in Table 2.1).
- The notch filter in Chapter 5 has a promising simulation results. Its frequency tuning range and noise figure is comparable to the notch filters reported in [7] and [14]. But this work is realized in a much cheaper solution: BiCMOS instead of the expensive GaAs.

1.4 Organization of the Thesis

This thesis is organized into eight chapters.

Chapter 1 Introduction provides an introduction to the motivation, objective and contribution of this work and an outline of the thesis.

Chapter 2 Literature Review provides some background on the UWB techniques, the tunable microwave filters, the active inductors and the Q-Enhancement circuits. Then the proposed filter structures are described.

Chapter 3 Simulation Studies on Active Inductor describes the theory, circuit design and simulation results of the proposed active inductor and Q-Enhancement circuit.

Chapter 4 Bandpass Filter Based on Active Inductor presents the circuit design of the bandpass filter. It shows the basic structure of the filter and their functions, respectively. It also presents the simulation results.

Chapter 5 Simulation Studies on Notch Filter 1 with Varactor Tuning presents a differential notch filter with varactor tuning. The schematic design, layout design, and post layout simulation results are presented.

Chapter 6 Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure describes another differential notch filter employing the

active inductor for frequency tuning. Both the schematic design and the simulation results are presented.

Chapter 7 Simulation Studies on Notch Filter 3 with Bias Tuning of Single-ended Structure presents a single-ended notch filter employing the active inductor for frequency tuning. Both schematic design and layout design are performed. Post layout simulation results are presented.

Chapter 8 Notch Filter – Fabrication and Measured Results presents the testing setup and measured results of Notch Filter 1 presented in Chapter 5, which has been fabricated and measured.

Chapter 9 Conclusions and Recommendations acts as a conclusion to the whole Meng thesis project. Difficulties encountered in this project and suggestions for future research on this subject are presented.

Chapter 2 Literature Review

This chapter serves as an introduction to the technology background of this work. It provides a literature review on the UWB techniques, the tunable microwave filters, the active inductors and the Q-Enhancement circuits.

2.1 Ultra Wide Band (UWB) Technology/Communications

UWB is a wireless technology involving transmitting, receiving and processing of very broad bandwidth microwave frequency signals. Compared to most of other wireless technologies, which use a single frequency signal as a carrier, UWB technology transmit and receive signals modulated by short pulses with long intervals between them to avoid interference to existing users. The major advantage of UWB technology lies in its ability of transmitting and receiving signals at very high data rates over short distance at low power density with a relatively simple and low cost transceiver structure. The UWB communication systems are expected to work in the 3.1 to 10.6 GHz band.

Although often considered a recent breakthrough in broad-band wireless technology, the concept of Ultra Wide Band has a history of more than 40 years. This technology first came out in the early 1960s on time-domain electromagnetics [15]. In their early ages, the UWB systems are designed for low probability of detection (LPD) radar, and communication systems. But at that time, the UWB systems are only limited to military and government usage, until February 2002, Federal Communications Commission (FCC) has adopted the first report and order which permits the commercial operation and marketing of UWB technology. Moreover, in its recent UWB report and order, FCC has promulgated a broad definition

for UWB communication technology: 20% fractional or minimum 500MHz bandwidth regardless modulation strategies and communication types.

2.2 Microwave Filters

Tunable microwave filters can be realized by many methods, but whatever the tuning techniques may be, the frequency variation is accomplished by varying the inductive or the capacitive loading of the resonators. For most of tunable microwave filters, there are three basic types (Fig. 2.1): mechanically tunable, magnetically tunable, and electronically tunable filters. They will be discussed separately in the following sections.

Fig. 2.1: Tree Structure of Main Types of Microwave Filters

2.2.1 Mechanically Tunable Filters

Normally there are two types of mechanically tunable filters. The first one is the coaxial mechanically tunable filters, which realizes the tuning by sliding an inner conductor back and forth [16, pp. 1013]. The other one is the waveguide mechanically tunable filters, the side walls of which can be moved to realize the frequency tuning [16, pp. 1020]. Examples of the mechanically tunable filters are presented in [17], [18] and [19]. The filter in [18] operates below 1 GHz, while the

one in [19] can work at 36GHz with a tuning range over a 25% bandwidth. Mechanically tunable filters have large power handling capability and low insertion loss, so they are often employed in long distance communication or radar systems [20], but their tuning speed is very low, and their size is too large to be integrated into modern transceiver systems.

2.2.2 Magnetically Tunable Filters

Magnetically tunable filters include yttrium iron garnet (YIG) filters, magnetostatic wave filters, evanescent waveguide filters and printed E-plane filters [20].

YIG filters normally employ single-crystal YIG spheres or other low loss ferrites ($(\text{LiFe})_{0.5}\text{Fe}_2\text{O}_4$ or barium ferrites) in their resonators [20]. This type of filters has multioctave tuning range, very high selectivity, spurious-free response and compact size [20]. Another advantage of YIG filters is that, if the anisotropy effects are neglected, the center frequency for a given shape of the resonator has no relationship with its size, and is only determined by the bias magnetic field [20]. However the YIG filters only have moderate tuning speed, normally below some milliseconds/GHz. Examples of this type of filter are shown in [21], [22] and [23]. The filter reported in [23] can be tuned from 50GHz to 75GHz with a 6dB insertion loss.

Magnetostatic wave (MSW) filters are realized by thin YIG films grown by liquid phase epitaxy on gadolinium gallium garnet substrates [20]. The bandwidth of this type of filters is usually very narrow (0.1% ~1%) and their insertion loss

normally is very high (20~30dB) [20]. However, recently low insertion loss MSW filters has been reported. The bandpass MSW filters reported in [23] has an insertion loss about 10dB. This filter has a tuning range from 3 to 7GHz with a bandwidth around 30~50MHz.

The major problem of evanescent waveguide filters is their poor power handling capability, normally lower than 200mW [20]. Higher power signals will degrade the filter performance. One method to solve this problem is to design a filter operating in off-resonance region [20]. The example of this type filters are reported in [24] and [25]. The filter reported in [24] is a three-section filter operating at off-resonance region. It can operate between 8 to 12GHz with a 300MHz tuning range. In [25], a five pole filter designed in resonant below-cutoff waveguide is reported. The filter has a tuning range from 8.4 to 9.2GHz.

There is a well-known theory that the resonant frequency of a resonator partially loaded with ferrite can be tuned by varying the bias magnetic field. The printed E-plane filters are realized based on the above theory [20]. This type of filters has low insertion loss and high power handling capability, and they can be applied into communication systems, radar and navigation systems. There are also some drawbacks of this type of filters [20]. First, there should be an absence of ferrite of loading in the coupling sections, otherwise the stop band will be narrow and the bandwidth varies dramatically. Second, all air gaps between ferrite and waveguide narrow wall must be considered for evaluating the eigenvalue problem, otherwise a serious error in the computation of resonator eigenvectors will occur. Third, some criteria for the choice of suitable ferrite material and DC bias field are

required for high power handling capability. Finally, the millimeter-wave filter design requires very high accuracy in fabrications of the filter, while when the frequency goes above 40GHz, the ferrite slabs are too thin and brittle to be handled safely. Two examples of E-plane filter have been reported in [26] and [27]. The filter in [26] has a center frequency of 15GHz, and the other one in [27] can operate beyond 30GHz.

There is a common drawback of all the magnetically tunable filters: the size of them is too large and it is very difficult to integrate these filters into the modern transceiver systems.

2.2.3 Electronically Tunable Filters

Electronically tunable filters have a very fast tuning speed (about 1GHz/s) over a wide (an octave) tuning range, and they have a compact size [20]. They have been widely applied in electronic support measures (ESM) receivers [20]. Basically there are two types of electronically tunable filters. The first type of the electronically tunable filters is fabricated using transmission lines (microstrip, coplanar waveguide and etc.) for filter structures and either RF varactors or the MEMS (Micro-Electro-Mechanical Systems) capacitance switches for frequency tuning. Examples of this type of filters are reported in [28]-[32]. The filters in [28] and [29] realize the frequency tuning by employing varactors. The filter in [28] can be tuned from 700MHz to 1.33GHz, while the one in [29] can be tuned from 18.6GHz to 21.4GHz, with a constant fractional bandwidth of $7.4 \pm 0.1\%$ and a mid-band insertion loss of 3.85 to 4.15dB. In [30] a tunable combline filters using GaAs FETs in cold configuration as tuning devices are described. By varying the

bias voltage of the GaAs FETs, the equivalent capacitance of the FETs can be changed. The tuning range achieved for this filter is from 8.0GHz to 12.0GHz. The filters described in [31] and [32] achieve their tunable performance by using the MEMS switches as tuning devices. The filter in [31] can be tuned from 812MHz to 1752MHz, while the one in [32] has a tuning range from 16.5GHz to 22GHz.

The second type of the electronically tunable filters is totally different from the former one in their basic filter structures. Appropriate MOSFET and BJT configurations and lumped RLC elements are employed to construct this type of filters, instead of transmission line structures. Although limited by the transition frequency f_T and other parasitics due to the process, the achievable operating frequency of this type of filters is much lower than the former ones (normally below 5~6GHz), they still draw a lot of attentions due to their much smaller size. Another problem associated with these filters is their poor linearity. That is because both varactors and active inductors are nonlinear circuits.

For the second type of the electronically tunable filters, there are basically two strategies to realize frequency tuning: using varactors [7] and [33]-[36], or using active inductors [10]-[12] and [37]. Some design examples are summarized in Table 2.1. Some of the filters in Table 2.1 are realized with GaAs MESFET (Metal Semiconductor Field Effect Transistor) [11], [12], [33], [36]. Their center frequency of operation band can go as high as 11GHz [33]. However, the low cost solutions: BiCMOS and CMOS process also show their potential in microwave filter design [10], [35], & [37]-[39]. But the center frequency achieved is much lower, around 2GHz only [35] & [39]. Obviously, it is too low for UWB

communication systems. On the other hand, their noise performance is not good enough and their tuning range is quite limited.

For active radio frequency circuit design, bipolar junction transistor (BJT) looks more suitable, because normally BJT has smaller size (capacitance) and larger transconductance per unit current; that is to say: BJT is faster than the MOSFET for the same size. However, MOS transistor has better linearity than BJT transistor. There are two reasons. First, C_π of the bipolar transistor is comprised of the base-charging capacitance C_b and the emitter-base depletion layer capacitance C_{je} [40, pp. 33]. Both C_b and C_{je} are voltage dependent. While for MOSFET C_{gs} , C_{gd} and C_{gb} is oxide capacitance, which is signal independent. Although C_{sb} and C_{db} of MOSFET is also junction capacitance and signal dependant, they have much less importance than C_{gs} and C_{gd} . On the other hand, for MOSFET, the small signal drain current [40, pp. 51] is:

$$i_d = k' \frac{W}{L} (V_{GS} - V_t) v_i + \frac{k'}{2} \frac{W}{L} v_i^2 \quad (2.1)$$

where

$$k' = u_n C_{ox} \quad (2.2)$$

(In Eqn. (2.1), W and L are the width and length of the MOS transistor respectively. V_{GS} is the DC (Direct Current) bias gate source voltage, while V_t is the threshold voltage of the transistor. In Eqn. (2.2), u_n is the average electron mobility in the channel, and C_{ox} is the gate oxide capacitance per unit area.) While the small signal collector current of BJT [40, pp. 28] is:

$$i_c = \frac{I_C}{V_T} v_i + \frac{1}{2} \frac{I_C}{V_T^2} v_i^2 + \frac{1}{6} \frac{I_C}{V_T^3} v_i^3 + \dots \quad (2.3)$$

(In Eqn. (2.3), I_c is the collector DC bias current, and V_T is the thermal voltage.) Comparing Eqn. (2.1) and (2.3), it is easy to find that i_d only contains first order and second order components of small signal input voltage v_i , while i_c contains all of the higher order items other than v_i and v_i^2 . So the relationship between i_d and v_i is more linear than that between the i_c and v_i . Therefore, although BJT is faster than MOS transistor, CMOS process provides a solution with better linearity.

Table 2.1 Filter performance in other publications

Ref.	Filter type	Process	Center frequency (GHz)	Q factor	Rejection Bandwidth at -10dB	Noise figure (dB)	Power Gain (dB)	DC power (mW)
[10]	Bandpass	AMS 0.35 μ m	0.72~1.03	5~75	N.A.		20	12
[38]	Bandpass	CMOS 0.8 μ m	0.869~0.893	30	N.A.	6.0	17	78
[37]	Bandpass	CMOS 0.5 μ m	1.68	19~250	N.A.	5.5	31.4 ¹	24.3
[35]	Bandpass	CMOS 0.35 μ m	1.93~2.19	20~170	N.A.			5.2
[39]	Bandpass	Bipolar	1.6~2	3~350	N.A.		7	24.36
[36]	Bandpass	GaAs	3.6~4	90~100	N.A.	19		
[11]	Notch	GaAs	1.7~2.1		50MHz		-30	
[12]	Notch	GaAs	0.625~2	10			<-45	
[33]	Notch	GaAs	8.5~11		60MHz	5	-30	

1: Voltage gain

2.3 Active Inductors

For the active tunable filter design, the active inductor plays a very important role. In recent years, much effort has been put into the area of active inductor research. Normally, active inductor can be realized by two methods: series or parallel resonators. One type of series active inductor is introduced by [41]. It is constructed by a transistor with feedback impedance between its drain and gate, as shown in Fig. 2.2. After a simple analysis, it is found out that (In this

chapter, to simplify the analysis, it is assumed that all the transistors only consist of the gate source capacitor C_{gs} and the voltage control current source related to g_m):

$$Z_{in} = \frac{1 + j\omega C_{gs} Z}{g_m + j\omega C_{gs}} \quad (2.4)$$

And if $g_m \gg j\omega C_{gs}$ ($\omega_T = \sqrt{\frac{g_m}{C_{gs}}} \gg \omega$), Eqn. (2.4) can be changed to:

$$Z_{in} = \frac{1 + j\omega C_{gs} Z}{g_m} \quad (2.5)$$

If a resistive feedback is applied in Fig. 2.2 ($Z = R$), Eqn. (2.5) will be changed to:

$$Z_{in} = \frac{1}{g_m} + \frac{j\omega C_{gs} R}{g_m} \quad (2.6)$$

Then the active inductor in [41] can be modeled as an inductor in series with a resistor.

Fig. 2.2: Active Inductor in [41] and its Small Signal Model

The main problem of this type of active inductors is its poor quality due to the real part of $1/g_m$ in Eqn. (2.6). To improve the quality factor of this type of active inductors, the resistive feedback in Fig.2.2 may be replaced by a resistor in

series with an inductor ($Z = R + j\omega L$), then Eqn. (2.5) becomes:

$$Z_{in} = \frac{1 - \omega^2 LC_{gs}}{g_m} + \frac{j\omega C_{gs} R}{g_m} \quad (2.7)$$

A negative real part will be generated to improve the quality of the active inductor, but this negative real part is frequency dependent and not suitable for broadband designs. Furthermore, active inductors in parallel structure are more convenient to be implemented into the filter design, so only parallel active inductors will be utilized in this work. Therefore, the series active inductor presented in [25] is not suitable in this project, and in the following paragraphs, only the active inductors in parallel configurations will be focused.

Fig. 2.3: Active Inductor in [10] (NMOS and PMOS)

In [10], a simple active inductor is proposed. As shown in Fig. 2.3, this active inductor can be realized by NMOS (left) or PMOS (right). Whether it is designed by NMOS or PMOS, the equivalent small signal models and their

analysis are the same. The equivalent small signal circuit of this active inductor is shown in Fig. 2.4. In Fig. 2.4, C_1 and C_2 represent the gate source capacitors of M_1 and M_2 respectively, g_{m1} and g_{m2} are the transconductance of M_1 and M_2 , and v_1 and v_2 are the small signal voltage across C_1 and C_2 .

Fig. 2.4: Equivalent Small Signal Circuits for the Active Inductor in [10]

According to Fig. 2.4:

$$y_{in} = \frac{g_{m1}g_{m2}}{j\omega C_1} + j\omega C_2 + g_{m2} \quad (2.8)$$

So the active inductor can be modeled as a parallel resonator comprised of

$C = C_2$ and $L = \frac{C_1}{g_{m1}g_{m2}}$ with a parasitic resistor $R = \frac{1}{g_{m2}}$. The main drawback of

this inductor is its poor quality due to the existence of the real part g_{m2} in Eqn. (2.8), which will downgrade the filter quality factor, when utilized.

In [42] and [43], another active inductor is presented. This active inductor and its equivalent small signal circuit are shown in Fig. 2.5. And according to Fig. 2.5:

$$y_{in} = j\omega C_1 + \frac{(g_{m3} + j\omega C_3)g_{m1}g_{m2}}{(g_{m2} + j\omega C_2)j\omega C_3} \quad (2.9)$$

If carefully selecting transistors size and their bias currents, so that

$$g_{m2} + j\omega C_2 = g_{m3} + j\omega C_3 \quad (2.10)$$

Eqn. (2.9) is changed to:

$$y_{in} = j\omega C_1 + \frac{g_{m1}g_{m2}}{j\omega C_3} \quad (2.11)$$

Then it is obvious, that the circuit in Fig. 2.5 is not only inductive but also a lossless parallel resonator, as long as Eqn. (2.10) is satisfied.

Fig. 2.5: Active Inductor in [42] and its Equivalent Small Signal Circuit

There are two main drawbacks of the active inductor reported in [42] and [43]. First, the inductive behavior of this inductor is certified by Eqn. (2.10). However, in most of practical applications, Eqn. (2.10) can not be satisfied ideally, due to the unavoidable parasitics and the mismatch between M_2 and M_3 . Second, parasitic capacitance introduced by the current sources I_1 and I_2 must be taken into consideration. In Fig. 2.5, only the capacitance of I_2 can be absorbed by C_1 , while

the capacitance of I_1 can't be absorbed by any individual capacitor. If the capacitance of I_1 is assumed to be C_p , then the small signal equivalent circuit in Fig. 2.5 can be revised as shown in Fig. 2.6. And Eqn. (2.9) is changed to:

$$y_{in} = j\omega(C_1 + \frac{C_3 C_p}{C_3 + C_p}) + \frac{(g_{m3} + j\omega C_3)g_{m1}g_{m2}}{(g_{m2} + j\omega C_2)j\omega(C_3 + C_p)} + \frac{C_p}{C_p + C_3} g_{m3} \quad (2.12)$$

If Eqn. (2.10) is satisfied, Eqn. (2.12) is changed to:

$$y_{in} = j\omega(C_1 + \frac{C_3 C_p}{C_3 + C_p}) + \frac{g_{m1}g_{m2}}{j\omega(C_3 + C_p)} + \frac{C_p}{C_p + C_3} g_{m3} \quad (2.13)$$

Fig. 2.6: Revised Small Signal Model of the Active Inductor in [42]

Comparing Eqn. (2.11) and Eqn. (2.13), it is obvious that not only the self-resonant frequency of the resonator is decreased with the existence of C_p , but also a real part of $\frac{C_p}{C_p + C_3} g_{m3}$ is presented, which will degrade the quality factor of the active inductor.

Another broad band floating active inductor is reported in [44]. Because

this work only requires grounded active inductors, the active inductor reported in [44] is revised to a grounded active inductor shown in Fig. 2.7. Its small signal equivalent circuit is shown in Fig. 2.8.

Fig. 2.7: Active Inductor in [44]

By the analysis in Chapter 3, it is found out:

$$y_{in} = (1 - \frac{g_{m1}C_2}{C_1g_{m2}})g_{m3} + \frac{g_{m1}g_{m3}}{j\omega C_1} + j\omega C_3 \quad (2.14)$$

So the active inductor of [44] is also a parallel resonator.

Although for the active inductor of [44], there is also a real part in Eqn. (2.5), this real part can be canceled by making

$$g_{m1} = g_{m2} \text{ and } C_1 = C_2 \quad (2.15)$$

If Eqn. (2.15) is satisfied, Eqn. (2.14) is changed to:

$$y_{in} = \frac{g_{m1}g_{m3}}{j\omega C_1} + j\omega C_3 \quad (2.16)$$

Then a lossless active inductor is realized.

Fig. 2.8: Equivalent Small Signal Circuit of the Active Inductor in [44]

Compared to the active inductor reported in [42] and [43], failure to satisfy Eqn. (2.15) will only degrade the quality of the active inductor and has no influence on its inductance behavior. Moreover the parasitic capacitance introduced by current source I_1 and I_2 can be easily absorbed by C_3 and C_1 respectively, so they will not degrade the inductor quality factor and will only function as additional parasitic capacitances in parallel with the active inductor and reduce the self-resonant frequency of this active inductor.

From the above comparison of the several active inductors, it is found that the active inductor in [44] is the best one, and it will be utilized in this work.

2.4 Negative Impedance Circuit (NIC)

Microwave tunable filters normally employ negative impedance circuit (NIC) for quality factor control. Typically, NIC is realized by feedback structures. Two examples of NIC are reported in [34], they are shown in Fig. 2.9 and 2.10.

Fig. 2.9 (a)

Fig. 2.9 (b)

Fig. 2.9 (a): The NIC in [34] and (b): its Small Signal Model

Analysis of Fig. 2.9 shows:

$$y_{in} = j\omega C_1 - \frac{g_{m1}g_{m2}}{\frac{1}{R} + j\omega C_2} \quad (2.17)$$

If $R \ll \frac{1}{j\omega C_2}$, Eqn. (2.17) is changed to:

$$y_{in} = j\omega C_1 - g_{m1}g_{m2}R \quad (2.18)$$

Then a NIC circuit paralleled with a capacitor is achieved. The main problem of this type of NICs is that the R required is too small (typically 10 to 15ohm, because $R \ll \frac{1}{j\omega C_2}$ must be satisfied.) for microwave application. The small

value of R will consume more DC power and limit the negative conductance it can provide.

Another NIC circuit is shown in Fig. 2.10, and its admittance is:

$$y_{in} = \frac{j\omega C_2 - \frac{g_{m1}g_{m2}R_3}{1 + g_{m1}R_1 + j\omega C_1(R_1 + R_3)}}{1 + (g_{m2} + j\omega C_2)R_2} \quad (2.19)$$

Assume $g_m \gg j\omega C$, $g_m R \gg 1$ and R_1 is comparable to R_3 , Eqn. (2.19) is changed to:

$$y_{in} = \frac{-g_{m1}g_{m2}R_3}{(1 + g_{m1}R_1)(1 + g_{m2}R_2)} \approx \frac{-R_3}{R_1R_2} \quad (2.20)$$

Then the value of this NIC is only dependent on the resistors and independent on the transconductance of the transistors. So this type of NICs only provides fixed negative impedance, and the tuning is not available. However, in our applications, tuning of the NIC is very important, so it is not suitable to our design.

Fig. 2.10: The other NIC in [34] and its Small Signal Model

One more NIC is reported in [45], but its structure and analysis is just similar as the one in Fig. 2.10. In [46] several NICs are provided with very simple feedback structures. But their negative real parts are strongly frequency dependent, which makes it not suitable for broadband applications, such as UWB systems. Furthermore, their single-ended structures suffer from noise and interference coupled by power supplies and substrates, and they normally have higher even order distortions compared to their balanced counterparts [46].

In this work, a balanced NIC reported in [10], [38] and [46] is utilized. This NIC is shown in Fig. 2.11, and its admittance is:

$$y_{in} = -\frac{1}{2}g_m + \frac{1}{2}j\omega C_{gs} \quad (2.21)$$

This type of NICs has two advantages: first, its negative real part is frequency independent; second, its negative real part can be easily controlled by varying its bias currents, which make it a good choice for UWB or other broadband applications.

Fig. 2.11: Balanced NIC in [10] and its Small Signal Model

2.5 Motivation

All the three types of the microwave tunable filters have been analyzed and discussed above. The main problem of mechanically and magnetically tunable filters is their large sizes, so that they can't be integrated into modern transceiver systems. While for electronic tunable filters, the main problem is their poor performance. As presented in Table 2.1, the active filter realized by BiCMOS and CMOS process only can achieve a center frequency at about 2GHz with a several hundred MHz tuning range [35] & [37]. Although the filter realized by GaAs and transmission line structures have better performance: a center frequency at several GHz with a tuning range up to 2.5GHz [33], its tuning range is still not broad enough for UWB applications, and also, this type of filters is more costly and not easy to be integrated into modern transceiver systems.

In this work (UWB application), the filters designed by BiCMOS and CMOS/RF process are selected. The BiCMOS and CMOS/RF process provides a low cost solution. This type of design can be easily integrated into existing transceiver systems. A lot of examples of this type of filter have been proposed in [10], [35], and [37]-[39], but there are still many problems remain unsolved. First is to improve the tuning range of the filters. UWB requires a tuning range from about 3GHz to 10GHz, while the published works only have a tuning range of several hundred MHz. Second is to improve the noise figure of the filters. UWB requires a maximum 3dB noise figure for front-end filters; however, the presented filters only can achieve a minimum noise figure at about 5 to 6dB, as shown in Table 2.1.

2.6 Proposed Filter Configurations

This work proposed one bandpass filter and three bandstop filters. The bandpass filter is designed in differential structure, as presented in Fig. 2.12. The filter structure is an amplifier loaded by the active inductors and negative impedance circuit. Similar design in reference [10], [35], and [38] shows a tuning range of several hundred MHz. However, with a better active inductor, this design may be able to achieve a tuning range of about 3 GHz, a very important improvement for UWB applications. A LNA stage is provided in front of the filter to improve its noise performance and input matching to meet the requirement of the UWB systems. At the output of the filter, a buffer is designed to improve its output matching.

Fig. 2.12: Basic Configuration of the Bandpass Filter

As stated in Chapter 1, a very critical problem faced by UWB systems is the interferences generated by other narrow band communication systems, such as WLAN. Hence the bandstop filters is very useful for UWB radio. So the design and investigation of notch filters will also be performed in this project.

The first notch filter is realized in emitter degeneration structure, as shown in Fig. 2.13. According to [14] and [33], this type of filter is expected to achieve a frequency tuning range $>2\text{GHz}$ and a noise figure about 5dB. These results are still not enough for UWB applications, but great improvement will be achieved compared to reported works summarized in Table 2.1. In this filter, varactor is employed for frequency tuning to investigate the difference in tuning capability of the varactor and the gyrator inductor. The main problem of this structure is its poor input matching due to the capacitive loading at the emitters of Q_1 and Q_2 .

Fig. 2.13: Basic Structure of Notch Filter 1

Emitter degeneration for BJTs (also called source degeneration for MOSFETs) is defined as a structure which is composed of some impedance connected in series with the emitter of a BJT transistor [40, pp. 198-200], as illustrated in Fig. 2.14.

Fig. 2.14(a): Emitter Degeneration

Fig. 2.14(b): Source Degeneration

Because the first notch filter has the problem of its poor input matching, another notch filter (Notch Filter 2) with different structure is designed. As presented in Fig. 2.15, this filter realizes the bandstop function by reversing a bandpass response. Since the resonator now is located at the drain of the input transistors, a better input matching ($< -10\text{dB}$) is expected to meet the requirement of UWB applications. A LNA stage is employed to improve the noise performance. Notch Filter 2 is designed in CMOS process to further reduce the cost. Because varactor tuning scheme requires a large voltage tuning range (in this case even larger than the supply voltage, which will be stated in Chapter 5), the varactor tuning structure is not suitable to low power, low voltage systems, especially the portable devices of UWB communication systems. Hence, a gyrator active inductor is utilized for frequency tuning in this notch filter. The active inductor used in Notch Filter 2 has the same structure as the one employed in the bandpass filter, except that all the BJT transistors are replaced by their CMOS counterparts. With this active inductor, a frequency tuning range about 3GHz is expected, which is an important improvement for UWB applications, compared to existing notch filters summarized in Table 2.1.

Fig. 2.16: Fundamental Structure of Notch Filter 3

2.7 Conclusions

In this chapter, a brief overview on UWB radio, microwave tunable filters, active inductors and Q-Enhancement circuits (negative impedance circuits) was presented. Three types of microwave tunable filters were introduced, discussed and compared. Some published active inductors and Q-Enhancement circuits were reviewed and investigated. Finally, the proposed filter structures were presented.

In this project, microwave tunable filters design in BiCMOS/CMOS process is focused, which is relatively low cost and enables a highly integration of

Literature Review

the transceiver systems. The detailed filter designs will be presented in the following chapters.

Chapter 3 Simulation Studies on Active Inductor

3.1 Introduction

The shortcomings of the passive on-chip inductor mainly lie in the larger area occupied and poor quality factor due to resistive loss and capacitive coupling to the substrate [15]. So in this work, filters are designed by active inductors, in which the inductive behavior is realized through combination of several active and passive components.

In this chapter the design of an active inductor based on gyrator concept is presented. The inductance of the active inductor can be easily controlled by tuning its bias current. And a Q-Enhancement circuit to control the quality factor of the active inductor will also be presented. Their simulation results will be analyzed and discussed.

3.2 Theory

3.2.1 Gyrator

Active inductors can be realized by gyrator concept [47, pp. 130-132]. The basic structure of a gyrator is shown in Fig. 3.1. The relationships between the voltage and current between the two ports are:

$$I_1 = G_{m1}V_2 \quad (3.1)$$

$$I_2 = -G_{m2}V_1. \quad (3.2)$$

Then if the port 2 is connected with an arbitrary impedance Z , then

$$Z_1 = \frac{V_1}{I_1} = \frac{V_1}{G_{m1}V_2}. \quad (3.3)$$

Since

$$-G_{m2}V_1 = I_2 = -\frac{V_2}{Z}, \quad (3.4)$$

$$\frac{V_1}{V_2} = \frac{1}{G_{m2}Z}. \quad (3.5)$$

Substitute Eqn. (3.5) into Eqn. (3.3), then

$$Z_1 = \frac{1}{G_{m1}G_{m2}Z}. \quad (3.6)$$

If Z is a capacitor and $Z = \frac{1}{j\omega C}$, Eqn. (3.6) changes to

$$Z_1 = \frac{j\omega C}{G_{m1}G_{m2}} \quad (3.7)$$

Then the inductive behavior is clear at a glance, and the inductance equals to $\frac{C}{G_{m1}G_{m2}}$. So the capacitive loading Z has been converted to an inductive loading by G_{m1} and G_{m2} .

Fig. 3.1: Gyrator

3.2.2 Active Inductor

As stated in Chapter 2, the active inductor employed in this design has been presented in Fig 2.7. Here we redraw the active inductor and its equivalent small

circuit model in Fig. 3.2 and Fig. 3.3. As Shown in Fig. 3.2, this active inductor is constructed by a NMOS (N-channel Metal Oxide Semiconductor) cascade stage (M_1 and M_2) connected with a PMOS (P-channel Metal Oxide Semiconductor) common gate stage (M_3) as a negative feedback. Two current sources (I_1 and I_2) are employed in this design. By tuning the current flowing through them, the inductance value can be easily controlled.

Fig. 3.2: Active Inductor

Ideally, the current sources are supposed to possess infinite output impedance without any other parasitics, but in practical implementation, current sources normally possess finite impedance and will contribute some parasitic

capacitance to the design, which will downgrade the performance of the active inductor, as mentioned later.

The small signal equivalent circuit of the active inductor is shown in Fig. 3.3. To simplify the analysis, the parasitic effects due to the current sources will be ignored and the transistor is assumed only comprised of a C_{gs} and a voltage control current source denoted by g_m . Other parasitic effects will be taken into account later. In Fig. 3.3, the C_1 , C_2 , and C_3 represent the C_{gs} of M_1 , M_2 , and M_3 respectively. And v_1 , v_2 and v_3 represent the small signal voltage across C_1 , C_2 and C_3 respectively.

Fig. 3.3: Equivalent small signal circuit of the Active Inductor

By a careful observation of Fig. 3.3, following equations can be written:

$$v_3 = -v \quad (3.8)$$

$$v_2 = -(g_{m2}v_2 - g_{m1}v_1) \frac{1}{j\omega C_2} \quad (3.9)$$

$$v_1 = -g_{m3}v_3 \frac{1}{j\omega C_1} \quad (3.10)$$

$$i = -j\omega C_3 v_3 + g_{m2} v_2 - g_{m3} v_3. \quad (3.11)$$

Rearrange Eqn (3.9):

$$v_2 (g_{m2} + j\omega C_2) = g_{m1} v_1. \quad (3.12)$$

Substitute Eqn. (3.8) and Eqn. (3.10) into Eqn. (3.12), then:

$$v_2 (g_{m2} + j\omega C_2) = g_{m1} g_{m3} v \frac{1}{j\omega C_1}. \quad (3.13)$$

So:

$$v_2 = \frac{g_{m1} g_{m3} v}{j\omega C_1 (g_{m2} + j\omega C_2)}. \quad (3.14)$$

Substitute Eqn. (3.8) and Eqn (3.14) into Eqn. (3.11), then:

$$i = \frac{g_{m1} g_{m2} g_{m3} v}{j\omega C_1 (g_{m2} + j\omega C_2)} + g_{m3} v + j\omega C_3 v. \quad (3.15)$$

So the admittance Y of the inductor is:

$$y_{in} = \frac{i}{v} = \frac{g_{m1} g_{m2} g_{m3}}{j\omega C_1 (g_{m2} + j\omega C_2)} + g_{m3} + j\omega C_3. \quad (3.16)$$

$$y_{in} = \frac{g_{m1} g_{m2} g_{m3} (g_{m2} - j\omega C_2)}{j\omega C_1 (g_{m2} + j\omega C_2) (g_{m2} - j\omega C_2)} + g_{m3} + j\omega C_3. \quad (3.17)$$

$$y_{in} = \frac{g_{m1} g_{m2}^2 g_{m3}}{j\omega C_1 (g_{m2}^2 + \omega^2 C_2^2)} - \frac{j\omega C_2 g_{m1} g_{m2} g_{m3}}{j\omega C_1 (g_{m2}^2 + \omega^2 C_2^2)} + g_{m3} + j\omega C_3. \quad (3.18)$$

Assume $g_{m2}^2 \gg \omega^2 C_2^2$ ($\omega_{T2}^2 = \frac{g_{m2}^2}{C_2^2} \gg \omega^2$), Eqn. (3.18) is changed to:

$$y_{in} = (1 - \frac{g_{m1} C_2}{C_1 g_{m2}}) g_{m3} + \frac{g_{m1} g_{m3}}{j\omega C_1} + j\omega C_3. \quad (3.19)$$

As shown in Eqn. (3.19), the active inductor presented here is actually a parallel resonator. The first part of Eqn. (3.19) is the real part of the active inductor. If the transistors M_1 and M_2 have the same size and identical bias current, the conductance of the active inductor reaches zero, so the Q factor is infinite. But

unfortunately, due to some second order effects and the parasitics, normally it is not the case. So a tunable Q-Enhancement circuit may still be unavoidable. The second part is the resulting inductance:

$$L = \frac{C_1}{g_{m1}g_{m3}}. \quad (3.20)$$

According to Eqn (3.20), it is convenient to tune the inductance by control the bias current of M_1 and M_3 . It also shows how the gyrator functions: the inductance is realized by converting the C_1 through M_1 and M_3 . The last part: C_3 is the capacitor in parallel with the inductor, which limits the self resonant frequency of the inductor. From Eqn. (3.19) the self resonant frequency of the active inductor is:

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m3}}{C_1C_3}} = \sqrt{\omega_{T1}\omega_{T3}}. \quad (3.21)$$

where $\omega_{T1} = \frac{g_{m1}}{C_1}$ and $\omega_{T3} = \frac{g_{m3}}{C_3}$.

Now let's consider the effect of other parasitics mentioned before. The existence of the current sources will generate additional parasitic capacitors in parallel with the inductor. The current source I_1 adds a capacitor in parallel with C_3 , while I_2 adds another one in parallel with C_1 . These caps will degrade the maximum tuning range and the highest center frequency achievable. Furthermore, the finite output impedance of the current sources will function as a resistor in parallel with the inductor, which will downgrade the quality factor of the active inductor. As shown in Fig. 3.3, the output resistance of the transistors, r_o , is ignored. But in fact, r_o does have influence on the inductor behavior. The effect of r_o can be viewed as an equivalent resistor in parallel with the active inductor. Higher resonation frequency requires larger bias current of the active inductor and

will result in a smaller output resistance r_o and a lower quality factor, since r_o is inverse proportional to the bias current [48, pp. 31]. Hence, more bias current is required for the Q-Enhancement circuit at higher operating frequency.

3.2.3 Q-Enhancement Circuit

As mentioned before, the active inductor designed in this work requires a Q-Enhancement circuit to improve its quality factor. The basic principle of Q improvement is to add negative impedance in parallel with the resonators. Assume the conductance of the existing resistor R is G_p , and the conductance of the negative impedance is $-G_n$, then the total conductance $G_{total} = G_p - G_n$ [38]. If $G_p = G_n$, G_{total} is zero, so that R_{total} is infinite. For a parallel resonator, the quality factor $Q = \frac{R}{\omega_0 L}$ ($\omega_0 = \frac{1}{\sqrt{LC}}$) [49, pp. 215], so Q will become infinite when R reaches infinite.

In this design, a type of balanced negative impedance circuit (NIC) has been used to enhance the quality factor, which is also presented in reference [10]. The negative conductance $-G_n$ is generated by a positive feed back network consisting of two NMOS transistors. Either of them has its gate connected by the drain of the other one, as shown in Fig. 3.4 (a).

The small signal equivalent circuit of the Q-Enhancement circuit is shown in Fig. 3.4 (b). Considering differential input signal applied at v_1 and v_2 , the potential of “s” will be constant, so the point “s” is a virtual ground for differential input signal at v_1 and v_2 . Then Fig. 3.4(b) is rearranged to Fig. 3.4(c). No small

signal current will flow through the point “s”, since it is connected to a current source. So finally Fig. 3.4(c) is revised to Fig. 3.5(d).

Fig. 3.4: Q-Enhancement circuit (a) and its Small Signal Model: (b) ~ (d)

A careful observation of Fig. 3.4 (d) shows that: (remember: “s” is “ground”).)

$$i = g_{m2}v_2 + v_1j\omega C_{gs1} \quad (3.22)$$

$$i = -g_{m1}v_1 - v_2j\omega C_{gs2} \quad (3.23)$$

Add Eqn. (3.22) and Eqn (3.23), then

$$2i = g_{m2}v_2 + v_1j\omega C_{gs1} - g_{m1}v_1 - v_2j\omega C_{gs2} \quad (3.24)$$

For differential design, $g_{m1} = g_{m2} = g_m$ and $C_{gs1} = C_{gs2} = C_{gs}$ are required. Then

Eqn. (3.24) can be rearranged to:

$$i = -\frac{1}{2}g_m(v_1 - v_2) + \frac{1}{2}j\omega C_{gs}(v_1 - v_2) \quad (3.25)$$

So
$$y_{in} = \frac{i}{v_1 - v_2} = -\frac{1}{2}g_m + \frac{1}{2}j\omega C_{gs} \quad (3.26)$$

Then the y_{in} can be easily controlled by tuning the bias current in M_1 and M_2 in Fig. 3.4, since the negative conductance is equal to $-g_m/2$. This tuning is definitely important in practical filter design, because the parasitic resistance due to the loss of the inductors and capacitors is frequency dependant.

3.3 Differential Active Resonator Design

3.3.1 Design before the Simulation Results

In this chapter, the active resonator is denoted as a circuit composed of active inductors and negative impedance circuit. As mentioned in section 3.2.1, the active inductor presented here can be modeled as a parallel resonator, which is composed of an active inductor, a capacitor and a resistor. So it is convenient to connect the active inductor and the Q-Enhancement circuit in parallel. And since the Q-Enhancement circuit presented in section 3.2.2 is constructed in differential structure, it is very nature to build the active resonator in differential structure, as shown in Fig. 3.5.

Fig. 3.5: Differential Active Resonator

In Fig. 3.5, L_1 and L_2 are the inductance of the active resonator, expressed by Eqn. (3.20). C_1 and C_2 are the capacitance of the active resonator, including C_3 in Eqn. (3.19), and other parasitic capacitance contributed by the Q-Enhancement circuit and all the current sources. R_1 and R_2 are the parasitic resistance of the resonator including the real part of Eqn. (3.19) and all other equivalent parallel parasitic resistance; and R' is the negative resistance of the NIC. The differential resonator presented here can be viewed as the two single-ended active resonator as shown in Fig. 3.6. For either side (left or right), the input admittance is:

$$y_{in} = \left(\frac{1}{R} + \frac{2}{R'} \right) + j\omega C + \frac{1}{j\omega L}. \quad (3.27)$$

Fig. 3.6: Analysis of Differential Active Resonator

The detailed schematic design of the differential active resonator is presented in Fig. 3.7. In this schematic, two active inductors are allocated along the two sides of the Q-Enhancement circuit. Other transistors compose the bias network. The Port 1 for S-parameter simulation is located at the top of the schematic.

Fig. 3.7: Detailed Differential Active Resonator Design

3.3.2 Simulation Results of the Differential Active Resonator

An S-parameter together with a DC simulation has been performed by Cadence 5.0 to characterize the impedance of the differential active resonator. As stated above, the inductance of the active inductor can be controlled by varying its bias current. The DC simulation provides all the design parameters of g_m s and C_s of Eqn. (3.19) at different bias current. According to these design parameters, the inductance and self resonant frequency of the active inductor have been calculated using Eqn (3.20) and Eqn. (3.21), as illustrated in Table 3.1. The simulated resonant frequency of the active resonator is also shown in the last column of Table 3.1. The resonant frequency of the active resonator is much lower than the self resonant frequency of the active inductor due to additional parasitic capacitance introduced by the Q-Enhancement circuit, the current sources and all other parasitics.

Table 3.1: Design Parameters of the Active Inductor

Bias current (A)	g_{m1} (S)	C_1 (F)	g_{m3} (S)	C_3 (F)	Achieved inductance (H)	f_1^* (Hz)	f_2^{**} (Hz)
0.75m	14.41m	38.27f	11.40m	145.1f	0.233n	27.4G	3.128G
1.25m	17.91m	39.84f	16.06m	156.4f	0.139n	34.2G	4.047G
2.5m	22.96m	40.93f	23.77m	162.4f	75.0p	45.6G	5.412G
5m	27.71m	41.29f	31.87m	163.6f	46.8p	57.6G	6.624G

* f_1 : self resonant frequency of the active inductor

** f_2 : resonant frequency of the active resonator

Fig. 3.8 shows the graph of inductance vs. bias current. It is clearly that the inductance decreases from 233pH to 46.8pH with the increasing bias current from 0.75mA to 5mA.

Fig. 3.8: Inductance of the active inductor vs. biasing current

Fig. 3.9 presents the real and imaginary part of y_{in} of the active resonator biased at 5mA. In Fig. 3.9, both $\text{Re}[y_{11}]$ and $\text{Im}[y_{11}]$ reaches zero at about 6.6GHz, so that an infinite impedance will be generated at this frequency, as shown in Fig. 3.9. The $\text{Re}[y_{11}]$ produce some negative value at higher frequency due to the

existence of the negative impedance circuit and the frequency dependant parasitic resistance.

Fig. 3.9: y_{in} of the Active Resonator in Differential Mode

Fig. 3.10: Frequency Tuning Capability of the Differential Active Resonator

Fig. 3.10 presents the tuning capability of the differential active resonator. At resonant frequency, a high quality parallel resonator will produce extremely high impedance. When bias at different current (0.75-5mA), the resonator will resonate at different frequency (3.1-6.6GHz), with very high quality factor as demonstrated in Fig.3.10.

The presented active inductor can produce an inductance from 0.233nH to 46.8pH in simulation. With this inductor the presented resonators achieves a tuning range from 3.1GHz to 6.6 GHz, larger than the active inductor in the report works [10]-[12], which only have tuning ranges of several hundred MHz.

The 3.1 to 6.6 GHz tuning range is still not large enough for UWB applications, which require an operating frequency range from 3.1 to 10.6GHz. However, this work is only an initial attempt to study on gyrator active inductors, and the achieved results will be used in future research to improve the performance of the active inductor.

3.4 Single-ended Active Resonator Design

3.4.1 Design before the Simulation Results

In section 3.3 a differential active resonator has been proposed. However, for single-ended filters, single-ended active resonators are required. The active inductor proposed in this chapter also can be employed in single-ended design. But there are two main difficulties in realizing a single-ended active resonator:

- I. A broadband single-ended tunable negative impedance circuit is very difficult to realize.

- II. Employing the proposed active inductor in single-ended mode requires two additional pins at V_{bias1} and V_{bias2} for AC ground as shown in Fig. 3.2. While differential active inductor only requires two bias voltages on V_{bias1} and V_{bias2} , which can be provided by internal bias circuits.

So in this design, a single-ended resonator is designed with the use of differential active inductor and negative impedance circuit, as shown in Fig. 3.11. Similar to the differential resonator design in Fig. 3.5, in Fig. 3.11, L is the inductance of the active resonator, expressed by Eqn. (3.20). C is the capacitance of the active resonator, including C_3 in Eqn. (3.19), and all other parasitic capacitance. R is the parasitic resistance of the resonator including the real part of Eqn. (3.19) and all other equivalent parallel parasitic resistance. R' is the resistance of the negative impedance circuit.

Fig. 3.11: Single-ended active resonator employing differential active Inductor and negative impedance circuit

Compared Fig. 3.11 with Fig. 3.5, the only difference is that the y_{in} here is now calculated in single-ended mode. After a tedious analysis of Fig. 3.11, the input admittance of the active inductor is:

$$y_{in} = \frac{R_2(1 - \omega^2 L_2 C_2) + j\omega L_2}{j\omega L_2(R_2 + R') + R_2 R'(1 - \omega^2 L_2 C_2)} + \frac{1}{R_1} + \frac{1}{j\omega L_1} + j\omega C_1 \quad (3.28)$$

Obviously the equation is too complicated to analyze, especially the first term.

Fortunately, the circuit in Fig. 3.11 can be analyzed in an alternative way.

Since the active inductor and the negative impedance circuit is differential, $L_1 = L_2$

$= L$, $C_1 = C_2 = C$ and $R_1 = R_2 = R$. Therefore at resonant frequency $\omega_0 = \frac{1}{\sqrt{LC}}$, the

circuit shown in Fig. 3.11 is simplified to the circuit in Fig. 3.12. The input admittance of the circuit is:

$$y_{in} = \frac{1}{R_1 + R'} + \frac{1}{R_2} \quad (3.29)$$

In case $R' = -(R_1 + R_2)$, y_{in} will be zero. So the single-ended active resonator acts similarly to its differential counterpart at the resonant frequency. But their out band performance are different since there is distinct difference between Eqn. (3.27) and Eqn. (3.28). This is also shown in the simulation results.

Fig. 3.12: Active resonator at ω_0

And according to Eqn. (3.29), R_1 and R_2 can be totally cancelled by R' , as long as $R' = -(R_1 + R_2)$, no matter whether R_1 equals to R_2 or not. That is to say, any mismatch between R_1 and R_2 will be absorbed by R' . Furthermore, if there is some mismatch between the imaginary part of the active inductor, for example $C_1 = C_2 + \Delta C$ and $L_1 = L_2 + \Delta L$, the admittance y_1 of the left half of the active resonator in Fig. 3.11 becomes:

$$y_1 = j\omega C_1 + \frac{1}{j\omega L_1} = j\omega C_2 + j\omega \Delta C + \left(\frac{1}{j\omega L_1} - \frac{1}{j\omega L_2}\right) + \frac{1}{j\omega L_2} \quad (3.30)$$

because

$$\frac{1}{j\omega L_1} - \frac{1}{j\omega L_2} = \frac{L_2 - L_1}{j\omega L_1 L_2} = \frac{1}{j\omega \frac{L_1 L_2}{-\Delta L}} \quad (3.31)$$

By substituting Eqn. (3.31) into Eqn. (3.30), Eqn. (3.30) is changed to

$$y_1 = j\omega C_1 + \frac{1}{j\omega L_1} = j\omega C_2 + \frac{1}{j\omega L_2} + j\omega \Delta C + \frac{1}{j\omega \frac{L_1 L_2}{-\Delta L}} \quad (3.32)$$

Assume $C' = \Delta C$ and $L' = \frac{L_1 L_2}{-\Delta L}$, L_1 and C_1 can be viewed as L_2 and C_2 are in parallel with L' and C' . L' and C' will cause shifting of the center frequency of the resonator, and the bias current for the negative impedance circuit may also vary. But as long as ΔC and ΔL is small enough, L' and C' will have little effect on the performance of the active resonator.

The detailed single-ended active resonator design is shown in Fig. 3.13. The configuration of the single-ended active resonator is almost the same as its differential counter part, except that the port1 for simulation is now connected in single-ended mode.

Fig. 3.13: Detailed Single-ended Active Resonator Design

3.4.2 Simulation Results of the Single-ended Active Resonator

Fig. 3.14: y_{in} of the Active Resonator in Single-ended Mode

An S-parameter together with a DC simulation has been performed by Cadence 5.0. Because the Single-ended active resonator has exactly the same structure as its differential count-part, they have same DC simulation results. So

the single-ended active resonator has exactly same inductance and resonant frequency as the differential resonator, which have been summarized in Table 3.1, Fig. 3.8, and Fig. 3.9. The y_{in} of the single-ended active resonator biased at 5mA is shown in Fig. 3.14. In Fig.3.14, both of the $\text{Re}[Y_{11}]$ and $\text{Im}[Y_{11}]$ of the single-ended resonator reach zero at about 6.6GHz, the same as the differential resonator, but their out of band performance are different, as analyzed in sub section 3.3.1.

3.5 Conclusions

The proposed active inductor can produce an inductance from 0.233nH to 46.8pH in simulation. Both differential and single-ended active resonators are realized by employing the proposed active inductor and Q-Enhancement circuit. With this inductor the presented resonators achieves a tuning range from 3.1GHz to 6.6 GHz. The tuning range is larger than the active inductor in the report works [10]-[12], which only have tuning ranges from about 300MHz to 1GHz plus. Compared to the active inductor in [7] & [13], this inductor doesn't have a superior performance, but it is realized in CMOS process, which is much less expensive than the GaAs process used in [7] & [13].

Although the 3.1 to 6.6 GHz tuning range is still not large enough for UWB applications, which require an operating frequency range from 3.1 to 10.6GHz, this work is only an initial attempt to study on gyrator active inductors, and the obtained results will be used in further improvement on the performance of the gyrator active inductor in future research work.

Simulation Studies on Active Inductor

In the following chapters, both bandpass filters and band stop filters employing the presented active inductor will be designed and discussed. First is the bandpass filter.

Chapter 4 Bandpass Filter Based on Active Inductor

Inductor

4.1 Introduction

This chapter presents a bandpass filter designed in $0.25\mu\text{m}$ IBM BiCMOS process with 2.5V power supply. The basic idea of the bandpass filter comes from [10], but both operating frequency and tuning range of the one in [10] is not high enough for UWB application. The bandpass filter designed in this chapter employs the differential gyrator active inductor presented in Chapter 3 to improve its performance. Both the basic design theory and schematic simulation results of the bandpass filter are presented here.

4.2 Theory

4.2.1 Top Level Configuration

The top level design of this bandpass filter in this chapter is composed of three blocks: a LNA, a bandpass filter and an output buffer, as shown in Fig. 4.1.

Fig. 4.1: Top Configuration of the Bandpass Filter

The LNA in Fig. 4.1 is used to improve the input matching and noise performance of the filter; and the output buffer is used to improve the output matching of the filter.

4.2.2 LNA

The LNA is used for improve the input matching and noise performance of the filter. The basic LNA structure is a differential pair (Q_1 and Q_2) loaded by resistive loadings, as shown in Fig. 4.2.

Fig. 4.2: The basic structure of the LNA

4.2.2.1 Input Matching Design of the LNA

A bipolar transistor with an impedance Z connected to its emitter, will present input impedance (Fig.4.3) [50, pp. 175]:

$$Z_{in} = r_b + \frac{g_m Z}{j\omega C_\pi} + Z + \frac{1}{j\omega C_\pi} \quad (4.1)$$

And if Z is an inductor with inductance L_1 , then the Eqn. (4.1) changes to:

$$Z_{in} = r_b + \frac{g_m L_1}{C_\pi} + j\omega L_1 + \frac{1}{j\omega C_\pi} \quad (4.2)$$

Fig. 4.3: Small Signal Equivalent Circuit for Input Matching

Then by carefully selecting the size of the transistor, and the inductance of the inductor, we can make $j\omega L_1$ and $\frac{1}{j\omega C_\pi}$ cancel each other at the resonant frequency ω_0 . Then by properly choosing the bias current of the BJT, we can make $r_b + \frac{g_m L_1}{C_\pi} = R_s$. Then the circuit is perfectly matched to R_s at ω_0 . Although at the frequency other than ω_0 , the imaginary part cannot be cancelled to zero, we can relieve its effect by choosing smaller L_1 and Larger C_π . The reason is that for series resonator, quality factor $Q = \frac{\omega_0 L}{R}$. By reducing the L , the Q will be smaller, and then a flatter frequency response of input matching (S_{11}) is achieved. So the influence of the frequency variation on the input impedance will be relieved. Because L_1 functions as emitter degeneration, normally only small value of the L_1 is selected due to gain and noise consideration. Then the inductance in Eqn. (4.2) may not be enough, so except inductor L_1 connected at the emitter of the transistor,

another inductor L_2 may be needed at the base of the BJT to provide additional inductance, as presented in Fig. 4.4.

Fig. 4.4: Input Matching Design

4.2.2.2 Noise Performance Optimization

Since this filter is intended to be implemented as a front-end design, the noise performance is very important.

The noise figure of a common emitter stage [50, pp.174] is:

$$NF = 1 + \frac{r_b}{R_s} + \frac{1}{2g_m R_s} + \frac{g_m R_s}{2\beta} \quad (4.3)$$

And the noise figure reduces to a minimum value of $NF_{\min} = 1 + \sqrt{(1 + 2g_m r_b) / \beta}$ for optimized source impedance $R_{S,opt} = \sqrt{\beta(1 + 2g_m r_b) / g_m}$.

Since R_s is fixed to 50 Ohm, by properly choosing a g_m , NF can reach an optimized value. From Eqn. (3.6), it is shown that NF is optimized, when

$$\frac{1}{2g_m R_s} = \frac{g_m R_s}{2\beta} \text{ at } g_m = \frac{\sqrt{\beta}}{R_s}. \text{ So bias current } I_C = \frac{V_T \sqrt{\beta}}{R_s}. \text{ Assume } V_T = 26 \text{ mV},$$

$R_s = 50 \text{ Ohm}$ and $\beta = 100$, then $I_C = 5.2 \text{ mA}$. It is quite a large bias current. The

large bias current also can increase the gain of the filter stage so as to reduce the noises contributed by the following stages. To minimize the r_b , a larger size bipolar transistor will be selected. But large size transistor will introduce more parasitic capacitance at the input. These parasitic capacitors should be taken into considerations, since it is very important for high frequency approximation. It is easy to see that the NF at higher frequency will not be as good as the one at lower frequency, because the β will tend to be lower at higher operating frequency.

As mentioned in section 3.3, the selection of the transistor size and bias current will also affect the input impedance too. So it is actually a trade off between input impedance matching design and noise optimization.

4.2.3 Bandpass Filter

4.2.3.1 Filter Structure

The basic configuration of the bandpass filter is depicted in Fig. 4.5. This bandpass filter is composed of a differential pair (Q_1 and Q_2) loaded by two resonator circuits: (R_1, L_1, C_1) and (R_2, L_2, C_2). The design of these resonators has been presented in Chapter 3. The advantage of the differential structure lies in the high rejection of common mode noise, better linearity (no second order harmonics for perfect matching) and higher achievable voltage swing [51, pp. 101-102]. Furthermore, when the packaging effects are taken into account, the differential structure is less prone to oscillation due to their low common mode gain [52, pp. 355]. Of course, these improvements are achieved by sacrificing the power consumption and chip size, because compared to their single-ended counter parts, their DC power dissipation and chip size are almost doubled.

Fig. 4.5: The Simplified Structure of the Bandpass Filter

4.2.3.2 Active Inductor and Q-Enhancement circuit

The resonators in Fig. 4.5 are realized by a differential active resonator composed of two active inductors and a Q-Enhancement circuit, which has been presented in Chapter 3. The center frequency tuning is realized by varying the bias current of the active inductor, which will in turn change the inductance of the active inductor; and a Q-Enhancement circuit is used to maintain a high Q performance.

The active inductor and Q-Enhancement circuit used in this chapter are almost the same as presented in Chapter 3, except that NMOS transistors are

replaced by BJT transistors as shown in Fig. 4.6. The analysis of these circuits has been presented in Chapter 3 and will not be repeated here.

Fig. 4.6: Active Inductor and Q-Enhancement circuit in BJT

4.2.4 Output Matching Design

The output impedance of a filter with a structure in Fig. 4.5 is almost equal to the impedance of the resonators, considering transistors Q_1 and Q_2 providing high output resistance. Since the imaginary part of the resonator admittance y :

$\text{Im}[y] = j\omega_0 C + 1/j\omega_0 L = 0$, when $\omega_0 = \sqrt{\frac{1}{LC}}$, the imaginary part of the resonator

admittance is zero at ω_0 . Here ω_0 is the resonant frequency of the resonator and center frequency of the filter pass band. Furthermore the real part of the resonator admittance is also zero, if the Q-Enhancement circuits cancel the parasitic resistance completely. That is to say, Z_o (the output impedance of the filter) is infinite at ω_0 . It will provide poor output matching to the loading (normally 50 Ohm for single-ended design, 100 Ohm for differential). And if it is directly

Bandpass Filter Based on Active Inductor

connected to the load, the total circuit will be unstable. Furthermore since the 50 Ohm loading impedance is also in parallel with the resonator, it will degrade the Q factor of the filter dramatically. So in this case, an output buffer is necessary to provide impedance matching and isolation between the resonator and the loading.

Since the input capacitance of the buffer will influence the frequency response of the filter, the emitter follower (also known as common connector) is preferred than the source follower. Another advantage of the emitter follower is the much higher g_m at the same bias current. The emitter follower stage and its equivalent small circuit model are shown in Fig. 4.7(a)-(b).

Fig. 4.7(a): Emitter Follower Stage

Fig. 4.7(b): Equivalent Circuit of the Emitter Follower Stage

In Fig. 4.7(b), the input and output impedances of the buffer stage are:

$$R_i = r_\pi + (\beta_0 + 1) (R_L \parallel r_o) \quad (4.4)$$

$$R_o = \alpha_0 / g_m + R_s / (\beta_0 + 1) \quad (4.5)$$

The input impedance of the buffer stage is quite large, since the R_L is multiplied by the factor of $\beta_0 + 1$. So the buffer itself will have little effect on the quality factor of the filter. And the output impedance is around $1/g_m$, so by controlling the bias current, R_o can be any value required.

4.3 Design before the Simulation Results

The detailed schematic design of LNA and bandpass filter is shown in Fig. 4.8. The LNA and its bias are located at the left of the filter. The bias for the filter is not included in this figure, because it is built in another block, which will be shown later.

Fig. 4.8: Schematic Design of LNA and Filter

Bandpass Filter Based on Active Inductor

The schematic design of the output buffer is shown in Fig. 4.9. The output buffer is composed of a differential common emitter stage followed by an emitter follower. The emitter follower is used to provide the low impedance output matching, while the common emitter stage is used for provide additional isolation between the 50 Ohm loading and the resonator of the filter to protect the quality factor of the bandpass filter from being degraded by the low impedance loading, as discussed before.

Fig.4.9: Schematic Design of the Output Buffer

Fig. 4.10 presents the top level design of the bandpass filter. The LNA and the filter are located at the left side. The output buffer is located at the right side. The bias network of the filter is seated at the bottom of the Fig. 4.10. In S-parameter simulation, port 1 is connected to the input (on the left) of design in Fig. 4.10, and port 2 is connected to the output (on the right) of the design.

Bandpass Filter Based on Active Inductor

Fig. 4.10: Top level design of the bandpass filter

4.4 Simulation Results

Schematic design and S-parameter simulation has been done for the bandpass filter employing the active inductor mentioned above using Cadence 5.0. The power consumption of the bandpass filter is about 68.7mW.

4.4.1 S-parameters, K and NF

S-parameters provide a complete description of RF networks [53, pp. 196]. Fig. 4.11 shows a two-port RF network and its S-parameters. Assume port 1 is the input port connected to the source and port 2 is the output connected to the load. At port 1, the incident and reflected wave voltages are a_1 and b_1 respectively. At port 2, they are a_2 and b_2 . The S-parameter is defined as [49, pp. 169-170]:

$$b_1 = S_{11}a_1 + S_{12}a_2 \quad (4.6a)$$

$$b_2 = S_{22}a_2 + S_{21}a_1 \quad (4.6b)$$

Fig. 4.11: Two port network and its S-parameters

Then S-parameters are given by [49, pp. 170]:

$$S_{11} = \frac{b_1}{a_1}, \text{ with } a_2 = 0. \quad (4.7a)$$

$$S_{21} = \frac{b_2}{a_1}, \text{ with } a_2 = 0. \quad (4.7b)$$

$$S_{22} = \frac{b_2}{a_2}, \text{ with } a_1 = 0. \quad (4.7c)$$

$$S_{12} = \frac{b_1}{a_2}, \text{ with } a_1 = 0. \quad (4.7d)$$

Hence, S_{11} is a measurement to input matching. A smaller S_{11} means less reflected power refer to the incident power. S_{22} is a measurement to output matching. S_{21} is the forward voltage gain, specifying the filter's function in our case. S_{12} is the reverse voltage gain, determining the leakage from the filter output to its input.

In normal communication systems, both of the input and output matching (S_{11} and S_{22}) is require to be $<-10\text{dB}$ at least. The requirement on S_{21} depends on different applications, and for this filter design, $S_{21}>0\text{dB}$ is enough, as long as its

noise performance is acceptable. The reverse isolation (related to S_{12}) normally is required to be $>20\text{dB}$. For front end design, a 3dB noise figure must be achieved to meet the minimum requirement.

One of the most important requirements that an amplifier/filter circuit must meet is a stable performance. This is particular important for RF circuits, which tends to oscillate depending on frequency and termination [49, pp. 470]. There are two types of stability [53, pp. 612]:

1. Unconditional stability: The network is stable for all passive source and load impedances.
2. Conditional stability: The network is stable only for a certain range of passive source and load impedances. This case is also referred to as potentially unstable.

Any network is considered to be unconditional stable, if the following necessary and sufficient conditions are met [53, pp. 614]:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1, \quad (4.8)$$

And $|\Delta| < 1 \quad (4.9)$

Here the Δ is defined as:

$$\Delta = S_{11}S_{22} - S_{12}S_{21}. \quad (4.10)$$

The K in Eqn. (4.8) is denoted as stability factor or Rollett factor [49, pp. 474]. In practical implementation, normally $K > 1$ is not enough to ensure the network stability, and $K > 10$ must be satisfied.

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The S_{21} and noise figure of the filter operating at highest center frequency 5.9GHz are shown in Fig. 4.12. The gain at that point is around 44dB, and the noise figure at this frequency is about 3dB. At lower frequency, the noise figure is even lower. The 3dB noise figure meets the minimum requirement of the front-end design for UWB applications, and it is better than other bandpass filters in [36]-[38]. S_{11} and S_{22} are shown in Fig. 4.13. S_{22} is obviously below -10dB through overall the frequency range. S_{11} is also less than -10dB between the range from 3GHz to 10GHz. In the pass band, both S_{11} and S_{22} are even better. The -10dB S_{11} and S_{22} are acceptable for UWB applications. Fig. 4.14 shows the S_{12} is less than -80dB, which is more than enough for UWB radio. Fig. 4.15 demonstrates the stability factor K, which is more than 50. The stability factor K is large enough to ensure a stable performance for the filter.

Fig. 4.12: S_{21} and Noise Figure of the Bandpass Filter

Bandpass Filter Based on Active Inductor

Fig. 4.13: S_{11} and S_{22} of the Bandpass Filter

Fig. 4.14: S_{12} of the Bandpass Filter

Bandpass Filter Based on Active Inductor

Fig. 4.15: K factor of the Bandpass Filter

4.4.2 Frequency Tuning

Fig. 4.16 shows the center frequency tuning of the bandpass filter. The center frequency can be tuned from about 2.25 GHz to 5.90 GHz, so that the broadband tuning is realized. The frequency tuning range is larger than reported bandpass filters in [10], [35]-[39], which only have tuning ranges of several hundred MHz. However, this tuning range is still not large enough for UWB applications, which require an operating frequency range from 3.1 to 10.6GHz. This design is only an initial attempt to study on the bandpass filter realized with gyrator active inductors. And these results will be used for further improvement of the filter performance.

Fig. 4.16: Frequency Tuning of the Bandpass Filter

In Fig. 4.16, the gain of the bandpass filter reduces significantly with frequency. That's because the gain of the LNA and the output buffer in Fig. 4.1 reduce with frequency due to their parasitic capacitive loadings.

4.4.3 Q-factor Control

Fig. 4.17 demonstrates the results of Quality Factor control. By tuning the bias current of the negative impedance circuit, the Q factor is tunable from 7.3 to 55.6. It is also can be seen that when the Q is improved, the gain (S_{21}) increases also. The reason is that by increasing the quality factor, the resistive part of the resonator is more and more cancelled, so the magnitude of the output impedance is increased and in turn the gain rises up. This Q-factor control will be very important to design a high quality bandpass filter for UWB applications, because the quality factor of filters will vary with process, temperature and the operation frequency.

Fig. 4.17: Q-Factor Tuning of the Bandpass Filter

4.5 Conclusions

The schematic design of a new tunable bandpass filter has been completed. The basic filter structure comes from [10], but a different gyrator active inductor with higher performance has been used in this design. Both the frequency tuning (from 2.25 GHz to 5.90 GHz) and Quality Factor control (from 7.3 to 55.6) have been realized. A 3dB noise figure is achieved which meets the minimum requirement of the front-end design for UWB applications, and it is better than other reported bandpass filters in [36]-[38]. The achieved frequency tuning range (2.25GHz to 5.9GHz) is larger than reported bandpass filters in [10], [35]-[39], which only have tuning ranges of several hundred MHz. However, this tuning range is still not large enough for UWB applications, which require an operating frequency range from 3.1 to 10.6GHz.

The performance of the presented bandpass filter is not sufficient for UWB applications, due to the limited frequency tuning range. However, this work is only an initial attempt to study on the bandpass filter realized with the presented gyrator active inductors, and these results will be used into further enhancement of the filter performance.

As stated in Chapter 1, a very critical problem faced by UWB systems is the interference generated by other narrow band communication systems, such as WLAN. Rejecting the in band interference is very important for UWB radios. Hence, in our case, we think bandstop filters (also called notch filters) may be more useful than bandpass filters. Therefore, due to the time and cost consideration,

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we will not put the presented bandpass filter into practical implementation, and we will focus on the design and investigation of notch filters in the following chapters.

Chapter 5 Simulation Studies on Notch Filter 1 with Varactor Tuning

5.1 Introduction

Notch filter (bandstop filter) is a type of filter, whose amplitude response possesses two passbands separated by a stopband, as shown in Fig. 5.1 [54, pp. 6]. Because one of the major problems faced by UWB communication systems is to reject the in-band interferences generated by other narrow band communication systems as stated in Chapter 4, notch filters will play an important role in UWB systems.

Fig. 5.1: Amplitude response of an ideal notch filter

In this chapter, a bandstop filter designed in $0.25\mu\text{m}$ IBM BiCMOS process with 3.3V power supply is presented. The basic idea of this type of design comes from [14] and [33]. In [14] and [33], a type of single-ended notch filter with varactor tuning is presented. With high performance GaAs MESFETs, this type of notch filter achieves a tuning range from 8.5GHz to 11GHz and a 5dB noise figure. In this chapter the presented notch filter is realized in a differential structure with varactor tuning. Both schematic and layout design of this notch filter are completed, and post-layout simulation results are presented here.

5.2 Theory

5.2.1 Basic Filter Structure

The basic Notch Filter structure is shown in Fig. 5.2. The filter is realized in differential structure. The resonator is connected at the emitter of the input transistor as an emitter degeneration stage. The equivalent transconductance of the emitter degeneration stage [40, pp. 199] is:

$$G_m \approx \frac{g_m}{1 + g_m Z_E} \tag{5.1}$$

Fig.5.2: Basic Structure of Notch Filter 1

In Eqn. (5.1), Z_E is the impedance seen at the emitter of the input transistor Q_1 . In this case, it is the impedance of the resonator. At oscillating frequency, the impedance of the resonator goes to infinite, so from Eqn. (5.1), the G_m falls to zero. Furthermore, if the Q of the resonator is high enough, at out of band

frequency, the Z_E is near to zero, and it is obvious the G_m will be equal to g_m . So in band $G_m \approx 0$, while at out of band $G_m \approx g_m$, the bandstop behavior is obvious.

5.2.2 Output Matching

Because the resonators are not located at the connector of the input transistor, the output matching design is simplified compared to the bandpass filter in Chapter 4. No output matching stage is needed in this design, because the output impedance of the filter is mainly determined by the loading resistor now (R_L in Fig. 5.3). In actual design, to cancel the parasitic capacitive loading at the output, an on chip inductor (L_1 in Fig. 5.3) is added in series with the loading resistor.

Fig. 5.3: Simplified output matching design with cascade connection

Furthermore, at high frequency, to reduce the effect of the resonator on the output impedance of the filter, the input transistor is constructed by two transistors

Simulation Studies on Notch Filter 1 with Varactor Tuning

in cascade connection, as shown in Fig. 5.3. Transistor Q_3 can be viewed as a common base stage. Its output impedance [40, pp. 191] is:

$$Z_o \approx R_L \parallel \left(\frac{g_{m3} r_{o3}}{\alpha_{03}} Z_{E3} \right) \quad (5.2)$$

Z_{E3} is the impedance seen at the emitter of the Q_3 . From Eqn. (4.2), Z_{E3} is increased by the factor of $\frac{g_{m3} r_{o3}}{\alpha_{03}}$, and R_L is in parallel with $\frac{g_{m3} r_{o3}}{\alpha_{03}} Z_{E3}$, so the effect of Z_{E3} on Z_o is much reduced. (Notice: Z_{E3} in Eqn. (5.2) is different from Z_E in Eqn. (5.1), which is the impedance at the emitter of Q_1 . Actually, Z_{E3} is equal to $\frac{g_{m1} r_{o1}}{\alpha_{01}} Z_E$.)

5.2.3 Frequency Tuning Scheme

In this filter design, varactors are used for frequency tuning. The varactors employed in this filter can operate in a reverse bias voltage range from 0 to 5V. The varactors have less capacitance at high reverse bias potential. To achieve a frequency tuning range as large as possible, we need to make full use of the varactor operation range: 0 to 5V. But it complicates our design, because VDD, the supply voltage is only 3.3V, which is lower than the maximum tuning voltage of the varactor. A bias voltage higher than the supply voltage has two disadvantages. First, it may cause break down of the transistors; second, for electrostatic discharge (ESD) protection circuit, any signal level should be between VDD and VSS to make sure all the ESD protection diodes are reverse biased in normal operating condition. In this design, a DC blocking capacitor is employed between the varactor and the internal circuit to protect it from break down. And one more DC supply higher than 3.3V is used for ESD protection (Fig. 5.4).

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Fig. 5.4: ESD Protection Circuit and the Varactor

5.2.4 Active Inductor

The active inductor used in this design and its small signal equivalent circuits are shown in Fig. 5.5.

Fig. 5.5: Active Inductor and its Small Signal Equivalent Circuit

Assume $C = C_1 + C_{\pi}$, and at RF frequency band, r_{π} is neglectable compared to C , then:

$$y_{in} = \frac{g_m + j\omega C}{1 + j\omega CZ} \tag{5.3}$$

If Z is an inductor, then Eqn. (5.3) changes to

Simulation Studies on Notch Filter 1 with Varactor Tuning

$$y_{in} = \frac{g_m + j\omega C}{1 - \omega^2 LC} \quad (5.4)$$

At microwave frequency, we can select a large C_1 (remember: $C = C_1 + C_\pi$) to make $g_m \ll j\omega C$ and $1 \ll \omega^2 LC$, then Eqn. (5.4) is changed to $y_{in} = \frac{1}{j\omega L}$.

To improve the quality factor of the resonator mentioned above, a Q-Enhancement circuit is used. The Q-Enhancement circuit employed here is the same as the one presented in section 4.2.3.2. Because the varactors have lower quality factor when it is reverse biased at lower potential, more bias current is needed for the Q-Enhancement circuit at the lower resonant frequency. That is totally reverse to the active inductor presented in Chapter 3, in which the Q-enhancement circuit requires more bias current at the higher operating frequency.

5.2.5 Input Matching

The input section of the notch filter in Fig. 5.2 is depicted in Fig. 5.6. According to Fig. 5.3 and Eqn. (4.1), the input impedance of the filter is:

$$Z_{in} = r_b + \frac{g_m L}{C_\pi} \frac{1}{1 - \omega^2 LC} + \frac{j\omega L}{1 - \omega^2 LC} + \frac{1}{j\omega C_\pi}, \quad (5.5)$$

and the real part of Eqn. (5.5) is:

$$Z_{re} = r_b + \frac{g_m L}{C_\pi} \frac{1}{1 - \omega^2 LC}. \quad (5.6)$$

By a simple analysis to Eqn. (5.6), it is obvious that Z_{re} will be a negative or a small positive value when ω is larger than $\omega_0 = \frac{1}{\sqrt{LC}}$. And if the difference

between ω and $\omega_0 = \frac{1}{\sqrt{LC}}$ is small enough, Z_{re} will even be a large negative

value. So input matching of this structure is very poor and the whole circuit tends to oscillate easily.

Fig. 5.6 (a): Input Section of Notch Filter 1, and (b): its Small Signal Equivalent Circuit

In actual design, some passive components are used to compensate for the negative impedance. After compensation, although the stability of the filter has been ensured, the input matching is still poor. The noise performance suffers a lot from this passive compensation.

5.3 Design before the Simulation Results

The detailed schematic design of Notch Filter 1 is presented in Fig. 5.7. All the input matching sections, output matching sections, active inductors, frequency tuning sections and Q-Enhancement circuit, are depicted in Fig. 5.7. Other parts out of the circles in Fig. 5.7 are bias networks. In simulation, the input pins (v_{inp} and v_{inn}) are connected to Port 1 and the output pins (v_{op} and v_{on}) are connected to Port 2.

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Fig. 5.7: Schematic Design for Notch Filter 1

The layout design of Notch Filter 1 is shown in Fig. 5.8.

Fig. 5.8: Layout Design for Notch Filter 1

5.4 Simulation Results

The post layout simulation of the notch filter in Fig. 5.7 to 5.8 has been performed using Cadence 5.0. The simulation results are shown from Fig. 4.6 to Fig. 4.11. The total DC power consumption of Notch Filter 1 is about 82mW.

5.4.1 S-parameters, K and NF

The simulation results in Fig. 5.9 show that the filter has a 3dB gain and 5dB out-of-band noise figure. As indicated in section 5.2.1, at resonant frequency, the gain of the filter will fall to near zero. That is why the S_{21} falls dramatically at about 4.3GHz. The very low gain at 4.3GHz causes a very high in-band noise figure (more than 40dB), because the signal at this frequency is attenuated dramatically, so that the signal to noise ratio at this frequency is very low. In notch filter designs, only the out-of-band noise figure is concerned, because the in-band signal is designed to be rejected. Here, the in-band is defined as “inside the rejection band”, and the out-of-band is defined as “outside of the rejection band”. In this design the out-of-band NF is about 5dB, similar to the reported works in [14] and [33], and further improvement on NF is needed for UWB systems.

The S_{11} of this filter is very poor, only at about -3dB, as shown in Fig. 5.10, so this notch filter has a very poor input matching, just as we have discussed earlier. No S_{11} (input matching) results are produced in [14] and [33]. This poor input matching is not acceptable by UWB systems. The S_{22} in Fig. 5.10 is <-10dB below 3.5GHz, but it needs further improvement at higher frequency. The S_{12} in Fig. 5.11 is sufficient for UWB applications. The notch filter has a K factor larger than 100, as shown in Fig. 5.12 and it is good enough for UWB applications.

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Fig. 5.9: Simulated S₂₁ & NF of Notch Filter 1

Fig. 5.10: Simulated S₁₁ and S₂₂ of Notch Filter 1

Simulation Studies on Notch Filter 1 with Varactor Tuning

Fig. 5.11: Simulated S₁₂ of Notch Filter 1

Fig. 5.12: Simulated K factor of Notch Filter 1

5.4.2 Frequency Tuning

Fig. 5.13 shows that the center frequency of this filter can be tuned from around 4.3GHz to 6.5GHz. The tuning range here is about 2.2GHz, similar to the 2 to 2.5 GHz tuning range of reported works in [14] and [33]. And it is a little less than 3.6GHz tuning range of the bandpass filter realized by gyrator active inductor in Chapter 4. The achieved frequency tuning range is not large enough for UWB systems, but this filter are still useful in UWB applications, since they successfully covers the frequency band of WLAN, the largest interference jamming the UWB radio.

Fig. 5.13: Simulated Frequency tuning of Notch Filter 1

5.4.3 Q-factor Control

The Q-factor control of Notch Filter 1 is depicted in Fig. 5.14. A quality factor up to 107 is achieved. Higher quality notch filter will provide higher rejection to the in-band signal, as shown in Fig. 5.14. Hence, notch filter with higher quality is almost expected by UWB systems. In this design, a 40dB rejection is achieved, a little better than 30dB rejection of the reported works in [14] and [33]. The reported works in [14] and [33] are designed in high performance GaAs, so that they can achieve a high quality design without the Q-Enhancement circuit.

Fig. 5.14: Simulated Q-factor Control of Notch Filter 1

5.5 Conclusions

A new tunable bandstop filter has been designed. Both the schematic and layout design are performed, and the post-layout simulation results have been presented. The basic filter structure comes from [14] and [33]. The filter in this chapter is designed by BiCMOS, a less costly process compared to GaAs, and it is designed in differential structure while the original ones in [14] and [33] are single-ended designs. The advantage of the differential structure lies in the high rejection of common mode noise, better linearity (no second order harmonics for perfect matching) and higher achievable voltage swing [51, pp. 101-102]. Furthermore, when the packaging effects are taken into account, the differential structure is less prone to oscillation due to their low common mode gain [52, pp. 355].

The notch filter presented here achieves a 5dB noise figure and 2.2GHz tuning range, similar to the published works in [14] and [33]. But the noise performance is not sufficient for UWB applications, so further improvements are necessary. The achieved frequency tuning range is not sufficient for UWB applications, but this filter are still useful in UWB systems, considering it successfully covers the frequency band of WLAN, the largest interference jamming the UWB radio. The 40dB in-band rejection of this notch filter is better than the 30dB rejection of the published works in [14] and [33]. And it is acceptable to UWB applications.

This notch filter employs varactor for frequency tuning. The achieved tuning range here (4.3GHz to 6.5GHz) is a little less than the tuning range of the

Simulation Studies on Notch Filter 1 with Varactor Tuning

bandpass filter in Chapter 4 (2.25 to 5.9GHz), which exploits gyrator active inductors for frequency tuning. The main problem of the varactor tuning scheme is that it requires a large voltage tuning range (in this case it is 0-5V, even larger than the 3.3V supply voltage, as stated in section 5.2.3), so the varactor tuning is not suitable to low power, low voltage systems, especially the portable devices of UWB systems.

The major problem of this notch filter is its poor input matching (the S_{11} is -3dB only, while at least -10dB is required for front end design in UWB systems), which is unacceptable for UWB applications. A solution must be found in future research.

This notch filter has been fabricated and measurement results will be presented in Chapter 8.

Since Notch Filter 1 has the problem of input matching, another notch filter (Notch Filter 2) with different structure to avoid the input matching problem will be designed in next chapter. The new notch filter will be designed in CMOS process to further reduce the cost. Because varactor tuning scheme requires a large tuning voltage, which makes it not suitable to low power, low voltage systems, the gyrator active inductor presented in Chapter 3 will be utilized for frequency tuning in the new notch filter.

Chapter 6 Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

6.1 Introduction

This chapter presents a new notch filter designed in $0.13\mu\text{m}$ IBM CMOS/RF process with 1.5V supply voltage.

Since Notch Filter 1 has the problem of input matching, the notch filter in this chapter (Notch Filter 2) is designed in a different structure to avoid the input matching problem. The basic idea of the new notch filter comes from [11] and [12], which provide a type of bandstop filters in GaAs process, operating at around 1 to 2 GHz. To reduce the cost, Notch Filter 2 will be designed in CMOS/RF process. As explained in Chapter 5, because varactor tuning scheme requires a large tuning voltage, which makes it not suitable to low power, low voltage systems, the gyrator active inductor presented in Chapter 3 will be exploited in this notch filter design to improve its frequency tuning capability to about 3GHz. The schematic design and simulation have been performed.

6.2 Theory

6.2.1 Basic Filter Structure

The basic topology of this filter is shown in Fig. 6.1. Although the filter presented in Fig. 6.1 is depicted in a single-ended structure to simplify its analyses, the actual notch filter is designed in differential configuration. And the analyses of both filters are similar.

Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

Fig. 6.1: Basic Topology of Notch Filter 2

Obviously M_1 and the parallel resonator consisting of L and C in Fig. 6.1 exhibit a bandpass frequency response. To achieve a bandstop response, M_2 and M_3 are employed to invert the bandpass response. The small signal equivalent circuit of the above notch filter is shown in Fig. 6.2.

Assume Z is the impedance of the parallel resonator (L and C in Fig. 6.2), then:

$$v_{gs2} = v_{in}g_{m1}Z \quad (6.1)$$

It is obvious, that:

$$i_{out} = v_{in}g_{m3} - v_{gs2}g_{m2} \quad (6.2)$$

Substitute Eqn. (6.1) to (6.2), then:

$$i_{out} = v_{in}g_{m3} - v_{in}g_{m1}Zg_{m2} \quad (6.3)$$

Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

Rearrange it:

$$i_{out} = v_{in} (g_{m3} - g_{m1}g_{m2}Z) \quad (6.4)$$

So the equivalent transconductance of the filter is:

$$G_m = g_{m3} - g_{m1}g_{m2}Z \quad (6.5)$$

Remember $Z = \frac{j\omega L}{1 - \omega^2 LC}$, and substitute Z into Eqn. (6.5):

$$G_m = g_{m3} - g_{m1}g_{m2} \frac{j\omega L}{1 - \omega^2 LC} \quad (6.6)$$

If the Q of the active resonator is high enough and we carefully select proper value of g_{m1} , g_{m2} and g_{m3} , we can make the G_m is around g_{m3} out of band and nearly zero in band. Then the bandstop frequency response is achieved.

Fig. 6.2: Small Signal Equivalent Circuit of Notch Filter 2

6.2.2 LNA

To improve the noise figure of the filter, a LNA is employed in front of the filter. The LNA is also designed in differential structure, but its analysis is similar to the single-ended LNA proposed in following paragraphs.

Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

The simplified LNA structure is shown in Fig. 6.3. And its small signal equivalent model is presented in Fig. 6.4. In Fig. 6.4, if the gate-drain capacitance and the source-bulk capacitance are ignored to simplify the analysis, then the input impedance of the LNA [50, pp. 173] is:

$$Z_{in} \approx \frac{g_m L_1}{C_{gs}} + (L_1 + L_2)s + \frac{1}{C_{gs}s} \tag{6.7}$$

Fig. 6.3: LNA Design

Fig. 6.4: Equivalent Small Signal Model of the LNA

Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

According to Eqn. (6.7), by carefully selecting the size of the transistor, and the inductance of the inductor, we can make the imaginary part of Eqn. (6.7):

$j\omega(L_1 + L_2)$ and $\frac{1}{j\omega C_{gs}}$ cancel each other at the resonant frequency ω_0 . Then by

properly choosing the bias current of the BJT, we can make the real part of Eqn.

(6.7): $\frac{g_m L_1}{C_{gs}} = R_s$. Then the circuit is perfectly matched to R_s at ω_0 . Although at the

frequency other than ω_0 , the imaginary part cannot be cancelled, we can relieve this effect by choosing smaller L_1 , L_2 and Larger C_{gs} . The reason is that for series

resonator, quality factor $Q = \frac{\omega_0 L}{R}$ [49, pp. 215]. By reducing the L , the Q will be

smaller, and then a flatter frequency response of input matching (S_{11}) is achieved.

So the influence of the frequency variation on the input impedance will be relieved. Because L_1 functions as source degeneration, normally only small value of the L_1 is selected due to gain and noise consideration. That is the reason why another inductor L_2 is necessary at the gate of M_1 to provide additional inductance, as presented in Fig. 6.3.

Since L_1 acts as source degeneration, the equivalent transconductance of the LNA stage is decreases. And to achieve low noise performance, the bias current of the LNA is quite large. Although the current source has larger impedance and can provide higher gain, in this design a resistor is used as the loading of the LNA stage rather than a current source. There are two reasons. Firstly, the current source presents a much larger parasitic capacitance at the output of the LNA, which will reduce the speed of the LNA, so it is not suitable for a broadband design. Secondly, although the current source can reduce the noise

Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

contributed by the following stage, and it can provide higher gain when used as the load, the current source itself is very noisy. In fact it degrades the noise performance of the LNA.

Because the LNA output is connected to the input transistor of the filter inside the IC, rather than a pin connected to the PCB board, it is unnecessary to consider the output matching of the LNA.

The noise figure of a system consisting of two stages [50, pp. 45] is:

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} \quad (6.8)$$

(In Eqn. (6.8), all the NFs and the power gain A_{ps} should be ratios, not in dB.) So if the LNA has higher power gain, the noise performance of the system will be improved. But a higher gain of the LNA will reduce the linearity of the whole system. Therefore, the selection of the gain of the LNA is a trade off between noise performance and linearity. In this design, the gain of the LNA is around 8dB.

6.2.3 Active Inductor

The active inductor and the negative impedance circuit used in this design are the same as the differential active resonator design presented in Chapter 3. The analysis of the differential active resonator has also been presented in Chapter 3.

6.3 Design before the Simulation Results

The detailed schematic design is shown in Fig. 6.5. The differential LNA, notch filter, active inductor and the Q-Enhancement circuit are indicated in Fig.

Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

6.5. The transistors out of the circles in this figure are used to construct bias network. The v_{in} is the input of Notch Filter 2 and connected to Port 1 in simulation. The v_{out} is the output and connected to Port 2.

Fig. 6.5: Schematic design of Notch Filter 2

6.4 Simulation Results

The schematic design and simulation of the filter in Fig. 6.5 has been performed by Cadence 5.0. The total power consumption is about 97.7mW. The simulation results are presented in following sub-sections.

6.4.1 S-parameters, K and NF

Fig. 6.6 to Fig. 6.9 is the S-parameter simulation results, when the center frequency of the notch filter is at the lowest center frequency, 2.9GHz. The simulation results in Fig. 6.6 show that the filter has a 5dB gain and a minimum

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7dB out-of-band noise figure. The achieved noise figure is much better than the 13 to 16dB noise figure of the reported work in [12]. No results about noise performance are provided in [11]. However, the noise performance achieved in this design is still not sufficient for the front-end filter in UWB applications, which requires a maximum 3dB noise figure.

The S_{11} of this filter (<-10 dB) is much better than the S_{11} of the filter in Chapter 5 (-3 dB), as shown in Fig. 6.7. And it satisfies the requirement of UWB systems. The output matching (S_{22}) is shown in Fig. 6.7, exhibiting a good performance (<-12 dB) over all the UWB range (about 3 to 10G). The achieved S_{12} (<-40 dB) in Fig. 6.8 and K factor (>50) in Fig. 6.9 are good enough to UWB applications.

Fig. 6.6: S_{21} and NF of Notch Filter 2

Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

Fig. 6.7: S_{11} and S_{22} of Notch Filter 2

Fig. 6.8: S_{12} of Notch Filter 2

Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

Fig. 6.9: K factor of Notch Filter 2

Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

6.4.2 Frequency Tuning

This notch filter achieves a large frequency tuning range from around 2.9GHz to 5.9GHz, as shown in Fig. 6.10. With exploiting the gyrator active inductor presented in Chapter 3, the frequency tuning range of Notch Filter 2 is much improved, compared to the 1.8-2.2GHz tuning range of the reported work in [11] and the 0.625-2.0GHz tuning range in [12]. The achieved frequency tuning range of Notch Filter 2 is not broad enough for UWB systems, but this filter are still useful in UWB applications, since they successfully covers the frequency band of WLAN, the largest interference jamming the UWB radio.

Fig. 6.10: Frequency Tuning of Notch Filter 2

Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

6.4.3 Quality Factor Control

The Q-factor control of Notch Filter 2 is depicted in Fig. 6.11. A quality factor up to 126 is achieved. Higher quality notch filter will provide higher rejection to the in-band signal, as shown in Fig. 6.11. Hence, notch filter with higher quality is almost expected by UWB systems. In this design, a 40-50dB rejection is achieved, better than the 30dB rejection of the reported works in [11] and [12].

Fig. 6.11: Quality Factor Control of Notch Filter 2

6.4.4 Linearity Performance

In S-parameter simulations, RF circuits are approximated with a linear model to obtain their small signal responses. However, filters realized by active devices are initially nonlinear, and their nonlinearity has distinct influence on their performances.

One important phenomena related to nonlinearity is “Gain Compression” [50, pp. 15]. At certain operating frequency, the gain of an active circuit is not constant and will vary with the input signal amplitude. In most cases of interest, the gain will drop with the increasing input signal level, and even approach zero. In RF circuits, this effect is quantified by the “1-dB compression point,” defined as the input signal level which causes the gain to drop by 1 dB, compared to the small signal gain [50, pp. 15-16]. Here the small signal gain is the gain of the circuit with the assumption that all nonlinear effects are negligible. Sometimes the “1-dB compression point” is called the “input referred 1-dB compression point”, and the output signal level at the 1-dB compression point is called the “output referred 1-dB compression point”.

Fig. 6.12: Definition of the 1-dB compression point

Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

Another important phenomena related to nonlinearity is “Intermodulation” [50, pp. 17-22]. When two signals at different frequencies are applied to a nonlinear system, the output will generate some components that are not the harmonics of the input signals. This is called intermodulation (IM). Assuming two signals at ω_1 and ω_2 enter a nonlinear system, the output of the nonlinear system will exhibit two components at $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$. If the difference between ω_1 and ω_2 are small, the components at $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$ will appear in the vicinity of ω_1 and ω_2 , as shown in Fig. 6.13. Therefore, the intermodulation products at $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$ may fall into other desired channels adjacent to ω_1 and ω_2 , and corrupt the signals of interest, as shown in Fig. 6.14.

Fig. 6.13: Intermodulation in a nonlinear system

Fig. 6.14: Corruption of a signal due to Intermodulation

In RF circuits, the “third intercept point” (IP3) is used to characterize the intermodulation behavior. The parameter is measured by a two tone test, as shown in Fig. 6.13. Assuming both the signals at ω_1 and ω_2 have amplitude A , and A is

Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

sufficiently small at the beginning, so that all high order harmonics are negligible. When A increases, the fundamental signal at ω_1 and ω_2 increase in proportional to A , whereas the third order IM products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ increase in proportional to A^3 [50, pp. 19]. On a logarithmic scale (Fig. 6.15), the magnitude of the third order IM products increases at three times the rate of the fundamental components. The “third intercept point” is defined as the intersection of these two lines. The horizontal coordinate of the intersection is called the input IP3 (IIP3), and the vertical coordinate of the intersection is called the output IP3 (OIP3).

Fig. 6.15: Definition of the IP3

As stated above, the 1dB compression point is a measurement to the power handling capability of RF circuits, and the IP3 is a measurement to the capability of suppression to the IM products of RF circuits. For typical RF circuits, the 1dB compression point and the IP3 are expected to be as large as possible.

In this design, the achieved input referred 1dB compression point and IIP3 of this filter is around -13.9dBm (Fig. 6.16) and -4.5dBm (Fig. 6.17) respectively. These results are acceptable for UWB applications.

Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

Fig. 6.16: Input & Output Referred 1dB Compression Point of Notch Filter 2

Fig. 6.17: Input & Output IP3 of Notch Filter 2

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The 1dB compression point and IP3 only show the out of band linearity performance of the notch filter. For in band signals, the capability of the filter to reject the input signal is more important. The rejection of Notch Filter 2 to input signal with different power at 5.9GHz is summarized in Table. 6.1.

Table 6.1: Rejection capability of Notch Filter 2:

Frequency	Input Power	Output Power	Rejection
5.9GHz	-48.01dBm	-92.96dBm	44.95dB
5.9GHz	-38.01dBm	-84.16dBm	46.15dB
5.9GHz	-28.01dBm	-72.7dBm	44.69dB
5.9GHz	-18.01dBm	-29.74dBm	11.73dB

The Table 6.1 has been converted into Fig. 6.18(a) and (b). In Fig. 6.18(a), the output power increase linearly with the input power, until the input power reaches -18.01dBm. At that point, the output power increases dramatically. That is also verified by Fig. 6.18(b), the rejection is almost constant until the input power reaches -18.01dBm, then the rejection decreases to 11.73dB.

As shown in Table 6.1 and Fig. 6.18(a) & (b). The bandstop filter has better rejection over the input signal with lower input power. That is caused by the nonlinearity of the active inductor and Q-Enhancement circuit. As stated in Chapter 3, the inductance and the quality factor of the active resonator are controlled by the transconductance g_m of the transistors, and the g_m relies on the bias current of the transistors. When the input signal is large enough to have

Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

distinct influence on the bias current, the g_m will be varied, and the inductance and the quality factor of the active resonator will be varied in turn.

Fig. 6.18(a): Ouput power vs. Input power

Fig. 6.18(b): Rejection vs. Input power

Fig. 6.18: Rejection capability of Notch Filter 2

6.5 Conclusions

A novel notch filter has been successfully designed. Both schematic design and simulation results have been presented. Compared to the filters reported in [11] and [12], this filter is realized in the CMOS/RF process instead of the expensive GaAs.

This notch filter achieves a frequency tuning range from around 2.9GHz to 5.9GHz, as shown in Fig. 6.10. With exploiting the gyrator active inductor presented in Chapter 3, the frequency tuning range of Notch Filter 2 is much improved, compared to the 1.8-2.2GHz tuning range of the reported work in [11] and the 0.625-2.0GHz tuning range in [12]. The achieved frequency tuning range of Notch Filter 2 is not enough for UWB systems, but this filter are still useful in UWB applications, since they successfully covers the frequency band of WLAN, the largest interference jamming the UWB radio.

With employing a LNA stage in front of the filter, this notch filter achieves a much better noise performance compared to the published works in [11] and [12]. This work achieves a noise figure at about 7dB, whereas the reported work in [12] only has a noise figure at 13 to 16dB. No noise performance results are provided in [11]. However, the 7dB noise figure is not enough for the front end design of UWB applications.

The problem on noise figure may be solved by improving the gain of the LNA, but that will worsen the linearity of the whole circuit. Another way to improve its noise performance is to increase g_{m3} relative to g_{m1} and g_{m2} (Eqn.

Simulation Studies on Notch Filter 2 with Bias Tuning in Differential Structure

(6.5)), but that will also worsen its linearity, because, to reject the same input signal a larger voltage amplitude is required at the gate of M_2 . Therefore, the noise performance and the linearity of the notch filter is a trade-off. In future research, this design may be carefully optimized to achieve a good balance between the noise figure and the linearity performance.

Because fabrication of MMIC (Microwave Monolithic Integrated Circuit) is extremely expensive and time costing, this design is not fabricated due to time and cost consideration.

In next chapter, another notch filter (Notch Filter 3) will be designed and investigated. The basic structure of Notch Filter 3 is the same as the Notch Filter 1 presented in Chapter 4. To improve the input matching of this type of filter, a LNA is exploited at the input of the filter, which will provide a -10dB input matching. Moreover, a gyrator active inductor is employed instead of the varactor in Notch Filter 1. Notch Filter 3 utilizes the same active inductor as the one used in Notch Filter 2, so a similar tuning range will be achieved (about 3 GHz). Notch Filter 3 is also designed in the low cost CMOS process, and it is realized in single-ended configuration to further reduce the chip size and the cost.

Chapter 7 Simulation Studies on Notch Filter 3 with Bias Tuning of Single-ended Structure

7.1 Introduction

As stated in Chapter 5, Notch Filter 1 has very poor input matching. One way to solve this problem is to add a LNA at the input of the notch filter. So a third notch filter (Notch Filter 3) is designed and investigated. The basic structure of Notch Filter 3 is the same as the Notch Filter 1 in Chapter 4, except a LNA stage is employed at the input of the filter, which will provide a -10dB input matching. Moreover, because the varactor is not suitable to low voltage low power systems, as explained in Chapter 5, the gyrator active inductor presented in Chapter 3 is employed in this design to realize frequency tuning instead of the varactor. Since Notch Filter 3 utilizes the same active inductor as the one used in Notch Filter 2, a similar frequency tuning range will be achieved (about 3 GHz). Notch Filter 3 is also designed in the low cost CMOS process, and it is realized in single-ended configuration to further reduce the chip size and the cost.

The filter in this chapter is designed in IBM 0.13 μ m CMOS/RF process, and the power supply is 1.5V. The schematic design, layout design, and the post-layout simulation of this filter are presented here.

7.2 Theory

7.2.1 Basic Filter Structure

Except that this notch filter is designed in CMOS rather than BJT, its basic topology is the same as the one presented in chapter 5, and a LNA stage is added

Simulation Studies on Notch Filter 3 with Bias Tuning of Single-ended Structure

in front of the filter to improve its input matching and NF performance, as shown in Fig. 7.1. Another major difference is that the filter in this chapter employs an active inductor in gyrator concept for frequency tuning instead of the varactors used in chapter 5, because varactors is not suitable to low voltage, low power systems, as stated in Chapter 5. Furthermore, this notch filter is designed in single-ended structure due to size and cost consideration, so that the LNA and the active resonator used in this chapter are also designed in single-ended configuration.

Fig. 7.1: Fundamental Structure of Notch Filter 3

7.2.2 LNA Design

The LNA exploited in this design is the same as the one presented in Chapter 6, except the LNA used in this chapter is designed in single-ended structure. Their analysis is similar and will not be repeated here.

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7.2.3 Active Inductor

The active inductor and the negative impedance circuit used in this design are the same as the single-ended active resonator design presented in Chapter 3. The analysis of the single-ended active resonator has also been presented in Chapter 3.

7.3 Design Before The Simulation Results

7.3.1 Schematic Design

The detailed schematic design of Notch Filter 3 is presented in Fig. 7.2 to Fig. 7.4. Fig. 7.2 shows the top level design of Notch Filter 3. Notch Filter 3 consists of a LNA on the left of Fig.7.2 and a filter on the right. In S-parameter simulation, Port “vin” on the left side of Fig. 7.2 is connected to Port 1, and Port “vout” is connected to Port 2.

Fig. 7.2: Top level design of Notch Filter 3

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The detailed LNA design is presented in Fig. 7.3. Since the output of this LNA is connected to the input of the filter on chip, output matching of LNA is not necessary.

Fig. 7.3: Schematic Design of the LNA

Fig. 7.4: Schematic design of the filter

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Schematic design of the filter is shown in Fig. 7.4. Positions of the input matching section, active inductors, and Q-Enhancement circuit etc. are indicated in Fig. 7.4. Other parts out of the circles in Fig. 7.4 are the bias network for the filter.

7.3.2 Layout Design

The layout design of Notch Filter 3 is presented in Fig. 7.5.

Fig. 7.5: Layout design of Notch Filter 3

7.4 Simulation Results

The post layout simulation of the notch filter in Fig. 7.4 and 7.5 has been carried out by Cadence 5.0. The total power consumption is about 85.7mW. The simulation results are presented in following sub-sections.

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7.4.1 S-parameters, K and NF

Fig. 7.6 to Fig. 7.9 presents the S-parameter simulation results. The simulation results in Fig. 7.6 show that the filter has a maximum 7dB gain and a 4 to 7dB out-of-band noise figure. The achieved noise figure is better than Notch Filter 2 and similar to Notch Filter 1. The noise performance achieved in this design is still not sufficient for the front-end filter in UWB applications, which requires a maximum 3dB noise figure. The S_{11} of this filter (<-10 dB) is much better than the S_{11} of the filter in Chapter 5 (-3 dB), as shown in Fig. 7.7. And it satisfies the requirement of UWB systems. The output matching (S_{22}) is shown in Fig. 7.7, exhibiting a good performance (<-15 dB) over all the UWB range (about 3 to 10G). The achieved S_{12} (<-25 dB) in Fig. 7.8 and K factor (>10) in Fig. 7.9 meet the minimum requirement of UWB applications.

Fig. 7.6: S_{21} and NF of Notch Filter 3

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Fig. 7.7: Input and Output Matching of Notch Filter 3

Fig. 7.8: S_{12} of Notch Filter 3

Simulation Studies on Notch Filter 3 with Bias Tuning of Single-ended Structure

Fig. 7.9: K factor of Notch Filter 3

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7.4.2 Frequency Tuning

This notch filter achieves a large frequency tuning range from 2.815GHz to 6.026GHz, as shown in Fig. 7.10. The achieved frequency tuning range of Notch Filter 3 is similar to Notch Filter 2 in Chapter 6, because they exploit the same active inductor for frequency tuning. The frequency tuning range of Notch Filter 3 is still not enough for UWB systems, but this filter are still useful in UWB applications, since they successfully covers the frequency band of WLAN, the largest interference jamming the UWB radio.

Fig. 7.10: Frequency Tuning of Notch Filter 3

7.4.3 Quality Factor Control

The Q-factor control of Notch Filter 3 is depicted in Fig. 7.11. A quality factor up to 67 is achieved. In this design, a 40dB rejection is achieved, similar to Notch Filter 1 and Notch Filter 2. The Q-factor achieved is acceptable to UWB applications.

Fig. 7.11: Q-factor Control of Notch Filter 3

7.4.3 Linearity Performance

The input referred 1dB compression point and IIP3 of Notch Filter 3 are about -17.8dBm (Fig. 7.12) and -9.3dBm (Fig. 7.13) respectively. A little worse compared to Notch Filter 2. That would be no surprising, since differential structures initially has better linearity than their single-ended counter parts, as explained in Chapter 4. These simulation results are acceptable for UWB applications.

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Simulation Studies on Notch Filter 3 with Bias Tuning of Single-ended Structure

As explained in Chapter 6, the filter performance depends on the active inductor, while the performance of the active inductor relies on the transconductance of the transistors. However, transconductance, g_m is strongly signal dependant. Therefore the active notch filter has linearity problem in the stop band. Table 7.1 shows the rejection capability of Notch Filter 3 for the signal at 6.026 GHz.

Table 7.1: Rejection capability of Notch Filter 3:

Frequency	Input power	Output power	Rejection
6.026GHz	-58.21dBm	-91.74dBm	33.53dB
6.026GHz	-48.21dBm	-75.01dBm	26.80dB
6.026GHz	-38.21dBm	-51.31dBm	13.10dB
6.026GHz	-28.38dBm	-31.29dBm	02.91dB

Table 7.1 has also been converted into Fig. 7.14(a) and (b). From these figures, it is very clear that the rejection to the input signal of Notch Filter 3 decreases with the increasing input signal power. For example, when the input signal is -58.21dBm, the notch filter can provide a rejection of 33.53dB; while when the power of the signal goes up to -28.38dBm, the filter only has a rejection of 2.91dB. Therefore, the notch filter can only provide higher rejection to the signal at lower power level. Especially when the signal goes up to beyond -30dBm, very little rejection will be provided. The linearity of the notch filter can be improved by reducing the gain of the LNA in Fig. 7.1, so that the input signal power level at the input of the filter will be decreased. But that will also increase the noise figure of the notch filter.

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Fig. 7.14(a): Output power vs. Input power

Fig. 7.14(b): Rejection vs. Input power

Fig. 7.14: Rejection capability of Notch Filter 3

7.5 Conclusions

A novel notch filter design has been successfully performed. Its schematic design, layout design and post layout simulation results have been presented. To further reduce the cost and the chip size, this filter is designed in single-ended structure.

The basic configuration of Notch Filter 3 is similar to Notch Filter 1 in Chapter 5. Because the input matching of Notch Filter 1 is very poor (S_{11} is only about 3dB.), a LNA stage is employed to at the input of the filter to improve its input matching, and a $S_{11} < 10\text{dB}$ is achieved, which is acceptable by UWB applications.

As stated in Chapter 5, the varactor is not suitable to low voltage, low power systems, since it requires a large voltage tuning range from 0 to 5V for frequency tuning. Therefore, in Notch Filter 3, gyrator active inductors presented in Chapter 3 are exploited for frequency tuning, and a tuning range from 2.815GHz to 6.026GHz is achieved, a little larger than the 4.3GHz to 6.5GHz frequency tuning range of Notch Filter 1. The frequency tuning range of Notch Filter 3 is not enough for UWB systems, but this filter are still useful in UWB applications, since they successfully covers the frequency band of WLAN, the largest interference jamming the UWB radio.

Notch Filter 3 achieves a noise figure at about 4 to 7dB, and it is not enough for the front end design of UWB applications. The noise performance of Notch Filter 3 can be improved by increasing the gain of the LNA, but the linearity

Simulation Studies on Notch Filter 3 with Bias Tuning of Single-ended Structure

of Notch Filter 3 will be degraded, since the signal at the input of the filter will be increased by the LNA.

Notch Filter 3 can only provide higher rejection to the signal at lower power level. Especially when the signal goes up to beyond -30dBm, very little rejection will be provided. The linearity of Notch Filter 3 can be improved by reducing the gain of the LNA, so that the input signal power level at the input of the filter will be decreased. But that will also increase the noise figure of the notch filter. Therefore, there is a trade off between the linearity and the noise figure of Notch Filter 3.

Because fabrication of MMIC (Microwave Monolithic Integrated Circuit) is extremely expensive and time costing, this design is not fabricated due to time and cost consideration.

In next chapter, measured results of Notch Filter 1 in Chapter 5 will be presented and discussed.

Chapter 8 Notch Filter - Fabrication and Measured Results

8.1 Introduction

Notch Filter 1 in Chapter 5 is designed in $0.25\mu\text{m}$ IBM BiCMOS process with 3.3V power supply. This notch filter has been fabricated and measured in a laboratory setting. This IC using probe pads instead of common pads at input and output of the filter. The measured results of Notch Filter 1 will be presented and discussed here.

8.2 Measurement Setup

The on-wafer layout of Notch Filter 1 is shown in Fig. 8.1.

Fig. 8.1: On wafer layout

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The two groups of white squares (five squares in either group) in Fig. 8.1 are the probe pads for input and output. The input section of Notch Filter 1 is located at the right of the layout in Fig. 8.1. The output section of Notch Filter 1 is located at the bottom of the layout of Fig. 8.1. The tuning section including the varactors is located on the top of Fig. 8.1. Another photograph of the on-wafer layout with the probes is shown in Fig. 8.2. The black shadows in Fig. 8.2 are the probes.

Fig. 8.2: On-wafer layout with probes

The measurement setup is shown in Fig. 8.3. On the left side of Fig. 8.3 is the vector network analyzer (VNA). On the right side of Fig. 8.3 is the Cascade probe station. Fig. 8.4 shows the printed circuit board (PCB) on the probe station, including a microscope (top center) and two probes (left and right side). Fig. 8.5 shows the probes (left and right bottom corner) and the chip (center).

Notch Filter – Fabrication and Measured Results

Fig. 8.3: Measurement Setup

Fig. 8.4: The PCB on the probe station

Fig. 8.5: The Probes and the Chip

8.3 Measurement Results

8.3.1 S-parameters and NF

The S-parameters results of the notch filter is measured by the Agilent Technologies N4421A S-parameter Test Set and the E8364B PNA Series Network Analyzer, and PLTS (physical layer test system) calibration is used. The measured S-parameters results are shown from Fig. 8.6 to 8.7. The S_{21} in Fig. 8.6 is 3-5dB less than the simulated S_{21} , which may be caused by the fabrication tolerance and the contact resistance between the probes and the probing pads. The S_{21} must be improved to beyond 0dB to meet the requirement of UWB applications. The measured S_{12} in Fig. 8.6 is similar to the simulation results and good enough for UWB applications. Similar to the simulation results, the measured S_{11} in Fig. 8.7 is very poor. It is not acceptable to UWB applications. The measured S_{22} in Fig. 8.7

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is similar to its simulated result and further improvement is required as stated in Chapter 5.

Fig. 8.6: Measured S_{21} and S_{12} of the Practical Notch Filter

Fig. 8.7: Measured S_{11} and S_{22} of the Practical Notch Filter

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The noise figure of the practical notch filter is measured by using the Agilent N8975A NFA Series Noise Figure Analyzer. As presented in Fig. 8.8, the measured noise figure is almost 20dB worse than the simulated results. The reason maybe comes from the loss contributed by the fabrication tolerance, the contact resistance between the probes and the probing pads, and other parasitics which is difficult to estimate accurately in the simulation, such as packaging effect and other parasitics on board.

Fig. 8.8: Measured Noise Figure of the Practical Notch Filter

8.3.2 Frequency Tuning

As can be seen in Fig. 8.9, the center frequency of the filter can be tuned from 5.17GHz to 5.52GHz, with a quality factor around 40. The notch depth of the filter is more than 40dB. The achieved 350MHz frequency tuning range is too much smaller than the simulated results (2.2GHz). Because the varactor is seated on the ground, while one terminal of the varactor is connected to the outside of the chip, as shown in Fig. 5.4, the varactor is very sensitive to any parasitics connected

to that terminal, for example the parasitics due to the package effect and the on board parasitics. This may be the main reason why the frequency tuning range is smaller than expected. To solve this problem, the varactor should not be put on the ground directly; rather it will need another fabrication.

Fig. 8.9: Measured Frequency Tuning of the Practical Notch Filter

8.3.3 Linearity Performance

The 1dB compression point and IP3 of the practical notch filter are measured by using the ROHDE & SCHWARZ Signal Generator SMIQ06B and the HEWLETT PACKARD Spectra Analyzer 8595E. The measured input referred 1dB compression point and IIP3 of this filter are 4dBm and 15.4dBm respectively. These results are acceptable to UWB applications.

8.4 Conclusions

The notch filter designed in Chapter 5 has been fabricated and measured in a laboratory setting. The measured results have been presented. Compared to simulation results, the gain is around 3-5dB less, while Noise Figure is much higher. The reason maybe comes from the contact resistance between the probe and the probing pad and other parasitics which is difficult to estimate accurately in the simulation, such as package effect. As predicted by simulation in Chapter 5, the input matching of the filter is very poor. On the other hand, the achieved frequency tuning range: 350MHz is much smaller than the simulation results. Because the varactor is seated on the ground, while one terminal of the varactor is connected to the outside of the chip, any parasitics at that terminal will affect the filter performance. This may be the main reason why the frequency tuning range is smaller than expected. To solve this problem, the varactor should not be put on the ground directly.

Although simulation results of Notch Filter 1 in Chapter 5 are promising, measurement results on the input matching, noise figure and the frequency tuning range of this practical filter are very poor and not acceptable by UWB applications. They are caused by the fabrication tolerance and other unexpected parasitics, including package effect and on board parasitics. In future research, a LNA is necessary at the input of the filter to improve its input matching and noise performance. The frequency tuning scheme should be carefully designed to avoid the influence from parasitics. One example is presented in Fig. 8.10. For a differential design, the pin of “Vtune” is a virtual ground, so parasitics at this point have little effects on the filter performance.

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Fig. 8.10(a): Existing frequency tuning scheme including the varactor and ESD protection diodes, which is sensitive to parasitics at “Vtune”.

Fig. 8.10(b): Proposed frequency tuning scheme including the varactor and ESD protection diodes, which is not sensitive to parasitics at “Vtune”.

Chapter 9 Conclusions and Recommendations

9.1 Conclusions

Ultra Wide Band (UWB) radio is a relative new wireless RF technology developed to transfer signals at hundreds of Mbit/s over very short distance at very low power densities. UWB systems are inherently broadband from 3 to 10 GHz, and have to coexist with the existing narrow band communication systems. Therefore, in UWB systems, front-end filters to minimize interferences from exiting communication systems for 3-10 GHz are the key component in the transceiver design.

In this project, the objective has been targeted on design and investigation on both bandpass and bandstop microwave active tunable filters with active inductors or varactors in BiCMOS and CMOS/RF processes. Because UWB radio is ultra broadband from 3 to 10GHz, the frequency tuning capability of these filters has been investigated and discussed. Since a noise figure less than 3dB is the most critical requirements of the receiver front-end design, the noise performance of these filters has been investigated and analyzed.

In this project, an active inductor based on the gyrator concept has been designed and investigated to realize the frequency tuning. One bandpass and two bandstop tunable active filters employing this active inductor have been designed and developed. Another notch filter utilizing varactor for frequency tuning has also been designed and investigated. All these filters are designed in BiCMOS and CMOS processes.

In Chapter 3, a gyrator active inductor has been designed and investigated. The schematic design and simulation have been carried out. A gyrator active inductor with an inductance from 46.8pH to 233pH and a self resonant frequency from 3.1 to 6.6GHz has been presented.

For the bandpass filter in Chapter 4, the schematic design and simulation have been performed. Both the frequency tuning (from 2.25 GHz to 5.90 GHz) and Quality Factor control (from 7.3 to 55.6) have been realized. With the LNA in front of the filter, a 3dB noise figure is achieved.

For the bandstop filters, three different structures have been designed and investigated from Chapters 5-7. Notch Filter 1 (Chapter 5) employs varactors for frequency tuning (4.3 to 6.5GHz). Because it avoids using the high noise active inductor, it possesses the best noise performance in simulation (5dB). However, this structure has two major disadvantages: first, the bias voltage for the varactor tuning may be higher than the supply voltage; second, the filter performance is very sensitive to the parasitics at the terminal for voltage tuning of the varactor. Although simulated results are promising, measured results of Notch Filter 1 in Chapter 8 are worse than what had been simulated, especially for the frequency tuning (5.17 to 5.52GHz) and the noise figure (>25dB). The reason mainly comes from the fabrication tolerance, the unexpected parasitics at the probe pad and the external pin of the varactor, as stated in Chapter 8.

Compared to Notch Filter 1 (Chapter 5), Notch Filter 2 (Chapter 6) and Notch Filter 3 (Chapter 7) employ active inductors for frequency tuning. Because

Conclusions and Recommendations

the active inductor is noisier than the varactor, to improve their noise performance, a LNA stage is added in front of them. The LNA also improves the input matching of the filters ($<-10\text{dB}$). The major difference between Notch Filter 2 and Notch Filter 3 is their filter structures. Notch Filter 2 realizes the bandstop performance by reversing a bandpass structure, while Notch Filter 3 employs the active resonator as source degeneration to get the bandstop response. Both Notch Filter 2 and Notch Filter 3 use the same kind of active inductor, so their frequency tuning ranges are almost same (about 3 to 6GHz). But Notch Filter 2 has better rejection ability, while Notch Filter 3 has better noise performance ($>4\text{dB}$). The major problem of the active inductors is that their operations are strongly dependent on input signal strength. That is because the performance of the active inductor relies on the transconductance g_m of the transistors, while g_m is strongly signal dependant, as explained in Chapter 6.

9.2 Recommendations

In this project, several difficulties are encountered:

- The gyrator based active inductor is quite noisy, so that the filters employing active inductor for frequency tuning have poor noise performance.
- To improve the noise performance, a LNA is necessary in front of the filter, but the linearity of the filter will be sacrificed. A trade off between noise performance and linearity of the filter exists.
- Filters employ varactors for frequency tuning has better noise performance, but this type of filters requires a large tuning voltage, so that they are not suitable to low voltage systems.

Conclusions and Recommendations

- In practical implementation, the fabrication tolerance and the parasitics have large influence on the filter performance at microwave frequency. Some of the parasitics are hard to estimate accurately, such as the parasitics due to packaging effect and the PCB design.

The filters presented in this work need further development before they can be put into practical applications. These developments can't be performed in this thesis due to time and cost constraints.

- For Notch Filter 1, the frequency tuning part should be redesigned to reduce the parasitic effects, as shown in Fig. 8.10. A LNA stage should be put before it to improve its noise performance and input matching.
- For Notch Filter 2 and Notch Filter 3, further research is necessary on the relationship between their noise performance and linearity, so that a good balance between NF and linearity can be found. Notch Filter 2 and Notch Filter 3 should be fabricated and tested. Then the actual performance of the three notch filters can then be compared.
- A frequency tuning scheme combined with varactors and active inductors may provide a larger frequency tuning range.
- The main constraint of this project is the practical implementation. Researchers should be very careful on this subject in future research. Design margin to cover the fabrication tolerance and the unexpected parasitics are necessary.

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