Nanoscale strained-Si/SiGe and double-gate MOSFET modeling

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Abstract

A new approach to modeling non-classical CMOS devices, such as strained-silicon (s-Si) and double-gate (DG) MOSFETs, is presented. We have employed a unified regional, non-pinned surface-potential based modeling approach, which is consistent with the prior development for bulk-MOS formulations. The key idea is to develop unified models with the correct physics and boundary conditions built into them, so that there is a seamless transition of models among different device structures like bulk, DG, SOI, and strained silicon. Threshold-voltage models are derived for surface- and buried-channel strained-silicon MOSFETs based on the 1-D Poisson equation. A unified regional modeling (URM) approach has been used to develop a single-piece physics-based charge model. An implicit iterative technique to calculate surface potential and charge was developed using the URM solutions. The model is generic and can be applied to all hetero-structure devices. With the structural and band information, the model can predict the threshold voltage, surface potential, charge and capacitance in surface- and buried-channel strained-silicon MOSFETs. A doping dependant shift in the plateau of a strained-silicon MOSFET C–V curve was observed. The physics behind this behavior was studied and modeled physically. A study on the different mobility models for strained-silicon MOSFETs has been carried out.

Multiple-gate structures, such as double gate, Ω gate, π gate and surrounding gate, are gaining a lot of attention due to their excellent sub-threshold characteristics and scalability. DG MOSFETs can be classified into symmetric and asymmetric MOSFETs based on the structure and bias applied at the two gates. When doping is included in the modeling of multiple-gate structures, the field equation is not integrable. We have used

URM solutions to solve the potential at the front and back gates regionally for both symmetric and asymmetric structures. A drain-current model based on the unified regional potential solutions has been derived.

Different techniques to extract the physical parameters, such as oxide thickness, strained-silicon layer thickness, band offsets, and doping in the channel have been demonstrated. The model parameters used in the non-classical MOSFET models are consistent with the bulk-MOS formulations. We have step-by-step extraction techniques to extract the model parameters for the length/width dependent threshold-voltage, drain-current, and charge models.

In summary, the methodologies and formulations documented in this thesis represents an extension of the URM approach to non-classical CMOS structures as well as a demonstration on the first step towards unification of MOS models.

List of Symbols

Symbol	Remark
V_{gs}	Gate to source voltage
V_{gb}	Gate to bulk voltage
V_{ds}	Drain to source voltage
V_{db}	Drain to bulk voltage
V_{bs}	Bulk to source voltage
V_{cb}	Channel to bulk voltage
V_{deff}	Effective drain to source voltage
$V_{deff,\Delta}$	Effective drain to source voltage with <i>non-pinned</i> ϕ_s -solutions
$V_{deff,\Delta p}$	Effective drain to source voltage with <i>non-pinned</i> ϕ_s/ϕ_p -solutions
V_{geff}	Effective gate to source voltage
$V_{geff,\Delta p}$	Effective gate to source voltage with $V_{tp,\phi}$
$V_{geff,\Delta}$	Effective gate to source voltage with $V_{t,\phi}$
V_{dsat}	Saturation drain to source voltage
V_{dd}	High drain to source voltage ($V_{ds} = 1.2V$)
V_{d0}	Low drain to source voltage ($V_{ds} = 0.05V$)
V_{bb}	High bulk voltage ($V_{bs} = -1.2V$)
V_{b0}	Low bulk voltage ($V_{bs} = 0$)
V_{gg}	High gate to source voltage ($V_{gs} = 1.2V$)
V_{b0}	Low bulk voltage ($V_{bs} = 0$)
$V_{GBF}, V_{GBA}, V_{gbs}$	Forward unified model
V_{GBR}	Reverse unified model
V_t	Unified threshold voltage
$V_{t,\phi}$	“Non-pinned” ϕ_s -based threshold voltage
A_b	Bulk charge factor
n_i	Intrinsic carrier concentration
V_{th}	Thermal voltage
t_{ox}	Gate oxide thickness
ϵ_{ox}	Permittivity of oxide
ϵ_{si}	Permittivity of silicon
χ	Electron affinity
ϵ_{sige}	Permittivity of silicon germanium
m_o	Effective mass
m_e	Electron mass
m_h	Hole mass
ϕ_{ms}	Work function difference
ϕ_m	Work function for poly gate
V_{FB}, V_{fb}	Flat-band voltage
N_{ch}	Channel doping concentration

N_{sub}	Uniform substrate doping concentration
N_a	Acceptor concentration
N_d	Donor concentration
W	Effective channel width
L_{eff}	Effective channel length
L_g	Drawn gate length
X_j	Lightly-doped drain junction depth
X_{dep}	Depletion width
$\psi, \psi(x)$	Position dependent surface potential
ψ_{sL}	Channel surface potential at drain end
ψ_{s0}	Channel surface potential at source end
ϕ_f	Silicon intrinsic Fermi potential
ϕ_s	Channel surface potential
$\phi_{CC}, \phi_{cc,}$	Regional accumulation channel surface potential
$\phi_{ACC}, \phi_{acc,}$	Unified regional accumulation channel surface potential
ϕ_{DD}, ϕ_{dd}	Regional depletion channel surface potential
ϕ_{SUB}, ϕ_{sub}	Unified regional depletion channel surface potential
ϕ_{SS}, ϕ_{ss}	Regional strong inversion channel surface potential
ϕ_{STR}, ϕ_{str}	Unified regional strong inversion channel surface potential
ϕ_{DS}, ϕ_{ds}	Unified regional channel surface potential from depletion to strong inversion regions
ϕ_{SEFF}, ϕ_{seff}	Unified full regions channel surface potential
ϕ_{th}	Potential at the threshold voltage
ϕ_{px}	Potential across the oxide
t_{Si}	Strained silicon thickness or thickness of channel in DG
ΔE_c	Conduction band offset
ΔE_v	Valence band offset
$\phi_{p, str.}$	Unified regional Strong inversion channel surface potential
$\phi_{peff,}$	Unified full regions poly surface potential
Δ	Non-pinned surface-potential at strong inversion region
ΔE_g	Increase of energy gap in van Dort's model
Q_g	Unified gate charge per unit area
Q_d	Unified drain charge per unit area
Q_s	Unified source charge per unit area
Q_b	Unified bulk charge per unit area
Q_i	Inversion charge per unit area
Q_{sc}	Space charge per unit area
$Q_{b, str}$	Bulk charge at strong inversion region per unit area
$Q_{b, acc}$	Bulk charge at accumulation region per unit area
$Q_{b, ds}$	Bulk charge from depletion to strong inversion regions per unit area
$Q_{b, sa}$	Bulk charge from accumulation to strong inversion regions per unit area
Q_{b0}	Unified bulk charge from accumulation to strong inversion regions per unit area for $V_{ds}=0$

$A_{s,\Delta}$	Q_s auxiliary functions
$A_{d,\Delta}$	Q_d auxiliary functions
$D_{b,\Delta}$	Q_b auxiliary functions
C_{gg}	Gate capacitance
C_{dg}	Drain capacitance
C_{sg}	Source capacitance
C_{bg}	Bulk capacitance
σ_a	Smoothing parameter in $\mathcal{G}_r$ function for unified accumulation channel surface-potential formulation
σ_f	Smoothing parameter in $\mathcal{G}_f$ function for unified depletion channel surface-potential formulation
δ_ϕ	Smoothing parameter in $\mathcal{G}_{eff}$ function for unified ϕ_{seff}/ϕ_{ds} formulation
ρ_r	Smoothing parameter in $\mathcal{G}_r$ function for unified accumulation gate surface-potential formulation
ρ_f	Smoothing parameter in $\mathcal{G}_f$ function for unified depletion gate surface-potential formulation
$I_{ds,lin}$	Linear drain current
$I_{ds,sat}$	Saturation drain current
I_{ds}	Unified drain current
I_{ds}	Drain current
μ_0	Mobility degradation with transverse-field effect
μ_{eff0}	Mobility degradation with lateral/transverse-field effect
μ_{eff}	Effective mobility degradation
$E_\perp$	Transverse-field
E_{eff}	Effective transverse-field
E_{satn}	Effective saturation field
v_0	Velocity field relation
v_{sat}	Saturation velocity
v_h	Velocity overshoot
$E_{ }$	Lateral-field
δ_0	Length-dependent lateral-field factor
V_{geff}	Effective gate to source voltage
γ	Channel Body factor
C_d	Depletion capacitance
g_m	Transconductance
g_{ds}	Output drain conductance
I_{on}	Saturation current (I_{ds} @ $V_{ds}=V_{gs}=V_{dd}$)
μ_1	Mobility parameter for Coulombic scattering
μ_2	Mobility parameter for surface roughness scattering
μ_3	Mobility parameter for phonon scattering

C_{oxeff}	Effective oxide capacitance
Q_{b1}, Q_{b2}	Unified bulk charge per unit area at the surface and interface
Q_{i1}, Q_{i2}	Inversion charge per unit area at the at the surface and interface
Q_{acc1}, Q_{acc2}	Accumulation charge per unit area at the surface and interface
t_{SiGe}	Silicon germanium cap layer thickness
ϕ_{s1}, ϕ_{s2}	Potential at the surface and interface
$\phi_{cc1}, \phi_{cc2}, \phi_{dd1}, \phi_{dd2}, \phi_{ss1}, \phi_{ss2}$	Regional accumulation, depletion and strong inversion potential at the surface and interface.
$\phi_{acc1}, \phi_{acc2}, \phi_{sub1}, \phi_{sub2}, \phi_{str1}, \phi_{str2}$	Unified accumulation, depletion and strong inversion potential at the surface and interface.
V_{t1}, V_{t2}	Threshold voltage at the at the surface and interface
V_{FB1}, V_{FB2}	Flat-band voltage at the at the surface and interface
$E_{g,SiGe}$	Energy band gap in Silicon germanium
$n_{i,SiGe}$	Intrinsic carrier concentration in Silicon germanium
L_D	Debye Length
x_{d1}, x_{d2}	Depletion widths calculated from the surface and interface
ϵ_{SiGe}	Permittivity of Silicon germanium
N_c, N_v	Effective density of states at the conduction and valence band
ϕ_b	Surface potential at the bottom gate
ϕ_0	Mid-gap potential in a s-DG
E_s, E_b	Electric field at the front and bottom gates
$\epsilon_{oxf}, \epsilon_{oxb}$	Permittivity of oxide at the front and bottom gate
C_{oxf}, C_{oxb}	Oxide capacitance at the front and bottom gate
t_{oxf}, t_{oxb}	oxide thickness at the front and bottom gate
V_{FBf}, V_{FBb}	Flat-band voltages at the front and bottom gate
V_{FDf}, V_{FDb}	Voltage spent in depleting the channel from the front and bottom gates
$\phi_{s,d}, \phi_{b,d}$	Unified regional depletion potential from the front and bottom gates
$\phi_{s,vi}, \phi_{b,vi}$	Unified regional volume inversion potential from the front and bottom gates
$\phi_{s,str}, \phi_{b,str}$	Unified regional strong inversion potential from the front and bottom gates
$x_{d,f}, x_{d,b}$	Depletion width due to the front and back-gate.
Q_{ox}	Fixed oxide charge
Δ_2	Non-pinned interface-potential at strong inversion region
ϕ_B	Twice Fermi potential

CHAPTER 1: INTRODUCTION

1.1 Motivation

One of the key electronic components in the integrated circuit (IC) is the metal-oxide-semiconductor field effect transistor (MOSFET). The IC industry has been driven by the Moore's Law, which states that the number of transistors in a chip doubles roughly every two years. The industry has tried to follow the Moore's Law since 1960, which has resulted in tremendous increase in speed and density and decrease in power dissipation and cost per transistor. The industry has used scaling to keep in pace with Moore's law. With scaling of the transistors, a number of issues arise, such as gate leakage current, poly-silicon depletion and limits in doping the source, drain and channel. Material and processing techniques, such as high-K dielectrics, metal electrodes, different annealing techniques, elevated source/drain and halo implants for engineering the channel, have been employed by the industry to overcome these difficulties. With further scaling of the transistors, a number of short-channel effects (SCEs), such as reduced threshold voltage, increased leakage current and reduced mobility due to the high doping in the channel, have been observed. Hence, it is important to look for new methods of improving performance, while taking advantage of the current silicon technology base. Non-classical CMOS device structures [1], [2] like strained-silicon MOSFETs, ultra-thin body (UTB), Silicon-on-Insulator (SOI) MOSFETs and double-gate (DG) MOSFETs have been receiving considerable attention. Strained-silicon MOSFETs are fabricated by different methods. Some of the most commonly used techniques are growing a thin layer of strained silicon on top of a relaxed silicon-germanium buffer layer, straining with a

silicon–nitride cap and silicon–germanium pockets in the source and drain [3], [4]. Strained-silicon MOSFETs achieve very high drive current due to the high mobility in the channel. Strain has contributed to most of the performance improvements in the last few technology nodes. SOI MOSFETs have a thin layer of silicon on top of a silicon dioxide insulating layer, which is on top of a silicon substrate [5], [6]. The SOI MOSFETs exhibit reduced junction capacitance, improved electrical isolation and a relatively lower doping. Partially depleted SOI MOSFETs also create a floating body node. A good design can exploit the floating body capability of SOI MOSFETs. DG MOSFETs are receiving tremendous attention due to its very high drain current, ideal sub-threshold slope and excellent short-channel characteristics [7], [8]. These make DG MOSFETs the ideal choice for scaling below 25nm technologies.

The main goal of compact model development is to describe the terminal behavior of the devices mathematically (DC, small signal and large signal) in such a way as to facilitate the applications of circuit analysis techniques such as Kirchoff's current and voltage laws to a comparatively large assembly of interconnected devices to yield a circuit function. This mathematical capability assumes particular importance in case of monolithic circuit designs where once the design is committed to silicon, the results are binary, i.e., either the fabricated circuit works or it does not work to the designed specifications. Hardly anything except redesigning the circuit can be done for retrieval in case of negative results.

The carrier concentrations and their transport in the device is governed by the Poisson's equation and current-continuity equations, which follow from the Maxwell's equation by neglecting the magnetic effects as the device dimensions are a very small

fraction of wavelength at the highest frequencies these devices are expected to operate at. The transport is mainly governed by drift-diffusion phenomenon that has been further refined to take into account the local energy distribution of carriers through energy balance effects. All these effects are accounted for to different degrees in device simulators such as MEDICI, TAURUS, SENTAURUS, ATLAS, etc. While these simulators are able to predict the terminal behavior at DC, large-signal and small-signal levels, their use in the design of circuits is prohibited by not only the extremely large simulation time and exorbitant computational resources, but also by non-guarantee of the convergence due to large size of the ill-conditioned numerical equations. Compact models address these gaps and are thus essential.

The MOSFET devices, development of compact models for which is the goal of this thesis, are inherently two-dimensional. The charge and transport equations describing the devices are highly non-linear and there are no known exact analytical solutions for the problem. In fact, that provides the reason for the numerical simulation techniques for these devices. Leave alone the transport, even the Poisson's equation can not be integrated twice analytically for the simplest case where the doping is uniform and the carrier concentrations are described by simple Boltzmann statistics. This gives an ample space for a good combination of mathematical ingenuity and physical understanding to arrive at closed-form analytical expressions which describe the electrical terminal behavior of the device with reasonable accuracy and are favorably disposed towards application of circuit analysis techniques such as Kirchoff's current and voltage laws.

While there are attempts reported in the literature to model the devices using look-up tables which, in turn, does not delve into the physics of the devices deeply, the

design community does not prefer this approach in general as the lack of physical insights leading to circuit innovations are almost completely absent. The compact models on the other hand have the insights of simpler physics built into them. Invariably, the compact models decouple the two-dimensional problem into two or more one-dimensional problems, for example, the charge distribution problem (Gauss's Law) is in focus when looking into the dimension perpendicular to the gate and charge transport (current continuity) is in focus when looking at the channel in the direction parallel to the gate electrode. This in essence describes the gradual channel approximation that may not be rigorously accurate; more so for modern small dimensional devices, but it still holds the fort to help arrive at the tractable solution of the problem in the domain of analytical expressions. With the help of mathematical ingenuity such as describing the gate voltage and drain voltage by some effective numbers, which depend both on the applied bias and the device structural parameters such as device size and doping concentration, the dimensional decoupling works and yields acceptably accurate description of terminal behavior.

Advanced Compact Models (CMs) for bulk MOSFETs have been developed [9] and standardized to a large extent. Different modeling techniques like surface-potential based, charge-based and threshold-based models have been used to model bulk MOSFETs. BSIM4 and BSIMSOI have been the industry standard models for bulk and SOI technologies. BSIM4 and BSIMSOI are threshold-voltage based models and their major bottlenecks are lack of symmetry and poor accuracy in the weak inversion region. Industry has been standardizing a new model, PSP, a surface-potential based model for bulk MOSFETs.

Bulk CMOS and SOI CMOS technologies have been the main workhorse of the semiconductor industry. However, these technologies appear to be facing the red brick wall while considering scaling beyond 45nm node on account of the leakage currents threshold-voltage control, lower mobility values etc. mentioned above. With this the industry is slowly shifting attention to non-classical CMOS structures leading to a need to develop models for these non-classical devices such as strained-silicon MOSFETs, Double-Gate MOSFETs, etc. The motivation of this work is to understand the physics underlying these non-classical CMOS devices and physically model them facilitating development of analytical (closed form) description of their terminal behavior.

1.2 Objectives

The objective of the present research work is to (1) understand the physics underlying the strained-silicon and double-gate MOSFETs, (2) formulate and develop a new Unified Regional Model (URM) for the threshold voltage, surface potential, charge, and current, with scalability for different geometries and structure variations, (3) use the physics-based models to extract structural and process parameters like strained-silicon thickness, band offsets, channel doping, (4) extract AC and DC model parameters in a *step-by-step* calibration procedure validated with numerical simulation and experimental data.

1.3 Major contributions of the Thesis

The major contributions of this research work are:

- 1) Threshold-voltage model has been derived for both surface-channel [10] and buried-channel [11] devices based on the 1-D Poisson solution. Geometry scaling and bias scaling have also been included physically in the model, which is consistent with the bulk formulation [12].
- 2) A new effect on the C–V characteristics of strained-silicon MOSFETs with variations in the substrate doping has been studied and explained with physically derived equations. The plateau in a strained-silicon MOSFET C–V characteristics shifts from the inversion side to the accumulation side with increase in substrate doping [13].
- 3) Single-piece unified regional charge model for strained-silicon MOSFETs from accumulation to inversion has been derived [14]. The flat-band voltage at which accumulation occurs at the different interfaces is calculated physically. The URM approach is used to derive the charge pieces in each region and then unified using an interpolation function. The scalability of the model has also been tested.
- 4) An implicit iterative technique to calculate the surface potential, charge and capacitance in strained-silicon MOSFETS has been proposed [11]. The modeling approach is very generic and can be applied easily to other hetero-structures. The scalability of the model is also tested for different layer thicknesses, band offsets and channel doping.
- 5) A detailed study on the different mobility models for strained-silicon MOSFETs has been done. The present day MOSFETs have a number of stressors like STI, silicon nitride cap, SiGe source/drain doping and SiGe substrate. A study was done on an empirical holistic model that captures the effect of all the stressors.

- 6) A technique to extract physical parameters like strained-layer thickness, doping and band offset from the strained-silicon C–V characteristics has been developed [15]. The model equations are used for the extraction. The model has been validated using TCAD simulations and experimental data.
- 7) A unified regional model for the surface potential and mid-gap potential of a doped symmetric DG MOSFET model has been developed [16]. The scalability of the model was tested for various channel thicknesses and doping as well as different front and back-gate oxide thicknesses.
- 8) A generic unified potential model applicable to Symmetric DG (s-DG), Asymmetric DG (a-DG) and SOI MOSFETs has been developed. The model is derived based on the Gauss law at the two gates and a general Poisson solution. The model is solved regionally and unified using an interpolation function. This model is generic and can be applicable to partially-depleted (PD) and fully-depleted (FD) SOI, s-DG, a-DG and bulk MOSFETs. The seamless transition of the model across various device topologies has been demonstrated.
- 9) A drain-current model has been derived for DG MOSFETs. The model has been derived based on the calculated front and back-gate potentials.
- 10) The DC and AC models for strained-silicon MOSFET have been developed and implemented in MATLAB. The model is used to extract the physical and model parameters from TCAD and experimental data.

1.4 Organization of the Thesis

The thesis consists of seven chapters. Chapter 1 introduces the motivation and the objective of this work, as well as the main contributions from the research and the organization of the thesis.

Chapter 2 outlines the existing modeling approaches and the need for modeling of the non-classical CMOS structures. The chapter then explains the unified modeling approach that has been employed for modeling the non-classical CMOS structures.

Chapter 3 focuses on the modeling of strained-silicon MOSFETs. The chapter first explains the physics behind the improved performance of strained-silicon MOSFETs. Models have been developed for the threshold voltage, surface potential, charge, drain current and capacitance. The effect of substrate doping on the C-V characteristics of strained-silicon MOSFETs has also been studied and explained physically in this chapter. The chapter also explains an iterative technique to calculate surface potential and charge in hetero-structures.

Chapter 4 explains the different multiple-gate structures and their operation. The chapter also briefs on the existing DG MOSFET models and the necessity to include doping in the model. The chapter then explains the modeling of potential, charge and drain current in doped symmetric and asymmetric DG MOSFETs.

Chapter 5 presents parameter extraction techniques. The chapter explains how the model equations can be used to extract the physical parameters from numerical or experimental electrical data. The validity of the model has been tested with experimental data. The chapter then explains the AC and DC model parameter extraction procedure for non-classical MOSFETs.

Chapter 6 verifies the strained-silicon and double-gate MOSFET models with experimental data and simulated Medici data. The scalability of the strained-silicon model across different variations in germanium mole fractions, channel thickness and terminal bias has been tested. The seamless transition of the DG model to various device topologies like UTB, SOI and bulk MOSFETs has been demonstrated. Summary and conclusions of the different models developed for strained-silicon and DG MOSFETs as well as suggestions and recommendations for future investigation to enhance the modeling methodology are presented in Chapter 7.

CHAPTER 2: EXTENDING BULK MODEL TO NON-CLASSICAL CMOS STRUCTURES

Compact models are mathematical descriptions of electrical terminal behavior of the semiconductor devices. These models are needed during the design of circuits, and their use is particularly indispensable during the design of the monolithic integrated circuits. The device simulators making use of rigorous numerical techniques to address the complex physical mechanism responsible for the experimentally observed terminal behavior of devices are of limited use in circuit designs as the circuit blocks may comprise hundreds and or even thousands of interconnected devices and the device simulators will need prohibitively large computation resources, if at all the problem can be solved. Thus, the purpose of compact modeling is to derive simple, fast, physical, scalable and accurate representation of the electrical characteristics of the MOSFET such that these models can be useful design aids for designing of circuit blocks with a capability to address the needs of a number of technological nodes in the era of exponential growth in scaling of technology.

The earliest compact models were reported about 45 years ago [20]. With the aggressive scaling of the MOS transistor and its increasing usage in RF and analog applications, the need for more accurate and computationally less intensive models arises. As the physics involved in the operation of semiconductor devices is very complex, it is quite a challenge to develop models that are physical, accurate over the entire bias and geometry spectrum, computationally efficient, and predictive to help in evaluation of the upcoming technology nodes.

2.1 Bulk Modeling Approaches

The MOSFET is inherently a 2-D electronic device. An input voltage is applied in the x -direction perpendicular to the gate to modulate the amount of (inversion) charge, which flows near the surface in the y -direction when a voltage is applied between the source and the drain ends. The traditional first step in developing a compact model is to decompose the 2-D problem into two coupled 1-D problems [17]-[19]. The 1-D solution, which links the applied gate voltage to the electric potential at the semiconductor/insulator interface, is called the input-voltage equation. This is obtained by the 1-D solution of Poisson equation. The other 1-D solution, which relates the current passing through the device to the quasi-Fermi potential resulting from the voltage applied between the source and the drain terminals, is called the output-current equation. This decomposition of the 2-D problem into two 1-D problems is called the Gradual Channel Approximation (GCA) as it assumes the lateral electric field varies gradually along the channel such that it has no effect on the charge distribution along the direction perpendicular to the channel. Pao and Sah [20] derived the double-integral solution for the drain current. The Pao–Sah double integral is given by

$$I_{ds} = \mu \frac{W}{L} C_{ox} \gamma \int_{V_{sb}}^{V_{sb}+V_{ds}} \int_{\phi_F}^{\phi_s} \frac{e^{(\phi-2\phi_F-V_{cb})/v_{th}}}{\sqrt{\phi_s(y) + v_{th}} e^{(\phi-2\phi_F-V_{cb})/v_{th}}} d\phi dV_{cb}. \quad (2.1)$$

The double-integral model is physical and accurate for long channel devices, but computationally very intensive and provides little intuition to the circuit designers, and hence, cannot be used in compact models. At the same time, till today the Pao–Sah double-integral expression remains the benchmark for other compact models.

The double integral model can be further simplified with the help of Charge Sheet Approximation (CSA) which assumes that the inversion layer is a sheet of electrons (or holes for pMOS) of zero thickness. All current MOSFET models are based on the CSA [21], [22]. They assume that the inversion layer is infinitesimally thin, that is, the potential does not vary through the thickness of the inversion layer. Charge Sheet Approximation has been used in three different ways resulting in three different approaches to Compact Model Development:

1. Threshold-voltage based models;
2. Surface-potential based models;
3. Charge-based models.

2.1.1 Threshold-voltage based models

The early SPICE models needed simple and computationally less intensive solutions. The threshold-voltage based models do not require the calculation of surface potential. This model assumes that the surface potential has a linear dependence on the gate and drain voltages in the sub-threshold region and the surface potential is pinned to a constant value ($2\phi_F + V_{cb}$) when the gate voltage is higher than the threshold voltage. This simple assumption makes the core of the threshold-voltage based models. Threshold-voltage based models are not very accurate in the strong-inversion region. To improve the accuracy, different correction terms have been incorporated into the models in a semi-empirical way. The threshold-voltage based models inherently have different solutions in different regions of operations of the device, which have to be unified using mathematical functions. SPICE and SPICE-like simulators demand continuity of model even in higher-order derivatives for AC and distortion analyses. Further, to provide an accurate

representation of terminal behavior for all dimensions that the circuit design people can use, the threshold-voltage based models use a “binning” approach for geometry scaling. Thus, a large number of empirical model parameters are used in threshold-voltage based models to capture the short-channel and higher-order effects. Another difficulty that comes to the fore for threshold voltage based models is lack of symmetry. The MOS transistor is inherently symmetrical device with respect to interchange of drain and source terminal. Therefore, the mathematical smoothing in threshold-voltage based models has to be chosen with caution to preserve symmetry and higher-order continuity. MOS Model 9, BSIM3 and BSIM4 [23]-[26] are some of the popular threshold-voltage based models in use at present.

2.1.2 Surface-potential based models

MOSFET theory was initially derived by Pao and Sah in the 1960's [20], [27]. The carrier charge was related to the potential at the insulator- substrate interface – so called surface potential. The Pao–Sah model uses a double-integral solution (equation 2.1) to calculate the drain current in the device. By applying the GCA, a 1-D Poisson equation linking the gate voltage with the surface potential can be derived. This equation is implicit and needs to be solved iteratively. With the computational power available in those times, the earlier SPICE models could not afford the numerical iterative approach. After 40 years of hibernation, the surface-potential based models are starting to get increased attention. High computational power and advanced iteration techniques have made calculation of surface potential quite affordable. Models like HiSIM [28], [29] and MOS Model 11 [30], [31] use an iterative approach to calculate the surface potential, while PSP model [32], [33] uses an explicit expression based approach to model the

surface potential. In surface-potential based models, the charge and drain current are calculated from the surface potentials at the source and drain ends. In explicit models, it is not possible to get a surface potential in all regions. The holes for nMOS (and electrons for pMOS) are usually neglected in the solution to keep the problem tractable. Different mathematical techniques have been employed to arrive at an explicit expression for surface potential [32].

2.1.3 Charge-based models

EKV, ACM and BSIM5 are some of the popular inversion-charge based models [34]-[36]. The input-voltage equation is derived as a relation between the node charges and the terminal voltages. The charge-based models are derived based on modeling the g_m/I_d characteristics accurately which is important from analog circuit design point of view. They are targeted mainly for analog applications. The output-current equation is also expressed as a function of the node charges. Charge is the independent variable in these derivations. These models are again based on the GCA and the CSA assumptions. The bulk charge and inversion charge are linearized with respect to surface potential at each gate bias. The drain current is a quadratic and linear function of the drain/source-end charge densities. Accumulation region still needs to be modeled separately in the charge-based models.

2.2 Modeling Non-Classical CMOS Structures

Conceived in Lilienfield's historical patent issued in 1926 and delivered in the late 1960s, planar bulk MOS transistors have been the basic building block in IC's since the dawn of the semiconductor industry. As MOSFETs are approaching their physical scaling limits – it is becoming extremely difficult to achieve the same gate control over

the channel as is desired by the circuit applications beyond 45nm node. Alternative device architectures like multiple-gate structures, ultra-thin body SOI and strained-silicon MOSFETs are being explored for further scaling. Bulk MOSFET models have been developed for four decades and form the backbone of the IC design landscape. Bulk MOSFET models have been able to cater to different technology nodes but with the addition of a sizeable number of model parameters to account for the higher-order effects which are becoming more and more prominent with scaling. However, the question remains whether these models can maintain this trend as the industry shifts to non-classical CMOS? As we slowly move to non-classical MOSFETs, there are several issues that need to be addressed.

1. Can our existing bulk MOSFET models cater to different device topologies with more empirical parameters, or do we need to develop models taking into account the physically correct boundary conditions?

The designers consider compact models as a black-box that gives the terminal electrical characteristics for any given set of inputs. With so much efforts already having been put into the development of bulk models, do we start afresh for non-classical MOSFETs or do we add more empirical parameters to the existing bulk MOSFET models to fit non-classical devices? The advanced bulk MOSFET models may be able to predict certain device types with some more empirical fitting parameters. But, the advanced MOSFET models already have hundreds of fitting parameters and more empirical parameters are only going to make the extraction more tedious and cumbersome with parameters values becoming more and more non-physical. With the new physics related to non-classical device

structures missing in the bulk MOSFET models, extending bulk model to non-classical MOSFET may lose scalability. Also, bulk MOSFET models may miss some new device physics like floating-body effects in SOI [37], the capacitance plateaus in strained-silicon MOSFETs [38] and the volume inversion in DG MOSFETs [39]. Hence, it is very important to develop physical models that are predictive and scalable rather than just fitting the bulk MOSFET models to match non-classical CMOS devices.

2. Do we develop and standardize different models for different types of device structures or operations and let the designer choose the model, or do we develop a “universal” model that switches seamlessly between different device types and topologies?

There are currently different models for bulk and SOI MOSFETs. Lot of effort is also being put into the modeling of the multiple-gate MOSFET device structures. Though different devices like bulk, SOI and DG MOSFETs are being modeled considering their own unique physics, the different devices are basically built by small variations in the structures in terms of silicon thickness, oxide layer thickness and work functions of the different gates. Figure 2.1 shows the seamless transition of devices across different topologies [40], [41]. When the silicon layer thickness of a partially-depleted (PD) SOI MOSFET is scaled down and it is comparable with the depletion width, then the substrate is fully depleted and we get a Fully-Depleted (FD) SOI MOSFET. If the back oxide thickness of a FD SOI MOSFET is scaled and is comparable to the front oxide thickness, it forms an Asymmetric Double Gate (a-DG) MOSFET. When the oxide thickness and work

functions of the top and bottom gates are the same, it forms a Symmetric Double-Gate (s-DG) MOSFET. Half of an s-DG MOSFET can also be modeled as an ultra-thin body “bulk” MOSFET. When the thickness of the substrate is larger than the maximum depletion widths, the device goes back to a PDSOI MOSFET which has the same boundary conditions as bulk-MOS for the 1-D solution.

Figure 2.1: Seamless transition of devices across various topologies [40].

As mentioned before, all compact models start with the basic 1-D Poisson equation. The model equations for different type of devices are derived by solving the Poisson's equation with the appropriate boundary conditions. If the models are derived with the correct physics built into it, there should be a possibility of capturing the seamless transition between different device models based on the

boundary conditions and structural parameters. The boundary conditions for these devices can be written as

- Bulk $\phi_b = 0$ and $\phi'_b = 0$
- PD-SOI $\phi_b = 0$ and $\phi'_b \approx 0$
- FD-SOI $\phi_b \neq 0$ and $\phi'_b \neq 0$
- a-DG $\phi_b \neq 0$ and $\phi'_b \neq 0$
- s-DG $\phi_0 \neq 0$ and $\phi'_0 = 0$

where ϕ_b is the potential at the back gate and ϕ_0 is the potential at the mid-point of s-DG MOSFET channel. Even the 2-D short-channel effects can be captured across various topologies by deriving the 2-D effects based on quasi 2-D solutions. Our basic idea is to develop a unified model, which is scalable across different bias, geometry and different MOSFET device structures.

2.3 The Unified Regional Approach

In this section, the unified regional model (URM) for bulk CMOS developed by Chiah [42] is reviewed, on which this research is based as an extension of the approach to strained-silicon and DG MOSFET modeling. Threshold-voltage based models pin the surface potential at $2\phi_F$, where ϕ_F is the bulk Fermi potential. This approximation is neither physical nor accurate in the moderate and strong inversion. Further, the threshold-voltage based models may suffer from the issue of symmetry with reference to source and drain terminals. The industry is slowly shifting its focus to surface-potential based models. The surface-potential based models demand high accuracy of surface potential as the charge and the current are exponentially related to the difference between the surface

potentials and quasi-Fermi potentials at the source and the drain ends. Surface-potential solutions can only be calculated numerically. Now people tend to use different mathematical tricks and approximations to solve for the surface potential analytically. Solving the surface potential physically at the flat-band condition and at the threshold-voltage conditions is not trivial [43]. In this thesis, we propose a unified regional approach to modeling the surface potential, charge and current [44].

The 1-D Poisson equation of a bulk MOSFET can be written as

$$\frac{d^2\psi}{dx^2} = -\frac{\rho}{\epsilon_{Si}} = -\frac{q(p-n+N_D-N_A)}{\epsilon_{Si}} = \frac{q}{\epsilon_{Si}}(n-p+N_A-N_D). \quad (2.2)$$

The holes and electrons can be expressed in terms of the intrinsic concentration and Fermi potential, under the assumption of no carrier generation and recombination in the silicon, as shown below

$$n = n_i e^{(\psi - \phi_F - V_{cb})/v_{th}} \quad (2.3)$$

$$p = n_i e^{-(\psi - \phi_F)/v_{th}} \quad (2.4)$$

The acceptor and donor concentration for a p-substrate in nMOSFETs can be expressed below to ensure neutrality in the deep bulk with constant quasi-Fermi Levels [20]:

$$N_A = n_i e^{\phi_F/v_{th}} \quad (2.5)$$

$$N_D = n_i e^{-(\phi_F + V_{cb})/v_{th}} \quad (2.6)$$

where ϕ_F is the Fermi potential, V_{cb} is the channel-bulk voltage, n_i intrinsic carrier concentration, and v_{th} is the thermal voltage. We can rewrite the Poisson's equation from (2.1) in the form

$$\frac{d^2\psi}{dx^2} = \frac{q}{\epsilon_{Si}} \left[n_i e^{(\psi - \phi_F - V_{cb})/v_{th}} - n_i e^{-(\psi - \phi_F)/v_{th}} + n_i e^{\phi_F/v_{th}} - n_i e^{-(\phi_F + V_{cb})/v_{th}} \right]. \quad (2.7)$$

By using the relation $N_A = n_i e^{-\phi_F/v_{th}}$, we can rewrite (2.7) in the form

$$\frac{d^2\psi}{dx^2} = \frac{qN_A}{\epsilon_{Si}} \left[e^{(\psi-2\phi_F-V_{cb})/v_{th}} - e^{-\psi/v_{th}} + 1 - e^{-(2\phi_F+V_{cb})/v_{th}} \right]. \quad (2.8)$$

The 1-D Poisson equation (2.8) is the starting point for all different devices. The devices are then modeled based on the boundary conditions applied to the Poisson equation. The 1-D Poisson equation is integrable and we can get an expression for the field. For a bulk MOSFET, the following boundary conditions are applied to the integral, assuming that the electric-field and potential in the region beyond the maximum depletion width are zero

$$\begin{aligned} \psi(0, y) &= \phi_s(y) \\ \psi(x_d, y) &= 0 \\ \psi'(x_d, y) &= 0 \end{aligned} \quad (2.9)$$

The field equation is given by the expression

$$-\frac{d\psi}{dx}\bigg|_{x=0} = E_{Si} = \sqrt{\frac{2qN_A}{\epsilon_{Si}}} \sqrt{v_{th} \left(e^{-\phi_s/v_{th}} - 1 + \frac{\phi_s}{v_{th}} \right) + v_{th} e^{-(2\phi_F+V_{cb})/v_{th}} \left(e^{\phi_s/v_{th}} - 1 - \frac{\phi_s}{v_{th}} \right)}. \quad (2.10)$$

From the charge-balance equation, we can relate the gate charge, space charge and the fixed oxide charge by the expression

$$\begin{aligned} Q_g &= -(Q_{sc} + Q_{ox}) \\ Q_g + Q_{ox} &= -Q_{sc} \end{aligned} \quad (2.11)$$

The gate charge and the space charge can be calculated from the boundary condition

$$\begin{aligned} Q_g &= \epsilon_{ox} E_{ox} \\ Q_{sc} &= -\epsilon_{Si} E_{Si} \end{aligned} \quad (2.12)$$

The electric field at the oxide–silicon interface in the oxide region can be written by taking the electrostatic potential as the line integral of electric field,

$$E_{ox} = \frac{V_{ox}}{t_{ox}} = \frac{V_{gb} - \phi_{MS} - \phi_s}{t_{ox}}. \quad (2.13)$$

Now from (2.10), (2.11), (2.12) and (2.13), we can derive the charge balance equation for a bulk MOSFET

$$\begin{aligned} & C_{ox}(V_{gb} - \phi_{MS} - \phi_s) + Q_{ox} \\ &= \text{sgn}(\phi_s) \sqrt{\frac{2qN_A}{\epsilon_{Si}}} \sqrt{v_{th} \left(e^{-\phi_s/v_{th}} - 1 + \frac{\phi_s}{v_{th}} \right) + v_{th} e^{-(2\phi_F + V_{cb})/v_{th}} \left(e^{\phi_s/v_{th}} - 1 - \frac{\phi_s}{v_{th}} e^{V_{cb}/v_{th}} \right)}. \end{aligned} \quad (2.14)$$

Rewriting the charge balance equation in (2.14) we get the voltage balance equation as

$$\begin{aligned} & V_{gb} - V_{FB} - \phi_s \\ &= \text{sgn}(\phi_s) \gamma \sqrt{v_{th} \left(e^{-\phi_s/v_{th}} - 1 + \frac{\phi_s}{v_{th}} \right) + v_{th} e^{-(2\phi_F + V_{cb})/v_{th}} \left(e^{\phi_s/v_{th}} - 1 - \frac{\phi_s}{v_{th}} e^{V_{cb}/v_{th}} \right)} \end{aligned} \quad (2.15)$$

where the body factor is given by $\gamma = \sqrt{2\epsilon_{Si}qN_A}/C_{ox}$ and the flat-band voltage is given by

$$V_{FB} = \phi_{MS} - \frac{Q_{ox}}{C_{ox}}. \quad (2.16)$$

The field equation (2.10) is not integrable second time and the surface potential can only be calculated by numerical iteration. We adopt a unified regional approach to calculate the surface potentials for different bias regions and unify them using smoothing functions.

2.3.1. Piecewise solutions

Piecewise regional ϕ_s solutions can be easily obtained by solving the Pao–Sah equation in different bias regions under appropriate physically valid assumptions. In the accumulation region, there is no depletion of acceptors or significant concentration of electrons. Hence we can consider only the holes and neglect the electrons, donors and

acceptor terms in the Poisson's equation. The regional Pao–Sah equation for accumulation region is written in the form

$$V_{gb} - V_{FB} - \phi_s = -\gamma \sqrt{v_{th}} e^{-\phi_s/v_{th}}, \quad (V_{gb} < V_{FB}). \quad (2.17)$$

Let us assume $v_{gf} = (V_{gb} - V_{FB})/v_{th}$, $\phi_s = \phi_s/v_{th}$, $G = \gamma/\sqrt{v_{th}}$, $X = e^{-\phi_s/2}$, then (2.17) can be rewritten as $\ln(G/2) - v_{gf}/2 = \ln(GX/2) + GX/2$. This is a well known Lambert W function form and the exact solution [45] is given by the *Lambert W* function [46], $\mathcal{L}\{w\}$.

$$\begin{aligned} \frac{GX}{2} &= \mathcal{L}\{w\}, \quad w = (G/2)e^{-v_{gf}/2}, \\ \phi_{cc} &= V_{gb} - V_{FB} + 2v_{th}\mathcal{L}\{w\}, \quad (V_{gb} < V_{FB}) \end{aligned} \quad (2.18)$$

The ϕ_{cc} solution is true in the accumulation region, when $V_{gb} < V_{FB}$. The regional Pao–Sah equation for depletion region is written in the form

$$V_{gb} - V_{FB} - \phi_s = \gamma \sqrt{\phi_s}, \quad (V_{gb} > V_{FB}). \quad (2.19)$$

The regional solution can be written in the form

$$\phi_{dd} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{gb} - V_{FB}} \right)^2, \quad (V_{FB} < V_{gb} < V_t). \quad (2.20)$$

The depletion-region solution cannot be extended to below the flat-band as it gives imaginary values due to change in the sign of interface surface potential. In strong inversion, both the acceptor and electron terms have to be included in the regional Pao–Sah voltage equation.

$$V_{gb} - V_{FB} - \phi_s = \gamma \sqrt{\phi_s + v_{th}} e^{(\phi_s - 2\phi_F - V_{cb})/v_{th}}, \quad (V_{gb} > V_t). \quad (2.21)$$

To solve for strong inversion, we try to use the approximation $\phi_B = \phi_{s0} = 2\phi_F$ to get the final solution [47].

$$V_{gb} - V_{FB} - \phi_{s0} = \gamma \sqrt{\phi_{s0} + v_{th} e^{(\phi_s - 2\phi_F - V_{cb})/v_{th}}}, \quad (V_{gb} > V_t) . \quad (2.22)$$

By solving (2.22) for ϕ_s one obtains the regional solution

$$\phi_{ss} = \phi_{s0} + V_{cb} + \Delta, \quad (V_{gs} > V_t) \quad (2.23)$$

where Δ is given by the expression

$$\Delta = v_{th} \ln \left\{ \frac{1}{v_{th}} \left[\left(\frac{V_{gb} - V_{FB} - \phi_{ss}}{\gamma} \right)^2 - (\phi_{s0} + V_{cb}) \right] + 1 \right\} . \quad (2.24)$$

In this way, the complete non-integrable Pao–Sah voltage equation is broken into regional pieces and solved explicitly. These piecewise regional solutions are only valid in their respective regions of operation.

Figure 2.2: Piecewise (lines) ϕ_s solutions, compared with iterative solution (circle).

Figure 2.2 shows the regional piecewise solutions in the accumulation, depletion and inversion regions.

2.3.2. Unified regional solutions

As shown in the previous section, the regional solutions are valid in the respective validity regions only. To get a unified regional solution, the following smoothing functions in [44], [48] are used. The $V_{gb} - V_{FB}$ function can be divided into two complementary functions

$$V_{gbf} = \mathcal{G}_f \{x; \sigma_f\} \equiv 0.5 \left(x + \sqrt{x^2 + 4\sigma_f} \right) \quad (2.25a)$$

$$V_{gbr} = \mathcal{G}_r \{x; \sigma_a\} \equiv -0.5 \left(-x + \sqrt{x^2 + 4\sigma_a} \right) \quad (2.25b)$$

where $x = V_{gb} - V_{FB}$, which are used to get two complementary functions, V_{gbf} and V_{gbr} . These complementary functions are valid in the accumulation and depletion regions respectively and then get pulled to zero in the other regions. Thus, they can be added appropriately to obtain the $V_{gb} - V_{FB}$ function valid in both regions. These complementary functions are used in the regional accumulation and depletion solutions (2.18) and (2.20) to get a unified regional solution.

$$\phi_{acc} = V_{gbr} + 2v_{th} \mathcal{L} \{w\} \quad (2.26)$$

$$\phi_{sub} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{gbf}} \right)^2 \quad (2.27)$$

The complementary functions can be added together to obtain a solution from accumulation to depletion ($\phi_{sa} = \phi_{sub} + \phi_{acc}$) due to the identity relation $V_{gbf} + V_{gbr} = V_{gb} - V_{FB}$. The unified solutions follow the regional solutions in their regions of operation and are then controlled by the smoothing function in the transition region. Similarly, Δ in (2.24) is smoothed out by $\Delta = v_{th} \ln(b_{eff})$, where

$$b_{eff} = \frac{1}{v_{th}} \mathcal{G}_f \left\{ \left(\frac{V_{ga}}{\gamma} \right)^2 - (\phi_{s0} + V_{cb}); \sigma_{eff} \right\} + 1 \quad (2.28)$$

$$V_{ga} = \mathcal{G}_f \{ V_{gb} - V_{FB} - \phi_{str}^*; \sigma_{vga} \} \quad (2.29)$$

$$\phi_{str}^* = \phi_{s0} + V_{cb} + \frac{\phi_{sub} - (\phi_{s0} + V_{cb})}{\sqrt{1 + \left[\frac{\phi_{sub} - (\phi_{s0} + V_{cb})}{4v_{th}} \right]^2}} \quad (2.30)$$

to obtain the unified regional “non-pinned” ϕ_s solutions: $\phi_{str,(s/d)} = \phi_{s0} + V_{(s/d)b} + \Delta_{(s/d)}$ where $\Delta_s = v_{th} \ln(b_{eff})|_{V_{cb}=V_{sb}}$ and $\Delta_d = v_{th} \ln(b_{eff})|_{V_{cb}=V_{db}}$ are evaluated at the source and drain ends, respectively. A unified solution ϕ_{ds} from the depletion to strong inversion can be obtained by using the smoothing function

$$\begin{aligned} \phi_{ds} &= \mathcal{G}_{eff} \{ \phi_{sub}, \phi_{str}; \delta \} \\ \mathcal{G}_{eff} \{ x, x_{sat}; \delta \} &\equiv x_{sat} - 0.5 \left[x_{sat} - x - \delta + \sqrt{(x_{sat} - x - \delta)^2 + 4\delta x_{sat}} \right] \end{aligned} \quad (2.31)$$

As we have used two complementary functions in the surface potential calculation, the ϕ_{ds} solution can be added directly with the ϕ_{acc} solution to get a unified single piece non-pinned surface potential ϕ_{seff} . The single piece unified non-pinned surface potential is then valid in all regions of operation. The single piece surface potential solution is not used in the charge and current formulations. We can obtain single piece surface potential solutions which are continuous and smooth across several differentials, but we use our unified regional pieces to calculate the charge and current equations. This is useful in calculating all the individual charges separately. All the charges can then be added to obtain a unified gate charge.

Figure 2.3: Piecewise (crosses) and unified regional (lines) ϕ_s solutions, compared with iterative solution (circle) [44].

Figure 2.3 shows the regional piecewise and unified regional solutions compared with the iterative Newton–Raphson solution giving the exact solution.

Figure 2.4: Unified regional ϕ_s solutions and the combined solutions ϕ_{sa} (accumulation/depletion) and ϕ_{seff} (all region) as well as its 1st/2nd-order derivatives (inset) [44].

Figure 2.4 shows the comparison of the combined unified model with the Newton–Raphson iterative solution. The continuity of the model and matching with higher-order derivatives is also verified. One of the disadvantages of the unified regional modeling approach is the accuracy of the model is not high in the regions where regional solutions are unified, like near the flatband voltage region or the region where the model shifts from depletion to strong inversion. Another disadvantage is the dependence of the accuracy on the smoothing function and model parameter accuracy.

2.3.3. Unified regional charge model

The unified charge expressions across the accumulation, depletion and strong inversion regions are calculated based on the unified regional surface-potential solutions. Though our model has a single piece unified surface potential, the charge model is calculated based on the unified regional surface potential solutions. The accumulation charge is usually assumed to be position independent. The inversion charge can be neglected in this region of operation. The bulk-charge term depends only on the holes in the accumulation region and, hence, can be modeled based on the relation

$$Q_{b,acc} = -C_{ox} (V_{gbr} - \phi_{acc}). \quad (2.32)$$

V_{gbr} and ϕ_{acc} are the unified function and the unified regional accumulation solution. The bulk charge due to the accumulation has an asymptotic solution in the region below flat band. The accumulation charge goes to zero above the flat-band voltage. In the depletion region above flat-band voltage, the bulk charge just constitutes the depletion charge. The depletion charge can be calculated based from ϕ_{sub} the unified regional surface potential solution in the depletion region. The depletion charge can be given by the expression

$$Q_{b,sub} = -C_{ox} (V_{gba} - \phi_{sub}) \quad (2.33)$$

$$Q_{b,sub} = -C_{ox} \left[(V_{gbf} - \phi_{sub}) + (V_{gba} - V_{gbf}) \right]. \quad (2.34)$$

By using the relation $V_{gbf} - \phi_{sub} = \gamma \sqrt{\phi_{sub}}$, we can get the bulk-charge expression

$$Q_{b,sub} = -C_{ox} \left[(V_{gba} - V_{gbf}) + \gamma \sqrt{\phi_{sub}} \right]. \quad (2.35)$$

The unified depletion solutions calculated based on the left-hand side and right-hand side of the Pao–Sah equation are shown in (2.33) and (2.35). The bulk charge consists of the holes and depletion charge. A unified bulk-charge solution valid from accumulation to depletion can be given by

$$Q_{b,sa} = Q_{b,acc} + Q_{b,sub}. \quad (2.36)$$

In the strong inversion region, the depletion width remains a constant and the bulk charge ceases to increase. A unified bulk-charge model valid from accumulation to strong inversion can be obtained by replacing the ϕ_{sub} in the $Q_{b,sub}$ model with the ϕ_{ds} expression in (2.31)

$$Q_{b0} = Q_{b,acc} + Q_{b,ds} \quad (2.37)$$

where $Q_{b,ds}$ is given by the expression

$$Q_{b,ds} = -C_{ox} \left[(V_{gba} - V_{gbf}) + \gamma \sqrt{\phi_{ds}} \right]. \quad (2.38)$$

Threshold-voltage based models use a pinned surface potential in the strong inversion. This is not accurate in the moderate inversion region and the capacitance is inaccurate in the strong inversion. The new unified charge models are derived based on the non-pinned surface potential. The charge balance equation can be written as

$$Q_g(y) = -[Q_i(y) + Q_b(y) + Q_{ox}] \quad (2.39)$$

$$Q_i(y) = Q_{sc}(y) - Q_b(y) \quad (2.40)$$

$$Q_b(y) = -C_{ox}\gamma \operatorname{sgn}[\phi_s(y)] \sqrt{v_{th} \left(\exp\left[\frac{-\phi_s(y)}{v_{th}}\right] - 1 \right) + \phi_s(y)}. \quad (2.41)$$

Figure 2.5: The derivatives of Q_b and its regional components with respect to V_{gb} and the inset shows smoothness of C_{bg} .

And the induced channel charge can be determined by combining the potential balance equation with charge neutrality equation

$$Q_{sc} = -C_{ox} [V_{gb} - V_{FB} - \phi_s(y)]. \quad (2.42)$$

The inversion charge is partitioned into source and drain charges, based on the Ward–Dutton partitioning [49]. The non-pinned surface-potential based URM for charge models are re-derived similar to the V_t -based pinned charge model.

$$Q_d = \frac{Q_D}{WL} = -C_{ox} \left(\frac{V_{gt,\phi}}{2} - \frac{A_{b,\Delta}}{3} V_{d\text{eff},\Delta} + A_{d,\Delta} \right) \quad (2.43)$$

$$Q_s = -C_{ox} \left(\frac{V_{gt,\phi}}{2} - \frac{A_{b,\Delta}}{6} V_{d\text{eff},\Delta} + A_{s,\Delta} \right) \quad (2.44)$$

$$Q_{b, str} = -C_{ox} \left(\gamma \sqrt{\phi_{str, s}} + D_{b, \Delta} \right) \quad (2.45)$$

The auxiliary functions are given by

$$A_{s, \Delta} = \mathcal{A}_{\Delta} (1 - \mathcal{B}_{\Delta}) \quad (2.46)$$

$$A_{d, \Delta} = \mathcal{A}_{\Delta} \mathcal{B}_{\Delta} \quad (2.47)$$

$$D_{b, \Delta} = (A_{b, \Delta} - 1) V_{deff, \Delta} \mathcal{D}_{\Delta} \quad (2.48)$$

$$\mathcal{A}_{\Delta} = \frac{A_{b, \Delta}^2 V_{deff, \Delta}^2}{12 (V_{geff, \Delta} - 0.5 A_{b, \Delta} V_{deff, \Delta})} \quad (2.49)$$

$$\mathcal{B}_{\Delta} = \frac{5 V_{geff, \Delta} - 2 A_{b, \Delta} V_{deff, \Delta}}{10 (V_{geff, \Delta} - 0.5 A_{b, \Delta} V_{deff, \Delta})} \quad (2.50)$$

$$\mathcal{D}_{\Delta} = \frac{3 V_{geff, \Delta} - 2 A_{b, \Delta} V_{deff, \Delta}}{6 (V_{geff, \Delta} - 0.5 A_{b, \Delta} V_{deff, \Delta})} \quad (2.51)$$

V_{geff} and V_{deff} are modified to

$$V_{geff, \Delta} = \frac{2 n v_{th} \ln \left(1 + e^{(V_{gs} - V_{t, \phi}) / (2 n v_{th})} \right)}{1 + 2 n (C_{ox} / C_d) e^{-(V_{gs} - V_{t, \phi} - 2 V_{off}) / (2 n v_{th})}} \quad (2.52)$$

and

$$V_{deff, \Delta} = V_{deff} + \Delta_{EFF, ds}, \quad (2.53)$$

$$V_{gt, \phi} = n v_{th} \ln \left(1 + e^{(V_{gs} - V_{t, \phi}) / (n v_{th})} \right). \quad (2.54)$$

The complete set of URM equations can be found in [42]. The capacitances are calculated by numerical differentiation of the respective charges and are given by the expression

$$C_{ij} = \delta_{ij} \frac{\partial Q_i}{\partial V_j}, \quad \delta_{ij} = \begin{cases} 1 & (i = j) \\ -1 & (i \neq j) \end{cases}. \quad (2.55)$$

Figure 2.6 shows the components of bulk charge and the inset shows the tuning of the complimentary functions at flat-band voltage to maintain charge neutrality. Figure 2.7 shows the comparison of drain and source capacitance with Medici data. The inset also shows the source and drain charges that constitute the inversion charge.

Figure 2.6: Unified regional bulk charge in accumulation ($Q_{b,acc}$) and depletion/inversion ($Q_{b,ds}$) and the V_{ds} -dependent component ($-C_{ox}D_{b,\Delta}$). The inset shows tuning for charge neutrality at flat band [44].

Figure 2.7: Channel, drain, source capacitances from the derivatives of Q_i , Q_d , Q_s (inset), compared with Medici data (symbols) [42].

CHAPTER 3 STRAINED-SILICON / SILICON-GERMANIUM MOSFET MODELING

The semiconductor industry has been driven by the tremendous scientific and manufacturing advancement that has centered on Si CMOS technology. Perhaps the most telltale sign of the changing Si industry is that new materials are being taken seriously as replacements for SiO_2 as the gate dielectric and isolation layer, metal gates for polysilicon as the gate electrode, and strained silicon for Si as the conducting channel. These materials are required to continue the steady progression of CMOS technology. One of the most interesting of these material changes involves the Si substrate itself. Silicon has been the workhorse of the semiconductor industry, but its fundamental properties in terms of carrier mobility and associated intrinsic performance are reaching their limits. These limitations start to become showstoppers for further enhancement of performance for various applications and the Si substrate material is being replaced by strained silicon, silicon-germanium and high-speed semiconductor materials. On the immediate horizon, one of the most promising candidates for the replacement of bulk-Si channels in the CMOS technology is the strained Si.

Strained-Si technology enables improvements in CMOS performance and functionality via replacement of the bulk, cubic-crystal Si substrate in the channel region with a Si substrate that contains a tetragonally distorted, biaxially strained Si thin film at the surface. Due to changes in its crystalline structure (i.e., its symmetry is different due to its strain state), the strained-Si film has electronic properties that are superior to those of bulk-Si. Specifically, the strained-Si film has larger electron and hole mobilities, which translate into larger drive current capabilities for nMOS and pMOS transistors. It is

quite a challenge to incorporate the strained-Si behavior in compact models because new physical effects such as reduced band gap, band offsets, and higher mobility have to be considered.

3.1 Strained-Si/SiGe Channel Devices

Strain can be introduced in the channel by a number of methods. Strain can be induced by a nitride capping layer on top of the gate, a silicon germanium source/drain junction or by epitaxially growing a layer of silicon on top of a SiGe substrate. Unwanted strain is also introduced during various steps of processing like shallow trench isolation (STI), silicidation, etc.

In this chapter, we extend our unified regional modeling approach to strained-Si based hetero-structure MOS devices.

3.1.1 Lattice structure

The $\text{Si}_{1-x}\text{Ge}_x$ alloy is with Ge occupying the substitutional sites and can be viewed as a crystal in which a fraction x of the Si atoms have been replaced by Ge atoms. The difference in lattice constants between Si and Ge ($\approx 4.2\%$) has a large impact on the properties of the resulting alloy. The macroscopic lattice constant of a uniformly mixed alloy can be approximated by a linear interpolation between the lattice constants of pure Si and pure Ge.

$$a_{\text{SiGe}} = a_{\text{Si}}(1-x) + a_{\text{Ge}}(x) \quad (3.1)$$

where x is the mole-fraction of Ge in the mixture. As the lattice constant varies as a function of germanium mole-fraction, there will be a lattice mismatch between the epitaxial layer and the lattice substrate when SiGe is used with Si or Ge. When a thin epitaxial layer is grown on a substrate, the film is forced to adopt the lattice constant of

its host substrate. The stress imposed by the substrate deforms the crystal and this deformed crystal is known as pseudomorphic. In the plane parallel to the substrate interface it acquires the lattice structure of the host substrate. When the film exceeds a critical thickness, dislocations form to relieve the strain and the film relaxes. The critical thickness is fundamentally a function of the lattice mismatch. The maximum thickness of the pseudomorphic layer at which it is thermodynamically stable is referred to as the “critical layer thickness”. It is one of the most important parameters in the pseudomorphic growth of heteroepitaxial films.

Strained-Si is the result of depositing a thin film of Si on top of a relaxed SiGe substrate. This material will be under tensile strain and the in-plane lattice constant will be increased above its equilibrium value.

Figure 3.1: The lattice structure of relaxed SiGe (top) and silicon (bottom).

The lattice structure of relaxed silicon and silicon germanium are shown in Fig. 3.1. If layers are grown below the critical thickness then they become strained with the lattice symmetry changing from cubic to tetragonal as shown in Fig. 3.2. If the thickness of the strained layer exceeds the critical thickness, dislocations are formed as shown in Fig. 3.3 and the strain is relieved.

Figure 3.2 Strained silicon on top of relaxed SiGe.

Figure 3.3: Strain in silicon layer relieved due to misfit dislocations as it is grown above the critical thickness.

3.1.2 Band alignment

Band alignments giving rise to band offsets or band discontinuities are very important for junction device applications. In a MOSFET it controls the amount of charge carrier confined in the high mobility channel. Strain-induced modification of Si/SiGe films is said to have a significant impact on the band structure and carrier transport.

3.1.2.1 Effect of strain on the conduction-band

The ellipsoidal six-fold degenerate valleys in the silicon conduction band are shown in Fig. 3.4. Strain causes this 6-fold degenerate band to split into a 2-fold degenerate, perpendicular band Δ_2 and a 4-fold in-plane degenerate band Δ_4 [50]. In compressive strain the Δ_4 band moves lower in energy compared to the Δ_2 band, while in the tensile strain the Δ_2 forms the lower conduction-band.

Figure 3.4: (a) A six-fold degenerate silicon conduction-band minima; (b) the two dark ellipsoids are up in energy while the four white ellipsoids are down in energy; (c) the two perpendicular ellipsoids are down in energy while the four ellipsoids are up in energy [51].

3.1.2.2 Effect of strain on the valence-band

The effect of compressive and tensile strain on the valence-band is shown in the Fig. 3.5. In both cases the degeneracy between the LH (Light Holes) band and the HH (Heavy Holes) band is lifted and the valence-band maxima are higher in energy compared to the unstrained case [52], [53], [54]. Strain also reduces the in-plane effective mass of the holes. Fig. 3.5 shows the effect of strain on the valence band. Strain removes the degeneracy between the LH band and HH band hence improving the hole-mobility.

Figure 3.5: Valence band under different strain conditions. Strain is found to remove the degeneracy between the LH band and the HH band [52]. (What is SO in the figure?)

3.1.2.3 Strained Si_{1-x}Ge_x on relaxed silicon

When a thin film with a large lattice constant is grown on a smaller lattice constant substrate, the film maintains the in-plane lattice constant of the substrate and is under a biaxially compressive strain [55]. Figure 3.6 shows the resultant band offset between a strained-SiGe film grown on Si. This structure shows a type I band alignment where the entire band offset occurs in the valence-band, while the band offset in the conduction-band is very small. This type of structure is favorable for confinement of holes and is used in pMOSFETs

Figure 3.6: Band offset between compressively strained Si_{0.7}Ge_{0.3} and silicon [57].

3.1.2.4 Strained-silicon on relaxed $\text{Si}_{1-x}\text{Ge}_x$

When a thin silicon epi-layer is grown on a relaxed SiGe layer it shows a Type II band alignment as shown in Fig. 3.7. Type II band alignment has several advantages over the common type I band alignment as it has a band offset in both the valence band and the conduction band [56], [57], [58]. So, strained-Si layers have very high electron and hole mobilities, which allows band gap engineering in the column IV material system to realize strained-Si based CMOS technology.

Figure 3.7: Band offset between tensile strained-Si and relaxed SiGe [57].

3.1.3 Mobility

Low-field mobility is given by

$$\mu = \frac{q\tau}{m^*} \quad (3.2)$$

where q is the electronic charge, τ is the momentum relaxation time and m^* is the conductivity effective mass.

3.1.3.1 Relaxed SiGe

The mobility in such alloys is generally lower than in bulk Si until the alloy approaches pure Ge [59]. This is due to the alloy scattering. The random distribution of

Si and Ge atoms in the lattice causes a variation in the potential, which tends to scatter the carriers strongly.

3.1.3.2 Strained SiGe

In both the compressive and tensile strain we have splitting of light-hole and heavy-hole bands. In the case of strained SiGe on relaxed Si we have compressive strain, so the heavy-hole band is higher in energy and dominates the transport [60]. The density of states and the effective mass are both reduced compared to bulk Si as a result of the compressive strain. Strained SiGe devices exhibit a high hole mobility compared to the bulk Silicon.

3.1.3.3 Strained silicon

Strained silicon grown on relaxed silicon germanium is advantageous as it exhibits enhanced electron mobility and it also retains a very good Si/SiO₂ interface. It serves as a potential well for both electrons and holes, hence, can be used both as a surface channel and a buried channel.

3.1.3.4 Effective mass and phonon scattering

The enhancement of mobility in strained-Si is due to the reductions in the carrier conductivity effective mass and the inter-valley scattering rates. In strained-Si grown on relaxed SiGe, the Si 6-fold degenerate valley is split into 2-fold and 4-fold degenerate valleys and the Δ_2 minimum is lower in energy with respect to the Δ_4 minima and is, thus, preferentially occupied by the conduction electrons.

The conductivity effective mass m^* for transport parallel to the interface in bulk Si is determined from the contribution of all 6 valleys and is given by

$$\frac{1}{m^*} = \frac{1}{3} \left(\frac{1}{m_l} + \frac{2}{m_t} \right) \quad (3.3)$$

where m_l is the longitudinal mass and m_t is the transverse mass of any one valley. In tensile strained-Si only the transverse masses of the Δ_2 minima contribute for transport perpendicular to the growth direction. Thus the effective mass in this case is given by

$$\frac{1}{m^*} = \frac{1}{m_t}. \quad (3.4)$$

The value of m_l and m_t do not change significantly from their bulk Si value [61]. As the electrons have a smaller effective mass in the transverse direction, there is a decrease in the effective mass which, in turn, causes an increase in the electron mobility. At room temperature phonon scattering is more important and the mobility in strained-Si is increased even further over bulk silicon due to a reduction in inter-valley scattering between the Δ_2 and Δ_4 minima. This increases the mobility through an increase in the energy relaxation time, τ .

3.1.3.5 High field velocity saturation and overshoot

As the electric field parallel to the current flow is increased the electron drift velocity increases and reaches the saturation value. These high electric fields are very common in short-channel devices and are a major limiting factor.

As can be seen in Fig. 3.8, as the electric field increases and the velocity saturates, the calculated difference between the electron velocities for strained and unstrained cases also diminishes.

Figure 3.8: Calculated drift velocity at high electric field in strained and unstrained-Si [62].

3.1.3.6 Mobility summary

The lattice structure, band alignment and the transport properties of strained-Si and strained-Si germanium were discussed. The low-field mobility of these materials can be summarized in Table 3.1.

Table 3.1 Properties of strained materials

	Strained Si _{0.7} Ge _{0.3} on relaxed Si	Strained Si on relaxed Si _{0.7} Ge _{0.3}
Electron mobility (cm ² /Vs)	350 ^a	2830 ^b /1100 ^c
Hole mobility (cm ² /Vs)	630 ^d	1760 ^e /190 ^f

- a Theory [63]
- b Measured, buried channel [64]
- c Measured, surface channel [59]
- d Measured, buried channel [65]
- e Theory, buried channel [66]
- f Measured, surface channel [59]

3.1.4 Surface and buried channel strained-Si MOSFET

In the previous sections, the different band offsets and transport properties were studied. Based on the band offset and molbility, we can design different architecture of devices which make use of the Si and SiGe stained layers.

3.1.4.1 nMOS structures

Figure 3.9 shows the layer structures of several types of nMOS devices based on strained-Si. Figure 3.9 (a) is the most widely used structure for nMOS. A surface channel strained-Si nMOS with a strained layer on top of a relaxed-SiGe buffer [67]. Figure 3.9 (b) shows a buried-channel strained-Si nMOS, with a relaxed SiGe cap layer on top of the strained-Si channel [68]. The mobility in the channel is improved further due to the reduction in interface scattering. But in high fields, inversion charges also form at the top surface and a parasitic channel is formed. Fig. 3.9 (c) includes a modulation doping layer below the channel and the channel is undoped [69]. This is to reduce the impurity scattering in the channel.

Figure 3.9: Layer structures of strained-Si based nMOS devices.

3.1.4.2 pMOS structures

Many groups have tried to use the surface-channel strained-Si MOSFET for both the nMOS and the pMOS devices, due to their high hole and electron mobilities. Figure 3.10 (a) shows a typical surface-channel strained-Si device structure [70] [71]. Figure 3.10 (b) shows the typical buried-channel strained-Si pMOS [72] [73]. The strained-SiGe channel has a higher hole mobility due to the compressive strain in the channel. The cap layer is used to get a good quality oxide and to reduce interface scattering. Figure 3.10 (c) shows the buried-channel device with a modulation doping layer introduced to reduce impurity scattering in the channel [74].

Figure 3.10: Layer structures of strained-Si based pMOS devices.

3.2 Threshold Voltage Model

Threshold voltage of a MOSFET is one of the most important parameters in device design and modeling and circuit design. Threshold voltage has been the fulcrum of

all previous generation threshold-voltage based compact models, but the recent advanced surface-potential based compact models do not use the concept of threshold-voltage. Our Unified Regional Modeling approach uses the length/width dependent threshold-voltage model to capture all the geometry and bias dependency in the drain current.

3.2.1 Threshold voltage definitions

There are several threshold-voltage definitions that has been used in the literature [75] with specific emphasis on its measurement/extraction. The constant-current method is the de facto industry standard. A combination of maximum- g_m and constant-current method is used in the URM approach.. The linear threshold-voltage for each device is determined from linear extrapolation of the I_{ds} - V_{gs} curve to zero I_{ds} from the point where the transconductance (g_m) peaks. The corresponding critical current (I_{crit}) at $V_{gs}=V_{t0}$ is interpolated from the $\log(I_{ds})$ vs. V_{gs} curve [76]. Figure 3.11 shows the maximum- g_m method to determine the linear threshold-voltage. The critical current is used in the determination of threshold-voltage at different substrate and drain bias. The extracted critical current is scaled with W/L and is used for the extraction of threshold-voltages at different lengths and widths.

Figure 3.11: The maximum transconductance V_i definition and $I_{crit}@V_{i0}$, used in the constant current definition [77].

3.2.2 Threshold voltage of a surface-channel strained-Si device

An analytical threshold-voltage model is derived from Poisson's equation for a surface-channel strained-Si nMOS transistor. The threshold-voltage model is described in terms of structure, energy band and material parameters. The cross-section of a surface-channel strained-Si nMOS is shown in Fig. 3.12. The structure consists of a thin layer of strained-Si grown on top of a relaxed SiGe buffer layer.

Figure 3.12: Schematic of a surface-channel strained-Si nMOSFET.

For very small drain voltages and long-channel, the gradual channel approximation can be employed.

$$\frac{\partial^2 \psi}{\partial y^2} \approx 0. \quad (3.5)$$

In the depletion region, we can neglect the holes, electrons and donor terms in the 1-D Poisson's equation. If only the acceptors are considered the Poisson's equation can be integrated twice. In strained-Si MOSFETs the strained layer thickness is thin compared to the depletion width. Depletion layer potential in the SiGe substrate can be written as

$$\phi_3(x) = \frac{qN_A x^2}{2\epsilon_{SiGe}} \quad (t_{Si} < x < x_{d2}). \quad (3.6)$$

When a strained-Si layer is grown on top of a SiGe substrate, there is both a conduction-band offset as well as a valence-band offset in the top strained-Si layer. Hence, the potential at the strained-Si/SiGe interface (as defined in Fig. 3.12), ϕ_{s3} and ϕ_{s2} are linked by the relation $\phi_2(x) = \phi_3(x) + \Delta E_C$. The potential variation in the strained-Si layer can be written as [10], [78].

$$\phi_1(x) = \frac{qN_A x_{d2}^2}{2\epsilon_{SiGe}} + \frac{qN_A t_{Si}^2}{2\epsilon_{SiGe}} + \frac{qN_A t_{Si} x_{d2}}{\epsilon_{Si}} + \Delta E_C \quad (0 < x < t_{Si}). \quad (3.7)$$

The potential across the oxide can be written as

$$\phi_{ox}(x) = \frac{qN_A x_{d2}^2}{2\epsilon_{SiGe}} + \frac{qN_A t_{Si}^2}{2\epsilon_{SiGe}} + \frac{qN_A t_{Si} x_{d2}}{\epsilon_{Si}} + \frac{qN_A t_{ox}(t_{Si} + x_{d2})}{\epsilon_{ox}} + \Delta E_C, \quad (0 < x < t_{ox}). \quad (3.8)$$

The surface potential at threshold is given by the conventional definition

$$\phi_{th} = \frac{2kT}{q} \ln \left(\frac{N_A}{n_i} \right). \quad (3.9)$$

The conduction-band offset at the top layer causes the electrons to invert at the top strained-Si/SiO₂ interface.

$$\phi_{th} = \phi_1(t_{Si}). \quad (3.10)$$

The intrinsic concentration changes with the effective density of states and the energy bandgap. It is given by the expression

$$n_i = \sqrt{N_c N_v} \exp(-E_g/2kT). \quad (3.11)$$

From (3.7), (3.9) and (3.10) the maximum depletion width in the SiGe substrate can be calculated from the expression

$$x_{d2} = \sqrt{t_{Si}^2 - \frac{\epsilon_{SiGe}}{\epsilon_{Si}} t_{Si}^2 + \frac{2\epsilon_{SiGe}}{qN_A} (\phi_{s0} - \Delta E_C) - t_{Si}} \quad (3.12)$$

where $\phi_{s0} = 2\phi_F$ is the surface potential at strong inversion. The threshold voltage is obtained by substituting the boundary condition

$$V_t - V_{FB} = \phi_{ox}(t_{ox}). \quad (3.13)$$

The long-channel linear threshold-voltage is given by the function

$$V_{t0} = V_{FB} + (\phi_{s0} - \Delta E_C) + \frac{qN_A(x_d + t_{Si})}{C_{ox}}. \quad (3.14)$$

As weak inversion and current saturation regions are easy to handle in bulk-referenced models [19], the derivation is done based on bulk reference for the drain current. The model equation is given by

$$V_t = V_{t0} - (A_b - 1)V_{bs} \quad (3.15)$$

where V_{t0} is given by (3.14) and A_b is given by the expression

$$A_b = 1 + \frac{\zeta \cdot \epsilon_{SiGe}}{C_{ox} \sqrt{t_{Si}^2 - \frac{\epsilon_{SiGe}}{\epsilon_{Si}} t_{Si}^2 + \frac{2\epsilon_{SiGe}}{qN_a} (\phi_{s0} - \Delta E_c)}} \quad (3.16)$$

where ζ is a fitting parameter introduced due to the Taylor approximation. It is extracted from one set of V_t vs. V_{bs} data and can be used to predict strained-Si devices with different Ge mole fractions.

3.2.3 Threshold voltage of a buried-channel strained-Si nMOS transistor

The threshold voltage of a buried-channel strained-Si nMOSFET has also been derived. Figure 3.13 shows the schematic of a buried-channel strained-Si n-MOSFET. It is similar in structure to the surface channel device except for a thin relaxed SiGe cap layer on top of the strained-Si. Figure 3.13 shows the potentials ϕ_{s1} , ϕ_{s2} and ϕ_{s3} at the respective interfaces.

Figure 3.13: Schematic of a buried-channel strained-Si nMOSFET [11].

The buried-channel strained-Si device has two threshold-voltages as the electrons invert at the top SiGe/SiO₂ interface and also the strained-Si/SiGe interface [11]. We can

derive the 1-D Poisson equation similar to that for the surface channel strained-Si device.

The potential at the bottom interface is given by

$$\phi_{s3} = \frac{qN_A x_{d2}^2}{2\epsilon_{Si}} + \Delta E_C \quad (3.17)$$

where x_{d2} is the depletion width in the region below the bottom interface. The potential

ϕ_{s2} is given by the relation $\phi_2(x) = \phi_3(x) - \Delta E_C$. When inversion occurs at the bottom s-

Si/SiGe interface, the potential at the strong inversion is given from the definition.

$$\frac{qN_A x_{d2}^2}{2\epsilon_{Si}} + \Delta E_C = \phi_{s3} = 2\phi_F = 2 \frac{kT}{q} \ln \left(\frac{N_A}{n_{i,Si}} \right) \quad (3.18)$$

where ϕ_F is the Fermi potential with $n_{i,Si}$ being the intrinsic carrier concentration in the Si substrate. The depletion width x_{d2} is calculated using the expression.

$$x_{d2,vt2} \equiv x_{d2}(V_{t2}) = \sqrt{\frac{2\epsilon_{SiGe}(2\phi_F - \Delta E_C)}{qN_A}}. \quad (3.19)$$

Hence, the total depletion width is given by the expression

$$x_{d1,vt2} \equiv x_{d2,vt2} + t_{SiGe}. \quad (3.20)$$

At V_{t2} the potential at the top interface is given by the expression

$$\phi_{s1} = \phi_{s2} + V_{Si} = \frac{qN_A x_{d2}^2}{2\epsilon_{Si}} + \left(t_{SiGe} \frac{qN_A x_{d2}}{\epsilon_{Si}} + \frac{qN_A t_{SiGe}^2}{2\epsilon_{Si}} \right) \quad (3.21)$$

Based on the threshold-voltage definition and 1-D voltage balance equation, the threshold voltage (V_{t2}) is given by the expression

$$\begin{aligned} V_{t2} &\equiv V_{gb} \Big|_{\phi_{s3}=2\phi_F} = \phi_{MS1} + V_{ox} + \phi_{s1}(x_{d1,vt2}) \\ &= \phi_{MS1} - \frac{Q_{ox}}{C_{ox}} - \frac{qN_A(t_{SiGe} + x_{d2,vt2})}{C_{ox}} + \phi_{s1}(x_{d1,vt2}). \end{aligned} \quad (3.22)$$

The threshold voltage (V_{t1}) is defined as the voltage at which electrons invert at the top

surface. When electrons invert at the top surface, the potential at the top interface can be given by the expression

$$\phi_{s1} = 2\phi_F = \frac{qN_A x_{d1,vr1}^2}{2\epsilon_{Si}}. \quad (3.23)$$

The depletion width can be derived from (3.23). The inversion charge due to the electrons inverting in the strained s-Si/SiGe interface should also be included in the 1-D voltage balance equation. $Q_{i2}(V_{t1})$ is the inversion charge at V_{t1} due to electron inversion at the bottom interface.

$$\begin{aligned} V_{t1} \equiv V_{gb} \Big|_{\phi_{s1}=2\phi_F} &= \phi_{MS1} + V_{ox} + \phi_{s1}(x_{d,vr1}) \\ &= \phi_{MS1} + \frac{Q_{ox}}{C_{ox}} + \frac{qN_A x_{d,vr1}}{C_{ox}} - \frac{Q_{i2}(V_{t1})}{C_{ox}} + \phi_{s1}(x_{d,vr1}). \end{aligned} \quad (3.24)$$

To derive the inversion charge at the bottom interface, we consider that the top SiGe cap layer is depleted of any mobile charges. The inversion charge at the bottom interface $Q_{i2}(V_{gb})$ can be approximated by $-C_{oxeff}(V_{gb} - V_{t2})$, and at $V_{gb} = V_{t1}$

$$Q_{i2}(V_{t1}) = -C_{oxeff}(V_{t1} - V_{t2}). \quad (3.25)$$

The SiGe cap layer can also be considered as a dielectric. Hence, the effective oxide capacitance is given by the expression

$$C_{oxeff} = \left(\frac{1}{C_{ox}} + \frac{t_{SiGe}}{\epsilon_{SiGe}} \right)^{-1} \quad (3.26)$$

From (3.24) and (3.25), the threshold-voltage at the top interface can be derived as

$$V_{t1} = \frac{\phi_{MS1} - \frac{Q_{ox}}{C_{ox}} + \frac{qN_A x_{d1,vr1}}{C_{ox}} + \phi_{s1}(x_{d1,vr1}) - \frac{C_{oxeff} V_{t2}}{C_{ox}}}{1 - \frac{C_{oxeff}}{C_{ox}}}. \quad (3.27)$$

3.2.4 Non-uniform doping and short-channel effects

The ideal long-channel threshold-voltage model discussed in the previous sections uses a uniform substrate doping and is derived using the 1-D Poisson equation. The basic idea in extending the model to the short-channels is to maintain the simple 1-D physical form and build all the 2-D effects like charge sharing, reverse short-channel effect, barrier lowering, into the threshold voltage model [12], [79]. The non-uniform doping profiles like the threshold adjust implant and halo implants are physically built into the model as Gaussian profiles using the Gaussian peak and spread [12], [79]. All short-channel models are physically built into the threshold-voltage model.

3.3 Unified Charge Model

In this section, we will derive the unified charge model for strained-Si MOSFET. This section describes how the URM can be used to capture the charge accumulation in the top surface and interface physically by an explicit model. This section also describes an implicit iterative method to calculate the charge, potential and intrinsic capacitance in strained silicon MOSFETs.

3.3.1 Single-piece charge model for strained-Si nMOSFETs

The capacitance–voltage characteristics of a strained-Si nMOSFET show a plateau in the accumulation region [38]. Figure 3.7 shows the band offset when a thin layer of strained-Si is grown on top of the relaxed silicon germanium substrate. The tensile strain causes a band offset in both conduction as well as valence-bands. The conduction-band offset causes the electrons to invert at the top $\text{SiO}_2/\text{s-Si}$ interface and, hence, there is a shift in the threshold-voltage, which was analyzed in the previous

section. The valence-band offset causes the holes to accumulate first at the bottom s-Si/SiGe interface. When the holes accumulate at the bottom surface, the top surface acts like a dielectric. This confinement of holes at the interface causes a plateau in the accumulation region. When the gate voltage is further decreased, holes accumulate at the top surface. This screens the bottom interface and the capacitance approaches C_{ox} .

A single-piece charge model from accumulation to inversion that can scale for different substrate doping (N_A), strained-Si thickness (t_{Si}) and germanium mole-fraction (x) has been derived. The key idea is to derive the exact flat-band values at which accumulation of holes starts to occur at the top and the bottom interfaces from 1-D Poisson equation. The derived flat-band voltages are applied to the regional surface potential and charge models. The regional solutions are then unified to get a single-piece unified charge model. When the germanium mole-fraction is set to zero, the strained-Si model goes back to the bulk-Si model, which indicates the correct incorporation of the physics underlying the strained silicon model presented here.

The URM solutions for surface potential and charge in bulk MOSFETs were discussed in Chapter 2. In this chapter, the URM approach will be extended to the strained-Si charge model. The model would be validated with Medici simulations. The energy-band properties like the band gap, electron affinity, band offsets and permittivity are mole-fraction dependant [80], [81]. They are given by the relations

$$E_{g,SiGe}(x) = 1.155 - 0.43x + 0.0206x^2 \text{ [eV]} \quad (0 < x < 0.85) \quad (3.28)$$

$$\Delta E_C(x) = 0.63x \text{ [eV]} \quad (0 < x < 0.4) \quad (3.29)$$

$$\Delta E_V(x) = (0.74 - 0.53x)x \text{ [eV]} \quad (0 < x < 0.4) \quad (3.30)$$

$$N_{C,SiGe}(x) = [2.80 + (1.04 - 2.80)x] \times 10^{19} [\text{cm}^{-3}] \quad (3.31)$$

$$N_{V,SiGe}(x) = [1.04 + (0.60 - 1.04)x] \times 10^{19} [\text{cm}^{-3}] \quad (3.32)$$

$$\epsilon_{SiGe}(x) = K_{SiGe}(x) \epsilon_0 = (11.8 + 4.2x) \epsilon_0. \quad (3.33)$$

These mole-fraction dependent band parameters are used in both Medici and in the compact model presented here.

Subscripts “1” and “2” will be used to denote physical quantities at the s-Si/SiO₂ and s-Si/SiGe interfaces, respectively. The flat-band voltage at which the accumulation starts at the s-Si/SiO₂ interface is similar to the bulk expression and is given by

$$V_{FB1} = \phi_M - \left(\chi_{Si} + \frac{E_{g,Si}}{2} + \phi_F^* \right) - \frac{Q_{ox}}{C_{ox}} \quad (3.34)$$

where the Fermi potential, band gap and the electron-affinity are given by the relations

$$\phi_F^* = \frac{v_{th}}{2} \left[\ln \left(\frac{N_{Si}}{n_{i,Si}} \right) + \ln \left(\frac{N_{Si}}{n_{i,SiGe}} \right) \right] \quad (3.35)$$

$$\chi_{Si} = \chi_{SiGe} + \Delta E_C \quad (3.36)$$

$$E_{g,Si} = E_{g,SiGe} + \Delta E_V - \Delta E_C \quad (3.37)$$

$$n_{i,SiGe} = \sqrt{N_{C,SiGe} N_{V,SiGe}} \exp \left(-\frac{E_{g,SiGe}}{2kT} \right). \quad (3.38)$$

To model the bulk charge, the accumulation charge and the depletion charge need to be included. Directly applying the V_{FB1} to the accumulation charge, we get the following expression

$$\begin{aligned} Q_{b,acc1} &= +C_{ox} (V_{gb} - V_{FB1} - \phi_{cc1}) \\ &= +C_{ox} (2v_{th} \mathcal{L}\{w_1\}) \equiv +C_{ox} V_{tacc} \end{aligned} \quad (3.39)$$

where

$$\phi_{cc1} = V_{gb} - V_{FB1} + 2v_{th} \mathcal{L}\{w_1\} \quad (3.40)$$

$$w_1 = \frac{\gamma}{2\sqrt{v_{th}}} \exp\left(-\frac{V_{gb} - V_{FB1}}{2v_{th}}\right). \quad (3.41)$$

Here, $\mathcal{L}\{w_1\}$ is given by the Lambert W function. The regional depletion charge is given by the expression

$$Q_{b,sub} = -C_{ox}\gamma\sqrt{\phi_{sub}} \quad (3.42)$$

where the unified regional solution ϕ_{sub1} is given by the expression

$$\phi_{sub1} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{gbf1}}\right)^2 \quad (3.43)$$

$$V_{gbf1} = \sigma_{a1}v_{th} \ln\left[1 + \exp\left(\frac{V_{gb} - V_{FB1}}{\sigma_{a1}v_{th}}\right)\right] \quad (3.44)$$

V_{gbf1} as discussed in chapter 2 is the regional solution for the $V_{gb} - V_{FB1}$ expression. (3.44) uses a logarithmic expression, which has a very similar behavior to the square-root function discussed in chapter 2. The capacitance corresponding to the respective accumulation and depletion charges can be obtained by numerical differentiation of the charges with respect to the gate voltage.

Figure 3.14: Direct playback of the bulk charge model from bulk for $x = 0.3$, compared with Medici (circle), which shows the model missing the “plateau” and inaccuracy in the depletion region [14].

Figure 3.14 shows the direct playback of the charge model from bulk-MOS model to a s-Si/Si_{0.7}Ge_{0.3} device. The flat-band voltage equation (3.34) captures the mole-fraction dependant shift in the flat-band voltage. But the model misses the plateau completely and there is also an inaccuracy in the depletion region. The model does not include the holes accumulating in the s-Si/SiGe interface. This needs to be captured physically in the model to investigate the experimentally observed C–V behavior.

Holes start accumulating in the s-Si/SiGe interface when the gate voltage reaches the flat-band voltage V_{FB2} . At V_{FB2} the top strained-Si is depleted of any mobile charges and a thin layer equivalent to the Debye Length is also depleted of charges in the SiGe substrate. The expression for V_{FB2} can be derived by solving the 1-D Poisson equation as above. At the flat-band condition, there are no mobile charges and, hence, only the charge due to acceptors can be considered,

$$Q_{b2} = -q(N_{Si}t_{Si} + N_{SiGe}L_D) \quad (3.45)$$

where L_D is given by the Debye Length

$$L_D = \sqrt{\frac{kT\epsilon_{SiGe}}{q^2 N_{SiGe}}} \quad (3.46)$$

From potential balance considerations, the gate-to-bulk voltage at V_{FB2} is given by the sum of the potentials

$$V_{FB2} \equiv V_{gb} = \phi_{MS2} + V_{ox} + V_{Si} + V_{LD} \quad (3.47)$$

where the work function difference is given by

$$\phi_{MS2} = \phi_M - \left(\chi_{SiGe} + \frac{E_{g,SiGe}}{2} + \phi_F^* \right) \quad (3.48)$$

From (3.36) and (3.37) we can rewrite (3.48) as

$$\begin{aligned} \phi_{MS2} &= \phi_M - \left[\chi_{Si} - \Delta E_C + \frac{1}{2} (E_{g,Si} + \Delta E_C - \Delta E_V) + \phi_F^* \right] \\ &= \phi_M - \left(\chi_{Si} + \frac{E_{g,Si}}{2} + \phi_F^* \right) + \Delta E_C + \frac{1}{2} (\Delta E_V - \Delta E_C) \\ &= \phi_{MS1} + \Delta E_C + \frac{\Delta E_g}{2} \end{aligned} \quad (3.49)$$

where

$$\Delta E_g = \Delta E_V - \Delta E_C \quad (3.50)$$

Considering that there are no mobile charges in the substrate, the charge balance equation can be written in the form

$$Q_g = -(Q_{b2} + Q_{ox}) \quad (3.51)$$

From Gauss law, (3.47) and (3.51)

$$V_{ox} = \frac{Q_g}{C_{ox}} = \frac{q(N_{Si}t_{Si} + N_{SiGe}L_D)}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad (3.52)$$

Within a Debye Length, there are no mobile charges and the potential across the Debye Length can be calculated by solving a 1-D Poisson equation as

$$V_{LD} = \frac{qN_{SiGe}L_D^2}{2\epsilon_{SiGe}}. \quad (3.53)$$

The potential across the strained-Si channel can also be derived in a similar manner

$$V_{Si} = t_{Si} \frac{qN_{SiGe}L_D}{\epsilon_{SiGe}} + \frac{qN_{Si}t_{Si}^2}{2\epsilon_{Si}} \quad (3.54)$$

With all these potentials derived, the flat-band voltage V_{FB2} in (3.47) can be rewritten as

$$\begin{aligned} V_{FB2} &= \phi_M - \left(\chi_{SiGe} + \frac{E_{g,SiGe}}{2} + \phi_F^* \right) - \frac{Q_{ox}}{C_{ox}} \\ &\quad + \frac{q(t_{Si}N_{Si} + N_{SiGe}L_D)}{C_{ox}} + \frac{qN_{Si}t_{Si}^2}{2\epsilon_{Si}} + \frac{qN_{SiGe}L_D t_{Si}}{\epsilon_{SiGe}} + \frac{qN_{SiGe}L_D^2}{2\epsilon_{SiGe}} \\ &= V_{FB1} + \Delta V_{FB} \end{aligned} \quad (3.55)$$

where

$$\Delta V_{FB} = \Delta E_C + \Delta E_g / 2 + \Delta V_{fb} \quad (3.56)$$

and

$$\Delta V_{fb} = \frac{q(t_{Si}N_{Si} + N_{SiGe}L_D)}{C_{ox}} + \frac{qN_{Si}t_{Si}^2}{2\epsilon_{Si}} + \frac{qN_{SiGe}L_D t_{Si}}{\epsilon_{SiGe}} + \frac{qN_{SiGe}L_D^2}{2\epsilon_{SiGe}} \quad (3.57)$$

is the shift in the flat-band due to the potential and charges in the strained-Si channel and the Debye length in the SiGe substrate

The accuracy of the model depends on the physics behind the flat-band voltages. The remarkable prediction of the flat-band voltages can be further explained by probing into the potentials and hole concentrations at the two interfaces from the Medici device simulator, as shown in Fig. 3.15. The corresponding band diagrams near the two flat-band voltages are shown in Fig. 3.16, which are physically modeled in our V_{FB} equations. V_{FB1} is where the surface potential $\phi_s = 0$ (and $p_s = N_{Si}$), as shown by the solid lines in Fig. 3.15, which corresponds to “equal potential at the surface and bulk” ($E_s = E_i$), as

shown in Fig. 3.16 by the thin dotted horizontal line (labeled $E_s = E_i$), which depends only on $\Delta E_g(x)$ and $\Delta E_C(x)$. The bands are not flat in this region due to band offsets at the s-Si/SiGe interface. Probing into the s-Si/SiGe interface, when the interface potential $\phi_i = 0$ (and $p_i = N_{Si}$), as shown in Fig. 3.15 by the dotted lines and the solid circles ($V_{gb} \approx -0.7$ V), the band is flat at the s-Si/SiGe interface whereas holes are still accumulated. An additional ΔV_{fb} is added to the band bending to model V_{FB2} . V_{FB2} is indicated by the open circles on the dotted lines in Fig. 3.15, and further validated by the corresponding band diagram shown in Fig. 3.16 (solid lines), in which a depletion region within a Debye Length is well predicted with accurate numerical value ($L_D = 9.7$ nm) for the given Si_{0.7}Ge_{0.3} device. All the calculated parameters agree with the results from Medici simulation for various Si_{1-x}Ge_x devices, which are supported by the energy band, electric potential, and charge calculations.

Figure 3.15: Hole concentrations (left axis) and surface potentials (right axis) at the Si/SiO₂ (solid) and Si/SiGe (dotted) interfaces extracted from the Medici device. Calculated V_{FB1} and V_{FB2} correspond directly to the numerically probed device parameters [14].

Figure 3.16: Band diagrams of the Medici device near the two calculated V_{FB1} and V_{FB2} gate-bias conditions, further supporting the definitions and physics built into the model (which physically relates to x , t_{Si} and N_{Si} parameters) [14].

When accumulation occurs at the bottom s-Si/SiGe layer, the top strained-Si channel also acts like a dielectric layer and the effective oxide capacitance is given by

$$C_{oxeff} = \left(\frac{t_{ox}}{\epsilon_{ox}} + \frac{t_{Si}}{\epsilon_{Si}} \right)^{-1}. \quad (3.58)$$

The same model as used in $Q_{b,acc1}$ can be used with the flat-band voltage V_{FB2} and the effective oxide capacitance C_{oxeff} .

$$Q_{b,acc2} = +C_{oxeff} (V_{gb} - V_{FB2} - \phi_{cc2}) = +C_{oxeff} (2v_{th} \mathcal{L} \{w_2\}) \quad (3.59)$$

where

$$\phi_{cc2} = V_{gb} - V_{FB2} + 2v_{th} \mathcal{L} \{w_2\} \quad (3.60)$$

$$w_2 = \frac{\gamma_2}{2\sqrt{v_{th}}} \exp \left(-\frac{V_{gb} - V_{FB2}}{2v_{th}} \right). \quad (3.61)$$

The charge from (3.59) can predict the plateau as it models the accumulation of holes at the s-Si/SiGe interface. But it cannot be directly added to the $Q_{b,acc1}$ model. Once

accumulation starts at the top s-Si/SiO₂ interface, the holes accumulating at the top interface shield the bottom interface. Hence accumulation of holes at the bottom interface should cease. We can rewrite (3.60) as

$$\phi_{wcc2} = V_{gb} - V_{FB2} + 2v_{th} \mathcal{L}\{w_{f1}\} \quad (3.62)$$

where w_{f1} is modified from (3.61) by replacing $V_{gb} - V_{FB1}$ in the argument of $\mathcal{L}\{w\}$ with V_{gbf1} in (3.44)

$$\begin{aligned} w_{f1} = w_2 &= \frac{\gamma_2}{2\sqrt{v_{th}}} \exp\left(-\frac{V_{gb} - V_{FB2} - V_{FB1} + V_{FB1}}{2v_{th}}\right) \\ &= \frac{\gamma_2}{2\sqrt{v_{th}}} \exp\left(-\frac{(V_{gb} - V_{FB1}) - (V_{FB2} - V_{FB1})}{2v_{th}}\right) \\ &= \frac{\gamma_2}{2\sqrt{v_{th}}} \exp\left(-\frac{V_{gbf1} - \Delta V_{FB}}{2v_{th}}\right) \end{aligned} \quad (3.63)$$

ΔV_{FB} is defined in (3.56) and modeled by (3.57). The unified regional model defined in (3.59) is now given by

$$\begin{aligned} Q_{b,wcc2} &= -C_{oxeff} (V_{gb} - V_{FB2} - \phi_{wcc2}) \\ &= +C_{oxeff} (2v_{th} \mathcal{L}\{w_{f1}\}) \equiv +C_{oxeff} V_{twcc} \end{aligned} \quad (3.64)$$

When the gate is biased at a voltage higher than the flat-band voltage, it operates in the depletion region. The charge in the depletion region can be given by the expression

$$Q_{b,sub2} = -C_{ox} \gamma_2 \sqrt{\phi_{sub2}} \equiv -C_{ox} V_{tsub} \quad (3.65)$$

where ϕ_{sub2} is the surface potential at the s-Si/SiO₂ interface. When $V_{FB2} < V_{gb} \ll V_t$, a layer (with charge Q_{sc2}) is depleted beyond the fully depleted regions of s-Si and a Debye Length in SiGe, as schematically shown in the inset of Fig. 3.17. If we define the surface potentials at the s-Si/SiO₂ and s-Si/SiGe interfaces to be ϕ_{s1} and ϕ_{s2} , respectively, they are

related by

$$\phi_{s1} = V_{Si} + V_{LD} + \phi_{s2} \quad (3.66)$$

where V_{Si} and V_{LD} are already defined in (3.53) and (3.54), respectively, and ϕ_{s2} is the surface potential at the s-Si/SiGe interface. The total space charge in (3.65) is given by the sum

$$Q_{b0} + Q_{b2} = Q_{b,sub2} = -C_{ox}\gamma_2\sqrt{\phi_{s1}}. \quad (3.67)$$

When the gate voltage is larger than the flat-band voltage, the accumulation charges can be neglected. The potential balance equation can be written as

$$V_{gb} = \phi_{MS2} + V_{ox} + \phi_{s1}. \quad (3.68)$$

The Charge balance equation can also be written in the form

$$Q_g = -(Q_{b0} + Q_{b2} + Q_{ox}) \quad (3.69)$$

where Q_{b2} is given by

$$Q_{b2} = -C'_{oxeff}\gamma_2\sqrt{\phi_{s2}} \quad (3.70)$$

$$C'_{oxeff} = \left(\frac{t_{ox}}{\epsilon_{ox}} + \frac{t_{Si}}{\epsilon_{Si}} + \frac{L_D}{\epsilon_{SiGe}} \right)^{-1} \quad (3.71)$$

Combining (3.68) to (3.71)

$$V_{gb} = \phi_{MS2} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{b0}}{C_{ox}} - \frac{-Q_{b0} - C_{ox}\gamma_2\sqrt{\phi_{s1}}}{C_{ox}} + \phi_{s1}. \quad (3.72)$$

Since from (32) $V_{FB2} = \phi_{MS2} - Q_{ox}/C_{ox} + \Delta V_{fb}$, (3.72) is given by

$$V_{gb} - V_{FB2} + \Delta V_{fb} - \phi_{s1} = +\gamma_2\sqrt{\phi_{s1}}. \quad (3.73)$$

This regional piece can be solved explicitly to get the surface potential in the depletion region,

$$\phi_{s1} = \left(-\frac{\gamma_2}{2} + \sqrt{\frac{\gamma_2^2}{4} + V_{gb} - V_{FB2} + \Delta V_{fb}} \right)^2. \quad (3.74)$$

With $V_{gb} - V_{FB2}$ being replaced by the smoothing function $\sigma_{a2} v_{th} \ln \left[1 + \exp \left(\frac{V_{gb} - V_{FB2}}{\sigma_{a2} v_{th}} \right) \right]$,

$V_{gb} - V_{FB2} + \Delta V_{fb}$ is replaced by V_{gbf2} in (3.74)

$$V_{gbf2} = \Delta V_{fb} + \sigma_{a2} v_{th} \ln \left[1 + \exp \left(\frac{V_{gb} - V_{FB2}}{\sigma_{a2} v_{th}} \right) \right], \quad (3.75)$$

and the body factor is given by

$$\gamma_2 = \frac{\sqrt{2q\epsilon_{SiGe}N_{SiGe}}}{C_{ox}}. \quad (3.76)$$

Hence the bulk charge due to depletion is given by (3.65), where ϕ_{sub2} is given by

$$\phi_{sub2} = \left(-\frac{\gamma_2}{2} + \sqrt{\frac{\gamma_2^2}{4} + V_{gbf2}} \right)^2. \quad (3.77)$$

Figure 3.17: The two interpolation functions in relation to the two flat-band voltages and ΔV_{fb} (for the actual $s\text{-Si}/\text{Si}_{0.7}\text{Ge}_{0.3}$ device). The inset shows the layer structures under the depletion condition [14].

The inset of Fig. 3.17 shows the schematic of the layer depleted below the strained-Si channel and the Debye Length. Figure 3.17 shows the two interpolation functions in relation to the two flat-band voltages and ΔV_{fb} .

Figure 3.18: Direct playback for modeling “accumulation + depletion” at V_{FB2} [(b') + (c)]; changing (b') to (b) for modeling screening of accumulation of holes at the Si/SiGe interface [(b) + (c)]; then adding charge due to accumulation at Si/SiO₂. [14].

Figure 3.18 shows the different charge components corresponding to the holes accumulated at the top s-Si/SiO₂ interface, the holes accumulated at the bottom s-Si/SiGe interface and the charge due to the acceptors. The figure clearly shows the model predicting the plateau due to the accumulation of holes at the bottom interface. The screening of the bottom interface when holes start accumulating at the surface is captured by the smoothing function in the model. The direct addition of all the regional unified pieces gives a single-piece bulk charge model.

$$\begin{aligned} & \text{let } \\ & \text{let } \\ & \text{let } \end{aligned}$$

Figure 3.19: Modeled regional bulk charges and surface potentials (inset) corresponding to those in Fig. 3.17. Note that the $Q_{b,wcc2}$ stops increasing when $Q_{b,acc1}$ starts to increase, and ϕ_{sub2} approaching a finite value (ΔV_{fb}) as $V_{gb} < V_{FB1}$. [14]

Figure 3.19 shows the modeled regional bulk charges and surface potentials corresponding to the capacitance shown in Fig. 3.18. The inset shows the regional surface potential solutions. These solutions are used in the calculation of charges. The figure shows the holes accumulating in the bottom s-Si/SiGe interface when $V_{FB1} < V_{gb} < V_{FB2}$. In the region $V_{gb} < V_{FB1}$ holes start accumulating at the top interface and then further accumulation of holes at the bottom interface ceases. The physical parameters like doping, strained-Si thickness and mole-fraction dependant energy-band parameters have been built into the model.

3.3.2 Effect of substrate doping on the C–V characteristics

The unified charge model for a surface channel strained-Si nMOSFET was discussed in section 3.3.1. The surface channel strained-Si nMOS has a plateau in the accumulation side due to the accumulation of holes at the two interfaces. Similarly the

physics behind the surface-channel strained-Si pMOSFETs is studied. The strained-Si layer on top of a relaxed SiGe buffer has a type II band alignment and there is a band offset in both the conduction-band edge and the valence-band edge. The valence-band offset should cause an inversion of holes first at the bottom interface and then at the top interface. Hence, a plateau on the inversion side of the pMOS was expected. Contrary to the expected result, our experimental results exhibited a band offset in the accumulation side of the pMOSFET [13]. Figure 3.20 shows the measured gate capacitance of a bulk silicon and a surface-channel strained-Si pMOS. The Si wafers consist of strained-Si on a uniform relaxed $\text{Si}_{0.75}\text{Ge}_{0.25}$ buffer layer grown on a thick graded SiGe buffer. pMOS capacitors were formed by implanting the substrate with a phosphorus dose of $2 \times 10^{13} \text{ cm}^{-2}$ at energy of 300 keV. The thermal oxide is grown at 800 °C in a dry ambient.

Figure 3.20: Measured gate capacitance of bulk-Si and surface-channel s-Si pMOS with Ge mole fraction of $x = 0.25$ [13].

Simulation and modeling

To investigate the physics behind the abnormality exhibited in the surface-channel strained-Si pMOS, a number of numerical simulations with different substrate doping were carried out. Figure 3.21 shows the simulated C–V characteristics of a strained-Si

pMOS and nMOS for different substrate doping concentrations. In a surface-channel strained-Si nMOS, the plateau is in the accumulation side of the curve for all substrate doping. The potential well formed by the strained-Si is at the surface and, thus, no barriers exist to confine the electrons away from the surface. As a result, the electron inversion layer always forms at the top interface explaining the absence of any plateaus in the inversion region. But in the strained-Si pMOS, as the substrate doping increases, the plateau shifts from the inversion to the accumulation side. This is consistent with the observed experimental data.

Figure 3.21: Medici simulated C - V characteristics of a surface-channel s-Si nMOS and pMOS with varying substrate doping concentrations as indicated in the legends.

To probe into the physical mechanisms, internal potential solutions for Medici simulations are extracted at each gate bias. Based on the coordinate shown in Fig. 3.22

along a vertical cutline, the potential at the ‘top’ (s-Si/SiO₂) interface (referenced to that in the deep bulk) is named as $\phi_{s1} \equiv \phi_s(0)$. The potentials at the ‘bottom’ (s-Si/SiGe) interface are defined as $\phi_{s2} \equiv \phi_s(t_{Si-})$ and $\phi_{s3} \equiv \phi_s(t_{Si+})$. The difference between ϕ_{s2} and ϕ_{s3} is either the conduction-band offset (ΔE_C) or valence-band offset (ΔE_V) at that interface.

Figure 3.22: A schematic cross section of the surface-channel strained-Si device and a vertical cut-line of the potential profile.

$$\phi_{s2} - \phi_{s3} = \Delta E_C \quad (3.78)$$

$$\phi_{s2} - \phi_{s3} = \Delta E_V \quad (3.79)$$

For pMOS threshold-voltage (V_t) analysis, valence-band and (3.79) with ϕ_{s3} should be used since it is related to hole inversion in SiGe above $|V_t|$; whereas for pMOS flat-band (V_{FB}) analysis, total band bending is measured from the conduction-band and (3.78) with ϕ_{s2} should be used, since it is related to electron accumulation in s-Si below $|V_{FB}|$. The above discussed potentials ϕ_{s1} , ϕ_{s2} and ϕ_{s3} are probed at low (10^{15} cm^{-3}) and high (10^{18} cm^{-3}) substrate doping concentrations to show the threshold-voltage and flat-band voltage conditions. Figure 3.23 shows the probed potentials. The threshold-voltages and flat-band voltages are defined as the gate voltages at which the potential at the surface or interface reaches $2\phi_F$ and zero, respectively. At low-doping, the holes first invert at the bottom interface and then at the top interface, hence, there are two threshold-voltages.

When the bottom surface inverts, the potential at the top s-Si/SiO₂ interface is given by the expression

$$\phi_{s1} = \phi_{s2} + V_{Si} = \left(\Delta E_v - \frac{qN_{sub}x_{d2}^2}{2\epsilon_{SiGe}} \right) - \left(t_{Si} \frac{qN_{sub}x_{d2}}{\epsilon_{SiGe}} + \frac{qN_{sub}t_{Si}^2}{2\epsilon_{Si}} \right). \quad (3.80)$$

As the substrate doping increases, the last term in (3.80) becomes greater than the valence-band offset. Then, the top surface reaches a potential of $2\phi_F$ faster than at the bottom interface and, hence, inversion occurs first at the top interface. The holes inverted at the top interface screen the bottom interface. This explains the gradual missing plateau in inversion as the doping increases.

Figure 3.23: The potentials probed at different interfaces in the s-Si pMOS with substrate doping of (a) $1 \times 10^{15} \text{ cm}^{-3}$ and (b) $1 \times 10^{18} \text{ cm}^{-3}$ [13]

In Fig. 3.23, for a doping concentration of $2 \times 10^{18} \text{ cm}^{-3}$, ϕ_{s1} reaches a potential of $2\phi_F$ faster and, hence, no plateau is seen in the gate capacitance curve, but in the case of a low-doping of $1 \times 10^{15} \text{ cm}^{-3}$, the potential at the bottom interface ϕ_{s3} reaches $2\phi_F$ faster than at the top interface, hence, hole inversion first occurs at the bottom interface and as

the top interface potential ϕ_{s1} reaches $2\phi_F$, inversion starts at the top interface. Figure 3.23 shows the band bending in a s-Si pMOS at flat-band and threshold-voltage conditions for low and high substrate doping. The flat-band voltage is defined as the voltage at which the potential at the interface reaches zero. When the potential at the bottom interface (ϕ_{s2}) reaches zero, the boundary condition can be written as

$$-\frac{qN_{Si}x_{d1}^2}{2\epsilon_{SiGe}} + \Delta E_C = 0. \quad (3.81)$$

When the potential at the top interface (ϕ_{s1}) reaches zero, the boundary condition can be written as

$$-\frac{qN_{Si}x_{d2}^2}{2\epsilon_{SiGe}} - \frac{qN_{Si}x_{d2}}{\epsilon_{SiGe}}t_{Si} - \frac{qN_{Si}t_{Si}^2}{2\epsilon_{Si}} + \Delta E_C = 0. \quad (3.82)$$

The depletion width x_d mentioned in the boundary conditions is the width of the region depleted in the SiGe substrate after the top s-Si layer (t_{Si}) is already depleted. The depletion width x_{d1} calculated from (3.81) is used in the flat-band voltage calculation.

The flat-band voltage at the top and interface can be obtained from

$$V_{FB} = \phi_M - \left(\chi_{Si} + \frac{E_{g,Si}}{2} + \phi_F \right) - \frac{qN_{Si}x_d^2}{2\epsilon_{SiGe}} - \frac{qN_{Si}x_d}{\epsilon_{SiGe}}t_{Si} - \frac{qN_{Si}t_{Si}^2}{2\epsilon_{Si}} - \frac{qN_{Si}(x_d + t_{Si})}{C_{ox}}. \quad (3.83)$$

Using the corresponding calculated depletion widths from (3.81) and (3.82), the two expressions for flat-band voltage at the top and interface are

$$V_{FB2} = \phi_M - \left(\chi_{Si} + \frac{E_{g,Si}}{2} + \phi_F \right) - \Delta E_C - \frac{qN_{Si}x_{d1}}{\epsilon_{SiGe}}t_{Si} - \frac{qN_{Si}t_{Si}^2}{2\epsilon_{Si}} - \frac{qN_{Si}(x_{d1} + t_{Si})}{C_{ox}} \quad (3.84)$$

$$V_{FB1} = \phi_M - \left(\chi_{Si} + \frac{E_{g,Si}}{2} + \phi_F \right) - \Delta E_C - \frac{qN_{Si}(x_{d2} + t_{Si})}{C_{ox}}. \quad (3.85)$$

In low-doping cases, the difference between the two flat-band voltages is negligible as can be seen in Fig. 3.24. So, the electrons accumulate in the top s-Si layer, hence, no plateau is seen on the accumulation side. As the substrate doping increases, V_{FB2} is less than V_{FB1} and, hence, electrons first accumulate at the bottom s-Si/SiGe interface and then at the top s-Si/SiO₂ interface.

Figure 3.24: The band bending in the s-Si pMOS at flat-band and threshold-voltages with substrate doping of (a) $1 \times 10^{15} \text{ cm}^{-3}$ and (b) $2 \times 10^{18} \text{ cm}^{-3}$ [13].

Figure 3.24 shows the top interface reaching zero potential first in low-doping cases. At high-doping, electrons first start accumulating at the bottom interface. This explains the plateau in the accumulation region at high-doping conditions. The internal potentials

probed from Medici clearly explain the shift in the plateau. This effect of the substrate doping has also been observed in buried-channel strained-Si nMOS devices.

3.3.3 An implicit iterative technique

A single-piece explicit charge model for strained-Si MOSFETs has been derived using the two flat-band voltages in Section 3.3.1. The effect of substrate doping on the C–V characteristics of strained-Si MOSFET is also studied in Section 3.3.2. It has been known that the potential $\psi(x, y)$ inside an MOSFET can only be solved numerically whereas only the *surface* potential, $\phi_s \equiv \psi(0, y)$, can be analytically integrated out, as described by the well-known Pao–Sah equation. Analytical solution for any (internal) “interface” potential (at $x = t$) is only obtainable in depletion approximation [18]. This section presents a novel technique for calculating internal potential solutions based on potential and charge balance at the surface and a given interface using an internal iteration approach, which is applied to hetero-structure s-Si/SiGe MOSFETs for the calculation of surface potential, charge, and capacitance physically scalable for all terminal biases, Ge mole-fraction, strained/cap layer thickness, and channel doping [11].

We have used the URM approach to model the surface potential, interface potential, charge and capacitance. We derive physics-based equations in each region of operation and unify them using interpolation functions. A buried-channel s-Si nMOS device with a SiGe cap layer is used to demonstrate the technique. We use subscripts “1” and “2” to indicate quantities associated with the (SiO₂/SiGe) “top surface” and (SiGe/s-Si) “bottom interface,” respectively. For simplicity, we assume the channel doping (N) is uniform.

The potential/charge balance at the top surface is governed by the well-known Pao–Sah model. From Gauss law, the 1-D charge balance equation can be written as

$$V_{gb} - V_{FB1} - \phi_{s1} = -\frac{Q_{sc}}{C_{ox}} \quad (3.86)$$

where the flat-band voltage (V_{FB1}) is defined as the voltage at which the top surface potential reaches zero. Q_{sc} is the induced space charge (per unit area) in the channel which, in general, includes accumulation (Q_{acc}), depletion or bulk (Q_b), and inversion (Q_i) charges. $C_{ox} = \epsilon_{ox}/t_{ox}$ is the gate oxide capacitance (per unit area).

3.3.3.1 Depletion region

The surface potential of an nMOSFET can be solved regionally from the general equation (3.86). In the depletion region, hole accumulation and electron inversion charges can be assumed negligible. Then, (3.86) can be rewritten as

$$V_{gb} - V_{FB1} - \phi_{s1} = -\frac{Q_b}{C_{ox}}. \quad (3.87)$$

The depletion charge can also be represented by the surface potential

$$Q_b = -\gamma_1 \sqrt{\phi_{s1}} \quad (3.88)$$

where the body factor is given by

$$\gamma_1 = \frac{\sqrt{2q\epsilon_{Si}N}}{C_{ox}}. \quad (3.89)$$

As discussed in Chapter 2, we use the URM for all the individual pieces. The unified depletion formulation is given by

$$\phi_{sub1} = \left[-\frac{\gamma_1}{2} + \sqrt{\frac{\gamma_1^2}{4} + V_{gbf1}} \right]^2. \quad (3.90)$$

When the top SiGe cap layer is depleted of any mobile charges, it can be considered as a dielectric. The effective oxide capacitance can be written as

$$C_{oxeff} = \left(\frac{1}{C_{ox}} + \frac{t_{SiGe}}{\epsilon_{SiGe}} \right)^{-1}. \quad (3.91)$$

The flat-band condition, V_{FB2} at which the bottom interface potential reaches zero can be derived by writing the 1-D Poisson equation

$$V_{FB2} = V_{FB1} + \frac{qNt_{SiGe}^2}{2\epsilon_{SiGe}} + \frac{qNt_{SiGe}}{C_{ox}}. \quad (3.92)$$

If the total depletion width is given by x_{d1} , then (3.87) can be rewritten as

$$V_{gb} - V_{FB1} - \phi_{s1} = \frac{qNx_{d1}}{C_{ox}}. \quad (3.93)$$

The depletion width x_{d1} can be represented as

$$x_{d1} = x_{d2} + t_{SiGe} \quad (3.94)$$

where x_{d2} is the depletion width underneath the SiGe cap layer. When the top cap layer is depleted of any mobile charges, the surface potential can be written in terms of the interface potential as

$$\phi_{s1} = \phi_{s2} + \frac{qNt_{SiGe}^2}{2\epsilon_{Si}} + \frac{qNt_{SiGe}x_{d2}}{\epsilon_{Si}}. \quad (3.95)$$

From the above equations, we can rewrite (3.93) as

$$V_{gb} - V_{FB1} - \left(\phi_{s2} + \frac{qNt_{SiGe}^2}{2\epsilon_{Si}} + \frac{qNt_{SiGe}x_{d2}}{\epsilon_{Si}} \right) = \frac{qN(x_{d2} + t_{SiGe})}{C_{ox}} \quad (3.96)$$

$$V_{gb} - \left(V_{FB1} + \frac{qNt_{SiGe}^2}{2\epsilon_{Si}} + \frac{qNt_{SiGe}}{C_{ox}} \right) - \phi_{s2} = \frac{qNx_{d2}}{C_{ox}} + \frac{qNt_{SiGe}x_{d2}}{\epsilon_{Si}}. \quad (3.97)$$

Now, (3.97) can be simplified as

$$V_{gb} - V_{FB2} - \phi_{s2} = qN_{d2} \left(\frac{1}{C_{ox}} + \frac{t_{SiGe}}{\epsilon_{Si}} \right), \quad (3.98)$$

which can be rewritten as

$$V_{gb} - V_{FB2} - \phi_{s2} = \frac{qN_{d2}}{C_{oxeff}}. \quad (3.99)$$

The right hand side of (3.99) can also be represented in terms of the interface potential ϕ_{s2} from depletion approximation as

$$V_{gb} - V_{FB2} - \phi_{s2} = -\frac{\sqrt{2q\epsilon_{Si}N\phi_{s2}}}{C_{oxeff}} = -\gamma_2 \sqrt{\phi_{s2}}. \quad (3.100)$$

Similar to (3.90), we can express the unified regional (depletion) ϕ_{s2} solution using the interpolation function

$$\phi_{sub2} = \left[-\frac{\gamma_2}{2} + \sqrt{\frac{\gamma_2^2}{4} + V_{gbf2}} \right]^2 \quad (3.101)$$

where the body factor γ_2 is given by

$$\gamma_2 = \frac{\sqrt{2q\epsilon_{Si}N}}{C_{oxeff}} \quad (3.102)$$

and $V_{gbf2} = \mathcal{G}_f\{x_2; \sigma_f\}$ given by (2.24), with $x_2 = V_{gb} - V_{FB2}$.

3.3.3.2 Inversion region

In strong inversion, the space charge consists of depletion and inversion charges. Hence, (3.86) can be written as

$$V_{gb} - V_{FB1} - \phi_{s1} = -\frac{(Q_b + Q_i)}{C_{ox}} = -\frac{(Q_b + Q_{i1} + Q_{i2})}{C_{ox}} \quad (3.103)$$

where Q_{i1} and Q_{i2} are the inversion charges at the top and SiGe/Si interfaces. (3.103) can

also be rewritten as

$$V_{gb} - V_{FB1} - \phi_{s1} + \frac{Q_{i2}}{C_{ox}} = -\frac{(Q_b + Q_{i1})}{C_{ox}}. \quad (3.104)$$

In strong inversion, with $\phi_B = \phi_{s01} = 2\phi_f$ approximating ϕ_{s1} and solving for ϕ_{s1} one obtains

$$\phi_{str1} = \phi_{s01} + V_{cb} + \Delta_1, \quad (V_{gs} > V_t) \quad (3.105)$$

$$\Delta_1 = v_{th} \ln \left\{ \frac{1}{v_{th}} \left[\left(\frac{V_{gb} - V_{FB1} - \phi_{s1} + \frac{Q_{i2}}{C_{ox}}}{\gamma} \right)^2 - (\phi_{s01} + V_{cb}) \right] + 1 \right\}. \quad (3.106)$$

When inversion occurs first at the bottom interface, the cap layer acts as a dielectric and, hence, the potential balance equation can be rewritten as

$$V_{gb} - V_{FB2} - \phi_{s2} = -\frac{Q_{b2} + Q_{i2}}{C_{oxeff}}. \quad (3.107)$$

The strong inversion potential at the SiGe/Si interface can be modeled by the equation, with the approximation

$$\phi_{s02} = 2\phi_f - \frac{qNt_{SiGe}^2}{2\epsilon_{Si}} - \frac{qNt_{SiGe}(x_{d2})}{\epsilon_{Si}} \quad (3.108)$$

where x_{d2} is defined in (3.94)

$$\phi_{str2} = \phi_{s02} + V_{cb} + \Delta_2, \quad (V_{gs} > V_t) \quad (3.109)$$

$$\Delta_2 = v_{th} \ln \left\{ \frac{1}{v_{th}} \left[\left(\frac{V_{gb} - V_{FB2} - \phi_{s2}}{\gamma_2} \right)^2 - (\phi_{s02} + V_{cb}) \right] + 1 \right\}. \quad (3.110)$$

The strong inversion potential at the SiGe/Si interface can be modeled by the above equation. When inversion starts at the top interface, it shields the bottom interface, the potential balance equation can be written as

$$V_{gb} - V_{FB2} - \phi_{s2} + \frac{Q_{i1}}{C_{ox}} = -\frac{Q_{b2} + Q_{i2}}{C_{oxeff}}. \quad (3.111)$$

From (3.111), the strong inversion “delta” piece is modeled by the equation

$$\Delta_2 = v_{th} \ln \left\{ \frac{1}{v_{th}} \left[\left(\frac{V_{gb} - V_{FB2} - \phi_{s2} + \frac{Q_{i1}}{C_{ox}}}{\gamma_2} \right)^2 - (\phi_{s02} + V_{cb}) \right] + 1 \right\}. \quad (3.112)$$

The inversion charge at the top and bottom interfaces can be calculated by iterating the equations (3.105) and (3.109). We start with an initial guess where Q_{i1} can be set to zero.

3.3.3.3 Accumulation region

A similar approach to inversion can be employed for the accumulation region as well, as there is accumulation at both the top and bottom interfaces. The potential balance equation in accumulation can be written as

$$V_{gb} - V_{FB1} - \phi_{s1} = -\frac{(Q_{acc1} + Q_{acc2})}{C_{ox}}. \quad (3.113)$$

The equation can be rewritten as

$$V_{gb} - V_{FB1} - \phi_{s1} + \frac{Q_{acc2}}{C_{ox}} = -\frac{Q_{acc1}}{C_{ox}}. \quad (3.114)$$

The surface potential at accumulation is given by

$$\phi_{acc1} = V_{gbr1} + 2v_{th} \mathcal{L}\{w\} \quad (3.115)$$

where

$$w = \frac{\gamma_1}{2\sqrt{v_{th}}} \exp \left(-\frac{V_{gb} - V_{FB1} + \frac{Q_{acc2}}{C_{ox}}}{2v_{th}} \right) \quad (3.116)$$

and V_{gbr} is the complementary smoothing function defined in (2.24) and is given by

$$V_{gbr} = \mathcal{G}_r \{x; \sigma_a\} \equiv -0.5 \left(-x + \sqrt{x^2 + 4\sigma_a} \right) \quad (3.117)$$

to replace the $V_{gb} - V_{FB1}$ term by $V_{gbr1} = \mathcal{G}_r \{x_1; \sigma_a\}$ with $x_1 = V_{gb} - V_{FB1}$. When holes accumulate at the bottom SiGe/Si interface, the top cap layer acts like a dielectric. Similar to inversion, the potential balance equation can be given by

$$V_{gb} - V_{FB2} - \phi_{s2} + \frac{Q_{acc1}}{C_{ox}} = -\frac{Q_{acc2}}{C_{oxeff}}. \quad (3.118)$$

The interface potential in accumulation is given by

$$\phi_{acc2} = V_{gbr2} + 2v_{th} \mathcal{L} \{w_2\} \quad (3.119)$$

where

$$w_2 = \frac{\gamma_2}{2\sqrt{v_{th}}} \exp \left(-\frac{V_{gb} - V_{FB2} + \frac{Q_{acc1}}{C_{ox}}}{2v_{th}} \right) \quad (3.120)$$

and $V_{gbr2} = \mathcal{G}_r \{x_2; \sigma_a\}$ with $x_2 = V_{gb} - V_{FB2}$. The accumulation region is modeled by iterating (3.115) and (3.119). Figure 3.25 shows a flowchart of the implicit iterative technique to calculate the surface potential, charge and capacitance in strained silicon MOSFETs. The Q_{acc1} is assumed to be zero as an initial guess. The Q_{acc2} is calculated in (3.118). The calculated Q_{acc2} is used in (3.115). On further iterations, the potentials, charge and capacitance iterate to the right values.

Figure 3.25 Flowchart to demonstrate the implicit iterative technique to calculate the surface and interface potential.

Figure 3.26: Prediction of surface potential and intrinsic potential in a buried-channel nMOS ($x=0.3$) starting from an initial guess of $Q_{il}=0$ using internal iteration [11].

Figure 3.27: Prediction of charge in the surface and interface in a buried-channel nMOS ($x=0.3$) using internal iteration [11].

Figure 3.28: Prediction of C_{gg} in the surface and interface in a buried-channel nMOS ($x=0.3$) using internal iteration [11].

Figure 3.26 shows the calculated surface and interface potentials for a buried-channel strained-Si nMOSFET. The iteration results starting from the initial guess are also shown in the figure. The charge and the capacitance are calculated from the surface potential. Figures 3.27 and 3.28 show the calculated charge and capacitance, in subsequent

iterations, starting from the initial guess. Figure 3.27 clearly show that when the top layer is inverted, the electrons at the top surface screen the bottom interface. The dotted lines show that the electron concentration at the interface saturates. The figures show the plots for ten iterations. The iteration technique can also capture the plateau in the accumulation side of surface channel strained silicon nMOSFETs. The model also switches from the inversion side to accumulation side with increase in substrate doping.

3.4 Strained-Silicon Mobility Model

Several mobility models based on modeling the effective mass, intra-valley scattering using empirical fitting parameters have been discussed in literature. A simple, empirical model that is scalable and easy to extract has been developed by BSIM group at UC Berkeley [82]. This section discusses the empirical mobility model developed at Berkeley. The channels of a MOSFET can be strained by different techniques. There are several stressors, which can induce a strain in the channel. Some of the stressors are relaxed SiGe substrate, silicon nitride cap layer, SiGe source/drain, shallow trench isolation, silicide layers, spacers, gate stack etc. With so many stressors straining the channel, it is more efficient to develop a non-process specific (holistic) model to model the strain induced by all the stressors [82]. The strain components along all the three directions are captured to model the mobility.

Figure 3.29: TEM images of a strained silicon pMOSFET and nMOSFET strained by the SiGe source/drain and the capping layer respectively [83].

Figure 3.29 shows the TEM images of a strained-silicon pMOSFET and nMOSFET strained with the SiGe source/drain and the capping layers. The change in resistivity is related to the local stress through piezo-resistive coefficients. The mobility enhancement in the inversion layer is dictated by the average stress in the inversion layer.

$$\frac{\delta\mu}{\mu_0} \propto - \frac{\int_0^L S(x, L) dx}{L} = S_{avg}(L) \quad (3.121)$$

where $S(x, L)$ is defined as the stress along the channel. Process induced stress can be induced in all directions. When SiGe source/drain stressors are used, the channel is strained in the x and y directions [82].

$$\begin{aligned} S_{xx} &= \left(\frac{A1}{A2+L} + A3 \right) \cdot \left(\frac{B1}{B2+W} + B3 \right) \\ S_{yy} &= \left(\frac{A4}{A5+L} + A6 \right) \cdot \left(\frac{B4}{B5+W} + B6 \right) \end{aligned} \quad (3.122)$$

where $A1, A2, A3, A4, A5, A6, B1, B2, B3, B4, B5, B6$ are empirical parameters to capture the horizontal and vertical stress components. Stress due to the gate stack stressors is in the x direction. The principal component of the strain can be captured by the following empirical model:

$$S_{xx} = \left(A1 + \frac{A2}{A3 + L} + \frac{A4}{A5 + L} \right) \cdot \left(\frac{B1}{B2 + W} + B3 \right). \quad (3.123)$$

Stress due to the spacers is also in both x and y directions and can be modeled by the same empirical model as in (3.122). A holistic stress model would be a sum of all the three stress transfer directions. The number of parameters would be large and impossible to extract for a generalized model [82]. A multiple stressor model based on two dominant transfer techniques can be written as

$$\begin{aligned} \frac{\mu}{\mu_0} = 1 + & \left(A1 + \frac{A2}{A3 + L} + \frac{A4}{A5 + L} \right) \cdot \left(B1 + \frac{B2}{B3 + W} + \frac{B4}{B5 + W} \right) + \\ & \left(A6 + \frac{A7}{A8 + L} + \frac{A9}{A10 + L} \right) \cdot \left(B6 + \frac{B7}{B8 + W} + \frac{B9}{B10 + W} \right) \end{aligned} \quad (3.124)$$

The holistic model can capture the mobility variations for all types of stressors as the stress vectors are not process specific and depend on the stress components in different directions. Even when the channel is stressed by two or three different stressors like STI, capping layer, the model should be able to capture them. Good fits for both L and W variations are obtained using just 6 fitting parameters.

Figure 3.30: Prediction of the holistic model for different geometries modeled for a STI stressor, capping layer and also for multiple stressors [82].

Figure 3.30 shows the prediction of the strained silicon mobility model with numerical simulation data [82]. The geometric scalability of the model is tested with different stressors such as STI and capping layer. The scalability of the model has also been tested with multiple stressors.

3.5 Summary

Threshold-voltage models have been derived for the surface- and buried-channel strained-silicon MOSFETs. The threshold-voltage models are extended to short channel similar to the bulk MOSFET by building the effective channel doping into the model. Physics-based single-piece charge model for strained-silicon MOSFETs have been derived. An implicit iterative technique to calculate potential, charge and capacitance has been derived. The scalability of the model for different mole fraction, channel thickness and doping has been tested. Effect of substrate doping on the C–V characteristics of a surface channel s-Si MOSFET has also been studied. A review on a non-process specific holistic s-Si mobility model has been done.

CHAPTER 4 DOUBLE-GATE MOSFET MODELING

The double-gate (DG) MOSFET is similar to the ultra-thin body (UTB) SOI single-gate transistor, with the addition of a back-gate electrode fully self-aligned to the front-gate electrode. The DG MOSFET has superior control of short-channel effects for very small MOSFETs, due to the gate field from two gates, which reduces the influence of field from the source/drain. Also, since current can flow along both the top and bottom surfaces of the silicon body, rather than just along the top surface as in the case of UTB SOI single-gate MOSFET, the drive current can almost double that of the single-gate device. The superior electrostatic control of the gate over channel for double-gate structure is highly advantageous for MOSFETs as gate length is scaled below 25 nm [86]. DG MOSFETs are being fabricated in various device topologies.

4.1 Types of Multiple-Gate Structures

DG MOSFETs offer significant improvements in short-channel characteristics, but mass fabrication of DG MOSFETs is not easy. Different types of device geometries are being tried out to exploit the advantages of the multiple-gate MOSFETs. Some of the devices that are being widely tried out are shown in Fig. 4.1.

Figure 4.1: Different types of multiple gate structures [87], [88].

4.2 Symmetric and Asymmetric Double-Gate MOSFETs

Although different types of structures like Pi-Gate, Omega-gate, surrounding-gate MOSFETs and FinFETs are being investigated, the modeling can start with the DG MOSFETs as basic ‘model building block’. Other device architectures can be modeled by adding the corner effects and other extrinsic effects to the core DG MOSFET model. The DG MOSFET model can be classified into symmetric and asymmetric categories based on the structure and terminal biases applied to the two gates. Symmetric DG (s-DG) MOSFETs will have the same oxide thickness for the front and back gates and the gates are also tied together, so it is also called common gate DG MOSFET. The independent

asymmetric DG (a-DG) MOSFET may have different gate oxide thickness, different gate materials and/or different terminal biases applied to the two gates independent of each other.

4.3 Double-Gate MOSFET models

As the DG MOSFETs show promise of highly scaled down devices, they have been receiving considerable attention from the device modeling community. The undoped symmetric DG MOSFETs have been solved both explicitly [89]-[91] and iteratively [92]-[95]. BSIM group at Berkeley has also reported a solution the doped symmetric DG MOSFET problem using a perturbation approach [96]. The undoped asymmetric DG MOSFET has also been solved iteratively. Sparing a few, almost all efforts in DG MOSFET modeling have on the DGMOSFET structures with undoped channels.

4.3.1 Why is it important to model doping?

The volume of a DG MOSFET channel is very small, so the number of atoms in the channel would be small if it is doped. The dopant could be distributed randomly at different locations in different devices. Hence, it could cause fluctuations in electrical characteristics due to the fluctuation in dopant locations. Therefore, doping of the channel in DG MOSFETs is not desired and usually not used. Unfortunately, there would always be a small unintentional doping in a real process. Even a small unintentional doping ($\sim 10^{15} \text{ cm}^{-3}$) could cause a large shift in the surface potential. From compact-modeling point of view, the errors in surface potential due to ignoring doping can be of the order of *mili-volts*, which are unacceptable for compact models that are surface-potential based due to the exponential dependence of the drain-current on surface potentials. Apart from practical considerations, one of the main reasons for ignoring doping in existing DG

models is due to the ensuing mathematical difficulty - the Poisson equation cannot be integrated twice when doping is included.

To investigate the effect of doping, an ideal uniformly-doped long-channel DG MOSFET is simulated using Medici. Figure 4.2 shows the shift in the surface potential from the undoped MOSFET for different doping levels [16]. . Even if the surface potentials are normalized to their own Fermi potentials and the gate voltage is normalized with respect to the flat-band voltages, as would have been done in a model without considering the channel doping, there is an error of the order of mV when the channel is biased in depletion region. This is due to the presence of the acceptor atoms, as shown in Fig. 4.3, which depicts the difference in surface potential of a doped device from that of the undoped device. This implies that a model for undoped DG device cannot be accurate in predicting surface potentials with even (unintentional) doping concentrations.

Figure 4.2: Surface and mid-gap potentials extracted from an ideal Medici s-DG device with (uniform) channel-doping variations and compared with the undoped device [16].

Figure 4.3: The difference between the surface potential of the doped device with the undoped one in Fig. 1 after normalizing to the respective Fermi potentials [16].

Figure 4.4 shows the $\log(I_d)$ – V_g characteristics of an a-DG MOSFET from MEDICI simulations. The plot shows the shift in the drain-current characteristics with different channel doping for a channel thickness of 20 nm. The back gate is biased at zero volts. The plot shows the difference in the drain-current for different substrate doping indicating order of magnitude difference in the drain current in sub-threshold region when the channel doping in creases. Hence, developing a unified DG MOSFET model scalable for different channel doping is very important.

Figure 4.4: $\text{Log}(I_d)$ vs. V_g characteristics of an a-DG MOSFET with different substrate doping.

4.3.2 Double-gate MOSFET model

The basic starting equation for Double-gate MOSFETs is the Poisson's equation. Using the graduate channel approximation and an assumption of constant electron quasi-Fermi level in the direction perpendicular to gate, we get

$$\begin{aligned}
 \frac{d^2\psi}{dx^2} &= -\frac{\rho}{\epsilon_{Si}} = -\frac{q(p-n+N_D-N_A)}{\epsilon_{Si}} = \frac{q}{\epsilon_{Si}}(n-p+N_A-N_D) \\
 &= \frac{q}{\epsilon_{Si}} \left[n_i e^{(\psi-\phi_F-V_c)/v_{th}} - n_i e^{-(\psi-\phi_F)/v_{th}} + n_i e^{\phi_F/v_{th}} - n_i e^{-(\phi_F+V_c)/v_{th}} \right] \\
 &= \frac{qN_A}{\epsilon_{Si}} \left[e^{(\psi-2\phi_F-V_c)/v_{th}} - e^{-\psi/v_{th}} + 1 - e^{-(2\phi_F+V_c)/v_{th}} \right] \\
 &\equiv \frac{qN_A}{\epsilon_{Si}} G(\psi, V_c) \\
 G(\psi, V_c) &= e^{(\psi-2\phi_F-V_c)/v_{th}} - e^{-\psi/v_{th}} + 1 - e^{-(2\phi_F+V_c)/v_{th}}
 \end{aligned} \tag{4.1}$$

The generic boundary conditions at the two surfaces of the silicon (semiconductor) channel can be given by

$$\psi(0, y) = \phi_s(y), \quad E_x(0, y) = E_s(y) = -\phi'_s(y) \tag{4.2a}$$

$$\psi(t_{Si}, y) = \phi_b(y), \quad E_x(t_{Si}, y) = E_b(y) = -\phi'_b(y) \tag{4.2b}$$

(4.1) can be integrated once to get

$$\begin{aligned}
\frac{E_s^2 - E_b^2}{2} &= \int_{E_0}^{E_s} E_x dE_x = \int_{\phi_b}^{\phi_s} \frac{d^2\psi}{dx^2} d\psi \\
&= \frac{qN_A}{\epsilon_{Si}} \int_{\phi_b}^{\phi_s} G(\psi, V_c) d\psi \\
&= \frac{qN_A}{\epsilon_{Si}} \left\{ e^{-(2\phi_F + V_c)/v_{th}} \left[v_{th} \left(e^{\phi_s/v_{th}} - e^{\phi_b/v_{th}} \right) - (\phi_s - \phi_b) \right] \right. \\
&\quad \left. + v_{th} \left(e^{-\phi_s/v_{th}} - e^{-\phi_b/v_{th}} \right) + (\phi_s - \phi_b) \right\} \\
&\equiv \frac{qN_A}{\epsilon_{Si}} F_s^2(\phi_s, \phi_b, V_c). \\
F_s(\phi_s, \phi_b, V_c) &= \sqrt{e^{-(2\phi_F + V_c)/v_{th}} \left[v_{th} \left(e^{\phi_s/v_{th}} - e^{\phi_b/v_{th}} \right) - (\phi_s - \phi_b) \right] + v_{th} \left(e^{-\phi_s/v_{th}} - e^{-\phi_b/v_{th}} \right) + (\phi_s - \phi_b)}
\end{aligned} \tag{4.3}$$

The general boundary conditions are given for SOI/DG using the Gauss law at the front/top gate ($x = 0$):

$$E_s = -\phi_s' = -\frac{\epsilon_{oxf}}{\epsilon_{Si}} \frac{V_{gf} - \phi_s}{t_{oxf}}, \quad (V_{gf} \equiv V_g - V_{FBf}) \tag{4.4a}$$

and the back/bottom gate ($x = x_0 = t_{Si}$; $E_0 = E_b$, $\phi_0 = \phi_b$):

$$E_b = -\phi_b' = +\frac{\epsilon_{oxb}}{\epsilon_{Si}} \frac{V_{bf} - \phi_b}{t_{oxb}}, \quad (V_{bf} \equiv V_b - V_{FBb}) \tag{4.4b}$$

where V_j is the front ($j = g$) or back ($j = b$) gate voltage. $V_{FBj} = \phi_{MSj} - Q_{oxj}/C_{oxj}$ and $C_{oxj} = \epsilon_{oxj}/t_{oxj}$ are the flat-band voltages and oxide capacitance (per unit area) at the respective gates. Applying (4.4) to (4.3), one obtains *one* generic master (input) voltage equation with *two* unknowns (ϕ_s and ϕ_b).

$$\begin{aligned}
&\frac{C_{oxf}}{\epsilon_{Si}} (V_{gf} - \phi_s)^2 - \frac{C_{oxb}}{\epsilon_{Si}} (V_{bf} - \phi_b)^2 \\
&= \frac{qN_A}{\epsilon_{Si}} \left\{ e^{-(2\phi_F + V_c)/v_{th}} \left[v_{th} \left(e^{\phi_s/v_{th}} - e^{\phi_b/v_{th}} \right) - (\phi_s - \phi_b) \right] + v_{th} \left(e^{-\phi_s/v_{th}} - e^{-\phi_b/v_{th}} \right) + (\phi_s - \phi_b) \right\}
\end{aligned} \tag{4.5}$$

This equation cannot be solved explicitly as it has two unknowns. We use our unified regional solution to solve (4.5). We have solved the case of symmetric and asymmetric DG MOSFETs regionally [40].

4.3.2.1 Symmetric double-gate MOSFET model

The symmetric DG MOSFET, or the common-gate MOSFET, is a special case of DG MOSFETs where the field at the mid-gap is zero. For symmetric DG with identical gate materials, oxide thickness, and $V_g = V_b$, the potential gradient at the mid-gap ($x_0 = t_{Si}/2$) is always zero ($E_0 = -\phi'_0 = 0$). Figure 4.5 shows the generic DG MOSFET structure and the co-ordinates used in our model.

Figure 4.5: Generic MOSFET structure and coordinate.

For a symmetric DG MOSFET, using the boundary condition ($E_0 = -\phi'_0 = 0$) in (4.3),

$$\begin{aligned}
 F_s(\varphi_s, \varphi_0, v_c) &\equiv \left[\int_{\varphi_0}^{\varphi_s} G(\psi, V_c) d\psi \right]^{1/2} = \frac{E_s}{\sqrt{2qN_A/\epsilon_{Si}}} \\
 &= \text{sgn}(\varphi_s) \sqrt{v_{th} \left\{ e^{-(2\varphi_s + v_c)} \left[(e^{\varphi_s} - e^{\varphi_0}) - (\varphi_s - \varphi_0) \right] + (e^{-\varphi_s} - e^{-\varphi_0}) + (\varphi_s - \varphi_0) \right\}} \quad (4.6) \\
 &\equiv \text{sgn}(\varphi_s) \sqrt{f_\phi(\varphi_s, \varphi_0, v_c)}
 \end{aligned}$$

in which $\varphi_s = \phi_s/v_{th}$, $\varphi_0 = \phi_0/v_{th}$, and $v_c = V_c/v_{th}$ are the normalized (to the thermal voltage, v_{th}) surface potential, potential at $x = x_0$, and channel voltage, respectively. Applying (4.6)

and the mid-gap field to (4.5), we get the input voltage equation of a symmetrical DG MOSFET

$$(V_{gf} - \phi_s)^2 = \gamma^2 \left\{ e^{-(2\phi_F + V_c)/v_{th}} \left[v_{th} (e^{\phi_s/v_{th}} - e^{\phi_0/v_{th}}) - (\phi_s - \phi_0) \right] + v_{th} (e^{-\phi_s/v_{th}} - e^{-\phi_0/v_{th}}) + (\phi_s - \phi_0) \right\} \quad (4.7)$$

where $\gamma = (2q\epsilon_{Si}N_A)^{1/2}/C_{ox}$ is the body factor. The difference of ϕ_s and ϕ_0 can be expressed as

$$\phi_s - \phi_0 = \sqrt{2qN_A/\epsilon_{Si}} \int_0^{x_0} f(\phi_s, \phi_0, \phi_F, V_c) dx. \quad (4.8)$$

ϕ_s and ϕ_0 can be solved by combining (4.7) and (4.8), [16], [40]. But the second closed-form integral of Poisson equation in (4.8) is not possible. Hence, we get an implicit solution. We use a unified regional approach to solve this implicit equation. The DG MOSFET operation can be divided into four regions: accumulation, depletion, weak inversion (or volume inversion), and strong inversion. The potentials can be solved analytically in each region, and then smoothed using an interpolation function.

4.3.2.1.1 Accumulation

In the accumulation region, only the term corresponding to holes need be considered without any loss in accuracy. (4.7) can then be approximated by

$$(V_{gf} - \phi_s)^2 = \gamma^2 \left\{ v_{th} (e^{-\phi_s/v_{th}} - e^{-\phi_0/v_{th}}) \right\} \quad (4.9)$$

Also, we can integrate the Poisson equation twice when only the holes are considered

$$\frac{q(\phi_s - \phi_0)}{2kT} = \ln \left[\cos \left(\frac{t_{Si}}{2} \sqrt{\frac{q^2 N_A}{2\epsilon_{Si} kT}} e^{-\phi_0/2v_{th}} \right) \right] \quad (4.10)$$

ϕ_0 tends to be a constant when the gate voltage assumes large negative values. The minimum ϕ_0 can be determined from [102]

$$\phi_{0\min} = -\frac{2kT}{q} \ln \left(\frac{\pi}{t_{Si}q} \sqrt{\frac{2\varepsilon_{Si}kT}{N_A}} \right). \quad (4.11a)$$

We can see that $\phi_{0\min}$ is independent of oxide thickness as shown in (4.11a). The unified mid-gap potential in the accumulation region is obtained by unifying (4.11a) with the function V_{gbr} :

$$\phi_s = \mathcal{G}_{eff} \{ \phi_{0,\min}, V_{gbr}; \delta \} \quad (4.11b)$$

$$\mathcal{G}_{eff} \{ x, x_{sat}; \delta \} \equiv x_{sat} - 0.5 \left[x_{sat} - x - \delta + \sqrt{(x_{sat} - x - \delta)^2 + 4\delta x_{sat}} \right]$$

where V_{gbr} is defined by $V_{gbr} = \mathcal{G}_r \{ x; \sigma_a \} \equiv -0.5 \left(-x + \sqrt{x^2 + 4\sigma_a} \right)$ with $x = V_g - V_{FBf}$. Once the mid-gap potential is determined, the surface potential in accumulation can be calculated from (4.10).

4.3.2.1.2 Depletion

In the depletion region, when the channel is not fully depleted, the hole and electron terms can be considered negligible. When the channel is not fully depleted, the mid channel potential is zero (as in the case of a bulk MOSFET):

$$\phi_0 = 0, \quad e^{-2\phi_F/v_{th}} \left(e^{\phi_s/v_{th}} - e^{\phi_0/v_{th}} \right) \approx 0, \quad \left(e^{-\phi_s/v_{th}} - e^{-\phi_0/v_{th}} \right) \approx 0$$

Applying the above boundary conditions to the master equation (4.7) we get

$$V_{gf} - \phi_s = \gamma \sqrt{\phi_s} \quad (4.12)$$

The surface potential in the depletion region can then be obtained by the equation

$$\phi_{s,dd} = \left[-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_g - V_{FBf}} \right]^2. \quad (4.13a)$$

The regional solution in (4.13a) is not valid below the flat-band voltage as the square root would return imaginary values. The regional solution can be then converted to a unified regional solution by using the smoothing function defined by

$$V_{gbf} = \mathcal{G}_f \{x; \sigma_f\} \equiv 0.5 \left(x + \sqrt{x^2 + 4\sigma_a} \right) \text{ with } x = V_g - V_{FBf} \text{ to replace } V_g - V_{FBf} \text{ in (4.13a)}$$

$$\phi_{s,sub} = \left[-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{gbf}} \right]^2. \quad (4.13b)$$

The regional depletion solution shown in (4.13b) is not physical once the channel is fully depleted. The onset of weak inversion is at the voltage where the channel is just fully depleted, which is given from Poisson solution by the expression

$$V_{FD} = V_{FB} + \frac{qN_A(t_{Si}/2)^2}{2\epsilon_{Si}} + \frac{qN_A(t_{Si}/2)}{C_{ox}}. \quad (4.14)$$

In partially depleted and bulk devices, the V_{FD} lies above the region of operation and, hence, the model scales physically with thickness and doping. The accurate determination of V_{FD} is crucial for the unified modeling approach. The regional depletion piece is unified at the V_{FD} voltage using the same interpolation function as is used for the depletion and accumulation unification. The regional gate voltage solution that is applied to the depletion region ($V_{g,d}$) is given by the functions $V_{FD} - 0.5 \left(-x + \sqrt{x^2 + 4\sigma_f} \right)$, where $x = V_{gbf} + V_{FB} - V_{FD}$. V_{gbf} is the forward function at the flat-band voltage. This regional gate voltage solution is valid from flat-band voltage to the onset of weak inversion. The regional unified surface potential in the depletion region is given by

$$\phi_{s,sub} = \left[-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{g,d} - V_{FBf}} \right]^2. \quad (4.15)$$

The accurate determination of the V_{FD} voltage is the key to the regional model. Figure 4.6 shows the accurate prediction of the V_{FD} voltage for different channel doping in comparison with that extracted for the same device from Medici simulations.

Figure 4.6: Prediction of the fully-depleted voltage (V_{FD}) for different channel doping, validated with those extracted from the corresponding Medici simulation results [16].

4.3.2.1.3 Weak inversion

In the weak (or volume) inversion region, the channel is completely depleted. The holes and (inversion) electrons can be considered negligible as the strong inversion is yet to set-in, implying:

$$e^{-\phi_s/v_{th}} - e^{-\phi_0/v_{th}} \approx 0, \quad e^{-2\phi_F/v_{th}} (e^{\phi_s/v_{th}} - e^{\phi_0/v_{th}}) \approx 0 \quad (4.16)$$

In the weak-inversion region, the channel is fully depleted. So, the depletion charge is given by

$$Q_b = -qN_A (t_{Si}/2) \quad (4.17)$$

After applying (4.16) and (4.17) to the equation (4.7) we get

$$V_{gf} - \phi_s = \frac{qN_A (t_{Si}/2)}{C_{ox}}. \quad (4.18)$$

Rearranging the solution we get the surface potential solution for the weak inversion region

$$\phi_{s,vi} = V_g - V_{FBf} - \frac{qN_A(t_{Si}/2)}{C_{ox}}. \quad (4.19a)$$

The weak-inversion solution is derived assuming the complete depletion of the channel body and, hence, cannot be used in the depletion region. The regional solution can be unified using a regional gate voltage solution. The regional gate voltage solution for the weak-inversion region ($V_{g,inv}$) is given by the functions $V_{FD} + 0.5\left(x + \sqrt{x^2 + 4\sigma_f}\right)$ where x is given by $x = V_{gbf} + V_{FB} - V_{FD}$ and V_{gbf} is the forward function at the flat-band voltage.

The unified regional weak inversion solution is given by

$$\phi_{s,vi} = V_{g,inv} - V_{FBf} - \frac{qN_A(t_{Si}/2)}{C_{ox}}. \quad (4.19b)$$

The mid-gap potential in the weak inversion region can be calculated by considering the film to be completely-depleted. Applying the full depletion approximation, we get the regional unified mid channel potential as

$$\phi_{0,vi} = \phi_{s,vi} - \frac{qN_A(t_{Si}/2)^2}{2\epsilon_{Si}} \quad (4.20)$$

4.3.2.1.4 Strong inversion

When the surface potential reaches twice the Fermi potential (i.e., at the “threshold voltage,” V_t), the device operates in the strong-inversion region. In this region, a closed-form expression for the potential cannot be obtained when both the acceptor and the electron terms are included in the equation. We make use of the assumption of complete depletion of the channel body to derive a relation between ϕ_s and ϕ_0 [97], [98]:

$$\phi_s - \phi_0 = \frac{qN_A (t_{Si}/2)^2}{2\epsilon_{Si}}. \quad (4.21)$$

When this approximation is used, the surface potential in strong inversion can be derived as [99]

$$\begin{aligned} \phi_{s, str} &= 2\phi_F + \Delta \\ \Delta &= v_{th} \ln(a/b) \\ a &= \frac{1}{\gamma^2} (V_g - V_{FB} - \phi^*)^2 \\ b &= v_{th} \left\{ 1 - \exp \left[-\frac{1}{v_{th}} \left(\frac{qN_A (t_{Si}/2)^2}{2\epsilon_{Si}} \right) \right] \right\}. \end{aligned} \quad (4.22)$$

The strong-inversion potential is then smoothed with the other surface potential pieces to give a unified regional surface-potential expression [100]. As will be seen, the key to physical parameter scalability lies in the physically-derived expressions for the “turning” voltages, V_{FB} , V_{FD} , and V_t , combined with the interpolation functions in the unified regional approach.

Figure 4.7. Regional and unified solution for the surface and geometric center potentials of a doped s-DG MOSFET, compared with the ideal Medici device [16].

Figure 4.7 shows the regional surface potential and mid channel potential solutions from the model (lines) and Medici device simulations (symbols). A high channel doping (10^{18} cm^{-3}) with a 20-nm channel thickness device is used to show the various regional pieces, while the model physically scales with doping and channel thickness. The figure shows the regional accumulation, depletion, weak-inversion, and strong-inversion pieces. The transition from depletion to weak inversion is modeled physically by the fully-depleted voltage, V_{FD} . The strong-inversion piece is derived using a non-pinned delta function (4.22), consistent with our bulk-charge formulation [44]. In the volume and strong-inversion regions, the difference between ϕ_s and ϕ_0 is given by (4.21), which is the key to the volume-inversion modeling. The small error in ϕ_0 in the strong-inversion region is due to this approximation; however, its effect on ϕ_s is negligible. The accuracy of ϕ_0 does not have much effect on the drain-current formulation either. Hence, this simple regional unified surface-potential model can be used in the s-DG drain-current formulation.

4.3.2.2 Asymmetric double-gate MOSFET model

The asymmetric DG MOSFET or independent-gate MOSFET can have many different configurations, and asymmetry can arise from different gate work functions, different gate insulator thicknesses or dielectric constants, and different terminal biases applied to the two gates. Modeling of the doped asymmetric DG MOSFET is one of the most challenging tasks. The general equation for an a-DG MOSFET is given by (4.5)

$$\begin{aligned} & \frac{C_{oxf}}{\epsilon_{Si}} (V_{gf} - \phi_s)^2 - \frac{C_{oxb}}{\epsilon_{Si}} (V_{gb} - \phi_b)^2 \\ &= \frac{2qN_A}{\epsilon_{Si}} \left\{ e^{-(2\phi_F + V_{cb})/v_{th}} \left[v_{th} (e^{\phi_s/v_{th}} - e^{\phi_b/v_{th}}) - (\phi_s - \phi_b) \right] + v_{th} (e^{-\phi_s/v_{th}} - e^{-\phi_b/v_{th}}) + (\phi_s - \phi_b) \right\} \end{aligned} \quad (4.23)$$

where $C_{oxj} = \epsilon_{oxj}/t_{oxj}$ ($j=f,b$) are the front or back-gate capacitance (per unit area) with dielectric constant ϵ_{oxj} and thickness t_{oxj} , respectively. The equation can be rewritten in the form

$$\begin{aligned} & (V_{gf} - \phi_s)^2 - \frac{C_{oxb}}{C_{oxf}} (V_{bf} - \phi_b)^2 \\ &= \gamma_f^2 \left\{ e^{-(2\phi_f + V_{cb})/v_{th}} \left[v_{th} (e^{\phi_s/v_{th}} - e^{\phi_b/v_{th}}) - (\phi_s - \phi_b) \right] + v_{th} (e^{-\phi_s/v_{th}} - e^{-\phi_b/v_{th}}) + (\phi_s - \phi_b) \right\} \end{aligned} \quad (4.24)$$

where $\gamma_f = \sqrt{2\epsilon_{Si}N_A}/C_{oxf}$ is the body factor associated with the front gate. This general a-DG MOSFET equation can cater to several device topologies by applying the correct boundary condition.

4.3.2.2.1 Depletion

We have used two different cases for deriving the potentials in the depletion region in the front (top) and back (bottom) gates of an a-DG. The two cases are

1. When either one of the gates depletes the body of the channel completely, and,
2. When both the gates share the depletion charge in the channel.

When the MOSFET is operating in the depletion region, the potential and the field in the un-depleted neutral region is zero. Hence, we can consider both the gates as independent of each other. In the depletion region, the hole and electron concentration is negligible and can be ignored. The unified regional front- and back-gate surface potentials are given by:

$$\begin{aligned} \phi_{s,d} &= \left[-\frac{\gamma_f}{2} + \sqrt{\frac{\gamma_f^2}{4} + V_{gf}} \right]^2 \\ \phi_{b,d} &= \left[-\frac{\gamma_b}{2} + \sqrt{\frac{\gamma_b^2}{4} + V_{bf}} \right]^2 \end{aligned} \quad (4.25)$$

where $\gamma_f = \sqrt{2\epsilon_{Si}qN_A / C_{oxf}}$, $\gamma_b = \sqrt{2\epsilon_{Si}qN_A / C_{oxb}}$ and V_{gf} and V_{bf} are given by the functions

$$\begin{aligned} V_{gf} &= 0.5 \left(x + \sqrt{x^2 + 4\sigma_f} \right), \quad x = V_g - V_{FBf} \\ V_{bf} &= 0.5 \left(x + \sqrt{x^2 + 4\sigma_f} \right), \quad x = V_b - V_{FBb} \end{aligned} \quad (4.26)$$

where σ_f is a model parameter. The flat-band voltages at the two gates capture the change in work function in the gates. The total depletion widths at the front/back gate are given by the expressions

$$\begin{aligned} x_{d,f} &= \sqrt{\frac{2\epsilon_{Si}\phi_{s,d}}{qN_A}} \\ x_{d,b} &= \sqrt{\frac{2\epsilon_{Si}\phi_{b,d}}{qN_A}} \end{aligned} \quad (4.27)$$

We make use of a simple loop, which uses the sum of the depletion widths to calculate the biases at which the channel is fully depleted. The sum of the two depletion widths should be equal to the channel thickness.

$$t_{Si} = x_{d,f} + x_{d,b} \quad (4.28)$$

which is the key to linking the two “independent” front- and back-gate surface potential solutions. For the unified regional depletion solution, the front- and back-gate voltages at which the channel is fully depleted need to be calculated. Similar to the s-DG, the a-DG fully-depleted voltages are (independently) given by the 1-D voltage balance equation

$$\begin{aligned} V_{FDf} &= V_{FBf} + \frac{qN_A x_{df}^2}{2\epsilon_{Si}} + \frac{qN_A x_{df}}{C_{oxf}} \\ V_{FDb} &= V_{FBb} + \frac{qN_A x_{db}^2}{2\epsilon_{Si}} + \frac{qN_A x_{db}}{C_{oxb}} \end{aligned} \quad (4.29)$$

Similar to the s-DG formulation, the gate voltages V_g and V_b need to be smoothed at the V_{FDf} and V_{FDb} voltages to be used in the unified regional depletion solutions. The unified solutions are given by the expressions

$$\begin{aligned} V_{g,d} &= V_{FDf} - 0.5 \left(-x + \sqrt{x^2 + 4\sigma_f} \right), \quad x = V_{gf} + V_{FBf} - V_{FDf} \\ V_{b,d} &= V_{FDb} - 0.5 \left(-x + \sqrt{x^2 + 4\sigma_f} \right), \quad x = V_{bf} + V_{FBb} - V_{FDb} \end{aligned} \quad (4.30)$$

and the smoothed V_{gf} and V_{bf} functions are given by the expression (4.26). When the depletion charge is shared by both the gates, there is a zero field point in the body of the channel and hence bulk like solutions can be derived.

$$\begin{aligned} \phi_{s,sub} &= \left[-\frac{\gamma_f}{2} + \sqrt{\frac{\gamma_f^2}{4} + V_{g,d} - V_{FBf}} \right]^2 \\ \phi_{b,sub} &= \left[-\frac{\gamma_b}{2} + \sqrt{\frac{\gamma_b^2}{4} + V_{b,d} - V_{FBb}} \right]^2 \end{aligned} \quad (4.31)$$

The second case is when one of the gates depletes the channel completely. When the back gate depletes the complete channel, the potential due to depletion at the front and back gates can be given respectively by

$$\begin{aligned} \phi_{b,sub} &= \frac{qN_A t_{Si}^2}{2\epsilon_{Si}} \\ \phi_{s,sub} &= 0 \end{aligned} \quad (4.32)$$

Since the entire channel body is depleted by the back gate bias, the potential due to the depletion charges at the front surface is zero. The other scenario of front gate depleting the complete channel can be treated in a similar way. The fully depleted voltages V_{FDf} and V_{FDb} are calculated based on the expressions

$$\begin{aligned}
 V_{FDf} &= V_{FBf} \\
 V_{FDb} &= V_{FBb} + \frac{qN_A t_{Si}^2}{2\epsilon_{Si}} + \frac{qN_A t_{Si}}{C_{oxb}} \quad (4.33)
 \end{aligned}$$

The regional depletion solutions are then unified at the fully depleted voltages using the interpolation functions discussed above. When the gate voltages, metal work-function and oxide capacitances are the same for both the gates, they have equal depletion widths given by half of the channel thickness and, the unified regional depletion solution converges to the s-DG structure.

4.3.2.2.2 Weak inversion

In the weak or volume inversion, the channel has already fully depleted. The voltage for depleting the full channel is given by the same equations as given by (4.29) and (4.33), in which x_{df} and x_{db} are calculated from the derived $\phi_{s,sub}$ and $\phi_{b,sub}$ expressions. From the Poisson's equation, we can re-derive the field expression to get

$$\frac{d\psi}{dx} = \sqrt{\frac{2kTN_A}{\epsilon_{Si}}} \left(v_{th} e^{(\psi - V_c - 2\phi_F)/v_{th}} + \psi - C_1 \right) \quad (4.34)$$

where C_1 is an integration constant. We propose an approximation to break the right-hand side of (4.34) into sum of two square-root terms:

$$\frac{d\psi}{dx} = \sqrt{\frac{2kTN_A}{\epsilon_{Si}}} (\psi) + \sqrt{\frac{2kTN_A e^{-2\phi_F/v_{th}}}{\epsilon_{Si}}} \left(v_{th} e^{(\psi - V_c)/v_{th}} - C_1 \right) \quad (4.35)$$

When the Gauss law boundary conditions are applied to the front and back gates, we get two equations

$$V_g - V_{FBf} - \phi_s = \gamma_f \sqrt{\phi_s} + \gamma_f \sqrt{\left(v_{th} e^{(\phi_s - 2\phi_F)/v_{th}} - C_1 \right)} \quad (4.36)$$

$$V_b - V_{FBb} - \phi_b = \gamma_b \sqrt{\phi_b} + \gamma_b \sqrt{\left(v_{th} e^{(\phi_b - 2\phi_f)/v_{th}} - C_1 \right)}. \quad (4.37)$$

The $\gamma_f \sqrt{\phi_s}$ and $\gamma_b \sqrt{\phi_b}$ terms are the bulk-charge terms associated with the front and back gates. When the channel is fully depleted, the bulk charge terms can be replaced by $qN_A x_{df} / C_{oxf}$ and $qN_A x_{db} / C_{oxb}$, respectively. Now (4.36) and (4.37) can be approximated to get the following equations:

$$V_g - V_{FBf} - \phi_s - \frac{qN_A x_{df}}{C_{oxf}} = +\gamma_f \sqrt{\left(v_{th} e^{(\phi_s - 2\phi_f)/v_{th}} - C_1 \right)} \quad (4.38)$$

$$V_b - V_{FBb} - \phi_b - \frac{qN_A x_{db}}{C_{oxb}} = +\gamma_b \sqrt{\left(v_{th} e^{(\phi_b - 2\phi_f)/v_{th}} - C_1 \right)}. \quad (4.39)$$

The potentials at the front and back gates can be considered as the sum of the potential due to the depletion charge and that due to the inversion charge in weak and strong inversion.

$$\begin{aligned} \phi_s &= \phi_{s,d} + \phi_{s,i} \\ \phi_b &= \phi_{b,d} + \phi_{b,i} \end{aligned} \quad (4.40)$$

Now using (4.40) in (4.38) and (4.39) we get

$$\begin{aligned} V_g - V_{FBf} - (\phi_{s,d} + \phi_{s,i}) - \frac{qN_A x_{df}}{C_{oxf}} &= +\gamma_f \sqrt{\left(v_{th} e^{(\phi_s - 2\phi_f)/v_{th}} - C_1 \right)} \\ V_b - V_{FBb} - (\phi_{b,d} + \phi_{b,i}) - \frac{qN_A x_{db}}{C_{oxb}} &= +\gamma_b \sqrt{\left(v_{th} e^{(\phi_b - 2\phi_f)/v_{th}} - C_1 \right)}. \end{aligned} \quad (4.41)$$

The flat-band voltage, potential due to depletion and the bulk charge can be combined to give the fully depleted voltages as described in (4.29) and (4.33)

$$\begin{aligned}
V_g - \left(V_{FBf} + \phi_{s,d} + \frac{qNx_{df}}{C_{oxf}} \right) - \phi_{s,i} &= +\gamma_f \sqrt{\left(v_{th} e^{(\phi_s - 2\phi_f)/v_{th}} - C_1 \right)} \\
V_b - \left(V_{FBb} + \phi_{b,d} + \frac{qNx_{db}}{C_{oxb}} \right) - \phi_{b,i} &= +\gamma_b \sqrt{\left(v_{th} e^{(\phi_b - 2\phi_f)/v_{th}} - C_1 \right)}.
\end{aligned} \quad (4.42)$$

In the weak-inversion region, the terms $\phi_{s,vi}$ and $\phi_{b,vi}$ represent the inversion potential.

$$V_g - V_{FDf} - \phi_{s,vi} = \gamma_f \sqrt{\left(v_{th} e^{(\phi_s - 2\phi_f)/v_{th}} - C_1 \right)} \quad (4.43)$$

$$V_b - V_{FDb} - \phi_{b,vi} = +\gamma_b \sqrt{\left(v_{th} e^{(\phi_b - 2\phi_f)/v_{th}} - C_1 \right)}. \quad (4.44)$$

Combing (4.43) and (4.44) eliminating constant of integration C_1 and simplifying, we get an implicit equation. After applying the approximation $\ln[\cos(i\theta)] \approx \theta - \ln 2$ ($\theta \gg 1$) and omitting the $e^{\phi_{vi}/v_{th}}$ term and other negligible terms, we get a final explicit solution in the weak or volume inversion region [91]:

$$\phi_{s,vi} = \frac{\frac{C_{oxf}}{C_{oxb}} \left(1 + \frac{C_{oxb} t_{Si}}{\epsilon_{Si}} \right) (V_g - V_{FDf}) + (V_b - V_{FDb})}{1 + \frac{C_{oxf}}{C_{oxb}} \left(1 + \frac{C_{oxb} t_{Si}}{\epsilon_{Si}} \right)} \quad (4.45)$$

$$\phi_{b,vi} = \frac{\frac{C_{oxb}}{C_{oxf}} \left(1 + \frac{C_{oxf} t_{Si}}{\epsilon_{Si}} \right) (V_b - V_{FDb}) + (V_g - V_{FDf})}{1 + \frac{C_{oxb}}{C_{oxf}} \left(1 + \frac{C_{oxf} t_{Si}}{\epsilon_{Si}} \right)}. \quad (4.46)$$

The sub-threshold piece is given by adding the potentials in the depletion region and the weak-inversion region, as shown in (4.40). The weak-inversion potentials, given by (4.45) and (4.46), include the two flat-band voltages, channel thickness, two oxide capacitances and the two gate voltages. Hence, they scale physically with all structural and bias variations. When the two gate biases and oxide capacitances are set to be the

same as in the case of a s-DG structure, the model converges to the simple s-DG equations derived in (4.19).

4.3.2.2.3 Strong inversion

When the front gate is in strong inversion, surface potential (ϕ_s) is strongly influenced by V_g rather than by V_b . In that case, ignoring the coupling between the two gates, we get a solution for the strong inversion as [91]

$$\phi_{s, str} = V_{gi} - V_{FDf} - 2v_{th} \mathcal{L}_+ \left\{ \frac{q}{C_{oxf}} \sqrt{\frac{N_A e^{-2\phi_f/v_{th}} \epsilon_{Si}}{2kT}} e^{(V_{gi} - V_{FDf} - V_c)/2v_{th}} \right\} \quad (4.47)$$

where $\mathcal{L}_+\{w\}$ is the *Lambert W* function (principal branch). After the potentials are solved analytically in each region, we use the following smoothing function to obtain a unified (explicit) ϕ_s model [44]

$$\phi_s = \mathcal{G}_{eff} \{ \phi_{s, sub}, \phi_{s, str}; \delta \} \quad (4.48)$$

$$\mathcal{G}_{eff} \{ x, x_{sat}; \delta \} \equiv x_{sat} - 0.5 \left[x_{sat} - x - \delta + \sqrt{(x_{sat} - x - \delta)^2 + 4\delta x_{sat}} \right] \quad (4.49)$$

where δ is a smoothing parameter. The explicit regional ϕ_b equations are similar to those for ϕ_s by swapping subscripts 's' and 'b'

$$\phi_{b, str} = (V_b - V_{FDb}) - 2v_{th} \mathcal{L}_+ \left\{ \frac{q}{C_{oxb}} \sqrt{\frac{N_A e^{-2\phi_f/v_{th}} \epsilon_{Si}}{2kT}} e^{((V_b - V_{FDb}) - V_c)/2v_{th}} \right\} \quad (4.50)$$

$$\phi_b = \mathcal{G}_{eff} \{ \phi_{b, sub}, \phi_{b, str}; \delta \}. \quad (4.51)$$

There are four cases of interest for ϕ_s and ϕ_b in different asymmetric operating conditions:

(i) both gates biased in sub-threshold; (ii) front gate is biased in sub-threshold while back gate is biased in strong inversion; (iii) back gate is biased in sub-threshold while front gate is in strong inversion; and (iv) both gates are in strong inversion. Cases 1 and 4 have

been solved by utilizing the above explicit expressions for surface potentials. The solutions for case 1 and 4 are derived assuming both the gates are independent. Hence, the strong-inversion solutions need not be added to the depletion solution as derived in (4.40). For case 2 or 3, the behavior of ϕ_s and ϕ_b is a little different. For example, when ϕ_s is in strong inversion and ϕ_b in volume inversion, the behavior of ϕ_b can be extracted from ϕ_s based on the following relationship [91]

$$\phi_{b, str} = \phi_{b, sub} + (V_b - V_{FD b}) - \frac{2v_{th}}{1 + \frac{C_{oxb} t_{Si}}{\epsilon_{Si}}} \times L_- \left\{ \frac{-q}{C_{box}} \sqrt{\frac{N_A e^{-2\phi_F/v_{th}} \epsilon_{Si}}{2kT}} \left(1 + \frac{C_{oxb} t_{Si}}{\epsilon_{Si}} \right) e^{((V_b - V_{FD b}) - V_c)/2v_{th}} \right\} \quad (4.52)$$

When the back gate is not biased in strong inversion, the strong-inversion potential depends strongly on the front gate and the potential due to the depletion term is also added to the strong-inversion potential as in (4.40). The strong-inversion piece is then smoothed with the sub-threshold piece to get the unified back-gate surface potential.

Figure 4.8: Regional and unified solution for the front- and back-gate surface potentials of a doped a-DG MOSFET, compared with the exact solution from Medici device simulator. The back gate is biased at flat-band voltage.

Figure 4.9: Regional and unified solution for the front- and back-gate surface potentials of a doped a-DG MOSFET, compared with the exact solution from Medici device simulator. The back gate depletes the complete channel and is biased at weak inversion.

Figures 4.8 and 4.9 show the regional pieces and unified model for the surface potential at the front and back gates. The prediction of surface potential by the model with different back gate biased corresponding to different regions of operation is compared with MEDICI results. The approximation introduced in (4.37) is more accurate when the condition $v_{th} e^{(\phi - 2\phi_F)/v_{th}} \gg \phi$ is true, implying that the contribution of dopants is negligible compared to electrons. When the back gate is biased at a low voltage, the approximation in (4.37) is not very accurate. This causes the error in the strong-inversion piece of the back gate potential as shown in Fig. 4.8. But this error has little impact on the current and charge values, as the gate is not strongly inverted. When the back gate is biased in the weak inversion or strong inversion, the approximation is more accurate and Fig. 4.9 shows the prediction of the model. The model is very accurate when both the gates are biased in strong inversion and the bulk charge is negligible compared to the inversion charge. The accuracy of the model increases as the doping decreases. As the doping decreases, the bulk charge term becomes negligible and is accurate for undoped MOSFETs. The model is derived for a generic structure with two gates and is scalable for different oxide thickness, channel thickness, work function difference, and terminal bias.

4.3.2.3 Symmetric double-gate MOSFET drain-current model

The Pao–Sah double integral solution for the drain current is physical and includes both the drift and the diffusion components as it uses the channel quasi-Fermi potential [20]. This solution cannot be integrated in a closed form. Therefore, all the compact models make use of the charge-sheet approximation [21] to compute the drain current. The drain-current model can be derived based on several modeling techniques

like threshold-voltage based, surface-potential based and inversion-charge based as described in Chapter 2. The unified regional modeling (URM) approach uses a surface-potential based drain-current formulation which does not require very high accuracy of surface potential as demanded by the surface-potential based models. Several groups have solved the drain-current of undoped s-DG and a-DG MOSFETs using iterative and explicit approaches [101]–[104]. The drain-current for an s-DG MOSFET has also been derived based on an iterative approach [96]. This section presents a drain-current model for s-DG MOSFETs derived using the explicit surface and centre of the channel potentials using the URM approach [42]. In the strong-inversion condition, the drift current given by

$$I_{ds} = WvQ_i(y) = -\mu WQ_i(y) \frac{d\phi_s(y)}{dy} \quad (4.53)$$

which is the dominant component, where v is the drift velocity, μ is the carrier mobility and position-dependent inversion charge $Q_i(y)$ in half of the channel is defined based on the depletion approximation.

$$Q_i = -C_{ox} \left(V_{gb} - V_{FB} - \phi_s(y) - \gamma \sqrt{\phi_s(y) - \phi_0(y)} \right). \quad (4.54)$$

The total inversion charge in the channel is given by $2Q_i$. Under the strong-inversion condition, the integrated drain current across the channel from 0 to L_{eff} can be expressed as

$$I_{ds} = \frac{2\mu W}{L} \int_{\phi_s}^{\phi_D} Q_i(y) d\phi_s(y). \quad (4.55)$$

The integrated drain current can be formulated by substituting Q_i from (4.54) into (4.55). A Taylor expansion and further approximation of the bulk-charge term after current

integration at the average of the source and drain potential $[\bar{\phi} = (\phi_s + \phi_D)/2]$ gives the following expression

$$I_{ds} = \frac{2\mu C_{ox} W}{L} \left[V_{gbf} (\phi_D - \phi_s) - \frac{(\phi_D^2 - \phi_s^2)}{2} - \gamma \left(\sqrt{\bar{\phi} - \bar{\phi}_0} \Delta\phi \right) \right] \quad (4.56)$$

where ϕ_s and ϕ_D are the surface potentials at the source and drain side, respectively, which can be further simplified to

$$I_{ds} = \frac{2\mu C_{ox} W}{L} \left[V_{gbf} - \gamma \sqrt{\bar{\phi} - \bar{\phi}_0} - \bar{\phi} \right] \Delta\phi \quad (4.57)$$

where $\Delta\phi = (\phi_D - \phi_s)$. The diffusion current in the drain-current model can be derived as

$$\begin{aligned} I_{ds} &= 2\mu W v_{th} \frac{dQ_i}{dy} \\ \frac{dQ_i}{d\phi} &= -C_{ox} (-\bar{A}_b) = C_{ox} \bar{A}_b \\ &= \frac{2W\mu v_{th}}{L} \int_{\phi(0)}^{\phi(L)} \frac{dQ_i}{d\phi} d\phi = \frac{W\mu v_{th}}{L} C_{ox} \bar{A}_b \int_{\phi_s}^{\phi_D} d\phi \\ &= \frac{2WC_{ox}\mu}{L} v_{th} \bar{A}_b \Delta\phi \end{aligned} \quad (4.58)$$

where $\bar{A}_b = 1$ is the bulk charge factor at $\bar{\phi}$. The total drain current can be given by the expression

$$I_{DS} = \frac{2WC_{ox}\mu_s}{L} \left(V_{gbf} - \gamma \sqrt{\bar{\phi} - \bar{\phi}_0} - \bar{\phi} + \bar{A}_b v_{th} \right) \Delta\phi. \quad (4.59)$$

The $\Delta\phi$ in (4.61) can be replaced by the V_{deff} function and the final drain-current expression is given by the formulation

$$I_{DS} = \frac{2WC_{ox}\mu_s}{L} \left(V_{gbf} - \gamma \sqrt{\bar{\phi} - \bar{\phi}_0} - \bar{\phi} + \bar{A}_b v_{th} \right) V_{deff}. \quad (4.60)$$

The V_{deff} function is given by the function [105]

$$\begin{aligned}
 V_{dseff} &= V_{deff} - V_{seff} \\
 V_{deff} &= V_{sat} - \frac{1}{2} \left[V_{sat} - V_d - \delta_s + \sqrt{(V_{sat} - V_d - \delta_s)^2 + 4\delta_s V_{sat}} \right] \\
 V_{seff} &= V_{sat} - \frac{1}{2} \left[V_{sat} - V_s - \delta_s + \sqrt{(V_{sat} - V_s - \delta_s)^2 + 4\delta_s V_{sat}} \right]
 \end{aligned} \quad (4.61)$$

The saturation voltage V_{sat} derivation is consistent with our bulk URM approach. The V_{geff} function in the V_{sat} is given by

$$V_{geff} = \gamma \sqrt{\phi_s - \phi_0 + v_{th} e^{-2\phi_F/v_{th}} (e^{\phi_s/v_{th}} - e^{\phi_0/v_{th}})} - \gamma \sqrt{\phi_s - \phi_0}. \quad (4.62)$$

Figure 4.10 shows the drift and diffusion components of the double-gate MOSFET. The model does not require a high accuracy of surface potential at the source and drain ends.

The scalability of the model for different channel thickness and bias has also been tested.

Figure 4.10: The drift, diffusion and unified drain-current pieces for a doped s-DG MOSFET in the linear region.

4.4 Summary

Surface potential and mid-channel potential for the s-DG MOSFET have been modeled. The model derivation starts with regional solutions for the accumulation, depletion, weak-inversion and strong-inversion regimes of operation of the device. The resultant equations are unified using interpolation functions to yield a unified regional model for surface potential for the s-DG MOSFETs. Further, a generic model for the potentials at the front and back surfaces of an a-DG model is derived. The model is derived with a very general boundary condition and can scale for different device topologies like s-DG, a-DG, SOI and UTB devices. A unified drain-current model based on the surface and mid-channel potential is derived for the s-DG MOSFETs.

CHAPTER 5 EXTRACTION OF PHYSICAL AND MODEL PARAMETERS

This chapter discusses the techniques to extract the physical and model parameters from the measured or MEDICI simulated characteristics of the MOS device structures. There are several extraction and optimization tools commercially available for the extraction of the model parameters from industry standard models by different optimization algorithms. Physical parameters, such as oxide thickness, junction depth, channel doping, Ge mole fraction, strained-layer thickness can be obtained from a given process recipe but they are subject to process fluctuations. The models described in Chapters 2, 3 and 4 have been derived physically, and the performance of the model depends highly on the accuracy of the extracted physical parameters. One of the key advantages of the unified modeling approach has been the minimum measurement data requirement for calibration of the model. This chapter presents a methodology for extraction of the physical parameters of the strained-silicon MOSFET from one measured capacitance–voltage (C–V) measurement based on physics-based compact model and conventional C–V characterization techniques [15], [106], [107].

Strained-silicon gate capacitance

The measured gate capacitance of a surface-channel strained-silicon pMOSFET is shown in Fig 5.1. The MOS capacitors used in this work consisted of strained-Si film on a uniform relaxed SiGe buffer layer with a Ge mole fraction of 0.25 grown on a thick graded SiGe buffer on a silicon wafer. pMOS capacitors were formed by implanting the substrate with a phosphorus dose of $2 \times 10^{13} \text{ cm}^{-2}$ at energy of 300 keV. The thermal oxide was grown at 800°C in a dry O₂ ambient. The capacitors were also built on bulk Si for

reference. The C-V characteristics were measured using HP-4284 LCR meter. The plateau in a surface-channel pMOS shifts from the inversion side to the accumulation side with the increase in substrate doping. This has been discussed in Section 3.3.2. An implicit iterative technique was derived in Section 3.3.3 to capture the shift in the plateau physically.

Figure 5.1: Measured capacitance-voltage characteristics of a strained-silicon pMOS device.

In this chapter, we will use the model equations to extract the physical parameters like band offset and strained-silicon thickness from the measured data. The extracted material and structural parameters are then used in Medici to simulate the device structure for comparison with measured data to validate the extraction approach. The s-Si compact charge model is also compared with the experimental data using the extracted physical parameters.

5.1 Extraction of Physical Parameters

The capacitance-voltage characteristics of s-Si MOSFET give a lot of information regarding the confinement of carriers at different interfaces and in different regions of operation. Some of the physical parameters in s-Si MOSFETs can also be extracted

accurately from the C – V characteristics. As shown in Fig. 5.1 for the gate capacitance characteristics of an s-Si pMOS, when accumulation of electrons occurs at the bottom interface, the top strained layer is depleted of mobile charges and it acts like a dielectric. As discussed in Chapter 3, the effective capacitance is given by the oxide capacitance and the s-Si capacitance in series

$$C_{\text{oxeff}} = \left(\frac{1}{C_{\text{ox}}} + \frac{t_{\text{Si}}}{\epsilon_{\text{Si}}} \right)^{-1}. \quad (5.1)$$

The oxide capacitance and the effective capacitance values, in the accumulation and the “plateau” regions, respectively, extracted from the C_{gg} – V_{gb} curve (Fig. 5.1) are used to calculate the s-Si thickness

$$t_{\text{Si}} = \epsilon_{\text{Si}} \left(\frac{1}{C_{\text{oxeff}}} - \frac{1}{C_{\text{ox}}} \right). \quad (5.2)$$

Conventional C – V characterization techniques can also be used to extract the strained layer thickness and maximum depletion width. From the low-frequency C – V data, the depletion width (x_d) underneath the gate dielectric and the electrically active apparent carrier concentration (N_{net}) as a function of applied gate bias can be extracted by using the following equations [106], [107]

$$x_d = \epsilon_{\text{Si}} \left(\frac{1}{C_{\text{gg}}} - \frac{1}{C_{\text{ox}}} \right) \quad (5.3)$$

$$\frac{1}{N_{\text{net}}} = \frac{q\epsilon_{\text{Si}}}{2} \frac{d(1/C_{\text{gg}}^2)}{dV_{\text{gb}}}. \quad (5.4)$$

The net carrier concentration takes into account all the electrically active charges, both the fixed charges and mobile carriers are taken into account. Figure 5.2 shows a plot of the net electrical carrier concentration against the depletion width calculated from the

strained-Si/SiO₂ interface. This plot gives a clear understanding of the confinement of carriers at the different interfaces and the thickness of the top s-Si layer. The first peak appears at the s-Si/SiO₂ interface for both the electrons and holes, which explains the accumulation and inversion at the top interface. The second peak is explained by the accumulation of electrons at the s-Si/SiGe interface. The second peak corresponds to the thickness of the s-Si layer, which is extracted to be $t_{Si} = 5.1$ nm for the given data (Fig. 5.1). There is no peak at the second interface for holes and, hence, all inversion occurs only at the top s-Si/SiO₂ interface.

Figure 5.2: The net electrical carrier concentration as a function of depletion width extracted from Fig. 5.1 data. The two lines illustrate the confinement of carriers in the substrate [15].

The absolute value of the carrier concentration extracted along all regions of operation is plotted as a function of the gate voltage in Fig. 5.3. The carrier concentration is highest in the two extreme regions of operation due to the accumulation hole inversion layer and electron accumulation layer in the device. The small plateau near V_{FB2} (flat-band at the bottom interface) corresponds to the depletion region. The net concentration extracted there corresponds to the electrically active donor doping concentration in the n -type

substrate. The sharp transition after that corresponds to the sign change. The dips in the carrier concentration correspond to the flat-band and threshold-voltage conditions at the different interfaces. The model can be used to extract the conduction-band offset at the s-Si/SiGe interfaces as discussed below.

Figure 5.3: Variation of the electrical carrier concentration in a strained-silicon pMOS. The extracted values are: $N_{Si} = 5 \times 10^{18} \text{ cm}^{-3}$, $V_{FB1} = 1.1 \text{ V}$, $V_{FB2} = 0.5 \text{ V}$, $V_{tl} = 0.1 \text{ V}$ [15].

From basic physics, the following equations can be established. Potential balance:

$$V_{gb} = \phi_{MS} + V_{ox} + \phi_{s1}, \quad (5.5)$$

$$\phi_{s1} = \phi_{s2} + V_{Si}, \quad (5.6)$$

$$\phi_{s2} = \Delta E_C + \phi_{s3}, \quad (5.7)$$

where V_{ox} and V_{Si} are the voltage drops across the oxide and the s-Si layer. ϕ_{s1} , ϕ_{s2} , and ϕ_{s3} are labeled in Fig. 3.22.

Gauss' law:

$$V_{ox} = Q_g / C_{ox}. \quad (5.8)$$

Charge balance:

$$Q_g = -(Q_{ox} + Q_{sc}), \quad (5.9)$$

where Q_{sc} [sum of the bulk (Q_b) and inversion (Q_i) charges] is the induced space charge in the channel.

Depletion approximation:

$$Q_{sc} = Q_b + Q_i \approx Q_b = qN_{Si}(t_{Si} + x_d). \quad (5.10)$$

Poisson solution:

$$\phi_{s3} = -\frac{qN_{Si}x_d^2}{2\epsilon_{SiGe0}} \quad (5.11)$$

$$V_{Si} = -\frac{qN_{Si}x_d}{\epsilon_{SiGe0}}t_{Si} - \frac{qN_{Si}t_{Si}^2}{2\epsilon_{Si}}. \quad (5.12)$$

Flat-band is defined as the gate voltage at which the potential at the interface reaches zero (reference to the bulk). When the potential at the bottom interface (ϕ_{s2}) reaches zero, the boundary condition for $V_{gb} = V_{FB2}$ is given by

$$0 = \phi_{s2} = \Delta E_C + \phi_{s3} = \Delta E_C - \frac{qN_{Si}x_{d2}^2}{2\epsilon_{SiGe0}}. \quad (5.13)$$

When the potential at the top interface (ϕ_{s1}) reaches zero, the boundary condition for $V_{gb} = V_{FB1}$ is given by

$$\begin{aligned} 0 = \phi_{s1} &= \Delta E_C + \phi_{s3} + V_{Si} \\ &= \Delta E_C - \frac{qN_{Si}x_{d1}^2}{2\epsilon_{SiGe0}} - \left(\frac{qN_{Si}x_{d1}}{\epsilon_{SiGe0}}t_{Si} + \frac{qN_{Si}t_{Si}^2}{2\epsilon_{Si}} \right) \end{aligned} \quad (5.14)$$

where x_{d1} and x_{d2} are the widths of the depletion region in the relaxed SiGe substrate below the top s-Si layer, and the subscripts “1” and “2” correspond to the flat-band conditions at the top and bottom interfaces, respectively. As we do not know the exact mole fraction of germanium in the substrate, we have assumed that the SiGe permittivity

(ϵ_{SiGe0}) is equal to the permittivity of strained-silicon (ϵ_{Si}) in our model equations. This approximation turns out to have negligible effect on the result. Then, with $\epsilon_{SiGe0} = \epsilon_{Si}$, (5.13) and (5.14) give

$$x_{d2} = t_{Si} + x_{d1}. \quad (5.15)$$

Based on equations (5.5)–(5.12), the flat-band voltages at the two interfaces can be derived:

$$\begin{aligned} V_{FB1} &\equiv V_{gb} \Big|_{\phi_{s1}=0} = \phi_{MS1} + V_{ox} + \phi_{s1} \\ &= \phi_M - \left(\chi_{Si} + \frac{E_{g,Si}}{2} + \phi_F \right) - \frac{Q_{ox}}{C_{ox}} \\ &\quad - \frac{qN_{Si}(t_{Si} + x_{d1})}{C_{ox}}, \end{aligned} \quad (5.16)$$

$$\begin{aligned} V_{FB2} &\equiv V_{gb} \Big|_{\phi_{s2}=0} = \phi_{MS1} + V_{ox} + V_{Si} + \phi_{s2} \\ &= \phi_M - \left(\chi_{Si} + \frac{E_{g,Si}}{2} + \phi_F \right) - \frac{Q_{ox}}{C_{ox}} \\ &\quad - \frac{qN_{Si}(t_{Si} + x_{d2})}{C_{ox}} - \left(\frac{qN_{Si}x_{d2}}{\epsilon_{SiGe0}} t_{Si} + \frac{qN_{Si}t_{Si}^2}{2\epsilon_{Si}} \right). \end{aligned} \quad (5.17)$$

With (5.15), the shift in the flat-band voltage is given by

$$\begin{aligned} \Delta V_{FB} &\equiv V_{FB2} - V_{FB1} \\ &= -\frac{qN_{Si}t_{Si}}{C_{ox}} - \frac{qN_{Si}x_{d2}t_{Si}}{\epsilon_{SiGe0}} - \frac{qN_{Si}t_{Si}^2}{2\epsilon_{Si}}. \end{aligned} \quad (5.18)$$

The s-Si layer thickness has been extracted as shown in (5.2). The oxide capacitance is extracted from the capacitance-voltage characteristics. The substrate donor concentration has already been extracted physically in Fig. 5.3. The shift in the flat-band (ΔV_{FB}) can be extracted from Fig. 5.3. The depletion width x_{d2} is calculated from (5.18). The

conduction-band offset can then be calculated by substituting the depletion width x_{d2} into (5.13), which is $\Delta E_C = 0.23$ eV.

5.2 Verification of Extracted Physical Parameters

A Medici structure is built using the structural and material parameters extracted in the previous section. Figure 5.4 shows the structure of the extracted s-Si pMOS device. It consists of an s-Si layer on top of a relaxed SiGe substrate. The s-Si thickness, channel doping, and band offsets extracted are used in the simulation.

Figure 5.4: A strained-silicon pMOS structure extracted from the measured $C-V$ and simulated using Medici [15].

Figure 5.5 shows the pMOS band bending in the conduction and valence bands when the gate is biased at the flat-band and threshold voltages. Figure 5.6 shows the electron and hole concentrations at the top s-Si/SiO₂ and the bottom s-Si/SiGe interfaces. When the potential at the bottom interface reaches zero, electron accumulation occurs at the bottom s-Si/SiGe interface. When the potential at the top s-Si/SiO₂ interface reaches zero, accumulation occurs at the top interface. The electrons accumulated at the top s-Si/SiO₂ layer screen the bottom interface. The inversion of holes occurs only at the top surface.

The figure also clearly shows the flat-band and threshold-voltage conditions at which accumulation and inversion occurs at the interfaces.

Figure 5.5: The band bending in an s-Si pMOS at flat-band (V_{FB1} , V_{FB2}) and threshold-voltage (V_{t1}) conditions. Surface/interface potentials are indicated by ϕ_{s1} , ϕ_{s2} , ϕ_{s3} [15].

Figure 5.6: The simulated electron and hole concentrations at the s-Si/SiO₂ interface and the s-Si/SiGe interface [15].

To verify the accuracy of the extracted model parameters, the experimental curve in Fig. 5.1 is compared with the Medici simulations. The strained-silicon model based on the single-piece charge model is also compared with the measured and simulated curves. The

good matching as shown in Fig. 5.7 validated the proposed extraction methodology as well as the accuracy and the physics built into the compact model.

Figure 5.7: The measured, simulated (Medici), and modeled (Xsim) capacitance–voltage characteristics of a strained-silicon pMOS device [15].

5.3 Extraction of Model Parameters

After extracting the physical parameters as explained in Sections 5.1 and 5.2, the model parameters for the drain-current and charge models are extracted using a *one-iteration* extraction approach [108], [109]. The fitting parameter ζ is used in the surface channel strained silicon threshold voltage model. The parameter is extracted from the variation of threshold voltage with substrate bias from a bulk MOSFET and can be used for all the different germanium mole fractions.

The smoothing parameters $\sigma_{a1}, \sigma_{a2}, \sigma_f, \sigma_a$ are extracted from the flat-band condition. The smoothing parameters are fitted to satisfy charge neutrality at flat-band condition as well as continuity across regions of operation near flat-band and threshold points, including higher-order derivatives. The smoothing parameter δ is used to smooth the

interpolation of surface potential across depletion and the strong inversion range of biases. The *one-iteration* extraction approach is based on applying the unified regional model step by step, such that the parameters that have not been calibrated thus far have no effect in the current step of extraction, and once extracted, their values will not be affected by subsequent calibrations. After extracting the physical parameters, smoothing parameters are tuned in sequence one after the other. These smoothing parameters only affect the smoothness in the transitions regions in which they are defined. Each parameter associated with the modeled physical effect is calibrated at its extreme bias and/or geometry conditions where the effect is most pronounced. The model calibration can be carried out in one sequence based on weak parameter correlation. When a model parameter is found to have different values at different bias/geometry conditions, empirical functions are introduced to obtain the corresponding coefficients. Model accuracy can be further improved by an optional second iteration, with the extracted parameters as the initial values.

CHAPTER 6 RESULTS AND DISCUSSION

This chapter is devoted to the demonstration and verification of the AC and DC modeling of strained-silicon and double-gate MOSFETs. Models have been developed for the surface potential, threshold-voltage, charge, and capacitance of strained-Si MOSFETs. The potentials, charge and drain current have been modeled for double-gate MOSFETs. The models have been verified using MEDICI simulation data and some experimental data obtained from Institute of Microelectronics, Singapore. The model parameters and physical parameters have been extracted using the techniques discussed in Chapter 5.

6.1 Strained-silicon MOSFET Model Verification

Strained-silicon MOSFET models have been developed for the threshold-voltage, surface potential, charge, capacitance. The scalability of the model for various mole fraction, strained-layer thickness and terminal biases has been evaluated. The model was also validated using measured data from a strained-Si pMOS device.

6.1.1 Threshold-voltage model

The threshold-voltage model has been derived for both surface-channel and buried-channel s-Si MOSFETs. Figure 6.1 shows the prediction of the linear threshold-voltage for different Ge mole fractions in a surface-channel s-Si NMOSFET. As the mole fraction increases, the conduction-band offset increases, the channel inverts faster and, hence, the threshold voltage decreases. Figure 6.2 shows the prediction of the linear threshold voltage vs. substrate bias for different Ge mole fractions. The threshold-voltage model has been derived using bulk reference as discussed in Chapter 3. The fitting

parameter ξ introduced due to the Taylor approximation can be extracted from the bulk characteristics.

Figure 6.1: Prediction of the linear threshold voltage for different Ge mole fraction [10].

Figure 6.2: Prediction of the linear threshold voltage vs. substrate bias for different Ge mole fractions [10].

Figures 6.3 and 6.4 show the model prediction for a buried-channel s-Si nMOSFET for different substrate doping and SiGe cap-layer thickness. When the substrate doping of a buried-channel s-Si MOSFET increases, the top channel inverts first, as shown in Fig. 6.4 where $V_{t1} < V_{t2}$. Then the plateau in the inversion side disappears, and appears in the

accumulation side of a buried-channel s-Si nMOSFET. The major advantage of the URM approach is the physical scaling of the flat-band and threshold voltages with mole fraction, substrate doping, and cap-layer thickness variations. This accurate prediction of the V_t is the indication of accurate incorporation of the physics which explained the shifting of the plateau from the inversion side to the accumulation side.

Figure 6.3: Prediction of the surface and interface threshold voltages for different cap-layer thickness for a buried-channel s-Si nMOSFET [11].

Figure 6.4: Prediction of the surface and interface threshold voltages for different substrate doping for a buried-channel s-Si nMOSFET [11].

The long-channel threshold-voltage based models are extended to short channel by including the short-channel effects and the halo implants in the model following the same approach as in the bulk model [12]. Figure 6.5 shows the predicted linear threshold-voltage for different Ge mole fractions at different gate lengths. The short channel behavior is calibrated with only the control silicon-MOSFET data. The calibrated model can also be used to predict the V_t vs. L_g curve at different substrate and drain biases for different mole fractions. Figures 6.6(a) and 6.6(b) show the modeled V_t vs. $\log(L_g)$ curve at different drain and substrate biases for a Ge mole fraction of 20%. The strained-Si MOSFETs exhibit better threshold voltage roll-off characteristics with higher Ge mole fraction.

Figure 6.5: Prediction of the linear threshold voltage vs. gate length for different Ge mole fractions in a surface channel strained Si nMOSFET [11].

Figure 6.6: Prediction of the V_t vs. L_g curve for a Ge mole fraction of 20% for different substrate biases in a surface channel strained Si MOSFET at (a) $V_{ds} = 0.05$ V and (b) $V_{ds} = 1.2$ V [11].

6.1.2 Charge model verification

In this section, we show our modeled charges for a wide range of Ge mole fraction and s-Si layer thickness, validated by comparison with numerical (Medici) data. All physical parameters are the same as those used in Medici, and are shown in Table 6.1. The two fitting parameters σ_{a1} and σ_{a2} can be easily tuned by either using one set of $C-V$ data; or by the smoothest d^2Q_b/dV_g^2 at V_{FB1} and V_{FB2} without using any data. These parameters are then fixed for all device parameter and bias variations.

Figure 6.7: Modeled terminal charges compared with the Medici total gate charge (Q_g) and its first-/second-order derivatives (inset) [14].

TABLE 6.1
DEVICE PARAMETERS USED IN MEDICI AND MODEL

Symbol	Unit	Value	
		MEDICI	MODEL
t_{ox}	Nm	3	3
t_{Si}	Nm	12	12
N_{Si}	cm^3	2×10^{17}	2×10^{17}
N_{SiGe}	cm^3	2×10^{17}	2×10^{17}
ϕ_M	V	4.35	4.35
Q_{ox}	C/cm^2	0	0
L_g	μm	10	10
σ_{a1}	—	—	2.1
σ_{a2}	—	—	1.64

The four terminal charges are plotted in Fig. 6.7 and compared with the Medici Q_g data, including the first and second derivatives of Q_g (C_{gg} and C_{gg}') shown in the inset. The accuracy of the modeled gate charge and its first and second derivatives is self evident. Figure 6.8 illustrates accurate prediction of Ge mole fraction dependent “plateau”, including flat-band shift modeled by V_{FB1} and V_{FB2} in (3.34) and (3.55), the level of depletion modeled by ΔV_{FB} and γ_2 in (3.57) and (3.76), as well as the smooth transitions

near the two flat-band voltages and the threshold-voltage as evident by the well matched derivatives shown in the inset.

Figure 6.8: Predicted bulk-gate capacitances for various Ge mole fractions, compared with Medici data. The inset shows the derivatives of C_{bg} [14].

Figure 6.9 shows similar accurate predictions for C_{bg} and C_{bg}' (inset, on logarithmic scale) due to s-Si layer thickness variations, notably the level change in the “plateau” region as physically modeled by C_{oxeff} . Bulk-bias dependence of C_{gg} is shown in Fig. 6.10, with accurate matches with the numerically simulated data, including the “plateau” and the V_t shift.

Figure 6.9: Prediction of bulk-gate capacitances for two s-Si layer thicknesses, compared with Medici data, including accurate prediction in the derivatives on log scale (inset) [14].

Figure 6.10: Modeled gate capacitances for s-Si ($x = 0.3$) devices at various substrate biases [14].

The expressions for charge and surface potential of a buried-channel strained-silicon MOSFET were derived in Chapter 3. An implicit iterative technique based on the unified regional solutions was used to model the buried-channel s-Si MOSFET. The convergence of the surface potential, charge and capacitance from the initial guess to the final solution has been demonstrated in Chapter 3. The prediction of the surface and interface potentials for different substrate doping and cap-layer thicknesses has been demonstrated in Figs. 6.11 and 6.12.

Figure 6.11: Prediction of the surface and interface potential in a buried-channel nMOS for different substrate doping [11].

Figure 6.12: Prediction of the surface and internal potential in a buried-channel nMOS for different SiGe cap-layer thickness [11].

The capacitance–voltage curve of s-Si MOSFETs shows a “plateau” due to the confinement of carriers at the internal interface [11]. It is found that this plateau is dependent on substrate doping, and it switches from a plateau on the inversion side to that on the accumulation side as the substrate doping increases [13]. A buried-channel s-Si MOSFET has a SiGe cap layer on top of the s-Si channel. Generally, in a buried-channel nMOSFET, electrons invert at the bottom interface first and then at the top interface due to the conduction-band offset. As the substrate doping increases, the band bending in the top cap layer becomes greater than the conduction-band offset. Then, the top surface reaches a potential of $2\phi_F$ faster than at the bottom interface and, hence, inversion occurs first at the top interface. The electrons inverted at the top interface screen the bottom interface. This explains the gradual diminishing of plateau on the inversion as the doping increases. The flat-band voltage is defined as the gate voltage at which the potential (relative to that in the bulk) at the interface reaches zero. The flat-band voltages for the two interfaces have been derived physically by writing the one-dimensional Poisson

equation. In low-doping cases, the difference between the two flat-band voltages is negligible. So, the holes accumulate in the top SiO₂/SiGe interface, hence, no plateau is seen on the accumulation side. As the substrate doping increases, the difference between the flat-band voltages increases and, holes start accumulating at the bottom s-Si/SiGe interface first and then at the top SiO₂/SiGe interface. This explains the plateau in the accumulation region at high-doping conditions.

Figure 6.13: Prediction of the gate capacitance in a buried-channel nMOS ($x=0.3$) for a different substrate doping [11].

Figure 6.13 shows the accurate prediction of the model for different substrate doping. The plateau shifts from the inversion side to the accumulation side with increase in substrate doping. The shift in the plateau from the inversion to accumulation side has been modeled. The seamless shifting of the plateau in the modeled C-V curves exhibits the accuracy of the physics built into the model. The scalability of the model for different SiGe cap layer thickness and substrate bias is shown in Figs. 6.14 and 6.15.

Figure 6.14: Prediction of the gate capacitance in a buried-channel nMOS ($x=0.3$) for different SiGe cap layer thickness [11].

Figure 6.15: Prediction of the gate capacitance in a buried-channel nMOS ($x=0.3$) for a different substrate bias [11].

Figure 6.16 shows the measured gate capacitance of bulk silicon and an s-Si pMOS. The Si wafers used in this work consist of strained-Si on a uniform relaxed SiGe buffer layer with a Ge mole fraction of 0.25 grown on a thick graded SiGe buffer on a p-silicon substrate. PMOS capacitors were formed by implanting the substrate with a phosphorus dose of $2 \times 10^{13} \text{ cm}^{-2}$ at energy of 300 keV. The thermal oxide is grown at 800°C in a dry ambient. The capacitors were also built on bulk Si for reference. Capacitance-voltage characteristics were measured using HP-4284 LCR meter. The plot

also shows the comparison with TCAD data and playback of the model with the physical parameters extracted from the experimental data.

Figure 6.16: The measured, simulated (Medici), and modeled (Xsim) capacitance–voltage characteristics of a strained-silicon pMOS device [15].

6.2 Double-Gate MOSFET Model Verification

This section discusses the DG MOSFET models and their validation. Models have been developed for the surface potential, charge, and drain current of s-DG MOSFETs. A very generic model has been derived for the potential distribution for the a-DG MOSFET. We have discussed the importance of modeling of the DG MOSFETs with the doping in the channel in Chapter 4. This model is generic and scalable for different doping, oxide thickness and channel thickness. Hence, this unified model could be used to predict DG MOSFETs, SOI MOSFETs, Ultra-thin-body MOSFETs, and also bulk MOSFETs.

6.2.1 Symmetric double-gate MOSFET model verification

The potential and drain-current models for an s-DG MOSFET have been discussed in Chapter 4. The s-DG MOSFET model caters to different doping, and channel and oxide thicknesses. Figure 6.17 shows the schematic of a symmetric double-gate MOSFET.

Figure 6.17: Schematic of a symmetric double gate MOSFET

The potential at the surface and the mid-gap are solved analytically with approximations. Figure 6.18 shows the prediction of surface and mid-channel potentials for the s-DG model for different channel doping. The model converges to undoped structures when the substrate doping is reduced. The shift in the flat-band voltages, change in Fermi level and the potential due to the doping variation has been captured in the model. Figure 6.19 shows the surface and mid-channel potentials for different channel thicknesses and doping. Attention is drawn to the predicted switching point (fully-depleted voltage, V_{FD}), in particular, which is the key to doped-channel DG modeling.

Figure 6.18: Surface and mid-channel potential for doped s-DG for varying channel doping, showing that the curves shift towards the undoped cases the doping is decreased [40].

Figure 6.19: Surface and mid-channel potential for doped s-DG for different channel thickness and doping, showing transitions in depletion to weak/volume inversion and strong inversion [40].

Figure 6.20 shows the prediction of the surface potential and gate charge for different channel thickness. As the silicon thickness is increased more than the depletion width, the model converges to a partially depleted bulk-like device. The gate charge is calculated based on the left hand side of the voltage balance equation.

Figure 6.20: Surface potential and gate charge for doped s-DG/UTB at varying channel thickness, showing convergence to bulk device [40].

The drain-current model of an s-DG MOSFETs is based on the same formulation as is used in the development of bulk-MOSFET models. One of the advantages of the URM

approach is that it does not require a very high accuracy in modeling the surface potential for calculating the drain current. The error in the mid-channel potential due to the approximation has a negligible effect on the drain current. Further, the volume-inversion piece has been captured physically, as seen in Fig. 6.21(b).

Figure 6.21: Linear drain current ($V_d=0.05V$) for a s-DG MOSFET for different channel thickness. (a) linear scale, (b) log scale.

The prediction of the linear and saturation drain current is shown in Fig. 6.22. The figure shows the direct playback of the model for different drain biases using both linear as well as log scales.

Figure 6.22: Linear ($V_d=0.05\text{V}$) and saturation ($V_d=1.2\text{V}$) drain current for an s-DG MOSFET

(a) linear scale, (b) log scale.

6.2.2 Asymmetric double-gate MOSFET model verification

As a first step towards unification of the models, a unified model for the potentials has been developed. Some approximations have been used to derive unified regional analytical solutions for the a-DG MOSFET. Figure 6.23 shows the schematic of a asymmetric double-gate MOSFET.

Figure 6.23: Schematic of an asymmetric double-gate MOSFET

Figure 6.24 shows the prediction of the model for different substrate doping concentration. The back gate is biased at the flat-band voltage. The error in predicting the back gate potential is due to the Taylor series approximation in the derivation. For a given channel thickness, as the doping decreases, the bulk charge decreases and the accuracy of the model improves, as shown in Fig. 6.24. The model scales seamlessly to undoped a-DG MOSFET case with decrease in channel doping.

Figure 6.24: Prediction of the front and back gate potentials for a-DG MOSFET for different substrate doping.

Figures 6.25 and 6.26 shows the scaability of the model for different channel and back-gate oxide thicknesses for an undoped case. The undoped a-DG MOSFET can also be solved implicitly by Newton-Raphson (N-R) iteration. Figures 6.25 and Fig. 6.26 show the analytical model prediction compared to the implicit iterative solution.

Figure 6.25: Front/back-gate surface potential for undoped a-DG from (N-R) implicit and (regional) explicit solutions for varying channel thickness, compared with Medici data [40].

Figure 6.26: Front/back-gate surface potential for undoped a-DG from (N-R) implicit and (regional) explicit solutions for varying back-gate oxide thickness, compared with Medici data [40].

Figures 6.27 and 6.28 show the scalability of the model for different back gate oxide thickness and channel thickness in a doped channel case. As mentioned above the error in the predicting the back gate potential is due to the Taylor series approximation.

Figure 6.27: Front/back-gate surface potential for doped a-DG from explicit solutions for varying back-gate oxide thickness, compared with Medici data.

Figure 6.28: Front/back-gate surface potential for doped a-DG from explicit solutions for varying channel thickness, compared with Medici data.

Figure 6.29 shows the model prediction for a doped a-DG device with different back-gate bias. As the back-gate bias increases, there is more inversion charge than the bulk-charge and the accuracy of the back-interface surface potential improves. The a-DG MOSFET

model is derived with the generic boundary conditions and it converges to the symmetric structure when the two gates have the same physical parameters and are tied together.

Figure 6.29: Front/back-gate surface potential for doped a-DG from explicit solutions for varying back gate bias, compared with Medici data.

The generic model for a-DG front/back-gate potential has been evaluated for a lot of structure and bias variations. The model scales with doping, channel thickness, back-gate oxide thickness and the back-gate bias. Interestingly, as expected, the model converges to the solutions for s-DG, SOI, UTB, and bulk MOSFETs with corresponding structural inputs.

CHAPTER 7: CONCLUSION, ENHANCEMENT AND RECOMMENDATION

This chapter presents major conclusions for the models developed for strained-Si MOSFETs and double-gate MOSFETs. The recommendations for future work are also discussed in this chapter.

7.1 Conclusions and Model Enhancement

The unified regional modeling (URM) approach has been extended to non-classical CMOS structures. Models have been developed for the surface-channel and buried-channel strained-Si MOSFETs based on the analytical solution of 1-D Poisson's equation. The scalability of the model for different doping levels, strained-layer thickness and mole fractions has been evaluated. Short-channel effects were incorporated into the threshold-voltage model based on our bulk formulation.

An anomalous plateau is observed in the measured C-V characteristics of a surface-channel strained-Si pMOS device structure. The plateau shifts from the inversion side to the accumulation side with doping density. The physics behind the shift in the plateau has been incorporated into the model and validated with the numerical simulations using MEDICI simulator.

The analytical solution of 1-D Poisson's equation has been extended to yield a single-piece charge model for strained-Si MOSFETs. The flat-band voltages at which accumulation occurs at the surface and s-Si/SiGe-interface were derived physically and used in the URM approach to arrive at a single-piece charge model scalable for different Ge mole fractions and strained-layer thicknesses. An implicit iterative technique to

calculate the surface and interface potentials in strained-Si MOSFETs has been developed. The charge and capacitance are calculated based on the surface and interface potentials. The approach is generic to all hetero-structures and can be applied to other materials that exhibit accumulation of carriers at different interfaces for different gate biases due to different flat-band voltage corresponding to each interface.

The C-V characteristics of strained-Si MOSFETs are used to extract all the physical parameters like doping, band offset, strained-layer thickness using the conventional techniques and the developed model. The model parameters for the DC and AC operation of the devices are extracted using the same techniques as developed for the extraction of model parameters for bulk MOSFETs.

A study on the different mobility models has been carried out. A simple, empirical non-process specific holistic model catering to different kind of stressors reported by the BSIM group at Berkeley University is discussed in detail. Advanced MOSFETs are stressed by many intentional like SiGe substrate, SiGe source/drain, and unintentional stressors like STI, capping layer, silicides, LDD spacers etc. It is observed that the holistic model reported by the BSIM group empirically captures the change in mobility due to the multiple stressors.

The URM approach was also extended to double-gate MOSFETs. Most of the existing models reported in the recent literature do not include doping in the model formulation. The importance of including doping in the modeling has been brought out and discussed. A methodology for unification of different MOSFET models has been proposed. A 1-D Poisson equation solution generic to different structures like s-DG, a-DG, SOI, UTB and bulk MOSFETs has been derived.

The potentials at the surface and at the mid-channel of an s-DG MOSFET have been derived. The scalability of the model for different channel doping, channel thickness, and oxide thickness has been evaluated. The model converges to the bulk MOSFET model when the channel thickness is larger than the depletion width. A drain-current model for the s-DG MOSFET has been derived based on the solution of the potentials at the surface and mid-channel. The demand on accuracy of the surface potential is relaxed as the drain-current formulations are based on the URM approach. Surface potential based solutions calculate surface potentials at the source and drain ends. Charge and current are calculated using the differences in the source and drain potentials. URM does not use this approach and hence does not demand high level of accuracy in the surface potential. The Poisson's equation for a-DG MOSFET model with doping is not integrable twice to yield the surface potential solution. Approximations were thus used to simplify the input-voltage equation. The front/back-gate potentials were solved regionally in the depletion, weak inversion, and strong inversion regions. The models were unified with the help of a smoothing function to get single-piece top/back-gate potential. The error introduced into the model due to the Taylor approximation has been discussed for different cases. The model can converge to bulk, SOI, s-DG and UTB MOSFETs based on the structural input and the applied bias. The scalability of the model for different doping, channel thickness, oxide thickness, back-gate bias has been verified.

In summary, the thesis has extended the unified regional modeling approach to non-classical CMOS structures like strained-Si and double-gate MOSFETs. A methodology for the unification of different MOSFET models has also been proposed.

7.2 Recommendations for Future Research

Based on the findings of the research work in modeling methodology reported in this thesis, the following recommendations are suggested for future development:

- 1.) The strained-Si and double-gate MOSFET models are restricted to long- and wide-channel devices. Short-channel and narrow-width effects need to be physically derived based on quasi 2-D solutions and built into the compact model. The short-channel threshold voltage roll-off behavior can be built into the model by physically capturing the halo doping. Other short channel effects like DIBL, velocity saturation can also be built in based on the quasi 2-D solutions.
- 2.) The strained-Si and double-gate MOSFETs have been restricted to classical theory and first-order effects. Higher order effects like quantum-mechanical effects, poly depletion, self heating, fringing capacitances also need to be modeled and brought into the model. Poly-depletion effect can be captured by physical modeling of the potential in the poly-silicon. The correct estimation of the surface potential and poly-silicon potential will be the key to capturing poly depletion, poly-accumulation and poly-inversion effects. A quick approach to capture quantum mechanical effects would be to change the effective oxide thickness. A more physical approach would be to include the quantum mechanical correction in the surface potential. The latter approach captures both the threshold voltage correction and correction in the capacitance. The temperature dependence of the model is another interesting topic.
- 3.) The double-gate MOSFET model can be extended to other end-of-the-roadmap multiple-gate structures like FinFETs, pi-gate, and Ω -gate by including the corner

effects. The surrounding-gate MOSFET is also another emerging potential contender for end-of-the-roadmap space, which can be modeled by solving the Poisson equation in circular/cylindrical co-ordinates.

- 4.) A methodology for the unification of MOSFET models has been proposed in the thesis. The input voltage equation has been solved to get the front/back-gate potentials. A unified drain-current model needs to be developed based on the generic output current equation and the potential solutions. This would give a unified long-channel MOSFET model that can seamlessly cater to many devices like bulk, UTB, s-DG, a-DG and SOI.
- 5.) With the potentials being solved for SOI MOSFETs, the model can be extended to PD-SOI MOSFETs by including models for floating-body, substrate currents and other higher-order effects.

List of Publications

Journal

- [1] K. Chandrasekaran, X. Zhou, S. B. Chiah, W. Z. Shangguan, and G. H. See, "Physics-based Single-piece Charge Model for Strained-Si MOSFETs," *IEEE Trans. Electron Devices*, Vol. 52, No. 7, pp. 1555-1562, July 2005.
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Conference

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