Fabrication and characterization of silicon-on-insulator using low temperature wafer bonding

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School of Electrical & Electronic Engineering

Nanyang Technological University

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor of Philosophy

2005

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SUMMARY

Silicon-on-Insulator (SOI) technology presents one promising way of fabricating semiconductor devices on an insulating substrate rather than in a semiconductor bulk. Whereas SOI technology is becoming a mature technology for low-power CMOS circuits and represents the promising manufacturing technology for the next generation of ULSI low-power circuits, full SOI technology is not suitable for high power and high voltage device applications. A novel SOI structure that combines the advantages of SOI and JI (Junction Isolation) technologies, namely the partial SOI structure, is introduced.

Wafer bonding is selected as fabrication method for full SOI and partial SOI in this work. In order to allow the bonded wafer pair to withstand further wafer processes such as lapping, thinning and patterning, they have to be annealed at elevated temperature after the room temperature bonding to enhance the bond strength. However, the high temperature post-annealing used in the bonding process limits the applications of wafer bonding, especially in the bonding with processed wafers. Therefore, it is crucial to find a way to achieve strong bonding by low temperature annealing.

In present study, two low temperature wafer bonding methods, namely the medium vacuum wafer bonding (MVWB) and plasma activated wafer bonding (PAWB), are studied.

MVWB is performed successfully with improved bond strength and much higher bond speed as compared to the conventional air wafer bonding. Two main important parameters, namely annealing temperature (room temperature~500°C) and

annealing time (1~5 hours), are identified in the MVWB. Compared with the conventional wafer bonding, MVWB can improve the bonding quality dramatically, including higher bond strength (>20 Mpa, when annealed at temperature higher than 300°C for more than 4 hours), bond efficiency ($>90\%$, bond efficiency of almost 100% can be achieved if the bonding is performed in higher level clean room) and bond speed (5-hour is enough to achieve saturated bond strength). The effects of applied load during bonding, sequence of wafers contact and vacuum application, annealing temperature, annealing time, wafer orientation on the bonding quality were investigated experimentally and explained by the qualitative mechanisms of conventional wafer bonding and MVWB.

Mathematical model of MVWB is derived based on the mechanisms of water diffusion and reaction, which has crucial impact on bond strength. The results predicted by this model agree well with the experiments results. This model can be applied to predict the effects of annealing time, annealing temperature, ambient vacuum level, wafer orientation and wafer dimension on the bond strength.

To achieve high bond strength at low temperature, an effective approach is to activate the wafers by plasma prior to wafer bonding, namely plasma activated wafer bonding (PAWB). Ex-situ PAWB is performed and the results are compared with the conventional wafer bonding. It is found that ex-situ PAWB induces more bubbles, but higher bond strength (e.g. >15 MPa after 4 hours annealing at 400°C).

The mechanism of PAWB based on the conventional wafer bonding mechanism is proposed. It includes four different aspects: cleaning, roughening, enhancement of diffusivity of water, and viscous flow at low temperature.

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Chapter 1 INTRODUCTION

1.1 Motivation

SOI technology presents one way of fabricating semiconductor devices on an insulating substrate rather than in a semiconductor bulk. It has many advantages over bulk silicon substrate [1,2]. When the SOI technology is applied in the fabrication of the power devices and power integrated circuits (PICs), however, there are many shortcomings arising, such as reduced breakdown level and self-heating effect [3,4]. To overcome this problem, one novel SOI structure, namely partial SOI, was proposed [3,4]. Although this structure is much better than conventional SOI, especially in the application of power devices and PICs, its fabrication remains a key issue. There are many methods which could be used to fabricate this structure, such as SIMOX [5], Zone Melting Recrystallization (ZMR) [6], wafer bonding [7], and selective silicon and oxide etching, followed by selective epitaxial growth [8]. However, SIMOX has the inherent shortcomings, such as the low quality of the active film and a demand for the high temperature annealing. Large thermal stresses and film non-uniformity occur with the ZMR technique. A large thermal stress is also one serious issue in wafer bonding if the conventional wafer bonding is used that need high temperature annealing. Selective etching and epitaxial growth is very

complicated and not suitable for the mass production. Hence, in this work, low temperature wafer bonding is proposed to fabricate this novel structure for the first time because of the better quality of the resulting silicon film and its cost effectiveness [9].

Wafer bonding is increasingly becoming a key technology for materials integration in various areas of micro-electro-mechanical systems (MEMS), micro-opto-electro-mechanical systems (MOEMS), microelectronics, optoelectronics, semiconductor-on-insulator (SOI) and displays. It is also widely used for vacuum packaging, hermetic sealing and encapsulation [9,10].

There are numerous indirect bonding methods. The most straightforward way is to use additive intermediate layer, a joining “adhesive” or “glue”, which can bond two wafers together at low temperature [9]. But there are several disadvantages of having intermediate layer. The most obvious is the fact that upon completion of bonding, the structure is not a “single” structure but rather two structures being held together. Also, this intermediate material usually has a thermal expansion coefficient different from that of the substrates, thereby inducing stress upon thermal cycling. In addition, using intermediary joining materials prevents a direct contact between the two substrates from occurring. Direct material-material contact is necessary for many electrical and optical devices. For the partial SOI structure, partially Si-Si contact is necessary. Therefore, indirect wafer bonding using intermediate layer is not appropriate fabrication method in this work.

Several direct bonding methods are available. One common method is anodic bonding, which can achieve high bond strength at low temperature [11]. However, anodic bonding requires ionic conductivity materials and high electric field. The most

serious problem which cannot be tolerated in our project is that the sodium ions of glass that can degrade the performance of electronic devices.

To avoid the instability of intermediate layer and the existing of undesired components, such as mobile alkali ions, conventional direct wafer bonding were proposed. However, conventional bonding techniques require high temperature annealing for high bonding quality. Such high bonding temperature results in some problems such as thermally induced mechanical stress at bonded interface due to the difference of thermal expansion coefficients between the substrates [12], and damage of metal electrodes on the substrates after the bonding [13], as well as the prevention of temperature sensitive components inclusion in the bonded wafers [14]. Therefore, it is crucial to achieve strong bonding by low temperature annealing (usually below 420 °C, the melting point of aluminum electrode). Among them, there are two promising ways that have shown some success. One way is the direct wafer bonding in vacuum, such as bonding in ultrahigh vacuum (UHV) [15], low vacuum [16] and high vacuum after Ar beam surface activation [17]. The other way is to treat the wafer surface with plasma prior to conventional direct wafer bonding (Plasma Activated Wafer Bonding, PAWB) [18,19,20]. Experiments have shown a significant increase in the bond strength in both of these two methods.

Very little research has been done for vacuum wafer bonding [15-17]. In fact, only UHV and low vacuum level bonding have been studied by other researchers. However, UHV wafer bonding requires expensive apparatus and costly process, which is not appropriate for mass-production. It also usually requires preheating (~600°C) of the wafers prior to bonding, or application of pressure during bonding in addition to UHV condition [11]. On the contrary, the cost-effective vacuum wafer bonding, low vacuum wafer bonding, cannot achieve very good bonding quality on

the bond strength and efficiency [16]. Therefore, we would like to explore the middle member of their family, medium vacuum wafer bonding (MVWB). So far, there is no research result published on it and its mechanism is not understood indeed. As a result, further investigation should be done to understand the wafer bonding by medium vacuum processing.

In contrast, a lot of works have been done on PAWB. However, to the best of our knowledge, its mechanism has not yet been very clear either [20]. Therefore, PAWB was performed in this work and its qualitative mechanism was proposed.

Having these in mind, we conducted the present research work on MVWB and PAWB with an aim to study the effects of process parameters and explore the bonding mechanisms.

1.2 Objectives

The main objectives of this work are as follows:

- 1) Design and perform PAWB and MVWB.
- 2) Study the effects of various process parameters on the bonding quality of the PAWB and MVWB.
- 3) Explore the mechanisms of PAWB and MVWB.
- 4) Identify method to fabricate SOI by low temperature wafer bonding.

1.3 Contribution of the Thesis

The major contribution of the thesis covers four aspects:

- 1) Low temperature MVWB is performed successfully, and the bond strength is improved dramatically as compared to the conventional air wafer bonding. Two important parameters, namely annealing temperature and annealing time are identified in MVWB.
- 2) Mathematical model is developed for MVWB, and the model agrees well with the experiment results.
- 3) Oxygen is proven to be not suitable for partial SOI fabrication by simulation. Ar PAWB is performed and compared with conventional air wafer bonding and vacuum wafer bonding. A new qualitative mechanism of PAWB is proposed and verified by experiment results.
- 4) New method, combining SIMOX and wafer bonding to fabricate partial SOI is proposed.

1.4 Organization of the Thesis

The thesis is organized in six chapters.

Chapter one is the introduction of the thesis, including motivation, objectives, contribution and organization. The literature reviews of SOI technology and wafer bonding are presented in chapter two. Chapter three presents the experimental procedure of conventional wafer bonding, MVWB and PAWB. The instruments and characterization methods used in present work are also introduced in this chapter. Chapter four is devoted to the work in MVWB, including introduction, experiment results and mechanism of it. Similar work for PAWB is discussed in chapter 5. Finally, chapter 6 summarizes the results in this work and gives recommendation for future work.

Chapter 2 LITERATURE REVIEW

2.1 SOI Technology

2.1.1 Why SOI Technology

Silicon technology is now faced with gigahertz frequency and ultra-large-scale integration (ULSI) era instead of broad implementations of general-purpose processor, DRAM etc, with 10 million or more devices [21] per integrated circuit (IC) chip. In order to meet such demand, technology feature size has been scaled down to deep sub-micrometer regime nowadays, while the memory [e.g., dynamic access memory (DRAM)] has increased from a few thousand bits to current 128 million bits per chip, the clock frequency of the central processing unit (CPU or microprocessor) has increased from less than 1 MHz to current 4GHz for low-end computer application.

However, with the miniaturization of the devices, a number of drawbacks emerge in the standard bulk silicon technology, such as short-narrow channel effects, high-field effects, parasitic transistor and thyristor effects, and the increase of sub-threshold currents induced by the reduction of the device feature length, which renders the conventional silicon technology a limit and preventing the speed performance and functionality of integrated circuit from further enhancing [1,2].

To keep abreast with the tremendous development of computer and consumer-related, as well as the recently emerging personal communication (radio frequency (RF) IC technologies) and/or Internet-related products, it is necessary to continue to increase the speed performance and device density. A new semiconductor structure, SOI technology, is introduced to overcome these problems found in bulk silicon technology.

SOI stands for silicon on insulator, which presents one way of fabricating semiconductor devices on an insulating substrate rather than in a semiconductor bulk. It has become a major technology for the next generation ULSI because of the following advantages of SOI over the conventional bulk silicon substrates [1,2]:

1) Immunity to Radiation [22]

Owing to the excellent isolation provided by the buried oxide, the immunity of the SOI devices against high-energy particle illumination is excellent. Therefore, SOI CMOS devices are more suitable for operation in the environment with high-energy radiation than the conventional bulk CMOS devices. In fact, this is the reason for the early applications of the SOI technology in space or military oriented proposes.

2) Reduction in Parasitic Capacitance [23]

In addition to the radiation immunity property, the parasitic capacitances of SOI CMOS devices are also smaller than those of bulk counterparts due to the buried oxide layer (BOX). Moreover, parasitic capacitances between sources or drains regions and channel stoppers are indeed nonexistent in this technology.

3) Reduction in Power Delay Product [24]

The power-delay product of the SOI inverter circuit is much smaller as compared to that of the bulk, owing to the smaller parasitic capacitances in the SOI MOS devices;

4) High packing density and simplicity in manufacturing process [1,2]

Buried oxide is used for isolation in SOI CMOS devices. Therefore, the higher packing density and simpler fabrication process of SOI devices than bulk CMOS devices can be achieved since depletion regions of the reverse-biased p-n junction for isolation are no longer required. Also, because n-channel and p-channel SOI devices are totally isolated from each other and from the substrate, no latch-up exists.

5) Eliminating metal spike [1,2]

One of the most challenging tasks in VLSI technologies is metallization of shallow source and drain junctions. Barrier metals are applied in bulk silicon technologies to prevent metal spikes through shallow junctions. In SOI technology source and drain junctions are extended down to silicon dioxide, eliminating the danger of metal spikes.

Owing to the advantages of SOI technology over the conventional bulk silicon technology, SOI CMOS technology has been gradually recognized as a major VLSI technology. In addition to VLSI applications, SOI technology has also been used to realize communication circuits, microwave devices, BiCMOS devices, and even fiber optics applications for its superior performance. In addition, with the growing trends of the portable systems, low-voltage and low-power designs have been indispensable. In this aspect, SOI technology is suitable for integration of the low-voltage and low-

power VLSI circuits, because of the steeper subthreshold slope feature of SOI CMOS devices.

Generally speaking, manufacturing cost of the SOI wafer is more expensive than that of the bulk one, which is a bottleneck for development at present. However, the expensive wafer cost can be offset by fewer steps and fewer masks required in the SOI CMOS technology. Also, for SOI technology, higher integration density and smaller required die area and a better performance can be achieved. With the continuously growing demands on low-voltage, low-power and high-performance VLSI wafers, the profitability of SOI CMOS is promising.

2.1.2 Evolution of SOI Technology

Table 2.1 Evolution of the mainstream SOI technology [2]

Year	First Author	Technique
1978	Maurits [22]	SOS (silicon-on-sapphire)
1983	Lam [23]	SIMOX (separation by implanted oxygen) SOI ZMR (zone-melting-and-recrystallization) SOI
1986	Partridge [24]	SOS, SIMOX, ZMR SOI
1989	Colinge [25]	SIMOX, ZMR SOI, BESOI (bond-and-etch-back SOI)
1990	Auberton-Herve [26]	SIMOX, ZMR SOI, BESOI
1991	Vogt [27]	SIMOX, BESOI, ZMR SOI
1991	Colinge [28]	SIMOX, BESOI
1993	Feijoo [29]	SIMOX, BESOI
1993	Kawamura [30]	SIMOX, BESOI
1996	Auberton-Herve [31]	SIMOX, BESOI, Smart-cut SOI

Table 2.2 Comparison of some physical and electrical properties of the different SOI materials and application area [1]

Materials	Defect density	Thin Si thickness control	Minor. Carrier lifetime	Channel mobility	Application
ZMR	+	-	+	+	Rad.hard CMOS
ELO	-	- -	-	-	

Table 2.2 (continued) Comparison of some physical and electrical properties of the different SOI materials and application area [1]

LSPE	--	+	--	--	
FIPOS	++	+	++	+	
SIMOX	+	+	0/+	+	Deep sub-micron CMOS, rad.hard CMOS, BiCMOS
BESOI	++	--	++	+	Rad.hard CMOS, bipolar & power device

Note: Bulk silicon properties are indicated as a scale reference. ++=very good, +=good, 0=average, - = poor, --=very poor

Table2.1 shows the evolution of the mainstream SOI technologies. As can be seen in Table2.1, the CMOS industry began to be interested in the SOI technology in the late 1970s. A number of fabrication methods have been developed since then. There are many non-mainstream technologies used for SOI fabrication such as ELO (Epitaxial Lateral Overgrowth) [32], LSPE (Lateral Solid-Phase epitaxy) [33], FIPOS (Full Isolation by Porous Oxidized Silicon) [34] and ZMR (Zone-Melting Recrystallization) [35] etc. Listed in Table2.2 are advantages and disadvantages of some SOI technologies and their application.

Creating defect-free films of single-crystal silicon on an insulating layer is a technological challenge. Several techniques have been developed, but only a few are successfully used in the mass-production. According to Tables 2.1 & 2.2, SIMOX (Separation by Implanted OXygen) and BESOI (Bonded-and-Etch Silicon-On-Insulator) have become the mainstream SOI technologies. SIMOX technology has a good property of thin silicon thickness control, which makes SIMOX suitable for ultra-thin SOI devices [1,2]. In contrast, SOI wafers fabricated by BESOI technology offer the advantages of having a superior quality of the device layer and a thermally

grown buried oxide [1,2]. Therefore SIMOX and BESOI have their own strengths respectively. Recently, Smart-Cut SOI has emerged, which significantly reduced the cost and improved the efficiency of the thinning process [36].

2.1.3 SOI Grown by SIMOX

The first SiO₂ layer synthesized by ion implantation of oxygen into silicon was reported in 1963 [37], and in 1977 [38], the first buried oxide layer was produced by the same technique. Intensive work on SIMOX technology began in early 1980s. The principle of SIMOX material formation is very simple (shown in Fig2.1), consists of the formation of a buried layer of SiO₂ by implantation of oxygen ions beneath the surface of a silicon wafer. There are two main processes in SIMOX--Oxygen Implantation and Annealing. The shape and quality of SIMOX layers obtained by oxygen implantation depend on both the oxygen dose and the temperature of the wafer during the implantation process. As shown in Fig. 2.1, after the oxygen ion implantation is performed, a high temperature annealing step is necessary to form a device-worthy SIMOX structure. In general, the higher the annealing temperature is used, the better the quality of the material will be.

Figure 2.1 The principle of SIMOX: a heavy-dose oxygen implantation into silicon followed by an annealing step produces a buried layer of silicon dioxide below a thin, single-crystal silicon overlayer [39].

2.1.4 Partial SOI and Its Fabrication Methods

Whereas SOI technology is becoming a mature technology for low-power CMOS circuits and justifiably represents the main manufacturing technology for the next generation of ULSI low-power circuits since 1999, when IBM launched the first fully-functional SOI mainstream microprocessor [40], it is still an emerging technology for high-voltage power integrated circuits. An increased effect is now directed towards developing advanced SOI power device structures for integrated circuits. Compared to bulk junction-insulated (JI) devices, SOI devices and circuits offer improved isolation, reduced leakage currents and faster switching speed. However, power devices and PICs using SOI technology may suffer from reduced breakdown levels and self-heating effects [3,4].

A novel SOI structure which combines the advantages of SOI and JI technologies has been proposed by Cambridge University as shown in Fig. 2.2. As compared to conventional SOI structure, the new device structure has an interrupted oxide at one electrode of the devices, which is named partial SOI. The new partial SOI realizes an improved Resurf effect since the substrate plays an active role to reduce the electric field at the surface in the partial SOI structure. This is in contrast to the conventional SOI power devices, where the potential lines are crowded in the top SOI layer. From the numerical simulations of JI, SOI and partial SOI structure, it is worthwhile to note that the breakdown voltage of the partial SOI is even higher than that of JI [3]. This can be explained by the fact that the oxide layer near the silicon window can support part of the voltage. Compared to the conventional SOI power device technology, thin oxide layers can be used in the partial SOI structure, and the self-heating effect in partial SOI is drastically reduced as heat can now be dissipated through the substrate. Furthermore, since in both SOI and partial SOI structures the

current and the plasma injection are confined to the SOI layer, the switching speed of these structures is considerably superior to that of equivalent JI structure [3,4].

Figure 2.2 Schematic drawing of the partial SOI structure

This partial SOI structure can be fabricated by selective SIMOX [5], ZMR [6], or selective silicon and oxide etching, followed by selective epitaxial growth [8]. Local oxidation followed by wafer bonding is another possibility [7]. However, the first technique has the inherent shortcomings of conventional SIMOX, such as the low quality of the active film and a demand for the high temperature annealing. Large thermal stresses and film non-uniformity occur with the second recrystallisation technique. The third method is very complicated and not suitable for the mass production. A large thermal stress is also one serious issue in wafer bonding if one uses the conventional method that needs high temperature annealing. In this work, low temperature wafer bonding is selected as fabrication method for partial SOI.

2.2 Wafer Bonding Technology

2.2.1 Introduction

Wafer bonding generally refers to a process by which two wafers fuse and adhere to each other if they are put into close contact. From the first systematic investigation of room temperature adhesion between two optically polished glass plates performed in 1936 by Rayleigh [41], wafer bonding technique has been studied for several decades. Widespread interest in modern wafer bonding techniques was

generated by the report on silicon-silicon wafer bonding for silicon-on-insulator structure by two groups [42, 43] in 1986 in which the initial bonding of the two wafers at room temperature was followed by a high-temperature bond-strengthening heat treatment.

Although wafer bonding is by no means a new technique, recently it is gaining popular interest for a number of applications, such as high performance microelectronics (e.g. high performance partially depleted and fully depleted CMOS [44], double gate CMOS [45, 46], and 3D device integration [47]), photonics and optoelectronics [48], and microelectromechanical systems (MEMS) [49, 50]. Additionally, the capability of layering dissimilar materials makes it possible to integrate devices on a single chip.

Various technologies have been developed in the scope of wafer bonding, which can be divided into three categories:

1) Direct bonding (fusion bonding).

In direct bonding, two wafers are contacted without the assistance of any significant pressure, electrical fields or intermediate layers [9]. This bonding technique usually leads to strong bonds and is widely used in the SOI technology.

2) Anodic bonding. It is based on the joining of an electrical conducting material (e.g. silicon) and a material with ionic conductivity (e.g. alkali-containing glass) [51, 52]. Anodic bonding usually leads to strong and hermetic bonds and is widely used for micro-sensor fabrication and hermetic sealing of micromachined devices.

3) Intermediate layer bonding.

Several low temperature bonding methods using intermediate layers including metal, glass or organic compounds of variable thickness have been reported in recent

years [53, 54, 55]. Since it is usually less demanding on surface topography and cleanroom environment, intermediate layer bonding has been used in some special fields, such as optically pumped VCSELs [56] and chemical analysis devices [57].

As mentioned above, direct wafer bonding is selected in this project to fabricate the full and partial SOI structure for its advantages over SIMOX on the possibility of thick buried oxide, thicker and better silicon quality (work layer). Thus, direct wafer bonding technology will be discussed in details in the next section.

2.2.2 Direct Wafer bonding process

As direct wafer bonding is chosen in this work, the term wafer bonding used throughout the thesis will refer to direct wafer bonding unless otherwise stated.

A silicon wafer bonding fabrication process flow is illustrated in Fig. 2.3. It is generally accomplished by four basic steps. The first step is the preparation of the surface for bonding. Then, two as-bonded wafers are mated at the room temperature with or without any applied force, and the bonded area spreads laterally over the entire wafer area, typically in a few seconds. The bonding achieved at room temperature is usually relatively weak as compared to the metallicity, covalently, or ionically bonded solids. Therefore, for most of the applications, the room temperature bonded wafers have to undergo a heat treatment to strengthen the bonds across the interface. Frequently, one of the wafers is then thinned to a thickness that depends on the specific application and may be in the range of many microns down to a couple of nanometers. More details of the silicon wafer bonding process will be presented in the sequent sections.

Figure 2.3 Schematic wafer bonding process flow

There are two kinds of wafer bonding, namely the hydrophilic and hydrophobic wafer bonding. Their mechanisms are distinct [9]. Since the bonding quality of hydrophobic wafer bonding is lower than that of hydrophilic wafer bonding at low temperature [9], only hydrophilic wafer bonding will be discussed in this work.

2.2.2.1 Surface Preparation

It is well known that the forces involved in wafer bonding are mainly short-range intermolecular forces, such as Van der Waals forces, electrostatic Coulombic forces, capillary forces and so on [9]. Therefore, adequate surface smoothness, flatness, cleanliness, and surface activity of the mating wafers are essential for successful bonding at room temperature.

2.2.2.1.1 Polishing of Wafer Surface

Physical quality of the as-bonded wafers is one of the key issues that determine the quality of wafer bonding. Two parameters commonly used to describe the physical quality quantitatively are the *surface flatness* and *microroughness*. Surface flatness is a global, macroscopic measure of the deviation of the front surface of a wafer from a specified reference plane when the back of the surface of the wafer is ideally flat, as when the wafer is pulled down by vacuum onto an ideally clean, flat chuck. As shown in Fig. 2.4, the total thickness variation (TTV) is commonly used to specify the surface flatness, which is the difference between the highest and the lowest elevation of the top surface of the wafer.

Figure 2.4 Schematic for the definition of total thickness variation (TTV) [9].

During silicon wafer bonding at room temperature, each wafer of the pair will be elastically deformed to achieve conformity of the two surfaces. Thus the flatness nonuniformity of starting wafers can result in periodic strain patterns (contrast fluctuations) corresponding to typical spatial frequencies of the bonded pair. However, if the flatness nonuniformity is too large, unbonded areas may result.

In practice, it is found that the flatness variation of 1-3 μm over commercial 4" silicon wafers poses no obstacle for wafer bonding at room temperature because the deformation of the two wafers can easily accommodate this scale of surface waviness. Bow and warpage of wafers up to about 25 μm are also tolerable.

Micro-roughness is a local, microscopic parameter of wafer surface quality that is crucial in wafer bonding. Microroughness is usually characterized by a value such as RMS (root mean square), abbreviated as R_q , as measured by STM (scanning tunneling microscopy) and AFM (atomic force microscopy).

It has been demonstrated experimentally that R_q less than 5 Å is adequate for silicon wafer bonding at room temperature via hydrogen bonds [58]. Fortunately, this average roughness value is typical for commercially available prime grade bulk silicon wafers and silicon wafers with surface average roughness of less than 1 Å are also achievable.

In practice, both pure mechanical polishing and chemical-mechanical-polishing (CMP) can achieve a high degree of flatness, parallelism and smoothness of Si and silica glass pieces. But pure mechanical polishing does introduce a significant subsurface damage layer of ~20 µm in depth. Therefore, CMP is preferred in wafer bonding for the wafer surface polishing [9].

The effect of surface microroughness on the bondability is studied on the basis of the theory of contact and adhesion of elastic solids [59,60]. An effective bonding energy, the maximum of which is the specific surface energy of adhesion, is proposed to describe the real binding energy of the bonding interface, considering the influence of the wafer surface microroughness. Both the effective bonding energy and the real area of contact between rough surfaces depend on a dimensionless surface adhesion parameter, θ , as depicted in equations (2.1) and (2.2.)

$$w_b^* = \frac{w_b}{w} = R\sigma\eta_s \int_{s_b}^{\infty} \left[\frac{4\theta}{3\sqrt{2\pi}} \int_s^{\infty} (x-s^*)^{3/2} \exp\left(-\frac{x^2}{2}\right) dx - \sqrt{2\pi} \int_s^{\infty} \exp\left(-\frac{x^2}{2}\right) dx \right] ds^* \quad (2.1)$$

$$\theta = \frac{E^*}{w} \sqrt{\frac{\sigma^3}{R}} \quad (2.2)$$

where

w_b^* is the normalized specific effective bonding energy, w_b is the specific effective bonding energy, w is the specific surface energy of adhesion, $E^* = 4/3[E/(1-\nu^2)]$, ν is the Poisson's ratio and E is the Young's modulus. R is the radius of the elastic sphere, σ is the Gaussian height distribution of standard deviation, $\eta_s (=N/A_0$, N the asperities number and A_0 the asperities' normal area), the quantities R , σ and η_s are not independent but related, such that $R \cdot \sigma \cdot \eta_s = \text{constant}$. The value of this constant is between 0.05 and 0.1. s_b^* is the separation between two wafers, s^* ($=s/\sigma$, s mean asperity height of the wafer with rough surface). The normalized specific effective bonding energy, as a function of the adhesion parameter, is graphically shown in Fig. 2.5 [59].

Figure 2.5 Normalized specific effective bonding energy (solid line) and the normalized real area of contact (dashed line) as functions of the surface adhesion parameter. The contacted surfaces are a rough surface with Gaussian height distribution and a flat plane. Using the adhesion parameter as a measure, three regimes can be identified: I, the bonding regime for $\theta < 1$; II, the adherence regime for $1 < \theta < 12$; and III, the nonbonding regime for $\theta > 12$ [59].

2.2.2.1.2 Surface cleaning

Wafer bonding requires wafers with clean surfaces that are free of particulate, organic, and metallic contamination. This is important because the surface cleanliness has a direct effect on both the structural and electrical properties of the bonding interfaces as well as on the resulting electrical properties of the bonded materials.

The cleaning techniques employed prior to room temperature wafer bonding must be able to remove all contamination on the surfaces without degrading surface smoothness. These requirements are fully compatible with VLSI technology. The wet-chemistry wafer cleaning commonly used in the semiconductor industry is fully applicable to wafer bonding. Hydrogen-peroxide-based “RCA” wet cleans are most commonly used in the semiconductor industry and also in wafer bonding [61].

2.2.2.1.3 Surface Activation

It is obvious that Van der Waals dispersion force is ubiquitous and is applicable to almost all substances that are in intimate contact (so-called optical contact). Therefore, in practice, two solid-state plates of almost any material can bond to each other at room temperature provided that their surfaces are sufficiently flat and clean to allow the surface molecules of two plates to get close enough (sometimes only after some local elastic or plastic deformation of the solid) and van der Waals forces between the atoms on the touching surfaces are sufficiently strong. In practice, it is very costly to produce an optically smooth and flat surface, and hardly possible at all for some materials. Therefore, it would be highly desirable to create a reactive bonding surface to alleviate the surface smoothness requirement.

The activation methods will be discussed in the section of “low temperature wafer bonding” in details.

2.2.2.2 Annealing

To enhance the bonding adhesion, the water molecules at the bonded interface must be removed by dissolving into the surrounding materials or diffusing out of the interface in order to promote the condensation reaction between the OH groups as follows:

Such a reaction starts immediately at room temperature when they are in sufficient proximity [62]. However, the above reaction is reversible at temperature below 425 °C and most of the covalent Si-O-Si bonds cannot remain at the bonding interface with the existence of water at low temperature. Even at temperature higher than 425 °C, there are still some water molecules and OH groups at the bonding interface. For the bonding energy to achieve the bulk fracture energy, an annealing, typically at higher than 800 °C for hydrophilic Si/Si bonding, is necessary to remove the remaining water molecules and to fill up the interface microgaps by means of viscous flow of the native oxide [63]. The details of annealing are in the section of “conventional wafer bonding mechanism”.

2.2.2.3 Thinning

After annealing, the device wafer of the bonded pair usually needs to be thinned over the entire wafer. Device layer thickness and its uniformity requirements

vary with applications. Desired SOI layer thickness is usually obtained by grinding and polishing one side of the bonded pair.

At present, SOI thickness uniformity of $\pm 0.5 \sim \pm 0.3 \mu\text{m}$ in a 6" diameter wafer is available [10] by several methods in grinding and polishing, such as electrolytic in-process dressing (ELID) grinding method [64], and plasma assisted chemical etching (PACE) [65]. The uniformity can be much improved by CMP. After grinding and the removal of subsurface damage by chemical etching, CMP can be used to achieve a smooth surface and a desired thickness [66].

Etch stop methods is another effective thinning methods which utilize etching selectivity dependent on dopant concentration. Boron is typically used as a dopant [67]. However, during high temperature bonding annealing, boron can diffuse and the SOI layer will be smeared. Thus, the bonding annealing temperature is restricted. As a result, insufficient bond strength is a drawback in etch-stop bonded SOI wafers.

Smart Cut[®] process has emerged as a cost-effective thinning way for wafer bonding, making the direct wafer bonding technology feasible in VLSI and MEMS application [36]. As shown in Fig. 2.6, the device wafer is grown with a thick thermal oxide layer to be used as the buried oxide in the final SOI structure [2]. A hydrogen ion (H^+) implantation at a dose of $2 \times 10^{16} \sim 1 \times 10^{17} \text{ cm}^{-2}$ is carried out. After cleaning, the device wafer and the handle wafer are bonded together at a temperature slightly higher than the room temperature. Then the wafers are heated at 400-600°C. The implanted hydrogen atoms at a depth under the oxide layer gather to form blistering. If the amount of the implanted hydrogen atoms is sufficient, the blistering will cause flaking of the whole silicon layer. As a result, a thin-film silicon layer with a thickness identical to the depth of the hydrogen implant is left at the top of the buried

oxide. Then, a 1000 °C heating cycle strengthens the bonding of the two wafers. Because of blistering, the microroughness of the wafer surface may not be acceptable. Application of CMP to smooth the surface finalizes the smart-cut SOI procedure. No epitaxy is required for the smart-cut technology and the production throughput is high. Since the hydrogen profile after the H^+ implant is sharp, the thickness variation of the produced thin-film is small. Therefore, production cost and quality of the smart-cut technology is good.

Figure 2.6 Principle of smart-cut SOI process [2]

2.2.3 Conventional Wafer Bonding Mechanism

For hydrophilic wafer bonding, the wafers are covered with water molecules. The bonding at room temperature is caused by hydrogen bonds between the chemisorbed water molecules located on the opposing wafer surfaces. To break the hydrogen bonds between two wafer surfaces in order to allow silanol groups to react with each other and subsequently form stronger Si-O-Si bonds, high temperature annealing is always needed to enhance the diffusion of absorbed and produced water [68] as seen in Fig. 2.7. A detailed bonding model of conventional silicon described by Q. Y. Tong et al. [9] is widely accepted.

Figure 2.7 Proposed bonding model for hydrophilic Si wafer bonding at different temperatures. (a) Room temperature-110 °C: Formation of stable hydrogen bonding between molecular water across the bonding interface. (b) 110-150 °C: removal of interface molecular water and formation of siloxane bonds. (c) 150-800 °C: stable siloxane bonds. (d) >800 °C: viscous flow of interface oxide [9].

For hydrophilic wafer bonding, the annealing period can be divided into four stages as shown in Fig. 2.7:

a) From room temperature to 110 °C: slow fracture effect and interface water rearrangement.

During room-temperature bonding, the two wafers bond to each other via hydrogen bonding between the absorbed water molecules on the two surfaces. The linkage of two or three water molecules can form a bridge across the two bonding surfaces. All or most of the molecular water can only be removed from silica surfaces upon heating above 120 °C in air [69,70]. Since the water film structure exists at this stage [71], the main interface reactions in this temperature range should be: (1) The slow fracture effect of Si-O-Si bonds on both surfaces via attack by the interface water [69], i.e. the reverse reaction (2.3); (2) Rearrangement of the interface molecular water to form more stable hydrogen-bonded structures. The reactions are both time and temperature dependent. An increased density of silanol groups at the interface results in an enhanced bonding energy.

b) From 110 to 150 °C: condensation of silanol groups across the interface.

When the interface is drying gradually during annealing at > 110 °C, some of the molecular water diffuses along the bonding interface to the ambient, and some water molecules will diffuse through the surrounding native oxide and react with Si to form SiO₂ and hydrogen [9,70]. Thus, the forward reaction of reaction (2.3) will readily occur and more Si-O-Si groups between two surfaces will be produced. The oxide formed contributes to close the interface microgaps. The formation of strong siloxane bonds at the interface results in a rapid increase in surface energy of the bonded pair.

c) From 150 to 800 °C: bonding energy limited by contacted area.

It is believed that almost all silanol groups in the real contacted areas can be converted to siloxane bonds at ~ 150 °C [72]. From 150 to 800 °C, the surface energy of the bonded pairs has reached the value determined by the contacted area at the interface over which all silanol groups at the interface have converted to siloxane bonds. Since the bonding surfaces are never perfectly smooth, the area over which bonding really occurs is limited. In addition, inert gases such as nitrogen trapped in nanocavities formed by the microroughness of the two bonded surfaces may locally prevent the formation of siloxane bonds. Therefore, to get fully bonded wafer pair, higher temperature annealing is needed.

d) From 800 °C to above: complete bonding via oxide flow.

At temperature higher than 800 °C, viscous flow of the oxide occurs to fill up the interface microgaps and to form more siloxane bonds. Finally, after sufficient time annealing, completed bonded wafer pair can be achieved.

2.2.4 Bonding Characterization

The bonding quality of a bonded wafer pair is commonly described by bond efficiency and bond strength. Bond efficiency is expressed as the % of the bonded area over the entire wafer area, and is widely measured by the scanning image of the bonding interface. Bond strength is obtained by determining the tensile strength or surface energy of bonding. A number of nondestructive and destructive techniques are used to characterize the bonding.

2.2.4.1 Bonding Interface Imaging

One of the most serious problems in wafer bonding is the formation of unbonded area, also terms as interfacial bubble. Optical microscopy, infrared transmission, X-ray topography, acoustic microscopy, interface etching and cross-sectional analysis [9] are useful imaging methods for measuring the interface bubbles.

If one of the bonded wafers is transparent to visible light (e.g. a glass wafer) the bonded interface can be inspected directly with optical microscopy. This method is inexpensive, efficient and especially useful in adhesive wafer bonding since bond defects in adhesive wafer bonding are usually not very dependent on the wafer materials. However, it cannot be used to characterize bonded wafers consisting of nontransparent materials.

In infrared transmission imaging, the bonded wafers are placed between an infrared source and an infrared sensitive camera. Defects at the bond interface are displayed as contrasts in the infrared image. The technique is comparably simple, fast and inexpensive. However, Infrared transmission can only be used if all wafer materials involved are transparent to infrared light (e.g. silicon).

X-ray topography is a method used to obtain an image of deviations from ideal, undistorted lattice planes, which can only be applied to single crystalline materials. X-ray topography has a typical spatial resolution of 2-20 μm , which is much better than that of conventional infrared transmission techniques. However, X-ray topography is comparably expensive and time consuming.

Acoustic microscopy makes use of the fact that acoustic waves can propagate through solid-state materials. The scattering of acoustic waves depends on changes in the elastic properties of the materials and thus voids and defects at a bonded interface

can be detected. When an ultrasonic wave is introduced, it encounters an interface between two materials and is partly reflected and partly transmitted. In a material without defects, the only reflections one can record are those from the front and the back of the piece. But if a defect is encountered, the wave will reflect at that local interface and an echo will appear on the oscilloscope. Depending on the frequency range used, the resolution of acoustic microscopy can reach up to $10\mu\text{m}$. Acoustic microscopy measurements are easy to operate, fast and applicable to practically all materials.

In interface etching, one of the bonded wafers is sacrificially etched to a thin etch-stop layer with a suitable etching technique. Voids and defects can then be visually inspected through the thin etch-stop layer using optical microscopy. If larger defects are present at the bonded interface, the etch-stop layer can buckle or burst open, which indicates these areas are unbonded. For silicon wafers, the interface etching can be performed using wet etching or deep reactive ion etching (DRIE), in which SiO_2 can be used as the etch-stop layer.

Cross-sectional analysis of a bonding interface is done by cleaving or dicing a bonded wafer pair perpendicular to the bonding interface. The cross-section of the bonding interface can then be inspected using optical microscopy or scanning electron microscopy (SEM). In some cases, the cross-sections of the diced samples must be polished in order to obtain clear image of the bonding interface. This technique is especially useful for the inspection of bonding with thin intermediate bonding materials such as adhesives.

In this work, acoustic microscope is used. Optical microscopy and infrared transmission imaging are not applicable because SiO_2 wafer is used and it is not transparent to infrared light and visible light. X-ray topography isn't selected because

it is expensive and time consuming. Last two methods, interface etching and cross-sectional analysis aren't used for they are destructive characterization methods and the bonded wafers cannot be further used after this characterization.

2.2.4.2 Bond Strength Measurements

Pull test (tensile load test) [73] and crack opening test [74,75] are two most commonly used methods to measure bond strength, which are illustrated in Fig. 2.8 and Fig. 2.9, respectively. The pull test measures the tensile strength of a bonding while the crack opening test measures the surface energy of a bonding.

Figure 2.8 Schematic drawing of pull test

In pull test, bonded samples are pulled apart as illustrated in Fig. 2.8. The load necessary for destroying the bonding is measured. Load measurements are typically performed on strain test machines. The tensile strength of a bonding is computed as the tensile forces at the time of fracture divided by the bonded area of the sample.

The most convenient method of measuring the bonding energy of bonded pairs is the crack-opening method [75] schematically shown in Fig. 2.9. This technique is

based on the equilibrium of elastic forces of the bent separated part of a pair and bonding forces at the crack tip. The total bonding energy is given by Eq. (2.4)

$$r = \frac{3t_b^2 E_1 t_{w1}^3 E_2 t_{w2}^3}{8L^4 (E_1 t_{w1}^3 + E_2 t_{w2}^3)} \quad (2.4)$$

where E_1 and E_2 are respective Young's modulus of bonded wafer.

Figure 2.9 Schematic diagram of the crack-opening method. From [75]

In the crack opening test, also known as razor blade test, a blade with a defined thickness is introduced in the space between the bonded wafers as illustrated in Fig. 2.9. The length of the resulting crack is measured with infrared inspection and the surface energy keeping the wafers together is derived. Blade insertion tests are the least difficult tests to perform.

However, there are many drawbacks to this test [76]. The first is the inability to directly correlate surface energy to actual mechanical strength values through a theoretical expression.

The surface energy of Eq. (2.4) is based on the crack propagation of a linearly elastic solid. Again, this is inappropriate for single crystal silicon. The elastic modulus used in reference [75] was reported to be that for the wafer orientation of (100). The modulus to be used should be those that are tangential to the surface in the direction

of the crack propagation. Therefore, if only one module is used, then the surface energy measured would be dependent upon the direction the razor blade was inserted. For example, Young's modulus for (100) and (110) silicon are 130 GPa and 169 GPa respectively [77]. If the blade was inserted randomly between these directions, the data could have an error as high as ~30%.

The dependence of the surface energy on measured crack length raised to the fourth power is a source of another error. The error involved in measuring the distance between the razor blade and the crack tip, usually done indirectly via infrared imaging, must be minimized as much as possible, and thereby making the test difficult to administrate.

In addition, the crack opening method cannot be used if the bonding is too strong to introduce the blade without cracking one of the bonded wafers. Therefore, tensile and shear load test (pull test) was chosen as method to measure bond strength.

2.2.4.3 Chemical Characterization of Bonding Interface

Characterization of the interface is particularly challenging and may be best achieved using infrared radiation [78]. Conventional surface science techniques cannot penetrate through a wafer which is 0.5mm thick in this work. In addition, techniques such as x-ray photoelectron (XPS) and secondary ion mass spectrometry (SIMS) require grinding and etching prior to analysis, which is destructive and only possible for well bonded wafers (i.e., after a high temperature annealing). In contrast, infrared (IR) spectroscopy is well suited to the study of both the physical and chemical aspects of the interface at room temperature, and subsequent bonding after high temperature annealing.

In general, the IR radiation can easily reach the buried interface since Si is transparent above 1500 cm^{-1} . As a result, the characteristic high frequency ($> 2000\text{ cm}^{-1}$) stretching vibration of hydrogen-containing species such as Si-H, H_2O , OH, NH_x , and CH_x can be routinely probed. Furthermore, the lower frequency ($<1500\text{ cm}^{-1}$) modes of important atoms such as O, C, N, and F can also be studied, although this frequency region is quite challenging because of Si lattice absorption, diminishing IR source intensities, and the lower sensitivity of IR detectors below 1500 cm^{-1} . Therefore, the sample dimensions become critical if one wishes to probe the $700\text{-}1500\text{ cm}^{-1}$ spectral range.

Fourier Transform Infrared Spectroscopy (FTIR) is a powerful tool for identifying types of chemical bonds in a molecule by producing an infrared absorption spectrum that is like a molecular "fingerprint". It can be applied to the analysis of solids, liquids, and gasses. The term Fourier Transform Infrared Spectroscopy (FTIR) refers to a recent development in the manner in which the data is collected and converted from an interference pattern to a spectrum. Today's FTIR instruments are computerized which makes them faster and more sensitive than the older dispersive instruments.

One FTIR method proposed by Feijoó et al. [79], named multiple internal reflection geometry-Fourier infrared spectroscopy (MIRS-FTIR) or Multiple internal transmission-Fourier infrared spectroscopy (MIT-FTIR) [80], is a suitable characterization method for determine the chemical nature of the bonded interface layer. It is shown in Fig. 2.10. The bonded wafers are diced into rectangular samples ($3.8 \times 1.5\text{ cm}^2$, 1 mm total thickness) and the short ends of these samples are beveled at 45° to allow the IR radiation to enter and exit the samples after passing 38 times through the bonding interface. The 38 times can be calculated from Fig. 2.10. This

geometry provides an enhancement for absorption perpendicular to the interface [79]. Consequently, contributions by the outer silicon surface to the spectra are negligible compared to the interface absorption.

Figure 2.10 Schematic drawing of MIRS-FTIR measurement [79].

2.2.5 Low Temperature Wafer Bonding

Upon room temperature wafer bonding in air, the bonding energy is usually very low because the attraction between the pair is the van der Waals force and hydrogen bond. [81] In order to allow the bonded wafer pairs to sustain further wafer processes such as lapping, thinning and patterning, they have to be annealed at elevated temperature after the room temperature bonding to enhance the bond strength. However, the high temperature post-annealing used in the bonding process will limit the applications of wafer bonding, especially in the bonding with processed wafers as follows [82,83].

- 1) Thermal induced mechanical stress in bonding of materials with different thermal expansion coefficients;
- 2) Undesirable changes and reactions in the case of materials and structures which are sensitive to high temperature;
- 3) The occurrence of precipitates of oxides and vacancies at the bonded interface

during heat treatment.

Therefore, it is crucial to achieve strong bonding by low temperature annealing. Up to now, there are a number of studies which are aimed at the development of methods that can yield strong bonding at low temperature or even at room temperature [15-20,84-86].

One effective approach is using dry or wet methods to activate wafer surfaces after cleaning and before room temperature bonding. In some cases, the cleaning and activation process may be combined in which the cleaning treatment also activate the bonding surfaces like RCA cleaning that also can activate the surface. A DHF solution treatment to enhance the low temperature bonding energy of thermal oxide covered wafer bonding has been presented [84]. It was also found that surface activated by dipping in hot nitric acid [85], or in hot NH_4OH solution [86] can effectively enhance bond strength at low temperature as compared to that treated only in standard RCA solution.

Surface treatment by plasma exposure has also demonstrated the ability to enhance the bonding energy for wafer bonding [18-20]. An amorphous surface layer on silicon wafers, which was prepared by As^+ ion implantation, or thin film sputtering deposition, was also proved to be useful to enhance the bonding energy dramatically [84].

It was also found that boron doped surface layer (produced by Boron Ion Implantation or treatment by B_2H_6 plasma) can enhance the hydrophobic bonding energy [10,84]. The mechanism is believed to be due to the effect of the neighbouring boron which appears to weaken the Si-H_x bonds leading to reduction of the activation energy of release of hydrogen from the trapping centre [87,88]. But one dissimilar

layer with affluent boron will be produced, which may cause problem in VLSI application.

Vacuum wafer bonding is another way to achieve high bond strength at low temperature. Tong et al [16] proved the ability of low vacuum to improve the bond strength at low temperature. The improvement is believed to be that the out-diffusion of water and inert gas trapped at the interface can be accelerated by the vacuum at low temperature. Bonding conducted under ultra-high vacuum (UHV) is also very attractive for bonding wafers without native oxide [15]. For in-situ bonded pair of thermally cleaned hydrophobic silicon wafers under UHV, covalent bonds have been achieved at room temperature [15]. Very strong bonding has also been achieved at room temperature for silicon and gallium arsenide with the wafers cleaned and activated by an argon fast atom beam under UHV and in-situ bonded under an external pressure [89], which is a bit similar to the plasma treatment. But UHV wafer bonding usually requires preheating ($\sim 600^\circ\text{C}$) of the wafers prior to bonding, or application of pressure during bonding in addition to UHV conditions. It is also costly to be applied in the mass production [10].

Because of their simplicity and evident improvement of bond strength at low temperature, Plasma activation wafer bonding and vacuum wafer bonding were chosen as low temperature wafer bonding methods in this work.

2.3 Summary

SOI technology and wafer bonding technology were reviewed in this chapter. Owing to some advantages over the conventional bulk silicon substrate, SOI technology gains position in the fabrication of next generation ULSI. A number of

Chapter 2: Literature Review

fabrication methods have been developed since the idea of SOI was proposed, e.g. ELO, LSPE, FIPOS, ZMR and SIMOX and BESOI. The last two fabrications methods are most promising and have been used in mass production. Then, they were introduced in this chapter and wafer bonding was focused. The process and mechanism of conventional wafer bonding were emphasized as they are the basic knowledge for my study. The common characterization methods in wafer bonding were listed, such as methods to detect the voids, bond strength measurement, and chemical characterization of bonding interface.

The need for low temperature wafer bonding was analyzed. And several low temperature wafer bonding methods were presented, such as dry and wet activation, ion implantation, boron doping, vacuum wafer bonding and so on.

Chapter 3 EXPERIMENTAL PROCEDURES

3.1 Wafer Bonding Process

In this study, medium vacuum wafer bonding (MVWB) and plasma activated wafer bonding (PAWB) were chosen as low temperature wafer bonding methods. In order to distinguish the enhancement of these two low temperature wafer bonding methods, conventional direct wafer bonding was also performed.

As the mechanism of the low temperature wafer bonding is the focus in this project, two most important parameters were selected as main variables, namely annealing temperature and annealing time. They have crucial effects on wafer bonding and are playing key roles in the mechanism of wafer bonding [9]. Three kinds of wafer bonding, Si-Si, Si-SiO₂, and SiO₂-SiO₂, were performed. However, due to the similarity in their mechanisms [9], only Si-SiO₂ wafer bonding results will be shown in this work. Also, the whole bonding process was carried out in a clean room of class 10K in order to keep the process clean.

To reduce the randomness of experiment, for each bonding condition, six pairs of wafers were bonded. And for pull test, six diced samples from every bonded wafer were chosen to be tested and the bond strength was calculated based on the average fracture force.

The process flow of conventional wafer bonding, MVWB and PAWB are shown in Figures 3.1 to 3.3 respectively. The details of the steps mentioned in the process flows are described as follows.

Wafer: Si wafers used in this study are commercial bare CZ-grown 4", p-type, (100) wafers with resistivity of $1-50 \Omega \cdot \text{cm}$. SiO_2 wafers were (100) Si wafers covered with 5000-6000Å thickness of thermal oxide. For comparison, several Si(111)/Oxide bonding were performed. The (111) wafer are commercial bare CZ-grown 4", p-type wafers with resistivity of $1-50 \Omega \cdot \text{cm}$.

RCA1 Cleaning: The effect of the wet chemical cleaning process on the surface microroughness of Si wafers was studied by Miyashita et al [90]. The microroughness on the Si substrate surface and the oxide surface was evaluated with STM and AFM. The surface microroughness was found to increase in wet chemical processing, in particular in $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ cleaning (RCA1 cleaning). It has been shown that the microroughness does not increase at all if the NH_4OH mixing ratio in RCA1 solution is suppressed at a low level at $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}=0.05:1:5$ in contrast to the conventional mixing ratio of 1:1:5, and room temperature ultra-pure water rinsing is introduced right after the RCA1 cleaning. At the same time, the RCA1 cleaning with its NH_4OH mixing ratio suppressed at the low level has been found to be still very effective in removing particles and metallic impurities from the Si surface. Therefore, RCA1 ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}=0.05:1:5$) was chosen to fulfill the cleaning at 70°C for 10 minutes in the present work, followed immediately by a 5-minute DI water rinsing and N_2 gun drying step.

Chapter 3: Experimental Procedures

Figure 3.1 Conventional wafer bonding process flow

Figure 3.2 MVWB process flow

Figure 3.3 PAWB process flow

Room Temperature Bonding (RT Bonding): After drying, the two as-bonded wafers were contacted with each other in air from one edge as shown in Fig. 3.4. In this way, most of the air could be squeezed out and less bubble will be produced.

Figure 3.4 Schematic of room temperature wafer contact

Air or N₂ Annealing: After room temperature bonding, the bonded wafers were loaded into oven for annealing to enhance the bond strength. For annealing at room temperature up to 500°C, the annealing was performed in oven and the atmosphere is air. For 800-1000°C annealing, it was performed in N₂ ambient.

Plasma Activation: Plasma treatment was done in MARCH PX-1000 plasma system with a power of 200W, and an Ar gas flow rate of 30 sccm. The processing time is 30 seconds under a pressure of 90 mTorr.

Vacuum Annealing: After RCA1 cleaning, DI water rinsing, N₂ gun drying, and room temperature bonding were performed, the pre-bonded wafers were immediately loaded into the EV501 wafer bonder. The chamber in the bonder was

then pumped down, and when the vacuum reached 10^{-3} mbar, heating begun at a rate such that the temperature reached the value in 30 minutes and then it remained for a pre-set period of time. At the end of the annealing, temperature was lowered down to room temperature in 2 hours. The vacuum atmosphere was maintained at 10^{-4} mbar throughout the entire bonding process.

3.2 Instruments Used in Wafer Bonding

In this section, the main instruments used in this work are introduced, including oven for air bonding, vacuum wafer bonder and plasma treatment system.

3.2.1 Oven Used for Conventional wafer bonding

Annealing at less than 500°C is performed in an oven (LENTON WHT 6/30, from Lenton Inc.) shown in Fig. 3.5 (a). This oven can be operated at temperatures up to 600°C and is capable of continuous operation at maximum temperature.

Annealing at higher than 800°C is done in an oven (Tystar 4 Stack Four Horizontal furnace) shown in Fig. 3.5 (b). The Tystar oxidation furnace is primarily meant for oxidation/annealing batches of 4" silicon wafers or small samples placed on the surface of one 4" silicon wafer. The samples are placed in an atmosphere of constantly refreshed dry nitrogen at temperatures between $700\text{--}1000^{\circ}\text{C}$. At the moment there is no restriction on the length of an oxidation/annealing.

(a) LENTON Oven, WHT 6/30

(b) Tystar 4 Stack Four Horizontal furnace

Figure 3.5 Picture of oven used for conventional wafer bonding

3.2.2 Wafer Bonder Used for MVWB

EVG501 Wafer Bonding System is designed to perform all wafer bonding processes for wafer size up to 150 mm. It is a PC-control system, which mainly includes two parts: control part (one PC and one console) and vacuum chamber. The system is shown in Fig. 3.6 (a) and the plan-view of the opened chamber is shown in Fig. 3.6 (b). The maximum annealing temperature allowed for this chamber is 500°C.

(a) EVG501 system

(b) Plan-view of the chamber

Figure 3.6 Picture of wafer bonder, EV-501

3.2.3 Plasma Treatment System Used for PAWB

March PX-1000 plasma system is a RF plasma cleaner & etcher made by March Instruments, Inc. It is shown in Fig. 3.7. The PX-Series can control the vacuum, gas flow rate, chamber pressure, and RF power level.

Figure 3.7 Picture of March PX series plasma cleaning system

3.3 Characterization of Wafer Bonding

Various characterization tools are utilized to measure the properties of the bonded wafers.

- **Scanning acoustic microscopy (SAM)**

After bonding, the bonded pairs are examined under SAM using C-SAM SERIES D6000 from SONOSCAN Inc.. The resolution of the SAM to detect the bubble is $2.5\mu\text{m}$. Image analysis technique is employed to analyze the SAM micrographs as follows. Firstly, the pictures are changed to grayscale mode using an image processing software (Photoshop 7.0). The percentage of bubble is then calculated using Matlab 6.5 image processing toolbox.

- **Tensile pulling test**

Tensile pulling test is employed to characterize the bond strength. In this work, after the C-SAM measurement, the bonded wafers were diced into $10 \times 10 \text{ mm}^2$ pieces and the pairs which are bubble free detected by SAM were chose to do tensile strength measurement using an Instron tensile testing machine (Model 4505).

Figure 3.8 Setup for evaluation of bond strength.

Prior to tensile test, the top and bottom surfaces of the bonded pairs are roughened with abrasive paper and ultrasonically cleaned in acetone. The bonded pair is fixed between two aluminum alloy socles, which has also been sand blasted and ultrasonically cleaned in acetone. The test is done by applying a mechanical force. The schematic diagram of the pulling test machine used in the experiments is shown in Fig. 3.8. Six diced samples from one bonded pair are measured and the average value is taken as the bond strength of this bonded wafer.

- **Atomic force microscopy (AFM)**

Surface roughness of as-bonded wafer is measured using AFM (Dimension™ 3000). Tapping mode is used.

- **Contact angle measurement (CA)**

The hydrophilicity of a wafer surfaces can be easily determined by measuring the contact angle of a liquid drop (Glycerol rather than DI water). Contact angle of liquid droplet on wafer is measured in an optical contact angle system (OCA20, Dataphysics). Because the contact angle will decrease with the evaporation of the

Chapter 3: Experimental Procedures

liquid droplet, the picture of the liquid droplet on the wafer surface is snapped after ~ 2 seconds, and then the contact angle can be measured at almost the same condition. The volume of one liquid droplet is about 0.5 ml.

● Transmission electron microscopy (TEM)

The cross-section of the bonded wafer is observed by transmission electron microscopy (Philips CM 200FEG). The steps of sample preparation are shown in Fig. 3.9 schematically.

STEP 1

Cut rectangular wafers from bulk material using ultrasonic disc cutter

STEP 2

Coat all wafers with a thin layer of G-1 & load into Teflon™ mold

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STEP 3

CURE ON HOT PLATE AT 130°C FOR 10 MINUTES

Cure glued stack under pressure to form a strong bond between wafers.

STEP 4

Cut cylinder from stack using ultrasonic disc cutter

STEP 5

Glue cylinder inside metal tube.
Cure on hot plate.

STEP 6

Sliced specimen discs ready for disc grinding and dimpling.

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Step 7: Use goniometer disc mount to adjust plane of specimen and use precision disc grinder (Gatan Model 623 Disc Grinder) to prepare parallel-sided disc.

Step 8: Thin the center of the specimen by mechanical dimpling (Gatan Model 656 Dimple Grinder).

Step 9: Ion milling.(691 Precision Ion Polishing System (PIPS™))

Figure 3.9 Schematic of sample preparation for TEM

3.4 Summary

The processes of conventional wafer bonding, MVWB and PAWB were described. And the instruments used in the processes were introduced in details. To characterize the as-bonded and bonded wafers, SAM, pull test, AFM, contact angle

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measurement, TEM were utilized in this work. The characterization instruments were also introduced.

Chapter 4 MEDIUM VACUUM WAFER BONDING

(MVWB)

4.1 Why Low Temperature Wafer Bonding

As discussed in Chapter 2, conventional direct wafer bonding usually requires high-temperature annealing above 800°C or even 1000°C to achieve strong bonding. But there will arise many problems with high temperature treatment. Among them, thermally induced mechanical stress in bonding of materials with different thermal expansion coefficients may cause many serious problems. Mechanically, severe stresses can lead to deformation, debonding, and even fracture of the pair. In addition, stress also can degrade the performance of device fabricated on the bonded structure.

To get the quantitative degree of the stress induced by the annealing in the full SOI and partial SOI structure, the surface stress, interface stress and work layer stress were simulated by ANSYS, a finite-element analysis software. The result is shown in Table4.1. (Figure4.1 shows the dimension for the ANSYS simulation).

From the comparison, we may find that the high temperature (1150 °C) annealing induces the very severe stresses that are nearly three times of the stresses induced by low temperature (400°C) annealing. In addition, the stresses in partial SOI are a little larger than that in full SOI.

Chapter 4: Medium Vacuum Wafer Bonding

Therefore, it is proven quantitatively from the aspect of stress that low temperature wafer bonding process for fabrication of SOI and partial SOI is necessary.

Table 4.1 Comparison of stresses in full SOI and partial SOI at different annealing temperature

	Annealing Temperature (°C)	Max surface stress (MPa)	Max interface stress (MPa)	Max stress in work layer (MPa)
Full SOI	1150	480.4	288.57	625.9
	400	173.74	94.24	213.3
Partial SOI	1150	484.9	312.57	625.9
	400	175.28	103.54	218.6

Figure 4.1 Schematic of the model for the ANSYS simulation ($t1=500\text{ }\mu\text{m}$, $t2=1\text{ }\mu\text{m}$, $t3=50\text{ }\mu\text{m}$; $l0=100\text{ }\mu\text{m}$, $w0=100\text{ }\mu\text{m}$, $l1=50\text{ }\mu\text{m}$, $w1=50\text{ }\mu\text{m}$, Max interface strength for wafer bonding is 12 Mpa, Withdrawal velocity at 500 mm/min.)

4.2 Introduction of Vacuum Wafer Bonding

There are several vacuum wafer bonding methods published, such as wafer bonding in ultrahigh vacuum (UHV) (10^{-10} mbar) [15], wafer bonding after Ar beam surface activation in high vacuum (10^{-8} mbar) [17], wafer bonding at medium vacuum level (10^{-4} mbar) [91,92], and wafer bonding at low vacuum level (several mbar) [16].

Extensive studies on the effect of bonding parameters on the bond quality, which includes bond efficiency (the ratio of the bonded area to the entire wafer area) and bond strength, have been reported for conventional direct wafer bonding. Also, bond speed, which is defined as the reciprocal of the time to achieve saturation bond strength, is an important parameter if wafer bonding is to be employed for mass-production. Conventional wafer bonding usually requires more than one hundred hours achieving saturation of the bond strength, which is apparently not economical.

In contrast, MVWB is advantageous over the conventional direct wafer bonding in that it has higher bond strength and bond efficiency obtained at low annealing temperature, and the bond speed is dramatically enhanced. Therefore, MVWB deserves detailed study. In this chapter, detailed and systematic work on medium vacuum wafer bonding is presented.

While high bond strength can be achieved by MVWB, its mechanism is rarely discussed even qualitatively [91,92]. To our knowledge, no mathematical model has been established for the medium vacuum level wafer bonding. In this work, we develop a mathematical model for the medium vacuum wafer bonding by combining the diffusion-reaction theory and the theory of Knudsen diffusion in porous media. Experimental results are used to verify the mathematical model. Furthermore, this

model can be applied to study the effects of several processing and material parameters on the bond strength.

4.3 Experiment

To investigate the improvement of MVWB over conventional wafer bonding, experiments on the conventional direct wafer bonding and medium vacuum wafer bonding were performed as shown in Table 4.2 for comparison purpose. Since the two most important parameters in the study of mechanism of wafer bonding are annealing temperature and time, which have crucial effects on bonding quality, such as bond strength, efficiency and speed [9], different combination of annealing temperature and time are designed as in experimental Groups C, D and E.

As the influence of other variables on the bonding quality can provide help to comprehend the mechanism of wafer bonding, group A experiment is designed to study the effect of applied load; effect of ambient under which two as-bonded wafers are contacted is investigated by group B, and the effect of the wafer orientation on the bonding quality is studied by group D. The details of all processes mentioned are discussed below.

Table 4.2 Different wafer bonding processes to study MVWB

Bonding Group			Process						
			RCA Cleaning	Contact in Air	Vacuum (mbar)	Contact in Vacuum	Applied load (KN)	Annealing	
								°C	hour
Vacuum Bonding	Group A	A1	X*	X	X(10 ⁻⁴)		1	400	2
		A2	X	X	X(10 ⁻⁴)		2	400	2
		A3	X	X	X(10 ⁻⁴)		3	400	2

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	Group B	B1	X		$X(10^{-2})$	X	0	400	2
		B2	X		$X(10^{-3})$	X	0	400	2
		B3	X		$X(10^{-4})$	X	0	400	2
	Group C	C1	X	X	$X(10^{-4})$		0	25	1-5
		C2	X	X	$X(10^{-4})$		0	100	1-5
		C3	X	X	$X(10^{-4})$		0	200	1-5
		C4	X	X	$X(10^{-4})$		0	300	1-5
		C5	X	X	$X(10^{-4})$		0	400	1-5
		C6	X	X	$X(10^{-4})$		0	500	1-5
	Group D**	D1	X	X	$X(10^{-4})$		0	200	1-5
		D2	X	X	$X(10^{-4})$		0	300	1-5
		D3	X	X	$X(10^{-4})$		0	400	1-5
		D4	X	X	$X(10^{-4})$		0	500	1-5
Air Bonding	Group E	E1	X	X			0	200	1-5
		E2	X	X			0	300	1-5
		E3	X	X			0	400	1-5
		E4	X	X			0	500	1-5

Note: *:“X” means the process step was carried out; **: Si wafers used in the Si-SiO₂ bonding are all (100) orientated except in group D, in which (111) orientated Si wafers are used.

Influence of the applied load on wafer bonding is studied by processes shown in group A. After RCA cleaning and drying, the wafers are contacted immediately and loaded into the EV501 wafer bonder. The chamber in the bonder is then pumped down, and when the vacuum reaches 10^{-4} mbar, heating begins at such a rate that the temperature reaches 400 °C in 30 minutes and then it remains that value for 2 hours under different applied loads, 0, 1, 2 and 3 KN respectively. The load is applied only in the process of annealing. At the end of the 2-hour constant temperature annealing, the load is removed and temperature is lowered down to room temperature in 2 hours. The medium vacuum was maintained throughout the entire bonding process.

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In group B, after RCA cleaning and drying, the two wafers were immediately loaded into the bonder and separated by three flags. When the vacuum reached different levels (10^{-2} , 10^{-3} , 10^{-4} mbar), the flags were pulled out and two wafers were bonded together followed by annealing at a temperature of 400 °C for 2 hours. It is shown in Fig. 4.2 schematically.

Figure 4.2 Schematic diagram of wafer contacting in vacuum

In group C, after cleaning and drying, wafers were loaded into the vacuum bonder after being contacted in the air. Vacuum was then applied. When the vacuum level reached 10^{-3} mbar, heating began at such a rate that the temperature reaches the preset annealing temperature (25, 100, 200, 300, 400, 500 °C respectively) in 30 minutes and then maintained at the temperature for different duration (1, 2, 3, 4, 5 hours). Thereafter, the bonded pair was cooled down to room temperature in 2 hours. The designated vacuum level was maintained throughout the entire bonding process.

The processes of group D were used to investigate the effect of the wafer orientation on the bonding quality. The silicon wafers used are 4", 500 μm thick p-type, (111) standard bare wafers with resistivity of 1-50 $\Omega\text{-cm}$. The oxide wafers are the same as those used in other groups. The processes are also the same as those described in group C. The only difference is that the Si wafer used are (111) orientated.

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For comparison, the processes of conventional air wafer bonding are performed as group E experiments shown in Table 4.2. After cleaning and drying, two wafers were bonded in the air at room temperature and then they were loaded into oven. The oven began to heat up to the preset annealing temperature (200, 300, 400, 500 °C respectively) and maintain the temperature for different duration (1, 2, 3, 4, 5 hours). Finally, the oven was switched off and cooled down to room temperature. Since the samples annealed under 200 °C cannot withstand the dicing, we cannot achieve the bond strength of these samples, thus no comparison can be made with the vacuum bonding for samples annealed under 200°C.

4.4 Experimental Results and Discussion

4.4.1 Influence of Applied Load

Based on the models of conventional direct wafer bonding proposed by Stengl et al [93] and Tong et al [9], bonding sites between two wafers play a very important role in enhancing the bond strength. More bonding sites will result in higher bond strength. When the conventional wafer bonding is performed at low temperature (<600 °C), a lack of bonding sites causes incomplete bonding, and an applied load can push more bonding sites to be connected between two wafer surfaces. Therefore, a high-applied load yields high bond strength, as shown by the red curve [94] in Fig. 4.3

If, on the other hand, the bonded surfaces are fully hydrated through treatment such as the plasma activated wafer bonding, the distance between the two wafers is closed by van der Waals forces between bonding sites on the two surfaces until the entire wafer area is bonded. Therefore, the wafers are able to overcome most of the local waviness and an applied load is ineffective as shown by the work presented in

ref. [17]. The green curve in Fig. 4.3 shows this effect proven experimentally by Takagi et al [17].

Figure 4.3 Comparison of bond strength under different loads between our results and references [17, 94] Note: the two curves at the top right corner cited from references here show the trend of dependence of bond strength on applied load, the exact value is only for our results, meaningless to both of them.

However, our study on low temperature MVWB shows that the applied load does have an effect on the bond strength that is shown in Fig. 4.3 (the black curve with error bars). The higher the applied load, the lower the bond strength and the bonded pairs have highest bond strength when no load is applied. This is in contrast to the previous works [17,94]. In all cases of vacuum wafer bonding, the bond strengths are above 19 MPa, which is high enough for practical applications, such as dicing and device fabrication. Moreover, in the case of zero applied load, the bond strength is much higher than the cases where loads are applied 1kN, 2kN and 3kN respectively.

The dependence of bond strength on the applied load in vacuum wafer bonding indicated that the dominant bonding mechanism could be different from the

Chapter 4: Medium Vacuum Wafer Bonding

conventional and plasma treated low temperature wafer bonding. This dependence as observed in present study can be explained from two different dominant mechanisms, namely the enhanced diffusion effect of vacuum on trapped impurities [16] and electric field model in low temperature wafer bonding [76].

It is known that “vacuum” acts as a powerful “pump” which can suck the trapped gas, including water, out of the interface [16,91,92]. The reduction of trapped air and water at the bonding interface under vacuum significantly increase the bonding sites and allow covalent bond (siloxane) to be developed through the polymerization of silanol bonds on the bonding surfaces, i.e. through the reverse reaction (2.3). As more siloxane groups can be produced and hence more bonding sites can be bonded together, higher bond strength is resulted. This is evident from the SAM micrographs (Fig. 4.4) of the bonded pairs under different loads. The percentage of the unbonded area under different applied loads is shown in Fig. 4.5. From these two figures, we can find that the bubble size, bubble number and the percentage of the unbonded area increase with an increase in applied load. It is believed that a high-applied load keeps two wafer surfaces in tight contact at the early stage of wafer bonding. If there are impurities trapped during bonding process, such as gas, water molecule or water ring (tetramer) [93,95,96,97], the tight contact prevents them from escaping out of the bonding interfaces, which in turn cause the formation of bubbles or cavities.

Figure 4.4 C-SAM micrographs of the bonded wafers under different applied loads at temperature of 400°C, annealing time of 2 hours and vacuum of 10^{-4} mbar (black area is bubble)

Figure 4.5 Unbonded areas percentage under different applied loads

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Although the diced samples chosen for the pull test are those without bubbles as examined under SAM, the low bond strength for samples with high-applied load can be explained from the nano-scale perspective. Due to the nano-roughness of the surfaces before bonding, free volume is enclosed at the interface, and thus nano-sized voids are produced in the interface layer, which was observed by Reznicek et al [98]. Therefore, impurities can be trapped in these nano-sized voids in the interlayer, whose property is crucial to the bond strength. With higher applied load, more impurities will be kept in the interlayer. As a result, the density of the interlayer (i.e. the ratio, bonded area/whole surface area of bonded wafers) is reduced which result in lower bond strength observed. The effect of the trapped impurities is schematically shown in Fig. 4.6.

Figure 4.6 Schematic illustration of a trapped air bubble and nano-sized voids

Experimentally, our SAM has a spatial resolution of 2.5 μm as limited by the wavelength/frequency of the acoustic beam [9], thus nano-voids of size below 2.5 μm cannot be observed. Hence, samples that are chosen for tensile test could contain such nano-voids that are beyond the detection limit of our SAM, but the presence of nano-voids in the samples reduces the bond strength as observed in this work.

Also, under high applied load, water could be trapped at the bonding interface. The presence of water prevents the reaction (2.3) to proceed to the left side [9], rendering less siloxane to be produced, thus lower bond strength results.

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This is in contrast to conventional high temperature wafer bonding as reaction (2.3) is no longer reversible at $T > 425^\circ\text{C}$. Thus, the presence of water, if there is, will not affect the production of the siloxane, and also water can be easily diffused into bulk and react with Si via reaction (4.1) below at high temperature,

Hence, the dependence of bond strength on applied load in conventional wafer bonding after high temperature annealing is different from the present work about high temperature wafer bonding.

The dependence of bond strength of MVWB on applied load will be further verified by the MVWB model in section 4.5.6.4.

Also, from a low temperature wafer bonding model [76] based on oxidation model of Cabrera-Mott [99], when the applied load results in trapped gas or water, these impurities will block ionized oxygen or hydroxyl groups to sweep to the opposite surface to react and form more siloxane groups, resulting in low bond strength.

4.4.2 Effect of Wafer Contact Sequence

Fig. 4.7 shows the effect of the ambient at which wafers are placed in contact on the bond efficiency of the bonded wafer pairs. The bonding is done using the processes in Group B. Wafers bonded using process C5 (vacuum bonding and annealing at 400°C for 2 hours) is chosen as reference. The percentage of the unbonded area in each bonded wafer pair was calculated as shown in Fig. 4.8. It can be seen that the best bond efficiency can be achieved by contacting the two wafers in air rather than in vacuum. Also, the higher the vacuum level at which two wafers are contacted, the larger the unbonded area, i.e., the poorer the bond efficiency.

Figure 4.7 SAM pictures of the bonded wafers from Group B and C (all were annealed at 400 °C for 2 hours)

Figure 4.8 Percentage of the unbonded area of the bonded wafers as a function of the vacuum level from Group B and C (C5, 400 °C, 2 hours)

The above observation can be explained based on the mechanism of conventional direct wafer bonding [9,93]. When two wafers are bonded at room temperature, the two wafers are held to each other via hydrogen bonding between the adsorbed water molecules on the two wafer surfaces. The surface coverage of water on the silica surface depends on the relative humidity (RH) [71]. In a vacuum chamber, the RH is very low, and the wafer surfaces are thus covered with lesser water molecules according to Henry's law [100]. Therefore, less silanol groups (Si-OH) can be achieved through the reverse reaction of reaction (2.3) at room temperature. As a result, less siloxane groups (Si-O-Si) can be produced during annealing, which results in more bubbles and lower bond strength.

From the SAM pictures shown in Fig. 4.7, it can be seen that the bubbles are distributed almost over the entire bonded wafers for the cases of B1, B2 and B3. Thus, it is very difficult to dice out six pieces of bubble free samples of size $10 \times 10 \text{ mm}^2$ for the pull test. Furthermore, such poor bond efficiency is not useful for practical application. Hence, the pull test for the samples from B1, B2 and B3 was not performed.

4.4.3 Effect of Annealing

The effects of annealing temperature and time on the medium vacuum bonding and air wafer bonding are investigated here. The results of bond strength within 5 hours of annealing using the processes in groups C and E are shown in Fig. 4.9.

Figure 4.9 Experiments results of bond strength after different bonding processes, e.g., different annealing temperature, annealing time and annealing environment (vacuum and air atmosphere). “V”: denotes vacuum wafer bonding; “A”: denotes air wafer bonding.

From this figure, two apparent phenomena can be observed:

a) It is apparent that medium vacuum bonding can enhance the bond strength compared to the air bonding. In all cases of vacuum wafer bonding under different annealing temperatures, the bond strengths are above 10 MPa, which is high enough for dicing. Also, it can be observed that the bond strength after 300 °C annealing increases abruptly to above 20 MPa as shown in Fig 4.9. This bond strength is high enough for practical use. Moreover, in the cases of annealing over 300°C, most of the breakage occurs inside the silicon wafer during pull test rather than at the bonded interface. The fracture surface is shown in Fig. 4.10. The good bonding quality can be seen using the TEM as shown in Fig. 4.11.

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b) Saturated bond strength can be achieved in much shorter time (several hours) under medium vacuum as compared to that of tradition wafer bonding, which always takes more than hundred hours [9] and is not suitable for mass-production. In other words, vacuum can accelerate the bonding process. This shows the potential of medium vacuum wafer bonding for mass-production applications, alone or combined with other surface activation methods.

(a) Fractured surface after pull test (b) Zoom-in photo of the dashed area in (a)
Figure 4.10 Optical micrograph of the fracture surface of the bonded pair after pull test (MVWB, 400 °C, 2 hours annealing)

Figure 4.11 TEM micrograph of the cross-section of the bonded pair (MVWB, 400 °C, 2 hours annealing)

The two important phenomena observed could be interpreted by the mechanism of medium vacuum wafer bonding as discussed in section 4.4.1. Seen

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from the above discussion, it is reasonable to propose that medium vacuum produces similar but stronger effect as low vacuum level during wafer bonding, i.e. the medium vacuum accelerates the diffusion of trapped impurities, such as water, nitrogen and hydrogen [96,97].

Furthermore, the bonding interface can be considered as porous in nature immediately after room temperature bonding due to the surface micro-roughness and uncovered area by the attached water molecules [9]. As more bonding sites are bonded through reaction (2.3), the interface gradually closes up, and thus changing the interlayer to amorphous like SiO_2 in the annealing process.

Using the proposed bonding mechanism, one can see that medium vacuum can enhance the out-diffusion of water molecules and other trapped impurities [91,92] at the initial porous interface, hence speed up reaction (2.3) and the formation of Si-O-Si., and thus more bonding sites can be bonded before the interface close-up. This results in an increase in bond strength and efficiency as well as the bond speed (i.e. the time taken for the bond strength to reach saturation value is shorter).

To show the bond efficiency of medium vacuum wafer bonding, the SAM results of bonded wafers under 4 hours annealing time at different annealing temperatures, 25, 100, 200, 300, 400 and 500°C respectively are shown in Fig. 4.12. Only one representative SAM picture for each annealing process is shown, but the calculated unbonded area percentage with error bar is shown in Fig. 4.13. One can see that the bond efficiency improves tremendously when the annealing temperature is above 300°C. Therefore, considering both bond strength and efficiency, 300°C annealing is adequate for practical use.

Figure 4.12 SAM pictures of the bonded wafers under different annealing temperatures

Figure 4.13 Percentage of the unbonded area of the bonded wafers as a function of annealing temperature from Group C (4 hours annealing)

4.4.4 Effect of Wafer Orientation

Resnik et al. [101] found that wafers in the (111) orientation exhibited higher bonding abilities compared to (100) in case of bonding wafers with native oxides. This was believed to be due to higher density of available bonding sites as a consequence of enhanced chemical oxide growth rate and its homogeneity on (111) surface. Moreover, it was believed that due to higher positive charge of oxides grown on (111)-oriented silicon as compared to (100), desorption of interfacial water is accelerated, thus increasing the bonding energy at lower temperature [101].

To investigate the effect of wafer orientation on the MVWB, processes of group D were performed and the results are shown in Fig. 4.14. It can be seen that at low temperature, bond strength of (111) wafers is higher than that of (100) wafers which is consistent to the result of Resnik et al. [101]. But the difference becomes smaller at higher annealing temperature. This is because the fracture strength of Si wafers used in this work is around 25-30MPa. Hence, if the interface bond strength is above 25MPa, any improvement in bond strength due to wafer orientation will not be detected, resulting in the small differences in bond strength as observed. This is evidenced from the pull test results where most of the bonded pieces broke in the Si itself instead of at the interface after high temperature (300 and 400°C) annealing.

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Figure 4.14 Effect of wafer orientation on bond strength

4.5 Mathematical Modeling of the Mechanism of MVWB

Although vacuum is a crucial factor in vacuum wafer bonding. The effect of the vacuum it takes in different vacuum range should be different. In UHV wafer bonding, the native oxide on the RCA cleaned Si surface can be removed by heating

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at 850°C for 30 minutes in UHV. The super-clean Si surface should be reactive and by bonding them together in-situ, a near-perfect bonding interface should result since almost no foreign atoms would be present in the mating Si surfaces. This is the mechanism of UHV wafer bonding [15]. As the two wafers were pre-bonded at room temperature prior to being loaded into the vacuum chamber in our experiments, medium vacuum cannot take effect as UHV does. Therefore, the mechanism of UHV wafer bonding is not applicable in our case. On the other hand, based on the mechanism of low vacuum level wafer bonding [16], we propose that water plays a crucial role in medium vacuum level wafer bonding and the enhancement of bond strength compared to conventional wafer bonding is due to the acceleration effect on water diffusion due to vacuum ambient.

From the widely accepted model of conventional wafer bonding proposed by Tong et al. [9], the interface formed between the two bonded wafers is SiO₂ like, and the crucial parameter that determine the final bond strength (or bonding energy) is the concentration of water. To achieve higher bond strength, the product of the polymerization of silanol groups across the interface, water, must be removed from the interface. Therefore, the study on the method to increase the bond strength is the same as the study on water diffusion in SiO₂.

Water in oxide can influence its properties. A trace amount of water reduces its viscosity, chemical durability and mechanical strength of the oxide [102]. Water can get into or out of oxide by diffusion [103]. Transport of water and oxygen in quartz has been previously measured with isotopic exchange and diffusion of tagged water molecules (D₂O and H₂¹⁸O) and oxygen (¹⁸O₂). The results have been interpreted in terms of network diffusion of constituents such as OH⁻ and O²⁻ [104,105]. However, this mechanism is contrary to many other experimental results,

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such as the concentration and time dependence of the apparent diffusion coefficients and their low energies that depend on the openness of the oxide structure [102]. Reaction-diffusion model, which was proposed in 1969 [106], is generally accepted as model of water diffusion in glass and oxide. The permeation of water in SiO_2 involves a strong reaction with siloxane (Si-O-Si) bonds in the network, in which the molecularly dissolved water dissociates to form two OH units with the additional O ion being provided by the SiO_2 network. This can be written as the reversible reaction (2.3).

As discussed above, due to the surface micro-roughness of the wafers to be bonded, the bonded interface is porous in nature immediately after room temperature bonding. The resulting void areas contain neither water molecules bonded by hydrogen bonds nor Si-O-Si bonds. These void areas can be viewed as pores in the interface region called interlayer. A schematic illustration of the mechanism is shown in Fig.4.15.

Figure 4.15 Schematic of the porous interface and diffusion of water

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In this work, for the sake of simplicity, we neglect the diffusion of other trapped gases, such as nitrogen, hydrogen and so on. The justification for this assumption will be shown from the computation results shown later.

In the temperature range below 500°C, some of the molecular water diffuses along the bonding interface to the outside, but some water molecules will also diffuse through the surrounding oxide into Si wafer, which is shown in Fig. 4.16.

Figure 4.16 Schematic of the proposed diffusion model of water in bonded interface

Diffusion and reaction of gases within porous materials continues to receive major attention because of the wide variety of applications in the chemical industries. The major steps involved in these reactions are the transport of reactants into internal pore structure, chemical reaction on the pore surfaces and transport of products from the particle interior to the particle surface. Because of the inherent complexities of the pore structure, these steps are considerably more complicated to describe than those

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involving the transfer of reactants and products between the bulk phase and the outer surface of the solid. Depending on whether or not the porous solid is consumed by the reactions, the processes are generally classified as non-catalytic or catalytic reactions, respectively [107].

Because of the continuous evolution of the pore structure, non-catalytic reaction and transportation of gases in porous materials can be more difficult to model than catalytic reaction. Water diffusion and reaction described by equation (2.3) at the bonded interface in low temperature wafer bonding belongs to the family of non-catalytic reactions because the solid is involved in the reaction. With the water diffused out the interface and more siloxane groups formed, the pores are gradually filled until the porosity reaches a critical value below which all pore space exists in the form of finite, isolated clusters. At this point, no siloxane groups are formed as no water can diffuse out, and high temperature annealing is needed to produce viscous flow of oxide to fill these dead ends. This porosity is commonly referred to as percolation threshold of solid inasmuch as it is the lowest porosity that permits percolation of a fluid through the pore space.

4.5.1 Identification of Diffusion Mechanism of Water

As water diffusion plays a crucial role in the bonding mechanism, the mechanism of water diffusion in the porous interface need to be determined. To begin, we first calculate the mean free path of water diffusion λ , which is given as follows [108],

$$\lambda = \frac{kT}{\sqrt{2}\pi d^2 P} = \frac{kT}{\sqrt{2}\pi d^2 \frac{P_{\text{sat}}}{RH}} = \frac{1.38 \times 10^{-23} * 298}{\sqrt{2} \pi (4 \times 10^{-10})^2 \times \frac{3160}{50}} \approx 9.2 \times 10^{-5} \text{m} \quad (4.2)$$

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where λ is the mean free path in m, k is the Boltzmann constant, T is the absolute temperature in K, d is the diameter of water molecule, P is the partial pressure of water in Pa, P_{sat} is the saturation vapor pressure of water in Pa, and RH is the relative humidity.

From Tong's model [9], immediately after room temperature bonding, the distance between the two bonded wafers via hydrogen bonds is around 10 Å. This separation, together with the distance due to microroughness of the bonding surface that is around 5 Å on the average, the mean pore diameter can be estimated to be around 15 Å i.e., $d_0 = 2r_0 = 1.5 \times 10^{-9}$ m. This mean pore diameter is similar to the void size in glass found in the work of Huang et al. [109] and Donnet et al. [110]. Their values are 23 Å [109] and 10 Å [110]. However, the actual average pore diameters cannot be determined directly using TEM because the bond strength after room temperature bonding is too weak to withstand the TEM sample preparation.

Also, Reznicek et al. performed comparative TEM study of bonded silicon/silicon interfaces fabricated by hydrophilic [98], hydrophobic and UHV wafer bonding, and their TEM results for hydrophilic wafer bonding at annealing temperature higher than 130°C was found to have pore diameter of size 10 Å, and it is consistent with our estimation.

With this value of average pore diameter, the Knudsen number is computed to be [111],

$$N_{\text{Kn}} = \frac{\lambda}{2r_0} = \frac{9.2 \times 10^{-5}}{1.5 \times 10^{-9}} = 61000 \gg 10 \quad (4.3)$$

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Hence, it can be concluded that the water diffusion through the bonding interface is the Knudsen diffusion [111]. The Knudsen diffusion coefficient is independent of pressure, and it is given by [111],

$$D_K = 9700 * \bar{r} \sqrt{\frac{T}{M}} \quad (4.4)$$

where D_K is the diffusivity of water in cm^2/sec , $\bar{r}$ is the mean radius of the pore in cm, T is absolute temperature in K, and M is molecular weight of water.

Since the interface is of porous in nature as described earlier, the effective diffusivity of water need to be modified as follows,

$$D_{K,e} = D_K \frac{\epsilon}{\tau} = 9700 * \bar{r} \sqrt{\frac{T}{M}} * \frac{\epsilon}{\tau} = 9700 * \sqrt{\frac{T}{M}} * \frac{\epsilon * \bar{r}}{\tau} \quad (4.5)$$

where ϵ is the porosity which is defined as the ratio of the unoccupied space over the total space available, and τ is the tortuosity factor of the porous interface.

4.5.2 Development of Diffusion Model

The diffusion model in this work is shown in Fig. 4.16 schematically. Since the thickness of the interlayer ($L \approx 2 \sim 3\text{nm}$) [98] is much less than the diameter of the wafer ($d_{\text{wafer}} = 10\text{cm}$), we can simplify this problem to one-dimension model.

The diffusion of water out of the interlayer consists of three paths, one is the diffusion along the interface to the ambient and the other two are diffusions into the two wafers. Their respective diffusion fluxes are denoted as $J_{\text{H}_2\text{O}}$, J' and J'' as shown in Fig. 4.16. Based on the law of conservation of mass, we have,

$$\begin{aligned}
& (C_{H_2O,t+\Delta t} - C_{H_2O,t})_x * 1 * L * \Delta x / \Delta t \\
& = (J_{H_2O,x,t} * 1 * L - J_{H_2O,x+\Delta x,t} * 1 * L) + R * 1 * L * \Delta x - (J'_{x,t} + J''_{x,t}) * \Delta x * 1
\end{aligned} \tag{4.6}$$

where $C_{H_2O}(t, x)$ is the water concentration at time t and location x , and R is reaction rate of the reverse reaction (2.3). Here, the width of the structure is assumed to be 1 unit.

In the case of Si-SiO₂ wafer bonding, although one Si wafer is covered by native oxide layer, which is typically about 2-10Å and has lower density than thermal oxide, it cannot hold much of the water diffused into it, which is shown by experiments of Mack's et al. [96,97]. More importantly, the water diffused through native oxide will react with the surrounding Si to form hydrogen, which will diffuse back to interface and diffuse along the interface. The overall number of gas molecules is not affected by this reaction, since in exchange for each consumed water molecule one hydrogen molecule is released. But, at the condition of temperature lower than 500°C and pressure of water is very low, the chemical reaction of water with surrounding silicon is neglectable. In the case of the thermal SiO₂ covered Si wafers, although interface wafer can also diffuse into the surrounding oxide, the diffusion coefficient is quite low. Comparison between vertical and transverse diffusion coefficients will be performed in the section 4.5.5, which will show that transverse diffusion coefficients are much higher than vertical diffusion coefficients. Moreover, vacuum effect on the diffusion of water along interface has been confirmed by experimental results of Tong et al's low vacuum wafer bonding [16] and our medium vacuum wafer bonding. Therefore, in vacuum wafer bonding, J' and J'' is neglectable, thus equation (4.6) can be simplified to,

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$$\begin{aligned} & \left(C_{H_2O,t+\Delta t} - C_{H_2O,t} \right)_{\bar{x}} * 1 * L * \Delta x / \Delta t \\ & = \left(J_{H_2O,x,t} * 1 * L - J_{H_2O,x+\Delta x,t} * 1 * L \right) + R * 1 * L * \Delta x \end{aligned} \tag{4.7}$$

From the comparison between the bond strength of air wafer bonding and vacuum wafer bonding, we found that vacuum bonding can improve the bond strength dramatically [91,92]. This implies that the vacuum wafer bonding is diffusion-control process. In other words, we may presume that the reaction rate R is much faster than water diffusion during annealing.

Figure 4.17 Postulated interface chemical structures of hydrophilic Si/Si pairs immediately after RT contacting: (a) at an associated silanol site and (b) at an isolated silanol site (Reproduced from Fig. 4.27 [9] for ease of discussion)

Since there are more than one water molecule per bonding site as shown in Figure 4.17, we can assume that one pair of bonding sites is contacted when n water

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molecules are diffused out, but at the same time, one water molecule is produced again according to reaction (2.3). In other word, one water molecule will be produced when n water molecules diffuse out during bonding within the elemental volume shown in Figure 4.15. Thus, the rate of water molecules produced by reaction (2.3) is $R \cdot 1 \cdot L \cdot \Delta x$. The rate of water diffused out of the volume is given by $(J_{H_2O, x+\Delta x, t} - J_{H_2O, x, t}) \cdot 1 \cdot L$, hence

$$\frac{R \cdot 1 \cdot L \cdot \Delta x}{(J_{H_2O, x+\Delta x, t} - J_{H_2O, x, t}) \cdot 1 \cdot L} = \frac{1}{n} \equiv \delta \quad (4.8)$$

Substitute Equation (4.8) into Equation (4.7), we have

$$\begin{aligned} & \left(C_{H_2O, t+\Delta t} - C_{H_2O, t} \right)_x \cdot 1 \cdot L \cdot \Delta x / \Delta t \\ &= (J_{H_2O, x, t} \cdot 1 \cdot L - J_{H_2O, x+\Delta x, t} \cdot 1 \cdot L) - \delta \cdot (J_{H_2O, x, t} \cdot 1 \cdot L - J_{H_2O, x+\Delta x, t} \cdot 1 \cdot L) \end{aligned} \quad (4.9)$$

Equation (4.9) may be transformed to,

$$\left(\frac{C_{H_2O, t+\Delta t} - C_{H_2O, t}}{\Delta t} \right)_x = -(1 - \delta) \left(\frac{J_{H_2O, x+\Delta x, t} - J_{H_2O, x, t}}{\Delta x} \right)_t \quad (4.10)$$

Let $\Delta x \rightarrow 0, \Delta t \rightarrow 0$, Equation (4.10) becomes

$$\frac{\partial C_{H_2O}}{\partial t} = -(1 - \delta) \frac{\partial J_{H_2O}}{\partial x} \quad (4.11)$$

But

$$J_{H_2O} = -D_{K,e} \frac{\partial C_{H_2O}}{\partial x} \quad (4.12)$$

Hence, substitute equation (4.12) into equation (4.11), we have

$$\frac{\partial C_{H_2O}}{\partial t} = D_{K,e} (1 - \delta) \frac{\partial^2 C_{H_2O}}{\partial x^2} \quad (4.13)$$

Substitute equation (4.5) into equation (4.13),

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$$\frac{\partial C_{H_2O}}{\partial t} = 9700 * \sqrt{\frac{T}{M}} * \frac{\varepsilon * \bar{r}}{\tau} (1 - \delta) \frac{\partial^2 C_{H_2O}}{\partial x^2} = D_{eff}(t) \frac{\partial^2 C_{H_2O}}{\partial x^2} \quad (4.14)$$

where

$$D_{eff}(t) = 9700 * \sqrt{\frac{T}{M}} * \frac{\varepsilon * \bar{r}}{\tau} (1 - \delta) \quad (4.15)$$

Thus, we can describe $D_{eff}(t)$ as an effective time-dependent diffusion coefficient. Intuitively, as the diffusion proceeds, ε and $\bar{r}$ decrease, τ increase, so we can assume an empirical equation for $D_{eff}(t)$, as follows,

$$D_{eff}(t) = (\eta_0 - D_{equ.})e^{-bt} + D_{equ.} \quad (4.16)$$

At $t=0$,

$$\eta_0 = D_{eff}(0) = 9700 * \sqrt{\frac{T}{M}} * \frac{\varepsilon_0 * \bar{r}_0}{\tau_0} (1 - \delta) \quad (4.17)$$

As the bonding interface becomes amorphous oxide as $t \rightarrow \infty$ [76], we can approximate $D_{equ.}$ to be the equilibrium water diffusion coefficient in silica glass [112], hence

$$D_{equ.} = 1.9 \times 10^{-4} e^{(-71/RT)} \quad (4.18)$$

with $D_{equ.}$ in cm^2/s , R is the gas constant in $\text{kJ/mol} \cdot \text{K}$, and activation energy of water diffusion is 71 kJ/mol . Then, after substituting equation (4.16) into equation (4.14), we have

$$\frac{\partial C_{H_2O}}{\partial t} = [(\eta_0 - D_{equ.})e^{-bt} + D_{equ.}] \frac{\partial^2 C_{H_2O}}{\partial x^2} \quad (4.19)$$

In heated vacuum chamber, the water concentration is extremely low, i.e., $C_{H_2O}(0, t) \approx 0$ and $C_{H_2O}(10, t) \approx 0$, hence we have the boundary conditions as follows,

Initial Condition:

$$t = 0, C_{H_2O} = C_{H_2O}^0(x, 0) \quad (4.20)$$

Boundary Condition I:

$$t > 0, x = 0 \text{ cm} \quad C_{H_2O}(0, t) = 0 \quad (4.21)$$

Boundary Condition II:

$$t > 0, x = 10 \text{ cm} \quad C_{H_2O}(10, t) = 0 \quad (4.22)$$

4.5.3 Determination of the Bond Strength

To determine the bond strength, it is reasonable to assume that the bond strength is proportional to the concentration of chemical bonds between the two interfaces [76]. Thus the strength can be expressed as a function of time, t , as follows:

$$F(t) = k_1 C_{Si-O}(t) + k_2 C_{Hydro}(t) \quad (4.23)$$

where $F(t)$ is the bond strength, k_1 is the force needed to break one Si-O-Si bond, C_{Si-O} is the concentration of Si-O-Si bonds between two wafers, k_2 is the force needed to break one hydrogen bond between two wafers, and $C_{Hydro}(t)$ is the concentration of the hydrogen bonds at the interface between the two wafers. For a reason that will be clear later, the relationship between $C_{Hydro}(t)$ and C_{H_2O} can be given by

$$\frac{C_{Hydro}}{C_{H_2O}} = \frac{1}{m} \quad (4.24)$$

During annealing, the water is diffusing out, and hence the concentration of the hydrogen bonds will be decreasing and the concentration of the Si-O-Si will be increasing. If the number of total bonding sites is assumed to be constant, we have,

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$$C_{\text{Si-O}} = n_0 - \delta C_{\text{H}_2\text{O}} \quad (4.25)$$

where n_0 is the number of initially available bonding sites per unit area, which is equal to $4.6 \times 10^{14} \text{ cm}^{-2}$ [9], and δ accounts for the fact that there are more than one water molecule per bonding site, which has been defined in Equation (4.8).

To determine the bond strength, substitute equations (4.24) and (4.25) into equation (4.23), we have

$$\begin{aligned} F(t) &= k_1 C_{\text{Si-O}} + k_2 C_{\text{Hydro}} \\ &= k_1 (n_0 - \delta C_{\text{H}_2\text{O}}) + \frac{k_2}{m} C_{\text{H}_2\text{O}} = k_1 n_0 + \left(\frac{k_2}{m} - \delta k_1 \right) C_{\text{H}_2\text{O}} \end{aligned} \quad (4.26)$$

Since the bond strength of the bonded pair is position-dependent over the wafer surface, average value of the bond strength should be used to compare with the experimental results. Hence, equation (4.26) should be written as,

$$\bar{F}(t) = k_1 n_0 + \left(\frac{k_2}{m} - \delta k_1 \right) \overline{C_{\text{H}_2\text{O}}(t)} \quad (4.27)$$

where,

$$\overline{C_{\text{H}_2\text{O}}(t)} = \frac{\int_0^{d_{\text{wafer}}} C_{\text{H}_2\text{O}}(x, t) dx}{d_{\text{wafer}}} \quad (4.28)$$

4.5.4 Determination of Parameters' values

The next step is to evaluate η_0 , D_{equ} , b , m , k_1 and k_2 . From the interface chemical structure proposed by Tong et al. as shown in Figure 4.17, at an associated silanol site (two pairs of silanol groups), there are equivalent six water molecules as well as two effective hydrogen bonds attached, and two water molecules will be produced when this associated silanol site close and polymerize to two Si-O-Si bonds via reaction (2.3). For an isolated silanol site, there are six water molecules, two

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effective hydrogen bonds attached, and one water molecule will be produced when this site close. The results are summarized in Table 4.3.

Table 4.3 Number of function groups at the interface right after room temperature bonding

Group	Number at an associated silanol site (Two pairs of silanol groups)	Number at an isolated silanol site (One pair of silanol groups)
Water Molecule Attached	6	6
Effective Hydrogen	2	2
Water Molecule Produced	2	1

Since the surface density of the associated and isolated silanol groups are $C_{\text{asso}} = 3.2 \times 10^{14} \text{ cm}^{-2}$ and $C_{\text{iso}} = 1.4 \times 10^{14} \text{ cm}^{-2}$ respectively [9], constant, “m”, in equation (4.24) can be calculated as follows,

$$\frac{C_{\text{Hydro}}}{C_{\text{H}_2\text{O}}} = \frac{1}{m} = \frac{1 \times C_{\text{asso}} + 2 \times C_{\text{iso}}}{\frac{6}{2} \times C_{\text{asso}} + 6 \times C_{\text{iso}}} = \frac{3.2 \times 10^{14} + 2 \times 1.4 \times 10^{14}}{3 \times 3.2 \times 10^{14} + 6 \times 1.4 \times 10^{14}} = \frac{1}{3} \quad (4.29)$$

where the consideration is per bonding site. The initial water concentration right after room temperature bonding at the interface can also be calculated as,

$$\begin{aligned} C_{\text{H}_2\text{O}}(0) &= C_{\text{H}_2\text{O}}(x,0) \\ &= 3C_{\text{asso}} + 6C_{\text{iso}} \\ &= 3 \times 3.2 \times 10^{14} + 6 \times 1.4 \times 10^{14} = 1.8 \times 10^{15} \text{ cm}^{-2} \end{aligned} \quad (4.30)$$

The value of δ can be computed according to our definition of δ as follows,

$$\delta = \frac{1 \times C_{\text{asso}} + 1 \times C_{\text{iso}}}{3C_{\text{asso}} + 6C_{\text{iso}}} = \frac{n_0}{C_{\text{H}_2\text{O}}(x,0)} = \frac{4.6 \times 10^{14}}{1.8 \times 10^{15}} \approx 0.26 \quad (4.31)$$

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Assuming that the pores are space not covered by silanol groups and water molecules, then according to the definition of porosity as defined earlier, the initial porosity is given as,

$$\epsilon_0 = 1 - \frac{n_0}{C_{Si}} = 1 - \frac{4.6 \times 10^{14}}{1.355 \times 10^{15}} = 0.66 \tag{4.32}$$

where C_{Si} is the Si bond density on an Si(100) surface [113].

$$r_0 = \frac{d_0}{2} = \frac{1.5 \times 10^{-9} \text{ nm}}{2} = 7.5 \times 10^{-8} \text{ cm} \tag{4.33}$$

Assume $\tau_0 = 1.57$, (the choice of this value will be explained later), with equations (4.17) and (4.18), we can obtain η_0 and $D_{\text{equ.}}$ at different temperature as shown in Table 4.4.

Table 4.4 Constants of equation 4.19 at different temperatures

Temperature (°C)	η_0 ($\times 10^{-3} \text{ cm}^2/\text{s}$)	$D_{\text{equ.}}$ (cm^2/s)	b (s^{-1})
200	1.16	2.7×10^{-11}	3.0×10^{-4}
300	1.28	6.4×10^{-11}	1.3×10^{-4}
400	1.38	5.9×10^{-10}	5.3×10^{-5}
500	1.48	2.7×10^{-9}	3.1×10^{-5}

It is found that the bond strength of the sample saturated after 800°C annealing without viscous flow at higher annealing temperature, we can consider its bond strength as F_{max} . This also means that all the bonding sites have changed to Si-O-Si bonds between two wafers at this condition [9]. From our experiment results,

$$F_{\text{max}} = k_1 n_0 = 35 \text{ MPa} \tag{4.34}$$

Then,

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$$k_1 = \frac{F_{\max}}{n_0} \quad (4.35)$$

At $t=0$, the bonding of the wafers is simply via the hydrogen bonding, hence

$$F_{\min} = F(0) = k_2 C_{\text{Hydro}} = \frac{k_2}{3} C_{\text{H}_2\text{O}}(0, x) \quad (4.36)$$

However, the bond strength at this initial condition cannot be determined as the bonded pair cannot withstand the dicing process for the sample preparation of the pull test. Instead, we can use the surface energies of the samples bonded at room temperature and 800°C to obtain the bond strength of the sample bonded at room temperature. From Tong's model [9], surface energy at room temperature ($E_{\min}$) is 60mJ/m², and surface energy at 800°C ($E_{\max}$) is 1658mJ/m², thus,

$$\frac{F_{\min}}{F_{\max}} = \frac{E_{\min}}{E_{\max}} = \frac{60}{1658} \quad (4.37)$$

Thus,

$$F_{\min} = 35 * \frac{60}{1658} = 1.27\text{MPa} \quad (4.38)$$

Hence from equation (4.36), we can compute the value of k_2 as,

$$k_2 = \frac{3F_{\min}}{C_{\text{H}_2\text{O}}(0, x)} \quad (4.39)$$

And equation (4.27) can be transformed to,

$$\begin{aligned} \bar{F}(t) &= k_1 n_0 + \left(\frac{k_2}{3} - \delta k_1 \right) \overline{C_{\text{H}_2\text{O}}(t)} \\ &= F_{\max} + \left(\frac{\frac{3F_{\min}}{C_{\text{H}_2\text{O}}(0, x)}}{3} - \frac{n_0}{C_{\text{H}_2\text{O}}(0, x)} \cdot \frac{F_{\max}}{n_0} \right) \overline{C_{\text{H}_2\text{O}}(t)} \\ &= F_{\max} + \frac{(F_{\min} - F_{\max})}{C_{\text{H}_2\text{O}}(0, x)} \cdot \overline{C_{\text{H}_2\text{O}}(t)} \\ &= 35 - \frac{(35 - 1.27)}{1.8 \times 10^{15}} \cdot \overline{C_{\text{H}_2\text{O}}(t)} \\ &= 35 - 1.87 \times 10^{-14} \overline{C_{\text{H}_2\text{O}}(t)} \end{aligned} \quad (4.40)$$

where F in MPa, $\overline{C_{H_2O}}(t)$ in cm^{-2} .

Now, let us look back at equation (4.16). The value of the constant “b” can be determined by treating it as a fitting parameter of equation (4.19) when compare its computation results with the experimental data. The experimental data for bonding at various temperatures annealed for 4 hours are used for the comparison. Table 4.4 shown the values of “b” thus obtained.

The value of the initial tortuosity factor τ_0 is set at 1.57. This is the result of many trials on the solution of the PDE. It is found that its value has a rather limited range around 1.57. Any value of τ_0 deviates from 1.57 will render the bond strength impractical regardless of the value of “b”. For smaller τ_0 , the bond strength will be exceedingly larger, and vice versa.

Now that the values of all the parameters needed are known, as shown in Table 4.4, equation (4.19) can be solved using the boundary conditions in equations (4.20) to (4.22). Then, using equation (4.40), the change of $\bar{F}(t)$ with time can be obtained. Effect of the environment water concentration on bond strength can also be studied by changing the boundary conditions (4.21) and (4.22).

4.5.5 Results and Discussions for the Model

The simulation results of the vacuum wafer bond strength vs. time at different temperature are shown in Fig. 4.18.

Figure 4.18 Simulation results of vacuum wafer bond strength after different annealing processes

From this figure, the following conclusions can be made:

(1) For a given annealing temperature, there is saturation for the bond strength.

The higher the annealing temperature, the higher the saturated bond strength;

(2) At early stage of the annealing, the rate of enhancement of the bond strength is dramatically different at different annealing temperature. Faster improvement can be seen for higher annealing temperature;

(3) The saturated bond strength can be achieved in a much shorter time under medium vacuum level as compared to that of tradition wafer bonding which always takes more than one hundred hours [9].

To validate our model, we superimpose the experimental results onto the simulation results as shown in Fig. 4.19. It can be seen that our model agrees well with the experimental results.

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Figure 4.19 Comparison of bond strength of experiments and simulation

(a)

(b)

Figure 4.20 Simulation results of effective diffusion coefficients and activation energy in different annealing processes. (a) Effective diffusion coefficient and (b) Effective activation energy

The behaviour of $F(t)$ over time can be understood from the diffusion mechanism in porous media. Fig. 4.20(a) shows the change of D_{eff} with time at

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different temperatures. Diffusion coefficient at higher temperature decreases more slowly and hence its saturation value is higher than that at lower temperature.

As can be seen in Table 4.4, since $D_{\text{equ.}} \ll \eta_0$, Equation (4.16) can be simplified to ,

$$D_{\text{eff}}(t) = (\eta_0 - D_{\text{equ.}})e^{-bt} + D_{\text{equ.}} \approx \eta_0 e^{-bt} \quad (4.41)$$

This equation resemble the Arrhenius relationship for diffusion coefficient given as,

$$D = D_0 e^{-\frac{E_a}{RT}} \quad (4.42)$$

Thus, we have

$$D_0 = \eta_0 \quad (4.43)$$

$$\frac{E_a}{RT} = bt \quad (4.44)$$

and the effective activation energy of water diffusion is

$$E_a = b * R * T * t \quad (4.45)$$

Therefore, E_a is time and temperature dependent, and it is shown in Fig. 4.20 (b). The Figure shows that the activation energy is smaller at higher annealing temperature due to the strong temperature dependence of b , and it increases as annealing time increases. Since the activation energy can be viewed as an energy barrier for diffusion that must be overcome, Fig. 4.20 (b) shows that higher annealing temperature can ease the diffusion of water and that the diffusion is becoming difficult as the annealing process proceeds. This is expected since lower porosity implies a higher energy barrier [114]. In the process of annealing, progressive closure of pores at the highly disordered porous interface as occur as a result of water out-diffusion and formation of Si-O-Si bonds, which in turn enhances the bond strength. However,

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the progressive closure of pores also decreases the porosity. Thus, the effective diffusion coefficient is decreased and the effective activation energy is increased during the annealing process.

Finally, to further verify the simplification by ignoring the diffusion into surrounding thermal oxide, the vertical time-dependent diffusion coefficients at different temperature after different time, which are calculated using Doremus’s equation [100], and the transverse diffusion coefficients of water along the interface at different temperature are shown in Table 4.5. From this table, it is evident that the vertical diffusion coefficients are at least 10^8 orders smaller than the transverse diffusion coefficients. Therefore, the simplification is acceptable.

Table 4.5 Comparison of the diffusion coefficients of vertical and transverse diffusion

D (cm ² /s)		Time (hour)				
Type	Temperature (°C)	1	2	3	4	5
Vertical	200	7.8×10^{-11}	3.9×10^{-11}	2.6×10^{-11}	1.9×10^{-11}	1.6×10^{-11}
	300	1.4×10^{-9}	7.0×10^{-10}	4.6×10^{-10}	3.5×10^{-10}	2.8×10^{-10}
	400	1.1×10^{-8}	5.3×10^{-9}	3.5×10^{-9}	2.6×10^{-9}	2.1×10^{-9}
	500	4.7×10^{-8}	2.4×10^{-8}	1.6×10^{-8}	1.2×10^{-8}	9.5×10^{-9}
Transverse	200	0.39	0.13	4.5×10^{-2}	1.5×10^{-2}	5.2×10^{-3}
	300	0.8	0.5	0.31	0.2	0.12
	400	1.14	0.94	0.78	0.64	0.53
	500	1.32	1.18	1.06	0.95	0.85

4.5.6 Application of this model

With this model, it is possible to study the effects of other wafer bonding parameters on the MVWB, e.g., vacuum level, wafer orientation and wafer size.

4.5.6.1 Effect of Vacuum level

The effect of vacuum level can be examined by looking at the effect of ambient water concentration. Fig. 4.21 shows this effect at different annealing temperature and different annealing time. It can be seen that the water concentration affects the bond strength dramatically, and this show the significance of vacuum level in improving the bond strength. However, due to the limitation of the bonder used in this work, no experimental verification can be done to verify this effect.

On the other hand, the comparison between vacuum and air bonding provides evidence to this effect to a certain extent, and the results are shown in Fig. 4.9. From the comparison, we can find that vacuum application indeed enhance bond strength significantly.

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Figure 4.21 Effect of vacuum level on bond strength (The values shown at the bottom right corner, 0, 0.1, 0.21, are relative water concentration in the vacuum chamber. It is defined as, $\frac{\text{The water concentration at certain vacuum level}}{\text{The water concentration in air}}$)

It is to be noted that in the above calculation, when the water concentration increase to a large value close to 1, the model would need to be modified since vertically diffusion of water into wafers can no longer be ignored.

4.5.6.2 Effect of crystal orientation

To find the mechanism difference between Si(100)/Oxide bonding and Si(111)/Oxide bonding, the hypothesis from Resnik et al [101] is applied to the model derived above, i.e. the difference was believed to be due to higher density of available bonding sites as a consequence of enhanced chemical oxide growth rate and its homogeneity on (111) surface. With these consideration, the changes should be

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reflected on the improvement of n_0 , which is the number of initially available bonding sites per unit area. Constants k_1 and k_2 should be the same for (111) and (100) wafer bonding, because k_1 is the force needed to break one Si-O-Si bond, and k_2 is the force needed to break one hydrogen bond between two wafers. “b” is a temperature dependent parameter and is not related to the initial structure. So, we assume it is the same for (100) and (111) bonding at the same temperature.

However, as the available bonding sites increases for (111) wafer bonding, less empty space is available at the interface layer for water diffusion, and thus porosity ϵ_0 decreases and tortuosity τ_0 increases. This results in a decrease in η_0 according to equation (4.17) and the diffusion of water is restrained. Hence, we see that with the (111) wafer orientation, the number of bonding sites increases on one hand, but the ease of wafer diffusion decreases on the other hand, making a bond strength improvement limited with the (111) wafers.

From the above discussion, one can see from equation (4.17) that only $\frac{\epsilon_0 * \bar{r}_0}{\tau_0}$ is structure dependent and not related to temperature. Thus, we can define

$$\psi_0 = \frac{\epsilon_0 * \bar{r}_0}{\tau_0} \quad (4.46)$$

Then,

$$\eta_0 = D_{\text{eff}}(0) = 9700 * \sqrt{\frac{T}{M}} * \frac{\epsilon_0 * \bar{r}_0}{\tau_0} (1 - \delta) = 9700 * \sqrt{\frac{T}{M}} * (1 - \delta) * \psi_0 \quad (4.47)$$

As we did in the derivation of the mathematical model for (100) wafer bonding, the value of the constant “ ψ_0 ” for (111) wafer bonding can be determined similarly by treating it as a fitting parameter. The experimental data for (111) bonding annealed at 200°C and 4 hours are used for the comparison. From this comparison, we

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have $\psi_0 = 1.54 \times 10^{-8}$, and the value of η_0 at different other temperatures can be computed using equation (4.48). Their values are shown in Table 4.6.

Table 4.6 Constants of equation (4.19) at different temperatures of (111) bonding

Temperature (°C)	200	300	400	500
η_0 ($\times 10^{-4} \text{ cm}^2/\text{s}$)	6.14	6.76	7.34	7.86

Then the bond strength of (111) bonding is,

$$\begin{aligned}
 \bar{F}(t)_{(111)} &= k_1 n_{0(111)} + \left(\frac{k_2}{3} - \delta k_1 \right) \overline{C_{\text{H}_2\text{O}}(t)_{(111)}} \\
 &= \frac{F_{\max(100)}}{n_{0(100)}} \cdot n_{0(111)} + \left(\frac{F_{\min(100)}}{C_{\text{H}_2\text{O}}(0, x)_{(100)}} - \frac{n_{0(100)}}{C_{\text{H}_2\text{O}}(0, x)_{(100)}} \cdot \frac{F_{\max(100)}}{n_{0(100)}} \right) \cdot \frac{\overline{C_{\text{H}_2\text{O}}(t)_{(111)}}}{C_{\text{H}_2\text{O}}(0, x)_{(111)}} \cdot C_{\text{H}_2\text{O}}(0, x)_{(111)} \\
 &= \frac{F_{\max(100)}}{n_{0(100)}} \cdot n_{0(111)} + \left(\frac{F_{\min(100)}}{C_{\text{H}_2\text{O}}(0, x)_{(100)}} - \frac{n_{0(100)}}{C_{\text{H}_2\text{O}}(0, x)_{(100)}} \cdot \frac{F_{\max(100)}}{n_{0(100)}} \right) \cdot \frac{\overline{C_{\text{H}_2\text{O}}(t)_{(111)}}}{C_{\text{H}_2\text{O}}(0, x)_{(111)}} \cdot C_{\text{H}_2\text{O}}(0, x)_{(100)} \cdot \frac{n_{0(111)}}{n_{0(100)}} \\
 &= \frac{F_{\max(100)}}{n_{0(100)}} \cdot n_{0(111)} + (F_{\min(100)} - F_{\max(100)}) \cdot \frac{\overline{C_{\text{H}_2\text{O}}(t)_{(111)}}}{C_{\text{H}_2\text{O}}(0, x)_{(111)}} \cdot \frac{n_{0(111)}}{n_{0(100)}} \\
 &= \frac{n_{0(111)}}{n_{0(100)}} \cdot \left[F_{\max(100)} + (F_{\min(100)} - F_{\max(100)}) \cdot \frac{\overline{C_{\text{H}_2\text{O}}(t)_{(111)}}}{C_{\text{H}_2\text{O}}(0, x)_{(111)}} \right]
 \end{aligned} \tag{4.48}$$

where $\frac{n_{0(111)}}{n_{0(100)}} = \frac{1.176 \times 10^{15}}{0.677 \times 10^{15}} \approx 1.737$ since the available bond densities of (111) and

(100) orientation are $1.176 \times 10^{15} \text{ cm}^{-2}$ and $0.677 \times 10^{15} \text{ cm}^{-2}$ respectively [113]. It is to be noted that the quantity of the bond density is not simply the concentration of silicon-silicon bonds in the surface plane but is a smaller one, because not all the surface silicon bonds are available as reaction sites in any given instant of time. These geometric effects, which limit the availability of reaction sites, are called steric hindrance [113].

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The simulation and experiment results for (111) wafer bonding are shown in Fig. 4.22. For comparison, the results of (100) wafer bonding are also shown in the same figure. From Fig. 4.22, it is obvious that (111) wafer bonding has higher bond strength than (100)-oriented wafer bonding as observed by Resnik et al. [101], and the trend of the experiment results and simulation results agrees well, especially at low temperature, such as 200 and 300°C. The orientation dependence of bond strength implies that the basic assumption of the wafer bonding model derived is valid. However, the simulation results are always larger than experimental results for high temperature annealing. This is due to the breakage in Si rather than at interface when the bond strength is above 25 MPa as explained earlier.

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Figure 4.22 Comparison between the bond strength of Si(100)/Oxide and Si(111)/Oxide bonding at different temperatures, 200, 300, 400 and 500°C.

4.5.6.3 Effect of Wafer Dimension

4” wafers are most commonly used in almost all the published literatures related to wafer bonding. What is the influence of the dimension of as-bonded wafers on final bonding quality? The model derived in this work could shed some light to the question as shown in Fig. 4.23.

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Figure 4.23 Simulation results of the effect of wafer dimension on bond strength.

From Fig. 4.23, we find that the wafer dimension has significant influence on the bond strength: with the same annealing process, the larger the wafer is, the lower the bond strength will be. It is easy to qualitatively understand this result from the basis of this model. When the dimension is larger, the diffusion of water to ambient needs longer time, and hence the chance for pores to close up before water diffuse out is higher. As a result, more water will be trapped in the “dead” pore (without any channel connected to ambient) in the process of annealing, rendering lower bond strength as observed.

The experiments to determine the effect of wafer dimension will be done in future.

4.5.6.4 Effect of Applied Load

This model can also be used to analyze the effect of applied load, which is shown by the experiment results in section 4.4.1. In that section, qualitative explanation was given based on the qualitative model of MVWB. From this mathematical model, the same result of the effect of applied load on bond strength still can be achieved.

When the load is applied on the bonded wafers in the process of annealing, ϵ and $\bar{r}$ decrease, τ increase, from equation 4.15, the effective time-dependent diffusion coefficient, $D_{\text{eff}}(t)$, will be decreased. Therefore, the final bond strength will be reduced. This is consistent with the experiment result.

4.5.7 Statistical Analysis of the Model

In general experiments for key parameters identification, typical approach of changing one factor at a time is used, which does not allow for factors interaction to be investigated adequately. In contrast, design and analysis of experiments can determine readily not only how each factor affects the response variable of interest, but also how each factor might interact with one another. Design of experiment (DOE) is a scientific approach that allows us to better understand a process and how the inputs affect the output. In present work, we combined DOE and our model to study MVWB.

As shown in former sections of this chapter, the mathematical model of MVWB is developed and it can predict the effects of many parameters on bond strength, e.g. annealing temperature, annealing time, wafer dimension, crystal orientation, ambient vacuum level and so on. For a given wafer size in MVWB, the 3 main parameters are annealing temperature, annealing time and crystal orientation. Actually, the reason for different crystal orientation can induce different bond strength may be ascribed to the different OH density on surface of as-bonded wafers. Therefore, we have 3 experimental factors (A: annealing temperature, B: annealing time, C: OH density) and 1 response variable (bond strength). The ranges of the factors are shown below:

A: Annealing temperature (25-500°C)

B: Annealing time (0-5 hours)

C: OH density (1.8×10^{15} - 2.65×10^{15} cm⁻²) [9]

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The DOE is performed using a commercial software (STATGRAPHIC), and the analysis of variance (ANOVA) is used. This ANOVA table is important to determine the significant variables as shown in Table 4.7. The ANOVA table partitions the variability of bond strength into various affecting factors. The statistical significant of each factor is then tested statistically by comparing the mean square against an estimate of the experimental error. In this case, 5 effects have P-values less than 0.05, indicating that they are significantly different from zero at the 95.0% confidence level. To check the significances of factors graphically, Pareto chart can be used, as shown in Fig. 4.24. The vertical line indicates a confidence limit of 95% (p-value = 0.05). If the corresponding bar of a factor exceeds the vertical line in the chart, the factor is considered significant. It can be seen that the significant 5 factors are, B, A, BB, AB and C.

Table 4.7 Analysis of Variance for Bond Strength

Source	Sum of Squares	Mean Square	F-Ratio	P-Value
A	469.711	469.711	94.86	0.0002
B	1401.85	1401.85	283.12	0.0000
C	114.005	114.005	23.02	0.0049
AA	1.87442	1.87442	0.38	0.5653
AB	152.523	152.523	30.80	0.0026
AC	12.25	12.25	2.47	0.1766
BB	377.585	377.585	76.26	0.0003
BC	26.01	26.01	5.25	0.0705
CC	0.554423	0.554423	0.11	0.7515

Standardized Pareto Chart for Bond Strength

Figure 4.24 Standardized Pareto Chart for bond strength analysis

From the statistical analysis, the corresponding empirical model equation for bond strength is shown in equation 4.49. As only 5 factors are important, equation 4.49 can be simplified to equation 4.50:

$$F = -7.17227 - 0.0256811A + 5.315B + 7.87798C - 0.0000126316A^2 - 1.618B^2 - 2.14533C^2 + 0.0104AB + 0.0173375AC + 2.4BC \tag{4.49}$$

$$F = -7.17227 - 0.0256811A + 5.315B + 7.87798C + 0.0104AB - 1.618B^2 \tag{4.50}$$

Because the as-bonded wafers were not activated by special methods, such as plasma activation, OH density should be around $1.8 \times 10^{15} \text{ cm}^{-2}$. The estimated response surface is shown in Fig. 4.25. From it, it can be seen that,

- 1) The final bond strength increase with the annealing temperature, the highest value (around 40MPa) can be achieved at 500°C;

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- 2) The saturation bond strength can be obtained within 5 hours at any annealing temperature.

These two phenomena are consistent with the experiment results.

Figure 4.25 Estimated response surface at OH density= $1.8 \times 10^{15} \text{ cm}^{-2}$

4.6 Summary

Low temperature medium vacuum wafer bonding and conventional air wafer bonding were performed. Compared with the conventional wafer bonding, MVWB can improve the bonding quality dramatically, including higher bond strength, bond efficiency and bond speed. The effects of applied load, sequence of wafers contact and vacuum application, annealing temperature, annealing time, wafer orientation on the bonding quality were investigated experimentally and explained by the qualitative mechanisms of conventional wafer bonding and MVWB.

Mathematical model of low temperature vacuum wafer bonding was derived based on the water diffusion and reaction, which has crucial impact on bond strength. The results predicted by this model agree well with the experiments results. The

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diffusion-reaction model of diffusion of water in SiO_2 , and theory of diffusion in porous media with time dependent diffusion coefficient, are combined together for the derivation of the model. The effects of annealing temperature and time on the time-dependent effective diffusion coefficient, temperature-dependent diffusion activation energy and final bond strength are all studied by this model. This model can be applied to predict the effects of annealing time, annealing temperature, ambient vacuum, wafer orientation and wafer dimension on the bond strength. Finally, DOE was used to analyze the model of MVWB and it is found that annealing time is dominant factors to determine the bond strength.

From the experiment and simulation results, it can be found that optimized conditions for MVWB are: cleaned in dilute RCA solution, contacted before being loaded into vacuum chamber, annealed at higher than 300°C for more than 4 hours and no load applied in annealing process. The higher the clean room class and higher vacuum, the better bond quality.

Chapter 5 PLASMA ACTIVATED WAFER BONDING (PAWB)

5.1 Introduction

As shown in chapter 2, many low temperature wafer bonding methods have been proposed [10,15-20,84-86]. Among them, PAWB is an outstanding low temperature wafer bonding alternative. It can enhance the bond strength significantly at low temperature [18-20]. In addition, it is chosen as a promising low temperature wafer bonding method because [76]:

- 1) Plasma treatment is compatible with IC process and is widely accepted in most fabrication facilities;
- 2) Plasma process can be well controlled by varying the time, power, flow rate as well as the partial pressure inside the chamber;
- 3) It is a cost-effective process and suitable for mass-production.

In this work, simulation is used to choose the source gases of PAWB for fabrication of partial SOI structure considered here. Ex-situ PAWB is also performed and discussed. Based on the experimental results, a mechanism of PAWB is proposed.

5.2 Source Gas of PAWB for Fabrication Partial SOI

Although a lot of source gases for PAWB have been studied, such as O₂, N₂, Ar, Ar/H₂, SF₆, SF₆/O₂, CF₄, CF₄/O₂, CHF₃, Cl₂, BCl₃/Cl₂, NH₃ or Cl₂/SF₆, O₂ and Ar are the two most commonly used gases, which are also studied in this work [18-20,115].

Oxygen plasma is especially attractive for surface pre-treatment in wafer bonding since it is known to be very efficient in removing hydrocarbon and water related species [116]. Actually, PAWB has been utilized to fabricate commercial SOI wafers, which is termed as Genesis ProcessTM [117]. But after O₂ plasma treatment, the wafer will be covered by a thermally-grown like ultra-thin oxide layer, whose thickness is about 2-5nm [83,118]. In fabrication of full SOI structure, the ultra-thin oxide layer is integrated together with the thick oxide, thus its effect can be neglected. However, in partial SOI structure, the specially designed Si window will be covered by this ultra-thin oxide layer, which is shown in Fig. 5.1 schematically. The side-effect of this layer on the partial SOI structure has not been investigated.

Figure 5.1. Schematic of the partial SOI structure fabricated by oxygen PAWB with the ultra-thin oxide layer

In this work, finite element analysis and device simulation will be used to study the effect of this ultra-thin SiO₂ layer on the thermal distribution and electrical performances of a Lateral Insulated Gate Bipolar transistor (LIGBT) fabricated on the partial SOI structure.

The effects of the ultra-thin oxide layer on the thermal distribution are simulated using a Finite Element Analysis simulator, ANSYS5.6. Two-dimensional structures are used, which are shown in Fig. 5.2 with the dimensions indicated.

Figure 5.2 Structure for the ANSYS simulation

TSUPREM-4 is used in present work to simulate the fabrication process of the partial SOI LIGBT. The output structures of TSUPREM-4 are then used by MEDICI, a popular device simulator, to obtain the results of thermal distribution, turn-on and turn-off speed and breakdown voltage. The outline dimension of LIGBT is the same as the dimension of partial SOI structure.

The simulation results of thermal distribution of ANSYS are shown in figures 5.3 and 5.4. From the comparison, we can find that there is almost no difference between the two cases, with and without the ultra-thin oxide layer. It implies that although silicon dioxide is much poorer heat conductor compared with bare silicon,

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the ultra-thin dioxide layer doesn't affect the thermal distribution because of its thickness, i.e., partial SOI structure is still capable in overcoming the self-heating problem encountered by full SOI structure. This phenomenon can also be observed in the simulation results of MEDICI. The result will be shown later.

Figure 5.3 The thermal field distribution in the partial SOI structure (without the ultra-thin oxide layer) from ANSYS simulation

Figure 5.4 The thermal field distribution in the partial SOI structure (with the ultra-thin oxide layer) from ANSYS simulation

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Figures 5.5 and 5.6 show the structure used by MEDICI to simulate LIGBT performance. Figures 5.7- 5.15 show the MEDICI simulation results. It was found that the ultra-thin oxide layer does not affect the temperature distribution as shown in Figures 5.7 and 5.8.

The switching speed of the IGBT is also not affected by the ultra-thin oxide layer as shown in Figures 5.9-5.12. Because the main factor that affect the switching speed is the presence of the oxide layer at the anode side, instead of the existence of the silicon window at the cathode side [3,4].

On the other hand, the breakdown voltage is seriously degraded (Figures 5.13- 5.15) due to the existence of the ultra-thin oxide layer. The reason of this phenomenon is that the depletion region is still constricted in the thin n -drift layer that leads to high electric fields being developed in this region and the breakdown voltage is reduced although this oxide layer is ultra-thin. Hence, it is concluded that O_2 plasma treatment is not a good choice for devices build on the partial SOI structure that requires high breakdown voltage, such as power devices. On the other hand, if breakdown voltage is not of concern, O_2 plasma treatment is a viable approach for low temperature wafer bonding.

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Figure 5.5 The structure of IGBT based on partial SOI (without the ultra-thin SiO₂ layer caused by O₂ plasma treatment)

Figure 5.6 The structure of IGBT based on partial SOI (with the ultra-thin SiO₂ layer caused by O₂ plasma treatment)

Figure 5.7 Thermal distribution in IGBT (without the ultra-thin SiO₂ layer caused by O₂ plasma treatment) by MEDICI.

Figure 5.8 Thermal distribution in IGBT (with the ultra-thin SiO₂ layer caused by O₂ plasma treatment) by MEDICI

Figure 5.9 The gate turn-on I (anode) - time curve of the IGBT (without the ultra-thin SiO₂ layer caused by O₂ plasma treatment)

Figure 5.10 the gate turn-on I (anode) - time curve of the IGBT (with the ultra-thin SiO₂ layer caused by O₂ plasma treatment)

Figure 5.11 The gate turn-off I (anode) - time curve of the IGBT (without the ultra-thin SiO_2 layer caused by O_2 plasma treatment)

Figure 5.12 The gate turn-off I (anode) - time curve of the IGBT (with the ultra-thin SiO_2 layer caused by O_2 plasma treatment)

Figure 5.13 The breakdown voltage of the IGBT (without the ultra-thin SiO₂ layer caused by O₂ plasma treatment)

Figure 5.14 The breakdown voltage of the IGBT (with the ultra-thin SiO₂ layer (5nm) caused by O₂ plasma treatment)

Figure 5.15 Relationship between breakdown voltage of the IGBT and thickness of the ultra-thin oxide layer

5.3 Experiment

There are two main kinds of technologies in PAWB, namely, the in-situ PAWB and ex-situ PAWB [119]. Just as its name implies, in-situ PAWB technology means that wafer bonding is processed in the chamber of the equipment in which the wafers are also activated by plasma. Fig. 5.16 is the sketch map of the equipment in which in-situ PAWB is processed. On the contrary, ex-situ PAWB means that the wafers are withdrawn from the chamber after plasma treatment and the bonding is performed outside the chamber.

Surface activation by particle bombardment increases the surface adhesion for high bond strength by lowering the surface barrier. During low energy bombardment, surface passivation by hydrocarbons, nitrogen and oxygen, is removed. A very clean and dust-free environment is required to bond the wafers after plasma activation

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without a renewed passivation of the surfaces. The highly reactive surfaces will be affected by absorbing particles and contaminants if brought in contact within the environmental air. Therefore, in-situ PAWB is preferred. But due to the lack of equipment, only ex-situ PAWB is performed in this work. It is believed that ex-situ PAWB is still applicable to study the mechanism of the improved bond strength due to plasma treatment.

Figure 5.16 The sketch map of the equipment for *in-situ* PAWB (from [119])

Conventional air wafer bonding and ex-situ PAWB were performed as shown in Table 5.1. As discussed in chapter 4, the two most important parameters for the study of mechanism of wafer bonding, annealing temperature and time, are the main variables in the experiment.

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After study on different combination of power (100, 200, 400W), gas flow rate (30, 60,100sccm) and treatment time (30, 60, 120 seconds), the highest bond strength was achieved under the combination of power of 200W, Ar gas flow rate of 30 sccm, and processing time of 30 seconds under a pressure at 90 mTorr. Thus, all the plasma treatment processes in present work were performed under this condition.

In order to study the effect of annealing temperature and time on PAWB, processes in group A were designed. In these processes, the wafers were bonded after plasma treatment. The bonded wafers were then annealed at different temperatures (200, 300, 400 and 500 °C) for different period (1, 2, 3, 4, 5 hours) in the oven (LENTON WHT 6/30). Thereafter, the power of the oven was switched off and the bonded pair was cooled down to room temperature naturally.

For comparison, the processes of conventional air wafer bonding are performed as group B shown in Table 5.1. They are the same as group E shown in Table 4.2.

Table 5.1 Different wafer bonding processes to study PAWB

Wafer no.			RCA Cleaning	Plasma Treatment	Air Annealing	
					°C	hour
PAWB	Group A	A1	X	X	200	1-5
		A2	X	X	300	1-5
		A3	X	X	400	1-5
		A4	X	X	500	1-5
Air Bonding	Group B	B1	X		200	1-5
		B2	X		300	1-5
		B3	X		400	1-5
		B4	X		500	1-5

Note: “X” means the process step was carried out.

5.4 Experiment Results and Discussion

5.4.1 Bond Efficiency

The SAM pictures of conventional air wafer bonding and PAWB are shown in Fig. 5.17. From the comparison, it is obvious that ex-situ PAWB induce more bubbles and the bond efficiency is lower than conventional wafer bonding. After plasma treatment, the wafer surface is highly reactive and easily absorbs particles and contaminants if it is brought in contact with the environmental air. Tong et al. [120] proved that contaminants are the main source of bubbles in wafer bonding.

Figure 5.17 Comparison between SAM pictures of conventional air bonding and ex-situ PAWB

5.4.2 Bond Strength

The bond strength of ex-situ PAWB is shown in Fig.5.18. For comparison, the bond strength of conventional air wafer bonding is shown in the same figure. From the comparison, the enhancement of bond strength after plasma treatment is apparent. The mechanism of the improved bond strength will be discussed in the following section.

Figure 5.18 Experiment results of bond strength of conventional air wafer bonding and PAWB. “P”: denotes PAWB; “A”: denotes air wafer bonding.

5.5 Mechanism of PAWB

Plasma etching and deposition are the basic tools in the fabrication of microelectronics and MEMS devices [121]. Plasma-based etching allows the attainment of both selective and anisotropic processing in subtractive steps; plasma-based deposition allows the attainment of film stoichiometry and morphology control in additive steps. In both plasma-based etching and deposition, electromagnetic energy rather than thermal energy creates energetic atoms and radicals. In addition, plasma-substrate voltage differences can be set up, thereby creating charged-particle fluxes for anisotropy control in etching and film morphology control in deposition. The presence of both highly reactive species and bombarding fluxes in plasma-based processing makes the creation of reaction paths possible for highly tailored subtractive or additive functions even at relatively low temperatures.

Although plasma deposition and etching are used for different purposes, they are based on the same principles. Figure 5.19 shows a simplified diagram of a plasma thin-film process [122]. The process is composed of three interrelated mechanisms: plasma-phase reactions, particle transport, and surface-related reactions. The feed stream of the process usually contains several complex gases. The plasma-phase chemical reactions are difficult to predict using conventional reaction mechanisms because the system is a thermodynamically nonequilibrium system having nonstoichiometric reactants. There are two types of particles in the plasma phase: charged (ions and electrons) and neutral (radicals, atoms, and molecules). They are transported to the substrate surface by different mechanisms, the former by ion acceleration and the latter by diffusion. The surface reactions are complicated by the ion bombardment, the nonstoichiometric reactants, and the surface temperature. The activation energies of the surface reactions are a function of both temperature and ion

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bombardment energy. Ion bombardment also affects the film's morphology and physical structure.

However, a detailed understanding of the relevant phenomena is lacking. Most of our knowledge in this regard is empirical and the same situation also exists in the field of PAWB. Although it is obvious that the oxygen plasma bombardment may gives rise to chemical reaction at the silicon surface since it is oxidized, the use of argon plasma also results in formation of bonded interfaces with high bond strength at low temperature, hence the chemical reaction (oxidation) doesn't seem to be the dominant mechanism of PAWB [83].

Figure 5.19 Simplified plasma thin film process

Farrens et al [18,123] believed that the enhanced removal rate of water via oxide formation is directly related to the plasma exposure. Implanted charge, oxide damage, and interface states may all contribute to increasing the oxidation rate. Among these reasons, enhanced removal rate of water for hydrophilic wafer bonding, or H₂ for hydrophobic wafer bonding due to the presence of a damaged layer are widely accepted by many [13,20,83]. For instance, Amirfeiz et al [83] suggested that plasma treatment creates a porous surface structure that enhances the diffusivity of

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water molecules from the bonded interface, and then the oxidation rate will be improved based on the chemical reaction (2.3). Gan [84] believed that the amorphous Si layer induced by plasma treatment has an open structure with a much lower density than crystalline silicon, which is very similar to the hypothesis of Amirfeiz et al [83].

Farrens et al [18,123] proposed contact bond strength modeling and low temperature oxidation kinetics modeling, such that surface charge caused by plasma treatment is a very crucial factor to impact the bond strength. Roberds [76] also proposed one electric field model, based on the Cabrera-Mott's model of low temperature oxidation. However, Amirfeiz et al [83] found no evidence to sustain this hypothesis.

Wiegand et al [118] believed that the enhanced bonding energy of plasma treated wafer pairs is not only from the chemical reaction (2.3), there are also possibly further species on plasma treated surfaces connecting both surfaces that contribute to the effective bonding energy of the bonded wafer pairs. One explanation could be the generation of peroxide species (see Fig.5.20) on the silicon surface during the plasma treatment. After bonding, two opposite peroxide groups can react to form Si-O-Si bridges and oxygen as shown in Figure5.21. Another explanation could be a reorganization of the surface layer into stable silane Si-H_x ($x=1, 2, 3$) modification as described in [118]. Also, Takagi et al [124] expected that non-stoichiometric compounds caused by plasma treatment contribute to the bond strength improvement.

Figure 5.20 Suggested peroxides on the plasma treated silicon surface

Figure 5.21 Proposed reaction of two opposite peroxide groups to Si-O-Si bridges and oxygen in the interface of the plasma treated wafer bonding pairs

From the above discussion, and together with our experiment results, the mechanism of PAWB at low temperature is proposed here, which includes the following effects:

(1) Removal of contaminants on the surface;

The first aspect of the proposed mechanism is easy to understand [118]: The passivation of the surface with contaminants and absorbates increase the surface potential barrier and avoids strong bonds. During plasma treatment, the volatile passivation of the surface is cleaned and more dangling bonds are produced which can contribute to the enhancement of the bonding energy.

(2) Increase in the amount of silanol groups;

Bond strength usually correlates to the number of siloxane bonds, which are assumed to be generated by surface silanol groups through the chemical reaction (2.3) [9]. The plasma treatment prior to bonding has been thought to increase the number of silanol groups on the surface and therefore also the number of the siloxane bonds bridges. However, Wiegand et al proved that the “amounts” of water and hydroxyl

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groups of the wafers treated by plasma are almost the same as wafers without plasma treatment [118]. And this is consistent with our contact angle measurement results.

To quantify the hydrophilicity of the wafer surface, the measurement of contact angle of DI water droplet is commonly used. On smooth surface, it is known that the surface morphology has little effect on the contact angle [125], which implies that the contact angle can be used to quantify the hydrophilicity or the density of OH groups of a hydrophilic surface. In this work, when DI water is used to measure the contact angle, the contact angle of bare silicon surface is larger than 15° and of oxide wafer is larger than 45° . On the other hand, for samples after cleaning and plasma treatment, the contact angle is down to less than 1° , which is below the sensitivity of our measuring equipment (OCA20). Therefore, Glycerol (which has larger contact angle) rather than DI water was used to measure the contact angle.

The experiment results are shown in Fig. 5.22. From the figure, we can find that RCA cleaning can improve the hydrophilicity, further plasma treatment and cleaning can only improve hydrophilicity slightly, i.e., the density of silanol groups does not increase much. This is consistent with Wiegand et al's experiment results [118]. Compared with the scale of the bond strength enhancement observed, we can conclude that the slight improvement on the density of silanol groups is not the crucial reason for the improvement of bond strength in PAWB.

On the other hand, it is well known that plasma treatment increases the surface roughness [126]. Hence the total surface area of the wafers treated by plasma should be larger than that of wafers without plasma treatment. This is shown in Fig. 5.23 schematically. Therefore, while the density of silanol groups does not change much, the total amount of silanol groups over the entire surface still can be increased due to the plasma treatment.

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Figure 5.22 Contact angle of the wafers after different processes A: Before RCA cleaning; B: After RCA cleaning; C: After plasma treatment.

Figure 5.23 Schematic of the wafer surface before (upper figure) and after plasma treatment (lower figure)

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(a) Original wafer

(b) After RCA Cleaning

(c) After Plasma Treatment

Figure 5.24 3-D pictures of wafer surface after different process taken by AFM

The AFM results of the wafer surfaces are shown in Fig. 5.24. The roughness (root mean square) of different wafer surfaces after different treatments, are 0.160, 0.161, and 0.186nm respectively and it means that plasma treatment indeed roughens the surface, but slightly.

Furthermore, we speculate that the peaks and valleys on the wafer surface will be “clef” into smaller ones by plasma. That is to say, some smaller peaks and valleys will be induced on the surface and the surface feature frequency is increased by plasma treatment even the roughness does not change much. This can be illustrated as follows.

Referring to Fig. 5.25, surfaces A and B have peaks and valleys equidistant from the mean surface centerline, i.e., both surfaces are considered statistically to have the same “roughness” based on the definitions of R_q and R_a , although surface A contains noticeably more peaks than surface B. Hence, a better way to distinguish them is to characterize each surface’s feature frequency or wavelength. For complex surfaces, it would be helpful to know also which wavelengths occur most often and impart the greatest influence to the surface’s topography. This method of characterization is called the Power Spectral Density (PSD) [76], and it is used in this work for the characterization of surface as well as R_q .

Figure 5.25 Schematic of two surfaces with the same R_q and R_a , but different power spectral density (PSD).

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The results of PSD measurement by AFM are shown in Fig. 5.26. From comparison, we find that the proportion of the small wavelength is increased after the RCA cleaning and plasma treatment, which implies that the total surface area indeed increases. Thus, the amount of the silanol groups increases, and the bond strength is improved.

(a) Original wafer

(b) After RCA Cleaning

(c) After Plasma Treatment

Figure 5.26 PSD of wafer surface after different process**(3) Improvement of the diffusivity of water and gas trapped at the interface:**

The creation of a damaged layer induced by plasma treatment is widely accepted, and it is considered to be a reason for the improvement of the bond strength at low temperature. The enhanced diffusivity of the water or gas at the interface will accelerate the reversible chemical reaction (2.3) [13,20,83]. Thus, it can enhance the bond strength.

While the above qualitative explanation is widely accepted, there is no mathematical model developed for the phenomena. In this work, a model that studies the instantaneous planar diffusion source in an infinite medium is employed to investigate the diffusion in the bonded wafers. The diffusion problem considered here can be modeled as having a finite amount of diffusant that spreads into the adjacent semi-infinite solid as shown in Fig. 5.27 schematically[127]. At $t=0$, water concentrates at the bonded interface. This amount of water will then spread into the semi-infinite porous oxide as time increase. At last, water will distribute evenly all over the oxide.

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As we learn from chapter 4, porosity has crucial influence on the diffusion coefficients, but the porosity of the layer treated by plasma is unknown in this work. So, an accurate equation to describe the diffusion coefficient cannot be obtained. In order to study the effect of the porosity on the bond strength, hypothetic diffusion coefficients, such as 10^{-9} , 10^{-10} , 10^{-11} cm²/s, are used for the solution of the Fick's second law using FEMLAB, with equation (4.27) as well as the following conditions:

The initial condition is,

$$t = 0, C(x, 0)=0, \text{ for all } x \neq 0 \quad (5.1)$$

and the boundary condition is,

$$C(\pm\infty, t) = 0 \quad (5.2)$$

The results are shown in Fig. 5.28. From this figure, we find that the diffusion coefficients are very crucial in determining the final bond strength and speed. As the diffusion coefficient increases, the final bond strength increases and bond speed becomes faster. Since plasma treatment can create porous layer, it can therefore improve the bond strength and speed of bonding.

Figure 5.27 A Schematic of the instantaneous planar diffusion model illustrating the water diffusion from interface into wafer.

Figure 5.28 Simulation result of bond strength for different water diffusion coefficients (i.e., different porosity).

(4) Enhancement of viscous flow:

Improvement in the diffusion of water can enhance the final bond strength. However, based on the conventional wafer bonding mechanism [9], the bonding energy is limited by the contact area at low temperature, hence to obtain high bonding energy, which is achieved by PAWB even at low temperature ($<400^{\circ}\text{C}$), only enhancing the diffusion of water is not sufficient.

In the mechanism of conventional wafer bonding, complete bonding is achieved via viscous flow of the surface layer at high temperature over 800°C . Thus, to achieve high bond strength at low temperature, viscous flow of the surface layer should have occurred at low temperature after PAWB treatment.

It was reported that the viscosity of SiO_2 is greatly reduced when the SiO_2 contains H_2O [128]. As we know, the damaged oxide layer by plasma treatment is porous and contains more water than it does before plasma treatment. Thus, its viscosity is lower and viscous flow can take place at low temperature. As a result, the bond strength increases as larger contact area is available now at low temperature.

Also, there are more smaller peaks and valleys appear on the surfaces after plasma treatment as can be seen from the PSD results where the proportion of the frequency components at small wavelengths increases after the RCA cleaning and plasma treatment. The presence of larger number of smaller peaks and valleys will reduce the melting point of the damaged surface layer and make the viscous flow of this layer easier at low temperature [129]. As a result, high bond strength can be achieved at low temperature using PAWB.

5.6 Summary

To achieve high bond strength at low temperature, an effective approach is to activate the wafers by plasma prior to wafer bonding. Although oxygen is the popular gas source for plasma treatment, there is one thin oxide layer covering the whole wafer surface after the oxygen plasma treatment, whose thickness is about 2-5nm. The effect of this ultra-thin oxide layer on the performance of device fabricated on this substrate was studied. It is found that the thermal field and switching speed are not affected by this thin oxide layer. On the other hand, the breakdown voltage is reduced due to the existence of the oxide layer. Therefore, O_2 plasma treatment is not a good choice if the partial SOI structure is used for the fabrication of devices that need high

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breakdown voltage, e.g. power devices. In present work, Ar is selected as plasma source gas.

Ex-situ PAWB was performed and the results were compared with conventional wafer bonding. It is found that ex-situ PAWB induce more bubbles, but higher bond strength. Bubbles are believed to be due to the re-passivation and particle contamination when the plasma treated wafer is exposed to air.

More importantly, mechanism of PAWB based on the conventional wafer bonding mechanism was proposed in this chapter. It includes four different aspects: plasma treatment prior to bonding can clean and activate the wafer surface. At the same time, it will roughen the wafer surface so that more silanol groups are produced. More importantly, plasma treatment will damage the surface to produce a porous layer that can improve the diffusivity of water and gas trapped at the interface. In addition, viscous flow of this layer can occur at low temperature as it contains water and is amorphous in nature. The creation of more smaller peaks and valleys by plasma treatment is another reason to explain the low temperature viscous flow.

Chapter 6 CONCLUSION AND FUTURE WORK

6.1 Conclusions

Wafer bonding was proposed to fabricate SOI structure. To overcome the inherent shortcomings of conventional direct wafer bonding, such as thermal induced mechanical stress in bonding of materials with different thermal expansion coefficients, undesirable changes and reactions in the case of materials and structures which are sensitive to high temperature, and the occurrence of precipitates of oxides and vacancies at the bonded interface during heat treatment, two low temperature wafer bonding methods, MVWB and PAWB, were studied in this work.

Compared with the conventional wafer bonding, it was found that MVWB can improve the bonding quality dramatically, including higher bond strength (bond strength of MVWB > 20 MPa after annealing at 300 °C for 4 hours, but the bond strength of conventional wafer bonding under same condition < 10 MPa), bond efficiency (> 90%) and bond speed (5-hour is enough to achieve saturated bond strength, 100-hour or more is needed for conventional wafer bonding). The effects of applied load, sequence of wafers contact and vacuum application, annealing temperature, annealing time, wafer orientation on the bonding quality were investigated experimentally and explained by the qualitative mechanisms of conventional wafer bonding and MVWB.

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Mathematical model of MVWB was derived based on the kinetics of water diffusion and reaction. The results predicted by this model agree well with the experiments results. The diffusion-reaction model of diffusion of water in SiO_2 , and theory of diffusion in porous media with time dependent diffusion coefficient, are combined together for the derivation of the model. The effects of annealing temperature and time on the time-dependent effective diffusion coefficient, temperature-dependent diffusion activation energy and final bond strength are studied in this model. This model can be applied to predict the effects of annealing time, annealing temperature, ambient vacuum level, wafer orientation and wafer dimension on the bond strength.

PAWB is another effective approach to get high bond strength at low temperature. In present project, Ar ex-situ PAWB was performed and the results were compared with conventional wafer bonding. It is found that ex-situ PAWB induce more bubbles, but higher bond strength ($>15\text{MPa}$). Bubbles are believed to be due to the particle contamination when the plasma treated wafers are exposed to air.

Mechanism of PAWB based on the conventional wafer bonding mechanism was proposed in this work. It includes different aspects: plasma treatment prior to bonding can clean and activate the wafer surface. At the same time, it will roughen the wafer surface so that more silanol groups are produced. More importantly, plasma treatment will damage the surface to produce a porous layer that can improve the diffusivity of water and gas trapped at the interface. In addition, viscous flow of this layer can occur at very low temperature as it contains water and amorphous in nature.

Fabrication of full SOI can be easily accomplished by MVWB and PAWB.

6.2 Future Work

In this thesis we have developed and laid the groundwork on two low temperature wafer bonding methods, MVWB and PAWB, both on technologies and mechanisms. However, it is by no means exhaustive, and from our point of view, more work still need to be further studied.

6.2.1 Modification of Model

As the model of MVWB is the first time proposed in this field, it was simplified in the derivation process. For example, empirical equation (4.16) to describe $D_{\text{eff}}(t)$ as an effective time-dependent diffusion coefficient can be further refined by adding more appropriate coefficients rather than only one constant “b” that related to bond speed and annealing temperature. Also, more experiments are needed to verify the model, such as different size wafer bonding and bonding under different vacuum level, etc.

For the model of PAWB, more experiment results are needed to determine the diffusion coefficients, which should be a time and temperature dependent value.

To investigate the two models involved, detailed study using MIT-FTIR is required. In particular, the detailed investigation of the evolution of the water trapped at the interface will be interesting for us to understand the physics better.

6.2.2 In-situ PAWB

As shown in chapter 5, ex-situ PAWB associates severe bubble problem because the highly reactive surfaces attracts particles and contaminants when they are brought in contact with the environmental air. Therefore, in-situ PAWB is preferred

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for mechanism study and actual production to increase the bond efficiency and strength.

For PAWB, a RIE-like (reactive ion etching) system is commonly used. To do in-situ PAWB, the system need to be modified so that the two poles are movable, which allow two wafers to be processed simultaneously and to be bonded in the vacuum chamber without exposing them to ambient air after plasma treatment. Figures 6.1 and 6.2 show the system designed by us.

Figure 6.1 The detailed cross-section of the chamber

Figure 6.2 The cross-section of my plasma system and the substrate holders (upper and lower)

6.2.3 Characterization Methods

Except the fabrication methods, the characterization of bonded wafer is another important aspect. For example, the stress distribution after different annealing process is crucial if the bonded wafer will be used in high temperature environment. If there is critical stress accumulated, debonding or crack will easily happen. HR-TEM is a powerful tool to study the nano-size voids at the interface. It can help us to understand the mechanism of wafer bonding deeper.

In addition, when the bonded wafer is used as electronics device substrate, the importance of electronic characterization arises. For example, it is found that there exist positive charges in BOX (buried oxide) and they change the carrier concentration at the bottom of active SOI layers which are adjacent to BOX [130]. The presence of positive charges in the interface of thermal oxides is well known [130]. Since the interface between active SOI layers and BOX is originally a thermally oxidized interface, as described in the fabrication process, the presence of positive charges is expected. Based on the principle of electrical neutralization, positive charges in BOX collect negative charges, which are electrons, at the bottom of the active SOI layers. These electrons change the total carriers in p-type SOI layers drastically and deserve detailed further study.

6.2.4 Applications

6.2.4.1 Introduction

Although wafer bonding is by no means a new technique, recently it has been gaining popular interest for a number of microprocessing applications, such as, high performance microelectronics, photonics and optoelectronics, and MEMES. The

power of wafer bonding to create layers of high quality, crystalline materials without regard to their microstructure, orientation and lattice constant means that it can open up new directions of research into design of all of these kinds of devices. Additionally, the capability of layering dissimilar materials makes it possible to integrate devices on a single chip that until now have been incompatible. MVWB can be used in MEMS for wafer level packaging, such as hermetic sealing. But among all the applications of wafer bonding, SOI has certainly provided the biggest impetus to it. Therefore, in this chapter, fabrication of SOI is focused, which includes fabrication of full and partial SOI structures.

6.2.4.2 Fabrication of Full SOI

Full SOI structure was easily attained by MVWB with high bond strength as shown in chapter 4. The process flow is quite simple, which is shown in Fig. 6.3 schematically.

Figure 6.3 Schematic of the process flow to fabricate full SOI

Using our MVWB technology (400°C, medium vacuum, 4 hours), the SOI wafers are fabricated in class 100 clean room, through the help from a semiconductor company. The C-SAM picture is shown in Fig. 6.4. It can be seen from the Figure that perfect bond quality (without voids under C-SAM) is achieved. In addition, the bond strength is higher than 20MPa and most of the cracks occur inside the wafer rather than at the bonded interface during the pull test. Therefore, from the points of bond efficiency and bond strength, our MVWB technology is suitable for mass production of thick SOI wafer.

Figure 6.4 C-SAM picture of bonded SOI wafer fabricated in high class clean room using our MVWB technology.

6.2.4.3 Fabrication of Partial SOI

The process flow of fabrication of partial SOI is shown in Fig. 6.5, which includes 4 main steps, i.e., fabrication of patterned oxide wafer, polishing of patterned oxide wafer, MVWB and polishing or Smart CutTM to obtain the appropriate

thickness of device wafer. Among them, the last two steps were discussed in the previous chapters in details, and the first two steps will be discussed below.

Figure 6.5 Schematic of the process flow to fabricate partial SOI

6.2.4.3.1 Fabrication of Patterned Oxide Wafer

The patterned wafers are fabricated at Micro-fabrication Lab (MFL), NTU. The fabrication processes of patterned substrate wafers are as same as the field oxide processes. They are shown in following Fig. 6.6. The details are shown in Appendix.

Figure 6.6 Schematic of fabrication of patterned oxide wafer

Step 1: Pad Oxide

Pad oxide is used to prevent structural stress between the nitride and the substrate. Since a very thin layer is required, dry oxidation is used.

Step 2: Nitride Deposition

This is used to prevent unwanted areas from being exposed to the oxide. Nitride deposition is done using LPCVD. A temperature ramp of 785-790-800C in the LPCVD nitride furnace from the entrance end to the rear end of the processing tube was adopted to keep the rate of deposition more or less constant.

Step 3: Active Mask for Patterned Oxide

Define the area of the patterned oxide. The mask used is clear field, where the other area will be protected by the photoresist.

Step 4: Nitride Etch

Plasma etching is used to etch away the Silicon Nitride deposited. This is for the growing of patterned oxide. Plasma nitride etch was used for this etching process to ensure an anisotropy profile. Over etching was done to ensure complete etching.

Step 5: Photoresist Strip

Dry ashing and wet and wet cleaning were used to strip off the photoresist.

Step 6: Field Oxide

Wet oxidation is used to create the patterned oxide, which form the partial oxide at substrate wafer in PSOI structure. Immediately after this step, the wafer is annealed in N₂ to release oxide-trapped charges and decrease the number of fixed charges on the oxide. The temperature of wet oxide is 950°C.

Step 7: Nitride Strip

The nitride and pad oxide layer used in the previous steps are to be removed in this step. Before performing this step, the wafers were dipped in BOE to remove oxynitride that was formed on top of the nitride. If this is not done, the oxynitride can prevent phosphoric acid from reaching the nitride. The fabricated patterned substrate wafers was prepared for wafer bonding process. The wafers are fabricated at Microfabrication Lab in NTU. The oxide thickness is about 0.885µm.

6.2.4.4 Polishing of the Patterned Oxide Wafer

In order to measure the surface of patterned substrate wafer, the surface roughness tests were performed using STYLUS PROFILOMETER Taylor-Hobson. The result is shown at Figure 6.7. Thus, the partial oxide thickness above the substrate wafer is about 0.44 μm and further polishing is needed to obtain flat surface required by next step, wafer bonding.

Figure 6.7 Surface analysis of the fabricated partial oxide wafer by stylus profilometer.

As discussed in Chapter 2, both pure mechanical polishing and chemical-mechanical-polishing (CMP) can achieve a high degree of flatness, parallelism and smoothness of Si and oxide wafers. Regarding pure mechanical polishing, it does introduce a significant subsurface damage layer of $\sim 20\ \mu\text{m}$ in depth [9], but in fabrication of partial SOI by wafer bonding, the damaged layer is on the substrate wafer and won't degrade the performance of the device on this structure. Thus, pure mechanical polishing is applicable for polishing of the patterned oxide wafer.

However, due to the lack of this polishing machine, practical polishing isn't performed in this work.

Also as discussed in chapter 2, CMP is the commonly used polishing method in wafer bonding. Three types of slurries ILD3013, the Klebosol 1501-50 and the Klebosol 30N50 pHN from Eminess Technologies Inc, might be able to accomplish this task. The study on this is still in process and the experiment will be done in the near future.

Therefore, it looks like that the polishing of the partial oxide wafer to obtain the surface for wafer bonding is not an obstacle for the fabrication of partial SOI by wafer bonding.

6.2.5 New method to Fabricate Partial SOI: Hybrid of SIMOX and Wafer Bonding

Another method to fabricate partial SOI that combines the advantages of SIMOX and wafer bonding is shown in Fig. 6.8, named hybrid of SIMOX and Wafer Bonding (HSW). To our knowledge, we are the first to propose this method. When the conventional SIMOX is used for fabricating the partial SOI structure, high-energy implantation will be needed (especially for the fabrication of power device). However, such high-energy implantation will induce severe damage to the active wafer. In our method, we need only low energy implantation because the thickness of the silicon layer over the oxide layer could be very thin and the device layer with high quality can be bonded on the handle wafer. Therefore, HSW can obtain partial SOI without damage in the device layer, and the process is also simple.

Figure 6.8 The schematic of HSW

Fabrication methods of partial SOI, as shown in Figures 6.5 and 6.8, were proposed, but experiments cannot be performed due to the of lack of equipments.

The crucial step of the fabrication method shown in Fig. 6.5 is the polishing of the surface of patterned oxide wafer. Pure mechanical polishing and CMP with special slurry should be tried in future.

The fabrication method shown in Fig. 6.8, hybrid of SIMOX and wafer bonding also deserve for further study.

Author's Publications

1. *Mathematical model of low temperature wafer bonding under medium vacuum and its application*, **W. B. Yu**, C. M. Tan, J. Wei, S. S. Deng, G. Y. Huang, IEEE Transactions on Advanced Packaging (in press).
2. *Strengthening and accelerating effect of annealing in medium vacuum on low temperature wafer bonding*, **W. B. Yu**, C. M. Tan, J. Wei, S. S. Deng, G. Y. Huang, Journal of Micromechanics and Microengineering 15, p1001-1006 (2005).
3. *Influence of applied load on wafer bonding in vacuum*, **W. B. Yu**, C. M. Tan, J. Wei, S. S. Deng and M. L. Nai, Sensors and Actuators A115, n1, p67-72 (2004).
4. *Statistical Analysis of the Model of Medium Vacuum Wafer Bonding*, **W. B. Yu**, J. Wei, C. M. Tan, G. Y. Huang, accepted by ICMAT 2005 (International Conference on Materials for Advanced Technologies, Singapore)
5. *Making Wafer Bonding Viable for Mass Production*, **W. B. Yu**, C. M. Tan, and J. Wei, Materials Research Society Meeting (2005) (in press)
6. *Influence of applied Load on Wafer Bonding in Vacuum*, **W. B. Yu**, C. M. Tan, J. Wei, S. S. Deng and M. L. Nai, International Journal of Computational Engineering Science, V4, n2, 2003, P351-354.
7. *Influence of Plasma Treatment and Cleaning on Vacuum Wafer Bonding*, **W. B. Yu**, C. M. Tan, J. Wei, S. S. Deng and M. L. Nai, Proceedings of 5th Electronics Packaging Technology Conference, IEEE, (2003), p294-297.

8. *Low Temperature Wafer Bonding in Medium Vacuum*, **W. B. Yu**, C. M. Tan, J. Wei, S. S. Deng, accepted by ASME IMECE2004 (International Mechanical Engineering Congress and Exposition)
9. *Influence of Super-thin Oxide Layer on Device Fabricated on Partial SOI Substrate*, **W. B. Yu**, C. M. Tan, G. W. Zhang, and Z. H. Gan, accepted by ICMAT 2003 (International Conference on Materials for Advanced Technologies, Singapore).
10. *Mechanism of Plasma Activated Wafer Bonding at low temperature*, **W. B. Yu**, C. M. Tan, J. Wei, S. S. Deng, in preparation (2004).

Coauthored publications in the period of study as a candidate of PhD:

11. *Low Temperature Sol-Gel intermediate layer wafer bonding*, S. S. Deng, C M Tan, J. Wei, **W. B. Yu**, S. M. L. Nai and H. Xie, Thin Solid Films (accepted).
12. *Mechanism of Sol-Gel Intermediate Layer Low Temperature Wafer Bonding*, C. M. Tan, S. S. Deng, J. Wei, **W. B. Yu**, J. Phys. D, **38**, 1308-1312 (2005).
13. *Improvement in Sol-Gel Intermediate layer wafer bonding*, S. S. Deng, C M Tan, J. Wei, **W. B. Yu**, Thin Solid Films (accepted).
14. *Low temperature silicon wafer bonding by sol-gel processing*, S. S. Deng, J Wei, C M Tan, M L Nai, **W. B. Yu**, H Xie, Inter. J. Comp. Eng. Sci. **4**, 655-658 (2003).
15. *Silicon-to-Silicon Wafer Bonding Efficiency by Sol-Gel Process*, S. S. Deng, C M Tan, J Wei, **W. B. Yu**, M L Nai, G Y Huang, 5th Electronics Packaging Technology Conference, 2003. 421-424.

16. *Low temperature wafer bonding process using sol-gel intermediate layer*, S. S. Deng, J Wei, C M Tan, **W. B. Yu**, M L Nai, H Xie, 2004 ASME MEMS/NEMS Packaging Symposium (accepted).
17. *Silicon-to-silicon wafer bonding by tempered sol-gel intermediate layer*, S. S. Deng, C. M. Tan, J. Wei and **W. B. Yu**, The 1st International Conference on Nanotechnology, 2004 (accepted)
18. *Finite element modeling of residual mechanical stress in partial SOI structure due to wafer bonding processing*, G. Y. Huang, C. M. Tan, Z. H. Gan, G. Zhang, **W. B. Yu**, Proceedings of the 11th International Symposium on the Physical and Failure Analysis of Integrated Circuits. IPFA 2004.

Appendix

Step	Process	Description
1	PAD OXIDE	Target=300(+/-50) Å SiO ₂
	Pre-clean Bench --- WB-PC-1 (Insert 2 blank thickness test monitoring wafers for PAD Oxide and Nitride thickness monitoring)	Clean Process: PC1 Strip oxide in 20:1 HF until wafer surface dewet Monitoring Wafer must have pre-clean for thermal process
	Dry oxidation at 950°C: Furnace/Process Recipe: A4 or A3/320 Process Name: PAD OX (including one blank thickness monitoring wafer)	5 min. diluted dry oxidation, 950°C 58 min. dry oxidation, 950°C 1 min. diluted dry oxidation, 950°C 20 min. anneal, N ₂ , 950°C
2	NITRIDE DEPOSITION	Spec: 1650 (+/-50) Å Si ₃ N ₄
	Pre-clean Bench --- WB-PC-1 (Insert 1 blank thickness test monitoring wafers)	Clean Process: PC1 No pre-clean within 30 min. after step #8 Monitoring Wafer must have pre-clean for thermal process
	LPCVD Silicon Nitride Furnace: C2 Process Recipe: 220 Process Name: HS-Nitride Temperature: 785-790-800°C	
3	ACTIVE MASK Mask Layer: Active 10	Mask Set: Mask CD:
	Coat Photoresist --defines the active region	Coat Track Process Program: <u>1.1</u> S1813, 1.23 µm
	Align/Expose: System:	UV Intensity: 14.0 cm ² Exposure Time: 4.2 sec
	Develop Photoresist and hardbake	Develop Track Process Program: <u>2.3</u>
4	NITRIDE ETCH	Remove Nitride in Field area for LOCOS Within 60 mins after step 3
	Plasma Nitride Etch	Etch Mode: Plasma

Appendix

	Etcher: LAM 01 Recipe Name: Nit-1 Recipe No: 100 (ensure O ₂ descum step before etching)	Step: Main Overetch RF Power: 250 250 W SF ₆ : 200 200 SCCM O ₂ : 0 0 SCCM He: 50 50 SCCM Pressure: 500 500 mTorr Elect Gap: 2.0 2.0 cm Etch Time: EP 8% (≈60 sec)
5	PR Strip	Remove photoresist
	Dry ashing Asher process program #02	O2 Ashing: Endpoint + Over etch
	Wet cleaning Etch process name: nanostrip	Nanostrip clean: 60C, 10 mins QDR 6 cycles Spin rinse dry (SRD)
6	FIELD OXIDE	Target=7200(+/-250)Å
	Pre-clean Bench --- WB-PC-1	Clean Process: PC1
	Wet oxidation at 950°C Furnace/Process Recipe: A4/430 Process Name: FIELD OX	5 min. dry Oxydation, 950°C 300 min. Pyrogenic steam, 950°C 5 min. dry Oxidation, 950°C 10 min. Anneal, 950°C
7	NITRIDE STRIP:	Target: Tox Fox)>6200Å Tox (active) <50Å
	Clean wafer in Nanostrip Wet bench: WB-MK-1	Nanostrip clean: 60°C, 10 min. QDR 6 cycles IPA Dry (or SRD Dry)
	Oxynitride Etch Bench: WB-MK-1	BOE dip: 10sec Cascade Rinse: DI water resistivity>15 MΩ SRD
	Nitride Strip Bench: WB-MK-1 -remove Nitride in hot Phosphoric Acid	Reflux in H ₃ PO ₄ , 155°C Etch Time: about 45 min. Hot DI water Rinse: 5 min. Cascade Rinse: DI water resistivity>15 MΩ
	Pad Oxide Etch Bench: WB-MK-1	BOE dip: 20 sec. (backside dewet+10 sec.) Cascade rinse: DI water resistivity>15MΩ SRD

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