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Yu, Xiaopeng

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Fully-Integrated CMOS Building Blocks for Phase-Locked Loops in the Multi-GHz Range

YU XIAOPENG

School of Electrical & Electronic Engineering

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STATEMENT OF ORIGINALITY

I hereby certify the content of this thesis is the result of work done by me and has not been submitted for higher degree to any other University or Institution.

Date

Yu Xiaopeng

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ABSTRACT

The wireless communication industry is currently experiencing a tremendous growth. For Wireless LAN applications, the IEEE 802.11 multiple standards have been widely adopted for the short-range communication in the two ISM bands of 2.45 GHz and 5.1-5.8 GHz. This results in an increasing demand for highly integrated transceivers of lower power consumption and small die sizes. The frequency synthesizer, which is usually formed by a Phase-Locked Loop (PLL), is a major and critical component of a wireless transceiver because it operates at high frequency and consumes a very large portion of the total power consumption in the transceiver. Currently, there exist several different standards of operation; thus a multi-standard frequency synthesizer is desirable for operations under different wireless systems. The performance in power consumption and channel selection of a frequency synthesizer are limited by the two most important building blocks, namely the frequency divider and voltage-controlled oscillator (VCO). The objective of this project is to design the most critical building blocks for the multi-GHz frequency synthesizers. All proposed circuits are realized on cost effective CMOS technology (0.18 μm CMOS process) rather than bipolar, SiGe and GaAs technologies. The power consumption and the operating frequency of PLL circuits will be analyzed in details. The power consumption reduction and speed enhancement are realized through novel topologies proposed for the frequency dividers, which dominate the overall power consumption and speed performance of the PLL. A 1 V 4 mW 10 GHz divide-by-2 unit is proposed by using the modified dynamic MOS Current Mode Logic structure in post-layout simulation. Two prescalers, implemented with the dynamic CMOS circuit and the imbalanced

phase switching technique are proposed to achieve lower power consumption for a higher operating frequency. The dynamic CMOS divide-by-8/9 prescaler implemented with an E-True-Single-Phase-Clock dynamic circuit achieves a lower power consumption compared to that of existing designs. Due to the limitation of the process design kit, large size RFMOS FETs were used in the implementation; the current consumption was 25 mA for an input signal frequency of 3.5 GHz. If the device width is scaled down to 2 μm, low power consumption of 1.6 mW is achieved. The prescaler implemented with large RFMOSs in the front stages using the 4-to-1 imbalance phase switching technique can work from 2 GHz to well above 4 GHz with a power consumption of 32 mW for a supply voltage of 1.8 V. A large power consumption reduction is expected if smaller RFMOSs are available in the process design kit. The GHz operation of all-stage programmable counter is first achieved in this work by proposing a new re-loadable bitcell. The measurement result shows that the all-stage programmable counter can work up to 1.8 GHz with a power consumption of 5.8 mW for a supply voltage of 1.8 V.

To achieve the multi-band operation, a VCO with a wide tuning range of 5-6 GHz and a good phase noise performance is designed. A multi-band imbalance phase switching prescaler is used to cover the 5-6 GHz and 2-3 GHz WLAN bands. Moreover, to obtain a high resolution for the output frequency channels, a GHz all-stage-programmable counter is used in the design of the programmable frequency divider. By combining with other low frequency building blocks, namely the phase frequency detector, the charge pump and the loop filter, a complete 5-6 GHz frequency synthesizer is realized to cover both the IEEE 802.11a and the HIPERLAN II standards. Post-layout simulation shows that the whole frequency synthesizer is able to work with a low power consumption of 30 mW.

Besides configured as a frequency synthesizer, a PLL is also widely used as a clock data recovery (CDR) system. In this application, the phase detector has become the most challenging block in the PLL since it has to operate at the highest frequency with the two high speed input signals. A novel full-rate linear phase detector using an *I/Q* splitter is proposed for 10 Gb/s SONET applications.

The author's publications:

Journal publications:

X. P. Yu, M. A. Do, L. Jia, J. G. Ma, K. S. Yeo, "Design of a low power wide band high resolution programmable frequency divider," *IEEE Trans. VLSI*, Volume: 13, no. 9, pp. 1098- 1103, Sep. 2005.

X. P. Yu, M. A. Do, J. G. Ma, K. S. Yeo, R. Wu and G. Q. Yan, "10Gb/s linear full-rate CMOS phase detector for clock data recovery circuit," Analog *Integrated Circuits & Signal Processing,* Volume: 45, pp. 191-196, Kluwer Academic Publishers, 2005.

X. P. Yu, M. A. Do, J. G. Ma, K. S. Yeo, R. Wu and G. Q. Yan, "Low power high speed CMOS dual-modulus prescaler design with imbalanced phase switching technique," *IEE Proc. Circuits, Devices & Systems*, Volume: 152, Issue: 2, pp. 127- 132. Apr. 2005.

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Chapter 1

Introduction

1.1 Background and motivation

Phase-Locked Loops (PLLs) are widely used in communication systems. Thus, low cost and high performance PLLs are the key components of modern highly integrated communication transceivers.

In recent years, the rapid development of wireless communications has lead to an increasing demand for low cost lower power and high performance Integrated Circuits (ICs). The typical applications of wireless communication devices include cellular phones, global positioning systems and Wireless Local Area Network (WLAN), etc. Numerous communication standards have been proposed to define and optimize certain applications. For example, for voice applications, the Global System for Mobile communication (GSM), Code Division Multiple Access (CDMA), Personal Communication Systems (PCS) and 3G communications are proposed. Different WLAN standards, such as the IEEE 802.11 a/b/g standards, HIPERLAN I/II, Bluetooth are proposed to provide various high data rate wireless applications. The operating frequencies of these communication standards range from a few hundred MHz to several GHz.

The recent rapid expansion of the wireless communication market has driven world-wide electronic and communication device providers to develop small size, low cost, and high performance mobile terminals. Until recently, the wireless transceivers are implemented using the BJT, or GaAs process [1] [2]. The recent advancement of the CMOS technology makes it possible now to design and

implement Radio Frequency Integrated Circuits (RFICs) using the low cost CMOS processes [3].

The PLL is commonly used as a frequency synthesizer as well as to stabilize the LO in wireless transceivers. From a stable reference frequency, a PLL can synthesize carriers at precise frequencies. Modern communication systems always operate at closely allocated channels at very high frequencies. Therefore, a frequency synthesizer must have an excellent frequency purity to ensure a good noise performance in the up-converted or down-converted signals.

The volume of data over the telecommunication networks has increased rapidly with the increase of the internet data traffic [4]. As the network volume increases the capacity of the transmission links which connect the network switching nodes must be also increased. The major method is to use the Wavelength Division Multiplexing (WDM) in the optical fibre. One example is the Synchronous Optical NETwork (SONET), a data communication standard which defines optical carrier levels and electrical signals for the fiber-optic based transmissions. For example, the SONET OC-192 has a transfer rate of 9953.28 Mb/s. Its full clock rate is almost 10 GHz. PLLs are also used in data communications as Clock Data Recovery (CDR) circuits. At the receiver end of the channel, the digital data has to be sampled at the same rate as that of the transmitter end. The clock is recovered from the input data stream by a PLL based recovery circuit.

In all these applications, the phase noise performance of the PLL has a great impact on the system performance. Excessive phase noise causes cross-talk in wireless communications and increases the Bit Error Rate (BER) in data communications. A synchronous system also needs a low clock skew signal for increasing throughput. Thus a high frequency low jitter and low clock skew PLL is

prerequisite.

In the design of transceivers, there is a clear trend towards a full integration of the Radio Frequency (RF) front end on a single die for the purposes of low cost and low power. However, there are many difficulties in the realization of the fully integrated multi-GHz CMOS PLLs with high performances.

The first difficulty is the operating frequency. The relatively low f_T of MOSFETs limits the maximum operating frequencies of the high frequency building blocks such as the VCO and the frequency divider in a frequency synthesizer. Furthermore, there are other challenging requirements, for example, the low phase noise performances in the CMOS technology, the smaller die size, and the full integration.

Another issue related to the high operating frequency is the power consumption. In the design of wireless communication terminals, low power consumption means long battery life, which is a major consideration in the market of consumer electronics. For example, for a wireless terminal in the turn-on state, RF front end is working al the time, while the digital baseband past is working only 5% of the turn-on duration. Therefore, most of the power consumption comes from the RF front end. A PLL in the RF front end contributes significantly to the overall power consumption. In the PLL, especially in the ultra-high speed digital circuits, i.e., the frequency divider in the frequency synthesizer and the phase detector in the CDR, the power consumption increases linearly with the increase in operating frequency. As a result, such high frequency building blocks dissipate a great portion of the total power consumption in the RF front-end.

Through the development of modern wireless communications, many standards co-exist in the similar bands, while different standards are adopted in different

regions. Therefore, a transceiver system which is able to operate over a wide band for multi-standard applications is highly desired.

1.2 Wireless LAN and CDR standards

There are many popular wireless LAN standards proposed by global and regional organizations, e.g. Institute of Electrical and Electronics Engineers (IEEE), European Telecommunication Standards Institute (ETSI). The different standards can be classified by the operating bands. For example, the IEEE 802.11b/g and the Bluetooth work at 2.4 GHz, while the HIPERLAN I/II and the IEEE 802.11a are located in the 5-6 GHz band.

The Bluetooth standard was proposed by Ericsson in 1994. It includes a system solution consisting of hardware, software and interoperability requirements. The Bluetooth wireless technology uses the globally available unlicensed ISM radio band of 2.4 GHz, from 2.4 GHz to 2.479 GHz, in 1 MHz spacing channels. It uses the Frequency-Hopping Spread-Spectrum (HFSS) technology to mitigate the effects of interference and to increase the number of bits transmitted while expanding the bandwidth. The first generation of the Bluetooth specification has a secure exchange of data up to a rate of about 1 Mbps. IEEE 802.11b emerged in 1999 and has become the most popular wireless networking standard. It also operates in the 2.4 GHz radio band and uses the Direct Sequence Spread Spectrum (DSSS) technique to disperse the data frame signal over a relatively wide (30 MHz) portion of the 2.4 GHz band [5]. As a result, the immunity to radio frequency interference is improved. The IEEE 802.11a standard operates in the 5-6 GHz band using the Orthogonal Frequency Division Multiplexing (OFDM) technique for the packet based networks. Its maximum bit rate can reach 54 Mbps. The Media

Access Control (MAC) layer in the IEEE 802.11a is an extension of the Carrier Sense Multiple Access with Collision Detection (CSMA/CD) protocol employed in wired LANs [6].

The IEEE 802.11g standard incorporates the merit of the IEEE 802.11a standard but operates in the 2.4 GHz band. It has the same modulation scheme and MAC layer as that of the IEEE 802.11a standard. By using the OFDM modulation, its data rate increases to 54 Mbps as well.

The ETSI proposed its own standards in Wireless LAN, namely the HIPERLAN. The HIPERLAN I standard supports a maximum data rate of 23.5 Mbps with a total available bandwidth of 150 MHz. HIPERLAN II increases the maximum data rate to 54 Mbps with a total available bandwidth of 455 MHz. It has a similar definition in the physical layer as that of the IEEE 802.11a standard but it supports time critical services in the MAC layer [7].

Table 1.1: WLAN standards

Standard	Carrier Frequency (GHZ)	Number of Channels	Channel Spacing (MHz)	Total Bandwidth (MHz)	Maximum Data Rate (Mbps)
IEEE 802.11a	5.150-5.350 5.725-5.825	12	20	300	54
IEEE 802.11b	2.4-2.479	11	5	79	11
IEEE 802.11g	2.4-2.479	N/A	5	79	54
Bluetooth	2.4-2.479	79	1	79	1
HIPERLAN Type II	5.15-5.35 5.470-5.725	19	20	455	54

The state of art for the time division multiplexed (TDM) bit streams in the Dense

Wavelength Division Multiplexing (DWDM) system is the 10 Gb/s SONET OC-192 standard and its European counterpart, the synchronous data hierarchy (SDH) STM-64 [4]. The standard bit rate for these two standards is 9.95328 Gb/s with the non-return-to-zero (NRZ) coding.

1.3 Thesis organization

This thesis is organized into twelve chapters. Chapter 1 provides an introduction to the problem addressed, and an outline of the thesis.

The theory, mathematical description and operation of a PLL will be discussed in Chapter 2. The existing design techniques for VCO and frequency divider are reviewed.

Chapter 3 presents two high-speed prescalers. One is dynamic divide-by-8/9 prescaler, which is based on the E-TSPC logic. By analyzing and optimizing the power consumption in the E-TSPC divide-by-2 unit, a new divide-by-2/3 unit in the prescaler design is proposed. The performance of the prescaler based on this unit is silicon verified. The other prescaler is based on an imbalanced phase switching technique. The performance of the new prescaler is silicon verified.

Chapter 4 describes a GHz digital counter and the integration of a 5-6 GHz wide band high resolution frequency divider implemented with the high speed low power digital counter. The frequency divider is able to cover both the HIPERLAN II and the IEEE 802.11a standards.

Chapter 5 analyzes the phase noise in the TSPC based frequency dividers, while the analysis of the phase noises is verified by the simulation.

In Chapter 6, a frequency synthesizer based on the new frequency divider and VCO is presented.

In Chapter 7, a new linear full rate phase detector for SONET OC-192 is proposed. It has a better linearity over a wider frequency range compared to the results reported in the literature. Finally, a new 1 V 10 GHz divide-by-2 unit is proposed. This divide-by-2 unit using a dynamic MCML inverter is able to operate at higher frequencies with a lower power consumption.

Chapter 8 provides the conclusion of this dissertation.

Chapter 2

Overview of Phase-Locked Loops

The frequency synthesizer is an essential block in multi-channel wireless transceivers. Phase-Locked Loop (PLL) based frequency synthesizers are commonly used as local oscillators (LOs) in wireless receivers to down-convert the carrier frequency to a lower Intermediate Frequency (IF), or up-convert the IF signal to the RF signal [8]. PLLs are also used in clock data recovery circuits, e. g. SONET OC-192 applications [9] [10]. In this chapter, the operation of a basic PLL and its transfer function are analyzed, and the implementation of the PLL-based frequency synthesizer is described and discussed. The role and requirements of PLLs in the application of frequency synthesizers for wireless LAN are presented. Finally, the most challenging high frequency blocks, the VCO and the frequency divider are reviewed.

2.1 Building blocks of PLLs

A PLL is a negative feedback system which operates on the excess phase of periodic signals. A general topology of a PLL is shown in Figure 2.1 [11]. It is formed by a phase detector (PD), a loop filter, and a voltage controlled oscillator (VCO). If it is used as a frequency synthesizer, a frequency divider is also added between the VCO and PD.

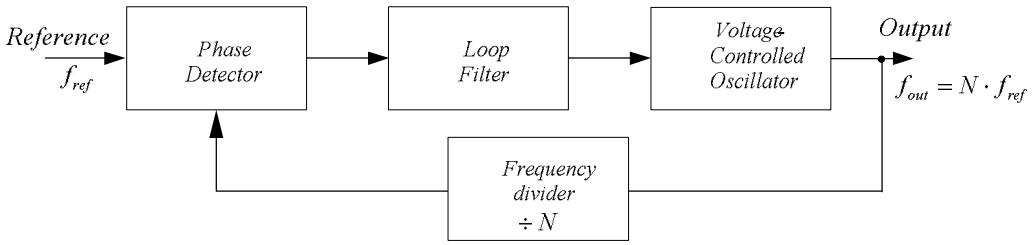


Figure 2.1: A general topology of a PLL

The phase detector compares the phase of the input reference signal and that of the oscillator's output signal or of the frequency divider's output in a frequency synthesizer. The output signal of the phase detector is a function of the phase difference between these two signals. The PD can be implemented in many methods, for example, the analog multiplier, XOR gate, Phase Frequency Detector (PFD), etc. The detailed analysis of the performance of different topologies can be found in [12]. The loop filter is usually implemented with a low pass filter that filters the output of the phase detector to produce the VCO's control voltage. In many applications, a charge pump is used before the loop filter to change the digital voltage output of the phase detector to the charging/discharging current. The filter is required to suppress the voltage ripple and to reduce the spurious tones and distortions of the RF oscillator.

The VCO produces an output signal, with an angular frequency, ω_{VCO}, which is controlled by the output voltage of the loop filter, V_{cont}, according to the following relationship:

$$\omega_{VCO}(t) = \omega_0 + K_{VCO}V_{cont} \tag{2.1}$$

where ω_0 is the center angular frequency of the VCO and K_{VCO} is the gain of the voltage-controlled oscillator. The output phase of the VCO is:

$$\theta_{VCO}(t) = K_{VCO}\int V_{cont}(t)dt \tag{2.2}$$

The frequency divider is used to extend the functionality of the loop to a frequency synthesizer. It divides the output frequency of the VCO by a ratio of *N*. In the stable condition, the output frequency of the PLL will be:

$$f_{out} = f_{ref} N \tag{2.3}$$

The division ratio, *N* can be changed to synthesize the different frequencies. If *N* is an integer, the PLL is called an integer-*N* frequency synthesizer.

The PLL is in a locked state when the phase difference at the PD output is constant with time and as a result these two input frequencies of the PD are equal. In the locked condition, all signals in the loop reach a steady state. The phase detector produces an output signal whose DC value is proportional to the phase difference of its two input signals. The loop filter suppresses the high-frequency components in the PD's output and generates a constant control voltage for the VCO. The VCO oscillates at a frequency which is equal to the reference frequency multiplied by the division ratio of the frequency divider.

If the output frequency step has to be smaller than f_{ref} , *N* can be a non-integer. Such a topology is called a fractional frequency synthesizer, which is usually used in high resolution and small channel spacing transceivers.

2.2 Linear model of PLLs

Although a PLL is normally a non-linear system because of the non-linearity of the phase detector, the VCO, and the divider, it is usually analyzed using a linear model when the loop is in a locked state [13].

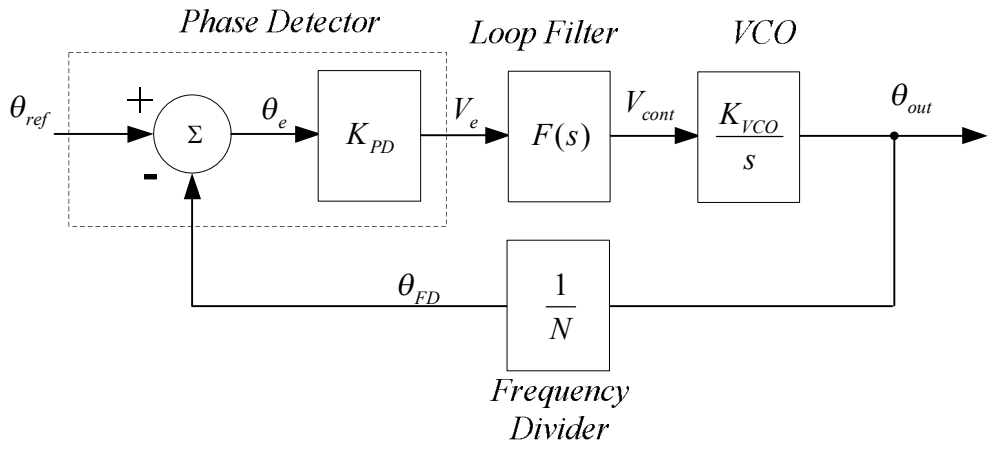


Figure 2.2: A linear model for PLL

The models for all building blocks in a PLL are summarized in Figure 2.2. For applications without a frequency divider, N is an integer with a minimum value of one. The transfer function of a PLL in S domain is given by:

$$H(s) = \frac{\theta_{out}}{\theta_{ref}} \tag{2.4}$$

where θ_{out} and θ_{ref} are the phases of the output signal and input reference signal respectively.

The phase detector produces the phase error signal which is equal to:

$$V_e(s) = K_{PD}[\theta_{ref}(s) - \theta_{FD}(s)] = K_{PD}\theta_e(s) \tag{2.5}$$

where $\theta_{FD}(s)$ and $\theta_e(s)$ are the phase signals at the frequency divider output and the phase detector output respectively while K_{PD} is the gain of the phase detector.

Consequently, the phase error signal generates the control voltage of the VCO which is given by:

$$V_{cont}(s) = V_e F(s) \tag{2.6}$$

where $F(s)$ is the transfer function of the loop filter.

The output phase is given by:

$$\theta_{out}(s) = \frac{K_{VCO} V_{cont}(s)}{s} \tag{2.7}$$

The output phase is then divided by N before it is fed back to the phase detector.

$$\theta_{FD}(s) = \frac{\theta_{out}(s)}{N} \tag{2.8}$$

Therefore, the transfer function of the PLL can be obtained:

$$H(s) = \frac{\theta_{out}(s)}{\theta_{ref}(s)} = \frac{K_{PD} K_{VCO} F(s)}{s + \frac{K_{PD} K_{VCO} F(s)}{N}} \tag{2.9}$$

By the same method, the transfer function for the phase error signal is given by:

$$\frac{\theta_e(s)}{\theta_{ref}(s)} = \frac{s}{s + \frac{K_{PD} K_{VCO} F(s)}{N}} \tag{2.10}$$

The PLL transfer function has a low-pass characteristic with a gain of N, while the phase error transfer function has a high-pass characteristic.

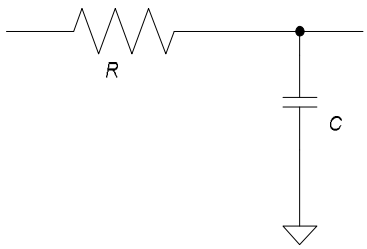


Figure 2.3: A lag RC filter

The dynamics of the PLL are decided by the transfer function of the loop filter $F(s)$. For example, if a simple lag RC filter as shown in Figure 2.3 is used, the filter will have a transfer function of:

$$F(s) = \frac{1}{(1+sRC)} \tag{2.11}$$

The transfer function of the PLL is given by:

$$H(s) = \frac{\theta_{out}(s)}{\theta_{ref}(s)} = \frac{NK_{PD}K_{VCO}}{s^2 NRC + sN + K_{PD}K_{VCO}} \tag{2.12}$$

It can be mapped to a control system with a transfer function of [12]:

$$H(s) = \frac{N\omega_n{}^2}{s^2 + 2\xi\omega_n s + \omega_n{}^2} \tag{2.13}$$

where $\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{NRC}}$ and $\xi = \frac{1}{2}\sqrt{\frac{N}{K_{PD}K_{VCO}RC}}$

ω_n and ξ are defined as the natural frequency and damping factor respectively.

This topology has limitations in the applications of PLLs. The natural frequency and the damping factor cannot be selected independently by selecting the values of R and C. Therefore, there will be a trade-off in determining these two parameters in the design of a frequency synthesizer.

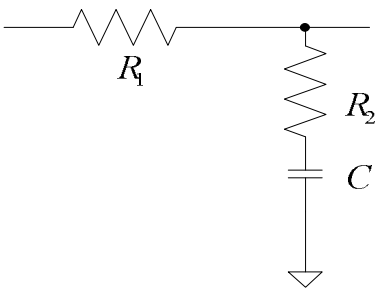


Figure 2.4: A passive lag-lead filter

If a resistor is added in series with the capacitor as Figure 2.4 shows, the transfer function of the filter changes to:

$$F(s) = \frac{1+\tau_2 s}{1+\tau_1 s} \tag{2.14}$$

where $\tau_2 = R_2 C$ and $\tau_1 = (R_1 + R_2)C$

The transfer function of the PLL is therefore:

$$H(s) = \frac{s\omega_n(2\xi - \frac{N^2\omega_n}{K_{PD}K_{VCO}}) + N\omega_n{}^2}{s^2 + 2\xi\omega_n s + \omega_n{}^2} \tag{2.15}$$

where $\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N\tau_1}}$ and $\xi = \frac{1}{2}\sqrt{\frac{K_{PD}K_{VCO}}{N\tau_1}(\tau_2 + \frac{N}{K_{PD}K_{VCO}})}$

For this topology, the natural frequency and damping factor can be determined independently.

The charge pump circuit is used to improve the performance of the PLL. The charge pump PLL has advantages compared with the traditional design. Its static phase error is zero, and the mismatch is negligible [14].

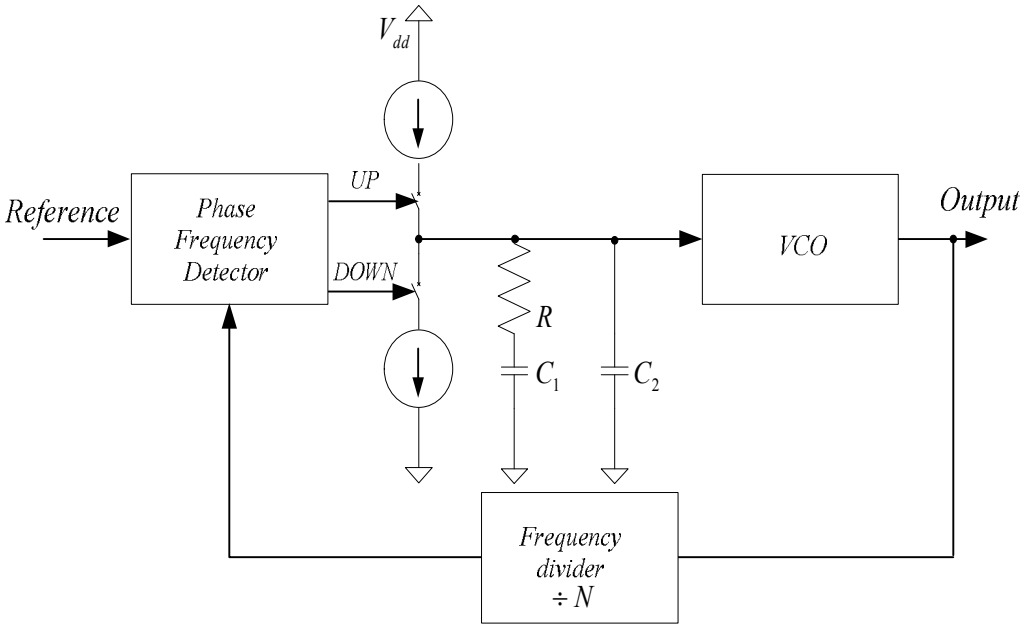


Figure 2.5: A Charge-pump PLL

Figure 2.5 shows the topology of a charge pump PLL with a 2nd order loop filter. It has been widely used for its outstanding advantages [13]. The output signals of the phase frequency detector, the *UP* and *DOWN* signals are used to drive the charge pump. The charge pump changes the control voltage of the VCO by applying positive and negative charges to the filter. The transfer function of the charge pump is given by:

$$\frac{I_d(s)}{\theta_e(s)} = \frac{I_{CP}}{2\pi} \tag{2.16}$$

where $I_d(s)$ and $\theta_e(s)$ are the Laplace transform of the average current over a cycle and of the phase difference output of the PFD, I_{CP} is the charging/discharging current.

The 2nd order loop filter has a transfer function of:

$$F(s) = \frac{1+\tau_2 s}{s(C_1+C_2)(1+\tau_1 s)} \tag{2.17}$$

where $\tau_2 = RC_2$ and $\tau_1 = \frac{C_1 C_2}{C_1 + C_2}$

Hence the transfer function of the PLL is found to be:

$$H(s) = \frac{K_{PD}K_{VCO}(\frac{1+s\tau_2}{C_1+C_2})}{s^3 + (\frac{1}{\tau_1})s^2 + (\frac{K_{PD}K_{VCO}\tau_2}{N(C_1+C_2)})s + (\frac{K_{PD}K_{VCO}\tau_2}{N(C_1+C_2)\tau_1})} \tag{2.18}$$

Approximating it with a second-order expression, the simplified transfer function is given by [15]:

$$H(s) \cong \frac{K_{PD}K_{VCO}(\frac{1+s\tau_2}{N(C_1+C_2)})}{s^2 + (\frac{K_{PD}K_{VCO}\tau_2}{N(C_1+C_2)})s} \tag{2.19}$$

The natural frequency and damping factor can be obtained:

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N(C_1+C_2)}} \text{ and } \xi = \frac{RC_2}{2}\omega_n$$

The poles are located at $-\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1}$

2.3 The performance of PLLs

The PLL is frequently used as a frequency synthesizer in the RF receiver. The design of the frequency synthesizer must follow the specifications that determine the quality of the generated signal and its effects on the received signals.

2.3.1 Tuning range and frequency resolution

The tuning range of the frequency synthesizer is usually designed to cover the operating frequency range of the selected standard taking into account the selection of the system architecture. The tuning range sets the minimum requirement for the operating range of the VCO in the frequency synthesizer. The frequency resolution of the synthesizer is normally designed according to the channel spacing of the specifications. In an integer-N PLL, the output frequency resolution is determined by the input reference frequency. The IEEE 802.11a standard has a channel spacing of 20 MHz. The center frequencies and channel spacing are listed in Table 1.1. The channel spacings and center frequencies for these standards vary even when they are located in the similar band. For example, the center frequencies of the IEEE 802.11b and Bluetooth can be expressed as (2402+k) MHz and (2412+$k\times 5$) MHz respectively, where k is an integer.

2.3.2 Phase noise

The phase noise is one of the most important parameters for the characterization of the synthesizer. The phase noise in the frequency synthesizer has a great impact over the noise performance of the RF receiver [16]. All frequency synthesizers rely on analog circuits, which introduce various types of nonidealities. The output of a PLL is not an ideal sine wave of an oscillating frequency, ω_0. A typical output spectrum of a PLL is shown in Figure 2.6:

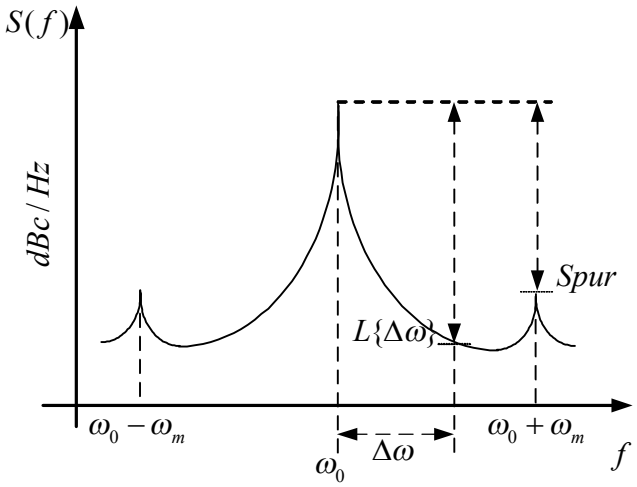


Figure 2.6: The output spectrum of a PLL

Phase noise $L\{\Delta\omega\}$ is defined as the ratio of the noise power in a bandwidth of 1 Hz at an offset frequency $\Delta\omega$ to the carrier power $P_{carrier}$. The result is a single sided spectral noise density in the unit of dBc/Hz.

$$L\{\Delta\omega\} = 10\log\frac{P_{noise}}{P_{carrier}} \tag{2.20}$$

In a PLL, the output of the VCO also has spurs. The energy is also concentrated on frequency other than the main oscillating frequency. The major sources of the ripple in the PLL are: the leakage currents in the filter and the charge-pump; the mismatch in the charge pump up and down current sources [17]. For the phase detector, the output clock is switched on and off periodically. The pull up and pull down currents in the charge pump introduce the current injection, ΔI_{CP}, which will cause ripple in the output of the VCO.

Phase noise and spurious signals affect the performance of the down-converted signal as shown in Figure 2.7 [18]. The section of the phase noise from the local oscillator noise that falls over the adjacent channel is down-converted on top of the desired signal. This output noise will degrade the signal-to-noise ratio (SNR) of the

down-converted signal. Therefore, the phase noise performance of the frequency synthesizer must be able to meet the requirement of the WLAN standards.

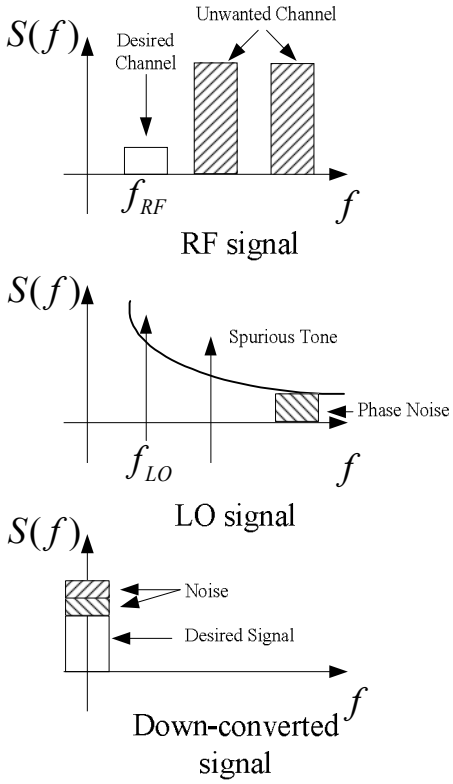


Figure 2.7: Effects of phase noise in a receiver

The requirement of the phase noise in a receiver is given by [8]:

$$L\{\Delta\omega\} < P_{sig\_\min}(dBm) - P_{blk\_\max}(dBm) - f_{BW}(dBHz) - SNR(dB) \qquad (2.21)$$

where $P_{sig\_\min}$ is the minimum received signal, $P_{blk\_\max}$ is the maximum blocking signal, f_{BW} is the bandwidth, and SNR is the minimum required SNR.

For example, in the Bluetooth applications, the phase noise in 3 MHz offset should below -116 dBc/Hz [19].

The spurious signal of the frequency synthesizer has a similar effect in the receiver's performance. Therefore, the maximum spurious level in the frequency synthesizer is given by:

$$spur\{\Delta\omega\} < P_{sig\_\min}(dBm) - P_{blk\_\max}(dBm) - SNR(dB) \quad (2.22)$$

However, the power spectrum of the spur is different from that of the phase noise. As shown in Figure 2.6, it is a pair of frequency components at a distance of $\pm f_m$ from the carrier frequency f_0.

2.3.3 Settling time

Another requirement in the design of the frequency synthesizer is the requirement of settling time. The WLAN standards define the requirement of switching between the different channels, e.g., in the HIPERLAN II, the required switching time for the change of the carrier is less than 1 ms [7].

In the frequency synthesizer, the covering of different channels is achieved by changing the division ratio of the frequency divider, for example, from the initial division ratio N to $(N+\Delta N)$ to switch to another channel. This will cause successive changes in the phase error, then in the control voltage and in the VCO's output frequency. After the feedback, the PLL settles down again. The time required for this complete procedure is called the settling time. Theoretically, the settling time is large and has an exponential behavior. Therefore, the specified output frequency error tolerance, ε, is introduced. The settling time, t_s of the PLL can be defined as:

$$t_s = \{t_s : |f_{out}(t) - f_{out}(\infty)| < \varepsilon\} \quad (2.23)$$

where $f_{out}(t)$ is the output frequency at time t, and $f_{out}(\infty)$ is the steady-state frequency of the VCO.

The analysis of the transient response can be obtained from a linear model if ΔN is much smaller than N. For example, for a simple loop filter PLL which has a transfer function of Equation 2.13, the change of the output of the PLL due to a

change of ΔN can be obtained:

$$\Delta f_{out}(\infty) = \Delta N f_{ref} \frac{(2\xi\omega_n + \omega_n^{\ 2})}{s(s^2 + s\xi\omega_n + \omega_n^{\ 2})} \tag{2.24}$$

The settling time for the new division ratio is given by:

$$t_s = \left| L^{-1}\{\Delta f_{out}(s) - \Delta f_{out}(\infty)\right| < \varepsilon \tag{2.25}$$

2.4 Voltage Controlled Oscillators

The voltage-controlled oscillator (VCO) is one of the most critical blocks in a frequency synthesizer. It mainly determines the phase noise performance of a frequency synthesizer. The performance parameters of the VCO include the tuning range, tuning linearity, output amplitude, and phase noise.

The tuning range of the VCO is determined by the application of the VCO. Some margins in the tuning range may be needed due to the process and temperature variations. The tuning linearity describes the nonlinear tuning characteristics of the VCO. Because the gain of the VCO can not be constant over the operating range, the output frequency can not change linearly with the control voltage. The output amplitude is another consideration. For less sensitivity to noise, a higher amplitude is desired. However, there will be trade-offs with the supply voltage, power dissipation and tuning range. Finally, the output signal purity, which is measured by the phase noise, is a key consideration in the application of a frequency synthesizer.

To design a VCO with good performances such as low phase noise and low power consumption, the fundamentals must be first understood. These include the basic principles of the oscillation, the relation between the power consumption and

device dimensions, effects from the quality factor of the devices specifically the LC tank and the identification of the noise source.

An oscillator can be described as a positive feedback system which amplifies its own signal at a selected frequency ω_0, as shown in Figure 2.8.

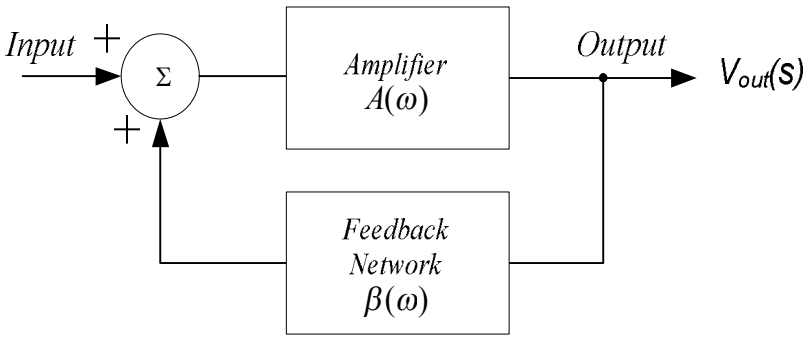


Figure 2.8: **Feedback diagram of an oscillator**

$A(\omega)$ and $\beta(\omega)$ are the gains of the amplifier and the feedback network respectively.

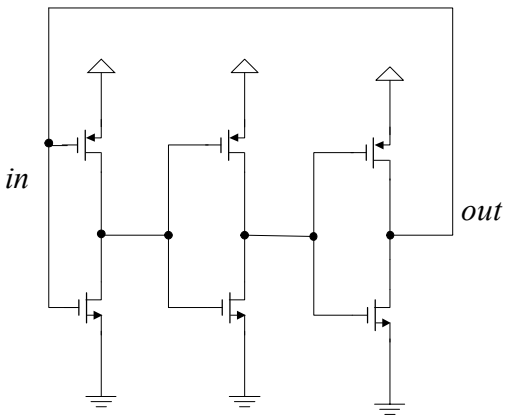
The transfer function of the oscillator is:

$$A = \frac{A(\omega)\beta(\omega)}{1 - A(\omega)\beta(\omega)} \tag{2.26}$$

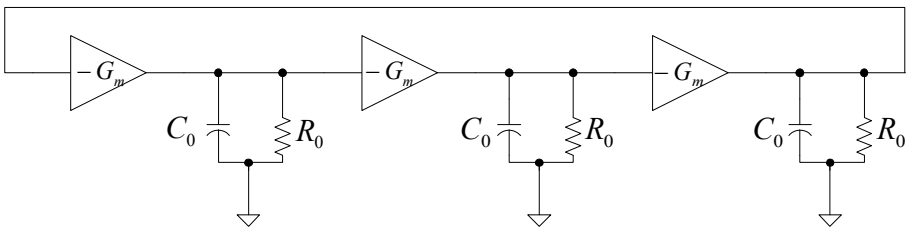
According to Barkhausen's Criteria, the system will oscillate at ω_0 when the closed loop gain approaches infinity under the following conditions: (1) the open loop gain is equal to unity, i.e. $A(\omega_0)\beta(\omega_0)=1$, and (2) the total phase shift of the loop is equal to $2\pi n$, where n is an integer or $\mathrm{Im}\{A(\omega_0)\beta(\omega_0)\} = 0$. In order to ensure the startup of the oscillation in presence temperature and process variations, the small signal loop gain is typically chosen to be 2-3 times of the required value.

2.4.1 Ring oscillators

Ring oscillators are widely used in PLL frequency synthesizers and clock recovery circuits. The implementation of the ring oscillator in the CMOS technology is easier since only transistors are required; hence a smaller silicon area is needed. Another advantage of the ring oscillator over the LC oscillator is its larger tuning range. In the ring oscillator, the Barkhausen's Criteria are achieved by the positive feedback of the output signal to the input. It is usually designed by cascading an odd number of single-ended inverters in a loop configuration as shown in Figure 2.9.a.



(a)



(b)

Figure 2.9: A three stage ring oscillator a) topology b) linear model

The tuning of the oscillator frequency can be obtained by many methods, e. g. using variable capacitors, or variable supply voltage, or the current-starved method [20]. The linear model for a ring oscillator is shown in Figure 2.9.b [21]. In this model, each stage contains a single pole with a DC gain of $-GmR_0$, the transfer function of the ring oscillator is therefore given by:

$$H(j\omega_0) = \left(\frac{-GmR_0}{1 + j\omega_0 R_0 C_0}\right)^N \tag{2.27}$$

where N is the number of the stages.

In this case, N is equal to 3. To meet the requirement of oscillation, the total phase shift is 180° and the loop gain should be equal to unity:

$$\left(\frac{-GmR_0}{1 + j\omega_0 R_0 C_0}\right)^3 = 1 \tag{2.28}$$

$$\tan^{-1}(\omega_0 R_0 C_0) = 60^0 \tag{2.29}$$

From these two equations, we can get $GmR_0 = 2$.

The oscillating frequency of the ring oscillator is decided by either the 3-dB bandwidth or the time delay of each stage [22]. For the large signal analysis, the oscillating frequency is given by:

$$f_0 \approx \frac{1}{2Nt_{delay}} \approx \frac{I}{2NC_L V_p} \tag{2.30}$$

t_{delay} is the time delay for each delay cell, I is the current passing through each delay cell, C_L is the load capacitance of each stage and V_p is the peak output voltage.

The oscillating frequency of a ring oscillator can be tuned by changing the load capacitance, equivalent resistance or transconductance of MOS transistors to change the delay since the delay of each stage is decided by the RC constant. The speed limitation of the ring oscillator is set by the transconductance to parasitic capacitance ratio. For a given supply voltage, increasing W/L of the MOS transistors to increase the transconductance can not increase the oscillating frequency significantly since the parasitic capacitances increase as well.

The ring oscillator suffers a relatively high phase noise level compared to that of the LC oscillator. The switching activities in a ring oscillator introduce a lot of disturbances in the oscillator. Moreover, the multiple stage design also has an accumulated noise level. As a result, the ring oscillator is not suitable in the high performance RF systems for its poor noise performance compared to that of the LC counterpart. A general discussion of the ring oscillator phase noise is given in [20] and the resulting phase noise is given by:

$$L(\Delta\omega) = \frac{3\Gamma^2_{rms}}{8\pi^2\Delta f^2}\frac{\overline{i^2_n}/\Delta f}{C_L{}^2 V_p{}^2} \tag{2.31}$$

Where Γ_{rms}, Δf, $\overline{i^2_n}/\Delta f$, and C_L are the root-mean square of Impulse Sensitivity Function (ISF), the offset frequency, the total noise power density and the output load capacitance respectively.

2.4.2 LC oscillators

An oscillator employing an LC tank offers a higher operating frequency and lower phase noise compared with that of a ring oscillator. Therefore, it is widely used in most modern RF systems even it requires a larger silicon area and has a smaller tuning range.

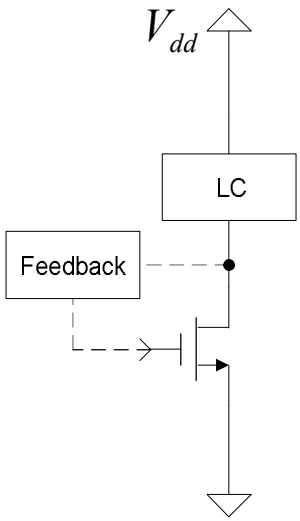


Figure 2.10: The general topology of a LC oscillator

Figure 2.10 shows the general topology for an LC oscillator. It consists of an active circuit and an LC resonator. As the LC resonator is the key block in the VCO, it is instructive to review the basic properties of RLC circuits. Figure 2.11 shows a simple model of the LC tank, both in the series combination and the parallel configuration. However, in a real circuit, due to the parasitic resistors in the inductor and capacitor, the above model is modified as in Figure 2.12.

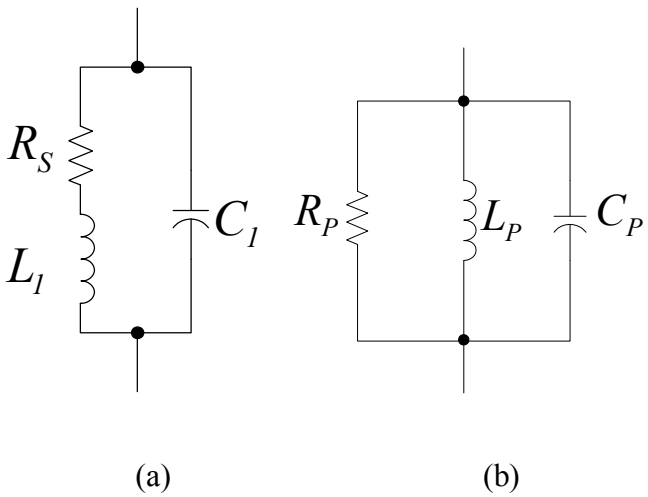


Figure 2.11: Conversion of a tank to three parallel components

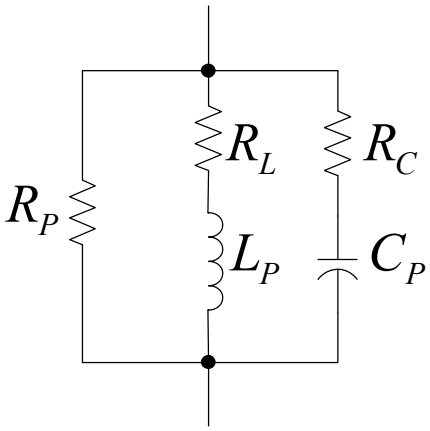


Figure 2.12: A complex model for the LC tank

At the resonant frequency, the imaginary part of the admittance of the LC tank is zero, thus the resonant frequency is given by:

$$\omega_0 = \frac{1}{\sqrt{L_P C_P}} \sqrt{1 - \frac{R_L^2 C_P}{L_P}} \tag{3.32}$$

The lossy LC-tank resonates at a lower frequency than that of the ideal tank formed by the ideal inductor and capacitor only.

The quality factor of a resonator using an inductor with a series resistor is given by:

$$Q_p = \frac{\omega L}{R} \tag{3.33}$$

For an ideal resonator, the value of R is equal to zero, and Q is infinite. In other words, the ideal resonator would not need to have active devices and no energy is needed to maintain the oscillation once the oscillation starts. However, in practice the Q of an on-chip inductor is quite low, typically from 3 to 20. The operating frequency is normally below 10 GHz. This is mainly due to their parasitic series resistance and the substrate loss [23].

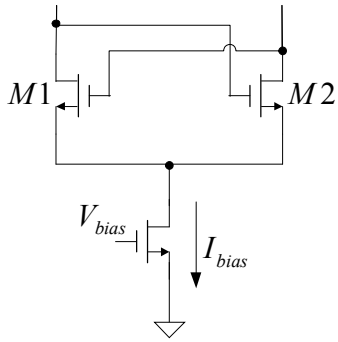


Figure 2.13: The cross-coupled structure

Due to the existance of the parasitic resistor, the energies in the capacitor and inductor are lossy and therefore, a negative resistance is needed to cancel the resistance therefore compensate the energy loss. In an LC Oscillator, the negative resistor is usually implemented by a cross-coupled differential structure as shown in Figure 2.13.

The negative resistance can is given by:

$$R = -\frac{2}{g_m} \tag{2.34}$$

where g_m is the transconductance of the transistors *M1* and *M2*.

To guarantee the oscillation, the transconductance is usually designed to be twice the required value. Hence, with enough negative resistance, the cross-coupled pair can compensate for the loss of the LC tank and maintain a stable oscillation.

Once the requirement of the transconductance has been determined, the power dissipation of the VCO can be obtained. The power consumption is given by:

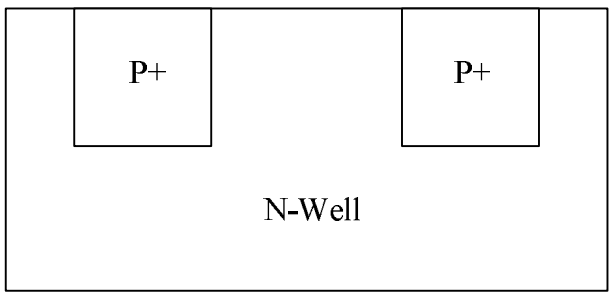
$$Power = (I_{M1} + I_{M2})V_{dd} \tag{2.35}$$

$$\text{while } I_{M1} = I_{M2} = \mu C_{ox}\frac{W}{2L}(V_{gs} - V_{th})^2 \tag{2.36}$$

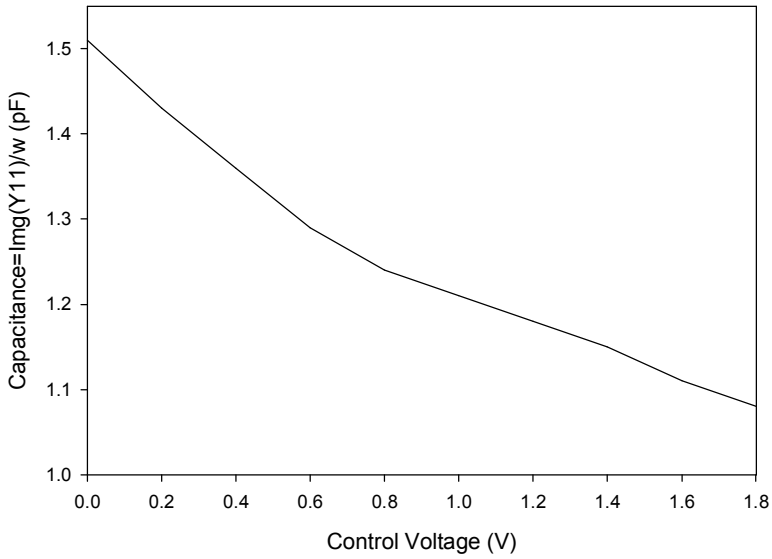
The resonant frequency of an LC oscillator is determined by the inductance and capacitance of the LC tank. Therefore, the tuning of the oscillating frequency can be carried out by changing the inductance or capacitance. Varactors are widely used as voltage-controlled variable capacitors. If a larger tuning range of the output frequency is required, a larger tuning ratio of the capacitance of the varactor is needed. There are several varactor options for the frequency tuning, such as PN-junction varactors, inversion mode varactors and accumulation mode varactors.

The PN-junction varactor

The PN-junction varactor is formed by the P+ diffusion on an N-Well as shown in Figure 2.14.a. Figure 2.14.b shows the simulation result of the C-V curve based on the Chartered Semiconductor Manufacturing (CSM) model for the 0.18 µm CMOS technology [24]. The PN-junction should be reverse-biased. The PN-junction varactor cannot be optimized to achieve both a large tuning range and high quality factor [25].



(a)

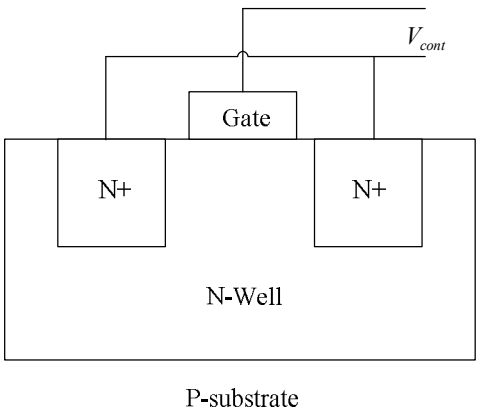


(b)

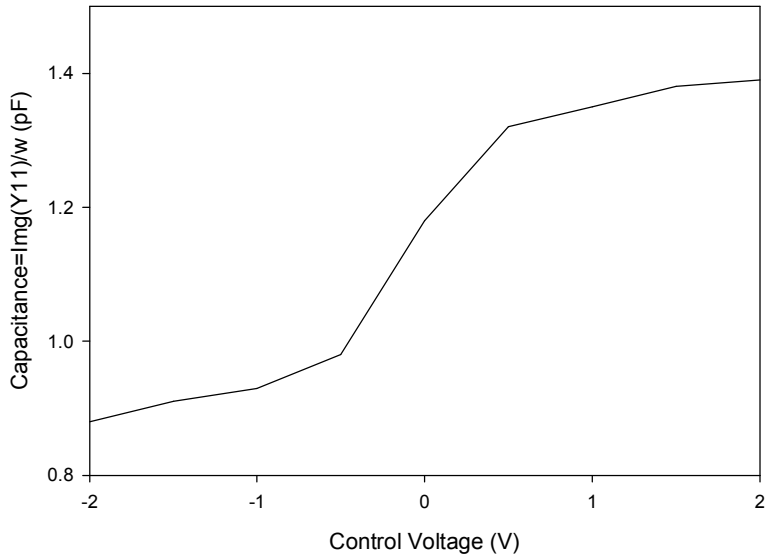
Figure 2.14: PN-junction varactor a) structure b) capacitance over voltage

The Accumulation-mode varactor

In a standard CMOS process, typical PN-junction varactors have very low Q values. The A-MOS varactor is implemented by using a P-channel MOSFET in a P-well/substrate or an n-Channel MOSFET in an N-well.



(a)



(b)

Figure 2.15: Accumulation-mode varactor a) structure b) capacitance over voltage

Figure 2.15 shows the varactor based on the NMOS transistor where the drain and source are connected together. By varying the gate-to-well voltage from a positive voltage above the flatband voltage to a negative value, the device goes from the deep accumulation region to the deep depletion region while the capacitance of the varactor drops. The accumulated charge on the surface of the silicon decreases with the drop of *Vg* until it reaches the flatband voltage. If *Vg* is less than the flatband voltage, the surface of the device undergoes the depletion. As a result, an additional capacitance is formed in series with the oxide capacitance which causes a decrease of the overall capacitance. The A-MOS varactor's Q varies significantly its tuning range due to the variation of its resistance value. However, even with the large variation of Q, in the worst case, the Q of an A-MOS varactor is still better than that of the PN-junction varactor. To achieve a better Q, more gate fingers should be used and the gate length should be minimized. The A-MOS

varactor is however less linear over the tuning voltage than the PN-junction varactor. As a result, the gain of the VCO using the A-MOS varactor is more non-linear [26].

Inductors

The inductor is a key element in determining the performance of an LC oscillator. The on-chip spiral inductor is constructed based on the lithography, where the geometry of coils is well-controlled. There are several topologies of the spiral inductor available, for example, square, hexagonal and circular. The square spiral inductor has been widely used for its easy layout. However, it has larger loss compared with the circular spiral inductor. Figure 2.16 shows a typical geometrical layout of a spiral inductor using the top metal layer and returning to outside through the underpass metal layer. The design parameters of an inductor are given by the number of turns (n), the metal width (w), the metal to metal spacing (s), the inner-hole diameter (d_{in}) and the outer diameter (d_{out}).

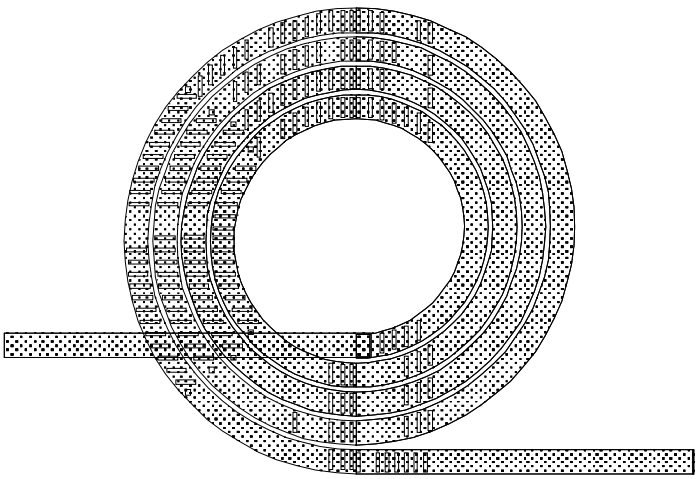


Figure 2.16: Geometry of a spiral inductor

The lumped element model is widely used to simulate the performance of an inductor [27] [28]. A typical π-equivalent model is shown in Figure 2.17.

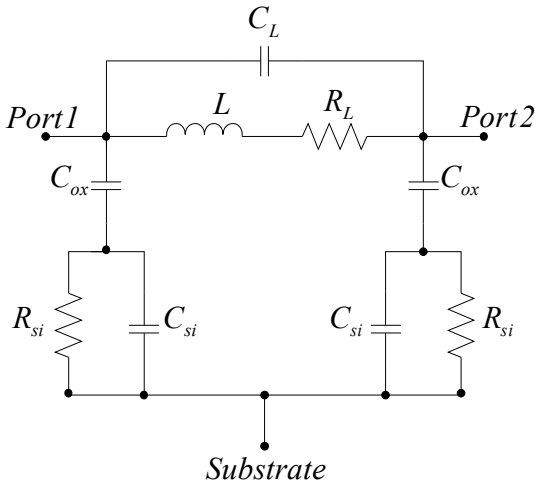


Figure 2.17: The lump element model of an on-chip inductor

It consists of nine components, where L is the total inductance produced by the metal winding and mutual coupling, R_L is the total loss of the inductor, C_{ox} is the capacitance between inductor and substrate, R_s and C_s are the parasitic resistance and capacitance of the substrate.

The total inductance of the spiral inductor is the sum of the self-inductance and the mutual-inductance [29]. It is given as:

$$L_{total} = L_{self} + M_{+} - M_{-} \tag{2.37}$$

where L_{self} is the total sum of the self-inductance of all conductor segments, M_{+} and M_{-} are the inductances due to positive and negative coupling between conductors respectively.

The mutual inductance is introduced by the magnetic coupling between the conductors. The same direction of the current flow results a positive coupling,

otherwise, a negative coupling is introduced. The detailed calculation of the mutual inductance is summarized in [30].

The efficiency of an inductor is defined by the Q, which is given by [31]:

$$Q = 2\pi \frac{energy\ stored}{energy\ lost\ \ per\ cycle} \tag{2.38}$$

Equation 2.38 defines the energy stored in the LC tank and provides an indication of how much energy is lost as it is being transferred between the capacitor and the inductor. The energy stored in the LC tank is actually the sum of the average magnetic and electric energies. However, for a silicon spiral inductor, only the energy stored in the magnetic field is of interest. Any energy stored in the form of electric field by the parasitic capacitance is counterproductive [32]. Hence, Q is proportional to the net magnetic energy stored, which is equal to the difference between the peak magnetic and electric energies:

$$Q = 2\pi \frac{Peak\ Magnetic\ Energy - Peak\ Electric\ Energy}{Energy\ Loss\ Per\ Cycle} \tag{2.39}$$

The detailed analysis about the on-chip spiral inductor can be found in [24] [30].

In a standard CMOS technology, the quality factor of the on-chip inductor is generally smaller than that of the capacitor. Therefore, the quality factor of an LC-tank is crucial to VCO designs.

2.4.3 Noise performance of an oscillator

The figure of merit for the noise performance of an oscillator is the phase noise which measures the short-term frequency stability of an oscillator. It is defined as [20]:

$$L(\Delta\omega) = 10\log\frac{P_{sideband}(\omega_0 + \Delta\omega)}{P_{carrier}} \tag{2.40}$$

where $P_{carrier}$ and $P_{sideband}(\omega_0 + \Delta\omega)$ are power of the carrier and the total power in a 1-Hz bandwidth at an offset of $\Delta\omega$ from ω_0 respectively. The unit is dBc/Hz where dBc indicates a measurement in dB relative to the carrier power.

In the design of an oscillator, the noise sources can affect both the amplitude and phase of the output signal. But the amplitude noise can be reduced by the amplitude limiting mechanism in the oscillator [20]. Therefore, amplitude noise is usually negligible. Phase noise can be regarded as the fluctuation of the zero crossing locations of a signal. The detailed explanation of this fluctuation can be found at [20]. The phase noise output is caused by both internal and external sources. The internal noise is the main source, which is caused by the noise of the oscillator's active elements, and the up-conversion of the baseband noise to the oscillator band. The external VCO noise includes the substrate coupling of unwanted signals, power supply fluctuations due the switching activity of digital/analog circuits. Noise coupled onto the control voltage applied across the varactor of the LC-tank varies the tank capacitance and hence the resonant frequency. This can be viewed as the frequency modulation (FM) noise mechanism which translates the low-frequency noise to the oscillating frequency. These phase noises on the VCO control line can expressed as a narrow-band FM which is given by [33]:

$$L(f_m) = 10\log(\frac{P_{noise}}{P_{carrier}}) = 10\log[\frac{(K_{VCO}V_{cont})^2}{2\Delta f^2}] \tag{2.41}$$

From this equation, it is observed that phase noise contribution from the control PLL output can be minimized by reducing the VCO's gain.

Because the amplitude of phase noise is small compared with the magnitude of the carrier signal, phase noise is approximated as a linear function of frequency. For example, a simple Linear Time Invariant (LTI) model can be expressed as [20]:

$$L(\Delta\omega) = 10\log[\frac{2kT}{P_{sig}}(\frac{\omega_0}{2Q\Delta\omega})^2] \tag{2.42}$$

where k is the Boltzman's constant, T is the absolute temperature, P_{sig} is the average power dissipated in the resistive part of the tank, ω_0 is the oscillation frequency, Q is the effective quality factor, and $\Delta\omega$ is the offset frequency from the carrier. This simple model only includes noise associated with the LC tank loss noise originating in the $\frac{1}{(\Delta\omega)^2}$ region and the noise floor contributions at a large frequency offset are not included. In the Leeson's formula, several nonlinear effects are added to the final noise expression. Leeson's formula is given by [20]:

$$L(\Delta\omega) = 10\log[\frac{2FkT}{P_{sig}}(1+(\frac{\omega_0}{2Q\Delta\omega})^2)(1+\frac{\omega_{1/f}^{\ 3}}{|\Delta\omega|})] \tag{2.43}$$

where F is an empirical parameter, and $\omega_{1/f}$ is the frequency of the corner between the $1/f^3$ and $1/f^2$. This model of phase noise of the oscillator is shown in Figure 2.18.

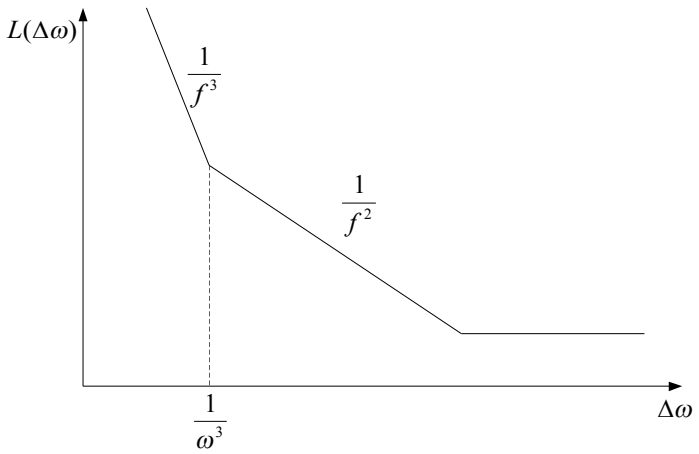


Figure 2.18: The spectrum of the phase noise

The Leeson's equation can be extended include the noise contributions [33] [34] [35]:

$$L(f_m) = 10\log[\frac{2FkT}{P_{sig}}(\frac{f_0}{2Qf_m})^2(1+\frac{f_{1/f}}{f_m}) + \frac{|Ks_{VCO}|^2}{2f^2{}_m}S_{VCNT} + \frac{|Ks_{Vdd}|^2}{2f^2{}_m}S_{Vdd} + \frac{|Ks_{bias}|^2}{2f^2{}_m}S_{bias})] \quad (2.44)$$

where S_{VCNT}, S_{vdd} and S_{bias} are the noise spectral densities of the control voltage, supply voltage and bias current respectively. Ks_{VCO}, Ks_{Vdd} and Ks_{bias} are the sensitivities of the oscillation frequency to the control voltage, supply voltage and bias current respectively.

The main limitations of the LTI noise model lie in that it is unable to predict the upconversion of the baseband noise to the VCO oscillation band, the effect of noise folding, and the cyclostationary nature of the active device noise. The Hajimiri model is proposed to solve these issues [20]. It is based on the Impulse Sensitivity Function (ISF). If an impulse charge is introduced into the capacitance of the output node of an oscillator in its steady state, amplitude and phase error will be generated. The amplitude error can be limited while the phase error can not be

attenuated. The phase error is the function of the time τ when the charge is injected. Therefore, the unit impulse response for the excess phase is given by:

$$h_{\phi}(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{\max}} u(t-\tau) \tag{2.45}$$

where $\Gamma(\omega_0\tau)$ is the ISF, $q_{\max}$ is the maximum charge which represents the oscillation amplitude, and $u(t-\tau)$ is the unit step. The ISF represents the dependence of the phase disturbance on the time at which the disturbance charge is injected. It is a function of the oscillator waveform, which reflects different system nonlinearities. The signal power of the phase noise caused by the charge injection can be expressed as:

$$S_n(\Delta\omega) = \frac{\Gamma^2{}_{rms}}{q^2{}_{\max}} \cdot \frac{\overline{i^2{}_n} / \Delta f}{4 \cdot \Delta\omega^2} \tag{2.46}$$

where $\Gamma^2{}_{rms}$ is the mean square value of the ISF and $i^2{}_n / \Delta f$ is the input noise source power spectral density. The ISF of each node should be derived for the sum of phase noise.

2.5 High Speed Frequency Dividers

The most challenging circuits in a PLL are the VCO and the frequency divider. The operating frequency of the VCO using the existing CMOS technologies can be in the multi-GHz range or even higher than 10 GHz [36] [37]. Such a high operating frequency requires a high speed frequency divider to accomplish the frequency synthesis. The analog frequency dividers have been used as an effective way to reduce the power consumption and to increase the operating frequency [38] [39]. However, the requirement of the channel selection in the frequency

synthesizer demands a programmable frequency divider. The limited bandwidth and division ratio are the inevitable drawbacks of the analog frequency divider in the implementation of the frequency synthesizer. Therefore, in the design of the high speed frequency synthesizer, especially for wideband or multi-band applications, the digital frequency divider is preferred. Because of its complex topology, the power consumption of the programmable frequency divider will be a great portion of the total power consumption in the frequency synthesizer. In this project, the low-power consumption will be the major consideration.

2.5.1 The implementation of frequency dividers

Cascaded divide-by-2 frequency dividers

The simplest way for implementing a frequency divider is to use cascaded divide-by-2 units. It has the highest operating frequency compared with other architectures since the critical path in the frequency division can be kept the shortest. However, the division ratio will be limited as the power of 2. For example, in [38], by placing a divide-by-2 unit before the prescaler, the overall division ratio of the frequency divider will be a multiple of 2. This will set a limitation on the programmable division ratio. To overcome this limitation, in [40], the phase switching technique is first proposed which can provide both even and odd division ratios even the divide-by-2 stages are used at the input of the frequency divider by switching between the different phase signals in the divide-by-2 units.

Reloadable digital counters

The reloadable digital counter is able to provide a frequency division ratio continuously ranging from 3 to 2^N, where N is the number of divide-by-2 stages. It can be used as a programmable frequency divider directly. In a reloadable digital counter, the number of the input pulses is accumulated until it is equal to a preset value when the counter is re-loaded. By changing the preset value, a programmable division ratio is achieved. Thus, in principle, the reloadable digital counter is most suitable to perform the programmable frequency division for a frequency synthesizer. However, the counter has a poor performance in the operating frequency and power consumption because it uses the additional logic gates besides the divide-by-2 units which introduce additional power consumption and propagation delays. Therefore, the reloadable digital counter is usually limited to the applications at low operating frequencies.

Pulse swallow integer frequency dividers

The most common method to form a high frequency programmable frequency division while maintaining a low power consumption is to use a pulse swallow integer frequency divider as shown in Figure 2.19 [8]. It combines a dual-modulus prescaler and two programmable counters. The advantage of this topology lies in the reduction of the operating frequency of the programmable counter while performing a programmable division ratio of $N \times P + S$, where N, P, and S are the division ratios of the prescaler, the programmable counter (P counter) and the swallow counter (S counter) respectively. In this divider, a dual-modulus prescaler, which is able to perform the dual division ratios of $N/N+1$, is employed. The implementation of the dual-modulus prescaler can be based on the synchronous

divider, e.g., the divide-by-4/5 or divide-by-2/3 cell, or the phase switching technique [40].

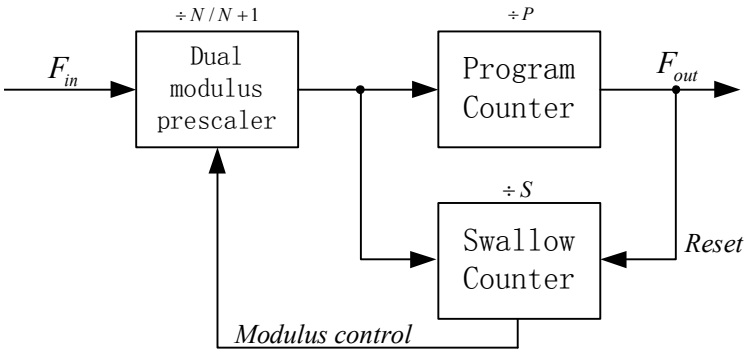


Figure 2.19: The pulse swallow integer frequency divider

Fractional-N frequency dividers

The integer frequency divider only provides the frequency division ratio equal to an integer, while the fractional-N frequency divider can provide a fractional division ratio. Figure 2.20 shows the block diagram of a fractional-N frequency divider. It consists of a dual-modulus prescaler and an accumulator. The fractional division is obtained by switching between the division value of N and (N+1). For instance, in order to achieve a divide-by-(N + *1/2*), a division by (N + *1*) is done after every division by N. Thus, the carry of the accumulator follows in the sequence of {010101…}, if the division by (N + 1) corresponds to a "1". Unfortunately, this technique generates unwanted low-frequency spurs due to the fixed pattern of the dual-modulus division. Many methods such as the Sigma-Delta modulator, ADC, phase interpolation technique, and pulse generation technique have been used to solve the problem [41][42][43]. However, such techniques require many additional blocks. In this project of multi-GHz Wireless LAN applications with large channel spacing, the integer-N frequency synthesizers are more practical and efficient [38].

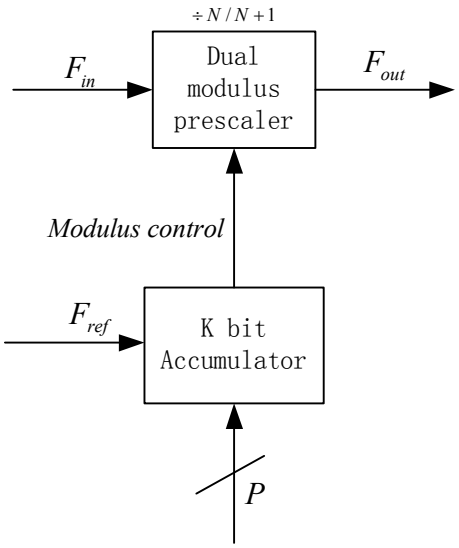


Figure 2.20: The fractional frequency divider

2.5.2 High speed digital circuits

In the design of high speed digital circuits, the operating frequency and power consumption are the key considerations. There are two major types of logic circuits, namely MOS Current Mode Logic (MCML) and CMOS dynamic circuits. In this section, the detailed analysis of the operating frequency and the power consumption in such types of logic circuits will be presented.

MCML

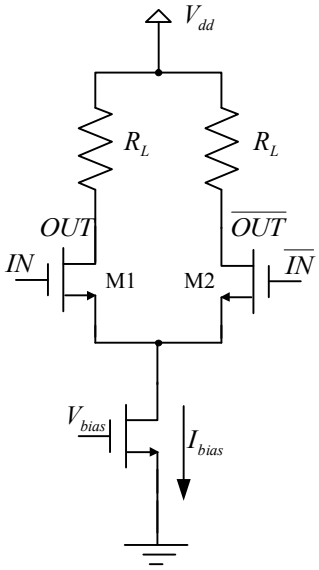


Figure 2.21: MCML inverter

MCML circuits are widely used in the mixed signal circuit design. Figure 2.21 shows a MCML inverter. Its operation is based on the differential input pair *M1* and *M2*. For example, if V_{gs} of *M1* is larger than V_{gs} of *M2*, the current passing through *M1* will larger than that of the *M2*. Therefore, the node *OUT* will be pulled down, until in the state where the two drain currents in *M1* and *M2* are equal. At the same time, $\overline{OUT}$ is pulled up through the load resistor. The voltage difference between these two nodes is defined as the output voltage swing, which is given by $I_{bias}R_L$, where the I_{bias} and R_L are the biasing current and load resistance respectively. At this state, the output voltages of the node *OUT* and the node $\overline{OUT}$ are $V_{dd} - I_{bias}R_L$ and V_{dd} respectively. Because of the differential topology, the noise performance of the MCML circuit is better than that of the single-ended logic circuit. Moreover, because of the low input and output voltage swing, the operating speed is also improved in the MCML circuit. However, the MCML circuit has a fixed biasing current which results in a higher power consumption

than that of the CMOS dynamic logic which only dissipates the power during charging and discharging. The application of the MCML circuits in VLSI designs has a complex design cycle and uses a large silicon area.

The propagation delay is defined as the delay between 50% transition points of the input and output waveforms. The propagation delay time is given as [44]:

$$t_p = \left[-\frac{d[A(s)/ds]}{A(s)} \right]_{s=0} \tag{2.47}$$

where t_p is the propagation delay, *A(s)* is the transfer function of the circuit.

From the view point of the digital circuit design, the propagation delay can be analyzed based on the time constant. In the MCML circuit, it is also based on the pull-up and pull-down network which can be expressed as a simple first order RC response. Therefore, the propagation delay is given by [45]:

$$D_{MCML} = C_L R_L = \frac{C_L \Delta V}{I_{bias}} \tag{2.48}$$

Where C_L and ΔV are the load capacitance and the output voltage swing respectively.

The power consumption of the MCML circuit is given by:

$$Power_{MCML} = V_{dd} I_{bias} \tag{2.49}$$

There is a trade-off between the power consumption and the propagation delay. For the consideration of short propagation delay, the smaller load capacitance and resistance are required. Therefore, a larger biasing current is preferred. However, a large biasing current results in a large power consumption.

For its small propagation delay compared with other logic families, the MCML is suitable for the high speed application. In [46], a comparison of the power consumption of the MCML and CMOS inverters has been investigated and

simulated using a 0.18 μm CMOS process. Simulation results show that for applications above 2 GHz, the MCML circuit is preferred if the power consumption is the key consideration. In the design of the frequency divider, the operating frequencies are different for the different stages of divide-by-2. Therefore, in the low frequency stages, a smaller biasing current can be used. For example, in [47], the biasing current is halved for the divide-by-2 stage working at half operating frequency. In this regard, the power consumption of the MCML circuit is also linearly proportional to the input frequency if the biasing current is scaled down in the cascaded divide-by-2 frequency divider even the power consumption for a certain MCML circuit is independent of the operating frequency.

The optimization of the power consumption of an MCML circuit for a given operating frequency is a complex procedure although the equations of the power consumption and the propagation delay look simple. Considerations must be given for numerous parameters individually such as the logic swing, load resistor, switch size and biasing current, etc.

For lower power consumption, a low supply voltage is preferred. However, the reduction of the supply voltage will reduce the output impedance of the current source and may shift the NMOS out of the saturation region, while reducing the mid-swing gain as well [48]. In general, the voltage swing should be as small as possible since a smaller voltage swing introduces a smaller propagation delay and the output swing is determined by product of the biasing current and the load resistance. However, the output can not be reduced to an indefinite value because it must be able to drive the next stage. Its lower limit is determined by the gain and the current switching requirements. If the voltage swing is too small, the follow

stage will need a high gain, hence a large transistor size which increases the load capacitance of the output node. This procedure in turn increases the propagation delay. The optimized value of the voltage swing ΔV_{opt} is given in [13]:

$$\Delta V_{opt} \approx \frac{10.3}{T}\frac{1+\varepsilon}{1-\varepsilon} ln(\frac{1}{\varepsilon})k \tag{2.50}$$

where $C = C_0 + k\beta$ is used to model the load capacitance, T is the period of the signal applied to the inverter input, and ε is the settling error of the exponential settling at the RC loaded output.

Finally, increasing the width of the differential pair transistors will increase the voltage gain. However, it will also increase the input and output capacitances.

CMOS dynamic circuit

The analysis of the CMOS dynamic circuit is based on the theory of the CMOS devices. The propagation delay and the power consumption of the CMOS digital circuit will be analyzed in this section.

The propagation delay of the CMOS circuit is given by [48]:

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} \tag{2.51}$$

where t_{pLH} is the propagation delay of the "low to high" transition, and t_{pHL} is the propagation delay of the "high to low" transition.

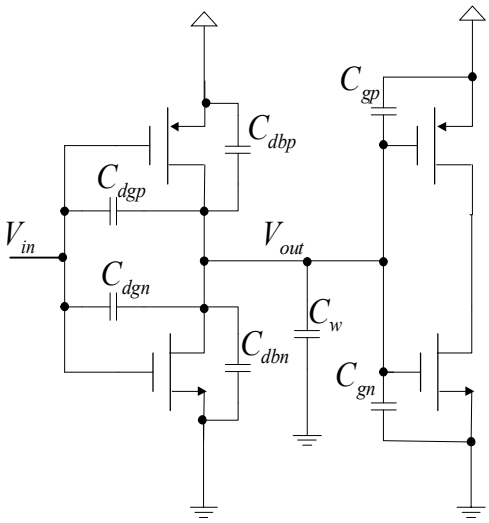


Figure 2.22: CMOS inverter

The first order analysis of the CMOS circuit can be performed for a CMOS inverter as shown in Figure 2.22 [48]. The propagation delay is calculated by integrating the capacitor charge and discharge current.

$$t_{pHL} = \frac{C_L V_{dd}}{\mu_n C_{ox} \frac{W}{L}(V_{dd} - V_{tn})^2} \tag{2.52}$$

$$t_{pLH} = \frac{C_L V_{dd}}{|\mu_p| C_{ox} \frac{W}{L}(V_{dd} - |V_{tp}|)^2} \tag{2.53}$$

Where C_L is the total load capacitance, which is given by:

$$C_L = (C_{dp} + C_{dn}) + (C_{gp} + C_{gn}) + C_w \tag{2.54}$$

From the above equations, to reduce the propagation delay, three methods can be implemented. The first method is to reduce the load capacitance. However, as the gate and diffusion capacitances are linearly proportional to the transistor's gate area, the reduction of the capacitance will reduce W/L if the minimum channel length is used. The reduction of W/L in turn increases the propagation delay since the charging/discharging currents are reduced. The second method is to increase

W/L, this way has the same problem as the first method. Therefore, the transistor sizing needs a careful consideration. The third method is to increase the supply voltage which will increase the power consumption.

There are three major sources of the power dissipation in digital CMOS circuits that are summarized in the following equation [49]:

$$P_{avg} = P_{switching} + P_{short-circuit} + P_{leakage} = \alpha_{0\to 1} C_L V_{dd}^{\ 2} f_{clk} + I_{sc} V_{dd} + I_{leakage} V_{dd} \qquad (2.55)$$

The first term represents the switching power consumption, where C_L is the load capacitance, f_{clk} is the clock frequency and $\alpha_{0\to 1}$ is the node transition activity factor, which is the average number of times that the node makes a power consuming transition in one clock period. The second term is due to the direct-path short circuit current, I_{sc}, which arises when both NMOS and PMOS transistors are simultaneously active, conducting a current directly from the supply to ground. Finally, the leakage current, $I_{leakage}$, which can arise from the substrate injection and subthreshold effects, is primarily determined by the fabrication technology.

In a well designed CMOS digital circuit, the switching power consumption is the dominant component of the total power dissipation. The supply voltage is the dominant parameter of the switching power consumption. If the output swing is not rail to rail, the switching power is given by [50]:

$$P_{switching} = \alpha_{0\to 1} C_L V_{dd} V_{swing} f_{clk} \qquad (2.56)$$

The node transition activity factor, $\alpha_{0\to 1}$, is decided by many factors such as the logic function, the logic style, and the signal statistics, etc. [49]. For example, the XOR and the NOR gates have different values of $\alpha_{0\to 1}$ for an input with a uniform distribution of high and low logic levels.

In the CMOS circuit, due to the non-ideal of the input signal, there will be a transition during which the PMOS and NMOS transistors are conducting simultaneously. This causes a short circuit (direct path) from supply voltage to ground. The short circuit power consumption is usually ignorable in the CMOS circuit [48]. However, in some high speed digital circuits, e. g. the E-TSPC logic [51], the PMOS and NMOS may not be configured complementarily. The direct path will exist within a large portion of the data transitions besides the rising and falling edges. As a result, the short circuit power will be comparable or even larger than the switching power.

2.6 Conclusion

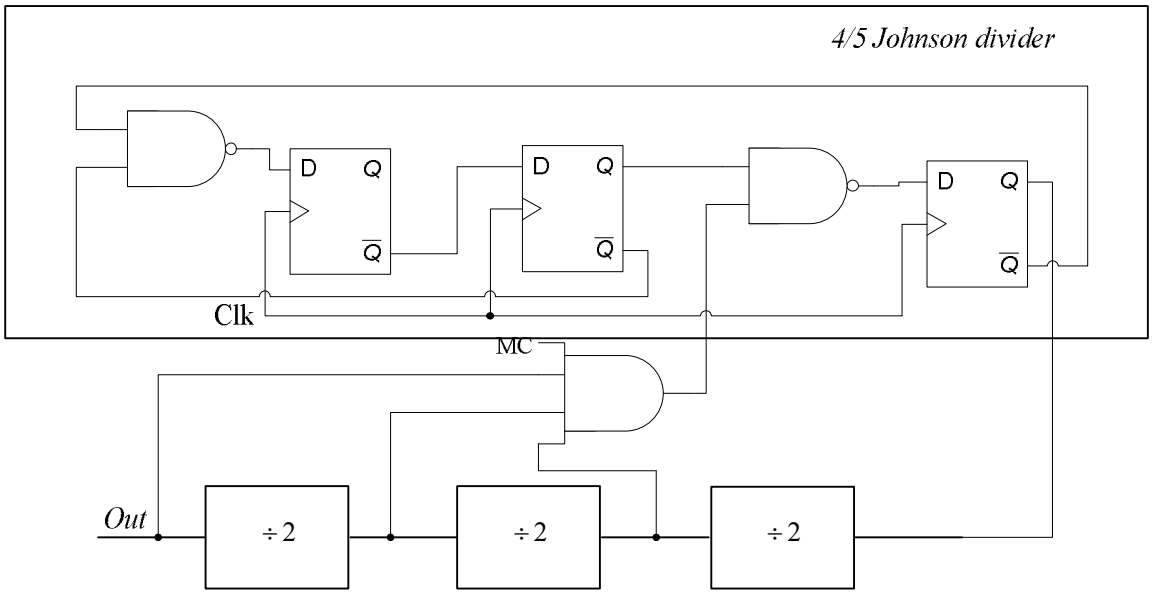
In this chapter, the basic theory for the phase locked loops are reviewed. The two major building blocks in the PLLs, namely the VCO and the frequency divider, are analyzed. The performances of the VCO are presented while the phase noise of the VCO is analyzed in details. Many digital frequency dividers, e.g., the cascaded divide-by-2, the prescaler and the digital counter are described and discussed. Finally, two major types of logic circuits, namely the TSPC and MCML circuits, are analyzed and compared.

Chapter 3

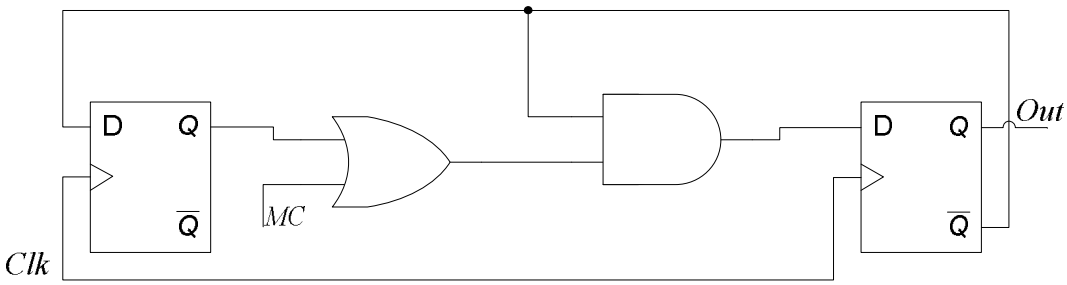
Design and Optimization of high speed CMOS Prescalers

3.1 Introduction

The prescaler is the most challenging part in the high speed frequency divider design because it operates at the highest input frequency. A dual-modulus prescaler usually consists of a divide-by-2/3 (or 4/5) unit followed by several asynchronous divide-by-2 units. Figure 3.1.a shows a traditional topology of a prescaler. In the high speed synchronous divider design, if the divide-by-4/5 unit is replaced with a divide-by-2/3 unit as shown in Figure 3.1.b, there will be less components operating at the full speed. Therefore, the divide-by-2/3 unit is widely used for its low power consumption. The modulus control signal, *MC* will decide the division ratio to be *N* or *N+1* where *N* is an integer. The operation of the divide-by-2/3 unit at the highest input frequency makes it the bottleneck of the prescaler design. To achieve these two different division ratios, extra logic gates and D flip-flops (DFF) are added to the divide-by-2 unit. As a result, the operating frequency is reduced since an additional propagation delay is introduced. The power consumption of this the divide-by-2/3 unit, which is the largest portion of the total power consumption in the prescaler, increases significantly as compared with that of the divide-by-2 unit due to the power consumption of the additional components.



(a)



(b)

Figure 3.1: Topology of the prescaler

(a) prescaler based on divide-by-4/5 Johnson divider (b) a divide-by-2/3 unit

3.2 The design and optimization of E-TPSC based prescaler

As discussed in the previous chapter, the MOS Current Mode Logic (MCML) circuit, which is of a high power consumption, is commonly used to achieve a high operating frequency, while a true-single-phase-clock (TSPC) dynamic circuit, which only consumes power during the switching, has a lower operating frequency. In [99], the dynamic circuit is used to achieve the low power

consumption. In [51], the E-TSPC logic is proposed to increase the operating frequency. However, this causes the additional power consumption. So far, the impacts of the modified topology over the operating frequency and power consumption have not been fully investigated. In this section, the power consumption and operating frequency of the E-TSPC logic is evaluated. Two major sources of the power consumption, namely the short circuit power and the switching power, in the E-TSPC divide-by-2 unit are calculated and simulated. Based on the analysis, a new divide-by-2/3 unit is proposed to achieve the low power consumption by reducing the switching activities and the short circuit current in the D flip-flops of the unit, and a dual-modulus prescaler is designed and implemented with the proposed unit.

3.2.1 TSPC and E-TSPC divide-by-2 units

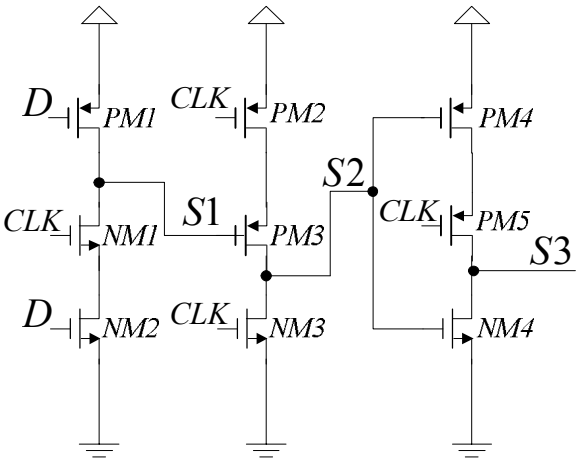
The toggled TSPC DFF [52] is the most popular divide-by-2 unit in the low power high speed frequency divider design, while the E-TSPC DFF [51] is proposed to increase the operating frequency. Figures 3.2.a and (b) show the topology of a TSPC DFF and an E-TSPC DFF respectively. When performing the divide-by-2 function, the output *S3* is fed back to *D*. The operation of both divide-by-2 units is shown in Figure 3.3.

An analysis of the propagation delay of the TSPC unit can be obtained from [48] as the RC delay. For example, the high-to-low propagation delay of a transition of the TSPC unit as shown in Figure 3.2.a is given by:

$$C_L = C_{dbNM4} + 2C_{gdNM4} + C_{dbPM5} + 2C_{gdPM5} + C_{gNM2} + C_{gPM1} \tag{3.1}$$

$$t_{pHL} = 0.69\tau = 0.69R_{on}C_L = 0.69R_{onNM5}C_L \tag{3.2}$$

where R_{onNM5} is the equivalent resistance of *NM5* during the high-to-low transition.



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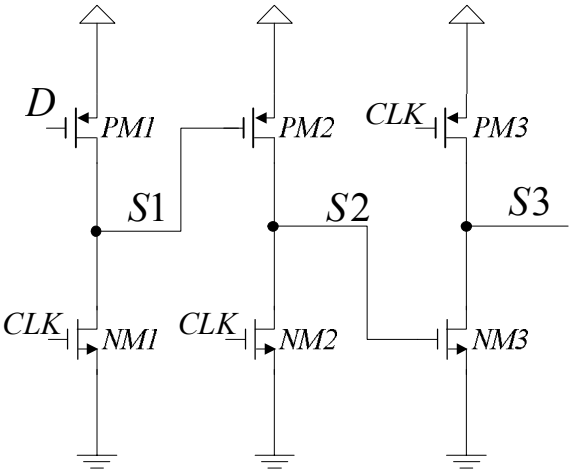


(b)

Figure 3.2: Dynamic DFFs a) TSPC b) E-TSPC

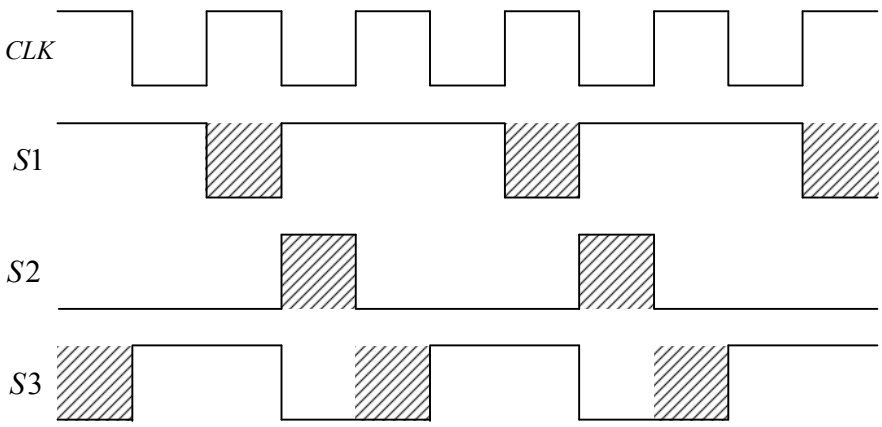


Figure 3.3: Operation of divide-by-2 function

In the E-TSPC, this delay is given by:

$$C_L = C_{dbNM3} + 2C_{gdNM3} + C_{dbPM3} + 2C_{gdPM3} + C_{gPM1} \tag{3.3}$$

$$t_{pHL} = 0.69\tau = 0.69R_{on}C_L = 0.69R_{onNM3}C_L \tag{3.4}$$

It is observed that the load capacitance of the E-TSPC logic style has been reduced as compared with that of the TSPC. So the propagation delay of the E-TSPC unit will be smaller. From the method proposed in [48], a manual calculation of the propagation delay for the two units can be obtained. Figure 3.4 shows the calculated and simulated propagation delay for these two units using the same MOS transistor size. In this simulation, the minimum channel length of 0.18 μm is used. The E-TSPC achieves a higher operating frequency as reported in [51].

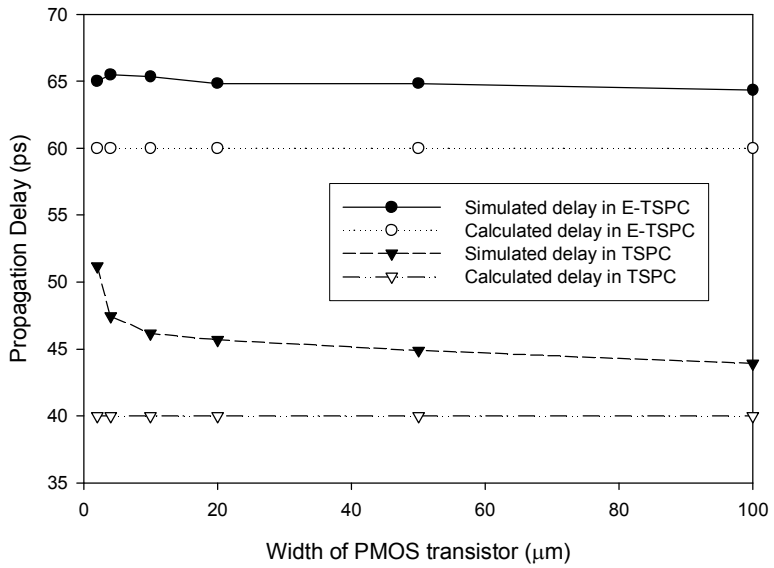


Figure 3.4: Propagation delays of the TSPC and the E-TSPC divide-by-2 unit

By reducing the load capacitance during charging and discharging, the switching power consumption can be reduced as well.

For the TSPC unit, the load capacitances of the three nodes *S1*, *S2* and *S3*, namely C_{LS1}, C_{LS2} and C_{LS3} are:

$$C_{LS1} = C_{dbPM1} + 2C_{gdPM1} + C_{dbNM1} + 2C_{gdNM1} + C_{gPM2} \quad (3.5)$$

$$C_{LS2} = C_{dbNM3} + 2C_{gdNM3} + C_{dbPM3} + 2C_{gdPM3} + C_{gPM4} + C_{gNM5} \quad (3.6)$$

$$C_{LS3} = C_{dbNM5} + 2C_{gdNM5} + C_{dbPM5} + 2C_{gdPM5} + C_{gNM2} + C_{gPM1} \quad (3.7)$$

For simplicity, the capacitances of other nodes, which also introduce parts of the power consumption, are not listed here.

For the E-TSPC unit, the load capacitances of each stage have been reduced as follows:

$$C_{LS1} = C_{dbPM1} + 2C_{gdPM1} + C_{dbNM1} + 2C_{gdNM1} + C_{gPM2} \quad (3.8)$$

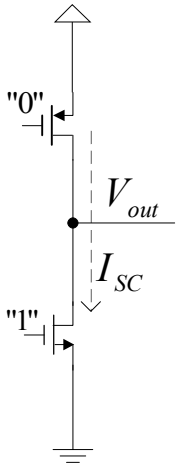
$$C_{LS2} = C_{dbPM2} + 2C_{gdPM2} + C_{dbNM2} + 2C_{gdNM2} + C_{gNM3} \quad (3.9)$$

$$C_{LS3} = C_{dbPM3} + 2C_{gdPM3} + C_{dbNM3} + 2C_{gdNM3} + C_{gPM1} \quad (3.10)$$

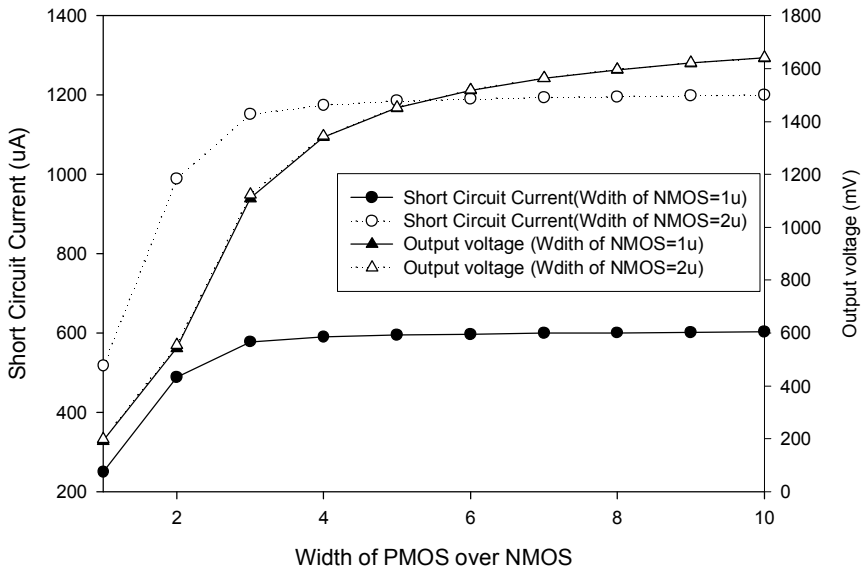
The E-TSPC unit has a lower switching power compared with that of the TSPC unit.

However, in the E-TSPC unit, there is a period during which a direct path from the supply voltage to ground is established in the operation of divide-by-2. In this period, the PMOS and NMOS transistors are turned on simultaneously. The shaded areas in Figure 3.3 mark the transition during which the short circuit takes place.

The behavior of the short circuit in a single stage of the E-TSPC DFF is analyzed in Figure 3.5. The short circuit current depends on the aspect ratio W/L of the PMOS and the NMOS. Depending on the configuration of the $\frac{W_p}{W_n}$, the operation region of the PMOS and the NMOS can be either the triode region or the saturation region.



(a)



(b)

Figure 3.5: Short circuit in the E-TSPC logic style

(a) Schematic (b) Simulation results

Figure 3.5.b shows the short circuit current and the output voltage versus $\frac{W_p}{W_n}$, where W_p and W_n are the widths of the PMOS and the NMOS transistors respectively. If $\frac{W_p}{W_n} \leq \frac{\mu_n}{\mu_p}$, the short circuit current is decided by the PMOS, and its operation region changes from the saturation region to the triode region with the

increase of $\frac{W_p}{W_n}$. When $\frac{W_p}{W_n} \geq \frac{\mu_n}{\mu_p}$, with the increase of $\frac{W_p}{W_n}$, the NMOS shifts from the triode region to the saturation region. When both the NMOS and the PMOS are in the triode region, the short circuit is given by:

$$I_{short=}\mu_n C_{ox}\frac{W_n}{L}[(V_{GSn}-V_{tn})V_{DSn}-\frac{V^2{}_{DSn}}{2})] = \mu_p C_{ox}\frac{W_p}{L}[(V_{SGp}-|V_{tp}|)V_{SDp}-\frac{V^2{}_{SDp}}{2})] \qquad (3.11)$$

where $V_{DSn}=V_{out}$ and $V_{SDp}=V_{dd}-V_{out}$

V_{out} increases with the increase of $\frac{W_p}{W_n}$ before the NMOS transistor reaches the saturation.

As marked in Figure 3.3, for all the three stages in the E-TSPC unit, there is a quarter of the period during which the direct path is established from supply voltage to ground. From the calculation of the short circuit current, the short circuit power in the E-TSPC unit can be determined by the product of supply voltage and the short circuit current.

From above analysis, the two sources of power consumption in the E-TSPC unit exhibit different characteristics. In the E-TSPC unit, the short circuit current and the power of each stage are decided by the sizes of the MOS transistors only. For the switching power, it is linearly proportional to the input frequency for a fixed size of the MOS transistors. The two types of the power consumption can be determined using the process parameters [48]. One stage of the E-TSPC unit, as shown in Figure 3.5(a), is examined. For simplicity, $\frac{W_p}{W_n}$ is 2 [53] and the channel length for all the transistors is 0.18 μm. The input signals of Figure 3.5 are logically low for the PMOS and logically high for the NMOS. As a result, the PMOS and NMOS transistors are turned on simultaneously, and the short circuit in

one stage of the E-TSPC DFF can be determined. For a comparison, an inverter with the same transistor size but the input signal is a square wave is also simulated to obtain the value of the switching power in the E-TSPC. To evaluate the different switching powers of the E-TSPC and the TSPC due to the different capacitive loads, the load of one PMOS for the E-TSPC unit and the load of one PMOS plus one NMOS for the TSPC unit are used in the calculation and simulation. These two loads can be viewed as the different capacitances between the E-TSPC and TSPC logic types.

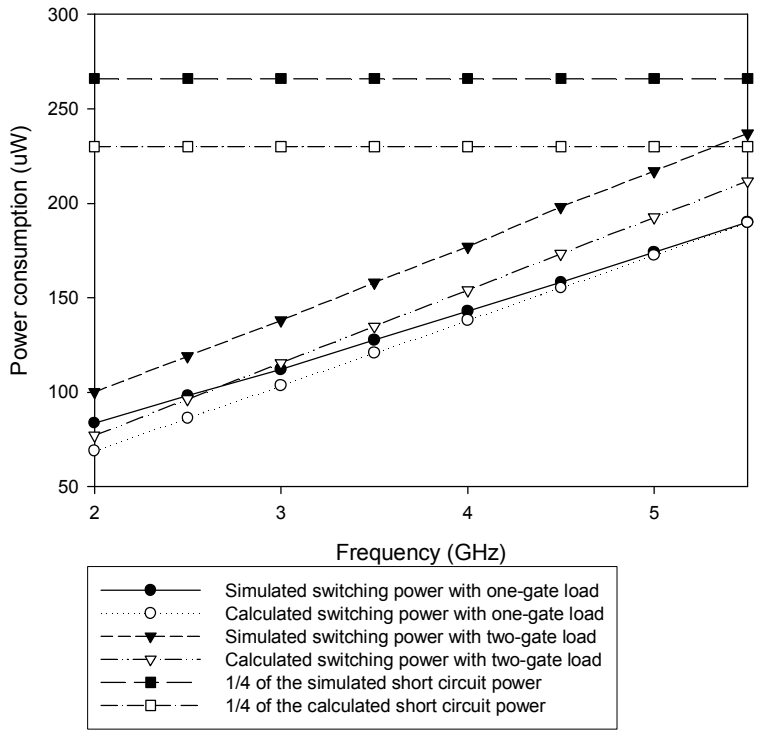


Figure 3.6: The switching power and short circuit power in one stage of E-TSPC

Figure 3.6 shows the calculated and simulated power consumption results of these two sources of the power consumption. The short circuit power is fixed over the operating frequency. While the switching power in the inverter is linearly proportional to the input frequency. With the increase of the operating frequency,

the value of the switching power gradually approaches that of the short circuit power. However, the short circuit power is always larger than the switching power. For the one PMOS load in the inverter, the switching power is lower as compared with that of the one PMOS plus one NMOS load. Figure 3.7 shows the results of two power sources in an E-TSPC unit and a TSPC unit. The E-TSPC unit has a lower switching power. However, its short circuit power is much larger than the switching power. Within the operating frequency range, the E-TSPC unit has a larger total power consumption than that of the TSPC unit.

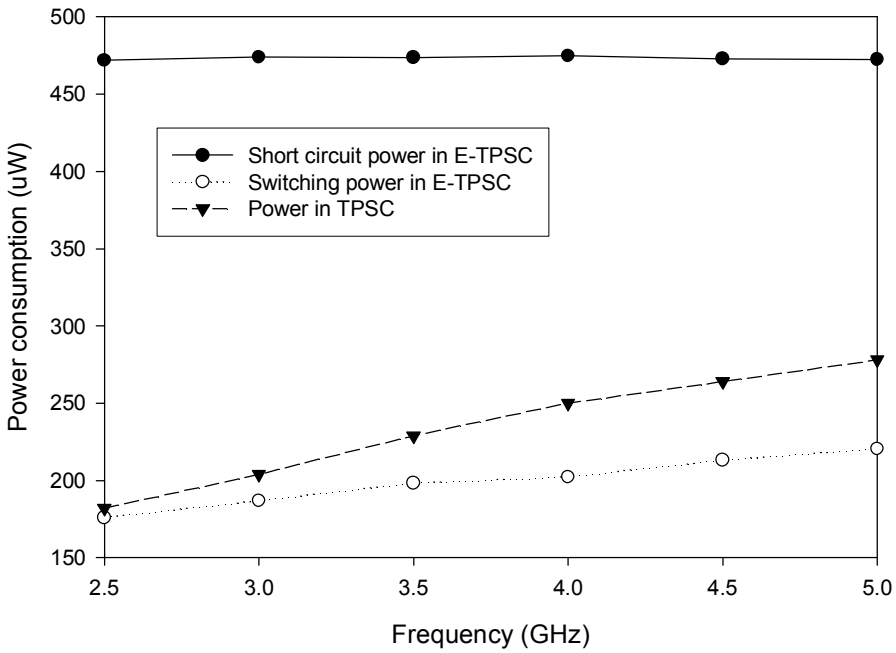


Figure 3.7: The switching power and short circuit power in the E-TSPC and TSPC unit

3.2.2 E-TSPC based divide-by-2/3 unit

The E-TSPC divide-by-2 unit has the merit of the high operating frequency compared with the traditional TSPC divide-by-2 unit. In [51], an E-TSPC based divide-by-4/5 unit is used to form a high speed prescaler. To reduce the number of

components working at full-speed, the divide-by-2/3 is used in [99]. Since the divide-by-2/3 unit consists of two toggled DFFs and additional logic gates, one way to effectively reduce the delay and power consumption is to integrate the logic gates to the divide-by-2/3 unit [54]. In [99], a gate-integrated dual-modulus prescaler based on the dynamic circuit has been proposed to achieve the high operating frequency and low power consumption. This design uses two DFFs while the divide-by-4/5 unit in [51] uses three DFFs. The divide-by-2/3 unit in [99] is shown in Figure 3.8.

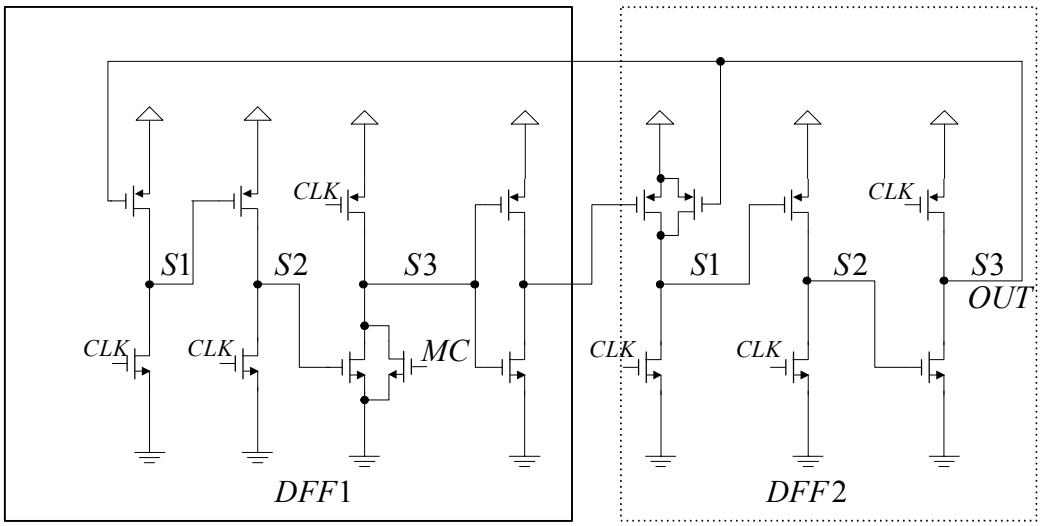


Figure 3.8: The divide-by-2/3 unit in [99]

When the modulus control signal MC is logically low, it performs the divide-by-3 function. If the output of DFF2 is logically low, the node *S1* of DFF2 is disabled, so the nodes *S2* and *S3* of DFF2 will have no switching activities, therefore, no switching power dissipation. DFF1 operates all the time while DFF2 only operates when the output of DFF2 is logically high. When MC is logically high, the output of DFF1 will be disabled to achieve the divide-by-2 function. However, the nodes *S1* and *S2* of DFF1 still have switching activities since the output of DFF2 still

feeds back to DFF1. So both D flip-flops switch at half of the input frequency and even DFF1 does not participate in the divide-by-2 function. As a result, the divide-by-2 unit dissipates more power even only one toggled DFF is needed. Such a topology introduces unnecessary power consumption which is a significant part of the total power consumption. Moreover, during a quarter of the period, the short circuit power still exists in DFF1 as discussed in the previous section.

3.2.3 Proposed topology

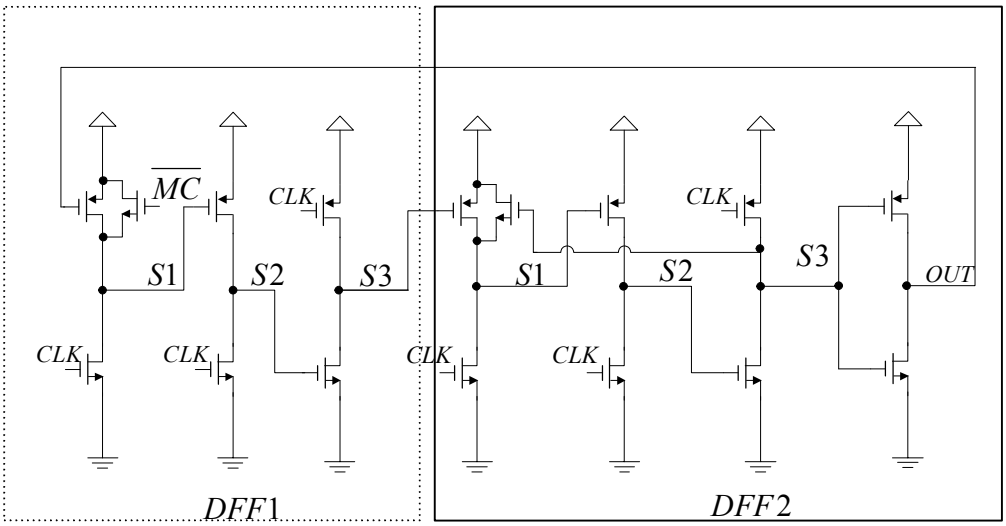


Figure 3.9: The proposed divide-by-2/3 unit

The difficulty of designing the divide-by-2/3 unit is to minimize the overall power consumption. During the divide-by-2 operation, it is not necessary for both DFFs to operate at full-speed since only one toggled DFF is needed to perform the divide-by-2 function. If only one DFF is active during the divide-by-2 operation, theoretically, a 50% reduction of the power consumption is achieved. In [99], the output of DFF1 is manually pull down by the *MC* controlled NMOS, but DFF1 still works at full speed. To reduce the unnecessary power consumption, a new

divide-by-2/3 unit which can effectively block the switching activities and the short circuit is proposed as shown in Figure 3.9. Different from [99], in this topology, two AND gates are used instead of one OR gate and one AND gate as in [54] to achieve a symmetrical architecture. By changing the *MC* controlled NMOS at the output of DFF1 to an $\overline{MC}$ controlled PMOS, DFF1 is blocked at the input. As a result, nodes *S1*, *S2* and *S3* of DFF1, which have the logical values of "1", "0" and "1" respectively, are blocked. DFF1 has no switching activities or short circuit while DFF2 functions as a toggled divide-by-2 unit. Hence, the proposed divide-by-2/3 unit only has one active DFF when it performs the divide-by-2 function and the power consumption is reduced significantly. Even for the divide-by-3 operation, due to the complementary logic type, the power consumption is also slightly reduced due to the reduction of the short circuit power consumption in DFF1 as shown in Figure 3.11.

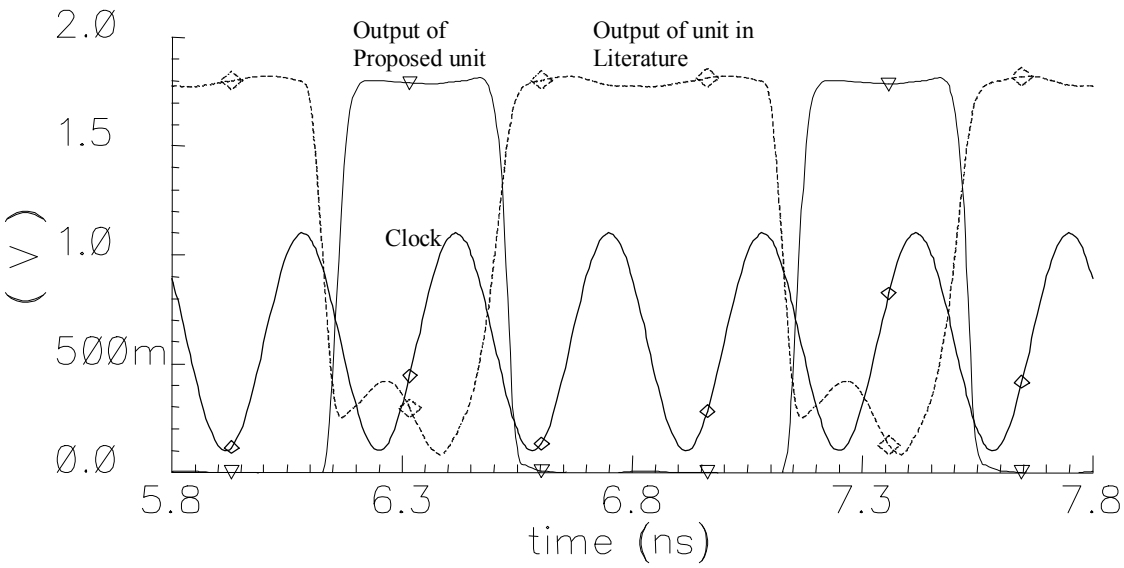


Figure 3.10: Output divide-by-3 waveform of two divide-by-2/3 units

3.2.4 Simulation and silicon verifications

A comparison of the performances of this new divide-by-2/3 unit and the E-TSPC unit in [99] is carried out on the grounds that the design in [99] achieves the best performance in literature so far. The simulations are performed by using the Cadence SPECTRE RF for a 0.18 μm CMOS process. The PMOS and NMOS devices of these two units are of the same size.

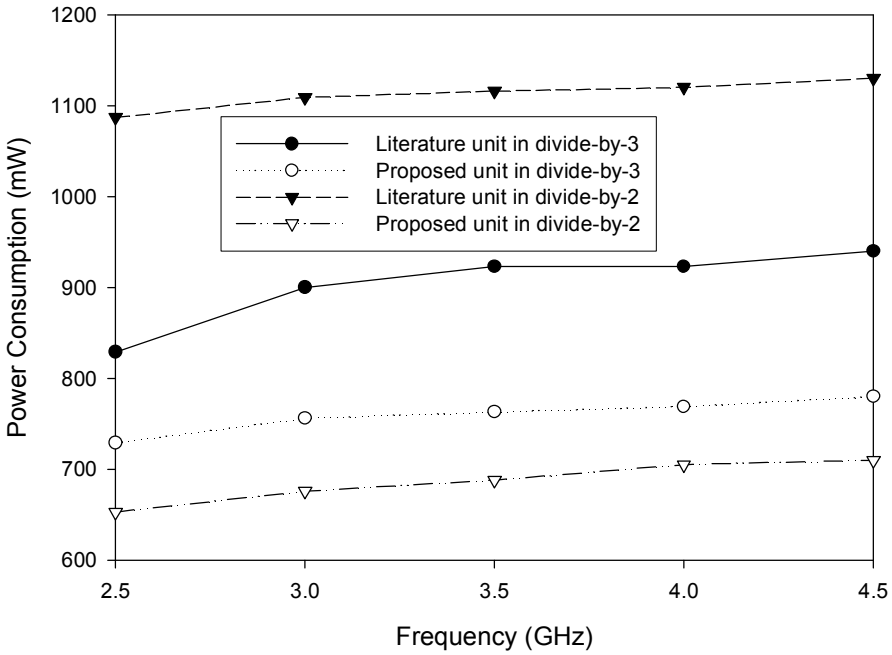


Figure 3.11: Power consumption vs. operating frequency of the proposed divide-by-2 unit and the divide-by-2 unit in [99].

Figure 3.11 shows the simulation results of the power consumption *vs* the operating frequency of two units for the operations of divide-by-2 and divide-by-3. In the divide-by-3 operation, the proposed unit has about 10% lower power consumption reduction compared with that of the unit in [99]. In the divide-by-2 operation, the proposed unit dissipates less than 60% of the power consumption of the unit in [99] due to the former's reduced switching activities and short circuit in

DFF1. If two operations are of the equal probabilities in the dual-modulus prescaler, a 25% reduction in the power consumption is achieved for the proposed unit. With an input frequency of 4.5 GHz, the power consumption is only 790 μW giving a power consumption/frequency ratio of 0.18 μW/MHz. Compared with 3.27 μW/MHz in [51], a great power consumption reduction is achieved. To further verify the advantages of this proposed prescaler, a divide-by-8/9 dual-modulus prescaler using the same architecture in [99] but with the proposed divide-by-2/3 unit is implemented. In this divide-by-8/9 prescaler, the proposed divide-by-2/3 unit is followed by two stages of the toggled TSPC divide-by-2 units.

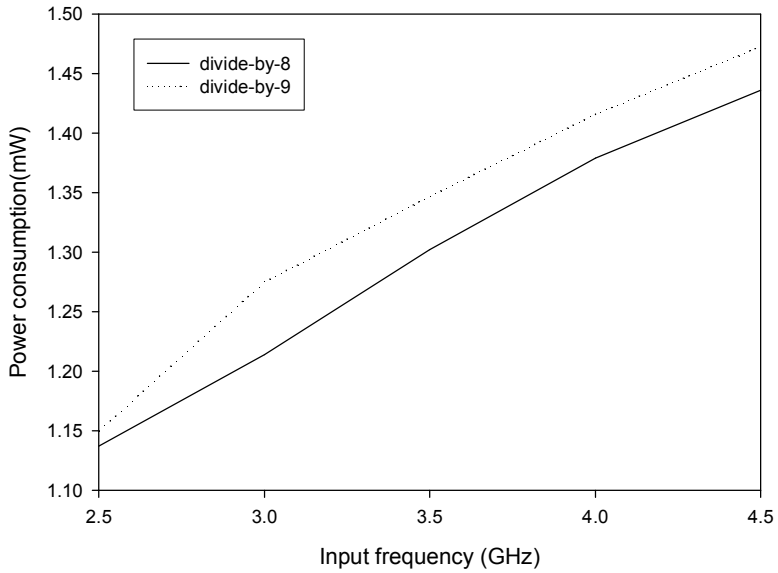


Figure 3.12: Power consumption of the proposed divide-by-8/9 prescaler

Figure 3.12 shows the power consumption *vs* the operating frequency of the proposed prescaler. An ultra low power consumption is achieved in the proposed prescaler. In the proposed prescaler, $\frac{W_p}{W_n} = \frac{2\mu m}{1\mu m}$ is used for the verification of the

calculation, even the transistor sizing is an effective way to increase the operating frequency [55].

For the silicon verification, the proposed prescaler is fabricated using the CSM 1P6M 0.18 µm CMOS process with the RFMOS. Because the RFMOS provided by CSM is non-scalable and quite large ($\frac{W}{L}$ for RF PMOS and RF NMOS are $\frac{60\mu m}{0.18\mu m}$ and $\frac{30\mu m}{0.18\mu m}$ respectively), the simulation is performed again using the RFMOS model.

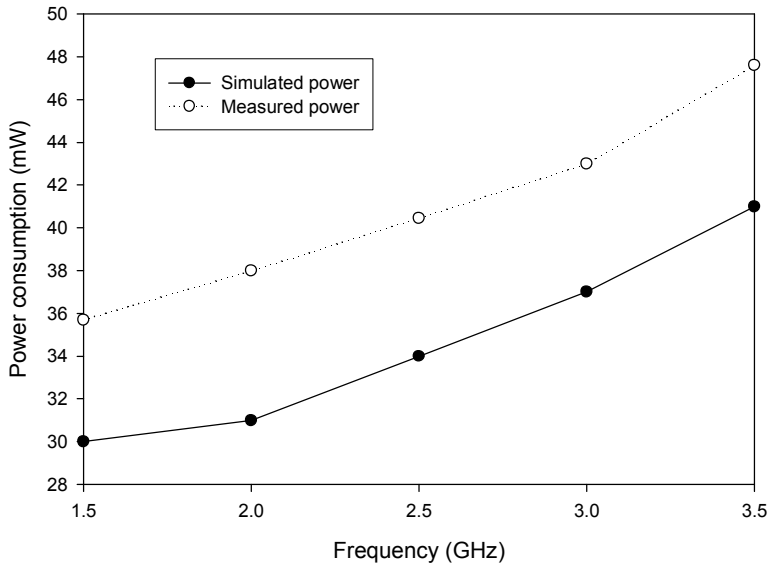


Figure 3.13: Simulated and measured results of the proposed prescaler with RFMOS

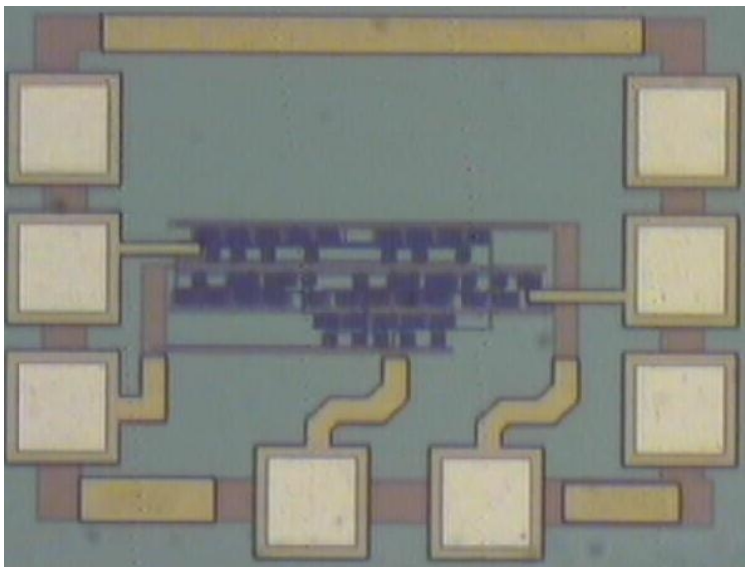


Figure 3.14: Die photo of the proposed prescaler

Figure 3.13 shows the simulation result of the prescaler by using the RFMOS. Due to the large transistor size, the power consumption increases significantly, as it is linearly proportional to width of the MOS transistors. Moreover, the simulation is limited to 3.5 GHz because beyond such frequency, the MOS transistors reach the melt current due to the large currents introduced by the large transistor sizes.

Figure 3.14 shows the die photo of the proposed divide-by-8/9 dual-modulus prescaler. The active area takes about 100µm × 80µm due to the implementation of RFMOS, while the die size is about 500µm × 350µm in adding the test buffer and pads. On wafer tests are carried using an RF probe station. The input signal for the measurement is provided by the HP E4433B 0.25 MHz-4 GHz signal generator, while the output signals are captured by Lecroy Wavemaster 8600A 6G oscilloscope.

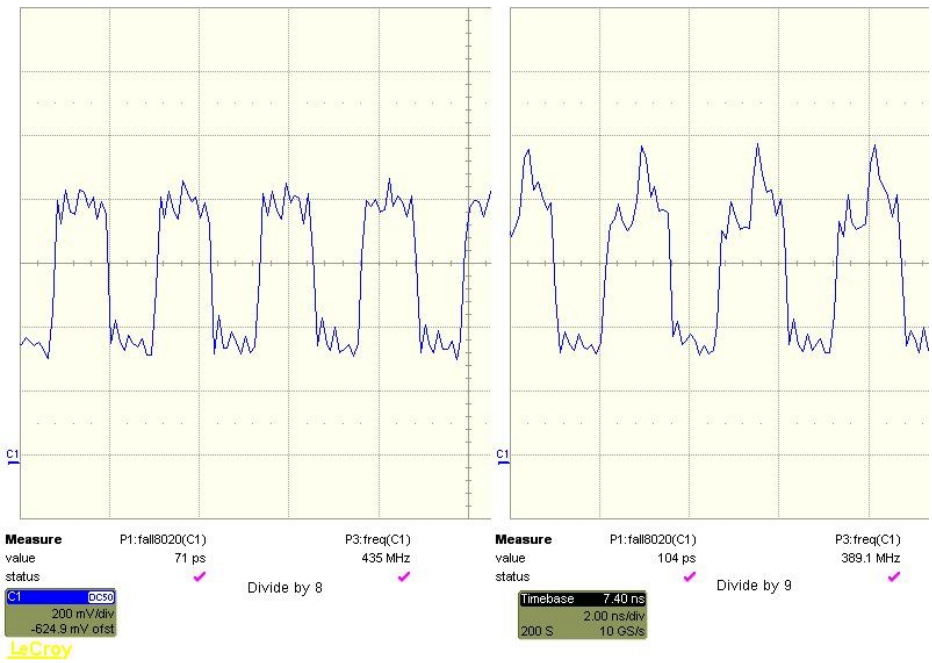


Figure 3.15: Measured transient results of the proposed divide-by-8/9 prescaler

Figure 3.15 shows the measured transient results of the prescaler with an input of 3.5 GHz for a 1.8 V supply voltage. The current dissipation is 20 mA for the test chip. To verify the relationship between the device sizes vs. power consumption, the prescaler with the same topology but with smaller device sizes is also fabricated. Because the models of the normal MOS provided by CSM haven't been verified at high frequencies and too small transistors are susceptible to process variations. In this case, the aspect ratios $\frac{W}{L}$ for RF PMOS and RF NMOS are $\frac{32\mu m}{0.18\mu m}$ and $\frac{16\mu m}{0.18\mu m}$ respectively. As a result of the halved device sizes, the current dissipation for the measured chip reduced to 8.6 mA with the supply voltage of 1.5V with a 4 GHz input in the measurement in the same environment. If the device is further scaled down to 2 μm and 1 μm for the PMOS and NMOS, the power consumption would be reduced to 1.6 mW for the prescaler by comparing the simulations for the two sizes of MOS transistors. The operating

frequency should be the same as the propagation delay is independent of the width the transistors as shown in the previous section. Hence, the power/frequency is 0.5 μW/MHz, compared with 8 μW/MHz in [51].

3.3 Low power high speed CMOS dual-modulus prescaler with Imbalanced phase switching technique

At the beginning of this chapter, the architecture of a dual-modulus prescaler is presented. The dual-modulus control is achieved by a synchronous counter (divide-by-2/3 or 4/5) at the first stage. Then several stages of divide-by-2 stages are used to achieve the desired division ratios. Besides these blocks, there is an additional logic block to control the modulus of the divide-by-*N*/*N*+*1* at the end of one division cycle. However, the logic of the detector for the reload signal becomes very complex as the number of stages increases since the detector needs to detect the outputs of all stages. Such a topology also limits the operating frequency while increasing the power consumption. In [40], the phase switching technique is first proposed as shown in Figure 3.16.a. In its design, the change of modulus is carried out by shifting within four phase signals ($F4I$, $F4Q$, $\overline{F4I}$, and $\overline{F4Q}$) at the raising edge of F_{out} , and for the remaining time only one phase signal is selected as the output. For example, at the end of one division cycle, the output of the phase-select block switches from $F4I$ to $F4Q$, therefore, a 90-degree delay is introduced. Since the period of signal $F4I$ is four times of the input signal F_{in} , this delay is exactly one period of input signal F_{in} . Hence, the dual-modulus of divide-by-*N*/*N*+*1* is achieved.

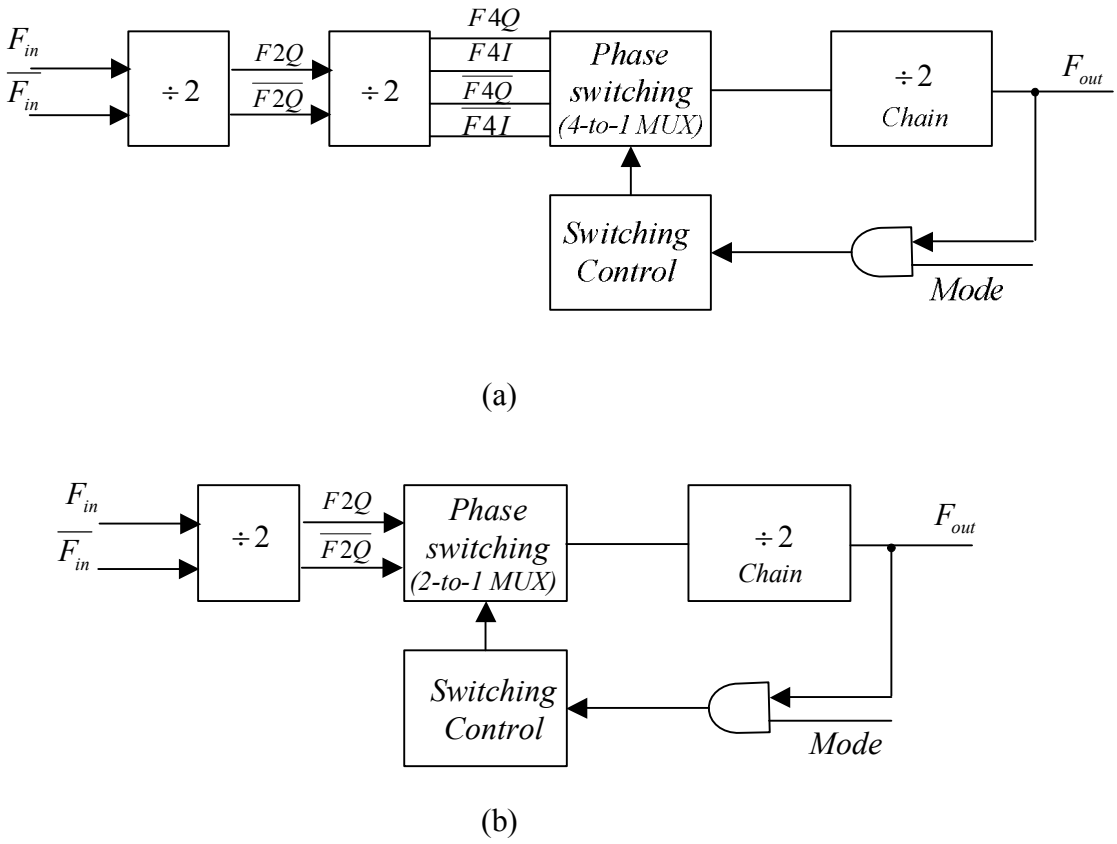


Figure 3.16: The architecture of the phase switching Technique
a) Topology in [40], b) Topology in [56]

This architecture only has one divide-by-2 stage operating at a full speed. Hence, the power consumption is reduced. In [56], a simplified design based on [40] is proposed in which the switching of phase is carried out between two complementary signals ($F2Q$ and $\overline{F2Q}$) as shown in Figure 3.16.b. Because the period of $F2Q$ is twice of the period of the input signal F_{in}, the switching between $F2Q$ and $\overline{F2Q}$ which introduces 180-degree delay also get a delay of one period of input signal F_{in}. In this topology, because the phase switching is carried out at half of the input frequency, only one 2-to-1 MUX is needed instead of 4-to-1 MUX (usually consists of three 2-to-1 MUXs). Moreover, in [40], a 4-state-machine is needed to control the 4-to-1 MUX. This 2-to-1 phase switching

prescaler has a simpler topology and lower power consumption. However, this architecture suffers from the glitch [57]. As a result, the operating frequency is limited to low frequencies. Many modifications have been made to remove the glitch [57] [58]. In [57], a re-timer circuit is added to synchronize the input signals of the phase switching block, while in [58], two additional divide-by-2 circuits are used to further reduce the operating frequency of the phase switching block. Nevertheless, all these modifications introduce complex architectures. The complexity of the architecture and the expense of the power consumption hamper the ease of implementing the phase switching technique. Until now, no effective way has been proposed to solve this problem without the trade-off. In this section, the operating frequency and power consumption of the phase switching prescaler are analyzed, while an imbalance phase switching method is proposed to solve the glitch issue without any trade-off. As a result, the operating frequency is increased in the proposed prescaler.

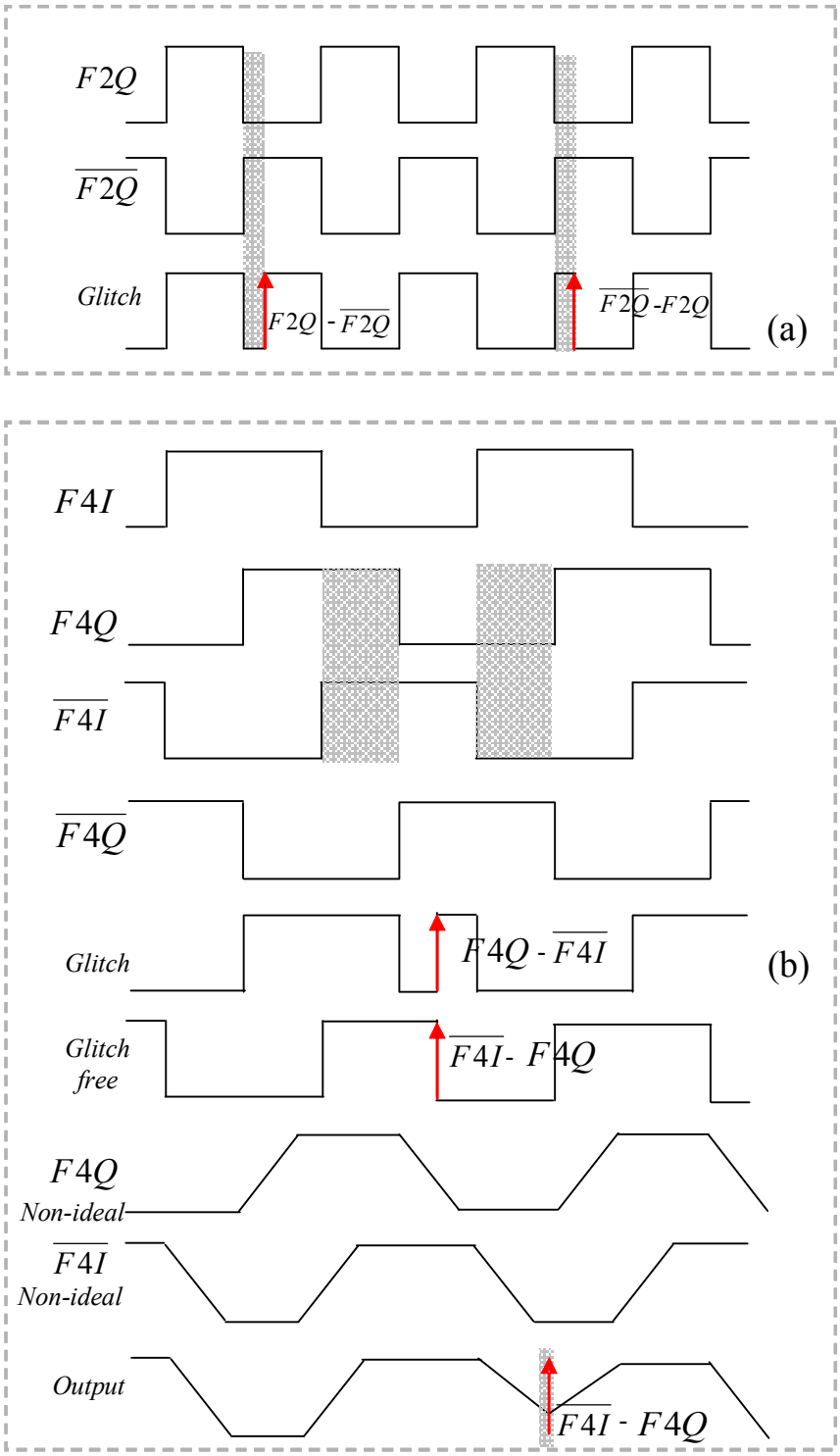


Figure 3.17: Limitation in the 50% duty cycle phase switching technique

a) Glitch in 2-to-1 phase switching, b) the correct timing window for 4-to-1 phase switching

3.3.1 Challenging of phase switching prescaler design

In a phase switching based prescaler, the function of a dual-modulus is achieved by switching between the different phase signals. In the divide-by-*(N+1)* mode, at every rising edge of F_{out}, the output of the phase-select block is switched to a 90-degree delay signal [40], while in the divide-by-*N* mode, the prescaler only acts as a divide-by-2 chain. In this way, there is only one master-slave toggled DFF divide-by-2 unit operating at the full speed. Therefore, the first stage will be critical to the operating frequency and power consumption of the whole prescaler. However, in order to operate the dual-modulus prescaler at the full speed of the first divide-by-2 block, the phase switching block must be able to function precisely even it operates at a lower frequency. The phase switching block must switch from one phase signal to the next phase signal within a certain time. The delay in the phase switching control loop is an issue in implementing this technique. For example, in [40], the phase switching block must be able to work at $\frac{F_{in}}{4}$ for an input frequency of F_{in} to make the prescaler work properly. As shown in Figure 3.17.b, for example, the output shifts from $F4Q$ to $\overline{F4I}$ to get an extra 90-degree delay at the rising edge of F_{out}. Due to the delay of the control loop, the switching will lag behind the rising edge of F_{out}. Only the switching, which takes place within the shaded area where $F4Q$ and $\overline{F4I}$ are of the same logic value, will work properly. Otherwise, a glitch will be generated if the switching is carried out at the transition which is marked with the arrow. The phase switching must be done within $\frac{T4}{4}$ to achieve the divide-by-*(N+1)* function, where T4 is the period of

the $F4Q$ signal. In this regard, the operating frequency of the prescaler is also decided by the phase switching block.

For the 2-to-1 phase switching proposed in [56], the switching is carried out between $F2Q$ and $\overline{F2Q}$. There is no transition where these two signals have the same value, thus glitches are unavoidable as shown in Figure 3.17.a. The compensation is carried out by controlling the rising and falling edges of the signals so that the erroneous trigger will not take place at the following stage [56]. However, such method is not robust enough to make the prescaler work properly. So the prescaler in [56] can only work at a lower frequency compared with [40] even it is implemented on a more advanced process. The maximum operation frequency in [40] is 1.75 GHz for a supply voltage of 3 V by using a 0.7 μm CMOS process, while in [56], only 1.5 GHz is achieved for a supply voltage of 2.7 V by using a 0.5 μm CMOS process. However, due to the simplified topology, the power consumption in the later design [56] has been reduced significantly in comparison with that of the former design [40].

The way to effectively solve this problem is to increase the delay budget. In [57], a re-timer circuit is used, but the design is complex and still not robust enough [58]. In [58], a novel one cycle removing method has been proposed. Instead of using the traditional switching sequence of $F4I$, $F4Q$, $\overline{F4I}$, and $\overline{F4Q}$, the alternative method in [58] switches in the reverse direction. For example, as shown in Figure 3.17.b, it does not shift from $F4Q$ to $\overline{F4I}$ (adding 90°), but from $\overline{F4I}$ to $F4Q$ (removing 90°) for the output signal of the phase switching block. By changing the switching direction, the division ratio is decreased by one instead of increased by one. In this way, the glitch will not be generated as shown in Figure 3.17.b. Theoretically, this method is glitch free because the switching is from the logic

high to the logic low and the next stage is a rising edge trigger. The transition of switching has no impact on the output division ratio. However, at the high operating frequency, the rise and fall time of $F4Q$ and $\overline{F4I}$ will be comparable to $\frac{T4}{4}$. As shown in Figure 3.17.b, if the switching is carried out when $F4Q$ and $\overline{F4I}$ are both at logic "0" (marked with arrow), the output signal may have an invalid rising edge as marked. So this output signal of the phase switching block is not able to trigger the following stage of the divide-by-2. Therefore, an incorrect division ratio takes place.

Hence, the operating speed of the phase switching prescaler is decided by the first divide-by-2 stage and the delay budget in the phase switching block. The divide-by-2 stage using the MCML circuit can achieve a high operating frequency [97] [98]. The maximum operating frequency of a divide-by-2 master-slave divider is given by [38]. The operating frequency of 18 GHz in the divide-by-2 stage can be achieved in existing 0.18 μm CMOS technology. However, the maximum operating frequency of the phase switching prescaler reported so far is only 8 GHz in simulation [58].

This is because the challenge lies in the phase switching block which is commonly realized in CMOS digital circuits. Its stringent delay requirement for the correct switching sequence can set a limitation for the overall performance.

In the phase switching prescaler design, the MCML toggled DFFs are used at the high speed divide-by-2 units to achieve a high operating frequency while obtaining the I and Q signals. At the subsequent frequency divide-by-2 chain, because of its low operating frequency, the CMOS dynamic circuit is implemented. As discussed before, the power consumption of both types of logic circuits are linearly

proportional to the operating frequency. For simplicity, the power consumption of these two types of circuits can be written as:

$$P_{MCML} = K_{MCML} f_{in} \tag{3.12}$$

$$P_{CMOS} = K_{CMOS} f_{in} \tag{3.13}$$

Where f_{in}, K_{MCML} and K_{CMOS} are the operating frequency, power versus frequency coefficients of the MCML and CMOS circuits respectively.

It is obvious that the first divide-by-2 stage will take a large portion of the power in the prescaler. For example, in the cascaded divide-by-2 frequency divider, if the power consumption for the first stage is *P1*, the maximum value (limitation) of the sum of the power consumption in following stages is also *P1* since the maximum of $\sum_{i=1}^{n} \frac{P1}{2^i}$ is equal to *P1*. However, in the prescaler design, the additional circuit in the phase switching block will introduce the additional power consumption. For simplicity, it is assumed that the prescaler has a general architecture including high speed differential divide-by-2 MCML circuits followed by CMOS dynamic circuits. The power consumption of the prescalers in [56], [40] and [58] are:

$$Power_{2-1} = K_{MCML} f_{in} + (K_{MUX} + K_{DFF}) \frac{f_{in}}{2^{n+1}} + \sum_{i=1}^{n} K_{CMOS} \frac{f_{in}}{2^i} \tag{3.14}$$

$$Power_{4-1} = K_{MCML} (\frac{3 f_{in}}{2}) + (3K_{MUX} + 2K_{DFF}) \frac{f_{in}}{2^{n+1}} + \sum_{i=1}^{n-1} K_{CMOS} \frac{f_{in}}{2^{i+1}} \tag{3.15}$$

$$Power_{8-1} = K_{MCML} (\frac{4 f_{in}}{2}) + (7K_{MUX} + 3K_{DFF} + K_{other}) \frac{f_{in}}{2^{n+1}} + \sum_{i=1}^{n-2} K_{CMOS} \frac{f_{in}}{2^{i+2}} \tag{3.16}$$

Where f_{in} is the input frequency of the prescaler and *n* is the number of stages in the divide-by-2 ring (The stages of divide-by-2 rings in Figure 3.16.a and Figure 3.16.b are *n*-1 and *n* respectively).

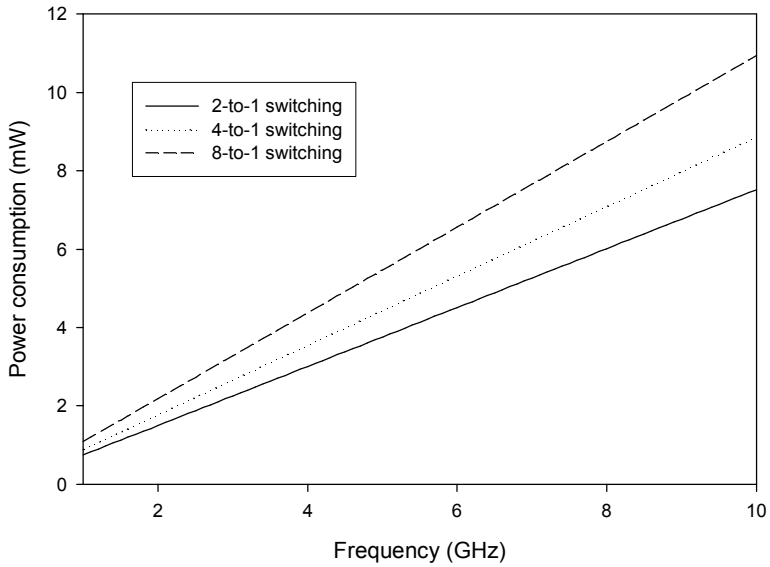


Figure 3.18: Power consumption vs. operating frequency of the three equations

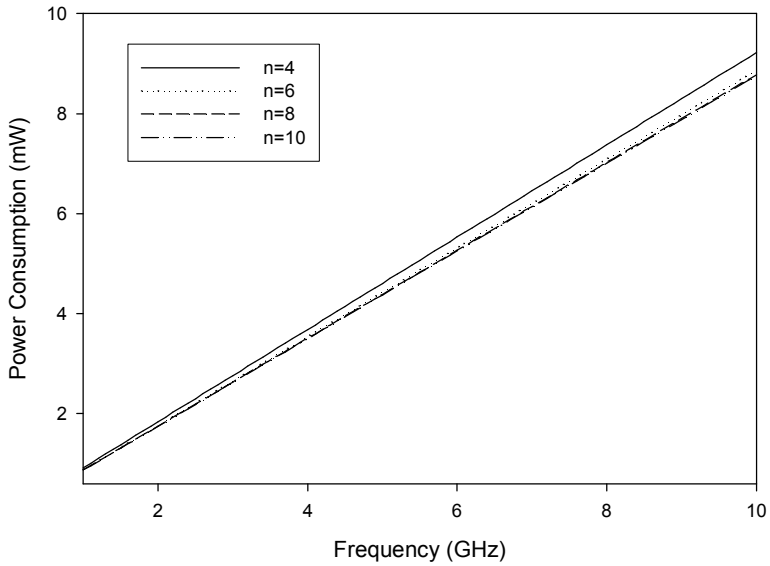


Figure 3.19: Power consumption vs. operating of 4-to1 switching with different stages

From these equations, it is observed that the switching moves backward and reduces the operating frequency of the phase switching block causing more power consumption. For simplicity, K_{MCML} and K_{CMOS} are set as 0.5 mW/GHz and 0.25 mW/GHz respectively. It is assumed that the power consumption of one MUX is

half of one MCML divide-by-2 stage, while K_{DFF} is equal to K_{CMOS} since the dynamic divider-by-2 unit is implemented with a toggled DFF. Figure 3.18 shows the power consumption for three different phase switching techniques at different operating frequencies where six stages are used. For other configurations, similar results are obtained as well.

The additional power consumption, represented as $(K_{MUX} + K_{DFF})\frac{f_{in}}{2^{n+1}}$, decreases with the increase of the division ratio. The total power consumption will decrease with the increase in the number of stages. For example, if the stage changes from four to six, the divide-by-2 stages are added at the divide-by-2 chain. Because the operating frequency of the phase switching blocks is divided by four, the total power consumption still reduced. Figure 3.19 shows the power consumption of a 4-to-1 phase switching prescaler with the different number of stages (4,6,8 and 10) while other parameters are kept the same. From this observation, the phase switching technique is suitable for the prescaler of large division ratios compared with the traditional topology with a divide-by-4/5 or divide-by-2/3 unit [59].

3.3.2 Imbalanced phase switching technology

All the previous work is based on the phase signals of 50% duty cycle. However, it is not necessary for the phase signals to have a 50% duty cycle since the following stages are edge-triggered. As long as the output of the phase switching block provides a correct rising edge, the prescaler will work properly. In the topology of 2-to-1 phase switching as shown in Figure 3.16.b, if we manually change the duty cycle, for example, by using two AND functions at the four output phases

($F4I$, $F4Q$, $\overline{F4I}$, and $\overline{F4Q}$), we can get two output signals of $\frac{1}{4}$ duty cycle (P1 and P2) as shown in Figure 3.20.a. Such a step offers a great improvement in the delay budget for the phase switching block. If the phase switching is carried out between *P1* and *P2*, for the *N/N+1* method in [56], the correct timing window is $\frac{T2}{4}$ (in [56], the value is 0) as shown in the shaded area of Figure 3.20.a, where *T2* is the period of *P1* and *P2*. If the reverse switching method in [58] is used, as long as the switching between these two signals is within $\frac{T2}{2}$ ($\frac{T4}{4}$), the glitch can be avoided as shown in Figure 3.20.a. Hence, the delay budget of the 4-to-1 phase switching technique in [40] can be achieved with the proposed 2-to-1 phase switching. Consequently, the power consumption is reduced as given by above equations. We can apply this method to the 4-to-1 phase switching topology in [40] as shown in Figure 3.20.b. Here $F4I$, $F4Q$, $\overline{F4I}$, and $\overline{F4Q}$ are replaced with the $\frac{1}{4}$ duty cycle phase signals *F41, F42, F43* and *F44*, which are of a 90-degree phase difference respectively. For the divide-by-*N/N+1* method, for example, the signals shift from *F42* to *F43*, the delay budget will be $\frac{T4}{2}$ as shown shaded. Hence, a 100% increase in the delay budget is achieved compared with that in [40]. If the divide-by-(N-1)/N method in [58] is used, when the output switches from *F43* to *F42*, the correct timing window for switching is also enlarged and the period of logic "0" will be larger as shown shaded in the lower part of Figure 3.20.b. Hence, an improved delay budget is achieved. This improvement in the delay budget will increase the operating frequency of the prescaler since the major

constraint of the operating frequency in the phase switching prescaler lies in the delay budget of the phase switching.

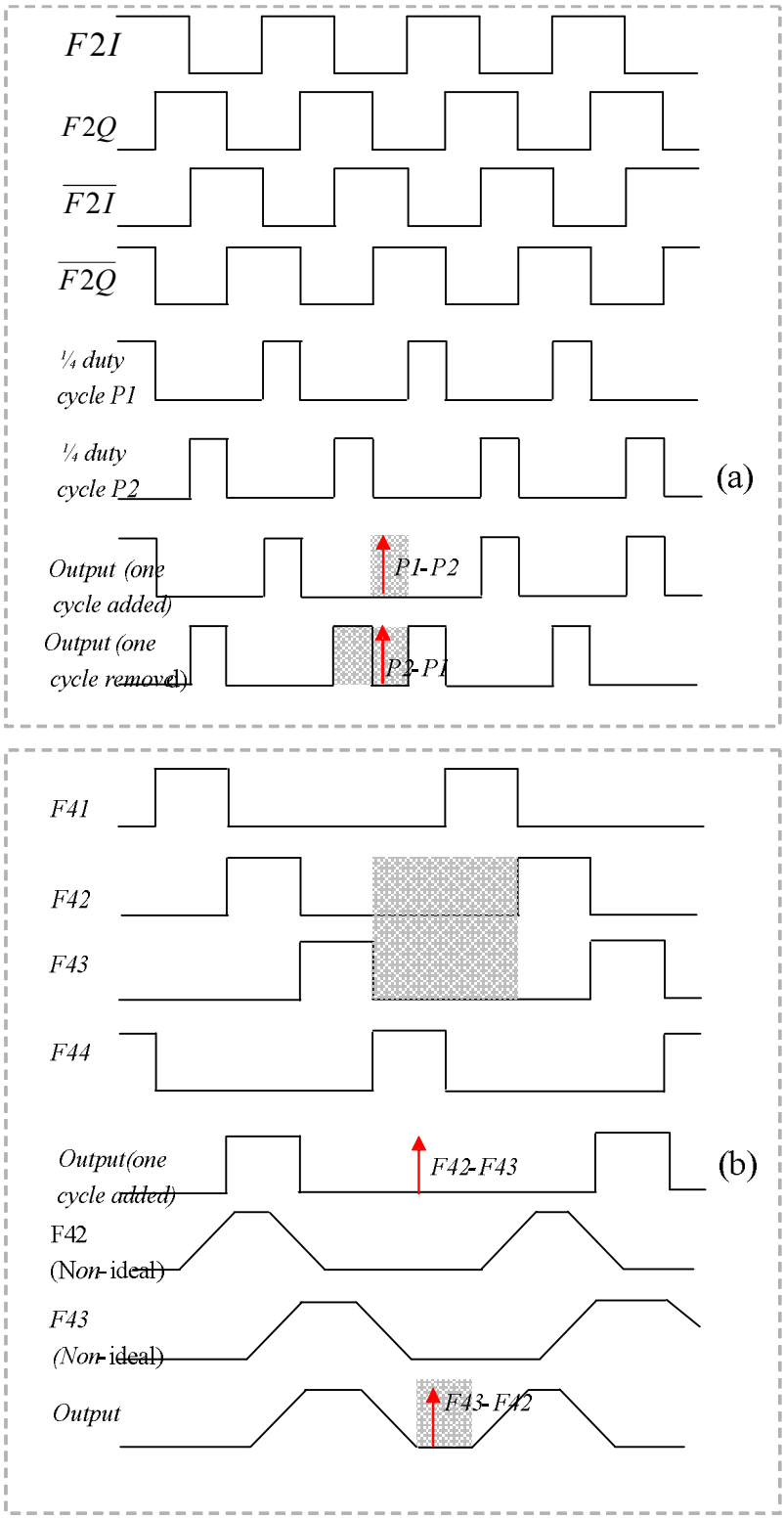
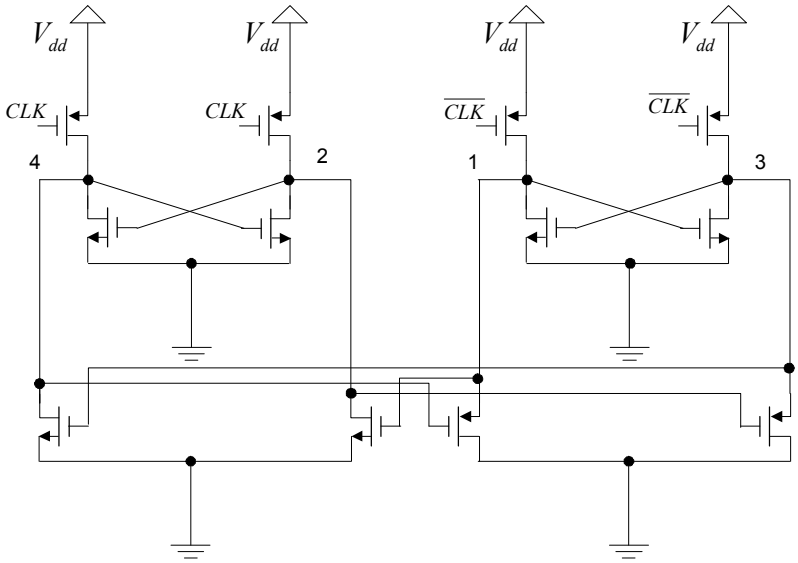
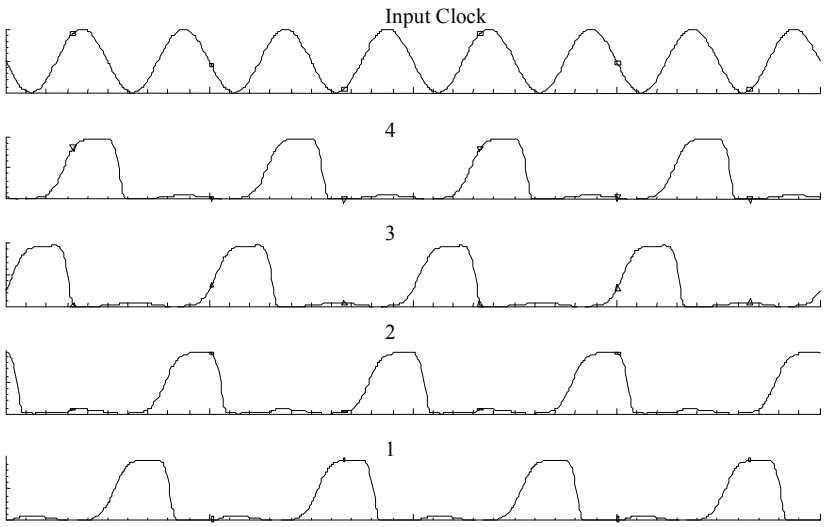


Figure 3.20: The operation of the imbalanced phase switching
a) 2-to-1 phase switching, b) 4-to-1 phase switching

3.3.3 Design of prescaler with the imbalanced phase switching technique



(a)



(b)

Figure 3.21: Divider in [102]

a) Topology, b) 1/4 duty cycle output signals

To verify the merits of this technique, the prescalers based on the topology of 2-to-1 [56] and 4-to-1 [40] phase switching implemented with the proposed technique have been constructed. AND gates can be used to obtain the $\frac{1}{4}$ duty cycle phase

signals [60]. However, the operation of the AND gate at $\frac{F_{in}}{2}$ will introduce additional power consumption which will greatly hamper the overall performance. As a result, there will be no advantage of the power consumption in the proposed topology. The solution without any trade-off is to use a frequency divider which is able to provide the imbalance phase signals directly. So the high speed non-differential frequency divider proposed in [102] is used to provide the $\frac{1}{4}$ duty cycle phases. Figure 3.21 shows the topology and four output signals of the frequency divider reported in [102].

The $\frac{1}{4}$ duty cycle phase signals are generated without any additional block. Two proposed prescalers are based on the same architectures as shown in Figure 3.16.a and Figure 3.16.b except that the divide-by-2 unit before the phase switching block is replaced with the divider given in [102]. For the other blocks, we follow the blocks reported in [58] with standard CMOS digital circuits. The high speed divide-by-2 units are implemented with the MCML toggled DFF in [58]. While the low speed divide-by-2 chain consists of the cascaded TSPC divide-by-2 units. The four-state machine which has been described in detail in [58] has been implemented with the circuit proposed in [30]. Theoretically, this 2-to-1 phase switching divide-by-(N-1)/N prescaler will be able to operate at a frequency comparable to that of the divide-by-N/N+1 in [40] while maintaining a simpler architecture. The 4-to-1 phase switching divide-by-(N-1)/N prescaler will be able to work at the highest frequency as compared to that of the prescalers implemented with the traditional 50% duty cycle phase switching technique. To illustrate the advantage of the imbalanced phase switching technique over the traditional

technique, 4-to-1 phase switching divide-by-*N*/*N*+*1* and divide-by-(*N*-*1*)/*N* prescalers based on the 50% duty cycle signals as reported in [40] are also constructed for a comparison. This comparison eliminates the difference of the performance due to the different processes. All the prescalers use the CSM 0.18 μm CMOS process with the same transistors' sizes.

Moreover, to achieve the multi-modulus, a MUX can be used to select the output signals between the different stages of the output. For example, as shown in Figure 7.7, in the divide-by-2 chain, if the first stage's output is used as the output, the output signal is divide-by-7/8, otherwise the output will be divide-by-15/16. Because of the low operating in the MUX, the additional power consumption is small. By this means, the application of a dual-band division (i.e. 2-3 GHz and 5-6 GHz) is feasible.

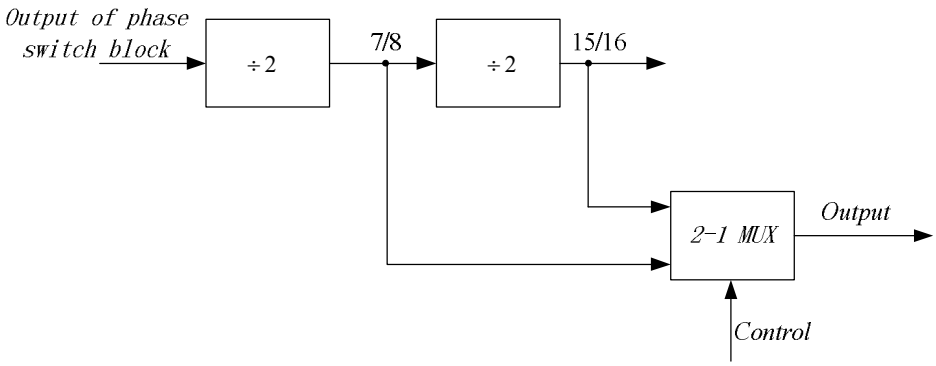


Figure 3.22: **Multi-modulus applications**

3.3.4 Simulation and silicon verifications

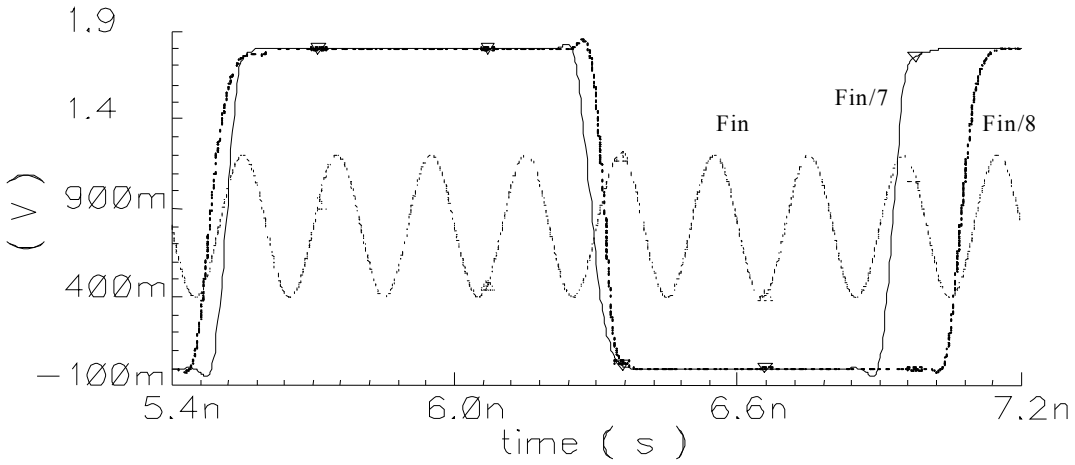


Figure 3.23: Simulated input and output waveforms of the proposed prescaler

The simulations of the prescalers are performed using the Cadence SPECTRE RF for the CSM 0.18 µm CMOS process. Figure 7.8 shows the simulation result of the output signal of the proposed 2-to-1 phase switching prescaler (divide by 7 and by 8) with a 5 GHz input, while it is able to work properly up to 6 GHz with a supply voltage of 1.8 V. Owing to the novel technique and its simple architecture, the proposed circuit can function well over the frequency range from 1.5 GHz to 6 GHz with the low power consumption.

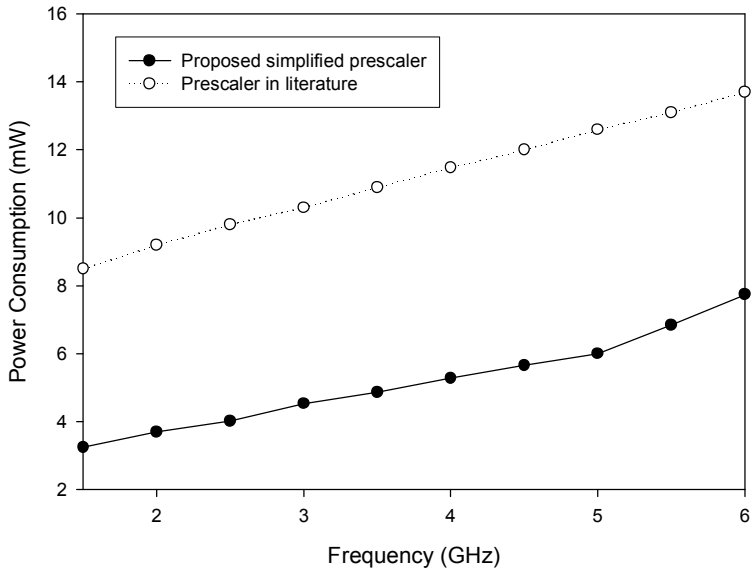


Figure 3.24: Power consumption vs. operating frequency of the proposed 2-to-1 phase switching prescaler and the 4-to-1 phase switching prescaler in [40]

Figure 3.24 summarizes the power consumption versus the operating frequency range of the proposed 2-to-1 phase switching divide-by-7/8 prescaler and the traditional 4-to-1 phase switching divide-by-8/9 prescaler with 50% duty cycle signals. (the divide-by-8/9 prescaler in [40] also achieves a maximum operating frequency of 6 GHz). Over the operating frequency range, it is observed that the proposed prescaler achieves a significant reduction of the power consumption due to the simplified structure while it maintains the same operating frequency with the prescaler in [40]. For the 6 GHz input, the power dissipation of the proposed prescaler is only 7 mW. The merits come from the increase of the delay tolerance comparable to the 4-to-1 phase switching while maintaining a simpler topology. If the one cycle removing method in [58] is used for the topology in [40], the maximum operating frequency of the divide-by-7/8 prescaler with 50% duty cycle phase switching will be 7.5 GHz. For the proposed 4-to-1 phase switching, its power consumption is 15 mW, only 3 mW more than that of the prescaler in [40].

However, its operating frequency can reach 10 GHz due to the increased delay budget in the phase switching block.

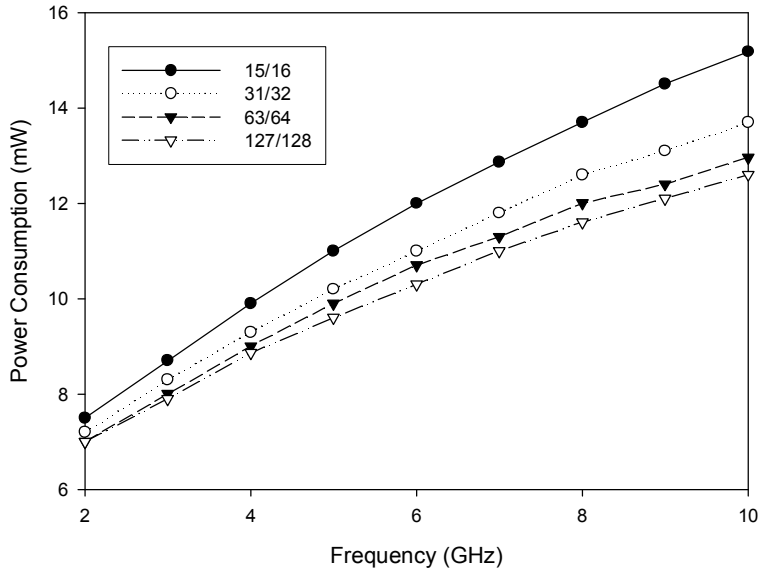


Figure 3.25: Power consumption vs. operating frequency of the proposed 4-to-1 phase switching prescaler with different division ratios

Figure 3.25 summarizes the power consumption over the operating frequency of this prescaler, which shows the prescaler achieves an operating range of 2 GHz to 10 GHz. The results for different division ratios agree well with the above analysis that for an increment of the division ratio, the power consumption of the prescaler will decrease due to the reduction of the power consumption of the phase switch control block. Table 3.1 compares two proposed prescalers with other work in the literature in terms of the building blocks, glitch performance, operating frequency and power consumption.

Table 3.1: Comparison to other published prescalers

Work	Phase switching	Additional blocks	Technology (μm)	Frequency (GHz)	Power (mW)
[40]	4-to-1 MUX	4 state machine	0.7 CMOS	1.75	24(measured)
[56]	2-to-1 MUX	No	0.5 CMOS	1.5	1.7(measured)
[57]	4-to-1 MUX	Re-timer 4 state machine Decoder	0.25 CMOS	5	/
[57]	8-to-1 MUX	Divide-by-2 XOR gate 8 state machine	0.18 CMOS	6/8	11.3/12.3 (Simulated)
Simulated 4-1in [40] for divide-by-8/9	4-to-1 MUX	4 state machine	0.18 CMOS	6	13 (Simulated)
Simulated 4-1in [40] for divide-by-7/8	4-to-1 MUX	4 state machine	0.18 CMOS	7.5	13 (Simulated)
Proposed 2-1	2-to-1 MUX	No	0.18 CMOS	6	7 (Simulated)
Proposed 4-1	4-to-1 MUX	4 state machine	0.18 CMOS	10	15 (Simulated)

The proposed prescaler is fabricated in the CSM 0.18 μm CMOS process. Figure 3.26 shows the die photo of a 4-to-1 phase switching prescaler with dual band application. The die size is about $500\mu m \times 450\mu m$ including the test buffer and pads. Due to the limitation of equipment, only the single-end sine input below 4 GHz is available. Therefore, the fully integrated Balun [61] is needed to provide a differential input for the prescaler. However, in the application of 4 GHz, the method proposed in [102] using the trans-gate and an inverter to obtain the differential signals is sufficient even though this method has a larger phase imbalance. Moreover, due to the limitation of large size RFMOS provided by the CSM, the power consumption of first two stage of the prescaler will be larger than

the previous simulation. The post-layout simulation shows the power consumption of the proposed prescaler is 28 mW.

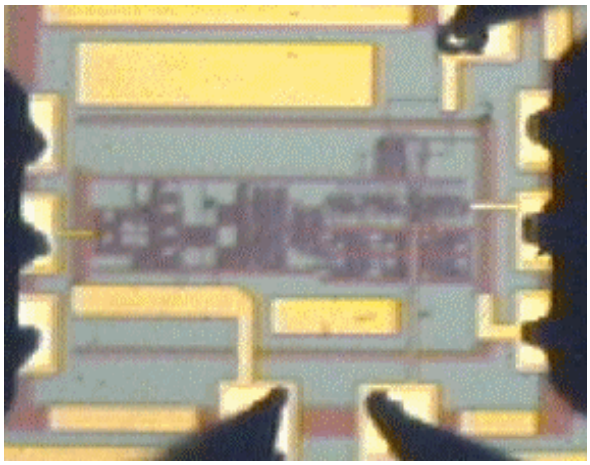
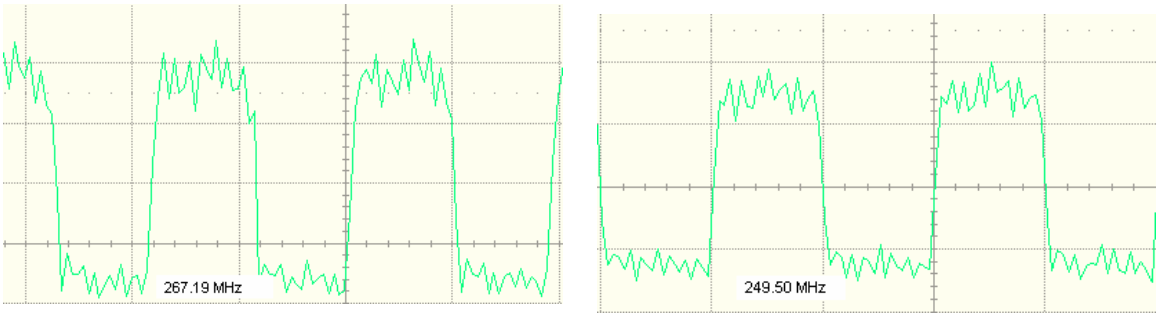
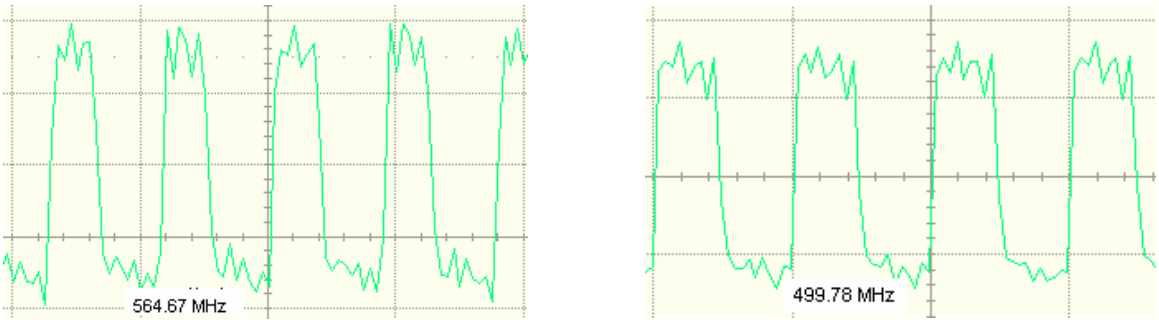


Figure 3.26: Die photo of the proposed phase switching prescaler



(a)



(b)

Figure 3.27: Operation of the proposed phase switching prescaler

On wafer tests are carried using the Cascade RF probe station. The input signal for the measurement is provided by the HP E4433B 0.25 MHz-4 GHz signal generator, while the output signals are captured by Lecroy Wavemaster 8600A 6G oscilloscope. Figure 7.12 shows the measured transient results of the prescaler with an input of 4 GHz for a 1.8 V supply voltage. The operations of dual-band and dual-modulus have been achieved. The power dissipation is 32 mW for the test chip which agrees well with the simulation result with RFMOS. The proposed 4-to-1 phase switching prescaler is also fabricated with the normal MOS provided by CSM to verify the low power operation. Figure 3.28 shows the die photo of this prescaler. It is able to work properly from 1 GHz to 4 GHz (limitation of input source) with 1.5 V supply voltage. Figure 3.29 summarizes the power consumption vs. operating frequency of this prescaler. The current dissipation is only 6.6 mA at 4 GHz. This agrees well with the simulation results shown in Figure 3.25.

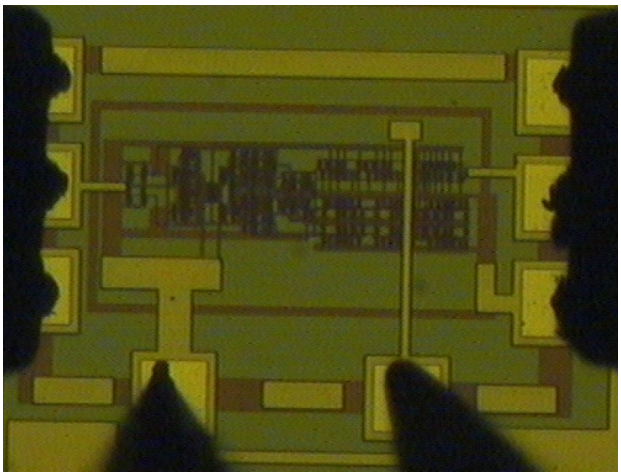


Figure 3.28 Die photo of the 4-to-1 phase switching prescaler

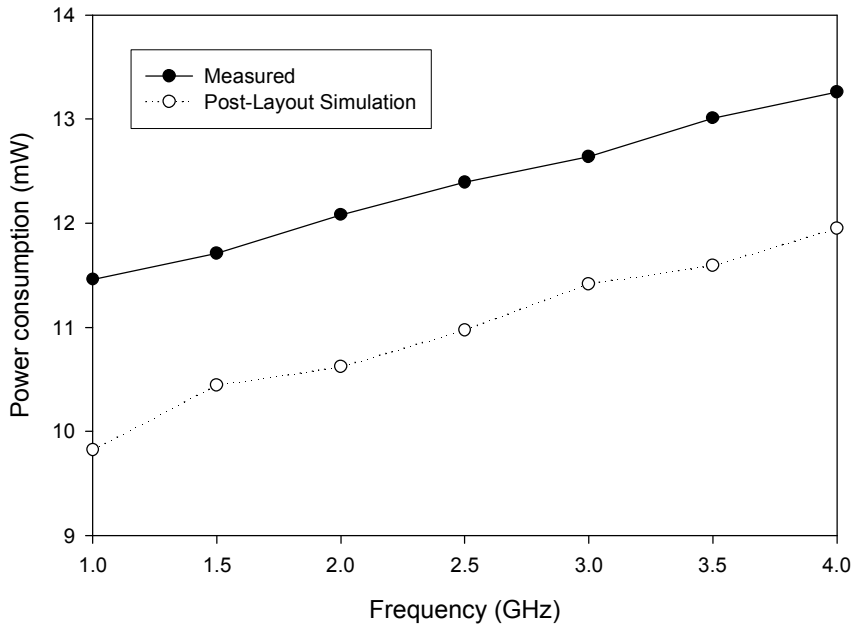


Figure 3.29 Power consumption vs. operating frequency

3.4 Conclusion

In this chapter, two topologies for high-speed prescalers are presented.

Firstly, the power consumption and operating frequency of the extended true-single-phase-clock (E-TSPC) based frequency divider is investigated. The short circuit power and the switching power in the E-TSPC based divider are calculated and simulated. A new low power divide-by-2/3 unit of a prescaler is proposed and implemented using a CMOS technology. Compared with the existing design, a 25% reduction of power consumption is achieved. Simulation results show that a divide-by-8/9 dual-modulus prescaler implemented with this divide-by-2/3 unit using a 0.18 μm CMOS process is capable of operating up to 4.5 GHz for a 1.8 V supply voltage with 1.5 mW power consumption. The prescaler's performance is verified by the measurement results.

A novel imbalanced phase switching technique for the high speed prescaler design is investigated. Different from the traditional 50% duty cycle phase switching

technique, it uses $\frac{1}{4}$ duty cycle phases to increase the delay budget in the dual-modulus control. It significantly improves the performance of the prescaler in the operating frequency and power consumption, compared with the existing 50% duty cycle phase switching technique. This improvement makes it possible for applications in the ultra high speed CMOS prescaler design. Two prescalers, with 2-to-1 and 4-to-1 phase switching, are designed using this technique. The proposed 2-to-1 phase switching divide-by-7/8 prescaler with the simplified topology using the CSM 0.18 μm CMOS process is capable of operating from 1.5 GHz to 6 GHz for a 1.8 V supply voltage with 7 mW power consumption. Such operating frequency ranges cover most of the wireless LAN standards. The prescaler with 4-to-1 phase switching can work from 2 GHz to 10 GHz with a power consumption of 15 mW for a supply voltage of 1.8 V in simulation. The performance of prescaler is silicon verified with RFMOS and normal MOS. The proposed method is promising in the application of multi-GHz CMOS prescaler design without any trade-off.

A part of this chapter is published in [62].

Chapter 4

Design of a Low Power Wide Band High Resolution Programmable Frequency Divider

4.1 Introduction

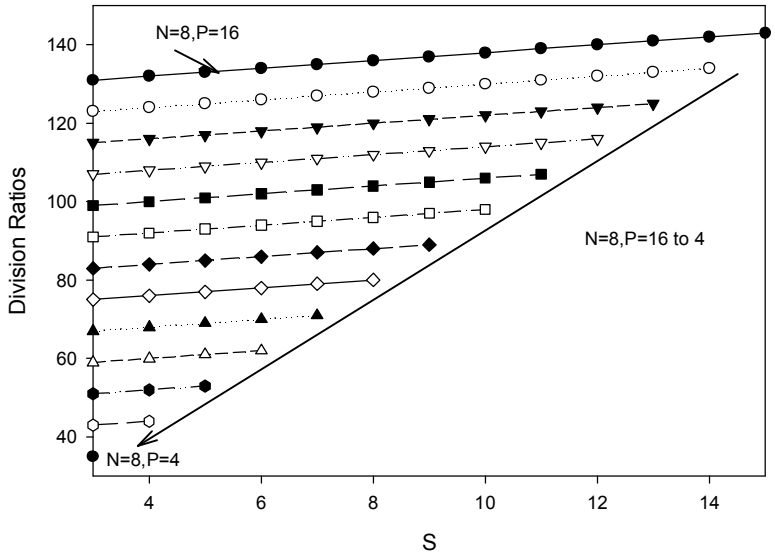
Frequency synthesizers have been the basic building blocks in modern communication systems. The operating frequency of the frequency synthesizer is limited by that of the frequency divider and the voltage-controlled oscillator. The function of the channel selection in the frequency synthesizer demands the programmable division ratios for the frequency divider. The integer-N frequency synthesizers are more practical, less costly and of low spurious sideband performance as compared with the fractional-N frequency synthesizer [38]. For radio frequency applications, the integer-N frequency divider is usually formed by a prescaler, a program counter (P counter) and a swallow counter (S counter). Such a topology can provide a programmable division ratio of $N \times P+S$, where N, P and S are the division ratios of three blocks respectively. The prescaler provides a dual-modulus of $N/N+1$. The P counter provides a fixed division ratio according to the requirement of the overall division ratio, while the continuous division ratios from 3 to 2^n is achieved through the S counter by periodically reloading the divide-by-2 stages, where n is the number of stages of the S counter. The continuous division ratio is used to select the desired channels. Much research has been focused on the prescaler design for its highest operating frequency [59]. However, in the modern communication system, there is an increasing demand for multi-standards applications. For example, in the 5-6 GHz band, there are HIPERLAN I/II and

IEEE 802.11a standards, they work within the similar band but at different centre frequencies and channel spacings. Although many frequency synthesizers for the 5-6 GHz wireless LAN applications have been reported [2] [38], the requirement for wide band and high resolution operations continue to be the problems. To satisfy these requirements, different reference frequencies, and different arrangement for *N*, *P* and *S* counters are selected for different applications [38] [99]. For example, only the UNII bands are covered in [2] [38]. In this chapter, a new wide band high resolution programmable frequency divider is proposed. The wide band and high resolution are obtained by using the all-stage programmable topology in both counters. A programmable counter using a new D flip-flop is able to operate at higher frequencies with lower power consumption compared with that of the existing designs.

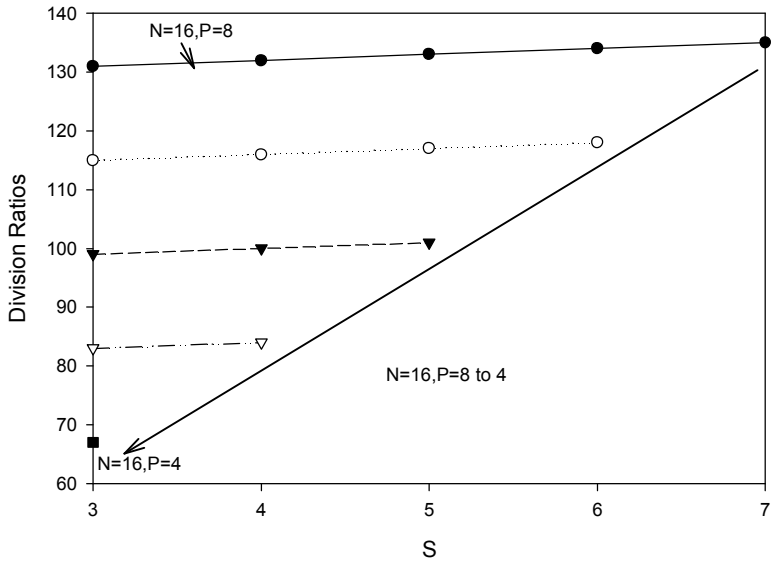
4.2 Design consideration

The high speed digital frequency divider is usually formed by cascading divide-by-2 stages. However, this method will only give the division ratios equal to the power of 2. The reloadable digital counter offers a better solution providing a frequency division ratio continuously ranging from 3 to 2^n, where n is the number of divide-by-2 stages [63]. In a reloadable counter, the number of the input pulses is accumulated until it is equal to a preset value when the counter is reloaded. By changing the preset value, a programmable division ratio is achieved. The counter is fully programmable if all the divide-by-2 stages are reloadable. Each of this reloadable stage is called a bitcell. In many existing design of integer frequency dividers, the *N* and *P* are fixed while the *S* is variable to get the desired output

frequencies [38]. If both the P counter and S counter are programmable, more division ratios can be obtained.



(a)



(b)

Figure 4.1: Division ratios available

a) *N*=8, *P* from 4 to 16 and *S* from 3 to 15 b) *N*=16, *P* from 4 to 8 and *S* from 3 to 7

For example, as shown in Figure 4.1.a, we set *N*=8, *P* from 4 to 16 and *S* from 3 to 15 while *S* is always smaller than *P*. The division ratios are fixed to one of the curve for a fixed *P*. If *P* is variable, the number of the variable division ratios increases significantly. As shown in Figure 4.1.b, *N* is set at 16, *P* changes from 4 to 8 to get the same range of division ratios as in Figure 4.1.a. The available division ratios have, however, been reduced significantly due to the smaller range for *P* and *S*. Thus, for a desired operating band, the high resolution can be obtained by using a smaller division ratio for the prescaler while increasing the range of the counter's division ratios.

However, in the design of such a wide band high resolution frequency divider, the digital counter must be able to operate at high operating frequencies within the constraints of a low power consumption. Therefore, the design of a high speed low power counter is the key consideration. The key parameters of high speed digital circuits are the operating frequency and the power consumption.

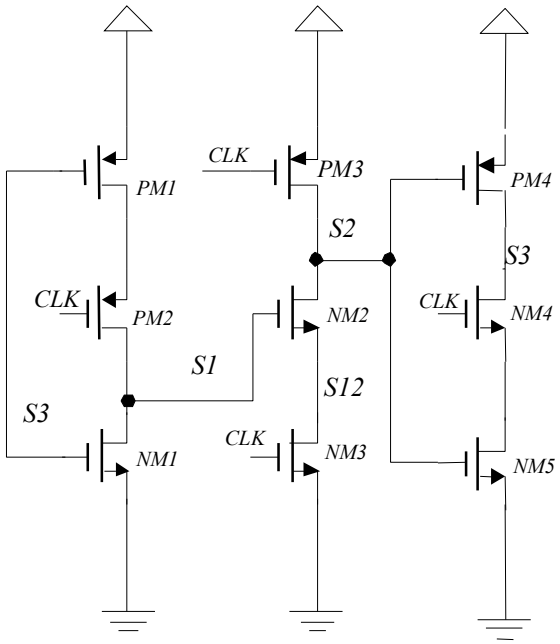


Figure 4.2: Toggled TSPC DFF as a divide-by-2 unit

The toggled TSPC DFF is the most popular divide-by-2 unit in the single-end frequency divider design due to its high operating frequency and low power consumption [52]. Its maximum operating frequency is inversely proportional to the propagation delay [64].

Figure 4.2 shows a toggled TSPC divide-by-2 unit. The low-to-high transition of the output of signal *S3* includes two steps. At the rising edge of *CLK* , node *S2* is pulled down to ground, then *S3* is charged to the logically high since *PM4* is turned on when *S2* has a logic low. Therefore, t_{pLH} is the sum of the delay of these two steps, while t_{pHL} can be determined from the discharging of *S3*.

The major power consumption of a TSPC divide-by-2 unit is the sum of the switching power for the three stages:

$$P_{swithing} = \sum_{i=1}^{3} f C_{Li} V_{dd}^{\ 2} \tag{4.1}$$

For the toggled divide-by-2 unit, the clock for individual blocks is half of the input clock.

As the values of these MOS capacitors can be determined by the process parameters [48], the propagation delay of the TSPC divide-by-2 unit can be obtained by manual calculation. The propagation delay is also obtained by a simulation using the Cadence SPECTRE RF for the CSM 0.18 μm CMOS process. In the high speed digital circuit, for lower load capacitor, the length of transistors is kept at the minimum (0.18 μm). For simplicity, the ratio of the width of PMOS over the width of NMOS is 2 [53] and all PMOS transistors all have the same width which are twice the width of all NMOS transistors.

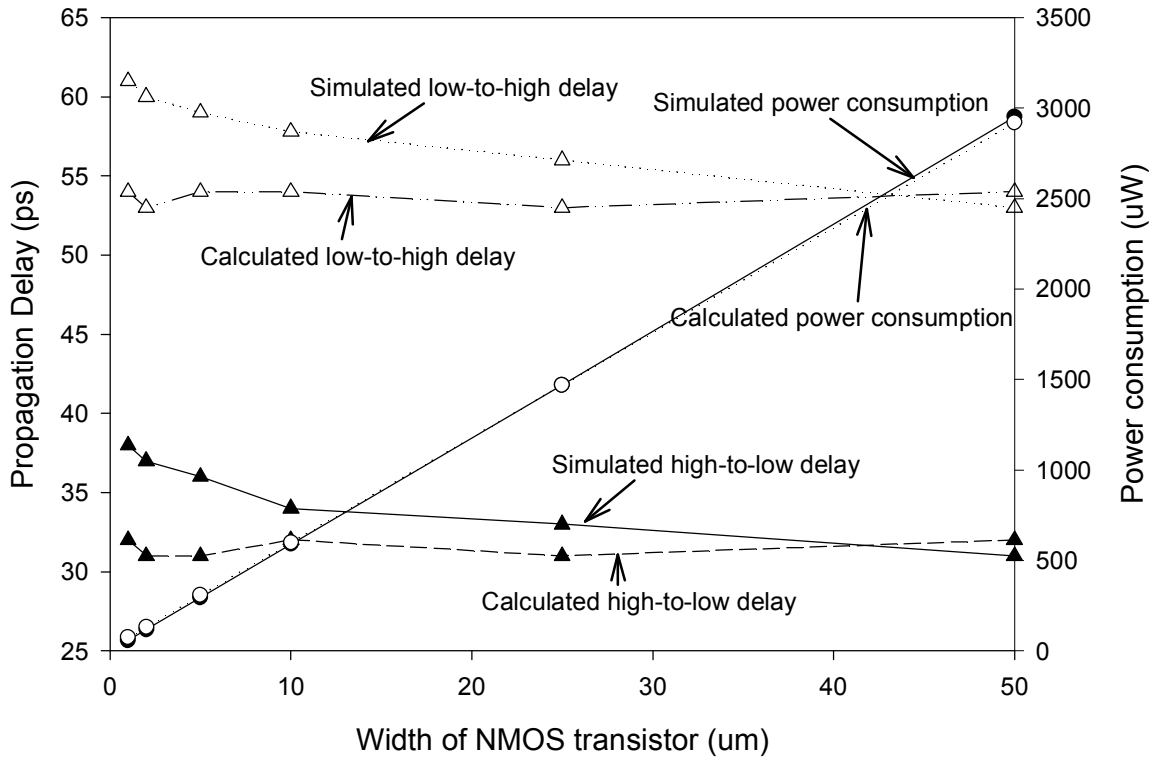
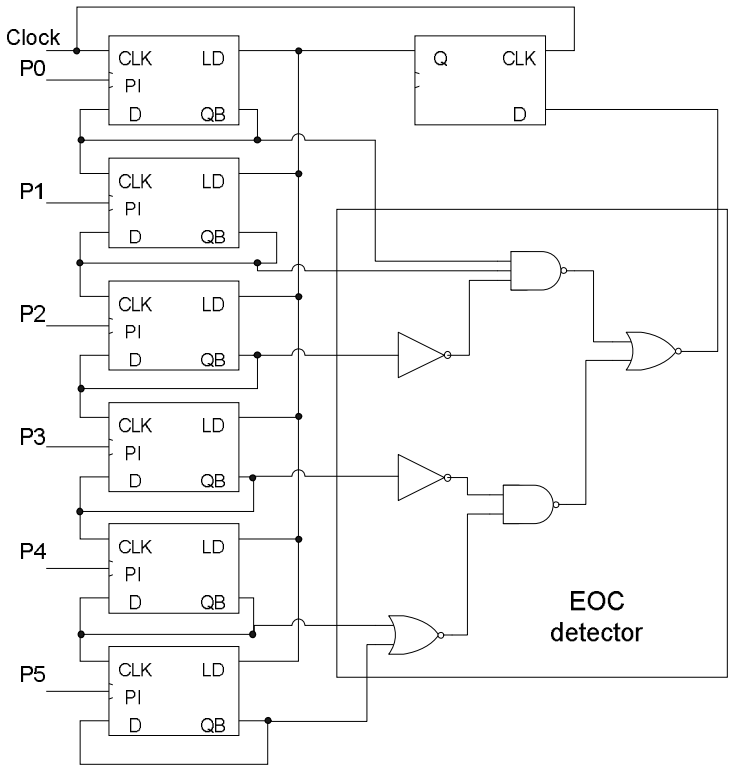


Figure 4.3: The propagation delay and power consumption of the TSPC divide-by-2 unit

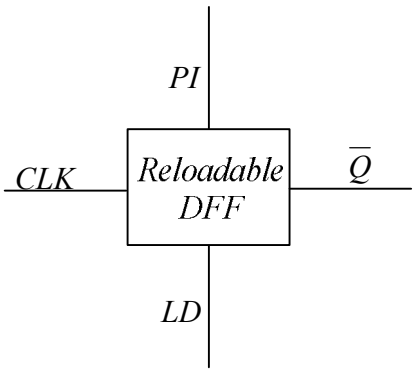
Figure 4.3 shows the calculated and simulated propagation delay and power consumption of the TSPC divide-by-2 for different sizes of MOS transistors as that of the divide-by-2 units. Here the load is an inverter which has the same sizes of MOS transistors. With the increase of W/L, the propagation delay remains almost constant, while the power consumption increases linearly. Because the equivalent resistance is inversely proportional to W/L, while the load capacitance increases linearly with the width of the transistor, as a result, the RC delay remains almost constant. The power consumption is linearly proportional to the load capacitance which is decided by the width of the transistor.

4.3 Design of a high speed low power digital counter

The toggled TSPC DFF can only function as a divide-by-2 stage. However, the programming function of the frequency divider requires the bitcell to be reloadable. The general topologies of the counter [63] and the reloadable bitcell are shown in Figure 4.4.a and Figure 4.4.b.



(a)



(b)

Figure 4.4: A general topology of the digital counter

a) topology of counter b) the bitcell

For each bitcell, if the reload signal LD is logically low, the bitcell is functioning as divide-by-2. When LD is logically high, the input data signal will be disabled, and the programmable bit signal PI will be loaded to output. Because the reload can be triggered at any time, the total propagation delay, the sum of the divide-by-2 delay and the reload delay, decides the maximum operating frequency. As the reload function is only triggered once within the entire division cycle, for a division ratio much larger than 2, the power consumption when the bitcell is functioned as a divide-by-2 unit can be regarded as the power consumption of the bitcell. In [65], a novel reloadable TSPC-based bitcell is proposed as shown in Figure 4.5. In this bitcell, the upper block which is a traditional 9-transistor TSPC D flip-flop (DFF) functions as a divide-by-2 unit, while the lower part provides the reload function. With the input of signal LD, $PM5$ will pull up the output to logically high or to keep it at logically low depending on the value PI.

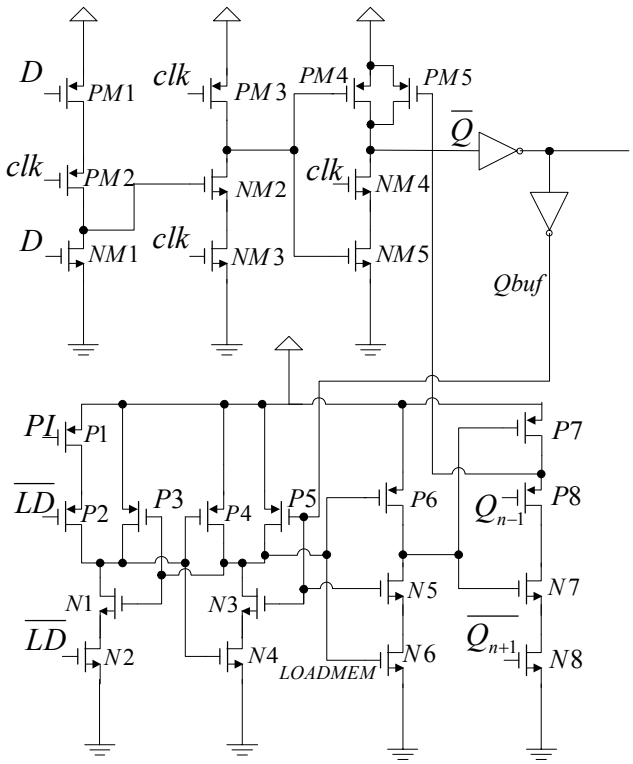


Figure 4.5: Schematic of the bitcell in [65]

The same analysis on the power consumption and propagation delay can be performed in this bitcell as well. When *LD* is logically low, the bitcell is a divide-by-2 unit. In difference with a single TSPC unit, C_{dbPM5} will be added to the load capacitance for the final stage. The other delay is the reload delay， which is defined as the propagation delay of *PI* to the output. During the reload, *PI* is first loaded to *LOADMEM*. At the next arrival of *Qbuf*, the value is loaded to *PM5*, which will change the output value. This step (from *LOADMEM* to $\overline{Q}$) includes three stages of the propagation delay. The step of reload has a larger delay than that of the TSPC divide-by-2 operation. Compared with a toggled TSPC divide-by-2 bitcell, the additional power consumption in this bitcell can be considered as due to the additional inverters' switching power, while *P5* creates a short circuit power because the direct path is established periodically with the switching of *N3*. Moreover, *N3* is also periodically switched by *Qbuf*.

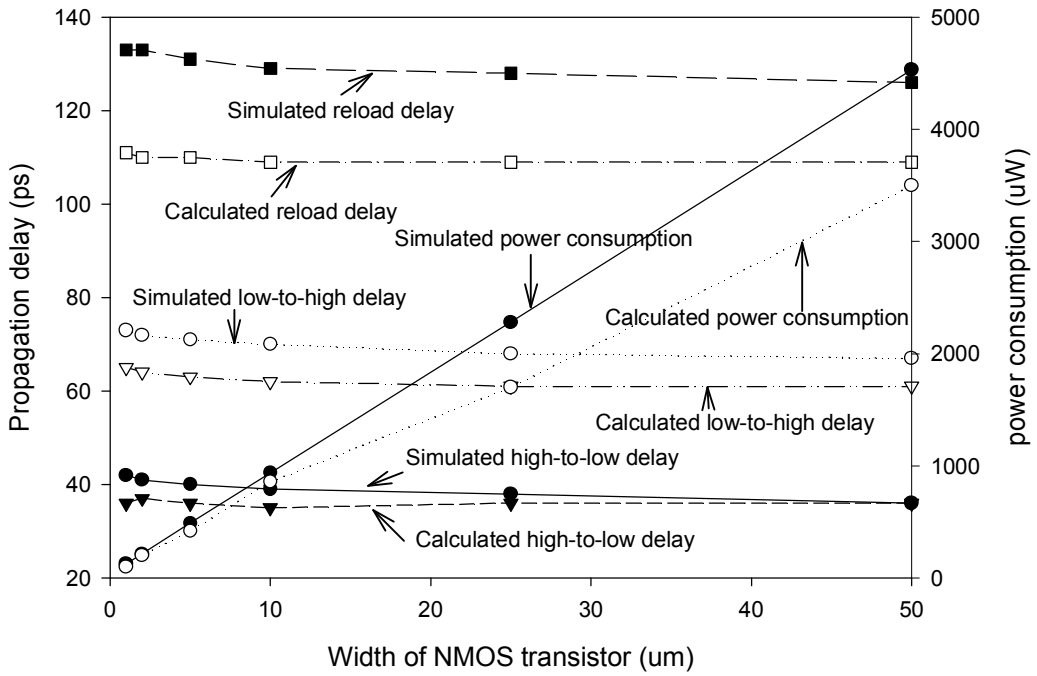


Figure 4.6: The propagation delay and power consumption of the bitcell in [65]

Figure 4.6 shows the calculated and simulated propagation delay and power consumption for this bitcell. Compared with a single TSPC divide-by-2 stage, the power consumption and propagation delay increase greatly. Moreover, as *PM5* is used to pull up the output signal to logically high without a complementary NMOS, the output voltage may settle at a middle value during the reload since *NM4* and *NM5* will be turned on periodically. Finally, the bitcell has a complex structure with 30 MOS transistors.

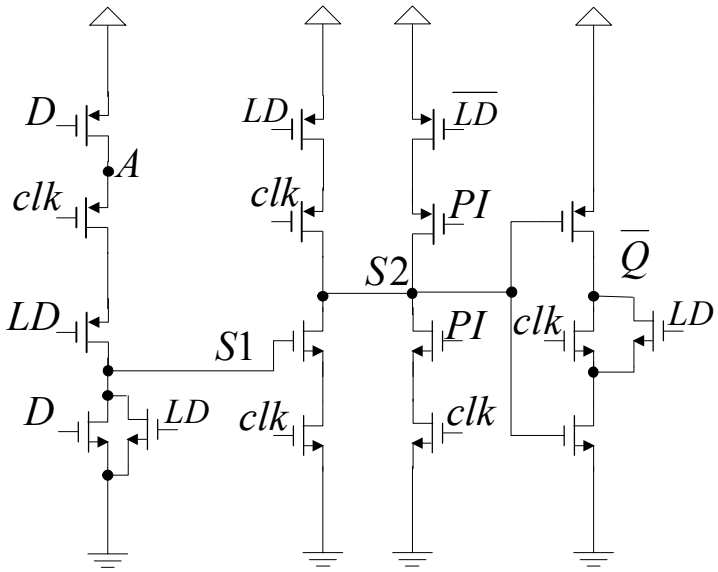


Figure 4.7: The schematic of the bitcell in [66]

A novel bitcell with an integrated reload function into the TSPC based D flip-flop is first proposed in [66] [67] as shown in Figure 4.7. In this bitcell, if *LD* is logically low, the bitcell performs the divide-by-2. When *LD* is logically high, node *S*1 is discharged to "0" to isolate the input signal *D* from output signal $\overline{Q}$. At the same time, nodes *S*2 , *S*3 and $\overline{Q}$ are made transparent to the loaded value *PI* . This bitcell greatly reduces the circuit complexity of the reloadable bitcell in [65]. However, it suffers a glitch at the high frequency as shown in Figure 4.8.

Since the LD signal is the logical result of outputs of all stages of the counter, LD will lag behind D. If the output has changed from logic high to low and LD becomes logically high to load PI with a high at the output, because of the late arrival of LD, the output will generate a glitch as shown in Figure 4.8. Such a glitch will cause an erroneous trigger to the next stage if a programmable counter based on [66] is used as illustrated in Figure 4.8. The glitch will charge up the node A of the next stage of the bitcell to a logic high which will consequently charge node $S1$ to high after LD becomes a logic low ($S1$ is transparent to node A when LD is logically low). Consequently, $S2$ will be pulled down and the output of this bitcell will be high.

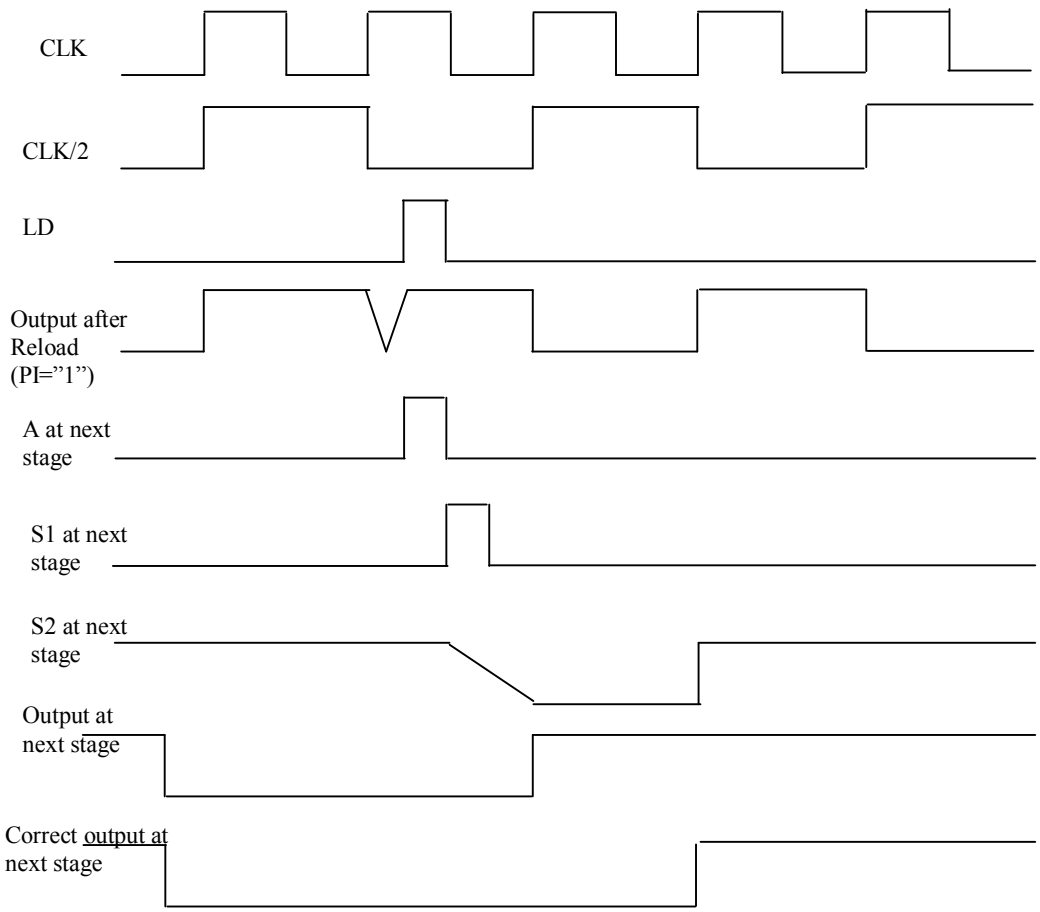


Figure 4.8: The glitch in the bitcell in [66]

A new bitcell is proposed which has an improved architecture to solve the impact of the glitch as shown in Figure 4.8. $\overline{Q}$ is fed to node D when the bitcell performs the divide-by-2 function. It is modified from the bitcell proposed in [68] and based on the similar method as in [66]. The number of MOS transistors has been reduced. Moreover, to achieve a higher operating frequency, the critical path for the signal has been optimized by placing the LD or $\overline{LD}$ controlled MOS transistors near the supply voltage or ground. In the proposed bitcell, during reload, $\overline{PI}$ is loaded to $\overline{Q}$ instead of $S2$ to reduce the delay from PI to the output. Moreover, in the proposed bitcell, there is a LD controlled feedback to remove the erroneous charge in $S2$ during the reload. The charge at node A will have no impact on node $S2$. Therefore the charging voltage in the node A will not cause an erroneous trigger to the next stage of the bitcell. As a result, the glitch in [66] will not have any impact on the proposed bitcell based frequency divider. The power consumption of the LD controlled inverter is negligible since the reload is only triggered once in a whole division cycle. The problem of the glitch in the bitcell of [66] has been solved effectively without any trade-off.

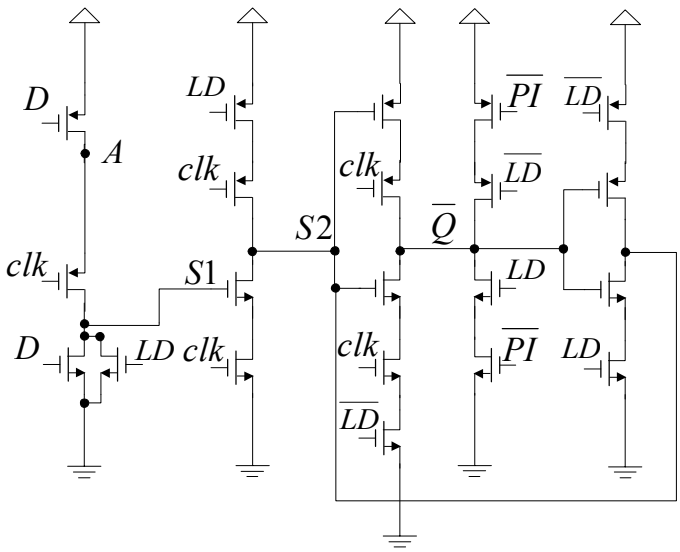


Figure 4.9: The schematic of the proposed bitcell

The power consumption of the proposed bitcell can still be analyzed based on the switching activities for the devices. When LD is logically low, the right side is disabled, while the left side is a toggled TSPC divide-by-2 unit. The MOS devices on the right side will be the load capacitors of the divide-by-2 unit. The increase of the power consumption as compared with the other bitcells can be calculated and simulated by adding the capacitances to that of a TSPC divide-by-2 unit.

For the propagation delay of the bitcell, if LD is logically low, the bitcell functions as a divide-by-2 unit. The right side of the bitcell is blocked, while at the left side, LD and $\overline{LD}$ controlled PMOS and NMOS will be switched on constantly and can be modeled as fixed resistors, which can be treated as a source resistor for the switching MOS transistors [48]. The equivalent resistance and capacitance can be obtained from the equations in [48]. When LD is logically high, the left side of the bitcell is blocked, $\overline{PI}$ is loaded to $\overline{Q}$ by only passing one stage of LD controlled inverter. The total delay for the proposed bitcell is still less than that of previous bitcells even though the delay for this divide-by-2 increases due to the additional load capacitances.

Figure 4.10 shows the calculated and the simulated propagation delay and power consumption of the proposed bitcell and of the bitcell in [65]. Here the propagation delay is the sum of the divide-by-2 and reload delays. The proposed bitcell achieves about 20% reduction from the power consumption of the bitcell in [65]. The total delay of the proposed bitcell is much lower than that of the previous bitcell due to the great reduction in the reload delay. Since the operating frequency is inversely proportional to the propagation delay, about 25% improvement of the operating frequency is foreseeable.

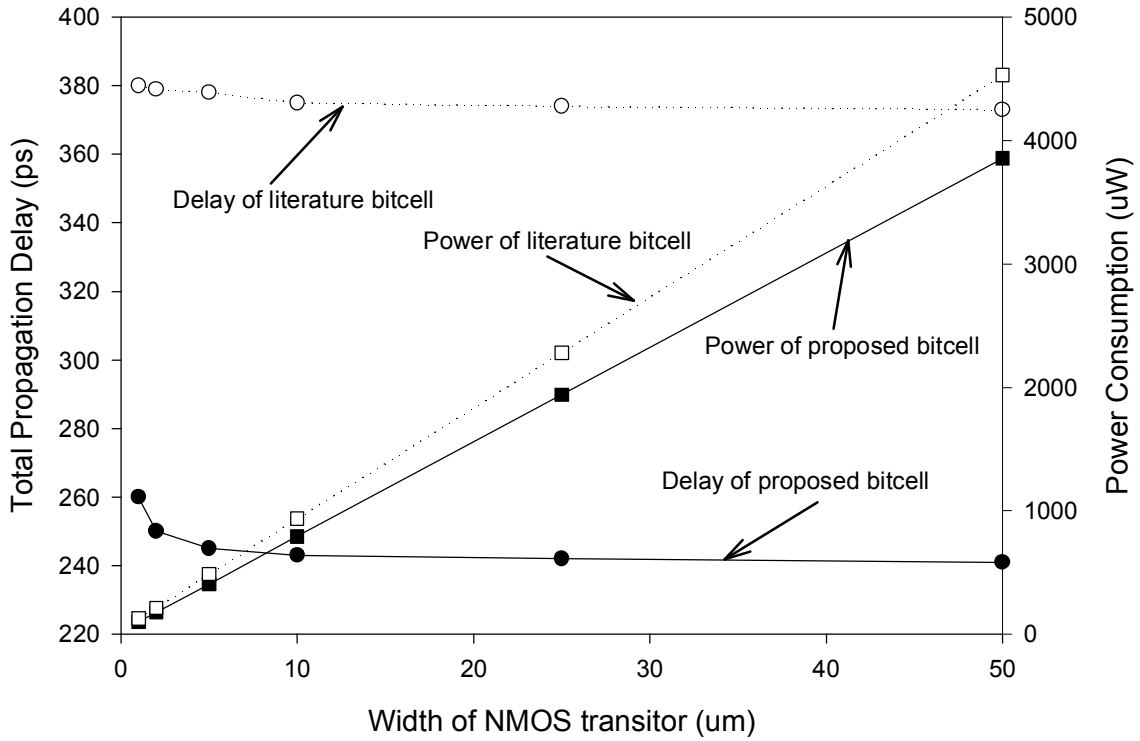


Figure 4.10: The power consumptions and propagation delays of the bitcell in [65] and the proposed bitcell

Moreover, since the procedure of the reload is triggered by the complementary configured PMOS and NMOS and there is an *LD* controlled NMOS and *S1* to disable the second stage, the full swing of the reloaded output is achieved. Compared with the one pull up PMOS in [65], the middle level of the output is avoided.

4.4 Simulation and measurement results of the counter

A comparison of the performances of this new bitcell, the bitcell in [65] and the single TSPC divide-by-2 unit, which does not have the reload function, is carried out. The PMOS and NMOS devices of all individual bitcells are of the same size.

The simulations are performed using the Cadence SPECTRE RF for the CSM 0.18 μm CMOS process. Moreover, the results are also verified for these circuits fabricated under the same process. The measured power consumption for the three bitcells: single TSPC divide-by-2 unit, the proposed bitcell and the bitcell in [65] are shown in Figure 4.11.

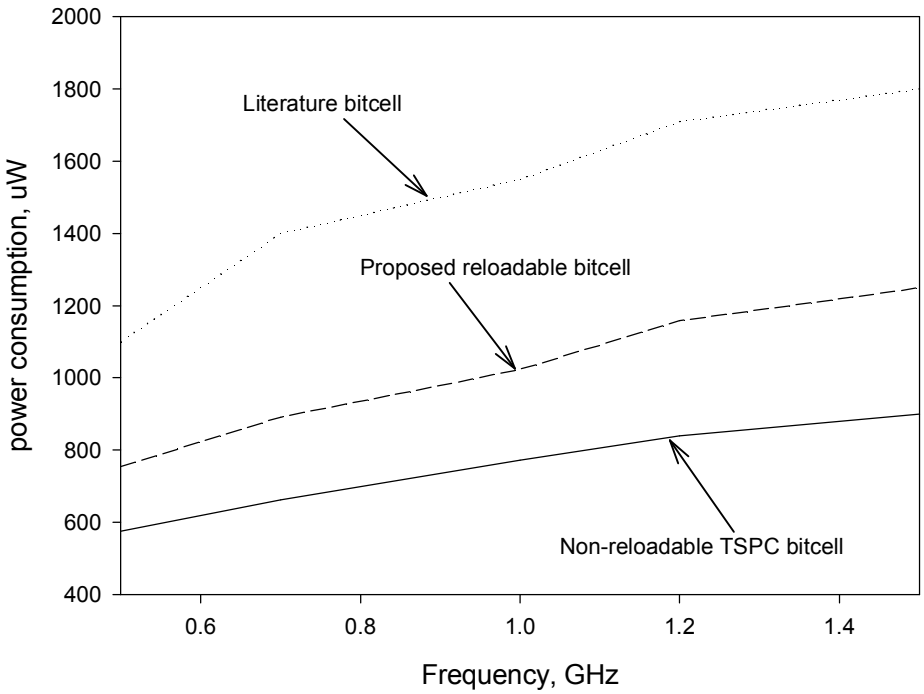


Figure 4.11: The power consumption of the three bitcells

Because of the glitch problem, the bitcell in [66] could not be simulated to provide comparable results. The input signal is a square waveform with a rail-to-rail logic. The single TSPC divide-by-2 unit has the lowest power consumption while the proposed bitcell achieves about 30% reduction in the power consumption of the bitcell in [65]. The measurements for these three dies are carried out with the same

conditions of the input frequency and input swing (The power consumption for the buffer is excluded).

A programmable counter based on this bitcell is constructed using the architecture in Figure 4.1.a [63]. To compare the performance of this proposed bitcell with that used in the counter in [63], a six-stage counter has been realized also using AMS 0.8 μm CMOS process. Simulation shows the proposed counter is able to work up to 1 GHz with a power consumption of 13.5 mW under the supply voltage of 5 V. In [63], the counter achieves 723 MHz with the power consumption of 17.2 mW under the same supply voltage. Further simulations, layout design and fabrication of the proposed counter are, however, based on the CSM 0.18 μm CMOS process. The active area of this programmable counter is about $150 \times 75\ \mu m^2$ while the total die size is $300 \times 400\ \mu m^2$ including the test pads. The test chip is shown in Figure 4.12.

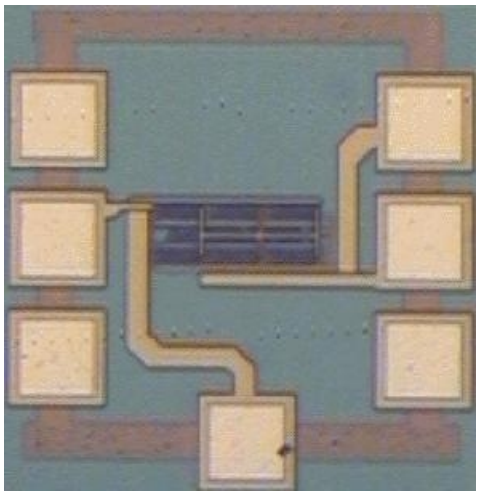


Figure 4.12: The die photo of the proposed counter

For test proposal, the divide-by-32/33 (*PI* information of 100001 and 100000 respectively for six stages) is used to illustrate that the chip can work properly

since the total propagation delay of the first stage decides the maximum operating frequency.

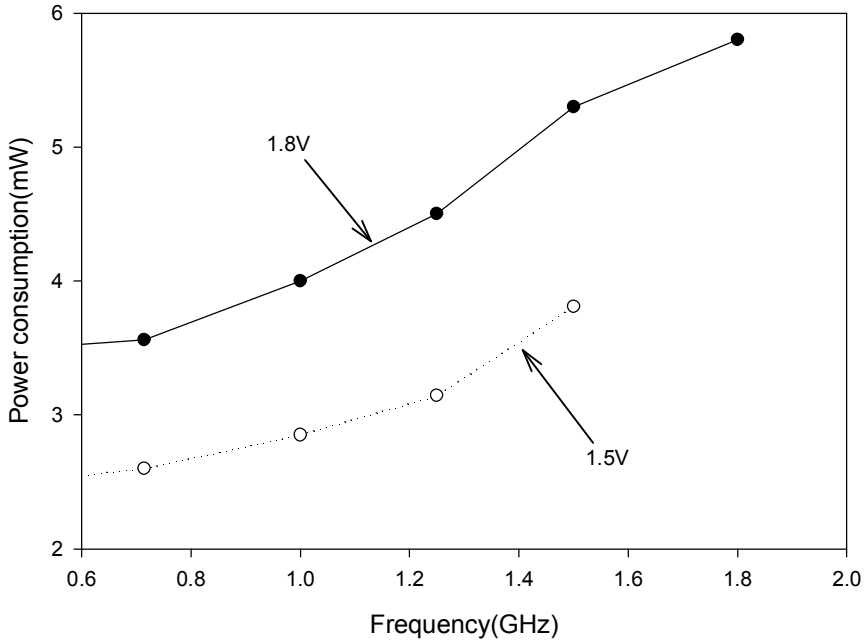


Figure 4.13: The power consumption vs. frequency of the proposed counter

Figure 4.13 shows the measurement results for the power consumption *vs* the operating frequency of this programmable counter. In the post-layout simulation, for a 1.8 V supply voltage, this programmable counter achieves a maximum operating frequency of 1.8 GHz and dissipates about 5.7 mW as shown in the solid circled line. It can operate up to 1.5 GHz and consumes 3.5 mW for a 1.5 V supply voltage as illustrated by the dashed circled line. Measurement are carried out on-wafer with an RF probe station, the input signal is provide by the HP E4433B 0.25 MHz~4 GHz signal generator, while the output signals are captured by Lecroy Wavemaster 8600A 6G oscilloscope. Measurement shows that the proposed counter can work up to 1.5 GHz with the1.5 V supply voltage and the power consumption is 3.5 mW (the power-hungry output buffer consumes 8 mW), while

it can operate up to 1.8 GHz with a power consumption of 5.8 mW (buffer consumes 10 mW) for a supply voltage of 1.8 V.

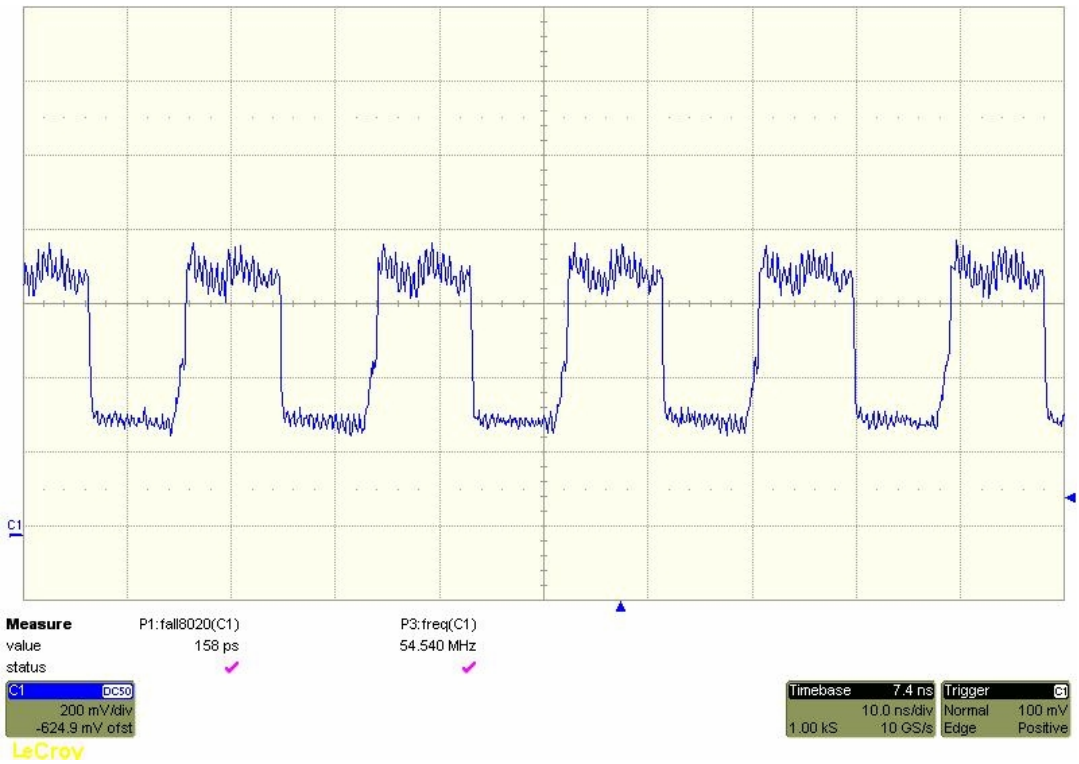


Figure 4.14: The measured transient result of divide-by-33 for the proposed counter

Figure 4.14 shows the output transient waveform for the divide-by-33 function with an input signal of 1.8 GHz. The proposed counter is the first to achieve the GHz operation for the all-stage programmable counters with a low power consumption. The power/frequency of the proposed counter is 3.2 μW/MHz, while this value is 28.6-34.3 μW/MHz in [65], which is derived from the measurements in [65] for the operating range.

4.5 A Wide band high resolution frequency divider

The proposed programmable counter can be easily implemented in a frequency synthesizer for applications below 1.8 GHz. Moreover, it is also suitable for

implementing a wide range and high resolution programmable frequency divider for wireless LAN applications by using the structure in [38]. The prescaler can be implemented by any of the topology in the literature [38] [99] [59]. For this implementation, a low power divide-by-4/5 dynamic prescaler in [99] is used. The S counter has the same topology as P counter except for the only difference in the bitcell design where the *LD* signal for the left part in the proposed bitcell is replaced with a *STOP* signal to provide the modulus control signal of the prescaler [66]. Difference from the traditional topology in [38] where the P counter has a fixed division ratio, the P and S counters in this design are all implemented with the proposed bitcells which are all-stage programmable. This frequency divider for 5-6 GHz applications has a division ratio of $4 \times P + S$. P is from 4 to 2^m and S is from 3 to $2^n - 1$ where m and n are the stages of P counter and S counter respectively. Such division ratios will be able to cover all the demand frequencies for the wireless LAN standards in 5-6 GHz as table I shows.

Here the reference frequency of 5 MHz is used to cover all the center frequencies of the two standards. The frequency divider achieves a low power consumption of 18 mW in the post-layout simulation. An ultra wide range divider of a low power consumption is achievable by using the proposed programmable counter. This topology can also be used in the 2.4 GHz wireless LANs such as IEEE 802.11b/g and Bluetooth.

Table 4.1: Center frequencies for HIPERLAN II and UNII

Frequency(GHz)	**5.18**	**5.2**	**5.22**	**5.24**	**5.26**	**5.28**	**5.3**	**5.32**			
Division ratio	1036	1040	1044	1048	1052	1056	1060	1064			
N	4	4	4	4	4	4	4	4			
P	255	255	255	255	255	255	255	255			
S	16	20	24	28	32	36	40	44			
Frequency(GHz)	**5.5**	**5.52**	**5.54**	**5.56**	**5.58**	**5.6**	**5.62**	**5.64**	**5.66**	**5.68**	**5.7**
Division ratio	1100	1104	1108	1112	1116	1120	1124	1128	1132	1136	1140
N	4	4	4	4	4	4	4	4	4	4	4
P	255	255	255	255	255	255	255	255	255	255	255
S	80	84	88	92	96	100	104	108	112	116	120
Frequency(GHz)	**5.745**	**5.765**	**5.785**	**5.805**							
Division ratio	1149	1153	1157	1161							
N	4	4	4	4							
P	255	255	255	255							
S	129	133	137	141							

The frequency divider has been fabricated in the CSM 0.18 μm CMOS technology. For the test proposal, a 5 GHz VCO has been used as the frequency source. The proposed imbalance phase switching prescaler is used, the division ratio for the prescaler is divide-by-31/32, so the six-stage counter.

Figure 4.15 shows the die photo of the VCO with frequency divider. Figure 4.16 shows the post-layout and measured power consumption vs. operating frequency. Because the first divide-by-4 stage is implemented with the large size RFMOS provided by the CSM, the power consumption is large. However, the measured results agree well with the post-layout simulation. The output transient result of divide-by-1217 is shown in Figure 4.17. The operating of different division ratio can be controlled by the *PI* signal for different stages.

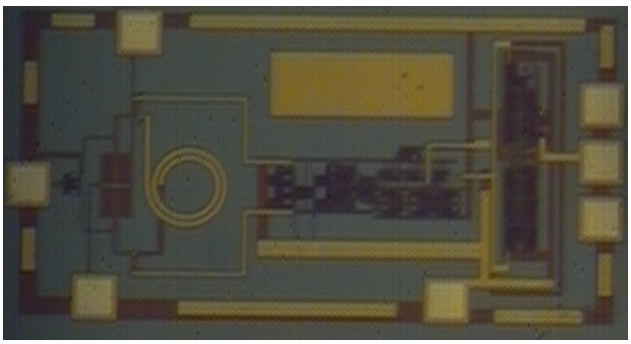


Figure: 4.15: Die photo

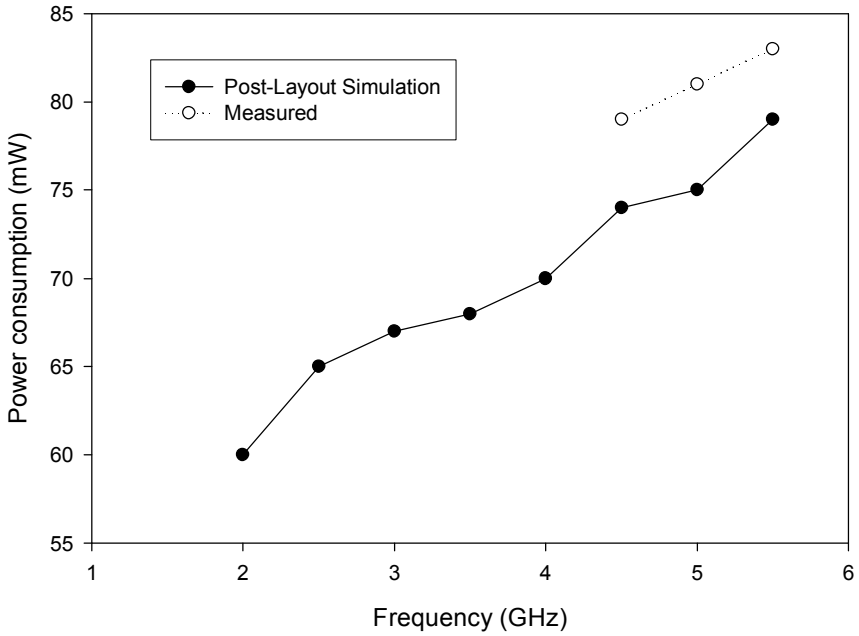


Figure 4.16: Power consumption vs. operating frequency

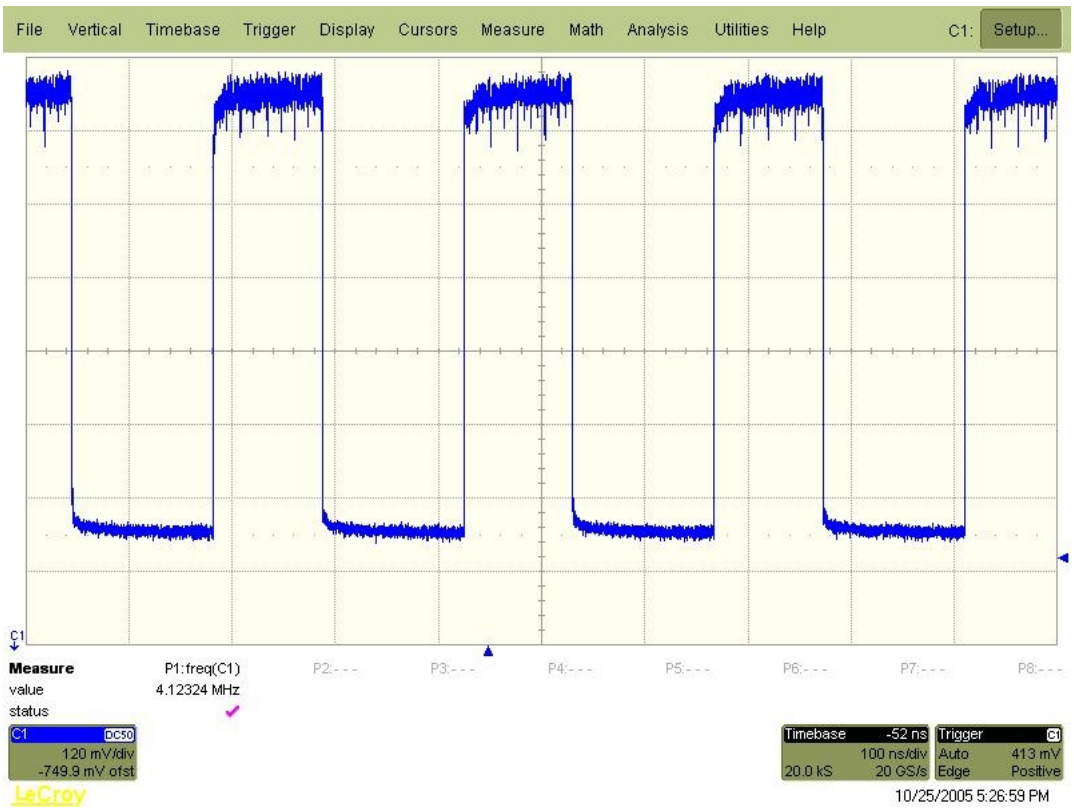


Figure 4.17: Output waveform of the frequency divider

To verify the low power operation of the proposed frequency divider, some of the previous designs implemented with RFMOS have been fabricated using the normal MOS in the new MPW (March 2005).

The proposed 2-to-1 phase switching prescaler was fabricated together with the P counter and S counter to provide a low power frequency divider. Figure 4.18 shows the die photo of the proposed frequency divider.

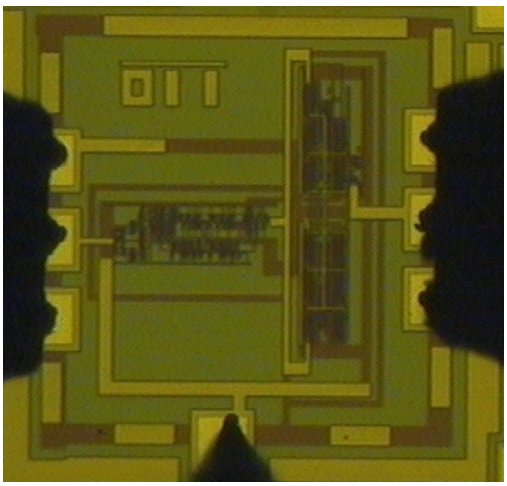


Figure 4.18 The Die Photo of the proposed frequency divider

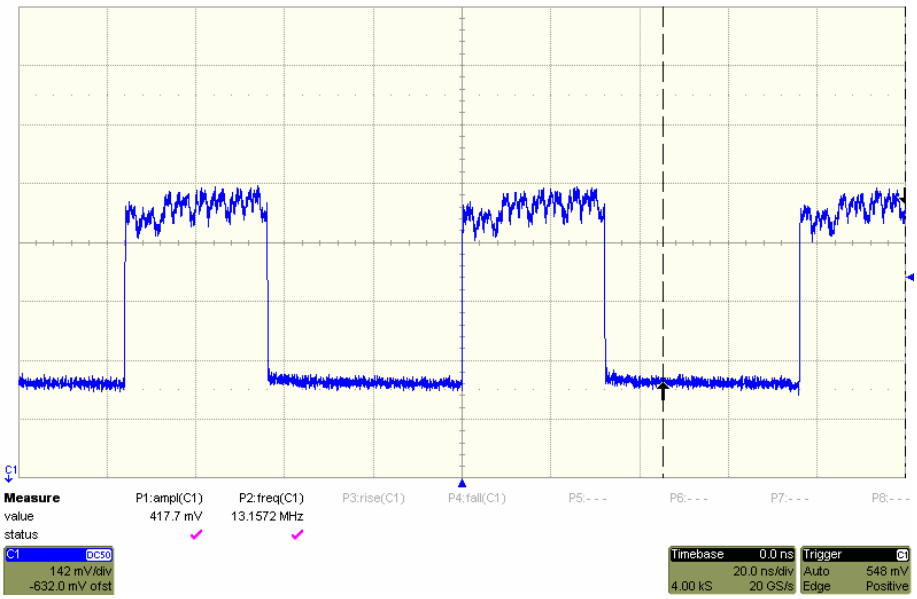


Figure 4.19 The output of the frequency divider with 4 GHz input

This frequency divider can operate from 1 GHz to 4 GHz with a low power consumption, Figure 4.19 shows the output waveform with the 4 GHz input, while the power consumption vs. operating frequency for this divider is summarized in Figure 4.20.

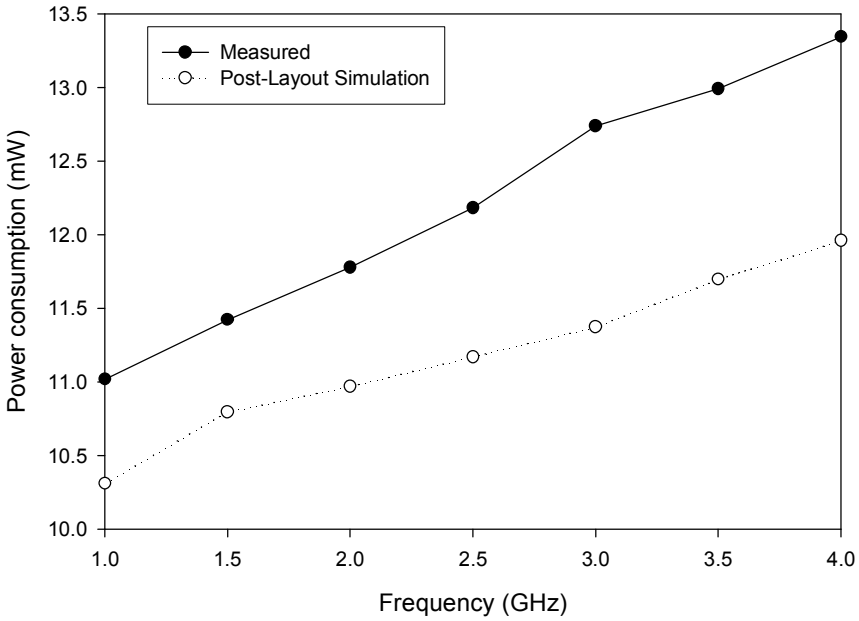


Figure 4.20 power consumption vs. operating frequency

The total power consumption for this frequency divider is only 13 mW, this agrees well with the post-layout simulation in Chapter 3. In other words, the performance of proposed 2-to-1 phase switching prescaler is silicon verified.

In this chapter, the counter integrated with the E-TSPC based prescaler to provide a frequency divider is proposed as well. A divide-by-4/5 E-TSPC based prescaler has been combined with the counters to form a low power high resolution frequency divider. The die photo is shown in Figure 4.21.

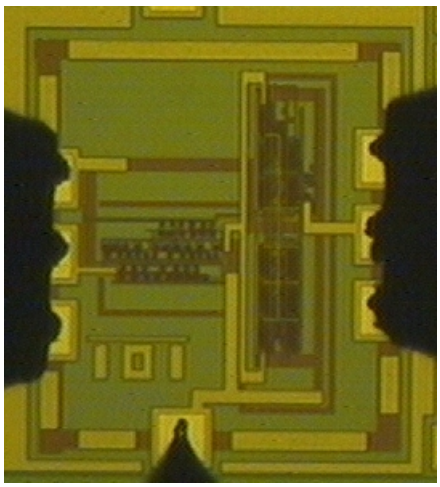


Figure 4.21 Die photo of the E-TSPC based frequency divider

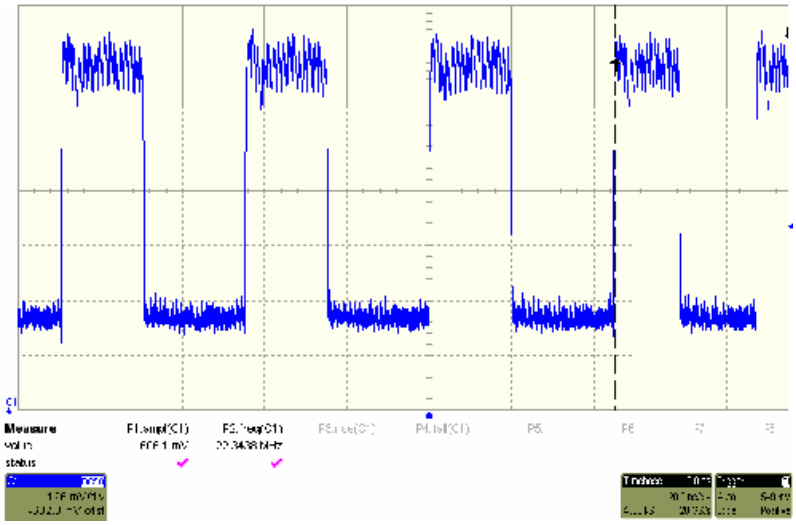


Figure 4.22 Output of the frequency divider with 4 GHz

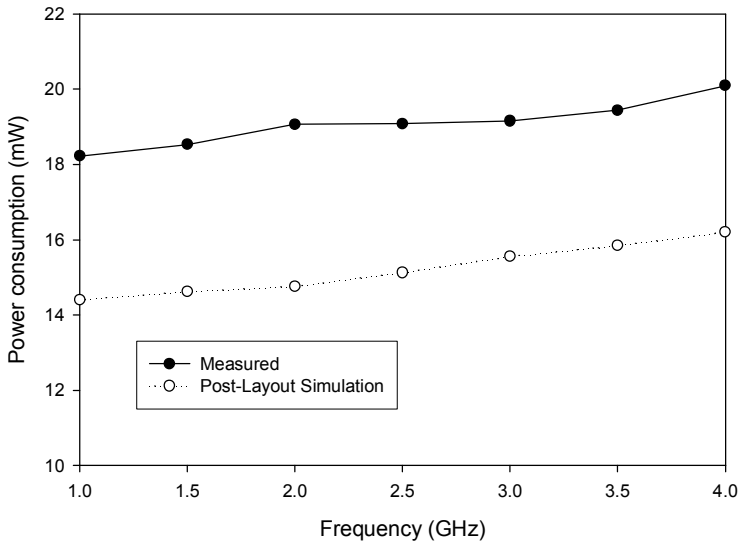


Figure 4.23 power consumption vs. operating frequency

Figure 4.22 shows the output of the frequency divider with 4 GHz input. Figure 4.23 summarizes the power consumption vs. operating frequency of the divider. The measurement results agree well with the post-layout simulation results.

4.6 Conclusion

The design difficulties of the wide band high resolution programmable frequency divider for the multi-standard applications are investigated. A high speed low power counter is successfully implemented for the multi-standard operations. The proposed programmable counter with the new reloadable bitcell achieves higher operating frequencies and lower power consumption in comparison to the performance of the existing designs. Measurement results show the first GHz all-stage programmable divider with a low power consumption is achievable with the proposed bitcell. The application of this counter in a 5 GHz wide-range frequency divider is described.

A part of this chapter is published in [68].

Chapter 5

Phase Noise in the TSPC Based Frequency Divider

5.1 Introduction

A PLL synthesizer is used as a variable frequency source in a communication system, where the frequency divider is employed to provide the selectable division ratio to the PLL synthesizer. Noise in the frequency divider has an important impact on the performance of the PLL, especially for a large division ratio, the noise accumulated in the frequency divider may corrupt the output signal [69]. Hence, the phase noise of the frequency divider should be predicted during the design of the whole PLL system. The frequency divider is usually a digital circuit. The various noise sources in the circuit affect the zero crossing instants of the output signal and the resultant phase noise is a random process sampled at the divider output frequency [70]. As a result, the analysis of the phase noise in the frequency divider should be based on the time domain jitter. Traditionally, the phase noise of the frequency divider is given by some empirical equations from the measurement results [69] [71]. In [70], a phase noise model derived from the physical circuit is proposed. However, the model is only applicable to MCML (MOS Current Mode Logic) circuits and it is based on the time invariant mode for some of the noise sources. With the advancement of the CMOS technology, the GHz or multi-GHz single-end frequency dividers based on the True-Single-Phase-Clock (TSPC) have become popular for their lower power consumption and easier integration to the VLSI system as compared with that of MCML circuits [68] [99].

Thus, the phase noise and power consumption of the TSPC based frequency divider need to be determined as well. In this chapter, the phase noise in the TSPC based frequency divider is analyzed by using a time-variant model from the physical derivation. The model is applicable to TSPC based dividers including the single divide-by-2 units and the prescalers. The calculation and simulation of the phase noise in the prescaler design are verified by the measurement results.

5.2 Phase noise and jitter in frequency dividers

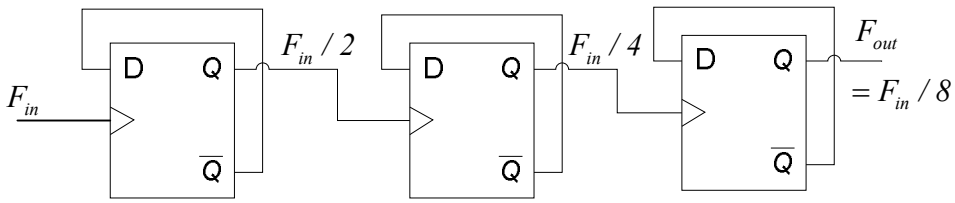


Figure 5.1: The Asynchronous divider

A frequency divider usually consists of cascaded divide-by-2 units as shown in Figure 5.1. If a dual-modulus division is desired, additional logic units are required. In this asynchronous divider, the output signal of one stage is the input of the next stage. The time jitter, σ_t, is cumulative. In each divide-by-2 stage, the actual transition is decided by the previous stage while its own jitter is added to the output signal. For a noiseless frequency divider, the jitter at the input will cause the same amount of jitter at the output, so the output phase deviation, ϕ_{out} is given by [69]:

$$\phi_{out} = \frac{\phi_{in}}{N} \tag{5.1}$$

where ϕ_{in} is the input phase derivation and N is the division ratio of the frequency divider.

In the frequency domain, the relationship between the Power Spectral Densities (PSDs) of these two signals is given by:

$$S_{out} = \frac{S_{in}}{N^2} \tag{5.2}$$

where S_{out} and S_{in} are the Power Spectral Densities over all the modulation frequencies of the two signals respectively.

In [69], the phase noise in the frequency divider is modeled by the empirical equation:

$$S_{out} = K_0 + \frac{K_1}{f_m} \tag{5.3}$$

where f_m is the modulation frequency, K_0 and K_1 are constants representing white noise and flicker noise respectively.

The time domain jitter can be written in terms of the integral of the PSD of the phase S_ϕ within the Nyquist band [70]:

$$\delta_{t_0}{}^2 = \frac{1}{4\pi^2 f^2{}_{out}} \int_0^{f_{out}/2} S_\phi(f)\,df \tag{5.4}$$

where δ_{t_0} is the time jitter, f_{out} is the output frequency.

Therefore, the output single-side-band-to-carrier ratio (SSCR) of the thermal noise is given by:

$$L_W = 4\pi^2 f^2{}_{out}\delta_{t_0}{}^2 \tag{5.5}$$

By using this equation, the phase noise in the frequency divider can be determined by the time jitter.

In the previous work, the time domain analysis is based on the empirical models. In [70], a novel time jitter model based on the physical noise sources is proposed. The time jitter is obtained by determining the variance of the output voltage at the zero crossing point. The variance of the output voltage is the sum of the noise Power Spectral Density within the noise bandwidth divided by the slope of the output waveform. However, in [70], the model hasn't considered the time variant effect of the jitter. The slope is given by a fixed value while the different noise currents are assumed to have the same effect on the output waveform. Moreover, the derivation of the voltage variance, especially for the input MOS pair and tail MOS transistors is carried out from the delay analysis which is a complex procedure. Until now, no simple but effective method has been proposed to analyze the noise sources in the frequency divider.

5.3 Time-variant jitter method

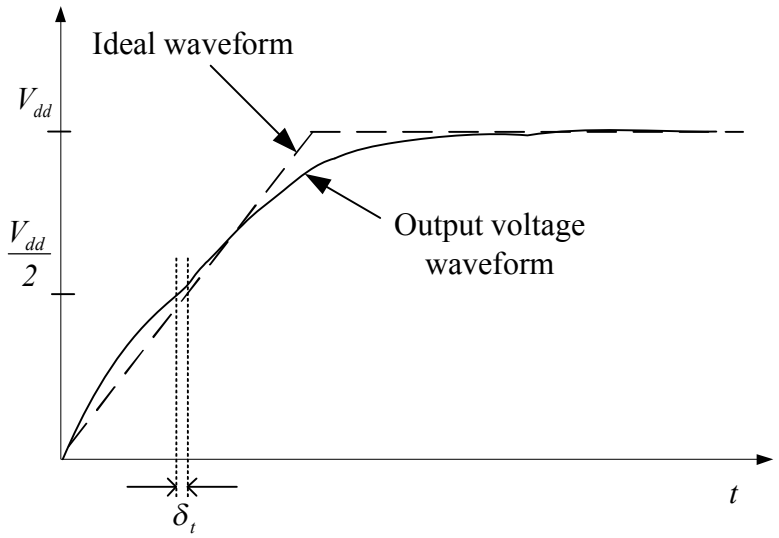


Figure 5.2: The output voltage waveform and time jitter

In general, noise affects the phase and amplitude of a frequency divider. However, the phase noise is the only concern because the amplitude noise can be suppressed by the frequency divider [72]. In [70], the time jitter is obtained by dividing the variance of the voltage by the slope of the output waveform. To precisely predict the time domain jitter, the time-variant model for oscillators [20] is implemented in the analysis of the frequency divider since the TSPC divide-by-2 unit can be modeled as a three stage ring oscillator [40].

As shown in Figure 5.2, at the zero crossing point, for a small current impulse, the resultant phase shift $\Delta\phi$ is proportional to the voltage change, ΔV:

$$\Delta\phi = \Gamma(\omega_0 t)\frac{\Delta V}{V_{max}} \tag{5.6}$$

where V_{max} is the voltage swing across the capacitor, $\Gamma(x)$ is the Impulse Sensitivity Function (ISF) which defines the sensitivity of the output phase to an impulse input. The ISF has different values at different points within a period. The ISF of the output waveform in an inverter based ring oscillators is shown in Figure 5.3. During the rising edge, the injection will cause the phase shifts. In the region where the output is logically high or logically low, the injection can only cause the amplitude change. The maximum value of the ISF is located at the zero crossing point of the output waveform.

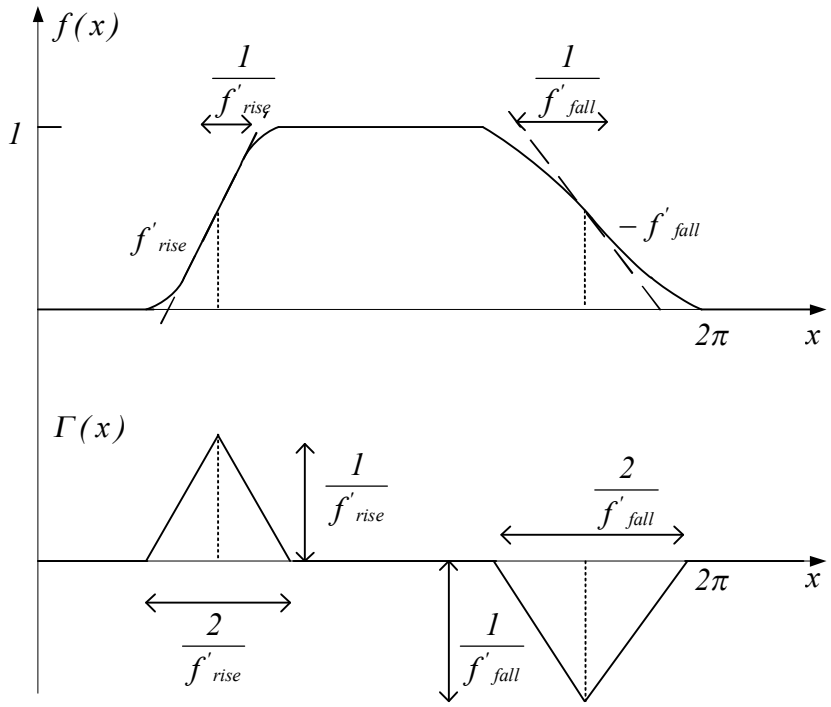


Figure 5.3: ISF in a ring oscillator

Another parameter need to be determined is the Noise Modulating Function (NMF), $\alpha(\omega_0 t)$. The statistical properties of some random noise sources in the MOS transistors may change with the time in a periodic manner. A white cyclostationary noise current, $i_n(t)$, can be written as:

$$i_n(t) = i_{n0}(t)\alpha(\omega_0 t) \tag{5.7}$$

where $i_{n0}(t)$ is a white stationary process. Therefore, $\overline{i^2_{n0}} / \Delta f$ is the maximum of the periodically varying noise power density. By introducing the NMF, the effects of the difference noise currents in the circuits can be determined more precisely since the total noise is the sum of the noise sources with different weights.

The output phase is therefore [23]:

$$\phi(t) = \int_{-\infty}^{t} i_n(\tau)\frac{\alpha(\omega_0 t)\Gamma(\omega_0 t)}{q_{max}} d(\tau) \tag{5.8}$$

The above time variant model is suitable in the analysis of the VCO. The major difference between the ring VCO and the frequency divider is that, the VCO generates an oscillating frequency. The phase noise is equal to the integral of the ISF multiplied by the noise spectrum within one period. However, in time domain analysis of the frequency divider, the time jitter is equal to the voltage variance divided by the slope at the zero crossing point. In [70], a constant slope is assumed while the different noise sources are assumed to have the same impact on the output waveform. However, the slope for the output waveform varies at different time transitions. The variant slope can be obtained by the derivative of the output waveform. Thus, different weights for different noise currents are needed to get the total voltage variance at the zero crossing point as proposed in [20]. Finally, the time jitter and phase noise can be obtained by using the method of the time domain analysis in [70].

The proposed method is first applied in the inverter. For a single inverter, both the thermal noise and flicker noise in PMOS and NMOS transistors will affect the jitters of the zero crossing points of the output waveform.

For the MOS transistors, the power density of the thermal noises is given by [73]:

$$\overline{i_n^2} = \overline{i_{nd}^2} + \overline{i_{ng}^2} = 4KT\Delta f(\gamma g_{d0} + \alpha g_g) \tag{5.9}$$

where g_{d0} is the drain-source conductance at zero V_{ds} and the parameter g_g is

$$g_g = \frac{\omega^2 C^2_{gs}}{5 g_{d0}} \tag{5.10}$$

and the flicker noise power density is given by [20]:

$$\overline{i_n^2} = \frac{K}{f} \frac{g_m^2}{WLC^2_{ox}} \tag{5.11}$$

For PMOS devices, K is typically about $10^{-28} C^2/m^2$, whereas for NMOS devices it is about 50 times larger [20].

In an inverter, noise is introduced by both PMOS and NMOS transistors. However, they produce different impacts on the output waveform at the zero crossing point. Therefore, the transient results of the currents in the PMOS and NMOS transistors are needed to obtain the NMF. The other parameter is the slope of the output waveform at the zero crossing point. The calculation of the ISF in this case is not the same as that in [20], where the derivative of the nominal output waveform is calculated and then divided by the frequency to get the phase difference [85]. However, for the proposed time domain analysis, only the slope of the voltage signal is required, therefore, only the derivative is taken to get the time varying slope for the output waveform. Then the NMFs for all noise sources are divided by the slopes at the zero crossing points to get the impact factors of different noise sources. By summing all the noise sources' impact factors on the time jitter, the total time jitter caused by the thermal noise (Johnson Equation in [70]) for a single inverter can be obtained as:

$$\delta^2{}_t = \sum_{i=1}^{n} \frac{\overline{i_i^2} R^2}{4 C_L S L^2} \alpha_i^2 \tag{5.12}$$

where the SL is the slope at the zero crossing point, α_i is the noise modulation function which describes the different weights in the impact of noise sources. The total phase noise can be obtained the equation (5.5).

As for the flicker noise, $L(f_m)$, which is usually analyzed based on the frequency domain, is given by:

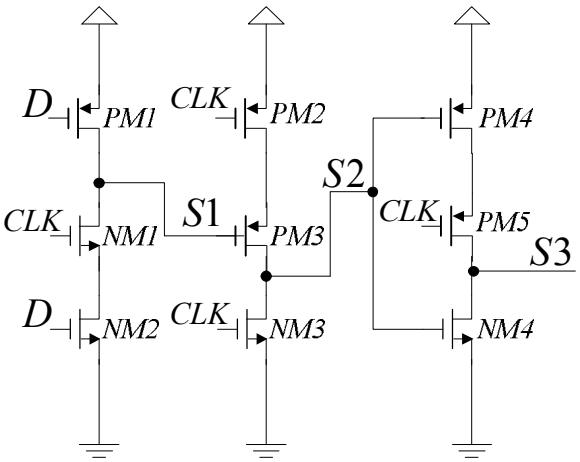
$$L(f_m) = \frac{2\pi^2 f^2{}_{out} S^2{}_V (f_m) \alpha^2}{SL^2} \tag{5.13}$$

where $S^2_V(f_m)$ is the PSD of the flicker noise.

Different from the method in [70], the time variant slope and NMF are used in equation (5.13).

In a traditional TSPC divide-by-2 unit [52] as shown in Figure 5.4.a, which consists of two latches as an MCML DFF except for the single-end configuration, the output jitter is the sum of the jitters in the three stages. In this analysis, the rising edge of the TSPC divide-by-2 unit is taken into account since the rise and fall times can be adjusted to get a symmetrical waveform [20]. Moreover, the cascode NMOS configuration in this divide-by-2 unit can be analyzed using the current starve inverter in [20].

Besides the TSPC divide-by-2 unit, the E-TSPC divide-by-2 unit as shown in Figure 5.4.b, is also widely used for high speed applications. However, in the TSPC divide-by-2 unit, due to the short circuit within a quarter period, one transistor will always be on, the NMF will be different from that of a single inverter.



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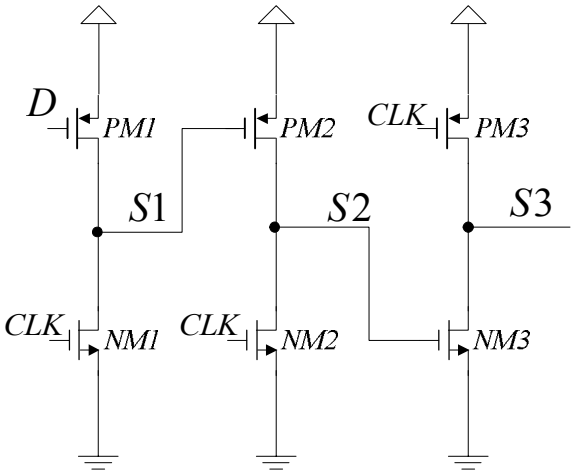
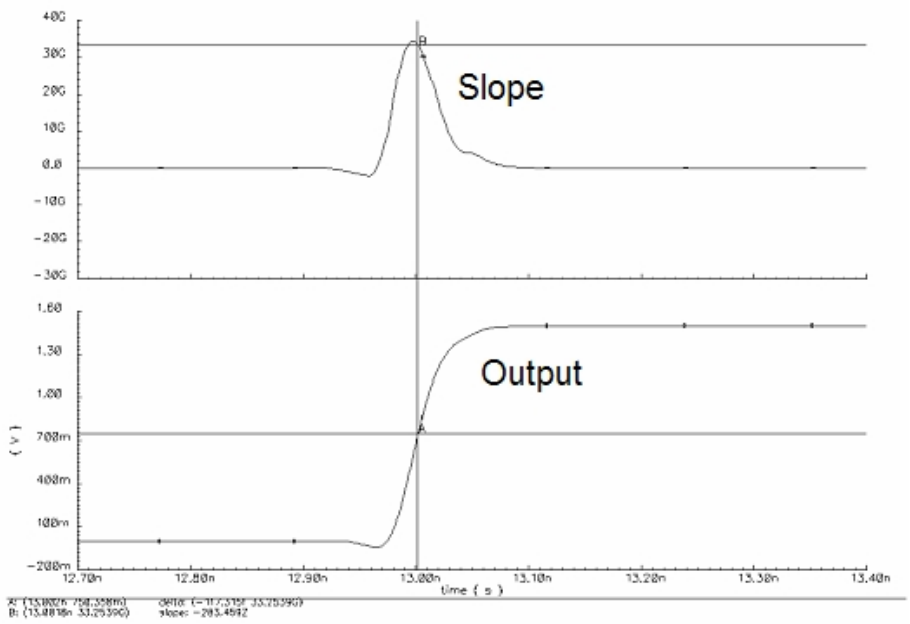


(b)

Figure 5.4: Dynamic DFF a) TSPC b) E-TSPC

5.4 Noise estimation

The simulation and calculation of the phase noise is first applied to the inverter. Because the noise level of an inverter is very small, ten cascaded identical inverters are used in the simulation. The input source for the simulation is the output of a VCO followed by the divide-by-2 stages, which is a typical configuration in a frequency synthesizer. The time variant slope and NMF, which are shown in Figure 5.5, are obtained by the simulation using the Cadence SPECTRE RF.



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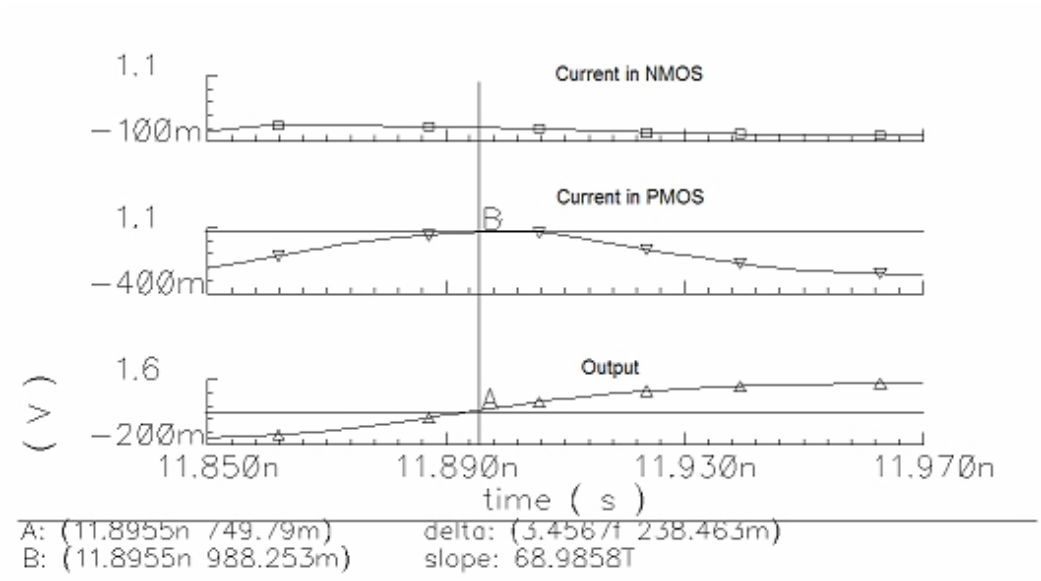

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Figure 5.5: The time variant slope and NMF in an inverter

a) The time variant slope b) NMF during rising edge

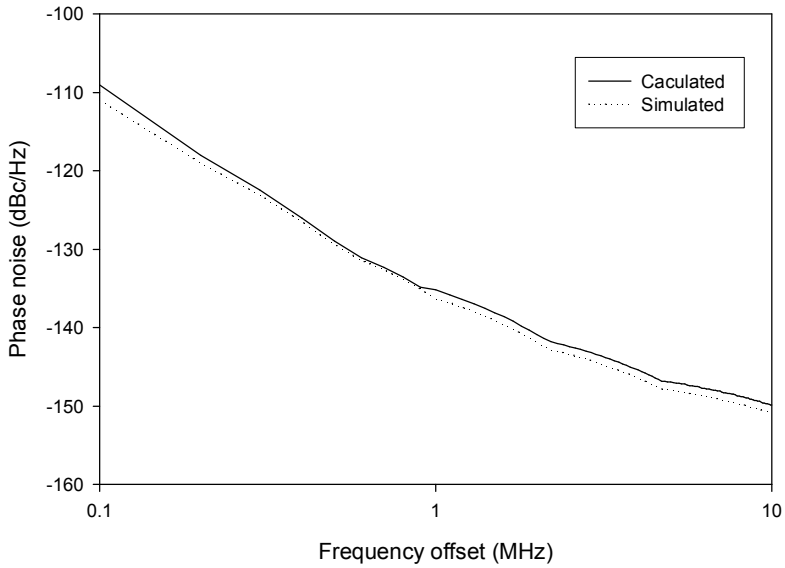


Figure 5.6: Phase noise in the inverter chain

The product of the time variant slop and NMF is the effective modulation factor for the noise sources. Therefore, the final voltage variance at the zero crossing point can be obtained according to equation (5.12). Figure 5.6 shows the simulated phase noise and calculated phase noise based on equation (5.12) and (5.13) for this inverter chain.

The phase noise of the TSPC divide-by-2 unit is also calculated and simulated using the same method where the jitter is cumulative in the three stages. For a noiseless divide-by-2 unit, since the output frequency is halved, the output phase noise will be 6 dB less than the input value according to equation (5.2). The output noise of the divide-by-2 function is compared with the ideal case, which is equal to the input noise minus 6 dB.

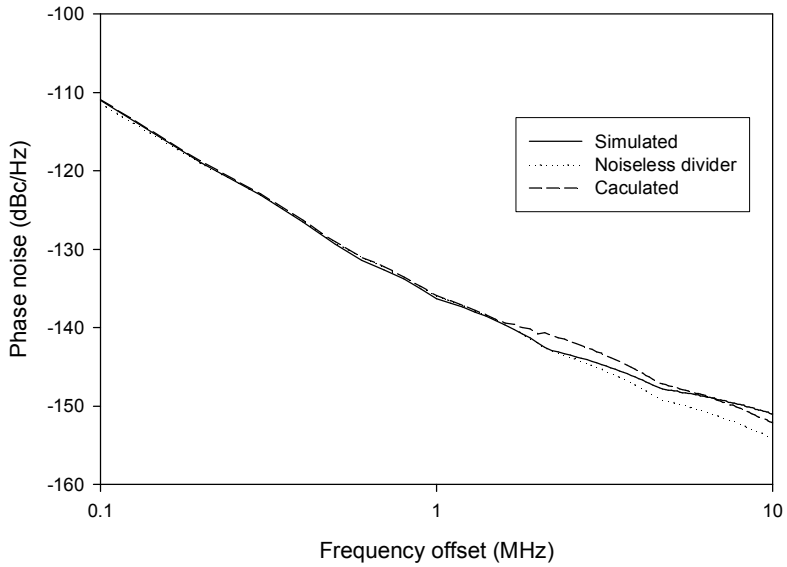


Figure 5.7: Phase noise in the TSPC divide-by-2 unit

Figure 5.7 shows the simulated results of the phase noise with an input of 1 GHz square waveform in a divide-by-2 unit. The dotted line shows the estimated phase noise for a noiseless divide-by-2 unit and the dashed line shows the calculated phase noise. An increase of the supply voltage will help to reduce the phase noise at the expense of the power consumption [70]. However, an increase of W/L cannot improve the noise performance effectively. As W/L increases, the current and the thermal noise of the MOSFET also increase.

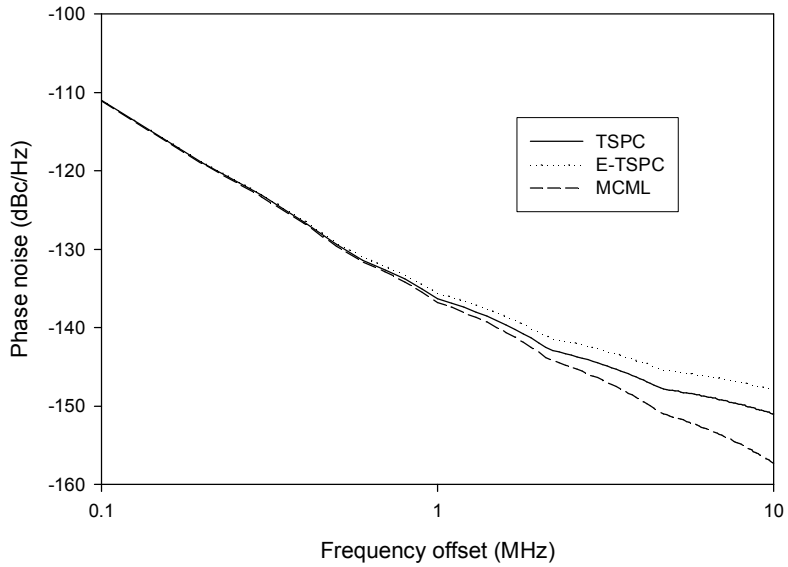


Figure 5.8: Phase noise in the three divide-by-2 units

The E-TSPC divide-by-2 unit has a higher operating speed as compared with that of the TSPC divide-by-2 unit [51]. As shown in Figure 5.4.b, for the E-TSPC divide-by-2 unit, the capacitive load of each stage is reduced by one gate capacitor. However, because the PMOS and NMOS transistors are not used in a complementary manner to form a dynamic circuit, the E-TSPC unit has a short circuit over a quarter period. Therefore, the NMF of the E-TSPC divide-by-2 unit will be larger than that of a TSPC divide-by-2 unit. For comparison, the E-TSPC and TSPC divide-by-2 units are simulated with the same input frequency as shown in Figure 5.8. It is observed that the E-TSPC unit have a higher noise level and power consumption even it has a higher operating frequency. The simulation results agree well with the calculated results by using the proposed model.

Finally, the MCML structure, which has a low phase noise, is also simulated as shown in Figure 5.8. As reported in [70], the MCML has a better noise performance compared with that of the TSPC single-ended counterpart. However,

the power consumption is larger than that of the TSPC based single-ended divider. It is not easy to make a comparison for the power consumptions for these different logic families under the same simulation condition. For the same sizes of the MOS transistors in this simulation, the power consumptions in the MCML, E-TSPC and TSPC units are 700 μW, 450 μW and 85 μW respectively.

5.5 Design implementation

In the design of high speed prescalers, the MCML, E-TSPC and TSPC circuits are usually used. From above analysis and simulation, their characteristics can be summarized as follows: The MCML circuit has a better phase noise and higher operating speed. However, it has a fixed power consumption which makes the MCML circuit more suitable for the applications above 1 GHz. The E-TSPC circuit has a higher operating speed than that of the TSPC circuit but has a poor noise performance while maintaining a higher power consumption. Therefore, the E-TSPC circuit is only suitable when the operating speed is not achievable for the TSPC circuit. The TSPC circuit has the lowest power consumption in the GHz operating range with a fair phase noise performance among the three types of circuits.

Therefore, a good topology in the design of a prescaler is: In the high speed input stage, the MCML divider is used to achieve high speed and good noise performance while the TSPC divide-by-2 unit is implemented to reduce the power consumption while maintaining a good balance in the phase noise performance.

Figure 5.9 shows the topology of a phase switching prescaler [62]. In this prescaler the first two stages are implemented with the MCML structure. In the following divide-by-2 chain, the cascaded TSPC divide-by-2 units are used. In this

arrangement, the power consumption is optimized while a good balance in the noise performance is achieved. The simulation results show the proposed prescaler is able to operate with a 10 GHz input frequency while dissipating only 15 mW by using the novel imbalance phase switching technique of [62]. The simulated phase noise is -145 dBc/Hz at a 600 kHz offset for a divide-by-8 function.

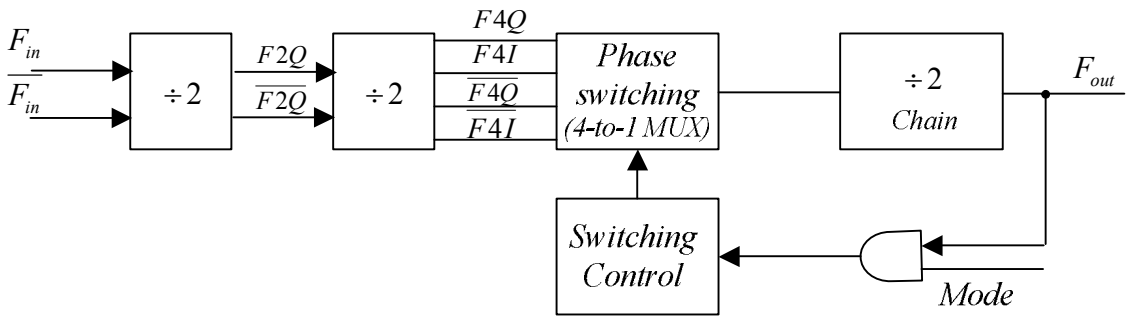


Figure 5.9: The proposed prescaler

5.6 Conclusion

In this chapter, the phase noise in the frequency divider is analyzed. A new time varying model for the time domain jitter is proposed. This model is verified by the simulation results in the TSPC based frequency divider. The trade-off between the phase noise and power consumption in the TSPC based logic family is analyzed. Based on the analysis, a new prescaler that has a better balance in the operating frequency, power consumption and phase noise performance is proposed. The estimation of the phase noise is verified by the simulation results.

Chapter 6

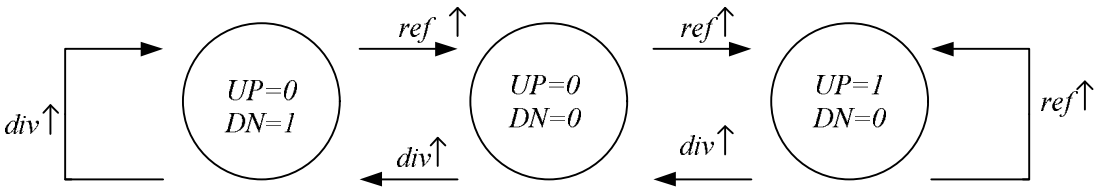
A 5-6 GHz frequency synthesizer

In the previous chapters, the system level design issues of a frequency synthesizer have been discussed. In this chapter, a low power frequency synthesizer for the 5-6 GHz wireless LAN applications is demonstrated. In this frequency synthesizer, the proposed wide band high resolution frequency divider is implemented.

6.1 Phase frequency detector

The phase frequency detector (PFD) compares the output signal from the frequency divider with an external reference source which is normally from a crystal oscillator. The PFD is implemented with a commonly used finite three state machine. Its state machine diagram and waveforms of its inputs and outputs are shown in Figure 6.1.

The PFD has two output signals, namely the *UP* and *DN* signals. If the output of the frequency divider rises before the input reference signal, the signal *DN* is logically high. In the reversed case, the signal *UP* has a logic high. If the rising edges of both input signals are in phase, then both *UP* and *DN* signals remain low. The two output signals will be logically low when the two input signals are both logically high. The output pulse widths of the *UP* and *DN* are proportional to the input phase difference between the two input signals.



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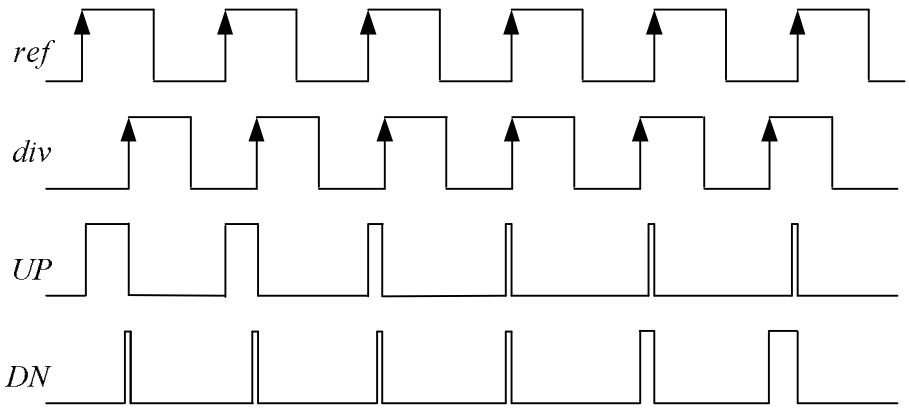


(b)

Figure 6.1: The PFD a) state machine b) Operation

The PFD can be implemented with two flip-flops [12] as shown in Figure 6.2. The phase detection range is from -2π to 2π .The delay in the reset path is used to eliminate the dead zone [74]. It is usually implemented with a chain of inverters. The average voltage of the difference of two outputs is linearity proportional to the input phase difference within the operating range. When these two input signals are almost in phase but not perfectly in phase, due to a finite rise time in the PFD, the outputs can both be reset to both zero. The gain of the PFD becomes zero. This is called the dead zone. The detailed analysis and the effect of the dead zone are described in [75].

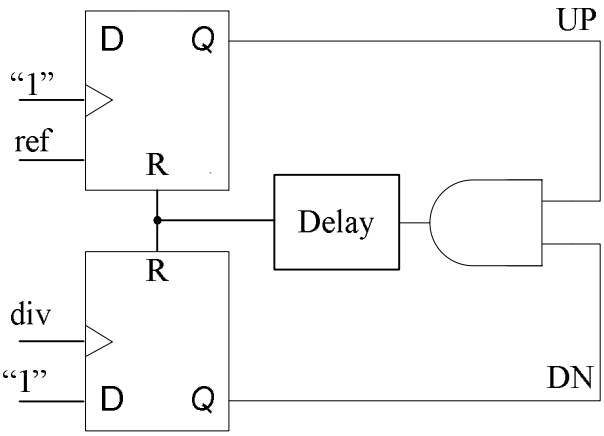


Figure 6.2: A tri-state PFD

The flip-flop used in the PFD can be RS flip-flop or dynamic flip-flops [76] [77] [78]. Many other PFDs are also reported in [79]. The precharge type PFD is illustrated in Figure 6.3.

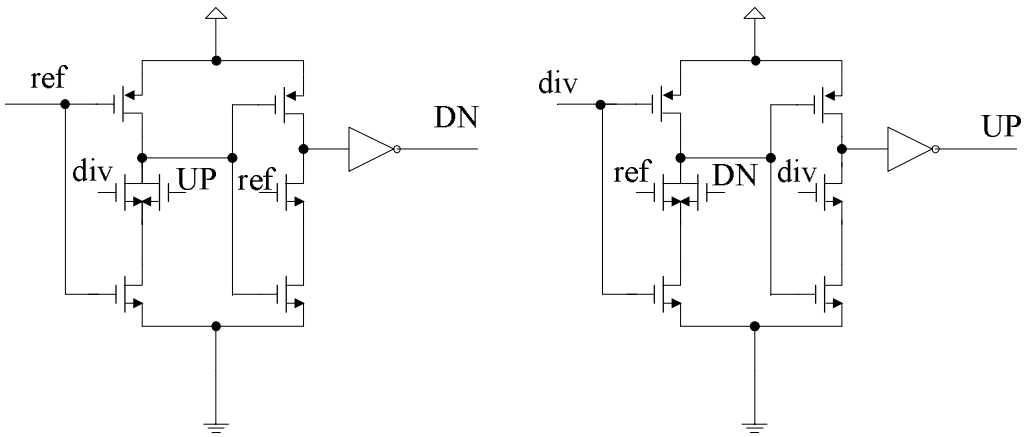


Figure 6.3: Other PFDs

The advantage of the Modified Precharge Type PFD (MPTPFD) [80] is that both the *UP* and *DN* output signals are simultaneously logically high for a minimum amount of time sufficiently long to eliminate the dead zone while reasonably short to minimize the perturbation on the loop filter during the short circuit of the charge

pump. Therefore, MPTPFD is chosen in this system. The detailed comparisons of this PFD with some other PFDs can be found in [80].

Figure 6.4 shows the schematic of the PFD used in this design. The layout of this PFD is shown in Figure 6.5. A careful layout design is done for the symmetry of the input and output signals.

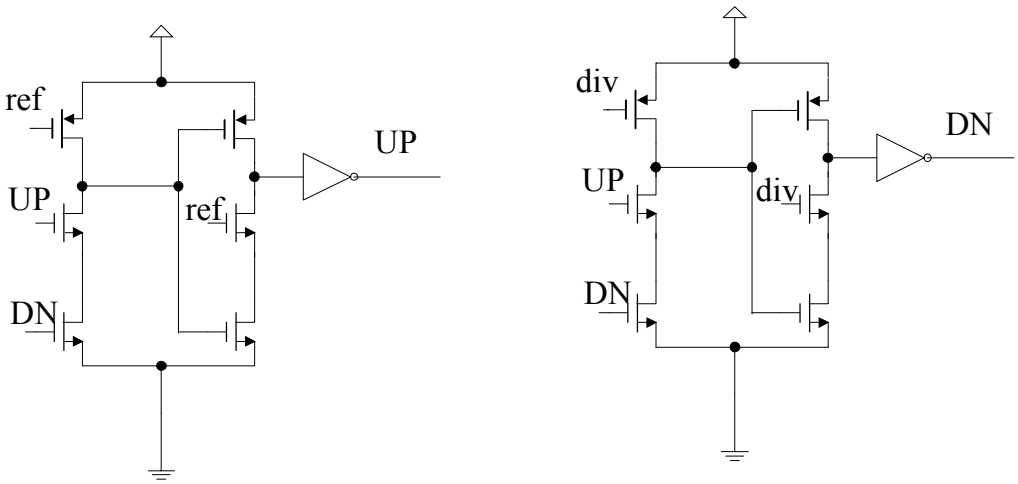


Figure 6.4: Schematic of the PFD

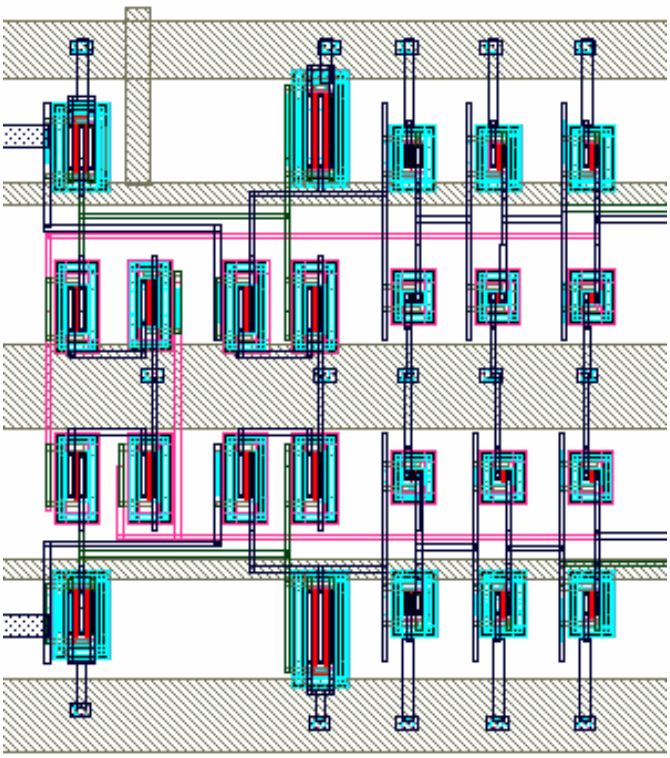


Figure 6.5: Layout of the PFD

The post-layout simulation and corner simulation are carried out to ensure that the functionality of proposed PFD can meet the requirements of such a application.

6.2 Charge pump

The charge pump (CP) is controlled by the *UP* and *DN* signals of the PFD circuit. When the *UP* signal is high, the *CP* deposits charge to the capacitors in the loop filter to increase the control voltage of the VCO. If the *DN* signal is high, it discharges from the loop filter. In a simple charge pump as shown in Figure 6.6, the charges on either C_{UP} or C_{DN} and those on the capacitors in the loop filter will be shared. This could induce large glitches in the charge pump current. The glitches will increase the phase noise and power level of the spurs in the PLL output spectrum.

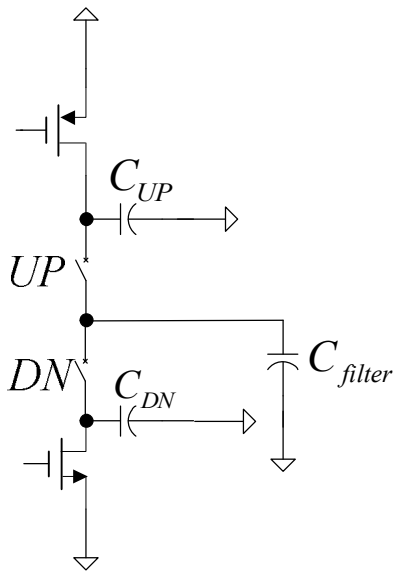


Figure 6.6: A conventional charge pump

The charge pump circuit [81] used in this project consists of two input differential pairs that act as switches, one current source that supplies biasing current as required, two current mirrors, a pump-up sub-circuit and a pump-down sub-

circuit. In order to avoid the switching mismatches, the *UP* and *DN* switches have to use the same type of transistors [17], because the switching times for NMOS and PMOS transistors are different. The current mismatch and the switching time mismatch occur in pumping the charge to the loop filter by the *UP* and *DN* operations. The detailed analysis and calculation of the impact of time mismatch can be found in [17]. Therefore, only NMOS switches are used for the charge pump in this design (Figure 6.7). The charging and discharging currents can be adjusted by the transistors at the output stage. If we increase the size of PMOS transistor at the output stage, the charging current will increase.

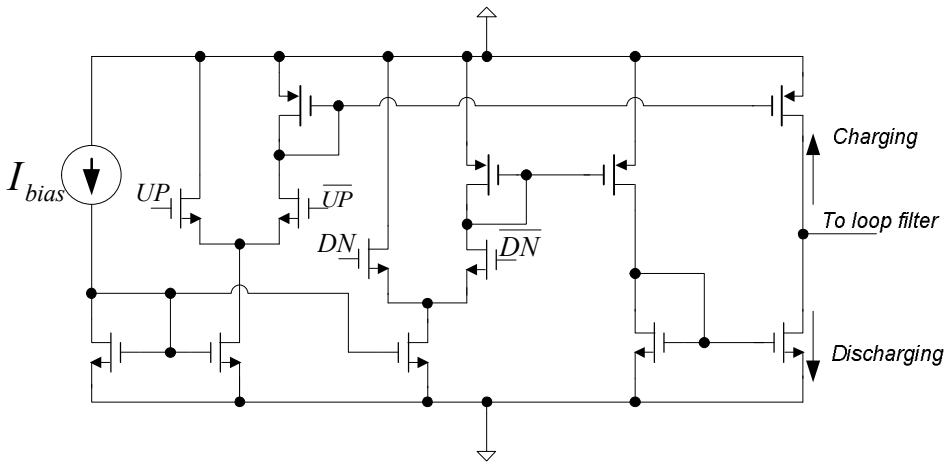


Figure 6.7: Topology of the charge pump

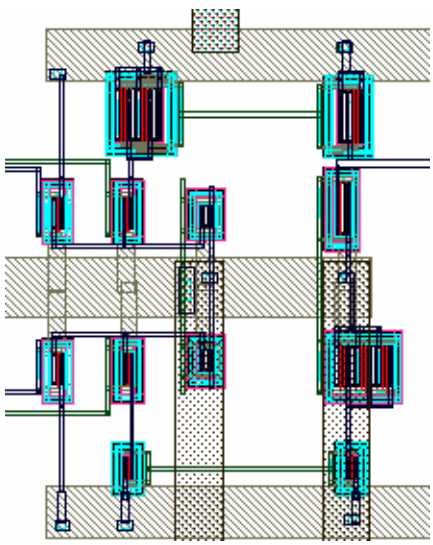


Figure 6.8: Layout of the charge pump

The charge pump also suffers from non-ideal effects such as the leakage current, mismatches and the delay offset. The analysis of these effects is given in [17]. In this design, the charging current is set at 50 μA. The PMOS and NMOS pairs are carefully sized to reduce the mismatch. The transient simulation is carried out to ensure a fast and symmetrical response. The layout of the charge pump which is shown in Figure 6.8 also maintains a good symmetry for the input pairs.

6.3 Loop filter

In the design of a loop filter, there are many parameters to be considered. These parameters have contrast effects with each other. For example, increasing the damping ratio results in a higher overshoot in the transient response. The values of the capacitors must not be too large since the PLL is used for a high operating frequency, while the resistor value is expected to be low to minimize the thermal noise.

Having described the steps of designing the filter in the previous chapter, a phase margin of 55° is chosen including a 10° phase tolerance to take into account the non-idealities of the system.

In general, the bandwidth of a system indicates the ability of reproducing the input signal and the speed of response. The rise time and the bandwidth are inversely proportional to each other. A large bandwidth will give a faster response of the PLL at the expense of more noise. Therefore, the selection of the bandwidth needs two considerations, namely, the response of the system and frequency range of noise. In this design a unity-gain frequency, also called the loop bandwidth, of 1.25 Mrad/s is chosen taking into account the above considerations.

For an optimal design, a small charge pump current, an adequate phase margin, and a large unity-gain frequency are desired. However, the charge pump current should be sufficiently large compared with the noise level. In addition, an adequate phase margin is maintained to ensure the loop stability against any process variations. The unity-gain frequency is limited to satisfy the noise (spurious-tone) performance.

In this project, a 2nd order passive loop filter is used. The parameters of the loop filter are determined based on the parameter of the PLL.

Table 6.1: Design Specification

Parameters	Unit
I_{cp}	50 μA
K_{vco}	200 MHz/V
N	1030 – 1165
Phase Margin (PM)	55°
Unity-Gain frequency (ω_μ)	1.25 Mrad/s

The gain of the VCO is 200 MHz/V. While the average N = 1097. The time constants can be calculated using the equations below [82]:

$$\tau_p = \frac{\sec(PM) - \tan(PM)}{\omega_\mu} \tag{6.1}$$

$$\tau_z = \frac{1}{\omega_\mu{}^2 \tau_p} \tag{6.2}$$

$$C_1 = \frac{\tau_p K_{PD} K_{VCO}}{\tau_z \omega_\mu{}^2 N} \sqrt{\frac{1+(\tau_z \omega_\mu)^2}{1+(\tau_p \omega_\mu)^2}} \tag{6.3}$$

$$C_2 = C_1(\frac{\tau_z}{\tau_p} - 1) \tag{6.4}$$

$$R_2 = \frac{\tau_z}{C_2} \tag{6.5}$$

From the design specifications of Table 6.1, we choose C2=5 pF, C1=50 pF, and R1=200 kΩ after compromising with other performances [83].

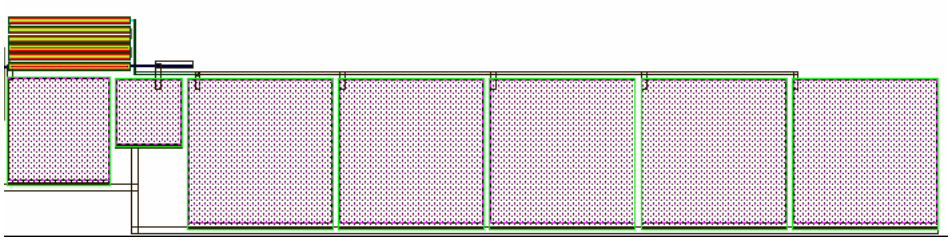


Figure 6.9: Layout of the loop filter

Figure 6.9 shows the layout of the loop filter. The Poly substrate resistors and MIM capacitors in the CSM library are used.

6.4 Design of the wideband VCO

A typical CMOS LC VCO employs a differential topology with cross-coupled NMOS, PMOS or complementary NMOS and PMOS pairs to realize the negative resistance to compensate for the loss of the resonator. The differential topology has advantages in a fully integrated circuit realization, providing the rejection of the common-mode supply and substrate noise and differential outputs. The negative resistance is created by the positive feedback of the cross coupled transistors. The variations of the differential topology with the cross-coupled pairs are shown in Figure 6.10. The selection of a topology depends on specifications of the VCO (phase noise, power consumption, and tuning range) and the technology.

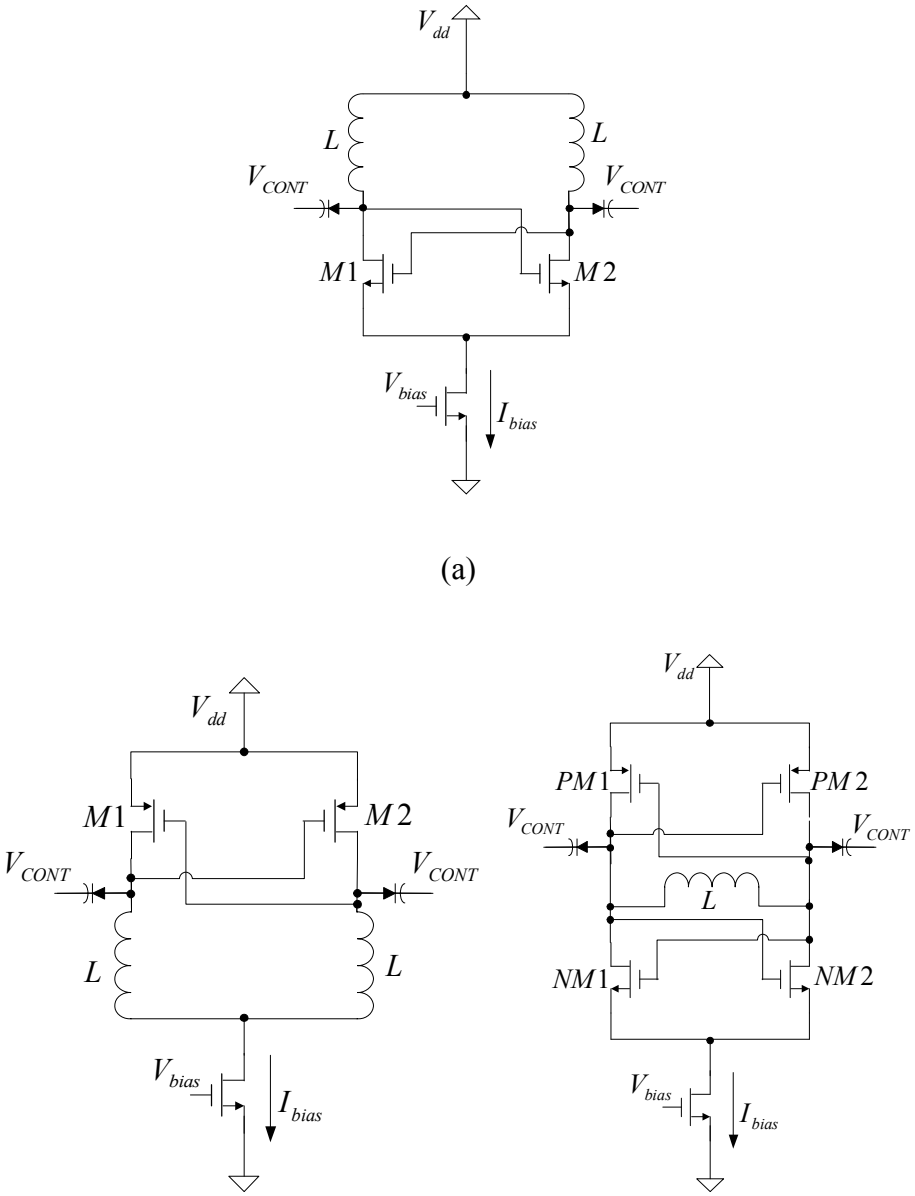


Figure 6.10: Topology of LC oscillators
a) NMOS only b) PMOS only c) NMOS-PMOS

The NMOS only topology in Figure 6.10.a has the advantage of higher transconductance per area compared with the PMOS only topology (Figure 6.10.b) due to the higher mobility of charges in NMOS devices than in PMOS devices.

Hence smaller transistor capacitances will contribute to the total parasitic capacitance of the resonator. However, PMOS devices have lower flicker noise than that of NMOS devices. For the NMOS-PMOS complementary topology, power consumption is lower than the NMOS or PMOS only topologies since the current is reused. For the same current consumption, the PMOS-NMOS topology has a better noise performance since it has twice the output amplitude compared to that of the NMOS only topology for a given current. As a result, for the same peak-to-peak output, the PMOS-NMOS topology has a lower bias current and a better symmetry in the output rise/fall time by matching the sizes of the PMOS/NMOS pair. The drawback of the PMOS-NMOS topology is the maximum output voltage swing is limited to the supply voltage.

A current source is used for biasing the active devices. It is also used to limit the output amplitude of the VCO and present a high impedance to the nodes connected to the resonator to decouple supply or ground from the resonator. However, the noise in the biasing rail MOS transistor is an important noise source in the VCO. Therefore, bipolar transistor can be used in the BiCMOS technology for a better noise performance [84]. And the VCO without the tail MOS transistor has been used for a high output amplitude and better phase noise [85].

There is a trade-off between the power consumption, the tuning range, and the phase noise performance when choosing the sizes of the MOS transistors and the basing point ($V_{gs} - V_{th}$). For lower power consumption, ($V_{gs} - V_{th}$) should be as low as possible. However, it requires a high value in W/L of the MOS transistors for a desired gain. As a result, larger parasitic capacitances will reduce the tuning range of the VCO. Alternatively, if W/L is reduced to increase the tuning range, the

output amplitude will be reduced. Hence, the phase noise, which is inversely proportional to the square of the amplitude, will increase significantly.

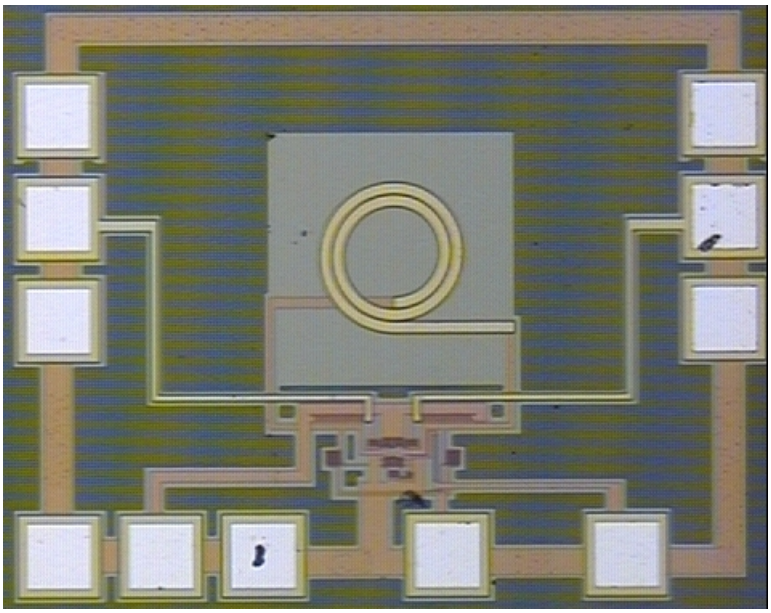


Figure 6.11: Test chip for a 5 GHz VCO

In the design of high frequency VCO, the main issue is the high quality factor of passive devices. The linearity of the varactor should be well to get a linear tuning frequency of the VCO. The transistor sizes should be choosing to have enough gain and maintain oscillation. In this project, a 5 GHz VCO has been designed based on the PMOS-NMOS topology. It has been implemented with the CSM 0.18 µm CMOS process. Figure 6.11 shows the die photo for the test chip. The measurement is carried out on wafer by the Cascade RF probe station. Figure 6.12 shows the measured output spectrum for this VCO. The tuning range of this VCO is shown in Figure 6.13.

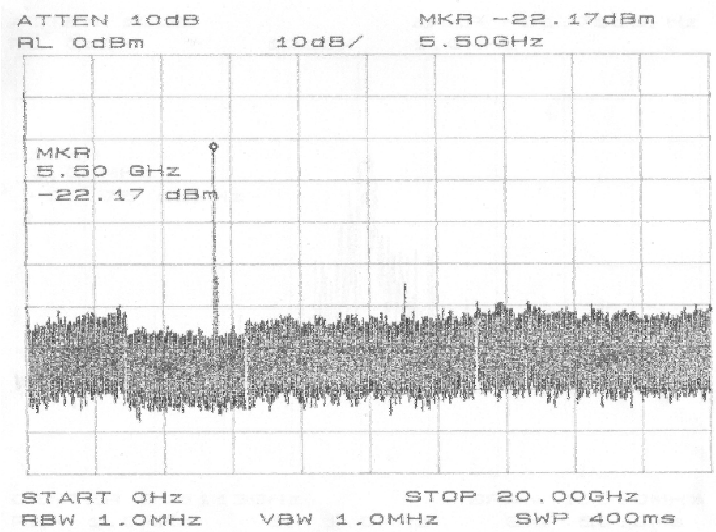


Figure 6.12: Measured output spectrum

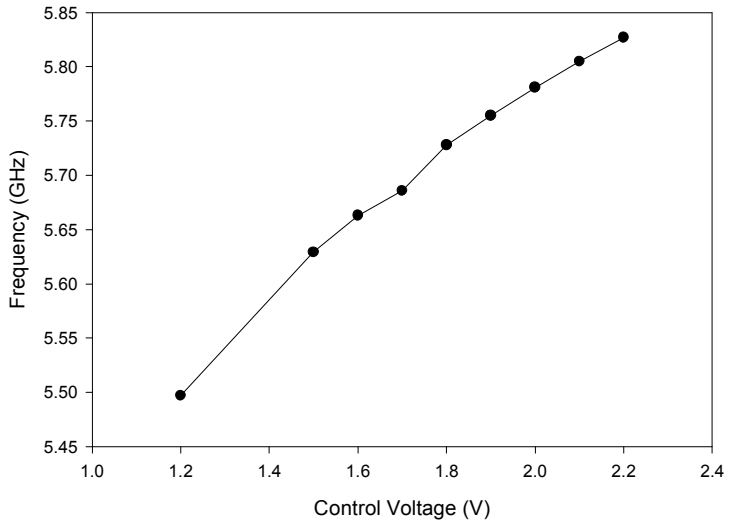


Figure 6.13: Operating range of the proposed VCO

It is observed that this VCO can not meet the requirement of the 5-6 GHz wireless LAN applications. Therefore, a wide band VCO is proposed by using two groups of PN-varactors.

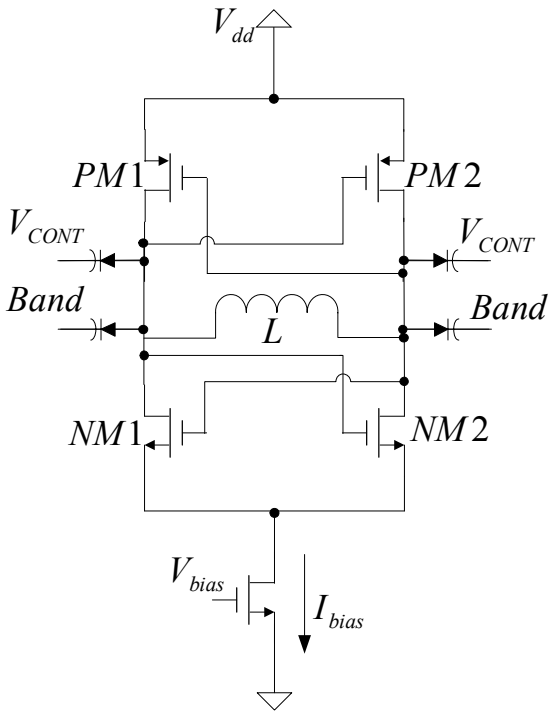


Figure 6.14: The proposed wide band VCO

Figure 6.14 shows the topology of the proposed VCO. By using the two groups of tuning voltage, the *Band* signal is connected to V_{dd} or ground for the different operating mode. The quality of the inductor provided by the CSM 0.18 µm CMOS process with a value of 1 nH has a quality factor of 7 in the frequency of 5.5 GHz while the varactors with a value of 500 fF have a quality factor of 30. Figure 6.15 shows the layout of this VCO. In the layout design, the symmetrical layout is maintained. While the interconnection of metal lines are keep compact to reduce the parasitic effects. The post-layout simulated tuning range and phase noise are shown in Figure 6.16 and Figure 6.17 respectively. The disadvantage of this topology lies in the additional control voltage is used. This means additional pad and larger silicon area is needed.

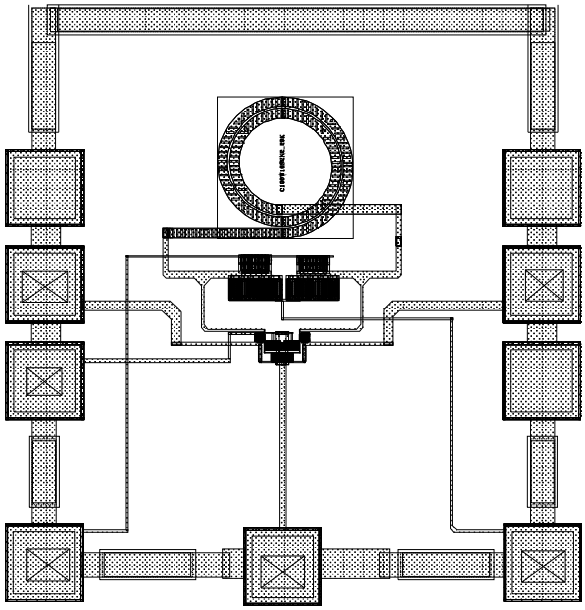


Figure 6.15: Layout of the proposed VCO

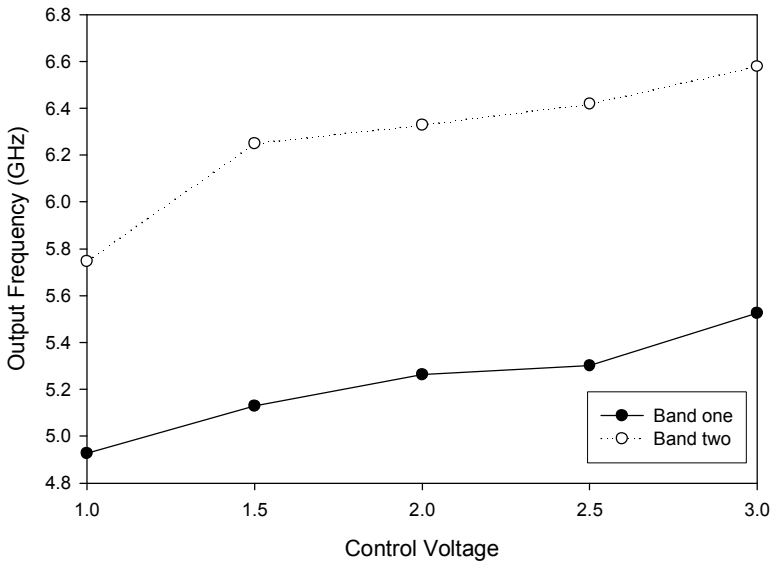


Figure 6.16: Tuning range of the proposed VCO

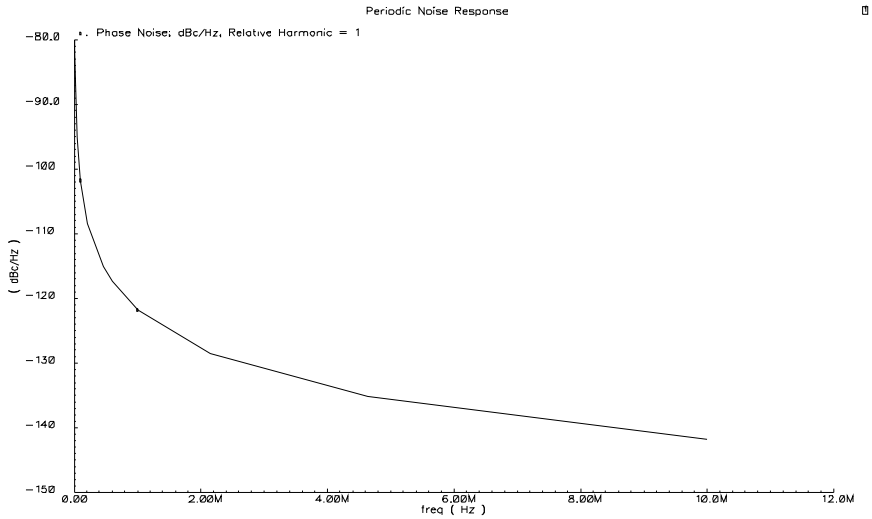


Figure 6.17: Output phase noise of the proposed VCO

6.5 Layout issues of the frequency synthesizer

In the layout design, the major concern for integrating the complete frequency synthesizer on a single chip is the noise coupling to the VCO from the prescaler. There should be not any close loop surrounding the inductors. The prescaler which is immediately next to the VCO can produce a large switching noise into the substrate. The noise can be coupled back to the VCO degrading its spectral purity. Therefore, several substrate contacts surrounding the prescaler are added to ground its switching noise. These contacts will also be helpful to minimize the coupling and parasitic capacitance to other routing wires.

Besides the VCO and prescaler, the other blocks, the PFD, charge pump and loop filter which are digital or mixed-signal circuits also need good isolation. The large area substrate contacts are used around such building blocks to reduce the noise

coupling to the VCO. The supply voltage for the VCO is also separated to reduce the coupling trough the power lines.

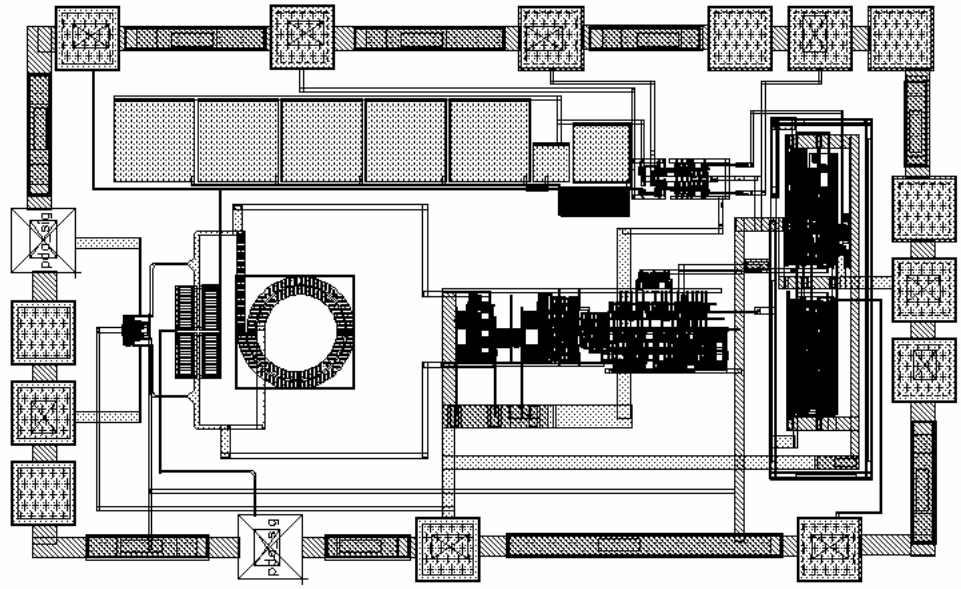


Figure 6.18: Layout of the proposed frequency synthesizer

The layout for the whole frequency synthesizer is shown in Figure 6.18. The total area is about $1100\mu m \times 700\mu m$.

6.6 Post layout simulation results

The behavior simulations, e.g. simulations in the Agilent Advanced Design System (ADS) or Mentor Graphic VHDL & VHDL AMS (Analog/Mixed Signal) are usually performed in the design of the complete frequency synthesizer. However, in the circuit implementation, there are many non-ideal effects. Therefore, the transistor level simulation using the Cadence SPECTRE RF is also carried out to include the non-ideal effects, e.g. the propagation delay in the loop, which may impact on the performances of the frequency synthesizer.

Figure 6.19 shows the output power spectrum of the proposed synthesizer respectively. The output transient result of the control voltage for the frequency synthesizer is shown in Figure 6.20.

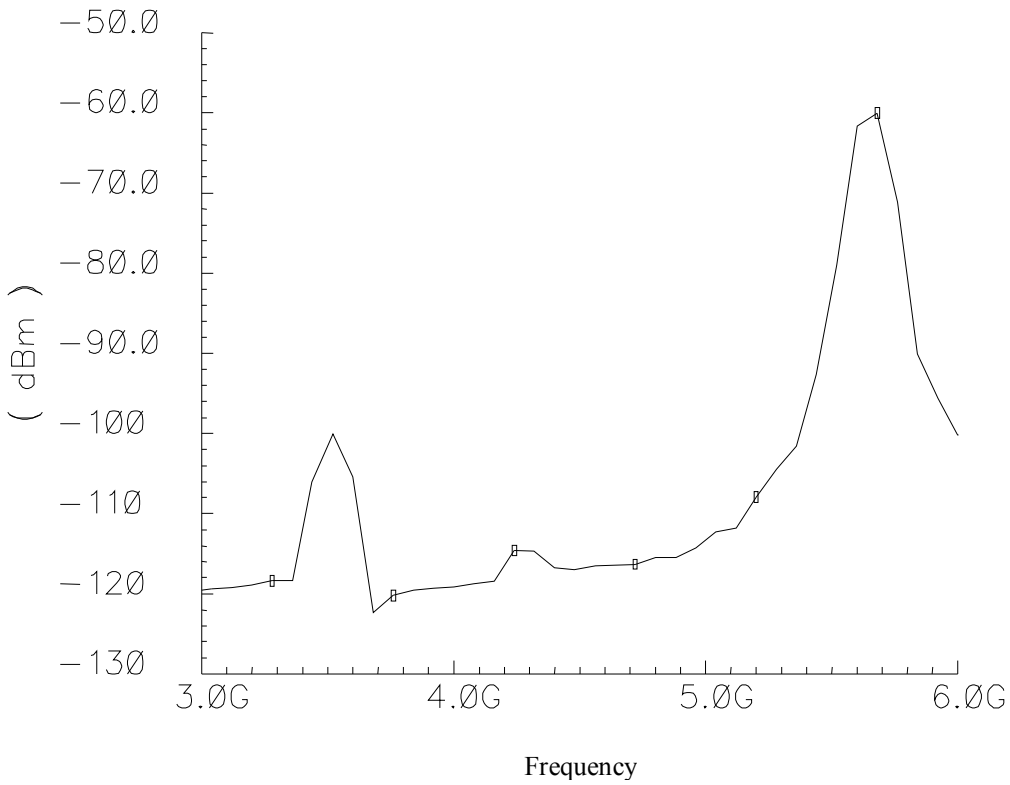


Figure 6.19: Output spectrum of the proposed PLL

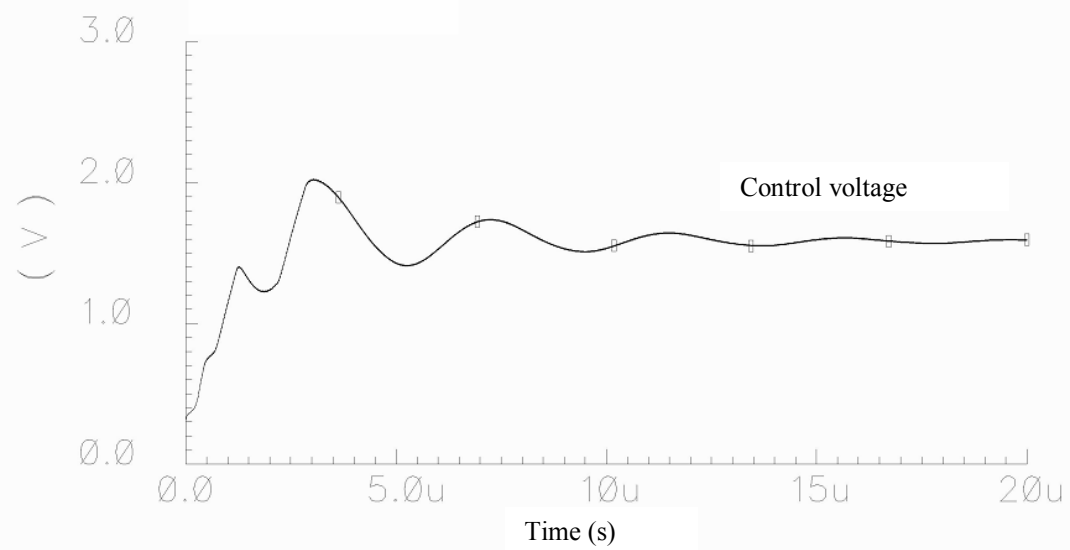


Figure 6.20: Transient response of the control voltage of the proposed PLL

6.7 Conclusion

In this chapter, the implementation of a 5-6 GHz frequency synthesizer is demonstrated using the CSM 0.18 µm CMOS technology. Several design techniques including wide band high resolution frequency divider and low phase noise wide band VCO are implemented in this design. The phase noise of the PLL is -120 dBc/Hz at the 1 MHz offset. The power consumption of this frequency synthesizer is 30 mW with an active chip area of $0.8\,mm^2$.

Chapter 7

High Speed Phase Detectors and Divide-by-2 Units

In Chapter 6, a 5-6 GHz frequency synthesizer implemented with the proposed building blocks has been demonstrated. As a basic sub-system in modern communications, the PLL has other potential applications, e. g. the CDR application. In the frequency synthesizer, the PD is always operating at low frequencies. However, in the CDR applications, the PD operates at higher frequencies. This makes the PD a challenging building block in the design of PLL. For the MCML structure, which is used as a basic divide-by-2 unit in high speed frequency dividers, the low power consumption and high operating frequency are very essential. In the CDR system (for SONET OC-192), a divide-by-2 unit which is able to operate at a 10 GHz is desired. In this chapter, these two building blocks are investigated and designed as an extension of the work in previous chapters. The design of a complete CDR system is, however, is complex and beyond the scope of this thesis.

7.1 A 10 Gb/s linear full-rate CMOS phase detector

Unlike the applications in a frequency synthesizer, in the CDR applications, the clock recovered by the PLL based CDR must satisfy three important conditions [10]: (1) It must have a frequency equal to the data rate, i.e. 10 GHz for 10 Gb/s data rate application. (2) It must be able to give a certain phase relationship with respect to the data to sample the input data. (3) It must have little jitters as it is the principal contributor to the retimed data jitters.

Such requirements come from the characteristics of the data format in the optical communication system. The non-return-to-zero (NRZ) data is most often used data format in the high speed optical communication applications to maximize the data rate within a given channel bandwidth. It is a more bandwidth intensive scheme compared with the return-to-zero (RZ) data. Figure 7.1 shows an example of the two data formats for the identical bit pattern. However, the RZ data requires twice the bandwidth of NRZ data to transmit the same bit sequence [10]. NRZ data has two attributes which make the recovery of clock and data signals, especially for the procedure of the phase detection, difficult. When there is absence of data transition, i. e., if the input NRZ data stream is a long sequence of "1"s or "0"s, the phase detector must not produce any false phase comparison. Moreover, the phase detector must incorporate some nonlinear operation to generate spectral information at the clock frequency. As a result, the phase detector for random data applications must be able to provide two essential functions: data transition detection and phase difference detection to cater for the attributes of the NRZ data format [10].

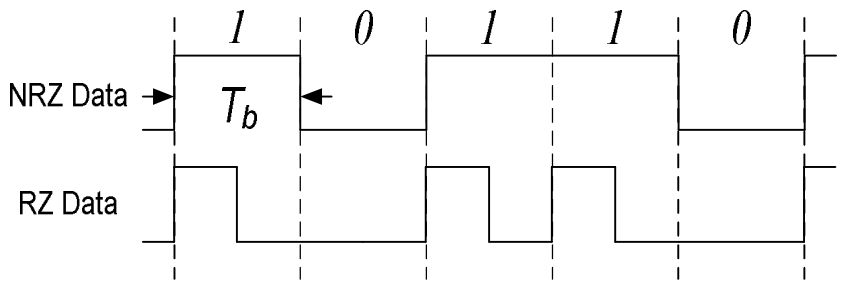


Figure 7.1: NRZ and RZ bit streams with identical bit patterns

The key considerations of the PD design are based on the design of the whole CDR system. Figure 7.2 shows a generic topology of a CDR system, which is different

from the conventional phase-locked loop (PLL) architecture for the frequency synthesis.

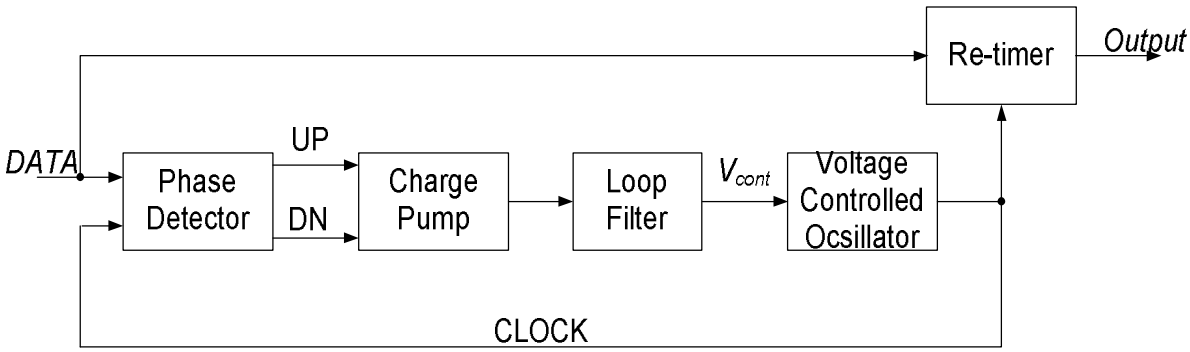


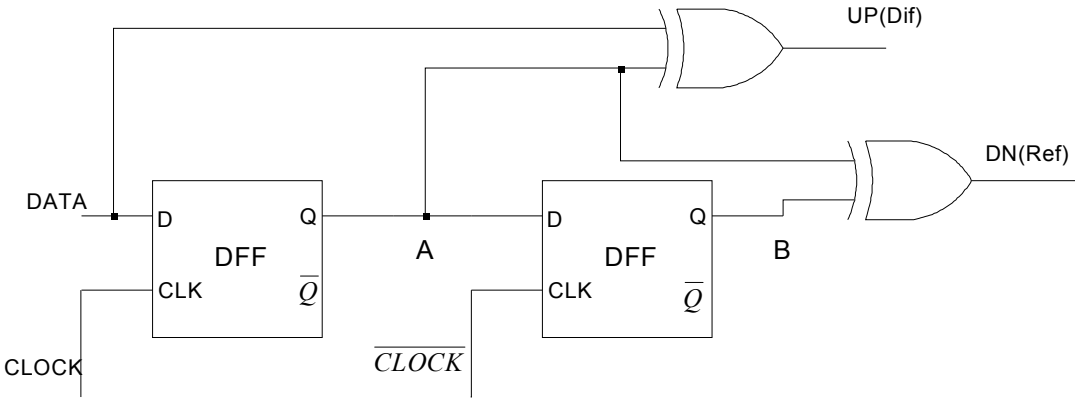
Figure 7.2: A generic topology of the CDR system

In a frequency synthesizer, the output of the VCO is divided by the frequency divider before it fed back to the PD. For the CDR circuit, the clock signal recovered from the VCO is directly fed back to the PD. Hence, the PD in this case must deal with high speed input data and clock signals. It must be able to provide a phase difference output with a good linearity over a wide range of the input phase offset to drive the charge pump and the loop filter. Among all the building blocks, the PD and the VCO are two most critical blocks which determine the overall performance of the CDR system. Due to the highest operating frequency, they are the most challenging blocks to be realized under the existing CMOS technology. For the application of SONET OC-192, the input data is 10 Gb/s NRZ data, which requires the PD to compare the 10 GHz clock signal with a 10 Gb/s data signal with a very broad spectrum. Moreover, the PD is formed by high speed digital circuits, which will take a great portion of the total power consumption. Such requirements have made the PD the most challenging block of the CDR system to be designed [86].

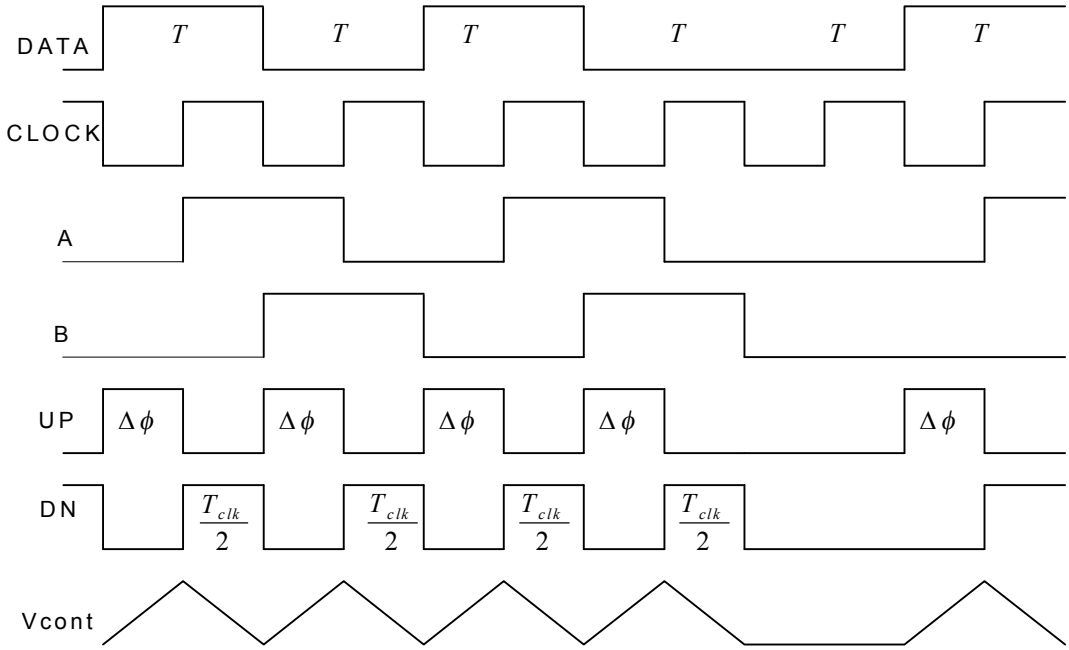
7.1.1 Review of linear PD design

Traditionally, there are two main categories of PDs that are dealing with random data input, namely the linear PD and the binary PD. A typical example of the binary PD is the Alexander PD [87]. The Binary PD produces two digital outputs, the *UP* and *DN*, to signal if the data is early or late with respect to the VCO clock. Normally, the binary information is spilt into two loops [88]. One loop is the phase-control loop formed with the *UP* and *DN* signals directly modulating the VCO frequency. The other loop is the frequency loop in which the *UP* and *DN* outputs are integrated with the charge pump and loop filter to control the second tuning input from the VCO. As compared with the architecture of the linear CDR circuit, the binary CDR architecture is more complicated, especially in the VCO design since the VCO requires two sets of tuning inputs. In the binary CDR circuit, the linear theory is not applicable any more; therefore the jitter exhibits highly nonlinear characteristics. The most undesired feature of the binary CDR circuit is that the binary PD creates significant ripples on the VCO control line and hence great jitters at the VCO output [89].

The linear PD has an average output voltage that is linearly proportional to the phase difference between the data and clock inputs. The merit of well-defined gain characteristics between the output of a linear phase detector and the clock/data phase offset at the inputs makes it become the main stream of the phase detector in the CDR design [90]. In this chapter, only the linear PD is discussed.



(a)



(b)

Figure 7.3: Hogge's PD (a) Architecture (b) Operation

Hogge's PD is widely used for its simple topology [91]. Figure 7.3 shows the topology and operation of the Hogge's PD. The input data signal is first sampled by the clock signal at the first DFF, producing the signal *A* which is a delayed replica of the input data. The delay time is just the phase difference between the input data and clock signal. The signal *A* is then XORed with the input data signal

to give the output signal *UP*. The pulse width of the output signal *UP* (Dif) is therefore linearly proportional to the input phase difference and a pulse appears for each data transition. The output pulses are called proportional pulses, which provide the function of the phase difference detection. The other output pulse *DN* (*Ref)* is produced to eliminate the data pattern dependency. The reason is that the average value of the *Dif* pulses is a function of the data transition density, which is not able to uniquely represent the phase difference for various data patterns. For instance, the average value of the signal *Dif* is not changed if the transition density falls by a factor of two and the phase difference rises by the same factor [92]. The signal *DN* (Ref) appears on every data transition edge and has a constant pulse width. In the Hogge's PD, the signal *A* is further sampled by the complementary signal of the clock to produce the signal *B*, then the signals *A* and *B* are XORed to get the signal *DN*(*Ref)*. The *UP* and *DN* signals are fed to the charge pump and the loop filter to generate the control voltage of the VCO. Under the lock-in condition, the rising edge of the clock signal samples the midpoint of each bit for optimal sampling of the data stream, where *Dif* and *Ref* produce equal pulse widths [92].

The Hogge's PD has a very simple topology which is easy to implement. However, for the application of the 10 Gb/s SONET OC-192 standard. To overcome the difficulties of implementation using the 0.18 μm CMOS process, in [93], a half-rate CDR architecture is proposed. In this design, the VCO is operating at a frequency equal to half of the data rate, therefore reducing the operating frequency of the PD. The topology of this simplified half-rate linear phase detector is shown in Figure 7.4.

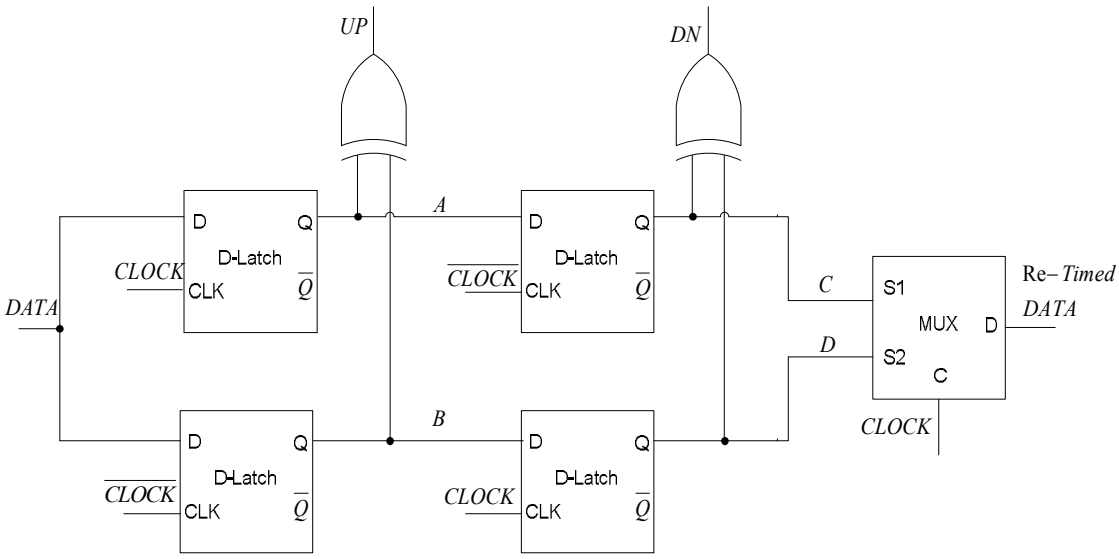


Figure 7.4: Half-rate PD in [93]

The half-rate linear PD consists of four latches and two XOR gates. The data is applied to the inputs of two sets of the cascaded latches, each constituting a flipflop that retimes the input data signal. The clock signal is operating at half rate, i.e., 5 GHz for 10 Gb/s NRZ input data stream. The pulse width of the signal A and the signal B will be $\frac{T_{CLK}}{2}+\Delta\phi$ and $\frac{T_{CLK}}{2}-\Delta\phi$ respectively, where T_{clk} is the period of the clock signal and $\Delta\phi$ is the phase difference between the input data and clock signals. Then these two signals are XORed to get the *UP* (*Dif*) signal which has a pulse width of $\Delta\phi$ for each data bit. The pulse width of the *UP* signal is linearly proportional to the input phase difference. Similar to the Hogge's PD, to get the reference signal, the signals A and B are further sampled by the complimentary clock signals to generate the signal C and the signal D. The two signals are identical except for a phase difference which is equal to half of the clock period. Then the signal C is XORed with the signal D to produce a constant-width pulse on every data transition, which is the *DN* (*Ref*) signal.

7.1.2 Limitation in existing designs

From the brief review of existing designs, it is observed that full-rate operation of 10 Gb/s application of PD implemented in the 0.18 μm CMOS process is still not available. In the Hogge's PD, the clock-to-*Q* delay for the D flip-flop is in the same order of the clock period and the conventional Hogge's-type phase detector will not function reliably. Moreover, the Hogge's PD has the problem of the half period skew [89].

The first challenge of the PD design for CDR applications lies in the operating speed. To solve the difficulty of the high operating frequency, in [93], a half rate clock is used instead. However, its circuit implementation still has the problems of producing the output pulse as short as half of the bit duration [94]. Moreover, the half-rate operation also makes the system sensitive to the data pattern [90].

Another issue in the Hogge's PD design is the output data pattern. In the Hogge's PD shown in Figure 7.3, the *UP* and *DN* signals of PD's output are used to drive the charge pump and loop filter to generate the control voltage of the VCO. The control voltage of the VCO suffers a ripple as illustrated in Figure 7.3.b, because the pulses of the *UP* and *DN* are of limited pulse width and *DN* always follows *UP* without overlaps. As a result, the output frequency of the VCO will fluctuate even in the locked condition [89]. To solve the problem of the half period skew, a complex topology has been proposed [95]. Until now, there is no simple and effective way to solve these two issues in the design of the phase detector for 10 Gb/s applications.

7.1.3 Proposed topology

From the above analysis for the existing PDs, the difficulty of operating at the full clock rate lies in the requirement of the narrow output pulses. Even for the half rate PD in [93], the restriction of the narrow pulses still exists because the pulse width of the phase difference output signal is $\Delta\phi$, which is less than half of a bit duration. If the pulse widths of the *UP* and *DN* signals can be enlarged but their difference still follows a linear relationship with the input phase offset, the difficulty in the circuit design can be overcome. For example, if the output pulse width is change to $T-\Delta\phi$, where T is the bit duration, the output signal is still linearly proportionally to the input phase difference but the pulse width has been enlarged. The implementation of circuit design becomes easier. The bottleneck of the PD design lies in the two input signals, namely the clock signal and the input data signal.

In this design, the input data are split into the *I* and *Q* data streams to double their pulse width while maintaining the data information (data transitions).The clock is kept at 10 GHz. The *I/Q* splitter circuit is implemented by a toggled master-slave D flip-flop (DFF) as shown in Figure 7.5. It consists of two D-latched. MCML (MOS Current Mode Logic) circuits are used for their good noise performance and high speed operation. Hence, the *DATA/2Q* and *DATA/2I* output signals trace the rising edge and falling edge of the input data respectively as shown in Figure 7.6, and the pulse width of the output signals has been enlarged. If the input data pattern is “1010”, a 100% increase of the pulse width for both signals can be achieved.

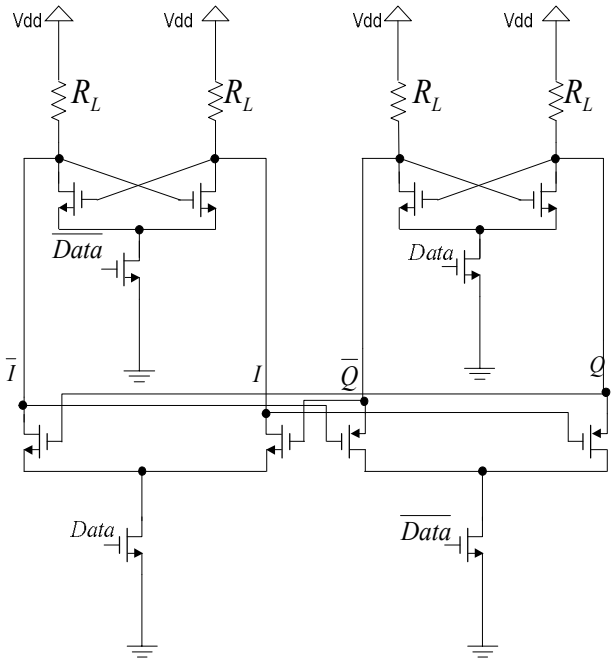
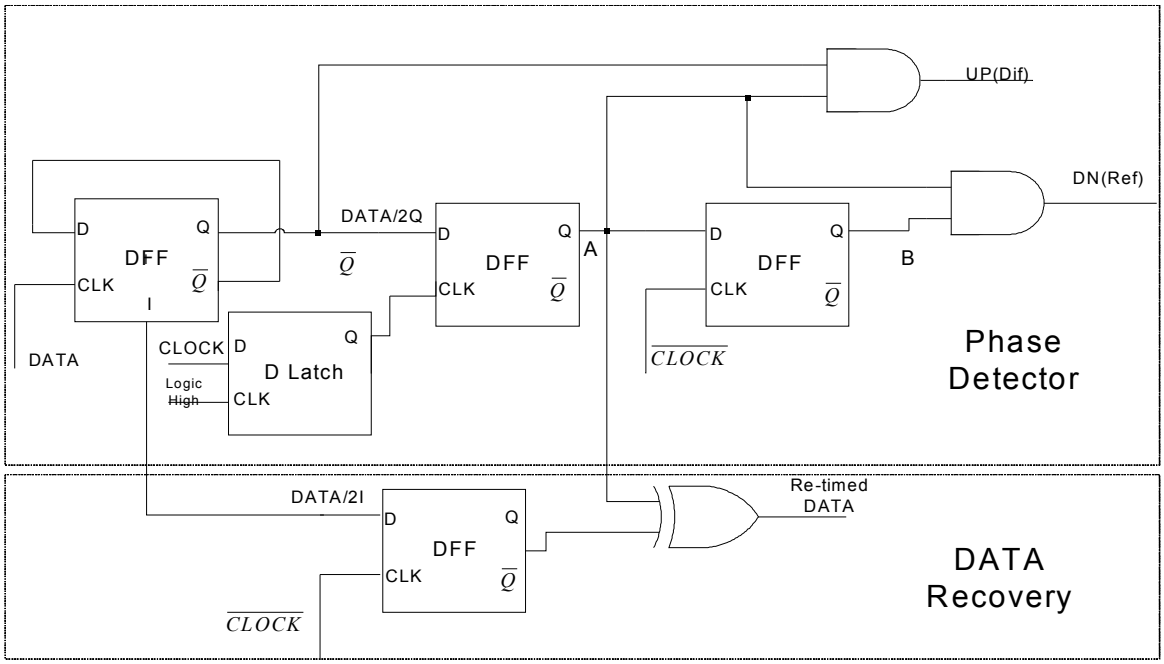


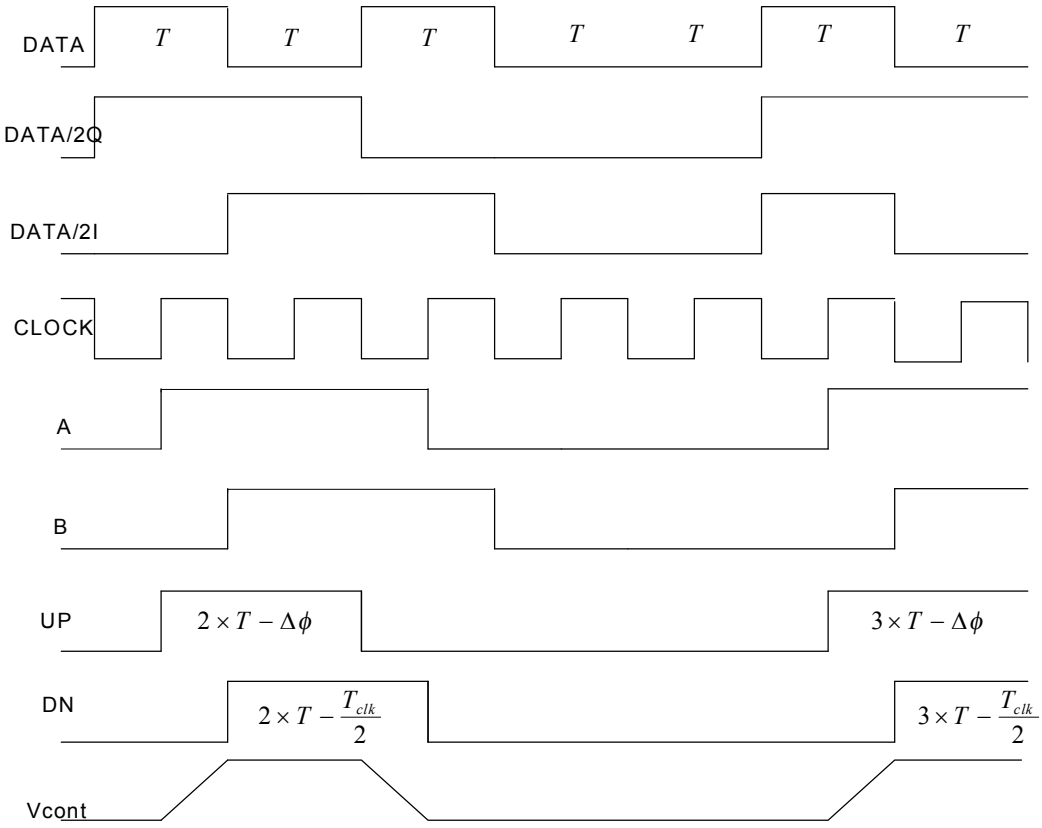
Figure 7.5: Toggled master slave DFF as an I/Q splitter

At the following stages, the logic XOR in the Hogge's PD is changed to the AND function in the proposed PD to provide a linear relation between the input phase offset and the output signal. As the toggle D flip-flop is formed by two master-slave D latches, which delays the input *DATA* signal by one D-latch. To compensate for the delay between the *CLOCK* signal and the *I/Q DATA* signals, the *CLOCK* signal is passed through a D-latch. Different from [93], by using the full-rate clock, the proposed PD satisfies the requirement of narrow output pulses and has the performance of a full-rate linear PD. Moreover, the proposed PD improves the output data pattern. The pulse width is enlarged to give a stable output to the charge pump and the loop filter. The *UP* and *DN* signals are used to drive the charge pump as the charging and discharging respectively. In Figure 7.3.b (Hogge's PD), the total ON time of the phase difference signal (*UP*), the charging time is $m \times \Delta\phi$, where m is the number of data transitions and $\Delta\phi$ is the input phase offset. The total ON time of the phase reference signal (*DN*), the

discharging time is $m \times \frac{T_{clk}}{2}$, where T_{clk} is the period of the *CLOCK* signal. In the proposed PD as shown in Figure 7.6.b, the total ON time of these two signals has been enlarged to $n \times T - m \times \Delta\phi$ and $n \times T - m \times \frac{T_{clk}}{2}$ respectively, where n is the number of clock periods and T is the bit duration, T = 100 ps for the 10 Gb/s data rate. Due to the overlap between the *UP* and *DN* signals, the ripples in the control voltage of the VCO caused by the half period skew has been reduced.



(a)



(b)

Figure 7.6: The proposed PD a) topology b) operation

To achieve the 10 GHz operation with a good noise performance, the building blocks in the proposed PD are constructed by MCML structures. Among them, the DFF is the most challenging cell in this design because of its high operating frequency. The inductors can be incorporated in the DFFs to extend the bandwidth [86], however, this will introduce large silicon areas of inductors. So in the proposed designs, only the optimization and transistor sizing are carried out based on the standard MCML DFFs. The topology of the DFF is the same as Figure 7.5 shows; the only difference is that in Figure 7.5, the output signal of Q is fed back to the input of the first D latch.

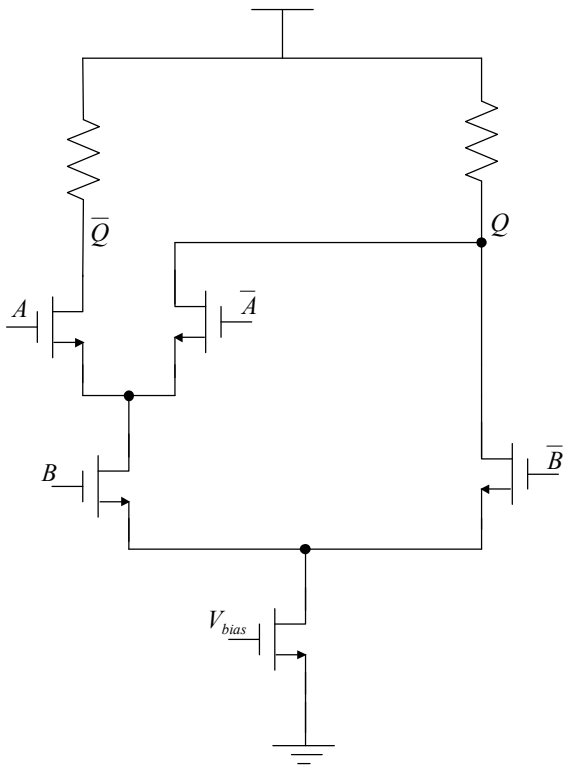


Figure 7.7: The schematic of the MCML AND gate

The resistive load is used instead of the PMOS load to reduce the load capacitor of the output. As discussed in Chapter 4, at higher operating frequency (bit-rate), to reduce the delay, the biasing current is increased which the load resistor is reduced to keep a similar output voltage swing. The AND gate is also implemented with

MCML structure. Figure 7.7 shows the MCML circuit implementation of AND gate.

7.1.4 Simulation results

A comparison of the proposed PD and the half-rate PD in [93] is carried out on the grounds that [93] achieves the best performance in literature so far. The PMOS and NMOS devices of all individual blocks are of the same size and all the blocks are standard MCML circuits. The simulations are performed using the Cadence SPECTRE RF for the CSM 0.18 μm CMOS process. Because of the design difficulties, in [93], the 2.5 V supply voltage is used to reduce the propagation delay. However, in the proposed PD, it is able to function properly at a lower supply voltage of 1.8 V instead of the 2.5 V supply voltage. Figure 7.8 and Figure 7.9 show the simulation results of the PD in [93] and the proposed PD respectively.

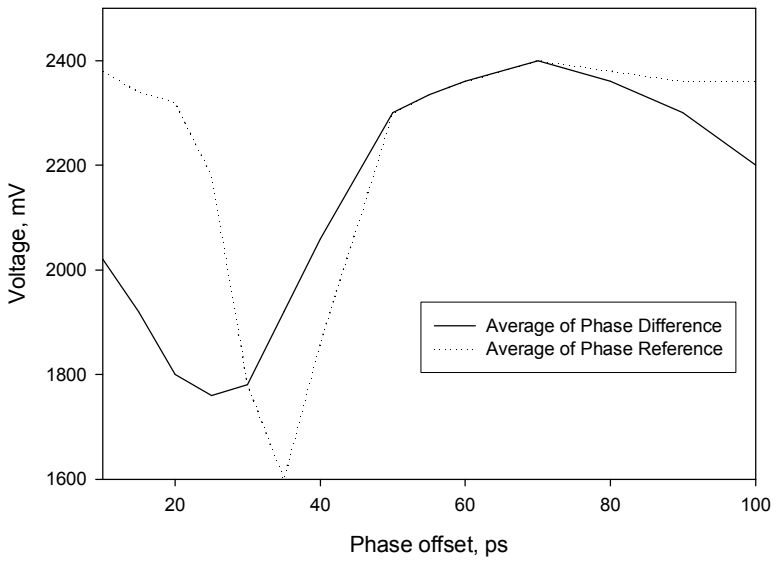


Figure 7.8: Simulation result of the PD in [93]

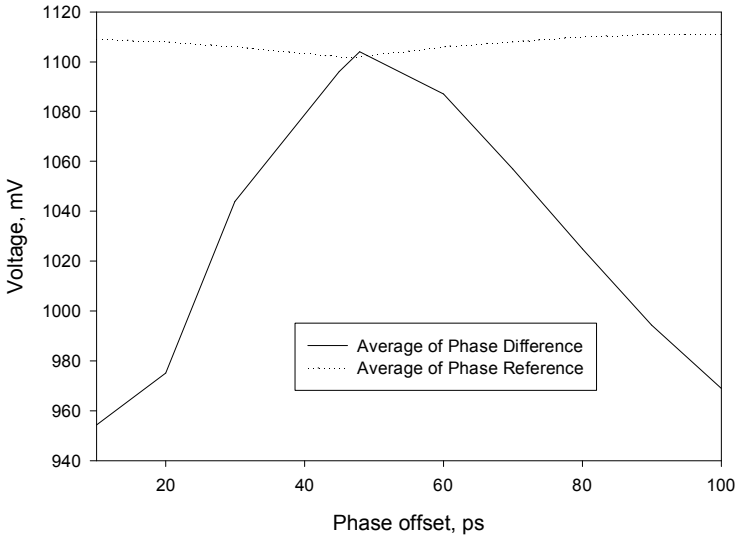


Figure 7.9: Simulation result of the proposed PD

The horizontal axis presents the input phase offset, which is from 0 ps (0 degree) to 100 ps (360 degree), while the vertical axis indicates the average output voltage for the phase difference UP and phase reference DN signals. In the half-rate PD, one operation cycle of the input phase offset is from 0 ps to 100 ps, while in the proposed full-rate PD, the operations are from 0 ps to 50 ps and 50 ps to 100 ps. The results show that the proposed PD has a wider operating range of input phase offset with a better linearity as compared with that of the PD in [93]. As shown in Figure 7.8, the average output voltage of the *DN* signal of the PD in [93] suffers a glitch at about 35 ps and the linear operating range of the *UP* signal is limited. However, as shown in Figure 7.9, for the proposed PD, the average output voltage of the *UP* signal is linearly proportional to the input phase difference for the whole operating range (0 ps to 100 ps), while the average value of the *DN* signal is almost constant. The two signals have approximately the same average value in the locked condition (50 ps). The power consumption of the proposed PD is 31 mW with a 1.8 V supply voltage for the 10 GHz clock and 10 Gb/s NRZ data, while the power

consumption of the PD in [93] is 28 mW under the same operating condition. The results show that the proposed PD is able to operate at the full clock rate and deliver a better performance than that of the PD in [93]. Table 7.1 compares the proposed PD with some PDs reported.

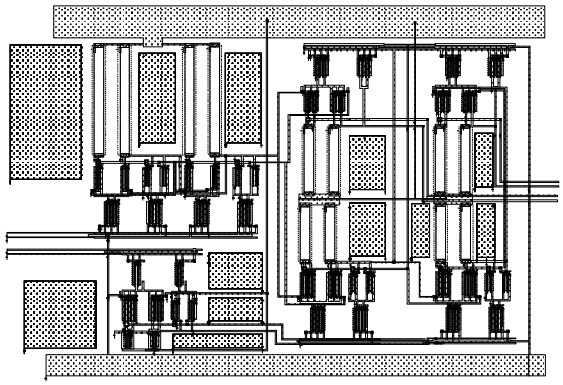


Figure 7.10: Layout of the proposed PD

The layout of the proposed PD, as shown in Figure 7.10 is performed and the post-layout simulation is done by including the process corner and parasitic effects. Because the proposed PD is designed using the standard MCML logic units, its performance can be obtained as that of the pre-layout simulation. However, the power consumption increases significantly to 65mW.

Table 7.1: Comparison between proposed PD and other PDs reported in Literature

PD	Linear/Binary	Data rate	Block elements	Power Consumption
Linear PD in [93]	Linear	10-Gb/s Half rate	4 Latches and 2 XOR gates	33mW Measured (28mW simulated)
Binary PD in [96]	Binary	10-Gb/s Half rate	6 DFFs and 3 Multiplexers	42mW Measured
Proposed PD	Linear	10-Gb/s Full rate	1 D latch, 3 DFFs and 2 AND gate	31mW Simulated

7.2 A new 1 V 10 GHz CMOS frequency divider with low power consumption

The divide-by-2 unit is the basic building block of the frequency divider. In the SONET OC-192 applications, a divide-by-64 function, which is formed by the cascaded divide-by-2 units, is also needed. Several CMOS high speed frequency dividers, including static and dynamic load dividers, have been reported [97] [98]. In these designs, the MCML circuits are used to achieve the high operating frequency and low phase noise at the expense of a continuous dissipation of power. A dynamic CMOS circuit, which only consumes power during the switching, is, however, limited to a lower operating frequency [99]. Therefore, the choice between the MCML and the dynamic circuit is a trade-off in power consumption and operating frequency. In this chapter, the parameters of a basic frequency divider are examined and a new dynamic inverter for the D flip-flops using MCML configuration is proposed to achieve a low power consumption with an enhanced output swing. A frequency divider implemented with this D flip-flop is also presented.

7.2.1 Design challenging in the divide-by-2 unit

At the overview of PLL, the power consumption and propagation delay of the MCML circuit have been analyzed in detail. The MCML circuit has two drawbacks, one is the constant power dissipation, and the other is the difficulty of the full integration in a digital system [100]. In [100], a dynamic MCML circuit with limited output swing is proposed to reduce the power consumption since the power consumption is linearly proportional to the voltage swing. Thus, there is a trade-off between the output voltage swing and the power consumption. In the frequency synthesizer application, the frequency divider consists of cascaded

divide-by-2 units. Therefore, the output swing is an important parameter as its amplitude must be sufficient to drive the next stage. The output signal of an MCML circuit is pulled down from V_{dd} periodically with a voltage swing of V_{swing}. If the swing is not large enough to drive the capacitive load of the next stage, a source follower is needed at the output stage of the divide-by-2 unit to increase the voltage swing [44]. The requirement of the source follower introduces the additional components and power consumption. Such a requirement makes the MCML circuit undesirable for large scale integration. Moreover, there is a dilemma in deciding the value of the load resistor. For high operating speeds, the load resistance should be as low as possible. However, a large load resistance is needed for a sufficient voltage swing to drive the next stage [97]. To solve this difficulty, the dynamic PMOS load was first proposed for the MCML frequency divider to replace the constant resistive load and to increase the operating frequency [97]. However, the supply voltage of the frequency divider still has to be high enough to ensure a proper operation. The minimum value of the supply voltage is given by [101]:

$$V_{dd} > \left|V_{tp}\right| + V_{tn} + 0.3 \tag{7.1}$$

For example, for the CSM 0.18 μm CMOS process, where the V_{tn} and $\left|V_{tp}\right|$ are about 0.5 V and 0.3 V respectively, the minimum supply voltage is about 1.1 V.

In [101], the inverters of MCML blocks (single-end part), which are illustrated in Figure 7.11.a, b, c, are investigated, and their output swings (slew rate) are simulated.

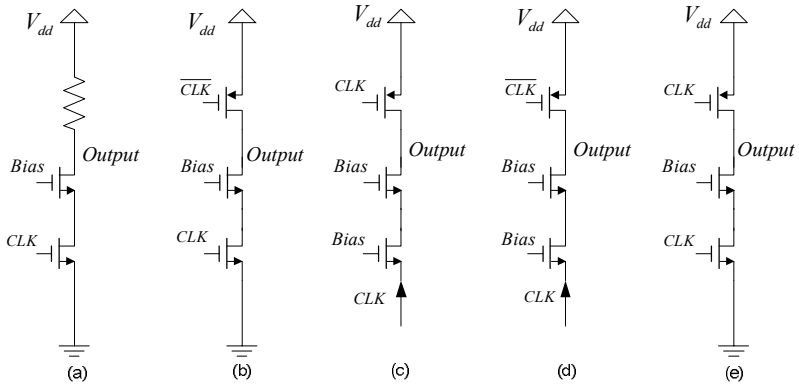


Figure 7.11: The inverters of different load

Figure 7.11.c shows a novel common-gate configuration which is implemented for 1 V supply voltage applications as proposed in [101]. In its inverter design, a PMOS transistor is used as the dynamic load. By using the common gate topology, the low supply voltage under 1V is achieved. The inverters and frequency divider in [101] are shown in Figure 7.11.c and Figure 7.12. Because of the inversed input in the common-gate configuration, the inverters in Figure 7.11.b and Figure 7.11.c have the same logic function. By reducing the supply voltage, the power consumption is reduced greatly. However, from the view point of the digital CMOS circuit design, when *CLK* has a logic low, the output should be pulled down to a logic low; however, the logic low of the input in the PMOS load will pull up the output. Such an operating mode actually causes a short circuit of the supply voltage to the ground. The removal of the rail NMOS in [101] and [102] causes a constant "on" status for the latch stage which increases the power consumption.

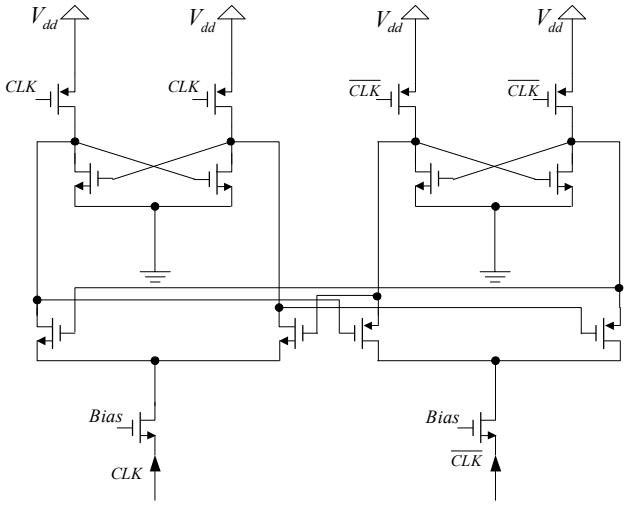


Figure 7.12: The divide-by-2 unit in [101]

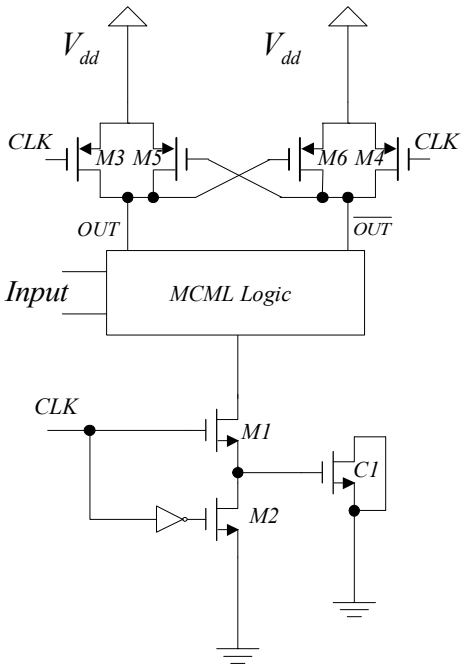


Figure 7.13: Dynamic MCML

In [100], the Dynamic Current Mode Logic (DyCML) is first proposed as shown in Figure 7.13. In this design, a *CLK* controlled PMOS-NMOS pair is introduced. It employs a dynamic current source with a virtual ground to eliminate the static power and other side effects associated with the conventional static current source

[100]. As shown in Figure 7.13, during the low phase of the clock, the precharge transistors, *M3* and *M4* are turned on to charge the output to a logic high, while *M2* is turned on to discharge capacitor *C1* to the ground. Meanwhile, *M1* is off, eliminating the DC path from the supply to ground. This architecture achieves the high speed characteristics of the MCML circuit and overcomes its drawbacks. There is no static power consumption in this circuit since *M1* and *M3* will never be turned on simultaneously. However, in this topology, the output swing is still limited due to the cascade of NMOS transistors.

7.2.2 Proposed topology

A new MCML inverter that integrates the dynamic configuration, instead of only the dynamic load, is proposed as shown in Figure 7.11.d. It optimizes the performances in the power consumption and output voltage swing. Differing from [101], in this inverter, since the input of the PMOS load is $\overline{CLK}$, a dynamic circuit is formed, and the output swing is enhanced significantly with the common-gate pull-push configuration.

The operation can be described as follows: if the signal *CLK* has a logic low, the biasing voltage will turn on the rail NMOS, then the output will have a logic low as well. In this state, the logic high of signal $\overline{CLK}$ turns off the PMOS, consequently, the leakage of current to ground is blocked. Therefore, the proposed inverter is logically equivalent to a dynamic circuit shown in Figure 7.11.e, a dynamic configuration of an inverter. As a result of the differential configuration of the dynamic circuit, the static power consumption is reduced and no longer proportional to the input frequency. This topology is similar to the configuration of

DyCML in [100]. However, by removing the cascaded MOS transistors, the parasitic capacitances have been reduced and the output voltage swing has been enhanced. The proposed inverter is able to operate at a higher frequency with lower power consumption and larger output swing.

7.2.3 Simulation results

A comparison of the performance of this new inverter, the inverter in [101], the dynamic load [97] and resistive load inverters [98], is carried out on the ground that [101] achieves the best performance in the literature so far. The PMOS and NMOS devices of all individual bitcells are of the same size. The simulations are performed using the Cadence SPECTRE RF for the CSM 0.18 μm CMOS process.

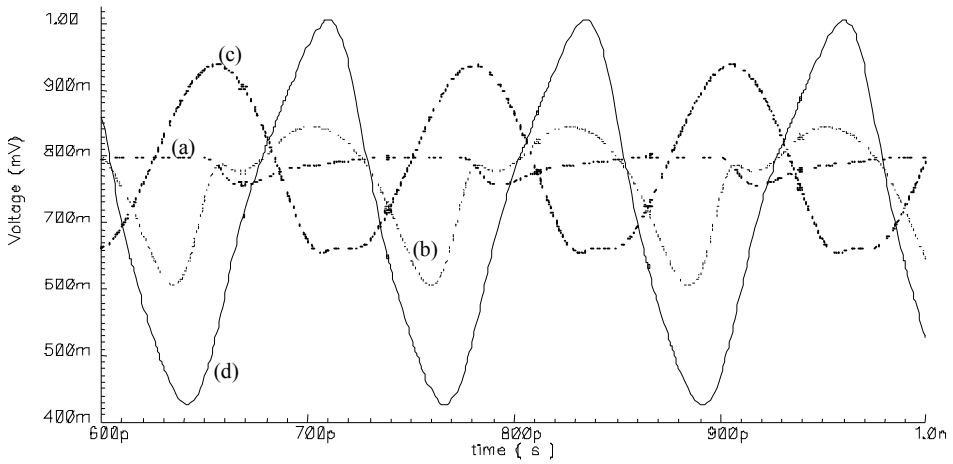


Figure 7.14: The transient results of the inverters

(a) **resistive load (b) dynamic load (c) [101] (d) proposed**

The transient result of these four inverters, namely resistive load, dynamic load, inverter in [101], and proposed inverter, are illustrated with (a), (b),(c), (d) in Figure 7.14 respectively. The results show that the proposed inverter is able to provide an enhanced output swing better than that of other inverters.

Figure 7.15 and Figure 7.16 summarize the simulation results of the output swing and power consumption of four inverters: the proposed inverter, the inverter in [101], the dynamic load and resistive load inverters respectively. All the MOS transistors employed are of the same size. In the typical working conditions, where the biasing voltage that should be as large as possible to achieve a high headroom is 1 V, and the input amplitude is 0.3 V, the proposed inverter dissipates less than 50% of the power consumption of the inverter in [101] due to the former's reduced static current. As the input amplitude increases, the power consumption of all existing inverters increases while the power consumption of the proposed inverter increases slightly.

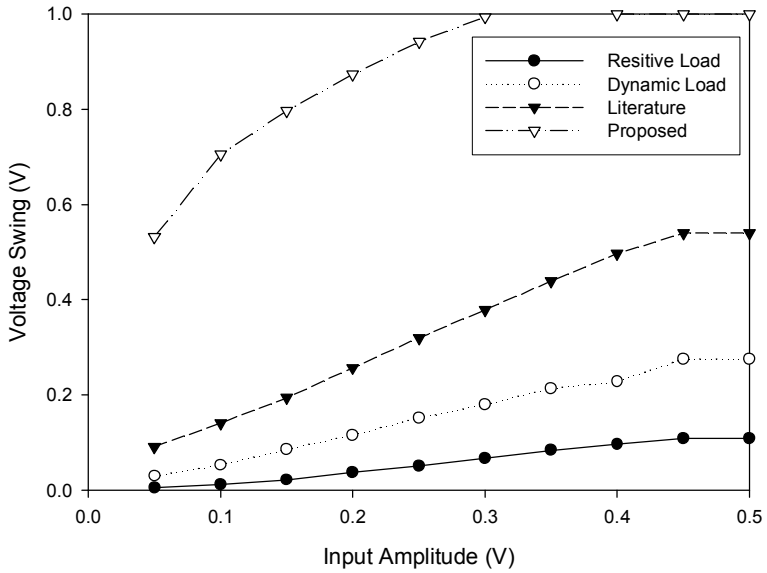


Figure 7.15: The output voltage swing for the inverters

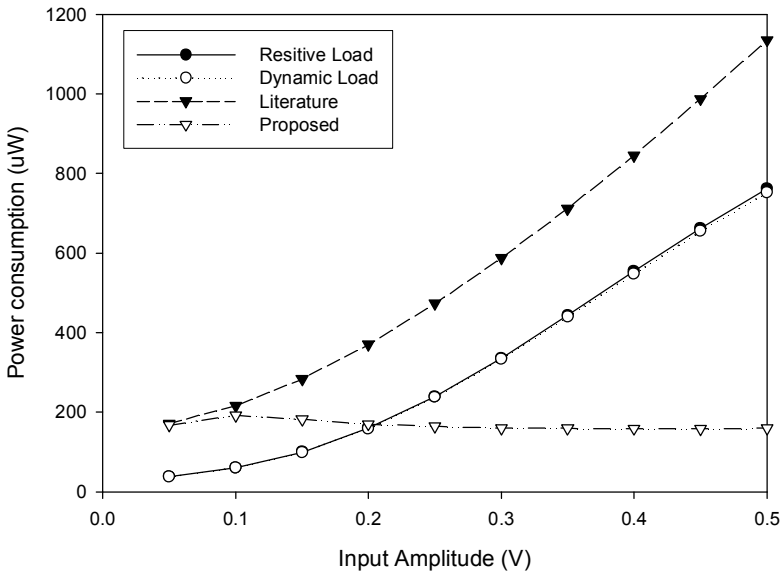


Figure 7.16: Power consumptions of the inverters

For the output swing, the proposed inverter achieves an improvement of more than 200% as compared to the output swing of inverter in [101]. The merit of the higher output swing is its ability to directly drive the following stages without using an additional buffer.

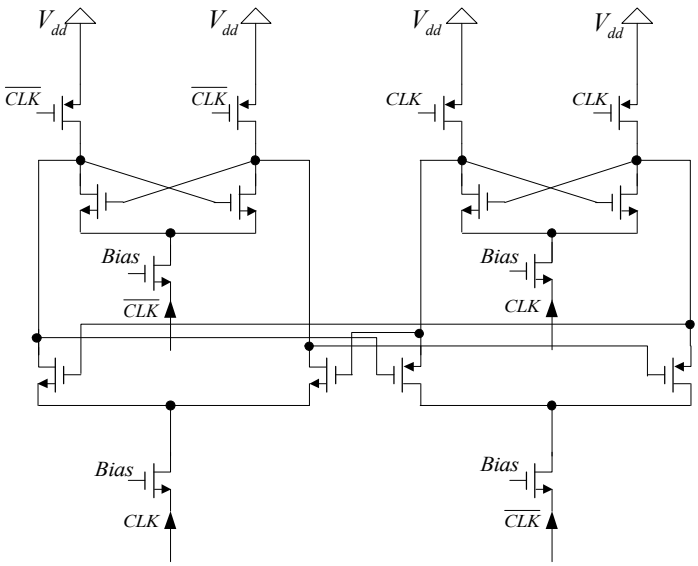


Figure 7.17: The proposed frequency divider

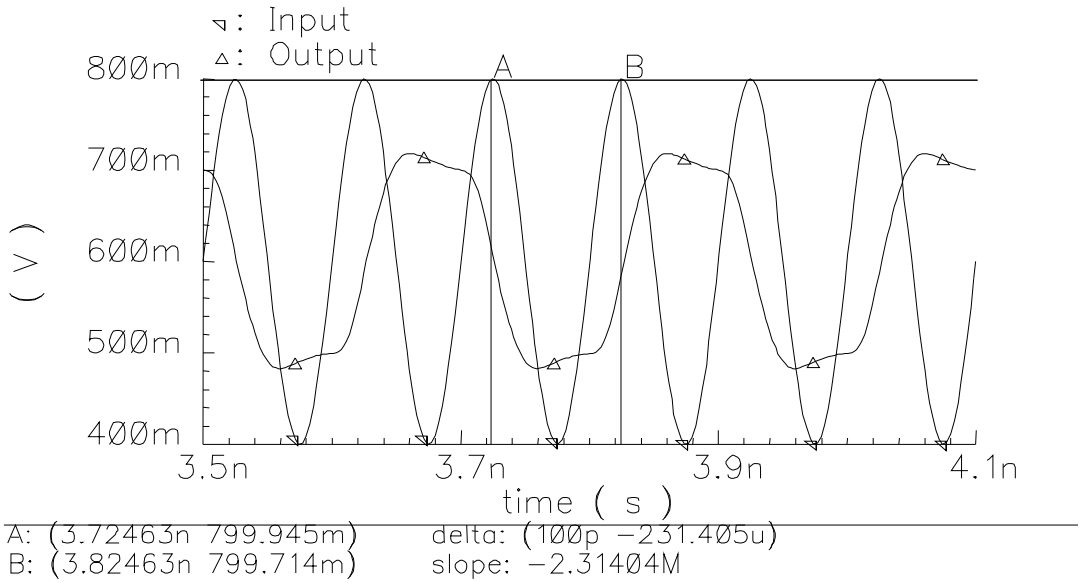


Figure 7.18: The transient result of the proposed frequency divider

To further verify the advantages of this proposed inverter, an MCML frequency divider implemented with this inverter is constructed as shown in Figure 7.17. The common gate rail NMOS in the latch stage is used to reduce the static power consumption. The function of the divide-by-2 is achieved in a similar manner as reported in [102]. In order to eliminate the difference in the process, simulations of the proposed frequency dividers and the divider in [101] with the same configuration and transistors' size are performed in the CSM 1P6M 0.18 µm CMOS process to verify the power consumption and the maximum operating frequency.

Figure 7.18 shows the transient result of the proposed frequency divider with an input of 10 GHz, while Figure 7.19 summarizes the simulation results of the power consumption over the operating frequency of the two frequency dividers. Due to the process limitations, the simulation above 10 GHz is not performed. However, the result shows that the proposed frequency divider is able to operate at higher frequencies with lower power consumption in comparison to the performance of

the frequency divider in [101].

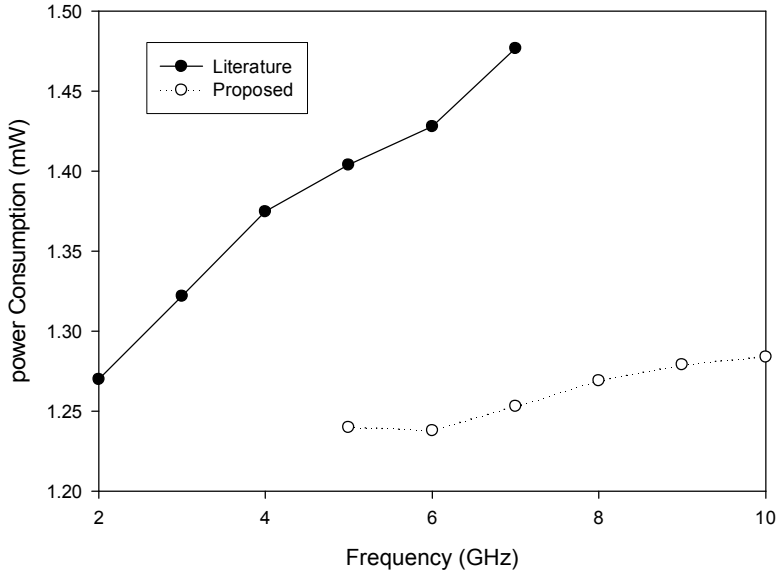


Figure 7.19: Power consumption vs. operating frequency of the two dividers

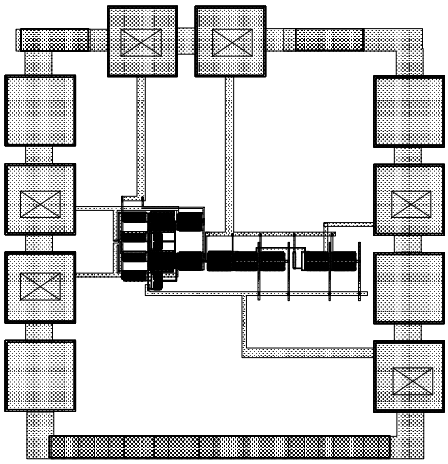


Figure 7.20: Layout of the frequency divider

The layout of the proposed frequency divider is carried out and the post-layout simulation is performed including the process corner and parasitic effects. The total power consumption increases to about 4mW. The power consumption vs. operating frequency is summarized in Figure 7.21.

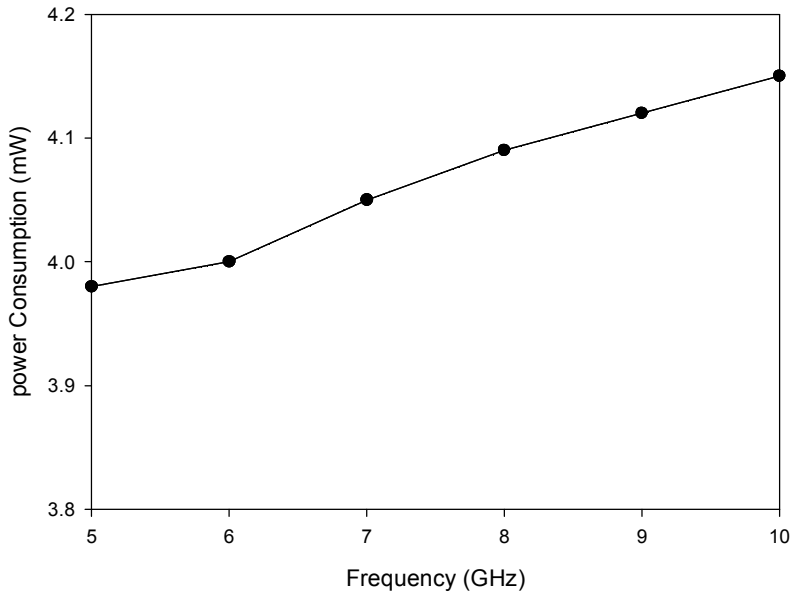


Figure 7.21: Power consumption vs. operating frequency

7.3 Conclusion

The design of a high speed PD for PLLs used in the SONET OC-192 is also investigated. A new full-rate linear phase detector for the 10 Gb/s CDR is proposed. Its circuit implementation is less stringent compared with traditional designs. By splitting the input data into the I/Q streams, the pulse width of input data is enlarged. The full-rate operation of 10 Gb/s is achieved for the 0.18 μm CMOS process. The proposed PD can operate at a supply voltage down to 1.8 V, and has a linear response over the full operating range of input phase offset of 100 ps.

A new inverter that integrates a dynamic circuit into the MCML structure to provide an enhanced output swing and a low power consumption, is proposed. It is suitable for the high speed CMOS frequency divider design. A frequency divider implemented with the proposed inverter achieves a lower power consumption and enhanced output swing in the comparison to the performance of existing designs in

the literature. Post-layout simulation shows the frequency divider implemented with this inverter using the CSM 0.18 µm CMOS process is capable of operating up to 10 GHz for a 1 V supply voltage with 4 mW power consumption.

The work of this chapter is published in [103] and [104].

Chapter 8

Conclusion

8.1 Conclusion of remarks

This thesis describes a wide range of techniques employed in the phase-locked loop. The investigation covers mainly two high frequency building blocks of the phase-locked loop, which are the VCO and the frequency divider.

In Chapter 2, the fundamentals of the PLL and frequency synthesizer have been reviewed. The basic building blocks of the PLL are introduced and the linear model of the PLL is analyzed. The role of the frequency synthesizer in the receiver and transmitter is discussed. The requirements in the design of frequency synthesizers for wireless communications are presented. A review of various VCO designs is presented. Some design considerations, particularly the design of the LC tank and the design of the amplifier, are discussed. Finally, the basic theory for the high speed frequency division is reviewed. Many digital frequency dividers, the cascaded divide-by-2 units, the prescaler and the digital counter have been presented. The two major types of logic circuits, namely the TSPC and MCML circuits are analyzed and compared. Finally the low power techniques in the high speed digital frequency dividers are discussed.

In Chapter 3, the imbalanced phase switching technique is analyzed in detail and implemented in a multi-GHz prescaler design. Different from the traditional 50% duty cycle phase switching technique, it uses $\frac{1}{4}$ duty cycle phases to increase the delay budget in the dual-modulus control. It improves the performance of the

prescaler in operating frequency and power consumption. Two prescalers, with 2-to-1 and 4-to-1 phase switching are designed using this technique. The proposed 2-to-1 phase switching divide-by-7/8 prescaler using the simplified topology and the CSM 0.18 μm CMOS process is capable of operating from 1.5 GHz to 6 GHz with a 1.8 V supply voltage and 7 mW power consumption. The prescaler with 4-to-1 phase switching can work from 2 GHz to 10 GHz with a power consumption of 15 mW for the supply voltage of 1.8 V. This chapter also describes a new dynamic divide-by-8/9 prescaler, which is based on the E-TSPC logic. By analyzing and optimizing the power consumption in the E-TSPC divide-by-2 unit, a new divide-by-2/3 unit for the prescaler design is proposed. The prescaler is silicon verified.

Chapter 4 describes a multi-GHz digital counter and the integration of 5-6 GHz wide band high resolution frequency divider implemented with the high speed low power digital counter. By using the low power high speed digital counter, with a power consumption of 5.8 mW for 1.8 GHz operation, the frequency divider is able to cover the HIPERLAN II and IEEE 802.11a standards with a high resolution and wide operating range.

Chapter 5 analyzes the phase noise in the TSPC based frequency divider, which is essential with the wide range implementation of the TSPC logic style high-speed frequency division.

In Chapter 6, a frequency synthesizer based on the new frequency divider and VCO is presented. Several design techniques including wide band high resolution frequency dividers and low phase noise wide band VCOs have been implemented in this design. A 5 GHz VCO has been designed and implemented using the CSM 0.18 μm CMOS process. Two groups of varactors are used in a wide range VCO to provide the wide operating range which is able to cover all the channels of IEEE

802.11a and HIPERLAN II. Post layout simulations show that the 5 GHz operation has been achieved with a wide tuning range and low phase noise.

In Chapter 7, a new linear full rate phase detector for SONET OC-192 is proposed. By splitting the input data into the *I/Q* streams, the pulse width of input data has been enlarged, therefore, the full-rate operation of 10 Gb/s is achieved for the 0.18 μm CMOS process. The proposed PD can operate at a supply voltage down to 1.8 V, and has a linear response over the full operating range of input phase offset of 100 ps. This chapter also describes a new 1 V divide-by-2 unit which is able to operate at 10 GHz with lower power consumption. It uses a new inverter that integrates a dynamic circuit into the MCML structure to provide an enhanced output swing and a low power consumption. The frequency divider using this inverter is capable of operating up to 10 GHz with a 1 V supply voltage and 1.3 mW power consumption in the simulation.

On-wafer measurements of the above circuits are carried out using the HP8510C Network Analyzer and Cascade Microtech Coplanar Ground-Signal Ground (GSG) probes. The HP Spectrum Analyzer 8593E with the frequency range from 9 kHz to 26.5 GHz was connected to the RF probe to examine the spectrums of the VCO output. The transient response of the frequency divider is captured by the Lecroy Wavemaster 6 GHz oscilloscope.

8.2 Future work

In some wireless communication standards, for example the GSM, CDMA 2000, the channel spacing is relatively narrow. Therefore, the fractional-N frequency divider is more suitable. The delta-sigma modulator can be used to suppress the

spur in the fractional-N divider [58]. The proposed prescalers can be used in the fractional-N divider.

In the high speed divide-by-2 unit of the phase switching prescaler, the injection-locked frequency divider in [38] can be used to achieve lower power consumption and higher operating frequency.

Another possible future work is to reduce the area of the capacitor in the loop filter design. In the layout of the frequency synthesizer, the capacitors always take a large silicon area. If the capacitance multiplexer in [58] is used, the silicon area can be reduced.

For the measurement of the phase noise in the frequency divider, a VCO can be used as the input noise source. The measured phase noise of the VCO and of the frequency divider can be used to verify the proposed noise model.

In the design for CDR applications, the proposed PD can be combined with the 10 GHz VCO [85] for the SONET OC-192 applications.

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