Investigations of the dielectric-semiconductor interface and bulk dielectric effects on charge transport in high performance organic field effect transistors on flexible substrates

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NANYANG TECHNOLOGICAL UNIVERSITY

INVESTIGATIONS OF THE DIELECTRIC – SEMICONDUCTOR INTERFACE AND BULK DIELECTRIC EFFECTS ON CHARGE TRANSPORT IN HIGH PERFORMANCE ORGANIC FIELD EFFECT TRANSISTORS ON FLEXIBLE SUBSTRATES

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A thesis submitted to the Nanyang Technological University in fulfillment of
the requirement for the degree of Doctor of Philosophy

by

Tan Huei Shuan

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2010**

ABSTRACT

Organic field-effect transistors (OFETs) exhibiting high mobilities and low-operating voltages is key for their successful realization in plastic electronics applications. It has become increasingly evident that the dielectric and dielectric-semiconductor interface is of critical importance to OFETs' device performance, influencing mobility, low voltage operation and output currents.

This thesis reports on the concept of introducing high k silica films prepared via a sol-gel (SG) methodology as potential gate dielectrics that enable high performance OFETs on plastic substrates. Compared to OFETs fabricated on thermal oxide (SiO_2) and SiN_x , an improved device characteristic is distinctively and consistently observed in OFETs fabricated on sol-gel silica dielectric. In particular, through the innovative approach of tri-layer sol-gel silica gate dielectric architecture, both Pentacene and P3HT FETs with gate bias of ≤ -5 V, demonstrated saturation mobilities of $\sim 6.55 \text{ cm}^2/\text{Vs}$, $\sim 0.5 \text{ cm}^2/\text{Vs}$ respectively with current on-off ratio of $> 10^5$ on plastic substrates. X-Ray diffraction, photoluminescence/absorption, Raman spectroscopy and near edge X-ray absorption fine studies display enhanced molecular ordering and packing through a more homogeneous and better in-phase intermolecular coupling in the pentacene organic semiconductor deposited on sol-gel silica. This phenomenon is induced by the excellent surface properties of sol-gel silica (Roughness of $< 0.3 \text{ nm}$ and low surface energy) promoting lesser structural defects at the dielectric-semiconductor interface. These studies provide consistent proof that dielectric-semiconductor interface, film morphology and structural defects are the determining factors which impact charge carrier mobility, threshold voltage and other figures of merit of OFETs.

One of the phenomenon studied using this sol-gel silica system is the effect of dielectric constant on charge carrier mobilities. By varying the duration of argon or air plasma and thus modulating the polar –OH groups in the dielectric bulk, the k of the tri-layer SG silica was tuned from ~ 7 to ~ 9 . This acts as a platform to study the effect of high bulk dielectric constant (high k) on device performance while preserving a similar dielectric surface energy and chemistry. Both Pentacene and P3HT FETs showed lower mobilities with increasing k , demonstrating that the charge transport in OFETs could be limited by the high polarizability of the gate dielectric that leads to energetic disorder at the dielectric – semiconductor interface.

In order to examine the viability of employing sol-gel silica dielectrics for large scale plastic electronic devices, the mechanical flexibility of the sol-gel silica FETs was investigated. The slight increase in the drain currents upon bending strain (2.27%) was probed using Raman spectroscopy, which revealed enhanced in-phase coupling of the C-H bending mode due to strain induced improvement in the packing of the pentacene molecules. The sol-gel silica film withstood 12500 bending cycles without any significant degradation or device performance or gate leakage current, confirming that these flexible and robust gate dielectric films that yield some of the highest reported device mobilities are suitable for plastic electronics applications.

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CHAPTER 1 INTRODUCTION

1.1 Challenges of Plastic Electronics

Since the invention of the world's first transistor in 1947, transistors made of inorganic semiconductor materials, such as silicon continue to dominate the microelectronics industry. However, in recent years, with the advent of conjugated polymers, Organic Field Effect Transistors (OFETs) have emerged as potential candidates for innovative applications such as large-area flexible-displays, low-cost radio frequency identification tags, and integrated light emitting and light harvesting devices. Although it is recognized that these devices would not displace Si microelectronics, the alternative applications that these may spawn has led to intense worldwide research efforts in this field of organic or printed electronics.[1-5].

For the realization of the aforementioned applications, OFETs with high mobility (comparable to amorphous Si) must at the same time offer low voltage operation, low temperature processing, and compatibility with plastic substrates. In general, thermally grown SiO₂ (TOX) on silicon has been widely used as a substrate for OFETs, mainly due to its superior electrical properties which make it suitable as the test-bed for new molecules. However large area electronics applications would entail organic electronics on glass or flexible foil substrates, thus making solution processed gate dielectrics a necessity [6].

Organic dielectrics or polymeric materials with their ease of large area processability can be viewed as the ideal choice; however their low dielectric constants make very high voltage (> 20 V) operations necessary. Self-assembled monolayers (SAMs) [7, 8] and self-assembled multilayers (SAMTs) [9] have been proposed as alternative dielectric materials for low voltage OFETs. However, this approach is limited

by the chemistry required for silane/phosphate coupling to the dielectric surface where the uniformity over a large area may be difficult to achieve. Thus, the use of appropriate high- k inorganic materials would afford low voltage device operation while also being insoluble to the solvent used for the organic semiconductor deposition (in the case of bottom-gate structures). The shortcomings of most high- k inorganic materials, such as Al_2O_3 , TiO_2 , Ta_2O_5 , and Si_3N_4 is the requirement for complex and expensive deposition processes, high temperature, and incompatibility with low cost, solution processed methodologies.[10] To overcome these limitation, sol-gel based high- k dielectrics have been proposed [11, 12], yet concerns over interfacial compatibility with organic semiconductors (OSCs) remain [13] while the requirement for high temperature annealing process is incompatible with plastic substrates.[12]

In parallel to the rapid development and dramatic improvement in knowledge and manipulation of molecular design [14-18]; it is increasingly evident that electrical performance (mobility [13], hysteresis [19], threshold voltage (V_{Th}) [20] as well as the operating voltage) of the OFETs is critically influenced by the chemical composition, surface functionalization, and surface morphology (roughness) of the gate dielectric [10, 13, 21, 22]. A comprehensive understanding of the interplay between gate dielectric surface properties which influence the morphology, molecular ordering of the organic semiconductor and their effect on device properties is still being developed.

Besides, the suitability of high k insulator as gate dielectric materials is highly questionable due to its processability, morphological concerns and in particular the possible influence on the distribution of electronic states in the active layer. Dimitrakopoulous *et al.* proposed that high k insulator could induce more carriers to fill the traps at lower gate bias thus ensuring higher mobility in OFETs. [12] On the other hand, Veres *et al.* proposed that low k insulator is a more suitable candidate for OFETs as high

k insulator is believed to increase the energetic disorder at the dielectric-semiconductor interface leading to lower carrier mobility.[23] Although previous reports of devices exhibiting high mobilities on both high and low k dielectric exists, none of the studies are able to isolate other factors such as surface roughness or surface energy of the dielectric layers which influence the data interpretation of the carrier mobility in OFETs.[24-26]

Hence, this thesis will focus on the two key challenges highlighted in the introduction above: (1) development of a solution processed high k dielectrics for low voltage operating OFETs with electrical and mechanical stability and (2) to gain an understanding on the effect of *surface* and *bulk* properties of the gate dielectric on the OFETs' device performance.

1.2 Research objectives and scope

To address the gaps in the literature, the main objectives of this thesis may be summarized as follows:

1.2.1 Realization of sol gel silica dielectrics for OFETs fabricated on plastic substrates

In order to meet the stringent requirements for gate dielectric of high performance OFETs such as solution processability, high k , excellent surface properties, the thesis focuses on the feasibility of using sol gel based inorganic dielectrics for fabrication of OFETs on rigid (Silicon) and flexible substrate (Polyethylene terephthalate). The thesis explores the basic issues involved in thin film formation, *surface* and *bulk* properties of sol gel based dielectrics and device architecture engineering to achieve high performance OFETs.

1.2.2 Investigate the impact of sol gel dielectrics on device performance:

A critical analysis of the various factors that influence the interactions between gate dielectric and organic semiconductors in OFETs will be evaluated in this thesis. The questions addressed concern sol gel dielectric surface and bulk properties that influence the charge transport in organic semiconductors. In order to answer these questions, oligomer semiconductor (Pentacene) was employed mainly due to its high degree of crystalline order, which allows it to be structurally characterized by using diffraction and microscopic techniques. A systematic study of the gate dielectric surface chemistry affecting the morphology and growth of pentacene was carried out to analyze their effects on OFETs characteristics.

In order to study the effect of high dielectric constant (k) of gate dielectric on charge transport, a multilayer sol gel dielectric stack with tunable dielectric constant and identical surface chemistry was designed and fabricated. The effects of charge localization induced by the polar nature of the dielectric were verified in both polycrystalline pentacene and semicrystalline P3HT. Deposition of a capping layer on the highly polar dielectric provides insights on the screening effect on the charge carrier from dipolar disorder at the dielectric semiconductor interface.

1.2.3 Investigate the contribution of dielectric induced morphological changes and inter-molecular interactions towards device performance:

Although progress has been made in understanding the factors that influence OFET performance, there are still numerous areas of critical importance for which inconsistent explanation is found in the literature. Interface traps and structural defects are generally influenced by the growth behavior of organic semiconductor on the gate dielectric which will be greatly affected by the inherent surface roughness of the substrate. Thus,

observation of microstructures and molecular order via atomic force microscopy (AFM) and X-ray diffraction (XRD) will provide insights on the morphology and structural ordering of pentacene grains, while Raman spectroscopy will be employed to explore the fundamental information related to molecular ordering and to probe semiconductor-dielectric interfacial interactions and their impact on FET performance.

1.3 Thesis organization

The thesis is organized as follows. Chapter 2 briefly introduces the various concepts in organic semiconducting devices. A brief literature review of the current gate dielectrics employed as well as the issues associated with their application in OFETs is presented followed by recent approaches to improve OFET device performance. Chapter 3 describes the various techniques employed in this thesis including optical, structural and electrical characterization as well as device fabrication. Chapter 4 details the experimental results followed by its discussion in Chapter 5. The discussion explores the surface properties of the dielectric (morphology, interface traps) as well as its bulk effects (dielectric constant). Concluding remarks are presented in Chapter 6 and recommendations for future studies in Chapter 7.

CHAPTER 2 LITERATURE REVIEW

2.1 Organic Semiconductors

Organic semiconductors have been introduced by chemists as early as the late 1940s, however important discoveries have occurred only in more recent years (ca. 1974) in polyacetylene based conjugated polymers leading to (Alan Heeger, Hideki Shirakawa, Alan MacDiarmid) the Nobel Prize in Chemistry in 2000[27]. Such polymers are regarded as an interesting class of materials possesses extensive range of properties[28, 29] that may be tuned by chemical functionalization and manipulation. Over the past decade, rapid progress has been made to control the material properties at the molecular level to impose different molecular packing during growth, add side groups that enhance properties that improve charge transport.[30, 31] Past investigations were mainly challenged by material instabilities which include environmental conditions and/or processing methods[32], and structural defects that prevented the measurement and understanding of the intrinsic properties of the organic materials.[2, 33, 34] Today, with improved understanding of the material behaviors in different conditions (such as temperature, moisture and light) and interactions during processing, such discussed instabilities have been circumvented.

Generally, organic semiconductors are classified into 2 types, polymers and small molecules. Polymeric molecules typically have high molecular weights and are relatively easy to process from solution and are present as amorphous or partially crystalline in the solid-state. Small molecules on the other hand have low molecular weights and are normally deposited by thermal evaporation. They normally consist of acenes and currently offer mobilities higher than hydrogenated amorphous silicon[35, 36].

Pentacene is the most extensively studied organic semiconductors for OFETs based on small molecules, with oligothiophenes and their derivatives being the next most important. The highest reported mobility is up to $6 \text{ cm}^2/\text{Vs}$ for the former [37] and $1 \text{ cm}^2/\text{Vs}$ for the latter[38]. Major improvements have been achieved by modification of the insulator-semiconductor interface. Most devices are grown by vapor deposition on silicon oxide. In particular, surface modification of self-assembled monolayer before organic layer deposition, with octadecyltrichlorosilane (OTS) giving good results with pentacene on silicon oxide. Besides, substrate heating and very slow deposition rate leads to better molecular organization also reported to be an effective method to enhance the device characteristics.[39]

Polythiophenes are well-known to be used as the active layer in polymeric FETs due to their higher mobility, good solubility, and easy processability. After pioneering work on spin-coated poly (3alkylthiophene) (P3AT)[40], it is now established that the performance of polymeric FETs critically depends on the chemical and structural ordering of the chains at the dielectric-polymer interface. Exposure of films to air causes polymer doping and degradation of the transistor. Regioregular polyquarterthiophenes (PQTs) have therefore been developed to ensure processability, structural regularity, and extensive π -conjugation with enhanced resistance to O_2 -doping.[14, 41] Liquid-crystalline-like thieno[3,2-b]thiophenes polymers have been shown to have highly organized morphology and large crystal domains and hence exhibit good transistor stability under static storage and operation in dry N_2 ($\mu = 0.2\text{-}0.7 \text{ cm}^2/\text{Vs}$) [42]

Table 2. 1 Summary of OFET performance of p- and n-channel semiconductors.

Ref.	Semiconductor [a]	μ (cm ² /Vs)	I_{ON}/I_{OFF}
<i>p-channel</i>			
[7, 8]	6T	0.00021-0.034	$\sim 10^4$
[43]	BS8T2	0.006	$\sim 10^6$
[7, 8]	DE6T	0.2	
[7, 8]	DFHCO-4T	0.02	$\sim 10^3$
[44]	DH-5T	~ 0.03	
[7, 8]	DH-6T	0.02-0.04	$\sim 10^3$
[45]	Et-6T	0.03-0.05	$> 10^5$
[13]	F8T2	10^{-5} - >0.02	10^2 - 10^6
[46]	Me ₂ -6T	0.02	
[47]	Me ₄ -Pentacene	0.3	10^3 - 10^5
[48]	P3BT	0.0002-0.04	
[5, 49-51]	P3HT	0.001-0.2	10^2
[11, 12, 52-60]	Pentacene	0.08-3	10^2 - 10^8
[61, 62]	Pentacene-precursor	0.01-0.89	10^5 - 10^7
[30]	Pentacene-TIPS	0.17	$\sim 10^5$
[14]	PQT-12	0.14	$\sim 10^7$
[13, 63]	PTAA	10^{-5} - >0.01	10^3 - 10^5
[42]	PTTT-14	0.6-0.7	$\sim 10^7$
[26, 64]	Rubrene	1.5-20	
[65]	TFB	~ 0.0003	$\sim 10^4$
[43]	TS6T2	0.06	$\sim 10^5$
<i>n-channel</i>			
[66-69]	C ₆₀	10^{-4} -0.5	10^2 - 10^4
[70]	C ₈₄	0.0005	$\sim 10^3$
[71]	CuPc	0.01	
[72]	DFH-6T	0.01	10^5
[44]	FCuPc	~ 0.02	
[22]	FTTTTF	0.4	10^8
[73]	T3CN	0.2	$> 10^6$

[a] 6T, sexithiophene; C₆₀, fullerene; C₈₄, solution processable fullerene-derivative; CuPc, copper phthalocyanine; DFH-6T, oligothiophenes containing or substituted with carbonyl groups; DH-4T/DH-5T/DH-6T/Et-6T/Me₂-6T, hexyl-substituted thiophenes oligomers; FCuPc, perfluorophthalocyanine; F8T2, poly(9,9-dioctylfluorene-co-bithiophene); FTTTTF, mixed perfluoroarene-thiophene oligomers; P3HT, poly(3-hexylthiophene); PTAA, polytriarylamines; P3BT, poly(3-butylthiophene); Pentacene-precursor, soluble pentacene precursor; Me₄-Pentacene, soluble pentacene with methyl groups; Pentacene-TIPS, soluble pentacene derivative; PQT, regioregular polyquaterthiophenes; TFB, poly[(9,9-dioctylfluorene-2,7-diyl)-*alt*-(phenylene-[*N*-(*p*-2-butylphenyl)iminophenylene])];

In the case of N-type organic semiconductors, the compounds showing the highest electron mobilities are currently fullerene C₆₀ [68] and *N,N*4-dialkyl-3,4,9,10-perylene tetracarboxylic diimide derivatives[74], with values up to 0.5 cm²/Vs. Because C₆₀ forms isotropic solids, the films do not require particular attention to control molecular orientation as in other organic materials. The other n-channel semiconductors are mostly based on oligothiophenes in which the molecular energy levels have been tuned by substitution with cyano, perfluoroalkyl/aryl, and alkyl/arylcarbonyl. The performance of n-channel organic transistors is notoriously inferior with respect to p-channel organic transistors and there are a few plausible explanations for this. Firstly, most conjugated aromatic cores have relatively small electron affinities so that these materials tend to transfer holes better than electrons. In such materials, the induced electrons tend to occupy trap states where they are relatively immobile. Secondly, the trapping of electrons in the presence of oxygen and moisture results in degradation of the performance of n-channel organic semiconductors very easily.

2.1.1 Organic Molecular Crystals

Organic semiconductors are characterized by their *intramolecular* bonds with the alternation of single (σ) and double (π) bonds, referred to as *conjugation*, where the hybridized sp^2 orbitals form the σ bonds and the nonhybridized p_z orbitals form the π bonds – delocalized over the molecule. The σ bonds are strong and positioned lower in energy whereas π -electrons are the main part of the intermolecular conduction in these organic semiconductors. The filled molecular orbitals (π -bonding orbitals) form the valence states where its highest energy orbital is called Highest Occupied Molecular Orbital (HOMO) while the vacant orbitals (π^* -antibonding orbitals) with its lowest

energy orbital regarded as Lowest Unoccupied Molecular Orbital (LUMO) form the conduction states.

The interplay between *dispersion* (van der Waals) forces between induced dipoles and *electrostatic* interaction between permanent multipoles (quadrupoles) determine the crystal structures [27]. The two competing interactions promote different molecular stacking to minimize the energy, resulting in the characteristic organic molecular crystals interplanar distance of $> 3.4 \text{ \AA}$. In order to maximize the π -overlap, the van der Waals interactions of the molecules are most probably adopting “face-to-face” orientation. The type and amount of π -overlap can be controlled by the nature, size, and position of the substituting group in the molecular backbone[75, 76], leading to various stacking patterns, hence polymorphism which indicates the presence of different arrangement for a given molecules but with similar lattice energies. This phenomenon has been identified to be driven by the growth conditions and/or subsequent treatment, substrate type, substrate temperature, and thickness of the film. On the contrary, the presence of quadrupolar moments have a preference of “edge-to-face” stacking (i.e. the hydrogen atom of one ring encounters the π -network of the adjacent molecule), resulting the most common crystal packing which is regarded as herringbone arrangement (Figure 2.1)

There are four polymorphs detected for Pentacene ($\text{C}_{22}\text{H}_{14}$), which is a planar molecule composed of five benzene rings (Figure 2.1). Pentacene has a triclinic structure (space group $P\bar{1}$) and a density of 1.32 g/cm^3 with two molecules per unit cell arranged in a herringbone configuration in its bulk phase. Vacuum-deposited thin films, however, form a structure that has been referred to as the “thin film phase”[77] in which the interplanar spacing ($d_{001} = 15.4 \text{ \AA}$) [77] is different from that in pentacene bulk crystals ($d_{001} = 14.5 \text{ \AA}$)[78]. For evaporated thin films with certain critical thickness, the bulk polymorph has been found to coexist with the “thin film phase”. [79]

Figure 2. 1: (a) Chemical structure of pentacene. Pentacene crystal structure in its single crystal: (b) view along the [100] axis (the layered structure can be seen) and (c) the herringbone arrangement within the layer, view along the long axis of the molecule. The unit cell orientation is also drawn (After ref. [32]).

2.1.2 Transport in Organic Semiconductors

Considering that the HOMO-LUMO gap for organic semiconductors are in the range of 1-4eV [27], they are known to have *wide-band-gap* and *small bandwidth*. Hence, organic materials are often regarded as insulators as an electron has to attain sufficient energy to be excited from the HOMO level to the LUMO level and thus contribute to conduction. To generate charge carriers in the organic semiconductors, the three common approaches are:

- (a) Injection of carriers from metallic electrodes (in the case of OFETs),
- (b) Optical excitation (creation of electron-hole pairs as in the case of photovoltaics)
- (c) Electrostatic or chemical doping (mainly for conductor materials).

In contrast to inorganic semiconductors which are characterized with strong covalent and ionic bonding, organic molecular solids are held by van der Waals and electrostatic type of weak intermolecular forces, resulting in lower bonding energies. [56]. It is important to understand that the low mobility characteristics of the organic semiconductor are a consequential effect of the interaction of charge carrier with the lattice environment, thus leading to polarization effects and charge carrier localization. Furthermore, the weak Van der Waals interactions also result in small electronic

bandwidth which represent the orbital overlap strength of the HOMOs and the LUMOs . The smaller bandwidth of polymers compared to oligomers explains the lower conduction for polymers ($\mu = 10^{-8}$ - 10^{-4} cm²/Vs) [56] than for oligomers/small molecules ($\mu = 10^{-3}$ - 10^{-1} cm²/Vs) [58]. To further elaborates, Polymers have higher disorder and are limited by hopping of charges between polymer chains, which can be depicted as self-exchange rates. The self-exchange rate is affected by : (i) the electronic coupling between adjacent molecules (transfer integral) [59][80], which needs to be maximized, and (ii) the reorganization energy (λ_{reorg}), which needs to be minimized for efficient charge transport. In the case of the embedded pentacene molecules, there is very little difference in λ_{reorg} with respect to an isolated pentacene molecule, indicating a weak dependence on intermolecular interactions [60], thus may be ignored in comparing substrate-induced intermolecular interactions.

Due to the existence of organic crystal polymorphism, the degree of co-facial configuration is particularly important as it accommodates the largest electronic splitting in the HOMO and LUMO states, resulting in higher charge carrier mobilities. Thus, a complete microscopic understanding will require the inclusion of further properties of the excitations in the consideration as intermolecular interactions. It is also essential to highlight that structural defects and chemical impurities present in the crystal lattice promote the localization of the charge carriers, either forming new states in the HOMO-LUMO gap leading to electronic traps, or scattering the charges. Hence, such defects and impurities decrease mobility [61].

Table 2. 2: Comparison of characteristic features of organic molecular and covalent crystals. (After Ref. [81])

Covalent crystal (e.g, Si-type crystal)	Organic molecular crystal
Strong covalent type of interaction (characteristic interaction energies $E_{\text{cov}} = 2\text{--}4\text{ eV}$)	Weak van der Waals of interaction (characteristic interaction energies $E_{\text{vdW}} = 10^{-3}\text{--}10^{-2}\text{ eV}$)
prominent charge carrier delocalization	charge carrier and exciton localization
Charge carriers as free holes and electrons	Charge carriers and excitons as polaron-type quiparticles
High charge carrier mobilities and large mean free path ($l \sim (100 - 1000) a_0$) at room temperature	Low charge carrier mobilities ($\mu \sim 1\text{ cm}^2/\text{Vs}$) and small mean free path ($l \sim a_0 = \text{lattice constant}$) at room temperature
Small effective mass of charge carrier $m_{\text{eff}} \leq m_e$	Large effective mass of charge carrier $m_{\text{eff}} = (10^2\text{--}10^3) m_e$
Band-type charge carrier transport	Hopping-type charge carrier transport
Excitons as Wannier-type quasiparticles	Excitons as molecular Frenkel-type quasiparticles
High melting and sublimation temperatures, high mechanical strength, low compressibility	Low melting and sublimation temperatures, low mechanical strength, high compressibility

2.2 Organic Field-Effect Transistors (OFETs)

Similar to the famous Si based MOSFET structure which is today dominating the electronics market, the organic field effect transistor (FET) is a three terminal device, which are referred to as gate (G), drain (D) and source (S, connected to ground). The gate dielectric behaves like a capacitor and the charge carriers accumulated at the organic semiconductor and dielectric interface forming the active channel are modulated by the electric field applied at the gate electrode. There are 2 main architectures used; top contact and bottom contact with bottom gated as shown in Figure 2.2. Since most organic

semiconductors are fragile materials, the deposition of organic semiconductors on top of the insulator is much easier than vice-versa, i.e. in top-gated devices.

Figure 2. 2: Various OFET device configurations (After Ref. [10])

The figures of merits in the operation of a FET are the charge carrier mobility and the on/off current ratio. The first determines the switching speed and the maximum current. This parameter can be extracted from current-voltage measurements, and would ideally be as large as possible. Typically, the magnitudes of charge carrier mobility for polycrystalline organic materials devices are in the range from 0.1-1 $\text{cm}^2/\text{V}\cdot\text{s}$ while the best single crystal organic materials achieving mobilities of $\sim 15 \text{ cm}^2/\text{V}\cdot\text{s}$ [64]. The current on/off ratio denotes the switching of the device from a non-conducting (off) state to a conducting (on) state. A low off current is desired to eliminate leakage while in the inactive state. On-Off current ratios as high as 10^6 are suitable for most applications, and can be reached by the current generation of OFETs [2].

2.2.1 Operation principle in OFETs

In stark contrast to inorganic materials, organics transport current by majority carriers, and an inversion regime does not exist. This major difference is related to the nature of charge transport in each of these semiconductors. In well-ordered inorganics (for e.g. single-crystal Si), the delocalization of electrons over equivalent sites leads to a band-type mode of transport, with charge carriers moving through a continuum of energy levels in the solid. In less-ordered organic materials, the proposed mechanism is hopping between discrete, localized states of individual molecules. The presence of impurities or inconsistencies in structure may result in ‘traps’ that modify the relative energy levels [25], and hinder the flow of charge carriers as shown in Figure 2.3. Another interesting aspect observed in the operation of OFETs is the gate voltage-dependent mobility. Such dependency is predicted by the Vissenberg’s model [64] based on the multiple trapping and release (MTR) model which is extensively used in amorphous-Si:H [65]. Briefly, as the gate voltage increases, injected charge-carriers tend to fill the traps and the subsequent injected carriers can move with microscopic mobility as trapping events becomes less efficient, resulting in improvement in charge transport. It is also worth noting that there is a gate voltage-dependent channel thickness [66] observed only at high gate bias which is contradicting to studies which show that the conducting channel is of ~ 6 monolayers thick.[82]. Besides, quantum mechanical calculations have shown that the additional charge is almost uniformly distributed over the whole entity in short conjugated molecules [67], which signify that the actual distribution of charge-carriers in the film is not continuous; Study has however suggested that the distribution tends to be a staircase, where the width of each step equals one monolayer[40].

Figure 2. 3: (a) The energy level diagram of an organic TFT at $V_G = 0$ and $V_D = 0$. (b-e) Demonstration of the principle FETs operation for the case of (b) electron accumulation, (d) transport, (c) hole accumulation, and (e) transport. (After Ref. [69])

I - V characteristics of OFETs can be adequately described by models developed for inorganic semiconductors[83, 84]. A typical plot of output characteristic (drain current I_{DS} versus drain voltage V_{DS} at various gate voltages V_{GS}) and transfer characteristic (drain current I_{DS} versus gate voltage V_{GS} at constant drain voltages V_{DS}) are shown in Figure 2.4.

Figure 2. 4: I - V curves for a FET operation. (Left) Output characteristics (I_D - V_D) for different applied gate voltage (V_G). The curves can be modeled by expression of equation

2.1 and 2.3. (right) Transfer characteristics (I_D - V_G), semilogarithmic plot (right y-axis) and plot of $\sqrt{|I_D|}$ - V_G (right y-axis).[85]

In an ideal case, the transistor channel is active only when the gate voltage (V_{GS}) value exceeds the value of the threshold voltage (V_{TH}). Below this point, the transistor is turned off, and there is no conduction between drain and source (sub-threshold region). There are two distinct regimes in the operation of the field effect transistors can be distinguished (Figure. 2.4(left)). At low V_{DS} ($V_{DS} \ll V_{GS}$), I_{DS} increases linearly with V_{DS} (linear regime) and is approximately determined from the following equation:

$$I_{DS} = \frac{WC_i\mu}{L} \left(V_{GS} - V_{Th} - \frac{V_{DS}}{2} \right) V_{DS} \quad (2.1)$$

where L is the channel length, W is the channel width, C_i is the capacitance per unit area of the insulating layer, V_{Th} is the threshold voltage, and μ is the field effect mobility, which can be calculated in the linear regime from the transconductance,

$$g_m \approx \left. \frac{\partial I_{DS}}{\partial V_{GS}} \right|_{V_{DS}=\text{const}} \approx \frac{WC_i}{L} \mu V_{DS} \quad (2.2)$$

by plotting I_{DS} versus V_{GS} at a constant low V_{DS} , with $-V_{DS} \ll -(V_{GS} - V_{TH})$, and equating the value of the slope of this plot to g_m .

For $-V_{DS} > -(V_{GS} - V_{TH})$, I_{DS} tends to saturate (saturation regime) due to the pinch-off of the accumulation layer, and is modeled by the equation

$$I_{DS} \approx \frac{WC_i\mu}{2L} (V_{GS} - V_{TH})^2 \quad (2.3)$$

In the saturation regime, μ can be calculated from the slope of the plot of $\sqrt{|I_{DS}|}$ versus V_{GS} . The calculated mobility in the saturation regime is larger than the linear regime mobility due to the gate voltage-dependent mobility as previously discussed.

2.2.2 Fabrication of OFETs

Commonly, silicon dioxide on silicon substrate is employed as the test bed for new organic molecules, where the highly doped silicon wafer acting as gate electrode, thermal oxide as the dielectric layer and lithographically patterned source and drain electrode. The organic semiconductors will be deposited at the last step of process either by casting from solution (i.e. polymers) or vapor deposition (i.e. oligomer or small molecules). From the points of view of manufacturing ease in process integration, such fabrication processes are not highlighting the potential of organic materials, for example large area and low cost processing. Besides, in order to realize complex circuit architectures and to maximize on/off ratio of organic semiconductor devices, patterning of semiconductor is required. Consequently, it is thus imperative to develop innovative methods that are simple and efficient to be used for the large scale applications and the efforts are summarized in Table 2.3:

Table 2. 3: The common printing methods to deposit and pattern the organic semiconductors [86]

Methodology	Working Principle	Remarks
Screen Printing [70]	The major elements of the devices were deposited from solutions through stainless steel mechanical masks	A simple technique where space resolution is in the range of 35-100 μm , several times larger than the critical length needed for realistic application
Micro contact printing [71]	Uses elastomeric stamps to print patterns of self-assembled monolayers (SAMs) that are then used either as resists preventing removal of pre-deposited materials, or as initiators to promote materials deposition.	High resolution printing method down to 2 μm . The technique can be extended to reel to reel fabrication by making use of cylindrical stamps.
Inkjet printing [72] [73]	Operates by electronically controlling the production of droplets of ink which when applied to the substrate form the image. Three categories of inkjet printing: i) Continuous inkjet ii) Drop on Demand Inkjet Printing iii) Bubble Jet printing	Size resolution limited to 20-50 μm due to spreading of the droplets on the substrate. Such problem could be solved by confining the spreading of the water-based ink with a repelling pattern, hydrophobic regions that define the device dimensions.

2.3 Gate Dielectric Materials: An Overview

Gate dielectric is the insulating material separating the active semiconductor from the gate electrode. The role of the gate insulator is at least as important to the performance of OFET as that of the active semiconductor. It is important to highlight that the dielectric-semiconductor interface is where the conducting channel is formed in OFETs. Studies indicate that the conduction takes place at the first few monolayers of the semiconductor next to the semiconductor-insulator interface[82], thus the device performance is limited by the quality of the interface, and only in part by the bulk properties. The quality of channel is determined by the roughness of the semiconductor-dielectric interface [73], the surface energy of the insulator which affects the molecular ordering of the semiconductor and the density of defects and impurities present in this region [24].

Besides the effect of surface morphology, the nature of the insulator has also electrical consequences. Considering the low mobilities (typically $< 1\text{cm}^2/\text{Vs}$) of organic semiconductors, achieving high capacitance to induce sufficient charge carriers for formation of active channel at lower voltage is of great importance to reduce the power requirements of these devices. Based on equation (2.4) for the charge induced on the semiconductor as a function of gate voltage,

$$Q = CV = \frac{(\epsilon_o kA)}{t} V \quad (2.4)$$

Where ϵ_o is the vacuum permittivity ($8.85 \times 10^{-12} \text{ F/m}$), A is the area, k and t is the permittivity or dielectric constant and thickness of the dielectric materials respectively. Increasing the capacitance by reducing thickness of the dielectric layer is a straight forward method. However, thinner films have higher probability of defects such as pin holes, which could offer conduction pathway via Frenkel Poole emission or hopping

conduction [87], resultant in high leakage current and low breakdown strength as high electric field are observed at a given voltage for thinner film.

Dimitrakoulous *et al.* demonstrated the first low voltage operating ($< -4\text{V}$) OFETs based on high permittivity (k) dielectric materials (Barium Zirconate Titanate) [12], and at the same time showing improvement in the carrier mobility of pentacene by using high k materials (BZT and Si_3N_4) compared to SiO_2 based devices. The multiple trapping and release model was employed to explain such observations. Briefly, the higher k insulators can induce sufficient number of carriers to fill the traps, and these carriers are generated by the field effect at much lower gate voltages, any subsequently injected carriers are free to move with the microscopic mobility associated with carriers in the delocalized band, thus accounting for the high mobilities observed at such low voltages in higher k insulator based devices. However, the suitability of high k materials as gate dielectric is still under debate due to their high temperature process requirement, morphological concerns and possible influence on the distribution of electronic states in the active layer.

In particular, Veres *et al.* have hypothesized that the high polarity associated with high k of the insulator enhances charge carrier localization in amorphous polymer semiconductor and results in lower mobility as depicted in Figure 2.5 (a). [13, 23] It was demonstrated in the study that for current-driven applications, the mobility increase will compensate for the reduced capacitance associated with the low k dielectric, yet the morphological concerns of different gate dielectric on the data interpretation of the increased charge carrier mobility was not eliminated. In accord with the argument put forward by Veres *et al.*, the adverse effects of high k gate dielectrics on carrier mobility in rubrene single crystal devices have been demonstrated. [88] Several other research groups have attempted to study the effect of dielectric constant on device performance which shown to improve the mobility. For example, Jang *et al.* have successfully demonstrated

that by varying the dielectric constant, k of poly vinyl phenol with varying degrees of crosslinking, mobility increases with higher k . However, the range of dielectric constants explored do not show the high degree of polarizability required to reflect the true effect.[24] Another report by Jung et al. has attempted to demonstrate mobility increase with higher k value by using Titania-Polystyrene composite as gate dielectric, but the effect of pentacene morphology changes were not ruled out.[25] Therefore, till date, the effect of k of insulator on device performance still lacks a proper test-bed for verification.

Figure 2. 5: (a) Carrier mobility of amorphous PTAA decreases with higher dielectric constant insulator[23] in contrast to (b) carrier mobility of pentacene increase with increasing dielectric constant. [25]

The confluence of these two important gate dielectric effects (surface and bulk effect) has stimulated new research approaches, where the selection and design of the optimal dielectric film must meet stringent requirements, namely high capacitance, low leakage and a deposition process compatible with the electrode, semiconductor and substrate. At the same time the dielectric film must be able to offer optimal surface properties for optimum molecular ordering to achieve high performance OFET devices.

The three major dielectric classes used in OFETs, that is high- k inorganic, polymers, and self-assembled small molecules, are described in detail below.

2.3.1 Inorganic Dielectric Materials

As mentioned earlier, high power consumption resulting from high operating voltages of OFETs has served as the driving force for development of inorganic dielectric materials with high dielectric constant (high- k) properties to replace the conventional SiO₂/Si substrate, to increase the FET density on integrated circuits while preserving good insulator properties [76], however, as shown in Table 2.4, the OFETs performance with this kind of gate dielectrics generally still leads to low mobility and a high degree of variability.

Table 2. 4: Summary of the inorganic dielectrics (thickness d , capacitance C_i , dielectric constant k , breakdown field E_B) and their OFET characteristics. (After Ref. [7])

Ref.	Dielectric [a]	Method [b]	d (nm)	C_i (nF/cm)	k	E_B (MV/cm)	Semicond. [c]	μ (cm ² /Vs)	I_{ON}/I_{OFF}	Year
[11, 12]	BZT	sputt.	122		17.3		Pentacene	0.32	10 ⁵	1999
	BST				16		Pentacene	0.4-0.5		
	Si ₃ N ₄				6.2		Pentacene	0.6		
[44]	Ta ₂ O ₅	anodiz.	70		23	4-5	DH-5T	~0.03		2000
[49]	Ta ₂ O ₅	e-beam	100	180	21	>1	P3HT	~0.2		2002
[53, 54]	Al ₂ O _{3+x}	sputt.	270	22	7	~3	Pentacene	0.14	10 ⁶	2003
[63]	Al ₂ O ₃	anodiz.	120	60		~8	PTAA	3x10 ⁻⁵		2003
[55]	Ta ₂ O ₅	anodiz.	86	248	24		Pentacene	0.24	10 ⁴	2003
[71]	Ta ₂ O ₅	sputt.		66			CuPc	0.01		2003
[53]	SiO _x	PECVD					Pentacene	0.2-0.4	~10 ⁸	2003
[89]	Si ₃ N ₄		300		6.4~7.1	>6	PQT-12	0.09	~10 ⁷	2007
[50]	TiO ₂	sputt.	97	373	41	~3	P3HT	5x10 ⁻³	10 ²	2004
	Al ₂ O ₃		93	79	8.4		P3HT	6x10 ⁻³	10 ²	
[51]	Al ₂ O ₃	anodiz.	~7	600-700	9-11	~8	P3HT	~10 ⁻³		2004
							Pentacene	0.06-0.1		
[26]	Ta ₂ O ₅ -air	sputt.			25		Rubrene	1.5-20		2004
[56]	Gd ₂ O ₃	IBAD	90	280	7.4		Pentacene	0.1	10 ³	2004
[60]	TiO ₂ +PαMS	anodiz.	8+10	228			Pentacene	0.8	10 ⁴	2005

[a] Abbreviations: BZT, barium zirconate titanate; BST, barium strontium titanate, PαMS, poly(α-methylstyrene)

[b] Dielectric deposition method. Abbreviations: sputt., sputtering; anodiz., anodization; PECVD, plasma-enhanced chemical vapor deposition; IBAD, ion-beam-assisted deposition

[c] Abbreviations: DH-5T, dihexylquinquethiophene; FCuPc, perfluorophthalocyanine; P3HT, poly(3-hexylthiophene); PTAA, polytriarylamines; CuPc, copper phthalocyanine.

2.3.2 Polymeric Dielectric Materials

The ability of material to be solution processed enabled it to be readily integrated with low cost processes (For e.g. spin-coating, casting, or printing at room temperature and under ambient conditions) to form a film with good characteristics is one of the key requirements in plastic electronics. Polymeric gate dielectric materials are readily suitable to fulfill these requirements with its ability for chemical structure modification, thus tailored physical properties. With this reason, polymers exhibiting a broad and complementary solubility and processability and dielectric properties (k values) can be selected for application in many electronic devices (Table 2.5) [8].

Despite its solution processability, hysteresis is the main problem observed in the higher k polymeric dielectric [22, 52]. In particular, there is the atypical behavior of a so-called hygroscopic insulator field-effect transistor (HIFET), where a hundredfold increment in I_{ON} were recorded at very low voltages (less than 1 V) under ambient atmosphere and the current modulation is depending on the relative humidity and the time of exposure [79]. The mechanism for the current modulation was attributed to the ionic processes that occur in the moisturized gate dielectric close to the semiconductor-dielectric interface.

Recently, in the effort to induce higher capacitance value in the polymeric dielectric, innovative demonstration of increased effective k value has been done via crosslinked melamine-PVP combined with high k TiO_2 nanoparticles[58], and solution-processed high k BaTiO_3 nanoparticles filled high k PVA polymer[90]. Moreover, polymeric dielectric could impose solubility issue – susceptible to attack by organic solvents that are commonly used during subsequent processing of devices. Thus, this hybrid approach could be the solution to overcome disadvantages of each inorganic and

polymeric dielectric. However, the roughness of the hybrid film is often a concern where roughness increases with increased loading of the high-k nanoparticles.

Table 2. 5: Summary of the polymeric dielectrics (thickness d , capacitance C_i , dielectric constant k , breakdown field E_B) and their OFET characteristics. (After Ref [7])

Ref.	Dielectric [a]	Method [b]	d (nm)	C_i (nF/cm)	k	E_B (MV/cm)	Semicond. [c]	μ (cm ² /Vs)	I_{ON}/I_{OFF}	Year
[38]	CYPEL	Cast		6	18.5		6T	0.034		1990
	PVA			10	7.8			0.00021		
[5]	PI	Print		20			P3HT	0.01-0.03		1997
[52]	PVP-CL	SC	260	~12	3.6	2-3	Pentacene	2.9	10 ⁵	2002
	PVP-CP		380	~2	4.0	1-2		3.0	10 ⁵	
[48]	CYPEL	SC	1200	8.85	12		P3BT	0.04		2004
	PVP		900	5.59	5			0.0002		
	PVA		500	17.8	10			0.03-0.003		
[57]	Polynorb.	SI-ROMP	~1200	~3			Pentacene	0.1-0.3	~10 ²	2004
[58]	PVP-CL	Cast	600-700		3.5-5.4		Pentacene	~0.25	~10 ³	2004
	nanoTiO ₂									
[65]	BCB	SC	50	235		>3	TFB	~0.0003	~10 ⁴	2004
[59]	CPVP-C _n	SC	~15	~300	~6	3-6	Pentacene	0.1	~10 ⁴	2005
	CPS-C _n		~15	~225	~3	3-6		0.08	~10 ⁴	

[a] Abbreviations: CYPEL, cyanoethylpullulan; PVA, polyvinylalcohol; PI, polyimide; PVP-CL, crosslinked polyvinylphenol; PVP-CP, polyvinylphenol copolymer; PVP, polyvinylphenol; Polynorb., polynorbornene; PVP-CL nanoTiO₂; PVP-crosslinked TiO₂ nanoparticles; BCB, divinyltetramethyldisiloxane-bis(benzocyclobutene); CPVP-C_n, crosslinked polyvinylphenol; CPS-C_n, crosslinked polystyrene.

[b] Dielectric deposition method. Abbreviations: Cast, casting; Print, screen-printing; SC, spin-coating; SI-ROMP, surface-initiated ring-opening metathesis polymerization.

[c] Abbreviations: 6T, sexithiophene; P3HT, poly(3-hexylthiophene); P3BT, poly(3-butylthiophene); TFB, poly[(9,9-dioctylfluorene-2,7-diyl)-*alt*-(phenylene-[*N*-(*p*-2-butylphenyl)iminophenylene)]

2.3.3 Self-Assembled Mono- and Multilayers as Dielectric Materials

The exploitation of self-assembled monolayers (SAMs) as ultrathin dielectric materials for OFETs was first explored in the attempt to lower the operating voltage while at the same time maintaining the gate-induced charge carrier density at the channel. Table

2.6 presents the various SAMs used in OFETs fabrication. Although the monolayers were demonstrated as an excellent electrical insulator which are capable to induce high density of carrier, at the same time offer leakage current densities as low as 10^{-8} A/cm² for an average field of 5.8 MV/cm, the challenge of film uniformity across a large area must be addressed prior to its deployment into useful application [10]

Table 2. 6: Summary of the polymeric self-assembled dielectrics (thickness d , capacitance C_i , dielectric constant k , breakdown field E_B) and their OFET characteristics. (After Ref. [10])

Ref.	Dielectric [a]	d (nm)	C_i [b] (nF/cm)	E_B (MV/cm)	Semicond. [c]	μ (cm ² /Vs)	I_{ON}/I_{OFF}	Year
[7, 8]	OTS	2.8	153	9-12	6T	0.00036	$\sim 10^4$	2000
	PhO-OTS	2.5	900	14	DE6T	0.2		2004
					Pentacene	1.0	$\sim 10^4$	
	SAMT-I	2.3	400 [1100]	5-6	DH-6T	0.04	$\sim 10^3$	2005
	SAMT-II	3.2	710 [2500]	6-7	DH-6T	0.02	$\sim 10^3$	
	SAMT-III	5.5	390 [760]	6-7	DH-6T	0.06	$\sim 10^3$	
					6T	0.002	$\sim 10^3$	
					DFHCO-4T	0.02	$\sim 10^3$	
					FPcCu	0.003	$\sim 10^2$	

[a] Abbreviations: OTS, octyltrichlorosilane; PhO-OTS, OTS containing an aromatic (phenoxy) end group; SAMT, self-assembled multilayer.

[b] Values in brackets were measured in MIM structures.

[c] Abbreviations: 6T, sexithiophene; DE6T, diethyl-sexithiophene; DH-6T, (α,ω -dihexylsexithiophene); DFHCO-4T, (2,7-[bis(5-perfluorohexylcarbonylthien-2-yl)]-4H-cyclopenta-[2,1- b :3,4- b']-dithiophen-4-one); FCuPc, perfluorophthalocyanine.

Self-assembled multilayers (SAMTs) [11] were introduced as more consistent dielectric materials which could achieve better device yields than SAMs. The laboratory device yields were reported to be > 95%. This approach utilizes three-dimensional (3D) crosslinked dielectric SAMTs grown from solution via self-limiting sequential deposition of siloxane building blocks, highly polarizable layers, and siloxane capping layers. Yet, the presence of the Si/SiO₂ interface underneath the SAMT layer strongly limits the

maximum charge that could be induced in the accumulation layer, resulting in underestimated C_i values. This result illustrates the critical importance of having highly π -polarizable dipolar layers in enhancing SAMT k , while preserving excellent insulator properties. This approach is, however limited by the chemistry required for silane/phosphate coupling to the substrate surface.

2.4 Sol-Gel gate dielectrics

In addition to the direct strategy of using one single material as the gate dielectric layer, several approaches with more complex/hybrid dielectric systems were studied. The work on sol-gel dielectric systems is basically driven by the motivation to prepare gate dielectric via a solution processable strategy for large area application, where the products of the sol gel process to enhance the OFETs performance or to tune the electrical characteristics in a certain way, with prioritizing the simplicity and low-cost of organic electronics.

2.4.1 Sol-Gel method for gate dielectric in OFETs

Silsesquioxane resins have been explored as the gate dielectric materials and could meet the stringent requirements for use in OFETs [91]. The low-molecular-weight precursors have the molecular formula $\text{RSiO}_{1.5}$, where R can be hydrogen or alkyl, alkenyl, alkoxy, or aryl groups. The glass resin oligomers are soluble in common organic solvents which permit the use of various conventional liquid coating techniques, compatible with non-photolithographic, low-cost microcontact printing to produce films of the required thickness by adjusting the solution concentration. The low curing temperature permits the use in plastic substrates. The cured films have high dielectric

strength, low leakage current, good hydrolytic and thermal stability along with high chemical resistance to many organic solvents.

2.4.2 Overview of sol-gel process steps

In general, the sol-gel process involves the evolution of inorganic network. Sol refers to the formation of a colloidal suspension and the subsequent gelation of the sol to form a three dimension network in a continuous phase which is known as gel. The precursor for synthesis of these colloids consists of complex of metal with various reactive ligands. The Si-O-Si can be processed via sol-gel methods and the common alkoxides used is tetramethoxysilane (TMOS) and tetraethoxysilane (TEOS).

In general, there are 3 common methods used to make sol-gel monoliths:

- (A) Gelation of colloidal powder solutions;
- (B) Hydrolysis and poly-condensation of alkoxide precursors followed by supercritical drying of gels; or
- (C) Hydrolysis and polycondensation of alkoxide precursors followed by aging and drying under ambient conditions.

Briefly, the processes involved in making sol-gel-derived silica monoliths for all the three above mentioned approaches can be summarized as follows[92]:

- (1) Colloidal powders or liquid alkoxide precursors (e.g., $\text{Si}(\text{OR})_4$, where R is alkyl) is hydrolyzed by mixing with water where hydrolysis occurs:

- (2) The hydrated silica tetrahedral interacts in a condensation reaction:

As the polycondensation reaction occurs, continual linkage of $\equiv\text{Si}-\text{OH}$ tetrahedral takes place, consequently results in a SiO_2 network. The H_2O and $\text{R}-\text{OH}$ is the by

products from the condensation reaction and remains in the pores of the network. As precursor mixed with the water, the hydrolysis and polycondensation reactions concurrently initiate at numerous sites within the precursors + H₂O mixture solution. As sufficient interconnected Si-O-Si bonds are created, they are regarded as colloidal particles or a sol. The size of the sol particles and the degree of cross-linking within the particles (i.e. density) depend sensitively upon the pH and R ratio ($R=[\text{H}_2\text{O}]/[\text{Si}(\text{OR})_4]$) among other variables.

- (3) Gradually, the colloidal particles and the condensed silica species connect together to form a three-dimensional network with time. The physical characteristics of the network are determined by the size of particles and the extent of crosslinking prior to gelation. As the viscosity of sol increases during gelation, it could result in solid object.
- (4) Aging of a gel is a process involves maintaining the cast object for a period of time, completely immersed in liquid. During aging, polycondensation continues along with localized solution and reprecipitation of the gel network, which increases the thickness of interparticle necks and decreases the porosity, indicating that the strength of the gel increases with aging. An aged gel with sufficient strength is particular important to resist cracking during drying.
- (5) Drying process basically involves removal of liquids from the interconnected pore network. Undesired capillary stresses can develop during drying especially when the pores are small(<20nm), resulting in gels cracking. There are 3 methods to prevent the occurrence of cracking;
 - (a) Control the drying process by decreasing the liquid surface energy with addition of surfactants or elimination of very small pores;
 - (b) By hypercritical evaporation which avoids the solid-liquid interface; or

- (c) By obtaining monodisperse pore sizes by controlling the rates of hydrolysis and condensation

After the removal of surface silanol (Si-OH) bonds from the pore network, a chemically stable ultra-porous solid is formed. The porous gel-silica made by method (c) described above is optically transparent with interconnected porosity and has sufficient mechanical strength.

- (6) Heating the porous gel at high temperatures induce densification to occur, eliminating the pores and increased the density of the silica film ultimately becomes equivalent to that of fused silica. To a large extent, the densification temperature depends on the dimensions of the pore network, the connectivity of the pores, and the surface area. Plasma treatment has been reported to aid in densification of the gel at room temperature.

2.5 Progress in OFETs device performance

Till date, tremendous progress has been made in OFETs. In particular, there have been many reports of elevated mobilities in pentacene based FETs as shown earlier in Table 2.1. However, to achieve sufficient low operating voltage at the same time to attain high on-off current ratio (at least $> 10^6$) with high operating speed for real integrated circuits applications, it is undoubtedly that improvements in designing new organic molecule may not be the complete solution. It is important to emphasize that OFETs are *interface* devices in which device performance are strongly associated to the dielectric layer. To further fine-tuning the current achievements in device performance, a greater depth of understanding in the influence of the dielectric layer itself and the effects of organic semiconductor-dielectric interface must be elucidated.[10], [35]

In order for the dielectrics layer to have a distinct impact in device performance, a critical breakthrough approach must achieve the desired bulk properties of dielectric layer as following:

- High capacitance to realize low voltage operation device to reduce power consumption.
- High dielectric strength to ensure long-term electrical reliability
- Low leakage current
- Insignificant hysteresis behavior
- Conformal coverage
- Good thermal and chemical stability
- Simple deposition process to be compatible to flexible substrates and at the same time offer high fabrication yields for large area application.

Next, from the scientific standpoint, a full understanding on the effects of the organic semiconductor- dielectric interface on charge transport is still not entirely understood. The following segment will thus comment on the efforts and progress in stabilize the device performance through studies on optimization of the improved molecular ordering and controlled interface between organic semiconductor and dielectric:

- In general, the efforts in optimization of the deposition of pentacene have shown promising results in OFETs, yet, there is still a huge variation in the reported mobility in the literature, infers that there is still more to learn as small processing differences can have large effects on device performance. In particular, the variation in orientation of the pentacene molecules with respect to the substrate (especially for the first monolayer) is reported to be determined by the balance between the pentacene-substrate and pentacene-pentacene interactions [87]. When pentacene is deposited onto inert and smooth substrates such as oxide or non-polar polymeric dielectrics,

pentacene molecules aligned its long axis vertically on the substrate [2]. Study has proposed that the (001) plane in pentacene crystals has the lowest surface energy [88]. Coupled with a weakly interacting substrate, the intralayer pentacene-pentacene interactions are stronger than pentacene-substrate interactions. With this reason, pentacene will be inclined to form crystals with the (001) plane parallel to the substrate plane, leaving the lowest energy surface exposed. Hence, understanding the effects of substrate's surface energy and chemistry on molecular orientation of pentacene will undoubtedly help to achieve better optimization of device performance.

- Surface treatment is another widely employed method for interfacial control to improve device performance[93]. Commonly, the conventional cleaning procedures such as wet chemistry or UV-ozone treatment on SiO₂ leave a highly water-like(hydrophilic) surface on which water adsorbs [91], which could act as electron trapping sites to limit charge carrier mobility. The role of SAMs is thus to change the wetting properties of SiO₂ to create a low surface energy (hydrophobic) surface. Study has shown that Pentacene grain sizes on SAMs are usually smaller than those observed on SiO₂ [95], attributable to the increased roughness [94] after SAMs treatment. However, from the structural point of views, pentacene deposited on silanized substrate such as octadecyltrichlorosilane (OTS) on SiO₂ recorded a lower dislocation density ($0.5 \times 10^{11} \text{ cm}^{-2}$) than pentacene on pristine SiO₂ ($0.9 \times 10^{11} \text{ cm}^{-2}$) which underwent an identical growth conditions . Hence, interfacial control is an importance aspect in optimization of device performance which depends on the quality or the surface condition of the substrate (dielectric's surface chemistry for the case of bottom contact device)
- According to the standard nucleation and growth models, it is expected that the nucleation rate increases, and thus the size of the grains decreases, with increasing

surface energy [40]. Currently, it is critical to note that the effect of grain size on OFETs performance is still controversial issue. On the basis of conventional polycrystalline theories, it is expected that mobility of the charge carrier increase with larger grain size. It has been shown theoretically that charge transport in polycrystalline medium is limited by grain boundaries which have large potential energy that impede the charge transport in the inter-grain regime, hence bigger grain size dictates lesser number of grain boundaries, leading to improved charge transport. Although similar observation has been reported earlier for oligothiophenes[97], several results attest the opposite is true for pentacene [95,98] and polythiophenes[99].

- In addition to the morphology observations, there is still much controversy regarding electronic transport in these organic molecular materials, although all of these materials have overlying similarity in their crystal structures – nearly all crystallize in a herringbone or herringbone-like structure in which molecules have consistently large overlap of their conjugated portions [57]. Possible explanations range from large π - π overlap to near band-like structure, although a true picture is still evolving. The only irrefutable conclusion at this point is that herringbone-like structure seems to be conducive to higher field-effect mobilities in organic molecular crystals [84].

In addition the direct influence of inherent chemical and physical properties of the organic semiconductor and dielectric layer in device performance as discussed above, device architectures also play a critical role in improvements of device performance. Bottom gate with top-contact OFETs normally have the highest performance, attributable to the reduced contact resistance at the source and drain electrodes, related to reduce structural disorder at that interface due to dramatic morphology changes and/or dewetting

of the semiconductor on/near the metallic source and drain electrodes [100]. Bottom gate with bottom contact architecture is easy to fabricate with the conventional lithographical patterning approach, can also be improved by control of the interface of metallic source-drain electrodes.[94] Simple SAMs on metal electrodes can alter the molecular growth, hence enhancing the crystallinity [101]. SAMs have the added advantage of being chemically bound to the surface of the electrode material, thereby minimizing contributions of smaller-molecular-weight species migrating under high-field in OFETs [84].

CHAPTER 3 EXPERIMENTAL PROCEDURES

This chapter contains a brief summary of experimental procedures for the synthesis and deposition of sol gel silica to be used as viable gate dielectric materials. In addition, the procedures to modify bulk properties of sol gel silica via plasma treatment are presented. Besides, the methodology of deposition of SiN_x at room temperature via reactive sputtering is described in detail. OFET fabrication and its electrical characterization including current-voltage (I - V) and capacitance-voltage (C - V) is also presented. Material characterization techniques including atomic force microscopy (AFM), X-ray diffraction (XRD), transmission electron microscopy (TEM) and X-ray Photoelectron Spectroscopy (XPS) were also used extensively for this project.

3.1 Low temperature processing of inorganic gate dielectric

This thesis focuses on development of inorganic gate dielectric materials which are processed at low temperature in order to be compatible to processes limited by plastic substrate. The two low temperature processed gate dielectrics materials studied in this thesis are (1) sol gel silica which is solution processable and annealed at 100° C and (2) SiN_x deposited at room temperature by using un-conventional reactive sputtering

3.1.1 Silica synthesis through sol-gel techniques and its deposition

Sol-gel (SG) silica solution was prepared by a two-step acid-base catalyst procedure by mixing tetraethylorthosilicate (TEOS, 99.9% purity), ethanol, water, and HCl in the following molar ratios: 1:10:3.5:0.003. After stirring at room temperature for 90 minutes, 150 μ l of the base catalyst (0.1 M NH₄OH) was then added into the solution. The clear

solution was aged for 72 hours under constant stirring at room temperature. The flow chart for synthesizing silica sol and its thin film deposition is shown in Figure 3.1

The solution was filtered through a 0.2 μm PTFE membrane filter prior to spin coating at 2000 rpm on the substrate to form the sol-gel silica thin film. Different sol-gel silica thicknesses were obtained by dilution of three-day (72 hours) aged solution by absolute ethanol (Aldrich). For instance, 20wt % and 10 wt% of sol gel silica in ethanol would yield $\sim 60\text{nm}$ and $\sim 20\text{nm}$ respectively after annealing at 100°C . In order to prevent film cracking, all sol-gel silica films were first dried in air with long heating ramp up time of 1 hour to reach 100°C . The slow drying (evaporation) is intended to allow sufficient stress relaxation and thus reduce the stress stored in the shrinkage of the gel. The thickness of the silica film also plays a vital role in determining the formation of a crack and pin-hole free silica film on plastic substrate. The films were further heated at 100°C , 10^{-6} mbar, before organic semiconductors film deposition.

Figure 3. 1: Flow chart of sol-gel silica synthesis and deposition

3.1.2 Reactive sputtering of SiN_x at room temperature

SiN_x was deposited at room temperature with a Radio Frequency (RF) sputtering system by using a Silicon target (99.99% purity) at a background vacuum pressure of 4×10^{-6} Torr. Argon gas flow rate of 10 sccm was admitted to the chamber first to generate the plasma for substrate and target cleaning for 10 minutes. Then, Nitrogen gas flow rate was slowly increased to 25sccm. The deposition was carried out under the base pressure of 20 mTorr, RF power of 300W and reverse power of 50W. 29nm thick of SiN_x film was obtained after 6 minutes deposition. The deposition rate of SiN_x can be controlled by the ratio of Nitrogen (N₂) to Argon (Ar) flow rate.

3.1.3 Tri stratal sol-gel silica as gate dielectric

The sol-gel silica solution was prepared by using tetraethylorthosilicate, TEOS (99.9% purity, from Aldrich), ethanol, water, and HCl in molar ratios of 1:10:3.5:0.003 as described above. After 3 days of aging, sol-gel silica was further diluted to 1, 2, 10, and 20 wt %, with ethanol, to yield spin coated film thicknesses of 7, 15, 24, and 65 nm respectively. To form the first thin sol-gel layer (7 or 24 nm), the diluted solution was spin coated on PET substrates, annealed at 80°C for 20 min, and underwent a 3 min air plasma treatment (700 V DC, 15 mA DC, 10.5 W, Plasma Cleaner PDC-32G-2, Harrick Plasma) prior to subsequent layer deposition. The central thicker layer (15 or 65nm) was formed using the same process. Upon spin coating of the third sol-gel silica layer (7 or 24nm), the tri-stratal dielectric was dried at 80°C for 20 mins on hot plate in air and further annealed at 100°C, for 2 h at 10^{-6} mbar prior to organic semiconductor deposition. Argon plasma or air plasma was employed in this study to modify the dielectric constant of the tri stratal sol-gel silica with variation of duration of treatment of 2, 3 or 4 minutes.

3.2 OFET fabrication

The fabrication techniques of OFETs are described in four sections. The first part describes the pre treatment and cleaning procedure for the plastic substrate, the second part deals with the different organic semiconductors used in this project. In the third part, different organic thin-film depositions techniques such as thermal evaporation and spin-coating, are discussed. The last part deals with metal source-drain electrode evaporation to form the top-contact. Figure 3.2 shows the OFETs structures used in this thesis.

Figure 3. 2: OFET structures with top-contact configuration.[Gate =Aluminium on Flexible substrate,PET, SiNx= 28.95nm reactive Sputtered SiNx, SG = Sol-gel silica, OSC = Organic semiconductor, Source/Drain = gold] ; Figure 3.2 (a) and (b) shows OFETs with single layer gate dielectric of SG silica and SiNx respectively, (c) and (d) OFETs with bilayer gate dielectric (SG silica as the interlayer between OSC and TOX or SiNx) and (e) OFETs with trilayer SG gate dielectric as gate dielectric where bottom and middle layer of SG silica were exposed to plasma treatment.

3.2.1 Substrate pre-treatment and cleaning

Plastic substrate preheating

100nm aluminium (Al) coated on 125 μm thick Polyethylene terephthalate (PET) flexible film was used as substrate and subjected to a thermal treatment (140°C for 15mins) to enhance dimensional and thermal stability to prevent further film deformation during the subsequent processes.

Substrate cleaning

- a. The substrate was then cleaned with isopropyl alcohol (IPA) for 10 minutes, and then rinsed with IPA and blown dry using N_2 gas.
- b. Subsequently, the substrates were subjected to plasma-cleaning for 2 minutes with the following parameters: 700 V DC, 15 mA DC, 10.5 W, Plasma Cleaner PDC-32G-2, Harrick Plasma).
- c. All substrates were immersed in Deionised-water (DI-water) for 10 minutes, rinsed with IPA and blow dried with N_2 gas.
- d. The substrates were then baked on hotplate at 65°C for 10 minutes.
- e. The cleansed substrate was then attached to glass substrate by using KaptonTM tape for easy handling and as a support for subsequent processes. Besides, the aluminium masked by kapton tape would be used as gate electrode in electrical testing.

3.2.2 Organic Semiconductors: Material and Deposition

The small molecule semiconductor pentacene (Aldrich), (Purified through vacuum sublimation to remove contaminants such as water and 6, 13-pentacenequinone) and soluble polymer semiconductor Poly-(3-hexylthiophene-2,5-diyl) (Sepiolid™ P grade from BASF), was used as received. Figure 3.3 shows the molecular structure of pentacene and P3HT respectively. Deposition of pentacene was performed in a thermal evaporation system from BOC Edwards (model Auto 306 coating system) with OLED heating source in alumina crucible. The 450 Å pentacene film was evaporated under a vacuum of $\sim 10^{-7}$ mbar; at substrate temperatures of 100°C, and deposition rates of 0.5 Å/ s. 10mg/ ml of P3HT was dissolved in dichlorobenzene and thin film of P3HT was formed by using spin coating condition of 1000rpm for 60s, followed by annealing in vacuum at 110°C for 20 minutes. Thickness of annealed P3HT was ~ 35 nm.

Figure 3. 3: Chemical structures of Pentacene and P3HT

3.2.3 Metal Evaporation

After the deposition of organic semiconductor films, gold source-drain electrodes were deposited with shadow mask to obtain top-contact geometry by using thermal evaporation under base pressure of 10^{-6} mbar. Gold electrodes are employed here to achieve good ohmic contact with the organic semiconductors. Devices with different width to length (W/L) ratio were designed in a 25mm x 25mm metal shadow mask (Figure 3.4).

Figure 3. 4 : W/L dimensions of transistors on the Metal shadow mask.

3.3 Characterization techniques

- Electrical characterization

Instrument: Desert Cryogenics probe station coupled with Keithley 4200-SCS and HP 4284 LCR meter

All electrical measurements were done in a Desert Cryogenics probe station (TTP-6) with a base pressure of 5×10^{-5} mbar. The position of each probe arm can be adjusted precisely via a three dimension (x,y,z axis) translation stage. This probe station is also equipped with a stage that can be cooled with a liquefied nitrogen or

helium. Combined with a silicon diode temperature sensor and a Lakeshore L-331 temperature controller, this system allows low temperature electrical characterization over temperatures ranging from 4.2K to 400K. The I-V and C-V characteristics were measured using a Keithley 4200-SCS semiconductor parametric analyzer and a HP 4284 LCR meter respectively. The C-V measurements were done on metal insulator metal (MIM) configuration at a frequency of 1 kHz with an AC signal of 15mV.

- **Atomic Force Microscopy (AFM)**

Instrument: DimensionTM 3100 series

Both Pentacene and P3HT films were characterized in tapping mode in air by using scan size of 1 and 5 μ m at a scan rate of 1 Hz. The internal gain and proportional gain were 0.4 and 0.6 respectively.

- **Ellipsometer**

Instrument: M-44 Ellipsometer, J.A. Woollam, Co., Inc. with WVASE 32TM Software

Both Sol gel silica and SiNx film thickness were measured by Ellipsometer by using wavelength from 450 to 950nm, at an incident angle of 60°C. The thicknesses were calculated by using a SiO₂ and Si₃N₄ on Al model.

- **Goniometer**

Instrument: Goniometer

The water contact angle was measured at room temperature of 23°C and humidity level of 65% with deionised water droplets. Contact angle goniometry (CAG) was used to evaluate the general hydrophilicity or hydrophobicity of a surface.

- **Fourier Transform Infrared Spectroscopy (FT-IR)**

Instrument: Perkin Elmer System 2000

The infrared spectra data of the sol gel silica dielectric on a bare N-type Si wafer were obtained using the spectrum v200 software. Each samples will be repeatedly scanned four times over the range of $4000 - 400 \text{ cm}^{-1}$.

- **Transmission Electron Microscopy**

**Instrument: JEOL JEM-2100F Field Emission Electron Microscope
equipped with double tilt holder, CCD and TV rate camera.**

The high resolution TEM (HRTEM) images were performed at 200kV by using a high contrast objective aperture (20um in diameter) equivalent to a point to point resolution of $1.7\text{\AA}$. The samples were prepared by a grinding a stack of epoxy glued sol gel silica coated Si wafer to a thickness of $\sim 100\text{um}$. The sample was then affixed on a Copper (Cu) grid. Next, the samples underwent dimpling to obtain thickness of $\sim 15\text{um}$ to 20um . Lastly, the sample was ion milled from both sides to electron transparent thickness regimes (20 -100nm).

- **X- ray Photoelectron Spectroscopy**

Instrument: VG ESCALAB 2201 – XL Imaging XPS

A monochromatic Al $K\alpha$ X-ray source at 1253.6eV was used. C1s, Si 2p and N1s, Au 4f levels were recorded at an electron take off angle of 90° .

- **Synchrotron X-ray Diffraction**

**Instrument: X-ray diffraction system with synchrotron X-ray at Singapore
Synchrotron Light Source (SSLS)**

Thin films of organic semiconductors were analyzed with beam line of 8.04 keV over the 2θ range of 2° to 30° .

- **Near Edge X-ray Absorption Fine Structures (NEXAFS)**

Instrument : Absorption spectrum measure system with synchrotron X-ray at Singapore Synchrotron Light Source (SSLS)

The NEXAFS measurements were performed at room temperature (RT) in total-electron yield (TEY) mode with a photon energy resolution of 0.1 eV. The linear polarization factor of synchrotron light at the SINS beam line was measured to be about 0.95.

- **Photoluminescence (PL)/Absorption/Raman Spectrum Measurement**

**Instrument: Confocal Raman microscope WITec CRM200 (PL/Raman)
Shimadzu UV-2501 PC UV-vis (absorption)**

PL, absorption, and Raman spectra were recorded in ambient conditions. Absorption spectra of organic thin-film were obtained using transmission mode set up. The sol-gel silica coated on microscope glass slide and the uncoated glass was served as the baseline. Confocal Raman microscope was used for the PL and Raman study. A double-frequency Nd:YAG excitation laser with wavelength of 532 nm was coupled into the system with single mode fiber. The power of the laser on the sample can be adjusted with linear continuous variable filter. The PL and Raman signals were collected via backscattering configuration (Olympus 100X objective lens, NA 0.95) to a TE-cooled CCD with laser spot dimension of ~500 nm.

CHAPTER 4 RESULTS

This chapter details the results of the various experiments undertaken in this thesis. Firstly, the use of solution processable sol gel silica as gate dielectric material for OFET applications was explored. Due to charge electret nature of the single sol-gel layer, a blocking layer was found to be necessary. Thus, the feasibility of room temperature deposited SiNx on aluminium gated plastics by RF reactive sputtering to be used as a blocking layer was successfully investigated. In order to realise a completely solution processable dielectric, an approach involving the deposition of tri stratal sol gel silica, amenable to plastic substrates was developed. Furthermore, the effect of plasma treatment on bulk and surface properties of sol gel silica was also studied. The mechanical testing to examine the flexibility of the devices was also carried out. Lastly, a correlation of bulk effect (such as dielectric constant) and surface effect (which determine morphology and structural disorder of the organic semiconductor) on the device performance was investigated.

4.1 Sol-gel silica thin film as gate dielectric for OFETs

4.1.1 Bulk and surface properties of sol gel silica thin film

It was found that to a large extent the superior film formation of sol-gel silica on substrates depends on its film thickness. This constraint is more stringent for sol-gel silica coated on aluminium gated PET flexible substrates than silicon substrate. It was experimentally shown that macroscopic cracks are often observed in sol-gel silica for film thickness $> 100\text{nm}$ on plastic, while this problem was not detected for sol-gel silica coated on silicon substrate. Besides, superior film smoothness and minimal pin hole

density were obtained only when the substrates underwent proper cleaning procedures to obtain a highly hydrophilic (water-like) surface which enhance the wettability of sol gel silica. High density of pin holes is undesirable as the electrical insulating properties of sol-gel silica will be affected. Table 4.1 summarizes the physical properties of spin coated thin film of sol-gel silica prepared at different thickness by dilution with ethanol.

Table 4.1: Film thickness of sol gel silica coated on different substrate (Silicon or Aluminium coated PET) under similar spin coating condition of 2000rpm and annealing temperature of 100°C with heat ramp rate of 1.7°C/min for 1 hour.

Weight% of SG silica in Ethanol	Substrate	Thickness ^a	Macroscopic cracks	Surface RMS Roughness (nm)
0	Si	356 ± 6nm	No	0.19 ± 0.02
	Al gated PET ^b		Yes	0.2 ± 0.02
50	Si	178 ± 5nm	No	0.19 ± 0.02
	Al gated PET		Yes	0.2 ± 0.05
20	Si	63 ± 2nm	No	0.2 ± 0.01
	Al gated PET		No	0.31 ± 0.04
10	Si	22 ± 2nm	No	0.20 ± 0.02
	Al gated PET		No	0.34 ± 0.03

^a Measurement was carried out with ellipsometer with 10 samples for each dilution.

^b 100nm thick Aluminium coated on 125 µm thick Polyethylene tetrathalate (PET) flexible substrate.

Figure 4. 1: Infrared absorption spectrum of 60nm and 355nm sol gel silica thin films. (Inset: Spectra to show water peak at 1630cm^{-1})

Infrared spectroscopy has been employed to analyze the chemical species in sol gel silica film of different thickness. Both spectra for sol gel silica of thickness of 60nm and 355nm show similar peak positions with the exception of the signal intensity (lower for the thinner sol gel silica film). The broad peak located in the range of $3000\text{--}4000\text{cm}^{-1}$ corresponds to the fundamental stretching vibrations of different hydroxyl groups suggesting the presence of two different forms of --OH group, (1) The physisorbed free water trapped within the ultra-porous structure and (2) the hydroxyl groups associated with the sol gel silica surface.[95] The small peak located at about 1630cm^{-1} is identified as the deformation mode of H_2O molecules trapped in the pores.[96] In the range of 400 to 1500cm^{-1} , several distinct peaks were observed at 570 , 800 and 1080cm^{-1} and were identified as the bond-rocking, the bond bending, and the bond stretching bands in the SiO_2 lattice respectively. In particular, the broad 1080cm^{-1} band with its shoulder could suggest different siloxane environment in the SiO_2 network structure of the sol-gel silica film (i.e. the siloxane could exist both as Si-O-Si for the skeletal network and as Si-OR

for the internal surface coverage[97]). The presence of Si-OH bonds in this thin film is confirmed by the distinct peak at 950cm^{-1} which is related to the stretching vibrations of silanol groups.[96]

Figure 4. 2 :TEM images of a cross sectional sample of sol-gel silica thin film on Si wafer. The right image is the enlarged view of the sol-gel silica to show existence of randomly distributed *close pores* with average pore size of 12nm. The top 30nm appears to be dense without pores.

Under TEM inspection, the cross-sectional view of sol gel silica thin film (355nm) on Si wafer shows 2 distinct features, i.e. the top approximate ~30nm of the film appears to have a dense structure and other part comprises of randomly distributed close pores structures (with average pore size of ~12nm). The dense structure is similar to those of silica networks generated via plasma treatment [98] while the porous structures is commonly observed for thin film formation by sol gel process as a result of the two step acid-base catalyzed sol gel process.[92]

Figure 4. 3 :Water contact angle measurements to reveal a hydrophobic surface of sol gel silica and AFM images to show crack free surface of sol gel silica on Silicon wafer (left) and plastic substrate (right).

As surface energy and surface roughness of the gate dielectric are the important aspects affecting the organic molecule ordering, water contact angle and AFM were done on both sol gel silica coated on silicon and plastic substrates. Low surface energy was observed for sol gel silica surface with water contact angle of $\sim 70^{\circ} \pm 5^{\circ}$ for both thin films on plastics and silicon wafer (Figure 4.3). Besides, AFM images reveal a crack free surface with negligible pin holes, attributable to slow heating rates and low temperature processing of 100°C . The surface roughness of sol gel silica thin film deposited on silicon and aluminium gated PET was measured to be $\sim 1.9\text{\AA}$ and $3.1\text{\AA}$ respectively. The slight increase in roughness could be attributed to the inherent rougher surface of plastic substrate compared to the atomically flat surface of silicon wafer.[99]

4.1.2 Device characteristics of sol gel silica dielectric based OFETs on rigid

Substrate

To evaluate the suitability of sol gel silica as gate dielectric, top contact structure OFETs based on pentacene as the active layer was fabricated on sol gel silica as shown in Figure 4.4(a). A capacitor based on metal (gold)- insulator- semiconductor (MIS) structure, measured at 1kHz, yielded $C_i = 25.1 \text{ nF/cm}^2$ indicating a dielectric constant, k for sol-gel silica thin film to be ~ 10.02 which is almost 3x that of thermal oxide ($k = 3.89$). The high k for TEOS based sol gel silica materials have been previously reported to be due to moisture trapping in pores.[100] Thus, the high k properties of the sol gel silica could be explained by the TEM images shown in figure 4.2 which reveal random distribution of nanopores in the film. This is further supported by the FTIR spectra (Figure 4.1) which detected the presence of water molecules.

The pentacene FETs fabricated on sol gel silica (355nm) operated under a gate voltage of -5V with a threshold voltage (V_{TH}), on-off ratio, sub threshold swing (s.s) of -1.76V, 10^3 and 300mV/dec respectively. The saturation mobility (μ_{sat}) of $2.08 \text{ cm}^2/\text{Vs}$ was determined from the slope of the transfer characteristics ($\sqrt{|I_{DS}|}$ versus V_{GS} for $V_{DS} \geq V_{GS}$ of -5V) based on equation [2.1]. The typical transfer characteristics are shown in Figure 4.4(a). It is interesting to note that a gate sweep-rate dependent meta-stable clockwise hysteresis was observed. With the sweeping rate decreasing from 0.125V to 0.01V/s, the hysteresis window was gradually reduced accompanied by an increase in maximum drain current (I_{on}). There are two plausible reasons which could explain the gate sweep rate dependent hysteresis behavior- (1) space charge electrets creation as the electrons from gate is injected into sol-gel silica film or (2) polarization of the dielectric (dipolar electrets).

Figure 4. 4 (Top-a) - The bottom gate (N-type highly doped Si) top contact structure of the Pentacene device with single layer SG Silica as gate dielectric. (Bottom-a) The sweep rate dependent hysteresis window in transfer characteristics of Single layer SG silica based device. (Long = 0.01V/s, Medium= 0.05V/s and Short= 0.125V/s) (Top-b) Device structure comprises of 45nm of TOX beneath of SG silica. (Bottom-b) Comparison of the transfer characteristics of devices with (red line) and without (black line) blocking layer of TOX.

To corroborate the variation in hysteresis and the change in the I_{on} with different gate sweeping rate, pentacene FETs were fabricated by using sol gel silica coated on thermal oxide (45nm) / Si substrate. The thermal oxide (TOX) was employed here to act as a blocking layer to encumber the charge injection from gate (in this case the highly doped N type Si is the bottom gate) to create space charge electrets, if any, or else FETs on the bilayer dielectric would still show the clockwise hysteresis, as TOX which is located beneath of sol gel silica would not interact the polarization field caused by sol gel silica onto the active layer. As evident from Figure 4.4(b), the hysteresis behavior diminished and a lower off current was detected for bi-layer dielectrics FETs. Hence, the

introduction of blocking layer below the sol gel silica confirmed that the clockwise hysteresis was a consequence of charge storage in bulk sol gel silica due to charge injection from gate bias. The lower mobility value for bilayer FETs ($0.98 \text{ cm}^2/\text{Vs}$) compared to single layer FETs ($2.08 \text{ cm}^2/\text{Vs}$) could be attributed to the lower effective capacitance per unit area. ($C_{i, \text{ TOX+ Sol Gel Silica}} = 17.1 \text{ nF/cm}^2$ while $C_{i, \text{ sol gel silica}} = 25.1 \text{ nF/cm}^2$) due to the absence of space charge electret field and a thicker dielectric film. Besides, the capacitance of the single layer SG silica might be *underestimated* since the presence of space charge electrets may create extra electric field on the active channel, thus leading to overestimation in the carrier mobility calculation, similar effects were observed in highly polar organic polymer such as CYMM and PVA. [13]

On comparing the electrical performance of devices with sol gel silica as gate dielectric to the control device which uses 45nm TOX, the former device shows a notable improvement in charge carrier mobility, sub-threshold swings and threshold voltages (Figure 4.5). A summary of device characteristics of a single layer sol gel silica and TOX with and without sol gel silica is presented in Table 4.2.

Table 4. 2: Summary of electrical performance of Pentacene FETs on TOX, sol gel Silica and sol gel silica + TOX.

Dielectric	μ_{sat} ($\text{cm}^2/\text{V s}$)	V_{th} (V)	S.S (mV/decade)	$I_{\text{ON}}/I_{\text{OFF}}$	C_i (nF/cm^2)	Effective k
TOX (45nm)	0.11	-6.13	400	1.21×10^7	76.7	3.89
Sol-gel (355 nm)	2.08	-1.76	300	1.00×10^3	25.1	10.06
SiO ₂ (45nm)+ Sol-gel (342nm)	0.95	-3.63	289	4.07×10^6	17.1	7.5

Figure 4. 5 :(a) Output characteristics (I_{DS} Vs V_{DS}) curves obtained from pentacene based FETs with (a) 45nm thermally grown SiO_2 (TOX) unilayer film (control device) , (b) SG silica and 45nm (TOX) bilayer film.

4.2 OFETs with sol gel silica dielectric based on flexible substrates

The previous section has established that low temperature and solution processed sol gel silica is a high k gate dielectric which yields high performance pentacene FETs at low operating voltage. To fabricate OFETs on plastics substrate with sol-gel silica, however, there are two process requirements. Firstly, as mentioned in section 4.1, sol-gel silica is susceptible to cracks upon thermal annealing due to the mismatch of the coefficient of thermal expansion (CTE) with the plastics substrate. It is experimental observed that sol-gel silica with film thickness $> 100\text{nm}$ suffer severe cracking issue. To solve this problem, dilute sol gel silica (10wt% or 20wt% of sol-gel silica in ethanol) is employed on plastic substrates to yield a uniform films with minimum pin hole defect

density at thickness ranging from 20nm to 60 ± 5 nm thick sol-gel silica with an average surface roughness RMS value of 3.1 ± 0.5 Å. Secondly, a low temperature processed blocking layer beneath the sol gel silica film must at the same time amenable to plastic substrate processing temperature is mandatory to suppress the unfavorable hysteresis effect due to space charge electrets creation as described earlier. For this reason, two approaches were proposed to realize the fabrication of OFETs with sol-gel silica on plastics, i.e. (1) a room temperature deposition of SiN_x via Radio Frequency (RF) reactive sputtering is examined and (2) a tri-stratal sol-gel silica architecture approach coupled with plasma treatment to induce densification in thin SG silica films to act as a blocking layer.

4.2.1 A bilayer dielectric approach: Sol gel silica and reactive sputtered SiN_x

Measurement of Metal-insulator-metal (MIM) capacitor structures at 1 kHz with AC signal level of 15mV of the reactive sputtered uni-layer SiN_x (28.95 ± 2 nm) yielded a C_i and k values of 70.8 nF/cm^2 and 2.316 respectively. On the other hand, the bi-layer gate dielectric comprising a 28.95nm SiN_x and 65nm sol-gel silica dielectric yielded effective C_i and effective k values of 48.53 nF/cm^2 and 5.15 respectively. Besides, a significant reduction in gate leakage current density (inset of Figure 4.6) was observed in the bilayer dielectric configuration which is readily attributed to the increase of effective film thickness. According to equation of capacitor in series [4.1]

$$\frac{1}{C_{\text{tot}}} \equiv \frac{1}{C_{\text{SG}}} + \frac{1}{C_{\text{SiN}_x}} \quad (4.1)$$

where C_{tot} is the overall capacitance value measured for bilayer gate dielectric, C_{SG} and C_{SiN_x} represents the capacitance of single layer sol gel silica and SiN_x respectively, the k

for 65 ± 5 nm sol-gel silica could be calculated and show a value of ~ 11 , which is consistent with the 355 nm sol-gel silica high k value and thus helps to improve the overall effective k of the bilayer gate dielectric.

Figure 4. 6: Capacitance-voltage measurement based on Metal-insulator- Metal (MIM) structure of the uni-layer (SiNx) and bi-layer (SiNx+ SG silica) was measured at 1kHz at a signal level of 15mV. The inset shows the leakage current measurement through the (dashed line) uni-layer SiNx.

X-ray photo electron spectroscopy (XPS) was used to study a possible link between the SiNx stoichiometry and the relatively low dielectric constants of the SiNx films employed in this study. The mean atomic ratio n_N/n_{Si} , determined from the corresponding N 1s and Si 2p core-level (Figure 4.7) from the 28.95 nm SiNx was found to be 0.26, which implies a low concentration of N 1s as compared to Si 2p in this film. Although XPS is generally not used for stoichiometric determination of thin films, the SiNx film thickness is merely double that of the penetration depth of the XPS thus providing an approximate indication of the relatively low amount of atomic concentration of [N 1s] compared to [Si 2p]. Therefore in this study, although the XPS does not account

for bulk properties but supports the quantitative analysis of the SiN_x film. Furthermore, it is known that reactive sputtering of silicon cathode in the N₂ glow discharge is not a conventional method to form a stoichiometric Si₃N₄ film as argon and nitrogen gas mixture often resulted in excess Si incorporation in the deposited nitride films.[101]. However, even though the SiN_x film deposited by reactive sputtering by using the current parameter has low k properties, the room temperature processing methodology is especially attractive for plastic substrates. The dielectric constant of the reactive sputtered SiN_x may be modulated by varying the RF power density or by controlling the ratio of flow rate of argon to nitrogen [102], but is not presented here as it is beyond the scope of this thesis.

Figure 4. 7 : XPS spectrum of 29nm SiN_x (a) N 1s narrow scan spectra, and (b) Si 2p narrow scan spectra. XPS in this study does not account for bulk properties of the SiN_x but support in quantitative analysis of the present of atomic concentration of N1s Si 2p

Both pentacene FETs on unilayer SiN_x and bilayer SiN_x + sol-gel silica exhibited typical linear and saturation device characteristics at operating voltage up to -5V as shown in Figure 4.8 (b). The saturation carrier mobility and threshold voltages were extracted from the saturation region based on equation 2.3. The pentacene device on unilayer SiN_x recorded a μ_{sat} , threshold voltage, sub threshold swing and on-off ratio of $9.5 \times 10^{-2} \text{ cm}^2/\text{Vs}$, -1.25V, 581mV/dec and 10^3 respectively, whereas devices with bi-layer

gate dielectrics (sol-gel silica + SiNx) displayed an order of magnitude improvement in saturation mobility to record an impressive value of $0.95\text{cm}^2/\text{Vs}$ with drain current modulation of more than 10^5 as shown in Figure 4.8(d). Compared to devices on SiNx which has capacitance per unit area of $70.8\text{nF}/\text{cm}^2$, the bilayer gate dielectric devices has smaller effective capacitance value ($45.3\text{nF}/\text{cm}^2$) due to overall thicker films. Despite of lower capacitance, a lower threshold voltage (-1.15V) and smaller sub-threshold swing($355\text{mV}/\text{dec}$) was recorded in the bilayer dielectric FETs. Besides, the bilayer FETs display only insignificant hysteresis upon multiple forward and reverse gate-voltage sweeps, which could imply that SiNx has effectively safeguarded the charge injection from aluminium gate into the sol-gel silica. Thus, the insignificant hysteretic transfers characteristics of the bi-layer gate dielectric devices, coupled with improvement in threshold voltages and sub-threshold swings, despite the lower capacitance value of the bi-layer gate dielectric indicates a better pentacene- sol-gel silica interface(negligible impurities and trap sites) than the pentacene-SiNx. The electrical performance of these transistors is comparable to the previous section which described pentacene devices on sol-gel silica and TOX as bilayer gate dielectric. These observations strongly suggest that improved charge carrier mobilities are not caused by the bulk capacitance effect but indicate that it is clearly a semiconductor- dielectric interface phenomenon since similar enhancement in charge carrier mobility is observed even with different thickness of sol gel silica film.

Figure 4. 8: (a) Schematic of top contact pentacene with unilayer SiNx dielectric and bilayer dielectric comprising of SiNx + sol-gel silica. (c) The photograph of the devices on plastic substrate. (b) And (d) Output and transfer characteristics of device based on unilayer SiNx (dashed line) and bilayer SiNx + sol-gel silica (solid line).

4.2.2 A tri-stratal sol gel silica approach

Since the applicability of sol-gel silica as an effective gate dielectric to yield high performance and low voltage operating OFETs on plastics have been demonstrated in the previous section, the effort to realize an all solution processable methodology to process gate dielectric for large area application was pursued in this section. A tri-stratal architecture of sol gel silica comprising a thin-thick-thin configuration was proposed in this study as shown in Figure 4.9. To form the first thin sol gel silica, the diluted solution (10wt% sol-gel silica in ethanol) was spun coated on aluminium gated PET substrate and was subjected to 180 seconds of air plasma [98] prior to subsequent layer deposition. The

plasma treatment yielded a dense silica layer as verified by TEM images (Figure 4.7), enabling this layer to act as a blocking layer preventing charge injection from gate. The central thicker layer was formed by using the same process and also yielded a dense surface layer which seals the moisture rich nano pores to impart high k . Finally thin sol-gel silica ($\sim 10\text{nm}$) was spun coated to serve as a surface modification layer to provide an optimal surface for the organic semiconductors deposited on top of this dielectric stack. It is important to highlight that the final top layer was not subjected to plasma treatment in order to preserve the hydrophobic nature of the sol gel silica film, as the atmospheric air plasma treatment is known to be effective in removing organic species from the surface.[103]

Figure 4. 9 :Device structure with tri-stratal sol-gel silica as gate dielectric and TEM image of cross-sectional view of tri stratal sol-gel silica on Si substrate.

By using the tri-stratal sol-gel silica processing methodology, two different thickness tri-layer sol-gel silica stacks were prepared for fabrication of capacitor and OFETs as shown in the inset of Figure 4.10(a). The capacitance measurements from MIM structure at 1kHz recorded $74.3\text{nF}/\text{cm}^2$ for the tri -layer 113nm sol-gel stacks and the dielectric constant was calculated to be ~ 10 , whereas the thinner tri- layer stacks (29nm)

recorded a higher capacitance value (303nF/cm^2) due to its thinner resultant film thickness but the k was calculated to be ~ 9.8 . The leakage current density measurement reveals that the 29nm tri-layer sol-gel silica stacks suffers higher gate leakage current as a consequence of reduce thickness as shown in Figure 4.10(b).

Figure 4. 10 : (a)Plots of capacitance- voltage at 1kHz and (b) the leakage current density of 113nm (black solid line) and 29nm (red dotted line) tri layer sol-gel silica stacks.

The pentacene FETs fabricated on tri-stratal sol-gel silica (113nm or 29nm) operate under a gate voltage of -3V , displayed no sign of hysteresis behavior in the transfer characteristics as shown in Figure 4.11 (a) (Red line), signifying that 3 minutes air plasma treatment on the first layer of thin sol-gel silica is able to promote densification of the thin silica film (~ 7 or 10nm) which could act as an effective blocking layer to the creation of space charge electrets. Besides, pentacene devices on 113nm tri-stratal sol-gel silica recorded a threshold voltage, sub-threshold swing and on - off current ratio of -0.83V , 260mV/dec and $\sim 10^5 - 10^6$ respectively. In particular, a near zero volt gate bias turn on voltage was observed, implying minimal presence of hole traps or dopants at the pentacene- sol-gel silica interface. A saturation charge carrier mobility, μ_{sat} of $3.42\text{cm}^2/\text{Vs}$ was determined from the slope of transfer characteristics ($\sqrt{I_{\text{DS}}}$ Vs V_{GS} for

$V_{DS} \geq V_{GS}$), while an effective linear mobility, μ_{eff} of $1.62 \text{ cm}^2/\text{Vs}$ was derived from its transconductance in the linear regime at $V_{DS} \leq V_{GS}$. For the pentacene FETs on 29nm trilayer sol-gel stacks, a minor increments in drain currents compared to the reference 113nm tri layer sol-gel (3minutes air plasma treatment) stack was observed as evidenced from Figure 4.11(b) (red curve) ascribed to its higher capacitance ($303 \text{ nF}/\text{cm}^2$). However, the μ_{sat} and the channel conductance (g_d) were not affected by the tri-stratal sol-gel silica thickness (113nm *Vs* 29nm), displaying only small variations in values of $3.42 \text{ cm}^2/\text{Vs}$ to $3.5 \text{ cm}^2/\text{Vs}$ and ~ 1.5 to $2 \mu\text{S}$ at V_{GS} of -3V (Figure 4.11(c)). It is important to highlight that these values are perhaps amongst the highest mobilities reported for pentacene devices fabricated on plastic substrates.

Figure 4. 11: (a),(b) Transfer characteristics of 113nm and 29nm tri-stratal sol-gel silica stack pentacene device measured in vacuum and air. (c) Plots of conductance (g_d) and μ_{eff} (inset, derived from transconductance) at operating voltages of -3V . (d) Transfer characteristics of 113nm sol-gel silica stack device measured in vacuum and ambient (Inset) shows the ATR- FTIR spectrum of the 24nm sol-gel silica with detection of Si-OH species.

To further evaluate the effect of the tri stratal sol-gel silica gate dielectric on device performance, both 113 and 29 nm thick SG stacks were also tested in air environments (humidity level $\sim 65\%$). For the 113 nm tri stratal sol-gel silica, one order of magnitude higher off current (At $V_{GS} = 0V$, $I_{off,ambient} = 3.19$ nA compared to $I_{off,Vacuum} = 0.21$ nA) was detected resulting in a reduced on-off ratio of 10^3 (at $V_G = -3.0$ V), accompanied by a more prominent clockwise hysteresis (Figure 4.11(a)- blue line). These effects may be readily attributed to the creation of space charge electrets in the SG silica, where moisture in the ambient may lead to an *increased* formation of Si-OH groups under the influence of an electric field. Similar reports of electrets have been reported in the literature.[104] The origin of these observations is most probably related to the incomplete densification of the bottom sol-gel silica layer (24 nm) by using a 3 minutes air plasma treatment. This was further confirmed by the ATR- FTIR spectra as shown as the inset in Figure 4.11 (d) which detected the presence of Si-OH species in 24 nm SG silica films. In contrast, the 29 nm tri stratal sol-gel silica maintained the hysteresis-free transfer characteristics (Figure 4.11(c)), however, the off-current severely degrades, associated with an increase in leakage current by 2 orders of magnitude. However, it is worth noting that the tri-layer SG dielectric enables gate modulation, albeit with a reduced on-off ratio of 10^3 , without any significant degradation of mobilities , $\mu_{sat,air} = \sim 2.99 \text{ cm}^2/\text{Vs}$.

4.3 Tuning of dielectric constant of tri-stratal sol gel silica stacks via plasma treatment

To further exploit the potential of tri-stratal sol-gel silica stacks which have been demonstrated to shown excellent OFET performance (i.e. high charge carrier mobility of $3.5\text{cm}^2/\text{Vs}$ for PET substrate based pentacene FET at gate bias of -3V), the effect of different plasma treatment (air or argon) and variation in treatment duration on bulk properties of tri stratal sol-gel silica were explored. Using similar processing methods as described in the section 4.2.2, tri stratal sol-gel silica stacks samples were prepared with air or Argon plasma treatment for durations of 2, 3, and 4 minutes for the bottom and central layer.

4.3.1 The investigation of plasma treatment and duration on bulk properties of tri stratal sol-gel silica

The variation in the bulk properties of the tri-stratal sol-gel silica upon changing the plasma duration and atmosphere for the bottom two layers were studied by preparing Metal –Insulator-Metal capacitor structures as shown in Figure 4.12(a). The experimental data reveals that the capacitance increases with longer duration of air plasma while it decreases with increasing duration of Ar plasma treatment. Besides, the thickness of sol-gel silica reduces with longer air plasma treatment (from 2 minutes to 4 minutes) but no significant thickness variation was found in samples treated with Ar plasma.

Figure 4. 12 : (a) Schematic representation of capacitor (Metal-insulator-metal) with tri-stratal sol-gel silica.(b)plots of leakage current density of tri-stratal sol-gel silica with different plasma treatment. [(c) and (d)] Variation in thickness and dielectric constant of tri-stratal sol-gel silica stack subjected to different duration of argon (Ar) and air plasma respectively

Based on the capacitance and thickness of the tri stratal sol-gel silica film which underwent different duration of air or Ar plasma, the dielectric constant, k was calculated based on equation (2.4). It is interesting to note that increasing the air plasma duration from 2 to 4 minutes increases the k of the tri-stratal sol-gel silica from 8.92 to 9.95, while a downward trend (9.86–7.93) was visible in samples with increasing Ar plasma treatment (Figure 4.12(d)). Furthermore, no significant variation in leakage current density was observed for the tri-stratal sol-gel films with different plasma treatments as evidenced in Figure 4.12 (b).

4.3.2 Device characteristics of OFETs on tri stratal sol-gel silica with different dielectric constant

Pentacene FETs were fabricated on tri-stratal sol-gel silica with different effective dielectric constants. The transfer characteristics as evidenced in Figure 4.14. (c) and (d) show all devices modulate the drain current from off state to on state of $> 10^5$ at gate bias of merely -3V. Interestingly, dielectric constant dependent carrier mobility was detected in these pentacene FETs. The highest saturation mobility (μ_{sat}) obtained was $6.3\text{cm}^2/\text{Vs}$ for pentacene FETs on 4 minutes Ar plasma treated tri-stratal sol-gel silica (Figure 4.13(a) and (b)), which has the lowest calculated effective k of 7.98. This is the highest mobility value reported for pentacene devices on flexible substrate till date. Among all, the lowest μ_{sat} of $1.8\text{cm}^2/\text{Vs}$ was obtained on 4 minutes air plasma treated tri-stratal sol-gel which has the highest k value of 9.87. As summarized in Figure. 4.14(e), the μ_{sat} of pentacene devices is lower when k of the tri-stratal sol-gel silica is higher.

In order to illustrate the universal nature of the high k gate dielectric effect on carrier mobility, solution processed semi-crystalline P3HT FETs were fabricated whose results are in agreement with the previous discussion. As evident from Figure 4.14(f) and (g), high performance P3HT FETs were obtained in which gate biasing of -5V can be used to modulate I_{DS} over four orders of magnitude. A μ_{sat} of $0.43\text{cm}^2/\text{Vs}$ was achieved by P3HT FETs on tri-stratal sol-gel silica treated with 4 minutes Ar plasma(Figure 4.13(c) and (d)). This is again one of the highest μ_{sat} in P3HT FETs reported on a plastic substrate. The mobility of P3HT is known to depend to a large extent on the degree of head to tail regioregularity and deposition conditions[105]. It is believed that the low surface energy on the smooth sol gel silica surface can promote better crystallinity of P3HT resulting in high mobility (similar effect has been shown in PQT-12).[31] Akin to

the observations on polycrystalline pentacene FETs, a reduction of charge carrier mobility in P3HT devices with increasing k was observed as illustrated in Figure 4.14(h). Negligible hysteresis windows and comparable subthreshold swings imply negligible disparity in the interfacial chemistry once more indicating that the discrepancy in carrier mobility can only be affected by the different high k values of the dielectric stack. (Figure 4.14(e) and (h))

Figure 4. 13: The output and transfer characteristics of the Pentacene and P3HT FETs on tri stratal sol-gel silica underwent 4 minutes Ar Plasma treatment, demonstrating high carrier mobility with low operating voltage ($< 5V$).

Figure 4. 14: (a) and (b) Device test structure of pentacene and P3HT FETs on tri stratal sol-gel silica stacks (c),(d) and (f),(g) Similar V_{on} and hysteresis behaviour was observed in transfer characteristics of Pentacene and P3HT FETs on tri stratal sol-gel silica underwent Air or Argon plasma treatment respectively. (e) And (h) Plots of carrier mobility and k value to show both pentacene and P3HT FETs show lower mobility with increasing k .

4.4 Mechanical bending experiment on sol gel silica based FETs on plastics substrate

One of the important requirements for building organic field effect transistor on plastic substrate is bendability. In order to demonstrate the robustness of the devices built on plastic substrate, bending test on the devices by placing the devices on a curved holder with bending radius of 24mm was carried out. The tensile strain was calculated to be 2.27% based on rigorous strain (S) [106] as described in equation 4.2

$$S = \frac{d_f + d_s}{2R} \left(\frac{1 + 2\eta + \chi\eta^2}{(1 + \eta)(1 + \chi\eta)} \right) \quad (4.2)$$

where R represents the bending radius, d_f the thickness of the gate dielectric layer, d_s the thickness of the base film layer (substrate), $\eta = d_f/d_s$, $\chi = Y_f/Y_s$, and Y_f and Y_s are Young's modulus of the gate dielectric layer and substrate, respectively. Here, we can estimate that η is almost 0 because d_f and d_s are 105nm and 125 μ m, respectively. From the structural parameters of present devices, this equation relating strain to bending radius can be approximated by $d_s/2R$. During the bending test, the devices are subjected to tensile stress in the direction perpendicular to the channel length as no significant changes in the effect on the direction of strain versus direction of current flow has been earlier reported by T. Someya *et al.* [106] Therefore, the electrical characterization (before, during, and after bending) was carried out for the same device (113 nm tri stratel sol-gel silica), in ambient environment as shown in Figure 4.15(a). The gate leakage of the devices remained unchanged, however, an increase in I_{DS} was observed for the devices ($W/L = 500 / 150$) subjected to bending stress. The saturation mobilities (μ_{sat} , $V_D = -3.0$ V) before, during, and after bending were calculated to be 1.98, 2.35 and 2.48 cm^2/Vs respectively. This behavior was observed on a total of four samples and no degradation in device characteristics was detected.

Figure 4. 15: Schematic diagram of the bending test. (b) Transfer characteristics of the Pentacene FETs with 113nm of tri stratal sol-gel silica measured before, during and after bending.

4.5 Molecular Ordering Investigations on Pentacene Deposited on TOX, SiNx and Sol-Gel Silica

The correlation between the dielectric-semiconductor interfacial morphology & surface chemistry, bulk molecular order of organic semiconductor, and electronic transport are yet to be elucidated as mentioned in section 2.5. In this section, atomic force microscopy (AFM) is employed to study the morphological changes of pentacene deposited on various substrates which have different surface chemistry, roughness and surface energy. Besides, materials characterization techniques such as X-ray Diffraction, Near Edge X-ray absorption fine structure (NEXAFS), Raman spectroscopy and photoluminescence are used to systematically study the crystallinity, molecular ordering, and structural disorder of the pentacene deposited on sol-gel silica in contrast to that on p thermally grown SiO₂ (TOX).

4.5.1 Atomic Force Microscopy Study

It has been reported that the growth behavior of pentacene molecule is greatly dependent on deposition temperature and is also sensitive to the surface properties of the substrate.[107, 108] In this study, the pentacene molecule was deposited at a controlled substrate temperature of 100°C on various substrates with different surface properties as mentioned earlier in section 4.1 to 4.3. I.e. TOX/Si, sol-gel silica/TOX/Si, SiNx/ Al gated PET and SG/SiNx/ Al gated PET.

The morphology of the pentacene on TOX/Si substrate has a regular small granular grain size in the range of $\sim 0.5 \mu\text{m}$ with formation of only few smaller and uneven terraces (Figure 4.16(a)), while the morphology of pentacene on sol-gel silica/TOX/Si substrate exhibits a larger granular grain size of $\sim 2.5 \mu\text{m}$ (Figure 4.16 (b)). The pentacene on SiNx/Al PET substrate shows irregular grain with size ranging from 0.2 μm to 0.5 μm . (Figure 4.16 (d)) For the pentacene on sol-gel silica/ SiNx/ Aluminium PET substrate, the pentacene grains also exhibited a well-defined terraced-structure, but unlike the big granular structure shown in the case of pentacene on sol gel silica/TOX, the pentacene molecule is dendritic in structure with a series of 12-14 terraces (Figure 4.16 (c) and (f)). Both pentacene molecule on sol-gel silica /TOX/Si or sol-gel silica/SiNx/Al PET substrate shows consistent terrace height and it was determined to be about 16 Å and 15.5 Å respectively (Figures (c-1) and (f-1)), which is close to the length of the pentacene molecule (16.01 Å), suggesting that the long axis of the pentacene molecule was inclined by about $\sim 20^\circ$ from the normal to the substrate.

Figure 4. 16: Morphology of pentacene film on (a) TOX/Si and (b) sol-gel silica/TOX/Si thin-film. (c) High resolution AFM images of pentacene on sol-gel silica along with (c-1) its surface profile indicating the terrace height (~1.6 nm) and the pentacene molecule orientation relative to the substrate (~20°). (d) SiNx/Al PET substrate (e) sol-gel silica/SiNx/Al PET and (f) High resolution AFM image of Pentacene on sol-gel silica/SiNx/Al PET (f-1) its surface profile indicating the terrace height (~1.55 nm)

4.5.2 X-ray Diffraction Study

The X-ray synchrotron source (S-XRD) patterns for 500 Å thick pentacene layers (Figure 4.17), exhibit a series of (00*l*) lines, indicating a highly textured material with peaks corresponding to the thin film phases of pentacene with interplanar spacing of 15.5 Å, in agreement with the terrace step height as observed from its AFM image (Section 4.5.1). The mean crystalline domain size perpendicular to the plane (*hkl*) ($\bar{L}_{hkl}$), the degree of structural disorder (g_{11}), and the average number of reflecting planes ($\bar{N}$) can be calculated from the half width of the diffraction peaks, according to the α^* law or paracrystal theory [109, 110], from the following expression:

$$(\delta s)_0^2 = (\delta s)_c^2 + (\delta s)_{11}^2 = \frac{1}{\bar{L}_{hkl}^2} + \frac{\pi^4 g_{11}^4 m^4}{\bar{d}_{hkl}^2} \quad [12] \quad (4.3)$$

where $(\delta s)_0 = 2 \cos \theta \delta \theta / \lambda$ is the overall broadening, excluding instrumental broadening, θ is the diffraction angle, $\delta \theta$ is in radians, λ is the X-ray wavelength, $(\delta s)_c$ indicates the broadening associated with the crystalline domain size, $(\delta s)_{II}$ measures the broadening associated with the second kind of crystal structure distortions, m is the diffraction order, and $\bar{d}_{hkl}^2$ is the mean spacing between (hkl) planes. Furthermore, for a wide range of partially ordered materials, $\sqrt{\bar{N}} g_{II}$ value is about 0.15 ± 0.05 [111], where $\bar{N}$ is the average number of reflecting planes of the crystal in the film. The $\bar{L}_{hkl}$ were calculated to be 519 Å and 595 Å, while the g_{II} were determined to be 1.85 % and 1.40 % for pentacene film on TOX and sol-gel dielectric respectively. Since the instrumental broadening was not subtracted from the width of S-XRD peak, hence the calculated crystallite size represents the lower bound [77]. Number of reflecting planes $\bar{N}$ was estimated to be 66 and 115 ML (monolayers) on TOX and sol-gel dielectric.

Figure 4. 17: Synchrotron X-ray diffraction patterns of pentacene films on TOX and sol-gel silica. Inset: Calculations on crystalline size, structural disorder (g_{II}), and number of reflecting planes (N) based on paracrystal theory.

4.5.3 Near Edge X-ray Absorption Fine Structure Spectroscopy (NEXAFs)

NEXAFS is a versatile synchrotron-based spectroscopy technique which provides information of the electronic structure and the orientation of the adsorbed ultra thin molecular layers on a variety of different substrates. The high resolution NEXAFS spectrum at the C 1s K edge (deepest core shell) for 3nm pentacene deposited on SiO₂ and sol-gel silica is shown in Figure 4.18 (a) and (b) respectively. Both spectra reveal two distinct features i.e. (1) The presence of two main discrete transitions between 283 eV and 288eV followed by (2) a broader spectrum at higher energy. According to literature, the first group is the manifestation of basic involvement of π^* LUMO and LUMO +1 orbitals while the broader spectrum is related to the σ^* orbitals. [112, 113] Besides, both NEXAFS spectra show a large modulation evident in the difference between spectra obtained at incidence angle of 90° and 20°, suggesting well ordered pentacene film. Briefly, the orientation of pentacene molecule can be determined by comparing the angular variation of peaks of the absorption spectra. It is obvious that the π^* orbital intensity is most intense near normal incidence, whereas σ^* -orbital intensity is greatest at incidence angle of 20°. This piece of information reveals that π^* -orbitals is preferentially oriented in the substrate plane, indicating that the pentacene molecule adopted an edge on orientation on both TOX and sol-gel silica substrate. The long axis tilt, on the other hand, is determined from the σ^* intensity variation. Since the σ^* - orbitals is greater near the glancing incidence (20°), it implies that the long axis of σ^* orbitals is normal to the substrate. Therefore, in both cases, pentacene films are confirmed to adopt a standing up orientation on TOX and sol-gel silica. As the intensity of the peaks varies with different incident angle, according to equation 4.4 and based on the analysis described in [114, 115],

$$I = A \left\{ \frac{P}{3} \left[1 + \frac{1}{2} (3 \cos 2\Theta - 1)(3 \cos 2\alpha - 1) \right] + \frac{(1-P)}{2} \sin 2\alpha \right\} \quad (4.4)$$

Where

I is the bound state resonance intensity, the integrated area of a normalized and deconvoluted peak

A is a constant, analogous to the extinction coefficient of conventional optical spectroscopy

P is the polarization factor the beamline

Θ is the angle of the beam relative to the substrate plane

α is the angle of the vector orbital relative to substrate normal

the pentacene molecule has an average orientation angle of about $75^\circ \pm 5^\circ$ away from the surface normal of TOX substrate which is similar to the reported value[115], whereas the conjugated plane of pentacene molecule is almost vertical aligned (90°) on SG silica surface.

Figure 4.18: NEXAFS Spectra obtained for (Left-a) 3nm Pentacene on TOX while (right-b) 3nm Pentacene on sol-gel silica.

4.5.4 Raman Study

The Raman peaks at 1158 cm^{-1} and 1177 cm^{-1} (Figure 4.19) originates from the C-H in-plane vibration of the pentacene molecule.[116] There is down-shift for both peaks of pentacene film on sol-gel silica, implying that pentacene molecules are more homogeneous, thus leading to a lower molecular relaxation energy [116, 117]. The peak at 1158 cm^{-1} may be deconvoluted to three vibrational modes at: 1158 cm^{-1} (ν_0), 1154 cm^{-1} (ν_1), and 1162.5 cm^{-1} (ν_2). The ν_1 band has been associated with in-phase intermolecular coupling (twinning) vibrations of different pentacene molecules in a unit cell, while the ν_2 band has been associated with the out-of-phase intermolecular coupling of different pentacene molecules in one (00 l) plane and its adjacent (00 l) plane [118, 119].

Figure 4. 19: Raman Spectra of pentacene films on TOX and sol-gel silica thin-film.

4.5.5 Photoluminescence study

Photoluminescence spectra of pentacene (Figure 4.20) exhibits excitation structures between 1.8 eV and 2.6 eV with the most pronounced peak detected at 1.81 eV. The energetically lowest single excitation at 1.81 eV has been modeled based on molecular Frenkel excitons (including Davydov splitting) or a charge transfer excitation, or a mixture of both [120]. It was also observed that there is suppression of the 2 eV and 2.15 eV peaks in pentacene films on sol-gel silica compared to that on TOX. Since the excitations above 1.81 eV are purely electronic in origin and not due to vibrations [120], they may be attributed to non-equilibrium recombination.

Figure 4. 20 : PL spectra of pentacene film on TOX and sol-gel silica thin-film.

Chapter 5 DISCUSSION

This chapter is divided into four sections. The first section will discuss the process of silica thin film formation via sol-gel silica methodologies and its implication as gate dielectric will be central to the discussion. The second section will be divided into 2 parts. The first part will focus on the improved performance of OFETs on sol-gel silica thin-film, discussing the influence of sol-gel silica dielectric surface properties on device performance, compared to OFETs on thermally grown Silicon dioxide (TOX). The second part will deal with the effect of the bulk properties of dielectric on device characteristics such as energetic disorder at the semiconductor-dielectric interface caused by high k and electrical characterizations of sol-gel silica based device at low temperature. The last section will focus on assessing data on the transistor device stability. i.e. (1) the flexibility of the plastic based device will be evaluated with cyclic mechanical bending tests. (2) Correlate the effect of mechanical tensile stress on the molecular ordering of the pentacene molecule.

5.1 Sol-gel silica film properties

5.1.1 The effect of thermal annealing on sol-gel silica film properties

The highlight of the sol-gel silica thin-film used in this thesis is the high k bulk properties and at the same time offer low surface energy (hydrophobic) and atomically flat surfaces ($< 3.1\text{\AA}$). Based on the information provided by FTIR and TEM images shown in Figure 4.1 and 4.2, the sol-gel silica thin-film properties could be schematically drawn in Figure 5.1. Porous silica comprising primarily Si-OH and H-O-H bonds gives rise to its high k , whereas the dense silica comprising majority Si-O-C bonds relative to Si-O-H bonds contributes to the low surface energy.

Figure 5. 1: Schematic cross-section of single sol-gel silica thin-film layer on Si wafer.

It is important to highlight that the sol-gel silica films were formed by thermally condensing the alkoxide precursor (TEOS) in two steps, first at temperature of 80°C or 100 °C in air and second at temperature of 100 °C in high vacuum (10^{-6} mTorr) for two hours. The existence of the hydroxyl (-OH) groups in the bulk sol-gel silica film could be attributed to the incomplete curing action by the mild annealing conditions used. In order to ensure complete dehydration of the film, it is necessary to identify that “water” is present in two forms: free water within the ultra-porous gel structure (i.e., physisorbed water) and hydroxyl groups associated with the gel surface. This dehydration of physisorbed water is complete at 170 °C.[92] Only by using very high curing temperatures (i.e., 400 °C) or extended curing time at temperatures in the range of 100-200 °C, would the concentration of hydroxyl groups be sufficiently decreased for use in low dielectric constant applications [91, 92]. It was also observed that the sol-gel silica thin-film has lower contact angle of only $\sim 50^\circ$ after the first curing step, compared to contact angle of $\sim 75^\circ$ after the second curing step at high vacuum, suggesting high vacuum and heat (100 °C) causes further dehydration of physisorbed water and partial removal of hydroxyl groups, mainly at the surface and area near the surface. Consequently, this produces the characteristic $\sim 75^\circ$ contact angle, yielding a low energy

surface without the need of any silane treatment. Concurrently, the structure and texture of the gels evolve: the isolated hydroxyl groups within the pore surface react with each other, bringing particles together (during the course of a polycondensation reaction), thereby eliminating pores within the sol-gel silica and forming the densified layer. If the trapped water in the pores is unable to be desorbed prior to pore closure, it is trapped inside the densified gel [92]. This could probably be the origin for the high dielectric constants measured in the sol-gel silica films.[100] Furthermore, the required high temperature of up to 400 °C for complete dehydration signifies that the high k property of sol-gel silica thin-film is stable and well-suitable for the organic electronics processes and applications.

5.1.2 The effect of plasma treatment on sol-gel silica film properties

As presented in section 4.3, tri-stratal sol-gel silica with thin-thick-thin gate dielectric architecture employed the methodology of plasma treatment to achieve densification of the bottom thin silica film while modulating the –OH species in the thicker central silica layer. In general, k can be altered by the presence of polar –OH groups in the dielectric.[12, 103, 121, 122] During air plasma of the middle and bottom layers, polar –OH groups can originate due to the breaking of the unhydrolysed –OR groups as well as owing to interaction of the resultant dangling bonds with moisture[123]. The reduction in film thickness of sol-gel silica with increasing duration of air plasma is readily attributable to the presence of O₂ plasma species which effectively remove –OR groups and facilitate the condensation reaction between the –OR and –OH group, thus resulting in thickness reduction. (Figure 4.12 (c)) This leads to the trend of increasing k with increasing duration of air plasma (Figure 4.12 (d)).

Conversely, an inert gas such as argon is less effective in eliminating -OR bonds thus resulting in lesser -OH group formation when exposed to air.[124] Hence, the thickness of sol-gel silica film which is independent of Ar plasma duration (Figure 4.12 (c)), signifies that increasing the duration of Ar plasma treatment purely promotes densification[124] of sol-gel silica surface without introducing polar -OH species responsible for increasing the k of the bulk of central film. Hence the trend of lower k with increasing Ar plasma was observed (Figure 4.12(d)).

5.2 The influence of surface properties of gate dielectric on OFETs device characteristics

The effect of sol-gel silica dielectrics on its field-effect transistor performance has been studied extensively by using the thermally evaporated pentacene molecule on rigid (Si) and flexible (PET) substrate. As presented earlier in section 4.2 and 4.3, the main benefits of employing sol gel silica as gate dielectric material can be highlighted as 1) possess high k properties which enable low voltage operating OFETs; 2) low temperature processing amenable to solution and plastic substrate process and 3) enhanced device performance compared to pentacene FETs fabricated on TOX and SiNx. Apart from the increased carrier densities related to the presence of strongly polar dielectrics [125, 126]; improved interfacial ordering and grain size [127, 128] as well as reduced interfacial trap densities [129-131] may be considered as contributing factors to the observed improved device characteristics.

5.2.1 The effects of interfacial chemistry and trap density on device performance

The gate dielectric plays a vital role in the characteristics of the OFET devices, and in particular the mobility of the charge carriers is critically determined by the intrinsic properties of the semiconductor-dielectric combination, directly affecting the semiconductor structural order especially in the case of bottom gate structure. Table 5.1 summarizes the device characteristics of pentacene FETs on different dielectric interface. Noticeably, it was observed that devices with pentacene and sol-gel silica interface consistently showed impressive device characteristics regardless of the different thicknesses of sol-gel silica next to pentacene layer, thus suggesting that this phenomenon is clearly an evidence of semiconductor-dielectric interface phenomenon.

Table 5. 1: Summary of electrical performance of Pentacene FETs on different dielectric interface

Substrate	Dielectric	μ_{sat} ($\text{cm}^2/\text{V s}$)	V_{th} (V)	s.s (mV/decade)	N_{max} (cm^{-2})	$I_{\text{ON}}/I_{\text{OFF}}$ ($\times 10^6$)	C_i (nF/cm^2)
Si	TOX (45nm)	0.11	-6.13	400	2.73×10^{12}	12.1×10^6	76.7
Si	Sol-gel (355 nm)	2.08	-1.76	300	6.33×10^{11}	1×10^3	25.1
Si	SiO ₂ (45nm)+ Sol-gel (342nm)	0.95	-3.63	289	6.59×10^{11}	4.07×10^6	26.6
PET	SiNx (28.95nm)	0.095	-1.15	581	4.32×10^{12}	1×10^3	78.95
PET	SiNx(28.95nm)+ Sol-gel (60nm)	0.98	-0.9	230	8.68×10^{11}	2×10^5	48.59
PET	Tri layer Sol-gel (20nm/60nm/20nm) With 3 minutes Ambient plasma	3.42	-0.83	151	7.3×10^{11}	2.07×10^6	77.3

According to experimental and theoretical works by Carlo *et al.*, the potential barrier between grains is found to be the determining factor for mobility degradation observed in devices with small grain size. In this study the mobility variation observed for pentacene on different gate dielectric could be readily related to the regular large

pentacene grains ([127, 128]) observed on sol-gel silica thin film ($\sim 2.5\mu\text{m}$), compared to ~ 0.2 to $0.5\mu\text{m}$ irregular grains size observed on TOX and SiNx. Even though the morphology of pentacene is different for sol-gel silica on Silicon and plastic substrate (granular vs dendritic) (Figure 4.16), possibly due to dissimilar surface roughness of the corresponding sol-gel silica film on different substrate, it is important to highlight that the average size of pentacene grains did not change with changing sol-gel silica thicknesses, confirming the surface dielectric effect. As the deposition rate and substrate temperature were identical for all the difference substrates, the resulting larger grain growth of pentacene molecule could only be attributed to the smoothness and the hydrophobic nature of sol-gel silica surface properties (RMS roughness of $< 0.3\text{nm}$ and water contact angle of $\sim 72^\circ$), inducing and facilitating the molecular ordering of the pentacene layer. Furthermore, by comparing pentacene FETs on TOX and SiNx which both shows to have similar small grain size of pentacene molecule, the lower mobility obtained in Pentacene/SiNx is most probable related to the poor surface roughness of SiNx film ($\sim 3.1\text{nm}$) compared to TOX ($\sim 0.31\text{nm}$). It has been reported that the charge transport is confined at the first 6nm of the semiconductor next to the dielectric layer [82], hence, the charge carrier mobility can be improved by reduction in surface scattering mechanism with smoother interface between dielectric and organic semiconductor.[132]

The better interfacial effect of the sol-gel silica with pentacene molecule is explicitly evident in the improvement of the threshold voltage (V_{TH}) presented in section (4.2.2), where early turn on is detected for pentacene devices with lower effective capacitances (Table 5.1). Besides, another key observation in this study is the improvement in the subthreshold swing (s.s) in the devices with pentacene and sol-gel silica film interface; The s.s. is associated to interfacial trap density which can be calculated based on equation 5.1

$$N_{\max trap} = \frac{C_i}{q} \left(\frac{q \cdot S \cdot S \log e}{k_B T} - 1 \right) \quad (5.1)$$

where k_B is Boltzmann 's constant, T is temperature in Kelvin, e is the base of the natural logarithm, q is the electronic charge, $s.s$ is the reciprocal subthreshold slope in (V/decade), and C_i is the capacitance per unit area of the gate dielectric. The calculated trap densities from its $s.s$. shows consistently lower trap densities for the devices on sol gel silica than the devices on TOX and SiN_x (Table 5.1), further suggesting the superior surface properties of the sol gel silica thin film enabled lesser interfacial traps densities ,resulting in improved devices characteristics.

According to literature, sources of traps are localized at impurities, semiconductor-dielectric interface, and chemical/physical defects.[1] Considering that pentacene molecule is deposited on sol gel silica, TOX and SiN_x by using the identical processing method, the presence of traps due to impurities may be neglected. In particular, trap density has been largely attributed to the differences in the dielectric-semiconductor interface chemistry with Si-OH groups which are known to trap electrons rather than holes, suppressing mobility in N-type organic semiconductor ,while introducing extra holes at the semiconductor–dielectric interface for charge balance, resulting in a positive V_{TH} shift in the hole dominating charge transport.[65, 133] In this study however, the positive V_{TH} shift in the pentacene devices on sol-gel silica compared to that of TOX and SiN_x cannot be appropriately correlate to these electron trapping Si-OH groups because the surface of sol-gel silica film is hydrophobic (due to the presence of unhydrolysed Si-OR group and indicated by the water contact angle of $\sim 75^\circ$), thus lesser Si-OH groups as discussed earlier in Section 5.1. For that reason, investigation in the changes in microstructure and molecular ordering induced by the sol gel silica film surface properties

is thus essential to provide insights to understand the origins of the enhanced device performance in the sol gel silica based FETs.

5.2.2 Correlation between Morphology, Molecular Ordering, and Enhanced Transistor Performance

It has been discussed in the previous section that pentacene films deposited on the sol-gel silica dielectric showed an increase in grain size from $\sim 0.4 \mu\text{m}$ on TOX to $\sim 2.5 \mu\text{m}$ on sol-gel silica dielectric (Figure 4.16). It is widely acknowledged that smoother [134] and lower surface energy [13, 135] dielectrics can induce and facilitate molecular ordering of pentacene molecule. In this study, the sol-gel silica surface properties seem to have the similar effect to facilitate the growth of larger pentacene grains.

The calculated $\bar{L}_{hkl}$ (the mean crystalline domain size perpendicular to the plane (hkl)) from their S-XRD FWHM peaks depicts the similar trend in increase grain size, and a more ordered pentacene film (g_H , the degree of structural disorder was determined to be 1.85 % and 1.40 % for pentacene film on TOX and sol-gel dielectric respectively), corroborated by the stronger intensities of the S-XRD diffractions peaks for pentacene on sol-gel silica. Besides, the better terrace structured of pentacene film on sol-gel silica is confirmed by the number of reflecting planes $\bar{N}$, estimated to be 66 and 115 ML (monolayers) on TOX and sol-gel dielectric, agreeable to its height distributions obtained from their AFM images (Figure 5.2).

Figure 5. 2: Pentacene morphology on (a) TOX and (b) sol-gel silica with its height distribution analysis.

Although it is widely reported that larger grain sizes (reduced grain boundaries) contributes to improved charge carrier mobility, however, it is also known that use of surface modification layer such as octyltrichlorosilane (OTS) leads to improved mobilities despite smaller grain sizes [136]. Coalescence studies of first and second layers leading to a uniform film before bulk film growth [22] as well as the reports indicating different molecular orientations within identical pentacene polymorphs [137] further emphasize the fact that improved device performance may not be explained solely via improvements in film morphologies. Therefore, NEXAFS, photoluminescence (PL) and Raman studies were employed to investigate the correlation between morphology observation, molecular orientation, intermolecular order, and solid-state packing since both exciton migration and carrier mobility are strongly dependent on the intermolecular overlap, leading to increased bandwidth [138] and thus resulting in improved charge carrier mobility.

Photoluminescence studies are routinely employed in material analyses as a measure of the defects (structural or impurities). In our measurements, the first emission energy transition (1.81 eV) from the PL spectra is comparable to the pentacene HOMO-LUMO gap ($E_g=1.88$ eV for thin film phase [139]) enabling its assignment to electron-hole pair recombination [140]. The suppression of the 2 eV and 2.15 eV peaks (and

nonequilibrium recombinations) in pentacene films on sol-gel may be attributed to larger grain sizes and larger cluster heights, similar to a report on island growth studies in pentacene films [141].

In addition, as explained earlier in section 2.1.2, the mechanism for charge transport of organic semiconductor at room temperature may be depicted as hopping transport, which is affected by [142, 143]: i) the electronic coupling between adjacent molecules (transfer integral) [80], and (ii) the reorganization energy (λ_{reorg}). The former factor needs to be maximized while the latter may be ignored in the case of pentacene thin films [144] in comparison with substrate-induced intermolecular interactions. Thus, Raman spectra of pentacene was used to probe the correlation between the intermolecular couplings and the charge carrier transport within pentacene films [118]. The Raman peaks at 1158 cm^{-1} and 1177 cm^{-1} (Figure 4.19) originate from the C-H in-plane vibration of the pentacene molecule has shown a down-shift for both peaks of pentacene film on sol-gel silica, implying that pentacene molecules are more uniform and homogeneous, thus leading to a lower molecular relaxation energy [116, 117]. The peak at 1158 cm^{-1} may be deconvoluted to consist of three vibrational modes at: 1155 cm^{-1} (ν_0), 1154 cm^{-1} (ν_1), and 1162.5 cm^{-1} (ν_2). As depicted in Table 5.2, the pentacene film deposited on sol-gel silica dielectric shows a stronger ν_1 relative to the ν_0 band intensity and the corresponding spectral area ratio of ν_1 to ν_0 bands (A_{ν_1}/A_{ν_0}) was 0.89, compared to 0.50 for pentacene film on TOX, indicating strong in-phase (intralayer) intermolecular interaction between pentacene molecules (Figure 5.3). Thus, the surface chemistry of sol-gel silica seems to promote an enhanced in-phase intermolecular coupling and facilitates the π -orbital overlap (improving transfer integral), thus leading to better carrier transport.[118]

Table 5. 2: The ν_0 , ν_1 , and ν_2 vibrational mode analysis of Raman spectra from pentacene films on TOX and sol-gel silica.

Sample	ν_0 band		ν_1 band		ν_2 band		A_{ν_1}/A_{ν_0}	A_{ν_2}/A_{ν_0}
	$\lambda_{\max}$ (cm^{-1})	A	$\lambda_{\max}$ (cm^{-1})	A	$\lambda_{\max}$ (cm^{-1})	A		
Pc on TOX	1157.9	4.27	1153.9	2.15	1162.5	0.58	0.50	0.14
Pc on SG silica	1157.3	2.01	1153.0	1.79	1160.4	0.35	0.89	0.17

Figure 5. 3: Schematic representation of the in-plane intermolecular coupling (1155 cm^{-1}) effect of the pentacene molecules within the same layer and out of phase coupling (1162 cm^{-1}) between different layers

Furthermore, the NEXAFS spectra presented in section 4.5.3 has shown a strong edge on characteristics of pentacene orientation. In particular, pentacene molecule is standing upright with its long axis tilt vertical with respect to sol gel silica surface compared to that of TOX which is characterized to have a 5° to 10° tilting angle from the normal of the substrate, supported by the stronger intensity of the π^* region detected for pentacene on sol-gel silica at the incidence angle of 90° compared to that of pentacene on TOX as evidenced from Figure 4.18. This observation is again aligned with the observation in S-XRD which shows a more ordered film of pentacene on sol-gel silica. Moreover, the near vertical pentacene molecule orientation on sol-gel silica also implies increased efficiency in π -overlap[77, 145] and thus stronger intermolecular coupling from

side to side (adjacent pentacene molecule), supporting the detection of stronger in-phase (intralayer) intermolecular interaction between pentacene molecules deposited on sol gel silica as presented in Raman analysis.

5.3 The influence of bulk properties of dielectric on device performance

5.3.1 Device hysteresis induced by space charge electrets

Hysteresis is undesirable in transistor characteristics and is known to be due to the impurities and trapped charges, such as hydroxyl groups that can capture electrons [146] at the semiconductor-dielectric interface, the bulk of the dielectric as well as due to the inherent properties of the dielectric [147]. As presented in section 4.1.2, the pentacene FETs on single layer SG silica shows a gate sweep rate dependent hysteresis behavior. Upon employing a bilayer dielectric with TOX or SiNx as the blocking layer beneath sol gel silica film in the fabrication of FETs, the hysteresis behavior diminishes accompanied with lower off current recorded in Pentacene FETs, yielded evidence of the hysteresis is bulk-related rather than interface-related. Similar to a recent report [148], such phenomenon is attributable to trapping of the electron injected from gate by the hydroxyl groups inside the pores (space charge electret). Sol-gel silica films are known to trap moisture in nanopores inside its bulk [92] ensuing in higher k values compared with TOX [100], which could be supported by the cross-sectional transmission electron microscopy (XS-TEM) observations to reveal the presence of these nanopores (~10-12 nm in diameter) and also a denser silica layer on its surface. (Figure 4.3) The hydroxyl groups contained in the nanopores near the Si substrate interact with the high electron density, resulting from the application of negative gate bias voltage, and form electron trapping centers which create charge electrets, as illustrated in schematic explanation in Figure 5.4. Due to the denser silica layer and the vacuum condition during measurement (desorption

of water species physically from the area near the surface), the trapping of electrons from the channel to the sol-gel silica is negligible. The presence of the space charge electret in the bulk SG silica dielectric create external electric field which induced holes in the active channel and thus resulting in higher off current in the pentacene FETs on single layer sol gel silica as shown in the transfer characteristics in Figure 4.4 and schematic diagram in Figure 5.4 illustrates the mechanism of creation of space charge electrets.

Similar to the mechanism in Si-FETs, these charge traps may be identified as border traps, are spatially separated from the Gate/sol-gel silica film interface; but however, the such interface are close enough to exchange charge under sufficient electric field. These borders traps respond slowly to the applied voltage sweep [149] and thus result in the sweep rate dependent transfer characteristics (Figure 4.5).

Figure 5. 4 : Schematic cross section of OFET with sol-gel silica as the gate dielectric. The minus signs represent volume charges injected and trapped into sol-gel silica from the gate. The plus signs represent the induced positive charges accumulated at the semiconductor interface. The upper part of sol-gel silica has denser structure, thus containing less water/-OH groups.

5.3.2 The effect of high k gate dielectric on charge transport in organic semiconductors

Although widespread efforts to synthesize high mobility organic semiconductors have taken a leap, the fabrication of low voltage driven OFETs is essential to reduce power consumption in electronic applications remains a challenge. With this intention, high permittivity (k) dielectrics compatible with plastic substrates which induce high capacitance at low voltages have been actively pursued.[1, 10, 87, 105] However, as shown in Table 2.3 in section 2.3, the OFET performance with this kind of gate dielectrics generally still leads to low mobility and a high degree of variability. Questions thus arise whether employing a high k insulator could provide a solution for both low voltage operations while ensuring high charge carrier mobility on the condition that the surface morphology of the high k insulator is not the determining factor in charge transport.

The experimental data shown in section 4.3 clearly demonstrated an adverse effect of high k gate dielectric on both pentacene and P3HT device performance. It is critical to note that the tri-stratal sol-gel silica is designed and fabricated in such a way that the top layer is processed identically to ensure similar surface roughness and surface energy, while having different high k value of the bulk dielectric. It is thus valid to state that the observed trend of higher k accompanied with lower charge carrier mobility was not caused by morphological concerns of the gate dielectric and its effects on the packing of the organic semiconductor. This could essentially also be supported by the fact that, in this study, all pentacene devices showed comparable turn on voltage (V_{on}) and insignificant hysteresis behavior (Figures. 4.14). V_{on} for a p-type transistor is the lowest voltage at which there are no mobile holes in the active channel and is dependent on the interface states. If electron acceptors are present in the p- type transistor V_{on} will become

positive while in the presence of hole traps it will shift to more negative values. The small variance in the V_{on} and negligible hysteresis behavior for all samples with different dielectric constant in the bulk of tri layer sol-gel silica suggests that the fixed charge at the surface of sol-gel silica stacks and interfacial chemistry at dielectric/semiconductor interface is alike since all the top layers of the tri-stratal sol-gel silica next to organic semiconductor were processed identically. Besides, the calculated subthreshold swing (Table 5.3) illustrates that the interfacial trap density is approximately comparable for all the samples, further implying that the improvement in the carrier mobility in the devices (Pentacene and P3HT) with sol-gel silica which underwent 4 minutes of Ar plasma was in fact influenced by the bulk properties of the dielectric film, which in this case is the lowest dielectric constant of all. The AFM images of the large dendritic grain of pentacene ($\sim 2.5 - 2.7\mu m$) for all samples proved that surface roughness and surface energy is not the root cause of such variation in the mobility. Therefore, it is certainly appropriate to eliminate factors such as molecule ordering, interface surface chemistry and physical property as mentioned earlier, to conclude that charge carrier mobility is lower with higher k gate dielectric.

The decrease in carrier mobility with increasing k has been reported both for disordered polymeric organic FETs and single crystal rubrene FETs.[23, 26]. Both reports attribute the observation to the charge localization of the organic semiconductors systems due to the interaction with the induced polarization in the gate insulator. Such interaction is stronger for larger k and qualitatively explains the reduced mobilities with increasing k . Veres et al. claimed that the dipole field present in the higher k gate dielectric may enhance the formation of local states in the conducting channel which induce carrier localization and reduce the charge carrier mobility.[13, 23] To further elaborate, the high polarizability of the dielectric results in the broadening of Gaussian

distribution of the energy levels near the HOMO level edge. The broadening effectively decreases the density of states at the Fermi energy and lowers the hopping probability, thus restricting the transport of charge carrier in the active channel. This explanation is in good agreement with the theoretical works by Bassler.[150]

Table 5. 3 :Room temperature device characteristics of Pentacene and P3HT FETs on tri layer SG silica with Argon (Ar) and air (Air) plasma treatment and RMS roughness of tri layer SG silica stack with different plasma treatment.

Plasma	Duration (mins)	RMS Roughness (Å)	Pentacene FETs*				P3HT FETs*			
			μ_{sat} (cm ² /Vs)	C_i (nF/cm ²)	V_{TH} (V)	$S.S$ (mV/dec)	μ_{sat} (cm ² /Vs)	C_i (nF/cm ²)	V_{TH} (V)	$S.S$ (mV/dec)
Ar	2	3.2	3.09	83.27	-0.94±0.02	175	0.113	80.25	-1.55±0.02	793
	3	3.5	5.54	78.56	-0.99±0.03	166.5	0.349	74	-1.71±0.03	710
	4	3.8	6.30	67.26	-1.11±0.08	156	0.429	60.25	-1.87±0.06	705
Air	2	2.1	4.90	78.99	-1.29±0.05	156.5	0.225	79	-2.00±0.03	895
	3	2.2	3.18	83.5	-1.29±0.05	156	0.204	81.62	-2.04±0.03	795
	4	2.1	2.09	92.1	-1.44±0.09	163	0.153	87.86	-2.30±0.07	852

* Data collection based on 8 devices each for every SG silica film with different plasma treatment. In total, 12 samples were prepared and 64 devices were tested.

It had been previously proposed that an intermediate low k layer which is at least 50nm thick could provide effective screening of the energetic disorder from dipoles in the dielectric.[13] This proposal is in accord with a recent quantitative analytical model developed by Richards et al., which further elaborates on the variation of energetic disorder caused by dipoles in the dielectric with varying distance from the interface.[151] This interestingly raised the possibility that the observed increased carrier mobility in OFETs devices with surface modification layers such as SAMs (OTS, HMDS and other silane treatment) [40, 152-154], in addition to the enhanced molecular ordering and

alignment which is the apparent first order effect to account for the improved mobility, a reduced energetic disorder due to less polar surface caused by the silane group may also be an underlying factor. In other words, the surface modification layer acts like a shield to screen the polarization effect of bulk gate dielectric onto the charge transport in active channel. In this work, the middle layer of tri-stratal sol-gel silica is the core contributor of high polarity to induce high capacitance to drive the transistor at low voltage. The ~20nm top dense layer of sol-gel silica is inadequate to screen the influence of dipole on the charge localization at the interface between active layer and dielectric as suggested by the literature report.[23] Hence, in order to verify the hypothesis of the possible screening effect of the energetic disorder caused by the polarization of the bulk high k gate dielectric, an extra capping layer of sol-gel silica (20nm) was added on top of the pristine tri-stratal sol-gel silica which underwent 2 minutes Ar plasma treatment. It was interesting to show that with approximately equivalent k value of 9.78 (the reference samples, tri-stratal sol-gel silica with 2 minutes Ar plasma) and 9.83 (with addition of capping layer), the pentacene FETs with capping layer on top of the tri-stratal sol-gel silica ($k=9.83$) shown 169% of improvement in charge carrier mobility to record a saturation mobility of $6.55\text{cm}^2/\text{Vs}$ (Figure 5.5). This provides evidence that energetic disorder caused by the polarization of the bulk dielectric, which is detrimental to the carrier mobility at the semiconductor-insulator interface could possibly be reduced in effect by extra dense sol-gel silica capping layer. It is however important to highlight that, a slight dependency of the threshold voltage on the dielectric constant has also been observed for the pentacene and P3HT FETs which is not fully understood.

Figure 5. 5: (a) and (b) Device architecture of tri-stratal sol-gel silica device with and without capping layer. (c) Transfer characteristics of the pristine samples tri-stratal sol-gel silica which underwent 2 minutes Ar plasma (Red) and samples with capping layer(Blue).

5.3.3 Impact of trapped moisture in bulk sol gel silica on charge transport at low temperature

The low temperature (100K-300K) dependence of the charge carrier mobility of pentacene FETs with tri-stratal sol-gel silica is shown in Figure 5.6(a). The mobility of pentacene FETs on tri-stratal sol gel silica decreases with decreasing temperature. At 125 K, the mobility of the sol-gel silica FET reduces to $\sim 2 \times 10^{-3} \text{ cm}^2/\text{Vs}$, which is 4 orders of magnitude lower than the mobility at 300 K ($\sim 6.5 \text{ cm}^2/\text{Vs}$). In addition, the measured characteristics indicate that there are two different temperature dependent mobility slopes. The activation energy (E_a) of pentacene FETs is given by the Arrhenius relation [34]:

$$\mu = \mu_0 \exp\left(-\frac{E_a}{k_b T}\right) \quad (5.2)$$

where μ_0 is the free carrier mobility, E_a is the activation energy to escape from trap states to delocalized states, and k_b is the Boltzmann constant.

As shown in Figure 5.6 (a) the low temperature dependent mobility of pentacene FET with sol gel silica follows the Arrhenius law in the temperature range 220K – 100K, with an apparent activation energy (E_a) of 53 meV, comparable with the literature values of pentacene on TOX [6]. This has been attributed to the activation energy for shallow traps due to grain boundaries and line dislocations in the pentacene film. [155] However, the temperature dependent mobility of pentacene FET with sol-gel silica is not monotonic, consisting of a second activation energy. The second E_a of 234 meV was detected at the temperature range from 300– 220 K, accompanied by a sudden increase in charge carrier mobility in the pentacene device at $T > 225$ K. This peculiar phenomenon is attributable to the water molecule trapped in the nanopores of the bulk sol gel silica film. Upon increasing the sample's temperature above 225K, the water molecule transforms from its solid state into its supercooled water transition phase (Coexistence solid state and liquid-state).[156] Thus, the polarization of these water molecule dipoles will induce additional effective gate field. The additional effective electric field is confirmed with a sudden increase of capacitance from 56nF/cm² to 85nF/cm² at temperature of 200K to 220K which is induced by the random water molecule dipoles in the solid state for this temperature range. Hence, with the increase of concentration of the mobile carriers, the channel conductivity as well as the charge carrier mobility will increase. The increase in off - current in the transfer characteristics of the sol gel device with temperature also signifies the increased channel conductivity as depicted in Figure 5.6(b).

Figure 5. 6: (a) Temperature dependent saturation mobility for Pentacene FETs with sol gel silica. (b) Transfer characteristics of Pentacene FETs with tri-stratal sol-gel silica, measured at 125K, 225K and 300K to show different hysteric behaviour.

In addition, it was also observed that there is a temperature dependent hysteresis in the sol-gel silica devices, increasing with temperature with clockwise direction, followed with decrease in its window at temperatures close to room temperature.(Figure 5.6(b)) In general, pentacene FETs displaying anticlockwise hysteresis has been related to pentacene structural defects [155]. As the hysteresis window is temperature dependent and in clockwise direction, the low temperature charge transport for sol-gel dielectric device could be dominated by the effects of water molecules residing in the nanopores. Upon freezing down to 120 K, the water molecule dipoles are randomly oriented; and upon increasing the temperature, above its glassy water temperature, the water molecule dipoles could be aligned easily resulting in the observed temperature dependent hysteresis behavior. In other words, the hysteresis in sol gel silica dielectric devices could be induced via bulk trapping of (1) space charge electret at room temperature at the absence of effective blocking layer and/or (2) dipolar electret which only occur at low temperatures.

5.4 Sol-gel silica device stability

5.4.1 Cyclic bending testing

The applicability of sol-gel silica dielectrics towards plastic electronics necessitates an investigation of the effects of mechanical strain on electronic properties of OFETs. It has been shown earlier in section 4.4 that no degradation on electrical performance of SG silica based devices was detected when the devices was subjected to bending strain of 2.27%. It is however interesting to observed an increase in drain current upon removal of the bending strain, which translated into increase in charge carrier mobility as shown in section 4.5. To further confirm the phenomenon, the sol-gel silica based device was subjected to a continuous 12500 cyclic bending testing for 15 hours in air (Humidity level $\sim 65\%$) as depicted in Figure 5.7(a). After the cyclic test, the leakage current (I_{GS}) was proven insignificantly affected and the transfer characteristics also show a similar increase of drain currents as depicted in Figure 5.7(c) and (d). These cyclic bending tests results indicate the robustness of sol-gel silica as potential gate dielectric candidates to be used for flexible electronics. Figure 5.7(e) reveals the environmental stability of the pentacene device on flexible substrate after storage for 18 months under humidity level of 65%.. Eventhough 15% degradation in the context of the drain current of the pentacene device was detected; similar drain current can be achieved by increasing the gate bias to -5V.

Figure 5. 7: (a) and (b) Schematic and the snapshot of the sample underwent cyclic bending test. (c) Comparison of the leakage current of the trilayer SG silica before and after 12500 cycles of bending strain. (d) The transfer characteristics of pentacene devices on the tri layer SG silica (4 minutes Argon plasma treated) to show improvement in drain current after the bending cyclic test. (e) Transfer Characteristics for the pentacene devices after storage in environment for humidity 65% for 18 months.

5.4.2 Correlation between organic molecular ordering and mechanical bending strain

As shown in section 4.4 and 5.4.1, the first bending experiment on pentacene devices on tri-stratal sol-gel silica (3 minutes air plasma) silica has been shown to improve pentacene carrier mobility upon recovery of the bending strain. A similar observation was detected after 12500 cyclic testing of other devices (on pentacene devices on tri-stratal sol-gel silica (4 minutes Argon plasma)). Thus, Raman spectroscopy was employed to examine the strain induced molecular changes in the tri-stratal sol-gel silica FETs by using the same bending test tool to ensure identical bending strains. As reported in [157, 158], the Raman peaks at 1158 and 1177 cm^{-1} originate from the C-H in-plane vibration of the pentacene molecule. The peak at 1158 cm^{-1} may be deconvoluted into three vibrational modes at: 1158 (ν_0), 1154 (ν_1), and 1162.5 cm^{-1} (ν_2). As explained earlier, the ν_1 band is associated with in-phase intermolecular coupling vibrations of different pentacene molecules in a unit cell, while the ν_2 band is correlated to the out-of-phase intermolecular coupling as illustrated in Figure. 5.8 (inset). Interestingly, the ν_1 bands show larger increment in the spectral area while ν_2 bands show smaller value after the devices were subjected to bending strain (Table 5. 4). This suggests that optimal π - π orbital overlap is improved upon bending and further enhanced after recovery from bending. Correlation between in-plane coupling (ν_1) and charge transport in pentacene thin films has been reported.[158] Hence, the slight increase in the drain current and the μ_{sat} upon bending strain may be explained on the basis of improved in-plane coupling. Similar observation in detecting higher drain current upon recovery from bending strain was reported and was attributed to bending stress induced phase transition in pentacene.[159]

Table 5. 4: The Gaussian/Lorentzian fitting results of the C-H bending modes of pentacene film on 113nm tri-stratal sol gel silica under different bending conditions. $\lambda_{\max}$ = Raman shift peak center. A = relative spectra area, Av_1/Av_0 = spectral area ratio of v_1 band to v_0 band, Av_2/Av_0 = spectral area ratio of v_2 to v_0 band.

Samples	v_0 band		v_1 band		v_2 band		Av_1/Av_0	Av_2/Av_0	I_{on}^a (μA)	μ_{sat} (cm^2/Vs)
	$\lambda_{\max}$ (cm^{-1})	A	$\lambda_{\max}$ (cm^{-1})	A	$\lambda_{\max}$ (cm^{-1})	A				
a) Before bending	1158.3	0.44	1153.3	0.33	1163.3	0.10	0.75	0.23	3.00	1.98
b) During bending	1158.3	0.36	1154.4	0.33	1163.7	0.10	0.92	0.28	5.70	2.35
c) After bending	1159.4	0.28	1155.5	0.42	1164.7	0.05	1.5	0.18	7.07	2.48

^a I_{on} was taken at $V_G = -3.0\text{V}$

Figure 5. 8: Raman Spectra of pentacene measured i) before bending, ii) during bending and iii) after bending. The Gaussian/Lorentzian functions used for the deconvolution are shown as the dotted line. Left Inset: schematic representation of the in-plane intermolecular coupling (1155cm^{-1}) effect of the pentacene molecules within the same layer and out of phase coupling (1162cm^{-1}) between the different layers. The right inset depicts the bending test set up with bending radius of 24 mm.

Chapter 6 CONCLUSIONS

This thesis presents an in-depth investigation of the effect of gate dielectric on the dielectric – semiconductor interface in particular and charge transport in general. Improvements in device performance brought about by the gate dielectric were studied in relation to the interfacial structural order, together with the influence of the dielectric on bulk and surface traps. The conclusions and original contributions generated from this thesis can be summarized as following:

1. Smooth (rms roughness $< \sim 3.0 \text{ \AA}$) and low surface energy ($\sim 70 \pm 5^\circ$) silica thin-films could be produced on plastic substrates through optimized sol gel processing methodologies. The lower surface energy of the silica film is brought about by the presence of non-hydrolyzed Si-OR surface groups, where R represents alkyl groups. The high k value (~ 10) of sol-gel silica films is attributed to the presence of hydroxyl groups and water molecules trapped in the nanopores present in the porous bulk film. The high k value will result in lowering of the driving voltages of typical organic field effect transistors. While typical oxide or polymer dielectric based OFETs operate at excess of -20 V, the sol-gel dielectric based devices showed excellent saturation currents as low as -3 V.
2. Improved OFET performance (charge carrier mobility, threshold voltage, and subthreshold swing) with mobilities as high as $\sim 6.55 \text{ cm}^2/\text{Vs}$ on plastic substrates were achieved with sol gel silica dielectrics in pentacene FETs as compared with mobilities of ~ 0.1 and $\sim 0.095 \text{ cm}^2/\text{Vs}$ on TOX and SiNx respectively. The consistent improvements in mobility on different dielectric layers (TOX and SiNx) suggest that

this surface modification is an important contributor, with reduced trap densities contributing greatly to the improved OFET performance. The low defect density and low surface energy promotes larger grain growth and improved crystallinity for pentacene as evidenced by analysis based on AFM, S-XRD and NEXAFS studies. Photoluminescence / absorption and Raman studies also highlighted that intermolecular interactions, and better molecule structural order are of great significance in comprehending the improved mobility, threshold voltages, sub-threshold swings, and lower interface trap densities.

3. In addition to the surface modification effect on the interfacial order and molecular packing, the ‘bulk’ of the sol gel silica films also affect charge transport through: a) the electret effect b) the effect of high k on mobility and interfacial dipolar disorder and c) the polarization effect of the moisture trapped in the sol gel silica nanopores.
4. One of the significant issues related to sol gel silica films is that the Sol-gel films directly deposited on gate electrodes yielded OFETs characterized by high leakage and large hysteresis caused by an electret mechanism, which entailed electron injection into the hydroxyl groups contained within the nanopores of the SG films. Rather than rely on a blocking layer which may not be compatible with plastic electronics, the tri-stratal sol-gel silica films coupled with appropriate plasma treatments yielded a skin layer comprising densified SG silica films (<25nm) that prevented electron injection from the gate and enabled the possibility of using a solution processed dielectric on plastic substrates without the need for electret blocking layers.

5. One of the noteworthy findings of this thesis demonstrate that addition of a low- k capping layer (on top of the tri-stratal sol-gel silica film) results in a >150% improvement in mobility. These findings clearly demonstrate that the charge transport in OFETs is not only influenced by the widely acknowledged effects of molecular ordering and interfacial morphology, but is strongly modulated by the polarizability of the gate dielectric, which may lead to charge localization and limit device performance.
6. Temperature dependent mobility, hysteresis, capacitance, and threshold voltage studies provided further insight into the effect of the gate dielectric's bulk properties on charge transport. The existence of hysteresis at temperature ranges of 200K-225K indicated strong polarization caused by dipoles attributable to water molecules trapped within the SG nanopores. Activation energies of 234meV and 53meV were detected above and below 225k respectively; with the latter value in excellent agreement with published literature.
7. The reliability of the sol gel silica based OFETs was verified by ambient ageing and mechanical flexing. Pentacene devices shown insignificant degradation in leakage current after being subjected to 12500 bending cycles (24mm bend radius). Besides complete recovery after each bend cycle, the drain current and charge carrier mobilities showed an increase of ~15 to 20 % respectively. Ramam spectroscopy revealed stronger intra layer π - π intermolecular coupling, suggesting that rather than degrading the quality of the semiconductor, bending strain actually improved the packing of the pentacene molecules. Devices that were stored under ambient conditions for over 18 months showed excellent device characteristics, albeit with a

moderate degradation of drain currents which could arguably be attributed to the organic semiconductor rather than the sol-gel silica dielectric.

In summary, it may be concluded that significant device enhancements were demonstrated by sol-gel silica based dielectric which is applicable to a broad range of organic semiconductors. The applicability and flexibility demonstrated by the sol gel silica dielectrics on plastic substrate is particular appealing for large area printed electronics applications. Fundamental understanding of the molecular ordering and interactions investigated in this study will further contribute to optimizing device performance and deployment of these materials and devices in printed electronics applications.

Chapter 7 RECOMMENDATIONS FOR FUTURE WORK

Stemming from this thesis study, the following possibilities for future work are recommended to further exploit the advantages of the sol-gel silica as gate dielectric in organic field-effect transistors.

7.1 Printed organic semiconductor circuits based on sol gel silica film

After successfully making discrete OFETs, the next natural step would be to integrate them in functional logic blocks and ultimately make circuits enabled by sol gel silica dielectrics. Initial experiments in the deployment of sol gel silica in bottom contact organic semiconductor (Pseudo – PMOS) inverter configuration have been carried out (Figure 7.1). Conventional lithography processing methodology was employed to fabricate sol gel silica dielectric modified SiNx based inverter with enhancement loads. The preliminary result shows a functional inverter, achieving gain of 2.5 matching the theoretical gain. Future suggested exploration includes process integration with printing methods such as screen printing and inkjet printing to print and pattern the tri-layer sol gel silica in one step to demonstrate low voltage operating pseudo PMOS inverter.

Figure 7. 1:(Left) The voltage transfer characteristics (VTC) of the inverter with sol-gel silica (50 nm) modification on 100nm thick SiNx. (Right) The transient response of the inverter with input pulsing of 1.35 kHz square wave.

7.2 Investigation of the energy alignment of the organic semiconductor on sol gel

silica

The investigation of the electronic properties at the interface between the pentacene on sol gel silica is important to provide additional information to understand the enhanced device mobility and comprehend the charge transport which takes place primary at the dielectric-organic semiconductor interface. The chemical reaction and charge transfer could be probed using X-ray photoelectron spectroscopy (XPS), while ultraviolet photoelectron spectroscopy (UPS) is useful to monitor the changes in valence band structure, work function and ionization potential of the semiconductor. Earlier literature has tried to study the interface between oligomer and Si or SiO₂. Although band bending was detected between oligomer and Si but energy level alignment at the oligomer - SiO₂ interface was not examined due to the charging effect of the 200Å thick SiO₂ during the photoelectron measurement. It is suggested that dilution methodologies be used to form

an ultrathin ($<5\text{nm}$) layer to minimize the charging effect and study the electronic states of organic semiconductors on sol gel silica.

7.3 Densification studies of sol gel silica by means of UV exposure

The stacked dielectric (trilayer) approach has been shown as the preferred way for the sol-gel silica to be deployed on flexible substrates. Most of the processing done thus far has been with spin coating and thermal annealing. For compatibility with large area processing, UV patternability will be an added advantage; and may be achieved with addition of photo acid generators. Another possibility to be considered would be the densification or skin formation on top of the sol gel silica films using UV exposure that will provide effects similar to rapid thermal processing and would yet be compatible with roll-to-roll processing of plastic electronics.

REFERENCES

- [1] C. D. Dimitrakopoulos and P. R. L. Malenfant, "Organic thin film transistors for large area electronics," *Adv. Mater.*, vol. 14, p. 99, 2002.
- [2] G. Horowitz, "Organic thin film transistors: From theory to real devices," *J. Mater. Res.*, vol. 19, p. 1946, 2004.
- [3] A. Dodabalapur, H. E. Katz, L. Torsi, and R. C. Haddon, "Organic Heterostructure Field-Effect Transistors," *Science*, vol. 269, p. 1560, 1995.
- [4] A. Dodabalapur, L. Torsi, and H. E. Katz, "Organic Transistors: Two-Dimensional Transport and Improved Electrical Characteristics," *Science*, vol. 268, p. 270, 1995.
- [5] Z. Bao, Y. Feng, A. Dodabalapur, V. R. Raju, and A. J. Lovinger, "High-Performance Plastic Transistors Fabricated by Printing Techniques," *Chem. Mater.*, vol. 9, p. 1299, 1997.
- [6] D. Knipp, R. A. Street, and A. R. Völkel, "Morphology and electronic transport of polycrystalline pentacene thin-film transistors," *Appl. Phys. Lett.*, vol. 82, p. 3907, 2003.
- [7] P. Fontaine, D. Goguenheim, D. Deresmes, D. Vuillaume, M. Garet, and F. Rondelez, "Octadecyltrichlorosilane monolayers as ultrathin gate insulating films in metal-insulator-semiconductor devices," *Appl. Phys. Lett.*, vol. 62, p. 2256, 1993.
- [8] J. Collet, O. Tharaud, A. Chapoton, and D. Vuillaume, "Low-voltage, 30 nm channel length, organic transistors with a self-assembled monolayer as gate insulating films," *Appl. Phys. Lett.*, vol. 76, p. 1941, 2000.
- [9] M.-H. Yoon, A. Facchetti, and T. J. Marks, "Octadecyltrichlorosilane monolayers as ultrathin gate insulating films in metal-insulator-semiconductor devices," *Proc. Natl. Acad. Sci. U.S.A.*, vol. 102, p. 4678, 2005.
- [10] A. Facchetti, M.-H. Yoon, and T. J. Marks, "Gate dielectrics for organic field-effect transistors: New opportunities for organic electronics," *Adv. Mater.*, vol. 17, p. 1705, 2005.
- [11] C. D. Dimitrakopoulos, I. Kyminis, S. Purushothaman, D. A. Neumayer, P. R. Duncombe, and R. B. Laibowitz, "Low-Voltage, High-Mobility Pentacene Transistors with Solution-Processed High Dielectric Constant Insulators," *Adv. Mater.*, vol. 11, p. 1372, 1999.
- [12] C. D. Dimitrakopoulos, S. Purushothaman, J. Kyminis, A. Callegari, and J. M. Shaw, "Low-Voltage Organic Transistors on Plastic Comprising High-Dielectric Constant Gate Insulators," *Science*, vol. 283, pp. 822-824, 1999.
- [13] J. Veres, S. Ogier, and G. Llyod, "Gate Insulators in Organic Field-Effect Transistors," *Chem. Mater.*, vol. 16, p. 4543, 2004.
- [14] B. S. Ong, Y. Wu, P. Liu, and S. Gardner, "High-Performance Semiconducting Polythiophenes for Organic Thin-Film Transistors," *J. Am. Chem. Soc.*, vol. 126, p. 3378, 2004.
- [15] Y. Wu, Y. Li, S. Gardner, and B. S. Ong, "Indolo[3,2-*b*]carbazole-based thin-film transistors with high mobility and stability," *J. Am. Chem. Soc.*, vol. 127, p. 614, 2005.
- [16] J. A. Letizia, A. Facchetti, C. L. Stern, M. A. Ratner, and T. J. Marks, "High electron mobility in solution-cast and vapor-deposited phenacyl-quarterthiophene-

- based field-effect transistors: Toward n-type polythiophenes," *J. Am. Chem. Soc.*, vol. 127, p. 13476, 2005.
- [17] M. L. Tang, T. Okamoto, and Z. Bao, "High-performance organic semiconductors: Asymmetric linear acenes containing sulphur," *J. Am. Chem. Soc.*, vol. 128, p. 16002, 2006.
- [18] R. J. Kline, D. M. DeLongchamp, D. A. Fischer, E. K. Lin, L. J. Richter, M. L. Chabiny, M. F. Toney, M. Heeney, and I. McCulloch, "Critical role of side-chain attachment density on the order and device performance of polythiophenes," *Macromolecules*, vol. 40, p. 7960, 2007.
- [19] H. E. Katz, X. M. Hong, A. Dodabalapur, and R. Sarpeshkar, "Polarizable gate organic field-effect transistors," *J. Appl. Phys.*, vol. 91, p. 1572, 2002.
- [20] J. Takeya, T. Nishikawa, T. Takenobu, S. Kobayashi, Y. Iwasa, T. Mitani, C. Goldmann, C. Krellner, and B. Batlogg, "Effects of polarized organosilane self-assembled monolayers on organic single-crystal field-effect transistors," *Appl. Phys. Lett.*, vol. 85, p. 5078, 2004.
- [21] C. Yang, K. Shin, S. Y. Yang, H. Jeon, D. Choi, D. S. Chung, and C. E. Park, "Low-voltage organic transistors on a polymer substrate with an aluminum foil gate fabricated by a laminating and electropolishing process," *Appl. Phys. Lett.*, vol. 89, p. 153508, 2006.
- [22] M.-H. Yoon, C. Kim, A. Facchetti, and T. J. Marks, "Gate dielectric chemical structure-organic field-effect transistor performance correlations for electron, hole, and ambipolar organic semiconductors," *J. Am. Chem. Soc.*, vol. 128, p. 12851, 2006.
- [23] J. Veres, S. Ogier, S. W. Leeming, D. C. Cupertino, and S. M. Khaffaf, "Low-k Insulators as the Choice of Dielectrics in Organic Field-Effect Transistors," *Adv. Funct. Mater.*, vol. 13, p. 199, 2003.
- [24] Y. Jang, D. H. Kim, Y. D. Park, J. H. Cho, M. Hwang, and K. Cho, "Influence of the dielectric constant of a polyvinyl phenol insulator on the field-effect mobility of a pentacene-based thin-film transistor," *Applied Physics Letters*, vol. 87, pp. 152105-3, 2005.
- [25] C. Jung, A. Maliakal, A. Sidorenko, and T. Siegrist, "Pentacene-based thin film transistors with titanium oxide-polystyrene/polystyrene insulator blends: High mobility on high K dielectric films," *Applied Physics Letters*, vol. 90, pp. 062111-3, 2007.
- [26] A. F. Stassen, R. W. de Boer, N. N. Iosad, and A. F. Morpurgo, "Influence of the gate dielectric on the mobility of rubrene single-crystal field-effect transistors," *Appl. Phys. Lett.*, vol. 85, p. 3899, 2004.
- [27] M. Pope and C. E. Swenberg, *Electronic Processes in Organic Crystals and Polymers*, 2nd ed. New York: Oxford University Press, 1999.
- [28] C. R. Kagan, D. B. Mitzi, and C. D. Dimitrakopoulos, "Organic-Inorganic Hybrid Materials as Semiconducting Channels in Thin-Film Field-Effect Transistors," *Science*, vol. 286, p. 945, 1999.
- [29] R. H. Friend, R. W. Gymer, A. B. Holmes, J. H. Burroughes, R. N. Marks, C. Taliani, D. D. C. Bradley, D. A. Dos Santos, J. L. Bredas, M. Logdlund, and W. R. Salaneck, "Electroluminescence in conjugated polymers," *Nature*, vol. 397, p. 121, 1999.
- [30] J. E. Anthony, J. S. Brooks, D. L. Eaton, and S. R. Parkin, "Functionalized pentacene: Improved electronic properties from control of solid-state order," *J. Am. Chem. Soc.*, vol. 123, p. 9482, 2001.

- [31] Y. Wu, P. Liu, S. Gardner, and B. S. Ong, "Poly(3,3"-dialkylterthiophene)s: Room-temperature, solution-processed, high-mobility semiconductors for organic thin-film transistors," *Chem. Mater.*, vol. 17, p. 221, 2005.
- [32] R. Ruiz, D. Choudhary, B. Nickel, T. Toccoli, K. C. Chang, A. C. Mayer, P. Clancy, J. M. Blakely, R. L. Headrick, S. Iannotta, and G. G. Malliaras, "Pentacene thin film growth," *Chem. Mater.*, vol. 16, p. 4497, 2004.
- [33] L. F. Drummy, C. Kübel, D. Lee, A. White, and D. C. Martin, "Direct imaging of defect structures in pentacene nanocrystals," *Adv. Mater.*, vol. 14, p. 54, 2002.
- [34] G. Horowitz, "Organic Field-Effect Transistors," *Adv. Mater.*, vol. 10, p. 365, 1998.
- [35] T. Kelley, "High-performance pentacene transistors," in *Organic electronics: Materials, manufacturing and applications*, H. Klauk, Ed. Weinheim: Wiley-VCH, 2006.
- [36] T. W. Kelley, D. V. Muyres, P. F. Baude, T. P. Smith, and T. D. Jones, "High Performance Organic Thin Film Transistors," *MRS Symp. Proc.*, vol. 771, p. 169, 2003.
- [37] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, S. Ponomarenko, S. Kirchmeyer, and W. Weber, "Relationship Between Molecular Structure and Electrical Performance of Oligothiophene Organic Thin Film Transistors," *Adv. Mater.*, vol. 15, p. 917, 2003.
- [38] X. Peng, G. Horowitz, D. Fichou, and F. Garnier, "All-organic thin-film transistors made of alpha-sexithienyl semiconducting and various polymeric insulating layers," *Appl. Phys. Lett.*, vol. 57, p. 2013, 1990.
- [39] Frank-J., Meyer zu Heringdorf, M. C. Reuter, and R. M. Tromp, "Growth dynamics of pentacene thin films," *Nature*, vol. 412, pp. 517-520, 2001.
- [40] H. Sirringhaus, P. J. Brown, R. H. Friend, M. M. Nielsen, K. Bechgaard, B. M. W. Langeveldvoss, A. J. H. Spiering, R. A. J. Janssen, E. J. Meijer, P. Herwig, and D. M. de Leeuw, "Two-dimensional charge transport in self-organized, high-mobility conjugated polymers " *Nature*, vol. 401, p. 685, 1999.
- [41] Y. Wu, P. Liu, S. Gardner, and B. S. Ong, "Room Temperature, solution processed, high mobility semiconductors for organic thin film transistors," *Chem. Mater.*, vol. 17, p. 221, 2005.
- [42] I. McCulloch, M. Heeney, C. Bailey, K. Genevicius, I. MacDonald, M. Shkunov, D. Sparrowe, S. Tierney, R. Wagner, W. Zhang, M. L. Chabinyc, R. J. Kline, M. D. McGehee, and M. F. Toney, "Liquid-crystalline semiconducting polymers with high charge-carrier mobility," *Nat. Mat.*, vol. 5, p. 328, 2006.
- [43] H. Usta, G. Lu, A. Facchetti, and T. J. Marks, "Dithienosilole- and Dibenzosilole-Thiophene Copolymers as Semiconductors for Organic Thin-Film Transistors," *J. Am. Chem. Soc.*, vol. 128, p. 9034, 2006.
- [44] J. Tate, J. A. Rogers, C. D. W. Jones, B. Vyas, D. W. Murphy, W. J. Li, Z. Bao, R. E. Slusher, A. Dodabalapur, and H. E. Katz, "Anodization and Microcontact Printing on Electroless Silver; Solution Based Fabrication Procedures for Low Voltage Electronic Systems with Organic Active Components," *Langmuir*, vol. 16, p. 6054, 2000.
- [45] A. R. Murphy, J. M. Frechet, P. Chang, J. Lee, and V. Subramanian, "Organic Thin Film Transistors from a Soluble Oligothiophene Derivative Containing Thermally Removable Solubilizing Groups," *J. Am. Chem. Soc.*, vol. 126, p. 1596, 2004.
- [46] G. Barbarella, M. Zambianchi, L. Antolini, P. Ostoj, P. Maccagnani, A. Bongini, E. A. Marseglia, E. Tedesco, G. Gigli, and R. Cingolani, "Solid-state

- conformation, molecular packing and electrical and optical properties of processable b-methylated sexithiophenes," *J. Am. Chem. Soc.*, vol. 121, p. 8920, 1999.
- [47] H. Meng, M. Bendikov, G. Mitchell, R. Helgeson, F. Wudl, Z. Bao, T. Siegrist, C. Kloc., and C. H. Chen, "Tetramethylpentacene: Remarkable Absence of Steric Effect on Field Effect Mobility," *Adv. Mater.*, vol. 15, p. 1090, 2003.
 - [48] R. Parashkov, E. Becker, G. Ginev, T. Riedl, H.-H. Johannes, and W. Kowalsky, "All-organic thin-film transistors made of poly(3-butylthiophene) semiconducting and various polymeric insulating layers," *J. Appl. Phys.*, vol. 95, p. 1594, 2004.
 - [49] C. Bartic, H. Jansen, A. Campitelli, and S. Borghs, "Ta₂O₅ as gate dielectric material for low-voltage organic thin-film transistors," *Org. Electron.*, vol. 3, p. 65, 2002.
 - [50] G. Wang, D. Moses, A. J. Heeger, H.-M. Zhang, M. Narasimhan, and R. E. Demaray, "Poly(3-hexylthiophene) field-effect transistors with high dielectric constant gate insulator," *J. Appl. Phys.*, vol. 95, p. 316, 2004.
 - [51] L. A. Majewski, R. Schroder, M. Grell, P. A. Glarvey, and M. L. Turner, "High capacitance organic field-effect transistors with modified gate insulator surface," *J. Appl. Phys.*, vol. 96, p. 5781, 2004.
 - [52] H. Klauk, M. Halik, U. Zschieschang, G. Schmid, W. Radlik, and W. Weber, "High-mobility polymer gate dielectric pentacene thin film transistors," *J. Appl. Phys.*, vol. 92, p. 5259, 2002.
 - [53] W. H. Ha, M. H. Choo, and S. Im, "Electrical properties of Al₂O₃ film deposited at low temperatures " *J. Non-Cryst. Solids*, vol. 303, p. 78, 2002.
 - [54] J. Lee, J. H. Kim, and S. Im, "Pentacene thin-film transistors with Al₂O_{3+x} gate dielectric films deposited on indium-tin-oxide glass," *Appl. Phys. Lett.*, vol. 83, p. 2689, 2003.
 - [55] Y. Iino, Y. Inoue, Y. Fujisaki, H. Fujikake, H. Sato, M. Kawakita, S. Tokito, and H. Kikuchi, "Organic Thin-Film Transistors on a Plastic Substrate with Anodically Oxidized High-Dielectric-Constant Insulators," *Jpn. J. Appl. Phys.*, vol. 42, p. 299, 2003.
 - [56] S. J. Kang, K. B. Chung, D. S. Park, H. J. Kim, Y. K. Choi, M. H. Jang, M. Noh, and C. N. Whang, "Fabrication and characterization of the pentacene thin film transistor with a Gd₂O₃ gate insulator," *Synth. Met.*, vol. 146, p. 351, 2004.
 - [57] I. Rutenberg, O. A. Scherman, R. H. Grubbs, W. Jiang, E. Garfunkel, and Z. Bao, "Synthesis of polymer dielectric layers for organic thin film transistors via surface-initiated ring- opening metathesis polymerization," *J. Am. Chem. Soc.*, vol. 126, p. 4062, 2004.
 - [58] F.-C. Chen, C.-W. Chu, J. He, Y. Yang, and J.-L. Lin, "Organic thin-film transistors with nanocomposite dielectric gate insulator," *Appl. Phys. Lett.*, vol. 85, p. 3295, 2004.
 - [59] M.-H. Yoon, H. Yan, A. Facchetti, and T. J. Marks, "Low-voltage organic field-effect transistors and inverters enabled by ultrathin cross-linked polymers as gate dielectrics," *J. Am. Chem. Soc.*, vol. 127, p. 10388, 2005.
 - [60] L. A. Majewski, R. Schroeder, and M. Grell, "One Volt Organic Transistor," *Adv. Mater.*, vol. 17, p. 192, 2005.
 - [61] A. R. Brown, A. Pomp, C. M. Hart, and D. M. de Leeuw, "Logic Gates Made from Polymer Transistors and Their Use in Ring Oscillators " *Science*, vol. 270, p. 972, 1995.

- [62] A. Afzali, C. D. Dimitrakopoulos, and T. L. Breen, "High-performance, solution-processed organic Thin-Film transistors from a novel pentacene precursor," *J. Am. Chem. Soc.*, vol. 124, p. 8812, 2002.
- [63] L. A. Majewski, R. Schroeder, and M. Grell, "Flexible high capacitance gate insulators for organic field effect transistors," *J. Phys. D: Appl. Phys.*, vol. 37, p. 21, 2004.
- [64] V. C. Sundar, J. Zaumseil, V. Podzorov, E. Menard, R. L. Willet, T. Someya, M. E. Gershenson, and J. A. Rogers, "Elastomeric transistor stamps: Reversible probing of charge transport in organic crystals," *Science*, vol. 303, p. 1644, 2004.
- [65] L.-L. Chua, P. K.-H. Ho, H. Sirringhaus, and R. H. Friend, "High-stability ultrathin spin-on benzocyclobutene gate dielectric for polymer field-effect transistors," *Appl. Phys. Lett.*, vol. 84, p. 3400, 2004.
- [66] J. Kastner, J. Paloheimo, and H. Kuzmany, *Solid State Sciences*. New York: Springer, 1993.
- [67] R. C. Haddon, A. S. Perel, R. C. Morris, T. T. M. Palstra, and A. F. C. Hebard, "C₆₀ thin film transistors," *Appl. Phys. Lett.*, vol. 67, p. 121, 1995.
- [68] C. P. Jarret, K. Pichler, R. Newbould, and R. H. Friend, "Transport studies in C₆₀ and C₆₀/C₇₀ thin films using metal-insulator-semiconductor field-effect transistors," *Synth. Met.*, vol. 77, p. 35, 1996.
- [69] S. Kobayashi, T. Takenobu, S. Mori, A. Fujiwara, and Y. Iwasa, "Fabrication and characterization of C₆₀ thin-film transistors with high field-effect mobility," *Appl. Phys. Lett.*, vol. 82, p. 4581, 2003.
- [70] T. D. Anthopoulos, F. B. Kooistra, H. J. Wondergem, D. Kronholm, J. C. Hummelen, and D. M. de Leeuw, "Air-stable n-channel organic transistors based on a soluble C₈₄ fullerene derivative," *Adv. Mater.*, vol. 18, p. 1679, 2006.
- [71] J. Yuan, J. Zhang, J. Wang, X. Yan, D. Yang, and W. Xu, "Bottom-contact organic field-effect transistors having low-dielectric layer under source and drain electrodes," *Appl. Phys. Lett.*, vol. 82, p. 3967, 2003.
- [72] A. Facchetti, Y. Deng, A. Wang, Y. Koide, H. Sirringhaus, T. J. Marks, and R. H. Friend, "Tuning the Semiconducting Properties of Sexithiophene by α,ω -Substitution - α,ω -Diperfluorohexylsexithiophene: The First n-Type Sexithiophene for Thin-Film Transistors," *Angew. Chem. Int. Ed.*, vol. 39, p. 4547, 2000.
- [73] T. M. Pappenfus, R. J. Chesterfield, C. D. Frisbie, K. R. Mann, J. Casado, J. D. Raff, and L. L. Miller, "A pi-Stacking Terthiophene-Based Quinodimethane Is an n-Channel Conductor in a Thin Film Transistor," *J. Am. Chem. Soc.*, vol. 124, p. 4184, 2002.
- [74] H. E. Katz, A. J. Lovinger, J. Johnson, C. Kloc., T. Siegrist, W. J. Li, Y.-Y. Lin, and A. Dodabalapur, "A soluble and air-stable organic semiconductor with high electron mobility," *Nature*, vol. 404, p. 478, 2000.
- [75] J. E. Anthony, D. L. Eaton, and S. R. Parkin, "A Roadmap to Stable, Soluble, Easily Crystallized Pentacene Derivatives," *Org. Lett.*, vol. 4, p. 15, 2002.
- [76] W. Gregor and W. Christof, "Growth of Aromatic Molecule on Solid Substrates for Applications in Organic Electronics," *J. Mater. Res.*, vol. 19, p. 1889, 2004.
- [77] C. D. Dimitrakopoulos, A. R. Brown, and A. Pomp, "Molecular beam deposited thin films of pentacene for organic field effect transistor applications," *J. Appl. Phys.*, vol. 80, p. 2501, 1996.
- [78] R. B. Campbell, J. M. Robertson, and J. Trotter, "The crystal structure of hexacene, and a revision of the crystallographic data for tetracene and pentacene," *Acta Cryst.*, vol. 15, p. 289, 1962.

- [79] I. P. M. Bouchoms, W. A. Schoonveld, J. Vrijmoeth, and T. M. Klapwijk, "Morphology identification of the thin film phases of vacuum evaporated pentacene on SiO₂ substrates," *Synthetic Metals*, vol. 104, p. 175, 1999.
- [80] J. L. Brédas, J. P. Calbert, D. A. Da Silva Filho, and J. Cornil, "Organic semiconductors: A theoretical characterization of the basic parameters governing charge transport," *Proc. Natl. Acad. Sci. U.S.A.*, vol. 99, p. 5804, 2002.
- [81] E. A. Silinsh and V. Capek, *Organic molecular crystals*. New York: AIP Press, 1994.
- [82] R. Ruiz, "Thickness dependence of mobility in pentacene thin film transistors," *Adv. Mater.*, vol. 17, p. 1795, 2005.
- [83] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. USA: John Wiley & Sons 1981.
- [84] S. M. Sze, *Semiconductors Devices: Physics and Technology*, 2nd ed. New York: Wiley, 2002.
- [85] G. Horowitz, "Organic transistors," in *Organic electronics: Materials, manufacturing and applications*, H. Klauk, Ed. Weinheim: Wiley-VCH, 2006.
- [86] D. Gamota, P. Brazis, K. Kalyanasundaram, and J. Zhang, "Printed Organic & Molecular Electronics," *Kluwer Academic Publishers*, 2004.
- [87] G. Wilk, R. Wallace, and J. Anthony, "High k gate dielectric: Current status and materials properties considerations," *J. Appl. Phys.*, vol. 89, pp. 5243-5275, 2001.
- [88] I N Hulea, S Fratini, H Xie, C L Mulder, N N Iossad, G Rastelli, S Ciuchi, and A. F. Morpurgo, "Tunable Fröhlich polarons in organic single-crystal transistors," *Nat. Mat.*, vol. 5, p. 982, 2006.
- [89] F. M. Li, A. Nathan, Y. L. Wu, and B. S. Ong, "Organic thin film transistor integration using silicon nitride gate dielectric," *Appl. Phys. Lett.*, vol. 90, p. 133514, 2007.
- [90] R. Schroeder, L. A. Majewsko, and M. Grell, "High Performance Organic Transistors Using Solution-Processed Nanoparticles Filled High k Polymer Gate Insulator," *Adv. Mater.*, vol. 17, pp. 1535-1539, 2005.
- [91] Z. Bao, V. Kuck, J. A. Rogers, and M. A. Paczkowski, "Silsesquioxane Resins as High-Performance Solution Processible Dielectric Materials for Organic Transistor Applications," *Adv. Funct. Mater.*, vol. 12, pp. 526-531, 2002.
- [92] L. L. Hench and J. K. West, "The sol-gel process," *Chem. Rev.*, vol. 90, p. 33, 1990.
- [93] Y.-Y. Lin, D. J. Gundlach, S. F. Nelson, and T. N. Jackson, "Pentacene-based organic thin-film transistors," *IEEE Trans. Elect. Dev.*, vol. 44, p. 1325, 1997.
- [94] D. J. Gundlach, J. E. Royer, S. K. Park, S. Subramanian, O. D. Jurchescu, B. H. Hamdani, A. J. Kline, L. C. Teague, O. Kirillov, C. A. Richter, J. G. Kushmerick, L. J. Richter, S. R. Parkin, T. N. Jackson, and J. E. Anthony, "Contact-induced crystallinity for high performance soluble acene-based transistors and circuits," *Nat. Mat.*, vol. 7, p. 216, 2008.
- [95] L. L. Hench and J. K. West, "The Sol gel process" *Chem. Rev.*, vol. 90, p. 33, 1990.
- [96] J. R. Martinez, F. Ruiz, Y. V. Vorobiev, F. Péres-Robles, and J. González-Hernández, "Infrared spectroscopy analysis of the local atomic structure in silica prepared by sol-gel," *J. Chem. Phys.*, vol. 109, p. 7511, 1998.
- [97] A. Bertoluzza, C. Fagnano, M. A. Morelli, V. Gottardi, and M. Guglielmi, "Raman and infrared spectra on silica gel evolving toward glass," *J. Non-Cryst. Solids*, vol. 48, p. 117, 1982.

- [98] L. Mascia and Z. Zhang, "Dense outer layers formed by plasma treatments of silica coatings produced by the sol-gel method," *J. Mater. Sci.*, vol. 32, p. 667, 1997.
- [99] D. K. Hwang, Jeong-M. Choi, J. H. Park, J. H. Kim, Eugene Kim, and S. Im, "Low-voltage pentacene thin-film transistor with a polymer/YOx/polymer triple-layer dielectric on a plastic substrate," *Electrochem. Solid-state Lett.*, vol. 10, pp. H117-H119, 2007.
- [100] S. Yu, T. K. S. Wong, X. Hu, and M. S. Yong, "Dielectric and Mechanical Properties of Surface Modified Organosilicate Films," *J. Sol-Gel Sci. and Tech.*, vol. 35, p. 69, 2005.
- [101] B. I., "Characterization of Nitride coating by XPS," *Surface & Coatings Technology*, vol. 151-152, pp. 194-203, 2002.
- [102] S. M. Hu and L. V. Gregor, "Silicon Nitride Films by Reactive Sputtering," *J. Electrochem. Soc.: Solid State Science*, vol. 114, p. 826, 1967.
- [103] H. R. Kim, H.-H. Park, S.-H. Hyun, and G. Y. Yeom, "Effect of O₂ plasma treatment on the properties of SiO₂ aerogel film," *Thin Solid Films*, vol. 332, pp. 444-448, 1998.
- [104] C. Huang, J. E. West, and H. E. Katz, "Organic field-effect transistors and unipolar logic gates on charged electrets from spin-on organosilsesquioxane resins," *Adv. Funct. Mater.*, vol. 17, p. 142, 2007.
- [105] Daniele Braga and G. Horowitz, "High Performance Organic Field Effect Transistors," *Adv. Mater.*, vol. 21, pp. 1473-1486, 2009.
- [106] T. Sekitani, Y. Kato, S. Iba, H. Shinaoka, T. Someya, T. Sakurai, and S. Takagi, "Bending experiment on pentacene field-effect transistors on plastic films," *Applied Physics Letters*, vol. 86, pp. 073511-3, 2005.
- [107] D. Knipp and R. A. Street, "Pentacene thin film transistors on large area compatible gate dielectrics," *J. Non-Cryst. Solids*, vol. 338-340, pp. 595-598, 2004.
- [108] S. Y. Yang, K. Shin, and C. E. Park, "The Effect of Gate-Dielectric Surface Energy on Pentacene Morphology and Organic Field-Effect Transistor Characteristics," *Advanced Functional Materials*, vol. 15, pp. 1806-1814, 2005.
- [109] R. W. G. Wyckoff, *Crystal Structures*, 2nd ed. New York: Interscience, 1971.
- [110] R. Hosemann and A. M. Hindeleh, "Structure of crystalline and paracrystalline condensed matter," *J. Macromol. Sci. Phys.*, vol. B34, p. 327, 1995.
- [111] A. M. Hindeleh and R. Hosemann, "Paracrystals representing the physical state of matter," *J. Phys. C: Solid State Phys.*, vol. 21, p. 4155, 1988.
- [112] M. B. Casu, P. Cosseddu, D. Batchelor, A. Bonfiglio, and E. Umbach, "A high resolution near-edge x-ray absorption fine structure investigation of the molecular orientation in the pentacene/poly(3,4-ethylenedioxythiophene): poly(styrenesulfonate) pentacene system," *J. Chem. Phys.*, vol. 128, p. 014705, 2008.
- [113] M. Alagia, C. Baldacchini, M. G. Betti, F. Bussolotti, V. Carravetta, U. Ekstrom, C. Mariani, and S. Stranges, *J. Chem. Phys.*, vol. 122, 2005.
- [114] Stohr, "NEXAFS spectroscopy," *Springer-Verlag*, 1992.
- [115] F. Zheng, B.-N. Park, S. Seo, P. G. Evans, and F. J. Himpsel, "Orientation of pentacene molecules on SiO₂: From a monolayer to the bulk," *The Journal of Chemical Physics*, vol. 126, pp. 154702-6, 2007.
- [116] M. Cazayous, A. Sacuto, G. Horowitz, P. Lang, A. Zimmers, and R. P. S. M. Lobo, "Iodine insertion in pentacene thin films investigated by infrared and Raman spectroscopy," *Phys. Rev. B*, vol. 70, p. 081309, 2004.

- [117] H. L. Cheng, S. Mai, W. Y. Chou, and L. R. Chang, "Influence of molecular structure and microstructure on device performance of polycrystalline pentacene thin-film transistors," *Appl. Phys. Lett.*, vol. 90, p. 171926, 2007.
- [118] H. L. Cheng, W. Y. Chou, C. W. Kou, F. C. Tang, and Y. W. Wang, "Electric field-induced structural changes in pentacene-based organic thin-film transistors studied by *in situ* micro-Raman spectroscopy," *Appl. Phys. Lett.*, vol. 88, p. 161918, 2006.
- [119] L. Farina, A. Brillante, R. G. Della Valle, E. Venuti, M. Amboage, and K. Syassen, "Pressure-induced phase transition in pentacene," *Chem. Phys. Lett.*, vol. 375, p. 490, 2003.
- [120] M. Grobosch, R. Schuster, T. Pichler, and M. Knupfer, "Analysis of the anisotropy of excitons in pentacene single crystals using reflectivity measurements and electron energy-loss spectroscopy," *Phys. Rev. B*, vol. 74, p. 155202, 2006.
- [121] H. R. Kim, H. H. Park, S. H. Hyun, and G. Y. Yeom, *Thin Solid Films*, vol. 332, p. 444, 1999.
- [122] S. Jeong, D. Kim, B. K. Park, S. Lee, and J. Moon, "Influence of silanol groups on the electrical performance of organic thin film transistors utilizing organosiloxane-based organic-inorganic hybrid dielectrics," *Nanotechnology*, vol. 18, p. 025204, 2007.
- [123] J.-J. Kim, H.-H. Park, and S.-H. Hyun, "The effects of plasma treatment on SiO₂ aerogel film using various reactive (O₂, H₂, N₂) and non reactive (He, Ar) gases," *Thin Solid Films*, vol. 377-378, pp. 525-529, 2000.
- [124] J.-J. Kim, H.-H. Park, and S.-H. Hyun, "The effect of plasma treatment on SiO₂ aerogel film using various reactive (O₂, H₂, N₂) and non-reactive (He, Ar) gases," *Thin Solid Films*, vol. 377-378, pp. 525-529, 2000.
- [125] T. Jung, A. Dodabalapur, R. Wenz, and S. Mohapatra, "Moisture induced surface polarization in a poly(4-vinyl phenol) dielectric in an organic thin-film transistor," *Appl. Phys. Lett.*, vol. 87, p. 182109, 2005.
- [126] Y. Qiu, Y. Hu, G. Dong, L. Wang, J. Xie, and Y. Ma, "H₂O effect on the stability of organic thin-film field-effect transistors," *Appl. Phys. Lett.*, vol. 83, p. 1644, 2003.
- [127] G. Horowitz and M. E. Hajlaoui, "Grain size dependent mobility in polycrystalline organic field-effect transistors," *Synthetic Metals*, vol. 122, pp. 185-189, 2001.
- [128] A. D. Carlo, F. Piacenza, A. Bolognesi, B. Stadlober, and H. Maresch, "Influence of grain sizes on the mobility of organic thin-film transistors," *Appl. Phys. Lett.*, vol. 86, p. 263501, 2005.
- [129] C. R. Kagan and P. Andry, *Thin-Film Transistors*, 1st ed. New York: Marcel Dekker, 2003.
- [130] M. McDowell, I. G. Hill, J. E. McDermott, S. L. Bernasek, and J. Schwartz, "Improved organic thin-film transistor performance using novel self-assembled monolayers," *Applied Physics Letters*, vol. 88, p. 073505, 2006.
- [131] J. Lee, J. H. Kim, S. Im, and D.-Y. Jung, "Threshold voltage change due to organo-inorganic interface in pentacene thin-film transistors," *Journal of Applied Physics*, vol. 96, pp. 2301-2304, 2004.
- [132] S. Steudel, S. D. Vusser, S. D. Jonger, D. Janssen, S. Verlaak, J. Genoe, and P. Heremans, "Influence of the dielectric roughness on the performance of pentacene transistors," *Appl. Phys. Lett.*, vol. 85, pp. 4400-4402, 8 November 2004.

- [133] G. Gu, M. G. Kane, J. E. Doty, and A. H. Firester, "Electron traps and hysteresis in pentacene-based organic thin-film transistors," *Appl. Phys. Lett.*, vol. 87, p. 243512, 2005.
- [134] S. E. Fritz, T. W. Kelley, and C. D. Frisbie, "Effect of Dielectric Roughness on Performance of Pentacene TFTs and Restoration of Performance with a Polymeric Smoothing Layer," *J. Phys. Chem. B*, vol. 109, p. 10574, 2005.
- [135] Y. Wu, P. Liu, and B. S. Ong, "Organic thin-film transistors with poly(methyl silsesquioxane) modified dielectric interfaces," *Applied Physics Letters*, vol. 89, p. 013505, 2006.
- [136] M. Shtein, J. Mapel, J. B. Benziger, and S. R. Forrest, "Effects of film morphology and gate dielectric surface preparation on the electrical characteristics of organic-vapor-phase-deposited pentacene thin-film transistors," *Appl. Phys. Lett.*, vol. 81, p. 268, 2002.
- [137] S. Schiefer, M. Huth, A. Dobrinevski, and B. Nickel, "Determination of the crystal structure of substrate-induced pentacene polymorphs in fiber structured thin films," *J. Am. Chem. Soc.*, vol. 129, p. 10316, 2007.
- [138] M. D. Curtis, J. Cao, and J. W. Kampf, "Solid-state packing of conjugated oligomers: From π -stacks to the herringbone structure," *J. Am. Chem. Soc.*, vol. 126, p. 4318, 2004.
- [139] P. Parisse, L. Ottaviano, B. Delley, and S. Picozzi, "First-principles approach to the electronic structure in the pentacene thin film polymorph," *J. Phys.: Condens. Matter.*, vol. 19, p. 106209, 2007.
- [140] S. P. Park, S. S. Kim, J. H. Kim, C. N. Whang, and S. Im, "Optical and luminescence characteristics of thermally evaporated pentacene films on Si," *Appl. Phys. Lett.*, vol. 80, p. 2872, 2002.
- [141] R. He, N. G. Tassi, G. B. Blanchet, and A. Pinczuk, "Fundamental optical recombination in pentacene clusters and ultrathin films," *Appl. Phys. Lett.*, vol. 87, p. 103107, 2005.
- [142] R. A. Marcus, "Electron transfer reactions in chemistry. Theory and experiment " *Rev. Mod. Phys.*, vol. 65, p. 599, 1993.
- [143] N. E. Gruhn, D. A. da Silva Filho, T. G. Bill, M. Malagoli, V. Coropceanu, A. Kahn, and J. L. Brédas, "The vibrational reorganization energy in pentacene: Molecular influences on charge transport," *J. Am. Chem. Soc.*, vol. 124, p. 7918, 2002.
- [144] S. T. Bromley, M. M.-. Torrent, P. Hadley, and C. Rovira, "Importance of intermolecular interactions in assessing hopping mobilities in organic field effect transistors: Pentacene versus dithiophene-tetrathiafulvalene," *J. Am. Chem. Soc.*, vol. 126, p. 6544, 2004.
- [145] D. Knipp, R. A. Street, A. R. Völkel, and J. Ho, "Pentacene thin film transistors on inorganic dielectrics: Morphology, structural properties, and electronic transport," *J. Appl. Phys.*, vol. 93, p. 347, 2003.
- [146] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: Wiley, 1982.
- [147] D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed. vol. Chap. 6. New York: Wiley, 1998.
- [148] S. Y. Park, M. Park, and H. H. Lee, "Cooperative polymer gate dielectrics in organic thin-film transistors," *Appl. Phys. Lett.*, vol. 85, p. 2283, 20 September 2004 2004.
- [149] D. M. Fleetwood, P. S. Winokur, R. A. Reber, T. L. Meisenheimer, J. R. Schwank, M. R. Shaneyfelt, and L. C. Riewe, "Effects of oxide traps, interface traps, and

- border traps on metal-oxide-semiconductor devices," *Journal of Applied Physics*, vol. 73, p. 5058, 1993.
- [150] H. Bassler, *Philos. Mag. A*, vol. 50, 1984.
- [151] R. T., B. M., and H. Sirringhaus, "A quantitative analytical model for static dipolar disorder broadening of the density of states at organic heterointerfaces.," *J. Chem. Phys.*, vol. 128, p. 234905, 2008.
- [152] S. Kobayashi, T. Nishikawa, T. Takenobu, S. Mori, T. Shimoda, T. Mitani, H. Shimotani, N. Yoshimoto, S. Ogawa, and Y. Iwasa, "Control of carrier density by self-assembled monolayers in organic field-effect transistors," *Nat. Mat.*, vol. 3, p. 317, 2004.
- [153] Y. Y. Lin, D. J. Gundlach, S. F. Nelson, and T. N. Jackson, "Stacked pentacene layer organic thin-film transistors with improved characteristics," *IEEE Elect. Dev. Lett.*, vol. 18, p. 606, 1997.
- [154] F. Meyer zu Heringdorf, -J., M. C. Reuter, and R. M. Tromp, "Growth dynamics of pentacene thin films," *Nature*, vol. 412, p. 517, 2001.
- [155] K. Puntambekar, J. Dong, G. Haugstad, and C. D. Frisbie, "Structural and electrostatic complexity at a pentacene/insulator interface," *Adv. Funct. Mater.*, vol. 16, p. 879, 2006.
- [156] Y. Maréchal, *The hydrogen bond and the water molecule: The physics and chemistry of water, aqueous and bio media*. Amsterdam: Elsevier, 2007.
- [157] M. Cazayous, A. Sacuto, G. Horowitz, P. Lang, A. Zimmers, and R. P. S. M. Lobo, "Iodine insertion in pentacene thin films investigated by infrared and Raman spectroscopy," *Physical Review B*, vol. 70, p. 081309, 2004.
- [158] H. L. Cheng, W. Y. Chou, C. W. Kuo, F. C. Tang, and Y. W. Wang, "Electric field-induced structural changes in pentacene-based organic thin-film transistors studied by in situ micro-Raman spectroscopy," *Applied Physics Letters*, vol. 88, pp. 161918-3, 2006.
- [159] C. Yang, J. Yoon, S. H. Kim, K. Hong, D. S. Chung, K. Heo, C. E. Park, and M. Ree, "Bending stress-driven phase transition in pentacene thin film for flexible organic field effect transistors," *Appl. Phys. Lett.*, vol. 92, p. 243305, 2008.

Appendix A- LIST OF ABBREVIATION

AFM	atomic force microscope (microscopy)
C-V	capacitance-voltage
FE	free exciton
FET	field-effect transistors
FT-IR	Fourier transform infrared spectroscopy
FWHM	full-width-at-half-maximum
HOMO	highest occupied molecular orbital
I-V	current-voltage
LUMO	lowest unoccupied molecular orbital
ML	monolayer
MOS	metal oxide semiconductor
MOSFET	MOS field-effect transistor
NEXAFS	Near Edge X-ray Absorption Fine Structures
nm	nanometer
OFET	organic field-effect transistor
ORMOSIL	organically modified silica (silicates)
OSC	organic semiconductor
PaMS	poly(α -methylstyrene)
PET	Polyethylene terephthalate
PL	photoluminescence
PMMA	poly(methyl methacrylate)
PQT	poly(3,3''-didodecylquarterthiophene)
RMS	root-mean-square
RT	room temperature
SG	sol-gel
S-XRD	synchrotron X-ray diffraction
TEM	transmission electron microscope (microscopy)
TOX	thermally grown silica (SiO ₂)
UV	ultraviolet
XPS	X-ray photoelectron spectroscopy

Appendix B- AUTHOR'S PUBLICATION LIST

Journal articles

- (1) The effect of dielectric constant on device mobilities of high performance, flexible organic field effect transistors
H. S. Tan, N. Mathews, T. Cahyadi, F.R. Zhu, S.G. Mhaisalkar, *Applied Physics Letters* 94 (26), 263303 (2009)
- (2) Enhancement of Carrier Mobilities of Organic Semiconductors on Sol-Gel Dielectrics: Investigations of Molecular Organization and Interfacial Chemistry Effects
T. Cahyadi, J. Kassim, **H.S. Tan**, S.R. Kulkarni, B.S. Ong, Y.L. Wu, Z.K. Chen, C.M. Ng, Z.X. Shen, S.G. Mhaisalkar, *ADVANCED FUNCTIONAL MATERIALS*, 19 (3), 378, (2009)
- (3) Integration of ink jet and transfer printing for device fabrication using nanostructured materials
B. Kumar, **H.S.Tan**, N. Ramalingam; S.G. Mhaisalkar, *CARBON*, Volume 47, Issue 1, 321,(2008)
- (4) Solution-processed trilayer inorganic dielectric for high performance flexible organic field effect transistors
H.S. Tan, S.R. Kulkarni, T. Cahyadi, J. Kasim, P.S. Lee, Z.X. Shen, F.R. Zhu, S.G. Mhaisalkar, *Applied Physics Letters* 93, 183503 (2008)
- (5) Low Temperature Processed Inorganic Gate Dielectrics for Plastic Substrate based Organic Field Effect Transistors
H. S. Tan, T. Cahyadi, Z. B. Wang, A. Lohani, Z. Tsakadze, Sam Zhang, F. R. Zhu, and S. G. Mhaisalkar, *IEEE Electron Device Letter*, 29, 698 (2008)
- (6) Electrical mechanism, hysteresis, and ambient performance of sol-gel silica gate dielectrics in pentacene field-effect transistors
T. Cahyadi, **H. S. Tan**, S. G. Mhaisalkar, P. S. Lee, F. Boey, Z. -K. Chen, C. M. Ng, V. R. Rao, and G. J. Qi, *Applied Physics Letters* 91, 242107 (2007)

- (7) Improved pentacene device characteristics with sol-gel SiO₂ dielectric films
T. Cahyadi, **H. S. Tan**, E. B. Namdas, S. G. Mhaisalkar, P. S. Lee, Z. -K. Chen, C. M. Ng, and F. Y. C. Boey. *Organic Electronics* 9, 455 (2007)
- (8) *Solution processable nanoparticles as high-k dielectric for organic field effect transistors* *Organic Electronics*.
Mahshid A., H.S. Tan, Nopphawan P., Nripan. N., Subodh G. Mhaisalkar
Accepted in Organic Electronics (May 2010)

Manuscripts in Preparation

- (1) Enhancement of charge carrier mobilities of organic semiconductor on sol-gel silica dielectrics
- (2) Continuous tuning of threshold voltage of Organic field effect transistors via organic semiconductors blends system

Conference Presentations:

- (1) Solution-Processed Inorganic Dielectric for High Performance Flexible Organic Electronics: Correlation between Enhanced Devices Performance and Molecular Ordering
H.S. Tan, S.R. Kulkarni, T. Cahyadi, J. Kasim, P.S. Lee,, Z.X. Shen, F.R. Zhu, S.G. Mhaisalkar
The MRS Spring Meeting, San Francisco, USA (2009)
- (2) Improved transistor characteristics of p-type and n-type organic semiconductor films on sol-gel silica as gate dielectric
T. Cahyadi, **H.S. Tan**, Z. -B. Wang, S. G. Mhaisalkar, Z. -K. Chen, and C. M. Ng
International Conference on Materials for Advanced Technologies, Singapore (2007)

Awards:

- (1) IEEE Electron Device Society George Smith Awards 2008