Implementation of wireless data collection system

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Implementation of Wireless Data Collection System

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A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Master of Engineering

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SUMMARY

This project is to study the concept of a wireless data collection system, then design and implement a system for the application of monitoring real-time WeiQi game. The system is able to monitor the targeted environment, process signal, transmit data through wireless channel and present received data in an appropriate manner. In addition, the system is capable of handling different applications concurrently.

The overall system is made up of several modules, which include the remote nodes that acquire information from the target, the wireless transmission module, which transmits collected data from remote node to the central station through a radio channel, and the central station that processes received data and acts as management station. The design and implementation for each module are explained in detail in this thesis.

The implementation was completed in two stages. Experiments have been conducted to verify system functionality. Performance of the wireless communication module under different conditions has been studied. The experimental results are discussed in this thesis. It shows that the system generally meets design requirements.

The project is to develop a system for practical applications. Hence, its emphasis is on practical aspects such as circuit design, implementations, troubleshooting, debugging and conducting experiments.

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CHAPTER 1. INTRODUCTION

1.1 Motivation

In the last two decades, rapid advancement of mobile communications technology, personal computing technology and semiconductor technology has been dramatically transforming industrial process management and manufacturing. The transformation helps to improve productivity, increase user convenience, reduce cost and lead to higher efficiency. The technology advancement is also influencing one's life style, turning it into "Digital Life Style", in which one can create, share and enjoy multimedia information in his own personalized virtual space in mobile environment.

Benefited from the advancement of the technologies mentioned above, wireless data collection system is of increasing importance and is widely used for various applications. Wireless data collection system has become faster, more reliable and smaller in size.

The demand for wireless system is forecasted to grow continuously. According to the market research conducted in 2002 by Virtual Development Corporation (VDC), the shipment of wireless products for monitoring and control is expected to increase from nearly \$109 million in 2001 to around \$752 million in 2006 in the region of North America, which is equivalent to annual growth rate of more than 47% [1]. Amongst these products, wireless data collection system plays an important role in the market place.

CHAPTER 1: INTRODUCTION

The application of wireless data collection system has gone beyond desk bound and wired systems. There are already many wireless data collection systems being developed or in service. One of these applications is WSS SR-1W Wireless Data Collection System [2]. In this system, the central node connected to host PC together with a number of remote nodes in a factory floor form a wireless data communication network. The central management terminal controls the nodes and collects data from them without wired cables. The system provides the flexibility in factory setup and eliminates the cost for installing and maintaining expensive cables.

Our daily life may also be influenced in vision of “Intelligent Home” in the near future. Imagine one can control all the electric appliances with a hand-held remote controller in front of a TV, by selecting up/down menus of appliances displayed on the TV. Without getting off from his chair, he can control lights, audio/video equipments or arm the security system. The heart of “Intelligent Home” is a wireless data collection system, in which a central station connects all electric appliances. Control command is sent out to the target appliance when one inputs a command. On the other hand, information from appliances are gathered and displayed. Brought by such a system, a more comfortable and convenient way of life style is to be expected.

Besides the applications mentioned above, wireless data collection system could also be applied to other areas such as military, scientific research and hazardous environment where least human intervention is expected. Being aware of the benefits brought by wireless data collection system, companies and departments would adopt more of such systems and stimulate market growth. Researching on more applications of wireless data collection system is the motivation of this project.

1.2 Objectives

The objective of this project is to investigate the concept of wireless data collection system and implement a prototype wireless data collection system that has the ability to collect data from the environment, transmit data through the wireless transceivers and present acquired data in appropriate manner. Other than that, the system is aimed to handle different applications concurrently, such as WeiQi (also called I-GO game) monitoring and utility meter readings applications implementing in this project.

The system is mainly designed for applications within in an indoor environment. The prototype system is designed to operate inside a building of 20 by 20 meters in dimension. The transceivers must be able to communicate up to 20 meters at very low bit error rate. As the number of simultaneously games held during a competition will be limited, the system is not required to monitor more than 6 games. In another word, the central station communicates with 6 remote nodes concurrently. Since the traffic generated by each node is very low, the total data rate required is foreseen to be less than 10 kbps. The bandwidth required will be twice the data rate.

For utility meter readings application, it is mainly an outdoor application and requires effective transmission distance up to 25 meters. The meter readings can be collected sequentially since the task is not time-critical. The required data rate is also very low. Hence a low data rate wireless transceiver with an effectively covered range up to 50 meters should meet the requirement.

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In WeiQi monitoring application, the remote node of the prototype system will be able to monitor the status of WeiQi game board and transmit the data to the central processing subsystem, where the game will be displayed and monitored continuously.

During the project development, a prototype wireless data collection system that includes hardware circuits and software programs are to be built up. A wireless communication protocol that governs multiple-access to the channel is to be designed and implemented. The system consists of three subsystems, namely, data acquisition subsystem (DAS), wireless transmission subsystem (WTS) and central processing subsystem (CPS). The CPS is able to communicate with multiple DAS simultaneously. The system involves implementing the electric circuits for DAS and WTS, developing control programs for host PC and firmware for the microcontroller.

The wireless data collection system is able to cater for various applications. Different applications utilize the common CPS and WTS. However, each application requires a unique DAS. This means individual DAS is designed to perform the particular tasks of the particular application, but adopts the same interface to the transmission module. Some modifications on the CPS may also be necessary.

In this prototype system, the DAS is responsible for detecting chess piece placement, digitizing the detected information and formatting them into data packets that are ready for transmission. Data can be transmitted wirelessly to the remote receiving antenna connecting to CPS. The CPS is to store, process and present received data in graphical manner. Meanwhile, it also manages the operations of the DAS.

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The system is developed in two phases. During the first phase, a commercially available RF development kit is used for the WTS. At the second phase, the RF development kit is replaced by customized RF module, which leads to smaller circuit size and higher system efficiency.

The important part of the project is to construct reliable circuits to detect chess piece movement and to develop software programs running on the microcontroller to control the circuits as well as to govern access to the wireless transmission channel.

The project requires background knowledge on embedded system, circuit designs and practical skills on circuit construction and debugging. In addition, strong knowledge of digital communications system and data communication network is also required. Software programming skills in C, assembly language and Visual Basic are required.

1.3 Major Contribution of the Thesis

The thesis investigates the concept, system model and applications of a wireless data collection system and then discusses the design and implementation process of a system for the application of monitoring real-time WeiQi game. Different communication protocols are discussed and implemented. The modification on protocols improves system efficiency.

Experiments have been conducted to verify system functionality. Performance of the wireless communication module under different conditions has been studied. The result shows that the performance of the wireless communication module is not

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sensitive to random noise but vulnerable to strong interferences. The experiments show that the designed system is able to monitor the targeted chessboard, transmit data wirelessly and present received data in an appropriate manner.

1.4 Organization of the Thesis

The thesis serves to document the work that has been done for the project. It is organized as follows.

Chapter 1 introduces the motivation, project objective and descriptions as well as organization of the thesis.

Chapter 2 presents literature review and overview on general system model of a wireless data collection system. The potential applications, advantages and the targeted system model are also discussed.

Chapter 3 discusses classifications of media access protocol based on the system architectures. Some well known short-range wireless communication technologies are presented. The wireless communication that will be implemented into the system is proposed.

Chapter 4 introduces some of the important development tools and resources, which are very important to the development of this project.

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Chapter 5 explains the process of designing and implementing hardware circuits of this system. Individual circuit module is presented in details.

Chapter 6 explains the development procedure for the programs running on host PC and the firmware running on microcontroller. Flow control of the wireless communication protocol is discussed as well.

Chapter 7 presents the results obtained from the experiments and discusses system capacity.

Chapter 8 summarizes the report with conclusions and recommendations for future work.

1.5 System Resources

The resources and tools that have been used during the development of this project are as follows. The tools are chosen based on the project requirements and subject to constraints of availability.

- **Hardware Resources and Tools**
 - Personal Computer
 - Virtual Wire DR1200 Development Kit
 - AT89C52 Microcontroller
 - OPB706B Infra-red Sensor
 - MAX232 and Other IC Chips
 - PCBs and Other Circuit Components

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- Oscilloscope
- **Software Resources**
 - Microsoft Visual Basic 6.0
 - C51 Professional Developer's Kit
 - Pspice
 - Microsoft Access
 - Windows XP Operating System
 - PC Serial Port Monitoring Program

The circuits are constructed and debugged using the hardware components and tools mentioned above. The firmware for microcontroller is developed in C and assembly language using C51 Professional Developer's Kit. Control programs running on personal computer is written using Microsoft Visual Basic 6.0. The database portion is based on Microsoft Access.

CHAPTER 2. WIRELESS DATA COLLECTION SYSTEM MODEL

This chapter gives the general overview of the wireless data collection system. The applications, advantages and the system model for the application of WeiQi game monitoring are discussed as well.

A wireless data collection system provides a platform that gathers and converts real world signals into a suitable digital format, then transmits the digital data to the central processing module through a common wireless communication channel and presents the data in an adequate manner. It employs different kinds of sensors and transducers for information gathering. A wireless data collection system is able to operate with minimum human intervention. In summary, it provides an easy and cost effective way of collecting data automatically.

The common way to achieve the wireless connection is to use either infrared or radio frequency for the communications link. Infrared communication link is widely used by remote controllers of TV, Air-Conditioning and many other electric appliances. However, infrared controllers requires light-of-sight direct path between the transmitter and receiver and must be pointing at the receiving appliances. In addition, any obstacle appears in between the transmitter and receiver will block the connection. Such constraints make it difficult to cover a wide range of areas for applications.

On the other hand, radio frequency link has much higher potentials than an infrared link, as it is able to penetrate obstacles and interior walls. Compared with wired system, it eliminates the need for laying cables and also supports various data

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transmission rates to suit the requirement of different applications. Advancement in low-power RF technology makes it widely used in many fields, including wireless data collection system.

There are diverse applications that can be integrated into wireless data collection system. Some of the potential applications are listed below.

- **General Applications**
 - Bar-code Reader and Bar-code Label Printers
 - Security Alarm System
 - Database Look-up
- **Manufacturing Plant Floor**
 - Smart ID Tags for Inventory Tracking and Identification
 - Time and Attendance Marking
 - Quality Control
 - Preventive Maintenance
- **Distribution**
 - Vehicle Tracking
 - Vendor Machine Refilling

Many of these applications need to transmit only a small amount of data. They demand a low data transmission rate and short transmission distance. Thus, low-bit-rate and short- distance radio frequency (RF) transceivers would satisfy the system requirements.

2.1 Literature Review

A wireless data collection system normally consists of three subsystems. The first one is data acquisition subsystem that gathers information from the environment. The next

CHAPTER 2: WIRELESS DATA COLLECTION SYSTEM MODEL

one is wireless transmission channel, through which digitized data are transmitted to central point. The last one is the central processing subsystem. As wireless data collection system exhibits so many advantages over the traditional wired system, some research works have been carried out to address the issues of designing and implementing such systems.

A small-size wireless data acquisition system for reading sensor outputs in practical experiments was described in [3]. The system comprises of two separate parts, namely, front-end circuit and terminal-end equipment. A sensor was mounted on the rotating axis of the experiment equipment. The front end captures sensor output, digitizes analog signal and transmits the signal to the terminal end. At the terminal, data are recorded and displayed. The wireless transceiver for this system operates at 433MHz ISM (Industrial, Scientific and Medical) frequency band and provides the maximum transmission bit rate of 20kbps. The system has overcome the problem of installing cables on the rotating axis. Experiment results were shown to be satisfactory.

The application on biomedical instrumentation was also investigated. In [4], a short-range, low-power wireless remote device and a self-organizing ad hoc network protocol were presented. The remote device includes the sensor and a small circuit board that contains signal pre-conditioning circuit and RF transceiver. The device is attached to a special finger ring that can be worn 24-hours daily. By wearing the ring, patient's heart rate and some vital signs can be monitored continuously. The gathered information is sent to the base station.

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Another unique feature of the above system is its wireless communication protocol. Since the device's transmission range is relatively short ($<30\text{m}$), an ad hoc network will be setup automatically when the system is up and running. The network protocol supports point-to-point communication between the device and base station, also supports multi-hop routing through repeaters so as to cover an extended range. This system is focused on ultra-low power consumption and lightweight design.

A wireless data collection system was developed for wind tunnel model applications in [5]. Current state of wind tunnel data collection requires the installation of long length of cables, which carry low-level sensor signals that are extremely susceptible to induced noise. Another issue is that these cables must be routed across the model balance. This system was designed as the alternative of current wired system. There are three novel components in its in-model subsystem. These components are MEMS (MicroElectroMechanical Systems) sensors, embedded signal conditioning circuits

Fig. 1. System Block Diagram for the System in Wind Tunnel Test

CHAPTER 2: WIRELESS DATA COLLECTION SYSTEM MODEL

and RF wireless transceiver. These components were installed in the models to be tested inside the wind tunnel. The RF transceiver was the available commercial unit. Figure 1 shows the system block diagram for one of the tests.

The data acquired by the MEMS sensors were transmitted to the receiving RF modem located at the plenum area. Unlike other applications, the antenna on-board the model had to be embedded inside the canopy surface so as to avoid any aerodynamic anomalies. Another problem might arise if the model skin is made of metal, which does not allow RF signal transmits through it. The problem could be solved by carefully selecting locations of the transmitting antenna. This system was designed to work under extreme conditions. Experiment results showed that the system was well suited for wind tunnel measurements.

In [6], the feasibility of implementing a wireless data collection system for monitoring lifeline after major earthquake was investigated. The system continuously monitors household utility meters and stores data in central database. In case of any emergency, high-priority data would be transmitted within a short time. TDMA (Time Division Multiple-Access) scheme and TD-CDMA (Hybrid Time Division-Code Division Multiple Access) scheme were employed at 2.1GHz and 2.4 GHz respectively. The number of household units to be monitored was huge. Accordingly, different transmission rate was designed for upper (288kbps) and lower (9.6/19.2kbps) layer.

The literature review presents some of the existing and on-going researches on wireless data collection systems. These systems are for various applications hence the requirements are different. These works will help to better understand and define the system model of this prototype system as its intended applications are novel.

CHAPTER 2: WIRELESS DATA COLLECTION SYSTEM MODEL

2.2 General System Model

In general, a wireless data collection system consists of three major subsystems. They are central processing subsystem (CPS), wireless transmission subsystem (WTS) and data acquisition subsystem (DAS). A system may contain multiple units of DAS. The WTS forms an ad-hoc and self-organizing network, which can be a single-hop or multi-hop network depending on application requirements. The CPS can connect to other networks such as Internet for data sharing. The general system model is presented in Figure 2.

Fig. 2. General Wireless Data Collection System Model

The CPS is usually a host PC running control programs. It is responsible for processing and presenting collected data in an appropriate manner. It can also store/retrieve data from a database and manage a number of DAS units.

CHAPTER 2: WIRELESS DATA COLLECTION SYSTEM MODEL

DAS must include sensors to convert real world information into digital format that can be processed by CPS. The sensor is to detect and convert physical characteristics, such as pressure, temperature and position into electrical signal. This is the very first step in data acquisition process. The second step involves signal conditioning, which is to amplify, attenuate and filter analog signal from sensor output. The next step is to perform analog-digital conversion (ADC). After ADC, a microcontroller processes the digitized signal and communicates with wireless transceiver.

A data collection system is able to cater for various applications. Each application has its unique DAS designed for that particular task. As seen from Figure 2, multiple DAS units are connected. These DAS units can be used for the same or different applications.

The WTS consists of RF transceivers and operates based on a set of pre-defined wireless communication protocol. Short-range and low power RF transceivers are widely used for the wireless link between CPS and DAS. The effective transmission range of these RF transceivers is usually less than 100 meters.

Some wireless data collection systems need to cover a small space only, hence require single-hop networks. In a single-hop network, data is transmitted between remote node and base station directly without the need of relaying data. Single-hop network is applicable if the distance between base station and remote node is shorter than the effective transmission range of RF transceivers.

CHAPTER 2: WIRELESS DATA COLLECTION SYSTEM MODEL

Some applications need to cover a large area such that they require multi-hop networks. It is more power efficient to emit low strength RF signal to travel a short distance and be relayed a number of times than transmitting high strength signal for a longer range. In such a multi-hop network, data originated from remote nodes or base station is relayed to the destination by repeaters. To relay data, repeaters must be installed to ensure complete coverage of the whole area. These repeaters should form networks using communication protocol that supports multi-hop routing.

2.3 Applications

This project focuses on the application of WeiQi game monitoring. WeiQi game has a very large popularity in the Far East countries such as China, Korea and Japan. It is a challenge to players' analytical skills and there is far more scope in WeiQi for intuition.

Fig. 3. Standard WeiQi Chessboard

A standard chessboard is marked with a grid of 19x19 lines as shown in Figure 3. The game starts with an empty board and the players take turns to place one chess piece at

CHAPTER 2: WIRELESS DATA COLLECTION SYSTEM MODEL

each turn on a vacant point. Black player plays first and the chess piece is placed on the intersections of the lines. Once surrounded by chess pieces of the other color, the chess piece is said to be “captured” and removed from the board as prisoner. The player who occupies larger area becomes a winner.

Nowadays WeiQi game is widely spreading and accepted by more people around the world. There are many competitions held and broadcasted in different countries every year. The traditional way of broadcasting WeiQi game on TV is through a video recorder, which records the game and broadcasts the video signal. An alternative is to reproduce the game through human efforts. However, these methods are not suitable for broadcasting over the Internet, as they consume too much bandwidth (1.17Mbps for video signal) or require human interventions. It is advantageous to monitor WeiQi game using wireless data collection system.

Utility meter reading is also of great interest. Currently household utility meters (gas, power and water meter) are analog devices. In tradition, meter readings are taken down manually house-by-house. This method requires too much manpower and work hours, and causes errors frequently. Adopting wireless utility meter reading system can solve these problems. This is to modify existing analog meters by installing a circuit module. The module includes a sensor circuit and a wireless transceiver. The circuit module is to record meter readings and transmit data to remote data terminals.

Data collected by data terminal can be relayed to respective company by means of existing infrastructure such as cellular network. The system is able to collect from a

CHAPTER 2: WIRELESS DATA COLLECTION SYSTEM MODEL

large number of meters accurately within a short period of time. Thus, continuous meter monitoring becomes possible.

2.4 Advantages of Application

A wireless system designed for WeiQi game monitoring will exhibit advantages over traditional methods. The system is highly automatic and can be managed from a central terminal (host PC).

The wireless system consumes much less transmission bandwidth. WeiQi game players usually think over a long time before placing a chess piece. Instead of video signal, the system transmits placement or status information of chess pieces only. Thus bandwidth consumption is reduced by a large extent, which makes it extreme suitable for Internet broadcasting.

The system also eliminates the need for cable wiring and is able to monitor many games simultaneously. It provides the flexibility of arranging multiple games concurrently. This is convenient for competition organizer to setup/change the layout of competition hall.

Other than that, the number of game referees can be reduced since a game referee is able to monitor several games at the same time through data terminal. This helps to reduce financial budget for organizer.

CHAPTER 2: WIRELESS DATA COLLECTION SYSTEM MODEL

The system is also useful for training purpose. Any game can be saved into database and retrieved at a later time. Players can replay the games for analysis and training purposes.

2.5 Applications System Model

Fig. 4. Applications System Model

The system model of applications for monitoring WeiQi game and utility meter reading is shown in Figure 4. The system includes the three major subsystems and implements a customized single-hop communication protocol. The CPS is a host PC with application programs running on it while the DAS comprises of remote node circuit and the customized transducer circuits.

The transducer circuits are built for the targeted applications and are different from each other. As such, it is necessary to modify the DAS module as well as to make

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some changes on the CPS software when additional application is to be included. However, WeiQi monitoring and utility meter monitoring applications are small scale, small range applications. Both applications require low transmission rate and small transmission range, hence they can use the same wireless transceivers and share the common communications channel. The interface to the wireless transceivers is designed to be identical. When other applications are to be implemented on the same system, it is necessary to modify the DAS and make some changes on the software running on the CPS. As seen from Figure 4, different applications share the same WTS and CPS because of similar requirements on the communication channel.

2.6 Function Descriptions

The three major functions of the CPS are data processing, displaying and accessing database. The CPS is responsible of maintaining the RF link between CPS and DAS. It decodes received RF data packets and verifies packet integrity. The game being monitored will be reproduced graphically. At the same time, the game can be saved into a database and be redisplayed in the future. Meanwhile, operator can control the system by sending commands through the CPS.

The WTS is to exchange error-free RF packets between DAS and CPS. It comprises of multiple RF transceiver units and the RF communication protocol that has been implemented. The transceiver connected to the CPS communicates with host PC over RS232 serial protocol. This is a duplex protocol and will be introduced in Chapter 4.

CHAPTER 2: WIRELESS DATA COLLECTION SYSTEM MODEL

Unlike wired communications, RF links encounter many more interferences. Thus a well-designed, robust communication protocol is essential in reliable radio links establishment. A protocol is designed and implemented for this application. The protocol will be discussed in Chapter 3.

The objective of the DAS is to gather desired information from real world and convert the information to digital format. For the application of WeiQi game monitoring, it includes a modified chessboard and remote node circuit, which consists of sensing circuit, signal conditioning and ADC circuit. Besides, it also includes a controlled power supply module that supplies steady power to the circuits.

The heart of the DAS is a microcontroller. The microcontroller manages operations of the DAS. It fetches digital signal from ADC, assembles data into data packets and send these packets to transceiver. At the same time, the microcontroller decodes received command from host PC and takes action accordingly.

After power up, the system initializes and waits for response from remote node. When the remote node is powered up, the microcontroller on-board starts to poll chessboard, assemble the information into RF data packets and transmit to the CPS. The CPS continues to process these data packets after they are received.

As seen from Figure 3, information (data packets) flows from DAS to CPS through WTS, whereas control information flows the opposite direction. The design and implementation of hardware circuits and software programs (firmware and PC program) will be discussed in Chapter 5 and Chapter 6 respectively.

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2.7 Conclusion

It is important to understand the general system model of a wireless data collection system. The system model of the application is constructed based on the general model and will help to understand the functions of each subsystems. Details of design and implementation will be given in Chapter 5 and Chapter 6.

CHAPTER 3. WIRELESS COMMUNICATION PROTOCOL

A robust wireless communication protocol is essential in setting up a reliable RF link between transmitter and receiver. A microcontroller is used in this project to handle the communication protocol. This chapter presents background knowledge of existing wireless media access control (MAC) protocols and some short-range wireless communication techniques. Such knowledge is very important in designing the single channel multiple access protocol that is to be implemented. The proposed protocol is designed specially for the application and constrained by system capability.

3.1 Classification of MAC protocol

Due to the nature of the wireless channel, issues such as time-varying channel, burst channel errors and location-dependent carrier sensing are to be considered. The mechanism of indoor radio propagation is especially complex, even if there appears to be a light-of-sight path between the transmitter and receiver. MAC protocol defines rules for orderly access to the shared medium and plays a crucial role in efficient and fair sharing of scarce wireless bandwidth. Techniques such as handshaking, error correction codes, smaller packet size and automatic retransmission scheme are adopted to improve network throughput.

There are many developed protocols for different types of wireless networks. MAC protocols can be classified into distributed MAC protocol and centralized MAC protocol based on the system architectures. Based on the modes of operation,

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centralized MAC protocol can be further divided into random access protocols, guaranteed access protocols and hybrid access protocol [7]. Figure 5 shows the classification of wireless MAC protocols.

Fig. 5. Classification of Wireless MAC Protocols

In random access protocol, nodes contend for access to the medium and the transmission is successful only if there is one node transmits. Contention resolution algorithm (CRA) is defined to resolved collisions in an orderly manner. Typical distributed random access protocols are ALOHA, Slotted-ALOHA and CSMA (Carrier Sense Multiple Access).

From Figure 5, it is seen that random access protocols can operate on both architectures. The difference is that, all nodes are of equal priority in distributed architecture and try to seize the channel when the channel is idle. In centralized architecture, the complexity and arbitration are moved into base station (BS), wherein the BS has explicit control on whom and when the channel is allocated to. All communications must go through the BS [7]. Guaranteed access and hybrid access protocols require a central BS, hence they are mostly found in centralized architecture.

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In guaranteed access protocol, nodes access the medium in an orderly manner, usually in a round-robin fashion. A typical scheme is to use a master-slave configuration, where a node transmits when it is polled by the master node. Another scheme is by token passing. A node sends data only when it has the token.

Hybrid access protocol is based on request-grant mechanism. During contend period, a node sends its request for transmission to BS by means of random access protocols. The BS schedules and allocates the bandwidth for nodes content for transmission. It takes the advantage of random access protocol and guaranteed access protocol, but heavy burden and complexity lie on the BS.

3.1.1 Distributed Random Access Protocol

Distributed random access protocol is discussed because it is seen as a suitable candidate for the protocol to be implemented. The protocol implemented in first development stage is similar to pure ALOHA and provides regulations to the access to wireless channel, flow control and error detection capability. ALOHA and CSMA will be further discussed.

ALOHA

Pure ALOHA was the first protocol proposed for packet radio networks. It is a classic example of distributed random access protocol. A node in this network transmits when it has data to send. The data is assembled into packets with error detection code. If multiple transmissions occur simultaneously, collision happens and the packets are damaged. The sender waits for acknowledgment (ACK) from the receiver after

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sending the packet. The sender concludes that the packet is lost if it does not receive ACK within some defined period. The sender retransmits with a randomly selected delay to avoid repeated collisions [8].

To study the performance of pure ALOHA, assume the same packet transmission time T_p for all packets. Let G be the traffic intensity, defined as the number of transmission attempts per packet time T_p , S be the throughput, or the number of successful packet transmissions per T_p . Assume traffic intensity obeys a Poisson distribution. The network throughput is given by

$$S = Ge^{-2G} \quad (1)$$

At very low traffic intensity, there will be very few collisions and hence $S \approx G$. At high traffic intensity, a large number of collisions will be expected, so $S \ll G$. The maximum throughput for ALOHA occurs at $G=0.5$, where $S=0.184$ [8].

Slotted ALOHA

Slotted ALOHA protocol divides the time axis into fixed length time slots of one packet transmission time, and synchronizes all nodes with a packet for transmission. A collision occurs if two or more nodes start transmission at the beginning of the same time slot. The probability of packet collision is reduced and maximum throughput is doubled to be $1/e$, or 37% [9].

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CSMA

In CSMA protocol, a node first senses the wireless channel if it has a packet to send. If the channel is sensed busy, the node delays its transmission and reschedules transmission attempts according to the back-off strategy. If the channel is sensed idle, the node will transmit immediately. Collision occurs only if two or more nodes start to transmit within the same short period time, which is the sum of propagation delay plus system delay.

As CSMA protocol prevents any node from destroying ongoing transmission, the probability of collision is reduced, compared with ALOHA. Obviously, it is able to achieve higher throughput than ALOHA, as has been proved by many studies.

3.1.2 Centralized Guaranteed Access Protocol

In centralized access protocols, arbitration and complexity are moved into the BS. Polling scheme is widely used in centralized guaranteed access protocols. In this scheme, the BS polls all the nodes in a round-robin fashion to gather transmission requests. Any node that has data to send responds with a request message, or *keep alive* message when it has no data pending to send. The BS then polls nodes for data according to the received request. The poll-request handshaking sets up a communication channel between the BS and node.

Polling scheme ensures a good communication link and minimizes waste of bandwidth caused by channel outage.

3.1.3 Comparisons of the Protocols

ALOHA provides a flexible way of managing channel access. Any node is allowed to transmit at any time, but successful only if there is a single node transmits. ALOHA does not guarantee that the receiver will receive the packet properly; hence it relies on back-off algorithms to retransmit corrupted data packets automatically.

ALOHA works well at very low traffic intensity, since very few collides are expected. Its performance drops dramatically as data intensity increases, with a maximum throughput at about 18%.

Though slotted ALOHA improves network performance, it requires timing of all devices to be synchronous, which creates obstacle in some system implementation. It is not suitable for the application due to the difficulty in synchronizing the BS and remote nodes in time.

CSMA performs better than pure ALOHA and slotted ALOHA in most situations. For systems employing random access protocols, the throughput increases as the offered traffic increases from zero, but reaches the peak for some optimum value of offered traffic. After that, the throughput decreases as the offered traffic continues to increase. Distributed random access protocols may become unstable and the delay may become infinite as the offered traffic increase to some extent [10]. At very high offered traffic, the throughput may go down to zero and consequently the delay may become infinite. Thus the network becomes unstable and cannot function as expected.

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However, the throughput can be maintained at a value close to the offered traffic while the delay is kept at an acceptable level if the offered traffic is below or slightly exceeding the optimum point. Hence, distributed random access protocols such as ALOHA and CSMA can be prevented from stability problem if the overall traffic load and number of users are kept at a low value.

In a centralized guaranteed access protocol (polling scheme), nodes transmit data at the interval determined by the BS. By means of handshaking, chance of a collision is minimized. Centralized guaranteed access protocol has lower possibility of collision than random access protocol. But it adds overheads for connection establishment and administration. It is not easy to compare the performance of distributed random access protocols and centralized guaranteed access.

Distributed random access protocols tend to be inherently robust such that removal of any one of the nodes will not collapse the network. On the contrary, removing the BS will bring down a centralized network. Thus the BS must be robust and powerful enough to schedule a large set of requests. Performance of the BS is crucial to the network performance.

Due to its flexibility and ease of implementation, a protocol that is similar to CSMA is implemented for the application. Stability problem will not occur for the implemented protocol, as the traffic load will be kept at a low level. The nodes share the common wireless transmission channel and compete for access using distributed random access protocol.

3.2 Short-range Wireless Communications Technology

Some technologies designed for low-power, short-range wireless communications are available or being developed. These technologies include some well-known standards such as IEEE 802.11.b series, Bluetooth, Ultra-WideBand (UWB) technologies and some other general-purpose short-range RF transceivers. IEEE 802.11.b series is the standard defined for wireless local area network. It is not suitable for this application since it is mainly designed for computer networks. There is a need to know about other technologies and understand their merits and limitations.

3.2.1 UWB Technology

Ultra-Wideband technology is loosely defined as any wireless transmission scheme that occupies a bandwidth of more than 25% of a center frequency, or more than 1.5 GHz [11]. It offers data rate of 100-500 Mbps at distances of 2-10 meters, using an average radiated power of about 200 microwatts.

Different from other RF technologies, UWB sends pulses of energy across a spectrum of frequencies to transmit data, instead of using a narrow-band frequency carrier. Being a carrier-less technique, it is based on sharing spectrum that has been occupied by other applications by means of the overlay principle, rather than looking for new frequency bands.

The bandwidth of UWB signal spreads from near DC to several GHz theoretically. It thus promises data rates of the order of Mbps, which is much higher than other

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techniques. In the near future, its principal application will be for high-speed, cable-free data transfers such as MP3 or video file transfers into portable device.

UWB has several potential advantages. It may allow simultaneous communication of multiple devices at high data rates by distributed control of interference levels. Given its ultra-wide spectrum, it provides robustness against fading and scalability. UWB also improves resource management and routing strategies [11].

However, UWB is still under development and facing some technical challenges. In order to meet the requirements of UWB radio system, currently existing modulation and coding techniques have to be modified [12], e.g. adaptive modulation methods and channel coding schemes need to account for the specific characteristics of the UWB radio channel. Another problem lies in mitigating multi-path effects. Antenna design and implementation for UWB radio device are more challenging than conventional narrowband systems. In addition, it is also necessary to further investigate interferences originating from other in-band radio signals, and interferences to existing radio systems caused by UWB radio signals [12].

3.2.2 Bluetooth Technology

Bluetooth is a short-range, low-power radio link (10-100 meters) between two devices operating in the unlicensed 2.4 GHz industrial, scientific, and medical (ISM) band. It facilitates ad-hoc connections for stationary and mobile communication environments.

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Bluetooth devices support point-to-point and point-to-multipoint connections. In point-to-multipoint connection, two or more devices sharing the same channel form a piconet. Each piconet has one master device and up to seven active slave devices. The devices can be in different states and involve in different procedures such as inquiry, paging and data transmission. The devices have to go through the process of connection establishment automatically before packet transmission starts.

The ISM frequency is divided into 79 frequency hop channels, each with 1 MHz. These channels are hopped according to a pseudo-random hopping sequence, which is determined by the piconet master device. The nominal hopping rate is 1600hop/second. Frequency hopping technique improves data security, reduces external interference and lowers the possibility of intrusion.

Bluetooth uses Time Division Duplex (TDD) scheme for full duplex transmission. The channel is divided into time slots of 625 μ secs. Each time slot corresponds to an RF hop frequency. The modulation technique uses Gaussian Frequency Shift Keying (GFSK), where binary data 1 is represented by a positive frequency deviation from the carrier frequency, whereas 0 is represented by a negative frequency deviation. With a 1 MHz bandwidth per frequency slot, the maximum raw transmission rate is 1 Mbits/sec.

Bluetooth supports asynchronous connectionless (ACL) link for data and synchronous connection-oriented (SCO) link for voice or a combination of both. The maximum data rate supported by ACL is 723.2 Kbps, while SCO is 64 Kbps.

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The basic architecture of Bluetooth consists of the link manager protocol and baseband controller at the lower layer and the RFCOMM, L2CAP layers at the middle, plus some standalone communication and data information protocols at the higher layers.

Bluetooth technology brings the convenience of connecting electronic devices together and simplifies the way of interaction with other electronic devices at a low cost in the future. But it is still facing some limitations. The first one is the delay in device discovery procedure, in which the timing in the worst case can be more than 10 seconds [13]. Another limitation is the external interferences originated from devices operating in this band. For example, microwave oven also operates at 2.4 GHz and may become a major source of interference.

3.2.3 General Short-range RF Transceiver

Besides RF standards such as UWB, Bluetooth, WLAN, there are some other low-power, short-range RF transceivers suitable for data acquisition applications. These products are developed and manufactured by private companies and are available in the market. In general such a transceiver consists of RF transmitter and receiver and provides standard RS232 serial port to exchange data with PC or other equipments. The transceiver is responsible for radio signal modulation and demodulation.

Such transceivers usually operate in unlicensed frequency band such as ISM, where short-range radio equipments are allowed to operate without individual license from the government. The operating frequency band is shared with other radio appliances;

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hence the devices operate subject to non-interference and non-protection basis. The effective transmission range is normally less than 100 meters. In most cases, the emitting power at transmitter is less than several mW.

These transceivers do not require complex modulation/demodulation modules. Frequency Shift Keying (FSK), Amplitude Shift Keying (ASK) and ON-OFF Keying (OOK) are commonly employed in these transceivers. Typically, the transmission rate varies from 9.8 Kbps to 100 Kbps, depending on the product specification. For example, the Virtual Wire DR1200 Development Kit supports OOK for low data rate (less than 30 Kbps) and ASK for high data rate.

In communication systems, Amplitude Shift Keying (ASK) refers to the modulation scheme that shifts transmitted signal power level to represent digital data. On-Off Keying (OOK) is a special case of binary ASK modulation, where only two signal levels are used to represent digital data “1” and “0”. In OOK mode, the transmitter transmits when data “1” is presented and remains silent when data “0” is to be sent.

In this thesis, the terms ASK and OOK both refer to binary ASK modulation but ASK represent different things than standard usage. In order to differentiate the two modulation schemes available in the transceiver, the term ASK in this thesis refers to binary ASK modulation where data “1” and “0” are represented by higher and lower transmitted signal powers respectively. These two modulation schemes are used because they are simple to implement in practice. Hence they can be found in some experimental wireless transceivers.

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These transceivers are flexible for various types of applications. As the transceiver does not normally bundle with a wireless protocol, designers are free to design the wireless communication protocol that is most suitable for the application. The requirement on processing capability of the microcontroller can be lower too. System design complexity and implementation cost can be reduced.

3.2.4 Conclusions

The wireless communication technologies discussed above emits RF signal power in the order of mW. But the transmission capability varies greatly. UWB has the highest data rate (100 – 500 Mbps), Bluetooth is in the middle, while other transceivers provide relatively lower data rate. However, further investigation on UWB is needed to achieve the projected data rate.

The general RF transceiver covers relatively a large area (less than 100 meters), while UWB has a much smaller coverage area (2-10 meters). Bluetooth is able to support up to 10 piconets within an area of 10 meters. The covered area of UWB or Bluetooth is small compared with general RF transceivers. Though it is possible to extend coverage using relay devices, this would increase the complexity of the system design, as well as the protocol design.

As 2.4 GHz is unlicensed frequency band, many other devices operate at this frequency band. These devices include UWB and Bluetooth. More devices will join in this range in the future. It is of concern that the 2.4 GHz could soon become

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congested. Thus more interference is expected, which leads to downgraded performance.

Unlike UWB and Bluetooth, the general RF transceivers usually provide a platform for RF signals modulating and demodulating only. There is much flexibility in implementing a customized communication protocol for the specific application. Thus, a RF transceiver other than UWB and Bluetooth is integrated into the system for this application. The transceiver will be introduced in Chapter 4.

3.3 Proposed Wireless Communication Protocol

A packet radio protocol is to be integrated with the RF transceiver to provide a simple but robust means for governing access to the common RF channel. A single-hop protocol is proposed based on the characteristics of the transceiver and capability of the microcontroller to achieve maximum channel utilization. The protocol will be implemented on the system.

Besides governing access to RF channel, the protocol is also responsible for encoding or decoding radio packets. At the transmitting side, the protocol receives data streams from PC or DAS, assembles data stream into radio packets, encodes radio packets and pushes data to RF transceiver. At the receiving side, the protocol retrieves raw data from RF transceiver, decodes the data and verifies data integrity. If no error is detected, received data is passed to the next stage and acknowledge (ACK) packet is sent back to transmitter.

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To verify data integrity, the protocol includes a 16-bit ISO 3309 error detection checksum. At transmission side, the protocol calculates 16-bit frame check sequence (FCS), which is attached to the packet before packet encoding. At receiving side, the protocol calculates FCS after packet decoding. The packet is error-free if computed result is equal to 0xF0B8. FCS calculation will be introduced in Chapter 4.

3.3.1 DC Balance Coding

Radio communication system employs some kinds of data encoding scheme for efficient transmission and extraction of clock information from received data stream. Encoding scheme should produce frequent transitions in the transmitted signal, which facilitates data clock synchronization and efficient data recovery at the receiver side. It should also condition the signals for DC-balance, which means the encoded signal has a '1' value for 50% of the time and a '0' value for another 50% of the time on average.

Decimal	HEX	Bit Pattern	Decimal	HEX	Bit Pattern
0	15H	010101	8	38H	111000
1	31H	110001	9	29H	101001
2	32H	110010	10	2AH	101010
3	23H	100011	11	0BH	001011
4	34H	110100	12	2CH	101100
5	25H	100101	13	0DH	001101
6	26H	100110	14	0EH	001110
7	07H	000111	15	1CH	011100

Table 1. Byte to 12-bit Conversion Table

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To achieve DC-balance, the radio protocol implements symbol conversion technique, which is a byte to 12-bit symbol conversion. Each byte of a message is encoded as a 12 bit symbol, always with six '1' bits and six '0' bits. The maximum number of consecutive '1's or '0's is 4. Table 1 is the conversion table. The drawback of DC-balancing is that required transmission bandwidth is increased by 50%.

3.3.2 Protocol Flow Chart

Fig. 6. Proposed Single-hop Protocol Flow Chart

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The protocol adopts the similar mechanism as CSMA to regulate access to RF channel. When a node has data to send, it senses the channel before transmitting the packet. If the channel is sensed idle, it will send the packet immediately and waits for ACK packet. Otherwise it will defer its transmission and retry after a random period. It will retransmit the packet if it cannot receive ACK packet within a specific period of time. The process continues until it reaches the maximum number of retries. Figure 6 depicts this process.

At the receiving side, the protocol checks for data integrity by computing the FCS when a radio packet is received. An ACK packet will be sent to acknowledge the transmitter if the packet is free of error. Duplicate received packets will be discarded. Duplicate packet occurs when the transmitter automatically retransmits the same packet if it cannot receive acknowledgement.

Address routing is also implemented. Each node has a unique node address that can be setup manually. The address is represented by a 4-bit value, which ranges from 0-16. 15 addresses are available with address 0 reserved for broadcast packet. The address space can be expanded as required by applications.

As the transmission range of the RF transceiver is large enough to cover the whole region of interest, the base station is able to communicate with remote nodes directly in this application. The proposed single-hop wireless network protocol should meet the requirements of this application. The protocol is essential in setting up a stable, robust and efficient radio network. The packet format and operations of the transceiver will be discussed in Chapter 6.

3.4 Multi-hop Wireless Communication Protocol

For an application whose coverage area is within the effective transmission range of RF transceivers, a single-hop wireless communication protocol is sufficient in setting up a network. In such application, the base station talks directly to remote nodes without the need to relay data by using routing algorithm.

Some applications may have to relay data to the base station at distant place, which is beyond the transmission range of RF transceivers. A multi-hop protocol is necessary in maintaining a network that supports packet routing so that data packets can be routed to the base station or destination node. The protocol should allow the network to initialize itself in a highly ad hoc and self-organizing manner so as to minimize human intervention.

Some routing schemes such as proactive routing and reactive routing exist for wireless multi-hop network. Proactive routing schemes try to keep all the information updated and are good for static networks. Reactive routing schemes would try to discover a route only when a request comes and are better for dynamic networks. There are even more complex routing schemes available. However, these existing routing schemes are not suitable for this application due to their complexity and high demand on memory, which exceeds the capability of the implemented microcontroller. An alternate multi-hop protocol is discussed for this application to incorporate multi-hop network. The protocol will extend the system capability to cover a larger range.

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3.4.1 Multi-hop Protocol Overview

Similar to single-hop network, a multi-hop network also includes a pre-defined base station and a number of remote nodes. Some nodes are out of the range of base station. Therefore some devices need to act as repeaters to relay data between base station and remote nodes. Theoretically, any neighboring node to the transmitting node can act as a repeater and forward packets to its next hop. This scheme makes full use of the nodes and reduces the number of device types, but it brings every node the burden of discovering routes and increases protocol complexity. It is not suitable for this application since the implemented microcontroller has limited performance.

Thus, it is recommended to install repeaters and move burden of routing discovery into repeaters. The repeater is similar to a node except that it implements modified firmware and it doesn't include data acquisition circuit. A multi-hop network can be implemented by merely adding repeaters into the system proposed in the previous section. The single-hop protocol discussed in previous section is still applicable. Together with newly installed repeaters, a multi-hop network can be setup with slight modification on existing nodes and base station. However, the fully implementation of multi-hop network required a number of nodes that are equipped with wireless transceivers. Thus, the proposed multi-hop network was not tested experimentally due to the limited hardware resources available.

The multi-hop protocol also implements DC balance coding, error detection coding and channel sensing mechanism to maximize network throughput. A node sends ACK packet to the transmitter upon receiving a packet successfully.

3.4.2 Multi-hop Protocol Operation

Similarly, each repeater is assigned a unique node address. All nodes and repeaters know the address of base station. Any data packet originated from remote node has explicitly set the destination address, which is base station address.

The multi-hop protocol introduces a concept called Distance Metric (DM). DM measures the distance from base station to a node or repeater. The DM of base station is zero while the DM of other node or repeater is determined by the process below. To determine DM, base station broadcasts a special packet with zero DM periodically. Any repeater that receives the packet increases the DM by one and re-broadcasts the packet. The DM of a node or repeater is equal to one plus the lowest DM that it can hear. This process is depicted in the figure below.

Fig. 7. DM Discovery for Multi-hop Network

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The dotted circle represents the effective coverage area of base station or repeater. Any node or repeater that can hear base station directly has its DM as 1. If a node hears from more than one repeater, it will choose the smallest DM. It is obvious that the nearer to base station, the smaller the DM is.

At the same time, all repeaters create tables containing a list of neighboring repeaters and the corresponding DM information from broadcast packets originated from base station. As shown in Figure 8, the repeater with DM as 2 creates a table that contains address and DM information of the two nearby repeaters. These nearby repeaters have DM as 1 and 3 respectively. For uplink communication, a repeater forwards received packet to one of its nearby repeaters with lower DM based on the table.

Fig. 8. Uplink Routing for Multi-hop Network

When a node (DM=4) sends a packet destined to base station as shown in Figure 8, the nearby repeater (DM=3) knows this packet is for base station and relays the packet to the next repeater (DM=2). The process continues until the packet reaches destination.

Fig. 9. Downlink Routing for Multi-hop Network

On the other hand, a node broadcasts a discovery packet to find out the address of base station periodically. Nearby repeaters response to the node and forwards the packet to base station. Hence base station is able to discover all active nodes and their corresponding DMs.

As shown in Figure 9, when base station has a packet for node A (DM=3), it sends the packet with address and DM information of node A. Subsequently, all repeaters with DM lower than node A will forward this packet. However, repeaters with the same DM as node A will not forward this packet. In this way, network overhead is reduced while the protocol remains easy to implement.

3.4.3 Hidden Node Problem

Performance of the proposed multi-hop protocol may be downgraded by hidden node problem. As shown in Figure 10, node A and B cannot hear each other but both can

Fig. 10. Hidden Node Problem for Multi-hop Network

hear from repeater C. In this case, node A is a hidden node to B. Collision occurs when A and B try to send packet to repeater C simultaneously.

To overcome this problem, handshaking procedure is adopted. Any node sends a short RTS (Request To Send) packet before transmission. Nearby repeater responses with CTS (Clear To Send) packet if the channel is idle. The node then starts transmission. The node will not continue transmitting data packet until it receives CTS packet. When a defined time limit is reached, the node will initiate transmission request again. This scheme reduces the chance of collision hence increases network throughput.

3.5 Conclusions

This chapter has discussed some types of wireless network protocols based on the system architectures and modes of operation. Some of the short-range, low-power wireless communication techniques are also discussed. A single channel, single-hop multiple access protocol that is designed for the application is proposed and implemented on the system. A multi-hop protocol based on the proposed single-hop protocol is also discussed in detail. As multi-hop network protocol produces more overheads and requires more time in transmitting a packet, its throughput is expected to be lower than single-hop network.

CHAPTER 4. DEVELOPMENT TOOLS AND RESOURCES

This chapter describes the major development tools and resources that have been used during the project development. These include the software toolkit C51 Professional Developer's Kit, which is used for firmware design and development; Microsoft Visual Basic, which is used for writing control programs running on PC and Pspice, which is used for drawing circuit diagrams. It is also required to be familiar with hardware parts such as AT89C52 microcontroller, various IC chips and so on. Knowledge on these tools and resources are important.

4.1 C51 Professional Developer's Kit

The C51 Professional Developer's Kit is the software tool for developing firmware running on the microcontroller. The firmware is developed using both C language and assembly language. The kit includes mainly the following components [14].

µVision2 Integrated Development Environment (IDE)

A51 Macro Assembler and C51 ANSI C Compiler

µVision 2 Debugger

BL51 Linker/Locator

The µVision2 IDE provides a complete environment for building up projects, writing source codes and debugging. µVision2 integrates the source code editor, C compiler, assembler and linker together, programs can be written in C, assembly language or a mixture of both languages.

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Fig. 11. μ Vision2 Block Diagram

The Keil C51 Compiler is compatible with ANSI C programming language. It includes some functions that are specifically supporting the 8051 families. These functions are modified to suit the specific task requirements. The A51 Assembler supports the entire instruction set of the 8051 and all its derivatives. The Compiler and Assembler create relocatable object files from source code programs. Figure 11 depicts the block diagram of μ Vision2 and the corresponding output files at different stages.

The BL51 Linker creates an absolute object module using the relocatable object files and library files. The absolute object module determines memory locations of all codes and data. The executable file is produced from the absolute object file and can be used for simulation by the Debugger.

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The Debugger includes a software simulator that can perform logical and timing simulations for an 8051 system. The firmwares are fully tested using the software simulator before converted into binary file and programmed into the MCU chip.

Though a simulator is able to simulate most of the operations of user programs and corrects the errors reside in the program, it is not a replacement to in-circuit emulator. A program working well on software simulator may not work properly in real-world hardware platform.

Due to the absence of in-circuit emulator, the software simulator is used for the project. The programs were tested using the simulator, then programmed into the microcontroller chip using a device programmer and tested on the target circuits. This process is time consuming and needs to be repeated whenever an error is found.

4.2 Introduction to AT89C52

The microcontroller (AT89C52) is implemented to manage operations of the DAC and the wireless communication protocol. The chip is a derivative of Intel's 8051 microcontroller. AT89C52 is selected because it provides the necessary features that are required by the application. The main features are as follows [15].

- Full duplex UART (RS-232 Serial Port)
- 256 Bytes Internal Data RAM
- 8K Bytes of In-System Reprogrammable Flash Memory
- Three 16-bit Timer/Counters
- Eight Interrupt Sources with Two Priority Levels

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Most of the on-chip peripherals are utilized in this project. The on-chip Flash memory is electrically erasable and reprogrammable, which allows user programs to be programmed into the chip using a device programmer for many times.

4.3 RS232 Serial Communication

The communication between the wireless transceiver module and host PC utilizes RS232 serial port standard. Understanding RS232 standard is necessary when debugging the circuits.

Baud rate measures how fast data can be transmitted. RS-232 uses only two voltage states, baud rate is identical to the maximum number of data bits that are transmitted per second, including overhead bits. Some commonly used baud rates are 9600, 19200 bps. Due to the overheads, the actual data rate is less than the baud rate.

RS232 is asynchronous communication protocol, in which a character is transmitted at a time. Each character is packed into a character frame that consists of start bit, data bits, the optional parity bit and the stop bits. Figure 12 shows a typical character frame encoding the letter “m” with 7 data bits, 1 party bit and 2 stop bits [16].

Fig. 12. Character Frame Encoding Character “m”

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Start bit indicates the beginning of each character frame. Its duration equals to one bit period. The optional parity bit follows the data bits and provides a simple error checking mechanism. Stop bits are the last part of a character frame. Data bits are sent from least significant bit (LSB) to most significant bit (MSB) using inverted logic. The data bits shown in Figure 12 are interpreted as “11011101” in binary, which is character “m” as defined by ASCII standard.

Since the logic levels of RS232 are different from CMOS logic level, a level converter is implemented to perform logic level conversion between RS232 and CMOS logic levels. The level converter uses an integrated chip MAX232.

4.4 DR1200 Development Kit

4.4.1 Overview

During the first stage of project development, a set of DR1200 development kit is used for the wireless transmission subsystem. The kit creates the virtual link between the DAS and CPS. The kit consists of two nodes as shown in Figure 13. Each node includes a data radio transceiver board and a protocol board. Understanding the kit thoroughly is very important in implementing the system.

Fig. 13. DR1200 Development Kit

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The data radio transceiver board is capable of transmitting/receiving data wirelessly. Its goal is to demodulate the received radio signal and modulate the transmitted information. The protocol board is responsible for handling tasks such as coding/decoding, error detection and flow control. At the base station, the protocol board interfaces with host PC and acts as the bridge between host PC and radio board.

The operating distance depends on many factors. Transmission power, data rate, receiver sensitivity and coding technique all play important role in determining the maximum transmission range. The range also varies with signal propagation environment. Usually radio signal propagates much further in open space environment, but much shorter in confined space, especially in dense cubical office space. At the rate of 19.2kbps, the estimated operating distance for the kit in open space is about 101 meters, but drops to 10.1 meters in dense cubical office [17].

The kit is configured to operate at the data rate of 22.5kbps at the frequency of 916.5MHz. The transmitter output power is typically -1 dBm, or 0.79 mW [18]. Appropriate coding techniques are adopted to improve channel efficiency.

4.4.2 Data Radio Board Operation

The heart of the data radio board is the TR1000 Amplifier-Sequenced Hybrid (ASH) transceiver. Simply speaking, the incoming radio signal is filtered by a narrow-band SAW (surface acoustic wave) filter to remove out-of-band noise. High frequency signal is down-converted to lower frequency and is then applied to two amplifiers to boost weak RF signal. After that, the signal goes through low pass filter and detector.

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The desired data appears at the output [17]. The reverse process will be gone through for transmission. Figure 14 is the block diagram of the ASH receiver.

Fig. 14. ASH Receiver Block Diagram

The radio board supports data rates up to 115.2 kbps. It supports On-Off Keying (OOK) and Amplitude Shift Keying (ASK) modulation. However, the interface circuit on the radio board needs to be redesigned for different modulation schemes. In OOK, the transmitter output is off between ‘1’ data pulses, whereas it transmits a pulse when data ‘1’ comes in. In ASK, ‘1’ pulse is transmitted at a higher power level, while ‘0’ is at a lower power level.

Although ASK and OOK are inferior in performance than other modulation schemes, they can still be found in some general-purpose wireless transceivers. This is because they are simple to implement in practice, which leads to lower cost. Because of its simplicity, ASK or OOK modulation scheme remains a good choice for applications whose requirements on bandwidth and power efficiency are not stringent.

The transceiver was pre-configured to OOK modulation in factory. To change the modulation scheme, a new radio board needs to be redesigned and fabricated. Though OOK mode transmits at lower rate than ASK, it conserves power because it transmits

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at a lower power level. Since the prototype system demands very low data rate, OOK modulation is sufficient in handling the traffic load.

It is very important to master the operating principle of the radio board. Coding technique and flow control must be implemented to cooperate with the radio board in order to design an efficient and robust wireless communication system.

4.5 Frame Check Sequence (FCS)

Data integrity may be lost during transmission due to interference in RF systems. Many mechanisms have been proposed to detect or correct errors occurred during transmission or storage. Cyclic Redundancy Code (CRC) protects data from errors by adding a certain amount of redundancy (FCS). CRC-16 is one of the powerful CRC for error detecting and has been widely adapted by many communication systems.

The CRC-16 is powerful that it is able to detect all single, double, triple and odd numbers of errors within a transmitted message whose length is 32751 bits or less. Furthermore, it can detect all burst errors of length 16 or less, more than 99.99 percent of 17 bit, 18 bit error bursts or longer error bursts [19]. The cost of this capability is a 16-bit FCS attached to the data packet.

The important characteristic of error detection code is that it is reproducible by others. At the transmission side, sender computes the FCS, which is added to the packet to be transmitted. At the receiving side, receiver computes the FCS of entire received packet to verify data integrity. If received packet is free of error, generated FCS will

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be equal to the preset constant value. Any other value implies an error in the received packet.

There are many studies on designing and implementing CRC codes. The generator polynomial $g(x)$ of the implemented CRC-16 is shown in (2).

$$g(x) = 1 + x^5 + x^{12} + x^{16} \quad (2)$$

Unlike hardware implementation where bit-wise computation is commonly used, byte-wise computation of FCS is more convenient and more efficient in software. In addition, table-driven computation replaces conventional methods to reduce computation power and make the program neat. Table-driven computation method is implemented into the protocol.

Together with retransmission scheme, adaptation of FCS enables the system to correctly transmit and receive data packets through the radio channel. The additional cost of this scheme is to slightly increase the packet redundancy.

4.6 Conclusions

This chapter introduces the major software resources and hardware tools that have been used during the project development. These resources must be understood and mastered for the purpose of turning the application into reality. Hardware circuits design and implementation will be discussed in the next chapter.

CHAPTER 5. HARDWARE DESIGN AND IMPLEMENTATION

This chapter discusses the design and implementation processes of individual subsystems for WeiQi game monitoring application. These subsystems include the front-end DAS, which monitors the game board and produces digital data, the WTS, which links the DAS and the CPS through the radio channel. The CPS is a host PC connected with the RF transceiver and will be discussed in Chapter 6 with the focus on software programs.

5.1 Application System Model

Fig. 15. Application Circuits Model

Figure 15 shows the circuit model of the applications. Based on functionality, the DAS circuits can be classified into sensing circuits (chessboard with sensors), signal conditioning and ADC circuits, and microcontroller unit (MCU) circuit.

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The circuits within DAS will be discussed first, followed by the microcontroller circuit and the WTS. The microcontroller is discussed as a separate module since it is responsible for different tasks during the two development stages. The CPS is a host PC with developed programs and will be discussed in Chapter 6.

5.2 Data Acquisition Subsystem

5.2.1 Overview

The DAS is responsible for detecting chess piece movements on the chessboard equipped with sensors, pre-processing gathered analogue signal and converting analogue signal into digital format. Digitised signal is buffered and fed into the microcontroller as indicated by the arrow in Figure 16. The wide arrows represent data flow direction within DAS.

Fig. 16. Circuit Modules

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Besides circuits that pre-process acquired information, additional circuit modules that decode control signals from microcontroller are necessary. The grey arrows in Figure 16 indicate the flow paths of control signals.

The communication between the DAS and WTS is bi-directional, so is between the WTS and CPS. Thus the DAS is able to receive control commands from the CPS. Individual circuit modules will be discussed in the following sections.

5.2.2 Chessboard with Sensors

A standard chessboard is marked with a grid of 19x19 lines, altogether with 361 crossing points. There are two types of chess pieces, namely, black and white. When a game is in progress, each player in turn places a chess piece at one vacant point on the chessboard, which is so called one movement. To detect placement of chess piece, the chessboard must be modified to install suitable sensors.

Since no sensor is able to penetrate chessboard for detecting chess piece, holes are drilled at each crossing point to allow installation of the sensors. These holes are large enough to hold sensors, but much smaller than the size of chess pieces. Hence the holes will not affect players playing games.

To fix up the sensors and install other electric components, a circuit board is installed under the modified chessboard. A board is installed at the bottom and is of the same size as the chessboard. These boards are mounted together with the circuit board sandwiched in between as shown in Figure 17 in the next page.

Fig. 17. Side Elevation of Chessboard

The sensor output level is changed when a chess piece is placed or removed from the chessboard. The sensor is not only able to detect presence or absence of chess piece, but also able to differentiate the chess piece between black and white. The chess piece is an ordinary type that is available on the market.

Due to the large number of crossing points (361 points) in a standard chessboard, a small-scale chessboard is setup for experiment purpose. During the first stage, an 8x8 chessboard is built to verify the feasibility of the application. Altogether 64 sensors are installed. These sensors form into 4 identical sensor arrays, each includes 16 sensors that form a 4x4 square. Figure 18 in the next page is the circuit diagram for one of the sensor arrays.

The sensors from the same sensor array share a common power supply unit. These sensor outputs (16 outputs) form a data bus (Vo0-VoF) and are fed into next stage.

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Fig. 18. Sensor Array Circuit

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Polling scheme is adopted to minimize power consumption. The DAS completes polling the whole chessboard every two seconds. During any polling cycle, only one sensor array is activated, while other arrays are in inactive mode. The sensors from the active array are powered up.

Four sensor arrays (0 to 3) are constructed in the first stage. During the second development stage, the chessboard is expanded to 12x12 and verifies the feasibility of expanding chessboard to standard size. Five more identical sensor arrays and the corresponding analog buffer circuit are added to complete the expansion. The rest of the circuits require no changes. In the future, expanding the chessboard is possible and can be done in the same way. The circuit diagram for the whole chessboard circuit is shown in Figure 19.

A reflective opto-switch miniature sensor is chosen. The sensor comprises of an infrared emitting diode and a phototransistor mounted in a black plastic housing. Output level of the phototransistor changes when a chess piece passes within its field of view [20]. Chess piece in different color also causes different output level.

As shown in Figure 18, a sensor consists of four pins, which are A, K, E and C. Pins A and K represent anode and cathode of the internal infrared emitting diode, whereas pins E and C represent emitter and collector of the phototransistor. The output level at Pin C is typically 4.5 V when no chess piece is present. The output level is between 0.4 to 0.5 V when white chess piece is presented. For black chess piece, the output becomes 3.1 V typically, but varies from 2 to 3.5V.

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Fig. 19. Entire Sensor Circuit

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As polling scheme is used for the chessboard, the duty cycle for each sensor is very low. A sensor will be polled once every two seconds. In considering sensor setup time and the time to stabilize power supply module, the microcontroller samples sensor outputs after the 50 milliseconds delay. The sensors will be powered up only during active mode. Hence, the active time for any sensor is less than 50 milliseconds in one polling cycle, which means its duty cycle is less than 2.5%. Power consumption is reduced by a large extent and the sensors lifetime will be extended.

5.2.3 Analog Buffer Stage

The analog signals from sensor outputs need to be buffered before performing analog to digital conversion. The purpose of this stage is to protect analog signal from interferences and keep the sensor outputs stable. The circuit diagram is shown in Figure 20.

To reduce circuit complexity without causing interference to the sensor outputs, three sensor arrays utilize a common analog buffer circuit. During each polling cycle, the sensor array and its associated analog buffer circuit will be activated simultaneously.

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Fig. 20. Analog Buffer Circuit

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5.2.4 ADC Stage

This stage converts analog signals from analog buffer output into digital format. Based on the experiment results, the threshold is set to the optimum level so as to obtain consistent digital output. The circuit diagram for ADC stage and digital buffer stage is shown in Figure 21.

There are three possible chess states each chessboard crossing point. These states are Absent, Black and White. Accordingly, there are three output states in digital format. Each state is encoded into 2 digits as shown in Table 2. The analog-to-digital conversion can be performed by using two comparators for each sensor output. The coding scheme must prevent a particular pattern from appearing within the data field of a packet. Hence, state ‘11’ is not implemented.

State	MSB	LSB
Absent	1	0
Black	0	0
White	0	1
Not Used	1	1

Table 2. Chess States Encoding

5.2.5 Digital Buffer Stage

This stage acts as a digital buffer interconnecting the ADC output and the parallel input port of the Microcontroller. The buffers hold the ADC output signal until data are ‘moved’ into the microcontroller.

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Fig. 21. ADC and Digital Buffer Circuit

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Each time a single sensor array is activated, 32 (16 sensors, 2 outputs for each sensor) parallel outputs flow out from the ADC stage. These outputs must be multiplexed since the microcontroller can only read in 8 parallel inputs at one time. The digital buffers act as the multiplexer. The illustration of signal multiplex is shown in Figure 22.

Fig. 22. Digital Signal Multiplex

The buffer circuit includes 4 digital buffers. Each buffer comprises of 8 parallel input lines and 8 parallel output lines. As shown in Figure 21, 'bit 0' output lines of the four buffers are tied together and form 'bit 0' of the data bus. The rest of the output lines are also connected together to form an 8-bit parallel data bus. The data bus connects to the input port of the microcontroller.

During the operation, the microcontroller polls the buffers in a round-robin fashion. The buffer output is enabled and the corresponding digital signals flow into microcontroller when the buffer is polled. It is important to ensure that only one buffer is enabled at any time so that data will not be corrupted.

5.2.6 Power Supply Module

The function of the power supply module is to provide controllable and stable DC current to the system. The power supply module contains multiple independent power supply units. Each power supply unit is able to turn on/off by control signal. At any time only one of these power supply units is activated to provide electric power to the active sensor array. The circuit diagram for the power supply module can be found in Figure 23.

5.2.7 Decode Circuit

This circuit module decodes the control signal sent out by the microcontroller and sends decoded control signals to the respective circuit modules. Physically the decoding circuit components are distributed in the circuits mentioned above and can be found in Figure 21 and 23.

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Fig. 23. Power Supply Circuit

5.3 Microcontroller Circuit

The microcontroller is the heart of the DAS. It interconnects the front-end signal conditioning circuits and the RF transceiver. The chip AT89C52 is chosen for this application and has been introduced in the previous chapter. Its task varies during the two development stages hence the circuits will be different. The microcontroller circuit will be discussed separately in the coming sections. However, there are some circuit blocks that are common in both development stages.

5.3.1 Common Circuit Blocks

These common circuit blocks force the microcontroller to work in normal operation. These circuit blocks are the RESET sub-circuit, Clock sub-circuit and RS232 logic level converter. The RESET and Clock sub-circuits must be included because they are required by the microcontroller.

Though AT89C52 has on-chip RS232 serial port, its logic level (TTL) is not compatible with the standard serial port logic level, which means it cannot interface directly to PC nor DR1200 development kit through serial port. The RS232 logic level converter completes conversion between the two logic levels. The circuit diagram in Figure 24 is implemented during the first development stage. The common circuit blocks are shown in this diagram.

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Fig. 24. Microcontroller Circuit Diagram for First Development Stage

5.3.2 Circuit for First Development Stage

During the first development stage, the DR1200 development kit is implemented and takes major responsibility for maintaining the wireless link. The microcontroller on the remote node focuses on gathering data from the DAS and interfaces with the kit through RS232 serial port. The circuit diagram is shown in Figure 24.

5.3.3 Circuit for Second Development Stage

During the second development stage, the DR1200 development kit is abandoned. Instead, the AT89C52 microcontroller takes the role of the kit in maintaining the wireless link as well as receiving data from the DAS. The AT89C52 chip handles all tasks such as packet coding/decoding, signal processing, flow control, and RF packet detection.

Fig. 25. Microcontroller Circuit for Second Development Stage

To transmit/receive RF signal, the AT89C52 chip connects to a data radio board that modules RF signal according to the input digital signal and demodulates received RF signal. Some electrical components are added to interface to the data radio board. Figure 25 is the snapshot of the microcontroller circuit while Figure 26 shows the circuit diagram.

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Fig. 26. Microcontroller Circuit Diagram for Second Development Stage

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5.4 Wireless Transmission Subsystem

The WTS allows the DAS and CPS communicate without the need to install any cable. The WTS is also different during the two development stages. At the first stage, the DR1200 development Kit is used for the RF link. As discussed in Chapter 4, a node includes one data radio board and one protocol board. The data radio board is responsible for signal modulation/demodulation. The protocol board has an on-board processor that implements the wireless protocol.

The protocol board communicates with the AT89C52 chip through RS232 serial port. The port setting is as follows: 19.2kbps of baud rate, 1 start bit, 8 data bits, 1 stop bit and no parity bit.

During the second development stage, the custom-made circuit board with AT89C52 chip replaces the protocol board and interfaces directly with the data radio board. Tasks supported by the protocol board in the first stage are moved into the AT89C52. Chapter 6 will discuss the firmware for the microcontroller. OOK modulation is adopted and the transmission rate of the air channel is 20kbps.

5.5 Some Design Considerations

Some important considerations should be taken during design and implementation stage. This would help to minimize circuit problems and reduce the difficulty of debugging. Especially for this analogous-digital mixed signal system, digital circuit

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may cause severe interference to the analogue portion if the circuit is not designed properly. Some of the important considerations are listed below.

- Separate analogue and digital circuit; connect the analogue ground to digital ground via a single point.
- Use coupling capacitor between power supply and ground of each chip; 100uF capacitor is used to remove low frequency interference, while 0.1uF eliminates high frequency components.
- Keep signal paths as short as possible and locate relative components as close as possible.
- Select lower operating frequency for microcontroller to reduce interferences and improve system stability.

5.6 Conclusions

This chapter focuses on discussing the hardware design and implementation of the DAS and WTS subsystems. These circuits provide the platform for software development and are the fundamental step to the development of this application. The developed circuits are shown in the figure below.

Fig. 27. Developed Circuits for WeiQi Game Monitoring

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This chapter discusses the software development and explains major tasks that are performed by the programs. The programs include the firmware that is burnt into the microcontroller and the programs that run on host PC. The firmware is written in C and assembly language using C51 Professional Developer's Kit, while the PC program is written using Microsoft Visual Basic. The software model, developed programs and RF communication protocol will be discussed in the following sections.

6.1 Block Diagram for Software Programs

Fig. 28. Block Diagram for Software Programs

Similar to the system model presented in previous chapter, the block diagram shown in Figure 28 also includes the three basic components, which are microcontroller firmware, wireless communication protocol and PC program.

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The microcontroller firmwares for the application of WeiQi game monitoring and utility meter readings are different, since they acquire data differently. However, the firmware modules that handle the wireless communication protocol are identical. The development process of the firmware for WeiQi game monitoring is discussed below.

6.2 Firmware Development

The firmware that runs on the microcontroller is critical to the success of this system. It has two main objectives. The first one is to acquire target information through the front-end circuits. The second one is to format RF packets and communicate with the other nodes obeying the RF protocol.

Similar to the development of the circuits for DAS, the firmware is also developed in two stages. DR1200 Kit is used for handling the major work of the protocol during the first stage. Thus the microcontroller focuses on gathering target information but also takes part in flow control process. During the second stage, the microcontroller has to handle all the tasks that are used to be completed by the DR1200 Kit in the first stage.

6.2.1 Firmware Development Process

The following steps are required to build the firmware for the AT89C52.

- a) Create project, select the target chip (AT89C52) and configure the tool settings
- b) Create source files in C and assembly languages using source editor
- c) Build the application with the project manager
- d) Compile and debug the programs using debugger

- e) Create HEX output file from the application and convert the file into BIN format
- f) Program (burn) the BIN file into target chip using device programmer
- g) Install target chip on the target board and test

If any problem is found or the firmware is not working as expected, step (b) to step (g) must be repeated until the firmware reaches expectation.

6.2.2 First Stage Development

The microcontroller AT89C52 is the heart of the DAS at the remote side. Since the DR1200 Kit implements some of the functions needed by the protocol, the AT89C52 focuses on managing the DAS circuit module. It is also required to process data and control packets as well as flow control. The major tasks to be performed by the AT89C52 are as follows.

- Detect and receive any signal coming from RS232 serial port
- Check for valid received packet
- Response to different types of received packets
- Perform serial port flow control
- Format packets to be transmitted
- Transmit packets to DR1200 Kit
- Control power supply module and sensor arrays
- Poll parallel input port for target data

The above functions are realized using C51 Professional Developer's Kit. The program was burnt into the chip and verified to be functioning properly.

Program Descriptions

Once powered up, the program starts the initialization process. This process initializes peripherals such as parallel I/O ports, Timer 0 (T0), Timer 1 (T1), Timer 2 (T2) and serial port. LED blinks when this process is completed.

The program setups three interrupts. T0 interrupt provides timing delay to poll sensor arrays and buffers. Once called, the service routine polls the sensor arrays and stores the data into input buffer. T1 is to provide timing information to the main program for packet flow control.

As serial port transmits characters one by one in asynchronous manner, serial port interrupt must be enabled so that the program is able to react immediately whenever a complete character is sent or received. Timer T2 is setup as a baud rate generator for serial port communication. The actual baud rate is 18.75kbps, which is slightly different from standard value. However, it is still acceptable.

The main program flow keeps checking the T1 counter, then formats and sends data packet to the transceiver after the specific time delay. The parallel port input buffer is ready for polling at this point of time.

There is a handshaking procedure before transmitting a packet. The program transmits the first byte of the packet to the transceiver. If the same byte is echoed back within 100 ms, the program will send the rest of the data packet out. The transmission process is then taken over by the serial port interrupt routine until the whole packet is

sent. The program attempts retransmission immediately if it receives no echo byte within 100 ms. Since serial port communication is duplex, immediate retransmission attempt increases the burden on the transceiver by a small amount only. This scheme reduces transmission delay and increases system throughput.

Once packet transmission is completed, the program waits for an acknowledgement (ACK) packet from the receiver. If an ACK packet is received within a specific time interval, the program discards the transmitted packet. Otherwise, the packet will be retransmitted or discarded if time out occurs.

As the main program executes, indicating LEDs blink accordingly. Along the way the program also scans RS232 serial port and checks received character for any valid packet.

Three interrupt service routines (ISR) are implemented. As the main program flow is interrupted and resumes only after the active ISR complete execution, the ISR should be made as short as possible. ISR improves program efficiency, but may cause an unexpected situation. The program must be designed very carefully so as to be able to handle all possible situations properly.

6.2.3 Second Stage Development

At remote node, the AT89C52 connects to front-end circuits and the data radio board, both via on-chip parallel input ports. Since the protocol board is removed from DAS,

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all computational burdens move to the AT89C52 chip. The firmware needs to acquire target data and implement the wireless communication protocol.

At the PC side, another AT89C52 interfaces to PC through RS232 serial port and the data radio board via parallel input ports. The firmware polls packets from the data radio board as well as forward/receive packets from host PC.

Firmware for AT89C52 at Remote Node

The important tasks for this microcontroller are as follows.

- Detect any incoming RF data stream from the data radio board
- Check for any valid received RF packet
- Response to received command packets
- ACK/NACK received packets
- Format data packets to be transmitted
- Perform packet coding/decoding
- Compute FCS checksum for error detection
- Transmit packets to the data radio board
- Control power supply module and sensor arrays
- Poll parallel input port for target data

The algorithm for acquiring data from the front-end circuits is similar to that in the first stage. However, attention should be paid to the data radio board, whose output pin RRX is being monitored continuously. Clock & Data Recovery Process is implemented to extract real-time clock and data information from received RF data stream. The algorithm is essential to system performance and will be discussed later.

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The firmware initializes on-chip peripherals such as timers, interrupts and I/O ports when it is powered up. After that, it transmits a broadcast packet twice to notify central base station (host PC) its address and status.

The on-chip timers provide timing information for polling data from parallel port. A data packet will be formatted and queue for transmission when a certain number of data bytes are collected. Packet overheads such as framing byte, address field, packet number will be added to the data bytes to construct a raw data packet. To ensure data integrity during transmission, the firmware computes the 16-bit FCS checksum and attaches FCS to the raw data packet.

After formatting a complete raw data packet, the firmware encodes the packet using byte-to-12-bit conversion so as to make the encoded RF packet DC-balanced. The coding scheme makes real-time clock recovery process possible at the receiving side and synchronization will not be lost after transmitting long sequence of data stream.

When a RF packet is ready for transmission, the firmware senses the channel to see if the medium is available. It starts transmitting the queuing packet if the channel senses idle. If the channel is busy, it defers its transmission and attempts after a random time interval.

On the other hand, reception of RF packet is started by detection of frame header from output data stream of data radio board. If the frame header is detected, the subsequent data stream will be stored into a buffer. Meanwhile, the firmware tries to decode received data stream and computes FCS checksum after the packet is completely

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received. The firmware will also check for duplication before executing received command word.

Firmware for AT89C52 at PC Side

The AT89C52 at PC side connects to host PC through RS232 serial port, and manages data radio board via parallel port pins. It is released from the burden of acquiring target data, whereas its tasks focus on handling RF communication protocol and exchanging packets between RF transceiver and serial port. Besides, it needs to response to queries from host PC. The following lists its major tasks.

- Detect any incoming RF data stream from the data radio board
- Check for any valid received RF packet
- Forward received RF data packets to host PC
- ACK/NACK received RF packets
- Format RF packets to be transmitted
- Perform packet coding/decoding
- Compute FCS checksum for error detection
- Detect and receive signal coming from RS232 serial port
- Perform serial port flow control
- Transmit packets from host PC to the data radio board

The firmware processes RF packets in a similar way as its counterpart. The difference is that it needs to monitor the serial port. If a serial port packet comes in, the firmware replies if the packet is a query packet. Or it will format a RF packet and transmits to the remote node if a command packet is received.

If a valid RF packet destined for host PC is received, the firmware will strip off packet overheads such as RF frame header, FCS checksum and form a serial port packet by attaching framing byte. It will acknowledge the sender while forwarding the serial port packet to host PC.

6.2.4 Real-time Clock & Data Recovery

During wireless transmission, jitter may occur due to noises presented in RF channel. The effect of jitter blurs data edges, which means zero crossing points (or threshold crossing points) of input signal may shift forward or backward. This brings difficulties in determining where data bit intervals occur. In order to receive RF packets properly, real-time clock recovery algorithm is implemented to synchronize RF receivers with the proper starting point of the received radio data stream.

The implemented algorithm tries to find out the proper data edge by averaging a number of data edges in time, since the jitter is caused by random noise. It samples data output pin (RRX) of the data radio board several times during a bit interval. A sample counter counts up and flips when it reaches the ceiling. It is estimated that a data threshold crossing point would occur at the midpoint of sample counter without jitter. However, the actual point occurs beyond/before the midpoint of the count under the effect of jitter. Thus, an offset is added or subtracted from the counter so as to shift the midpoint towards average data edge. As such, the optimum sampling point can be found and the effect of random noise is minimized.

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A RF framing pattern is used in conjunction with this scheme. The pattern '55H' is 12-bit binary data stream at the beginning of every packet. Effectively this scheme implements a virtual software clock and minimizes the effect caused by random noise. Thus accurate clock information and data can be extracted from received data stream. Receivers can be synchronized with extracted clock information, thus data bits can be determined. Meanwhile, receivers start receiving RF packet right after detecting the framing pattern. The subsequent data outputs are based on the sample taken at the mid point of each data bit in time.

Another algorithm resets the timer to one and a half bit time whenever a bit "1" (or Low to High state transition) is received while it is monitoring the wireless channel. The subsequent samplings take place at the mid point of every data bit according to the timer and the receiver starts to look for framing pattern. If the framing pattern is detected, the receiver will receive the whole incoming packet. Else the receiver will discard the incoming data and continues to monitor the channel. This scheme is easy to implement but is vulnerable to jitters caused by noise. In addition, the sampling may not occur at the exact mid point of a data bit. The error can be accumulated and cause sampling error if the incoming packet is sufficiently long in length.

The other simple clock and data recovery algorithm was also experimented. This algorithm starts receiving process right after a bit "1" (or Low to High transition) is detected. It samples several times during a bit interval and tries to take the average of the sample outputs. For example, the algorithm samples a data bit five times at the equal interval. If the sampling results are all "1"s, the output is "1". If the sampling

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results are two “1”s and three “0”s, then the output becomes “0”. This process will continue until all data bits are received.

This algorithm reduces the effect caused by strong burst interference. Burst interference may cause one or two sampling errors within a bit interval, thus its effect is mitigated. However, this scheme is vulnerable to inaccurate sampling time and random noise, as these errors can be accumulated and cause wrong output. Additionally, this scheme consumes more computational resources whereas its performance is not advantageous over the first algorithm.

6.2.5 Conclusions

Many problems occur during the firmware development process. The major difficulties are real-time clock & data recovery process and multi-tasking. Many tests have been conducted to find out an efficient and stable algorithm for clock and data recovery.

Handling multiple tasks simultaneously is not an easy job. The firmware has to scan the serial port and data radio board for any incoming packet. Some tasks such as RF data bits reception require immediate response from the firmware. Otherwise the data bit will be lost or corrupted. Therefore, such operation requires high priority. It is very important to allocate all possible tasks/events properly.

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The majority of the firmware is written in C language. To improve efficiency, in-line assembly language codes are used for some functions. In addition, data memory area is utilized efficiently to optimize the firmware.

6.3 Wireless Communication Protocol

6.3.1 Overview

During the first development stage, the protocol that is similar to pure ALOHA was implemented. The protocol features auto-retransmission scheme to ensure that destination is able to receive packets properly.

During the second development stage, the single-hop wireless communication protocol that was discussed in Chapter 3 was implemented. The protocol was modified to improve network throughput. The main improvement is the implementation of CSMA algorithm.

For CSMA, a node remains silent when it is in waiting state. If a node has a packet to send, it will listen to the channel to see if the channel is idle. If the channel is idle, the node starts transmission immediately. In case another node is transmitting, the node defers its transmission and listens to the channel after a random period of time. CSMA algorithm reduces the possibility of packet collision, and studies had been conducted and found that network throughput of CSMA was improved over pure ALOHA [21], which was implemented during the first development stage.

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The RF transceivers sharing a single channel are governed by the implemented protocol. Due to the nature of wireless communication, it is impossible for a transceiver to hear the channel while it is transmitting. Hence the communication system is half duplex, which means only a single direction communication is allowed at one time. A transceiver has to be able to switch between transmit and receive modes quickly. In most of the time, a transceiver stays in receiving mode and monitors the channel continuously. A transceiver changes to transmit mode only when it has a packet to send.

Each node has a 4-bit address that can be set manually. This provides 15-address space, while address 0 is reserved for broadcasting. By means of address routing, a node is able to talk with any other node within its transmission range. For this application, most communications will be between host PC and remote nodes.

6.3.2 Flow Control

Due to the complexity and high requirements on hardware, sliding window flow control is not suitable for the application. Instead, the protocol implements stop-and-wait flow control. After a single packet is transmitted successfully, the transmitting node waits for an ACK packet from the receiving node. The node will try to retransmit the same packet if it doesn't receive ACK packet after the time-out period. However, the pending packet will be discarded in case the maximum number of retries has been reached. At the receiving side, the node sends back an ACK if it receives a packet correctly. For WeiQi game monitoring, a node sends a packet only after a fixed time interval. It is unlikely that a node has more than one pending

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packets at one time. Hence, a simple stop-and-wait flow control works well under this situation.

When a remote node is powered up, it broadcasts a packet to inform the host PC (base station) about its node address and status. After receiving the broadcast packet, host PC acknowledges the remote node. The node information will be shown on the PC display. Operators can change the node status to start/stop monitoring a chess game by sending the command packets. The flow control procedure is shown in Figure 29.

Fig. 29. RF Protocol Flow Control

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The node that receives Start command from host PC turns into data collection mode and transmits data packets to host PC periodically. Figure 29 depicts a scenario where the ACK packet is lost or corrupted during transmission. The flow control process establishes a reliable wireless communication link.

RS232 serial protocol is applied between host PC and RF transceiver. The packet format and flow control are different from RF communication. If host PC has a packet to send, it formats a RS232 packet by adding packet headers and transmits the first byte of the packet to transceiver. The transceiver echoes back the same byte if it is idle. Host PC transmits the rest of the packet to the transceiver. The transceiver will forward received packet to host PC immediately after it receives a valid packet. The communication between host PC and transceiver will be discussed in PC program section.

6.3.3 Packet Format

RF Packet Format

The RF packets exchanged between transceivers include message portion and packet header. Figure 30 shows the packet format for the major types of RF packets.

Preamble is a special sequence that will not appear anywhere else within the packet. The sequence not only reminds receiver incoming of new RF packet, but also helps in clock and data recovery process. If the pattern of preamble appears within the body of a received packet, the packet is in error and will be discarded.

Data/Control Command Packet

Preamble	To/From Address	Packet Number	Packet Size	Message	FCS
----------	-----------------	---------------	-------------	---------	-----

ACK/NACK Packet

Preamble	To/From Address	Packet Number	IDS	FCS
----------	-----------------	---------------	-----	-----

Fig. 30. RF Packet Format

To/From address field contains destination node address and source node address. If the byte is filled with 0x00, it is treated as a broadcast packet. The packet will be broadcasted two times and will not be acknowledged by ACK/NACK packet. In some cases, the packet will be re-broadcasted after a defined period of time.

The packet number byte uses 1 to 126 repeatedly as the sequence number. ACK packet should include the packet number that is being acknowledged. A sequence number of 127 implies a telemetry packet. Telemetry packet is not implemented in this application but reserved for the future application.

For data and control command packets, Packet Size field determines the size of message field. It is removed from ACK/NACK packet since the packet size is fixed.

Message field contains data bytes or control command bytes. This is also called payload in communication system. The IDS field in ACK/NACK packet tells what type of packet it is. Last but not least, the FCS is a 16-bit long field that contains calculated FCS checksum for error detection.

Serial Port Packet Format

The serial port packet format is different from radio packet format. Figure 31 shows the respective packet format as defined by the firmware.

Data Packet Format

To/From Address	Packet Number	Packet Size	Framing Byte	Message	Packet Ending
-----------------	---------------	-------------	--------------	---------	---------------

ACK/NACK Packet Format

To/From Address	Packet Number	IDS
-----------------	---------------	-----

Fig. 31. Serial Port Packet Format

Compared with RF packet format, the preamble field is removed. Instead, a Framing byte is inserted before Message field. The framing byte is 0xC0 in hexadecimal. This framing pattern is unique and will not appear within any other fields. The message field can have up to 31 data bytes. In this project, it is fixed to be 22 bytes, including 20 data bytes and 2 overhead bytes. Hence, the length of one data packet is 26 bytes. The Packet Ending is 0x0D0A and it informs the other party that the packet has reached the end.

There are other special packet formats. For example, query packet originated from PC to request for local node address and the query reply packet. Other types of packets can be defined to cater for more features.

6.4 PC Program Development Process

The host PC that acts as base station of the system is the central management point for the application. PC programs allow system operator or WeiQi game referee monitor and manage remote nodes in real-time. PC programs are written using Microsoft Visual Basic and provide a graphical user interface. The following sections discuss the program flow chart and individual module.

6.4.1 PC Program Flow Chart

Several function modules make up the developed host PC program. For this application, the modules include serial port communication module, database module, application data processing and data displaying modules. For a system that can be used for multiple applications concurrently, the serial port communication module is a common module to all applications. Regardless the type of applications, all incoming and outgoing packets can go through this module by the same interface.

Fig. 32. PC Program Flow Chart (Receive)

The flow chart in Figure 32 shows the entire process of receiving RF packets for WeiQi game monitoring.

After receiving a complete packet from the RF module, the serial port communication module determines which application the newly arrived packet intends for by examining the contained application number. Application number '1' is for WeiQi

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game monitoring, while other numbers are for other applications. Then the program differentiates the packet type and process accordingly.

Fig. 33. PC Program Flow Chart (Transmit)

Figure 33 shows the process of transmitting a serial port packet to the RF module and waiting for the reply.

6.4.2 Serial Port Communication

The communication between host PC and attached RF transceiver follows RS232 serial port protocol. The module that is responsible for serial port communication scans the port from time to time to check for any incoming packet. This module of program is shared by all applications. If a valid packet is detected, the module determines which application the packet should be forwarded to.

Transmission of a packet is different from reception. After an outgoing packet is formatted, this module sends out the first byte of the packet and waits for acknowledgement. If the same byte is echoed back, the rest of the packet will be sent out through serial port. An RF packet is constructed and transmitted through the wireless channel. The firmware will then inform host PC the RF packet status (either ACK/NACK, time-out/lost). The PC program would follow the reception process as described above.

6.4.3 Application Data Processing

This program module needs to differentiate different types of packets and processes them in different ways. For broadcast packets, the program recognizes sending node address and sends back a command packet to acknowledge the node. For status packets (ACK/ NACK packet) the program will response accordingly. For data packets, it will strip off packet headers and save data bytes into a buffer. This module also processes operator inputs such as control commands.

6.4.4 Application Data Displaying

The program module is responsible for presenting data in a graphical manner. Besides, the program automatically calculates start time and duration of the game being monitored. User can edit information and record the game into database. This module is also able to replay past games recorded into database.

6.4.5 Database

A relational database is designed and implemented for the application using Microsoft Access. It is able to store/retrieved steps of WeiQi games. The database uses SQL (Structural Query Language) for updating or deleting records. SQL is the standard language for relational database management systems. SQL statements are implemented to sort and filter out unwanted records.

6.4.6 Multiple Concurrent Applications

The system is able to manage multiple applications concurrently. The application of utility meter readings has been implemented into the same system. It has its unique remote nodes but shares the same wireless channel and base station. Its remote nodes also include sensors, signal processing circuit and a microcontroller. Different types of microcontroller can be chosen. This application will be discussed in the Appendix.

These applications share the common program module for serial port communication. Received packets will be forwarded to the respective application for further process.

6.5 Conclusions

This chapter discusses the software program development. It includes the details in developing the firmware for microcontroller, PC programs running on host PC and the wireless communication protocol. The firmware is developed in two stages. Due to task differences, the firmware for remote node is different from the one for the node attached to host PC.

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Many experiments have been conducted to test the performance of the system during the two development stages. Experiments on transmission BER (Bit-Error-Rate) have been completed and the results are presented and discussed. Estimations on system transmission capability and hardware circuit delay are presented in this chapter.

7.1 Wireless Channel BER vs Distance

Compared with wired system, wireless communication system is more susceptible to external interferences. Performance degradation of wireless channel can cause system performance to drop significantly. It is of great importance to study the performance of wireless communication subsystem.

BER (Bit-Error-Rate) is commonly used to measure a communication system. During the second development stage, a number of experiments have been conducted to measure the performance of the wireless communication subsystem. The implemented protocol does not have error correction capability. Thus, the system is setup to measure BER of the wireless channel under different test conditions.

7.1.1 Experiments Setup

Some experiments are conducted to simulate the real operational environment of WeiQi game competition. In reality, several chessboards will be setup inside a

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competition hall, which is usually less than 20 by 20 meters. The two players will sit nearby whereas the wireless transceivers will be located near the WeiQi chessboards. It is expected to find no other large obstacles appear around the area.

During the experiments, the transmitter (remote node) sends packets continuously while increasing its distance to receiver. On the other hand, the host PC together with the attached node (receiver) is fixed at one point of the laboratory. More than 20 million sample bits were received. The received bits were compared with the original bits to compute BER and evaluate sources that may cause transmission errors.

The experiments have been setup to evaluate the relationship of BER against distance between the transmitter and receiver. There are many equipments and PCs inside the laboratory conducting experiments. In order to test system performance under normal condition, these equipments and PCs are operating as usual without being shut down purposely.

The first series of experiments are conducted in an indoor environment to simulate the actual operation of WeiQi game competition. These experiments are completed inside the laboratory while the transmitting distance is increased. Direct light-of-sight signal propagation path may or may not exist between transceivers.

The purpose of second series of experiments is to study the effect of human body near the transmitting antenna. A human body blocks the direct path between the transmitter and receiver. These experiments are to simulate the case where the players may sit between the direct communication paths between transceivers. The distance between

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the transmitting antenna and human body remains 20 cm. These experiments are also conducted inside the same laboratory.

The third series of experiments measure BER with a concrete wall between the transmitter and receiver. The main objective is to study the effect of heavy boundaries on communication link and also the potential interferences generated on neighboring transceivers. The receiver is placed inside the laboratory and the transmitter is outside the laboratory. The concrete wall is 1 meter away from the transmitting antenna.

Some experiments have been done to measure the BER performance at open space. The open space is clear to ensure no building or obstacle lies between the transmitter and receivers. In addition, within 10 meters range there is no large obstacle around the transceivers to reduce the effect of signal reflection.

7.1.2 Experiment Results and Discussions

The results for the first and second series experiments are presented in Table 3. The distance between the transmitter and receiver are 1.5 meters, 5 meters and so on. The maximum distance is limited by the dimensions of the laboratory.

Distance (m)	1.5	5	10	15	20	25
BER (Indoor)	6.96 E(-5)	7.85 E(-6)	1.50 E(-7)	8.36 E(-7)	3.21 E(-6)	9.29 E(-5)
BER (Human Body)	2.04 E(-6)	3.84 E(-7)	7.79 E(-7)	2.12 E(-6)	2.30 E(-6)	2.42 E(-4)

Table 3. BER vs Distance (Inside Laboratory)

As seen from Table 3, the experimental BER is found to be varying in the order of 10^{-7} to 10^{-5} . The BER limit is in the order of 10^{-7} for communications links less than

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15 meters. At 25 meters away, BER is in the order of 10^{-4} . The system performance drops slightly with the presence of human body. Generally speaking, the result shows that BER increases as distance.

However, in some cases inconsistency occurs. For example, the BER at 1.5 meters is worse than that at 5 meters. The received data bits are examined. It is found that most of the transmission errors occur within one or two short periods of time, while very few error bits are found outside these periods. This implies that these errors are most likely caused by strong burst interferences originated from other equipments. For the first experiment where the transmitter is 1.5 meters apart from the receiver, the error bits are found to appear within a one-second time interval but no error bit is found outside this time interval. Similar situations can be found for the case where the transceivers are located 5 meters apart.

For other cases, the error bits tend to spread randomly and in general BER increases as distance increases. These randomly distributed error bits are most likely caused by random noise. As such, the BER performance will drop dramatically if external interferences are present during the experiments and much higher BER value is expected. It is foreseen that BER performance will become more consistent when experimental data sample becomes larger.

The presence of human body downgrades BER performance but the effect is not significant. Similarly, BER value increases dramatically whenever burst interference is present, which is shown by concentrated error bits within a short period of time.

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Any equipment operating in near frequency band can become the potential sources of interferences. Mobile phone that operates at GSM900 band and PCs are possible sources. The system proves to be robust since only very few packets are found to be corrupted when strong external interferences present.

Table 4 shows the result for the third series of experiments. The concrete wall blocks the signal propagation path between the transmitter and receiver.

Distance (m)	3	5	8	10	15	20
BER	7.24 E(-6)	8.67 E(-5)	6.32 E(-4)	1.02 E(-3)	8.55 E(-2)	7.23 E(-2)

Table 4. BER vs Distance (With Wall Boundary)

Compared with previous experiments, the BER value is increased to a much higher level. It can be seen that the BER increases rapidly with distance. At 8 meters, the packet error rate can be approximated by:

$$6.32 \times 10^{-4} \times 336 = 0.212$$

where the number of data bits in one data packet is 336.

The above result shows that out of 5 received packets, more than one packet will be corrupted. As the transmitter moves away from the receiver a little bit further, it is expected that most packets will be corrupted.

The error bits are randomly distributed in time except a few concentration points. It is of high possibility that these concentrated error bits are caused by strong external interferences.

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The reduction of effective transmission range is because the concrete wall attenuates the RF signal significantly. As received RF signal level is very low, the RF receiver has difficulty in decoding data bits from random noise and interferences. Hence BER will increase dramatically.

Table 5 shows the result for experiments conducted in open space area. There are no obstacles in between the transceivers, neither within the range of 10 meters.

Distance (m)	5	20	40	60	80	100
BER	2.07 E(-7)	4.75 E(-6)	5.61 E(-4)	7.27 E(-5)	2.70 E(-4)	7.84 E(-4)

Table 5. BER vs Distance (Open Space)

The BER performance downgrades as transmission distance increases. It is in the order of 10^{-7} when transceivers are placed close. The performance drop at 40 meters is most probably due to burst interference after examining the error bits pattern.

At the distance of 60 meters, the packet error rate can be approximated by:

$$7.27 \times 10^{-5} \times 336 = 0.024$$

where the number of data bits in one data packet is 336.

At the distance of 100 meters, BER is much higher. The packet error rate can be approximated by:

$$7.84 \times 10^{-4} \times 336 = 0.263$$

where the number of data bits in one data packet is 336.

It can maintain a reliable communication link when the distance reaches 60 meters, but cannot meet the requirement of the prototype system at 100 meters distance due to its high packet error rate.

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However, packet error rate can be reduced if smaller packet size is adopted. For example, the packet error rate becomes

$$7.84 \times 10^{-4} \times 100 = 0.0784$$

when the number of bits in one packet is 100. As the performance of wireless communication is susceptible to external interferences, the transceiver is not recommended for creating reliable communication link above 80 meters in open space.

7.1.3 Conclusions on Experiments

The experiments evaluate the performance of the WTS under different conditions without implementing error correction code. The results show that the performance of wireless transmission subsystem is satisfactory within laboratory environments. Light obstacles such as human body do not significantly affect system performance. The system covers a range of 25 meters within laboratory environment and extends to 60 meters in open space environment. However, a number of transmission errors occur with the presence of strong interferences.

When heavy obstacles such as concrete walls isolate the receiver and transmitter, system performance is dropped dramatically. BER increases very fast as the distance increases.

7.2 System Capacity Estimation

7.2.1 Computation Capability of AT89C52

The AT89C52 microcontroller operates at 12 MHz, which gives the ability to execute a single instruction in 1 or 2 μ s. The firmware uses interrupt driven approach for data input and output. The firmware is capable of multi-tasking and gives priority to time-critical tasks. Hence, program efficiency is improved.

System performance is evaluated using the software simulator. The result shows that the microcontroller is able to complete all tasks as required. In general its computation capability fulfills system requirements. The firmware module that receives and transmits RF packets consumes most of the computation capacity. This implies that a faster microcontroller should be chosen to achieve higher wireless transmission rate.

7.2.2 Data Payload Estimation

The system design is based on a standard chessboard that has 361 (19x19) chess pieces. A standard chessboard can be divided into 25 identical smaller sensor arrays, which has 16 (4x4) chess pieces. Each chess piece is represented in 2 binary data bits, hence a single sensor array will be encoded into 32 (4x4x2) data bits, or 4 bytes.

The application is designed to refresh data, or complete polling the whole chessboard once every 2 seconds. This refreshing rate would be appropriate as players usually think for a long time before making a placement. Dummy data bytes will be inserted

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to keep all data packets the same length. To monitor one WeiQi game, the system must be able to transmit 100 (25x4) data bytes successfully within one polling cycle.

For radio communication system, error is likely to occur during transmission and a single bit error can damage the whole packet. It is wiser to transmit short packets rather than long ones. Another factor that limits packet length is the internal data memory size of AT89C52. Due the limited buffer size, the length of a data packet must be less than 30 bytes. Otherwise memory overflow problem will occur. Hence data bytes will be broken into 5 groups, each is 20 bytes and is carried by one data packet.

7.2.3 Wireless Transmission Capability

Each RF data packet carries 20 data bytes plus packet overheads. The overheads include RF preamble, address field, packet number, FCS and so on. The total number of packet overheads is 8 bytes. The length of a complete RF packet is 28 bytes. After applying byte to 12 bit encoding technique, RF packet length becomes 42 bytes.

An ACK packet will be transmitted back by receiving node if the data packet is received correctly. The length of an ACK packet is 6 bytes. The packet becomes 9 bytes long after encoding.

There are 5 data and 5 ACK packets to be exchanged within each polling cycle. The minimum number of bytes to be transmitted through wireless channel is:

$$5 \times 42 + 5 \times 9 = 255 \text{ bytes}$$

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Hence the minimum wireless transmission rate required is:

$$(255 \text{ bytes} \times 8 \text{ bits/byte}) / 2 = 1020 \text{ bps, or } 1.02 \text{ kbps}$$

The utilization level of wireless channel is:

$$1.02 \text{ kbps} / 20 \text{ kbps} \times 100\% = 5.1 \%$$

In a network system, offered traffic includes new and retransmitted packets due to packet collision and other types of transmission errors. The offered traffic will be slightly higher than 0.051 at the utilization level (or throughput) of 0.051 [22]. It shows that the number of retransmitted packets is very small for the implemented CSMA protocol. In another word, the probability of packet collision is very low. The system will be able to transmit collected data within specified period of time.

7.2.4 Serial Port Transmission Capability

Different from wireless channel, serial port communication is full duplex. The chance of packet collision is eliminated. Received data packets or ACK packets are forwarded to host PC, while control command packets are transmitted at the opposite direction. To be compatible with the radio packet protocols, each host packet is formatted to include 20 data bytes and some packet overheads. The packet length is 26 bytes, including 6 bytes of overheads. The length of control command packet is 8 bytes.

The serial port will finish transmitting 5 data packets in one polling cycles. The minimum number of data bytes is:

$$5 \times 26 = 130 \text{ bytes}$$

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According to RS232 specification, each byte is transmitted in a 10-bit character frame format. Hence, the estimated minimum transmission rate for data bytes is:

$$130 \text{ bytes/s} \times 10 \text{ bits/byte} / 2 \text{ second} = 650 \text{ bps}$$

The estimated serial port utilization is at this level:

$$725 \text{ bps} / 18.75 \text{ kbps} \times 100\% = 3.87\%$$

It is expected that very few control command packets will be sent out. Hence much lower transmission rate is required for the serial port from host PC to attached RF transceiver.

In considering the possibility of additional packets other than data packet, actual traffic intensity will be slightly higher. But it will be much smaller than the actual serial port capacity, which is 18.75 kbps.

From the above calculations, it is found that the serial port will be able to handle data stream arising from a single remote node without any difficulty. It is foreseen that the system is able to manage a small number of remote nodes.

7.3 System Delay

System delay concerns with hardware circuit delay and software delay. The issue of software delay has been rectified by carefully designing firmware and PC programs. This section concerns about hardware circuit delay only. Here circuit delay refers to time lag between the point where control signal is sent and the point desired data is

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ready at input port of the microcontroller. The delay mainly comprises of two portions: setup of circuit components and signal propagation time. The system should take into account the delays when designing DAS circuits.

Delay may cause problem in data acquisition module. As seen from Figure 34, there are two major loops that may produce significant delays. Loop one is the signal path for the microcontroller to poll buffer circuits, while loop 2 is the signal path for the microcontroller to poll sensor arrays on the chessboard.

Fig. 34. Circuit Delay Loops

The setup time of various hardware components can be obtained from datasheets. For signal propagation along wires, the maximum propagation time for Loop 1 is 3 ns. This is obtained by assuming the propagation speed for electrical signal along wires is around 2×10^8 meters per second. The maximum time lag for loop 1 is 125 ns, which is much less than the minimum software execution time $1 \mu\text{s}$. It is no harm to insert software delay ($4 \mu\text{s}$) before the microcontroller fetches data from its input port.

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Longer delay is expected for loop 2 because of its longer signal flow path. The measured time delay by oscilloscope is 1.5 ms. The main reason to this delay is the long setup time of sensors. Therefore, software delays must be inserted by the firmware to account for the circuit delay.

As verified by the experiments, the delays are handled properly. The system works as expected.

7.4 Experiment Results

The system is setup for verification of its functionality. A WeiQi game is played at the remote side. The game is monitored and acquired data is transmitted back to host PC through wireless channel. Host PC displays the game and manages remote nodes.

7.4.1 Test for First Development Stage

The DR1200 Development Kit is used for communication through wireless channel. The circuits and programs are proved to operate effectively. The system is able to monitor real-time WeiQi game and is capable of managing remote nodes from host PC.

The system has joined the university's College of Engineering Exhibition, 2004. The system for the exhibition is shown in Figure 35. Besides the application for monitoring WeiQi game, the system also implements the application for utility meter readings. The application for utility meter readings has been co-developed by another

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student group and is discussed in the Appendix. Three remote nodes transmit data to host PC simultaneously. Host PC proves to be able to process and present the received data.

Fig. 35. System Setup for CoE Exhibition

7.4.2 Test for Second Development Stage

During the second development stage, custom-made RF circuits replace the DR1200 Development Kit. The WeiQi chessboard size is expanded to 12x12. In the future, the chessboard can be expanded to standard chessboard size by adding sensor arrays in the same way.

Experiments have been conducted inside and outside the laboratory to verify system performance as well as to measure BER of the wireless channel. The experiments are completed to simulate the expected operating environment of the system. The channel BER is kept at a very low level and is shown to be satisfactory. The hardware circuits and software programs are able to operate as designed. The implemented wireless

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communication protocol maintains a good communication link between remote nodes and host PC.

Additional experiments show that the system correctly monitors the placement or removal of chess piece within two seconds, which is one of the design parameters. In general, the result shows that the system is able to operate properly in real environment and meets design requirements.

CHAPTER 8. CONCLUSIONS AND RECOMMENDATIONS

8.1 Conclusions

In this report, the concept and system model of wireless data collection system were presented. A wireless data collection system was proved to be capable of supporting diversified applications. In addition, it was shown that the system was able to integrating multiple applications simultaneously.

The application of monitoring real-time WeiQi game was implemented for the system. Applications of utility meter readings were also implemented. The system was implemented in two development stages. Experiments were conducted to evaluate system performance. The following points were proved based on the experiments.

- Hardware circuits operate as specified by design objective. The circuits are able to complete targeted tasks under the control of software programs.
- The implemented firmware and PC programs fulfil the requirements. Host PC becomes central management point of the system.
- The proposed wireless communication protocol governs access to the wireless channel and maintains a robust communication link between transceivers.
- The feasibility of integrating different applications into a single wireless data collection system is verified.

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In summary, the wireless data collection system concept was verified. The implemented system was proved to be functioning as designed.

8.2 Recommendations for Future Work

Though the implemented system exhibits satisfactory result, there is still much room to improve the prototype system. Some recommendations are listed as follows.

- The implemented system does not take into account the issue of data security. For some applications, encryption may become an important issue in order to keep unauthorized users outside the system. Some widely used encryption techniques include Block Ciphers and Stream Ciphers.
- Due to hardware limitations, the implemented wireless protocol is for single hop communication, which means all remote nodes talk to base station directly. To communicate with nodes at distant location, the multi-hop protocol should be implemented to provide larger coverage area.
- A more powerful microcontroller may be chosen to implement these new features. The new microcontroller should have stronger process power so as to handle more complicated tasks and increase wireless transmission rate. In addition, it should have larger data memory size so as to be able to allocate larger buffers for RF packets.

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- Due to limitations of available equipment, experiments on evaluating maximum RF channel capacity cannot be conducted. It is recommended that experiments be conducted to find out maximum number of nodes the system can support.

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APPENDIX

System for the Application of Utility Meter Readings

The system for the application of utility meter readings is integrated into the prototype system. It is a small-scale application and is mainly for outdoor purpose. The system also contains the common subsystems of a wireless data collection system. The figure below shows the system model of the application.

System Model for the Application of Utility Meter Readings

The remote agent acts as the data acquisition subsystem and interfaces to the wireless transceiver through RS232 serial port. The wireless transmission subsystem (WTS) consists of the nodes from DR1200 Development Kit and the wireless communication protocol. The central processing subsystem (CPS) is a host PC with developed control programs. In this application, the CPS is able to retrieve, store and present utility meter readings on the data terminal.

APPENDIX

The development of the data collection system is divided into the host and agent elements. The host element comprises mainly the implementation of the host software, while the agent element comprises the designing, construction and testing of the hardware, as well as the implementation of the agent firmware.

Remote Agent

The remote agent contains the sensors, analog-digital conversion (ADC) module, display module and the microcontroller together with its firmware. The sensors convert quantities such as liquid/gas flow-rate and volume or count the number of revolutions made by the rotating disc of a power meter into analogous electrical signals. The ADC module then converts analogous signals into digital pulses that can be recognized by the microcontroller. The microcontroller pre-processes the data and sends to the CPS wirelessly.

At the core of the remote agent system is a Microchip PIC16F877 Microcontroller. Running at a clock speed of 20 MHz, it is capable of performing the required data capture, outgoing frame generation and display functions needed by the application.

The purpose of the display module is to enable the user to view the values of the selected channel using the five 7-segment LEDs. A total of 4 channels and 4 different units are implemented.

The agent hardware was developed with the aid of a Microchip In-Circuit Debugger (ICD) development kit that utilizes the in-circuit debugging capability of the

PIC16F877 and Microchip's In-Circuit Serial Programming (ICSP). The figure below is a snapshot of the remote agent circuit.

Remote Agent Circuit

The firmware of the microcontroller decides the tasks that the agent needs to perform. The main task is to update the reading at each of its input channels. The firmware also handles the display of data onto the display module. Apart from these tasks, it is able to receive and execute commands from the CPS.

To maximize the efficiency and response speed of the system, interrupts are used to handle communication, input counting as well as other time critical operations. The firmware employs the use of a main loop to perform non-time critical tasks such as the displaying of data, channel selection and outgoing packet generation.

In summary, the agent acts as a remote data-logger, capable of sampling both analog as well as digital signals via its 4 input channels simultaneously. The sampled data is placed into a data frame and sent to a host computer via the transceiver.

Host PC Program

The CPS is a host PC that controls and coordinates activities of the remote agents. It is responsible for storing data received from the agents into a database and presenting this data to the user via the graphical user interface system. The figure below is the screenshot of the user interface.

ScreenShot of the User Interface on Host PC

The host software is developed using Microsoft Visual Basic. The programs include several software modules, which are the module for transmitting/receiving packets through serial port, the data processing module, the data display module and the database. The received meter readings can be displayed on the screen graphically or stored into database. Billing information can be calculated based on the collected data.

Protocol

The system requires bi-directional communications between the CPS and agents. As the transceivers communicate with each other using the same frequency, packet collision will occur if more than one transceiver transmits simultaneously. To prevent or at least minimize the occurrence of collisions, media access control is required to ensure that only one host application transmits. The implemented protocol is a random access protocol with the features of flow control, auto-retransmission and error detection. The protocol ensures a reliable wireless communication link between the host PC and remote agents.

Conclusion

The project has developed a wireless data collection system that is capable of logging 4 channels of data simultaneously onto a host computer. The system was successfully interfaced to an actual power meter and a liquid flow transducer. It was demonstrated during Nanyang Technological University's College of Engineering Technology Exhibition during the period of 9 – 13 March 2004. The demonstrated system was proved to be able to interface to utility meters, but also able to retrieve and store game moves from a digital Weiqi game board. Sharing of the wireless channel was made possible by the implementation of a media access mechanism.