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Junction Field Effect Transistor – based Optical Sensor

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2008

DECLARATION OF ORIGINALITY

I hereby declare that the research recorded in this thesis and the thesis itself was composed and originated entirely by myself in the Division of Microelectronics, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore and has not submitted for a higher degree to any other university or institution.

Other people who have contributed significantly to this work are acknowledged at the appropriate places in the thesis text.

Date

Mihaela Carp

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SUMMARY

Optical colour monitoring is essential in many medicine and biology-related applications where absorption/transmission in the visible range is studied. It is thus important to realize and employ good colour detectors which can correctly quantify in measurable units the optical and chromatic changes that appear in the transmission/absorption of the analyzed sample. Other important applications include food or textile dye characterization, high-density information storage and electro-photographic copying of documents.

The most well known photosensors, such as photodiodes and phototransistors, detect optical luminous intensity. These optical sensors provide an electrical output which is dependent on the intensity of incident light, but do not supply any information which can determine unequivocally the spectral composition of the incident light.

Standard colour sensitivity is achieved by employing three neighboring but independent detectors, each covered with a filter (typically a dyed polymer). Such a triad can then provide the desired full colour information in red (R), green (G), and blue (B) signals. Other colour sensors have been proposed, and in most of the cases they have a multijunction structure, with at least three junctions, and often more than three. Each junction detects the wavelengths of light situated in a certain range and, therefore, such devices can provide all the useful information regarding the spectral distribution of the incident light.

This thesis explores an entirely novel type of colour sensors, based on the Junction Field Effect Transistor (JFET) structure. The starting point is the dependence on wavelength of the silicon's absorption, combined with a two-junction structure configured in a JFET. The JFET was specifically chosen because of its key advantageous features:

- 1) It has a simpler structure than a 3-junction device, yet it can still delimitate 3 regions in which 3 different wavelength ranges can be identified to provide RGB output signals;

- 2) Insensitive to surface effects, such as interface traps occurring at the oxide-semiconductor interface. As a result, the noise level associated with the current fluctuation due to capture and release of free carriers at the surface is very low.
- 3) The two gate isolated terminals of the JFET allow two different input signals to be applied simultaneously for signal-mixing purposes.
- 4) The JFET I_{DS} current is made up predominantly by majority carriers, and thus the response speed is not limited by the minority carrier charge storage such in a bipolar transistor.
- 5) When used as a sensor it can work in three operational modes: photoconductive (with Source and Gate shorted), photovoltaic (i.e. as photodiode, with Source and Drain shorted) and like a phototransistor (with Gate biased, as a normal JFET).
- 6) It can operate beyond the cutoff voltage V_{GC} , resulting in a photo-response independent of almost all the device parameters, including chip area, so that no loss performance occurs for very small area devices.
- 7) Compatibility with standard silicon processing, which makes the integration of the sensor with read-out circuits possible in “smart” sensor chips.

The layout design and the practical fabrication of the color sensors are introduced followed by the practical measurements of the device structure parameters, and the electrical and optical characteristics of the fabricated color sensors.

Five novel colour sensing structures are designed starting from the basic JFET structure, in order to simplify the whole processes and improve the color responsivity of the initial basic JFET structure or other operational parameters. The electrical and optical characteristics of these devices are then analyzed through device simulations and compared with each other.

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Chapter ONE: INTRODUCTION

1.1. Color Sensors—Historic background and motivation

Without light, life as we know nowadays would not exist. From a scientific point of view light is the electromagnetic radiation visible to the eye, or in a more general sense, any electromagnetic radiation with wavelengths in the 400...700 nm range between ultraviolet and infrared. The three parameters of light most important for human sight and photodetectors in general are:

- Intensity, perceived by humans as the brightness of the light,
- Frequency (or wavelength), perceived by humans as the color of the light,
- Polarization (or angle of vibration), which is not perceivable by humans under ordinary circumstances but which, apparently, is important for some insects (bees and butterflies), and
- Phase. This latter parameter of light waves is most difficult to detect (also not perceived by human eye) but can be very important in certain application like holography [1].

The scientific analysis of color began with Sir Isaac Newton when he used a prism to disperse a small beam of white light into its component colors. In modern times Albert Einstein and Max Planck proved that one also can assign corpuscular properties to the electromagnetic radiation, thus establishing the dual nature of light which can be considered either as a wave or as consisting of a flux of photons, each photon carrying an amount of energy proportional to the frequency.

The detection of light based on its intensity is relatively simple. However, in many cases one is interested to determine some information related to the spectral composition of the incident light, and for a human observer this is immediately related to the notion of color. The main difficulty in the quantitative estimation of color arises from the fact that it is, at least partially, a subjective reaction to a specific visual stimulus. Attempting to attribute exact numbers to the combined responses of the human eyes and brain when excited by visual stimuli is very difficult. One reason for this difficulty is that the eye's

retina samples colour using only three broad bands, roughly corresponding to red, green and blue light.

Fig. 1.1. Light splitting prism

Furthermore, the signals from these colour sensitive cells (cones), together with those from the rods (sensitive to intensity only), are combined in the brain to give several different “sensations” of the colour. In other words, the human eye is a practical implementation of the tri-chromatic theory which describes how a mix of three separate spectral components (like red, green and blue in the example of the human eye), can match any visible colour—in this case by using three colour sensitive sensors.

From a historic point of view, sensors were initially designed to detect the light intensity. The photoconductor, or the photocell, was the first quantum photodetector developed after a long period of having only thermal photodetectors (in order to detect radiation in general metal bolometers were used as early as 1880, with platinum as the most common material). Photoconductivity was discovered by Smith in 1873 in selenium [2]. The photoconductor was appealing due to its simple structure, low cost, and rugged features. For these reasons, it was quickly adopted and is still used quite widely in applications for visible light such as photographic meters, flame/smoke/burglar detectors, card readers, etc. Extrinsic photoconductors can extend the long wavelength limit without using materials of very narrow energy band gap, and they are used as popular infrared detectors.

Chronologically, the next developed device was the *p-i-n* photodiode. The *pn* junction, developed in late 1940s, was used for many photonic devices such as photodiodes, solar cells, and LED's. The *p-i-n* photodiode, developed in the late 1950s, is an improvement over the regular *pn* photodiode. The importance of light absorption in a wide depletion region of a *p-i-n* structure was first addressed by Gartner in 1959 [3]. Further analysis of its performance as a photodetector and the fabrication using Ge was made by Riesz [4]. The *p-i-n* photodiode is common used in audio and video compact disc players, and in fiber optics communication systems. The *p-i-n* structure is also the most common detector for nuclear radiation among other semiconductor devices which

can be used as nuclear radiation detectors, such as the pn junction, the Schottky barrier diode and the photoconductor.

The phototransistor is a bipolar junction transistor that amplifies the photocurrent collected by its built-in junctions. It was proposed by Shockley et al. in 1951 [5] and it was first demonstrated by Shive in an n - p - n Ge structure in 1953 [6]. The advantages of the phototransistor were low cost, high gain and –in a subsequent stage- compatibility with integrated circuit technology that would evolve later. However, due to its low speed and inferior linearity it is used most commonly as a light sensitive switch in less-demanding systems. Heterojunction phototransistors have improved the speed and provide higher gain, but currently they are too costly to be commercially feasible for the common large scale applications of phototransistors, such as object and position detectors.

All the devices enumerated above are variations developed starting from on based on one or more p - n junctions. At the same time, they formed the starting point for other photosensors. Each of the above mentioned devices had been realized for a special purpose. Their design considered slightly different device physics, aspects, and consequently, their resulting structures are different. However, they all share in common the fact that they detect the light intensity and not the color of light, although in principle any of them may be used to develop simple color sensors.

The simplest way to conceive a color sensor is to realize an array of identical photosensing cells, i.e. pixels. Each pixel would comprise of three independent photosensors, with each photosensor detecting one primary color. Therefore, the easiest implementation uses coloured filters obtained by depositing different polymer dyes on top of three identical photosensors placed horizontally one next to another in a mosaic-like arrangement [7]. However, this *classical approach* of realizing a colour sensor has two important *disadvantages*:

- 1) *It employs polymer dyes as colour filters.* This can lead to inherent variations in the selectivity of the filters, due to the unpredictable and irreproducible aging of the polymers. Moreover, errors would appear in the correct pick-up and interpretation of the colours in the incoming light if small photolithographic errors shift the polymer mosaic pattern with respect to the underlying photodiode pattern thus resulting in Moiré effects;

- 2) *Three (or at least two) photodiodes are necessary for each element,* which leads to a large area occupied by one entire pixel, and thus determines a higher cost of the final device.

Nowadays, the requirement for color sensors is increasing since they have become a familiar part of our everyday lives, e.g. in digital and videos cameras. Emerging markets for simple typical applications include color reflectance photometers that detect changes in the colors of substances used in medicine (such as blood and urine analyses) [8] and other similar devices for bio/chemical applications. A distinctive place is devoted to hemoglobin measurements (indicating the blood oxygen content) that are carried out almost exclusively using such colorimetric methods.

Besides medicine and biology, colour measurement is important in printing or cosmetics industries, as well as in the food industry, either for quality estimation or for automatic selection of products. For instance, the reflectance of beef meat varies in time with its freshness (i.e. the exposure to oxygen). Similar analyses can also be performed on other foods, e.g. milk, orange or strawberry juice, or peach nectar for diagnosis of their storage conservation or for estimation of their alimentary properties [9-11]. However, for liquid samples the spectrometric absorbance measured with a through-sample light transmission method is more appropriate and thus the most often employed.

In the beginning, the main boost for the research and fabrication of optical sensors was given by solar cell and solid state camera applications. In the past few years, the color sensors based on CMOS manufacturing technology have begun to gain real market share. Perhaps ironically, MOS-based imagers predate CCDs (still the most often used imaging technique) by several years [12], but at the time the large geometries of the manufacturing technology made the pixel size much larger than that achievable in CCDs, which soon surpassed MOS-based imagers in terms of resolution. Today, sub-micron CMOS technology has removed this disadvantage and CMOS-based sensors can compete in terms of pixel size, while the cost of the process development does not have to be born by the color sensor development alone. CMOS-based imagers allow a higher level of integration than CCDs, because the technology allows standard CMOS analogue and digital circuitry to be implemented on the same device. However, such image sensors (CMOS and CCDs) are used mainly for single chip video and television cameras using arrays of photosensors covered by polymers (as described above) and not for the specific and targeted detection of color [13-15].

Besides digital cameras and television, an increasing interest for color sensors had appeared in optical communications, for high speed detectors for glass fiber communications with a high sensitivity in the part of spectrum where the glass fiber is optimally transparent. However, presently the favored wavelength for optical fiber

communication is 1.55 μm , and at this wavelength the silicon bandgap prevents photodetection whereas compound materials like InGaAs perform quite well. This explains the current shift of interest from silicon *p-i-n* photodiodes to detectors based on III-V or II-VI compounds for telecommunication applications.

Most of the color sensor devices were developed gradually and will be detailed in Chapter 3. For the moment it is worth highlighting here only one of the latest color detectors proposed by R.F. Wolffenbuttel [16], because it consists of a photodiode for operation in the visible spectrum integrated with electronic readout circuits and two different interfaces to a sensor bus system, all realized in a BIFET process. The output signal of the basic readout circuit is a series of pulse with their frequency proportional to the intensity of the incident light by modulating the duty cycle of an oscillator. On-chip electronic circuits have been designed and integrated together with the sensor for operating with a large dynamic range and a relatively small chip area. Photodiodes with different spectral responses have also been fabricated on a single chip in a standard CMOS process. Initial measurements on these devices have shown that the same readout principle can be used in CMOS technology. In CMOS technology a much smaller die area is needed if the sensor, the readout circuits and the digital interface are integrated on a single chip. [16]

Making a comparison between the evolution of light detectors in general and that of the color sensors in particular, one can conclude that the development of light detectors was based on the diversification of basic devices while color sensors appeared simply as an extension, a mere quantitative modification passed on the usage of an increased number of sensors in conjunction with polymeric filters and with using improved signal conditioning circuits, typically integrated on the same chip with the sensor or the imaging array. Therefore, it becomes quite clear that there is a need to design and develop a more effective color sensor with a simple signal processing circuit yet exhibiting more operational modes so that it could be easily applicable to multiple applications in various situations. An example of one such important application for bio/chemical purpose is the optical monitoring of absorption/transmission in the visible range through a studied sample of cells, tissue or solution, by employing colour sensors. In conclusion, it is very important and economically relevant to realize and employ good colour detectors as they allow quantifying in measurable units the colour received from an analyzed sample.

The immediate main aim of the project work described in this Ph.D. dissertation is to design novel colour sensors which can be used in (micro) systems capable to perform

accurate colour discrimination. The innovative contribution brought by this work is the study and design of a completely new and original type of color-sensing devices based on JFET structures and which is different from any of those reported in literature [17, 18]. As it will become evident from the other sections of this thesis, the photo-JFET offers certain key advantages over other similar devices, which are also listed in the subsequent Section 1.3.

1.2. Human vision and color sensation

Color, in its purest definition, is a combined physical and perceptual phenomenon. In order to understand how colour sensors work one must first consider human vision and to understand how it works.

Our perception of color arises from the composition of light, i.e. the energy spectrum of photons which enters the eye. In the eye, the photodetectors are concentrated on the retina, as shown in Fig. 1.2 [19]. The retina is a mosaic of two types of photoreceptors, rods and cones. Rods have their peak sensitivity at a wavelength of 498 nm and are used for vision under dark or dim light conditions. The rods are effective in sensing differences in light intensity -the flux of incident photons- not photon energy. This is why in dim light we perceive colored objects as shades of gray, not shades of color [1].

Our basic color vision is due to three types of cones: L-cones (red) with a peak sensitivity at 564 nm, M-cones (green) with a peak sensitivity at 533 nm, and S-cones (blue) with a peak sensitivity at 437 nm. The detailed curves for spectral sensitivity of each cone type are shown in Fig. 1.3 [20].

Cones are highly concentrated in a region near the center of the retina called the fovea. The maximum concentration of cones in the fovea is roughly 180,000 per square mm and this density decreases rapidly outside the fovea to a value of less than 5,000 per square mm. It is worth mentioning the existence of the blind spot caused by the optic nerve, which is void of any photoreceptors.

The standard definition of normal visual acuity (20/20 vision) is the ability to resolve a spatial pattern separated by a visual angle of one minute of arc. Since one degree contains sixty minutes, a visual angle of one minute of arc is 1/60 of a degree. The spatial resolution limit is derived from the fact that one degree of a scene is projected across 288 micrometers of the retina by the eye's lens.

Along a distance of only 288 micrometers, there are 120 color sensing cone cells packed one next to another. Thus, if more than 120 alternating white and black lines are

crowded side-by-side in a single degree of viewing space, they will appear as a single gray mass to the human eye.

Fig. 1.2. The human eye and the photodetectors located in retina [19].

Fig. 1.3. The basic type of photoreceptors: rods and cones and the response of the tree cones to incident light: cone R (pigment R) has a maximum sensitivity in the orange-red, cone G (pigment G) in the green-yellow, and cone B (pigment B) in the blue portions of the visible spectrum. The sensitivities of the three cones overlap and the perceived color is due to the relative response of the three cones [21].

Finally, it may be interesting to mention that, given the selectivity curves shown in Fig 1.3 and the relative numbers of each type of cone in the retina, for a beam of light to be considered as "white" by a human observer it must be made up of 11 % blue, 30 % red and 59% green (=100%). [19]

In conclusion, in order to ensure a straightforward solution for the most convenient usage one can imagine that the spectral sensitivity of our color sensor must present responses for the three primary colors at least similar with the sensitivities of the cones in the human eye. This would enable the color sensor to exhibit the same color discriminating capabilities and would also allow one to unambiguously identify and characterize each possible color with the help of the chromaticity diagram, as it will be detailed later in section 2.1.3.

1.3. Objectives of the thesis

Many of the colour sensors that have been proposed until now have used at least three junctions, and often more than three.

Other photosensing devices which have also been reported were designed of used for detection of light, especially the intensity and its spectral distribution, for information storage and in the electro-photographic reproduction of documents.

The JFET-based structure has been chosen in this work for developing colour sensors because it offers the following key advantages:

- Attractive, due to its simple structure and a simpler fabrication process than that required for multi-junction structures, while the same time allowing easy fabrication compatibility with standard CMOS processing;
- Exhibits a high gate impedance;
- The illumination-induced effects are not based on, or influenced by surface effects, such as interface traps occurring at the oxide-semiconductor interface. As a result, the photogeneration and collection of optically generated minority carriers is enhanced while at the same time the noise level associated with the current fluctuation due to capture and release of free carriers at the surface is very low because the device operation is not limited only to the surface of the device but uses the entire bulk of the semiconductor;
- Offers the capability to achieve tri-color discrimination using a simpler structure, comprising of less than 3 vertically stacked junctions because the information related to colours are all generated in one and the same detector, thus saving precious chip area: three different pixels (one each for the

detection of R, G, and B) are no longer needed as a single pixel can provide simultaneously all the colour information from a single location;

- The carrier transport in JFET is predominantly due to by majority carriers, and thus the response speed of a JFET is not limited by the minority carrier charge storage as in a bipolar transistor;
- Provides the possibility to use two independent gates to control the depletion region in channel and therefore enable different operation modes, depending on the desired application. Specifically, a JFET-based colour sensor can provide 3 different modes of operation:
 - o **Photoconductive mode:** this is obtained by connecting a resistor between the gate and the source, and the speed of response is basically determined by the capacitance of the gate region and the value of this resistor. This resistor or resistance may be formed within the same IC structure together with the JFET device formed by for example, diffusion, or using, polysilicon;
 - o **As a 'normal' phototransistor** (with the gates biased, as any usual JFET); and
 - o **Photovoltaic mode** (i.e. as a photodiode):, when the source and drain are short circuited together
- The isolated two gate terminals of a JFET structure also allow two different input signals to be applied simultaneously for signal-mixing purposes;
- It can operate beyond the cutoff voltage V_{GC} , resulting in a photoresponse independent of almost all the device parameters, including chip area, so that no loss performance should occur for very small area devices;
- It uses not only photogeneration, but in the channel region it also employs photoconductivity modulation, due to the modification of the resistivity of this region induced by the photogeneration of carriers;
- As a silicon based color-sensor with a quite simple structure it offers a very good compatibility with standard silicon processing, which makes the integration of the sensor with read-out circuits possible and straightforward. Furthermore, such Si-based sensors could also be easily integrated in novel types of architectures, e.g. in MEMS microsystems for characterization of bio/medical compounds/cells. Such a "smart" sensor could provide direct microprocessor-compatible output signal

- Unlike MOS-based devices (e.g. CCDs), JFET-based ones are extremely radiation-stable, i.e. their characteristics and performance is barely degraded in the presence of high energy radiation. This makes the JFET-based colour sensing pixel extremely attractive for space- and military-related applications, in this specific case particularly for usage in imaging arrays.

Consequently, the work carried out in this project and described in this dissertation had the following main objectives:

- Perform a thorough literature review and patent search regarding various optical and/or colour sensors in general and with specific focus on the JFET-based ones;
- Develop a detailed theoretical analysis of the operation of the JFET in order to better understand its operation modes not just as-is (i.e in darkness) but also to comprehend the effects that manifest upon illumination and therefore deduce their dependence on various geometrical dimensions or other device parameters (e.g. doping, junction depth, etc.)
- Carry out MATLAB simulation in order to visualize and plot the variation of the most important operational characteristics on the key device parameters;
- Verify the correctness of the developed equations and of the MATLAB results with FEA simulations using TCAD process and device simulations with TSUPREM and MEDICI. These simulations would also provide the final processing steps for the desired sensor structures as well as provide much more accurate modeling of the effects that affect the absorption of incident light and collection of the photogenerated charge carriers, as well as their wavelength dependences. Thus these simulation are vital in order to optimize the device structure(s) and its/their key features, such as the spectral response(s) and the effectiveness of the electrical control on these spectral response(s);
- Practical fabrication in the MFL cleanroom of NTU's EEE School;
- Measurement and testing of the realized devices.

1.4. Breakdown of the Thesis

This dissertation is organized into seven chapters. This first chapter described the background of the research, gave a brief introduction into the topic, and explained the targets and organization of this thesis.

Chapter 2 describes in more detail the fundamental aspects of semiconductor-based photodetectors and of photodiode physics, the *pn* junction-based structures relevant for color sensing and the development of new materials and structures for color sensors.

The existing literature is also reviewed, and the advantages and disadvantages of the different reported approaches are compared.

Chapter 3 describes the design of color sensors employing JFET-based structures based on both optical and electrical considerations. Then the fabrication process of these color sensors is designed theoretically. Furthermore, process modifications are made through computer simulations, in order to realize the desired devices with optimal spectral responses, and to achieve compatibility with a 2 μm standard CMOS process.

Chapter 4 details the optical and electrical virtual characterization of the color sensor designed and simulated in the previous chapters. Using advanced TCAD device simulations with TSUPREM and MEDICI, the main photoelectric parameters characterizing the designed color sensors, such as the photocurrents of the pn junctions, the spectral responses and the I-V curves for each junction or device region would be obtained and discussed.

The layout design and the practical fabrication of the color sensors based on both the theoretical model and the simulation model will be introduced in Chapter 5, followed by the practical measurements of the device structure parameters, and the electrical and optical characteristics of the fabricated color sensors.

Chapter 6 introduces five novel structures, designed starting from the initial basic JFET structures, in order to address their drawbacks and to improve their characteristics, such as the spectral response. Their electrical and optical characteristics obtained from TCAD simulations, will be presented, analyzed and compared with each other.

Chapter 7 presents the key findings and conclusion of this research. A critical discussion of the advantages and disadvantages of all the new JFET-based color sensors described in this thesis is also given. Finally, this chapter also makes suggestions for future work.

Chapter TWO: Fundamental and Theoretical Aspects. Literature Review

This chapter is intended to be a scientific introduction to the multiple aspects that are crucial for the complete understanding of the newly proposed JFET-based color sensors. Specifically, this chapter will review the basic physics and solid-state devices employed for photosensing and especially for color sensing, as well as highlighting the important differences between the proposed JFET-based color sensor and other previously reported color sensing devices.

2.1- Light, color and vision

The perception and comprehension of light and color involve the need to understand not only some of the basic laws of physics but also to identify and realize the often hidden ways in which the electromagnetic radiation, especially the visible light, interacts with matter, particularly with semiconductor materials. A good understanding of all these phenomena would then provide a good platform for understanding the concepts of color and how it can be detected in solid-state devices.

2.1.1- Light: Photons and Waves

Light is an electromagnetic wave and one color's spectral signature in the visible spectrum is dictated mainly by its wavelength.

The placement of the visible range of wavelengths (400–700 nm) in the whole electromagnetic spectrum is shown in Fig. 2.1. Infrared and radio waves are situated at the long wavelength (i.e. low photon energy) end whereas the ultraviolet (UV), X-rays and gamma rays lie at the short wavelength (i.e. high photon energy) end of the electromagnetic spectrum. The eye cannot sense radiation with wavelengths shorter than 400 nm and longer than 700 nanometers.

One can describe light either as electromagnetic waves, or as a stream of minute packets of energy –**photons**– which create a pulsating electromagnetic disturbance. A single photon of one color differs from a photon of another color only by its energy.

Fig. 2.1. The full electromagnetic spectrum, which also encompasses the visible region of light, extends from gamma rays with wavelengths of 10 Å to radio waves with wavelengths of one meter or greater [22].

A moving wave can be described by its **frequency** or number of cycles (or variations) per second, as well as by their **wavelength**. The velocity v , wavelength λ and frequency f (or its reciprocal, the wave period T) are related by

$$v = f\lambda = \frac{\lambda}{T}, \quad \text{in } \left[\frac{\text{m}}{\text{s}} \right] \quad (2.1)$$

As is well known, all electromagnetic radiation propagate through vacuum at a constant speed $c = 3 \times 10^8$ m/s.

2.1.2- Vision and color—a short history

The different wavelengths are detected by the human eye and then interpreted by the human brain as colors, ranging from red at the longest wavelengths (lowest frequencies/energies) to violet at the shortest wavelengths (highest frequencies/energies). The other intermediary frequencies are seen as various other colors and hues, depending on the specific mix of wavelengths of various intensities into which the original light can be decomposed.

The scientist Abu Ali al-Hasan ibn al-Haytham (965-c.1040), also known as Alhazen, developed a broad theory that explained vision, using geometry and anatomy, which stated that each point on an illuminated area or object radiates light rays in every direction, but that only one ray from each point, which strikes the eye perpendicularly, can be seen. The other rays strike at different angles and are not seen. Alhazen held light

rays to be streams of minute particles that traveled at a finite speed. Alhazen's work did not become known in Europe until the late 16th century [23].

Pierre Gassendi (1592-1655), an atomist, proposed a particle theory of light which was published posthumously in the 1660s. Isaac Newton studied Gassendi's work at an early age, and preferred his view to Descartes' theory of the *plenum*. He stated in his *Hypothesis of Light* of 1675 that light was composed of corpuscles (particles of matter) which were emitted in all directions from a source [23].

Thomas Young (1773-1892) did significant work on capillarity and the theory of elasticity; however it is for his optical work that he is chiefly remembered. His earliest work (1791) was in physiological optics in which he sought to explain how the eye functioned. He argued that the lens of an eye changed shape to focus light as necessary. He discovered the cause of astigmatism and in 1801 he suggested that the retina responded to three 'principle colors' only which combined form all the other colors. At the time when Young submitted his trichromatic theory, many artists had long known that they could mix all color shades by using three primary pigments; physicists, however, were still influenced by Newton's claim that the seven colors emanating from a prism are elementary (and therefore not mixable) [24].

In line with Thomas Young, Hermann von Helmholtz (1821–1894) first of all arranges the spectral colors on a curved line (Fig. 2.2) in order to achieve a better understanding of their mixtures. He imagined a kind of force field of colors —the color field— with white in the middle, corresponding to Newton's gravitational centre. Helmholtz noticed that in order to obtain white, he did not require equal quantities of violet-blue and yellow, for example. He thus arranged his colors in such a way that those complementary colors which were required in greater amounts were given greater "leverage" [25]. His main publication was the *Handbuch der Physiologischen Optik* (*Handbook of Physiological Optics*) and appeared between 1856 and 1867, with the English translation appearing 60 years later to world acclaim. Here, Helmholtz introduced the three variables which are still used to characterize a color: hue, saturation and brightness.

He was the first to unequivocally demonstrate that the colors which Newton had seen in his spectrum are different from colors applied to a white base using pigments. The spectral colors shine more intensely and possess greater saturation.

Fig. 2.2. The first spectral color arrangement proposed by Helmholtz [22].

They are mixed additively, whereas pigments are mixed subtractively, hence a different set of rules governs their combination in each case.

Another fact that increased the credibility of trichromatic theory appeared in 1855, when George Wilson of Edinburgh presented the first statistical analysis of color blindness.

In 1859, Maxwell, then 28 years old, presented his Theory of Color Vision, acknowledged as being the origin of quantitative color measurement (colorimetry). In this work, Maxwell demonstrated that all colors arise from mixtures of the three spectral colors —red (R), green (G), and blue (B), for example — on the assumption that light stimuli can be both added and subtracted. He allocated each of the three main colors to the corner of a triangle, into which we then placed a curve of spectral colors which is provided with technical data. A line of this type will reappear later in the CIE System. This is important, because all associated insights go back to Maxwell who, with his triangle, introduced the first two-dimensional color system based on psychophysical measurements [27].

Maxwell now became aware that the brilliance of a multicolored surface is relatively insensitive to changes in brightness, and was able to totally eliminate this as a determining factor by introducing the new parameters r , g and b , arrived at by dividing each tristimulus value by the total summed value of all primary stimuli: $r=R/(R+G+B)$, $g=G/(R+G+B)$, and $b=B/(R+G+B)$. These new color coordinates fulfill a simple condition: their sum is one ($r + g + b = 1$). This means that all their possible combinations can be represented as points within an equilateral triangle—the Maxwell triangle.

Fig. 2.3. The Maxwell triangle: (A) A white neutral point located in the center, (B) The result of a mixture of three colors [28].

Since their tristimulus values, or their color coordinates, add up to one, the triangle enables us to predict the result of a mixture of two colors (see Fig. 2.3). All possible combinations of any two colors will lie on the line connecting their respective positions within the triangle. Naturally, Newton's circle had already specified the results of color mixing. But Maxwell's achievement was that the geometrical relationship and spacing between the colors in his triangle have a precise meaning, based on psychophysical measurements.

With the aid of the point for white, Maxwell was able to specify three new variables – similar to H. von Helmholtz – which characterizes a color: the "hue", the "tint" and the "shade". Maxwell also showed how easy it is to form a link between these variables and portray colors as the sum of three primaries. The limitations of this triangle, incidentally, soon became apparent: its values are based on comparisons of pigments, but the light of spectral colors can be much more intense.

If all the spectral colors, together with the purple hues, are to be recorded in Maxwell's diagram, then his triangle must either be extended or reconstructed. The final result of this attuned method is the CIE system that will be detailed in the next section.

Even today, because machines alone cannot distinguish between yellow or red, the measurement of colors continues to be a difficult task without the usage of a dedicated color sensor. As always, the human being is alone in his ability to decide. It is into his eyes that light falls, and from his eyes that the world is viewed.

In conclusion, the spectral sensitivity of our color sensor should – in principle – provide three primary responses similar with the sensitivities of the cones in the human eye.

2.1.3- Color-measurement systems

Color measurement systems characterize colors by “decomposing”, them i.e. expressing them as a function of independent variables that relate to the color’s characteristics, like hue, saturation, and brightness. Such systems include the subjective Munsell and Ostwald systems and the quantitative CIE color system.

After Maxwell’s effort, another system was developed by the American painter Charles Munsell between 1905 and 1916. Munsell attempted to account for each color attribute in ordered visual steps. He introduced 100 steps for color "hue", starting with five main colors and five additional colors, and adopted an ordering system with 10 units of color "value" and an open scale called "chroma" (similar to saturation) [29]. The resultant three-dimensional system, shown in Fig. 2.4, can best be portrayed as a "color-tree" and is based on the principle of "perceived equidistance", to use the correct, although rather long technical term, and it is one of the most widespread —and nowadays most utilized— color-systems.

Ostwald wanted to achieve "harmony" with colors and verify whether a corresponding law could be formulated. With his analysis of color-harmony, Ostwald proceeded on the basis of his conviction that harmony is created by color-order. A double-cone is put forward with one white and one black tip between which a stepped grey-scale is arranged, modeled according to a fundamental psychophysiological law. The double-cone extends from a color-circle divided into 24 segments (the full colors) which in turn stem from the four proto-colors of yellow, red, blue and sea-green (Fig. 2.5) [30].

Despite the fact that science does not provide us with information about the harmonious combination of colors in the same way as with sounds Ostwald’s system nevertheless left its mark in the world of art: for example, the Dutch "De Stijl" movement with Piet Mondrian at its centre focused on his work — at any rate, Mondrian's treatment of colors in 1917 and 1918 had much in common with Ostwald's theories [30].

Using three parameters or attributes to define a color makes the color analysis more convenient as one can think of these parameters as forming a "color space" in analogy with the three spatial dimensions. Three "coordinates" (e.g. R, G, B) would then fully specify a color.

Fig. 2.4. The three-dimensional color system of Munsell [25].

Fig. 2.5. Ostwald's system: A color-circle (a) extends into a double-cone (b) [30].

Fig. 2.6. CIE chromaticity diagram [31].

In 1931 the International Commission on Illumination (usually known as the CIE, an abbreviation of its French name “Commission International de l'Eclairage”) defined a standard system in which all the tristimulus values would be positive and in which all visible colors could be unambiguously represented by two chromaticity coordinates x and y . Mapping the visual colors led to the now familiar horseshoe curve in the x, y plane known as the CIE chromaticity diagram. It is the basis for most quantitative color measurement at present.

The starting point for the creation of the CIE chromaticity diagram was provided by Grassmann's (1853–1854) laws, which have been rephrased in a modern formulation by Hunt [32]:

1. *To specify a colour match, three independent variables are necessary and sufficient.*
2. *For an additive mixture of colour stimuli, only their tristimulus values are relevant, not their spectral composition.*
3. *In additive mixtures of colour stimuli, if one or more components of the mixture are gradually changed, the resulting tristimulus values also change gradually.*

The mathematical formulations of Grassmann's laws of additive color matching are as follows [1]:

1. Symmetry law: If color stimulus A matches color stimulus B , then color stimulus B matches color stimulus A .

2. Transitivity law: If A matches B and B matches C , then A matches C .

3. Proportionality law: If A matches B , then $\alpha \cdot A$ matches $\alpha \cdot B$, where α is any positive factor.

4. Additive law: If A , B , C and D are any four color stimuli, then if any two of the following three conceivable colors matches hold:

$$A \equiv B, C \equiv D, (A + C) \equiv (B + D) \quad (2.2)$$

then so does the remaining match

$$(A + D) \equiv (B + C) \quad (2.3)$$

where $(A+C)$, $(B+D)$, $(A+D)$ and $(B+C)$ denote additive mixtures of A and C , B and D , A and D , B and C , respectively.

These laws are often called the stronger form of trichromatic generalizations of color matching. There are some constraints that have to be considered if Grassmann's laws are applied:

1. Matches have to be always made under similar observational conditions. If an observer sets a match where the fields have different spectral compositions, the match will not necessarily hold if he moves his eye, does not look centrally at the fields, or the sizes of the fields are changed.

2. The light exposure of the eyes will affect the state of *adaptation*. Although the persistence of colour matches is rather high, the spectral sensitivity of the eye can be influenced at very high irradiation levels.

3. If a larger area of the retina (e.g. a 10° field) is used for colour match, a failure of the proportionality law is found.

2.1.3.1- The RGB color space

Any set of three colors which when added in appropriate combination will yield white can be considered to be primary colors. It is useful to map the color space with a set of primaries like blue (B), green (G), and red (R). If unit amounts of B, G, and R produce white light, then they can be used like unit vectors to define the color space. The coordinates of a point in space defines a color C by

$$C = b \cdot \vec{B} + g \cdot \vec{G} + r \cdot \vec{R} \quad (2.4)$$

The coordinates b , g and r are called the tristimulus values with respect to that set of primaries. Early research was done with a specific set of RGB primaries, also called

reference color stimuli, or primary stimuli, or primaries: 700 nm, 546.1 nm and 435.8 nm and at certain magnitudes of these selected reference color stimuli [33].

The units of the three primaries have been set to such values that their mixture should provide a color match with an equal-energetic white test stimulus, i.e. a stimulus for which the same amount of power is irradiated ($\frac{dS(\lambda)}{d\lambda} = S_\lambda = \text{spectral resolution} = \text{const.}$) at every wavelength in the visible spectrum. Taking a luminance of 1 cd/m² of red light as 1 red unit, then 4.5907 cd/m² of green and 0.0601 cd/m² of blue light have to be added so that their mixture of them matches exactly the equal-energetic white stimulus of 5.6508 cd/m². Thus the chosen three new units have the following luminances:

Table 2-1. Luminance of the selected R, G, B matching stimuli [34]

red:	1,0000	cd/m ²	= 1 new R unit
green:	4,5907	cd/m ²	= 1 new G unit
blue:	0,0601	cd/m ²	= 1 new B unit

If between 380 nm and 780 nm all the monochromatic radiation of equal power within a small wavelength band are matched with the combination of the $\vec{R}$, $\vec{G}$, $\vec{B}$ primaries, the so-called *colour matching functions* (CMF) $\bar{r}(\lambda)$, $\bar{g}(\lambda)$ and $\bar{b}(\lambda)$ are obtained as shown in Fig. 2.7 [34].

If monochromatic test stimuli are used, one observes that e.g. a 520 nm green stimulus cannot be matched by any combination of the three matching stimuli. One comes nearest to the match only if blue and green matching stimuli are used, but an exact color match can only be obtained if some red light is mixed to the test stimulus:

$$C(520 \text{ nm}) + r \cdot \vec{R} \equiv b \cdot \vec{B} + g \cdot \vec{G} \quad (2.5)$$

where ‘ $\equiv$ ’ means ‘exact match’, i.e. the colour mixture of given amounts of the green and blue matching stimuli will fully correspond to the mixture of the test and red stimuli. Mathematically, the fact that one of the primaries light is mixed with the light of the test stimulus (instead of being added with the other two matching stimuli) means that a negative sign has to be used for that stimulus:

$$C = b \cdot \vec{B} + g \cdot \vec{G} - r \cdot \vec{R} \quad (2.6)$$

It should be, however, quite clear that this does not mean “negative red light”!

The R , G , B tristimulus values of a stimulus with $P(\lambda)$ spectral power distribution are [35]:

Fig. 2.7. The $\bar{r}(\lambda)$, $\bar{g}(\lambda)$ and $\bar{b}(\lambda)$ color-matching functions of the CIE 1931 Standard Colorimetric Observer [34].

$$R = k \sum_{380 \text{ nm}}^{780 \text{ nm}} P(\lambda) \bar{r}(\lambda) \Delta\lambda, \quad G = k \sum_{380 \text{ nm}}^{780 \text{ nm}} P(\lambda) \bar{g}(\lambda) \Delta\lambda, \quad B = k \sum_{380 \text{ nm}}^{780 \text{ nm}} P(\lambda) \bar{b}(\lambda) \Delta\lambda \quad (2.7)$$

or using the integral form

$$R = k \int_{380 \text{ nm}}^{780 \text{ nm}} P(\lambda) \bar{r}(\lambda) d\lambda, \quad G = k \int_{380 \text{ nm}}^{780 \text{ nm}} P(\lambda) \bar{g}(\lambda) d\lambda, \quad B = k \int_{380 \text{ nm}}^{780 \text{ nm}} P(\lambda) \bar{b}(\lambda) d\lambda \quad (2.8)$$

where k is a constant that can be used to couple the colorimetric (photometric) quantities to the radiometric ones: as seen from Table 2-1 the luminance of a colour matched by the amounts of R red units, G green units and B blue units will be [35]:

$$L = \vec{R} + 4.5907\vec{G} + 0.601\vec{B} \quad (2.9)$$

This means that the constant k can be chosen in such a way that if $P(\lambda)$ is a radiometric quantity, the L value will be a corresponding photometric quantity, e.g. if $P(\lambda)$ is measured in $[\text{W}/(\text{sr}\cdot\text{m}^2)]$ then L will be provided in $[\text{cd}/\text{m}^2]$.

To visualise a trichromatic colour system, the $\mathbf{R}$, $\mathbf{G}$, and $\mathbf{B}$ primaries can be thought of as the basis vectors of a three dimensional vector space. Figure 2.8 shows such a representation. Here a plane has been drawn where the $\vec{R}$, $\vec{G}$ and $\vec{B}$ vectors have unity values.

Fig. 2.8. Schematic representation of the RGB colour space: C is a colour stimulus, and a plane has been drawn where the primaries have unit values; r and g are the chromaticity co-ordinates of C in this plane [35].

From this representation it is also easy to see that only colour stimuli that lie within the tetrahedron drawn up by the three basic vectors can be produced by means of a simple additive mixture. For all other stimuli, thus also for most of the monochromatic ones, one of the basic primaries has to be given negative values, i.e. in the colour mixture one of the primaries has to be mixed to the test stimulus to achieve an exact colour match. This is equivalent with the finding in Figure 2.7 that the $\bar{r}(\lambda)$, $\bar{g}(\lambda)$, $\bar{b}(\lambda)$ functions show negative lobes, and that at the wavelengths of the matching stimuli two of the functions are always zero, and a single one shows positive value.

2.1.3.2- The XYZ color space

The same color which can be decomposed and expressed using the $\bar{r}(\lambda)$, $\bar{g}(\lambda)$, $\bar{b}(\lambda)$ functions can also be quantitatively matched to the CIE primaries and expressed in terms of the CIE chromaticity coordinates, which are the historical color matching functions deduced by painstaking experiments. They can be used to reliably predict color perception, and most applications now use the CIE system.

In 1931, experiments were performed to determine how a standard human observer perceives color. The experiments were done by projecting lights onto a screen and having an observer match one light using a combination of red, green, and blue lights. The observer changed the amounts of red, green, and blue light projected onto the screen so that the created light spot would match the single test light. In a few cases, one of the three matching stimuli had to be projected on the test light to be matched in order to

achieve an exact match, which was, in essence, subtracting light from the matching lights. These experiments were done with the observer having a very small (two degree) field of view (first condition related to third constrain of Grassmann's law).

The curves generated from these data were mathematically manipulated so that all the curves were positive and one of them (y) was equal to the luminosity function (the way humans perceive brightness). The resulting curves, x , y , and z , are referred to as the CIE 2° Standard Observer functions.

In 1964, similar experiments were performed using a larger (ten degree) field of view. At that time, more was known about the anatomy and function of parts of the eye and it was determined that the 10° field of view would be a better indicator of how color is actually perceived by humans than the two degree field of view. Thus, the CIE 10° Standard Observer functions were created.

The three dimensional colour space is a sub-space of this spectrum space, where any three independent vectors can be used as basis vectors of the colour space. Thus we can choose e.g. such basis vectors that the total volume of the colour cone is within the positive quadrant of the space. Just this has been done by the CIE at the time when the CIE trichromatic system was built [34], as it was felt that the manipulation with negative values in the colour matching functions may lead to calculation errors.

The basis vector transformation was done in such a form that:

1. The tristimulus values of the colour stimuli should again be equal in order to reproduce the equal-energetic spectrum (i.e. the white color);

2. All the photometric information (luminance, if the stimulus is measured in radiance units) should be in a single value, i.e. one of the colour matching functions should be equal with the $V(\lambda)$ -function. The $V(\lambda)$ -function is the curve that defines the relationship between the human sensation of light and the physical concept of energy, which is the quantity to which measuring instruments react.

3. The tristimulus values of all real colours should be positive and the volume of the tetrahedron should be as small as possible (i.e. the borders of the colour cone should touch the tetrahedron at as many as possible places).

With all these considerations in mind, the transformation adopted by the CIE was [36]:

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \begin{bmatrix} 2.76888 & 1.75175 & 1.13016 \\ 1 & 4.5907 & 0.0601 \\ 0 & 0.05651 & 5.59427 \end{bmatrix} \cdot \begin{bmatrix} R \\ G \\ B \end{bmatrix} \quad (2.10-a)$$

or in an expanded form:

$$\begin{aligned} X &= 2.76888R + 1.75175G + 1.13016B \\ Y &= 1.00000R + 4.59070G + 0.06010B \\ Z &= 0.05651G + 5.50427B \end{aligned} \quad (2.10-b)$$

It is evident in these equations that the Y component is identical with the luminance L previously introduced by equation (2.9). If the matrix elements are multiplied with 0.176967, the coefficient of $Y(R)$, in order to obtain a unit Y value when all the R , G and B stimuli have unit magnitudes as well, the matrix takes a simpler form:

$$\begin{vmatrix} 0.49 & 0.31 & 0.2 \\ 0.176967 & 0.812397 & 0.010636 \\ 0 & 0.01 & 0.99 \end{vmatrix} \quad (2.11)$$

where only the Y component is carrying six precisely chosen significant digits, while all the other matrix elements have only two non zero decimal digits. From this it is also evident that the X value is composed mainly from the R value, but the G and B values have also significant weight. The Z value is almost entirely composed by the B value.

The inverse transformation from the XYZ -system into the RGB one can be done by using the inverse matrix of (2.10-a):

$$\begin{vmatrix} 0.41846 & -0.15866 & -0.08283 \\ -0.09117 & 0.25243 & 0.01571 \\ 0.00092 & -0.00255 & 0.17860 \end{vmatrix} \quad (2.12)$$

One can see that all three matrices (2.10), (2.12) and (2.13) fulfill the requirement that an equal–energetic stimulus has in the system equal tristimulus values.

Color matching functions can be built in this system similarly to the $\bar{r}(\lambda)$, $\bar{g}(\lambda)$ and $\bar{b}(\lambda)$ color matching functions introduced above and shown in Fig. 2.7.

These corresponding functions in the XYZ system are called the $\bar{x}(\lambda)$, $\bar{y}(\lambda)$, and $\bar{z}(\lambda)$ color matching functions and they are the tristimulus values of the monochromatic primary stimuli.

Equation (2.13) shows the transformation with which these new color matching functions can be obtained from the $\bar{r}(\lambda)$, $\bar{g}(\lambda)$ and $\bar{b}(\lambda)$ color matching functions:

$$\begin{vmatrix} \bar{x}(\lambda) \\ \bar{y}(\lambda) \\ \bar{z}(\lambda) \end{vmatrix} = \begin{vmatrix} 2.76888 & 1.75175 & 1.13016 \\ 1.00000 & 4.59070 & 0.06010 \\ 0.00000 & 0.05651 & 5.59427 \end{vmatrix} \cdot \begin{vmatrix} \bar{r}(\lambda) \\ \bar{g}(\lambda) \\ \bar{b}(\lambda) \end{vmatrix} \quad (2.13)$$

Fig. 2.9. The CIE functions are derived from these RGB functions in such a way as to give all positive values. The RGB primaries must include some subtraction to cover the entire range of color perception [35]

The $\bar{x}(\lambda)$, $\bar{y}(\lambda)$, and $\bar{z}(\lambda)$ color matching functions form the *CIE 1931 Standard Colorimetric Observer*. They are tabulated in an ISO/CIE Standard [36] at 1 nm intervals to seven significant digits between 360 nm and 830 nm. A graphical representation is given in Fig. 2.9, whereas the tabulated values are given in Appendix A1. As it can be seen, all the values of these functions are non-negative, and the $\bar{y}(\lambda)$ -function has exactly the shape of the $V(\lambda)$ -function. One peculiarity of this transformation is that the $\bar{x}(\lambda)$ -function has turned out to have two maximums.

If it is desired to realize a sensor which delivers directly the tristimulus values of the monochromatic primary stimuli as outputs, then it should exhibit spectral selectivity curves that exactly match the curves of the $\bar{x}(\lambda)$, $\bar{y}(\lambda)$, and $\bar{z}(\lambda)$ color matching functions. This may be very difficult to implement practically, as the output values for each wavelength should have exact correspondence with the tabulated values. Given the deviations and tolerances of device parameters inherent in any mass production system, such an exact correspondence may not be practically achievable at a convenient cost. It may be more feasible to obtain a sensor with spectral characteristics similar to those of the eye, and whose outputs would be processed, e.g. using transforms as those highlighted in equations (2-10)-(2.13) above. The problem of chip-to-chip variability could be solved by using a self-calibration routine under standard conditions. This self-calibration would follow up the outputs provided by the sensor and would vary correspondingly the values of the transforms' coefficients from their ideal values for each specific chip, writing them

in an in-built programmable memory, so that the correct trichromatic signals would be always provided, even if the selectivity curves may have some variation from their ideally desired shape.

In 1976, a new CIE standard was released which corrected some of the problems raised by the initial diagram. In the 1976 diagram the distance between two points on the diagram is proportional to the perceived color difference. However, this 1976 CIE standard has failed to gain acceptance, and the 1931 CIE is almost universally used.

2.2- Optical properties of semiconductors

2.2.1- Introduction

Fig. 2.10 shows the general case for the interaction of light with a solid-state system composed of a multilayer coating on top of a substrate. Reflection of light waves occurs whenever the light penetrates from one medium into another, the amplitudes of the reflected and transmitted light beams being dependent on the differences in refractive indices between each two adjacent materials

When light is incident on a transparent thin film it produces two reflected beams: one from the front and one from the back surface. These two beams can interfere with each other to enhance or reduce the light intensity. However, for understanding the operation of a photodetector it is more important to highlight another important optical phenomenon, namely **absorption**.

The speed of light in vacuum, $c = 3 \times 10^8$ m/s but in any medium the speed of light c_m is smaller

$$c_m = \frac{c}{n} \quad (2.14)$$

where n is called refractive index. Optical phenomena require the usage of the so-called “characteristic (optical) admittance” of a medium, $N = n - i \cdot k$, which is typically referred to as the “complex refractive index”. Its two components are: n , the refractive index, and k , the extinction coefficient (related to losses, i.e. the attenuation of light propagating through the respective material), respectively. Both n and k are material properties [30]:

$$N^2 - k^2 = \frac{\epsilon_r}{\mu_r} \quad (2.15) \quad \text{and} \quad 2nk = \frac{\mu_r \sigma}{\omega \cdot \epsilon_0} \quad (2.16)$$

where ϵ_r and μ_r are the relative permittivity and permeability of the material, σ is the electric conductivity of the material and, ϵ_0 is the permittivity of vacuum and ω the

angular frequency of the electromagnetic wave. Finally, it must be highlighted that in any material, both n and k are varying with the wavelength, $n = n(\lambda)$, and $k = k(\lambda)$.

Based on k , the so-called absorption coefficient α can be defined as:

$$\alpha = \frac{4\pi k}{\lambda} \quad (2.17)$$

This means that the attenuation of light A after traveling through a sheet of material of thickness “ x ” will be $A \propto \exp(-\alpha x)$.

As mentioned before, k is wavelength dependent. Fig 2.11 shows that in silicon k decreases significantly with the wavelength [37]. Therefore, incident light of different wavelengths will have different penetration depths in the medium (silicon), i.e. the longer the wavelength, the deeper the penetration depth. Hence, the dependence of k on λ is one fundamental principle for the operation of our color sensor, on the basis of which its structure will be designed.

Fig. 2.10. Light in air incident on a thin film(s) layer penetrates through the semiconductor forming a transmitted light beam with light reflected from the top (surface 1) and bottom layer (surface 2).

Fig. 2.11. Variation of the extinction coefficient k versus wavelength λ for monocrystalline Si [37].

In spite of the different material dependencies, the exponential decay law can be universally used to express the attenuation of any wavelength through any material. It means that each successive interval of equal thickness absorbs an equal fraction of the photons passing through it. Each successive interval, however, receives fewer photons than the preceding interval because the number of transmitted photons decreases with depth.

For example, a material sample can be considered to be made up of identical adjoining slices of equal thicknesses. If this thickness is such that the first layer absorbs one-half of the photons, then only half of the original numbers of photons are incident on the second layer which also absorbs one-half of these, i.e. a quarter of the original number of photons incident on the sample surface, and so on for multiple layers. Although simple at the first sight, this principle is essential in determining the operation of multijunction color sensors, as will be seen in the subsequent section.

2.2.2- Absorption of Light

We shall examine here in more detail the formalism for the absorption of light in the simplest case. Consider a beam of light of intensity I incident normally into a material thickness (e.g. with a uniform concentration of absorbing pigments). It is also considered that no reflection and refraction occur. The photons therefore penetrate into the material and will be absorbed at different depths.

The mechanism for absorption is that a photon transfers all its energy to an electron in the absorbing material. The photon is "lost" from the light beam as it is absorbed in a single event. The electron is excited by the gain in energy to a higher energy state in the electron configuration around the atom.

This single-event transfer of photon energy to an electron and the disappearance of the photon are closely related to the photoelectric effect where the electron is ejected from the material in a single event.

The decrease in intensity of the light or photon flux as the beam penetrates into the material can be visualized if we separate the absorbing material into a set of thin, equal thickness slices of thickness t (Fig. 2.12). The material is isotropic and homogeneous and the thickness t is chosen so that only a small fraction of light A is attenuated in passing through this layer. The fraction of light absorbed in the first layer is $(1-A)$ times the incident intensity I . For example, if the fraction of light absorbed per layer is 10% of the incident flux, then for 100 photons incident on the first layer, $A \cdot I = 0.1 \times 100$ i.e. 10 photons will be absorbed and 90 photons are transmitted to the second layer. The light intensity incident on the second layer is $(1-A) \cdot I$ and $A(1-A) \cdot I$ will be absorbed in this

second layer. The amount transmitted through the second layer is $(1-A)^2 \cdot I$. To continue our example, with 90 photons incident on the second layer, $A \times 90 = 0.1 \times 90 = 9$ photons will be absorbed and 81 transmitted.

The process continues with fewer photons being transmitted into layer 3, layer 4, and so on, therefore with fewer photons being absorbed in each successive layer although the attenuation factor A remains constant for each layer. The absorption of photons in each layer is summarized in detail in Table 2.2.

Fig. 2.12. Light incident on a light absorbing material that is represented by a stack of layers of equivalent thickness, t . The decreasing length of the arrows as the light penetrates shows qualitatively the progressively reduced intensity of light.

Table 2.2. Transmission and absorption of light considering slices of material of equal thickness, each with an attenuation factor A .

	Incident on layer	Absorbed in layer	Transmitted through layer
Layer 1	I	AI	$(1-A)I$
Layer 2	$(1-A)I$	$A(1-A)I$	$(1-A)^2I$
Layer 3	$(1-A)^2I$	$A(1-A)^2I$	$(1-A)^3I$
...	...	...	...
Layer n	$(1-A)^{n-1}I$	$A(1-A)^{n-1}I$	$(1-A)^nI$

For n layers, the total absorption T_A in all layers (i.e. in the bulk of the entire material) will be

$$T_A = A + A(1-A) + A(1-A)^2 + \dots + A(1-A)^{n-1} \quad (2.18)$$

The first term in equation (2.18) represents the absorption by the first layer, the second term represents the absorption by the second layer, and so on.

The total transmitted light T_T through the n^{th} layer is

$$T_T = (1-A)^n \quad (2.19)$$

Equation (2.19) is more conveniently written using an exponential function based on the absorption coefficient α , the intensity of light $I(t)$ at depth t , for an incident intensity I_0 is given by

$$I(t) = I_0 \cdot e^{-\alpha \cdot t} \quad (2.20)$$

where α is given as a fraction per distance such as 0.2 per cm.

Fig. 2.13 shows the intensity of light as a function of penetration distance into materials with two different absorption coefficients. At the depth where $\alpha \cdot t = 1$, the intensity has dropped $1/e$ (a factor of 0.37) times the incident intensity.

All the above relations rely on the fact that the absorption of light is not dependent on the light intensity in the considered medium. For a given wavelength of light, each successive equal-thickness of the medium absorbs an equal fraction of light passing through it, but the amount of light it receives is successively decreasing. Hence, the intensity of light passing through a medium will decrease with depth.

To summarize briefly some of the conclusions:

- The number of photons absorbed in a given thickness Δx (and therefore the variation in light intensity ΔI) is proportional to the incident intensity I :

$$-\Delta I \propto I \cdot \Delta x \quad (2.21)$$

- If α denotes the absorption coefficient as the fraction of photons absorbed per unit thickness, then equation (2.21) can be written more accurately:

$$-\Delta I = \alpha \cdot I \cdot \Delta x \quad (2.22)$$

or in standard differential notation as:

$$-dI = \alpha \cdot I \cdot dx \quad (2.23)$$

- This equation can be integrated from the surface at $X=0$ to a depth x , and leads to the relation that the intensity $I(x)$ at depth x is given by

$$I(x) = I_0 \cdot e^{-\alpha \cdot x} \quad (2.24)$$

.where I_0 is the number of photons at $x=0$, $I_0=I(x=0)$.

Fig. 2.13. The intensity of light transmitted through an absorbing material: a) as a function of wavelength b) as a function of thickness d in cm for: (1) 10% absorbance, and (2) 50% absorbance per cm [38].

For small values of αx , for example $\alpha \cdot x = 0.01$, equation (2.24) can be written as a linear expansion:

$$I(x) = I_0(1 - \alpha \cdot x) \quad (2.26)$$

The absorption of light in successive layers (as presented in Table 2.2) forms the basis for the understanding of the operation of the multijunction color sensor as its equations can be used to deduce the location of each junction and the width of each depleted region that are necessary in order to obtain certain spectral responses.

2.2.3- The Photoconductivity Effect

Photoconductivity is an increase in the electrical conductivity of a solid material exposed to electromagnetic radiation due to the addition of free carriers generated by the absorption of photons. The rate at which free carriers are generated and the time over which they remain free determines the amount of increase in conductivity.

Photons are absorbed in a solid through a process known as the photoelectric effect whereby a photon interacts with an electron by giving all its energy to the electron. In effect, the photon disappears and energy is transferred to an electron. The photoelectric process is responsible for the absorption of visible light with energies of 2 to 3 eV as well as for X-rays with energies a thousand times greater than that of visible light.

Light quanta—photons—may cause different types of transitions in a semiconductor that increase the concentration of electrons in the conduction band and/or holes in the valence band and, hence, would enhance the semiconductor's conductivity. An intrinsic photoconductor uses band-to-band transitions. It responds to any radiation whose wavelength in vacuum satisfies the condition $\lambda \text{ in } [\mu\text{m}] < 1.24/E_g [\text{eV}]$ where E_g is the band gap energy. Extrinsic photoconductors often operate at cryogenic temperatures,

since at higher temperatures the conductivity may be dominated by carriers thermally excited from impurity levels.

For a uniform illumination, the generation rate of electron-hole pairs is given by

$$G_L(\omega) = \frac{Q_C P_I}{\hbar \omega L} \quad (2.27)$$

where P_I is the absorbed optical power per unit area (in W/m^2), L is the active thickness of the photoconductive film, and Q_C is quantum efficiency, i.e. the number of electron-hole pairs created per absorbed photon.

Fig.2.14. Energetic transitions caused by photon absorption in semiconductors:
 (a) In an intrinsic semiconductor (valence band to conduction band transition),
 (b) In an extrinsic semiconductor (from a deep donor level to the conduction band);
 (c1) and (c2) Also in an extrinsic semiconductor, transitions from the valence band to a deep acceptor, and from a deep acceptor level to the conduction band, respectively.

2.3- Photodiode physics.

A typical planar photodiode structure (shown in Fig.2.15) is most commonly fabricated in a lightly to moderately doped n -type silicon substrate. The front of the wafer is heavily doped with a p -type dopant, like boron, by ion implantation, in such a way as to produce a shallow junction. The rear of the wafer is heavily doped with an n -type dopant, such as phosphorus, for better ohmic contact. A top oxide layer is grown by thermal oxidation, with a reduced thickness in the active area of photodiode, allowing incident light in, while passivating the silicon surface. An anti-reflective (AR) coating, deposited by PECVD or CVD, can reduce the reflection of the light from the surface. The front and rear electrodes are the contacts for collecting the generated carriers.

The depletion region has a built-in electric field caused by the fixed space charges generated due to the initial diffusions of majority carriers across the junction. This region is important to photodiode performance as it provides the faster portion of device response and converts photons into electron-hole pairs at higher efficiency. Enlarging the depth of the depletion region is the common way to improve device performance when operated as a photoconductor.

Fig. 2.15. Structure of a photodiode under zero bias and the process of photocurrent collection

Depleted region (built-in electric field or externally applied reverse bias potential)

Fig. 2.16. Band diagram of a photodiode under zero bias and the process of photocurrent generation.

When electron-hole pairs are created in the depletion region, e.g. due to external illumination as shown in Fig. 2.16, most of the electrons and holes rapidly drift in opposite directions due to the built-in field, until they exit the depletion region. Then, these carriers cause a photocurrent flow when a circuit is closed between the front and rear electrodes. The remaining photons penetrate into the base region and excite electron-hole pairs when absorbed. From these neutral regions only those free carriers which can diffuse up to the edge of the depleted region will contribute to the overall output photocurrent.

Reverse bias is required to form a large potential barrier preventing the diffusion of majority carriers on both sides that can give rise to a forward current [39]. Moreover, reverse biasing will increase the depletion width and hence increase the efficiency in electron-hole separation and collection. However, at the same time it would modify the spectral response of the device, too.

2.4- Optical Phenomena in Semiconductor Devices

2.4.1- Absorption of light in a planar pn junction

Fig. 2.17 shows a schematic description of a planar *pn* junction illuminated with a incident light of intensity $I_0(x, \lambda)$. The absorption of incident light for every region will be calculated in this section using equation (2.24) while at the same time considering that the reflection at the semiconductor-air interface is negligible.

For region 1, the incident intensity is I_0 and the transmitted intensity is I_{3tr} calculated with

$$I_{3tr} = I_0 \cdot e^{-\alpha(\lambda)f(y)} \quad (2.28)$$

where $f(y)$ is the bottom line of region 1 approximated with an equation of a linear dependence $f(y) = m \cdot y + n$. Making all the necessary calculations one will obtain the following final results.

$$I_{1abs} = I_0 \cdot \left[1 - e^{-\alpha(\lambda) \left(\frac{w}{w_1} \cdot y + d \right)} \right] \quad (2.29)$$

Integrating from 0 to w_1 results in:

$$\int_0^{w_1} I_{1abs} dy = \int_0^{w_1} I_0 \left[1 - e^{-\alpha(\lambda) \left(\frac{w}{w_1} \cdot y + d \right)} \right] dy \Rightarrow I_{1abs} = I_0 \cdot \left[1 + \frac{e^{-\alpha(\lambda)d}}{\alpha(\lambda)w} \cdot (e^{-\alpha(\lambda)w} - 1) \right] \quad (2.30)$$

For region 2 the absorbed intensity is

$$I_{2abs} = I_{1tr} - I_{2tr} = I_0 \cdot e^{-\alpha(\lambda) \cdot d} - I_0 \cdot e^{-\alpha(\lambda) \cdot (d+w)} = I_0 \cdot e^{-\alpha(\lambda) \cdot d} (1 - e^{-\alpha(\lambda)w}) \quad (2.31)$$

Region 4 is identical with region 1 due to the symmetry of the device with respect to the vertical axis AA'. Consequently, one can write:

$$I_{3abs} = I_{1abs} = I_0 \cdot \left[1 + \frac{e^{-\alpha(\lambda)d}}{\alpha(\lambda)w} \cdot (e^{-\alpha(\lambda)w} - 1) \right] \quad (2.32)$$

The total light absorbed in the depleted region is:

$$I_{abs}(\lambda, d, w) = I_{2abs} + 2 \cdot I_{1abs} = I_0 \cdot e^{-\alpha(\lambda)d} (1 - e^{-\alpha(\lambda)w}) + 2 \cdot I_0 \cdot \left[1 + \frac{e^{-\alpha(\lambda)d}}{\alpha(\lambda)w} \cdot (e^{-\alpha(\lambda)w} - 1) \right]$$

$$\text{i.e. } I_{abs}(\lambda, d, w) = I_0 \cdot \left\{ e^{-\alpha(\lambda)d} (1 - e^{-\alpha(\lambda)w}) + 2 \cdot \left[1 + \frac{e^{-\alpha(\lambda)d}}{\alpha(\lambda)w} \cdot (e^{-\alpha(\lambda)w} - 1) \right] \right\} \quad (2.33)$$

Using eqn. (2.33) in a MATLAB simulation for a planar *pn* junction with a junction depth at 50 nm and a depletion width of 200 nm the ratio I_{abs}/I_0 obtained is illustrated in Fig. 2.18.

Fig. 2.17. Illuminated pn -junction highlighting the various region of interest and generated photocurrents

Fig. 2.18. MATLAB simulation of the ratio I_{abs}/I_0 for a planar pn junction with a junction depth at 50 nm and a depletion width of 200 nm, obtained using eqn. (2.33).

Fig. 2.19. MATLAB simulation of the carrier generation rate for a junction 50 nm deep and with a depletion width of 200 nm using eqn. (2.33) & (2.36).

2.4.2- Optical Generation and Carrier Generation Rate in Silicon

The number of incoming photons generated per second per unit area, or photon flux (ϕ), in an incident light of intensity $I(x, \lambda)$ is given by:

$$\phi(x, \lambda) = \frac{I(x, \lambda)[Wcm^{-2} \text{ or } Js^{-1}cm^{-2}]}{E_{ph}(\lambda)[J]} = \frac{I(x, \lambda)}{hc / \lambda} \quad (2.34)$$

where E_{ph} is the photon energy

The number of photons generated per second per unit volume is known as Optical Generation Rate, $G_{opt}(x, \lambda)$ and is given by [40]:

$$G_{opt}(x, \lambda) = -\frac{d\phi(x, \lambda)}{dx} = -\frac{1}{hc / \lambda} \frac{dI(x, \lambda)}{dx} = \frac{\alpha(\lambda)}{hc / \lambda} I_o(\lambda) e^{-\alpha(\lambda)x} \quad (2.35)$$

The number of electrons (and holes) generated per photon is defined as the quantum efficiency, η . Ideally, the quantum efficiency in silicon would be equal to 1 [41]. The Carrier Generation Rate, $G_{eh}(x, \lambda)$, which is the number of electrons (and holes) generated per second and per unit volume, is given by:

$$G_{eh}(x, \lambda) = \eta G_{opt}(x, \lambda) = \eta \frac{\alpha(\lambda)}{hc / \lambda} I_o(\lambda) e^{-\alpha(\lambda)x} \quad (2.36)$$

In practice, the incident radiation may consist of a spectrum of wavelengths. Therefore, the total carrier generation rate at a point is calculated by integrating over the wavelength spectrum of the incident radiation (λ_1 to λ_2) [18]:

$$G_{car}(x) = \int G_{car}(x, \lambda) d\lambda = \int_{\lambda_1}^{\lambda_2} \eta \frac{\alpha(\lambda)}{hc/\lambda} I_o(\lambda) e^{-\alpha(\lambda)x} d\lambda \quad (2.37)$$

Using eqns. (2.33) and (2.37) in a MATLAB simulation for a planar *pn* junction with a junction depth at 50 nm and a depletion width of 200 nm the total carrier generation rate obtained is illustrated in Fig. 2.19.

2.5- Color Sensor Design Approaches

There are many applications that require accurate and automatic measurement of color in a short time and this has driven the development of integrated color sensors. Many sensors have employed a 3-colour polymer filter approach to obtain three independent responses covering the visible spectrum [32, 42]. This type of sensor has several disadvantages: large occupied area, color response shift due to polymer aging, color aliasing and significant optical cross-talk. For this reason, various other types of solutions were sought by researchers. The following sections will give a concise review of solid-state color sensing devices previously reported in literature.

2.5.1- The triple junction structure

In a former chapter, a brief survey presented a few solid-state devices most closely related to a color sensor. Indeed, photoresistors, photodiodes, phototransistors, PIN photodiodes, diode arrays and matrices, metal-insulator-semiconductor (MIS) diodes and the charge-coupled devices (CCD) are commercially available and can be used to detect light.

One of the most obvious approaches to realize a color-sensing pixel in bulk silicon is simply to have three junctions on top of each other in order to obtain a complete colour sensor that would provide signals for all the three primary colours. Its functioning relies on the previously mentioned dispersion of k with λ (see again Fig. 2.11) so that the thickness of the silicon itself serves as a natural filter. In other words, both detection and filtration are now carried out simultaneously within the same structure. Furthermore, the vertical stacking of the 3 junctions enables the read-out of the correct colour measurement of the incoming light from a single spot, not from 3 different locations (although very close to each other) as in the classical filter-based approach.

A structure with three vertically integrated photodiodes can be achieved in various ways. One reported realization employed selective epitaxial growth (SEG) in order to obtain a large amount of control over the doping and junction depths. Bartek [43] et. al.

fabricated and measured, and Mohajerzadeh et. al. [18] used process and device simulations to model the fabrication of such a structure and its spectral response (Fig.2.20). In both cases, three independent spectral responses were obtained.

(a)

(b)

Fig. 2.20. (a) A color sensor with three vertically stacked photodiodes; (b) The normalized simulated spectral response [17].

The structure of Mohajerzadeh, shown in Fig.2.20–a as a device with a thyristor-type *pnpn* structure, was reported as capable to be employed for simultaneous detection of the three primary colours [18]. Just as for the SEG-based device, the doping profile and reverse bias conditions were tailored by using TCAD process and device simulators (TSUPREM-IV and PISCEB-2B), respectively, to achieve what were considered to be optimum spectral responses (shown in Fig.2.20–b). The authors found that the final output signals corresponding to the primary colours (RGB) can be extracted (in principle) by performing simple linear transformations with the detected currents:

$$B = \frac{I_1}{I_2}; \quad G = 2 \left(\frac{I_2}{I_3} + \frac{I_3}{I_2} \right); \quad R = 1.25 \left(\frac{I_4}{I_3} \right); \quad (2.26)$$

where I_1 , I_2 , I_3 , and I_4 are the currents collected at terminals 1, 2, 3 and 4.

Bartek's SEG-based device was more complicated: extra lightly doped regions were introduced to tailor much more accurately the depth of the depletion regions and to enhance the spectral selectivity. Fig. 2.2–a shows the structure of such a sensor. The obtained responses, shown in Fig.2.20–b, were achieved when the depletion region of the top, middle and bottom diodes extended in depth between 50 and 200 nm, from 200 to 800 nm, and from 1500 to 500 nm from the surface in the bulk of the Si, respectively (the substrate-epi junction is not used). The structure has been implemented using a Selective Epitaxial Growth (SEG) process, which enables selective stacking of additional epitaxial layers after completion of the conventional processing. Its fabrication is compatible with a standard bipolar processing and enables on-chip integration of read-out circuitry to realize a smart sensor on a single chip. However, although the SEG process is fully compatible with standard bipolar processing, it is not usually employed in a standard CMOS process. Moreover, it requires a specialized machine and dedicated know-how in order to apply such a process successfully. Therefore employing SEG may not be a very practical alternative and other approaches continued to be searched in order to obtain more feasible color sensors.

The above-mentioned devices clearly indicate that a triple-well junction structure, as used in the devices shown in Figs. 2.20 and 2.21, is the most suitable for providing a complete set of RGB output signals. Furthermore, it is also possible to realize such a structure using CMOS-compatible processing [44], provided that SEG or other non-standard methods are not employed.

(a)

(b)

Fig. 2.21. Colour sensor with vertically stacked photodiodes realized using SEG:
a) Schematic device structure, and b) Its relative spectral responses [43].

Such a triple-junction structure was also patented by Foveon [45], a company specialized in the fabrication of imaging chips for digital cameras. The schematic structure based on a triple-well CMOS process is shown in Fig. 2.23 and was used in the realization of a chip used in one of Sigma's digital cameras [46]. However, a disadvantage of this Foveon's color sensor is that it is limited by structural and fabrication parameters, especially when the junctions are created by diffusion as is the case for this device version. This makes it difficult to achieve a spectral response similar with the optimal desired one. The top-most diffused layer has a thickness of the order of a few tenths of a micron whereas the deepest well has a depth of several microns. This latter fact means that a large device area will result, i.e. the device is not entirely suitable for miniaturization but for fabricating single discrete device rather than arrays of very small pixels. Another disadvantage is the necessity of complicated electronics for signal processing and for subsequent data conditioning. All the above disadvantages can be addressed if one could design another device more suitable to color measurement or spectral measurement, and which will be much more beneficial in terms of the ease of manufacture and cost. Foveon has tried to address these issues with a second patent, which employs a multi-junction structure: basically an extra 'insulating' junction was inserted between every two adjacent 'sensing' junction, resulting in a very complex multi-junction device whose fabrication relies on two epi growth steps which are also combined with very high energy (1 MeV) and high dose implants to realize the necessary contacting regions through both these epitaxial layers [47]. Obviously, such a complex approach is not very feasible unless one has the available technology to apply it but this may not always be the case (National Semiconductor's technology was licensed to Foveon to realize their device but not everyone may have the money to buy such a license, or the facilities to implement it). Therefore, it would be more practical to develop alternative devices or structures which could be easily used for color sensing, that do not require 'exotic' technologies for fabrication, which also could provide RGB outputs from a single detector, and which can easily be miniaturized into small-sized pixels for large imaging arrays.

The junction field transistor (JFET) satisfies all the above conditions while also exhibiting other advantageous features, as it was mentioned in detail previously, in section 1.3. Due to all these reasons it was adopted as the main starting point from which various color sensor structures were designed in this project, as it will be detailed later in the following chapters of this thesis.

Fig. 2.22. Schematic representation of Foveon's first color sensor with a triple-well structure [45].

Fig. 2.23. Foveon's triple-well structure spectral responses for the top, middle and bottom junction, respectively[45].

The basic concept of the junction field-effect transistor (JFET) was described by Shockley in 1952 [48] and was mainly intended for low-voltage signal processing applications. Its primary features are a high input impedance and faster inherent switching speed because of the absence of the minority carrier recombination, which limits the speed of the classical bipolar transistors. Thus, as a majority carrier device, the JFET does

not needs any stringent lifetime control requirements that are essential for the fabrication of the bipolar transistor.

2.5.2- The PhotoJFET

S.G. Bandy and J.G. Linvill developed one of the first photo-JFETs mentioned in literature, which is shown in Fig. 2.24 [49]. The field effect photo-detecting structure introduced in this paper was a single device capable of producing an output voltage (of the order of volts) linearly related to the incident illumination intensity. The top and bottom gate are connected at the same potential V_G in order to completely enclose the channel. If the top gate has a thickness less than the diffusion length L_n of its minority carriers, then the junction collects all the carriers generated by the incident light in the top gate so that the top gate and channel form an effective photodiode.

The design for an optimum field-effect photodetector of this type has to maximize the channel impedance (responsivity) which is subject to constraints of surface area and deviation from linearity over a specified range in drain signal.

In conclusion, this photo-JFET required an impractical scheme for photodetection using a photodiode in series with a resistor of very high resistance, both components being integrated in a single solid-state device. The impedance of this device is voltage-controlled over a range extending, for all practical purposes, to infinity. Both of these features substantially reduce the surface area from what would be needed for an equivalent photodiode-series resistance combination.

Fig. 2.24. The JFET photodetector [49].

Fig. 2.25. Junction FET photodetector with maze geometry; aspect ratio $\cong w/2L$ [49].

The basic motivation for conceiving this JFET photodetector was to provide a single device that could produce output voltages comparable to devices operating in the charge storage mode for the same illumination levels, but yet avoiding the problems of switching inherent in the charge-storage mode, especially at low light levels. In this charge-storage mode the gate-channel junction is charged with a gate pulse and then left floating, so that any ensuing illumination discharges the junction, with the channel width and hence the current drain being proportional to the total illumination integrated over a period of time. Simplicity of fabrication, the possibility of achieving larger responsivity-bandwidth products by using a meander-shaped gate layout (the so-called 'maze' structure) and real-time operation are assets of this JFET photodetector that makes it more amenable to certain applications than other types of photodetectors.

The maze structure, shown in Fig.2.25, allows a longer channel length L and smaller channel width w for the same total device area $W \cdot L$, thereby increasing channel impedance at $V_G = 0$, R_0 , and hence the responsivity, which in this case is proportional to the square of device area.

2.5.2- The SIT-based image sensor

A new type of JFET is the Static Induction Transistor (SIT) proposed by Nishizawa and coworkers in 1975 [50]. Despite its different name, it is actually a vertical JFET in which carriers are injected from a source to a drain across a potential barrier induced in a current channel and wherein the height of the potential barrier can be varied in response to a gate bias voltage applied to a gate and to a drain bias voltage applied to the drain to thereby control the magnitude of a drain current of the transistor. The peak of the potential barrier is defined by Nishizawa as intrinsic gate. The SIT has the advantage

that its I–V characteristic curve is nearly linear over a very wide range of drain current values, including the low drain current region.

Selecting appropriate values for the impurity concentrations, and/or thickness of the substrate and of an epitaxial layer grown thereon one can easily attain the above-mentioned properties. The first usage of the SIT was as a dynamic RAM memory element and the authors optimized it for this purpose. In order to obtain a high speed operation one must minimize the channel resistance in order to satisfy the condition $r_s \cdot G_m < 1$, especially at low drain currents and irrespective of the magnitude of the gate bias voltage, where G_m is the intrinsic transconductance under the condition of zero series resistance. While in the JFET the series channel resistance is responsible for negative feedback effects resulting in the saturation of D.C. characteristics, in the case of the SIT the role of the series resistance is different, and this resistance can be made sufficiently small so that the saturation of the characteristics would not occur.

Moreover, Nishizawa proposed the usage of SITs as semiconductor image sensors in 1983 and more particularly, used the back-illuminated devices presented in Fig. 2.30 for this purpose [51].

Nishizawa's work indicates how one can optimize certain device characteristics, such as the device series resistance from the source to the intrinsic gate (the region in which the drain current is substantially controlled). In addition, for a low impurity concentration of the channel region and a small width of the channel region the depletion layer extends from the gate so as to form an intrinsic gate of potential barrier type, and to pinch off the channel region. Additionally, the gate length is selected short to provide a very small series resistance. Also, if a potential barrier is produced in the intrinsic gate region, the height of this potential barrier can be controlled by varying either the gate or the drain potential. For this reason, the SIT is able to exhibit a non-saturating type of current versus voltage characteristics. Moreover, its gate capacitance can be reduced drastically by using a very small gate length, which makes it suitable for high-speed and low power dissipation operation. A one-dimensional diagram of the potential distribution of the SIT from source to drain is schematically shown in Fig. 2.27-a. Here ΔV_D is the deviation of the drain voltage, W is the distance from the center of the gate (denoted as "intrinsic gate") to the drain neutral region, and W_g is the distance between the source neutral region and the intrinsic gate.

Fig. 2.26. Schematic diagram of the SIT image sensor cell [51].

Fig. 2.27. (a) Potential distribution in SIT in normal operation mode [50], and (b) Its equivalent circuit [52].

A high sensitivity semiconductor photoelectric converter can be obtained by electrically isolating the gate region of a SIT which exhibits its typical non-saturating current versus voltage characteristic. Optically generated minority carriers are then stored in the gate region to control the potential thereof. Such a photodetector provided with an insulated gate is then very effective in enhancing the dynamic operational range. The fact that the SIT exhibits non-saturating characteristics enables the enlargement of the output current simply by increasing the drain voltage.

An image pick-up device can be constituted by integrating photoelectric semiconductor elements together with SIT, i.e. using a MOS transistor as a light-detector. Therefore, if the amount of light irradiated on the device is not abundant, the electric charge which is stored will be small, i.e. a strict direct proportionality between the incident light intensity and stored charge is observed. Therefore, it is typically not possible to obtain a large signal with such devices if the light is weak. Furthermore, leakage of the stored electric charge often occurs when it is being transferred. The

detection of light, however, is carried out by utilizing the pn junction at the source region which is now used as a photodiode. Therefore, a SIT-based image pick-up device has similar drawbacks related to or resulted from the charge transfer problems, for example, a low sensitivity to light for single stand alone series.

However, integrating a multiplicity of SIT-based photoelements resulting in a high-speed and high sensitivity image pick-up device. A switching transistor may be merged in the gate region of each photoelectric converter element to enhance the operation speed of the image pick-up device.

The authors also realized a SIT-image sensor circuit configuration suitable for standard TV format and they confirmed experimentally its pick-up operation and the operational characteristics of SIT have been analyzed from this point of view [52].

For this project, studying the application of the SIT as a photodetector was a good starting point for developing a similar structure but which may be used as a color sensor.

2.5.3- Patent search

The patent search was dictated by two considerations: first of all, the literature review revealed extremely few JFET-based photodetectors. Secondly, the patent application for JFET-based color sensors with the structures resulting from the work carried out in this project required that a patent search should be done first. However, just as for the literature review, it must be underlined that only a very small percentage of the entire huge number of patents which can be found effectively deals with JFETs as photodetectors, and almost none mentions their possible usage as color sensors. We shall briefly overview here only the most important patents found in our search.

J.M. Shannon is the first inventor that used the JFET as a solid-state image sensor [53]. The main object of his invention was to realize an improved solid-state imaging device for operation in the charge storage mode providing higher signal-to-noise ratio. One can see in Fig. 2.28 that the inventor modified the classical JFET structure and used instead an annular gate. The operation of this device can be briefly described as follows. When a suitable voltage pulse is applied to the gate (and thus across the pn junction between the gate and substrate), a depletion region will extend from the gate junction in an annular shape completely blocking the channel between the common source and each of the drains.

Fig. 2.28. Drawings revealing Shannon's first opto-JFET: (a) A top view of a linear array of elements (d); (b) A cross-sectional view of (a) along the line 2-2; (c) A cross-sectional view along the line 3-3; (d) The circuit diagram, and (e) Various voltage waveforms associated with its operation.

When the gate voltage is removed, the depletion regions remain in place during a frame time, except for their slow discharge due to dark current leakage. To interrogate any image element, a voltage pulse is applied to the drain of that element and this can be done at any time as this read-out is nondestructive. Without any incident radiation the channel of an element exhibits a high impedance and its output signal will be small as is transmitted across the impedance in series with that element. Light incident on that image element between interrogations will cause the stored charge to leak off at a rate proportional to the radiation intensity and the resistance of the channel reduces accordingly.

However, this operation mode has a serious disadvantage due to the dependence on the radiation intensity: if the incident light intensity is not sufficient then the gate diode cannot discharge and no output signal can be read.

Later, in 1976, J. M. Shannon et al. filled a new patent with a similar device operated in the same manner [54] but for which the dependence of its performance on the radiation intensity was addressed by using another structure and different materials. Fig. 2.29(a) shows the cross-sectional structure of this proposed solid-state device which would be more suitable for operation in a charge storage mode, with the circuit connections for operation and various voltage waveforms associated with its operation.

Layer 1 is photosensitive and radiation is incident at the upper surface of the device, as shown in Fig. 2.29(a). The electrode layer 4 allows the passage of radiation which, in order to be useful for the device, should be absorbed within a depletion region or within a minority carrier diffusion length away from any of the depletion regions developed around p -type grains 3. The generation of electron-hole pairs causes the discharge of the p -type grains and the depletion regions contract correspondingly, thus opening up the current paths within the n -type host material between electrodes 4 and 5. In this example the host material 2 is granular n -type ZnO and the discrete regions 3 consist of grains of p -type ZnTe which form a plurality of rectifying junctions with the bulk of the n -type material. The complementary structure is also possible: to have discrete regions 3 of n -type grains in a p -type host material. Moreover, modifying the type of materials additionally increases the number of different combinations which could be realized, such as: n -type ZnO with p -type ZnTe, n -type CdS with p -type CuS, or n -type polycrystalline silicon with p -type silicon grains. The authors also suggested that yet another possibility is to use a multitude of metal particles distributed in a host semiconductor material thus forming Schottky barriers.

Fig. 2.29. The improved JFET-based photodetector patented by Shannon in 1976:
 (a)–(c) Cross-sections of the electronic solid state optical detector operated in a charge storage mode, also showing the circuit connections for normal device operation and the extension of depletion regions with voltage applied; (d) Various voltage waveforms associated with the normal operation of the device [54].

Figures 2.29 (a)–(c) show the variation of the depletion regions' widths with potential applied between the electrodes 4 and 5 in various cases:

- a) In an equilibrium state with small depletion regions 6 associated with the built-in voltages of the pn junctions;
- b) When applying a reverse bias voltage pulse the depletion region 7 widens, and
- c) The magnitude of the charging voltage pulse V_R determines the positive charge in the depletion region to become evenly distributed and the host material 2 completely depletes the regions between the grains thus effectively blocking the current path between electrodes 4 and 5.

The device can be interrogated in a non-destructive read-out manner many times subsequent to the application of the charging voltage pulse V_R by applying voltage pulses V_I of relatively small magnitude between electrodes 4 and 5. The output voltage V_O is measured across the resistor R . This device operates in a charge storage mode and in a radiation integrating manner in that the output signals are indicative of the radiation incident on the layer in the period following the application of the charging pulse.

Figure 2.29 (d) shows the input voltage waveform during the frame time intervals t_{F1} , t_{F2} , t_{F3} , t_{F4} and the output voltage waveform associated with such a mode of operation. During frame interval t_{F1} the incident radiation intensity is high, whereas during frame interval t_{F2} no radiation is incident. During frame interval t_{F3} the incident radiation intensity is smaller than in frame interval t_{F1} , and in the last frame interval t_{F4} the incident radiation intensity is equal with that provided in frame interval t_{F1} . The output voltage V_O rises during t_{F1} due to the integrating effect of the layer formed by grains and saturates when the grains have fully discharged before falling to zero at the end of t_{F1} on application of the resetting potential to block the conduction path between electrodes 4 and 5. As incident radiation is absent during t_{F2} the output voltage V_O remains at zero and rises again during t_{F3} when radiation is incident. One can see from the difference in the output voltage V_O during t_{F1} and t_{F3} frames that the only variable is the incident radiation intensity.

Unfortunately, all the advantages are concealed both by the materials used in fabrication of the device and by its dimensions (layer 1 is 10 cm $\times$ 10 cm large and 5 μ m thick). The invention presents as well a 1 mm $\times$ 1 mm device formed in a n^+ -silicon substrate with a similar structure but in which the granular structure is replaced by an array of p -type regions buried at the interface between two n -type epitaxial layers (each 10 μ m thick). The authors chose the above mentioned materials, especially the metal

oxides, for their optical properties like transparence (for the base bulk material in which the grains are embedded) and emissive radiation favorable for the conversion of incident radiations of very different wavelengths into visible light.

The devices described above are excellently suited for the detection of light, but not for accurate color discrimination. Indeed, these devices were intended to be used for information storage and to reproduce an optical image of the document using electro-photographic means with no special care devoted to accurate color reproduction.

The next patent that was issued to the same authors was an image display and/or conversion device comprising an array of Field Effect Transistor (FET) structures with an individual display (electro-luminescent diode LED) electrically in series with the source and/or drain of each transistor [53].

Another invention describing a JFET-based device was patented by Jan Lohstroh [55] and is shown in Fig.2.30. The invention relates to a semiconductor device which consists of a n -type channel region (9) located between the source region (8) and drain region (7) and bounded by two oppositely located gate electrodes (4 & 13) each forming a rectifying junction with the channel region and in which the photosensitive junction is formed by a gate electrode (4) which shows a floating potential.

The “floating” gate electrode (4) may be charged by simultaneously applying to the other gate electrode (13) a voltage pulse of sufficiently large amplitude so that punch-through occurs thereby reducing the number of majority charge carriers. After charging, the zones (4), in the subsequent integration period, not counting the normal thermal generation of charge carriers, can be discharged only as a result of absorption of incident electromagnetic radiation in/or near the depletion regions and which results in the generation of electron-hole pairs. The quantity of radiation which has been incident and absorbed during an integration period in and/or near the channel region, therefore resulting in a reduction of the thickness of the depletion region, can be determined by measuring the conduction of the channel region by conveying an electric current between the source and the drain regions.

One of the important advantages of this sensor is that its reading is non-destructive and, therefore, the stored signal can be read more than once, if desired. Moreover, the influence of interference signals, for example, switching signals, can be considerably reduced during reading. A further important advantage of the described way of reading is that the electromagnetic signal converted into electric charge occurs in an amplified manner in the output signal.

Fig. 2.30. (a) Plan view of punchthrough resetting JFET image sensor; (b) Cross-sectional view taken along line III of (a); (c) Cross-sectional view taken along line II of (a); (d) Electric circuit diagram of the JFET image sensor; (e) Voltage applied to the gate as a function of time t ; (f) Potential of the floating gate electrodes of the semiconductor device presented in (a) as a function of time t ; (g) Electric output signals derived from the output of the semiconductor device presented in (a) as a function of time t [55].

Due to the fact that each transistor is each time adjusted at the individual threshold voltage during the charging of the buried zones 4, the transistors T_1 , T_2 , T_3 and so on (Fig. 2.30), will give substantially the same output signals upon absorption of the same quantities of electromagnetic radiation, irrespective of the spreading in the threshold voltages.

The dispersion of the threshold voltages is caused in particular by spreading in the thickness and doping of the channel regions. Moreover, this spread may be so large that a lower limit is imposed by it on the minimum quantity of radiation to be absorbed at which a reliable signal is still supplied by the transistors.

The influence of the spread in the threshold voltage of FET on the output signals can be considerably reduced by adjusting, during charging, the voltage on the gate electrode of each FET to match the specific threshold value of each individual transistor. As a result of this described method the network of these devices is particularly suitable for detecting radiation of only very small intensity.

Later, using the same theory presented in [55] but with an improved method, Jun-ichi Nishizawa proposed a back-illuminated static induction transistor (SIT)-based device shown in Fig.2.31 for memory storage purposes with a floating storage region set at the surface of the substrate, but which can also be used as an imager [56].

The n^+ region 23, the n^+ region 25 and the p^+ region 26 serve as drain, source and gate regions, respectively, of the vertically configured SIT in a semiconductor substrate 22. An n^- region 24 serves as channel region of this SIT. The device works as follows: optical irradiation incident onto the device through transparent electrode 21', where the positive voltage $V_S (+)$ is applied, generates electron-holes in region 22. The generated holes are flowing toward the n^+ buried region 23 and stored in the n^+p^- junction adjacent to n^+ buried region 23. The stored holes lower the potential height for electrons in the n^+ buried region 23 resulting in flowing out of electrons from the n^+ buried region 23 toward the transparent electrode 21'.

The increase of stored holes in the n^+p^- junction increases the amount of flowing out electrons from the n^+ buried region 23 due to the lowering of the n^+p^- junction potential, so that n^+ buried region 23 is depleted of electrons and therefore tends to exhibit a positive potential.

In the read-out process, the reverse gate bias voltage applied on the gate p^+ region 26 returns to zero. The read-out process is finished by electrons in the surface n^+ region 25 flowing into the positively biased n^+ buried region 23 through the n^- channel region 24. The stored voltage proportional to the optical input is detected through the sense

amplifier Q. This type of operation is called the carrier depletion-storing mode because in this case the shortage of electrons in the n^+ region makes up the stored charge. In this carrier depletion storing mode, the reverse bias voltage between the n^+ floating region 23 and the p^+ gate region 26 increases with increasing the positive bias voltage V_o (the write-in voltage).

Fig. 2.31. (a) Plan view of a SIT-based image sensor; (b) Cross-sectional view taken along line A-A' of (a); (c) Cross-sectional view taken along line B-B' of (a); (d) Electric circuit diagram of the semiconductor image sensor; (e) The potential distribution in the optical sensing region composed by the n^+ region 21, p^+ region 22 and n^+ region 23; (f) The electric field intensity distribution in the same optical sensing region of the semiconductor device presented in (a) [56].

The opposite is also true, i.e. excess electrons can be stored in the n^+ floating region 23 in the so-called carrier accumulation-storing mode. It is obvious that a SIT-based memory cell is also realized with a structure having a floating storage region buried in the substrate.

The circuit unit presented in Fig 2.31(d) shows that the bit line BL is connected to the n^+ region 25 and the word line WL is connected to the p^+ gate region 26. The optical sensing region is represented by the two diodes D_1 and D_2 . The potential and field intensity profiles in the n^+ (21) p^- (22) n^+ (23) optical sensing region, provided that a positive voltage $V_s(+)$ is applied, are shown in Fig. 2.31(e) and (f).

The carrier depletion-storing mode is superior to the carrier accumulation-storing mode improving the memory performance parameters such as the retention characteristics, the temperature dependence of memory retention characteristics and the operational tolerance. Accordingly, the main object of this invention was to provide a semiconductor image sensor in which the SIT serves as a read-out transistor or a refresh transistor and NOT as a photodetector or color sensor. It is also worthwhile to highlight that this is a back-illuminated-type semiconductor image sensor comprising a photosensitive region where there exists an intense electric field. This strong electric field is required in order to push the photogenerated carriers into the floating region and at least one read-out transistor is necessary to acquire the charge stored in the optical region, as shown in Fig. 2.31.

In conclusion, many of the found patents that used JFET-based sensors had good sensitivity, especially to long wavelengths and were designated to be compatible with the existing imaging systems, e.g. the conventional horizontal blanking period in HDTV applications. However none of the found patents dealt with color detection and, moreover, none of the previously described devices can be used “as is” for color sensing unless its structure would be drastically modified and/or improved. Nevertheless, the patent search proved that the idea of employing JFET’s or JFET-based devices for optical sensing is in principle correct, although entirely new structures must be thought of in order to achieve the desired color sensing function.

2.5.4- The ‘Lambda Diode’

Logical gates typically employ CMOS transistors in modern digital integrated circuits. The ‘Lambda Diode’ is a peculiar and quite interesting device which can be used for similar purposes, i.e. as an elementary block for building logical circuits, only that it employs exclusively JFET’s. A completely original contribution of this work is the

proposal of using JFET-based ‘Lambda Diode’ for color sensing, idea which—to our knowledge—has never tried by anyone else. Although no previous article could be found that would mention the usage of the Lambda Diode as a photodetector, preliminary simulation results that will be detailed later justify the further investigation of this type of device for color photodetection.

The first design of a ‘Lambda Diode’ type of circuit belongs to S. Koike et al [57]. Their patent claims a negative resistance device formed by series-connection of a complementary pair of insulated gate type FET’s (field effect transistors), their sources being connected together and the gates of each of the FET’s was being connected to the respective drain of the other FET. At least one FET was considered to have a double layered gate insulation film under the gate electrode, thereby forming a non-volatile memory element. The inventors used this negative resistance device as a highly efficient memory cell which requires little power in writing-in, erasing and memory-holding.

The so-called ‘Lambda Diode’ is a circuit similar to that described in Koike’s patent, but in this case only JFETs are used. The two-terminal device of S. Koike et al. is composed of an n -channel and a p -channel MNOS FET, as shown in Fig. 2.32 (a), (b) and (e) while its I–V characteristic is presented in Fig. 2.32(d) [58].

S. Koike et al. developed later a nonvolatile semiconductor device and particularly a nonvolatile bistable memory based on their negative resistance device [58]. For the JFET-based ‘lambda diode’ Alexei Krasnopolski proposed a design in which the two JFETs can be integrated and connected directly through the wafer [59].

Similarly to the usual semiconductor diode, the ‘lambda diode’ has two states: it is either conducting (its impedance tends to null) or not conducting (its impedance tends to infinity). Just like the usual diode the ‘lambda diode’ in the non-conducting state has a current close to 0, practically defined only by the leakage current. However, the lambda-diode has an essentially different characteristic (see Fig. 2.33) from that of a normal pn junction. In order to keep a diode in the conducting state one needs a forward-bias voltage of about 0.5 - 0.7 V whereas a much higher applied voltage is necessary to reach the peak current of the lambda diode.

The lambda-diode is not conducting both for voltages larger than a cut-off value V_C or when the applied with voltage equals 0V and has no a current through it in this state (except for the leakage). This latter feature may prove to be extremely beneficial for our photodetecting purposes: in contrast with the simple JFET, which is a normally-ON device for any applied drain-to-source bias V_{DS} , the lambda-diode can be a normally-OFF device provided that the applied V_D bias is larger than the cut-off voltage V_C

(alternatively Q_1 and Q_2 can be designed such that their threshold voltage $V_{T1,2}$ will provide a cut-off voltage V_C smaller than the desired supply bias voltage).

Fig. 2.32. (a) Schematic sectional view of a p-channel MNOS FET; (b) Schematic sectional view of a n-channel MNOS FET; (c) Circuit diagram of a MOSFET-based 'Lambda Diode' type of device; (d) Λ -shaped I - V characteristic relating the input voltage and current flowing between the 36' and 26' terminals, exhibiting negative resistance in a large portion; (e) Schematic cross-sectional view of the device. [58]

Fig. 2.33. Comparative I–V characteristics of (a) p–n junction diode, and (b) The lambda–diode [59].

Moreover, having in its composition both p - and n -type JFET's can be an advantage for optical sensing, as the user may choose to have any of these two transistors as the photosensing elements, depending on the desired application and available technology.

It is necessary to highlight that the lambda-shaped I–V characteristic does not prevent the operation of this device as a diode (if one applies a bias voltage of polarity opposite to that considered previously when obtaining the lambda-shaped I–V characteristic), but only improves its dynamic characteristics.

The reported applications of the lambda–diode were related only to developing logic gates based on complementary JFETs (CJFETs), as this type of circuit has the following advantages: it requires only one single supply source, without any shift of the logical level between the gate's input and output; the CJFET gates also have micro-power ability similar to CMOS, and therefore can also work without power consumption in static states (provided that $V_{\text{bias}} > V_C$).

2.6- Conclusions

The literature review and patent search which have been carried out clearly showed that no JFET-based color sensors have yet been reported, although a few types of JFET-based photodetectors were developed. On one hand, this was a clear proof of the profound originality of the work carried out in this project. On the other hand, it has shown that –at least in principle– JFET-based color sensing should be feasible, although much work would probably be required to adapt the reported structures into devices fully suited for the desired final aim (color sensing). Therefore, the next step was to start the

theoretical calculations of a simple JFET structure and of its operational characteristics in order to understand how its behaviour would be altered upon illumination and how spectral selectivity could be achieved. The next chapter presents the results of such elaborate theoretical calculations and of MATLAB simulations, which on their turn constituted the starting points for even more detailed MEDICI and TSUPREM-IV TCAD simulations that led to a more exact prediction of the JFET color sensors characteristics and which will be presented in other subsequent chapters.

Chapter THREE: Theoretical Consideration and Simulation of JFET–based Color Sensing Structures

3.1. The fundamental equation of the JFET

Fig. 3.1 presents the schematic diagram of the n -channel JFET considered in our analysis with a channel length L , a channel width Z , channel depth $2a$, and h is depletion layer width.

This analysis will deduce the detailed current voltage characteristics for a JFET with an arbitrary charge distribution and a structure as shown in Fig. 3.1b. Because of symmetry of the device, it is sufficient to consider only the upper half of the device, where h is the depletion layer width at an arbitrary point, and y_1 and y_2 are the depletion layer widths at Source and Drain, respectively.

The entire calculation of the JFET's drain–source current, which is obtained starting from Poisson's equation considering a gradual–channel approximation, is presented in Appendix 1. In this chapter it is necessary to employ just an intermediary step, namely the **fundamental and general equation for JFET drain–to–source current:**

$$I_D = \frac{2Z\mu}{\epsilon_s L} \int_{y_1}^{y_2} [Q(a) - Q(h)] h \rho(h) dh \quad (3.1)$$

where $Q(y)$ is the charge distribution given in general by

$$Q(y) = \int_0^y \rho(y) dy \quad \text{with } \rho(y) \text{ charge density in } [C/cm^2] \quad (3.2)$$

In particular, for the specific case of a uniformly doped semiconductor with a doping concentration N_A then the charge distribution given by equation (3.2) will become $Q(y) = q \cdot N_A \cdot y$.

From equation (3.1), a more detailed expression of I_{DS} can be obtained for an n -channel device (when $V_G < 0$ and $V_D > 0$)

$$I_{DS} = g_{\max} \cdot \left\{ V_{DS} - \frac{2}{3a} \sqrt{\frac{2\epsilon_s}{q \cdot N_D}} \left[(V_{DS} + V_{GS} + V_{bi})^{3/2} - (V_{GS} + V_{bi})^{3/2} \right] \right\} \quad (3.2)$$

where $g_{\max} = \frac{2Z\mu}{L} Q(a)$.

Fig. 3.1. Fundamental structure of a classical n-channel JFET: a) Schematic cross-sectional view of a simple structure with top and bottom gates. The dashed line delimitates the actual operating area in the center of the structure. b) The device under study in this chapter and its main geometrical parameters.

Fig. 3.2. The upper half of the device considered in the calculation of I_{DS}

The maximum current I_{DSat} for a given V_G occurs at that point where the channel is pinched off and this current is obtainable from equation (3.2):

$$I_{DSsat} = \frac{Z\mu \cdot q^2 N_D^2 a^3}{3\epsilon_s L} \left(1 - 3\frac{y_1^2}{a^2} + 2\frac{y_1^3}{a^2} \right) \quad (3.3)$$

$$I_{DSsat} = I_P \cdot \left[1 - 3\left(\frac{V_{bi} + V_G}{V_P} \right) + 2\left(\frac{V_{bi} + V_G}{V_P} \right)^{3/2} \right]$$

where V_P and I_P are the pinch-off voltage and the pinch-off current which are given by

$$I_P = \frac{Z\mu \cdot q^2 N_D^2 a^3}{3\epsilon_s L} \quad (3.4a)$$

$$V_P = \frac{qN_D a^2}{2\epsilon_s} \quad (3.4b)$$

The point where pinch-off occurs is denoted by P, and is defined as the point where the depleted regions of top and bottom gate, respectively merge together. This point moves forward the point P' with the increasing of applied drain voltage V_D . The depletion region completely covers the channel when $V_D = V_{DSat}$. From equations (3.4a) and (3.4b) it is clear that in order to increase I_P one should employ a device geometry with a large (Z/L) ratio, high mobility and low doping concentration in channel. The last requirement comes about because the depletion layer width at breakdown is approximately proportional to $(N_D)^{-1/2}$ and this makes the $N_A^2 a^3$ terms in I_P proportional to $(N_D)^{-1}$.

The saturation voltage is given by:

$$V_{DSsat} = V_P - V_{bi} - V_G = \frac{qN_A a^2}{2\epsilon_s} - \frac{kT}{q} \ln \left(\frac{N_A N_D}{n_i^2} \right) - V_G \quad (3.5)$$

The I_{DS} vs. V_{DS} current–voltage characteristic for one V_G value is sufficient to completely describe the device behavior for any channel impurity profile. The fundamental equation of the JFET can now be rewritten as:

$$I_{DS}(V_G, V_{DS}) = \int_{y_1}^{y_2} F(h) dh = \int_{y(V_G)}^{y(V_G+V_D)} F(h) dh \quad (3.6)$$

The integral can be split in two series to yield:

$$I_{DS}(V_G, V_{DS}) = \int_{y(0)}^{y(V_G+V_D)} F(h) dh + \int_{y(V_G)}^{y(0)} F(h) dh \quad (3.7) \quad \text{or}$$

$$I_{DS}(V_G, V_D) = I_{DS}(0, V_G + V_D) + I_{DS}(0, V_G) \quad (3.7a)$$

Equation (3.7a) states that if the relationship between I_{DS} and V_G is known in the case $V_G = 0$, the right–hand side of equation (3.7a) enables the calculation of I_{DS} for any combination of V_G and V_D [91].

3.2. Static characteristics

Channel conductance

The potential of point P in Fig. 3.1 is always fixed at the value V_{sat} given by equation (3.5) after pinch–off occurs. As the drain potential increases, the depletion layer width also increases uniformly in all directions and this causes the point P to move toward the source. The potential at the point P remains fixed at the same value but the effective distance (length) of the neutral channel from the source to drain reduces. This results in a finite value of the channel conductance in the saturation region and which depends on the applied drain bias.

Series resistance

Because of the finite distance between gate, source and drain, as show in figure 3.3, there also are the series resistances R_S (source resistance) and R_D (drain resistance) outside the channel region. These resistances, which cannot be modulated by the gate voltage, reduce the I_{DS} at the same applied drain and gate bias (as compared to the ideal device where such resistances are not present) and reduce both the drain conductance and the transconductance. For this reason, in equation (3.2), V_{DS} and V_G should be replaced by $V_{DS} - I_{DS} \cdot (R_S + R_D)$ and $V_G - I_{DS} R_S$, respectively.

The effect of the free carrier's mobility

As the electric field increases, the free carrier's mobility decreases, resulting in a decrease of the drain current. The general behavior of the I_{DS} versus V_{DS} characteristic, however, remains essentially the same.

The assumption of a constant mobility for the free carriers in the channel, irrespective of the drain voltage applied to JFET is valid as long as electric field along the channel remains below 1×10^3 V/cm (true for devices with long and/or narrow channels). At low gate bias voltage, the field dependence of mobility has several effects on the characteristics shown in Fig. 3.4:

- 1) It reduces the slope of the output characteristics near the origin;
- 2) Drain current saturation occurs at lower drain voltage [60].

Fig. 3.3. The parasitic serial resistances in a JFET: R_S (source resistance), R_D (drain resistance) and the drain conductance $(g_{D0})^{-1}$

Fig. 3.4. Effect of field dependence of mobility on the JFET characteristic curves: **red**—field dependent mobility, **black**—field independent mobility. [60]

Fig. 3.5. Characteristic curves for the JFET: a) output characteristics and b) transfer curve, respectively [62].

Analysis of I - V characteristics

Examples of typical characteristic curves of a JFET are shown in Fig. 3.5. Ideally, for a given gate voltage value V_G the current is nearly constant over a wide range of Source-to-Drain voltages if the transistor is operated in the saturated regime.

The control over the JFET is due to the depletion of charge carriers in the n -channel. When the gate potential is made more negative, a larger depletion zone is formed around the gate regions(s). This reduces the current flow for a given value of source-to-drain voltage. Therefore, modulating the gate voltage modulates the current flow through the device.

The transfer characteristic for the JFET is useful for visualizing the gain from the device and identifying the linearity region. The gain is proportional to the slope of the transfer curve. The current value I_{DSS} represents the maximum current for the device which is the value obtained when the gate is shorted to ground. The gate voltage at which the I_{DS} current reaches zero is called the "pinch voltage", V_P . Note that the dashed line representing the gain in the linear region of operation strikes the zero current line at about half the pinch voltage.

Understanding the classical characteristics of the JFET is the first step necessary toward the calculation of the optoelectric properties of the JFET sensor that will be presented in the next section.

3.3. The proposed color sensor

3.3.1. Generic structure of a JFET-based color sensor

A "photodetector" can be defined as a device that responds to the presence of optical radiation by producing an electromotive force or a variation in its electrical

resistance, which is independent of the spatial distribution of the optical radiation. An "optical sensor" however, can be considered a structure/system a broader meaning, i.e. in general it is an input device for the measurement, detection, analysis or recording, of light, or a part of a reproduction or transmission chain that is sensitive to optical radiation, e.g. due to the use of a photoelectric effect. An optical sensor can therefore include a plurality of photodetectors [61].

The above-mentioned definitions clearly indicate that a JFET sensitive to light could be considered a photosensitive semiconductor device. However, to employ such a device for color sensing requires a new re-thinking and redesign of its structure based on optical considerations in order to utilize it as such. For this reason, the first important aspect to be investigated will be the opto-electrical conversion process related to the collection of charge carriers generated in various regions of the JFET structure presented in Fig. 3.6.

The device proposed in this work has two gates: a top and bottom gate, respectively. The top gate is relatively short to provide very small series channel resistance for the device, while its surface impurity concentration is $N_A = 10^{18} \text{ cm}^{-3}$. The reason for this value is that the top gate junction has a small depth and a high doping value can improve the collection efficiency of the photogenerated carriers. Such shallow p -type layers, realized by implantation with a maximum concentration typically at the surface and an abruptly decreasing doping profile with increasing depth, will improve the efficiency of carriers collection in the short wavelength domain of visible spectrum. This strong gradient of p -type doping concentration creates an internal field that will affect the motion of the minority carriers (high doping effects).

The top gate also has a guard ring with the impurity concentration $N_A = 10^{20} \text{ cm}^{-3}$ necessary to protect the junction from accidental breakdown. Different voltages can be applied onto the top and bottom gates.

The impurity concentration of the channel region is selected low ($N_D = 10^{14} \text{ cm}^{-3}$) and the width of the channel region is selected small ($a=2 \text{ }\mu\text{m}$) so that the channel region can be easily pinched off by the depletion layer extending from the gate, so as to form an intrinsic gate of potential barrier type.

It is also possible, in the structure shown in Fig. 3.6, to reverse the roles of the source region and the drain regions that are identically fabricated.

Beside the fact of using for the first time such a JFET-structure for optical (and color) sensing, another entirely novel aspect of this device is that the bottom gate is

realized by growing a heavily doped p^+ -buried layer on top of a p -type silicon substrate as this can be achieved in a short period and more conveniently by epitaxial growth that makes the manufacture of the device easier.

Theoretically, a negative voltage is applied to the top gate and/or a positive voltage is applied unto the drain electrode and therefore the top gate junction is reverse biased even if no separate biasing potential is applied on the top gate. When light falls onto this photo-JFET, after passing through the transparent antireflection film deposited on the upper exposed surface of the device, electron-hole pairs will be generated.

First, the photogenerated holes flow into the top p^+ gate region, which has a lower potential for the holes, to thereby bias on this gate region. That is, a bias voltage is produced between the gate region and the channel region, which is the sum of the built-in potential (reverse bias) and the electromotive force produced as a result of irradiation by light. This electromotive force is determined by the amount of absorbed light, or in other words, by the amount of electric charge produced in the gate region and that determines the gate capacitance to increase. In accordance with an increase in the amount of irradiated light, the depletion layer has shrunk thereby increasing the width of the neutral channel region so that a resistive characteristic appears. Also, in case a potential barrier is produced in the middle of the channel region, the height of this potential barrier can be controlled by either the gate or the drain potential, and determine the device to exhibit a non-saturating type I_{DS} versus V_{DS} characteristic. Such a non-saturating characteristic enables enlargement of the output current simply by increasing the drain voltage.

Secondly, the photogenerated electrons will be directed towards the channel and will ultimately contribute to the I_{DS} current.

A similar process would happen in the depleted region of the bottom gate. The main difference between the top and bottom gate is that the first one will absorb short wavelength light (blue-violet) whereas the later one will detect long wavelength light (red).

One of the advantages of this JFET based sensing device is that light absorption and detection is not limited to the photodetector closest to the illuminated surface top gate junction such that there is an enhancement of collection of optically generated minority carriers. Another advantage is that such a JFET sensor can be used in three different operation modes. The first operation mode (*JFET mode*) simply employs each junction as a photodiode, hence the structure in this case could be considered rather a vertical two-junction device. In order to operate in *photoconductive mode* it is enough to establish a conduction path between the gate and the source regions.

Fig. 3.6. Schematic cross-sectional view of a proposed photo JFET structure indicating the photocurrent components and the layers in which the associated charge carriers are generated. The subscripts in the variable x denote the layer boundaries, with x_{1pc} , x_{2pc} , x_{1nc} and x_{2nc} describing the limits of the surface depletion layer, x_{sp} and $x_{1J} + x_{1n}$ those of the superior junction depletion layer in the top gate and channel, respectively, and, similarly, $x_{2J} - x_{3m}$ and $x_{2J} + x_{3p}$ are the boundaries of the lower junction depletion layer the channel and in the buried layer, respectively. This notation are used only on section 3.3.

If a resistor is connected between source and gate, the response speed will be determined by the capacitance of the gate region and the value of this resistor. This resistor or resistance may be formed within the same JFET device, e.g. diffusion or by using a thin resistive film, for example, polysilicon.

Another operation mode is the *photovoltaic mode* when the source and drain terminals are connected together. However, literature data indicate that the spectral response in this case is very low compared with the photoconductive and gate biasing modes described before.

The next section will study in detail the current-voltage characteristics of the proposed photo-JFET. The next section will study in detail the current-voltage characteristics of the proposed photo-JFET.

3.3.2. Theoretical analysis of the JFET-based color sensor

The final stage in the opto-electrical conversion process concerns the collection of generated charge carriers. This part offers the mathematical background for the device operation, with immediate important applications and implications regarding both the fabrication of the device, its optimization and its flexibility in operation. The generic basic device structure, characteristic for the proposed silicon-based JFET-based color sensor, consists of a layered doping profile as shown in Fig. 3.6. This figure also indicates the different current components and will, therefore, be used as a reference in the computations carried out to derive the equations presented in this section. It can also be seen that in such a device two depleted regions arise in which generated charge carriers are separated due to the high internal electric field and, in between, in the channel region, a quasi-neutral layer exists in which the diffusion of the photogenerated minority charge carriers and the drift of the majority ones are predominant. The upper-most depleted region is due to charge in the protective oxide layer whereas the other space charge regions occur on either side of a pn junction due to the built-in voltages, and may be enhanced by a reverse voltage applied across each junction. The structure depicted in Fig. 3.6 consists of a shallow p -type layer implanted in an n -epilayer on a p -type substrate and is thus compatible with a standard CMOS process. Although such an approach reveals obvious advantages, alternatives are quite possible and are indeed reported in the literature survey in the previous chapter. This restriction of the theoretical discussion to a most generic configuration offers the possibility to simplify the problem, since the epilayer and substrate doping can be considered to be constant and only the doping gradient of the shallow top gate p^+ -type layer has to be taken into account. Moreover, the

results that will be obtained remain valid and can also be applied equally well for different versions of the same basic device structure which will be introduced later, in subsequent sections. The charge collecting proprieties will now be discussed for a *PNP* structure of an *n*-channel JFET sensor, but the results are, apart from the obvious adaptations, also applicable in an *NPN* structure of a *p*-channel JFET device.

The steady-state response of a photodetector upon the generation of optically induced electron-hole pairs can be described by the current density equations, under the boundary conditions valid at that particular depth, and the continuity relations. The boundaries of the different layers can be derived by solving the Poisson equations for both the surface space-charge region and the two junction space-charge regions. This section will detail the entire device operation analysis derived starting from these equations.

The current density equation is generally composed of a drift current density component, proportional to the amount of charge traversing per unit of time a layer governed by an electric field, and of a diffusion component proportional to the diffusion coefficient and the carrier concentration gradient. For electrons, respectively holes, in the one-dimensional problem these are formulated by:

$$\begin{aligned} J_n &= q\mu_n n(x)E + qD_n \frac{dn(x)}{dx} & (a) \\ J_p &= q\mu_p p(x)E - qD_p \frac{dp(x)}{dx} & (b) \end{aligned} \quad (3.8)$$

in which μ_n and μ_p denote the electron, and hole mobilities, respectively, connected to the respective diffusion coefficients, D_n and D_p , through the Einstein relation $D_i = \frac{k \cdot T}{q} \cdot \mu_i$. [63].

The continuity equations describe the balancing process of excess minority charge carriers towards the thermal equilibrium density. The total rate of charge variation is, therefore, determined by the generation rate G and the recombination rate U [cm^{-3}/s] and the change in the minority current density according to:

$$\begin{aligned} \frac{\partial n_p(x)}{\partial t} &= G_n - U_n + \frac{1}{q} \frac{\partial J_n(x)}{\partial x} = G_n - \frac{n_p - n_{p0}}{\tau_n} + n_p(x) \mu_n \frac{\partial E(x)}{\partial x} + \\ &+ \mu_n E(x) \frac{\partial n_p(x)}{\partial x} + D_n \frac{\partial^2 n_p(x)}{\partial x^2} \end{aligned} \quad (3.9)$$

which results from the insertion of equation (3.8a) for J_n under the low injection conditions. In equation (3.9), $n_p(x)$ stands for the actual electron density in a *p*-type layer

and n_{p0} for the electron density in that layer at thermal equilibrium. The time constant τ_n refers to the electron lifetime in the p -type layer. A similar expression can be derived with respect to the holes in the n -doped layer:

$$\begin{aligned} \frac{\partial p_n(x)}{\partial t} = G_p - U_p + \frac{1}{q} \frac{\partial J_p(x)}{\partial x} = G_p - \frac{p_n - p_{n0}}{\tau_p} - p_n(x) \mu_p \frac{\partial E(x)}{\partial x} - \\ - \mu_p E(x) \frac{\partial p_n(x)}{\partial x} + D_p \frac{\partial^2 p_n(x)}{\partial x^2} \end{aligned} \quad (3.10)$$

in which the coefficients have the same meaning apart from the obvious adaptations. The electron and hole generation rates at depth x , $G_n(x)$ and $G_p(x)$, respectively, are caused by either external effects, such as incident photons or high-energy nuclear particles or by internal causes, such as impact ionization due to high electric fields. The discussion in this case naturally focuses on optically generated charge carriers.

The absorption process of incident photons can be modeled as a Poisson probability distribution with an average penetration depth equal to $1/\alpha(\lambda)$. Therefore, the probability of the absorption of a photon at the depth x is equal to $\alpha(\lambda) \exp(-\alpha(\lambda)x)$. The incident photon flux entering the silicon is equal to $I_o(\lambda)[1-R(\lambda)]$, where $I_o(\lambda)$ denotes the number of incident photons of wavelength λ and R is the silicon substrate's reflectivity. This leads to a generation rate at the depth x equal to

$$G(x) = I_o(\lambda)[1-R(\lambda)]\eta\alpha(\lambda)\exp(-\alpha(\lambda)x), \quad (3.11)$$

where the optical parameters have meanings indicated in the previous section. The photocurrents in the two junctions of the device shown in Fig. 3.6 can now be calculated by analyzing the individual contributions of the depleted and neutral layers.

The surface space-charge region originates from either mobile positive charges, such as sodium ions which might have entered the oxide during processing, or surface traps induced by high energy radiation, or the surface-state charge, or fast surface states that originate from the disruption of the silicon lattice at the interface [60]. In the color sensor proposed here, an oxide layer can also be applied as a masking material. This measure allows matching the oxide layer thickness with the projected range of the p -type dopant implanted in silicon in order to obtain a top gate region with a maximum in the doping profile at the surface [63]. However, this method also adds a significant concentration of B^+ ions into the oxide. The net result of all these charges is a surface electric field in the p^+ -type top gate layer, which attracts minority charge carriers to the $Si-SiO_2$ interface. Assuming a device structure having both a p^+ -type top gate layer with an abrupt impurity concentration change from a constant acceptor impurity to a constant

donor impurity N_d in the underlying n -type layer as well as a constant oxide charge concentration N_{ox} extending in the oxide from the silicon surface up to a distance x_{ox} , allows the calculation of the surface potential and the associated surface depletion layer using the Poisson equation. This equation states:

$$-\frac{\partial^2 V}{\partial x^2} = \frac{\partial E}{\partial x} = \frac{\rho(x)}{\epsilon} \quad (3.12)$$

Application of this equation in both the oxide and the upper layer yields two expressions for the surface potential:

$$\Phi_s = \frac{q}{\epsilon_o \epsilon_{SiO_2}} \int_{-x_{ox}}^0 \int N_{ox} dx dx = \frac{q}{\epsilon_o \epsilon_{Si}} \int_0^{x_{sp}} \int N_A dx dx \quad (3.13)$$

Hence:

$$x_{sp} = x_{ox} \sqrt{\frac{N_{ox} \epsilon_{Si}}{N_A \epsilon_{SiO_2}}} \quad (3.14)$$

Minority charge carriers captured within this surface depleted region will be swept to the silicon surface and will recombine there because of the high density of surface states. This simplified model shows one of the reasons for a poorer quantum efficiency at short wavelengths where the penetration depth is minimum. A possible improvement would involve the implantation of negative charges in the oxide to compensate for the positive oxide charge (stripping the B^+ dopes oxide and growing a new one may not eliminate the charge since the Si substrate consumed during the oxide growth is also B^+ doped, hence B^+ ions will remain incorporated in the new oxide layer, too, although their concentration may be different from that implanted in the first oxide). Alternatively, a transparent metal MOS gate biased to a negative voltage sufficient to cause flatband at the surface of this MOS system in the top gate region will yield a similar improvement. For this latter solution care must be taken in considering the possible optical influence due to wavelength dependent absorption in this top electrode. In particular the thoughtless application of relatively thick polysilicon gates is most undesirable due to polysilicon's large absorption coefficient for blue and green light, [49], which will render ineffective most of our device (except the bottom junction which can still detect the red component of the visible spectrum).

Another conclusion arising from equation (3.14) concerns the advantage of having a high surface acceptor doping density. This conclusion is only valid up to a concentration of about 10^{18} cm^{-3} , as it is a consequence of the introduced assumptions with respect to the top gate doping profile and the neglecting of any high doping effects in this region.

The actual implanted layer will reveal a maximum surface concentration at a projected range determined by the implant dose and a decreasing density with increasing depth. The internal field induced by this doping gradient affects the motion of the minority carriers and this effect can be reflected accordingly in the carrier density equations. In thermodynamic equilibrium conditions the majority carriers current density in the top layer must equal zero, as charge carriers have nowhere to go, which yields [64]:

$$J_p = q\mu_p N_A(x)E(x) - qD_p \frac{\partial N_A(x)}{\partial x} = 0 \quad (3.15)$$

Hence,

$$E(x) = \frac{D_p}{\mu_p} \cdot \frac{1}{N_A(x)} \cdot \frac{\partial N_A(x)}{\partial x} = \frac{kT}{q} \cdot \frac{1}{N_A(x)} \cdot \frac{\partial N_A(x)}{\partial x} \quad (3.16)$$

This effect would result in an electric field repelling the minority charge carriers from the surface interface as the doping concentration decreases at greater depths and would therefore enhance the spectral response in the blue-UV part of the spectrum. However, two different effects oppose this conclusion. The first effect arises from the redistribution of boron into the oxide during annealing due to its segregation coefficient being smaller than unity, resulting in a decreased doping concentration in Si towards the surface and a subsequent majority-carrier dragging field near the surface. Therefore, an implantation energy with an associated projected range slightly greater than the oxide thickness and a relatively low-temperature annealing must be applied.

The second effect originates from the occurrence of a different recombination mechanism at high impurity concentrations, the Auger process. For lightly doped silicon crystals the energy levels of the impurity atoms can be considered discrete, as their number is small enough to avoid overlap and to maintain perfect periodicity of the crystal. Therefore, the edges of the valence and conduction band are well defined. An increased doping concentration causes the formation of impurity bands and a tail instead of an edge in the valence and conduction band and thus leads to a narrowing of the band gap. This effect does not only affect the optical properties, as the wavelength dependence of absorption is directly related to the size and shape of the band gap, but also results in a higher intrinsic carrier concentration, $n_i = \sqrt{N_C N_V} \exp\left(-\frac{E_g}{kT}\right)$, at increasing doping density and constant temperature. The latter is usually accounted for by introducing a net

intrinsic carrier concentration, $n_{ie} = n_i \exp\left(-\frac{E_g}{kT}\right)$, which subsequently leads to a

decreased net doping, $N_{eff}(x) = \frac{N(x)}{\left(\frac{n_{ie}}{n_i}\right)^2}$, at a projected increased profile and becomes

predominant at doping levels exceeding 10^{19} cm^{-3} . Therefore, an extra retarding field can occur in the p -type top layer, driving the minority charge carriers towards the surface charge region, which might subsequently lead to a further reduction of the low-wavelength quantum efficiency. This detrimental effect can be avoided by limiting the surface concentration to the already prescribed $N_A(0) = 10^{18} \text{ cm}^{-3}$. Under this restriction equation (3.14) can be applied safely for obtaining the boundary of the shallow layer in which generated charge carriers will be lost.

The total photocurrent density generated in this surface depleted layer can be calculated by integration of the generation rate over the entire layer thickness, which yields:

$$\begin{aligned} J_{sd} &= I_o(\lambda) \cdot [1 - R(\lambda)] \cdot \eta q \cdot \alpha(\lambda) \int_0^{x_{sp}} e^{-\alpha(\lambda)x} dx \Rightarrow \\ J_{sd} &= I_o(\lambda) \cdot [1 - R(\lambda)] \cdot \eta q \cdot \left[1 - e^{-\alpha(\lambda)x_{sp}}\right] \end{aligned} \quad (3.17)$$

This component does not contribute to the detected photocurrent as the charge carriers recombine at the surface and consequently poor quantum efficiency is generally observed at the short wavelength part of the visible spectrum due to the high corresponding absorption coefficient. Much research has been performed to improve the properties of the silicon photodiodes in this respect.

The width of the space charge region extending on either side of a pn junction can also easily be derived using the Poisson equation. For a one-dimensional abrupt junction approximation one obtains the following results for the upper junction [63]:

$$\begin{aligned} -\frac{\partial^2 V}{\partial x^2} &= \frac{\partial E}{\partial x} = \frac{\rho(x)}{\epsilon} = -\frac{q}{\epsilon_o \epsilon_{Si}} \cdot N_A \quad \text{for } x_{1p} \leq x \leq x_{1J} \\ -\frac{\partial^2 V}{\partial x^2} &= \frac{\partial E}{\partial x} = \frac{\rho(x)}{\epsilon} = -\frac{q}{\epsilon_o \epsilon_{Si}} \cdot N_D \quad \text{for } x_{1J} \leq x \leq x_{1n} \end{aligned} \quad (3.18)$$

$$\begin{aligned} -\frac{\partial^2 V}{\partial x^2} &= \frac{\partial E}{\partial x} = \frac{\rho(x)}{\epsilon} = -\frac{q}{\epsilon_o \epsilon_{Si}} \cdot N_A \quad \text{for } x_{2p} \leq x \leq x_{1J} \\ -\frac{\partial^2 V}{\partial x^2} &= \frac{\partial E}{\partial x} = \frac{\rho(x)}{\epsilon} = -\frac{q}{\epsilon_o \epsilon_{Si}} \cdot N_D \quad \text{for } x_{1J} \leq x \leq x_{2n} \end{aligned} \quad (3.19)$$

Hence,

$$x_{1n} = \sqrt{\frac{2\epsilon_s(V_{TG} + V_{bi})}{qN_D}} \quad x_{2n} = \sqrt{\frac{2\epsilon_s(V_D + V_{TG} + V_{bi})}{qN_A}}$$

$$\begin{aligned}
 x_{1p} &= \sqrt{\frac{2\epsilon_s(V_{TG} + V_{bi})N_D}{qN_A^2}} & x_{2p} &= \sqrt{\frac{2\epsilon_s(V_D + V_{TG} + V_{bi})N_D}{qN_A^2}} \\
 x_{1J} - x_{1p} &= \frac{N_D}{N_D + N_A} \sqrt{\frac{2\epsilon_o\epsilon_{Si}}{q} \cdot (V_{bi} + V_{TG}) \cdot \left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \\
 x_{1n} - x_{1J} &= \frac{N_A}{N_D + N_A} \sqrt{\frac{2\epsilon_o\epsilon_{Si}}{q} \cdot (V_{bi} + V_{TG}) \cdot \left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \\
 x_{1J} - x_{2n} &= \frac{N_A}{N_D + N_A} \sqrt{\frac{2\epsilon_o\epsilon_{Si}}{q} \cdot (V_{bi} + V_{TG} + V_D) \cdot \left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \\
 x_{2p} - x_{1J} &= \frac{N_D}{N_D + N_A} \sqrt{\frac{2\epsilon_o\epsilon_{Si}}{q} \cdot (V_{bi} + V_{TG} + V_D) \cdot \left(\frac{1}{N_A} + \frac{1}{N_D}\right)}
 \end{aligned} \tag{3.20}$$

where V_{bi} denotes the built-in diffusion potential equal to $\frac{kT}{q} \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right)$ and V_G , and V_D are the gate voltage applied across the upper junction, and the drain bias voltage, respectively. Similarly, the boundaries of the depleted regions on either side of the lower junction can be found to be equal to:

$$\begin{aligned}
 x_{2J} - x_{1n} &= \frac{N_A}{N_D + N_A} \sqrt{\frac{2\epsilon_o\epsilon_{Si}}{q} \cdot (V_{bi} + V_{TG}) \cdot \left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \\
 x_{1p} - x_{2J} &= \frac{N_D}{N_D + N_A} \sqrt{\frac{2\epsilon_o\epsilon_{Si}}{q} \cdot (V_{bi} + V_{TG}) \cdot \left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \\
 x_{2J} - x_{2n} &= \frac{N_A}{N_D + N_A} \sqrt{\frac{2\epsilon_o\epsilon_{Si}}{q} \cdot (V_{bi} + V_{TG} + V_D) \cdot \left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \\
 x_{2p} - x_{2J} &= \frac{N_D}{N_D + N_A} \sqrt{\frac{2\epsilon_o\epsilon_{Si}}{q} \cdot (V_{bi} + V_{TG} + V_D) \cdot \left(\frac{1}{N_A} + \frac{1}{N_D}\right)}
 \end{aligned} \tag{3.21}$$

All charge carriers generated within a junction depletion layer are collected in the respective junction as the propagation time across the depletion region is much smaller than the carrier lifetime due to built-in electric field. Using equations (3.17–3.21) and considering $d = x_{1n} + x_{1p}$ and $w + d = x_{2n} + x_{2p} \Rightarrow w = x_{2n} + x_{2p} - d = x_{2n} + x_{2p} - x_{1n} - x_{1p}$, the photocurrent in the upper junction depleted region is therefore equal to:

$$\begin{aligned}
 J_{sd} &= I_o(\lambda)[1 - R(\lambda)]hq\alpha(\lambda) \int_0^{f(y)} e^{-\alpha(\lambda)x} dx dy = \\
 &= I_o(\lambda)[1 - R(\lambda)]hq \cdot \left\{ 1 + \frac{\exp(-\alpha(\lambda) \cdot (x_{1n} + x_{1p}))}{\alpha(\lambda)(x_{2n} + x_{2p} - x_{1n} - x_{1p})} [\exp(-\alpha(\lambda)(x_{2n} + x_{2p} - x_{1n} - x_{2n})) - 1] \right\}
 \end{aligned} \tag{3.22}$$

where the subscripts have the meaning already depicted in figure 3.6. Similarly, the photocurrent in the bottom gate junction depleted region can be described by:

$$J_{ld} = I_o(\lambda)[1 - R(\lambda)]\eta q \alpha(\lambda) \int_0^{f(y)} e^{-\alpha(\lambda)x} dx dy =$$

$$= I_o(\lambda)[1 - R(\lambda)]\eta q \cdot \left\{ 1 + \frac{\exp(-\alpha(\lambda)(x_{3n} + x_{3p}))}{\alpha(\lambda)(x_{4n} + x_{4p} - x_{3n} - x_{3p})} [\exp(-\alpha(\lambda)(x_{4n} + x_{4p} - x_{3n} - x_{3p}) - 1)] \right\}$$

(3.23)

where

$$x_{3n} = \sqrt{\frac{2\epsilon_s(V_{BG} + V_{bi})}{qN_D}} \quad x_{4n} = \sqrt{\frac{2\epsilon_s(V_D + V_{BG} + V_{bi})}{qN_A}}$$

$$x_{3p} = \sqrt{\frac{2\epsilon_s(V_{BG} + V_{bi})N_D}{qN_A^2}} \quad x_{4p} = \sqrt{\frac{2\epsilon_s(V_D + V_{BG} + V_{bi})N_D}{qN_A^2}}$$

If the same gate voltage value is applied on both the top and bottom gates then the depleted regions will have the same widths ($x_{3n} = x_{1n}$, $x_{3p} = x_{1p}$, $x_{4n} = x_{2n}$, $x_{4p} = x_{2p}$) and hence the density current will also be the same if the doping concentrations of the two gates will be identical.

Minority charge carriers generated within the non-depleted part of the *p*-type implanted layer are assumed to drift towards x_{1p} due to the electrical field created by the flux of majority carrier, described by equation(3.16), resulting in an extra current density component at x_{1p} equal to:

$$J_{up} = I_o(\lambda)[1 - R(\lambda)]\eta q \cdot \alpha(\lambda) \int_0^{f(y)} e^{-\alpha(\lambda)x} dx dy =$$

$$= I_o(\lambda)[1 - R(\lambda)]\eta q \cdot \left\{ 1 + \frac{\exp[-\alpha(\lambda) \cdot (x_{1j} - x_{2p} - x_{sd})]}{\alpha(\lambda) \cdot (x_{2p} - x_{1p})} \cdot [\exp(-\alpha(\lambda) \cdot (x_{2p} - x_{1p})) - 1] \right\}$$

(3.24)

The final issue that has to be considered with respect to the collection efficiency is the extent to which charge carriers generated in a quasi-neutral layer in between depleted layers contribute to the photocurrent and, moreover, to which of the respective junctions will the diffusion current prevail.

We calculated the current-voltage characteristics based on the gradual channel approximation presented in detail in Appendix 1. It states that the carrier density related to the variation of the electric field E_x in the x direction (along the channel) is much smaller than that related to the variation of the electric field E_y in the y direction

(perpendicular on the channel): $\frac{dE_x}{dx} \ll \frac{dE_y}{dy}$. Therefore the electric field in the depletion

region may be considered in the y direction only and the electric field in the channel may be considered in the x direction only. This separation allows us to solve the two-dimensional problem in a one-dimensional manner.

Consequently, the diffusion in the neutral part of the epilayer and substrate can be calculated by solving the continuity relation in a neutral layer where $E(x) = E_x$ under the appropriate boundary conditions and the insertion of the result in the current density equation at both the adjacent lower boundary of the upper junction and upper boundary of the lower junction.

Assuming a positive voltage applied to the drain, with the gate-source voltage kept at a constant value, a non-uniform depletion width occurs along the channel as presented in Fig. 3.6. As V_{DS} is made more positive the width of the depletion layer at the end of the channel increases, and thus the incremental channel conductance will decrease. Thus, if the channel is long compared with its thickness, then the channel will pinch-off at the drain end and the channel current will saturate at a drain-gate voltage equal and of opposite sign of pinch-off voltage. The degree of saturation is a function of the device geometry. A long channel will become more saturated (have a lower $\frac{dI_D}{dV_{DS}}$) than a short channel.

First, by solving the continuity relation in a neutral layer where $E(x) = E_x$ the constant value of the longitudinal field is given by:

$$E_x = \frac{V_D}{L_{eff}} \quad (3.25)$$

where L_{eff} is the effective length of the channel. The effective length of the channel depends of the specific state of JFET which are depicted in fig 3.7.(a-c):

- In the linear state $V_D < V_P$, given by equation (3.4b), presented in fig 3.7.(a) and in the pinch-off state $V_P \leq V_D \leq V_{DSat}$. The potential at the end of the channel (point P in fig 3.7(b)) is fixed at the value V_{sat} given by equation (3.5) the effective length of the channel is equal with the device length $L_{eff} = L_{channel}$.
- In the saturation state $V_D \geq V_{DSat}$ (presented in fig 3.7.(c)) As the drain potential increases, the depletion layer width also increases uniformly in all direction and this causes the point P to move toward the source. The voltage at the point P remains fixed at same value but the effective channel distance from the source to drain reduces. The n -channel and the drain terminal are separated now by a space

charge region which has the length ΔL and L_{eff} is the effective length of the channel.

Fig. 3.7. (a) Space charge regions in channel and I - V characteristics for zero gate voltage for a small drain voltage

Fig. 3.7. (b) Space charge regions in channel and I - V characteristics for zero gate voltage for a drain voltage to achieve the pinch – off voltage V_P

Fig. 3.7. (c) Space charge regions in channel and I - V characteristics for zero gate voltage for a drain voltage to higher than drain saturation voltage V_{DSat} . The n -channel and drain terminal are separated now by a space charge region which has the length ΔL

The continuity relation for electrons in the neutral part of the channel states can be used for the all situation presented in Fig 3.7.:

$$D_n \frac{\partial^2 n_p(x)}{\partial x^2} - \frac{n_p - n_{p0}}{\tau_n} + I_o(\lambda)[1 - R(\lambda)]\eta\alpha(\lambda)e^{-\alpha(\lambda)x} - \frac{V_D}{L_{eff}} = 0 \quad (3.26)$$

We will solve this expression for the state $0 \leq V_D \leq V_p$, because in the case of the saturation state $V_D \geq V_{DSat}$ (presented in fig 3.7(c)) equation (3.26) becomes a double non-homogenous, once because of existence of the so called free term $\left(\frac{V_D}{L_{eff}}\right)$ and secondly, because of the field dependencies of the distance.

It is well-known that the solutions of the non-homogenous equation are based on particular solutions of the attached homogeneous equation that in this case is equation:

$$D_n \frac{\partial^2 n_p(x)}{\partial x^2} - \frac{n_p - n_{p0}}{\tau_n} + I_o(\lambda)[1 - R(\lambda)]\eta\alpha(\lambda)e^{-\alpha(\lambda)x} = 0 \quad (3.26a)$$

Applying the boundary conditions $n_p(x_{un}) = n_{p0}$ and $n_p(x_{ln}) = n_{p0}$ yields $n_p(x_{un}) = n_{p0}$ and $n_p(x_{ln}) = n_{p0}$ yields $p_n(x)$ for $x_{1J} + x_{1n} < x < x_{2J} - x_{3n}$:

$$\begin{aligned} n_p(x) = & \frac{I_o(\lambda)[1 - R(\lambda)]\eta\alpha(\lambda)}{D_n((1/L_n)^2 - \alpha(\lambda)^2)} \left\{ \frac{\exp\left[-\alpha(\lambda)(x_{2J} - x_{3p}) - \frac{(x_{2J} - x_{3p})}{L_n}\right]}{\exp\left[-2 \cdot \frac{(x_{1J} + x_{1p})}{L_n}\right] - \exp\left[-2 \cdot \frac{(x_{2J} - x_{3p})}{L_n}\right]} - \right. \\ & - \frac{\exp\left[-\alpha(\lambda)(x_{1J} + x_{1p}) - \frac{(x_{1J} + x_{1p})}{L_n}\right]}{\exp\left[-2 \cdot \frac{(x_{1J} + x_{1p})}{L_n}\right] - \exp\left[-2 \cdot \frac{(x_{2J} - x_{3p})}{L_n}\right]} \times \exp\left(-\frac{x}{L_n}\right) + \\ & + \frac{\exp\left[-\alpha(\lambda)(x_{2J} - x_{3p}) + \frac{(x_{2J} - x_{3p})}{L_n}\right] - \exp\left[-\alpha(\lambda)(x_{1J} + x_{1n}) + \frac{(x_{1J} + x_{1n})}{L_p}\right]}{\exp\left(2 \cdot \frac{(x_{1J} + x_{1p})}{L_n}\right) - \exp\left(2 \cdot \frac{(x_{2J} - x_{3n})}{L_p}\right)} \times \\ & \left. \times \exp\left(\frac{x}{L_p}\right) + \exp(-\alpha(\lambda)x) + \frac{V_D}{L_{eff}} x \right\} \quad (3.27) \end{aligned}$$

where L_n denotes the diffusion length of electrons in the n -type layer: $L_n = \sqrt{D_n \tau_n}$. The current density equation describing the photocurrent entering the upper junction depleted region at $x = x_{ln}$ can be obtained by insertion of the continuity relation in:

$$\begin{aligned}
 J_{sn} = J_n|_{(x_{1J}+x_{1n})} &= -qD_p \frac{dn(x)}{dx} \Big|_{(x_{1J}+x_{1n})} = \frac{I_o(\lambda)[1-R(\lambda)]\eta\alpha(\lambda)L_{1pm}}{1-(\alpha(\lambda)L_{1pm})^2} \times \\
 &\times \left\{ \frac{\exp\left(-\alpha(\lambda)(x_{2J}-x_{3n})-\frac{x_{2J}-x_{3n}+x_{1J}+x_{1n}}{L_{1pm}}\right) - \exp\left(-\alpha(\lambda)(x_{1J}+x_{1n})-\frac{2(x_{1J}+x_{1n})}{L_{1pm}}\right)}{\exp\left(\frac{-2(x_{1J}+x_{1n})}{L_{1pm}}\right) - \exp\left(\frac{-2(x_{1J}+x_{1n})}{L_{1pm}}\right)} \right. \\
 &- \frac{\exp\left(-\alpha(\lambda)(x_{2J}-x_{3n})+\frac{x_{2J}-x_{3n}+x_{1J}+x_{1n}}{L_{1pm}}\right) - \exp\left(-\alpha(\lambda)(x_{1J}+x_{1n})+\frac{2(x_{1J}+x_{1n})}{L_{1pm}}\right)}{\exp\left(\frac{2(x_{1J}+x_{1n})}{L_{1pm}}\right) - \exp\left(\frac{2(x_{1J}+x_{1n})}{L_{1pm}}\right)} + \\
 &\left. - + \alpha(\lambda)L_{1pm} \exp[-\alpha(\lambda)(x_{1J}+x_{1n})] \right\} \quad (3.28)
 \end{aligned}$$

In a similar manner the current density equation describing the photocurrent entering the lower junction depleted region at $x = x_{3n}$ can be obtained

$$\begin{aligned}
 J_{ln} = J_n|_{(x_{2J}-x_{3n})} &= -qD_n \frac{dn(x)}{dx} \Big|_{(x_{2J}-x_{3n})} = \frac{I_o(\lambda)[1-R(\lambda)]\eta\alpha(\lambda)L_{2pm}}{1-(\alpha(\lambda)L_{2pm})^2} \times \\
 &\times \left\{ \frac{\exp\left(-\alpha(\lambda)(x_{2J}-x_{3n})-\frac{2(x_{2J}-x_{3n})}{L_{2pm}}\right)}{\exp\left(\frac{-2(x_{1J}+x_{1n})}{L_{2pm}}\right) - \exp\left(\frac{-2(x_{2J}-x_{3n})}{L_{2pm}}\right)} - \right. \\
 &- \frac{\exp\left(-\alpha(\lambda)(x_{1J}+x_{1n})-\frac{(x_{2J}-x_{3n})+x_{1J}+x_{1n}}{L_{2pm}}\right)}{\exp\left(\frac{-2(x_{1J}+x_{1n})}{L_{2pm}}\right) - \exp\left(\frac{-2(x_{2J}-x_{3n})}{L_{2pm}}\right)} - \\
 &- \frac{\exp\left(-\alpha(\lambda)(x_{2J}-x_{3n})+\frac{2(x_{2J}-x_{3n})}{L_{2pm}}\right)}{\exp\left(\frac{2(x_{1J}+x_{1n})}{L_{2pm}}\right) - \exp\left(\frac{2(x_{2J}-x_{3n})}{L_{2pm}}\right)} - \\
 &- \frac{\exp\left(-\alpha(\lambda)(x_{2J}-x_{3n})+\frac{(x_{2J}-x_{3n})+x_{1J}+x_{1n}}{L_{2pm}}\right)}{\exp\left(\frac{2(x_{1J}+x_{1n})}{L_{2pm}}\right) - \exp\left(\frac{2(x_{2J}-x_{3n})}{L_{2pm}}\right)} + \\
 &\left. + \alpha(\lambda)L_{2pm} \exp[-\alpha(\lambda)(x_{2J}-x_{3n})] \right\} \quad (3.29)
 \end{aligned}$$

The photocurrent detected in the lower junction also contains a component due to charge carriers generated beyond the lower boundary of its space charge region and able to diffuse towards this region, which can be described by the current density equation at $x = x_{2J} + x_{3pc}$. In this case, however, it is not needed to use different boundary conditions for solving the continuity relation, as two depleted layers enclose this quasi-neutral layer (i.e. the portion of the channel left un-depleted).

The actual boundary conditions in this problem are therefore described by $n_p(x_{2J} + x_{3pc}) = n_{p0}$ and $n_p(x_{2J}) = n_{p0} + (D_n/S_n)(\partial n_p(x)/\partial x)$, where S_n denotes the recombination velocity of electrons at the rear surface of this p^+ -type layer. Applying these conditions to the continuity equation for electrons yields $n_p(x)$ for $x_{2J} + x_{3pc} < x < x_{2J}$:

$$\begin{aligned}
 n_p(x) = & \frac{I_o(\lambda)[1-R(\lambda)]\eta\alpha(\lambda)}{D_n((1/L_{3nm})^2 - \alpha(\lambda)^2)} \times \\
 & \times \left\{ \left(\left(1 - \frac{D_n}{S_n L_{3nm}} \right) \exp \left[-\alpha(\lambda)(x_{2J} + x_{3p}) - \frac{x_{2J} + x_{3p}}{L_{3nm}} \right] \right. \right. \\
 & \left. \left. - \left(\left(1 + \frac{D_n}{S_n L_{3nm}} \right) \exp \left(-2 \frac{x_{2J}}{L_{3nm}} \right) - \left(1 - \frac{D_n}{S_n L_{3nm}} \right) \exp \left[-2 \frac{(x_{2J} + x_{3p})}{L_{3nm}} \right] \right) \right. \right. \\
 & \left. \left. - \frac{\left(1 + \frac{\alpha(\lambda) D_n}{S_n} \right) \exp \left(-\alpha(\lambda) x_{2J} - \frac{x_{2J}}{L_{3nm}} \right)}{\left(1 + \frac{D_n}{S_n L_{3nm}} \right) \exp \left(-2 \frac{x_{2J}}{L_{3nm}} \right) - \left(1 - \frac{D_n}{S_n L_{3nm}} \right) \exp \left[-2 \frac{(x_{2J} + x_{3p})}{L_{3nm}} \right]} \right\} \times \\
 & \times \exp \left(-\frac{x}{L_{3nm}} \right) + \left(\frac{\left(1 + \frac{D_n}{S_n L_{3nm}} \right) \exp \left[-\alpha(\lambda)(x_{2J} + x_{3p}) + \frac{x_{2J} + x_{3p}}{L_{3nm}} \right]}{\left(1 - \frac{D_n}{S_n L_{3nm}} \right) \exp \left(2 \frac{x_{2J}}{L_{3nm}} \right) - \left(1 + \frac{D_n}{S_n L_{3nm}} \right) \exp \left[2 \frac{(x_{2J} + x_{3p})}{L_{3nm}} \right]} \right. \\
 & \left. - \frac{\left(1 + \frac{\alpha(\lambda) D_n}{S_n} \right) \exp \left[-\alpha(\lambda) x_{2J} + \frac{x_{2J}}{L_{3nm}} \right]}{\left(1 - \frac{D_n}{S_n L_{3nm}} \right) \exp \left(2 \frac{x_{2J}}{L_{3nm}} \right) - \left(1 + \frac{D_n}{S_n L_{3nm}} \right) \exp \left[2 \frac{(x_{2J} + x_{3p})}{L_{3nm}} \right]} \right) \times \\
 & \times \exp \left(\frac{x}{L_{3nm}} \right) - \exp(-\alpha(\lambda)x) \Big\}
 \end{aligned} \tag{3.29}$$

The current density equation describing the photocurrent entering the lower junction depleted region at $x = x_{2J} + x_{3pc}$ can be obtained by intersection of the continuity relation in:

$$\begin{aligned}
 J_{ln} = J_n|_{(x_{2J}+x_{3p})} &= -qD_n \frac{dn(x)}{dx} \Big|_{(x_{2J}+x_{3p})} = \frac{I_o(\lambda)[1-R(\lambda)]\eta\alpha(\lambda)L_{3nm}}{1-(\alpha(\lambda)L_{3nm})^2} \times \\
 &\times \left\{ \left(1 + \frac{D_n}{S_n L_{3nm}}\right) \exp\left[-\alpha(\lambda)(x_{2J} + x_{3p}) + \frac{(x_{2J} + x_{3p})}{L_{3nm}}\right] \right. \\
 &\left. - \left[\left(1 - \frac{D_n}{S_n L_{3nm}}\right) \exp\left(\frac{2x_{2J}}{L_{3nm}}\right) - \left(1 + \frac{D_n}{S_n L_{3nm}}\right) \exp\left[\frac{2(x_{2J} + x_{3p})}{L_{3nm}}\right] \right] \right. \\
 &\left. - \frac{\left(1 + \frac{\alpha(\lambda)D_n}{S_n}\right) \exp\left[-\alpha(\lambda)x_{2J} + \frac{x_{2J}}{L_{3nm}}\right]}{\left(1 - \frac{D_n}{S_n L_{3nm}}\right) \exp\left(\frac{2x_{2J}}{L_{3nm}}\right) - \left(1 + \frac{D_n}{S_n L_{3nm}}\right) \exp\left[\frac{2(x_{2J} + x_{3p})}{L_{3nm}}\right]} \right. \\
 &\left. - \frac{\left(1 - \frac{D_n}{S_n L_{3nm}}\right) \exp\left[-\alpha(\lambda)(x_{2J} + x_{3p}) - \frac{(x_{2J} + x_{3p})}{L_n}\right]}{\left(1 + \frac{D_n}{S_n L_{3nm}}\right) \exp\left(-\frac{2x_{2J}}{L_{3nm}}\right) - \left(1 - \frac{D_n}{S_n L_{3nm}}\right) \exp\left[-\frac{2(x_{2J} + x_{3p})}{L_{3nm}}\right]} \right. \\
 &\left. - \frac{\left(1 + \frac{\alpha(\lambda)D_n}{S_n}\right) \exp\left[-\alpha(\lambda)x_{2J} + \frac{x_{2J}}{L_{3nm}}\right]}{\left(1 + \frac{D_n}{S_n L_{3nm}}\right) \exp\left(-\frac{2x_{2J}}{L_{3nm}}\right) - \left(1 - \frac{D_n}{S_n L_{3nm}}\right) \exp\left[-\frac{2(x_{2J} + x_{3p})}{L_{3nm}}\right]} \right. \\
 &\left. - \alpha(\lambda)L_{3nm} \exp[-\alpha(\lambda)(x_{2J} + x_{3p})] \right\}
 \end{aligned} \tag{3.30}$$

The subscripts have the same meaning as indicated in figure 3.6. In literature, equations (3.27) through (3.30) for similar structures are sometimes expressed in hyperbolic functions, which is a result of having made a different choice for the homogenous solution of the continuity relation [61, 65]. As $\cosh(x)$ and $\sinh(x)$ can be expressed in terms of $\exp(x)$ and $\exp(-x)$, these two types of expressing the solutions are interchangeable.

The value of the various photocurrent components and the total photocurrent detected in the top junction, $J_s = J_{ud} + J_{up} + J_{un}$, and that in the bottom junction $J_l = J_{ld} + J_{lp} + J_{ln}$, for a certain sensor configuration were used in a MATLAB simulations, whose results will be shown later, in chapter 5.

Chapter FOUR: Modeling of JFET structures

The modeling of JFET structure was made in two stages: first, MATLAB simulations and, after that, TCAD simulations have been performed. In all model building various assumptions were considered and it was also required that certain conditions should be met for estimating the desirable output characteristics. A more useful improvement is obtained when using an iterative approach because it is logical to move through stages of simulations, each stage providing insight as to how the next simulation step should be run.

4.1. MATLAB simulation of theoretical JFET

The starting point was the study of the characteristic curves of a classical JFET. In essence, JFET's are "normally on" (normally-saturated) devices. The application of a reverse-biasing voltage between gate and source causes the depletion region of that junction to expand, thereby "pinching off" the channel between source and drain through which the controlled current travels. If a reverse voltage is applied between the gate and source V_{GS} one can control the current between source and drain by varying the value of V_{GS} .

Recalling equation (3.2), one can see that the performance of a JFET is affected by the following factors: structural (geometric) dimensions and device (or material) parameters such as the type of doping and resistivity of various regions which are directly influenced by the impurity doping profiles and junction layer thicknesses.

MATLAB simulations of the equations (3.2–3.5) provide some rough but useful estimations which can indicate if the device would work properly with the desired design values of the geometrical and material parameters such as doping concentrations, junction depths, and reverse bias voltage V_{GS} .

All simulations examined the variation of one or two device parameters as a function of just one of the studied variables while maintaining the others constant.

Fig. 4.1. Variation of I_D as a function of the channel length L

Fig. 4.2. Variation of I_D as a function of half channel depth a

Fig. 4.3. Variation of I_D as a function of the channel doping concentration N_D

Fig. 4.4. Variation of I_{Dsat} as function I_P and V_P , as determined by the variation of the half channel depth a

Fig. 4.5. Variation of V_p as a function of I_p and the value of channel doping concentration N_D

Fig. 4.6. Variation of V_{Dsat} associated with I_{Dsat} function of the half channel depth a

This dependence associated with previous graphs “(Fig. 4.1–6)” shows us that all parameters are linear dependent of geometrical parameters with two exceptions: the channel doping and the device length. Therefore, all important device characteristics resulted in a sequential choice of the following values for the geometrical and device parameters $N_D = 10^{16} \text{ cm}^{-3}$, $Z = 4 \text{ }\mu\text{m}$; $a = 2 \text{ }\mu\text{m}$; $L = 12 \text{ }\mu\text{m}$ for the next step in simulation: the variation of I_D , V_{DS} , I_P and V_P as function of V_G and V_D , presented in figure 4.7.

Another investigated aspect was the influence of the gate junction depth. It can be seen in Fig. 4.8 a difference of only $0.03 \text{ }\mu\text{m}$ in the gate junction depth produce a variation of 0.4 mA in saturation source–drain current.

Using photocurrent equations (3.25) and (3.28) and the geometrical parameters established above the photocurrents generated in the different regions of the interest of the device were obtained from MATLAB simulations. These results are shown in Fig. 4.9.

Fig. 4.7 Variation of I_D function of V_D @ constant V_G

Fig. 4.8 Influence of the depth of gate junction on I_D

Fig. 4.9. Photo-responses for the top gate, channel and bottom gate regions of a photo-JFET, as resulted from MATLAB simulations for a device with the following geometrical parameters:

Channel with $N_D = 10^{16} \text{ cm}^{-3}$, $Z = 4 \text{ μm}$, $a = 2 \text{ μm}$, $L = 12 \text{ μm}$, Source and Drain with $N_A = 10^{18} \text{ cm}^{-3}$, Top Gate with $x_{TG} = 0.08 \text{ μm}$, $N_{TG} = 4.5 \cdot 10^{16} \text{ cm}^{-3}$.

However, these MATLAB simulations results were obtained considering only the theoretical equations describing the behavior of ideal devices. Therefore, in order to take into account the realistic effects taking place in actual devices, the previous calculation must be completed by TCAD simulations carried out using TSuprem and MEDICI for the technological fabrication optimization and device characterization, respectively.

4.2. TCAD modeling of JFET structures

4.2.1. Introduction

The facilities of our EEE School, namely the Micro Fabrication Laboratory (MFL) allow the practical realization of devices as those described in this thesis. However, it should be remembered that experimentation in a fabrication line is very expensive and time consuming. Technology Computer Aided Design (TCAD) and Design of Experiments (DOE) can be integrated to develop and optimize the fabrication process for the JFET-based color sensors. Figure 4.10 illustrates how this has been implemented successfully by using commercially available software tools which can provide the best approach to integrate factory simulation.

The use of Technology Computer Aided Design (TCAD) has become widespread in the semiconductor manufacturing industry [67–69]. As an alternative to running physical splits on real silicon wafers, it can provide a faster and more cost effective method of evaluating semiconductor device performance after process changes. In this chapter, device simulation tools are employed to investigate the effect of manufacturing changes on JFET response.

Several common semiconductor-device modeling tools are now available in Nanyang Technological University. These tools are especially valuable to students in the School of Electrical and Electronic Engineering, as they allow users to perform a variety of computer simulations, ranging from device processing to device and circuit performance.

The following software's programs were used:

TSuprem-IV: for modeling of the processing of 1-D and 2-D structures on crystalline silicon. The input parameters are the process steps and device layout or cross-section and the output is the device structure.

Medici: for device modeling of 1-D and 2-D structures of single, poly- and amorphous-Si. The inputs are the device structure and voltages, and the output consists

4.2.2. TCAD methodology: Simulator limitations

According to the chart in figure 4.10 the first step in simulation was to design the processing sheet for a small device, a JFET with a drain-to-source length of 20 μm and an epi-layer (for the channel region) of 4 μm deep. The primary tools used were TSUPREM-IV and MEDICI.

TSUPREM-IV is a computer program for simulating the processing steps used in the manufacture of silicon integrated circuits and discrete devices. The types of processing steps modeled by the current version of the program include oxidation, ion implantation, and inert ambient drive-in of silicon, epitaxial growth, and low temperature deposition and etching of various materials. The process architecture of a JFET-based color sensor assumed is similar to current CMOS processes, employing shallow top gate junctions and deeper main source/ drain regions followed by metallization.

The second simulator tool used was MEDICI™ from Avant!. It is a 2-dimensional device simulator originally based on Stanford University's PISCES. MEDICI uses non-linear iteration methods to solve the partial differential equations governing the electrical behavior of semiconductors (Poisson's equation, the continuity equations, carrier energy balance equations, and the lattice heat equation) [70]. The simulator incorporates various mobility, recombination, band-gap, and tunneling models as well as an advanced application module for modeling optoelectronic devices.

These simulation tools, though powerful, are not without their limitations for the modeling of devices. Some of the issues encountered during this simulation work were:

Simulation mesh: Accurate device simulation requires that the simulation mesh is adequately specified. As the simulation time is proportional to the number of mesh points squared one does not usually want too many nodes. Unfortunately, an adequate node count is not easy to specify, being dependent on the device and the type of simulation. One methodology (the one adopted here) is to gradually increase the mesh resolution until the difference in the simulation results becomes negligible.

Simulation parameters: The simulation tool is merely solving a set of coupled equations. It is up to the user to provide meaningful coefficients for these equations. In particular (as has been discussed in Section 2.3) minority carrier lifetimes, depletion depth and diffusion lengths are very important for JFET operation. Unfortunately these parameters are dependent on variety of factors difficult to control or to predict accurately for an accurate simulation such as wafer contamination, defects introduced during processing and their evolution during/after subsequent annealing treatments applied.

These parameters are not easy to measure without fabricating special test structures. They are also liable to vary from an equipment set to another and indeed from batch to batch. Therefore, in this case the default parameters already build-in or specified by the simulation software's have been used. While this may not produce simulation results precisely matching reality, it still allows the investigation of the main process parameters affecting JFET performance, which is the main purpose of this investigation.

Optical modeling limitations: The MEDICI optical advanced application module has been used in this analysis. This module can be used to model photo-generation in the silicon caused by incident photons. While it does permit ray tracing of incident beams through the dielectric stack it does not model the constructive and destructive interference necessary to obtain the final antireflectant (AR) effect of such a multilayer stack. This can be due to large periodic fluctuations in quantum efficiency, especially for very short wavelengths, of up to ~ 450 nm. Therefore, the final structures of the JFET-based sensors included AR coatings that had been previously designed and optimized separately with another software (TFCalc). However, the MEDICI software used to analyze the device characteristics does model the wavelength dependence of photon absorption in silicon, which is the most important aspect of the simulation in this case.

4.2.3. TCAD methodology: Experimental procedure

Two different methods were used to define the device structure:

a) 1-D doping profiles: These were obtained for diverse devices. The structure was created inside the device simulator by reading the profiles into designated device regions. The lateral diffusion of the impurities was approximated by a Gaussian tail-off. Because of such an approximation, this method is less accurate in the lateral dimension compared with the real measurement. However, it allows the device dimensions to be defined inside the device simulator.

b) Analytical profiles: Doping levels can be fully defined analytically using the device simulator. This was a different approach used to create the photo-JFET structure and to optimization its performance, especially the spectral responses. This provides the greatest flexibility, as the designer has new complete freedom to alter the junction depths and doping levels of the device. While it is not as accurate as either method defined above, the capability of being able to alter the structure easily is a great aid to understanding the device dependencies on structure and process.

It is often assumed (sometimes incorrectly) that when measurements and simulations disagree, then the simulator must be wrong. In fact, there are errors and

uncertainties associated with both electrical and physical testing that cannot be avoided when measurements are made. Therefore, a trade-off has to be reached between CPU time (fine grid) and instability in current results (coarse grid) and this can be done by "calibrating" the input factors (adjusting model coefficients) to the output responses.

4.2.4. DOE simulations: results

In the first part of our experiment, just one of the process variables was deliberately changed in order to observe the effect the changes have on one or more response variables presented in Fig.4.1–4.8. In a subsequent stage of a (statistical) design of experiments (*DOE*) was used to intentionally change more process variables (or factors) in order to observe the effects of the changes of the combined factors on one or more response variables. Therefore, DOE is an efficient procedure for planning experiments so that the data obtained can be analyzed to yield valid and objective conclusions.

DOE begins with determining the objectives of an experiment and selecting the process factors for the study. An *Experimental Design* is the laying out of a detailed experimental plan in advance of doing the experiment. Well chosen experimental designs maximize the amount of "information" that can be obtained for a given amount of experimental effort.

The statistical theory underlying DOE generally begins with the concept of *process models* [77].

4.2.4.1. Process Models for DOE: Black box process model

It is common to begin with a process model of the 'black box' type, with several discrete or continuous input factors that can be controlled—that is, varied at will by the experimenter—and one or more measured output responses. The output responses are assumed continuous. Experimental data are used to derive an empirical (approximation) model linking the outputs and inputs. These empirical models generally contain first and second-order terms.

Often the experiment has to account for a number of uncontrolled factors that may be discrete, such as different machines or operators, and/or continuous such as ambient temperature or humidity. Figure 4.11 illustrates this situation.

4.2.4.2. Process Models for DOE: Linear fit model

The most common empirical models fit to the experimental data take either a linear form or quadratic form.

Fig. 4.11. Black Box' Process Model Schematic for a typical process

A linear model with two factors, X_1 and X_2 , can be written as

$$Y = \beta_0 + \beta_1 X_1 + \beta_2 X_2 + \beta_{12} X_1 X_2 + \varepsilon \quad (4.1)$$

where ε is the experimental error.

Here, Y is the response for given levels of the main effects X_1 and X_2 and the $X_1 X_2$ term is included to account for a possible interaction effect between X_1 and X_2 . The constant β_0 is the response of Y when both main effects are 0.

For a more complicated example, like in our situation, a linear model with four factors X_1, X_2, X_3, X_4 and one response, Y , would be (if all possible terms were included in the model):

$$\begin{aligned} Y = & \beta_0 + \beta_1 X_1 + \beta_2 X_2 + \beta_3 X_3 + \beta_4 X_4 + \beta_{12} X_1 X_2 + \beta_{13} X_1 X_3 + \\ & + \beta_{14} X_1 X_4 + \beta_{23} X_2 X_3 + \beta_{24} X_2 X_4 + \beta_{123} X_1 X_2 X_3 + \beta_{234} X_2 X_3 X_4 + \\ & + \beta_{341} X_3 X_4 X_1 + \beta_{412} X_4 X_1 X_2 + \beta_{1234} X_1 X_2 X_3 X_4 + \varepsilon \end{aligned} \quad (4.2)$$

The three terms with single " X 's" are the *main effects* terms. There are $k(k-1)/2 = 4*3/2 = 6$ *two-way interaction* terms and *four three-way* interaction term (which is often omitted, for simplicity) and one all interaction term plus ε experimental error. When the experimental data are analyzed, all the unknown " β " parameters are estimated and the

coefficients of the "X" terms are tested to see which ones are significantly different from 0.

4.2.4.2. Process Models for DOE: Quadratic fit model

A second-order (quadratic) model (typically used in *response surface* DOE's with suspected curvature) does not include the three-way interaction term but adds three more terms to the linear model, namely

$$\beta_{11}X_1^2 + \beta_{22}X_2^2 + \beta_{33}X_3^2 \quad (4.3)$$

Clearly, a full model could include many cross-product (or interaction) terms involving squared X's. However, in general these terms are not needed and most DOE software defaults to leaving them out of the model.

4.2.4.3. Key steps for DOE

Obtaining good results from a DOE involves these seven steps:

1. Set objectives: The objective for our experiment is that to obtain the best colour sensitivity for the proposed device.
2. Select process variables: Process variables include both *inputs* and *outputs* - i.e., *factors* and *responses*. The first part of our simulation provide us the input variables that should be: *factor A: N_D -channel doping, factor B: Z -the width of device, factor C: a -half channel width, factor D: L -the length of device and the out put variables(responses) : current intensity I_D , pinch-off intensity I_P , saturation current intensity I_{DSat} , saturation voltage V_{DSat}*
3. Select an experimental design: In this case there are more than 3 factors and it is desired to begin with a design as small as possible and (so-called "*Screening design*") to identify which factors and combination of effects are the most important. The most popular experimental designs are *two-level designs* for each factor. There are a number of good reasons why using only two levels is the most common choice amongst engineers: one reason is that it is ideal for screening designs, simple and economical. Additionally, it also gives most of the information required to go to a multilevel response surface experiment if one is needed. For our DOE various strategies that ensured an appropriate choice of runs have been used. Properly chosen fractional factorial designs for 2-level experiments have the desirable properties of being both *balanced* and *orthogonal* [78].

Taguchi employs design experiments using specially constructed tables, known as "Orthogonal Arrays (OA)", to treat the design process.

Table 4.1. L_9 - A 3^{4-2} Fractional Factorial Design 4 Factors at Two Levels (16 runs) [78]

Run	A	B	= X	C	D
1	-1	-1	x_1	-1	-1
2	+1	-1	x_2	-1	-1
3	-1	+1	x_3	-1	-1
4	+1	+1	x_4	-1	-1
5	-1	-1	x_1	+1	-1
6	+1	-1	x_2	+1	-1
7	-1	+1	x_3	+1	-1
8	+1	+1	x_4	+1	-1
9	-1	-1	x_1	-1	+1
10	+1	-1	x_2	-1	+1
11	-1	+1	x_3	-1	+1
12	+1	+1	x_4	-1	+1
13	-1	-1	x_1	+1	+1
14	+1	-1	x_2	+1	+1
15	-1	+1	x_3	+1	+1
16	+1	+1	x_4	+1	+1

4. Execute the design
5. Check that the data are consistent with the experimental assumptions.
6. Analyze and interpret the results. Calculations of result averages and averages for factor-level effects, which only involve simple arithmetic operations, produce answers to major questions that were unconfirmed in the earlier steps about the project. However, questions concerning the influence of factors on the variation of results—in terms of discrete proportion—can only be obtained by performing analysis of variance (ANOVA). The results are presented in figures 4.12–4.17 and will be discussed later. The analysis of variance (ANOVA) consists in calculating the mean (average) values for the results of the runs and for factor-level effects. The obtained information provides useful data to major questions that were unanswered in the earlier steps of the project. However, the answer to questions concerning the influence of factors on the variation of results—in terms of discrete proportion—can only be obtained by performing

the analysis of variance. Calculate the cumulative probability of each residual using the formula: $P(j\text{-th residual}) = j/(N+1)$ with P denoting the cumulative probability of a point, j is the order of the value in the list and N is the number of entries in the list.

Fig. 4.12. The estimation of I_D function of factors A, B, C, D and their interaction

Fig. 4.13. The estimation of V_{DSat} function of factors A, B, C, D and their interaction

Fig. 4.14. The estimation of I_{Dsat} function of factors A, B, C, D and their interaction

Fig. 4.15. The estimation of I_P function of factors A, B, C, D and their interaction

Fig. 4.16. The estimation of V_P function of factors A, B, C, D and their interaction

The four factors, and their corresponding assigned values used in our DOE are:

- Factor A: $N_D - 1 \cdot 10^{-14} \text{ cm}^{-3}$ and $5 \cdot 10^{-15} \text{ cm}^{-3}$;
- Factor B: $Z - 2 \text{ } \mu\text{m}$ and $10 \text{ } \mu\text{m}$,
- Factor C: $a - 1 \text{ } \mu\text{m}$ and $3 \text{ } \mu\text{m}$,
- Factor D: $L - 2 \text{ } \mu\text{m}$ and $10 \text{ } \mu\text{m}$.

Interaction among factors, which is the response due to one factor's effect on another factor, is quite common in industrial experiments. Although interactions among several factors, and between factors at three or four levels, are also present, we will study interaction between factors for only two-levels.

7. Results: All the figures present the least squares estimation of factors that is equal with the difference of means for each factor and their interaction using the cumulative model. The following conclusions can be drawn from the plots for the output results V_P , V_{DSat} , and I_D shown in Fig. 4.16, 4.13 and 4.12, respectively, that there is a clear dividing line between the influence of two factors A and C and their interactions AC (all estimations $> 80 \%$) and that of the other two factors, B and D, and interactions AB,

$AD, BD, BC, CD, ABC, ABD, ACD, BCD$ and $ABCD$ (all | estimations | < 80 %). As a rule, this suggests that only the first terms A, C and AC should be retained as “important” and discards the remaining ones as “unimportant”. However, one exception will be made because the estimation percentage is high (80 %) ” the factors B and AB will also be retain in the “important part (with | estimations | > 50 %). The plots for the output results I_P and I_{DSat} in Fig. 4.15 and 4.14 shows a split in four “blocks” but the clear division between “important” and “unimportant” factors can be observed to occur for the same factors mentioned previously.

4.2.4.4. Conclusions

The primary goal of this experiment was to identify the most important factors in maximizing the best colour sensitivity for the proposed device.

The various preceding graphics plots and estimations analysis showed that the channel doping N_D and the half-channel depth “ a ” were the most important factors. This will be the foundation for the design of several versions of devices corresponding to a sequence of small experiments that will give us more useful results.

4.2.5. TSuprem IV simulations: results

From the results of the previous simulation it was deduced that the variation of the channel doping N_D and the channel depth “ a ” are the key parameters whose variation would affect most the behavior of the device. Practically, the channel doping N_D can be modified during the device fabrication while different geometrical dimensions can be assigned to a variety of version of JFET devices. The basic and most fundamental JFET-based color sensor and all the variations derived from it are presented in the next sub-sections with results of TSuprem-IV simulation that provided the concentration profiles for all the region of interest: top-gate, bottom gate, source and drain.

4.2.5.1. DEVICE 02

DEVICE02, presented in Fig. 4.17, is the basic JFET with a normal top gate, bottom gate, source and drain. Because the concentration profiles for source S and drain D are identical for almost all the devices with the exception of DEVICE08 we will present only once their concentration profile in Fig. 4.18. The doping concentration profiles for the top-gate are shown in Fig. 4.19 and it can be easily seen that its value is high in order to improve the breakdown of top-gate-to-channel junction.

Fig. 4.17. The structure of Device02 with detailed values for concentration and type of layers for each of the four terminals: TG, BG, S & D.

Fig. 4.18. The doping concentration profile for the Source S (drain D) with detailed values for the junction depth and doping concentration for epi-layers.

Fig. 4.19. The doping concentration profile for the top-gate *TG* for *DEVICE02* with detailed values for the junction depth and doping concentration for epi-layers.

Fig. 4.20. The structure of *Device03* with detailed values for concentration and type of layers for each of the four terminals: *TG*, *BG*, *S* & *D*.

Fig. 4.21. The doping concentration profile for the contact top-gate TG for *DEVICE03* with detailed values for the junction depth and doping concentration for epi-layers.

Fig. 4.22. The doping concentration profile for the top-gate TG for *DEVICE03* with detailed values for the junction depth and doping concentration for epi-layers.

4.2.5.2. *DEVICE 03*

DEVICE03, presented in Fig. 4.20, is an enhancement of the basic JFET with a top gate improved with two guard rings that will further increase the protection of the top junction against breakdown. As a result, the doping concentration of the top-gate region can be reduce and also the top-gate junction can be more shallow, in order to increase the collection of carriers photogenerated by the shortest wavelengths as was theoretically shown by the Matlab simulation as in Fig. 2.19. The doping concentration profiles for the ring and top-gate are shown in Fig. 4.21 and Fig. 4.22, respectively.

4.2.5.3. *DEVICE 04*

DEVICE04 presented in Fig. 4.23, is a modification of the basic JFET with a top gate under a N-well. This N-well was introduced with the same intention of increasing the collection of carriers photogenerated by the shortest wavelengths by increasing the depletion region width for the N-well-top-gate junction. The doping concentration profiles for this device are shown in Fig. 4.24.

4.2.5.4. *DEVICE 05*

DEVICE05 presented in Fig. 4.25 is a JFET with two top gates. Each top gate consist of two regions: highly doped and deeper region acting both as contact region and breakdown protective ring, and a low doped but very shallow region for the collection of carriers photogenerated by the shortest wavelengths. The doping concentration profiles for device with two the top gates are shown in Fig. 4.26 and Fig. 4.27.

The main reasons that this will be is an ideal color sensors are:

- It has two gates at two different depths;
- The low value of space-charge region width at surface will increase the collection of carriers photogenerated by the shortest wavelengths;
- More precise control over depletion region width through the two gates will accomplish accurate color detection.

4.2.5.5. *DEVICE 08*

DEVICE08, presented in Fig. 4.28, is derived from DEVICE02 by replacing one of the *n*-type contacts of Source/Drain with the *p*-type one. This should improve the collection of carriers photogenerated in the channel by middle-range wavelengths (green), by Source and Drain. The doping concentration profiles for this device are shown in Fig. 4.29 and Fig. 4.30.

Fig. 4.23. The structure of Device04 with detailed values for concentration and type of layers for each of the five terminals: TG, N-Well, BG, S & D.

Fig. 4.24. The doping concentration profile for the N-Well-top-gate TG for DEVICE03 with detailed values for the junction depth and doping concentration for epi-layers.

Fig. 4.25. The structure of Device05 with detailed values for concentration and type of layers for each of the five terminals: TG1, TG2, BG, S & D.

Fig. 4.26. The doping concentration profile for the top-gate TG1 for DEVICE05 with detailed values for the junction depth and doping concentration for epi-layers.

Fig. 4.27. The doping concentration profile for the top-gate *TG2* for *DEVICE05* with detailed values for the junction depth and doping concentration for epi-layers.

Fig. 4.28. The structure of *Device08* with detailed values for concentration and type of layers for each of the five terminals: *TG1*, *BG*, *S* & *D*.

Fig. 4.29. The doping concentration profile for the drain D for *DEVICE08* with detailed values for the junction depth and doping concentration.

Fig. 4.30. The doping concentration profile for the Source S for *DEVICE08* with detailed values for the junction depth and doping concentration.

4.2.7. Antireflection coating design

The next step after establishing the geometrical parameters of our device is to maximize the optical properties of the device by covering its surface with an antireflection coating. The theoretical considerations and the simulation results related to this aspect are detailed in the next two sub-sections.

4.2.7.1. Antireflection theoretical consideration

An optical coating consist of one or more thin layers placed on a surface of a material (substrate) which alters the way in which this substrate reflects and transmits light. One type of optical coating is an antireflection coating, which reduces unwanted reflections from surfaces, and in the beginning was commonly used on spectacles and photographic lenses.

Whenever a ray of light moves from one medium to another some portion of the light is reflected from the surface (known as the interface) between the two media. The strength of the reflection depends on the refractive indices of the two media as well as the angle of the surface to the beam of light. The exact value can be calculated using the Fresnel equations. [79]

When the light meets the interface at normal incidence (i.e. perpendicularly to the surface), the intensity of reflected light is given by the reflection coefficient or reflectance, R :

$$R = \frac{(n_0 - n_s)^2 + k^2}{(n_0 + n_s)^2 + k^2} \quad (4.4)$$

where n_0 and n_s are the refractive indices of the first and second media, respectively. The value of R varies from 0.0 (no reflection) to 1.0 (all light reflected) and is usually quoted as a percentage. Complementary to R is the transmission coefficient or transmittance, T . If the effects of absorption and scattering are neglected, then the value T is always $1-R$. Thus if a beam of light with intensity I is incident on the surface, a beam of intensity RI is reflected, and a beam with intensity TI is transmitted into the medium.

The simplest form of antireflection (AR) coating was observed by Lord Rayleigh in 1886. He found that old, slightly tarnished pieces of glass transmitted more light than new, clean pieces. This effect, presented in Fig. 4.31, can be explained by envisioning a thin layer of material with refractive index n_l between the air (index n_0) and the substrate (index n_s). The light ray now reflects twice, once from the surface between air and the thin layer, and once from the layer-to-substrate interface.

Fig. 4.31. Reflection and transmission of an uncoated and coated surface

Fig. 4.32. Interference in a quarter-wave antireflection coating for a single layer and for a stack composed of 3 layers

From the equation (4.4), and the known refractive indices, reflectivities for both interfaces can be calculated, and denoted R_{01} and R_{1S} , respectively. The transmission at each interface is therefore $T_{01} = 1 - R_{01}$ and $T_{1S} = 1 - R_{1S}$. The total transmittance into the glass is thus $T_{1S}T_{01}$. Calculating this value for various values of n_1 , it can be found that at one particular value of optimum refractive index of the layer, the transmittance of both

interfaces is equal, and this corresponds to the maximum total transmittance into the glass.

This optimum value is given by the geometric mean of the two surrounding indices:

$$n_i = \sqrt{n_0 n_s} \quad (4.5)$$

The use of an intermediate layer to form an AR coating can be thought of as analogous to the technique of impedance matching of electrical signals. Further reduced reflection could in theory be made by extending the process to several layers, gradually varying the refractive index of each layer between the index of the air and the index of the substrate.

Practical AR coatings, however, rely on an intermediate layer not only for its direct reduction of the reflection coefficient, but also use interference in the layer. Assume the layer thickness is controlled precisely such that it is exactly one-quarter of the wavelength of the light deep ($\lambda/4$), forming a quarter-wave coating (Fig. 4.32). If this is the case, the incident beam I , when reflected from the second interface will travel exactly half its own wavelength further than the beam reflected from the first surface. If the intensities of the two beams, R_1 and R_2 , are exactly equal, then since they are exactly out of phase, they will destructively interfere and cancel each other. Therefore, there is no reflection from the surface, and all the energy of the beam must be in the transmitted ray, T .

Further reduction is possible by using multiple coating layers, designed such that reflections from the surfaces undergo maximum destructive interference or, like the triple stack in Fig. 4.32, that all reflections are in phase and only a certain wavelength is transmitted.

4.2.7.2. Antireflection simulation

The software used for designing and modeling of optical thin film coatings was TFCalc thin film design software developed by Software Spectra. The software was selected because of its advantageous features easy to use and availability.

TFCalc's most important quality for this project is its capability to perform optimization of a certain coating for a desired wavelength. Optimization is the primary method—but not the only method—by which multi-layer coatings are designed. It works by adjusting the thickness and/or the refractive index of layers so that the coating's performance (reflectance, transmittance, color, etc.) is close to the desired performance (also called the optimization targets)

The difference between the coating's performance and the desired performance is computed in the merit function:

$$F = \left(\frac{1}{m} \sum_{j=1}^m \left| \frac{P_j^D - P_j}{N_j * Tol_j} \right|^k \right)^{1/k} \quad (4.6)$$

where m is the number of optimization targets, P_j is the computed performance of the design, P_D is the desired performance, and $N_j * Tol_j$ is a weighting factor for each target. F is the quantity that the optimization process seeks to minimize. Note that if $F = 0$, then the coating's performance is the same as the desired performance. However, in most cases, it is not possible to find a design such that $F = 0$. Instead, there are methods that attempt to make F as small as possible.

In our design, TFCalc was used to optimize the transmittance of the AR coating for the visible part of the light spectrum (300-800 nm) using no more than three layers in order to keep the fabrication process simple. Furthermore, only Si-compatible materials should be used in this design, such as silicon oxide SiO_2 , LPCVD silicon nitride Si_3N_4 and low stress nitride. The results obtained from TFCalc optimization are presented in Fig.4.33–4.35, while the composition of the stack is given in Table 4.1–4.3 for single, double and triple layers, respectively.

However, unlike the classical case for which $R = 0$ at a single design wavelength (and for which the optical thickness of the layer is $\frac{\lambda}{4}$) our aim here is to achieve $R \cong 0$ on a bandwidth as large as possible.

$$n \cdot d = \frac{\lambda}{4} \Rightarrow d = \frac{\lambda}{4n} \quad (4.7)$$

For example, for silicon nitride $n=2$, then for a wavelength of 400 nm the thickness of the layer will be easy calculated as:

$$d = \frac{\lambda}{4n} = \frac{400}{4 \cdot 2} = 50\text{nm} \quad (4.8)$$

As it can be noticed from the Fig. 4.33 and 4.34, the optimization of the same stack of layers for different wavelength produces different results in transmission and interference. Therefore if our purpose is to enhance the blue wavelength collection we cannot risk decreasing the transmission for the all other wavelength from the visible spectrum. From the same graphs we can see the best results are:

- a) For the single layer of 38.87 nm of SiN where the transmission is higher than 75 % for all wavelengths in the visible spectrum

- b) The stack of layers composed by 10 nm SiO₂ + 20 nm SiN + 85 nm SiO₂ where the transmission is higher than 70 % for all wavelengths in the visible spectrum.

Fig. 4.33. Transmission through AR coating for a single layer

Table 4.1. The composition of single AR coating and the optimization for a certain wavelength

Code	Layer		Zero reflectance wavelength [nm]
	Thickness [nm]	Material	
AR1A	28	SiN	400
AR1B	20	SiN	400
AR1C	38.87	SiN	400

Fig. 4.34. Transmission of a two layer AR coating

Table 4.2. The composition of a two layer AR coating and the optimization for a certain wavelength

Code	Layer no.1		Layer no.2		Optimization for the wavelength [nm]
	Thickness [nm]	Material	Thickness [nm]	Material	
AR2A	10	SiO ₂	20	SiN	400
AR2B	10	SiO ₂	20	SiN	550
AR2C	11.02	SiO ₂	22.08	SiN	550
AR2D	10	SiO ₂	28	SiN	550
AR2D300	5.35	SiO ₂	14.41	SiN	400
AR2E	15	SiO ₂	20	SiN	400
AR2F	20	SiO ₂	28	SiN	400

Fig. 4.35. Transmission of a three layer AR coating

Table 4.3. The composition of a three layer AR coating and the optimization for a certain wavelength

Code	Layer no.1		Layer no.2		Layer no.3		Optimization for the wavelength [nm]
	Thickness [nm]	Material	Thickness [nm]	Material	Thickness [nm]	Material	
AR3A	10	SiO ₂	20	SiN	85	SiO ₂	400
AR3B	10	SiO ₂	28	SiN	100	SiO ₂	400
AR3C	30	SiO ₂	28	SiN	400	SiO ₂	400
AR3D	20	SiO ₂	28	SiN	200	SiO ₂	400
AR3A 550	10	SiO ₂	28	SiN	100	SiO ₂	550

4.3. Standard JFET results and experiments

4.3.1. Process simulator MEDICI

Device simulation is the best established discipline within the semiconductor simulation domain due to early emphasis: starting with famous work of Gummel in 1964 the first simulation including all three spatial dimensions is published already in 1980 by Buturula et.al. [76] MEDICI provides a way for device engineers to analyze, design, and optimize semiconductor devices before manufacturing them. It numerically solves the partial differential equations governing the electrical behavior of semiconductors device (Poisson's equation, the continuity equations, carrier energy balance equations, and the lattice heat equation) using non-linear iteration methods.

The equations are discretized in 1D, 2D, or 3D space on a non-uniform grid. Finite element and finite difference methods are used to obtain a set of non-linear equations and an iterative solution method is applied until a self-consistent solution is found. Models are used to represent physical characteristics of the material (mobility, recombination rates, and dielectric constants) at each point. [70] As the structures and models used for contemporary 2D device simulation become more complex, the challenges placed on mesh generation become more demanding.

Since the JFET based color sensor fabricated in TSUPREM-IV is imported into MEDICI, the simulation mesh (grid) and the structure information (doping profiles, materials and etc.) of TSUPREM-4 will be used. The accurate simulation of complex device geometry along with advanced device models demands localized areas of high mesh density. To ensure rapid convergence of complex device models, high-quality mesh elements are required in areas with large electric fields and high current density. At the same time, the number of mesh nodes must be minimized to increase throughput. In addition, the transfer of device structures from process to device simulation should be facilitated by a convenient, automatic and robust set of mesh generation tools.

4.3.2. Principal case

This section emphasizes the basic aspects of the behavior of a JFET in order to obtain its static model. Fig. 4.36 shows in cross section the basic structure of the basic JFET device for color-sensing from which various other subsequent versions have been

derived. The S/D n^+ regions are not visible in Fig. 4.36 because MEDICI does not allow highlighting regions of similar doping type that differ only in doping concentration.

Fig. 4.36. Cross sectional view of the device simulation model of an n - channel JFET: a) 3D doping profile of the initial grid for device 5, b) 2D view after regrid for device 5, highlighting built-in depletion region, c) 3D doping profile of the initial grid for device 3, d) 2D view after regrid for device 3.

We should emphasize that successful device simulation requires reliable results of technology process simulation, especially the critical influences of the doping profile. And doping profile is altered with each process step and this must necessarily change the mesh structure as well. The processing steps that change the grid are deposition, epitaxy, etching, photoresist development, oxidation, and silicidation. In addition, if adaptive gridding is enabled, the grid may be modified during ion implantation and diffusion. Therefore bring a lot of uncertainties in doping profiles that can lead to unsuitable

electrical characterizations or at least inaccurate results which cannot be used for device or process simulation.

4.3.3. Effect of epitaxial layer

The most important essential component for the performance of our device is the channel characterized by depth and doping concentration. In our process, the manufacture of the channel is based on epitaxial deposition so it necessary to detail the influence of epitaxial layer on the operation of the JFET-based structures.

During a semiconductor manufacturing process it is relatively easy to alter certain fabrication parameters in order to modify the structure of the final device. In particular, for the studied family of the JFET-based devices, the epitaxial layer thickness can be varied — wafer suppliers offer a range of substrates and also the NTU MicroFabrication Laboratory has the facility for growing epitaxial layers. If an epitaxial layer is grown on a heavily doped substrate the presence of this region of high doping can affect the device in two ways:

1. Lifetime: The lifetime of minority carriers in this heavily doped region will be much shorter than in the epilayer, and therefore carriers generated in this region are unlikely to be collected by the bottom gate of JFET.

2. Potential barrier: If the heavily doped region is p -type, a potential barrier will result at the substrate-epi junction, which will prevent minority carriers in the epi-layer moving downwards. This increases significantly the chance of the photogenerated carriers to be collected in the channel and would therefore enhance the spectral response in the long wavelength (red) range of the visible spectrum.

A variety of substrate doping levels and epi thickness were simulated and, as expected, it was found that the greatest effect on the current response occurred with the thinnest epi and the heaviest channel doping.

For this reason, the following discussion will focus on an optimized device with an n -epi region of $4\text{ }\mu\text{m}$ thick and a doping of 10^{16} cm^{-3} , grown on a p^{++} substrate with a doping of $2\cdot 10^{18}\text{ cm}^{-3}$, for the bottom gate and a thin top-gate region $0.5\mu\text{m}$ deep and a doping of $5\cdot 10^{16}\text{ cm}^{-3}$. The top gate region also has two p^+ rings at its lateral ends to improve the breakdown voltage. Figure 4.36 shows the 3D representation of the doping profiles for all the regions of this device

The spectral photo-response of the JFET sensor with a p^{++} substrate is improved over the visible spectrum due to the potential barrier caused by the junction between the n -epi region and the heavily doped p^{++} substrate as explained above. This is an important

result as it suggests that thinning the epi-layer may improve the quantum efficiency. Detailed calculation and optimizations based on the previously presented equations (3.27)–(3.30) demonstrated that the best results are obtained when the n -epi region of the JFET has a total thickness of 2 μm epi.

Fig. 4.37. 3D plot of doping profile of JFET with 2 μm epi-layer

Another important aspect that has to be considered is to examine the magnitude of “short channel effect” in the device with the previously chosen optimal n -epi thickness and doping levels, i.e. to check the presence and extent of the regions where the electric field is strong enough to drive the carriers into velocity saturation ($\mathcal{E} > \mathcal{E}_c$). Analyzing the short-channel JFET is more complex simply because the x component of the electric field in the channel is not small compared to the y component. The x direction is defined as extending from the edge of the source region horizontally into the drain region whereas the y direction is defined from the surface of top gate extending vertically downwards into the bottom gate and the quasi-two-dimensional gradual approximation used in modeling long channel device no longer suffices. Because a large y -direction electric field is required to sustain the top and bottom gate depletion regions, the shift in electric field in the channel from the y direction toward the x direction removes the necessary condition for forming the depletion regions. This leads to a unique phenomenon in the short-channel JFET in which the channel remains open (no channel pinch-off) even under a bias condition that will cause channel pinch-off in long channel JFET. This, however, is not equivalent with saying that the channel pinch-off can never occur in a short channel

JFET. It is possible to have a pinch-off in a short-channel JFET as well if both the gate and the drain voltages are relatively large. The simulated I - V characteristics of a short and long channel JFET's are given in figures 4.38 and 4.39, respectively.

Fig. 4.38. I_{DS} - V_{DS} characteristics of a short channel JFET for a device (D3) with the following geometrical parameters:
Channel with $N_D = 10^{16} \text{ cm}^{-3}$, $Z = 4 \text{ μm}$; $a = 4 \text{ μm}$; $L = 12 \text{ μm}$, Top Gate with $x_{TG} = 0.3 \text{ μm}$, $N_{TG} = 4.5 \cdot 10^{16} \text{ cm}^{-3}$, Source and drain $N_A = 10^{18} \text{ cm}^{-3}$,

Fig. 4.39. I_{DS} - V_{DS} characteristics of long channel JFET for a device (D3) with the following geometrical parameters:
Channel with $N_D = 10^{16} \text{ cm}^{-3}$, $Z = 4 \text{ μm}$; $a = 4 \text{ μm}$; $L = 85 \text{ μm}$, Top Gate with $x_{TG} = 0.3 \text{ μm}$, $N_{TG} = 4.5 \cdot 10^{16} \text{ cm}^{-3}$, Source and drain $N_A = 10^{18} \text{ cm}^{-3}$.

The preceding results are important for the desired application of such a structure (as a color sensor) as they constitute the first step toward analyzing and discussion the different regimes that can appear during the operation of the long channel JFET. In the following subsequent analysis a JFET with a n -channel with a doping level of 10^{16} cm^{-3} and $25 \mu\text{m}$ long, with a sub-micron-gate $0.08 \mu\text{m}$ deep and a 3D-doping profile shown in Fig. 4.37 will be considered.

a) Linear region (before channel pinch-off)

The bias conditions considered here are such that the two depletion regions developed by the top gate (TG) and bottom gate (BG) regions, respectively, in the conducting channel do not touch each other. Fig. 4.40 shows the simulated depletion region edges (dotted lines), the top and bottom p/n metallurgical junctions (dashed lines) and the electric field vectors (arrows) for various V_{GS} and V_{DS} . Note that the source and the drain regions are located at the far right and the far left ends of the structure, respectively.

Fig. 4.40. Electric field vectors (arrows) and the edge of the depletion regions of the long channel JFET biased in the linear region.

Fig. 4.41. The electron current vectors in the long channel JFET in the linear region

In the JFET, the electron flows predominantly along the x direction and is confined in the n -type channel sandwiched between the two depletion regions (Fig. 4.41). It should be mentioned that the MEDICI defines the depletion edges as the boundary where the majority-carrier concentration equals half of the net impurity concentration and it is important to point out that the shape of the channel is strongly influenced by and subject to this definition.

b) Saturation region (beyond channel pinch-off)

In this operational region the drain voltage increase further until it equalizes the pinch-off voltage that characterizes the onset point separating the linear and saturation regions. Consequently, the increase in the drain current is a result of the decrease in the effective channel length. This is evident in Fig. 4.42, which shows two plots depicting the shape of the conducting channel and the current flow through the device for the two different V_{DS} voltages.

The three-dimensional electron concentration for the linear, pinch-off and saturation regions are plotted in Fig. 4.43.

Fig. 4.42. The flow diagram illustrating the change of the channel shape and the channel pinch-off for a n -channel JFET.

Top: for $V_D = 13$ V, Bottom: for $V_D = 20$ V

Left: the edges of the depleted regions Right: Vectors representing the current through device. For all the cases: $V_{TG} = V_{BG} = V_S = 0$ V

Fig. 4.43. 3D-Total current density in device in the same bias conditions as those Fig. 4.42 for three different operational regimes: a) linear ($V_D = 0$ V), b) At pinch off ($V_D = 13$ V) and c) At saturation ($V_D = 25$ V).

c) Cutoff region

Consider now another sequence of bias conditions, in which the drain voltage is hold constant and the reverse bias of the gate voltage is gradually increased. For zero drain voltage, increasing the gate voltage will increase the extensions of the depletion regions uniformly throughout the channel. Thus, for a long channel JFET, it will take a smaller drain voltage to pinch-off the channel near the drain end if the gate voltage is larger. The entire channel region can be pinched-off (channel cut-off) if the gate voltage is sufficiently larger. In such a case, the electron current in the channel vanishes and the device is turned off. The results of simulations are given in Fig. 4.44 and 4.45, respectively.

Fig. 4.44. Electric field vectors (red arrows) and the current density flow vectors (right down-blue arrows) in an n-channel JFET. The change in the channel shape as the reverse bias for the gates is increased until channel cutoff is pictured with red dotted line.

Fig. 4.45. 3D–Total current density in device in the same bias conditions as those pictured in Fig. 4.44 for three different stages in the cut–off sequence: for all $V_D = 2$ V a) linear ($V_{TG} = V_{BG} = -1$ V), b) At pinch off ($V_{TG} = V_{BG} = -8$ V) and c) At cut–off ($V_{TG} = V_{BG} = -10$ V).

4.3.4. TSuprem IV–process development

Fig. 4.46 shows the final process flow for all the devices. It can be easily seen that since we had a single process for all the devices the major difference consists mainly in the parameters chosen for the ionic implantation and drive–in annealing. In order to ensure the variety considered in our DOE (section 4.2), the related parameters, like dopant dose, energy drive–in temperature and drive–in time will be adjusted for each wafer while they are fabricated using the available facilities of our existing 2 μm CMOS process.

Therefore, the process should be evaluated from the following standpoints:

1. The thermal budget should be minimized as much as possible. Thus, the drive –in processes for the diffusion of p^+ and n^+ contacting regions have been carried out at the minimum temperature in order to activate dopants and to restore the original crystal lattice, and before the implantation of shallow p region.
2. Antireflecting coating and metal light shields are necessary to be added in the „illuminated“ area and „dark“ area, respectively. These measures will improve the efficiency of light absorption and prevent any parasitic photogeneration due to stray light or illumination of undesired chip areas.

The corresponding TSuprem–IV simulation results were presented in the former section providing the doping profile and cross–sectional view for each device. The fabrication process will be detailed in the section 5.2 based on Fig. 4.46.

Process Legend

p ⁺ -type Silicon	n-type Silicon
p-type Silicon	n ⁺ -type Silicon
p ⁺⁺ -type Silicon	Photoresist
Thermal growth dioxide of silicon	Silicon nitride
Pad	Aluminum

For all devices

1. Start wafer: p-type $N_A = 4 \times 10^{13} \text{ cm}^{-3}$; width of device = 80
2. Epitaxy Thickness = 3 μm time = 5 min
Temp = 1080 °C $N_A = 2 \times 10^{13} \text{ cm}^{-3}$
3. Epitaxy Phosphorus Thickness = 5 μm
time = 10 min Temp = 1080 °C
 $N_D = 5 \times 10^{13} \text{ cm}^{-3}$

2

For all devices

Operation 4. Grow of sacrificial oxide
wet2 time=5 min. temp = 950 °C
 $x_{\text{ox}} = 300 \text{ \AA}$

Operation 5. Grow of sacrificial nitride
deposit nitride thick=0.13 μm ;

Fig. 4.46. Fabrication process of all JFET-based color sensor

Operation 6. n+ - implant S & D

Mask = **SDCON(jetstrM1 - NOIF)**

Open implant windows in nitride only

P dose = $3 \times 10^{13} \text{ cm}^{-2}$ E=110 keV/tilt=7° Rp = 0.1381 μm ; ΔRp = 0.0671 μm

Strip PR

For devices 3,4 & 5

For devices 8

Operation 7. Oxidation

Diffusion = eto2 time=30 min Temp=850 °C

Strip nitride

For devices 3,4 & 5

For devices 8

Operation 8. P+ - implant S

Mask = **DCON(jetstrM2 - OPL2)**

B dose = $5 \times 10^{14} \text{ cm}^{-2}$ E=30 keV/tilt=7° Rp = 0.1381 μm ; ΔRp = 0.0671 μm

Strip PR

For device 8

For device 2(LD)

6

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 9. n+ (p+) drive-in

N_2 time = 60 min Temp = 1000 °C

$x_{ox} = 300 \text{ \AA}$ – it is the same oxide because we will keep it until the end of the process.

**For devices
3, 4 & 5**

Operation 9. n+ (p+) drive-in

N_2 time = 60 min Temp = 1000 °C

$x_{ox} = 300 \text{ \AA}$ – it is the same oxide because we will keep it until the end of the process.

For device 8

For device 2(LD)

Operation 10. Implant of p – channel in LD

Mask: PCHANNEL (jfetstrM3 – DEPLT)

BORON dose = $5 \times 10^{19} \text{ cm}^{-2}$ E = 15 keV/tilt=7 $R_p = 0.0655 \mu\text{m}$; $\Delta R_p = 0.0337 \mu\text{m}$

Strip PR

For device 2(LD)

9

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 11. n+(p+) drive-in
 N_2 time = 60 min Temp = 1000 °C

$x_{ox} = 300 \text{ \AA}$ – it is the same oxide because we will keep it until the end of the process.

**For devices
 3, 4 & 5**

Operation 11. n+(p+) drive-in
 N_2 time = 60 min Temp = 1000 °C

$x_{ox} = 300 \text{ \AA}$ – it is the same oxide because we will keep it until the end of the process.

For device 8

For device 2(LD)

Operation 12. TG2 implant
 Mask : TGDEP(jfetstrM4 – PDIFF)

BORON dose = $5 * 10^{18} \text{ cm}^{-2}$ E=15 keV tilt=7° $R_p = 0.0655 \text{ μm}$; $\Delta R_p = 0.0337 \text{ μm}$ Strip PR

For device 3

For device 4

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 12. TG2 implant

Mask : **TGDEP(jetstrM4 - PDIFF)**

BORON dose = $5 \times 10^{12} \text{ cm}^{-2}$ E=15 keV tilt=7 Rp = 0.0655 μm ; ΔRp = 0.0337 μm Strip PR

For device 8

For device 5

Operation 13. Annealing N2 time=30 min. Temp = 900 °C

For device 3

For device 4

Operation 13. Annealing N2 time=30 min. Temp = 900 °C

For device 8

For device 5

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 14. n+ - implant pt Nwell

Mask = NWELL (fetstrM5 - NWELL)

P dose = $3 \times 10^{15} \text{ cm}^{-2}$ E=110 keV/tilt=7 Rp = 0.1381 μm ; ΔRp = 0.0671 μm Strip PR

For device 2(LD)

For device 4

Operation 15. Annealing N₂ time=30 min. Temp = 900 °C

For device 2(LD)

For device 4

Operation 16. n+ - implant pt Nwell

deposit nitride thick=0.13 μm ;

Mask = NWELLC (fetstrM6 - OCNT)

Open implant windows in nitride only

As dose = $3 \times 10^{15} \text{ cm}^{-2}$ E=20 keV/tilt=7 Rp = 0.1381 μm ; ΔRp = 0.0671 μm

For device 2(LD)

For device 4

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 16. n+ - implant pt Nwell
deposit nitride thick=0.13 μm ;
Mask = **NWELLC (jetstrM6 - OCNT)**
Open implant windows in nitride only
As dose = $3 \times 10^{13} \text{ cm}^{-2}$ E=20 keV/tilt=7 $R_p = 0.1381 \mu\text{m}$;
 $\Delta R_p = 0.0671 \mu\text{m}$

For device 8

For device 3

Operation 16. n+ - implant pt Nwell
deposit nitride thick=0.13 μm ;
Mask = **NWELLC (jetstrM6 - OCNT)**
Open implant windows in nitride only
As dose = $3 \times 10^{13} \text{ cm}^{-2}$ E=20 keV/tilt=7 $R_p = 0.1381 \mu\text{m}$;
 $\Delta R_p = 0.0671 \mu\text{m}$

For device 5

Operation 17. Oxidation
Strip nitride
Diffusion weto2 time=30 min Temp=850 $^{\circ}\text{C}$

For device 2(LD)

For device 4

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 17. Oxidation

Strip nitride

Diffusion weto2 time=30 min Temp=850 °C

For device 8

For device 3

Operation 17. Oxidation

Strip nitride

Diffusion weto2 time=30 min Temp=850 °C

For device 5

Operation 18. Implant of p+ contact region for Top Gates

Mask: TGCON(jetstrM7 - OPL1)

BF₃ dose = $5.5 \times 10^{14} \text{ cm}^{-2}$ E=25 keV/tilt=7 Rp = 0.0219 μm; ΔRp = 0.0099 μm Strip PR

For device 2(LD)

For device 4

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 18. Implant of p+ contact region for Top Gates
 Mask: TGCON(jetstrM7 - OPL1)
 BF_2 dose = $5.5 \times 10^{14} \text{ cm}^{-2}$ $E=25 \text{ keV/slt}=7$ $R_p = 0.0219 \mu\text{m}$;
 $\Delta R_p = 0.0099 \mu\text{m}$ Strip PR

For device 8

For device 3

Operation 18. Implant of p+ contact region for Top Gates
 Mask: TGCON(jetstrM7 - OPL1)
 BF_2 dose = $5.5 \times 10^{14} \text{ cm}^{-2}$ $E=25 \text{ keV/slt}=7$ $R_p = 0.0219 \mu\text{m}$;
 $\Delta R_p = 0.0099 \mu\text{m}$ Strip PR

For device 5

Operation 19. ANNEALING
 N_2 time=30 min Temp=850 °C

For device 2(LD)

For device 4

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 19. ANNEALING
 N_2 time=30 min Temp=850 °C

For device 8

For device 3

Operation 19. ANNEALING
 N_2 time=30 min Temp=850 °C

For device 5

Operation 20. Implant of Top Gates
 Mask: TGDEP (JetstrM8 - PWELL)
 BF_2 dose = $2.5 \times 10^{12} \text{ cm}^{-2}$ E=48 keV/tilt=7 $R_p = 0.0219 \mu\text{m}$; $\Delta R_p = 0.0099 \mu\text{m}$ Strip PR

For device 5

For device 3

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 21. ANNEALING N_2 time=30 min Temp=850 °C
Stripe oxide (All devices)

For device 5

For device 3

Operation 21. ANNEALING N_2 time=30 min Temp=850 °C
Stripe oxide (All devices)

For device 2(LD)

For device 4

Operation 21. ANNEALING N_2 time=30 min Temp=850 °C
Stripe oxide (All devices)

For device 8

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 22. Oxide layer for protection & contact patterning
wet2 time=5 min Temp=950 °C

For device 5

For device 3

Operation 22. Oxide layer for protection & contact patterning
wet2 time=5 min Temp=950 °C

For device 2(LD)

For device 4

Operation 22. Oxide layer for protection & contact patterning
wet2 time=5 min Temp=950 °C

For device 8

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 23. Contact formation
 deposit nitride thick=0.16 μm ;
 TEOS Deposit oxide thick=0.5 μm Temp = 720 $^{\circ}\text{C}$ + weto2time=30 min Temp=850 $^{\circ}\text{C}$
 Mask: **CONTACT (jetstrM9 – CONTACT)**
 Etch OXIDENITRIDE/OXIDE
 Strip PR

For device 5

For device 3

37

Operation 23. Contact formation
 deposit nitride thick=0.16 μm ;
 TEOS Deposit oxide thick=0.5 μm Temp = 720 $^{\circ}\text{C}$ + weto2time=30 min Temp=850 $^{\circ}\text{C}$
 Mask: **CONTACT (jetstrM9 – CONTACT)**
 Etch OXIDENITRIDE/OXIDE
 Strip PR

For device 2(LD)

For device 4

Operation 23. Contact formation
 deposit nitride thick=0.16 μm ;
 TEOS Deposit oxide thick=0.5 μm Temp = 720 $^{\circ}\text{C}$ + weto2time=30 min Temp=850 $^{\circ}\text{C}$
 Mask: **CONTACT (jetstrM9 – CONTACT)**
 Etch OXIDENITRIDE/OXIDE
 Strip PR

For device 8

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 24. Interconnection formation
deposit Aluminum thick=0.6 μm ;
Mask: **METAL1** (jetstrM10 – METAL1)
Patterned Al etch; Strip PR
Sintering N_2 time=30 min Temp=400 $^\circ\text{C}$

For device 5

For device 3

Operation 24. Interconnection formation
deposit Aluminum thick=0.6 μm ;
Mask: **METAL1** (jetstrM10 – METAL1)
Patterned Al etch; Strip PR
Sintering N_2 time=30 min Temp=400 $^\circ\text{C}$

For device 2(LD)

For device 4

Operation 24. Interconnection formation
deposit Aluminum thick=0.6 μm ;
Mask: **METAL1** (jetstrM10 – METAL1)
Patterned Al etch; Strip PR
Sintering N_2 time=30 min Temp=400 $^\circ\text{C}$

For device 8

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 25. PECVD UTEOS layer for protection & via patterning
Deposit oxide thick=0.5 μm Temp = 280 $^{\circ}\text{C}$

For device 5

For device 3

Operation 25. PECVD UTEOS layer for protection & via patterning
Deposit oxide thick=0.5 μm Temp = 280 $^{\circ}\text{C}$

For device 2(LD)

For device 4

Operation 25. PECVD UTEOS layer for protection & via patterning
Deposit oxide thick=0.5 μm Temp = 280 $^{\circ}\text{C}$

For device 8

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 26. Via formation

Deposit photoresist positive thick=1 μm ; expose

Mask: VIA (JetstrM11 – VIA)

Ech oxide in windows

Ech PR

For device 5

For device 3

Operation 26. Via formation

Deposit photoresist positive thick=1 μm ; expose

Mask: VIA (JetstrM11 – VIA)

Ech oxide in windows

Ech PR

For device 2(LD)

For device 4

Operation 26. Via formation

Deposit photoresist positive thick=1 μm ; expose

Mask: VIA (JetstrM11 – VIA)

Ech oxide in windows

Ech PR

For device 8

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 27. Shield formation
 Deposit Aluminum thick=0.6 μm ;
 Deposit photoresist positive thick=1 μm expose
 Mask: METAL2 (jfetstrM12 – METAL2)
 Patterned Al etch; Strip PR
 Sintering N_2 time=30 min Temp=400 $^{\circ}\text{C}$

For device 5

For device 3

Operation 27. Shield formation
 Deposit Aluminum thick=0.6 μm ;
 Deposit photoresist positive thick=1 μm expose
 Mask: METAL2 (jfetstrM12 – METAL2)
 Patterned Al etch; Strip PR
 Sintering N_2 time=30 min Temp=400 $^{\circ}\text{C}$

For device 2(LD)

For device 4

Operation 27. Shield formation
 Deposit Aluminum thick=0.6 μm ;
 Deposit photoresist positive thick=1 μm expose
 Mask: METAL2 (jfetstrM12 – METAL2)
 Patterned Al etch; Strip PR
 Sintering N_2 time=30 min Temp=400 $^{\circ}\text{C}$

For device 8

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Operation 29. Active window formation
 Deposit photoresist positive thick=1 μm expose
 Mask: **DesignF (JetstrM14 – ACTIVE)**
 Develop
 Etch nitride; Strip PR

For device 5

For device 3

Operation 29. Active window formation
 Deposit photoresist positive thick=1 μm expose
 Mask: **DesignF (JetstrM14 – ACTIVE)**
 Develop
 Etch nitride; Strip PR

For device 2(LD)

For device 4

Operation 29. Active window formation
 Deposit photoresist positive thick=1 μm expose
 Mask: **DesignF (JetstrM14 – ACTIVE)**
 Develop
 Etch nitride; Strip PR

For device 8

Fig. 4.46. Fabrication process of all JFET-based color sensor (continued)

Fig. 4.47. Mask alignment for the fabrication process of all JFET-based color sensor

4.3.5. MEDICI simulations: results

From the results of previous simulation we settle that the variation of the channel doping N_D and the channel depth “ a ” can be made through the fabrication while the geometrical dimensions of the proposed color sensor can be divided on the variety of devices that the most essentially TS-IV simulation was presented in the sections 4.2.5 with results of concentration profiles for top-gate, bottom gate, source and drain.

4.3.5.1. DEVICE 02

DEVICE02 presented in Fig. 4.17 is the basic JFET with a normal top gate, bottom gate, source and drain. The doping concentration profile for the device at 0.2 μm depth is shown in Fig. 4.47. The current-voltage characteristic for this type of device for the top-gate, bottom gate and drain is presented in Fig. 4.48, Fig. 4.49 and Fig. 4.50. The pinch-off voltage is 12 V and pinch-off current 27 $\mu\text{A}/\mu\text{m}$ and saturation voltage $V_{DSat} = 25\text{ V}$ $I_{DSat} = 30\text{ }\mu\text{A}/\mu\text{m}$. It can be seen in Fig. 4.51 that the electric field doesn't respect the assumption we made (the electric field only in the y -direction) and the overall electric field in the channel is altered toward the x -direction.

4.3.5.2. DEVICE 03

DEVICE03 presented in Fig. 4.20 is an enhancement of the basic JFET with a top gate improved with two guard rings that will increase the protection of breakdown junction between top-gate and channel. The current-voltage characteristic for this type of device was discussed extended in previous section and it will not be take up again here.

Fig. 4.47. The doping profile of a long channel JFET for a device (D02) with the following geometrical parameters:
Channel with $N_D = 10^{16} \text{ cm}^{-3}$, $a = 4 \mu\text{m}$; $L = 80 \mu\text{m}$, Top Gate with $x_{TG} = 0.3 \mu\text{m}$, $N_{TG} = 1 \cdot 10^{17} \text{ cm}^{-3}$, Source and drain $N_A = 4 \cdot 10^{19} \text{ cm}^{-3}$.

Fig. 4.48. I_{DS} – V_{DS} characteristics of long channel JFET for a device (D02) with the same geometrical and physical parameters as in Fig. 4.47

Fig. 4.49. I_{BG} – V_{DS} characteristics of long channel JFET for a device (D02) with the same geometrical and physical parameters as in Fig. 4.47

Fig. 4.50. I_{TG} – V_{DS} characteristics of long channel JFET for a device (D02) with the same geometrical and physical parameters as in Fig. 4.47

Fig. 4.51. Electric field profile of a long channel JFET for a device (D02) with the same geometrical and physical parameters as in Fig. 4.47 in the saturation region ($V_D = 25$ V)

4.3.5.3. DEVICE 04

DEVICE04 presented in Fig. 4.23 is a development of the basic JFET with a top gate under a N-well with the intention of increasing the collection of carriers for the blue wavelength by increasing the depletion region in the junction N-well-top gate. The doping concentration profile for the device is shown in Fig. 4.52. The pinch-off voltage is 10 V and pinch-off current 11.3 mA/ μ m and saturation voltage $V_{DSat} = 25$ V $I_{DSat} = 12.7$ mA/ μ m is presented in Fig. 4.52. The current-voltage characteristic for this type of device for the top-gate, bottom gate, nwell and drain is presented in Fig. 4.53, Fig. 4.54 Fig. 4.55, and Fig. 4.56. It can be seen in Fig. 4.57 (left part) that the electric field doesn't respect the assumption we made (the electric field only in the y-direction) and the overall electric field in the channel is altered toward the x-direction only for the beginning of the linear region ($V_D = 0$ V).

Fig. 4.52. The doping profile of a long channel JFET for a device (D04) with the following geometrical parameters:
 Channel with $N_D = 10^{16} \text{ cm}^{-3}$, $a = 4 \mu\text{m}$; $L = 85 \mu\text{m}$, Top Gate with $d_{TG} = 0.05 \mu\text{m}$, $N_{TG} = 1 \cdot 10^{16} \text{ cm}^{-3}$, Nwell: with $x_{NWell} = 0.5 \mu\text{m}$, $N_{NWell} = 2 \cdot 10^{16} \text{ cm}^{-3}$, Source and Drain $N_A = 8 \cdot 10^{19} \text{ cm}^{-3}$.

Fig. 4.53. I_{DS} - V_{DS} characteristics of long channel JFET for a device (D04) with the same geometrical and physical parameters as in Fig. 4.52

Fig. 4.54. I_{TG} – V_{DS} characteristics of long channel JFET for a device (D04) with the same geometrical and physical parameters as in Fig. 4.52

Fig. 4.55. I_{BG} – V_{DS} characteristics of long channel JFET for a device (D04) with the same geometrical and physical parameters as in Fig. 4.52

Fig. 4.56. I_{NWELL} – V_{DS} characteristics of long channel JFET for a device (D04) with the same geometrical and physical parameters as in Fig. 4.52

Fig. 4.57. Electric field profile of a long channel JFET for a device (D04) with the same geometrical and physical parameters as in Fig. 4.52 in the linear ($V_D = 0$ V) and saturation region ($V_D = 25$ V)

4.3.5.4. DEVICE 05

DEVICE05 presented in Fig. 4.25 is a JFET with two top gates, one with protective rings and low doping concentration and another one high doping concentration to increase the protection of breakdown junction. The doping concentration profile for the device is shown in Fig. 4.58. The pinch-off voltage is 7 V, pinch-off current $21.8 \mu\text{A}/\mu\text{m}$ and saturation voltage $V_{DSat} = 20 \text{ V}$, $I_{DSat} = 24 \mu\text{A}/\mu\text{m}$ is presented in Fig. 4.59. The current-voltage characteristic for this type of device for the top-gate1, top-gate2, bottom gate and drain is presented in Fig. 4.59, Fig. 4.60 Fig. 4.61, and Fig. 4.62. It can be seen in Fig. 4.63 (only for TG2) that the electric field doesn't respect the assumption we made (the electric field only in the y -direction) and the overall electric field in the channel is altered toward the x -direction only for the beginning of the pinch-off region ($V_D = 12 \text{ V}$).

Fig. 4.58. The doping profile of a long channel JFET for a device (D05) with the following geometrical parameters:
 Channel with $N_D = 10^{16} \text{ cm}^{-3}$, $a = 4 \mu\text{m}$; $L = 85 \mu\text{m}$, Top Gate1 with $x_{TG1} = 0.05 \mu\text{m}$, $N_{TG1} = 6 \cdot 10^{15} \text{ cm}^{-3}$, Top Gate2: with $x_{TG2} = 0.5 \mu\text{m}$, $N_{TG2} = 1 \cdot 10^{19} \text{ cm}^{-3}$, Source and Drain $N_A = 8 \cdot 10^{19} \text{ cm}^{-3}$.

Fig. 4.59. I_{DS} – V_{DS} characteristics of long channel JFET for a device (D05) with the same geometrical and physical parameters as in Fig. 4.58

Fig. 4.60. I_{TG1} – V_{DS} characteristics of long channel JFET for a device (D05) with the same geometrical and physical parameters as in Fig. 4.58.

Fig. 4.61. I_{TG2} – V_{DS} characteristics of long channel JFET for a device (D05) with the same geometrical and physical parameters as in Fig. 4.58.

Fig. 4.62. I_{BG} – V_{DS} characteristics of long channel JFET for a device (D05) with the same geometrical and physical parameters as in Fig. 4.58.

Fig. 4.63. Electric field profile of a long channel JFET for a device (D05) with the same geometrical and physical parameters as in Fig. 4.58 in the pinch-off region ($V_D = 12$ V)

4.3.5.5. DEVICE 08

The structure of DEVICE08 is presented in Fig. 4.28. The doping concentration profile for the device used in MEDICI simulation is shown in Fig. 4.64. The pinch-off voltage is 19 V and pinch-off current 67 mA/ μ m and saturation voltage $V_{DSat} = 35$ V $I_{DSat} = 77$ mA/ μ m is presented in Fig. 4.65. The current-voltage characteristic for this type of device for the top-gate, bottom gate and drain is presented in Fig. 4.65, Fig. 4.66 and Fig. 4.67. It can be seen in Fig. 4.68 (left part) that the electric field doesn't respect the assumption we made (the electric field only in the y -direction) and the overall electric field in the channel is altered toward the x -direction only for the beginning of the saturation region ($V_D = 25$ V). This means that the results we will get from the real measurements can be quite different from the simulated ones.

Fig. 4.64. The doping profile of a long channel JFET for a device (D08) with the following geometrical parameters:
Channel with $N_D = 10^{16} \text{ cm}^{-3}$, $a = 4 \text{ μm}$; $L = 80 \text{ μm}$, Top Gate with $x_{TG} = 0.05 \text{ μm}$, $N_{TG} = 6 \cdot 10^{15} \text{ cm}^{-3}$, Source $N_A = 6 \cdot 10^{19} \text{ cm}^{-3}$. and Drain $N_D = 8 \cdot 10^{18} \text{ cm}^{-3}$,

Fig. 4.65. I_D - V_D characteristics of long channel JFET for a device (D08) with the same geometrical and physical parameters as in Fig. 4.64

Fig. 4.66. I_{TG} – V_{DS} characteristics of long channel JFET for a device (D08) with the same geometrical and physical parameters as in Fig. 4.64.

Fig. 4.67. I_{BG} – V_{DS} characteristics of long channel JFET for a device (D08) with the same geometrical and physical parameters as in Fig. 4.64.

Fig. 4.68. Electric field profile of a long channel JFET for a device (D08) with the same geometrical and physical parameters as in Fig. 4.64 in the saturation region ($V_D = 25$ V)

4.4. Spectral response simulation results of photo - JFET

This section presents the primary aspects of the spectral response performance of a photo-JFET (device3 type like in figure) with the simulated structure presented in the last part of section 4.3. Fig. 4.69 shows the currents of JFET structure in all three optional regimes for top and bottom gates. The ratio between dark currents and the generated photocurrent are two orders higher for each of the optional regimes.

It can be seen from the Fig. 4.69 the peaks of photo generated currents collected by the top and bottom gate that a good separation of the detected colors can be achieved and can be improved by the bias conditions: the top gate photocurrent peaks wavelength shifts from 470 nm (blue) to 494 nm; this is expected when the depletion region increases and the bottom gate the peak wavelength shifts from 640 nm to 662 nm (red). Similarly,

Fig. 4.70 shows clearly that the collected drain photocurrent peaks wavelength shifts from 540 nm (green) to 608 nm is presented in when the drain voltage V_D increases from 1 V to 2 V (linear conditions) thus providing a good spectral response for the part of visible range.

Another phenomenon was observed when simulating the device illuminated with white light in bias condition of the drain voltage V_D close to pinch-off voltage V_P the drain photocurrent will equalize the saturation voltage and the peak wavelength will be fixed at 650 nm.

Linear region		Pinch - off region		Saturation region	
— BG	$V_D = 1 \text{ V}$ $V_{TG} = 0 \text{ V}$ $V_{BG} = -1 \text{ V}$	— BG	$V_D = 13 \text{ V}$ $V_{TG} = V_{BG} = 0 \text{ V}$	— BG	$V_D = 20 \text{ V}$ $V_{TG} = V_{BG} = -5 \text{ V}$
— TG		— TG		— TG	
— BG	$V_D = 2 \text{ V}$ $V_{TG} = V_{BG} = 0 \text{ V}$			— BG	$V_D = 11 \text{ V}$ $V_{TG} = V_{BG} = -2 \text{ V}$
— TG				— TG	

Fig. 4.69. The photo-responses of the top and bottom gates of JFET in all three regimes (lower and upper junction)

Fig. 4.70. The drain current photo-response of a JFET in the linear operation regimes.

It can be seen from the Fig. 4.69 and 4.70 that the most advantageous region of the operation of the JFET-based device for optimal color sensing is the linear region. Another simulation for the same device only in the linear operation region: $V_D = 1 \text{ V}$, $V_{BG} = 0 \text{ V}$, $V_{TG} = -1 \text{ V}$, $V_S = 0 \text{ V}$ is in Fig. 4.70.

This was the reason why for the DEVICE05 existing in the figure 4.25 with the doping profile existing in the Fig. 4.58 we study the spectral response only in the linear region with: a) $V_D = 0 \text{ V}$, $V_{BG} = 0 \text{ V}$, $V_{TG} = 0 \text{ V}$, $V_S = 0 \text{ V}$ and b) $V_D = 2 \text{ V}$, $V_{BG} = 0 \text{ V}$, $V_{TG} = 0 \text{ V}$, $V_S = 0 \text{ V}$ with the graphical output presented for each terminal (TG1, TG2, BG and D) in figures 4.71–4.75.

a

b

Fig. 4.71. The photo-responses of the top gate 1 of JFET (DEVICE05) in linear regimes: a) $V_D = 0$ V ($V_{TG} = V_{BG} = 0$ V), b) $V_D = 2$ V ($V_{TG} = V_{BG} = 0$ V)

a

b

Fig. 4.72. The photo-responses of the top gate 2 of JFET (DEVICE05) in linear regimes: a) $V_D = 0$ V ($V_{TG} = V_{BG} = 0$ V), b) $V_D = 2$ V ($V_{TG} = V_{BG} = 0$ V)

a

b

Fig. 4.73. The photo-responses of the bottom gate of JFET (DEVICE05) in linear regimes: a) $V_D = 0$ V ($V_{TG} = V_{BG} = 0$ V), b) $V_D = 2$ V ($V_{TG} = V_{BG} = 0$ V)

Fig. 4.74. The photo-responses of the drain of JFET (DEVICE05) in linear regimes:
a) $V_D = 0$ V ($V_{TG} = V_{BG} = 0$ V), b) $V_D = 2$ V ($V_{TG} = V_{BG} = 0$ V)

Fig. 4.75. The photo-response of JFET in linear region of operation for top and bottom gate (lower and upper junction)–MATLAB simulation

The results were presented in separate graphics because of the difference in the order of the current measured. To compare DEVICE03 (Fig. 4.69 half full dark green triangles for TG, half full pink triangles for BG and 4.70 full bright green circles for Drain) with DEVICE05 (Fig. 4.71b, 4.72b, 4.73b and 4.74b) the values for the peak wavelength and currents under the same conditions: $V_D = 2$ V and $V_{TG} = V_{BG} = 0$ V show the following:

- For the top gate, in DEVICE05 we have an improvement in the collection of carriers generated by wavelength in 400–450 nm domain (blue) because the peak shifts from 494 nm to 400 nm confirming our expectation:
 - DEVICE03 $\lambda_{TG} = 494$ nm & $I_{peak\ TG} = 420$ pA
 - DEVICE05 $\lambda_{TGI} = 400$ nm & $I_{peak\ TGI} = 0.450$ μ A
- For the bottom gate we have an improvement in the collection of carriers generated by wavelength in 650–750 nm domain (red):
 - DEVICE03 $\lambda_{BG} = 662$ nm & $I_{peak\ BG} = 280$ pA
 - DEVICE05 $\lambda_{BG} = 710$ nm & $I_{peak\ BG} = 0.040$ pA

- For the drain we have an improvement in the collection of carriers generated by wavelength in 450–550 nm domain (green):
 - DEVICE03 $\lambda_D = 608 \text{ nm}$ & $I_{peak D} = 3 \text{ pA}$
 - DEVICE05 $\lambda_D = 530 \text{ nm}$ & $I_{peak D} = 0.950 \text{ }\mu\text{A}$

At the moment, it can be concluded that, even if the results from MATLAB simulation (Fig. 4.75) are not consistent with those resulted from TCAD simulation results, good color detection by the various regions of the devices in the entire visible range.

4.5. Conclusions

This chapter has shown that the JFET behavior depends strongly not only of geometrical parameters (all the devices had mainly the same parameters but the pinch-off voltage and current are different for each device) but also of the bias conditions.

This chapter has revealed that the spectral response of different photo-JFET structures can be modified by changing the doping levels and junction depths inside the device. These changes are relatively easy to make during manufacturing but many would impact transistor and other device performance. To diversify the types of the devices we had two choices: one, to fabricate each device separate and two, to combine the process steps in such a way that will allow us to have the different device on the same wafer. The addition of extra masks and process steps limited to the first choice would allow such changes to be made without compromising JFET operation but would obviously increase manufacturing cost. Therefore we decide to compromise between fabrication and modeling by choosing the second option.

One important change that can easily be made is the epi thickness and simulations suggest that this may be a way of increasing the quantum efficiency of the photo-JFET by select a wider epi-layer and manage the bias condition to fit our demands.

Modeling of the JFET structure shows that the three responses can be changed significantly but it has been found easier to increase the responses than to decrease them. In the context of the JFET structure this means that it is probably undesirable to alter the structure to match the two responses — therefore a more complicated readout circuit may be required. More positively, the performance in the photo-JFET (DEVICE05) structure is superior to the standard JFET (DEVICE 03).

The changes investigated were to the epitaxial layer thickness, junction depths, and doping levels.

Chapter FIVE: JFET–Color Sensor Fabrication

5.1. Introduction.

In this chapter the fabrication of the JFET–based color sensors is described. The layout of all the devices depicted in section 4.2.5, for which the design considerations were expressed in section 4.2.4 and the fabrication process steps in Fig. 4.46, respectively, is shown in Fig.5.1. The parameters of interest for these fabricated JFET–based color sensors have been tested and measured.

5.2 Layout design

Besides the previous design of the cross-sectional structure of the JFET–based color sensors, the realistic design of the distribution of the contacts, the illumination regions, the insulation regions and the metal shield are essential for the optimum performance of the device.

Therefore, although challenging, the layout design is not as complex as that of VLSI IC's for industry applications. The CADENCE Virtuoso layout editor was used for the layout design based on the lambda-based Design Rules. It can be used to create and edit polygons, paths, rectangles, circles, pins, contacts, etc, or to place cells into other cells to create hierarchical designs, or to connect a pin or group of pins in a net internally or externally, or to automate each stage of the design task [47]. Because a modified 2 μm CMOS process was used for the fabrication of the JFET–based color sensors, the basic length unit λ was taken as 2 μm for the layout design.

The layout of the whole chip has been designed such that each JFET–based color sensor is realized twice: one chip is photosensitive, while the other is covered with a layer of metal, serving as a "blind" ("dark") reference

As Fig.5.1 shows, the yellow square encloses the reference area comprising 6 dices, and the red square surrounds all the 6 units of the sensors area, each unit

comprising 8 dices. The sensors denominated as "light" ones are true color sensing devices, whereas the so-called "dark" ones would act as a reference ("blind") device as the surface of each such "blind" device is covered with metal to block any illumination effect. Additionally, the chip contains the marks for mask alignment inserted in the lower left of the device layout.

Fig. 5.1. The JFET - based color sensing devices depicted in the VIRTUOSO layout editor. The yellow/red squares enclose the reference ("blind") the "light" areas, respectively.

Fig. 5.2 shows a blow-up detail for one unit of the sensor area. A dice comprise, of 2 to 7 devices connected to 15 or 24 pads, each with a $100 \times 100 \mu\text{m}^2$ area. Each dice was intended for mounting in a standard 24-pin Dual In Line (DIL) housing and subsequent wire-bonding. All the important geometrical details for all the devices are presented in Table 5.1, where Z, the width of the device, and L is the length of the channel (i.e. the distance between Source and Drain), while D2, D3, D4, D5 and D8 are abbreviations for DEVICE02, DEVICE03, DEVICE04, DEVICE05 and DEVICE08. The other abbreviations are: ZT is the device with zigzag shape of the top gate, IT is the device with interdigitated gate, MN and MT are the devices with for multiple N-Wells and multiple top gates, respectively.

Fig. 5.2. The sensor area depicted in VIRTUOSO layout editor without the protector shield. The red polygons represent the light-sensitive areas of the actual sensors. In the reference ("dark") devices, these areas are covered by a metallic layer.

Table 5.1. The essential geometrical parameters for the all devices and their distribution on the first 6 dices

Nr.	Dice	Type device	Device	Z [μm]	L [μm]	Z / L	Illuminated area [μm^2]	Gate area [μm^2]
1	1	D2&D5	A	260	760	0.342	139360	169000
2		D2&D5	B	260	760	0.342	180316	187200
3	2	D2	A	500	83	6.024	41500	53600
4		D5	B	499	84	5.940	35036	46016
5		D2	C	40	220	0.182	5000	8000
6		D2	D	30	1016	0.030	14000	30000
7		D2	E	18	516	0.035	2500	9000
8	3	D3	A	40	230	0.174	5250	6936
9		D2ZT	B	50	221	0.226	6760	-
10		D3	C	150	70	2.143	5850	6716
11		D2	D	150	60	2.500	3800	6000
12		D5IT	E	150	70	2.143	3366	7750
13		D3	F	50	70	0.714	1800	2116
14		D5IT	G	90	900	0.100	34200	-
8	4	D3	A	40	230	0.174	5250	6936
9		D3ZT	B	50	221	0.226	6760	
10		D3	C	150	70	2.143	5850	6716
11		D2	D	150	60	2.500	3800	6000
12		D5IT	E	150	70	2.143	3366	7750
13		D3	F	50	70	0.714	1800	2116
14		D5IT	G	90	900	0.100	34200	-
15	5	D4MN	A	260	800	0.325	157620	192400
16		D4MN	B	260	780	0.333	155806	192400
17	6	D3MT	A	512	439	1.166	51040	57600
18		D5MT	B	512	439	1.166	51040	57600

The remaining considerations from the complete list previously presented in detail in section 4.2.4 were applied at wafer level and are presented in table 5.2.

Table 5.2. The practical values of various factors modified at wafer level

Nr.	Wafer number	Channel half-width a [μm]	AR coating [$\text{\AA}$]	Channel doping conc. N_{Dch} [cm^{-3}]	Top Gate doping conc. N_{ATG} [cm^{-3}]
1	W1	2.75	400 Si_3N_4	$5 \cdot 10^{15}$	$4 \cdot 10^{14}$
2	W2	2.75	100 SiO_2 +280 Si_3N_4	$5 \cdot 10^{15}$	$5 \cdot 10^{15}$
3	W4	4.25	100 SiO_2 +280 Si_3N_4	$5 \cdot 10^{15}$	$4 \cdot 10^{14}$
4	W5	2.75	100 SiO_2 +400 Si_3N_4 +1100 PECVD SiO_2	$5 \cdot 10^{15}$	$5 \cdot 10^{15}$
5	W8	2.75	100 SiO_2	10^{15}	$5 \cdot 10^{15}$
6	W9	2.75	400 Si_3N_4	10^{15}	10^{15}
7	W13	4.25	400 Si_3N_4	10^{14}	10^{15}

5.3. Basic fabrication techniques

The manufacture of the JFET–based color sensor consists of a complex sequence of process steps that require high precision, repeatability, and cleanliness. The 9 main process steps are:

- a) Basic wafer cleaning ,
- b) Lithography patterning processes,
- c) Oxidation producing the oxide windows for diffusion,
- d) Ion implantation,
- e) Diffusion of boron and phosphorus, respectively,
- f) Creating contact oxide windows by using both wet etching and dry etching
- g) Deposition of AR coatings
- h) Sputtering aluminum and formation of the interconnection to bond pads
- i) Testing of the fabrication and device parameters.

Let us now mention briefly the main characteristics of each step listed above. The fabrication of our devices is based on the $2\mu\text{m}$ *n-well CMOS Process Flow* of the Micro Fabrication Laboratory (MFL) in Electrical and Electronic Engineering School. This was

necessary because no other fabrication alternatives was available, and also because it was necessary to illustrate the capability and limitations of this process with respect to the fabrication of the JFET-based color sensors.

It is more accurate to speak of the overall process as being rather a CMOS-compatible than a standard CMOS one, one of the main reasons being the use of epitaxy in our process. An epitaxial layer (or epi layer) is grown on the wafer surface to achieve the same single crystal structure of the wafer with accurate control over the doping type, doping concentration and thickness of the epi layer. The most common epitaxy growth method is vapor-phase epitaxy and it is the only affordable method of high quality monocrystalline growth for many semiconductor materials.

Surface contamination due to particles, metals, micro-roughness and watermarks has a great impact on the device electrical characteristics. In order to achieve a clean surface the wafers are cleaned before each process step to remove organic, inorganic, and metallic contamination. Particularly the cleaning prior to oxidation is critical. The wet-clean process used in MFL is the industry standard, the RCA clean, consisting of two steps denominated as standard clean 1 (SC-1) and standard clean 2 (SC-2). SC-1 is a mixture of ammonium hydroxide, hydrogen peroxide and DI water and it is capable of removing particles and organic materials. The removal of particles is primarily achieved through oxidation of the particle or electric repulsion. SC-2 is a mixture of hydrochloric acid, hydrogen peroxide and DI water and removes metals from the wafer surface. Many cleaning steps also include an HF last step to remove native oxide.

Much of the success of silicon as a largely used semiconductor material is owing to the properties of its native oxide, silicon dioxide (SiO_2), which is both an excellent insulator and an excellent passivation mask to inhibit contamination of the silicon surface. The oxide film that will act as a masking layer for several of the process steps is thermally grown on the wafer through a wet/dry oxidation process or deposited by, e.g., Chemical Vapor Deposition (CVD). CVD techniques have also been applied to deposit another often used dielectric, silicon nitride (Si_3N_4), as well as conducting materials such as epitaxial and polycrystalline silicon. Thermal oxidation is accomplished using an oxidation furnace or diffusion furnace since the oxidation is basically a diffusion process involving oxidant species. A process recipe is loaded into the high-temperature furnace to control the oxidation parameters.

The oxide growth rate is affected by time, temperature, and pressure. More specifically, oxide growth is accelerated by an increase in oxidation time, oxidation temperature, or oxidation pressure. Other factors that affect thermal oxidation growth rate

for SiO₂ include: the crystallographic orientation of the wafer; the wafer doping level; the presence of halogen impurities in the gas phase; the presence of plasma during growth; and the presence of a photon flux during growth [80].

To create the desired device, the previously grown or deposited layer has to be patterned, which is conventionally done by photolithography. A photolithographic mask with the desired feature defined is aligned to the wafer flat and the photosensitive polymer applied to the wafer is exposed to UV radiation, and developed. The lithography already sets a limit to the minimum attainable feature size (0.5 μm in the case of the OAI Mask Aligner), depending on the finest feature on the mask, the resolution of the photoresist, the wavelength of the exposure light (365 nm i-line in the case of the OAI Mask Aligner) and the printing technique [81]. Critical dimensions (CDs) are measured to achieve precise control over feature size dimensions.

After the patterning of the photoresist an etch step can take place to open the window for the next operation or the next step can take place through the existing oxide.

Doping increases silicon conductivity by adding small amounts of other elements. Common p-type dopant elements are trivalent from Group III a (boron) and n-type ones are pentavalent from Group V a (phosphorus, arsenic and antimony).

The introduction of dopants in a semiconductor is the most common application of ion implantation. Dopant ions such as boron, phosphorus or arsenic are generally created from a gas source, so that the purity of the source can be very high. Dopant atoms are ionized and then accelerated by an electric field until they impinge on the silicon surface, where they embed themselves. During subsequent thermal treatment, the dopants are activated and redistributed. The average penetration depth is called the range of the ions. Under typical circumstances ion ranges will be between 10 nm and 1 μm . Thus, ion implantation is especially useful in our cases for the top gate where the structural change is desired to be near the surface of the target. Because particular crystallographic directions of the silicon offer much lower stopping than other directions, most implantation is carried out using a tilt of a few degrees off-axis combined with a rotation of the wafer.

Ion implantation damages the crystal structure of the target which is often unwanted; therefore, for damage recovery implantation processing is often followed by a thermal annealing.

Thermal treatments are designed for different effects. Wafers can be heated in order to activate dopants, densify deposited films, change states of grown films, repair

damage from implants, move dopants or drive dopants from one film into another or from a film into the wafer substrate. The operation take place in a furnace and a process recipe is loaded to control the treatment parameters.

Contact windows are created through the silicon oxide layer by etching. Etch is the process of selectively removing unneeded material from the wafer surface, using either chemical or physical means. Dry etch exposes the wafer to a plasma that interacts physically or chemically (or both) to remove the surface material. Wet etch uses liquid chemicals to chemically remove the wafer surface material.

Critical etch parameters are: etch rate, etch profile (the shape of the sidewall of the etched feature), selectivity (the ratio of etch rates for two different materials), and uniformity (the capability of the process to etch uniformly across the entire wafer surface).

An isotropic etch profile is characterized by inherent undercutting, whereas an anisotropic etch takes place exclusively in one direction only. Other key issues to be considered in dry etching are:

- Residues: Various unwanted materials remain on the wafer after etching.
- Polymer formation: on the sidewalls to prevent lateral etching.
- Plasma-induced damage: should be avoided or minimized when charge sensitive devices such as MOS transistors are already realized on the wafer surface.
- Particle contamination and defects: that results from plasma etching.

Despite all these drawbacks wet etching has been largely replaced by dry etch because it is usually isotropic and cannot provide small features sizes. Wet etching is usually used to strip unwanted layers, such as photoresist, oxide or a silicon nitride.

As a last step, the different areas of doped silicon are connected by deposition of conductive layers, such as metals. Due to its many favorable properties, aluminum has been the most important material to perform this electrical function [82]. Moreover, its high reflectivity makes it is also an excellent material to be used for optical purposes, as mirrors. In our case it was used to form such metallic shield to block any illumination effect onto the reference devices.

Intermediate investigations of test structure, are commonly performed through the process to determine various parameters of interest, e.g. thickness of different layers, resistivity of diffused layers, critical dimensions (CD) measurements. Such measurements occur between the steps and are vital to ensure that the actual final device have the required structures.

5.4. Fabrication of the JFET-based color sensor

The detailed fabrication sequence of the JFET-based color sensor is presented in the standard process flow sheet given in Appendix 3. This section will explain significance and rationale behind every fabrication step.

As starting material 15 (100)-oriented *p*-type wafers with 0.01–0.1 Ωcm resistivity were used. Then *n*-type epitaxial layers with thicknesses of 5.5 μm and 8.5 μm and with doping concentration of 10^{14} , 10^{15} , and $5 \cdot 10^{14} \text{ cm}^{-3}$ were grown on various wafers. Arsenic was used as a dopant because it has a very low diffusivity and therefore would minimize its ex-diffusion into the underlying substrate.

Subsequently, a thin oxide layer (300 Å) was grown and a 1650 Å thick nitride layer was deposited onto it and patterned (using the *SDCON* mask) to define the Source/Drain for devices D02, D03, D04 and D05 and the *n*-type Source for device D08. This oxide served as the implant protection oxide and would not be etched away for most of the processing. The same mask defined the areas where a deep *n*-type isolation diffusion was required. Electrical isolation is needed around each photo-JFET to eliminate the possibility of collection of generated carriers from another neighboring photo-JFET.

After dry etching the exposed surface of the nitride layer, phosphorus ions were implanted through the first oxide layer (300 Å). Once the photoresist was stripped and the wafer cleaned, an oxide layer 1700 Å thick was thermally grown, the process contributing at the same time to the diffusion of electrically active dopants. This oxide served as implant protection so that the subsequent implant will not damage the surface of the silicon. The growth of this thin oxide on the exposed silicon areas also starts to create a small step (since approximately 44% silicon is consumed during thermal oxidation [82]) on the device surface. This step will allow the subsequent masks to be aligned easily.

Subsequently, the nitride layer is removed and the oxide layer is patterned (mask *DCON*) by opening windows through which boron ions are implanted to define the *p*-type Drain for device D08. The implanted boron is activated and diffused in an inert ambient (N_2) for 45 minutes at 1100°C.

Mask PCHANNEL was used to pattern the *p*-channel in lambda-diode device followed by a boron implant at low energy (30 keV) and moderate dose ($4 \cdot 10^{13} \text{ atoms/cm}^2$). The photoresist was then finally removed by O_2 plasma ashing. The drive-in was executed in an inert ambient (N_2) at 1100°C for only 35 minutes, since boron has a

high diffusivity and the concentration gradient of the implanted PCHANNEL region was large.

Next, the protection rings for the top gate in the device D03 were defined using the TGRING mask followed by a boron implant at low energy (25 keV) and with a relatively high dose (10^{15} atoms/cm²). As mentioned above the same 300 Å oxide was used to protect the Si surface for all the implants. This was possible due to two reasons: first, because the various different implantation take place in different locations on the device/wafer and second, it would allow the implantation of boron ions through it in the desired areas since its thickness is much smaller than the minimum value for 99.99% implant masking effectiveness which for boron implanted at an energy of 30 keV is 2000 Å. The photoresist was then finally removed by O₂ plasma ashing. The drive-in was carried out in an inert ambient (N₂) at a low temperature (900°C), again for a short time of 30 minutes, because boron has a very high diffusivity and the concentration gradient is large.

Subsequently, the *n*-well in device D04 was formed with the NWELL mask. Phosphorus is implanted at a high energy (110 keV) and high dose ($3 \cdot 10^{15}$ atoms/cm²). The high dose is necessary to have a high final surface concentration and to prevent the formation of any Schottky barriers at the contacts. After the implant, the photoresist is removed by O₂ plasma ashing.

The implanted phosphorus was activated and diffused in an inert ambient (N₂) at 900°C for 30 minutes. This short treatment will activate the phosphorus without increasing the thickness of initial implant oxide.

A 1650 Å thick silicon nitride layer was deposited by Low Pressure Chemical Vapor Deposition (LPCVD). Silicon nitride is mechanically very strong and was used as a “mold” for the next oxide growth step which will allow the subsequent masks to be aligned easily. The nitride was patterned (using the SDIMCON mask) using a dry etch process, whereby the nitride etch had to stop on the initial oxide layer deposited on the wafer.

Subsequently, an Arsenic implant was done at 20 keV with a dose of $3 \cdot 10^{15}$ atoms/cm². The photoresist is then finally removed by O₂ plasma ashing. No immediate subsequent drive-in was added since the next oxide growth can serve as activation and drive-in for the implanted arsenic, too.

An oxide layer of 1700 Å was grown by wet oxidation which created a small step that would allow the subsequent masks to be aligned easily.

After the nitride was stripped in hot phosphoric acid, the p^+ contacts for the top gate were patterned using *TGCON* mask followed by boron fluoride (BF_2) implantation at low energy (25 keV) and a dose of $5.5 \cdot 10^{14}$ atoms/cm². The boron fluoride was preferred because its ionic radii 87 pm is much bigger than that of boron ion (25 pm) which enables a much shallower penetration for the same implant energy [83]. Additionally, the total cross section for the ionization by electron impact is one of the essential data needed to be considered in selection of the species [84].

The impurities were electrically activated by an inert ambient (N_2) drive-in at 900 °C for 30 minutes. Again the drive-in time was very short and the temperature relatively low because it is necessary to have high concentration of boron at surface with minimal redistribution in depth.

The top gates with low doping profile were the last elements to be defined by lithography using mask *TG2DEP*. For the same reasons mentioned above, a BF_2 implantation was employed at different energies (40 & 48 keV) and doses ($8 \cdot 10^{11}$ atoms/cm² & $2.5 \cdot 10^{11}$ atoms/cm²) for different wafers. The resultant peak concentration is presented in the table 5.2 for the wafers that finalize the whole fabrication process. The final top junction depth will depend on the thermal budget of the following steps that should be minimized. Therefore, all subsequent anneal treatments were carried out at temperatures of 900 °C or below.

After an inert ambient (N_2) drive-in at 900 °C for 30 minutes, the oxide was striped and a thin layer of high quality oxide of 100 Å was grown in a dry O_2 ambient. This oxide serving a triple purpose: first, it provides a good top surface of the device, secondly, it is an insulator, and thirdly, it also acts as the first layer in the antireflection (AR) coatings designed for these devices. Next, silicon nitride layers were deposited by Low Pressure Chemical Vapor Deposition (LPCVD) with different thicknesses on each wafer (280 Å & 400 Å). Silicon nitride is optically transparent and mechanically very strong.

The last layer of the AR coating is a layer about 1350 Å of UD-TEOS (Undoped Tetraethyl Orthosilicate) SiO_2 deposited on the wafer surface at about 700°C. TEOS is a gaseous compound that thermally decomposes at around 700 °C to form silicon dioxide (SiO_2). The different crystalline structure of this oxide will lower the temperature at which the glass (oxide) starts to flow from 950 °C to 500 °C. This makes this oxide a very good material for surface planarization.

This oxide cannot be formed using wet oxidation because it has to be deposited on the top of the silicon nitride. Even if it could be thermally grown, such a step would be

undesired as it would need a long thermal processing time (high thermal budget) and this would affect the junction depths, especially the critical shallow p^+ region (*TOP GATE*). Moreover, the thick oxide may “suck” away the boron (oxide tends to take up boron away from the silicon surface) and create a significant dip in the boron surface concentration [85]. This oxide will serve also as the isolation layer in which the contact holes will be opened later.

Dry annealing is carried out at 850°C for 10 minutes to densify the UD-TEOS layer. Moreover, this step will also densify the previously deposited thin oxide layer.

Before the CONTACT mask patterning, the backside of the wafers was cleaned in a buffered oxide etch (BOE) solution.

Subsequently, contact holes were formed by dry etch in the oxide–nitride–oxide stack and a typical aluminum alloy for CMOS process Ti/TiN/AlSiCu (100/300/3500 Å) was subsequently deposited (by RF–sputtering) and patterned (mask METAL1) to create the bond pads and the metal interconnection for the top gates, source and drain.

After the metal etch, the presence of partially removed layers was noticed on some of the wafers, as shown in Fig. 5.3. The standard RCA cleaning process was not successful in the removal of this layer and three wafers were broken. Further investigations were not carried out since this layer was present only outside the illuminated area and thus it would not create any problems for the normal operation of the photosensitive devices. For this reason, the fabrication process was continued for the rest of the wafers.

A 0.5 μm thick oxide was deposited to insulate the previous Al layer from the subsequent second metal layer (to be done in the next step). This layer was deposited by PECVD because of the low deposition temperature (420 °C). Using the VIA mask, the oxide on the top of metal was removed to form via that would connect the first metal to the pads.

Subsequently, a second aluminum layer 2000 Å thick was sputtered and patterned (mask METAL2). The function of this layer is multiple; first, the pads are created in this layer. Secondly, the layer also acts as a light shield covering the photosensitive area of the “dark” photo–JFET’s, preventing their illumination. The thickness of the layer is smaller than that of standard Al (1.6 μm) in order to reduce the large tensile stress of the typical aluminum layer.

As with the first layer of metal, the 2nd aluminum layer was also patterned using a dry Reactive Ion Etch (RIE) process with high anisotropy to obtain vertical side walls.

An alloy step (sintering of the aluminum/silicon) took place at 425 °C for 25 minutes.

Next, a layer of UDTEOS oxide was deposited on the top layer with double scope: to protect the wafer surface against the influence of humidity and to create a flat and smooth surface.

Finally, the oxide on the top of bonding pads was removed to enable electrical contact (mask PAD) and to create the windows for the illuminated area (mask DesignF). The last step is backside metal deposition by evaporation of a 1 μm thick aluminum layer.

No more than 7 wafers completed the whole process and after final checking one of them had the second mask (DCON mask) misaligned, as it can be seen in Fig.5.4.

Fig. 5.3. The presence of partially removed layers on the surface of the wafers after the metal etches.

Fig. 5.4. The misalignment in wafer 2 after the completion of the process (magnification of microscope $\times 100$)

5.5. Conclusion

This chapter provided an overview on the fabrication of the JFET-based color sensors using a CMOS-compatible process. The first part briefly introduced the basic microfabrication steps, highlighting the CMOS process sequence and the focus of the second part is on adjustment of well-established CMOS technologies to fit the JFET-based color sensors process steps. The last part mentions few of the problems faced during the manufacture.

From a manufacturing point of view, the JFET-based color sensors process can be completed in a dedicated CMOS foundry and, constrained only by fabrication, are likely to benefit from this by enabling the realization of pixels in color-small size sensing arrays.

Chapter SIX: Optical and electrical measurements of JFET–Color Sensor

6.1. Introduction.

Electrical and spectral measurements have been performed in order to assess the efficiency of the JFET–based color sensor for color detection. In this chapter the measurement methods and results are presented along with a comparison with standard single junction photo-diode measurements.

6.2. Dark current measurements

Understanding the measurements of the electrical characteristics of the JFET–based color sensor is quite straightforward since we already mentioned the important parameters for the device in Chapter 3.

Before presenting the results, it is necessary to highlight again that the pinch–off voltage and its corresponding current are among the most important device parameters as presented in Tables 5.1 and 5.2. These theoretical values deduced using equations (3.4a and 3.4b) are summarized in Fig. 6.1.

Another aspect that needed to be addressed is that the dependence of the pinch–off intensity I_p on the ratio of the width of the device to device length is not linear, as it can be seen in Fig. 6.2. Therefore, the real value of pinch–off intensity that will be extracted later from measurements for each device on each wafer will be different from the theoretical values presented in Fig. 6.1. This difference appear from the theoretical consideration used to attain the electrical characteristics of device, mainly from consideration of a cross sectional (two dimensional plan) while the real device is three dimensional and depending on the device shape (Fig. 3.1 a & b) the pinch–off along the Z

direction does not occurs in the same time with pinch-off point denoted by P in Fig. 3.1 a & b.

The measurement setup for electrical characteristics comprised a HP semiconductor analyzer 4155B, which was also employed in the measurement of photocurrents generated under illumination, and was connected through four cables (Medium Power Source Monitor Units–MPSMU) to a probe station. The use of MPSMU cable is important for two reasons:

1. These are coaxial cables that reduce the leakage current caused by normal connection cables;
2. To reduce measurement errors caused by line frequency noise or any environmental noise source HP4155B takes a number of measurement samples and averages them to obtain one measurement point. The number of measurement samples taken during each measurement depends on the integration time. Setting a longer integration time increases the number of measurement samples, resulting in more accurate measurement data. The medium integration time depends on the power line cycle—in our case the power cycle line (PLC) is 50 Hz—hence, the medium integration time is 20 ms. However, the integration time also depends on the measurement range which depends on the type of the cable used. Therefore, the real integration time is given by measurement range, i.e. for measurement range of nanoamperes the integration time is $5 \text{ PLC} = 100 \text{ ms}$; for measurement range of hundred of picoamperes the integration time is $10 \text{ PLC} = 200 \text{ ms}$; for measurement range of tens of picoamperes the integration time is $50 \text{ PLC} = 1 \text{ s}$ [93].

Since this setup for electrical measurements was just a part of the larger setup used later for spectral measurements, the detailed structure will be presented later, in Fig. 6.22.

Fig. 6.1. The theoretical variation of the pinch-off current I_p as a function of the pinch-off voltage V_p for all the fabricated wafers.

Fig. 6.2. The theoretical dependence of pinch-off current I_p on the channel width/length ratio of a JFET - based color sensor.

6.2.1. I–V characteristics of real p – n diodes

The forward biased I–V characteristics of real p – n diodes are further affected by high injection and the series resistance of the diode. To illustrate these effects while summarizing the current mechanisms discussed previously let's consider a silicon p^+-n diode with $N_D = 1 \times 10^{15} \text{ cm}^{-3}$, $\tau_p = 10 \text{ } \mu\text{s}$, and $\mu_p = 450 \text{ cm}^2/\text{V}\cdot\text{s}$. The theoretical I–V characteristic of this diode in forward bias is shown in Fig. 6.3 on a semi-logarithmic scale and four different regions can be distinguished. The first region, for the very small forward bias, is dominated by the trap-assisted recombination in the depletion region, and has an ideality factor $\eta_1=2$ (the ideality factor is defined below; the subscripts refers to the number identifying the region). Secondly, the most important region of interest is the ideal diode region where the current increases by one order of magnitude as the voltage is increased by 55 mV. This region is referred to as having an ideality factor η of value equal with one ($\eta_2=1$). This ideality factor is obtained by fitting a section of the curve to the following expression for the current:

$$I_F = I_o \cdot e^{\frac{V_a}{\eta V_F}} \quad (6.1)$$

The ideality factor can also be obtained from the slope of the curve on a semi-logarithmic scale using:

$$\eta = \frac{\log(e)}{V_F \cdot m} = \frac{1}{54.6 \text{ mV/decade}} \quad (6.2)$$

where m is the slope in units of V/decade [80].

High injection occurs in a forward biased p – n diode when the injected minority carrier density exceeds the doping density. High injection will therefore occur first in the low doped region of the diode since that region has the highest minority carrier density.

Using the classical equation for the current characteristic in a diode and equation (6.1) the high injection occurs in a p^+-n diode for the following applied voltage:

$$V_a = 2V_F \ln\left(\frac{N_D}{n_i}\right) \quad (6.3)$$

Applying this equation for the practical diode example given previously results in a value $V_a = 0.55 \text{ V}$, which can be verified in Fig. 6.3 as the voltage where the ideality factor value changes from one to two. Finally, to the right of the ideal diode region, the current becomes limited by high injection effects and by the series resistance. In this region the current no longer increases exponentially with voltage. Instead, it increases

linearly due to the series resistance of the diode. This series resistance can be due to the contact resistance between the metal and the semiconductor, due to the resistivity of the semiconductor or due to the series resistance of the connecting wires. This series resistance can also be obtained from a transformed equation of the forward bias I-V curve plotted on a linear scale:

$$R_s = \frac{V_a}{I} \quad (6.4)$$

where I is the diode current and R_s is the series resistance.

These four regions can be observed in most $p-n$ diodes although the high-injection region rarely occurs, as the series resistance tends to limit the current first.

Fig. 6.3. The theoretical I-V characteristic of a forward biased diode.

Although the forward bias part of the I-V characteristics of a $p-n$ junction can provide vital information about that junction quality and its key features, the reverse bias portion is much more important for the practical application of the color sensors. This is due to the fact that photodiodes do not usually work in forward bias and an applied reverse bias can widen the depletion region and thus allow more photogenerated carriers to be collected under illumination. This results in a higher sensitivity of the device as well

as an altered spectral responsivity as compared to that obtained under short-circuit conditions. The maximum reverse bias value which can be applied on each junction theoretically can be limited by three major factors: junction breakdown, depletion region reach-through and distortion of the optimal spectral responsivity.

If a sufficiently large reverse bias is applied junction breakdown occurs, i.e. the p - n junction will conduct a very large reverse current due to avalanche generation of carriers. For our devices, a too low junction breakdown voltage would have only negative effects on the device, as the large reverse currents may recombine with the generated photocurrents, and would make the accurate extraction of the photocurrents impossible. The breakdown voltages for both junctions of the JFET sensors simulated are higher than 200 V, for the bottom junction and 50V, respectively for the top junction.

6.2.2. Measurement of I–V characteristics of the p - n junctions

I–V characteristics for each junction of the JFET-based color sensors were first tested on 5 dies on each fabricated wafer in the beginning for device D02. The average values resulted from forward and reverse bias measurements for each junction are shown in Fig.6.4 and 6.6 for wafer 1, Fig.6.8 and 6.10 for wafer 4, Fig.6.12 and 6.14 for wafer 5, and Fig.6.16 for wafer 13. The four typical regions in the I–V characteristics of each forward biased junction were identified and then the parameters of interest for each typical region were extracted from the curves plotted in log-log graphics shown in Fig.6.5 and 6.7 for wafer 1, Fig.6.9 and 6.11 for wafer 4, Fig.6.13 and 6.15 for wafer 5, and Fig.6.17 for wafer 13. It is necessary to remind the reader that wafers 1,4,5 and 13 have different values of channel width, channel doping concentration, and Top Gate doping concentration presented already in Table 5.2. The final extracted values for all the wafers are summarized in Table 6.1.

It can be seen that, for both junctions, the saturation current I_0 is larger for the top junction than for bottom one, for almost all wafers. This because I_0 is inversely proportional to the doping concentrations of the neutral regions of each junction which decrease gradually from the top to the bottom junction, while the other parameters (junction area, minority carriers diffusion coefficients) have insignificant changes and influence on I_0 . Except for W4–bottom, W5–bottom and W13–bottom, the value of the ideality factor η_1 is larger than 1 (close to 2) in the generation-recombination region (Region 1 in Table 6.1) than that for the “ideal” diffusion current region (Region 2 in Table 6.1) where the ideality factor η_2 is close to 1. Moreover, the values of η for the top junctions are larger than those for the bottom junctions. These differences arise from the

manufacture of each junction. The bottom junction was realized by epitaxial growth which means uniform doping concentration without surface defects while the top junction was realized by ion implantation implying the possible existence of a gradient in doping concentration, therefore affecting the abruptness of junction, and surface defects from implantation damage.

As mentioned previously, in the high-injection region (Region3 in Table 6.1), the values of η should be higher than 2, because the injected minority carrier density exceeds the doping density, and makes the injected current dominate this region. However, except for the top junction of W1, the values of η_3 for wafers 4, 5 and 13 are smaller than 2 because of the smaller minority diffusion currents caused by the higher doping concentration of the top gate.

The series resistance dominating the last region (Region4 in Table 6.1), increases from the top to bottom junction as it is inversely proportional to the doping concentration of the channel and direct proportional to the thickness of the doped layer.

Table 6.1. Values of the parameter characteristics for the forward bias I–V curves for each junction of JFET–based color sensor.

Nr.	Wafer number	Junction	I_0 [A]	V_0 [V]	Reg. 1 η_1	Reg. 2 η_2	Reg. 3 η_3	Reg. 4 R_s [Ω]
1	W1	top	$2.27 \cdot 10^{-7}$	0.60	1.71	1.07	3.09	20
		bottom	$1.25 \cdot 10^{-10}$	0.60	1.53	0.81	2.90	155.91
2	W4	top	$3.6 \cdot 10^{-7}$	0.80	2.5	1.62	4.6	17
		bottom	$1.768 \cdot 10^{-2}$	0.55	0.40	1.04	1.78	29.96
3	W5	top	$7.71 \cdot 10^{-9}$	0.60	2.65	0.42	1.27	24.40
		bottom	$1.98 \cdot 10^{-5}$	0.60	1.08	1.57	1.27	107.35
4	W13	top	–	–	–	–	–	–
		bottom	$3.88 \cdot 10^{-6}$	0.60	0.93	1.07	1.68	500

Fig. 6.4. The measured I–V characteristics for the bottom gate junction of JFET–based color sensing device 2 on wafer 1 in the absence of light.

Fig. 6.5. The logarithmic forward bias I–V characteristics for bottom gate junction of device 2 on wafer 1 with the delimited values for the four regions and their corresponding ideality factors.

Fig. 6.6. The measured I-V characteristics for the top gate junction of JFET-based color sensing device 2 on wafer 1 in the absence of light.

Fig. 6.7. The logarithmic representation of the forward bias portion of the I-V characteristic presented in Fig. 6.6, with the delimited values for the four regions and their corresponding ideality factors.

Fig. 6.8. The measured I-V characteristic for the bottom gate junction of JFET-based color sensing device 2 on wafer 4 in the absence of light .

Fig. 6.9. The logarithmic representation of the forward bias portion of the I-V characteristic presented in Fig. 6.8, with the delimited values for the four regions and their corresponding ideality factors.

Fig. 6.10. The measured I-V characteristics for the top gate junction of JFET-based color sensing device 2 on wafer 4 in the absence of light.

Fig. 6.11. The logarithmic representation of the forward bias portion of the I-V characteristic presented in Fig. 6.10, with the delimited values for the four regions and their corresponding ideality factors.

Fig. 6.12. The measured I–V characteristics for the bottom gate junction of JFET–based color sensing device 2 on wafer 5 in the absence of light.

Fig. 6.13. The logarithmic representation of the forward bias portion of the I–V characteristic presented in Fig. 6.12, with the delimited values for the four regions and their corresponding ideality factors.

Fig. 6.14. The measured I–V characteristics for the top gate junction of JFET–based color sensing device 2 on wafer 5 in the absence of light.

Fig. 6.15. The logarithmic representation of the forward bias portion of the I–V characteristic presented in Fig. 6.14, with the delimited values for the four regions and their corresponding ideality factors.

Fig. 6.16. The measured I–V characteristics for the bottom gate junction of JFET–based color sensing device 2 on wafer 13 in the absence of light.

Fig. 6.17. The logarithmic representation of the forward bias portion of the I–V characteristic presented in Fig. 6.16, with the delimited values for the four regions and their corresponding ideality factors.

6.2.3. The dark current measurements for JFET

The dark currents of the three junctions of the fabricated color sensors were measured using a 4-probe station enclosed in a metallic casing with a hood. The probes were connected directly to the above mentioned semiconductor analyzer HP 4155B.

The results obtained under zero and reverse bias applied only on the top gate are shown for each wafer in Fig. 6.18 (W1), 6.19 (W4), 6.20 (W5), 6.21 (W9) and 6.22 (W13). It can be seen that, as expected, the dark drain current is higher under zero bias than that obtained when the top gate is reverse biased. The measured values for the pinch-off current are higher than the calculated ones while the measured pinch-off voltages were lower than the calculated ones. This could be due to two reasons: a higher width to device length ratio (W/L) and a larger value of the device that the gate length in the real device, in contrast with the theoretical calculation in which was consider that the device length is equal with the gate length. A small theoretical variation in the channel depth ($0.2 \mu\text{m}$ in Fig.4.8) determines the pinch-off current I_P to increase (with 0.4 mA in Fig.4.8) and the pinch-off voltage V_P to decrease (with 1 V in Fig.4.8).

Fig. 6.18. The output characteristics for the JFET-based color sensing device 2 on wafer 1 measured in the absence of light.

Fig. 6.19. The output characteristics for the JFET-based color sensing device 2 on wafer 4 measured in absence of light.

Fig. 6.20. The output characteristics for the JFET-based color sensing device 2 on wafer 5 measured in the absence of light.

Fig. 6.24. The output characteristics for the JFET-based color sensing device 2 on wafer 9 measured in the absence of light.

Fig. 6.21. The output characteristics for the JFET-based color sensing device 2 on wafer 13 measured in the absence of light.

6.3. Spectral measurements of the JFET–based color sensor

6.3.1. The photocurrent generated under maximum white light microscope lamp illumination

In this case, a preliminary photosensitivity test was carried out by using the light source of the microscope in the probe station at its maximum emitted power which, measured with an optical power meter, is of 62 μW . The photogenerated currents of the drain junction of the fabricated JFET–based color sensor were measured again under zero bias and reverse bias, respectively. The obtained results are presented in Fig. 6.23 (W1), 6.24 (W4), 6.25 (W5) and 6.26 (W9), respectively, and they clearly show the significant enlargement of the current in the cases with illumination as compared to those without illumination and, furthermore, their values are different for each wafer corresponding to the diverse fabrication parameters specified already in Table 5.2.

However, the dark currents are significant under zero bias and can be directly measured. It is therefore not necessary to use any additional amplification for the collection of these currents. In addition, the dark currents strongly increase under reverse bias, when it may be more important to collect and extract efficiently the generated photocurrents.

The most sensitive device is the one on wafer 9, as this sensor exhibited the ratios of the photogenerated vs. dark currents much larger than of those devices on other wafers, probably due to low doping channel concentration and the antireflection layer.

The difference in the response for each device will allow a designer to choose how sensitive the device should be depending on the application desired. Silicon based color sensors already have widespread applications in science and industry, such as industrial automation, automotive systems, biomedicine, environmental monitoring and chemical analysis by optical absorption. Each of these applications has different requirements regarding the illumination source (low or high intensity), the sample measured (biological or material) and the output light (visual information received by color sensor).

The setup for the spectral responsivity measurement of the fabricated JFET–based color sensors shown in Fig.6.22, consisted of the following components:

- 1) A 10 W tungsten lamp, used as a white light source (quasi constant spectral output in the range 380 nm–800nm) powered from a low noise DC supply to avoid flicker;

2) This light source was fed through a calibrated monochromator to select the desired wavelength incident onto measured devices. This monochromator was under computer control via a GPIB bus;

3) A light guide coupled the light source to the monochromator, and a second one made the connection from the monochromator output to the probe station. This light guides ending tip was fixed in the probe station enclosure right above the measured chip. This beam of light illuminated either the JFET-based color sensor under test, or a reference Hamamatsu photodiode with which the incident power was measured at each wavelength. A microscope which was also inside the probe station enclosure would be used to locate the device (on the wafer) desired to be measured.

4) A semiconductor analyzer (HP 4155B) was connected to the probes of the probe station which were used to contact the corresponding bonding pads of the investigated junction and thus allow to measure the generated photocurrents as well as the dark currents. The sampling mode was used for HP 4151 in order to obtain 5 subsequent samples of photocurrents for each wavelength at different moments in time;

5) A PC to collect and process the measured data, control the monochromator as well as to extract and plot the spectral response curves for all the junctions.

6) An optical power meter was also used to test the power of the microscope's light incident onto the measured device.

Fig. 6.22. The spectral responsivity measurement setup for the JFET-based color sensing

Fig. 6.23. Measured output characteristics for the JFET-based color sensing device 2 on wafer 1.

Fig. 6.24. Measured output characteristics for the JFET-based color sensing device 2 on wafer 4.

Fig. 6.25. Measured output characteristics for the JFET-based color sensing device 2 on wafer 5.

Fig. 6.25. Measured output characteristics for the JFET-based color sensing device 2 on wafer 9.

6.3.2. Spectral calibration using a reference photodiode

The calibration of the whole measurement system was made using a Hamamatsu photodiode 1226-44BQ, which can detect light in a range from UV to visible spectrum with suppressed IR sensitivity.

Fig. 6.26. The geometrical parameters of Hamamatsu diode series 1226-44BQ for UV to visible spectrum with suppressed IR sensitivity

■ General ratings / absolute maximum ratings															
Type No.	Dimensional outline/ Window material *	Package (mm)	Active area size (mm)	Effective active area (mm ²)	Absolute maximum ratings										
					Reverse voltage VR Max. (V)	Operating temperature Topr (°C)	Storage temperature Tstg (°C)								
S1226-44BQ	Q/Q	TO-5	3.6 × 3.6	13	5	-20 to +60	-55 to +80								
Q: quartz glass															
■ Electrical and optical characteristics (Typ. Ta=25 °C, unless otherwise noted)															
Type No.	Spectral response range λ (nm)	Peak sensitivity wavelength λ_p (nm)	Photo sensitivity S (A/W)			Short circuit current Isc 100 λ		Dark current ID VR=10 mV Max. (pA)	Temp. coefficient of ID TCID (times/°C)	Rise time tr VR=0 V RL=1 k Ω (μ s)	Terminal capacitance Ct VR=0 V f=10 kHz (pF)	Shunt resistance Rsh VR=10 mV (Ω)		NEP (W/Hz ^{1/2})	
			λ_p	200 nm		Min.	Typ.								
				Min.	Typ.										
S1226-44BQ	190 to 1000	720	0.36	0.10	0.12	0.34	4.4	5.9	10	1.12	1	380	1	10	3.6 × 10 ⁻¹⁵

Fig. 6.27. The electrical and optical parameters of Hamamatsu diode series 1226-44BQ

Excerpts from the photodiode's data sheets with its geometrical, electrical and optical parameters are presented in Figs.6.26, 6.27 and 6.28.

The spectral distribution of the light power incident onto the tested devices, as measured with this photodiode is shown in Fig.6.29. It can be seen that the incident light power spectrum was not as even as expected with a pronounced peak at 566.5 nm. This is probably caused by the poor spectral transmission losses of the 5 meters long light guide,

especially for very short wavelengths when its light absorption apparently is very significant.

Fig. 6.28. The spectral sensitivity of the reference Hamamatsu photodiode 1226-44BQ highlighting the visible spectrum.

Fig. 6.29. The spectral sensitivity of the light incident onto the tested color sensors (i.e. at the end of the light guide coupled to the monochromator output) measured with Hamamatsu reference photodiode.

6.3.3. The photocurrents generated under visible light illumination

The spectral photocurrents curves obtained from measurements of the JFET-based color sensors on all the wafers are shown in Figs. 6.32 (W1), Fig.6.34 (W4), Fig.6.38 (W5), and Fig.6.40 (W13).

Fig.6.30 presents the channel I_D - V_D characteristics of the JFET-based color sensors on wafer 1 under illumination with monochromatic light namely Blue ($\lambda = 400$ nm), Green ($\lambda = 550$ nm) & Red ($\lambda = 680$ nm) light, respectively. The measurements were made separately for each illumination when the three contacts (Top Gate TG, Drain D and Bottom Gate BG) were in zero bias while the Source S was grounded. It can be seen that for each wavelength we have different values of the current and, as expected, the pinch-off voltage reduced from 15 V to 5 V. The characteristics have linear slope, therefore they enable the user to choose more suitable initial bias conditions, depending on the original requirements. All the spectral measurements were made in zero bias condition with the resulting currents in the microamperes range therefore it is possible to be necessary to amplify the signal. But one can choose another initial bias condition with the resulting currents in the miliamperes range that can be read it directly.

Fig.6.31 presents the spectral responses of the current collected at each terminal when the three contacts (Top Gate TG, Drain D and Bottom Gate BG) were in zero bias while the Source S was grounded. The photocurrents peaks are at 450 nm for I_{TG} , at 565 nm for I_D and at 625 nm for I_{BG} . The peaks for the same photocurrents measured for device 2 on the wafer 5 appear at approximately the same wavelength, namely like at 450 nm for I_{TG} , at 575 nm for I_D and at 650 nm for I_{BG} , as shown in Fig. 6.38. The variations are due to the difference by one order of magnitude in channel doping concentration (the channel doping for wafer 1 is lower than that of wafer 5) that can shift the position of peaks because of the different extension of the corresponding depleted regions.

Fig. 6.32 shows the variation of bottom gate's photocurrent with the applied drain voltage. There is a clear difference between the dark current, the photocurrent collected under green light illumination and that collected under red illumination, especially when $V_D > 5$ V. The photocurrent is linearly decreasing until the device is pinched-off after which the drain current is quasi-constant as a function of the drain voltage, provided that both the top and bottom gates are at zero bias voltage. The bottom gate photocurrent generated under blue light illumination has values very close to those of the dark current. This happens because at such short wavelength the absorption of this blue radiation takes place very close to the semiconductor surface and, consequently, the carriers

photogenerated by this phenomenon do not contribute to the current due to the carriers collected by the deeper bottom gate.

The peak value of I_D (under 0 bias) for the JFET-based color sensor device 2 on wafer 4 occurred at a much larger wavelength (580 nm instead of 500 nm, as shown in Fig. 6.34) because the channel of this device is wider (2 μm) than for the devices realized on other wafers (4.25 μm). Furthermore, the responses of the top and bottom gates are missing because the defective contact at the collection of data.

For wafer 5, it can be seen in Figs. 6.35–6.37 that the influence of the top depleted region can be increased by applying a reverse biasing on the top gate. This means that the top gate junction is much deeper than the simulated one. A lower quality of the antireflection layer could also influence negatively the output results. The AR layer was damaged while redoing a metal deposition and patterning step. This was necessary because, after metal was removed by plasma etching, it was found that the photoresist was partially striped on few areas wafer and the surface damaged. This accident happened as well for wafers 9 and 13 and caused the failure of several metal interconnections, sometimes for an entire wafer.

Fig. 6.30. The channel's measured photo-drain current of JFET-based color sensing device 2 for wafer 1 when illuminated with the primary three colors: Blue ($\lambda = 400$ nm), Green ($\lambda = 550$ nm) & Red ($\lambda = 680$ nm) under zero bias condition ($V_{TG} = V_{BG} = 0$ V)

Fig. 6.31. Measured spectral photocurrents curves for the JFET-based color sensor device 2 (wafer 1) under zero bias condition ($V_D = V_{TG} = V_{BG} = 0 \text{ V}$).

Fig. 6.32. The measured I - V characteristics for the bottom gate junction of JFET-based color sensing device 2 on wafer 4 when illuminated with: Green ($\lambda = 550 \text{ nm}$) & Red ($\lambda = 680 \text{ nm}$) under zero bias condition ($V_{TG} = V_{BG} = 0 \text{ V}$).

Fig. 6.33. The measured photo-drain current of JFET-based color sensing device 2 for wafer 4 for the primary three colors: Blue ($\lambda = 400$ nm), Green ($\lambda = 550$ nm) & Red ($\lambda = 680$ nm) under zero bias condition ($V_{TG} = V_{BG} = 0$ V)

Fig. 6.34. Measured spectral drain photocurrents for the JFET-based color sensor device 2 (wafer 4) under zero bias ($V_D = V_{TG} = V_{BG} = 0$ V F1-first data set, F2-second data set)

Fig. 6.35. The measured photo-drain current of the JFET-based color sensing device 2 on wafer 5 for the three primary colors: Blue ($\lambda = 400$ nm), Green ($\lambda = 550$ nm) & Red ($\lambda = 680$ nm).

Fig. 6.36. The measured photo-drain current of the JFET-based color sensing device 2 on wafer 5 illuminated by blue light ($\lambda = 430$ nm) when applying different reverse bias values on the top gate terminal.

Fig. 6.37 The measured photo-drain current of the JFET-based color sensing device 2 on wafer 5 illuminated by red light ($\lambda = 680$ nm) when applying different reverse biases on the top gate terminal.

Fig. 6.38. Measured spectral photocurrents curves for the JFET-based color sensor device 2 (wafer 5) under zero bias. The blue, green and red curves correspond to the photocurrents collected at top gate, drain and bottom gate, respectively with Source common.

Fig. 6.39. The measured I–V characteristics for the bottom gate junction of JFET–based color sensing device 2 on wafer 13 illuminated by blue light ($\lambda = 400$ nm) when applying different reverse biases on the top gate terminal.

Fig. 6.40. Measured spectral variation of the drain photocurrent for the JFET–based color sensor device 2 (wafer 13) under zero bias with common source

Fig. 6.41. Measured spectral variation of the top gate photocurrent for the JFET-based color sensor device 2 (wafer 13) under zero bias with common source

This is the reason why no measurements and spectral data could be obtained for wafer 9. This may also explain why the curves under blue illumination (even under reverse bias) appear like in fig 6.39, the characteristics are extremely similar. The peak shifts of the top gate's measured responses (fig 6.41) to green ($\lambda_{TG} = 475 \text{ nm}$) and that of the drain's measured responses (Fig. 6.40) to red ($\lambda_D = 590 \text{ nm}$) can both be explained only by assuming that the doping concentration of the epi-layer region of the channel has been severely modified, as compared to the initially designed values.

The photo-response of JFET-based color sensor device 2 on wafer 4 was compared with that obtained from the reference Hamamatsu photodiode and the spectral results are shown in Fig. 6.42 for two consecutive sets of measurements. However, it should be mentioned that the illuminated areas of device 2 (W4) and the reference photodiode are $\cong 0.14 \text{ mm}^2$ and 13 mm^2 , respectively, while the signal collected from device 2 (W4) at peak wavelength is more than double than that from the reference photodiode. In addition, the amplification of signal defined as ratio of measured photocurrents to corresponding dark currents profile for the JFET-based color sensor device 2 (wafer 4); respectively Hamamatsu photodiode are presented in Fig. 6.43, with

detailed profile for Hamamatsu in Fig. 6.44. The amplification for device 2 is 800-1000 while for Hamamatsu photodiode is 14.

Fig. 6.42. Measured spectral drain photocurrents curves for the JFET-based color sensor device 2 (wafer 4) in comparison with those of the reference Hamamatsu diode under zero bias (F1–first data set, F2–second data set)

Fig. 6.43. The ratio of measured drain photocurrents/dark currents versus wavelength for the JFET-based color sensor device 2 (wafer 4) and the Hamamatsu photodiode under zero bias (F1–first data set, F2–second data set)

Fig. 6.44. Blow-up of the ratio of measured drain photocurrents/dark currents profile for Hamamatsu diode under zero bias (F1–first data set , F2–second set data point) shown previously in Fig. 6.43

6.5. Conclusion

The RGB colorimetric system is a convenient way to describe color information, as it enables one to reconstruct back the color of light based on an additive color synthesis method. It is also a much more economical and easier method than a spectrometric approach.

Our silicon-based color sensor functions both as a filter and a detector simultaneously, using a JFET-based structure. Consequently, all the three R, G, B light hues are detected at the same time in the same location, eliminating the need for any polymer color filters. This allows a single pixel unit to provide full colorimetric information, thus saving precious chip area (which can be translated into greater resolution for a fixed area, or decreased area and cost for fixed resolution) while also avoiding the problem of color aliasing.

It is clear that the best performance was exhibited for wafer 5, when the peak values of the measured I_{blue} , I_{green} and I_{red} photocurrents occur at 450, 575 and 650 nm respectively. The peak value is largest for I_{green} followed by I_{red} and lastly I_{blue} . A

drawback of the device is sensitivity of top gate for blue is lower than that of drain and bottom gate for green and red, respectively.

The fact that the peak values for blue shift from 400 to 450 nm indicates that the top gate junction is deeper than the value simulated for all the wafers and the AR layers still need optimization. A low doping concentration of the channel (W9, W13) will provide a higher sensitivity at low intensity light in a device with a short channel width (W13). Also, doping concentration of the channel will conduct to a higher pinch-off voltage and current, therefore at a larger range of the linear region where the sensor can work in transistor mode.

Chapter SEVEN: Conclusion

7.1. Introduction.

The aim of this research presented in this thesis is to investigate the possibility of applying the wavelength dependence of the absorption coefficient in silicon for radiation in the visible part of the spectrum for color sensing. This effect is due to the indirect bandgap in silicon, which results in a large change in the momentum required for the generation of an electron-hole pair at energy of incident photons closer to the indirect bandgap at 1.12 eV. The absorption probability is related to the required change in momentum that has to be supplied by the lattice, resulting in a small absorption coefficient for long wavelength visible light and short penetration depth for short-wavelength. The immediate main aim is to design sensors capable to perform accurate color discrimination.

The JFET has been chosen because of following key features. First, it has no surface effects, such as interface traps occurring at the oxide–semiconductor interface. As a result, the noise level associated with the current fluctuation due to capture and release of free carriers at the surface is very low. Second, the isolated two gate terminals of JFET allow two different input signals to be applied simultaneously for signal-mixing purposes. Third, the carrier transport in JFET is made up predominantly by majority carriers, and thus the response speed of JFET is not limited by the minority carrier charge storage such in a bipolar transistor. It is a low–current device as seen from the simulations.

The basic model for the JFET–based color sensors was initially considered and further developed in the theoretical design, process and device simulations, and practical fabrication stages. Measurements of the fabricated JFET–based color sensor have been carried out. Moreover, in addition to this model, novel versions of the JFET–based color sensors have been introduced, characterized through TSUPREM and MEDICI simulations, and have been launched in fabrication. These new versions also constituted the bulk of a patent submission to NTU’s ITTO office.

The device design and realization of the JFET-based color sensors has been carried out in three stages. The first stage consisted of theoretical calculations in order to deduce how the light absorbed in the depletion regions (charge collection region) depended on each junction depth and its depletion width, which all in turn, depend on the type of semiconductor junction, doping concentration and the applied reverse bias voltage. MATLAB simulations were further developed to obtain the spectral response and optimize each sensing region such that the light absorbed at each region has almost the same peak value and dominates its respective color region.

For MATLAB simulations, the device has the channel with doping concentration $N_D = 10^{16} \text{ cm}^{-3}$, width $Z = 4 \text{ }\mu\text{m}$, half-depth $a = 2 \text{ }\mu\text{m}$, length $L = 12 \text{ }\mu\text{m}$, Source and Drain with doping concentration $N_A = 10^{18} \text{ cm}^{-3}$, Top Gate with junction depth of $x_{TG} = 0.08 \text{ }\mu\text{m}$ and doping concentration $N_{TG} = 4.5 \cdot 10^{16} \text{ cm}^{-3}$. For this device the spectral response has the peak values at 380, 550 and 700 nm.

The second stage comprised of the process (TSUPREM) and devices (MEDICI) simulations of the JFET-based color sensor. Using the previously designed parameters (junction depth, depletion width, doping concentration), the JFET-based color sensor structure was fabricated virtually on the workstation using TSUPREM IV. The processing steps were carefully designed to allow for a thermal budget as low as possible. The TSUPREM-IV fabricated color sensor was then exported to MEDICI, the device simulator. The proper light illumination and reverse biasing conditions were applied, and the photocurrents were obtained for the three primary colors.

The device has channel with doping concentration $N_D = 10^{16} \text{ cm}^{-3}$, half-depth $a = 4 \text{ }\mu\text{m}$; length $L = 80 \text{ }\mu\text{m}$, Top Gate with junction depth of $x_{TG} = 0.3 \text{ }\mu\text{m}$, doping concentration $N_{TG} = 1 \cdot 10^{17} \text{ cm}^{-3}$, Source and drain doping concentration $N_A = 4 \cdot 10^{19} \text{ cm}^{-3}$. For this device the spectral response has the peak values at 470, 543 and 640 nm.

Even we cannot make a comparison between MATLAB simulations and TCAD simulations because of differences in geometrical parameters of the device used we can conclude that the device used in MATLAB simulation gives us a better response.

The third stage was the actual implementation, using the $2 \text{ }\mu\text{m}$ n -well CMOS Process Flow of the MFL (Micro-Fabrication Laboratory) as a reference so that the process limits and capability could be met. All semiconductor regions were realized through photolithography, implantation and diffusion processes.

Finally, measurements on the fabricated devices were carried out. The colorimetric accuracy of the manufactured sensor is significantly worse than the

simulated approach. The best results are obtained on the wafer 5, with the peak values at 450, 575 and 650 nm. The fact that all peak values for blue are around 450 – 475 nm indicates that the top gate junction is deeper than the value simulated for all the wafers and the AR layer still need optimization. A low doped channel (W9, W13) will provide a higher sensitivity at low intensity light in a device with a short channel width (W13). Since we cannot make a comparison between measured devices and TCAD simulations because of differences in geometrical parameters of the device used we can see that the spectral result are similar the differences in spectral response being in range of 10 – 15 nm. The sensitivity of the present sensor is not a fundamental limitation of the approach *per se*, but rather a product of a non-optimized sensor design. It is likely that the non-uniformity problem can also be cured by altering the sensor layout.

7.2 Critical discussion of the current approach

This thesis has evaluated the performance of JFET-based color sensors fabricated with CMOS compatible process. Measurements on the fabricated devices showed that the color sensor exhibited color selectivity of acceptable quality, though not as good as the optimal color response. Nevertheless, the measurements clearly show that the concept is sound and it can be applied successfully for color detection, provided that care is taken during its practical implementation stage. The work in this project was also important because this proof-of-concept validation also highlighted problems that otherwise would not have been known had the work remained purely theoretical.

The project has covered the whole design and implementation of JFET-based color sensors and has also formulated a few new and original versions, which were included in a patent application.

The main advantages of the color sensors based on JFET-based structures are:

- Their operation is based on a colorimetric analysis of the incident light, which used decomposition in 3 basic primary colors (R, G and B). This RGB color system allows to describe uniquely the analyzed colorimetric information. It is also a convenient method since it enables one to retrieve the color of light based on additive color synthesis method, and therefore its translation into implementation in practical devices is much simpler than the alternative spectrometric method.
- The silicon-based JFET color sensors structure functions both as a filter and a detector simultaneously to the light in the visible range, eliminating the need for

polymeric color filters on 3 separate photodetectors for detection of the three primary colors (RGB). This would allow a more accurate colorimetric reading, as all the RGB signals are now provided from a single spatial location. This solution therefore saves up space and avoids the problem of color aliasing.

- Through suitable modification, the major process steps in a 2 μm CMOS process could be used to fabricate the JFET-based color sensors in this project.
- More novel versions, Device 4, Device 5 & Device 8, were designed based on the initial structure of the “classical” JFET-based color sensor, in order to ensure the simplicity of the fabrication process and enhance the color selectivity of the device.
- A further improvement is to employ a Junction Field Effect Transistor-based sensor, which can work in three operational modes: photoconductive (with Source and Gate shorted), photovoltaic, (i.e. as photodiode, with Source and Drain shorted) and as a phototransistor (with Gate biased, as a usual JFET).
- Another important advantage of a JFET-based sensor is that it can operate beyond the cutoff voltage V_{GC} , resulting in a photo-response independent of almost all the device parameters, including chip area, so that no loss performance occurs for very small area devices.

However, there were also some disadvantages:

- The colorimetric accuracy of the fabricated sensor was not as good as the optimal color response (theoretically designed), due to unexpected difficulties in the fabrication process.
- The unexpected processing failure (repeat patterning of first metal layer) of the classical version did not allow us to make comparisons between different types of sensors;
- The size of the color sensor is small enough to be suitable for image array applications with read-out circuits or it can be used as a monolithic stand-alone discrete device.
- The colorimetric accuracy is a function of the pn junction doping profile which is dependent on the technology, can be further optimized and accurately controlled only by increasing the process complexity. The disadvantages of the sensors investigated in this project would be addressed in the implementation of the next generation of color sensors.

The development of colorimetric sensors is important for any spectroscopic type of analysis in chemistry and biology, e.g. the characterization of bio/medical compounds/cells [86].

7.3 Applications

Silicon based color sensors already have widespread applications in science and industry, such as industrial automation, automotive systems, biomedicine, environmental monitoring and chemical analysis by optical absorption.

An example of a very useful colorimetric analysis in medical applications is that of the human blood for the detection of the quantity of hemoglobin present as shown in Fig. 7.1 [87], [88]. The characterization of powder mixtures in stirred tanks [89] (to determine the time necessary to obtain a homogeneous mixture) and color determination of ripeness of fruit or mixed paints are also other industrial applications where color sensors are necessary and useful. Therefore, the JFET-based color sensor could be employed in any application in which the analysis of the optical spectrum and/or the color is required.

Fig. 7.1 Spectral reflectance of human blood [87]

7.4. Future work

Future work should comprise an accurate modeling of the effects that affect the transmission of incident light and collection of the generated charge carriers, as well as

the wavelength dependences therein. This is necessary to enable better control on the effect of the various process and structural parameters on the device response.

An additional advantage of the silicon color-sensing principle is the compatibility with standard silicon processing, which makes possible the integration of the sensor with read-out circuits. Such a “smart” sensor will provide direct microprocessor-compatible output signals. Exploiting this capability is another task to be finalized in the future.

Consequently, more efforts should thus be oriented along these directions:

- 1) Calculate spectral and quantum efficiency for different structures,
- 2) Determine the colorimetric accuracy of dissimilar color sensor configurations,
- 3) Design the layout of the pixel array and associated circuitry.
- 4) Integrate the color sensing pixel together with its necessary interface read-out circuits in order to obtain a very good and compact imaging array [90]. In this later respect, the readout and reconstruction process can be simple, as it is no longer required to subtract one output from the other. This should also improve the noise performance slightly. However, the implementation of the circuits means that extra area must be dedicated for the color sensing part.
- 5) The design and fabrication of color sensors should be modified and applied in bio-related devices/applications. In particular, the color sensor introduced in this thesis can be integrated into a system of monitoring and chemical analysis by optical absorption, where it is used to obtain the colorimetric information of the samples, in order to analyze the characteristics of the sample before and after the bio/chemical reaction(s). Therefore, another aspect that we should considerate is the visual information received by color sensor in the form of the light reflected from the object and the light reflected from nearby objects. This interaction substantially changes the spectral composition and intensity of the reflected light. Brian A. Wandell and Shoji Tominaga developed a computational method to determine the components of the observed spectra, and an estimate of the illuminant without using a reference white standard [94]. B.A. Wandell and David H. Brainard also report the results of matching experiments designed to study the color appearance of objects rendered under different simulated illuminants on a CRT monitor [95]. These studies can be easily exploited as models in terms of visual mechanisms to further improve the sensitivity of the device as take in consideration the color appearance modeling.

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Invention Patent proposals:

1. D.P. Poenar, **M. Carp**, “Colour sensors based on (J)FET structures” – PCT application number: PAT-361-03-05-PCT. – AWARDED: Singapore Patent No.124472. It is still being processed in U.S.A. (Applic.No.: 60/544,496; Our PCT patent application number: PAT-361-03-05-PCT).

Conference Papers:

2. **M. Carp**, D. P. Poenar and R. S. Rama, “Novel Junction Field Effect-Based Colour Sensors”, paper JA-14-OR56, Symposium J, Materials for Advanced Sensors and Detectors, International Conference on Materials for Advanced Technologies ICMAT 2007, 1-6 July 2007, Singapore.

3. **M. Carp**, D.P. Poenar, and R.S. Rana, “Design & simulation of field-effect based color sensors”, paper 95-MDC-A0108, Section Mechanical and Physical Sensors, Asia-Pacific Conference of Transducers and Micro-nano Technology APCOT’06, 25-28 June 2005, Singapore.

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6. **M. Carp**, C. Iliescu, J.M. Miao F.E.H. Tay and D. P. Poenar, “Analyze of high boron doping from spin on diffusants source”, Proc. Thin Film 2004 and Nanotech 2004, pp. 170-171, Singapore, 13-17 July 2004.

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APPENDIX 1

Deduction of the Fundamental Equation of the JFET

Fig. A1.1. Fundamental structure of a classical n-channel JFET: a) Schematic cross-sectional view of a simple structure with top and bottom gates. The dashed line delimitates the actual operating area in the center of the structure. b) The device under study in this chapter and its main geometrical parameters.

Fig. A1.2. The upper half of the device considered in the calculation of I_{DS}

A field transistor is in essence a voltage controlled variable resistor. Varying the width of the depletion layer extending into channel can vary its resistance. The conduction process involves one type of carriers hence it is also called unipolar transistor.

Figure A1.1 is presents a JFET structure with an *n-channel* of length L , width Z and depth $2a$ (where a is the half-channel depth at zero bias and h is the depletion layer width).

In order to deduce the detailed current voltage characteristics for a JFET with an arbitrary charge distribution we consider now figureA1.2. Because of symmetry shown in figure A1.2 we need only consider the upper half of device where h is the depletion layer width at an arbitrary point and y_1 and y_2 are the width at Source and Drain, respectively.

The charge density is

$$Q(y) = \int_0^y \rho(y) dy \quad (\text{A1-1})$$

where $\rho(y)$ charge density in C/cm^3 .

The dependence of the reverse bias voltage V on h and $\rho(y)$ from Poisson's equation under the condition gradual-channel approximation, i.e. the depletion layer width h varies gradually along the channel (x -direction) is given by

$$-\frac{\partial^2 V}{\partial y^2} = \frac{\partial E}{\partial y} = \frac{\rho(y)}{\epsilon_s} \quad (\text{A1-2})$$

where E_y is electric field in the y direction and ϵ_s is the permittivity. Integration of the above equation from $y = 0$ to $y = h$ yields

$$E_y = -\frac{\partial V}{\partial y} = \frac{1}{\epsilon_s} \int_0^y \rho(y) dy + \text{const.} \quad (\text{A1-3})$$

The integration constant can be determined from the boundary condition that $E_y = 0$ at $y = h$ for an abrupt depletion layer and is obtainable from equation (A1-3) to be

$$-\frac{1}{\epsilon_s} \int_0^h \rho(y) dy.$$

From equation (A1-1-3):

$$\frac{\partial V}{\partial y} = \frac{1}{\epsilon_s} \left[\int_0^h \rho(y) dy + \int_0^y \rho(y) dy \right] = \frac{1}{\epsilon_s} [\varrho(h) - \varrho(y)] \quad (\text{A1-4})$$

Integrating once more from $y = 0$ to $y = h$ we obtain the voltage $V(h)$ across the depletion layer which include both the applied layer and the built-in voltages

$$V(h) = \frac{1}{\epsilon_s} \left[\varrho(h) \int_0^h dy - \int_0^h \varrho(y) dy \right] = \frac{1}{\epsilon_s} \left[h \cdot \varrho(h) - \int_0^h \varrho(y) dy \right] \quad (\text{A1-5})$$

Integrating by parts:

$$V(h) = \frac{1}{\epsilon_s} \int_0^h y \rho(y) dy \quad (\text{A1-6})$$

The maximum value for the upper limit of the integration occurs at the point where $h = a$ and the corresponding voltage is called the pinch-off voltage. Beyond this point the channel current remains essentially at a constant value. The pinch-off voltage is given by:

$$V_p = V(h = a) = \frac{1}{\epsilon_s} \int_0^a y \rho(y) dy \quad (\text{A1-7})$$

Differentiation of equation (A1-6) yields:

$$\frac{dV}{dh} = \frac{h \rho(h)}{\epsilon_s} \quad (\text{A1-8})$$

which shows that the voltage change required to move depletion region boundary a given distance, increases with the value of h and is proportional to the space-charge density at that boundary.

The junction capacitance per unit area is given by

$$C \equiv \frac{dQ(h)}{dV} = \left(\frac{dQ}{dh} \right) \left(\frac{dh}{dV} \right) \left[\frac{F}{cm^2} \right] \quad (\text{A1-9})$$

The depletion layer thus act as a plane capacitor with plate distance h and the capacitance is independent of charge profile.

The current density in the x -direction (transport along the channel) is given by the simple ohmic law equation, because $n \approx N_D$:

$$\vec{J} = q \mu_n n \vec{E} + q D_n \nabla n \Rightarrow J_x \cong \sigma(x) E_x \quad (\text{A1-10})$$

where J_x is current density, $\sigma(x)$ is the conductivity and E_x the electrical field along the x -direction ($-\partial V/\partial x$). The channel current is given by

$$I_D = 2Z\mu \cdot \frac{dV}{dx} \int_h^a \rho(y) dy \Rightarrow I_D dx = 2Z\mu \cdot \left(\frac{dV}{dh} \right) dh \cdot \int_h^a \rho(y) dy \quad (A1-11)$$

where μ_n is the drift mobility in the channel and factor 2 results from the added contribution of the lower half device. Substituting equation (A1-10) into (A1-11) and integrating with the boundary conditions $h = y_2$ at $x = L$ we obtain

$$I_D = \frac{2Z\mu}{\epsilon_s L} \int_{y_1}^{y_2} [Q(a) - Q(h)] h \rho(h) dh \quad (A1-12)$$

This is the fundamental and general equation for a JFET.

From equation (A1-12) we can derive two important device parameters namely the transconductance g_m and the channel conductance also called drain conductance g_D . The transconductance g_m is:

$$g_m \equiv \frac{\partial I_D}{\partial V_G} = \frac{\partial I_D}{\partial y_1} \cdot \frac{\partial y_1}{\partial V_G} + \frac{\partial I_D}{\partial y_2} \cdot \frac{\partial y_2}{\partial V_G} \quad (A1-13)$$

From equation (A1-8) $\frac{\partial V_G}{\partial y_1} = \frac{y_1 \rho(y_1)}{\epsilon_s}$ & $\frac{\partial V_G}{\partial y_2} = \frac{y_2 \rho(y_2)}{\epsilon_s}$ and from equation

(A1-13)

$$\begin{aligned} \frac{\partial I_D}{\partial y_1} &= \frac{\partial}{\partial y_1} \left\{ \frac{2Z\mu}{\epsilon_s L} \int_{y_1}^{y_2} [Q(a) - Q(h)] h \rho(h) dh \right\} \\ \frac{\partial I_D}{\partial y_2} &= \frac{\partial}{\partial y_2} \left\{ \frac{2Z\mu}{\epsilon_s L} \int_{y_1}^{y_2} [Q(a) - Q(h)] h \rho(h) dh \right\} \\ g_m &= \frac{2Z\mu}{L} [Q(y_2) - Q(y_1)] \end{aligned} \quad (A1-14)$$

which shows that g_m is equal to the conductance of the rectangular section of semiconductor extending from $y = y_1$ to $y = y_2$. The channel conductance results from (A1-8) and (A1-12):

$$g_D = \frac{\partial I_D}{\partial V_D} = \frac{2Z\mu}{L} [Q(a) - Q(y_1)] \quad (A1-15)$$

$g_D \rightarrow 0$ when $y_2 \approx a$ at which $V_D + V_G = V_P - V_{bi}$

For $V_D \rightarrow 0$, we have $y_2 \rightarrow y_1$ and g_D proportional to $[Q(a) - Q(y_1)]$. For any arbitrary charge distribution the following useful expression is obtained:

$$g_{D0} (V_D \rightarrow 0) = g_{ms} (|V_D| \gg |V_P|) = \frac{2Z\mu}{L} [Q(a) - Q(y_1)] = g_{\max} \left[1 - \frac{Q(y_1)}{Q(a)} \right] \quad (A1-16)$$

$$\text{where } g_{\max} = \frac{2Z\mu}{L} Q(a) \quad (\text{A1-17})$$

The above equation (A1-16) is particularly useful to derive the current-voltage characteristics for the case of a uniformly doped charge distribution. For a uniformly doped semiconductor n -type with doping N_D the function $Q(h)$ is given by $Q(h) = q \cdot N_D \cdot h$, so that

$$I_D = \frac{2Z \cdot \mu \cdot q^2 \cdot N_D^2}{\epsilon_s L} \left[\frac{a}{2} (y_2^2 - y_1^2) - \frac{1}{3} (y_2^3 - y_1^3) \right] \quad (\text{A1-18})$$

The depletion layer widths y_1 and y_2 for the top and bottom junctions, assumed to be abrupt, are given by

$$y_2 = \sqrt{\frac{2\epsilon_s (V_{bi} + V_G)}{qN_D}} \quad (\text{A1-19})$$

$$y_1 = \sqrt{\frac{2\epsilon_s (V_{bi} + V_G + V_D)}{qN_D}} \quad (\text{A1-20})$$

where $V_{bi} = \frac{kT}{q} \ln \left(\frac{N_A N_D}{n_i^2} \right)$ is the built-in potential for an abrupt junction, without using one step approximation

For a n -channel device $V_G < 0$ and $V_D > 0$, but we use the absolute value of V_G in all equations. Substitution of (A1-19) and (A1-20) in (A1-18) yields:

$$I_D = g_{\max} \cdot \left\{ V_D - \frac{2}{3a} \sqrt{\frac{2\epsilon_s}{q \cdot N_D}} \left[(V_D + V_G + V_{bi})^{3/2} - (V_G + V_{bi})^{3/2} \right] \right\} \quad (\text{A1-21})$$

where $g_{\max}$ is given by equation (A1-17).

The maximum current I_{Dsat} for a given V_G occurs at that point where the channel is pinched off and this current is obtainable from equation (A1-21):

$$I_{Dsat} = \frac{2Z\mu q^2 N_D^2 a^3}{6\epsilon_s L} \left(1 - 3 \frac{y_1^2}{a^2} + 2 \frac{y_1^3}{a^2} \right) \quad (\text{A1-22})$$

$$I_{Dsat} = I_P \cdot \left[1 - 3 \left(\frac{V_{bi} + V_G}{V_P} \right) + 2 \left(\frac{V_{bi} + V_G}{V_P} \right)^{3/2} \right]$$

where V_P and I_P are the pinch-off voltage and the pinch-of current which are given by

$$I_P = \frac{Z\mu q^2 N_D^2 a^3}{3\epsilon_s L} \quad (\text{A1-23a})$$

$$V_P = \frac{qN_D a^2}{2\epsilon_s} \quad (\text{A1-23b})$$

From equations (A1–23a) and (A1–23b) is clear that in order to increase I_P , one can employ device geometry with a large ratio (Z/L) , high mobility and low doping concentration in the channel. The last requirement comes about because of the fact that the depletion layer width at breakdown is approximately proportional to $(N_D)^{-1/2}$ and this makes the $N_A^2 a^3$ terms in I_P proportional to $(N_D)^{-1}$.

The saturation voltage is given by:

$$V_{Dsat} = V_P - V_{bi} - V_G = \frac{qN_A a^2}{2\epsilon_s} - \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) - V_G \quad (\text{A1-24})$$

The current–voltage characteristics for one value of V_G are sufficient to completely describe the device behavior for any channel impurity profile. Combining equation (A1–24) with equation (A1–12) the fundamental equation of JFET can be now rewritten as

$$I_D(V_G, V_D) = \int_{y_1}^{y_2} F(h) dh = \int_{y(V_G)}^{y(V_G+V_D)} F(h) dh \quad (\text{A1-25})$$

The integral can be split in two series to yield:

$$I_D(V_G, V_D) = \int_{y(0)}^{y(V_G+V_D)} F(h) dh + \int_{y(V_G)}^0 F(h) dh \quad (\text{A1-26a}) \quad \text{or}$$

$$I_G(V_G, V_D) = I_G(0, V_G + V_D) + I_G(0, V_G) \quad (\text{A1-26b})$$

Equation (A1–26a) states that if the relationship between I_D and V_G is known in the case $V_G = 0$, the right–hand side of equation (A1–26b) permits calculation of I_D for any combination of V_G and V_D .

APPENDIX 2

This analysis will deduce the detailed continuity relation for electrons in the neutral part of the channel states and which can be used for the all situation presented in Fig 3.7.:

$$D_n \frac{\partial^2 n_p(x)}{\partial x^2} - \frac{n_p - n_{p0}}{\tau_n} + I_o(\lambda)[1 - R(\lambda)]\eta\alpha(\lambda)e^{-\alpha(\lambda)x} - \frac{V_D}{L_{eff}} = 0 \quad (A2.1)$$

That can be rewritten as:

$$D_n \frac{\partial^2 n_p(x)}{\partial x^2} - \frac{n_p - n_{p0}}{\tau_n} = -I_o(\lambda)[1 - R(\lambda)]\eta\alpha(\lambda)e^{-\alpha(\lambda)x} + \frac{V_D}{L_{eff}} \quad (A2.1a)$$

$$\frac{\partial^2 n_p(x)}{\partial x^2} - \frac{n_p - n_{p0}}{L_n^2} = -\frac{I_o(\lambda)[1 - R(\lambda)]\eta\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)x} + \frac{V_D}{L_{eff}D_n} \quad (A2.1b)$$

The equation (A2.1b) is a second-order linear differential equation. It is nonhomogeneous because the right side is different of zero for all x under consideration.

If we substitute $y(x) = n_p(x) - n_{p0}$ the equation will become:

$$y'' - \frac{y}{L_n^2} = g(x) = -\frac{I_o(\lambda)[1 - R(\lambda)]\eta\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)x} + \frac{V_D}{L_{eff}D_n} \quad (A2.2)$$

The attached homogenous equation is

$$y'' - \frac{y}{L_n^2} = 0 \quad (A2.3)$$

For the nonhomogeneous equation (A2.2) a general solution can be written of the form:

$$y = y_h + y_p \quad (A2.4)$$

where y_h is a general solution of equation (A2.3) and y_p is any particular solution of equation (A2.2) (i.e. a solution given by two initial conditions).

We will use the method of undetermined coefficient (guessing method) to obtain the general solutions of the non-homogenous equation (A2.2) and this means that first we will acquire a particular solutions of the corresponding homogenous equation (A2.3)

where we substitute $y = e^{k \cdot x}$. This gives a solution if k is a root of the characteristic equation (A2.5).

$$k^2 - \frac{1}{L_n^2} = 0 \Rightarrow k_{1,2} = \pm \frac{1}{L_n} \quad (\text{A2.5})$$

Therefore, the general solution of (A2.3)

$$y_h(x) = C_1 e^{k_1 \cdot x} + C_2 e^{k_2 \cdot x} = C_1 e^{\frac{x}{L_n}} + C_2 e^{-\frac{x}{L_n}} \quad (\text{A2.6})$$

Applying the boundary conditions $y(x_{1J} + x_{1n}) = n_p(x_{1J} + x_{1n}) - n_{p0} = n_{p0} - n_{p0} = 0$
 $n_p(x_{2J} - x_{3n}) = 0$ and $y(x_{2J} - x_{3n}) = n_p(x_{2J} - x_{3n}) - n_{p0} = n_{p0} - n_{p0} = 0$ yields to subsequent values for the coefficients C_1 and C_2 :

$$\begin{aligned} y_h(x_{1J} + x_{1n}) &= C_1 e^{\frac{(x_{1J} + x_{1n})}{L_n}} + C_2 e^{-\frac{(x_{1J} + x_{1n})}{L_n}} = g(x_{1J} + x_{1n}) \Rightarrow \\ C_1 e^{\frac{(x_{1J} + x_{1n})}{L_n}} + C_2 e^{-\frac{(x_{1J} + x_{1n})}{L_n}} &= -\frac{I_o(\lambda)[1 - R(\lambda)]\eta\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{1J} + x_{1n})} + \frac{V_D}{L_{eff} D_n} \end{aligned} \quad (\text{A2.7a})$$

$$\begin{aligned} y_h(x_{2J} - x_{3n}) &= C_1 e^{\frac{(x_{2J} - x_{3n})}{L_n}} + C_2 e^{-\frac{(x_{2J} - x_{3n})}{L_n}} = g(x_{2J} - x_{3n}) \Rightarrow \\ C_1 e^{\frac{(x_{2J} - x_{3n})}{L_n}} + C_2 e^{-\frac{(x_{2J} - x_{3n})}{L_n}} &= -\frac{I_o(\lambda)[1 - R(\lambda)]\eta\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{2J} - x_{3n})} + \frac{V_D}{L_{eff} D_n} \\ C_1 &= e^{-\frac{(x_{1J} + x_{1n})}{L_n}} \cdot \left[-C_2 e^{\frac{(x_{1J} + x_{1n})}{L_n}} - \frac{I_o(\lambda)[1 - R(\lambda)]\eta\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{1J} + x_{1n})} + \frac{V_D}{L_{eff} D_n} \right] \Rightarrow \end{aligned} \quad (\text{A2.8})$$

$$\begin{aligned} C_1 &= e^{-\frac{(x_{1J} + x_{1n})}{L_n}} \cdot \left[-C_2 e^{\frac{(x_{1J} + x_{1n})}{L_n}} - \frac{I_o(\lambda)[1 - R(\lambda)]\eta\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{1J} + x_{1n})} + \frac{V_D}{L_{eff} D_n} \right] \Rightarrow \\ e^{-\frac{(x_{1J} + x_{1n})}{L_n}} \cdot \left[-C_2 e^{\frac{(x_{1J} + x_{1n})}{L_n}} - \frac{I_o(\lambda)[1 - R(\lambda)]\eta\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{1J} + x_{1n})} + \frac{V_D}{L_{eff} D_n} \right] &e^{\frac{(x_{2J} - x_{3n})}{L_n}} + \\ + C_2 e^{-\frac{(x_{2J} - x_{3n})}{L_n}} &= -\frac{I_o(\lambda)[1 - R(\lambda)]\eta\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{2J} - x_{3n})} + \frac{V_D}{L_{eff} D_n} \Rightarrow \end{aligned} \quad (\text{A2.9a})$$

$$\begin{aligned}
 C_2 e^{-\frac{(x_{2J}-x_{3n})}{L_n}} & \left(-e^{-\frac{2 \cdot (x_{1J}+x_{1n})}{L_n}} \cdot e^{\frac{2 \cdot (x_{2J}-x_{3n})}{L_n}} + 1 \right) = \\
 & = e^{-\frac{(x_{1J}+x_{1n})}{L_n}} e^{\frac{(x_{2J}-x_{3n})}{L_n}} \left[\frac{I_o(\lambda)[1-R(\lambda)]h\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{1J}+x_{1n})} - \frac{V_D}{L_{eff}D_n} \right] - \\
 & - \frac{I_o(\lambda)[1-R(\lambda)]h\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{2J}-x_{3n})} + \frac{V_D}{L_{eff}D_n} \Rightarrow
 \end{aligned} \tag{A2.9b}$$

$$\begin{aligned}
 C_2 e^{-\frac{(x_{2J}-x_{3n})}{L_n}} & \left(-e^{\frac{2(2a-x_{1n}-x_{3n})}{L_n}} + 1 \right) = \\
 & = e^{-\frac{(2a-x_{1n}-x_{3n})}{L_n}} \frac{I_o(\lambda)[1-R(\lambda)]h\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{1J}+x_{1n})} - e^{-\frac{(2a-x_{1n}-x_{3n})}{L_n}} \frac{V_D}{L_{eff}D_n} - \\
 & - \frac{I_o(\lambda)[1-R(\lambda)]h\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{2J}-x_{3n})} + \frac{V_D}{L_{eff}D_n} \Rightarrow
 \end{aligned}$$

$$\begin{aligned}
 C_2 e^{-\frac{(x_{2J}-x_{3n})}{L_n}} & \left(-e^{\frac{2(2a-x_{1n}-x_{3n})}{L_n}} + 1 \right) = \\
 & = \frac{I_o(\lambda)[1-R(\lambda)]h\alpha(\lambda)}{D_n} \left[e^{-\frac{(2a-x_{1n}-x_{3n})}{L_n}} e^{-\alpha(\lambda)(x_{1J}+x_{1n})} - e^{-\alpha(\lambda)(x_{2J}-x_{3n})} \right]
 \end{aligned}$$

$$\begin{aligned}
 C_2 & = \frac{e^{-\frac{(x_{2J}-x_{3n})}{L_n}}}{\left(-e^{-\frac{2(a-x_{1n}-x_{3n})}{L_n}} + 1 \right)} \cdot \left\{ \frac{I_o(\lambda)[1-R(\lambda)]h\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{1J}+x_{1n})} \cdot \left[e^{\frac{(a-x_{1n}-x_{3n})}{L_n}} - 1 \right] - \right. \\
 & \left. - \frac{V_D}{L_{eff}D_n} \cdot \left[e^{\frac{(a-x_{1n}-x_{3n})}{L_n}} - 1 \right] \right\} \Rightarrow \\
 C_2 & = e^{-\frac{(x_{2J}-x_{3n})}{L_n}} \cdot \frac{\left[e^{\frac{(a-x_{1n}-x_{3n})}{L_n}} - 1 \right]}{\left(-e^{-\frac{2(a-x_{1n}-x_{3n})}{L_n}} - 1 \right)} \cdot \left\{ \frac{I_o(\lambda)[1-R(\lambda)]h\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{1J}+x_{1n})} - \frac{V_D}{L_{eff}D_n} \right\}
 \end{aligned} \tag{A2.9c}$$

If we consider $e^{\frac{(a-x_{1n}-x_{3n})}{L_n}} = z$ then the ratio factor becomes:

$$\frac{\left[e^{\frac{(a-x_{1n}-x_{3n})}{L_n}} - 1 \right]}{-\left(e^{\frac{2(a-x_{1n}-x_{3n})}{L_n}} - 1 \right)} = \frac{z-1}{-(z^{-2}-1)} = \frac{z-1}{-\left(\frac{1}{z^2}-1\right)} = \frac{z-1}{\frac{(z^2-1)}{z^2}} = \frac{z^2(z-1)}{(z-1)(z+1)} = \frac{z^2}{z+1} =$$

$$= \frac{e^{\frac{2(a-x_{1n}-x_{3n})}{L_n}}}{\left(e^{\frac{(a-x_{1n}-x_{3n})}{L_n}} + 1 \right)}$$

And the coefficient of the second term in equation (A2.6) is:

$$C_2 = e^{-\frac{(x_{2J}-x_{3n})}{L_n}} \frac{e^{\frac{2(a-x_{1n}-x_{3n})}{L_n}}}{\left(e^{\frac{(a-x_{1n}-x_{3n})}{L_n}} + 1 \right)} \cdot \left\{ \frac{I_o(\lambda)[1-R(\lambda)]\eta\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{1J}+x_{1n})} - \frac{V_D}{L_{eff}D_n} \right\} \quad (A2.10)$$

Substituting (A2.10) in the equation (A2.8) we have:

$$C_1 = e^{-\frac{(x_{1J}+x_{1n})}{L_n}} \cdot \left\{ -e^{-\frac{(x_{2J}-x_{3n})}{L_n}} \frac{e^{\frac{2(a-x_{1n}-x_{3n})}{L_n}}}{\left(e^{\frac{(a-x_{1n}-x_{3n})}{L_n}} + 1 \right)} \cdot \left[\frac{I_o(\lambda)[1-R(\lambda)]\eta\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{1J}+x_{1n})} - \frac{V_D}{L_{eff}D_n} \right] - \right.$$

$$\left. - \frac{I_o(\lambda)[1-R(\lambda)]\eta\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{1J}+x_{1n})} + \frac{V_D}{L_{eff}D_n} \right\} \Rightarrow \quad (A2.11a)$$

$$C_1 = e^{-\frac{(x_{1J}+x_{1n})}{L_n}} \cdot \left[-e^{-\frac{(x_{2J}-x_{3n})}{L_n}} \frac{e^{\frac{2(a-x_{1n}-x_{3n})}{L_n}}}{\left(e^{\frac{(a-x_{1n}-x_{3n})}{L_n}} + 1 \right)} - 1 \right] \cdot \left[\frac{I_o(\lambda)[1-R(\lambda)]\eta\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{1J}+x_{1n})} - \frac{V_D}{L_{eff}D_n} \right]$$

Therefore the general solution $n_p(x)$ for $x_{1J} + x_{1n} < x < x_{2J} - x_{3n}$:

$$n_p(x) = \left[\frac{I_o(\lambda)[1-R(\lambda)]\eta\alpha(\lambda)}{D_n} e^{-\alpha(\lambda)(x_{1J}+x_{1n})} - \frac{V_D}{L_{eff}D_n} \right] \cdot$$

$$\left\{ e^{-\frac{(x_{1J}+x_{1n})}{L_n}} \cdot \left[-e^{-\frac{(x_{2J}-x_{3n})}{L_n}} \frac{e^{\frac{2(a-x_{1n}-x_{3n})}{L_n}}}{\left(e^{\frac{(a-x_{1n}-x_{3n})}{L_n}} + 1 \right)} - 1 \right] e^{\frac{x}{L_n}} + e^{-\frac{(x_{2J}-x_{3n})}{L_n}} \frac{e^{\frac{2(a-x_{1n}-x_{3n})}{L_n}}}{\left(e^{\frac{(a-x_{1n}-x_{3n})}{L_n}} + 1 \right)} \cdot e^{-\frac{x}{L_n}} \right\} \quad (A2.4)$$

$$\begin{aligned}
 p_n(x) = & \frac{I_o(\lambda)[1 - R(\lambda)]\eta\alpha(\lambda)}{D_p((1/L_p)^2 - \alpha(\lambda)^2)} \left\{ \frac{\exp\left[-\alpha(\lambda)(x_{2J} - x_{3n}) - \frac{(x_{2J} - x_{3n})}{L_p}\right]}{\exp\left[-2 \cdot \frac{(x_{1J} + x_{1n})}{L_p}\right] - \exp\left[-2 \cdot \frac{(x_{2J} - x_{3n})}{L_p}\right]} - \right. \\
 & - \frac{\exp\left[-\alpha(\lambda)(x_{1J} + x_{1n}) - \frac{(x_{1J} + x_{1n})}{L_p}\right]}{\exp\left[-2 \cdot \frac{(x_{1J} + x_{1n})}{L_p}\right] - \exp\left[-2 \cdot \frac{(x_{2J} - x_{3n})}{L_p}\right]} \times \exp\left(-\frac{x}{L_p}\right) + \\
 & + \frac{\exp\left[-\alpha(\lambda)(x_{2J} - x_{3n}) + \frac{(x_{2J} - x_{3n})}{L_p}\right] - \exp\left[-\alpha(\lambda)(x_{1J} + x_{1n}) + \frac{(x_{1J} + x_{1n})}{L_p}\right]}{\exp\left(2 \cdot \frac{(x_{1J} + x_{1n})}{L_p}\right) - \exp\left(2 \cdot \frac{(x_{2J} - x_{3n})}{L_p}\right)} \times \\
 & \times \exp\left(\frac{x}{L_p}\right) + \exp(-\alpha(\lambda)x) + \frac{V_D}{L_{eff}} x \Big\}
 \end{aligned}$$

APPENDIX 3

MicroFabrication Centre (MFC) Standard Job Submission Form
(please use this as the NTU Internal User Process Flow Request Form)

Job Owner	Alberta	MFC Job No		Job Priority	Normal
Staff/Student No.	C0144971R	Date Start	5-Jun-06	A/C Holder	Pooner David Puiu
Owner Contact No.		Date End		A/C Chargeable	
Approved Project No.					
		Mask Set		No of Mask Levels	1
Wafer Quality (Prime/2nd/Downy)	Prime	Wafer Orientation	<100>, <111>	Wafer Size (150 or 100 mm)	150
Wafer Type (p or n)	p-type	Resistivity (Ωcm)	0.01 - 0.1	New Wafer?	Y
Wafer Doping (B, P, As)	B	No. of Wafers	14	Wafer Supplier	NTU-MFL
Job Title					
JFET - based color sensor					
Brief Description of Job				No. of Process steps	64
				No. of Pages	20
Initiator:		Approved by A/C Holder:		Approved by Lab Manager:	
Alberta Corp		Pooner David		Ter Min Shi	

Step	Process	Process Description	Remark
0	Starting wafer	12 prime wafers <i>p</i> -type (B-doped), 0.01-0.1 Ω	Wafers 1-12 + 7 test wafers
1A	Epi substrate	5.5 μm	ONLY Wafers 1-3
1Aa	Preclean	PC1 clean	
1Ab	Epitaxy	Arsenic conc=5e15	
	Measure TEPI		
1B	Epi substrate	8.5 μm	ONLY Wafers 4-6
1Ba	Preclean	PC1 clean	
1Bb	Epitaxy	Arsenic conc=5e15	
	Measure TEPI		
1C	Epi substrate	5.5 μm	ONLY Wafers 7-9
1Ca	Preclean	PC1 clean	
1Cb	Epitaxy	Arsenic conc=1e15	
	Measure TEPI		
1D	Epi substrate	8.5 μm	ONLY Wafers 10-12
1Da	Preclean	PC1 clean	
1Db	Epitaxy	Arsenic conc=1e15	
	Measure TEPI		
1E	Epi substrate	8.5 μm	ONLY Wafers 13-14
1Ea	Preclean	PC1 clean	
1Eb	Epitaxy	Arsenic conc=1e14	
	Measure TEPI		
2	Initial oxide	Target: 300A	All wafers
2a	Preclean	PC1 clean	
2b	Furnace	A4	
	Recipe No. 410	950C, H ₂ /O ₂ , 9mins	
	Recipe Name: Wet Ox		
	Measure Tox		
3	LPCVD SiN	Target: 1650A	All wafers
	NITRIDE DEPOSITION	Spec: 1650 (+/-50) A Si ₃ N ₄	
	Pre-clean Bench --- WB-PC-1	Clean Process : PC1	
	- Insert one blank monitoring wafer	Monitoring Wafer must be pre-cleaned for furnace process	
	Furnace :	C2	
	Process Recipe :	220	
	LPCVD Silicon Nitride	DCS : 50 SCCM	
	Process Name : HS-Nitride	NH ₃ : 200 SCCM	
	Temperature : 785-790-800 C	Pressure : 300 mTorr	
		Dep Time : 45 Mins	
	Measure T _{SIN} (PW) 5 points		
	Measure T _{SIN} (TW) 5 points		
4	Litho-1	Mask layer:SDCON MASK A01	All wafers
4a	Coat Photoresist	AIO Photoresist Track	

	Coat Track Process Program : <u>1.1</u>	S1813, 1.23 um, 110C, 60sec	
4b	Align/Expose:	System :	
		UV Intensity : mW/cm2	
		Exposure Time : sec	
4c	Develop Photoresist and hardbake	AIO Photoresist Track	
	Develop Track Process Program : <u>2.1</u>	Develop : SD-W, 1 puddle, 60sec	
		Hardbake : 120C, 120sec	
4d	Inspect and measure Critical Dimension(CD)	Canon Microscope (Spec CD = 30.00 μ m)	
	DI- CD= 5 locations		
5	SiN etch		All wafers
5a	O2 Plasma Descum	Note Etch Condition:	
	Etcher	LAM 02 ??	
	Recipe Name :	Oxide Etch ??	
	Recipe No.: 999	Etch Mode: PE/Top	
		RF Power : 200 W	
		O2 : 20 sccm	
		Pressure : 100 mTorr	
		Elect Gap : 1.5 cm	
		Etch Time : 10 sec	
5b	SiN etch	LAM01	
	Recipe: Nit-1/no. 100	Pressure (mT):500	
		RF Power (W):250	
		Gap (cm):2	
		SF6 : 200 SCCM	
		O2 : 0 SCCM	
		He : 50 SCCM	
		Etch Time : EP 8% ($\approx$ 60 sec)	
	Measure T _{oxide} (PW) 5 points		
6	Measure T _{oxide} (TW) 5 points		
	NCONT IMPLANT	P-31, 110 keV. 7 degree, c/w 4 Quarter Imp	All wafers
	- implant Phosphorus to form the S & D	Dose : 3.0 E15	
7	PR strip	O2 Ashing : Endpoint + Over etch MK1-nanostrip: 60C, 10mins, QDR & SRD Dry	All wafers
8	Mark oxide	1700 A	All wafers
8a	Preclean	PC1 clean	
8b	Furnace	A4	
	Recipe No. 430	950C,O2, 5mins	
	Recipe Name:field ox	950C, H2/O2, ??? mins	
		950C,O2, 5mins	
		950C,N2, 10 mins	
	Measure Tox		
9	NITRIDE STRIP:		All wafers

9a	Clean wafer in Nanostrip	- Nanostrip clean :60°C, 10 min,	
		- QDR 6 cycles	
		- IPA Dry (or SRD Dry)	
9b	Oxynitride Etch	BOE dip: 10 sec	
	Bench : WB-MK-1	QDR 6 cycles	
9c	Nitride Etch	Reflux in H3PO4, 155C	
	Bench : WB-MK-1	Etch Time: about 45 min	
	- remove Nitride in Hot Phosphoric Acid	Hot DI Rinse-5 mins	
		Cascade Rinse --- to 15 MΩ	
	Measure Tox (Fox) =		
	Measure Tox(active) =		
10	Litho-2	Mask layer:DCON MASK B02	All wafers
10a	Coat Photoresist	AIO Photoresist Track	
	Coat Track Process Program : <u>1.1</u>	S1813, 1.23 um, 110C, 60sec	
10b	Align/Expose:	System :	
		UV Intensity : mW/cm2	
		Exposure Time : sec	
10c	Develop Photoresist and hardbake	AIO Photoresist Track	
	Develop Track Process Program : <u>2.1</u>	Develop : SD-W, 1 puddle, 60sec	
		Hardbake : 120C, 120sec	
10d	Inspect and measure Critical Dimension(CD)	Canon Microscope (Spec CD = 30.00 μm)	
	DI- CD= 5 locations		
11	PCONT IMPLANT	B-11, 30 keV. 7 degree, c/w 4 Quarter Imp Dose : 5.5 E14	All wafers
12	PR strip	O2 Ashing : Endpoint + Over etch MK1-nanostrip: 60C, 10mins, QDR & SRD Dry	All wafers
13	N P DRIVE-IN :		All wafers
13a	Preclean	PC1 clean	
13b	Furnace	A2 ?	
	Recipe no:210 ?	60 min, N2, 1100C	
14	Litho-3	Mask layer:PCHANNEL MASK C03	All wafers
14a	Coat Photoresist	AIO Photoresist Track	
	Coat Track Process Program : <u>1.1</u>	S1813, 1.23 um, 110C, 60sec	
14b	Align/Expose:	System :	
		UV Intensity : mW/cm2	
		Exposure Time : sec	
14c	Develop Photoresist and hardbake	AIO Photoresist Track	
	Develop Track Process Program : <u>2.1</u>	Develop : SD-W, 1 puddle, 60sec	
		Hardbake : 120C, 120sec	
14d	Inspect and measure Critical Dimension(CD)	Canon Microscope (Spec CD = 30.00 μm)	

	DI- CD= 5 locations		
15	PCHANNEL IMPLANT	B-11, 20KeV. 7 degree, c/w 4 Quarter Imp	All wafers
		Dose : 4E13	(THE VALUES of E & DOSE ARE NOT DEFINITIVE)
16	PR strip	O2 Ashing : Endpoint + Over etch MK1-nano-strip: 60C, 10mins, QDR & SRD Dry	All wafers
17	Pchannel DRIVE-IN :		All wafers
	Preclean	PC1 clean	
	Furnace	A2 ?	
	Recipe no:210 ?	60 min, N2, 1100C	
18	Litho-4	Mask layer:TGRING MASK D04	All wafers
18a	Coat Photoresist	AIO Photoresist Track	
	Coat Track Process Program : 1.1	S1813, 1.23 um, 110C, 60sec	
18b	Align/Expose:	System :	
		UV Intensity : mW/cm2	
		Exposure Time : sec	
18c	Develop Photoresist and hardbake	AIO Photoresist Track	
	Develop Track Process Program : 2.1	Develop : SD-W, 1 puddle, 60sec	
		Hardbake : 120C, 120sec	
18d	Inspect and measure Critical Dimension(CD)	Canon Microscope (Spec CD = 30.00 mm)	
	DI- CD= 5 locations		
19	TG & RINGS IMPLANT	B-11, 25 keV. 7 degree, c/w 4 Quarter Imp	All wafers
		Dose : 1 E15	
20	PR strip	O2 Ashing : Endpoint + Over etch MK1-nano-strip: 60C, 10mins, QDR & SRD Dry	All wafers
21	TG Anneal		All wafers
	Pre-clean Bench : WB-PC1	Clean Process : PC1	
	Furnace	B3	
	Recipe no: 733	5 min, N2, 900C	
	Recipe Name:anneal	25 min, N2, 900C	
22	Litho-5	Mask layer:NWELL MASK E05	All wafers
	Coat Photoresist	AIO Photoresist Track	
	Coat Track Process Program : 1.1	S1813, 1.23 um, 110C, 60sec	
	Align/Expose:	System :	
		UV Intensity : mW/cm2	
		Exposure Time : sec	
	Develop Photoresist and hardbake	AIO Photoresist Track	
	Develop Track Process Program : 2.1	Develop : SD-W, 1 puddle, 60sec	
		Hardbake : 120C, 120sec	
	Inspect and measure Critical Dimension(CD)	Canon Microscope (Spec CD = 30.00 mm)	

	DI- CD= 5 locations		
23	NWELL IMPLANT	P-31, 110 keV. 7 degree, c/w 4 Quarter Imp Dose : 3E15	All wafers
24	PR strip	O2 Ashing : Endpoint + Over etch MK1-nanostrip: 60C, 10mins, QDR & SRD Dry	All wafers
25	NWELL Anneal		All wafers
	Pre-clean Bench : WB-PC1	Clean Process : PC1	
	Furnace	B3	
	Recipe no: 733	5 min, N2, 900C	
	Recipe Name:anneal	25 min, N2, 900C	
26	NITRIDE DEPOSITION	Spec: 1650 (+/-50) A Si3N4	All wafers
26a	Preclean	PC1 clean	
	- Insert one blank monitoring wafer	Monitoring Wafer must be pre-cleaned for furnace process	
26b	LPCVD Silicon Nitride	DCS : 50 SCCM	
	Furnace : C2	NH3 : 200 SCCM	
	Process Recipe : 220	Pressure : 300 mTorr	
	Process Name : HS-Nitride	Dep Time : 45 Mins	
	Temperature : 785-790-800 C		
	Measure T _{SiN} (PW) 5 points		
	Measure T _{SiN} (TW) 5 points		
27	Litho-6	Mask layer:SDIMCON MASK F06	All wafers
	Coat Photoresist	AIO Photoresist Track	
	Coat Track Process Program : 1.1	S1813, 1.23 um, 110C, 60sec	
	Align/Expose:	System :	
		UV Intensity : mW/cm2	
		Exposure Time : sec	
	Develop Photoresist and hardbake	AIO Photoresist Track	
	Develop Track Process Program : 2.1	Develop : SD-W, 1 puddle, 60sec	
		Hardbake : 120C, 120sec	
	Inspect and measure Critical Dimension(CD)	Canon Microscope (Spec CD = 30.00 mm)	
	DI- CD= 5 locations		
28	SiN etch	LAM01	All wafers
	(ensure O2 descum step before etching)		
	Recipe: Nit-1/no. 100	Pressure (mT):500	
		RF Power (W):250	
		Gap (cm):2	
		SF6 : 200 SCCM	
		O2 : 0 SCCM	
		He : 50 SCCM	
		Etch Time : EP 8% (≈ 60 sec)	
29	N IMPLANT	As-75, 20 keV. 7 degree, c/w 4 Quarter Imp Dose : 3E15	All wafers (THE VALUES of E & DOSE ARE NOT DEFINITIVE)

	PR strip	O2 Ashing : Endpoint + Over etch MK1-nanostrip: 60C, 10mins, QDR & SRD Dry	All wafers
30	Mark oxide	1700 A	All wafers
	Preclean	PC1 clean	
	Furnace	A4	
	Recipe No. 430	950C,O2, 5mins	
	Recipe Name:field ox	950C, H2/O2, ??? mins	
		950C,O2, 5mins	
		950C,N2, 10 mins	
	Measure Tox		
31	NITRIDE STRIP:		All wafers
	Clean wafer in Nanostrip	- Nanostrip clean :60°C, 10 min,	
		- QDR 6 cycles	
		- IPA Dry (or SRD Dry)	
	Oxynitride Etch	BOE dip: 10 sec	
	Bench : WB-MK-1	QDR 6 cycles	
	Nitride Etch	Reflux in H3PO4, 155C	
	Bench : WB-MK-1	Etch Time: about 45 min	
	- remove Nitride in Hot Phosphoric Acid	Hot DI Rinse-5 mins	
		Cascade Rinse --- to 15 MΩ	
32	Litho-7	Mask layer:TGCON MASK G07	All wafers
	Coat Photoresist	AIO Photoresist Track	
	Coat Track Process Program : 1.1	S1813, 1.23 um, 110C, 60sec	
	Align/Expose:	System :	
		UV Intensity : mW/cm2	
		Exposure Time : sec	
	Develop Photoresist and hardbake	AIO Photoresist Track	
	Develop Track Process Program : 2.1	Develop : SD-W, 1 puddle, 60sec	
		Hardbake : 120C, 120sec	
	Inspect and measure Critical Dimension(CD)	Canon Microscope (Spec CD = 30.00 mm)	
	DI- CD= 5 locations		
33	PWELL IMPLANT	BF2-, 25 keV. 7 degree, c/w 4 Quarter Imp	All wafers
		Dose : 5.5E14	
34	PR strip	O2 Ashing : Endpoint + Over etch MK1-nanostrip: 60C, 10mins, QDR & SRD Dry	All wafers
35	PWELL Anneal		All wafers
	Pre-clean Bench : WB-PC1	Clean Process : PC1	
	Furnace	B3	
	Recipe no: 733	5 min, N2, 900C	
	Recipe Name:anneal	25 min, N2, 900C	
36	Litho-8	Mask layer:TG2DEP MASK H08	All wafers
	Coat Photoresist	AIO Photoresist Track	
	Coat Track Process Program : 1.1	S1813, 1.23 um, 110C, 60sec	
	Align/Expose:	System :	

		UV Intensity : mW/cm2	
		Exposure Time : sec	
	Develop Photoresist and hardbake	AIO Photoresist Track	
	Develop Track Process Program : 2.1	Develop : SD-W, 1 puddle, 60sec	
		Hardbake : 120C, 120sec	
	Inspect and measure Critical Dimension(CD)	Canon Microscope (Spec CD = 30.00 mm)	
	DI- CD= 5 locations		
37	TG1 IMPLANT	BF2-, 48 keV, 7 degree, c/w 4 Quarter Imp Dose : 2.5E12	All wafers (THE VALUES of E & DOSE ARE NOT DEFINITIVE)
38	PR strip	O2 Ashing : Endpoint + Over etch MK1-nanostrip: 60C, 10mins, QDR & SRD Dry	All wafers
39	TG1 Anneal		All wafers
	Pre-clean Bench : WB-PC1	Clean Process : PC1	
	Furnace	B3	
	Recipe no: 733	5 min, N2, 900C	
	Recipe Name:anneal	25 min, N2, 900C	
40	OXIDE STRIP (spec= 300 A)	Bench : WB-MK-1	All wafers
	Clean wafer in Nanostrip	- Nanostrip clean :60°C, 10 min, - QDR 6 cycles - IPA Dry (or SRD Dry)	
	Oxide etch in BOE	- BOE : 6:1 (about 6 mins)	
	Remove all oxide on wafer	Etch Time : Frontside dewet + 10 sec Overetch - Cascade rinse : DI water resistivity > 15 MΩ - IPA Dry (or SRD Dry)	
41A	Oxide for AR protection	150A (+/-5) A ???	ONLY Wafers 7,11 (THE VALUE Xox IS NOT DEFINITIVE)
	Preclean	PC1 clean	
	Furnace	A4	
	Recipe No. 410	950C, H2/O2, ??mins	
	Recipe Name: Wet Ox		
	Measure Tox		
41B	Oxide for AR	860 (+/-10) A	ONLY Wafers 1,2,3,4,6,9,10,12 NOT SURE YET WHICH WAFERS BUT ONLY 4 WAFERS
	Preclean	PC1 clean	
	Furnace	A4	
	Recipe No. 410	950C, H2/O2,	
	Recipe Name: Wet Ox		
	Measure Tox		
42A	NITRIDE DEPOSITION	Spec: 670 (+/-10) A Si3N4	ONLY Wafers 1,2,3,4,5,6,8,9,10,12
	Preclean	PC1 clean	

	- Insert one blank monitoring wafer	Monitoring Wafer must be pre-cleaned for furnace process	
	LPCVD Silicon Nitride	DCS : 50 SCCM	
	Furnace : C2	NH3 : 200 SCCM	
	Process Recipe : 220	Pressure : 300 mTorr	
	Process Name : HS-Nitride	Dep Time : 10 Mins	
	Temperature : 785-790-800 C	??	
	Measure T _{SiN} (PW) 5 points		
	Measure T _{SiN} (TW) 5 points		
42B	NITRIDE DEPOSITION	Spec: (+/-10) Å Si ₃ N ₄	ONLY Wafers 7,11
	Preclean	PC1 clean	
	- Insert one blank monitoring wafer	Monitoring Wafer must be pre-cleaned for furnace process	
	LPCVD Silicon Nitride	DCS : 50 SCCM	
	Furnace : C2	NH3 : 200 SCCM	
	Process Recipe : 220	Pressure : 300 mTorr	
	Process Name : HS-Nitride	Dep Time : 10 Mins	
	Temperature : 785-790-800 C	??	
	Measure T _{SiN} (PW) 5 points		
	Measure T _{SiN} (TW) 5 points		
43	TEOS DEPOSITION	UD-TEOS : 5000 (+/-150) Å	All wafers
	Pre-clean Bench --- WB-PC-1	Clean Process : PC1	
	LPCVD BP-TEOS		
	Furnace	C4	
	Process Recipe :	451	
	Process Name : UD-TEOS	(check dep rate in last cycle)	
	Layer 1: LPCVD UD-TEOS	UD-TEOS : 5000 (+/-150) Å	
	Temperature : 714-720-730	TEOS : 280 mG/min	
		Press : 300 mTorr	
		Dep. Time : » min ?	
	Measure T _{TEOS} (UD-TEOS)=		
44	TEOS DENSIFY	Target> = 5000 (+/- 50) Å on blank monitor wafer	All wafers
	Pre-clean Bench --- WB-PM-1	Clean Process : PC1	
	Include TEOS thickness monitoring wafers	** No HF dip	
	Monitoring Wafers must be pre-clean for thermal operation	No pre-clean if perform within 60 min after BP-TEOS deposition and stored in clean Teflon cassette	
44a	Wet Anneal at 850C :		
	Furnace/Process Recipe : B3/7 ?	30 min. H ₂ O, 850C	

	Process Name : Densify		
	Measure Tox(SD regions) =		
45	BACKSIDE ETCH	Removes backside films on the wafer	All wafers
	Coat Photoresist on wafer front surface	Coat Track Process Program : <u>1.1</u>	
	-- Protect front surface during backside etch	S1813, 1.23 um	
	Hard bake	Develop Track Process Program : <u>2.5</u>	
	Etch Backside TEOS	BOE 7:1 Etch : 4mins	
	Remove TEOS film on backside of wafer	Cascade Rinse --- to 12 MW	
	-- WB-MK-1	Spin Dry only	
46	PR strip	O2 Ashing : Endpoint + Over etch MK1-nanostrip: 60C, 10mins, QDR & SRD Dry	
47	Litho-9	Mask layer:CONTACT MASK I09	All wafers
	Coat Photoresist	AIO Photoresist Track	
	Coat Track Process Program : 1.1	S1813, 1.23 um, 110C, 60sec	
	Align/Expose:	System :	
		UV Intensity : mW/cm2	
		Exposure Time : sec	
	Develop Photoresist and hardbake	AIO Photoresist Track	
	Develop Track Process Program : 2.1	Develop : SD-W, 1 puddle, 60sec	
		Hardbake : 120C, 120sec	
	Inspect and measure Critical Dimension(CD)	Canon Microscope (Spec CD = 30.00 mm)	
	DI- CD= 5 locations		
48	CONTACT ETCH	Open contact holes for metal contact in TEOS(Etch: oxide:nitride:oxide)	All wafers
48a	O2 Plasma Descum	Note Etch Condition:	
	Etcher	LAM 02	
	Recipe Name :	Oxide Etch ??	
	Recipe No.: 999	Etch Mode: PE/Top	
		RF Power : 200 W	
		O2 : 20 sccm	
		Pressure : 100 mTorr	
		Elect Gap : 1.5 cm	
		Etch Time : 10 sec	
	Wet Contact Etch	BOE : 6:1 , Etch Time : <1 min	
	-- WB - MK-1	Cascade Rinse --- to 15 MΩ	
		Spin Dry only	
	Hard bake	Backing Oven	
		-- 120°C, 30 mins	
48b	Plasma Oxide etch (spec=5000A)	Etch Mode: plasma	
	Etcher	LAM 02	
	Recipe Name :	Oxide Etch	

	Recipe No:500	Step : Main	
	Overetch	RF Power : 550	
	200 W	Ar : 300 300	
	SCCM	CF4 20 20	
	SCCM	CHF3 : 45 45	
	SCCM	Pressure : 100 100	
	(Note : BPSG etch rate $\approx$ 4400Å/min)	mTorr	
	DO NOT overetch the contact	Elect Gap : 1.02	
		1.02 cm	
48c		Etch Time : $\approx$ 50 sec 50%	
		($\approx$ 75 sec)	
	Plasma Nitride Etch (spec=670 A)	Etch Mode: plasma	
	Etcher :	LAM 01	
	Recipe Name :	Nit-1	
	Recipe No.: 100	Step : Main	
	Overetch	RF Power : 250	
	250 W	SF6 : 200 200	
	SCCM	O2 : 0 0	
	SCCM	He : 50 50	
	(ensure O2 descum step before etching)	SCCM	
		Pressure : 500 500	
		mTorr	
		Elect Gap : 2.0	
		2.0 cm	
		Etch Time : EP	
		8% ($\approx$ 60 sec)	
	Measure Tox(active) =		
48d	Plasma Oxide etch (spec=300A) ?	Etch Mode: plasma	
	Etcher	LAM 02	
	Recipe Name :	Oxide Etch	
	Recipe No:	Step : Main	
	Overetch	RF Power : 550	
	200 W	Ar : 300 300	
	SCCM	CF4 20 20	
	SCCM	CHF3 : 45 45	
	SCCM	Pressure : 100 100	
	(Note : BPSG etch rate $\approx$ 4400Å/min)	mTorr	
	DO NOT overetch the contact	Elect Gap : 1.02	
		1.02 cm	
		Etch Time : $\approx$ 50 sec 50%	
		($\approx$ 75 sec)	

	Measure remaining oxide in contact region Tox (< 50A)	Ensure oxide in contact region is clear	
49	PR strip	O2 Ashing : Endpoint + Over etch MK1-nanostrip: 60C, 10mins, QDR & SRD Dry	All wafers
50	Metal Dep	Ti/TiN/Al=100A/300A/8500A	All wafers
	BPS sputter	BPS CL200	
	Recipe: 412 metal	Ti/TiN/AlSiCu =100/300/8500 A @ 375C	
51	Litho-10	Mask layer:METAL1 MASK J10	All wafers
	Coat Photoresist	AIO Photoresist Track	
	Coat Track Process Program : <u>1.1</u>	S1813, 1.23 um, 110C, 60sec	
	Align/Expose:	System :	
		UV Intensity : mW/cm2	
		Exposure Time : sec	
	Develop Photoresist and hardbake	AIO Photoresist Track	
	Develop Track Process Program : <u>2.1</u>	Develop : SD-W, 1 puddle, 60sec Hardbake : 120C, 120sec	
	Inspect and measure Critical Dimension(CD)	Canon Microscope (Spec CD = 30.00 μm)	
	DI- CD= 5 locations		
52	Metal etch	LAM03	All wafers
	Plasma etch: RIE mode	RF Power : 200 W	
		BC13 : 75 SCCM	
	Metal etch recipe: 800	Cl2 : 32 SCCM	
		N2 : 25 SCCM	
		Pressure : 275 mTorr	
		Elect Gap : 5.0 cm	
53	PR strip	O2 Ashing : Endpoint + Over etch MK2-ERS clean: 60C, 10mins, QDR & SRD Dry	All wafers
54	PECVD UDTEOS	Dep 5KA	All wafers
	P5000	420C	
	UDTEOS	TEOS	
		pressure	
	Measure Tox		
55	Litho-11	Mask layer:VIA MASK K11	All wafers
	Coat Photoresist	AIO Photoresist Track	
	Coat Track Process Program : <u>1.1</u>	S1813, 1.23 um, 110C, 60sec	
	Align/Expose:	System :	
		UV Intensity : mW/cm2	
		Exposure Time : sec	
	Develop Photoresist and hardbake	AIO Photoresist Track	
	Develop Track Process Program : <u>2.1</u>	Develop : SD-W, 1 puddle, 60sec Hardbake : 120C, 120sec	
	Inspect and measure Critical Dimension(CD)	Canon Microscope (Spec CD = 30.00 μm)	
	DI- CD= 5 locations		

56	VIA ETCH	Open contact holes for metal contact in UDTEOS(Etch: oxide)	All wafers
56a	O2 Plasma Descum	Note Etch Condition:	
	Etcher	LAM 02	
	Recipe Name :	Oxide Etch	
	Recipe No.: 999	Etch Mode: PE/Top	
		RF Power : 200 W	
		O2 : 20 sccm	
		Pressure : 100 mTorr	
		Elect Gap : 1.5 cm	
		Etch Time : 10 sec	
	Wet Contact Etch	BOE : 6:1 , Etch Time : <1 min	
	-- WB - MK-1	Cascade Rinse --- to 15 MΩ	
		Spin Dry only	
	Hard bake	Backing Oven	
		-- 120°C, 30 mins	
56b	Plasma Oxide etch (spec=5000A)	Etch Mode: plasma	
	Etcher	LAM 02	
	Recipe Name :	Oxide Etch	
	Recipe No:500	Step : Main Overetch	
		RF Power : 550 200 W	
		Ar : 300 300 SCCM	
		CF4 20 20 SCCM	
		CHF3 : 45 45 SCCM	
	(Note : BPSG etch rate ≈ 4400Å/min)	Pressure : 100 100 mTorr	
	DO NOT overetch the contact	Elect Gap : 1.02 1.02 cm	
		Etch Time : ≈50 sec 50% (≈ 75 sec)	
57	PR strip	O2 Ashing : Endpoint + Over etch MK2-ERS clean: 60C, 10mins, QDR & SRD Dry	All wafers
58	LIGHT SHIELD DEPOSITION:	Metallization: target = Al =0,5 um	All wafers
	Pre-clean Bench --- WB-PM-1	Clean Process : PC1	
		50: 1 HF Dip : 10 sec	
		Monitor wafer must be pre-cleaned	
	BPS sputter	BPS CL200	
	Metal Deposition	Al =0.5 um	
	Measure Sheet Resistance (Test wafer) =		
59	Litho-12	Mask layer:METAL2 MASK L12	All wafers
	Coat Photoresist	AIO Photoresist Track	
	Coat Track Process Program : 1.1	S1813, 1.23 um, 110C, 60sec	

	Align/Expose:	System :	
		UV Intensity : mW/cm ²	
		Exposure Time : sec	
	Develop Photoresist and hardbake	AIO Photoresist Track	
	Develop Track Process Program : <u>2.1</u>	Develop : SD-W, 1 puddle, 60sec Hardbake : 120C, 120sec	
	Inspect and measure Critical Dimension(CD)	Canon Microscope (Spec CD = 30.00 μ m)	
	DI- CD= 5 locations		
60	Metal etch	LAM03	All wafers
	Plasma etch: RIE mode	RF Power : 200 W	
		BC13 : 75 SCCM	
	Metal etch recipe: 800	Cl2 : 32 SCCM	
		N2 : 25 SCCM	
		Pressure : 275 mTorr	
		Elect Gap : 5.0 cm	
61	PR strip	O2 Ashing : Endpoint + Over etch MK2-ERS clean: 60C, 10mins, QDR & SRD Dry	All wafers
62	METAL-1 ALLOY	Sintering at 425C in Forming gas	All wafers
	Pre-clean Bench --- WB-	Clean Process : PM-1	
		ACT-CMI : 10 mins, 50-60 C	
		QDR : 6 cycles	
		IPA Dry	
	Furnace :	B4	
	Process Recipe	810	
	Process Name : ALLOY	20 min. N2=8 SLM, 425C, Load	
		25 min. N2=6 SLM, H2=100 SCCM, 425C	
		2 min. N2=6 SLM, 425C	
		20 min. N2=8 SLM, 425C, Unload	
63	PECVD UDTEOS	Dep 6KA	ONLY Wafers 2,5,8,11,12
	P5000	420C	
	UDTEOS	TEOS	
		pressure	
	Measure Tox		
64	Litho-13	Mask layer:PAD MASK M13+DesignF MASK N14	All wafers
	Coat Photoresist	AIO Photoresist Track	
	Coat Track Process Program : <u>1.1</u>	S1813, 1.23 μ m, 110C, 60sec	
	Align/Expose:	System :	
		UV Intensity : mW/cm ²	
		Exposure Time : sec	
	Develop Photoresist and hardbake	AIO Photoresist Track	
	Develop Track Process Program : <u>2.1</u>	Develop : SD-W, 1 puddle, 60sec Hardbake : 120C, 120sec	
	Inspect and measure Critical Dimension(CD)	Canon Microscope (Spec CD = 30.00 μ m)	
	DI- CD= 5 locations		
65	PAD ETCH	Open pad holes for metal contact in UDTEOS(Etch: oxide)	All wafers

65a	O2 Plasma Descum	Note Etch	
	Condition:		
	Etcher	LAM 02	
	Recipe Name :	Oxide Etch	
	Recipe No.: 999	Etch Mode: PE/Top	
		RF Power : 200 W	
		O2 : 20 sccm	
		Pressure : 100	
		mTorr	
		Elect Gap : 1.5 cm	
		Etch Time : 10 sec	
	Wet Contact Etch	BOE : 6:1 , Etch Time : <1 min	
	-- WB - MK-1	Cascade Rinse --- to 15 MΩ	
		Spin Dry only	
65b	Hard bake	Backing Oven	
		-- 120°C, 30 mins	
	Plasma Oxide etch (spec=5000A)	Etch Mode: plasma	
	Etcher	LAM 02	
	Recipe Name :	Oxide Etch	
	Recipe No:500	Step : Main	
		Overetch	
		RF Power : 550	
		200 W	
		Ar : 300 300	
		SCCM	
		CF4 20 20	
		SCCM	
		CHF3 : 45 45	
		SCCM	
	(Note : BPSG etch rate ≈ 4400Å/min)	Pressure : 100 100	
		mTorr	
	DO NOT overetch the contact	Elect Gap : 1.02	
		1.02 cm	
		Etch Time : ≈50 sec 50% (≈ 75 sec)	
66	PR strip	O2 Ashing : Endpoint + Over etch MK2-ERS clean: 60C, 10mins, QDR & SRD Dry	All wafers
67	Litho-14	Mask layer:DesignF MASK N14	All wafers
	Coat Photoresist	AIO Photoresist Track	
	Coat Track Process Program : 1.1	S1813, 1.23 um, 110C, 60sec	
	Align/Expose:	System :	
		UV Intensity : mW/cm2	
		Exposure Time : sec	
	Develop Photoresist and hardbake	AIO Photoresist Track	
	Develop Track Process Program : 2.1	Develop : SD-W, 1 puddle, 60sec Hardbake : 120C, 120sec	
	Inspect and measure Critical Dimension(CD)	Canon Microscope (Spec CD = 30.00 μm)	
	DI- CD= 5 locations		
68	Active region opening		All wafers
68a	O2 Plasma Descum	Note Etch	

		Condition:
	Etcher	LAM 02
	Recipe Name :	Oxide Etch ??
	Recipe No.: 999	Etch Mode: PE/Top
		RF Power : 200 W
		O2 : 20 sccm
		Pressure : 100
		mTorr
		Elect Gap : 1.5 cm
		Etch Time : 10 sec
	Wet Contact Etch	BOE : 6:1 , Etch Time : <1 min
	-- WB - MK-1	Cascade Rinse --- to 15 MΩ
		Spin Dry only
	Hard bake	Backing Oven
		-- 120°C, 30 mins
68b	Plasma Oxide etch (spec=5000A)	Etch Mode: plasma
	Etcher	LAM 02
	Recipe Name :	Oxide Etch
	Recipe No:500	Step : Main
		Overetch
		RF Power : 550
		200 W
		Ar : 300 300
		SCCM
		CF4 20 20
		SCCM
		CHF3 : 45 45
		SCCM
	(Note : BPSG etch rate ≈ 4400Å/min)	Pressure : 100 100
		mTorr
	DO NOT overetch the contact	Elect Gap : 1.02
		1.02 cm
68c		Etch Time : ≈50 sec 50% (≈ 75 sec)
	Plasma Nitride Etch (spec=500 A)	Etch Mode: plasma
	Etcher :	LAM 01
	Recipe Name :	Nit-1
	Recipe No.: 100	Step : Main
		Overetch
		RF Power : 250
		250 W
		SF6 : 200 200
		SCCM
		O2 : 0 0
		SCCM
	(ensure O2 descum step before etching)	He : 50 50
		SCCM
		Pressure : 500 500
		mTorr
		Elect Gap : 2.0
		2.0 cm
		Etch Time : EP
		8% (≈ 60 sec)
	Measure Tox(active) =	

68d	Measure remaining oxide in contact region Tox (=150A)	Ensure oxide in contact region is clear	All wafers
68e	Measure remaining oxide in contact region Tox (= 300A)	Ensure oxide in contact region is clear	All wafers
69	PR strip	O2 Ashing : Endpoint + Over etch MK2-ERS clean: 60C, 10mins, QDR & SRD Dry	All wafers
70	BACKSIDE METAL		All wafers
	Pre-clean Bench --- WB-PM-1	Clean Process : PC1	
		50: 1 HF Dip : 10 sec	
		Monitor wafer must be pre-cleaned	
	Metal Deposition	Evap	
	Equipment : INNOTECH	Al =1 um???	
71	DICING		
	PROCESS END		