Design, simulation and fabrication of silicon carbide metal semiconductor field effect transistors

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**DESIGN, SIMULATION AND FABRICATION OF
SILICON CARBIDE METAL SEMICONDUCTOR
FIELD EFFECT TRANSISTORS**

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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

2007

Design, Simulation and Fabrication of Silicon Carbide Metal Semiconductor Field Effect Transistors

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Summary

Silicon carbide (SiC) based metal semiconductor field effect transistors (MESFETs) are very well-suited for high power, high frequency and high temperature applications due to the excellent electronic and physical properties of SiC, such as wide band gap, high breakdown electric field strength, large electron saturation velocity and high thermal conductivity. The objective of this work is to design, simulate, fabricate and characterize SiC MESFETs.

In this work, Medici simulator and Matlab software were selected to study and model 4H-SiC MESFETs. The built-in physical models were chosen and their parameters were optimized to provide a good agreement with the experimental results obtained for 4H-SiC MESFETs. A three-region analytical model was also developed to simulate the behavior of short-channel SiC MESFETs under high drain voltage.

The device processing technology was successfully developed for the fabrication of SiC MESFETs. The reactive ion etching (RIE) process was used to form mesa isolation and channel recess etching with good surface uniformity and repeatable etch rate. Lift-off process was used to deposit metal masks for etching and to form metal contacts combined with self-aligned process. The sheet contact resistance of Ni/4H-SiC ohmic contacts is about $2.8 \times 10^{-5} \Omega \cdot \text{cm}^2$ and the barrier height of Ni/Au Schottky contacts to 4H-SiC is about 1.32 eV. The conventional 4H-SiC MESFETs fabricated with a $1.0 \mu\text{m}$ gate length (L_g) has a threshold voltage of about -5.6V and a maximum transconductance g_m of about 33 mS/mm. The small-signal cut-off frequency (f_T) and

maximum oscillation frequency (f_{max}) are about 3.08 GHz and 9.5 GHz respectively, obtained from the dual-finger gate device with a gate length $L_g = 1.25 \mu\text{m}$ under the bias of $V_{gs} = 0\text{V}$ and $V_{ds} = 30\text{V}$.

The drain-induced barrier lowering (DIBL) effect in conventional 4H-SiC MESFETs was investigated in detail by physical simulation. Our simulation results showed that for short gate length SiC MESFETs, the DIBL effect will result in large threshold voltage shift and significantly affect the device performance when a large drain voltage is applied. The DIBL effect is more dependent on the ratio of the gate length to channel thickness (L_g/a), rather than the channel thickness itself. High channel doping concentration has also been found to enhance the DIBL effect. In order to minimize the DIBL effect, the ratio of L_g/a should be kept much greater than 3 for practical 4H-SiC MESFETs, especially when the channel doping concentration is more than $5 \times 10^{17} \text{cm}^{-3}$. SiC MESFETs with a highly doped narrow channel layer were proposed and fabricated to reduce the DIBL effect. It is demonstrated that the threshold voltages of the narrow channel MESFETs are about -1.1V and independent of the gate length when the drain voltage applied is up to 40V. Concurrently, better saturation behavior with fairly lower output conductance, which is desirable for small signal applications, is achieved.

Dual-channel 4H-SiC MESFETs were designed and fabricated to provide high source-drain breakdown voltage and high output power. The experimental results of the $1.0 \mu\text{m}$ gate length device are compared with those of conventional devices with a single channel layer fabricated using exactly the same process flow. The saturation drain current density is about $280 \mu\text{A}/\mu\text{m}$ and the threshold voltage is about -14.0V

for the dual-channel MESFETs, which are both higher than the $125\ \mu\text{A}/\mu\text{m}$ and -5.6V measured for the conventional devices. The improvements are attributed to the high doped lower-channel layer. The dual-channel MESFETs exhibit a lower gate leakage current of about $6.5 \times 10^{-6}\ \mu\text{A}/\mu\text{m}$ and a higher breakdown voltage of about 145V , which are improved compared to the conventional devices, attributed to the lower doped upper-channel layer. Besides, a higher output power density of $4.6\ \text{W}/\text{mm}$ can be achieved for the dual-channel devices compared to $1.8\ \text{W}/\text{mm}$ for the conventional devices. On the other hand, the cut-off frequency of the device with $1.25\ \mu\text{m}$ gate length is about $1.58\ \text{GHz}$ which is slightly lower than that of the conventional devices.

The electrical performance of SiC MESFETs with a double-recessed structure was studied and compared with the conventional recessed structure. The simulated results showed that the saturation current and the output power density of the double-recessed structure are about 77% and 37.5% larger than that of the conventional structure. However, their threshold voltages are comparable and are -9.2V and -8.4V for the double-recessed and conventional structure respectively. The three-terminal breakdown voltages of double-recessed and conventional structure are about 109V and 137V , respectively which is consistent with published experimental results. The cut-off frequency and the maximum oscillation frequency of the double-recessed structure are $15.3\ \text{GHz}$ and $64.5\ \text{GHz}$ respectively compared to $10.0\ \text{GHz}$ and 38.0GHz for the conventional structure. Therefore, the double-recessed 4H-SiC MESFET has superior DC and RF performances compared to similar devices based on the conventional structure.

CHAPTER 1 INTRODUCTION

Chapter 1

Introduction

1.1 Motivation

Most traditional integrated circuit technologies based on silicon (Si) devices are generally limited to operation at junction temperatures below 200°C and voltage blocking capabilities of less than a few kilovolts by virtue of its intrinsic physical properties. Wide band gap semiconductors, such as crystalline silicon carbide (SiC), gallium nitride (GaN), aluminum nitride (AlN), boron nitride (BN), diamond and zinc selenide (ZnSe), offer the potential to overcome both the temperature and voltage blocking limitations of Si [1]. Among these semiconductors, SiC has emerged as the most promising due to several advantages it possesses, which include availability of commercial substrates, known device processing techniques, the ability to grow thermal oxide for use as masks in processing, device passivation layers and gate dielectrics. Indeed, SiC is the only compound semiconductor that can be thermally oxidized to form a high quality native oxide. Thus, it is possible to make all the devices found in Si integrated circuit technology using SiC.

Silicon carbide possesses many favorable properties making it interesting for high power, high temperature and high frequency device applications. Specifically, these properties are: wide band gap (~3.26 eV for 4H-SiC), high thermal conductivity (even

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higher than copper at room temperature), high breakdown electric field strength (approximately 10 times that of Si), high saturated drift velocity (high than gallium arsenide (GaAs)), high thermal stability and chemical inertness. Due to the above advantages, theoretical estimations have established that SiC-based devices can stand off higher voltages, can respond faster and are smaller in size. This enables weight and size savings as smaller transformers and capacitors are required. Another benefit derived from the use of SiC is that it renders cooling requirements less important because SiC electronics can operate at high temperature, and this could reduce the size and the cost of a power conversion and distribution system. All of these demonstrate that SiC is a very promising electronic material, especially for use in semiconductor devices operating at high temperature, high power and high frequency.

Up to now, microwave communication and radar electronics are implemented using GaAs technology. However if high power over the frequency range 1-10 GHz and high temperature operations are required, GaAs electronics would not be suitable due to its lower energy band gap. The alternative is then to develop SiC based electronic devices, such as metal semiconductor field effect transistors (MESFETs), which also can satisfy the requirements of future wireless communications. The demand of such high power microwave transistors will be in the areas of cell phone base stations, radar systems and high definition television transmitters [2]. Indeed prototype SiC-based transistors have been demonstrated to perform at power densities much higher than the theoretical maximum densities of GaAs based microwave transistors.

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The ideal, theoretical performance advantages of SiC based electronic devices have been known for some time. However, only recently has it been possible to realize some of these advantages in fabricated devices, primarily due to the immature crystal growth and device fabrication technologies of SiC.

The presence of micropipes in the SiC substrates and epilayers has been a key obstacle to the realization of high power SiC devices. However, with micropipe densities as low as $0.1/\text{cm}^2$ achieved for research grade wafers (reduced from over $1000/\text{cm}^2$ in just a few years) [3], indications are that SiC is now adequate for device fabrication of several millimeters square with reasonable yield [4,5]. Emphasis on defect is now switching from micropipes to closed-screw dislocation as there is a positive correlation between dislocation density and breakdown voltages [6].

It is known that the inert nature of SiC makes it suitable for operation in harsh environments; however, this positive benefit is a significant drawback when it comes to device fabrication. For example, no wet chemical under standard conditions will etch SiC at a rate sufficient enough for practical applications [7]. For this reason, micro-mechanical structures made from bulk material have largely been discounted. Existing conventional contact technologies are not suitable for reliable operation in high temperature and high power conditions that SiC enables [8]. The durability and reliability of metal-semiconductor contacts at high temperature are important considerations for SiC devices. Similarly, SiC high power devices contacts have to withstand high current density and also keep the power losses within reasonable limits [9]. Passivation of the SiC surface is not trivial and has yet to be fully understood. The effects of inadequate passivation have been observed in SiC microwave

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MESFETs, which leads to degradation of gain under continuous wave (CW) operation [3,10]. Some researchers [11,12] suggested a buried-gate structure to suppress the trapping induced instabilities, which can degrade the electrical performance of the devices operated at continuous waveband (CW) and to provide high drain current. However, experimental results showed that the source-drain breakdown voltage of buried-gate transistors was lower than that of conventional channel recessed structures. [12] Toshiya Y. *et al.* studied multi-delta doping layers with undoped inter-layers as the channel layer for 6H-SiC MESFETs to provide high breakdown voltage [13,14]. However, no saturation region was found in this type of transistors and the drain current was also limited. Therefore, further improvements may be made to overcome the above mentioned problems faced in SiC MESFETs.

1.2 Objectives

The objective of this work is to design, simulate, fabricate and characterize SiC MESFETs. Medici simulator [15] and Matlab software are used for the design and modeling of the device performance. A three-region analytical model has been developed to simulate the behavior of short-channel SiC MESFETs under high drain voltage. A complete fabrication process has also been developed for SiC MESFETs. The main fabrication process steps include mesa isolation and channel recess etching; thermal oxidation; source and drain contact formation, and gate contact formation. The lift-off process and self-aligned process are used in the contact formation, and the former is also used to form metal masks to protect active region during mesa and channel recess etching.

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Sub-micron gate length 4H-SiC MESFETs have been successfully fabricated to enhance the high frequency performance [16,17]. However, the threshold voltages of 4H-SiC MESFETs has been found to increase with decreasing gate length [17]. It also increases with increasing drain-source voltage. Both the above phenomena are originated from the drain-induced barrier lowering (DIBL) effect. High power and high frequency 4H-SiC MESFETs are particularly susceptible to this effect due to the large drain voltage applied and their short channel length. In this work, we have studied in detail the DIBL effect and its dependence on device structure parameters. It is found from the simulation results that narrow channel MESFETs are effective in reducing the undesirable DIBL effect. Narrow channel 4H-SiC MESFETs are subsequently designed, fabricated and characterized to reduce the undesirable DIBL effect.

Though narrow channel MESFETs can effectively minimize the DIBL effect, its output power density is lower compared to that of conventional devices. To address this issue, 4H-SiC MESFETs with a dual-channel layer are designed, fabricated and characterized. In the device structure, the higher doped lower-channel layer serves to increase the channel current while the lower doped upper-channel layer is used to improve the breakdown voltage. Therefore, a higher output power density can be achieved compared to the conventional channel devices. In this work, a double-recessed 4H-SiC MESFET structure is also proposed to improve both DC and RF performances. Such double-recessed 4H-SiC MESFETs are investigated in detail through physical simulation.

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1.3 Major Contribution

4H-SiC MESFETs were studied using Medici simulator and Matlab software with selected built-in physical models and optimized parameters for 4H-SiC. A good agreement was obtained between the experimental and simulation results for 4H-SiC MESFETs. A three-region analytical model was also developed to simulate the behavior of short-channel SiC MESFETs under high drain voltage.

The key process technologies were developed for SiC semiconductors. In particular, lift-off process was used to deposit metal as masks for SiC etch or as metal contacts on SiC. Self-aligned process was used to form source, drain and gate metal contacts. Rapid thermal anneal (RTA) process at 1000°C for 1 min in nitrogen ambient was developed to form good Ni/4H-SiC ohmic contacts with a sheet contact resistance of about $2.8 \times 10^{-5} \Omega\text{-cm}^2$. The barrier height of Ni/Au Schottky contacts to 4H-SiC is about 1.32 eV without annealing. Based on the developed processes for SiC, conventional 4H-SiC MESFETs with different gate length (L_g) of 1.0 μm , 1.25 μm , 1.5 μm , 2.0 μm , 2.5 μm and 3 μm were successfully fabricated and characterized. The threshold voltage is about -5.6V and the maximum g_m is about $32.8 \mu\text{S}/\mu\text{m}$ for 1.0 μm gate length devices. The small-signal cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) were about 3.08 GHz and 9.5 GHz respectively, obtained from the dual-finger gate device with $L_g = 1.25 \mu\text{m}$ under the bias of $V_{gs} = 0\text{V}$ and $V_{ds} = 30\text{V}$.

The drain-induced barrier lowering (DIBL) effect in conventional 4H-SiC MESFETs was investigated in detail by physical simulation. Our results have shown that for short gate length SiC MESFETs, the DIBL effect will result in large threshold voltage shift and significantly affect the device performance when a large drain voltage is

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applied. The dependence of the DIBL effect on the ratio of gate length over channel thickness (L_g/a) and the channel doping concentration (N_d) was studied. SiC MESFETs with a highly doped narrow channel layer were proposed and fabricated to reduce the DIBL effect. It was demonstrated that the threshold voltages of the narrow channel MESFETs are about -1.1 V and independent of the gate length when the drain voltage applied is up to 40V. Concurrently better saturation behavior with fairly lower output conductance is achieved which is desirable for small signal applications.

Dual-channel 4H-SiC MESFETs were fabricated and characterized. The experimental results obtained for the $1.0\text{ }\mu\text{m}$ gate length devices are compared with those of conventional devices with a single channel layer fabricated using exactly the same process flow. The saturation drain current density is about $280\text{ }\mu\text{A}/\mu\text{m}$ and the threshold voltage is about -14.0V for the dual-channel MESFETs, which are both higher than the $125\text{ }\mu\text{A}/\mu\text{m}$ and -5.6V measured for the conventional devices. The improvements are attributed to the high doped lower-channel layer. The dual-channel MESFETs exhibit a lower gate leakage current of about $6.5\times 10^{-6}\text{ }\mu\text{A}/\mu\text{m}$ and a higher breakdown voltage of about 145V, which are improved compared to the conventional devices, attributed to the lower doped upper-channel layer. Besides, a higher output power density of $4.6\text{W}/\text{mm}$ can be achieved for the dual-channel devices compared to $1.8\text{W}/\text{mm}$ for the conventional devices.

The electrical performances of SiC MESFET with a proposed double-recessed structure were simulated and compared with the conventional recessed structure. The simulated results showed that the saturation current and the output power density of the double-recessed structure are about 77% and 37.5% larger than those with the

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conventional structure while exhibiting comparable threshold voltages. The cut-off frequency and the maximum oscillation frequency of the double-recessed structure are 15.3 GHz and 64.5 GHz respectively compared to 10.0 GHz and 38.0 GHz for the conventional structure.

1.4 Organization of the Thesis

This thesis is mainly organized into eight chapters. The first chapter describes the motivation and objectives, major contribution and organization of the thesis. The second chapter presents the background and literature review for SiC semiconductor, contacts and MESFETs. Chapter three details the modeling and simulation of 4H-SiC MESFETs. Chapter four describes the fabrication and characterization of SiC MESFETs. Chapter five presents drain-induced barrier lowering (DIBL) effect in conventional 4H-SiC MESFETs, and shows the experimental results for narrow channel layer MESEFTs which were proposed used to reduce DIBL effect. Chapter six presents the results of 4H-SiC MESEFTs with a dual-channel layer structure which were designed and fabricated to improve the breakdown voltage and output power density of the devices. Chapter seven presents the simulation results of 4H-SiC MESFETs with a double-recessed gate to improve both the DC and RF performance of the devices. Chapter eight concludes the thesis and summarizes the results that have been achieved and it also includes recommendations for further research.

CHAPTER 2 BACKGROUND AND LITERATURE REVIEW

Chapter 2

Background and Literature Review

2.1 Introduction

The radio frequency (RF) performance of electronic devices is determined by both the structural design of the devices and the electrical and thermal characteristics of the semiconductor from which the devices are fabricated. In addition, the manufacture of RF devices requires low resistance ohmic contacts between the semiconductor and external metal conductors, and rectifying contacts to establish potential barriers for the control of currents within the device. Therefore the contact properties also critically determine the RF performance. It is noted that contact technology is particularly challenging for wide band gap semiconductors such as silicon carbide (SiC).

In this chapter, SiC material properties, SiC metal contact and SiC metal semiconductor field effect transistors (MESFETs) will be reviewed. The latest development in the area of SiC MESFETs will also be discussed.

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2.2 Properties of SiC

Silicon carbide as a semiconductor material offers some unique properties such as wide bandgap, high breakdown electric field strength, large electron saturation velocity and high thermal conductivity, making it interesting for high temperature, high-frequency and high power device applications. Proper exploitation of these properties enables SiC based devices to operate in regimes formerly not possible for solid state devices. For example, the wide band gap and high breakdown electric field strength of SiC allow it to be used for high power and high temperature electronic devices.

2.2.1 Crystallography of SiC

SiC chemically consists of 50% silicon atoms covalently bonded with 50% carbon atoms. It occurs in more than a hundred polytypes [18], with each having its own distinct set of electrical properties. However, only a few are commonly grown in a reproducible form acceptable for use as semiconductors for electronic applications, such as 4H-SiC and 6H-SiC with hexagonal lattice structures and 3C-SiC with a cubic lattice structure. Different polytypes of SiC are actually composed of different stacking sequences of Si-C dual-layer, which is treated as a basal layer consisting of a planar layer of silicon atoms coupled with a planar layer of carbon atoms [18]. The stacking direction, which is the crystallographic c-axis direction or the [0001] direction, is defined normal to the Si-C dual-layer. The difference between the polytypes is in the stacking order between succeeding double layers of carbon and silicon atoms.

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Fig. 2.1 The stacking sequence of double layers of the three most common SiC polytypes (the open circles denote silicon while the shaded circles denote carbon) [19].

In Fig. 2.1 the stacking sequences are shown for the three most common SiC polytypes, 3C, 4H and 6H [19]. If the first double layer is called the A position, the next layer that can be placed according to a closed packed structure will be at the B position or the C position. The different polytypes are constructed by permutations of these three positions. For instance the 4H-SiC polytype has a stacking sequence ABCBABC... The number “4” denotes the periodicity while the letter “H” denotes the resulting structure which in this case is hexagonal. The stacking sequences of 3C and 6H-SiC are ABCABC... and ABCACBABC..., respectively. It should be noted that the silicon atoms labeled “h” or “k” in Fig. 2.1 denote Si-C double layers that reside in “quasi-hexagonal” or “quasi-cubic” environments respectively with respect to their immediate neighbors above and below the dual-layers. SiC is a polar semiconductor across the c-axis, in that one surface normal to the c-axis is terminated with silicon atoms while the opposite surface normal to the c-axis is terminated with carbon atoms. As shown in Fig. 2.1, these surfaces are typically referred to as “silicon face” and “carbon face” respectively.

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2.2.2 Electrical Properties of SiC

Electrically, each SiC polytype exhibits unique properties due to the different arrangement of Si and C atoms within the SiC crystal lattice. Some of the more important semiconductor electrical properties of 3C, 4H, and 6H SiC polytypes are given in Table 2.1 [20,21], therein along with those of Si, GaAs, GaN and diamond for comparison. Note that some important electrical properties such as the electron mobility in 6H-SiC, are non-isotropic, in that they are a strong function of crystallographic direction of current flow and applied electric field.

Property	Si	GaAs	4H-SiC	6H-SiC	3C-SiC	GaN	Diamond
Band gap(eV)	1.12	1.42	3.26	3.02	2.39	3.45	5.45
Relative Dielectric Constant	11.8	12.8	9.7	9.7	9.7	11	5.5
Breakdown Field @ $N_D=10^{17}\text{cm}^{-3}$ (MV/cm)	0.3	0.4	//c-axis: 3.0	//c-axis:3.2 ⊥c-axis:>1	>1.5	4.1	10
Thermal Conductivity (W/cm·K)	1.5	0.5	3-5	3-5	3-5	1.3	20
Intrinsic Carrier Concentration (cm^{-3})	10^{10}	1.8×10^6	$\sim 10^{-7}$	$\sim 10^{-5}$	~ 10	--	--
Electron Mobility @ $N_D=10^{16}\text{cm}^{-3}$ (cm^2/Vs)	1200	6500	//c-axis:800 ⊥c-axis:800	//c-axis:60 ⊥c-axis:400	750	1250	2200
Hole Mobility @ $N_A=10^{16}\text{cm}^{-3}$ (cm^2/Vs)	420	320	115	90	40	250	1600
Saturated Electron Velocity($\times 10^7\text{cm/s}$)	1.0	1.2	2	2	2	2.2	2.7

Table 2.1 Properties of SiC compared to some well-known semiconductors.

The band gap of SiC is almost three times that of Si and over twice that of GaAs as shown in Table 2.1. This results in SiC having low intrinsic carrier concentration and high resistance to ionization from radiation. The relative dielectric constant of SiC which is a measure of the capacitive loading is about 20% less than those of Si and GaAs. A low dielectric constant reduces the device parasitic capacitances. In other

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words, for the same device parasitic capacitance, a larger device area can be used, which in turn permits higher RF power levels to be developed.

High breakdown field, high saturated electron velocity and high thermal conductivity are the key parameters that are particularly important for high power microwave devices. The wide band gap of SiC results in high critical electric field for breakdown, which is almost an order of magnitude greater than those of Si and GaAs. This allows SiC devices to be operated at much higher voltages, which is necessary to obtain high RF output power. The high breakdown field also allows devices such as field effect transistors (FETs), to be operated under extremely high electric fields, driving the electrons into their high saturation velocity across a large part of the conducting channel. This can offset the drawback of its low carrier mobility compared to Si and GaAs. At the same time, the high saturation velocity of SiC facilitates high device current density. The combination of high voltage and high current density results in very high power densities for SiC devices, which is an important consideration for high power microwave devices, since the device size is limited to a fraction of the wavelength of operation. The thermal conductivity of SiC is excellent and a factor of three higher than that of Si and a factor of eight higher than that of GaAs. The high thermal conductivity of SiC provides superior conduction of the heat generated by the high power density, and its wide band gap allows these devices to be operated at higher temperatures than are possible with Si or GaAs.

The most extensively investigated SiC polytypes for electronic applications are the 3C, 4H and 6H polytypes. In the case of 6H-SiC, the electron mobility in the direction of the c-axis is much lower than that along the basal plane. This leads to a significant

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electron mobility anisotropy ratio for 6H-SiC. In contrast, the significantly larger electron mobility in 4H-SiC, along with its reduced anisotropy, indicate that this polytype is superior compared to 6H-SiC in many applications, especially for power devices. Therefore, in this work, 4H-SiC will be used to fabricate the power devices.

2.3 SiC Contacts

Metal-semiconductor contacts are indispensable in all electronic devices. All useful semiconductor devices require high-quality ohmic contacts to transfer signals between devices and between the semiconductor and the external circuitry. Existing conventional contact technologies will likely not be suitable for reliable operation in high temperature and high power conditions that SiC enables [8]. The durability and reliability of metal-semiconductor contacts at high temperature are important considerations for SiC devices. Similarly, SiC high power devices contacts have to withstand high current density and also keep the power losses within reasonable limits [9]. Such stringent requirements for the contacts are never encountered in silicon power electronics.

Just as for conventional narrow band gap semiconductors that include silicon and GaAs [22,23,24], the basic physics and current transport mechanisms such as surface states, Fermi-level pinning, thermionic emission and tunneling, are also applicable to SiC contacts. The only difference is that the wider band gap of SiC allows higher effective Schottky barrier heights to be achieved. The microstructural and chemical state of the SiC-metal interface is crucial to the contact electrical properties. Therefore, pre-metal-deposition surface preparation [25], choice of metal [8, 9,26,27] and post-

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deposition annealing [25,28,29] play important roles in determining the performance of SiC-metal contacts.

2.3.1 SiC Ohmic Contacts

Ohmic contacts serve the purpose of carrying electrical current into and out of the semiconductor, ideally with zero resistance. The properties of various ohmic contacts to SiC have been widely reported [28,30,31]. In general, the specific contact resistances of SiC ohmic contacts at room temperature are generally higher than those of conventional semiconductor ohmic contacts. Lower specific contact resistances (ρ_c) are usually obtained for n-type 4H-SiC and 6H-SiC ($\sim 10^{-4}$ to 10^{-6} ohm $\cdot$ cm²) than for p-type 4H-SiC and 6H-SiC ($\sim 10^{-3}$ to 10^{-5} ohm $\cdot$ cm²). Consistent with narrow band gap ohmic contact technology, it is easier to make low resistance ohmic contacts to heavily-doped SiC, which can be achieved by nitrogen-rich epi-layer growth or high-dose ion implantation into SiC. The ohmic contacts are usually annealed at high temperature of around 1000 °C in a non-oxidizing ambient. Depending on the contact metallization employed, this anneal generally causes limited interfacial reactions (usually metal-carbide or metal-silicide formation) that broaden and/or roughen the metal-semiconductor interface, resulting in enhanced conductivity through the contact.

Although different metal contacts on SiC have been the subject of study in the last decade (Cr, Al, Ti, Pd, NiTi, TiC, etc. [22,32]), in many works nickel has been proposed as the most suitable candidate for the fabrication of ohmic contacts on n-type SiC due to their reproducible low specific contact resistance. It is deemed the industry standard ohmic contact to n-SiC [24,33,34]. For fabricating ohmic contacts

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on SiC using nickel, annealing processes of Ni/SiC are generally performed under different atmospheres (vacuum, N₂, Ar, forming gas) at 950 - 1000°C [28,29,35]. All have been found to result in low values of specific contact resistance. Ohmic contacts with $\rho_c = 3 \times 10^{-5}$ to $9 \times 10^{-5} \Omega \cdot \text{cm}^2$ were obtained for substrates with doping concentration $N_d = 7 \times 10^{18}$ to $4 \times 10^{18} \text{ cm}^{-3}$ correspondingly after rapid thermal anneal (RTA) in N₂ at 950°C [36]. These optimized contacts are electrically stable even after annealing in N₂ up to 1000°C. The high temperature anneal usually used for obtaining good ohmic contacts leads to the formation of nickel silicide (Ni₂Si) which is a stable phase in the Ni/SiC reaction [29,37].

2.3.2 SiC Schottky Contacts

Rectifying metal-SiC Schottky barrier contacts are useful for a number of devices including metal semiconductor field effect transistors (MESFETs) and fast-switching rectifiers. It has been shown that the barrier height in SiC Schottky contacts depends on the metal work function without strong Fermi level pinning. [9,27,38] Due to the wide band gap of SiC, almost all unannealed metal contacts to lightly doped 4H-SiC and 6H-SiC are rectifying.

SiC Schottky barrier diodes are especially attractive due to the high breakdown electric field and large band gap of SiC. Compared to Si devices, high voltage Schottky diodes based on SiC with relatively lower leakage current and on-resistance can be fabricated. [27,39] These SiC Schottky diodes have the potential to be valuable alternative to Si-based switching devices for applications where both power and speed need to be delivered. However, electric field crowding at the edges of the SiC Schottky contact can also lead to increased reverse-bias leakage current and reduced

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reverse breakdown voltage [40]. For high voltage Schottky diodes, special edge termination is required to minimize electric field crowding at the edges of the SiC Schottky barrier. [41,42,43] For example, the reverse breakdown voltage of such devices can be improved by applying field plate edge termination, with an oxide thickness of about 5 percent of the epi-layer thickness and a field plate overlap equals to the epi-layer thickness or beyond. [44]

2.4 SiC MESFETs

The MESFET was first proposed by Mead in 1966 [40] and has been widely fabricated using GaAs for both microwave and high-speed applications. The MESFET offers certain processing and performance advantages, such as low-temperature formation of the metal-semiconductor barrier, low resistance and low voltage drop along the channel length. It also offers good heat dissipation for power devices as the rectifying contact can also serve as an efficient thermal contact to heat sink. Compared to bipolar transistors, FETs have considerably higher input impedance, which allows them to be more readily matched to the standard microwave system at the input. Since FETs are unipolar devices, they do not suffer from minority-carrier storage effects, and consequently, have higher switching speeds and higher cutoff frequencies. In this work, SiC MESFETs are considered to combine the excellent properties of SiC and the advantages of MESFET. Their high power and high frequency performance will be investigated.

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Fig. 2.2 The cross-section of a conventional SiC MESFET.

Figure 2.2 shows the schematic cross-section of a recessed-channel SiC MESFET structure that consists of a semi-insulating substrate, p-type buffer layer, n-type channel layer and a highly doped n-type cap layer. The latter is required to achieve low resistance source and drain ohmic contacts, an important requirement in microwave devices. Recently, ion-implantation was also used to form ohmic contacts to replace the n^+ cap layer. [45] The gate metal is directly deposited on the channel layer between the source and the drain where the n^+ layer is over-etched. In MESFET structure, the most important parameters are the gate length (L_g) and width (W), the channel thickness (a) and doping concentration (N_d).

The basic operation principle of the MESFET is shown in Fig. 2.3. [46] The source is grounded and the Schottky gate contact is reverse-biased. The drain is firstly grounded to simplify the analysis. A depletion region with a thickness of h is located underneath the gate and extends into the channel layer, and only a negligible current flows through the gate contact. A conducting channel with a height ($a - h$) exists between the edge of the depletion region and the bottom of the active layer. The

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thickness of the depletion region (h) depends on the built-in voltage (V_b) of the Schottky gate and the applied gate-source voltage (V_{gs}). It can be expressed as:

$$h = \sqrt{\frac{2\varepsilon(V_b - V_{gs})}{qN_d}} \quad (2-1)$$

where ε is the permittivity of SiC and q is the electron charge.

Fig. 2.3 The operation principle of MESFET [46].

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A more negative gate-source voltage V_{gs} gives rise to a wider space-charge region and thus a narrower conducting channel, and vice versa as shown in Fig. 2.3(a). By varying the gate voltage, the depletion layer thickness is changed, so that the drain current from the drain to the source will be modulated. That means the current flowing under the depletion region can be controlled by the gate voltage.

When a positive drain-source voltage V_{ds} between the source and the drain terminals is applied, an electric field along the $-x$ direction is set up in the channel, where x -axis is defined to be directed from the source toward the drain parallel to the semiconductor surface. Driven by such a field, electrons move from the source toward the drain and give rise to the drain current I_d . As the potential difference between the channel and gate increases from the source to the drain, the space charge region (h) increases and consequently the height of the conducting channel ($a-h$) decreases towards the drain, as shown in Fig. 2.3(b). The detail analysis of the device operation will be present in Chapter three.

The region underneath the gate in Fig. 2.3 (a) is the intrinsic transistor. It governs the main function of MESFET, that is, to regulate the current and to amplify signals. The channel that is nearer to the drain and source form the extrinsic region. It deteriorates the device behavior due to its parasitic resistances and capacitances.

The microwave performance of MESFETs is strongly influenced by the material properties, such as electron mobility, electron saturation velocity, dielectric and thermal conductivity. The main drawback in using 4H-SiC for microwave devices lies in its poor low field electron mobility of $300 - 500 \text{ cm}^2/\text{Vs}$, at doping levels of

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interest for MESFETs, in the range of $1 \times 10^{17} - 5 \times 10^{17} \text{ cm}^{-3}$ [47]. This results in a larger source resistance and lower transconductance compared to GaAs based MESFETs. However, this drawback is partially offset by the high breakdown field strength of SiC that allows the MESFETs to be operated under extremely high electric fields, driving the electrons into their saturation velocity across a large part of the conducting channel. As SiC has high electron saturation velocity, therefore SiC MESFETs are suitable for high power operation in the microwave frequency range.

Drain-source breakdown voltage is another important factor that limits the maximum RF output power of a MESFET. The maximum power density can be expressed by [48,49]

$$P_{\max} = (V_{br} - V_{knee})^2 / 8R_L \quad (2-2)$$

where V_{br} is the drain-gate breakdown voltage, V_{knee} is the voltage required to reach saturation current and R_L is the load resistance. The poor low field electron mobility causes V_{knee} to be high, in the range of 5 to 10V. However, the breakdown field strength of SiC is nearly eight times higher than that of GaAs and this enables breakdown voltages in excess of 100V for SiC MESFETs, compared to about 20V normally observed in GaAs-based devices. In addition to improving the output power, the high voltage capability allows SiC MESFETs to be operated at high impedance matching and improves the performance of high power microwave circuits.

Another parameter that impacts the microwave performance of SiC MESFETs is the relatively deep ionization energy of the commonly used nitrogen shallow donors in SiC [50]. This leads to incomplete ionization of the donors in the FET channel, resulting in increased parasitic resistances and lower drain currents for a given

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channel doping level. For example, at a doping level of $5 \times 10^{17} \text{ cm}^{-3}$ in 4H-SiC, the electron density is calculated to be only $2.85 \times 10^{17} \text{ cm}^{-3}$. [46]

Availability of high resistivity or semi-insulating SiC substrates is another critical requirement to achieve good microwave performance. For low resistivity substrates where MESFETs are built upon, part of the RF power at the output is dissipated in the substrate, leading to lower gain and degraded RF performance. With the development of high resistivity and/or semi-insulating 4H-SiC substrates, most of the microwave MESFET work is presently focused on the 4H material. Besides, compared to 6H-SiC, significant improvement in both the power and frequency performance of SiC MFESFETs can be obtained by using the 4H-polytype of SiC due to its higher electron mobility and lower donor ionization energy.

The first 4H-SiC MESFETs were fabricated on conducting substrates [51]. These devices have gate dimensions of $0.7 \mu\text{m} \times 332 \mu\text{m}$ and channel thickness and doping of $0.26 \mu\text{m}$ and $1.7 \times 10^{17} \text{ cm}^{-3}$ respectively. The current density is about 300 mA/mm at $V_{ds}=25\text{V}$ and the maximum DC transconductance is in the range of 38 to 42 mS/mm. The cutoff frequency (f_T) and the maximum frequency of oscillation (f_{max}) values are 6.7 and 12.9 GHz, respectively, measured under the bias of $V_{ds} = 30\text{V}$ and $V_{gs} = 1.0\text{V}$. The high frequency performance of these devices was limited due to the conducting substrates used. Substantial improvements in RF performance were obtained by using high resistivity 4H-SiC substrates [52,53]. The highest f_{max} reported to date using this material is 42 GHz for devices with gate dimensions of $0.5 \times 200 \mu\text{m}^2$ [52]. The material structure consists of an undoped buffer layer and a channel layer with the thickness of $0.4 \mu\text{m}$ and doping of $5 \times 10^{17} \text{ cm}^{-3}$. These devices also showed a small-

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signal gain of 5.1 dB at 20 GHz under the bias of $V_{ds} = 40\text{V}$ and $V_{gs} = -6.5\text{V}$. These 4H-SiC MESFETs also showed excellent DC characteristics, with maximum drain current of 500 mA/mm and gate breakdown voltage in excess of 100V. This indicates the possibility of obtaining more than six times the power density achievable with GaAs MESFETs.

The development of high quality semi-insulating 4H-SiC substrates has enabled very significant advances in high power microwave devices [7,54]. Cree's optimized S-band power microwave MESFETs have a gate length of 0.7 μm and a channel doping of $3 \times 10^{17} \text{ cm}^{-3}$ [55,56,57]. These MESFETs were designed to have a threshold voltage of $V_{th} = -10\text{V}$, an I_{dss} of 300 mA/mm at $V_{ds} = 10\text{V}$ and a peak transconductance of 45 mS/mm. They have RF power densities of 4.6 W/mm at 3.5GHz, and the largest total RF output power from a single MESFET is 80 watts CW at 3.1 GHz coupled with a drain-source breakdown voltage of $V_{ds} > 150\text{V}$. With an increase in the channel doping and a reduction of the gate length to 0.45 μm , SiC MESFETs showed a power density of 4.3 W/mm at 10 GHz, with a peak power of 1.1W [3,58]. More recently, 0.4 μm MESFETs, also fabricated on semi-insulating 4H-SiC substrate, demonstrated f_T and f_{max} values of 18 and 50 GHz, respectively [16]. These MESFETs have a gate width of 0.5 mm and a channel doping of $3.0 \times 10^{17} \text{ cm}^{-3}$.

CHAPTER 3 MODELING AND SIMULATION

Chapter 3

Modeling and Simulation

3.1 Introduction

Modeling and simulation play an important role in modern semiconductor industry, especially for SiC due to the much more expensive SiC wafers and immature technologies compared to those of Si and III-V semiconductors. At present, the commercial device simulators such as Medici and DESSIS from Synopsys Inc. [59,60] and ATLAS from Silvaco International [61], are mainly catered for Si technologies. For them to be applied for SiC device simulation, the physical models and their parameters in the simulator should be selected and optimized to provide a good agreement with the experimental results for 4H-SiC. In this work, Medici simulator is selected to study SiC devices since it can handle well anisotropic properties of SiC and provide a faster convergence.

In this chapter, the basic equations involved in the physical simulation of devices will first be described, and the physical models and their parameters applicable to 4H-SiC will then be presented. A three-region analytical model to simulate the behavior of short-channel SiC metal semiconductor field effect transistors (MESFETs) under high drain voltage is proposed. The model has been shown to provide simulation results that are in good agreement with experimental results, compared to the commonly used

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two-region model. The equations used for calculating RF characteristics based on small signal S parameters extracted from the simulator or experimental measurements are presented.

3.2 Physical Simulation

3.2.1 Basic Simulation Equations (Drift-Diffusion Model)

The primary function of Medici is to self-consistently solve the three partial differential equations, in the Drift-Diffusion (DD) model that govern the electrical behavior of semiconductor devices. These are the Poisson equation and the current-continuity equations for electrons and holes shown in eqs (3.1), (3.2) and (3.3) respectively.

$$\epsilon \nabla^2 \psi = -q(p - n + N_d^+ - N_a^-) - \rho_s \quad (3.1)$$

$$\frac{\partial n}{\partial t} = \frac{1}{q} \vec{\nabla} \cdot J_n - U_n = F_n(\psi, n, p) \quad (3.2)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \vec{\nabla} \cdot J_p - U_p = F_p(\psi, n, p) \quad (3.3)$$

Here ψ is the intrinsic Fermi potential, q is the electron charge, ϵ_s is the permittivity of SiC, n and p are the electron and hole concentrations, N_d^+ and N_a^- are the ionized donor and acceptor impurity concentrations respectively and ρ_s is the surface charge density that may be present due to fixed charge in insulating materials or charged interface states. J_n and J_p are electron and hole current density respectively. Recombination-generation rate for electrons and holes are denoted by U_n and U_p respectively.

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From Boltzmann transport, J_n and J_p can be written as functions of the carrier concentrations and the quasi-Fermi potentials for electrons and holes, ϕ_n and ϕ_p respectively. Alternatively, J_n and J_p can be written as functions of ψ , n and p , consisting of drift and diffusion components:

$$\vec{J}_n = -q\mu_n n \vec{\nabla} \phi_n = -q\mu_n n \vec{\nabla} \psi + qD_n \vec{\nabla} n \quad (3.4)$$

$$\vec{J}_p = -q\mu_p p \vec{\nabla} \phi_p = -q\mu_p p \vec{\nabla} \psi - qD_p \vec{\nabla} p \quad (3.5)$$

In the above, μ_n and μ_p are electron and hole mobilities respectively, and D_n and D_p are electron and hole diffusivity respectively.

3.2.2 Physical Models and Parameters

To solve the DD equations for 4H-SiC devices, the low-field mobility, the field-dependent mobility, the Schottky barrier height, incomplete ionization of impurities, band gap and effective density of states, recombination and the impact ionization rate of 4H-SiC have to be considered. As for the model parameters, we have utilized those most recently published for 4H-SiC that provided the closest agreement with the experiment data. [62,63,64]

3.2.2.1 Mobility Models

The carrier mobilities μ_n and μ_p account for scattering mechanisms in electrical transport. Accurate determination of the field, temperature, and doping dependent mobility is crucial to device analysis and design. Medici contains several options with

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regard to mobility. The low field mobility in 4H-SiC is dependent on the doping and temperature and can be characterized by the following equation [65,66]:

$$\mu_0^{n,p} = \mu_{\min}^{n,p} + \frac{\mu_{\max}^{n,p} \left(\frac{T}{300} \right)^{\alpha_{n,p}} - \mu_{\min}^{n,p}}{1 + \left(\frac{N_{\text{total}}(x,y)}{N_{\text{ref}}^{n,p}} \right)^{\gamma_{n,p}}} \quad (3.6)$$

The subscripts and superscripts n, p represent the parameter values for electrons and holes respectively. $N_{\text{total}}(x,y)$ is the local total doping concentration. $N_{\text{ref}}^{n,p}$ and $\gamma_{n,p}$ are fitting parameters that reflect the dependence of mobility on ionized impurity scattering which arises from interactions with donor and acceptor ions, while $\mu_{\min}^{n,p}$ corresponds to the minimum mobility which occurs at degenerate doping levels. The parameters that we have used for 4H-SiC are shown in Table 3.1 [62,63]:

	Electrons (n)	Holes (p)
$\mu_{\min} \text{ (cm}^2\text{/Vs)}$	0	15.9
$\mu_{\max} \text{ (cm}^2\text{/Vs)}$	947	124
$N_{\text{ref}} \text{ (cm}^{-3}\text{)}$	1.94×10^{17}	1.76×10^{19}
α	- 2.15	- 2.15
γ	0.61	0.34

Table 3.1 The parameters of electrons and holes used in mobility model.

For the high field mobility, we apply the standard field dependent mobility Caughey-Thomas model for both electrons and holes [65,66]:

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$$\mu_{n,p} = \frac{\mu_0^{n,p}}{\left[1 + \left(\frac{\mu_0^{n,p} E^{n,p}}{\nu_s^{n,p}} \right)^{\beta_{n,p}} \right]^{1/\beta_{n,p}}} \quad (3.7)$$

where $E^{n,p}$ is the electric field in the direction of current flow, and $\nu_s^{n,p}$ is the saturation velocity. The parameter β accounts for the characteristics of the transition between low and high field mobility. The parameters used are as follows: [62,63]

$$\nu_s^n = 2.0 \times 10^7 \text{ cm/s}, \quad \nu_s^p = 2.0 \times 10^7 \text{ cm/s}, \quad \beta_n = 2, \quad \beta_p = 2.$$

From the low field and high field mobility models, the drift velocity (ν_n) versus electric field (E) relation for electrons in 4H-SiC can be determined,

$$\nu_n = \mu(E)E \quad (3.8)$$

3.2.2.2 Incomplete Ionization of Impurities

Poisson's equation (eq. 3.1) involves the ionized impurity concentrations N_d^+ and N_a^- in the expression for the space charge region in SiC [50]. This is because donors or acceptors in SiC do not ionize completely even at temperature higher than room temperature, just like the “freeze-out effect” in Silicon. Medici can treat this using Fermi-Dirac statistics with appropriate degeneracy factors g_c and g_v for the conduction and valance bands respectively. According to Fermi-like distribution [67], the density of ionized donors and acceptors can be expressed as

$$N_d^+ = \frac{N_d}{1 + g_c \cdot \exp\left(\frac{E_{Fn} - E_C + \Delta E_d}{k_B T}\right)} \quad (3.9)$$

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$$N_a^- = \frac{N_a}{1 + g_v \cdot \exp\left(\frac{E_v - E_{fp} + \Delta E_a}{k_B T}\right)} \quad (3.10)$$

where $g_c = 2$, $g_v = 4$, and ΔE_d and ΔE_a are the donor and acceptor impurity activation energies respectively. In 4H-SiC, the most common shallow donor and acceptor are nitrogen and aluminum respectively, with ΔE_d of 45meV and ΔE_a of 19.1meV. [21]

3.2.2.3 Band Gap and Effective Density of States

SiC is an indirect band gap semiconductor and 4H-SiC has the largest band gap among all the common SiC polytypes. [68] The dependence of band gap on temperature is not exactly known for 4H-SiC so far. In this work, with reference to Si, the band gap is assumed to have the following temperature dependence [40],

$$E_g(T) = E_g(300) + \alpha \left(\frac{300^2}{300 + \beta} - \frac{T^2}{T + \beta} \right) \quad (3.11)$$

where $E_g(300)$ is the band gap at room temperature and equal to 3.26eV, $\alpha = 4.59 \times 10^{-4}$, $\beta = 530$. [62,64] The effective densities of states in the conduction and valence band are described as

$$N_C(T) = N_C(300) \cdot \left(\frac{T}{300} \right)^{\delta_n} \quad (3.12)$$

$$N_V(T) = N_V(300) \cdot \left(\frac{T}{300} \right)^{\delta_p} \quad (3.13)$$

where $N_C(300) = 1.7 \times 10^{19}$, $N_V(300) = 2.5 \times 10^{19}$, $\delta_n = 146$ and $\delta_p = 30$. [62,64]

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3.2.2.4 Recombination

In this work, Shockley-Read-Hall (SRH) and Auger recombination are considered in the device simulation. Therefore, the recombination-generation rate U_n and U_p in eqs. (3.1) and (3.2) can be described as

$$U_n = U_p = U_{SRH} + U_{Auger} \quad (3.14)$$

SRH recombination is a process with phonon transitions via defects or traps located at an energy level (E_{trap}) near to midgap and its rate can be described as

$$U_{SRH} = \frac{np - n_i^2}{\tau_p \left[n + n_i \exp\left(\frac{E_{trap}}{kT}\right) \right] + \tau_n \left[p + n_i \exp\left(-\frac{E_{trap}}{kT}\right) \right]} \quad (3.15)$$

where τ_n and τ_p are the electron and hole life times respectively, and n_i is the intrinsic carrier concentration.

Auger recombination is a process in which the energy released from a direct recombination of an electron and a hole is transferred to another electron or hole. Its rate is given as follows

$$U_{Auger} = (C_n n + C_p p)(np - n_i^2) \quad (3.16)$$

where C_n and C_p are the Auger recombination coefficients for electrons and holes respectively. Their values at room temperature are given by $C_n = 7.0 \times 10^{-31} \text{cm}^6 \text{sec}^{-1}$ and $C_p = 2.0 \times 10^{-31} \text{cm}^6 \text{sec}^{-1}$. [62,64]

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3.2.2.5 Impact Ionization

Electron-hole pair generation from impact ionization is one of the phenomena that limits high voltage and thus high power device operation. The wide band gap of 4H-SiC inhibits impact ionization in MESFETs and thereby making it a very promising device for high field applications. The generation rate for electron-hole pairs due to impact ionization can be expressed by

$$G^H = \alpha_{n,ii} \frac{|\vec{J}_n|}{q} + \alpha_{p,ii} \frac{|\vec{J}_p|}{q} \quad (3.17)$$

where $\alpha_{n,ii}$ and $\alpha_{p,ii}$ are the electron and hole ionization coefficients respectively. The ionization coefficients [69] can be expressed in terms of the local electric field according to

$$\alpha_{n,ii} = \alpha_{n,ii}^{\infty}(T) \cdot \exp\left(-\frac{b_n}{E_{//}}\right) \quad (3.18)$$

$$\alpha_{p,ii} = \alpha_{p,ii}^{\infty}(T) \cdot \exp\left(-\frac{b_p}{E_{//}}\right) \quad (3.19)$$

where $E_{//}$ is the electric field components in the direction of current flow, and the factors $\alpha_{n,ii}^{\infty}(T)$ and $\alpha_{p,ii}^{\infty}(T)$ are given by:

$$\alpha_{n,ii}^{\infty}(T) = \alpha_0^n + \alpha_1^n \cdot T \quad (3.20)$$

$$\alpha_{p,ii}^{\infty}(T) = \alpha_0^p + \alpha_1^p \cdot T \quad (3.21)$$

The coefficients used for electrons are: $\alpha_0^n = 1.66 \times 10^6 \text{ cm}^{-1}$, $\alpha_1^n = 0$ and $b_n = 1.273 \times 10^7 \text{ V/cm}$, and for holes are: $\alpha_0^p = 5.18 \times 10^6 \text{ cm}^{-1}$, $\alpha_1^p = 1.07 \times 10^4 \text{ cm}^{-1} \text{ K}^{-1}$ and $b_p = 1.4 \times 10^7 \text{ V/cm}$. [63,64]

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3.2.2.6 Boundary Conditions

Ohmic contacts are characterized as simple Dirichlet boundary conditions, where the surface potential and electron and hole concentrations (ψ_s , n_s , p_s) are assigned to constant values. The minority and majority carrier quasi-Fermi potentials are equal and are set to the applied bias of that electrode, that is, $\phi_n = \phi_p = V_{applied}$. The potential ψ_s is fixed at a value consistent with zero space charge.

Schottky contacts to semiconductors are characterized by the work function (W_m) of the electrode metal and an optional surface recombination velocity. The surface potential at a Schottky contact is given by [40]

$$\psi_s = \chi_{semi} + \frac{E_g}{2q} + \frac{kT}{2q} \ln\left(\frac{N_c}{N_v}\right) - W_m + V_{applied} \quad (3.22)$$

where χ_{semi} is the electron affinity of the semiconductor, E_g is band gap, $V_{applied}$ is applied gate voltage, and N_c and N_v are the effective density of states for the conduction and valence bands respectively.

In the case of Schottky contact, the quasi-Fermi potentials for electrons and holes ϕ_n and ϕ_p are no longer equal to $V_{applied}$. The boundary conditions are defined by the current boundary conditions at the surface [40],

$$J_{sn} = q v_{sn} (n_s - n_{eq}) \quad (3.23)$$

$$J_{sp} = q v_{sp} (p_s - p_{eq}) \quad (3.24)$$

where J_{sn} and J_{sp} are the electron and hole current densities at the contact, n_s and p_s are the actual surface electron and hole concentrations respectively and n_{eq} and p_{eq} are

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the equilibrium electron and hole concentrations respectively, assuming infinite surface recombination velocities ($\phi_n = \phi_p = V_{applied}$). The surface recombination velocities for electrons and holes, v_{sn} and v_{sp} respectively, are calculated by the expressions

$$v_{sn} = \frac{A_n^* \cdot T^2}{q \cdot N_C} \quad v_{sp} = \frac{A_p^* \cdot T^2}{q \cdot N_V}$$

where A_n^* and A_p^* are the effective Richardson constants for electrons and holes respectively which take into account mechanical reflection and tunneling. The coefficients used for 4H-SiC are as follows: $\chi_{semi} = 3.8eV$, $A_n^* = 110 A/(K \cdot cm)^2$, $A_p^* = 30 A/(K \cdot cm)^2$. [63,64]

Using the models and parameters presented above, the I-V characteristics of SiC MESFET for the gate length of $1.5\mu m$ has been the simulated and compared with the experimental data [17] as shown in Fig. 3.1. It should be noted that the simulated results are in good agreement with the experimental data [17].

Fig. 3.1 The drain current versus the drain voltage for $L_g = 1.5\mu m$ [17].

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3.3 Three-Region Model

3.3.1 Background

Compared to numerical simulation, analytic simulation is a much faster and more economical method in device design. Analytical models can also provide a convenient and easy way to gain insight into the device physics and performance. Recently, Tsap [70] and Murray *et al.* [71] have derived analytical models for SiC based MESFETs in terms of Pucel-Haus-Statz (PHS) model [72] where the channel under the gate is divided into two regions and both field dependent mobility and velocity saturation are incorporated. Murray *et al.* used the Caughey-Thomas model [71,73] to replace the piece-wise linear velocity-field characteristics used in the PHS model, to describe the velocity-field characteristics of SiC. This is important as SiC, being a wide band gap semiconductor, reaches velocity saturation only at much higher field compared to GaAs. S. S. Mukherjee *et al.* [74] proposed an analytical model that includes trapping and thermal effects to fit the experimental results for 1 μ m gate length MESFET devices. All the above models suffer from the drawback that they have neglected the large voltage drop across the high field region between the gate and the drain. This effect is important and cannot be omitted for SiC MESFETs, especially for short channel devices, due to the high drain voltage involved. Indeed, two-dimensional numerical simulation [75] for GaAs MESFET has shown that the voltage drop across this ungated section may be larger than that across the high field region under the gate. H.L. Lv *et al.* [76] have considered the effect of the region between the gate and the drain and proposed a multi-parameter mobility model to fit the I-V characteristics for SiC MESFETs. However, their model is based on that the high field peak velocity exists in the velocity – field relation, which is applicable only for III-V

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semiconductors but not SiC. Besides, all these models did not include the incomplete ionization of dopants that is important for SiC due to the larger ionization energies.

In this work, we propose an improved three-region analytical model for short-channel SiC MESFETs that takes into account the two regions in the channel under the gate and the ungated high field region between the gate and the drain. In this model, the velocity-field relation based on the Caughey-Thomas model is used in the low field region. The parasitic resistances are included to solve for the channel current. For the high-field saturation region, which begins and ends at the points where the electric field is equal to the saturation field of SiC, the depletion depth is assumed to be a constant. Incomplete ionization of dopants and the trap effect arising from the substrate are also incorporated in our model. Using this analytical method, we have simulated the I-V characteristics of SiC MESFET, and obtained excellent agreement when compared with recently published experimental results [77].

3.3.2 Detailed Modeling

Poor low field electron mobility results in a larger source resistance and lower transconductance in SiC MESFETs compared to GaAs based devices [78]. This drawback can be partially offset by the high breakdown field strength of SiC that allows the MESFETs to be operated under extremely high electric fields, driving the electrons into their saturation velocity across a large part of the conducting channel. However, higher drain voltage will result in larger depletion region between the gate and the drain and hence higher voltage drop in the channel, which cannot be omitted in the modeling of the device performance. Based on the above consideration, a three-region analytical model is proposed to more accurately model SiC MESFETs. Figure

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3.2 shows the cross section of a SiC MESFET where the channel is saturated under high drain voltage. The channel is divided into such three regions labeled as region *I*, *II* and *III*. In region *I*, the electric field is low and the electron velocity is less than the electron saturation velocity (v_s). In this region, the velocity-field relation based on the Caughey-Thomas model is used to describe the electron transport characteristic. Once the electron velocity reaches v_s and cannot be further increased, the electric field at this point is called the saturation electric field E_s and the channel is saturated. With increasing drain voltage, along the direction from the source to the drain, the electric field in the channel arrives at the peak value at the end of the gate nearer to the drain side, and then decreases. The saturated channel ends at where the electric field decreases to E_s . The saturation regions below the gate and the ungated region between the gate and the drain are called region *II* and region *III*, respectively.

Fig. 3.2 The cross-section of a SiC MESFET showing the three regions formed under a large drain voltage.

The parasitic source and drain resistances are also included in Fig. 3.2. R_{dc} refers to the parasitic source and drain resistances that include the contact resistance and the SiC resistance under the source and the drain regions. The source resistance $R_S = R_{dc}$

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+ R_{S0} , where R_{S0} is a function of V_{gs} . Similarly, the drain resistance $R_D = R_{dc} + R_{D0}$ where R_{D0} is a function of V_{gs} and V_{ds} . A parasitic resistance R_b is added parallel to the channel to take into account leakage current arising from the depletion region between the channel and the buffer layers and the trap effects from the buffer layer or the substrate.

It should be noted that the relatively large ionization energy of the commonly found nitrogen shallow donors in SiC [79] leads to incomplete ionization of the donors in the channel, resulting in increased parasitic resistances and lower drain currents for a given channel doping level. However, this effect has not been included in the analytical models published so far. The saturation velocity (v_s) of 1.25×10^7 cm/s extracted by M.W. Huang et al [77] from his simulator is much lower than the measured value of 2.2×10^7 cm/s [80]. One possible reason for the discrepancy can be that they did not include incomplete ionization model in their simulator. In order to accurately model the I-V characteristics, incomplete ionization of dopants is included in our proposed three-region model. According to eq(3.9), the density of ionized donors can be rewritten as

$$N_d^+ = \frac{N_d}{1 + g_c \exp\left(\frac{E_F - E_D}{k_B T}\right)} \quad (3.25)$$

where E_D is the donor level. The electron concentration n_0 is given by

$$n_0 = N_d^+ \quad (3.26)$$

on the other hand

$$n_0 = N_c \exp\left(-\frac{E_C - E_F}{k_B T}\right) \quad (3.27)$$

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where N_C and E_C are the effective density of the states in the conduction band and the conduction band edge respectively.

Combining eqs(3.25), (3.26) and (3.27), we obtain

$$N_d^+ = n_0 = \frac{N_C}{2g_c} \exp\left(-\frac{E_C - E_D}{k_B T}\right) \left(\sqrt{1 + 4g_c \frac{N_D}{N_C} \exp\left(\frac{E_C - E_D}{k_B T}\right)} - 1 \right) \quad (3.28)$$

where $N_C = 1.7 \times 10^{19} \text{ cm}^{-3}$, thermal energy $k_B T = 0.02586 \text{ eV}$ and the donor activation energy $E_{DA} = E_C - E_D = 0.045 \text{ eV}$ [50]. Figure 3.3 shows the relations between the calculated ionized dopant concentration or electron density N_d^+ using eq(3.28) and the doping concentration in the range of $1 \times 10^{17} - 5 \times 10^{17} \text{ cm}^{-3}$ for different E_{DA} at room temperature. This is the doping levels of interest for practical SiC MESFETs. It can be seen that larger ionization energy E_{DA} results in lower N_d^+ , especially for larger doping level.

Fig. 3.3 Calculated electron density versus the dopant concentration for different donor activation energy.

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3.3.3 I-V Characteristics

For a low drain voltage applied to the MESFET, the channel layer can be treated as one-dimension to simplify the Poisson equation shown in eq(3.1). In this case, the channel potential $\psi(y)$ can be written as

$$\frac{\partial^2 \psi(y)}{\partial y^2} = -\frac{qN_d^+}{\epsilon_s} \quad (3.29)$$

It is subjected to the following boundary conditions:

$$\psi(0) = V_{gs} - V_{bi} \quad (3.30a)$$

$$\left. \frac{d\psi}{dy} \right|_{y=h} = 0 \quad (3.30b)$$

where $\psi(0)$ is the channel potential at the metal – SiC interface, V_{gs} is the gate-source voltage, V_{bi} is the built-in potential and h is the depletion width measured from the metal-SiC interface. Integrating eq(3.29) twice and applying eqs(3.30a) and (3.30b), we can solve eq(3.29) and obtain the following expression for the channel potential:

$$\psi(y) = -\frac{qN_d^+}{2\epsilon_s} y^2 + \frac{qN_d^+ h}{\epsilon_s} y + V_{gs} - V_{bi} \quad (3.31)$$

Therefore, the width of the depletion region under the gate can be written as

$$h(x) = \sqrt{\frac{2\epsilon}{qN_d} [V(x) - V_{gs} + V_{bi}]} \quad (3.32)$$

where $V(x)$ is the channel potential at any point x . The channel current I_c at any point x can be described as

$$I_c = qv(E)N_d A = qv(x)N_d W[a - h(x)] \quad (3.33)$$

where W and a are the channel width and thickness respectively.

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The velocity-electric field (v - E) characteristic in SiC is described using the Caughey-Thomas model, [80,81]

$$v(E) = \mu(E) \cdot E(x) = \frac{\mu_0 E(x)}{1 + \frac{\mu_0 E(x)}{\gamma_s}} \quad (3.34)$$

where γ is a fitting parameter that accounts for the bowing of the v - E characteristics. μ_0 is the low field mobility and its dependence on the doping concentration N_d at room temperature can be described as [67]

$$\mu_0 = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left(\frac{N_d}{N_r}\right)^\alpha} \quad (3.35)$$

where N_r and α are fitting parameters that reflect the dependence of mobility on impurity scattering arising from the interactions with donor and acceptor ions, while $\mu_{\min}$ and $\mu_{\max}$ are respectively the minimum mobility which occurs at degenerate doping levels and the maximum mobility in intrinsic SiC.

Under low drain voltage, the electric field in the channel is less than E_s and only region I exists. The depletion width under the gate nearer to the source (h_0) and the drain (h_1) are deduced from eq(3.32) and normalized to the channel thickness (a),

$$u_0 = \frac{h_0}{a} = \frac{1}{a} \sqrt{\frac{2\epsilon_s}{qN_d} (V_{bi} - V_{gs} + I_c R_S)} = \sqrt{\frac{V_{bi} - V_{gs} + I_c R_S}{V_p}} \quad (3.36)$$

$$u_1 = \frac{h_1}{a} = \frac{1}{a} \sqrt{\frac{2\epsilon_s}{qN_d} (V_{ds} + V_{bi} - V_{gs} - I_c R_D)} = \sqrt{\frac{V_{ds} + V_{bi} - V_{gs} - I_c R_D}{V_p}} \quad (3.37)$$

where

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$$V_p = \frac{qN_d^+ a^2}{2\epsilon_s} \quad (3.38)$$

In the linear mode under small drain voltage, the channel current I_c given by eq(3.33) can be expressed as

$$I_c = \frac{I_p [3(u_1^2 - u_0^2) - 2(u_1^3 - u_0^3)]}{1 + z(u_1^2 - u_0^2)} \quad (3.39)$$

where

$$z = \frac{qN_d^+ a^2 \mu_0}{2\epsilon_s L_g \gamma v_s} \quad (3.40)$$

$$I_p = \frac{q^2 N_d^{+2} \mu_0 W a^3}{6\epsilon_s L_g} \quad (3.41)$$

and L_g is the gate length.

With increasing drain voltage, electrons are accelerated and reach saturation velocity.

Therefore, the channel current is saturated and given as follows according to eq(3.33)

$$I_{csat} = q N_d^+ W a \gamma v_s (1 - u_s) \quad (3.42)$$

where u_s is the normalized depletion width at saturation current.

Based on eqs(3.39) and (3.42), u_s and I_c can be solved by iteration. The drain saturation voltage can be found using eq(3.37)

$$V_{Dmax} = u_s^2 V_p - V_{bi} + V_{gs} + I_c R_D \quad (3.43)$$

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When the drain voltage is larger than V_{Dmax} , the channel is under the saturation condition as shown in Fig. 3.1, and can be divided into three regions. Region *I* with a length of L_1 nearer the source is the low field region where $v < v_s$. Therefore, the analysis of this region follows the linear mode as described above. For the high field saturation region (regions *II* and *III*), which begins and ends at the points where $E=E_s$, the depletion depth h_s is assumed to be uniform. Note that region *II* is under the gate with a length of L_2 and region *III* is between the gate and the drain with a length of L_3 .

For region *I*, according to the analysis above, the channel current is given by

$$I_c = \frac{I_p \left(\frac{L_g}{L_1} \right) [3(u_s^2 - u_0^2) - 2(u_s^3 - u_0^3)]}{1 + z \left(\frac{L_g}{L_1} \right) (u_s^2 - u_0^2)} \quad (3.44)$$

where

$$u_s = \frac{h_s}{a} = \frac{1}{a} \sqrt{\frac{2\epsilon_s}{qN_d^+} (V(L_1) + V_{bi} - V_{gs})} = \sqrt{\frac{V(L_1) + V_{bi} - V_{gs}}{V_p}} \quad (3.45)$$

On the other hand, in the saturation region (region *II* or *III*), referring to eq(3.42), the channel current can be expressed as

$$I_{csat} = qN_d^+ W a \gamma v_s (1 - u_s) \quad (3.46)$$

As the channel current should be uniform in the channel, we equate eq(3.44) and (3.46) and obtain

$$L_1 = L_g z \left[\frac{(u_s^2 - u_0^2) - \frac{2}{3}(u_s^3 - u_0^3)}{\gamma(1 - u_s)} - (u_s^2 - u_0^2) \right] \quad (3.47)$$

At the junction of regions *I* and *II*, the potential can be obtained from eq(3.45)

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$$V(L_1) = V_p u_s^2 - V_{bi} + V_{gs} \quad (3.48)$$

At this point, electrons have reached saturated velocity and the corresponding electric field is the saturation field

$$E(L_1) = E_s = 2\gamma v_s / \mu_0 \quad (3.49)$$

The potential drop in regions *II* and *III* and L_3 can be analytically solved using two-dimensional Poisson equation based on the method developed by Chang et al [82] for GaAs MESFETs. The process is simpler for SiC MESFETs as high field peak velocity does not exist in SiC. Using Laplace's equation and boundary conditions, we obtain the potential drop across regions *II* and *III*

$$V(L_g + L_3) - V(L_1) = \frac{1}{3} E_s L_3 \left(2 \exp \frac{\pi L_2}{2h_s} + 1 \right) + \left(\frac{2}{\pi} h_s + \frac{1}{3} L_3 \right) E_s \sinh \frac{\pi L_2}{2h_s} \exp \left(-\frac{\pi L_3}{2h_s} \right) \quad (3.50)$$

and an equation involving L_3

$$L_3^2 \left(\frac{2V_p h_s}{a^2} - E_s \cosh \frac{\pi L_2}{2h_s} \right) = h_s^2 E_s \left(\exp \frac{\pi L_2}{2h_s} - 1 - \sinh \frac{\pi L_2}{2h_s} \exp \left(-\frac{\pi L_3}{2h_s} \right) \right) \quad (3.51)$$

Note that $V(L_1)$ and $V(L+L_3)$ refer to the potentials at the edge of region *II* nearer to the source and the edge of region *III* nearer to the drain respectively. The latter can be described as

$$V(L_g + L_3) = V_{ds} - I_c R_D \quad (3.52)$$

Using eqs(3.47), (3.50) and (3.51), and combining eqs(3.46), (3.48), (3.49) and (3.52), we can solve for L_1 , L_2 ($L_2 = L_g - L_1$), L_3 and the channel current I_c by iteration. Incorporating the parallel resistance R_b arising from the buffer layer, the drain current can be obtained

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$$I_D = I_c + V_{ds} / R_b \quad (3.53)$$

3.3.4 Results and Discussion

Using the three-region analytical model developed above, we simulated the I-V characteristics of a SiC MESFET with 0.7 μm gate length. The detailed model and device structure parameters [71,77] are shown in Table. 3.2. Figure 3.4 shows our simulated results using the three-region model and together with experimental data measured for such a device [51]. For comparison, the calculated results based on Murray's two-region model [71] are also included in the figure. It is noted that Murray's model is very coarse and the simulation results could not fit the experimental data well. This is likely due to the fact that the model did not consider the ungated saturation region between the gate and the drain and the parasitic resistances. In contrast the simulated I-V characteristics based on our proposed three-region model are in excellent agreement with the experimental data.

$\epsilon_s = 9.7 \epsilon_0$	$N_d = 1.7 \times 10^{17} / \text{cm}^3$
$\epsilon_0 = 8.85 \times 10^{-14} \text{F/cm}$	$a = 0.26 \mu\text{m}$
$\mu_{min} = 40 \text{cm}^2/\text{Vs}$	$L_g = 0.7 \mu\text{m}$
$\mu_{max} = 950 \text{cm}^2/\text{Vs}$	$L_{gs} = 0.3 \mu\text{m}$
$N_{ref} = 1.94 \times 10^{17} / \text{cm}^3$	$L_{gd} = 0.8 \mu\text{m}$
$\alpha = 0.61$	$W = 332 \mu\text{m}$
$v_s = 2 \times 10^7 \text{cm/s}$	$R_{dc} = 10 \Omega$
$V_{bi} = 1.1 \text{eV}$	$R_p = 2800 \Omega$

Table 3.2 The structural and device parameters used in the simulation.

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Fig. 3.4 Comparison of the simulated I-V characteristics using the three-region model, Murray's two-region model [71] and experimental data [51].

Using the three-region model, we also simulated I-V characteristics of a SiC MESFET we fabricated. Table 3.3 shows the detailed model and device structure parameters. The fabrication process will be presented in Chapter 4 in details. The simulated I-V characteristics are in good agreement with the measured curve as shown in Fig. 3.5.

$\epsilon_s = 9.7 \epsilon_0$	$N_d = 2.4 \times 10^{17} / \text{cm}^3$
$\epsilon_0 = 8.85 \times 10^{-14} \text{F/cm}$	$a = 0.20 \mu\text{m}$
$\mu_{min} = 40 \text{cm}^2/\text{Vs}$	$L_g = 1.0 \mu\text{m}$
$\mu_{max} = 950 \text{cm}^2/\text{Vs}$	$L_{gs} = 0.5 \mu\text{m}$
$N_{ref} = 1.94 \times 10^{17} / \text{cm}^3$	$L_{gd} = 1.5 \mu\text{m}$
$\alpha = 0.61$	$W = 50 \mu\text{m}$
$v_s = 2 \times 10^7 \text{cm/s}$	$R_{dc} = 5 \Omega$
$V_{bi} = 1.1 \text{eV}$	$R_p = 500 \Omega$

Table 3.3 The structural and fabricated device parameters used in the simulation for our own fabricated SiC MESFET.

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Fig. 3.5 Comparison of the simulated I-V characteristics using the three-region model and measured data for our own fabricated SiC MESFET.

3.4 Determination of RF Characteristics

Scattering or S parameters are commonly measured for operating frequencies in the microwave range since the measurement of external voltages and currents, and the realization of the required short-circuit conditions become more complicated. S parameters are defined as ratios of the powers of traveling waves: [46]

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad \begin{aligned} b_1 &= s_{11}a_1 + s_{12}a_2 \\ b_2 &= s_{21}a_1 + s_{22}a_2 \end{aligned} \quad (3.54)$$

where the subscripts 1 and 2 designate the input and the output network respectively, a and b are the powers of incoming (or incident) and outgoing (or reflected) waves. Figure 3.5 shows the two-port network with the incident (a_1, a_2) and reflected (b_1, b_2) waves. Figure 3.6 shows the test structure used for S-parameter measurements of two-port systems. [83]

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Fig. 3.6 Two-port network characterized by S parameters.

Medici allows AC small-signal analysis as a post-processing step after obtaining a DC solution. Gate and Drain terminals with a characteristic transmission line impedance of 50Ω are used for S parameters analysis both in the simulation and measurement. Therefore, we have

s_{11} : input reflection coefficient of 50Ω terminated output.

s_{21} : forward transmission coefficient of 50Ω terminated output.

s_{12} : reverse transmission coefficient of 50Ω terminated input.

s_{22} : output reflection coefficient of 50Ω terminated input.

Fig. 3.7 Illustration of on-wafer high frequency measurement for a two-port system [83].

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Based on the extracted S parameters from the measurement or simulator, the RF characteristics of the device can be obtained. Stability factor (k) and other gain parameters can be computed using the following equations [84]:

Stability Factor (k)

$$k = \frac{1 + |s_{11}s_{22} - s_{12}s_{21}|^2 - |s_{11}|^2 - |s_{22}|^2}{2|s_{12}s_{21}|} \quad (3.55)$$

For $k > 1$, the transistor is unconditionally stable and the Maximum Stable Gain (MSG) is given by

$$MSG = \frac{|s_{21}|}{|s_{12}|} \quad (3.56)$$

For $k < 1$, the transistor is conditionally stable and unintended oscillations may occur.

The Maximum Available Gain (MAG) is given by

$$MAG = \frac{|s_{21}|}{|s_{12}|} (k - \sqrt{k^2 - 1}) \quad (3.57)$$

The Forward Current Gain (h_{21}) can be expressed as

$$h_{21} = \frac{-s_{21}}{(1 - s_{11})(1 + s_{22}) + s_{12}s_{21}} \quad (3.58)$$

$$|h_{21}| [dB] = 20 \log_{10} |h_{21}| \quad (3.59)$$

In the above, the absolute value of the current gain is used because in some cases h_{21} may be negative, which means that there is a 180° phase difference between the input and output signals.

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The cutoff frequency f_T is the frequency at which the magnitude of h_{21} equals unity or zero decibel. By setting $h_{21} = 1$ we can obtain f_T , which can also be expressed as [85]

$$f_T \approx \frac{g_m}{2\pi (C_{gs} + C_{gd})(1 + g_{ds}R_S) + C_{gd}g_mR_S} \quad (3.60)$$

The maximum unilateral transducer power gain (U) is given by [84]

$$U = \frac{|s_{21}|^2}{(1 - |s_{11}|^2)(1 - |s_{22}|^2)} \quad (3.61)$$

$$U[dB] = 10 \log_{10} U \quad (3.62)$$

The maximum frequency of oscillation f_{max} is the frequency at which the unilateral power gain U equals unity. By setting $U = 1$, we can obtain f_{max} which can also be expressed as [85]

$$f_{max} \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})} \frac{1}{\left[4g_{ds}(R_i + R_S + R_G) + 4g_mR_G \frac{C_{gd}}{C_{gs} + C_{gd}} \right]^{\frac{1}{2}}} \quad (3.63)$$

CHAPTER 4 FABRICATION AND CHARACTERIZATION OF SiC MESFETS

Chapter 4

Fabrication and Characterization of SiC MESFETs

4.1 Process Development for SiC MESFETs

In principle, the process technology based on SiC is similar to that of conventional semiconductors such as Si and GaAs. However, there are some differences due to the inherent material properties of SiC. For example, no wet chemical solutions under standard conditions can etch SiC at a rate sufficient enough for practical application, and hence plasma etching is the most practical technique used for SiC. Also, temperatures as high as 2000°C is required to activate dopants and remove the irradiation induced damage after ion implantation in SiC. Therefore, annealing equipment for conventional semiconductors cannot be used.

In this work, a process has been developed for SiC MESFET fabrication. The main fabrication process steps begin with a 4H-SiC wafer grown with several epilayers and include mesa isolation and channel recess etching; thermal oxidation; source and drain contact formation, and gate contact formation. The lift-off process and self-aligned process are used. In this chapter, the details of each process step will be discussed.

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4.1.1 Wafer Preparation and Cleaning

The starting wafers purchased from CREE Inc. comprise a vanadium doped semi-insulating (SI) substrate, a p-type buffer layer (0.5 μm thick; doping concentration $N_a = 1.0 \times 10^{15} \text{ cm}^{-3}$), a n-type channel layer and a high doped ($> 1.0 \times 10^{19} \text{ cm}^{-3}$) n-type cap layer grown consecutively on top of the substrates as shown in Fig. 4.1. Three types of channel layer are used in this work and they are (i) conventional channel layer with a thickness of 0.2 μm and a doping concentration of $2.4 \times 10^{17} \text{ cm}^{-3}$, (ii) narrow channel layer with a thickness of 0.08 μm and a doping concentration of $8.0 \times 10^{17} \text{ cm}^{-3}$ and (iii) dual-channel layer which has a low doped upper channel layer with a thickness of 0.12 μm and a doping concentration of $1.4 \times 10^{17} \text{ cm}^{-3}$ and a high doped lower channel layer with a thickness of 0.12 μm and a doping concentration of $5.2 \times 10^{17} \text{ cm}^{-3}$. The multi-epi layers were analyzed using secondary ion mass spectrometry (SIMS) measurements by Charles Evans & Associates. The wafers were diced into $1\text{cm} \times 1\text{cm}$ size prior to process fabrication.

Fig. 4.1 SiC wafer with epilayers prior to process fabrication.

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First the diced samples were degreased in acetone, isopropanol, and de-ionized (DI) water under ultrasonic conditions for 15 mins each. This is to remove surface organic contaminants which may come from dicing or shipment, while isopropanol alcohol (IPA) is mainly used for degreasing and dissolving the acetone. After that, the wafers were cleaned using Radio Corporation of America (RCA) cleaning process. The RCA cleaning procedure comprises three steps as shown in Table 4.1. Standard clean 1 (SC1) with a 1:1:5 of $\text{NH}_4\text{OH} : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$ solution was used to remove insoluble organic contaminants at 80°C for 15 mins. Dilute HF (DHF) with a 1:50 of $\text{HF} : \text{H}_2\text{O}$ was then used to strip any thin silicon dioxide surface layer. Finally standard clean 2 (SC2) with a 1:1:5 of $\text{HCl} : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$ was applied to remove ionic and heavy metal atomic contaminants. After the RCA clean, the wafers were rinsed by flowing DI water and then dried in an oven for 30 mins at 110°C . Up to this point the wafers were ready for further processing.

Steps	Recipe details	Temperature ($^\circ\text{C}$)	Time
SC1	$\text{NH}_4\text{OH} : \text{H}_2\text{O}_2 : \text{H}_2\text{O} = 1:1:5$	80	15 mins
DHF	$\text{HF} : \text{H}_2\text{O} = 1:50$	25	30 secs
SC2	$\text{HCl} : \text{H}_2\text{O}_2 : \text{H}_2\text{O} = 1:1:5$	80	15 mins

Table 4.1 The procedure of RCA clean.

4.1.2 Mesa Isolation and Channel Recess Etching

Strong Si–C bonding makes SiC attractive for applications in harsh environments, however, it is a significant drawback when comes to device fabrication. No wet chemical under standard conditions can etch SiC at a rate sufficient enough for

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practical applications. [7] The only techniques for etching SiC include molten salt fluxes, hot gases, electrochemical processes and plasma etching. [86,87] Among them plasma etching is the most successful and mature technique and plays a crucial role in SiC device fabrication in terms of device pattern transfer.

Many plasma etching techniques have been studied including reactive ion etching (RIE), [87,88] inductively coupled plasma (ICP) etching, [89,90] and electron cyclotron resonance (ECR) plasma etching [91,92] etc. Compared to RIE, ICP and ECR provide higher etch rate and better surface quality due to their higher plasma density and the decoupling of ion energy and ion flux. However, RIE is still one of the most widely used etching techniques due to its simplicity, and plays an important role in device isolation and gate recess etching.

In this work, a RIE system using a 13.56MHz r.f. power source was used to etch SiC using a fluorine based gas mixture of CHF_3 and O_2 . Oxygen was added to enhance the active fluorine concentration and increase the SiC etch rate. The basic chemical reactions in the plasma are summarized below [87]

In the harsh plasma ambient, suitable masks must be selected for the etching process. A positive photoresist AZ1518 (1.8 μm) and Ni metal (200nm) were tested and compared. For Ni mask, a thin Ti layer (20nm) was added to improve adhesion between the mask and the SiC substrate since a thin pure Ni layer can peel off easily.

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It can also help remove the metal mask easily and completely after the RIE process by immersing into diluted HF solution. SiC wafers covered with these two masks were etched for 12 mins and the detailed process parameters are shown in Table 4.2 [93,94].

RF power	200W
Reflect power	1~ 3W
CHF3 flow rate	8sccm
O2 flow rate	2sccm
Self-bias	-342 ~ -348V
Chamber pressure	~100mTorr
Etching rate	~ 17nm/min

Table 4.2 Process parameters for RIE etching [93,94].

It was found that the photoresist is not suitable as a mask for SiC etching, since the etch rate of the photoresist is more than ten times faster than that of SiC. Besides, the photoresist may also contaminate the etched region during the process due to the ion bombardment. For Ni mask, the etching selectivity of SiC to Ni is more than 10 and it can withstand the harsh RIE ambient. Therefore, Ti/Ni mask structure was employed for mesa and channel recess etching in this work.

Ti/Ni mask layer was deposited on the wafers using lift-off technique which is the most popular process employed for discrete low noise device fabrication. In this work, photoresist AZ 5214E was used to create a negative wall profile using its image reversal property although in fact it is a positive photoresist. Typically, the thickness

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of the resist is about 1.4 μm when the spinning speed is set at 4000 rpm during the coating.

Figure 4.2 shows the detailed process flow for the lift-off technique. In Fig. 4.2(a), a layer of AZ 5214E is coated onto a clean wafer and prebaked at 105°C on a hotplate for 95 seconds. The mask pattern is then transferred to the resist using the Karl Suss mask aligner at exposure energy of 14mJ/sec for 4 secs, as shown in Fig. 4.2(b). After that the wafer is hard baked in an oven at 110°C for 8 minutes. This is a very important step since a special crosslinking agent in the resist formulation becomes active in the exposed areas, making it insoluble in the developer and no longer light sensitive. It should be noted that this reaction is active only for the hard bake temperature between 110°C and 130°C. On the other hand, the unexposed areas still behave like a normal unexposed positive photoresist. After the hard bake, the wafer is then subject to flood expose (without mask) as shown in Fig. 4.2(c). The unexposed areas in the first UV exposure are dissolved in standard developer for positive photoresist, leaving behind the crosslinked areas remained as shown in Fig. 4.2(d). Image reversal is therefore achieved and the overall result is the formation of a negative image of the mask pattern. After that, metal will be directly deposited on top of the patterned photoresist using e-beam evaporation as shown in Fig. 4.2(e). This is followed by lifting off of unwanted metal by dissolving the underlying photoresist with acetone. IPA is then used for dissolving the acetone. Figure 4.2(f) shows the final pattern formed.

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Fig. 4.2 The process flow for lift-off technique.

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Using the lift-off technique, the metal mask combined with 20nm Ti and 200nm Ni was deposited on the SiC wafer to cover the active region as shown in Fig. 4.3(a). After that the RIE process was used to etch all the SiC epilayers to reach the semi-insulating substrate to form mesa isolation. The metal mask was then removed using DHF and the wafer was cleaned using the RCA process. Figure 4.3(b) shows the active region formed for a single MESFET device. Similarly, metal mask was deposited using the lift-off process and the channel region was opened for recess etching as shown in Fig. 4.3(c). The n^+ top layer and a part of channel layer were etched by RIE and then the metal mask was removed as shown in Fig. 4.3(d). Figure 4.4 shows the optical micrograph of the device with a double-finger gate after channel recess etching.

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Fig. 4.3 Process flow for mesa isolation and channel recess etching: (a) metal mask deposition for mesa isolation using lift-off process; (b) mesa isolation by RIE; (c) metal mask for channel recess etching using lift-off process; (d) channel recess etching by RIE.

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Fig. 4.4 The optical micrograph of the device with the double-finger gate after mesa isolation and channel recess etching.

4.1.3 Thermal Oxidation

Surface damage on the wafer arising from the RIE etching can degrade the electrical performance of SiC devices. Therefore, a layer of sacrificial thermal oxide was grown and subsequently etched to remove any etch-induced damage. Following that, a thick thermal oxide was grown to form good isolation as shown in Fig. 4.5. Thermal oxidation of the wafers was carried out in a Lindburg furnace using ultra-pure O₂ (99.999%) at 1150°C. An oxide layer of 50 nm can be grown in about 6 hours.

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Fig. 4.5 Thermal oxidation.

4.1.4 Formation of Source and Drain Contacts

After thermal oxidation, the oxide layer on the source and drain regions need to be removed so that ohmic contacts can be formed. The source and drain mask was used to pattern photoresist and etch oxide. This photoresist mask was concurrently used to form source and drain metal using lift-off process. This is the so-called self-aligned process.

The self-aligned technique is frequently used for both digital and analog ICs with either epitaxial or implanted active layers. The steps involved as shown in Fig. 4.6 are as follows: (a) SiC wafer with an oxide layer coated by AZ 5214 photoresist; (b) the mask pattern is transferred to the resist using the image reversal property of AZ 5214E; (c) the oxide layer is etched with the photoresist mask in dilute HF solution ($\text{HF} : \text{NH}_4\text{F} : \text{H}_2\text{O} = 1:1:10$) with an etch rate of about 50nm/min; (d) and (e) show the normal lift-off process. Finally the metal was deposited on the SiC wafers at where the oxide was removed.

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Fig. 4.6 The process flow for self-aligned technique.

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Using the self-aligned technique, the source and drain metal of 200nm Ni was deposited as shown in Fig. 4.7. Figure 4.8 shows the picture of the double-finger gate MESFET under the optical microscope after the source and drain metal deposition.

Fig. 4.7 Source and drain metal deposition using self-aligned process.

Fig. 4.8 Source and drain metal deposition of a double-finger gate MESFET.

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Post metallization annealing of the source and the drain contacts was carried out at 1000°C for 1 min in nitrogen ambient to achieve good ohmic behavior through the formation of nickel silicide of Ni_2Si . [29,37] Figure 4.9 shows the temperature profile as a function of time during the rapid thermal process. The temperature was first increased to 950°C and kept for 40 secs and then increased to 1000°C to avoid the overshoot of the temperature which may occur if it was directly and abruptly increased to 1000°C.

Fig. 4.9 Temperature versus time under rapid thermal process.

The specific contact resistance (ρ_c), contact resistance (R_C) and sheet resistance (R_{sh}) for the ohmic contact were deduced using Transmission Line Model (TLM) [95]. The electrodes required were patterned and formed together with source and drain contact formation. Figure 4.10 (a) shows the optical micrograph of the TLM pattern. Figure 4.10 (b) shows the analysis model of TLM method where R_{sn} ($n = 1, 2, 3, \dots$) is the bulk resistance between two neighboring rectangular contacts (C_n and C_{n+1}) and R_c is

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the contact resistance between the ohmic contact and SiC. Therefore, the total resistance (R_T) between the neighboring contacts can be written as

$$R_T(i) = 2R_C + R_s(i) = 2R_C + \frac{R_{sh} \cdot d(i)}{W} \quad (i = 1, 2, \dots, 5) \quad (4.5)$$

where W is the contact width and d is the distance between neighboring contacts in the transmission line pattern. The relation between R_T and d is plotted as shown in Fig. 4.10(c). The term L_T shown in the figure is the transfer length. When the contact length $L > 1.5L_T$, ρ_c can be obtained by

$$\rho_c = R_C L_T W \quad (4.6)$$

In this work, the specific contact resistance on n^+ epilayer was deduced to be about $2.8 \times 10^{-5} \Omega \cdot \text{cm}^2$, which is comparable with most published data from about 10^{-4} to $10^{-6} \Omega \cdot \text{cm}^2$. [96]

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Fig. 4.10 Calculation of specific contact resistance using TLM. (a) Picture of TLM pattern; (b) TLM method; (c) the total resistance (R_T) versus the distance(d) between neighboring contacts in TLM.

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4.1.5 Formation of Gate Contacts

Similar to source and drain metal deposition, the gate metal was deposited using the lift-off technique after the oxide layer between the source and drain contacts was etched by the self-aligned technique as shown in Fig. 4.11. Double metal layers of 100nm nickel and 100nm gold were used for the gate contact. Fig. 4.12 shows the picture of a double-finger gate MESFET with a 1 μ m gate length after the gate metal deposition.

Fig. 4.11 Gate metal deposition using self-aligned process.

Fig. 4.12 Gate metal deposition of a double-finger gate MESFET.

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The gate-drain or gate-source Schottky diodes were characterized in terms of the forward and reverse current-voltage (I-V) curves. From the forward I-V characteristics, the Schottky barrier height (ϕ_B) and the ideality factor (n) can be obtained. According to the thermionic emission theory, the forward I-V characteristics of the gate Schottky contact is given by [40]

$$I = I_S \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] = AA^*T^2 \exp\left[-\frac{q}{kT}(\phi_B - \Delta\phi)\right] \quad (4.7)$$

where I_S is the saturation current, q is the electron charge, n is the ideality factor and kT is thermal energy equals to 0.02586eV at room temperature. ϕ_B is the barrier height, $\Delta\phi$ is the image force lowering, A is the contact area and A^* is effective Richardson's constant equals to $146 \text{ Acm}^{-2}\text{K}^{-2}$ for 4H-SiC. [97] For $V \gg kT$, eq.(4.7) can be written as

Fig. 4.13 Forward I-V Characteristics of the Schottky contact.

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$$\ln I = \ln(AA^*T^2) - \frac{q\phi_B}{kT} + \frac{q}{nkT}V \quad (4.8)$$

Figure 4.13 shows the forward I-V characteristics measured for the gate Schottky contact. Using eq.(4.8), we obtained $n = 1.18$ and $\phi_B = 1.32\text{eV}$, which is comparable with most published data where n is from about 1.05 to 1.21 and ϕ_B is correspondingly from 1.59 to 1.30 eV. [96]

4.1.6 Discussion

It should be noted that thermal oxidation is very important to remove surface damage arising from RIE etching and provide a good isolation between neighboring devices. The leakage currents between two neighboring devices were measured as shown in Fig. 4.14 for two samples with and without thermal oxidation to compare the quality of the mesa isolation. It is found that for the sample without thermal oxidation, the leakage current is about 0.1 mA when the applied voltage between the neighboring devices is 10V. However, for the sample treated with sacrificial thermal oxide and thermal oxide isolation, the leakage current is less than 3.0pA at the same bias. Sacrificial thermal oxidation also provides a good Schottky behavior. Figure 4.15 shows the forward I - V characteristics of the gate-source diodes for these two samples with and without thermal oxidation. It can be seen that the etch-induced surface damage significantly reduces the Schottky barrier and destroys the Schottky characteristics. Therefore, it is concluded that sacrificial thermal oxidation is crucial to remove the surface damage due to the plasma etching.

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Fig. 4.14 The leakage current between different devices on wafers with and without thermal oxidation for isolation.

Fig. 4.15 The effect of thermal oxidation to form isolation on Schottky behavior.

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4.2 Characterization of Conventional SiC MESFETs

In this section, we present the structure and characterization results of conventional 4H-SiC MESFETs. Both the DC and RF measurement results will be presented. Many devices with different gate lengths (L_g) of 1.0, 1.25, 1.5, 2.0, 2.5 and 3.0 μm were fabricated. All the devices with single-finger gate have a gate width (W) of 50 μm , gate-source spacing (L_{gs}) of 0.5 μm and gate-drain spacing (L_{gd}) of 1.5 μm .

4.2.1 Device Structures and Fabrication

Fig. 4.16 The cross-section of conventional 4H-SiC MESFET.

Figure 4.16 shows the cross-section of a conventional 4H-SiC MESFET. The starting wafer purchased from CREE Inc. comprises a vanadium doped semi-insulating substrate, a p-type buffer layer (0.5 μm thick; doping concentration $N_a=1.0\times10^{15}\text{cm}^{-3}$), a n-type channel layer and a high doped ($\sim 1.0\times10^{19}\text{cm}^{-3}$) n-type cap layer grown consecutively on top of the substrate. The channel thickness and doping concentration are 0.20 μm and $2.4\times10^{17}\text{cm}^{-3}$ respectively, which were deduced from secondary ions

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mass spectroscopy (SIMS) analysis by Charles Evans & Associates. The SIMS results for the wafer are shown in Fig. 4.17. The fabrication process follows the steps as discussed in section 4.1.

Fig. 4.17 The doping profile deduced from SIMS measurements for the conventional MESFET wafer.

4.2.2 Results and Discussion

The I - V characteristics of the devices were measured using the HP 4156A system. Figure 4.18 shows the characteristics of the drain current (I_{ds}) versus the drain-source voltage (V_{ds}) for 4H-SiC MESFETs with $L_g = 1.0$ μm. The gate voltage was varied from 0V to near pinch-off of -6V. Simulation results using Medici simulator are also plotted in this figure for comparison. The maximum saturation drain current density (I_{dsat}) is about 113 μA/μm under the bias of $V_{gs} = 0$ V and $V_{ds} = 20$ V. It should be noted that the simulated results are in good agreement with the experimental data.

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Fig. 4.18 The drain current versus the drain voltage for SiC MESFETs with $L_g=1.0\mu\text{m}$ under different gate voltage.

Figure 4.19 shows I_{ds} and transconductance (g_m) versus the gate voltage (V_{gs}) characteristics of $1.0\mu\text{m}$ gate length MESFETs under the bias of $V_{ds} = 1\text{V}$ and 40V . The threshold voltage (V_t) is about -5.6V when $V_{ds} = 1\text{V}$ as shown in fig. 4.19(a) and it is slightly increased when $V_{ds} = 40\text{V}$ as shown in fig. 4.19(b). This phenomenon is originated from the drain-induced barrier lowering (DIBL) effect which will be discussed in detail in the next chapter. It is found that the maximum g_m is about $5.8\mu\text{S}/\mu\text{m}$ at $V_{gs} = -4.4\text{V}$ for $V_{ds} = 1\text{V}$, as shown in fig. 4.19(a). However, at $V_{ds} = 40\text{V}$ g_m increases monotonically with decreasing V_{gs} due to the larger conductance channel under the high drain voltage of 40V . It reaches a maximum value of $32.8\mu\text{S}/\mu\text{m}$ at $V_{gs} = 0\text{V}$.

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Fig. 4.19 The drain current and transconductance (g_m) versus the gate voltage (V_{gs}) for SiC MESFETs with $L_g = 1.0\mu\text{m}$ under the bias of (a) $V_{ds} = 1\text{V}$ and (b) $V_{ds} = 40\text{V}$.

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Figure 4.20 plots V_t and I_{dsat} versus L_g . V_t is measured at $V_{ds} = 1\text{V}$ and I_{dsat} with $V_{gs} = 0\text{V}$ and $V_{ds} = 20\text{V}$. It can be seen that V_t is nearly constant and I_{dsat} decreases when L_g is increased from $1.0\text{ }\mu\text{m}$ to $3.0\text{ }\mu\text{m}$.

Fig. 4. 20 The threshold voltage (V_t) and the saturation drain current density (I_{dsat}) versus the gate length (L_g)

The microwave performance was characterized for the devices as shown in Fig. 4.12 with double-finger gate using HP 8510C network analyzer system. The small-signal high frequency characteristics of a $1.25\text{ }\mu\text{m}$ gate length SiC MESFET under the bias conditions of $V_{gs} = 0$ and $V_{ds} = 30\text{V}$ are shown in Fig. 4.20. From the current gain h_{21} , maximum stable gain and maximum available gain (MSG/MAG) obtained, the small-signal cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) were deduced to be 3.08 GHz and 9.5 GHz respectively. The RF characteristics of other 4H-SiC

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MESFETs with different gate lengths were also measured and the results are summarized in Table 4.1. As can be seen, f_T and f_{max} decrease with increasing gate length. For the MESFET with 1.0 μm gate length, its rf performance is worse off compared to those with 1.25 μm and 1.5 μm gate length. The possible reason is that the oxide layer under the gate was not totally removed for the 1.0 μm gate length devices due to the limitations of the equipment used for photolithography.

Fig. 4.21 Small-signal high frequency characteristics: The current gain h_{21} , maximum stable gain and maximum available gain (MSG/MAG) of 1.25 μm gate length SiC MESFET under the bias conditions of $V_{gs} = 0$ and $V_{ds} = 30\text{V}$.

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L_g (μm)	1.0	1.25	1.5	2	2.5
f_T (GHz)	2.86	3.08	2.9	1.65	1.6
f_{max} (GHz)	9.0	9.5	9.2	8.5	8.3

Table 4.3 Small-signal cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) of SiC MESFETs for different gate length under the bias conditions of $V_{gs} = 0\text{V}$ and $V_{ds} = 30\text{V}$.

4.3 Conclusion

The key process technologies were successfully applied for SiC semiconductor devices. In particular, reactive ion etching (RIE) based on a gas mixture of $\text{CHF}_3\text{-O}_2$ was applied to obtain good surface uniformity with stable, repeatable and acceptable etch rate. Lift-off process was used to deposit metal as masks for SiC etch or as metal contacts on SiC. Self-aligned process was used to form source, drain and gate metal contacts. Rapid thermal anneal (RTA) process at 1000°C for 1 min in nitrogen ambient was used to form good Ni/4H-SiC ohmic contacts with a sheet contact resistance of about $2.8 \times 10^{-5} \Omega \cdot \text{cm}^2$. The barrier height of Ni/Au Schottky contacts to 4H-SiC is about 1.32 eV without annealing. Based on the applied processes for SiC, conventional 4H-SiC MESFETs with different gate length (L_g) of 1.0 μm , 1.25 μm , 1.5 μm , 2.0 μm , 2.5 μm and 3 μm were successfully fabricated and characterized. The threshold voltage is about -5.6V and the maximum g_m is about $32.8 \mu\text{S}/\mu\text{m}$ for 1.0 μm gate length devices. The small-signal cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) were about 3.08 GHz and 9.5 GHz respectively, obtained from the dual-finger gate device with $L_g = 1.25 \mu\text{m}$ under the bias of $V_{gs} = 0\text{V}$ and $V_{ds} = 30\text{V}$.

Chapter 5 Drain-Induced Barrier Lowering Effect and Narrow Channel MESFETs

5.1 Introduction

Silicon carbide (SiC) based metal semiconductor field effect transistors (MESFETs) are very well-suited for high power, high frequency and high temperature applications due to the excellent electronic and physical properties of SiC, such as wide band gap, high breakdown electric field strength, large electron saturation velocity and high thermal conductivity. The main drawback in using SiC for microwave devices lies in its poor low field electron mobility of $300 - 500 \text{ cm}^2/\text{Vs}$, at doping levels of interest for conventional MESFETs in the range of $1 \times 10^{17} - 5 \times 10^{17} \text{ cm}^{-3}$ [47]. This results in a larger source resistance and lower transconductance compared to GaAs based MESFETs. However, this drawback is partially offset by the high breakdown field strength of SiC that allows the MESFETs to be operated under extremely high electric fields, driving the electrons into their saturation velocity across a large part of the conducting channel. As SiC has high electron saturation velocity, therefore SiC MESFETs are suitable for high power operation in the microwave frequency range. For example, the first commercial SiC MESFET was designed to operate directly from a base station's +48VDC supply [98]. To further enhance the high frequency performance of such devices, it is desirable to have short gate length MESFETs to reduce the transit time, enhance the transconductance and reduce the gate capacitance.

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However, under the conditions of large drain voltage and short gate length, two-dimensional effects will dominate the device operation [40], and short-channel effects will become increasingly significant, especially for drain voltage up to 48V or beyond. Such higher drain voltage will change the potential distribution and lower the potential barrier between the source and the drain in the channel layer, giving rise to the drain-induced barrier lowering (DIBL) effect [99,100,101,102].

The DIBL effect is an electrostatic effect that can change the channel from a state of pinch-off to conduction and result in a substantial leakage current. It also shifts the threshold voltage and renders the gate ineffective in controlling the channel. Consequently, the DIBL effect degrades the device performance which should be avoided in device and circuit design. In order to reduce this effect, the minimum gate length should be limited. Several studies have reported the DIBL effect in gallium arsenide (GaAs) [99,100] and silicon on insulate (SOI) [101,102] MESFETs. However, to date no similar results for SiC MESFETs have been reported. High power and high frequency 4H-SiC MESFETs are particularly susceptible to the DIBL effect due to the large drain voltage applied and their short channel length, both of which will enhance the effect. For example, the threshold voltages of 4H-SiC MESFETs have been found to increase with decreasing gate length [17]. Our experimental results obtained from the Cree commercial 4H-SiC MESFET (CRF-24010-101) revealed a large change in the threshold voltage from -10V to -18V when the drain-source voltage was increased from 10V to 48V . Therefore it is important to have a good understanding of the DIBL effect in such devices to help in their design and optimization.

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In this chapter, the DIBL effect in conventional 4H-SiC MESFETs is demonstrated and analyzed using the physical drift and diffusion model. Our results showed that for short gate length devices, the DIBL effect could result in a large threshold voltage shift and render the gate ineffective in controlling the channel when a large drain voltage is applied. We have also studied the dependence of the DIBL effect on the ratio of gate length over the channel thickness and on the channel doping concentration, the latter being a key parameter that determines the threshold voltage of a MESFET. SiC MESFET with narrow channel layer are proposed and fabricated to reduce the DIBL effect.

5.2 Device Structure

The cross-section of a recessed-channel MESFET structure simulated is shown in Fig. 2.2. The device structure consists of a semi-insulating substrate, p-type buffer layer (1.0 μm thick; doping density $N_a = 4.0 \times 10^{15} \text{cm}^{-3}$), n-type channel layer with a thickness underneath the gate region of $a = 0.20 \mu\text{m}$ and a doping concentration of $N_d = 3.1 \times 10^{17} \text{cm}^{-3}$, and a highly doped n type cap layer (0.2 μm thick; $N_d = 1.0 \times 10^{19} \text{cm}^{-3}$). The gate-source (L_{gs}) and gate-drain spacing (L_{gd}) are chosen to be 0.5 μm and 1.0 μm respectively. The semi-insulating substrate is modeled as a compensation-doped (vanadium) semiconductor with a high concentration ($8 \times 10^{16} \text{cm}^{-3}$) of deep level impurities. The activation energy of vanadium acceptor is selected as 1.05eV. [103]

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5.3 Origin of DIBL Effect

To investigate the DIBL effect in 4H-SiC MESFETs, the channel layer under the gate was fully depleted by applying a negative gate bias of $V_{gs} = -10\text{V}$, with the source grounded and the drain electrode maintained at 0V, that is, $V_{ds} = 0\text{V}$. Under this condition, the ability of the gate voltage to block current flow along the channel is determined by the potential variation along the channel near to the channel-buffer layer interface. Thus the DIBL effect can be investigated by studying the channel bottom potential variation.

Figure 5.1 shows the channel bottom potential (at the $y = a$ plane) for MESFETs with different gate lengths (L_g) as a function of the position along the channel, normalized with respect to the gate length (x/L_g). The coordinate x runs in the range of zero to L_g and the zero coordinate is located right at the edge of the gate near to the source. Along the x direction, it is observed that the potential first decreases, reaches a minimum in the middle of the gate before it increases towards the drain. This potential variation gives rise to a barrier that prevents any flow of electrons across the channel, with or without applied drain source bias V_{ds} . With decreasing L_g , the minimum potential in the channel was found to increase, resulting in a lower channel barrier. It can also be seen that the channel potential is nearly constant over much of the channel length for the long gate length device of $2.0\text{ }\mu\text{m}$; however, the potential barrier decreases and becomes negligible when the gate length is reduced to $0.3\text{ }\mu\text{m}$. This is mainly due to the electric field distribution in the channel layer that has changed from one dimensional in long gate length devices to two dimensional in short gate length devices. Therefore, the penetration of electric fields from the source and the drain elevates the channel potential, and resulting in the DIBL effect becoming

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more prominent for short gate length devices. Likewise, increasing V_{ds} produced the same effect, as shown in Fig. 5.2, where a MESFET with $L_g = 0.7\mu\text{m}$, $a = 0.20\mu\text{m}$ and $N_d = 3.1 \times 10^{17}\text{cm}^{-3}$ was considered. As can be seen, the channel potential barrier is substantially lowered with increasing V_{ds} , and the position of the minimum potential gradually shifts towards the source. Indeed there is no longer any channel barrier when the drain bias reaches 20V and beyond. This changes the channel from a state of pinch off to conduction and results in severe sub-threshold leakage current. In other words, the current of short channel MESFETs will be controlled by both the drain and gate potentials under saturation mode operation, rather than by the gate potential alone, which is undesirable for device and circuit design.

Fig. 5.1 The bottom channel potential distribution for different L_g under $V_{ds} = 0\text{V}$.

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Fig. 5.2 The bottom channel potential distribution for $L_g = 0.7\mu\text{m}$ under different V_{ds} .

5.4 DIBL's Dependences on Structure Parameters

The threshold voltage (V_T) of a MESFET is defined as the voltage applied to the gate electrode that results in an abrupt transition between turn-off and turn-on operations. Since lowering of the channel barrier will call for a larger gate voltage to keep the channel under pinch-off, therefore, the threshold voltage of the MESFETs is increased by the DIBL effect.

Figure 5.3 shows our simulated V_T as a function of the gate length for the MESFETs reported by H. Honda *et al* [17]. Also shown are the experimental data [17]. Three bias conditions of $V_{ds} = 1\text{V}$, 10V and 40V were considered in our simulation. The channel thickness and doping concentration are $a = 0.20\mu\text{m}$ and $N_d = 3.1 \times 10^{17}\text{cm}^{-3}$

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respectively. Note that our simulated V_T at $V_{ds} = 40\text{V}$ are in good agreement with the experimental results measured at the same V_{ds} [17]. For small drain voltage ($V_{ds} = 1\text{V}$) such that the MESFETs are operating in the linear region, V_T is observed to increase with decreasing L_g for $L_g < 0.6\mu\text{m}$ (or $L_g/a < 3$). On the other hand, when V_{ds} is increased to 10V and 40V which are in saturation region of the MESFETs operation, the corresponding L_g/a ratios at which V_T begins to change are increased to 6 and 8 respectively. Therefore, it can be seen that the DIBL effect results in much larger threshold voltage shift (ΔV_T) at shorter L_g and higher V_{ds} . Overall, the V_T shift is negligible when L_g/a is more than 5 ($L_g = 1.0\mu\text{m}$), and becomes significant when L_g/a is less than 3 ($L_g = 0.6\mu\text{m}$).

The effects of channel thickness (a) on the DIBL effect have also been studied. Figure 5.4 plots V_T as a function of the ratio L_g/a , for different a of $0.15\mu\text{m}$, $0.20\mu\text{m}$ and $0.25\mu\text{m}$ under $V_{ds} = 10\text{V}$ and 40V . It can be seen that when L_g/a is less than 8, the V_T shifts between the $V_{ds} = 10\text{V}$ and 40V are similar for different a at a constant L_g/a ratio. In other words, the DIBL effect is more dependent on the ratio of L_g/a , rather than a itself. Therefore, in order to minimize the DIBL effect, L_g/a should be kept greater than 3 for practical 4H-SiC MESFETs as shown in Fig. 5.3. This imposes an upper limit on the channel thickness for high frequency 4H-SiC MESFETs with short gate length, and ultimately limits the transconductance of the devices.

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Fig. 5.3 The threshold voltage versus the gate length and L_g/a under different drain biases: — Simulation curves, • Experimental data [17].

Fig. 5.4 The threshold voltage versus L_g/a at different channel thickness (a).

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The dependence of the DIBL effect on the channel doping (N_d) is also investigated in detail and the results are presented in Figs. 5.5 and 5.6. Figure 5.5 plots the threshold voltages versus different N_d under $V_{ds} = 40\text{V}$ and at different L_g/a ratios of 10, 6, 3.5 and 1.5. The structural parameters are kept the same as before except for L_g and N_d . It is clearly seen that V_t increases linearly with N_d for different L_g/a . Higher N_d results in thinner depletion region and wider channel opening under the gate and hence needs larger gate voltage to pinch off the channel. For the devices with long gate length ($L_g/a = 10$), the electric field in the channel can be treated as one dimensional for both low and high channel doping, therefore the DIBL effect is negligible. When L_g/a is decreased to 6, there is a slight shift in V_t at higher N_d . When L_g/a is further lowered to 1.5, V_t increases drastically, especially, for larger N_d .

Figure 5.6 plots V_t versus L_g and L_g/a at different N_d of 1.0×10^{17} , 3.1×10^{17} and $5.0 \times 10^{17} \text{cm}^{-3}$ under $V_{ds} = 1\text{V}$ and 40V . All the structural parameters are kept the same as before except for N_d and L_g . It can be seen that the increase in V_t between $V_{ds} = 1\text{V}$ and 40V is enhanced with increasing N_d . This dependence can be understood based on the operation of MESFETs. When the channel is more conductive, its potential distribution will be mainly determined by V_{ds} , rather than V_{gs} , that is, the gate has less control over the channel. When the DIBL effect sets in, a higher gate voltage will be required to influence the channel to cause it to be pinched-off, so that ΔV_t is larger. Alternatively, since the channel potential is more influenced by V_{ds} , therefore the device is more susceptible to the DIBL effect, whose primary cause is the large V_{ds} applied, resulting in a decrease in the potential barrier in the channel. Therefore the DIBL effect does depend on N_d and is stronger at larger N_d . Increasing V_{ds} will result

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in larger ΔV_t at higher N_d , as seen in Fig. 5.6. The lower limit for the L_g/a ratio should be increased much greater than 3 for devices with N_d larger than $5 \times 10^{17} \text{ cm}^{-3}$, so as to reduce the DIBL effect.

Fig. 5.5 The threshold voltage versus channel doping concentration under the drain bias of 40V with different ratio of L_g/a .

In short channel GaAs MESFETs, it was found that the the shift in V_t arising from the DIBL effect could be minimized by having a large N_d up to $1 \times 10^{18} \text{ cm}^{-3}$ [104]. To keep the pinch-off voltage constant, the channel thickness a was concurrently reduced in the process, accordingly to the following equation,

$$a = (2 \cdot \epsilon_0 \cdot \epsilon_r \cdot V_p / (q \cdot N_d))^{1/2} \quad (5.1)$$

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where ε_0 is dielectric constant in Vacuum, ε_r is relative dielectric constant, q is the electron charge and V_p is the pinch-off voltage.

The reported results apparently contradict what we have observed from our simulations that the DIBL effect is enhanced at larger N_d . We believe the better performance observed [104] was indeed attributed to the reduced channel thickness, resulting in a larger L_g/a ratio in accordance with our results, rather than the higher N_d .

Fig. 5.6 The threshold voltage versus L_g and L_g/a at different channel doping concentrations.

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Therefore, it is important to have a good understanding of the DIBL effect and its dependence on the L_g/a ratio and N_d in the design and optimization of the devices and circuits. In practice, other performance parameters such as output conductance and breakdown voltage should also be considered when deciding on the channel thickness and doping. Specifically, higher N_d will result in lower breakdown voltages, which should be avoided in high power devices.

SiC MESFETs are typically designed for high power and high frequency applications, and as such, will have short gate length, and are subject to large drain bias voltage, both of which will enhance the undesirable DIBL effect. In order to improve the high frequency performance, short gate length is preferred, and consequently, thinner channel layer should be selected to maintain a large L_g/a ratio and reduce the DIBL effect. This necessitates a higher doping in order to obtain high output power density. On the other hand, higher channel doping will enhance the DIBL effect, therefore, L_g/a should be kept much greater than 3, especially for devices with channel doping of more than $5 \times 10^{17} \text{ cm}^{-3}$. This, however, will compromise their high frequency performance.

5.5 SiC MESFET with a Narrow Channel Layer

To reduce the DIBL effect, SiC MESFETs with a highly doped narrow channel layer are proposed and fabricated. Figure 5.7 shows the cross-section of 4H-SiC MESFET structure with narrow channel layer. The starting wafer purchased from CREE Inc. comprises a vanadium doped semi-insulating substrate, a p-type buffer layer ($0.5 \mu\text{m}$ thick; doping concentration $N_a = 1.0 \times 10^{15} \text{ cm}^{-3}$), a n-type channel layer and a high

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doped ($> 1.0 \times 10^{19} \text{ cm}^{-3}$) n-type cap layer grown consecutively on top of the substrate. The channel thickness and doping concentration of the channel layer are $0.08 \text{ } \mu\text{m}$ and $8.0 \times 10^{17} \text{ cm}^{-3}$ respectively which were confirmed using SIMS analysis by Charles Evans & Associates as shown in Fig. 5.8. The channel thickness is smaller than the values (about $0.20 \text{ } \mu\text{m} \sim 0.25 \text{ } \mu\text{m}$) typically used in SiC MESFETs to result in a larger L_g/a ratio. The high doping concentration is used to compensate the effect of a narrow channel and maintain a high transconductance for the devices. For comparison, MESFETs with the conventional channel layer devices are also fabricated where the channel thickness and doping concentration are $0.20 \text{ } \mu\text{m}$ and $2.4 \times 10^{17} \text{ cm}^{-3}$ respectively. The gate lengths are 1.0, 1.25, 1.5, 2.0, 2.5 and $3.0 \text{ } \mu\text{m}$, and the gate width is $50 \text{ } \mu\text{m}$ for all devices, and L_{gs} and L_{gd} are $0.5 \text{ } \mu\text{m}$ and $1.5 \text{ } \mu\text{m}$ respectively.

Fig. 5.7 The cross-section of 4H-SiC MESFETs fabricated with narrow channel layer.

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Fig. 5.8 The doping profile from SIMS measurements for narrow channel wafers.

The I-V characteristics for 4H-SiC MESFETs with narrow channel layer and the conventional thicker channel layer are measured using HP 4156A and are shown in Figs. 5.9 and 5.10. For narrow channel layer with 1 μm gate length, the drain current (I_d) versus the drain-source voltage (V_{ds}) is plotted under the gate bias from 0V to -1.2V with a step of -0.2V as shown in Fig. 5.9(a). In comparison, Fig. 5.9(b) also shows $I_d - V_{ds}$ curves for conventional channel layer with the same L_g under the gate bias from 0V to -6V with a step of -1V . It can be seen that for narrow channel devices, better saturation behavior with fairly low output conductance is achieved, which is desirable for small signal applications. Figure 5.10 shows I_d and g_m versus V_{gs} under $V_{ds} = 40\text{V}$ for both devices. It is found that the V_t are about -1.1V and

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−6.3V at $V_{ds} = 40\text{V}$ for narrow channel devices and conventional channel devices, respectively. The transconductance for narrow channel devices and conventional channel devices are 3.75mS/mm and 32.8mS/mm, respectively, under the bias of $V_{gs} = 0\text{V}$ and $V_{ds} = 40\text{V}$.

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Fig. 5.9 Drain current versus drain voltage under different gate voltage with (a) narrow channel layer and (b) common channel layer.

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(a)

(b)

Fig. 5.10 Drain current and transconductance versus gate voltage under the drain voltage of 40V for SiC MESFETs with (a) narrow channel layer and (b) common channel layer.

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Figure 5.11 shows V_t versus V_{ds} for narrow channel and conventional channel MESFETs with different L_g . For narrow channel device with $L_g = 1\mu\text{m}$, V_t is about -1.1V and independent of V_{ds} applied from 1V to 40V . However, for conventional channel device with $L_g = 1.0\mu\text{m}$, V_t is shifted from -5.6V to -6.3V when the drain voltage is changed from 1V to 40V . It is also found that the threshold voltage shift (ΔV_t) can be omitted for $3.0\mu\text{m}$ gate length devices with conventional channel. As discussed before, V_t is shifted by the DIBL effect due to the large drain voltage applied for conventional channel devices. It is also known that the DIBL is minimized with large L_g/a ratio. Therefore, no significant V_t shift is observed for $3\mu\text{m}$ gate length devices. It can be predicted that submicron gate length devices will suffer from a larger $|\Delta V_t|$. However, if we use narrow channel device, the DIBL effect can be suppressed effectively, as shown in Fig. 5.11.

Fig. 5.11 The threshold voltage versus the drain voltage for different devices.

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5.6 Conclusion

The drain-induced barrier lowering effect in conventional 4H-SiC MESFETs has been investigated in detail by physical simulation. Our simulation results have shown that for short gate length SiC MESFETs, the DIBL effect will result in large threshold voltage shift and significantly affect the device performance when a large drain voltage is applied. The DIBL effect is more dependent on the ratio of L_g/a , rather than the channel thickness itself. High channel doping concentration has also been found to enhance the DIBL effect. In order to minimize the DIBL effect, the ratio of L_g/a should be kept much greater than 3 for practical 4H-SiC MESFETs, especially when the channel doping concentration is more than $5 \times 10^{17} \text{cm}^{-3}$.

SiC MESFETs with a highly doped narrow channel layer are proposed and fabricated to reduce the DIBL effect. The measured results are compared with the conventional channel layer devices fabricated in the same process flow. It is demonstrated that the threshold voltages of the narrow channel MESFETs are about -1.1 V and independent of the gate length when the drain voltage applied up to 40 V . However, for the conventional channel MESFETs with the applied drain voltage changed from 1 V to 40 V , the threshold voltage is increased from -5.6 V to -6.3 V for $1.0 \mu\text{m}$ gate length devices. Compared to conventional channel structures, narrow channel devices also achieve better saturation behavior with fairly lower output conductance which is desirable for small signal applications.

Chapter 6

Dual-Channel 4H-SiC MESFETs

6.1 Introduction

SiC MESFETs have received increased attention in recent years due to their high operating voltage, high power density and high frequency performance. These enable wider bandwidth operation, and lower the size and weight of communication systems compared to those using conventional technologies based on Si and GaAs. However, in the conventional structure, its operation is limited by the poor low field electron mobility of SiC which requires a high drain voltage applied to drive electrons to saturation. Under these conditions, short channel effect, especially drain-induced barrier lowering (DIBL) effect [105,106] will dominate the device performance. In order to minimize the DIBL effect, the channel layer has to be thin to maintain a large gate length to channel thickness ratio (L_g/a) which in turn limits the device power capacity. This necessitates a higher channel doping in order to obtain high output power density. However, in this case, the power density is still much lower compared to the conventional devices due to the narrow channel layer, though the undesirable short channel effect can be reduced. [107] Higher channel doping will concurrently result in larger leakage current and lower breakdown voltage [47]. Toshiya Y. *et al.* studied multi-delta doping layers with undoped inter-layers as the channel layer for 6H-SiC MESFETs to provide high breakdown voltage [108,109]. However, no

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saturation region was found in this type of transistors and the drain current was also limited. Some researchers [11,12,110] suggested a buried-gate structure to suppress the trapping induced instabilities which will decrease the electrical performance of the devices operated at continuous waveband (CW) and to provide high drain current. However, both experimental [12] and simulation results [110] showed that the source-drain breakdown voltage of buried-gate transistors was lower than that of conventional channel recessed structures.

In this chapter, we proposed and fabricated an improved structure for 4H-SiC MESFETs with a dual-channel layer that can overcome the above mentioned problems. The upper-channel layer is of lower doping concentration and serves to improve the Schottky characteristics of the gate, while the lower-channel layer is of higher doping concentration and acts as the main channel for the conduction of drain current. The dual channel layer MESFETs were found to have improved performance compared to conventional single channel layer devices, expect for slightly lower r.f. performance.

6.2 Device Structures and Fabrication

Figure 6.1 shows the recessed-channel 4H-SiC MESFET structure that includes a dual-channel layer with the lower-channel being higher doped than the upper-channel. The starting wafer purchased from Cree comprises a vanadium doped semi-insulating substrate, followed by a p-type buffer layer (thickness $0.5\mu\text{m}$; doping concentration $N_a = 1.0 \times 10^{15} \text{cm}^{-3}$), a n-type higher doped lower-channel layer (thickness $a_2 = 0.08\mu\text{m}$; doping concentration $N_{d2} = 5.2 \times 10^{17} \text{cm}^{-3}$), a n-type lower doped upper-channel layer (thickness $0.17\mu\text{m}$; $N_{d1} = 1.4 \times 10^{17} \text{cm}^{-3}$) and a highly doped n-type cap

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layer (thickness $0.20\mu\text{m}$, $N_d = 1.0 \times 10^{19} \text{cm}^{-3}$). The doping concentrations and the thickness were deduced from secondary ions mass spectroscopy (SIMS) analysis by Charles Evans & Associates as shown in Fig. 6.2. For comparison, conventional MESFETs with a single channel layer of thickness $a = 0.20\mu\text{m}$ and doping concentration of $N_d = 2.4 \times 10^{17} \text{cm}^{-3}$ were also fabricated and characterized.

The fabrication process involved mesa isolation and channel recess etching based on reactive ion etching. A layer of sacrificial thermal oxide was grown and subsequently etched to remove any etch-induced damage. Following that, a 50nm thick thermal oxide was grown at 1150°C for 6 hours by dry oxidation to form good isolation. After the self-aligned wet etching of the thin oxide layer, the source and drain metals consisting of 200nm nickel were deposited using electron-beam evaporation. The metal outside the contact areas was removed by lift-off process. The source and drain contacts underwent rapid thermal annealing at 1000°C for 1 min in a nitrogen ambient to achieve good ohmic characteristics. The typical specific contact resistance on n^+ epilayer extracted from the transmission line method (TLM) was deduced to be about $2.8 \times 10^{-5} \Omega \cdot \text{cm}^2$. The same lift-off process was used to deposit the gate metal that consists of Ni(100nm)/Au(300nm). No further thermal treatment was performed for the gate metal. The ideality factor and the barrier height of the Schottky contacts are about 1.18 and 1.32 eV respectively. The detailed fabrication process has been covered in Chapter four. The final thickness of the upper-channel under the gate region is around $a_1 = 0.12\mu\text{m}$. The gate lengths (L_g) of the devices are 1.0, 1.25, 1.5, 2.0, 2.5 and $3.0 \mu\text{m}$ and the gate width is $50 \mu\text{m}$. The gate-source spacing (L_{gs}) and gate-drain spacing (L_{gd}) are about $0.5 \mu\text{m}$ and $1.5 \mu\text{m}$ respectively.

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Fig. 6.1 The cross-section of 4H-SiC MESFETs fabricated with a dual-channel layer.

Fig. 6.2 The doping profile deduced from SIMS measurements for the MESFET wafer with dual-channel layer.

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6.3 Results and Discussion

The I-V characteristics of the devices were measured using the HP 4156A system. Figure 6.3 shows the characteristics of the drain current (I_{ds}) versus the drain-source voltage (V_{ds}) measured for the dual-channel 4H-SiC MESFETs with two different L_g of 1.0 μm and 3.0 μm . The source contact was grounded and the gate bias (V_{gs}) was varied from 0V to -15V in step of -3V. The maximum saturation drain current density (I_{dsat}) for two devices with $L_g = 1.0 \mu\text{m}$ and 3.0 μm are about 280 $\mu\text{A}/\mu\text{m}$ and 153 $\mu\text{A}/\mu\text{m}$, respectively under the bias of $V_{gs} = 0\text{V}$ and $V_{ds} = 40\text{V}$. Figure 6.4 shows the characteristics of I_{ds} and transconductance (g_m) versus V_{gs} for these two devices under a V_{ds} of 2.5V. As can be seen, the threshold voltage (V_t) is about -14.0V for both devices. The maximum g_m is about 9.24 $\mu\text{S}/\mu\text{m}$ at $V_{gs} = -12.5\text{V}$ for the MESFET with $L_g = 1.0\mu\text{m}$ and about 4.26 $\mu\text{S}/\mu\text{m}$ at $V_{gs} = -11.5\text{V}$ for the device with $L_g = 3.0 \mu\text{m}$.

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Fig. 6.3 Drain current versus drain voltage characteristics under different gate voltages for dual-channel 4H-SiC MESFETs with the gate length of (a) $L_g = 1.0\mu\text{m}$ and (b) $L_g = 3.0\mu\text{m}$.

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Fig. 6.4 The drain current and transconductance versus the gate voltage for dual-channel SiC MESFETs with (a) $L_g = 1.0\text{ }\mu\text{m}$ and (b) $L_g = 3.0\text{ }\mu\text{m}$ under $V_{ds}=2.5\text{V}$.

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It should be noted that for meaningful comparison between single and dual channel devices, the total channel thickness of dual-channel MESFETs under the gate electrode has been designed to be equal to the channel thickness of the conventional MESFETs under the gate electrode. On the other hand, the channel doping concentration of the conventional MESFETs has been chosen to be somewhere intermediate between the doping of the upper and lower-channel layers of the dual-channel MESFETs. The performance of these two types of devices with $L_g = 1.0\mu\text{m}$ are compared. The saturation drain current density (I_{dsat}) with $V_{gs} = 0\text{V}$ and $V_{ds} = 40\text{V}$ is about $280\ \mu\text{A}/\mu\text{m}$ for the dual-channel MESFETs. In contrast, it is only about $125\ \mu\text{A}/\mu\text{m}$ for the conventional MESFETs as can be deduced from Fig. 4.19(a). It is also noted that better saturation behaviour with fairly low output conductance is achieved for the dual-channel MESFETs compared to the conventional MESFETs. The maximum transconductance (g_m) and threshold voltage (V_t) for the dual-channel MESFETs are about $31\ \mu\text{S}/\mu\text{m}$ and -14.0V respectively. The corresponding values for the conventional devices are about $33\ \mu\text{S}/\mu\text{m}$ and -5.6V respectively. The larger I_{dsat} and V_t achieved for the dual-channel devices are attributed to the higher doped lower-channel layer. On the other hand the g_m is slightly lower, which may be due to the lower electron mobility in the higher doped lower-channel layer compared to the conventional single channel layer.

Figure 6.5 plots the gate leakage current as a function of the gate-drain voltage under reverse bias condition for both types of devices, with floating source electrode. For the dual-channel layer MESFETs the leakage current is around $6.5 \times 10^{-6}\ \mu\text{A}/\mu\text{m}$, which is lower compared to $2.5 \times 10^{-5}\ \mu\text{A}/\mu\text{m}$ measured for the conventional devices.

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A separate higher voltage measurement system was used to measure the breakdown voltages of the devices as shown in Fig. 6.6. The source-drain breakdown voltage measured with V_{gs} set at approximately V_t is about 145V for dual-channel devices and about 123V for conventional devices.

Fig. 6.5 Gate leakage current versus gate-drain voltage with floating source electrode for 4H-SiC MESFETs with dual-channel layer and conventional single channel layer.

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Fig. 6.6 The drain current versus the drain-source voltage for 4H-SiC MESFETs with dual-channel layer and conventional single channel layer under the $V_{gs} \approx V_t$.

The maximum theoretical output power density for a Class A amplifier is given by [111]

$$P_{\max} = \frac{I_{dsat}(V_b - V_{knee})}{8} \quad (6.1)$$

where I_{dsat} is the saturation drain current density, V_b is the drain-source breakdown voltage with $V_{gs} = V_t$ and V_{knee} is the knee voltage. According to the above equation, the maximum output power density of the dual-channel and conventional 4H-SiC MESFETs are about 4.6 W/mm and 1.8 W/mm respectively. Therefore, there is a significant improvement in the power density of dual-channel layer MESFETs compared to single channel layer MESFETs.

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The microwave performance of the dual-channel devices were characterized using HP 8510C net work analyzer system. Figure 6.7 shows the small-signal high frequency characteristics of 4H-SiC MESFET with $L_g = 1.25\mu\text{m}$ under the bias conditions of $V_{gs} = 0$ and $V_{ds} = 30\text{V}$. From the current gain h_{21} , maximum stable gain and maximum available gain (MSG/MAG) obtained, the small-signal cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) were deduced to be 1.58 GHz and 3.81 GHz respectively. For the devices with other gate lengths, their f_T is lower than 1.0GHz and could not be measured due to the limitations of the equipment. The trend of f_T versus the L_g is similar to that observed for the conventional one channel devices. However, the radio frequency (RF) performance of the dual-channel MESFETS is slightly worse than that of the conventional devices. A possible reason is that the higher doped lower-channel layer results in larger gate-drain and gate-source capacitances, which are two of the most important parameters that will degrade f_T and f_{max} . Therefore, in order to obtain devices with higher RF performance, MESFETs with submicron gate length should be considered for the dual-channel devices.

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Fig. 6.7 Small-signal high frequency characteristics: The current gain h_{21} , maximum stabile gain and maximum available gain (MSG/MAG) of $1.25\mu\text{m}$ gate length dual-channel 4H-SiC MESFET under the bias conditions of $V_{gs} = 0\text{V}$ and $V_{ds} = 30\text{V}$.

It should be noted that a two-channel layer structure MESFET device based on GaAs semiconductor has been proposed [40,112,113] to improve the linear d.c. transfer characteristics since the carrier concentration near the surface of the active layer is lower. In addition, the step doping channel devices are observed to exhibit superior noise performance since they can maintain good values of g_m near pinch off and minimum noise figure is usually obtained when the device is biased near pinch off.

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A United States patent [114] also showed that the radiation hardness of GaAs MESFET can be conspicuously improved up to a total exposure dose of about 1×10^8 roentgens using a two-channel layer structure. This is due to the fact that the rates of change of some electric parameters such as transconductance, saturated drain current and threshold voltage are related to the channel layer parameters when radiation is applied to the MESFET.

In comparison, our two-channel layer structure is proposed on a different basis, that is, to obtain large transconductance and breakdown voltage for SiC MESFET devices simultaneously. In principle, our design can also be applied to GaAs MESFET devices. It is well known that GaAs based MESFETs are widely applied in microwave device applications, driven by the higher electron mobility ($6500 \text{ cm}^2/\text{Vs}$). However, due to the low breakdown field (about 0.4 MV/cm) and saturated electron velocity ($1.2 \times 10^7 \text{ cm/s}$) of GaAs, no significant advantage can be derived using a two-channel layer structure GaAs MESFET.

Compared to GaAs, one main drawback in using SiC in microwave devices is its poor low field electron mobility of only about $800 \text{ cm}^2/\text{Vs}$. To compensate for this, it is important that the channel layer be highly doped to increase the current density, and the transverse electric field should be large to drive the carriers into velocity saturation to capitalize on their much larger saturated velocity ($2 \times 10^7 \text{ cm/s}$) compared to GaAs. These, however, will lead to a lower breakdown voltage for the device, despite that the critical breakdown electric field of SiC (3 MV/cm) is much larger compared to that of GaAs. Therefore, to achieve large current density and yet preserve a large breakdown voltage, it is important to have a two-channel layer

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structure. Indeed, our experimental results have also confirmed that the two-channel layer MESFETs can enhance the performance of SiC power devices.

6.4 Conclusion

4H-SiC MESFETs with a dual-channel layer were fabricated and characterized. The experimental results of the 1.0 μm gate length device are compared with those of conventional devices with a single channel layer fabricated using exactly the same process flow. The saturation drain current density is about 280 $\mu\text{A}/\mu\text{m}$ and the threshold voltage is about -14.0V for the dual-channel MESFETs, which are both higher than the 125 $\mu\text{A}/\mu\text{m}$ and -5.6V measured for the conventional devices. The improvements are attributed to the high doped lower-channel layer. The dual-channel MESFETs exhibit a lower gate leakage current of about $6.5 \times 10^{-6} \mu\text{A}/\mu\text{m}$ and a higher breakdown voltage of about 145V, which are improved compared to the conventional devices, attributed to the lower doped upper-channel layer. Besides, a higher output power density of 4.6W/mm can be achieved for the dual-channel devices compared to 1.8 W/mm for the conventional devices. The cut-off frequency of the device with 1.25 μm gate length is about 1.58 GHz, which is slightly lower than that of the conventional device.

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Chapter 7

SiC MESFETs with Double-Recessed Structure

7.1 Introduction

SiC based MESFETs are emerging as a promising technology for high power microwave applications such as transmitters for commercial and military communications. [115] This is made possible due to the superior properties of SiC and the relatively mature material growth and device fabrication technology. High power 4H-SiC MESFETs must be able to sustain large drain current and have high breakdown voltages. To allow for high drain current, a large product of the channel doping and thickness ($N \times a$) is required. However, a higher channel doping concentration will lower the breakdown voltage, [77] and a thick channel layer will lead to a lower aspect ratio of gate length to channel thickness (L_g/a) and result in short-channel and drain-induced barrier lowering (DIBL) effects which will degrade the device and circuit performance [105]. Some researchers suggested a buried-gate structure to suppress the trapping induced instabilities which will decrease the electrical performance of the devices operating at continuous waveband (CW). [11,12] However, the partial gate located on the channel layer nearer to the source

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electrode will result in a parasitic depletion region which reduces the cut-off frequency and decreases the channel current. [116]

In this chapter, we proposed and simulated a double-recessed 4H-SiC MESFET structure which allows a thicker channel and yet maintains a larger L_g/a ratio. The first recess was formed by reactive ion etching to define the channel in the active layer, while the second recess was realized by having half of the gate nearer to the source buried with a certain depth into the channel layer. Therefore, the structure has lower and upper gates, which control a thinner and a thicker part of the channel respectively. The thicker channel allows for higher drain saturation current and lower source and drain impedances whereas the thinner channel ensures that the channel can be effectively controlled by the gate bias. The DC and RF performances of the double-recessed 4H-SiC MESFETs have been simulated in details and the results are compared for those obtained from the conventional channel recessed structure.

7.2 Device Structures

SiC MESFETs based on the conventional channel recessed and double-recessed structures are shown in Fig. 7.1. The double-recessed structure in Fig. 7.1 (b) has a channel thickness of 0.25 μm , and is etched 0.05 μm before metal deposition to form the second recessed gate. As a result, the thickness of the channel layer underneath the lower gate is 0.20 μm . The channel doping $N_d = 3.0 \times 10^{17} \text{ cm}^{-3}$. To have a meaningful comparison, the channel thickness of the MESFET based on conventional structure is also set at 0.20 μm . This ensures that both devices will have comparable pinch-off voltages. Nickel was chosen for the gate Schottky contact with a work function of

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5.1eV. The other dimensions of both devices are as follows: gate length of the device $L_g = 0.7 \mu\text{m}$, gate-drain spacing $L_{gd} = 1 \mu\text{m}$, gate-source spacing $L_{gs} = 0.5 \mu\text{m}$. The doping and thickness of the buffer layer are $1.4 \times 10^{15} \text{ cm}^{-3}$ and $0.50 \mu\text{m}$ respectively. The semi-insulating substrate is modeled as a compensation-doped (vanadium) semiconductor with a high concentration ($8 \times 10^{16} \text{ cm}^{-3}$) of deep level impurities. The activation energy of vanadium acceptor is selected as 1.05eV. [103,105]

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(a)

(b)

Fig. 7.1 The cross-section of 4H-SiC MESFETs with (a) conventional recessed structure and (b) double-recessed structure.

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7.3 Results and Discussion

The threshold voltages (V_t) of the double-recessed and conventional structure are comparable and their simulated values are -9.2V and -8.4V respectively. The simulated drain current (I_d) versus the drain-source voltage (V_{ds}) for 4H-SiC MESFET with the double-recessed structure under the gate bias (V_{gs}) from 0V to -10V with a step of -2V are shown in Fig. 7.2 (b). The corresponding characteristics for the device with conventional recessed structure are shown in Fig. 7.2 (a) for comparison. It is found that the saturation current (I_{sat}) of the double-recessed 4H-SiC MESFETs at $V_{gs} = 0\text{V}$ is about 77% larger than that of the conventional structure at $V_{gs} = 0\text{V}$, arising from a wider channel opening outside of the buried gate region. Therefore, the double-recessed structure provides a larger I_{sat} than the conventional structure while maintaining a comparable V_t .

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Fig. 7.2 Drain current versus drain voltage under different gate voltages with (a) conventional structure and (b) double-recessed structure.

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The three-terminal breakdown characteristics of the devices were simulated with an applied $V_{gs} = V_t$, as shown in Fig. 7.3. The drain current (I_d) and the gate leakage current (I_g) versus V_{ds} are presented for both double-recessed and conventional structures. For both structures, it is noted that the increased currents at the drain electrodes mainly come from the leakage currents at the gate electrodes when comparing $I_g - V_{ds}$ and $I_d - V_{ds}$ curves. This reveals that the breakdown of SiC MESFETs at the applied V_{gs} occurred between the gate and the drain, instead of between the drain and the source. It can be seen that there is a decrease in the breakdown voltage (V_b) from 137V to 109V for the double-recessed structure compared to the conventional recessed structure. This is consistent with the experimental results for the buried gate structure [12]. A detailed investigation of the current flowlines in the devices show that the gate leakage currents mainly flow through the gate corner nearer to the drain side due to the electric field crowding at the corner. The decrease of the breakdown voltage for the double-recessed structure is attributed to the thicker channel which results in the vertical electrical field being more significant in the double-recessed device compared to the conventional one. C.S. Chang and D.S. Day studied the gate leakage current and the breakdown voltage in GaAs MESFETs using an analytic method and also found that the breakdown voltage is higher for thinner active layer [117].

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Fig. 7.3 Simulated breakdown curves of 4H-SiC MESFETs with conventional and double-recessed structures.

The maximum theoretical output power density for a Class A amplifier is given by eq. (6.1). According to this equation, the maximum output power density of the double-recessed and conventional recessed 4H-SiC MESFETs can be calculated and are 5.5W/mm and 4.0W/mm respectively. Therefore, there is a significant improvement in the power density of about 37.5% for the devices with a double-recessed structure.

Figure 7.4 shows the simulated small signal current gain h_{21} , maximum stable gain (MSG), maximum available gain (MAG) and unilateral power gain (U) for 4H-SiC MESFETs with double-recessed and conventional structures as a function of frequency under the bias conditions of $V_{gs} = 0V$ and $V_{ds} = 30V$. The results show that the cut-off frequency (f_T) and the maximum frequency (f_{max}) of the double-recessed

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structure are 15.3GHz and 70.6GHz, respectively. However, for the conventional structure, f_T and f_{max} are 10.0GHz and 45.0GHz respectively. The increases in f_T and f_{max} for double recess structure may be attributed to smaller effective gate length (L_{eff}) compared to the conventional structure. It should be noted that f_T and f_{max} are comparable for buried gate and conventional structure [12] due to the parasitic depletion region formed by the unburied gate nearer to the source. As can be seen from our simulation results, this problem is avoided in the double-recessed structure.

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Fig. 7.4 Simulated small-signal high frequency characteristics: h_{21} , MSG/MAG and G_u of 4H-SiC MESFETs with conventional recessed structure (a) and double-recessed structures with one-channel layer (b) under the bias conditions of $V_g = 0V$ and $V_{ds} = 30V$.

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7.4 Conclusion

The electrical performance of SiC MESFET with a double-recessed structure was simulated and compared to devices with conventional recessed structure. The simulated results showed that the saturation current and the output power density of the double-recessed structure are about 77% and 37.5% larger than that of the conventional structure respectively. However, their threshold voltages are comparable and are -9.2V and -8.4V for the double-recessed and conventional structure, respectively. The three-terminal breakdown voltages of double-recessed and conventional structure are about 109V and 137V respectively, which is consistent with the published results. The cut-off frequency and the maximum oscillation frequency of the double-recessed structure are 15.3GHz and 64.5GHz respectively compared to 10.0GHz and 38.0GHz for the conventional structure. Therefore, the double-recessed 4H-SiC MESFET has superior DC and RF performances compared to the similar devices based on the conventional structure.

CHAPTER 8 CONCLUSION AND FUTURE WORK

Chapter 8

Conclusion and Future Work

8.1 Conclusion

The device processing technology has been successfully developed to fabricate metal semiconductor field effect transistors (MESFETs) based on 4H-SiC semiconductors. Detailed device modeling and simulation have also been carried out to support the device design and fabrication. Drain-induced barrier lowering effect in SiC MESFETs was studied in detail. 4H-SiC MESFETs with narrow channel layer and dual-channel layer were fabricated and characterized, and their performances were also compared with devices having the conventional channel layer structure using the same process flow. A recessed-gate structure was also designed and simulated to improve the output power density and RF performance.

A two-dimensional numerical simulator Medici was selected to model the SiC MESFETs. The built-in physical models were chosen and their parameters were optimized to provide a good agreement with the experimental results obtained for 4H-SiC MESFETs. A three-region analytical model was also developed to simulate the behavior of short-channel SiC MESFETs under high drain voltage. Compared to the commonly used two-region model, the three-region model has included a third high field region between the gate and the drain where there is a large voltage drop. This

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region cannot be neglected under high drain voltage for short-channel SiC MESFETs. The I-V characteristics of SiC MESFET with 0.7 μm gate length were simulated based on our proposed three-region model and the results were in excellent agreement with the experimental data.

The device fabrication processes have been successfully applied for SiC MESFETs. The reactive ion etching (RIE) was used to form mesa isolation and channel recess etching. A recipe for the RIE of 4H-SiC based on a gas mixture of $\text{CHF}_3 - \text{O}_2$ was applied to provide an etch rate suitable for device fabrication, a good selectivity compared to the metal mask (Ti/Ni) and smooth etch surfaces. A recipe for the rapid thermal anneal (RTA) process for Ni/4H-SiC was used to form good ohmic contacts with sufficiently low contact resistance ($\sim 2.8 \times 10^{-5} \Omega \cdot \text{cm}^2$) for device contact applications. Lift-off and self-aligned processes were applied and optimized for the MESFETs fabrication work.

Using the developed processes, conventional 4H-SiC MESFETs with gate length (L_g) ranging from 1.0 μm to 3.0 μm were fabricated and characterized. The threshold voltage (V_t) is about -5.6V for the devices at $V_{ds} = -1\text{V}$. For the SiC MESFET with $L_g = 1.0\mu\text{m}$, the maximum transconductance (g_m) is about $32.8 \mu\text{S}/\mu\text{m}$ and the maximum saturation current density (I_{dsat}) is about $125 \mu\text{A}/\mu\text{m}$ under the bias of $V_{gs} = 0\text{V}$ and $V_{ds} = 40\text{V}$. The small-signal cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) were about 3.08 GHz and 9.5 GHz respectively, measured for the dual-finger gate devices with $L_g = 1.25 \mu\text{m}$ under the bias of $V_{gs} = 0\text{V}$ and $V_{ds} = 30\text{V}$.

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The drain-induced barrier lowering (DIBL) effect in conventional 4H-SiC MESFETs was investigated in detail by physical simulation. Our simulation results have shown that for short gate length SiC MESFETs, the DIBL effect will result in large threshold voltage shift and significantly affect the device performance when a large drain voltage is applied. The DIBL effect is more dependent on the ratio of L_g/a , rather than the channel thickness itself. High channel doping concentration has also been found to enhance the DIBL effect. In order to minimize the DIBL effect, the ratio of L_g/a should be kept much greater than 3 for practical 4H-SiC MESFETs, especially when the channel doping concentration is more than $5 \times 10^{17} \text{cm}^{-3}$. SiC MESFETs with a highly doped narrow channel layer were proposed and fabricated to reduce the DIBL effect. It is demonstrated that the threshold voltages of the narrow channel MESFETs are about -1.1 V and independent of the gate length when the drain voltage applied is up to 40 V . However, for the conventional channel MESFETs, the threshold voltage is changed from 1 V to 40 V for $1.0 \text{ }\mu\text{m}$ gate length devices. Compared to conventional channel structures, narrow channel devices concurrently achieve better saturation behavior and low output conductance which is desirable for small signal applications.

Dual-channel 4H-SiC MESFETs were fabricated and characterized. The experimental results of the $1.0 \text{ }\mu\text{m}$ gate length device are compared with those of conventional devices with a single channel layer fabricated using exactly the same process flow. The saturation drain current density is about $280 \text{ }\mu\text{A}/\mu\text{m}$ and the threshold voltage is about -14.0 V for the dual-channel MESFETs, which are both higher than the $125 \text{ }\mu\text{A}/\mu\text{m}$ and -5.6 V measured for the conventional devices. The improvements are attributed to the high doped lower-channel layer. The dual-channel MESFETs exhibit a lower gate leakage current of about $6.5 \times 10^{-6} \text{ }\mu\text{A}/\mu\text{m}$ and a higher breakdown voltage

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of about 145V, which are improved compared to the conventional devices, attributed to the lower doped upper-channel layer. Besides, a higher output power density of 4.6W/mm can be achieved for the dual-channel devices compared to 1.8 W/mm for the conventional devices. On the other hand, the cut-off frequency of the device with 1.25 μm gate length is about 1.58 GHz which is slightly lower than that of the conventional devices.

The electrical performance of SiC MESFET with a double-recessed structure was simulated and compared with the conventional recessed structure. The simulated results showed that the saturation current and the output power density of the double-recessed structure are respectively about 77% and 37.5% larger than that of the conventional structure. However, their threshold voltages are comparable and are -9.2V and -8.4V for the double-recessed and conventional structure respectively. The three-terminal breakdown voltages of double-recessed and conventional structure are about 109V and 137V respectively, which is consistent with the published experimental results. The cut-off frequency and the maximum oscillation frequency of the double-recessed structure are 15.3 GHz and 64.5 GHz respectively, compared to 10.0 GHz and 38.0 GHz for devices with conventional structure. Therefore, the double-recessed 4H-SiC MESFET has superior DC and RF performances compared to the similar device based on the conventional structure.

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8.2 Recommendations for Further Research

In this work, our study has mainly focused on the device design and process development for the fabrication of 4H-SiC MESFETs. 4H-SiC MESFETs with different structures such as conventional one channel, narrow channel and dual-channel were fabricated and characterized. Based on the results obtained, some suggestions are proposed for future work. These have not been accomplished in this project due to either lack of time or equipment.

8.2.1 Fabrication of SiC MESFETs with submicron gate length

In order to achieve higher RF performance, submicron gate length SiC MESFETs are required. As the line width is limited to 1.0 μm for photo lithography process in our clean room, the present process at our disposal is not suitable for submicron technology. In the future work, an e-beam writer can be used for the gate patterning while the other processes can remain the same. It should be noted that a set of newly designed masks are needed. Dual-channel MESFET will provide both high DC and RF performance if we can combine submicron gate length with dual-channel layers.

8.2.2 Fabrication of SiC MESFETs with double-recessed structure

Our simulation results have shown that SiC MESFETs with double-recessed structure have high DC and RF performance. To fabricate the double-recessed MESFETs, based on the present process, one addition mask is required. Figures 8.1 and 8.2 show the entire process flow for the fabrication of double-recessed devices. The added mask will be used in step (f) for the gate recess etching.

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Fig. 8.1 The process flow for SiC MESFET (part I): (a) SiC wafer with epilayers; (b) Metal mask deposition for mesa isolation using the lift-off process; (c) Mesa isolation by RIE; (d) Metal mask for channel recess etching using the lift-off process; (e) Channel recess etching by RIE.

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Fig. 8.2 The process flow for SiC MESFET (part II): (f) Metal mask for gate recess etching using the lift-off process; (g) Gate recess etching by RIE; (h) Thermal oxidation; (i) Source and drain metal deposition using self-aligned process; (j) Gate metal deposition using self-aligned process.

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8.2.3 Study of high temperature performance for SiC MESFETs

The high temperature performance of SiC MESFETs can be investigated for SiC MESFETs with different structures fabricated in this work. The model parameters can also be optimized to apply in the Medici simulator to fit the experimental results.

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Patents filed

1. Rusli and **Zhu Chunlin**, “Silicon Carbide Metal Semiconductor Field Effect Transistor with a Double - Channel Layer for High Voltage, High Power and High Frequency Applications”, *US Provisional Application No. 60/572,771*, May 2004.
2. Rusli and **Zhu Chunlin**, “Novel Structures of Silicon Carbide Metal Semiconductor Field Effect Transistors for High Voltage and High Power Application”, *PCT Application No. PCT/SG2005/000152 based on US60/572,771*, May. 2005.

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